A PWM (Pulse Width Modulated) Transconductance Amplifier

for High Current Numerical Protective Relay Testing

Kian Siong Ling

A thesis submitted to the Faculty of Graduate Studies of

The University of Manitoba

in partial fulfilment of the requirements of the degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering

University of Manitoba

Winnipeg

THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

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Abstract

Digital power system transient simulators are becoming an increasingly effective and powerful analysis tools for testing today's high-speed protective relays and evaluating performance of the power protection systems in greater detail. These digital simulators require external power conditioning amplifiers to generate the current and voltage waveforms comparable to the actual fault level in the secondary of current and voltage transformers.

In this thesis, the feasibility of constructing an efficient and portable power conditioning amplifier dedicated for relay testing was explored. Emphasis was placed on the design of the current amplifier by utilizing the power electronics technology. To ensure that the design approach is feasible, PSCAD/EMTDC simulations were conducted, and following that, a proof-of-concept hardware prototype of the amplifier was developed. It was demonstrated experimentally that a high performance current amplifier could be constructed by using the high efficiency switching technique.

Acknowledgements

First and foremost, the author wants to thank his advisor, Professor A.M. Gole, for his valuable support and guidance, and for providing opportunity of working on this thesis.

The author also expresses his utmost gratitude to his co-advisor, Professor P.G. McLaren, for believing in his ability to conducting this research work successfully.

The author wishes to thank Mr. Erwin Dirk for providing assistance in setting up laboratory equipment and offering invaluable advice during the duration of the research experiments.

Special thanks to the HVDC Research Centre Inc. for supporting financially the work of this thesis. Without their strong beliefs, this work cannot be completed.

Finally, I am grateful to my wife, Hai Lin, for supporting me and taking care of me all along.

Kian Siong Ling
Aug. 05

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Table A.1 Operators

d/dt	First order derivative

Table A.2 Parameters

A_c	Carrier signal amplitude
Al	Inductance (nH) obtained for every square number of winding turn
A_m	Modulation signal amplitude
A_{ord}	Amplitude of current order
B	Magnetic field
C_{fil}	Filtering capacitor value
C_{in}	Input capacitance of VSC
$C_{ov}, C_{ov1}.....C_{ov4}$	Overvoltage snubber capacitance
D_{high}	Upper freewheeling diode of a half bridge VSC
$D_{LH}, D_{LH1}....D_{LH4}$	Upper left freewheeling diode of a full bridge VSC
$D_{LL}, D_{LL1}....D_{LL4}$	Lower left freewheeling diode of a full bridge VSC
D_{low}	Lower freewheeling diode of a half bridge VSC
$D_{ov}, D_{ov1}.....D_{ov4}$	Overvoltage snubber diode
$D_{RH}, D_{RH1}....D_{RH4}$	Upper right freewheeling diode of a full bridge VSC
$D_{RL}, D_{RL1}....D_{RL4}$	Lower right freewheeling diode of a full bridge VSC
δ_t	Time delay
F_{BW}	Bandwidth of interest

Table A.2 Parameters

F_c	Carrier signal frequency
F_m	Modulation signal frequency
F_{ord}	Frequency of current order
F_P	Power bandwidth
F_S	Sampling frequency
H	DC magnetizing force
I_A	Peak current
I_c	Control current of Hall effect sensor
$\bar{I}_{cap}$	Average input capacitor current
I_{comp}	Compensating current
I_{DC}	DC bias current
I_{DS}	MOSFET current
I_{err}	Switching current error
I_{err2}	Output current error of a filtered VSC
I_{fil}	Filtered VSC output current
I_h	Harmonic component value
I_{load}, I_{loadA}, I_{loadB}, I_{loadC},	Load current
$\bar{I}_{load}$	Average load current
I_{max}	Maximum achievable load current
I_{noise}	Output noise level
I_{ord}, I_{ordA}, I_{ordB}, I_{ordC}	Input current order
I_{out}, I_{outA}, I_{outB}, I_{outC}	Pre-filtered VSC output current
I_{pri}	Primary current
I_{rated}	Rated current value
I_S	DC source current
I_{S-}	Negative source current
I_{S+}	Positive source current
I_{sec}	Secondary current
k	Constant value of the Hall effect element
L	Inductance value used in the magnetic core design
L_1.....L_9	Stray inductor values of VSC circuit
l_e	Effective path length (cm) of magnetic core
L_{fil}	Filtering inductor value
L_{load}	Load inductance
L_{max}	Maximum smoothing inductance

Table A.2 Parameters

L_s	DC source inductance
L_{smooth}	Smoothing Inductance
L_{SUM}	Sum of the stray inductor values
m_A	Amplitude modulation index
m_f	Frequency modulation index
N	Turn number of inductor winding
N_{pri}	Turn number of primary winding
N_{sec}	Turn number of secondary winding
PI_{err}	Error signal of PI controller
Q_{LH1}.....Q_{LH4}	Upper left MOSFET of a full bridge VSC
Q_{LL1}.....Q_{LL4}	Lower left MOSFET of a full bridge VSC
Q_{RH1}.....Q_{RH4}	Upper right MOSFET of a full bridge VSC
Q_{RL1}.....Q_{RL4}	Lower right MOSFET of a full bridge VSC
R_{fil}	Filtering resistor value
R_{load}	Load resistance
R_{ov}, R_{ov1}.....R_{ov4}	Overvoltage snubber resistance
R_{pass}	Pass element resistance
R_s	DC source resistance
R_t	Hall effect sensor terminating resistance
$S_{bipolar}$	Bipolar DC source
S_{high}	Upper switch of a half bridge VSC
S_{LH}	Upper left switch of a full bridge VSC
S_{LL}	Lower left switch of a full bridge VSC
S_{low}	Lower switch of a half bridge VSC
S_{RH}	Upper right switch of a full bridge VSC
S_{RL}	Lower right switch of a full bridge VSC
t	Time
t_{3level}	Maximum operating time of VSC using double hysteresis band control scheme
t_{CRPWM}	Maximum operating time of a CRPWM controlled VSC
t_{max}	Maximum operating time of a lossless VSC
T_{off}	Turn off time
T_{on}	Turn on time
T_S	Simulation time step
V_1	Voltage output of S_{LH} and S_{LL}
V_2	Voltage output of S_{RH} and S_{RL}

Table A.2 Parameters

V_{bus}	Capacitor bus voltage of VSC
VDC	DC Source voltage
V_{DS}	Drain-source voltage of MOSFET
V_H	Hall effect voltage
V_{load}	Load voltage
$\overline{V}_{load}$	Average load voltage
V_{ref}	Reference voltage
V_{SW}	VSC switching voltage
V_t	Hall Effect sensor output voltage
w_{hys}	Hysteresis bandwidth
Z_{load}	Load impedance

Table A.3 Abbreviations

AC	Alternate current
CRPWM	Current reference pulse width modulation
CT	Current transformer
D/A Converter	Digital to analog converter
DC	Direct current
DCCT	DC current transformer
DSMPS	Digitally-sourced model power system
DSP	Digital signal processor
DYNA-Test	Digital dynamic testing
emi	Electromagnetic interference
EMTP	Electromagnetic transient program
Eqn.	Equation
ESR	Equivalent series resistance
FACTS	Flexible AC transmission system
Fig.	Figure
GPS	Global positioning system
GS	Gate-source
GTO	Gate turn off transistor
HVDC	High voltage direct current
I/O	Input and output
IC	Integrated circuit
IGBT	Insulated gate bipolar transistor
LED	Light emitting diode
MOSFET	MOS field effect transistor

Table A.3 Abbreviations

P.U.	Per unit
PCB	Printed circuit board
PI	Proportional and integrated
PID	Proportional, integrated, and differential
PLD	Programmable logic device
PSCAD/EMTDC	Electromagnetic/power system simulation software
PWM	Pulse width modulation
RCD	Resistor, capacitor, and diode
RL	Resistor and inductor
RMS	Root mean square
RTP	Real time playback
RTPSS	Real time power system simulator and playback system
SMT	Surface mount technology
SPWM	Sinusoidal pulse width modulation
STATCOM	Static synchronous compensator
SVC	Static Var compensator
THD	Total harmonic distortion
TNA	Transient network analyzer
UPS	Uninterrupted power supply
VSC	Voltage source converter
VT	Voltage transformer

CHAPTER 1 Background Information

1.1 The Role of Real Time Power System Simulators in Protective Relay Testing Applications

Today's electric power systems are becoming increasingly complex. The contributions to this include larger locally regulated networks, increased size of power generation units, and emergence of power electronics systems such as HVDC (High voltage direct current) links, STATCOMs (Static synchronous compensators), and FACTS (Flexible AC transmission system) technologies. There is a growing trend toward using numerical protective relays to provide a faster protection and control solution for these advanced systems. To meet the ever increasing standard of service, higher performance in terms of selectivity and decision time for the protective relays are required, so that false tripping of the circuit breaker can be avoided, and reliable operation of the protection systems can be achieved.

It is therefore necessary to perform thorough and realistic tests on these relays over their operating range, as well as the protection and control schemes, by using transient voltage

and current test waveforms. The test waveforms should be as close as possible to the actual operating and fault level of the complex power systems. To faithfully reproduce these waveforms, it requires high performance real time simulators with accurate models of the power system network.

1.2 Classifications of Real Time Power System Simulators

In general, real time power system simulation systems can be classified into two major categories: analog or digital. The digital simulators can be subdivided further as either open or closed loop simulators. In the following sections, a brief overview on the characteristics and operating principles of these simulation systems are provided.

1.2.1 Analog Real Time Power System Simulators

Analog real time power system simulators were well established in the 50s [1]. These classical simulators, which include secondary injection test kit and TNA (Transient network analyzer) [2], are constructed from scaled down electrical models of the actual power system elements. By interconnecting the low power analog models, i.e. circuit breakers, transmission lines, transformers, generators, and electric machines, it is possible to form a simulated scaled model of the original high power network. Subsequently, real time voltages and currents derived from the simulated network can be extracted and applied to test the relay equipment.

Typical analog simulation systems are complex, bulky, and expensive, due to the reasons that the analog models used in these simulators occupy a very large physical space, and

are costly to make and maintain. Hence, legacy analog simulators are only used in those highly specialized power system research laboratories or relay manufacturing facilities, which have been unable to raise the resources to upgrade to modern test equipment.

Because of the cost and size constraints, only a finite number of hardware models can be installed into each analog simulator. As a result, these simulators lack the flexibility to model complex power systems with larger network size. It is also difficult to create and implement accurate models for the power system elements that are nonlinear, saturated magnetically, or involve switching operations. Examples include FACTS, HVDC converter stations, SVC (Static var compensators), line energization, load switching, power swing, and transformer inrush. The inability to produce accurately these models has limited effectiveness of the analog simulations.

To address the above problems, real time digital power system simulators were developed in the beginning of 80s [3] to provide an alternative approach to performing reliable transient testing of today's protection systems. With more than 20 years of development and the advent of high-speed microprocessors to perform sophisticated calculations, the digital simulators have become prevalent analysis tool in studying power systems and examining protection schemes.

1.2.2 Digital Power System Simulators

In digital simulation, the power systems elements are modeled mathematically using differential equations. By solving the equations numerically with high-speed computer to obtain the time incremental solution, complex transient behaviors of the power system

network can be simulated accurately. The network information can be extrapolated, monitored or modified during the ongoing simulation runs, and reconstructed in real time at the output stage of the simulation system via high-speed D/A (Digital to analog) converters.

Because of their capability to simulate today's highly complex electrical phenomena accurately as documented in [4], digital power system simulators are clearly superior when compared to their analog counterparts. Furthermore, the digital simulation systems also offer substantial advantages in terms of reduced physical size, more competitive price tag, and increased flexibility.

The cost and size are reduced because digital simulators are constructed from low power electronic components and microprocessors. In terms of flexibility, the same simulator can be reprogrammed to represent, theoretically, unlimited number of power system configurations. Moreover, without making any hardware modification, newly developed models of the power system elements can be integrated easily into the software library of the simulator. Finally, some of these simulators are also equipped with highly functional features to facilitate the testing process.

1.2.2.1 Classification of the Digital Power System Simulators

In general, if the processing speed is fast enough to complete the equation solving and generate all the data points to the output within the simulation time step, the simulation is said to be occurring in real time. If the information provided from the device under test

can be incorporated into the ongoing simulation run, simulators with such capability are referred as "real time, closed loop" type.

On the contrary, if the processing time is much longer than the time step, the computed data points have to be stored elsewhere in digital form and reproduced later at the device under test via a playback apparatus. The testing has to be performed in open loop because there is no real time interaction between the computer simulation and the responses of the device. Hence, such simulators are either called playback or open loop digital simulators.

The simulation time step is perhaps one of the most critical parameters in a simulation system design and needs to be carefully defined. However, there is not yet a fail-safe procedure to select the time step value. As a result, without sacrificing complexity and integrity of the simulated network, it should be selected to ensure that optimum accuracy and highest signal bandwidth of the simulation results can be produced [5].

1.2.2.2 Open Loop (Playback) Digital Power System Simulator

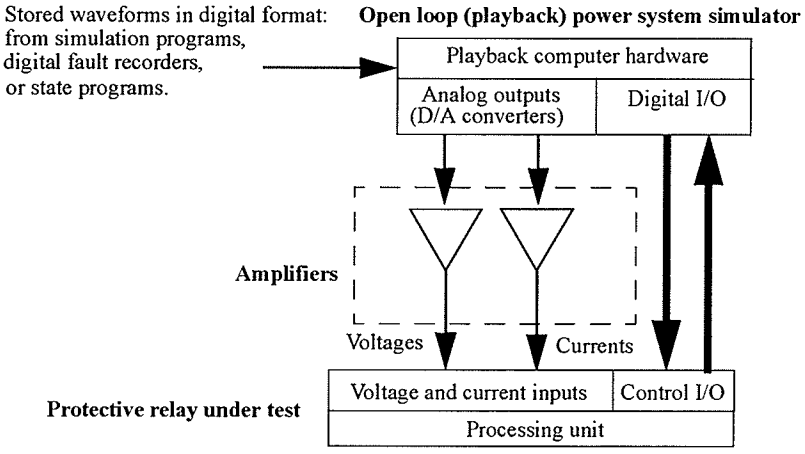


Fig. 1. 1 Typical open loop (playback) power system simulator setup diagram.

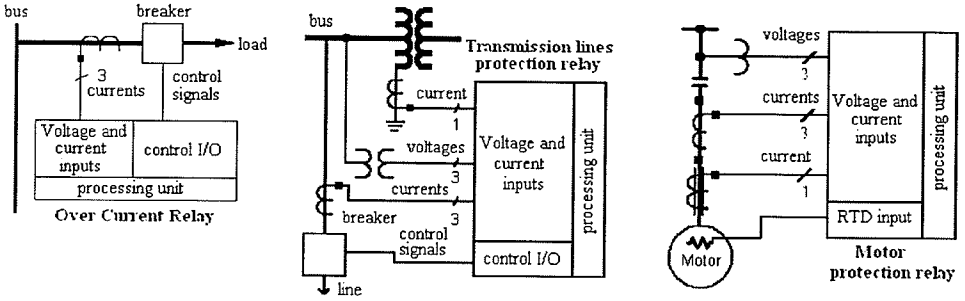
Simplified test setup of an open loop (playback) digital power system simulator is shown in Fig. 1.1. Examples of playback simulator include DYNA-Test [6] (Digital dynamic testing), DSMPS (Digitally-sourced model power system) [7] from General Electric, and RTP (Real time playback) system [8].

In general, test waveforms of the open loop simulators are generated off-line, either produced by using electromagnetic transient simulation programs such as EMTP (Electromagnetic transient program) [9] or PSCAD/EMTDC (Electromagnetic transient simulator including DC system) [10], recorded from digital fault recorders at substation, or artificially synthesized from user defined mathematical functions. These transient waveforms are stored in digital forms and can be reproduced later at the secondary side of CT (Current transformer) and VT (Voltage transformer) to the relay under test, via the D/A converters and power conditioning amplifiers. The D/A converters convert the digital data into low level analog signals, while the amplifiers scale up these signals to voltages and currents corresponding to the actual input level of the protective relay.

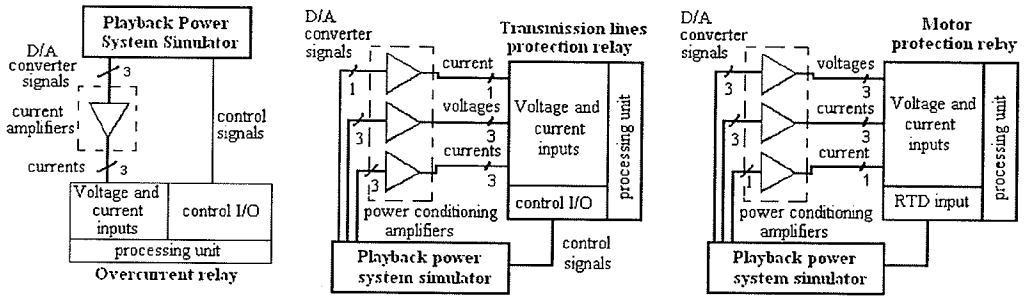
Most playback simulators are also equipped with digital I/O (Input and output) interface. The digital outputs would supply the status information of breakers and switches obtained from the simulation to the relay under test, and the digital inputs would accept information (trip or close signal to the breakers) generated by the relay.

Fig. 1.2 illustrates application examples of the playback simulator for the testing of overcurrent, transmission line, and motor protection relays. As shown in the figure, it is

possible to examine performance of various relays by using the digital simulator in conjunction with the power conditioner amplifiers.



a. Actual power system network.



b. Testing of the relays using the simulated power system network.

Fig. 1. 2 Various relay testing configurations using the playback simulator.

Finally, as documented in the literature, a large number of relay tests have been performed to demonstrate effectiveness of the open loop digital simulator. These include successful testing of distance relay characteristics using a WAPA based simulator [11], testing of transformer differential relay [12], and investigation of the waveform distortion effects on the operation of directional distance relay [13].

1.2.2.3 Advantages of the Open Loop Digital Power System Simulator

Compared to the closed-loop simulators, the open loop simulation systems demand less computational power because the simulation is conducted offline at a much slower

processing speed. Hence, these simulators are typically lighter, cheaper, and portable. Such compact design has made them favorable for field-testing.

Furthermore, some of the open loop simulators are also equipped with GPS (Global positioning system) clock receiver to perform end-to-end tests [14]. These simulators can apply pre-recorded disturbance waveforms simultaneously to the relays located at remote terminals of the transmission lines. Consequently, protection scheme of the power system that incorporates communication links, such as the pilot line assisted directional and distance schemes, can be examined in a more comprehensive fashion.

1.2.2.4 The Need for Closed Loop Power System Simulators

Open loop simulators offer a "poor man's" solution to the closed loop simulators because of their lower price tag and abilities to perform a wide range of relay testing applications. Nonetheless, there are certain tests that such simulators cannot perform effectively [15].

For instance, closed loop testing should be performed whenever timing of a relay tripping action due to the fault detection will influence the relay's responses to subsequent changes in the power system. To illustrate this, consider transmission line relay testing in applications with fast reclosing. During a fault, if the reclosure happens well before both the relay and power system settle to a new steady state condition, the relay will need to contend with a dynamic power system and possibly dynamics within itself. Hence, it is difficult to produce accurate results when the tests for tripping action and reclosure have to be conducted separately in a typical open loop fashion, which assumes that both actions are independent of each other.

In addition, because of the memory size constraint, open loop simulators are limited by playback time. They are not suitable for applications that require extended running time, such as tests for out-of step protection which last for several seconds and tests on the arcing phenomenon caused by high impedance fault which call for several minutes of simulation time.

Finally, closed loop simulators are also preferred whenever constant modification of the system parameters during a simulation run is required, and when there is a large number of test cases need to be investigated. During these scenarios, there will be constant back and forth actions between verification of the simulation results, checking of the responses from the relay, adjustment of the power system parameters, and changing of the test cases. By using a closed loop simulator, significant execution time can be saved from conducting these tests because the parameters can be adjusted on the run, the simulation results can be obtained instantly, and the batch-mode testing [16] feature can be used to automatically examine large array of test cases.

1.2.2.5 Closed Loop (Real Time) Digital Power System Simulators

Currently, there are only a handful of closed loop simulators reported in the literature. Examples of these simulators include RTDS (Real time digital simulator) [17] and ARENA^{TM} [18]. Distributed computing architectures, constructed by connecting multiple high-speed processors in parallel, are commonly used in these simulation systems to achieve the goal of real time computing.

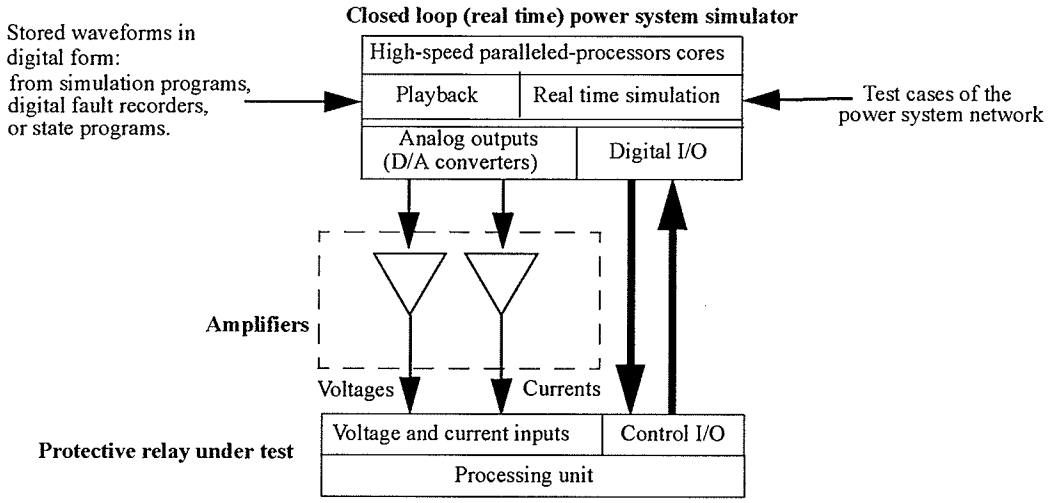


Fig. 1. 3 Typical close loop (real time) simulator test setup.

Simple setup of a closed loop test is illustrated in Fig. 1.3. Similar to the open loop simulators, transient current and voltage waveforms generated from the closed loop simulators can be applied to the protective relay via the D/A converters and power conditioning amplifiers. Closed loop simulators are also equipped with I/O interface to exchange information with the relay under test. However, there is a major difference between these two simulation systems: not only can the closed loop simulators playback recorded digital copy of the test waveforms, they can also perform the power system simulations in real time by uploading the test cases to their high-speed processing cores. The computation speed is so fast that it is possible to incorporate responses generated from the relay into the ongoing simulation run through the I/O interface.

A number of application examples for the closed loop power system simulator have been documented in the literature, such as testing of distance protection system in a series compensated network using the ARENE^{TM} simulator [19], protective relay testing for

high impedance faults in transmission line using RTDS [20], and testing of 500kV line relays to evaluate the effect of a series compensation upgrade [21]. As demonstrated in these examples, by virtue of their interaction with the devices under test, the closed loop digital power system simulators offer an ultimate solution to effectively study the performance of protective relays and the power protection systems.

1.3 The Need for Relay Testing Power Conditioning Amplifiers

No matter how effective the digital power system simulators are, they all have a common shortfall: low power output signals in the typical range of +/10V, whereas most inputs of the protective relays require up to hundreds of volts and amperes as test voltages and currents, respectively. For these digital simulators to operate as a protective relay test platform, they rely upon external power conditioning amplifiers to faithfully convert the low voltage signals to the actual CT and VT output levels.

Conventionally, analog amplifiers are used for this purpose. Typical examples include Techron's current and voltage mode amplifiers [22] and Crown's power amplifiers [23]. In general, these amplifiers are designed based on the class AB configuration. By connecting multiple units of power MOSFETs or transistors in parallel or series for power sharing, a high power rating can be achieved at the output stage of these amplifiers.

Although low noise, linear, and high frequency responses can be produced in the output waveforms, analog designs often suffer from the problems of low power efficiency. A typical class AB amplifier loses at least one fourth of its power at peak amplitude. Due to

the reason that the load impedance and compliance voltage are unknown values, the efficiency of a current amplifier is even lower. Consequently, output power rating of an analog amplifier is limited by the losses, and a significant amount of weight and size of the amplifier has to be utilized to dissipate the heat generated by these losses.

To illustrate the above arguments, consider that a 20A, 100V single-phase Techron 7570 current mode amplifier weights around 92 lb. in a 5U package (19" width x 8.75" height x 16.5" depth). For a typical 3-phase current testing, three such amplifiers are required, which weight more than 270 lb. in total and occupy plenty of space in a standard rack cabinet (70" height). Clearly, it will diminish the portable and lightweight advantages of the digital simulators by using these bulky amplifiers for relay testing applications.

Finally, because of their specialized and limited applications, true relay testing amplifiers are only available from a handful of vendors. These amplifiers, such as the OMICRON CM-line secondary injection amplifiers [24] and Doble F6000 series power system simulator amplifiers [25], are often built into the relay test set manufactured by the vendors and cannot be used in conjunction with other simulation systems. Hence, to address these problems, it is necessary to explore other means of amplifier design.

1.4 Overview of the Thesis Project

The purpose of this thesis is to develop a current (or transconductance) amplifier to serve as the output stage of a real time digital power system simulator used for high-speed relay testing. There are three major goals for the amplifier design: a precise and low noise

output comparable to the operating current level at the secondary of the CT, minimum phase shift in the output to allow for real time testing, and portable package size to provide the convenience of field testing.

To satisfy these conditions, the design of a PWM (Pulse width modulation) switching converter compensated with an analog current source was proposed in this thesis. PSCAD/ EMTDC modeling and simulations were conducted to explore the feasibility of such design measures. Subsequently, a proof-of-concept hardware prototype of the single-phase current amplifier based on the simulation findings was constructed in the laboratory.

The thesis structure is divided into 6 chapters:

Chapter 2 discusses and defines the required specifications of the current amplifier used for the sole purpose of numerical relay testing applications.

Chapter 3 presents a brief introduction for the power electronics principles and discusses various types of voltage source converter topology and switching techniques that will be examined in this project

Chapter 4 demonstrates the use of PSCAD/EMTDC as an effective tool in power electronics design. Simulations performed during this thesis are discussed and analyzed in this chapter.

Chapter 5 discusses various issues and problems encountered on the hardware design. The hardware experiment results conducted using the existing current amplifier prototype will also be presented and discussed.

and finally, **Chapter 6** will provide conclusion and future recommendation for this thesis.

CHAPTER 2 Specifications of the Relay Testing Current Amplifier

2.1 Introduction

In this thesis, the current amplifier will only be applicable for testing static (numerical and solid-state) relays, where burden impedance of the relay's current input is closed to zero ohm. The amplifier will not be used for testing electromechanical relays, which have a much slower response than static relays, but require a higher compliance voltage and VA rating to energize the induction or solenoid coil [26]. Different design criteria are required to address these particular needs, and hence they are not included in the scope of this thesis.

Due to its availability in the laboratory, the RTP (Real time playback) system, driven by the PSCAD/EMTDC offline simulator, was used as the input platform of the current amplifier in this project. The specifications of the current amplifier were based on the RTP's output characteristics, as well as the recommended specifications of the power conditioning amplifiers provided in Appendix A.

2.2 Outline and Discussion of Specifications

Table 2.1: Specifications of Current Amplifier

No.	Descriptions	Values
1	Input source	Low power voltage output from digital simulators, signal generator, or any playback instrument
2	Maximum input signal level	+/-10V
3	Conversion factor	From 1V/10A to 1V/14.142A
4	Output target	Current input of static protective relay with $5A_{rms}$ nominal rating
5	Output frequency	Small signal: DC to 20kHz at $5A_{rms}$. Power bandwidth: DC to 480Hz at $100A_{rms}$.
6	Maximum compliance voltage	+/-15V
7	Maximum group delay	50μs
8	Maximum phase delay	1μs
9	Peak current	$100A_{rms}$ for at least one second
10	Nominal output	$15A_{rms}$
11	Gain accuracy	0.2% of value at 50/60Hz
12	Noise factor	less than -66dB below rated output value (from DC to 20kHz)
13	Harmonic distortion	Maximum 1% for THD and higher order harmonics at 50/60Hz full scale output current
14	Maximum slew rate	0.425A/μs
15	Others	To be packaged in a 3U industrial rack enclosure

The proposed specifications of the current amplifier used for relay testing applications are listed in Table 2.1. Detailed discussion of these design goals are given as follows.

- The current amplifier will receive single-phase input signal in the range of +/-10V from a digital simulator, waveform recorder, or any other playback instrument. It will convert the input voltage signal to the appropriate output current level with a manually adjustable transconductance, for instance, 1V/10A or $1V/10A_{rms}$. The output current will be injected into the current input of the protective relay with a nominal rating of $5A_{rms}$.

• According to the Nyquist sampling theory, to properly construct a signal without any aliasing effects, the sampling frequency (F_S) has to be at least twice the bandwidth of interest (F_{BW}), as depicted in Eqn. 2.1.

$$F_{BW} = \frac{F_s}{2} \quad \text{(EQ 2.1)}$$

Currently, the time step of the RTP system is around 25 μs, which corresponds to F_{BW} of 20kHz. The bandwidth of 20kHz is more than sufficient to reconstruct the highest frequency of interest in power system simulation, which is typically in the range of 5kHz. To produce accurately the waveforms reconstructed by the RTP system, the frequency response of DC to 20kHz was specified for the current amplifier.

• The types of protective relay targeted are static relays, which have very low burden impedance. The impedance has a typical range of 0.14VA to 0.3VA for the $5A_{rms}$ nominal relay input. The major sources of impedance are from the terminals and test leads connecting the amplifier and the relay under test. Hence, in order to achieve a highly efficient performance, the power and compliance voltage losses resulting from the output connections should be kept as low as possible.

Clearly, the smaller the load impedance value, the lower is the compliance voltage requirement. Hence, an output rating of +/-15V was specified for the amplifier, which is sufficient for injecting the rated current of $100A_{rms}$ into a typical burden.

- The phase shift of the amplifier output waveforms should be kept at a minimum level in order to prevent any error during the real time testing. Maximum group delay of 50μs and phase delay of 1μs were recommended.

- The continuous rating of a protective relay's current input is usually 3 p.u. (per unit) of the nominal value at $5A_{rms}$. The one-second thermal rating of the current input could be as high as 100 p.u. of the nominal value. Thus, ideally, the current amplifier is required to produce a wide range of test currents, from as low as $15A_{rms}$ continuously to as high as $500A_{rms}$ momentary, in order to study the full behavior of the protective relay.

Practically, it is difficult to generate transient current of $500A_{rms}$, and occurrence of fault current at such a magnitude for very long duration is uncommon. In addition, most CTs are rated only at 20 p.u. of the nominal value. Hence, relay tests are normally conducted at a much lower current rating, typically at 10 p.u. of the nominal value.

In this thesis, the current amplifier was specified to deliver one-second rating of $100A_{rms}$ for a load impedance of less than 0.015Ω. At the maximum compliance rating of 15V, the amplifier was required to deliver the rated current of $100A_{rms}$ for at least ten cycles. Finally, the continuous rating of the amplifier was specified at $15A_{rms}$.

- There are two types of frequency bandwidth specified for the current amplifier: small signal and power bandwidths. In this thesis, the "small signal bandwidth" of DC to 20kHz was specified at the nominal $5A_{rms}$ rating. On the other hand, the current amplifier was specified to have a "power bandwidth" of DC to 480Hz at the rated current of $100A_{rms}$.

• Based on the power bandwidth rating, it is possible to calculate the maximum slew rate of the amplifier in accordance to Eqn. 2.2.

$$SlewRate = 2\pi \times F_p \times I_A \quad \text{(EQ 2.2)}$$

where I_A is the peak current and F_p is the power bandwidth. The slew rate was found to be 0.425A/μs from the above equation.

• To prevent unintentional pickup of the relay due to poor quality or contaminated waveforms generated by the amplifier, the noise, distortion, and error produced by the amplifier should be kept as small as possible. Recommended values of less than 1% THD (Total harmonic distortion) for any one component over the frequency of 60kHz, noise factor of less than -66dB from DC to 20kHz with respect to the rated current, and gain error of 0.2% at 50/60Hz were specified in this project.

Mathematical representations of the above specifications are defined as follows:

$$THD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_1} 100 \ \% \quad \text{(EQ 2.3)}$$

$$NoiseFactor = 20\log\left(\frac{I_{noise}}{I_{rated}}\right) \quad \text{(EQ 2.4)}$$

$$GainError = \frac{|I_{ord} - I_{load}|}{I_{ord}} 100 \ \% \quad \text{(EQ 2.5)}$$

where I_{ord} and I_{load} are the input reference and load current value, respectively, I_h is the harmonic component value of I_{load}, and I_{noise} is the switching noise level measured at the rated current (I_{rated}) of $100A_{rms}$.

- The amplifier must have a stable performance within its operating range and insensitive to fluctuations in the load value and supply voltage.

- Finally, the developed amplifier should have sufficient portability for ease of field-testing.

In the following chapter, a brief introduction on the power electronics technology will be provided. Principles and advantages of switching techniques used to operate the power electronics based converter will be explored and discussed.

CHAPTER 3 Introduction of Power Electronics Technology and Switching Techniques

3.1 Brief Overview of Power Electronics Technology

The history of power electronics technology can be traced as far back as 1900, when the first mercury arc valve rectifier was invented [27]. Having gone through several evolution phases and breakthrough developments, such as the introduction of thyristor in 1958 and the advent of high power and fast switching solid-state devices in the 80s, today, the technology of power electronics has been well developed. The market of power electronics based devices has expanded significantly, and its applications can be found everywhere, for example:

- Power supplies, DC converters, battery chargers, and audio amplifiers in low power consumer electronics
- UPS (Uninterrupted power supplies), arc furnaces, AC inverters, and machine drives in medium power manufacturing and industry sectors, and
- HVDC converters and FACTS (Flexible AC transmission systems) apparatus in very high power applications.

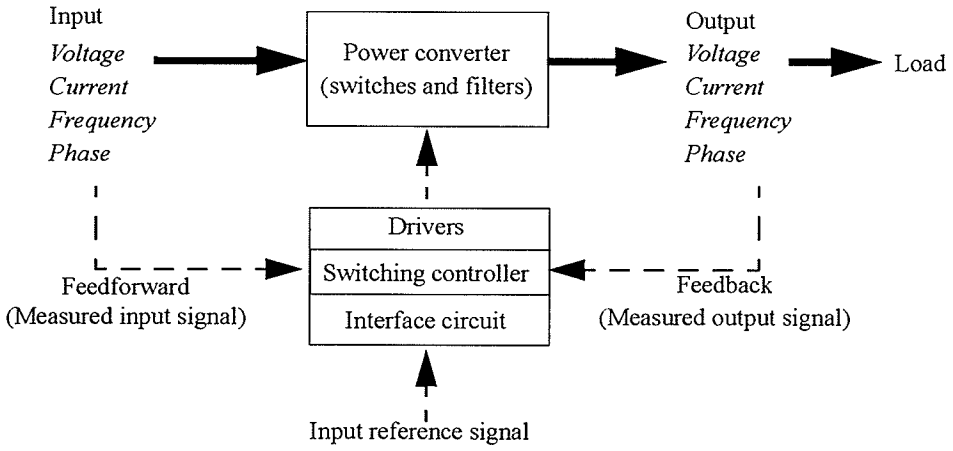


Fig. 3. 1 A generic structure of power electronics system.

The primary goal of the power electronics technology is to manipulate electrical energy by supplying voltages and currents in a form that is optimally suited for user loads. As shown in Fig. 3.1, this is achieved with a power converter system. By controlling the conduction state of the converter switches using a switching controller, the converter outputs (voltage, current, frequency, and phase) can be processed according to the conditions as requested by the input reference signal. The switching controller operates by deriving the optimal switching sequence and applying the firing pulses to the converter switches, in an attempt to minimize the error between the reference and the feedback signals.

3.2 Analog versus Switching Approach

In a traditional analog approach, in order to deliver power to an external load from a DC voltage source, a controlled pass element has to be introduced between the source and the load. As shown in Fig. 3.2, the pass element (R_{pass}) can be either passive, such as a variable resistor, or active, such as a transistor, operational amplifier, or MOSFET. By

controlling resistance of the pass element linearly, it is possible to vary the voltage drop across the element and, subsequently, the load voltage V_{load} and current I_{load}.

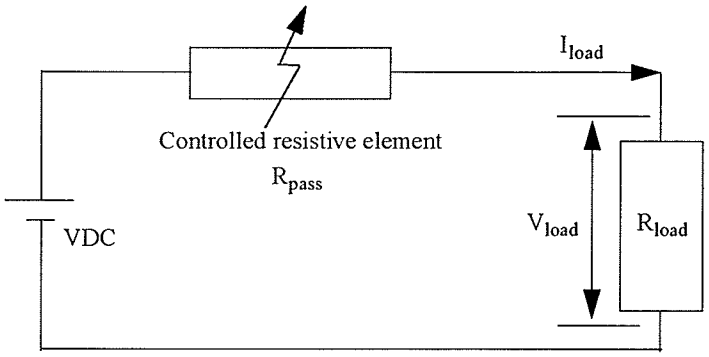


Fig. 3. 2 A simplified analog current or voltage control method.

Although a linear and low noise output can be produced with the analog approach, problems start to occur when an order for mid-range output level is issued. In this case, the resistance of the pass element has to be the same as the load value (R_{load}), and the power efficiency was found to be only 50% using Eqn. 3.1:

$$Efficiency = \frac{OutputPower}{InputPower} = \frac{\left(\frac{VDC}{2}\right)^2 \times \frac{1}{R_{load}}}{VDC^2 \times \frac{1}{2R_{load}}} \qquad \text{(EQ 3.1)}$$

The biggest problem arises when R_{load} is reduced to almost zero ohm (short circuit), and a very high current is injected into the load, similar to the applications of testing numerical relays utilizing current amplifier. The pass element has to withstand almost the entire voltage drop from the DC source, while experiencing a large current. Thus, the efficiency is reduced even further, and a massive heat sink employing cooling fans or even liquid cooling system is required to dissipate the excessive heat generated by the power loss.

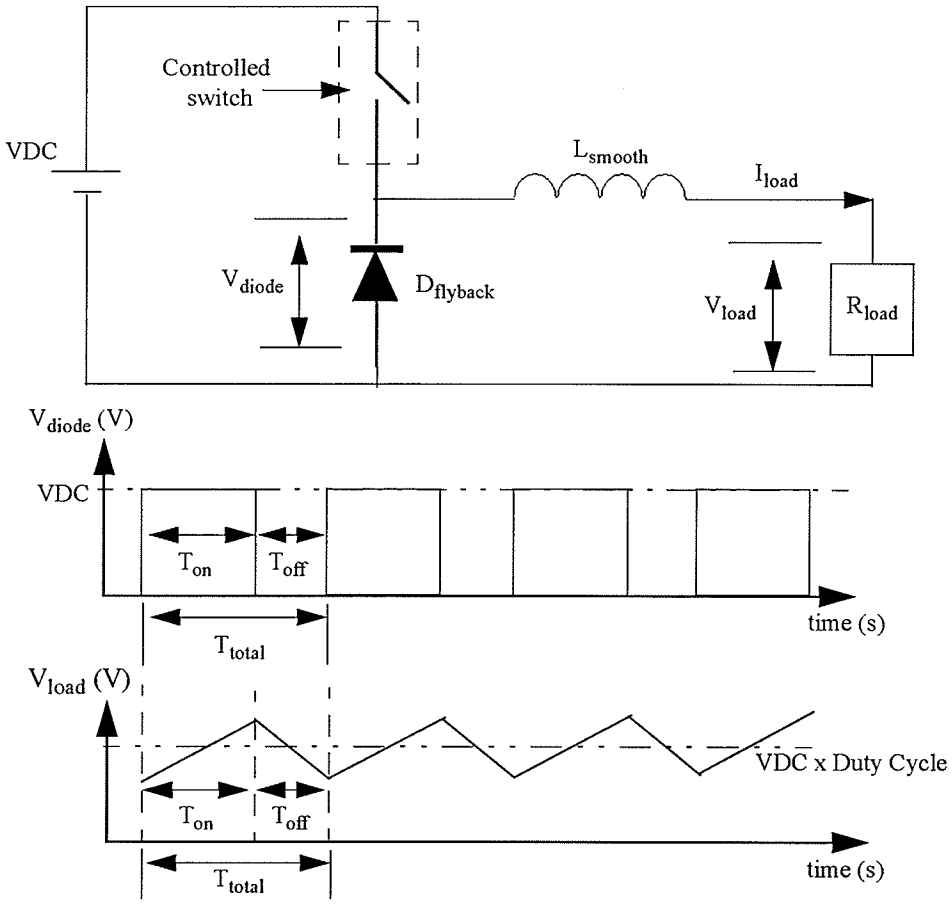


Fig. 3. 3 Simplified DC step down converter and its waveforms.

In contrast, most of the efficiency problems can be alleviated by using the switching approach. As shown in Fig. 3.3, the pass element in this case is controlled to operate in the active region, i.e., it will behave like a switch. By adjusting the conduction time of the switching element within a given frequency, it is possible to control the converter output voltage from 0V to VDC. Assuming that the switching element is ideal with zero turn-on resistance and infinite turn-off resistance, the average load voltage $\overline{V}_{load}$ is given as:

$$\overline{V_{load}} = VDC \times DutyCycle = VDC \times \frac{T_{on}}{T_{on} + T_{off}} \qquad \text{(EQ 3.2)}$$

where T_{on} is the conduction time, and T_{off} is the turn-off time of the switch.

The purpose of the inductor (L_{smooth}) is to filter the rectangular voltage (V_{diode}) produced by the switching actions, thereby providing a smoother waveform across the load. Since the inductor current (I_{load}) cannot be interrupted instantly, a flyback diode is also needed to freewheel the current whenever the controlled switch is turned off.

If the electrical components used in the switching converter are all ideal, the switching operation will be lossless. In reality, there are always static conduction and leakage losses incurred in the switching elements when they are in the on and off state, respectively. More importantly, these switching elements also suffer from dynamic losses when they are changed from the on state to the off state and vice versa. In addition, the filtering inductor does experience core loss and copper loss, and practical voltage source also contributes additional losses resulting from its internal source resistance.

However, compared to the conventional analog approach, the power losses of the switching converter are still considerably lower. These losses are not inherent as in the case of the linear design, and they can be minimized by using high quality components with much better static performance, high efficient passive filter, soft switching schemes, and snubber circuits. As a result, the switching converter can be made very efficient, to a point where the heat sinks and fans can be reduced in size or even eliminated, thus cutting down the physical size and weight of the converter.

3.3 Operation of the VSCs (Voltage Source Converters)

The step down switching converter introduced in the previous section can only deliver DC output. To produce both AC and DC waveforms for the purpose of current amplification, it is necessary to consider other converter topologies. Due to its simplicity, versatility, and ease of control, VSC (Voltage source converter) is the one of the best suited topologies to perform this specific task. In general, VSC has two configurations, half bridge and full bridge. The operating principles of these converters are provided as follows.

3.3.1 Half Bridge VSC

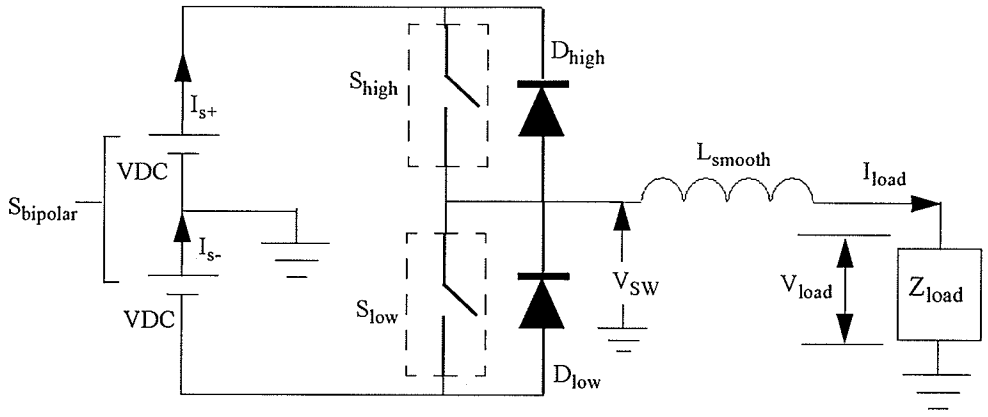


Fig. 3. 4 Simplified circuit diagram of half bridge VSC.

Simplified circuit diagram of a half bridge VSC is illustrated in Fig. 3.4. The half bridge topology is most commonly used in the multiphase inverting applications, such as AC machine drives, static Var compensators, 3-phase AC inverters, and HVDC links.

As shown in the figure, two power switches (S_{high} and S_{low}) and a bipolar DC source ($S_{bipolar}$) are needed in a single-phase setup. The switches can be any solid state devices: transistor, thyristor, MOSFET, GTO (Gate turn-off thyristor), or IGBT (Insulated gate

bipolar transistor). The outputs of the switches are connected to an inductor (L_{smooth}), which is used to limit the load current slew rate and filter the switching waveform. Freewheeling diodes (D_{high} and D_{low}) are also required to provide a conduction path for the inductor current (I_{load}) when the current-carrying switches are turned off. Since the switches are controlled to operate in the active region, the need for biasing is eliminated, and the VSC can be coupled directly to an external load (Z_{load}).

Through the selection of S_{high} and S_{low}, the smoothing inductor can be subjected to either a positive or a negative switching voltage (V_{SW}). As a result, I_{load} will flow at either an increasing or a decreasing rate according to Eqn. 3.3 and 3.4.

$$\frac{d}{dt}I_{load} = \left(\frac{V_{SW} - V_{load}}{L_{smooth}}\right) \quad \text{(EQ 3.3)}$$

$$V_{load} = \left(I_{load}R_{load} + L_{load}\frac{dI_{load}}{dt}\right) \quad \text{(EQ 3.4)}$$

where VDC is the source voltage, V_{SW} equals to +VDC when S_{high} is activated and -VDC when S_{low} is turned on, and R_{load} and L_{load} are the load resistance and inductance, respectively (assuming that the VSC is connected to a RL load).

As shown in Fig. 3.5, by controlling the conduction states of S_{high} and S_{low}, it is possible to produce V_{load} or I_{load} according to the input reference. Notice that as soon as a switch is turned off, there is a time delay (δ_t) introduced before turning on of the subsequent switch. Such time delay is required to prevent simultaneous turning on of both VSC switches and short circuiting of the DC source ("shoot through") during the switching transitions.

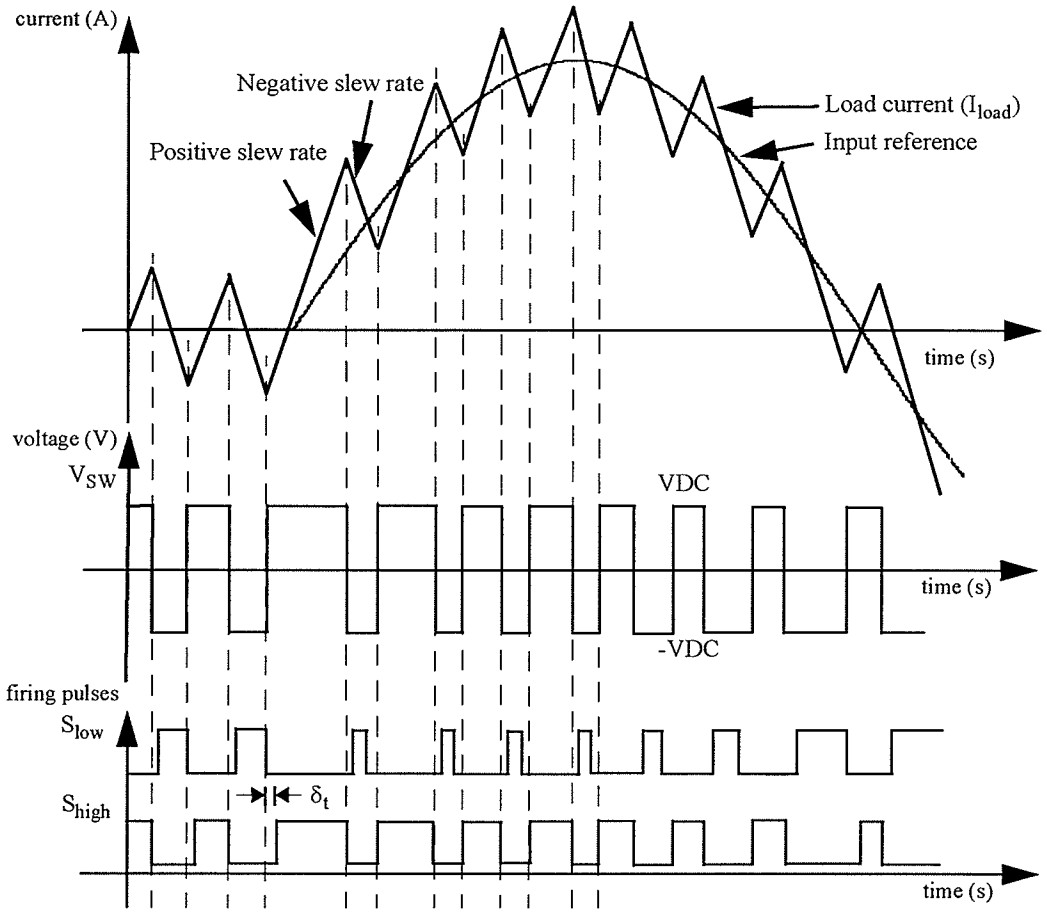


Fig. 3. 5 Typical output waveforms of half bridge VSC.

3.3.2 Full Bridge VSC

Simplified circuit diagram of a single-phase full bridge VSC is presented in Fig. 3.6. The full bridge topology is widely used in the applications of UPS, single-phase inverter, and class D audio amplifier. As shown in the figure, the full bridge circuit is similar to that of half bridge converter, except for the addition of two power switches and substitution of the bipolar DC source with a single output supply.

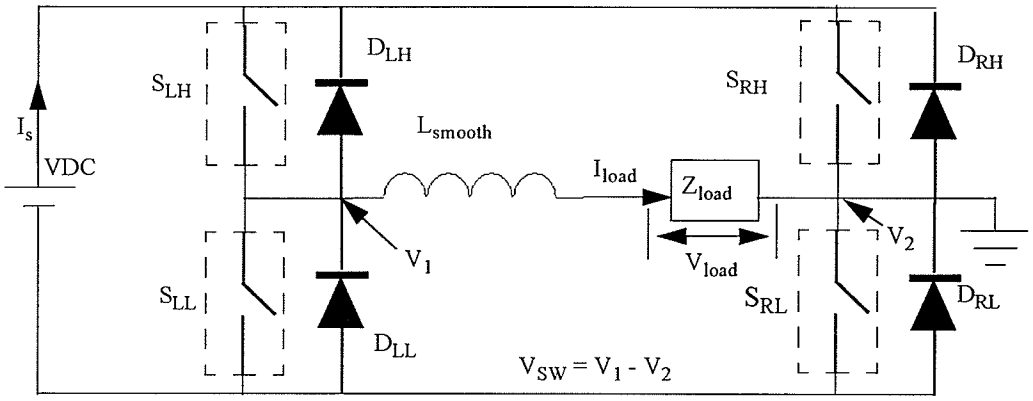


Fig. 3. 6 Simplified circuit diagram of full bridge VSC.

As in the case of the half bridge VSC, by changing the polarity of switching voltage (V_{SW}) across the smoothing inductor (L_{smooth}) and external load (Z_{load}) with positive or negative polarity, the load current (I_{load}) can be controlled at either an increasing or a decreasing rate according to Eqn. 3.3. In this case, V_{SW} is positive when S_{LH} and S_{RL} are both turned on, and negative when S_{RH} and S_{LL} are turned on.

Furthermore, the full bridge topology also allows for an additional switching state: zero. During the zero state, V_1 and V_2 share the same potential, and the voltage level of V_{SW} is zero. This happens whenever either the high side (S_{LH} and S_{RH}) or low side (S_{LL} and S_{RL}) switches are turned on. As a result, the load current will circulate within the loop through the switches and the inductor and decay exponentially according to Eqn 3.3.

$$\frac{d}{dt} I_{load} = \frac{-V_{load}}{L_{smooth}} \qquad \text{(EQ 3.5)}$$

Various switching combinations of the full bridge VSC are listed in Table 3.1. Notice that time delay for a short duration is also required to prevent the "shoot through" effect.

Finally, the commutation of the freewheeling diodes is dependent on the direction of I_{load}: (A) positive I_{load} and (B) negative I_{load}.

Table 3.1: Switching sequences of full bridge VSC.

Voltage Level		Conduction states of the switches				
Before	After	Before	Turning off	Commutation of diodes		After
Positive	Negative	S_{LH}, S_{RL} on	S_{LH}, S_{RL} off	A: D_{RH}, D_{LL} on	B: D_{LH}, D_{RL} on	S_{RH}, S_{LL} on
Negative	Positive	S_{RH}, S_{LL} on	S_{RH}, S_{LL} off	A: D_{LH}, D_{RL} on	B: D_{RH}, D_{LL} on	S_{LH}, S_{RL} on
Positive	Zero	S_{LH}, S_{RL} on	S_{LH} off, S_{RL} on	A: S_{RL} on, D_{LL} on	B: S_{RL} on, D_{LH} on	S_{LL}, S_{RL} on
Negative	Zero	S_{RH}, S_{LL} on	S_{RH} off, S_{LL} on	A: S_{LL} on, D_{RL} on	B: S_{LL} on, D_{RH} on	S_{LL}, S_{RL} on
Zero	Positive	S_{LL}, S_{RL} on	S_{LL} off, S_{RL} on	A: S_{RL} on, D_{LH} on	B: S_{RL} on, D_{LL} on	S_{LH}, S_{RL} on
Zero	Negative	S_{LL}, S_{RL} on	S_{LL} on, S_{RL} off	A: S_{LL} on, D_{RH} on	B: S_{LL} on, D_{RL} on	S_{RH}, S_{LL} on

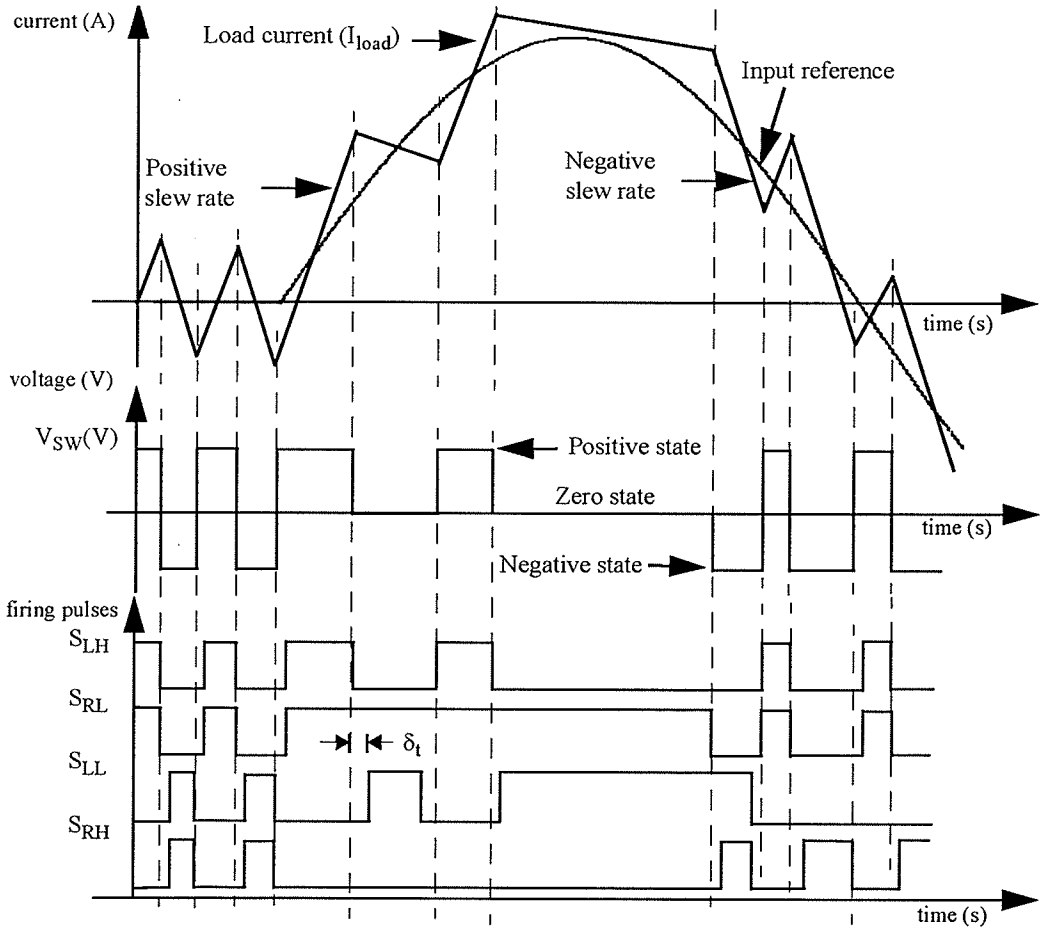


Fig. 3. 7 Typical output waveforms of full bridge VSC.

Finally, typical output waveforms of the full bridge VSC are presented in Fig. 3.7. It is clearly shown that the switching operations of both full bridge and half bridge VSC are similar, except for the introduction of zero switching state, in which the load current has a much lower slew rate.

3.3.3 Grounding Issue in the Full Bridge VSC Circuit

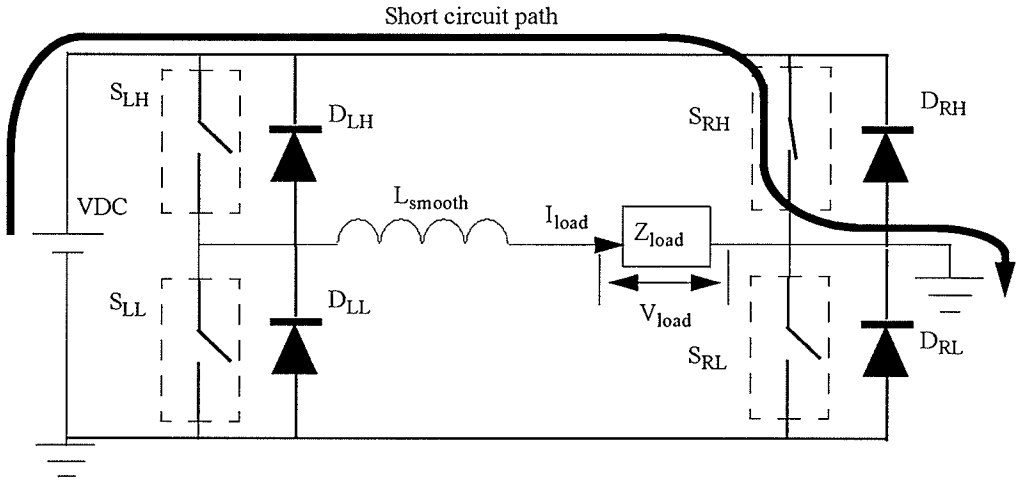


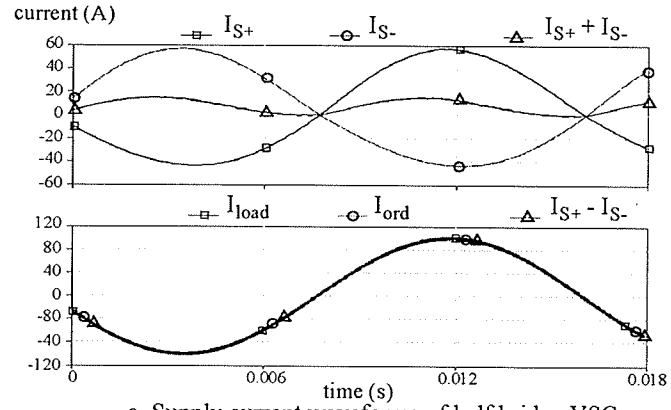
Fig. 3. 8 Short circuit of full bridge VSC due to grounding of DC source.

Unlike the half bridge VSC, a ground reference must not be connected simultaneously to both the negative terminal of the DC source and return path of the external load in a full bridge circuit. As shown in Fig. 3.8, short circuiting of the DC source will occur as soon as S_{RH} is turned on and the above two nodes are tied together. As a result, if it is required to ground the external load, the DC source must be electrically isolated.

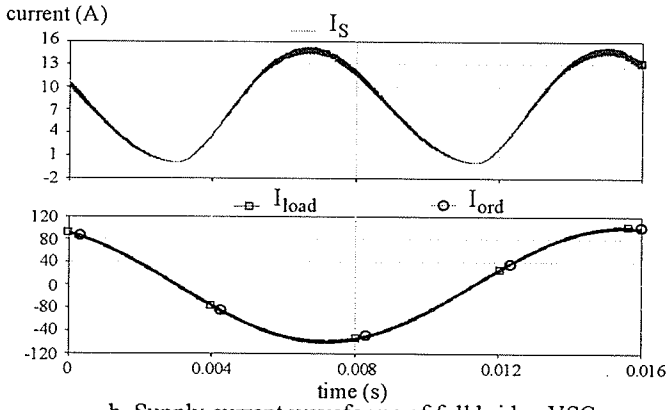
3.3.4 Source Current Waveforms of the Half bridge and Full Bridge VSC

Typical source current waveforms (I_{s+} and I_{s-}) of a half bridge VSC to generate load current (I_{load}) of 100A, 60Hz to a 0.02Ω load are presented in Fig. 3.9a. As shown in the

figure, the source currents with magnitude as high as 60A would flow from the positive supply rail to charge the negative rail and vice versa. The differential current (I_{S+}-I_{S-}) was the reflection of I_{load}, and only a low level of source current in the range of (I_{S+}+I_{S-}) was consumed in the load.



a. Supply current waveforms of half bridge VSC.



b. Supply current waveforms of full bridge VSC.

Fig. 3. 9 Simulated source current waveforms of full bridge and half bridge VSCs.

In contrast, by using a full bridge VSC, the simulation results of producing the same output current are presented in Fig. 3.9b. It is clearly shown that the source current (I_S) flows only in the positive direction and has a much lower value. Hence, the power supply can be utilized more effectively by using the full bridge configuration.

Because of a much lower supply rating, coupled with the advantages and flexibility of implementing a three-level control scheme, the full bridge VSC was chosen in this thesis as the fundamental building block of the current amplifier design.

3.4 Overview of PWM Switching Schemes for the Full Bridge VSC

One of the many benefits of using the VSC is that a large number of PWM (Pulse width modulation) switching control schemes are available [28]. With minimum modification in hardware component and a suitable mean to execute the switching algorithm, such as DSPs (Digital signal processors), microcontrollers, dedicated PWM control ICs (Integrated circuits), or even as simple as combination of logic gates, these control schemes can be implemented with ease. Using the same converter hardware, the pros and cons of each switching technique can be investigated. Subsequently, the optimum switching solution can be adopted for the desired application. The following discussion provides a brief overview on some of these switching techniques.

3.4.1 CRPWM (Current Reference Pulse Width Modulation) Switching Scheme

CRPWM is one of the most robust control schemes used in the VSC switching operation. It offers advantages of high simplicity in terms of operating principle and controller design. By implementing the control technique, it is possible to generate highly accurate output waveforms with instantaneous transient responses. Additionally, the CRPWM controller is capable of providing a stable switching performance because it is insensitive to external disturbances, such as sudden change in load value, supply line fluctuation, and noise interference.

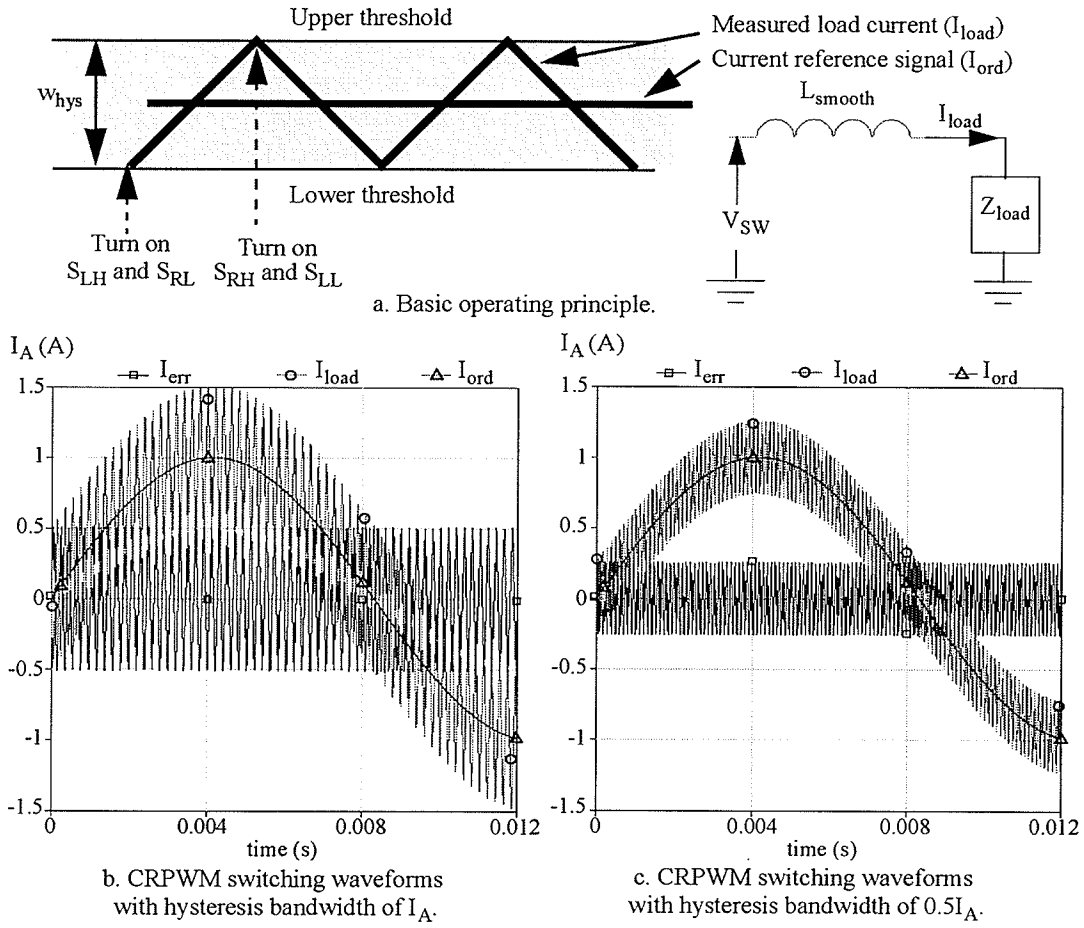


Fig. 3. 10 Operating diagram and sample waveforms of CRPWM switching scheme.

The control principle of the CRPWM technique is illustrated in Fig. 3.10a. A hysteresis band of a given width (w_{hys}) is first defined and imposed upon an input reference signal (I_{ord}). The reference signal is then compared with the measured load current (I_{load}) of the VSC. If I_{load} drops below the lower threshold of the hysteresis band, S_{LH} and S_{RL} of the converter will be turned on. As a result, a positive V_{SW} will be applied across the smoothing inductor (L_{smooth}) and load (Z_{load}), forcing I_{load} to rise above the threshold.

Conversely, if I_{load} exceeds the upper threshold, S_{RH} and S_{LL} will be turned on, and a negative V_{SW} will force I_{load} to fall toward the lower threshold.

Fig. 3.10b and 3.10c illustrate typical waveforms produced by a full bridge VSC to generate sinusoidal current of I_A, 60Hz into a short circuit load. Using w_{hys} of $0.5I_A$ and I_A, the input (I_{ord}), output (I_{load}), and error ($I_{err} = I_{ord} - I_{load}$) waveforms of the CRPWM control scheme are presented. By tracking the movement of I_{ord} while containing I_{err} within a given error threshold, it is clearly shown in the figure that the goal of a fast responding and robust current control technique can be achieved.

The switching frequency of the VSC is irregular and is closely related to the hysteresis bandwidth and the load current slew rate. Given a slew rate of $0.01I_A/\mu s$, the switching frequency was found to be approximately 5kHz when w_{hys} was I_A, and 9.75kHz when w_{hys} was reduced by half. The frequency increase is due to the reason that I_{err} will reach the hysteresis thresholds faster with a smaller w_{hys}.

Though possible to reduce the switching frequency by expanding the hysteresis bandwidth and decreasing the current slew rate, the low frequency operation will bring forth undesired effects of high ripple level, reduced power bandwidth, and filtering problems. Lowering the hysteresis bandwidth and increasing the slew rate can alleviate these effects, but create the problems of emi (electromagnetic interference), increased dynamic losses, and controlling issues. Thus, these compromises must be considered carefully before deciding the hysteresis bandwidth and slew rate values.

In either case, the irregularity in the switching frequency remains a challenging task in designing a passive filter for the power converter. There are also application problems resulting from the variable switching frequency, such as the limit cycle phenomenon in a three-phase system due to the interference between phase controls [29]. Consequently, various techniques have been proposed to keep the operating frequency of the CRPWM scheme at constant, which include the use of variable shaped hysteresis bands [30][31][32] and incorporation of higher order filter and nonlinear control method [33].

3.4.2 SPWM (Sinusoidal Pulse Width Modulation) Switching Scheme

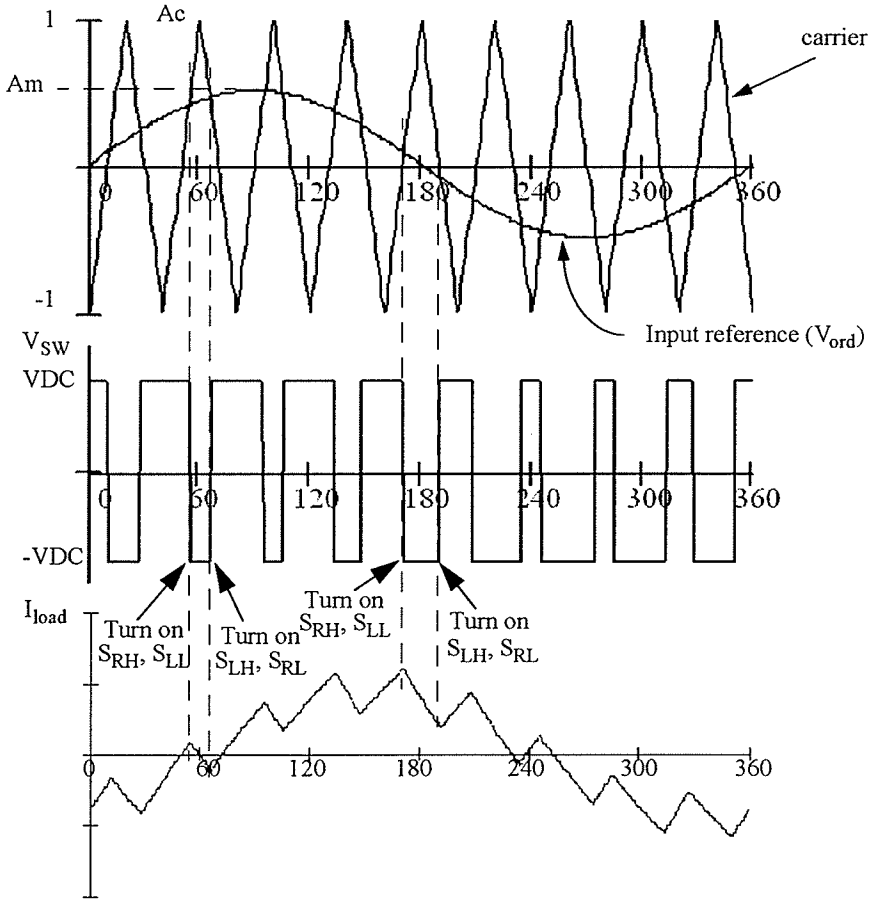


Fig. 3. 11 Typical output waveforms of SPWM switching scheme [34].

It is possible to maintain a constant switching frequency in the output waveform by using a SPWM control scheme. As shown in Fig. 3.11, a current waveform (I_{load}) resembling the input reference signal (V_{ord}) can be generated by modulating V_{ord} with a high frequency triangular carrier. Whenever V_{ord} crosses the carrier waveform, depending on whether it is greater or smaller than the carrier value, either a positive or a negative V_{SW} will be applied across the smoothing inductor (L_{smooth}) and external load (Z_{load}) of the VSC. Notice that there is only one on and off switching transition within each triangular wave period. Hence, switching frequency of the VSC is the same as the carrier wave frequency.

If the modulation signal is a sinusoidal waveform with amplitude A_m and frequency f_m, and the respective amplitude and frequency of the triangular carrier waveform are A_c and f_c, the ratios of A_m/A_c and f_c/f_m are known to be amplitude and frequency modulation index m_a and m_f, respectively. The fundamental component value of the output voltage can be controlled by adjusting m_a from 0 to 1. The remaining harmonic components appear as sidebands in the frequency spectrum, centered around the switching frequency and its multiples, i.e. around harmonics m_f, $2m_f$, $3m_f$, and so on.

For simulation purposes, assuming that the VSC operates with m_a of 0.8, VDC of 100V, m_f of 11, and modulation frequency of 60Hz, the simulated waveforms of V_{SW} and I_{load} and their respective frequency spectra produced by the SPWM control scheme are provided in Fig. 3.12.

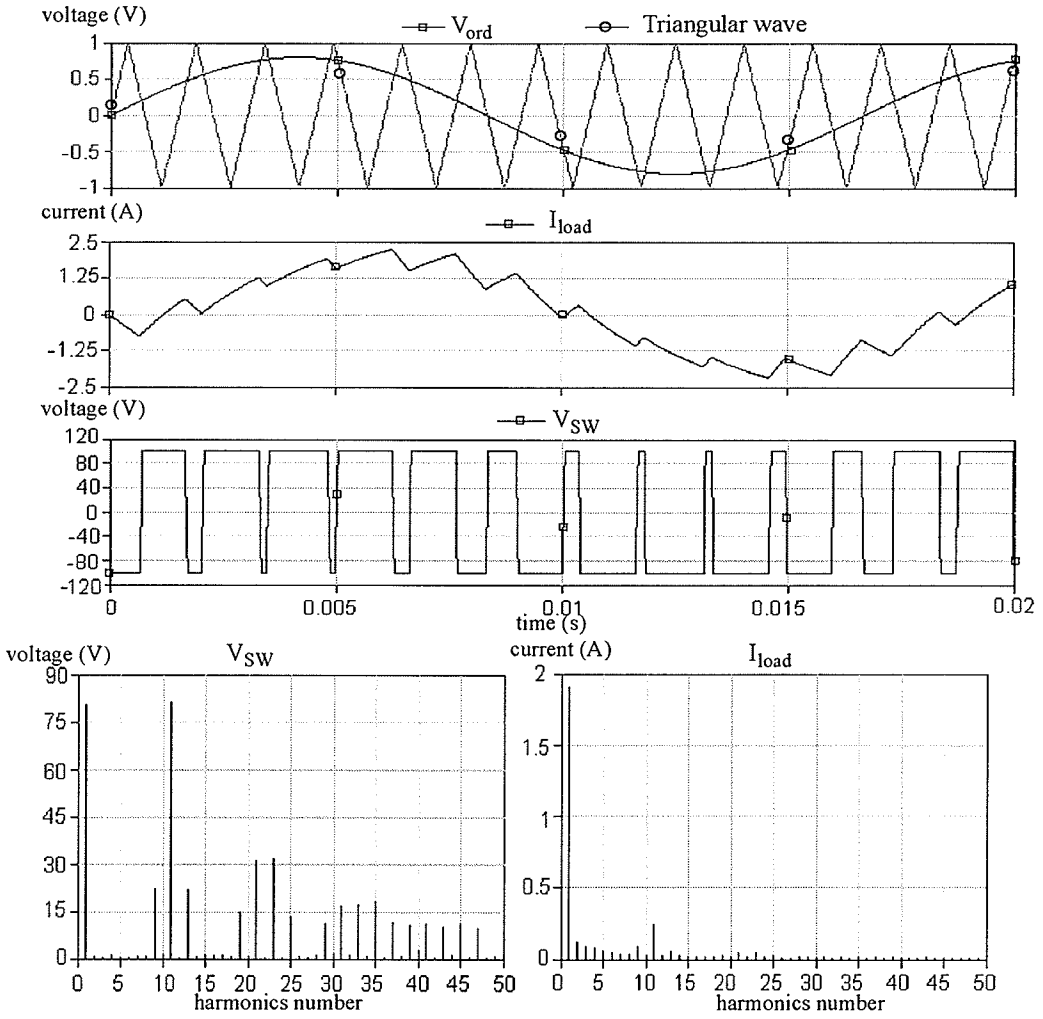


Fig. 3. 12 Simulated waveforms and frequency spectra of SPWM control scheme.

As shown in the spectra diagrams, the harmonic components of the output waveforms are shifted to a much higher frequency range. Using a combination of band pass and low pass filters, these high frequency harmonics can be removed easily. It is also shown that the fundamental component value (80V) of the voltage waveform is the product of m_a (0.8) and VDC (100V). Hence, the simulation results are in agreement with the discussed characteristics of the SPWM switching scheme.

The SPWM control scheme has the advantage of a constant switching frequency and hence determinable loses. Thus, it is best suited for generating any given voltage and eliminating selected lower order harmonics. Since SPWM is essentially a voltage-controlled technique, negative feedback system utilizing PID (Proportional, integrated, and differential) controller or lead lag compensator needs to be implemented to achieve the purpose of current control.

By using the negative feedback design, it is possible to ensure that the switching operation is insensitive to external disturbances. However, there will be phase shift and output error introduced by the voltage to current conversion and the feedback controller. In order to minimize the phase delay and output error, the feedback controller needs to be operated at high gain, which introduces excessive overshoot, oscillation, or even instability in the output waveforms. Consequently, though having the benefits of constant operating frequency, SPWM cannot perform as well as the CRPWM technique in terms of robust, stable, and instantaneous responses.

3.4.3 Three-Level Switching Techniques

In a typical amplifying application, it is always desired to suppress unwanted noise as much as possible to provide a high fidelity and low THD (Total harmonic distortion) output waveform. However, suppressing switching ripple of the VSC will bring forth problems of high dynamic losses, emi noise, and controllability. Nonetheless, there are other alternatives that can be implemented to achieve the performance of low switching frequency, while keeping the switching noise at low level, and one of these techniques is the three-level switching scheme.

There are a number of three-level control schemes documented in the literature, some of which are expansion of the original two-level methods, such as the doble hysteresis-band control schemes [35][36] and uni-polar PWM scheme based on the SPWM control method [37]. Recently, additional techniques, such as the use of two carrier waves in the dipolar modulation [38] and applications of sliding mode control technique [39], have also been introduced.

3.4.3.1 Three-level Double Hysteresis Band Control Technique

A double hysteresis band switching technique, which is similar to the CRPWM control scheme, can be used to illustrate operating principle of the three-level schemes. As shown in Fig. 3.13, two overlapping hysteresis bands of a given width (w_{hys}) are first defined and imposed around a reference signal (I_{ord}). The objective is to keep the measured load current (I_{load}) confined within the hysteresis thresholds by controlling its trajectory. As discussed in Section 3.3.2, the trajectory of I_{load} is dependant on the voltage (V_{SW}) applied across the smoothing inductor (L_{smooth}) and external load (Z_{load}) of the VSC. The three voltage states of V_{SW} are positive (VDC), negative (-VDC), and zero (0V), which will cause I_{load} to either increase, decrease, or decay exponentially.

Referring to Eqn. 3.3 and 3.5, given that the load voltage (V_{load}) is ranging from +15V to -15V, the magnitude of load current slew rate at the zero state is much lower, as compared to the positive and negative states. As a result, it is desired to control the switching operation mostly at the zero state, in order to reduce the operating frequency of VSC.

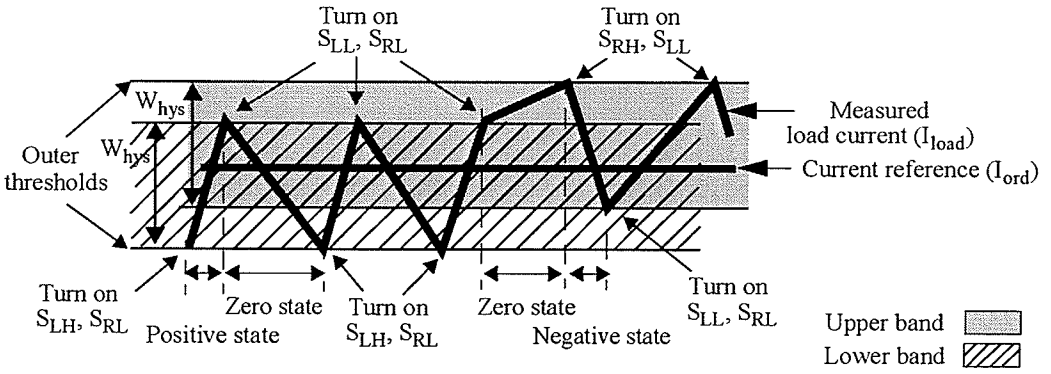


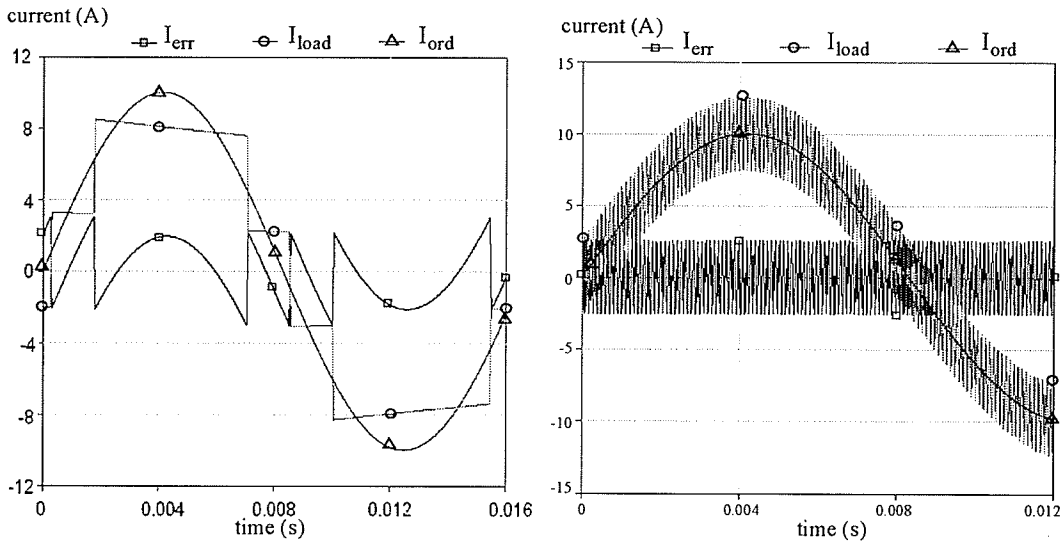
Fig. 3. 13 Operation of three-level double hysteresis band switching scheme.

As shown in the above figure, the lower hysteresis band is responsible for the state change of V_{SW} between positive and zero and vice versa, while the state change of negative and zero are controlled by the upper band. At any moment, there is only one active hysteresis band, and the trajectory of I_{load} is kept within the upper and lower thresholds of the active band by a switching controller.

If I_{load} can no longer track the movement of I_{ord} during the zero state, its trajectory will flow toward the outermost threshold of the inactive hysteresis band. The status of the hysteresis bands will be reversed from active to passive and vice versa as soon as I_{load} crosses the threshold. As a result, I_{load} is now controlled by the hysteresis band of the threshold it has just crossed.

Typical load current (I_{load}) and error (I_{err}) waveforms produced by the CRPWM and double hysteresis band switching techniques are presented in Fig. 3.14. These waveforms were obtained through the simulation of a full bridge VSC to deliver current of 10A, 60Hz

into a short circuit load, with a hysteresis bandwidth of 5A specified for both control schemes and a 1A offset separating the double band.



a. Three-level double hysteresis band control scheme. b. Two-level CRPWM control scheme.

Fig. 3. 14 Simulated waveforms of two-level and three-level control schemes.

As shown in the simulation results, I_{err} of the two-level control scheme was kept within the 2.5A threshold. Due to the 1A offset in the double band, I_{err} of the three-level scheme was slightly higher at 3A. By implementing the three-level scheme, the switching frequency of the VSC was approximately 50 times less than that of two-level scheme. Thus, the dynamic switching performance of the three-level scheme is clearly better.

The lowest frequency of the switching ripple produced by the three-level scheme was approximately 190Hz. Notice that the DC offset of the double band was also reflected in the load current waveform. As a result, it is difficult to remove the low frequency ripple and DC offset by using a conventional low pass passive filter. Unless the filtering problem

is addressed and the quality of the output waveform can be improved substantially, it is not feasible to implement the three-level scheme in the current amplifier design.

3.4.4 Other Advanced Control Schemes

In addition to the switching schemes discussed in the previous sections, there are other promising techniques utilizing advanced control principles documented in the literature, such as predictive controls [40], fuzzy logic [41], and neural networks [42]. These innovative approaches provide attractive opportunities to further improve existing performance of the switching converter and to overcome problems associated with the conventional switching techniques.

To review all of the power electronics switching methods, it will require extensive efforts and time, and it is not the purpose nor within the scope of this thesis to do so. Only the classical switching schemes discussed in the earlier sections are considered. Feasibility of these switching schemes used in the design of the current amplifier will be investigated in Chapter 4. By implementing the VSC and its switching algorithm with software simulation, any forthcoming problems can be addressed before constructing the hardware prototype, thereby resulting significant saving in cost and time.

3.5 Design Considerations for a Relay Testing Current Amplifier

Power electronics based converters are advantageous in providing a more efficient and hence "greener" voltage or current control solution. However, in order to achieve the high efficient performance, there is always trade-off. In general, switching converters suffer

from several shortcomings: more complicated overall design, lower waveform quality, reduced frequency bandwidth, undesired emi noise, and higher stresses on components.

As discussed in Section 3.2, there are always losses incurred during the operation of a switching converter. Design considerations have to be taken into account to ensure that these losses are minimized. Applications of snubber circuits, synchronous diodes [43], innovative switching techniques and topologies such as resonant converter [44] and multilevel schemes [45], and selection of better quality components, are a few examples that can be implemented to provide a more efficient and sound design. However, these additional measures have certainly complicated the converter design.

There are also other design issues that need to be addressed, such as the challenges of implementing the switching control digitally, limit cycle problem of a three-phase CRPWM control scheme, and needs to maintain constant switching frequency in certain applications for ease of filtering. Considerately efforts have been put forth to deal with these issues, thus further increasing complexity of the converter system.

The output error and emi noise resulting from the switching operation cannot be eliminated. Hence, precision and quality of the VSC waveforms can hardly surpass those produced using conventional analog method. Additionally, the emi noise can contaminate the supply line and affect proper operations of other proximal equipment. In order to minimize the effects of such interference, extensive shielding of the switching converter, as well as power line filter, are often needed.

Due to the finite response time of the switches and control circuitry, as well as the dynamic losses associated with high-speed switching, the switching frequency of a power converter cannot be increased indefinitely. In order to reduce the size of the passive filter and improve the filtering effects, it is desired to increase the switching frequency by at least seven to eight times the maximum frequency in the reference signal. With a typical switching frequency of 100kHz, the bandwidth of the output waveform is limited to 7kHz at best. Consequently, the frequency bandwidth of a classical switching converter is much lower, as compared to the analog devices, which can produce high fidelity output waveforms in the range of several megahertz.

Problems also arise when attempting to design passive filter for the relay testing current amplifier. Since the load impedance is very small and an unknown value, it is difficult to properly design a filter with the desired characteristic. The responses of the passive filter are dependent on the loading condition of the amplifier, as it will be shown in Chapter 4. Furthermore, any filter element applied in the high current path of the converter will translate to power loss and introduce unwanted phase delay, thereby affecting overall efficiency and performance of the amplifier.

Finally, due to the parasitic inductance inherent to the switches and connections within the circuit, as well as the reverse recovery characteristic of diodes, high-speed switching coupled with rapid interruption of the converter current will generate overvoltage, high di/dt and dv/dt. These stresses must be properly controlled to protect the electrical components from damaging and certain switches of the power converter from turning on inadvertently.

In the following chapter, possible solutions for some of the above problems will be explored. Upon implementing these solutions, it will be demonstrated from the software simulations that a high performance and yet efficient current amplifier design can be achieved.

CHAPTER 4 Software Simulations of the PWM Current Amplifier

4.1 Calculation of the Component Parameters

Before conducting the software simulation, the values of supply voltage (VDC) and smoothing inductance (L_{smooth}) must be decided for the VSC circuit. The VDC value must be higher than the 15V output compliance rating (specified in Chapter 2) by a significant margin. L_{smooth}, on the other hand, should be chosen such that the intended power frequency bandwidth of the current amplifier can be achieved.

During the VSC hardware development stage, it was learned that a 48V, 6A switch mode power supply and its matching capacitors were available off the shelf from suppliers. Hence, a decision was made to establish VDC equal to 48V. Upon deciding the DC source voltage, the value of L_{smooth} can be obtained as follows.

Assuming that the amplifier is required to deliver a sinusoidal output current waveform:

$$I_{ord} = A_{ord}\sin(2\pi F_{ord}t) \qquad \text{(EQ 4.1)}$$

where A_{ord} (A) and F_{ord} (Hz) are amplitude and frequency of I_{ord}, respectively, and t is time in second. The output current slew rate can be obtained by differentiating Eqn. 4.1:

$$\frac{dI_{ord}}{dt} = 2\pi F_{ord} A_{ord} \cos(2\pi F_{ord} t) \quad \text{(EQ 4.2)}$$

the slew rate is highest when t equals to n/F_{ord}, where n = 0, +/-1, +/-2, and so on. Notice that I_{ord} equals to 0A at these instances. Thus, the maximum slew rate is given as:

$$\frac{dI_{ordmax}}{dt} = 2\pi F_{ord} A_{ord} \quad \text{(EQ 4.3)}$$

For the load current to trace I_{ord}'s trajectory, it must have a much faster speed:

$$\frac{dI_{load}}{dt} \gg \frac{dI_{ordmax}}{dt} \quad \text{(EQ 4.4)}$$

Substituting Eqn. 3.3 and 4.3 into Eqn. 4.4, the following equation can be obtained:

$$\frac{V_{SW} - V_{load}}{L_{smooth}} \gg 2\pi F_{ord} A_{ord} \quad \text{(EQ 4.5)}$$

Assuming that the switching converter is connected to a resistive load (hence, $V_{load} = 0$ at $I_{load} = 0$) and by rearranging Eqn. 4.5, the maximum inductance L_{max} can be expressed as:

$$L_{max} = \left| \frac{V_{SW}}{2\pi F_{ord} A_{ord}} \right| \quad \text{(EQ 4.6)}$$

The maximum power frequency of the current amplifier was specified at 480Hz in Chapter 2. Hence, with V_{SW}, F_{ord} and A_{ord} equal to +/-48V, 480Hz, and $100A_{rms}$, respectively, L_{max} was found to be 113µH.

4.2 Calculation of the VSC's Maximum Output Values

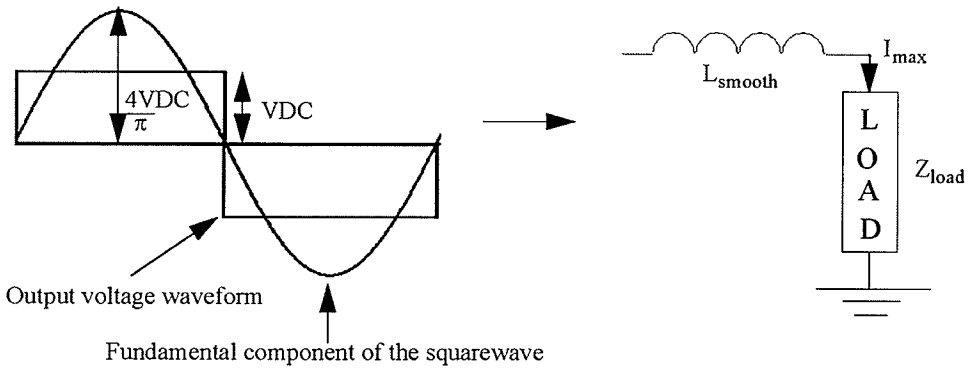


Fig. 4. 1 Maximum achievable output voltage of VSC.

Referring to Fig. 4.1, maximum output voltage of the VSC can be obtained by switching the bus voltage into a squarewave. By applying the squarewave across the smoothing inductor (L_{smooth}) and external load (Z_{load}), the maximum VSC output current (I_{max}) at the fundamental frequency is depicted as:

$$I_{max} = VDC \times \frac{4}{\pi} \times \frac{1}{sL_{smooth} + Z_{load}} \qquad \text{(EQ 4.7)}$$

assuming that the VSC is connected to a simple RL load with resistance R_{load} and inductance L_{load}:

$$Z_{load} = R_{load} + sL_{load} \qquad \text{(EQ 4.8)}$$

With L_{smooth} equals to 113μH and substituting various load values (0Ω, 0.433Ω, 0.611Ω, and 20μH) into Eqn. 4.7, frequency response curves of I_{max} are plotted in Fig. 4.2. It is clearly shown in the figure that I_{max} is dictated by the load value of the VSC. The highest attainable current rating occurs at Z_{load} of 0Ω. Higher inductive loads will lower the overall current rating. Higher resistive loads, similarly, will deteriorate the low frequency

performance of the VSC. Hence, loading conditions of the VSC must be carefully examined to ensure that the desired output waveforms can be delivered.

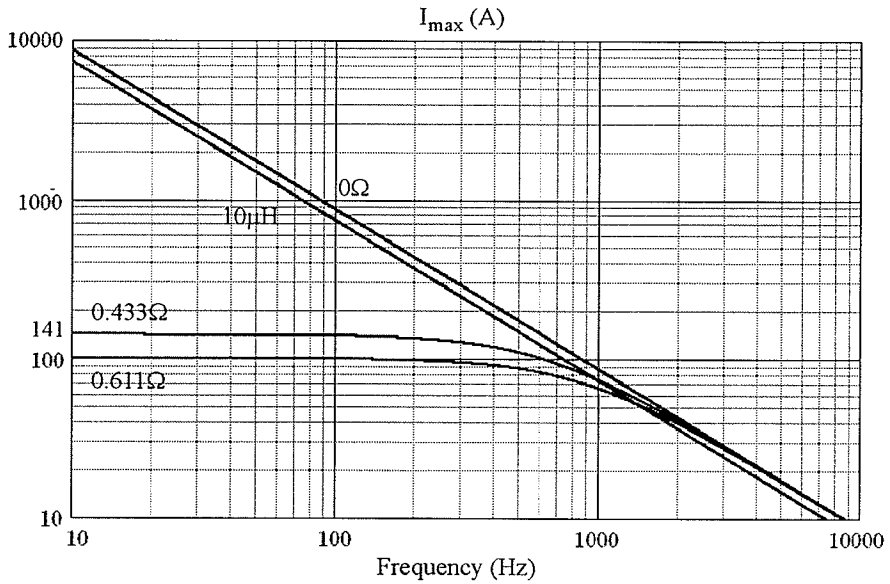


Fig. 4. 2 Maximum achievable current ratings of VSC at various load values.

For example, the load impedance must be kept well below 0.433Ω to generate the $100A_{rms}$ rated current at 60Hz. The allowable load impedance is also limited by the 15V compliance rating. To illustrate this, consider that injection of the rated current into a 0.433Ω load will produce load voltage of 61V, which is much higher than the compliance threshold. For the amplifier to operate within its specified range and deliver the rated current, the load impedance of the VSC must be further reduced to less than 0.106Ω

4.3 Simulation Results: CRPWM versus Sinusoidal PWM

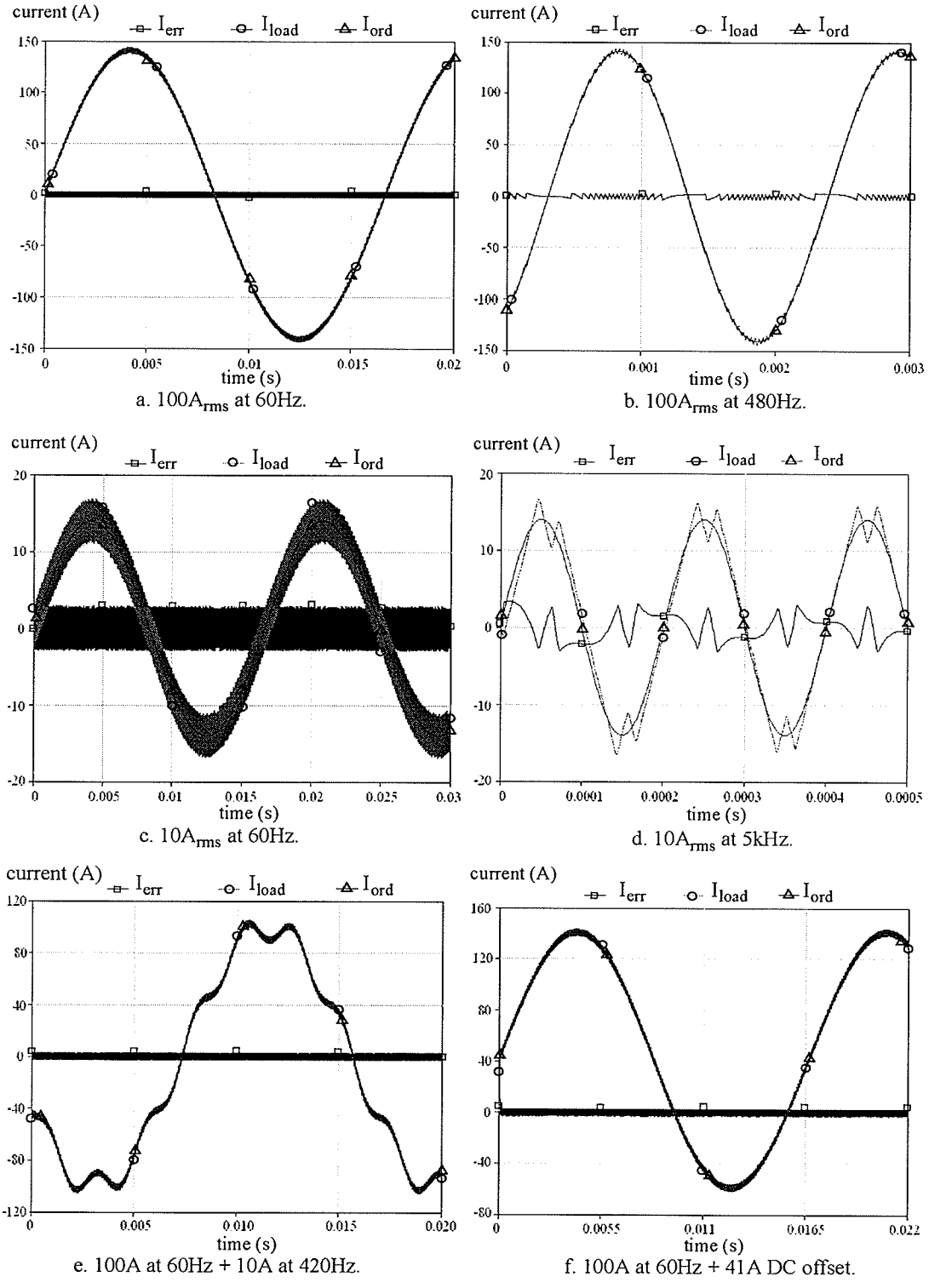
In this thesis, transient simulations of the full bridge VSC were performed using PSCAD/ EMTDC, which is an electromagnetic transient simulation program developed by the Manitoba HVDC Research Centre [46]. Sophisticated converter models can be simulated

easily by using power electronics components and advanced control logic models of the program. Coupled with a user-friendly interface to facilitate the simulation process, PSCAD/EMTDC is an ideal tool for examining the VSC design.

4.3.1 Simulation Results with the CRPWM Controlled Converter

The CRPWM control scheme was conducted using a full bridge VSC with VDC of 48V and L_{smooth} of 113μH. In order to keep the switching frequency well below 50kHz, hysteresis bandwidth of the control scheme was set to 5A. To demonstrate that a wide range of output waveforms can be produced by the VSC, simulations were performed for the current orders of $100A_{rms}$ at 60Hz and 480Hz, $10A_{rms}$ at 60Hz and 5kHz, 100A at 60Hz plus 10A at 420Hz, and 100A plus DC offset of 41A.

The input (I_{ord}), output (I_{load}), and error (I_{err}) waveforms of injecting the above currents into a short circuit load are provided in Fig. 4.3. As shown in Fig. 4.3a and 4.3b, the simulated VSC was capable of producing rated output of $100A_{rms}$ at 60Hz and at the power frequency of 480Hz. It is clearly shown in Fig. 4.3d that the waveforms produced by the CRPWM control scheme consist of minimum phase delay, even at a frequency as high as 5kHz. Furthermore, the control scheme was able to generate waveforms with high harmonic content and DC offset value, as demonstrated in Fig. 4.3e and 4.3f, respectively.



a. $100A_{rms}$ at 60Hz.

b. $100A_{rms}$ at 480Hz.

c. $10A_{rms}$ at 60Hz.

d. $10A_{rms}$ at 5kHz.

e. 100A at 60Hz + 10A at 420Hz.

f. 100A at 60Hz + 41A DC offset.

Fig. 4. 3 Simulation results of CRPWM control scheme at various current levels.

Notice that the output waveforms were heavily distorted with switching ripple. Thus, significant filtering effort is required to remove the switching noise and improve the waveform quality. As shown in the simulation results, I_{err} of the VSC can be kept within the 2.5A threshold. However, frequency of the switching operation was random, ranging from 30kHz to 40kHz. Finally, even if the current order is at zero level, the VSC was required to operate at high switching frequency, thus prompting high quiescent loss.

The simulation results demonstrate that the goal of constructing a high performance relay testing current amplifier is a few steps closer by utilizing the CRPWM technique. In order to proceed further, the problems of poor waveform quality, high dynamic loss, and high quiescent loss must be addressed. However, before discussing any possible solution, simulation results of the SPWM switching scheme are presented in the following section.

4.3.2 Simulation Results with a SPWM Controlled Converter

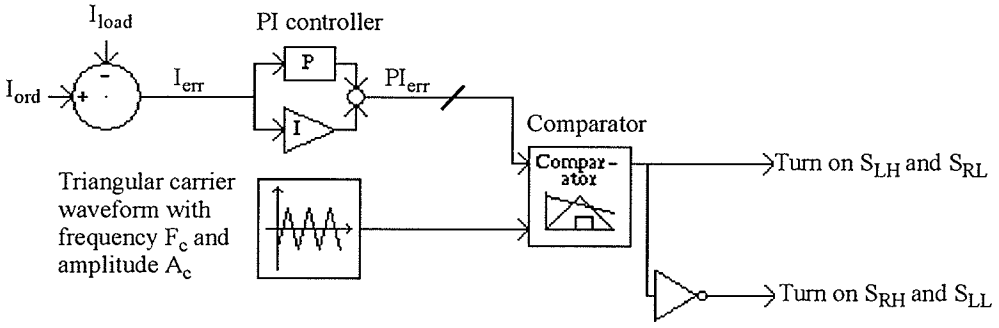
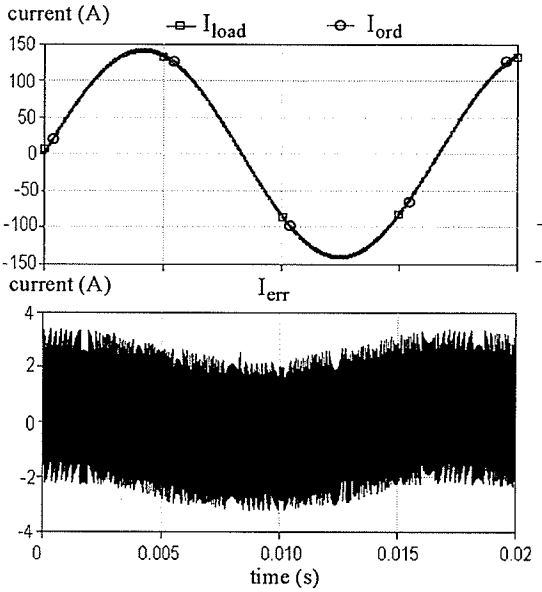


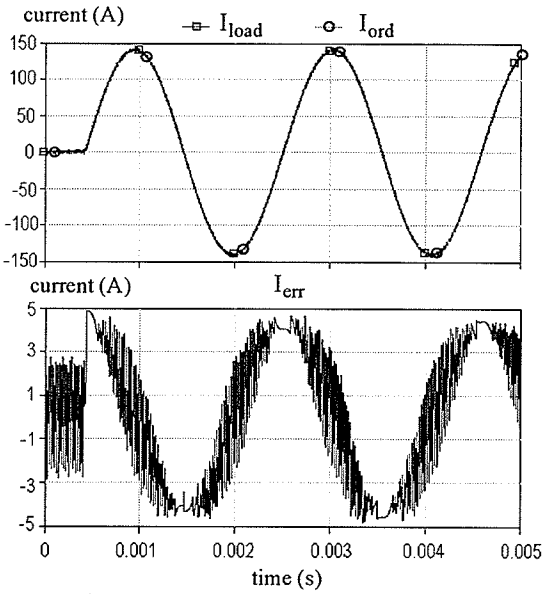
Fig. 4. 4 Negative feedback design of SPWM current controller.

As discussed in Section 3.4.2, SPWM is a voltage controlled switching technique. To achieve the goal of current control, the VSC must rely upon negative feedback design similar to the block diagram of Fig. 4.4. Rather than using the voltage order, it is the

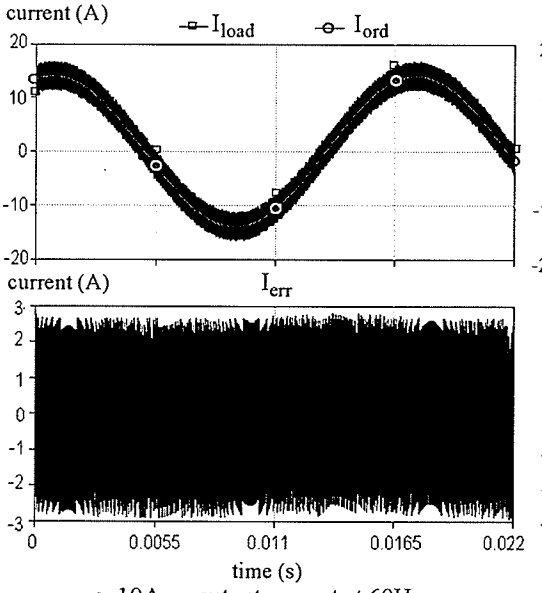
current error (I_{err}) that is compared with the triangular carrier wave. Notice that I_{err} will be processed by a PI (Proportional and integrated) controller before entering the comparator block. In doing so, the feedback error can be minimized, thus allowing generation of highly accurate output current waveforms.



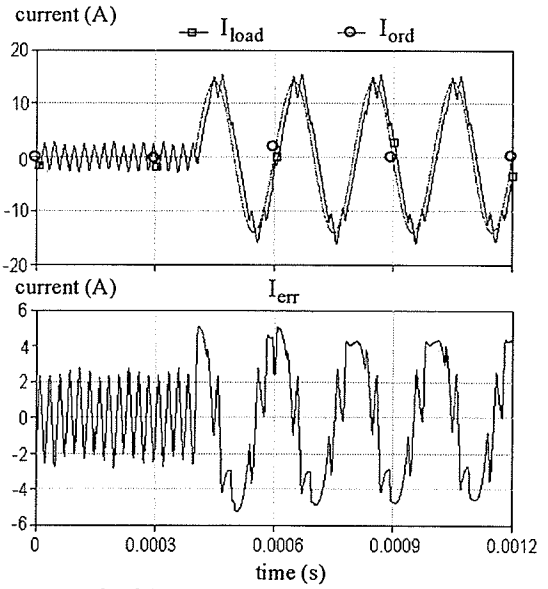
a. $100A_{rms}$ output current at 60Hz.



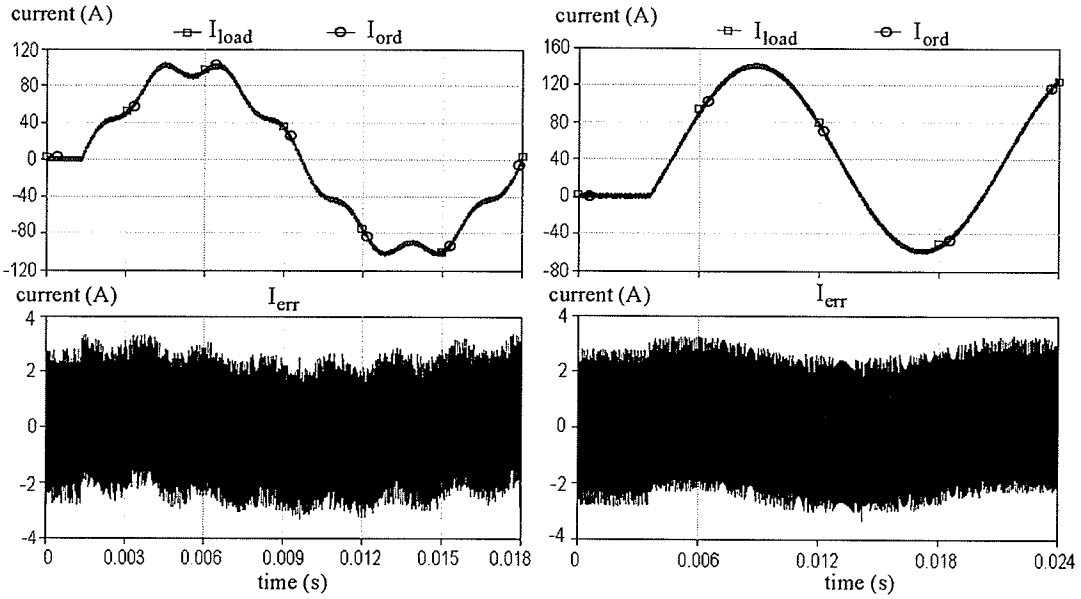
b. $100A_{rms}$ output current at 480Hz.



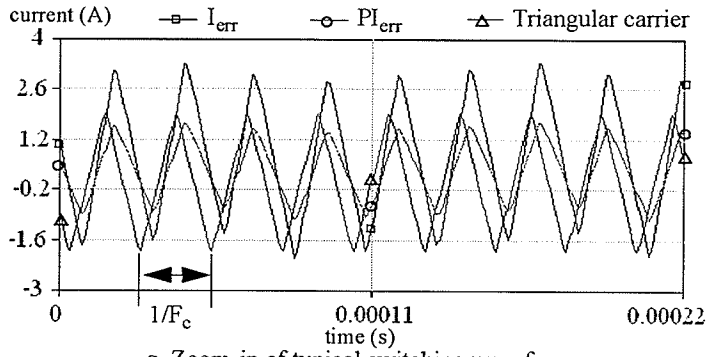
c. $10A_{rms}$ output current at 60Hz.



d. $10A_{rms}$ output current at 5kHz.



e. 100A output current at 60Hz plus 10A at 420Hz. f. 100A output current at 60Hz plus DC 41A.



g. Zoom-in of typical switching waveforms.

Fig. 4. 5 Simulation results of SPWM switching scheme at various current levels.

By implementing the SPWM control scheme, the input (I_{ord}), output (I_{load}), and error (I_{err}) waveforms of injecting various test currents into a short circuit load are given in Fig. 4.5. The frequency (F_c) and amplitude (A_c) of the triangular carrier were set to 40kHz and +/- 2A, respectively. The current orders were the same set of test waveforms used in the CRPWM control scheme simulations.

As shown in the simulation results, the VSC was capable of producing a wide range of currents by utilizing the SPWM control scheme and the negative feedback controller. The rated output waveforms of $100A_{rms}$ at 60Hz and at the power frequency of 480Hz were successfully generated and presented in Fig. 4.5a and 4.5b, respectively. The VSC was able to generate low level currents of $10A_{rms}$ at 60Hz and 5kHz as shown in Fig. 4.5c and 4.5d, as well as waveforms containing harmonic content (100A at 60Hz + 10A at 420Hz) and DC offset (100A at 60Hz + DC 41A) as provided in Fig. 4.5e and 4.5f, respectively.

Notice that the load current waveforms were also distorted with switching ripple. Thus, filtering is required to improve the waveform quality. In addition, it is clearly shown in Fig. 4.5e that there is a phase delay in the 5kHz output waveform. The delay was introduced by the PI controller and the process of voltage to current conversion. As shown in the switching waveforms of Fig. 4.5g, the PI error signal (PI_{err}) would cross the triangular wave twice within each period of 1/Fc. Thus, switching frequency of the VSC was kept constant at 40kHz. However, the simulated I_{err} could fluctuate from as low as 2A to as high as 5A.

The high gain design of the negative feedback system will introduce undesired current overshoot in the output waveforms. For example, referring to the waveforms generated by the SPWM control scheme in Fig. 4.6, a step change of current order (I_{ord}) from 0A to 100A in a 0.1Ω load would bring forth overshoot of 132% in the load current (I_{load}). In contrast, the load current waveform generated by the CRPWM control scheme was unaffected by the same disturbance.

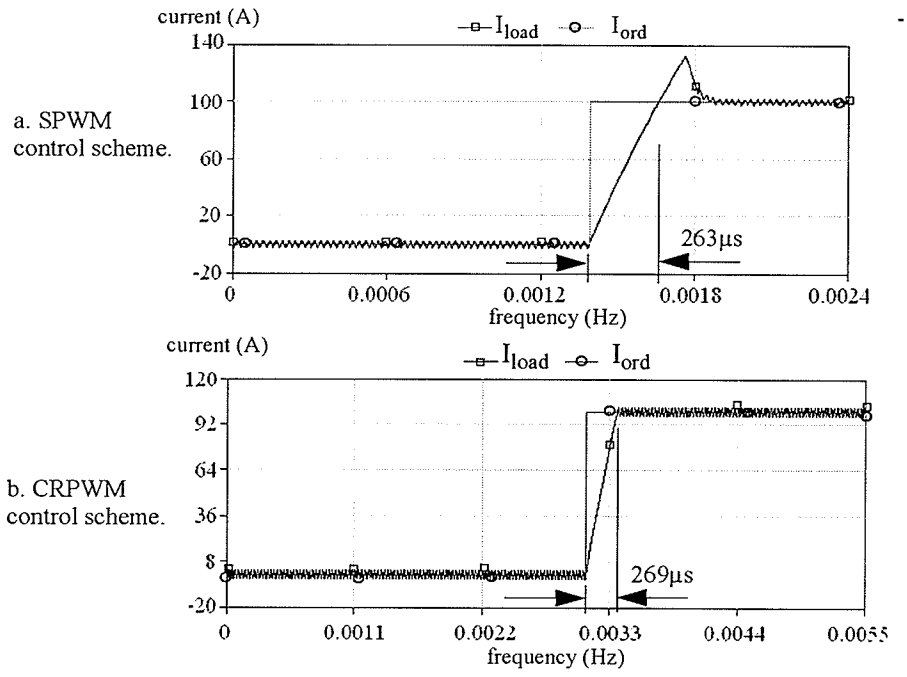


Fig. 4. 6 Simulated step responses of SPWM and CRPWM control schemes.

The SPWM switching scheme offers advantages of constant frequency operation, but it has uncontrollable output error. The CRPWM control scheme, on the other hand, operates at variable switching frequency, but the switching error can be contained within a given threshold. However, no matter which switching scheme is chosen, they both offer a much more efficient current control solution for the amplifier design, as compared to the conventional analog approach.

In the following sections, design measures will be introduced to further improve the existing switching performance and transform the VSC into a high performance relay testing current amplifier.

4.4 Implementation of Energy Storage Capacitor

Up until now, DC source of the VSC has been considered as ideal. In reality, any DC power supply will have a finite source impedance and limited current rating. Therefore, it is necessary to investigate these effects by simulating the circuits of Fig. 4.7.

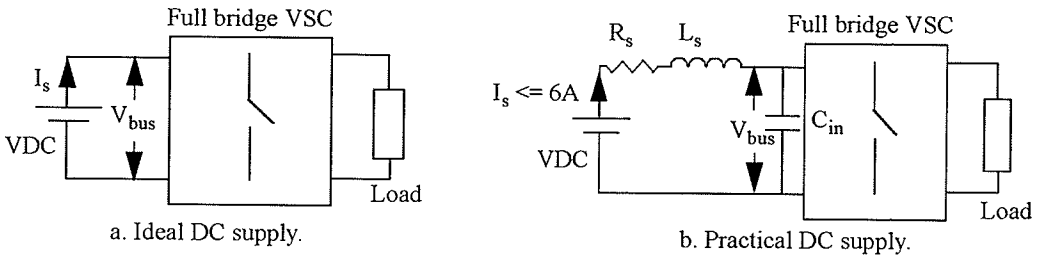


Fig. 4. 7 Simplified diagrams of ideal and practical DC source in the VSC circuit.

4.4.1 Simulation Results of the Ideal and Practical DC Source

The source current (I_s) and bus voltage (V_{bus}) waveforms of Fig. 4.8 represent results of simulating the ideal and practical DC source in the VSC circuit. The VSC was controlled by the CRPWM switching scheme with w_{hys} of 5A to deliver a current of $100A_{rms}$, 60Hz into a 0.1Ω load. As shown in Fig. 4.8a, if the DC source were ideal, V_{bus} would remain constant at 48V during the entire simulation run. However, I_s would rise to $100A_{rms}$ to accommodate the high power output demand.

In contrast, by using a practical DC supply, V_{bus} will drop below 48V, as soon as the power demand of the VSC exceeds the supply rating. The practical supply was modeled by having source impedance of (0.1Ω+0.1μH), input capacitance of 1000μF, and current rating of 6A. As shown in Fig. 4.8b, shortly after the power supply was overloaded, its protection scheme would reduce the supply voltage in an attempt to keep I_s below 6A. If

V_{bus} drops below the output compliance threshold of 10V, the VSC will fail to generate the desired current waveform.

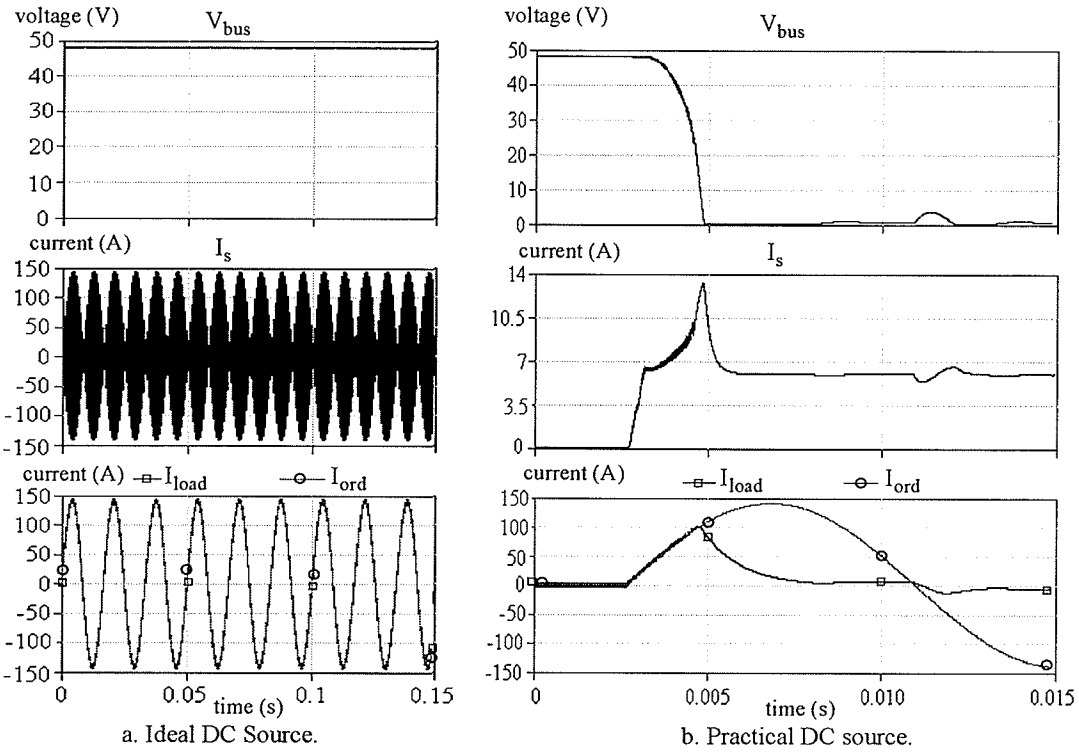


Fig. 4. 8 Simulation results of ideal and practical DC source in the VSC circuit.

4.4.2 Possible Solutions for the Lack of Power Issues

The above voltage drop problem can be alleviated by either increasing current capacity of the existing DC supply, or complementing the supply with a secondary source. In this project, the first option is definitely not a viable solution. It is difficult to obtain a 48V power supply that can deliver current as high as 100A. DC supply with such a high power rating will be heavy and bulky, and impractical to be integrated into the current amplifier design. Moreover, most relay tests will not be conducted for a prolonged period at very

high current level. Thus, it is ineffective to utilize DC source with high continuous power rating in the VSC circuit.

A better approach is to keep the supply rating unchanged at the 6A level. The high current surge during the transient testing is provided by a supplementary high capacity energy storage capacitor. Since the power supply is only accountable for the nominal rating of the current amplifier, its continuous power requirements can be reduced significantly.

4.4.3 Simulation Result of Implementing the Energy Storage Capacitor

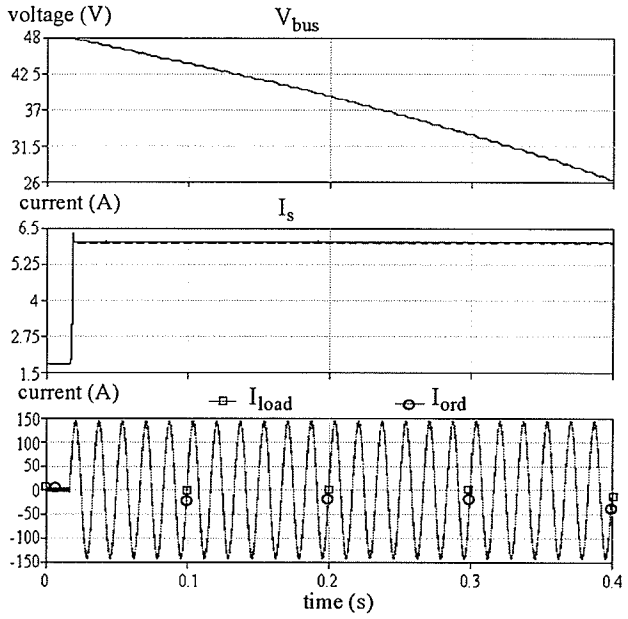


Fig. 4. 9 Simulation result of using a 0.5F energy storage capacitor in the VSC circuit.

Simulation result of using a 0.5F capacitor to complement the practical DC supply is provided in Fig. 4.9. It is clearly shown that the simulated VSC was capable of producing $100A_{rms}$ into a 0.1Ω load for more than 20 cycles, even if the source current (I_s) was limited to only 6A.

4.4.4 Determination of the Required Energy Storage Capacitor Value

It is possible to estimate analytically the maximum operating time (t_{max}) of a lossless VSC, starting from the onset of the high current injection test, until the load current fails to keep up with the current order. To simplify the calculation, assuming that the source impedance (R_s, L_s) is negligible, and the VSC will produce a 100A DC current, which has the same output power as the $100A_{rms}$ sinusoidal waveform.

Referring to Fig. 4.10 and Eqn. 4.9, the overall power supplied by the DC source and the high capacity capacitor must be balanced by the power dissipated into the load plus the power loss of the switching operation:

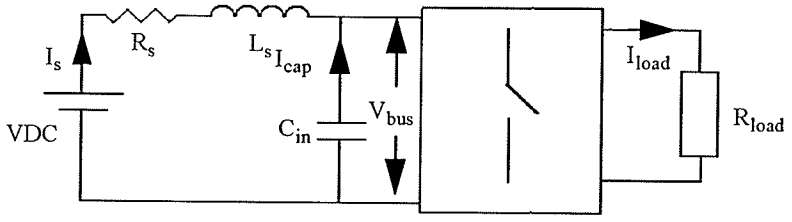


Fig. 4. 10 Practical circuit of implementing the energy storage capacitor.

$$\bar{V}_{bus}\bar{I}_{cap} + \bar{V}_{bus}\bar{I}_s = (\bar{I}^2_{load}R_{load} + P_{loss}) \qquad \text{(EQ 4.9)}$$

where I_s equals to 6A, $\bar{V}_{bus}$ is the average bus voltage, C_{in} is the input capacitance, P_{loss} is the power loss, and $\bar{I}_{cap}$ and $\bar{I}_{load}$ are the average capacitor and load current, respectively. Since the VSC is assumed lossless, the value of P_{loss} is zero. $\bar{I}_{cap}$ can also be expressed as:

$$\bar{I}_{cap} = -C_{in}\frac{d\bar{V}_{bus}}{dt} \qquad \text{(EQ 4.10)}$$

The VSC will fail to generate the output current, as soon as:

$$\overline{V}_{bus} = \overline{I}_{load} R_{load} \qquad \text{(EQ 4.11)}$$

By solving Eqn 4.9, 4.10, and 4.11, maximum operating time (t_{max}) of a lossless VSC can be obtained for any given value of load resistance (R_{load}).

It is also possible to obtain the maximum running time of the current injection test through software simulation. By simulating the practical VSC circuit of Fig. 4.10 and executing the CRPWM control scheme with a 5A hysteresis bandwidth, the maximum operating time (t_{CRPWM}) can be measured from the start of the high current test, until the moment when the VSC fails to generate the requested current waveform.

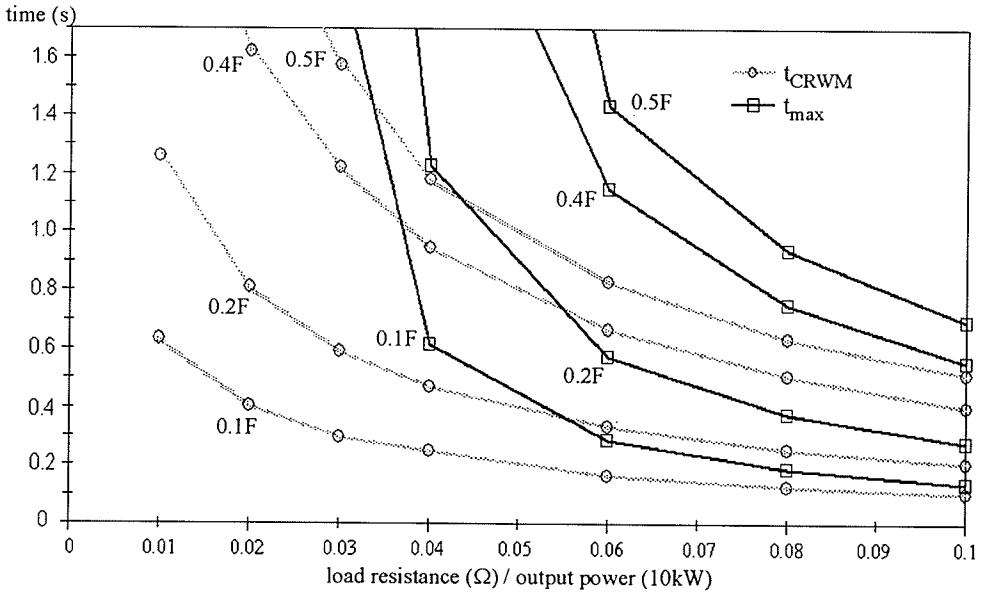


Fig. 4. 11 Maximum operating time of VSC for delivering 100A DC current.

Using various capacitance values (0.1F, 0.2F, 0.4F, and 0.5F), the resulting curves of t_{max} and t_{CRPWM} are presented in Fig. 4.11. It is clearly shown in the figure that the high current operating time can be increased substantially by using the energy storage

capacitor. The higher the value of C_{in}, the longer the switching operation can be performed for a given load resistance (output power). Given the same loading condition and C_{in} value, there is a discrepancy, especially at low load resistance, between t_{max} and t_{CRPWM}. The differences are mainly due to the static and dynamic power losses ignored in the calculation of t_{max}.

The ten-cycle power rating of delivering rated current of $100A_{rms}$ to a 15V load is 1061W. According to the simulation results, such performance can be accomplished by using C_{in} of approximately 0.172F. In contrast, if the VSC was lossless, the minimum value of C_{in} could be further reduced to 0.127F. Thus, by improving the power efficiency of the switching converter, it is possible to minimize the required capacity and physical size of the energy storage capacitor.

4.5 Filtering of the VSC Output Waveforms

One of the major problems in dealing with a power electronics based converter is the poor quality waveform it produces. The high frequency switching noise of the output waveforms needs to be attenuated substantially by low pass filtering. However, as discussed in Section 3.5, it is difficult and inefficient to design passive filters with unknown load value. The designing task becomes even more difficult for VSC that executes variable frequency switching scheme. Even if the switching frequency can be maintained at a constant level to allow for easier filter implementation, the filtering will bring forth undesired effects of phase shift and gain error in the output waveforms.

A novel filtering system, which incorporates a combination of passive low pass filter and analog active filter, is presented in this thesis to address the above problems. The passive filter is used to attenuate the high frequency switching harmonics. The lower frequency harmonic noise including any DC offset, on the other hand, can be cancelled by the active filter. Consequently, it is possible to effectively remove the switching error resulting from the converter operation by using such a filtering system.

4.5.1 Design of the Low Pass Passive Filter

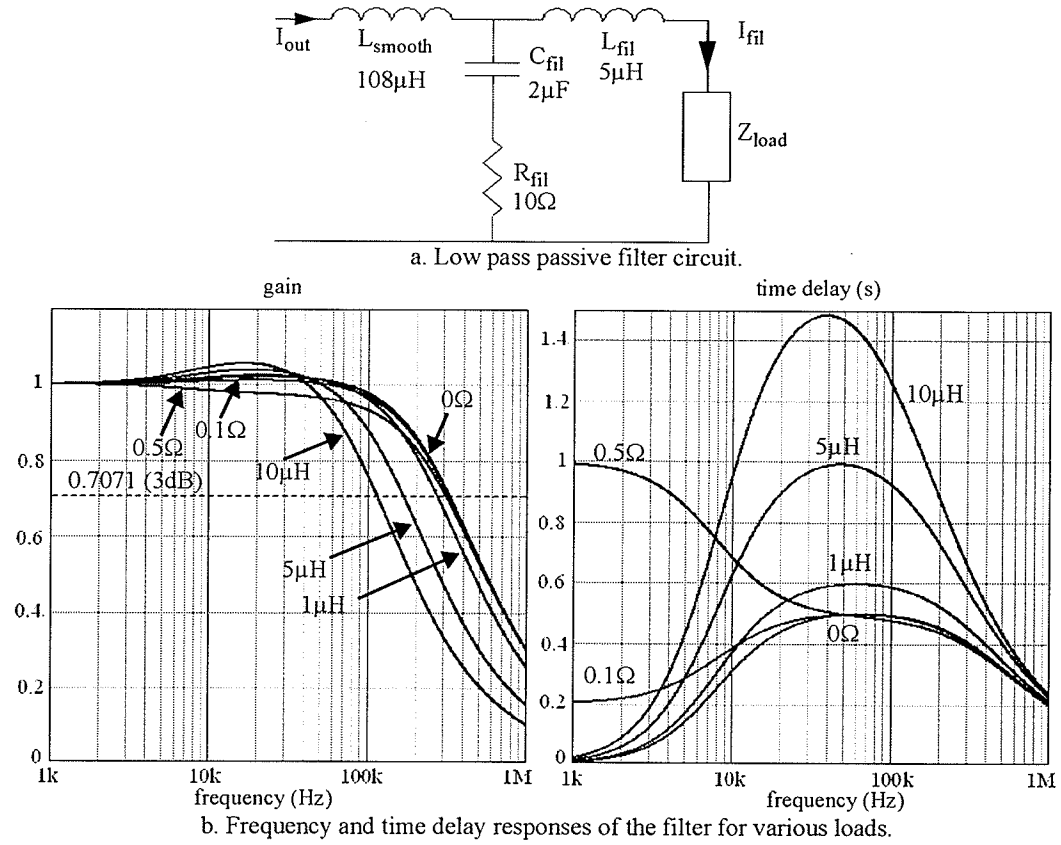
As shown in Fig. 4.12a, a two-pole LCR (Inductor, capacitor, and resistor) filter was implemented in the VSC circuit. The characteristic equation of the low pass filter is:

$$\frac{I_{fil}}{I_{out}} = \frac{\frac{1}{sC_{fil}} + R_{fil}}{Z_{load} + sL_{fil} + \frac{1}{sC_{fil}} + R_{fil}} \qquad \text{(EQ 4.12)}$$

The filter was constructed using L_{fil} of 5μH, C_{fil} of 2μF, and R_{fil} of 10Ω to achieve a 3dB cut-off frequency of 100kHz, which is almost one decade beyond the 20kHz amplifier bandwidth. In order to keep the overall slew rate limiting inductance at the desired value of 113μH, notice that the value of L_{smooth} was adjusted to 108μH.

Fig. 4.12b illustrates the gain and time delay responses of the low pass filter, when it is connected to various loads (0Ω, 0.1Ω, 0.5Ω, 1μH, 5μH, 10μH). It is clearly shown that the filter responses are dependent on the loading condition. However, regardless of the load value, the filter is capable of attenuating substantially any switching harmonics beyond 100kHz. Even at a load value as high as 10μH, the time delay and overshoot of the filtered

waveforms are kept well below 1.5μs and 110%, respectively. Hence, the phase and gain errors resulting from the filtering can be minimized, even if the load impedance value is unknown.



a. Low pass passive filter circuit.

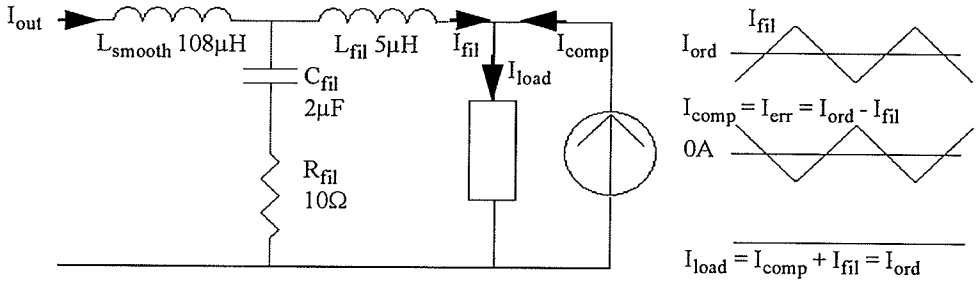
b. Frequency and time delay responses of the filter for various loads.

Fig. 4. 12 Design and implementation of low pass passive filter.

4.5.2 Design of the Active Filter

The active filter can be constructed using an analog current source, which is capable of generating highly accurate, high frequency, and linear current waveforms. As shown in Fig. 4.13a, the current source is fed with the error signal (I_{err}) and delivers to the external load a compensating current (I_{comp}). Referring to Fig. 4.13b, I_{comp} is an exact duplicate of

I_{err}. By combining the filtered current (I_{fil}) and the compensating current, it is possible to reduce the switching error significantly and produce a high quality load current waveform (I_{load}) equal to I_{ord}.



a. Circuit diagram of the active and passive compensators. b. Compensation waveforms.

Fig. 4. 13 Design and implementation of analog current compensator.

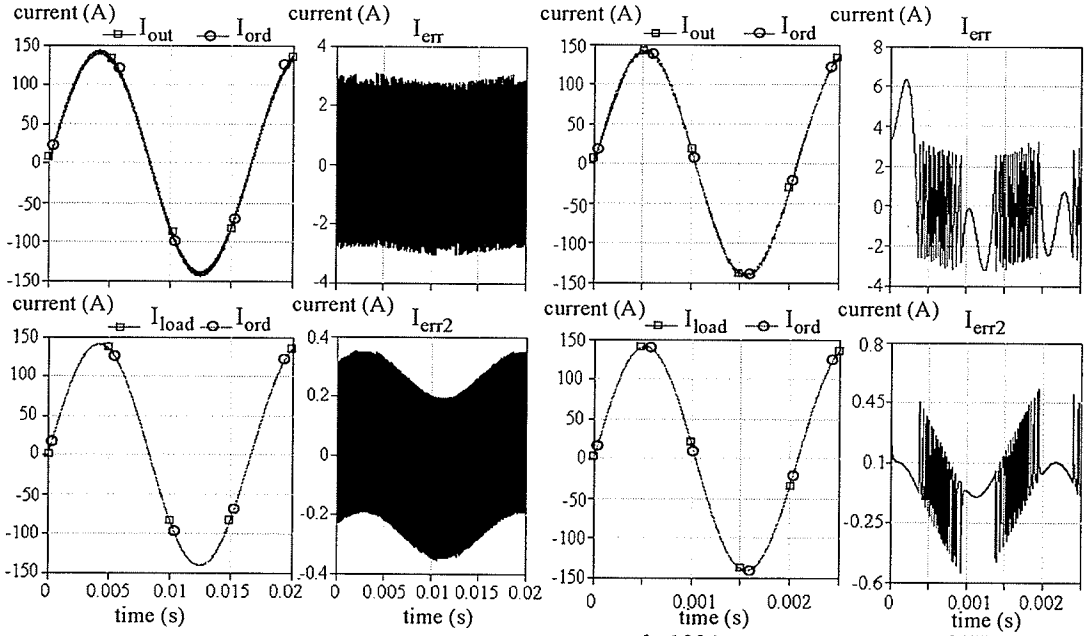
Notice that the active filter is intended for compensating I_{fil}, rather than the smoothing inductor current (I_{out}). In doing so, the bandwidth requirement of the analog compensator can be reduced to the cut-off frequency of the passive filter, thereby substantially simplifying the current source design.

As discussed in Chapter 1, the implementation of the analog approach will bring forth drawbacks of poor power efficiency and increased package size in terms of amplifier design. To minimize these drawbacks, output rating of the current source must be kept at a low level. Consequently, the active filtering approach is only applicable for a VSC that executes a constant-error switching scheme, such as the CRPWM control technique.

4.5.3 Simulation Results of the Active and Passive Filtering System

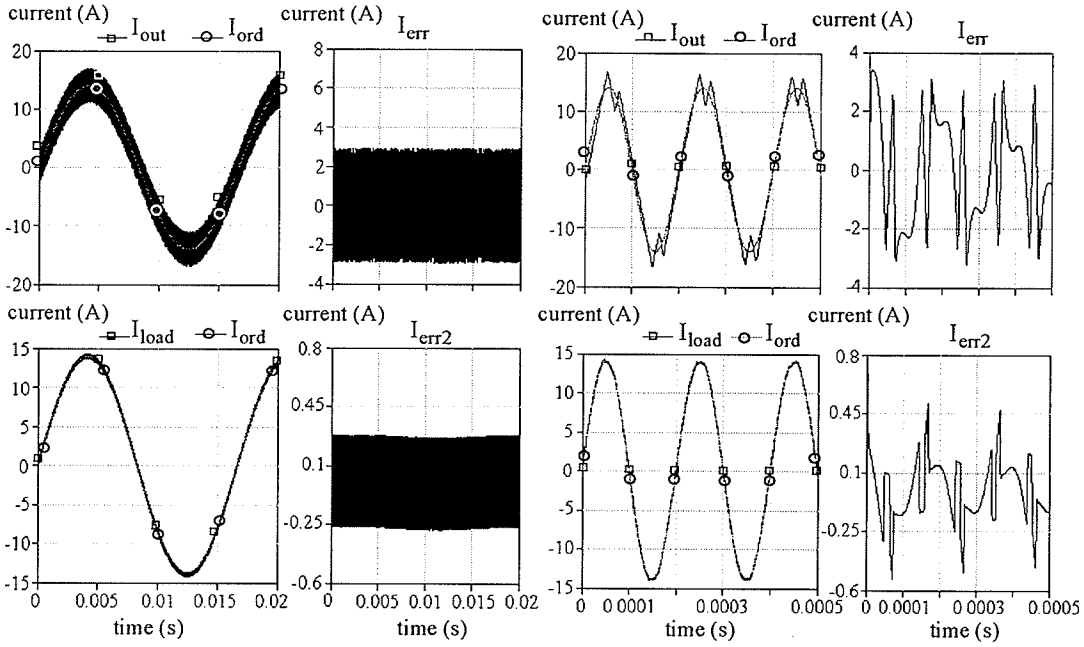
Simulation results of applying both the active and passive filters in the VSC circuit are presented in Fig. 4.14. For ease of comparison, the VSC would produce the same test waveforms used in the simulation examples of CRPWM and SPWM control schemes.

By utilizing the CRPWM control scheme with w_{hys} of 5A, the input (I_{ord}), pre-filtered (I_{out}), and filtered (I_{load}) waveforms of the VSC to generate the test currents into a 0.1Ω load are presented in the figure. It is clearly shown in the simulation results that the VSC has barely noticeable output noise (I_{err2}). This is because as much as 94% of the current error (I_{err}) was suppressed by the hybrid filter. The hybrid filter was also capable of reducing the switching ripple for currents as low as $10A_{rms}$ (Fig. 4.14c and 4.14d), as well as waveforms containing harmonic content (Fig. 4.14e) and DC offset (Fig. 4.14f).



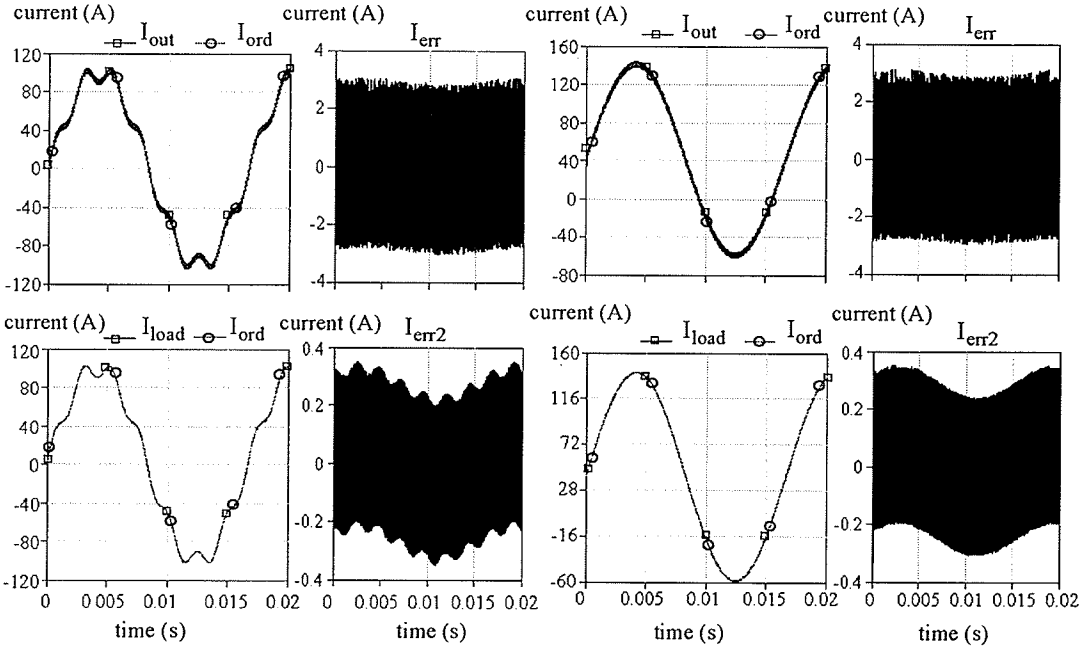
a. $100A_{rms}$ output current at 60Hz.
Peak I_{err2}: 0.35A.

b. $100A_{rms}$ output current at 480Hz.
Peak I_{err2}: 0.58A.



c. Output current of $10A_{rms}$ at 60Hz. Peak value of I_{err2}: 0.28A.

d. Output current of $10A_{rms}$ at 5kHz. Peak value I_{err2}: 0.61A.



e. Output current of 100A, 60Hz plus 10% of its 7th harmonics. Peak value of I_{err2}: 0.35A.

f. Output current of 100A, 60Hz plus DC offset of 41A. Peak value of I_{err2}: 0.33A.

Fig. 4. 14 Simulation results of implementing the passive and active filtering system.

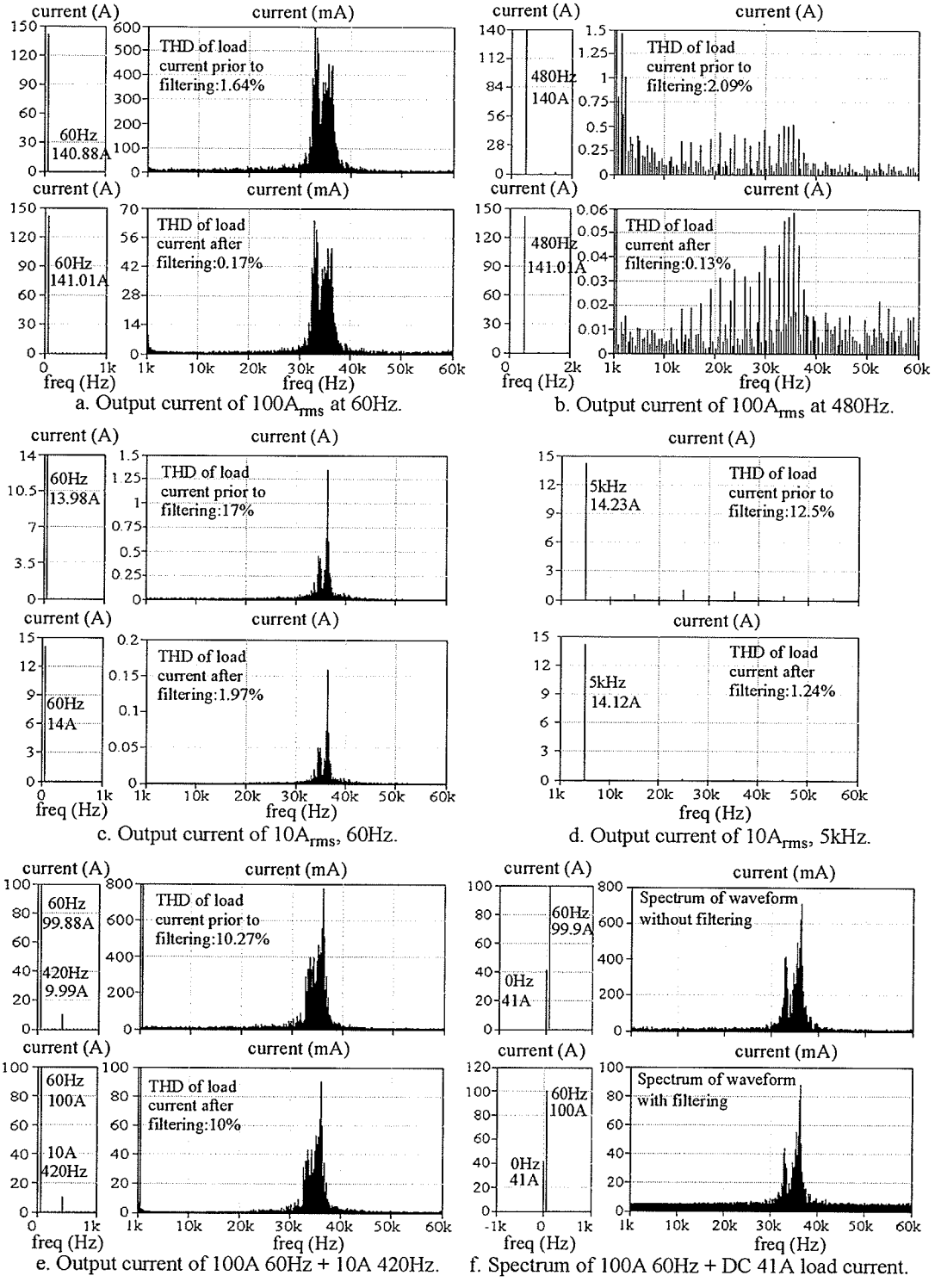


Fig. 4. 15 Spectra diagrams of waveforms before and after implementing the hybrid filter.

Frequency spectral analysis of the load currents (I_{load}), with and without using the hybrid filter, was performed and illustrated in Fig. 4.15. As shown in the figure, there is a significant reduction of THD (Total harmonic distortion) for the filtered load currents: from as much as 2.09% down to 0.13% for the $100A_{rms}$ waveform in Fig.4.15b and from 17% down to 1.97% for the $10A_{rms}$ waveform in Fig. 4.15c. Furthermore, other than the case of Fig. 4.15c ($10A_{rms}$ at 60Hz), harmonics of the filtered load currents are well below 1% with respect to their fundamental value.

Finally, the fundamental component of the filtered current waveforms has almost the same value as the input reference signal. The worst-case accuracy is approximately 100.8% for producing the current of $10A_{rms}$, 5kHz as seen in Fig. 4.15d. Thus, it is confirmed by the simulations that the VSC, compensated with the hybrid filter, is capable of generating highly accurate and low noise output current waveforms.

4.6 Low level Current Cut-off Measure

4.6.1 Problems of the VSC Switching Schemes at Low Current Level.

Although switching noise of the VSC can be substantially reduced with the hybrid filter, the resulting noise factor and THD are still considerably high at low current level. As shown in Fig. 4.16a and 4.16b, by using the CRPWM switching scheme with w_{hys} of 5A, the generation of $5A_{rms}$ currents at 60Hz and 5kHz would produce output error (I_{err2}) as high as 0.28A and 0.44A, respectively. Furthermore, if the frequency of the current order (I_{ord}) is increased to 20kHz, the VSC will be too slow to react to the high frequency

request. As a result, as shown in Fig. 4.16c, the analog current source was required to deliver as high as 7.7A to compensate the switching error.

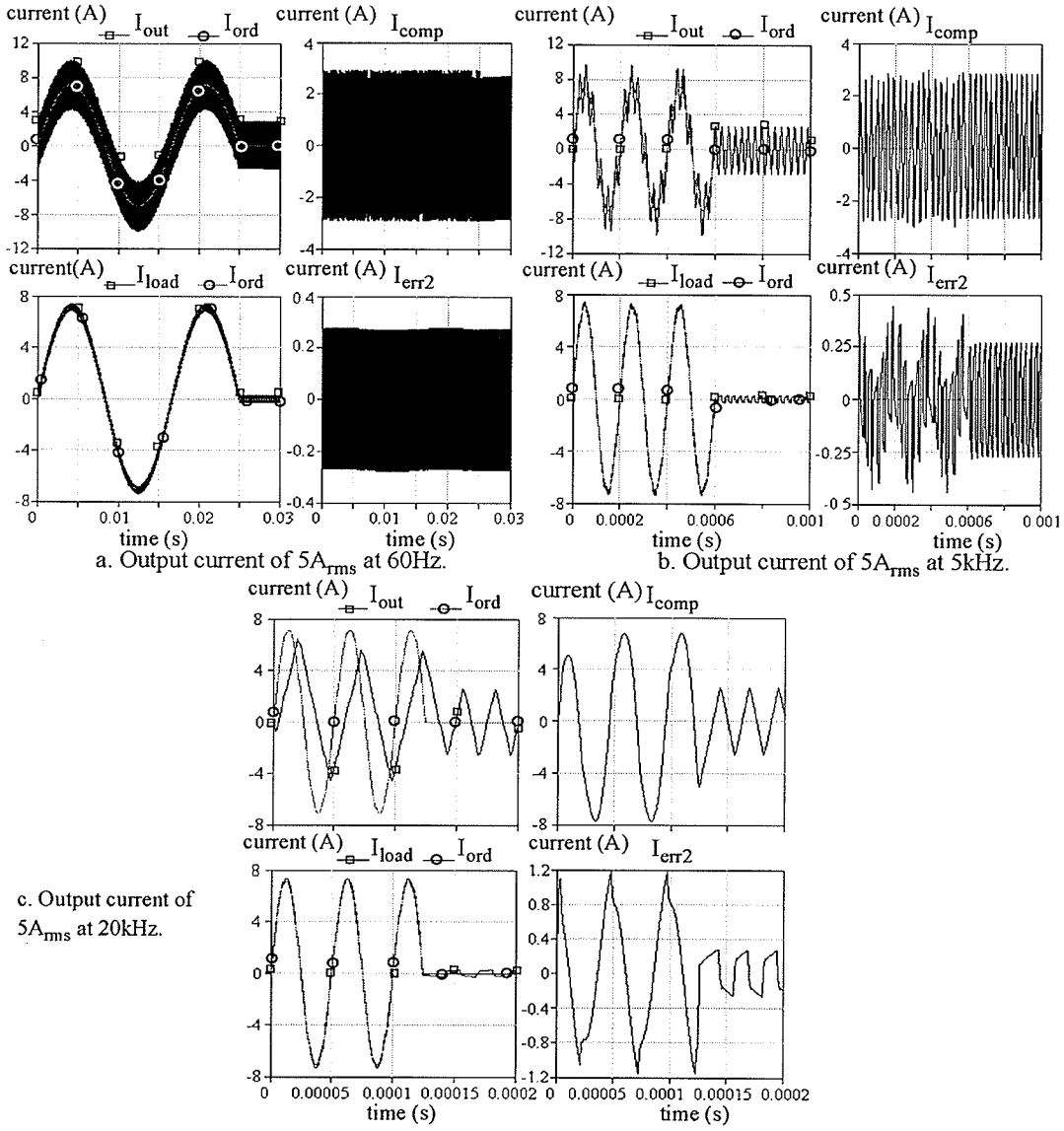


Fig. 4. 16 Simulation results of low current waveforms at $5A_{rms}$.

Finally, notice that the VSC has to operate even if the value of I_{ord} is zero, and the analog source has to supply a steady stream of compensating current to overcome the switching

ripple. Instead of cutting off the current flowing from the converter system to the external load, the current compensation obviously causes a high level of undesired quiescent loss.

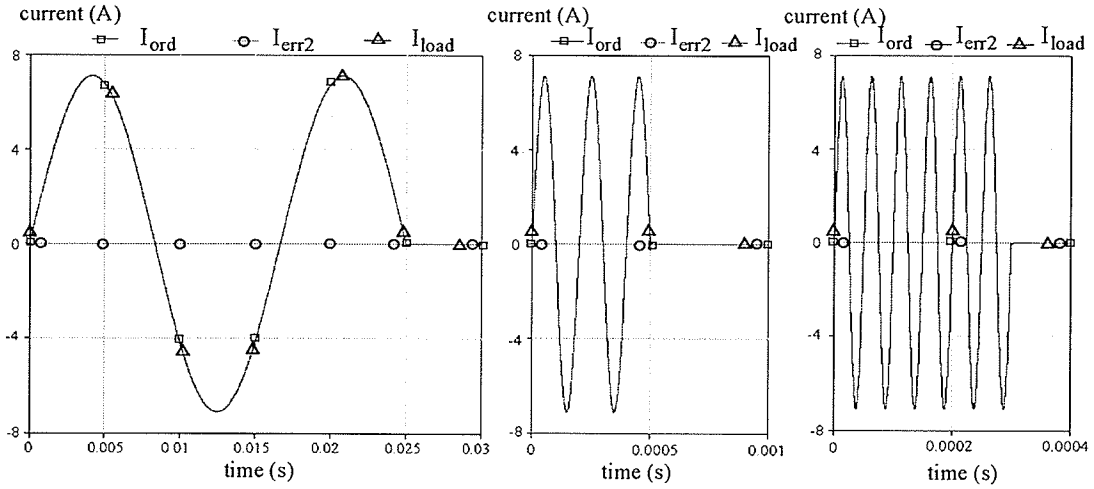
4.6.2 Implementation and Simulation Results of the Low Current Cut-off Scheme

In this project, a control technique was derived to address the above problems. The control method calls for an additional hysteresis band placed upon the reference waveform (I_{ord}). The hysteresis thresholds are set in a way that the VSC will stop its switching operation, as soon as I_{ord} falls within +/-$5A_{rms}$. Notice that the $5A_{rms}$ threshold coincides with the nominal input rating of a typical protective relay. I_{ord} must rise above +$5.66A_{rms}$ or drop below -$5.66A_{rms}$ for the switching operation to resume. In doing so, any current less than $5A_{rms}$ will be supplied by the analog source, thereby ensuring high quality waveforms at the small signal level.

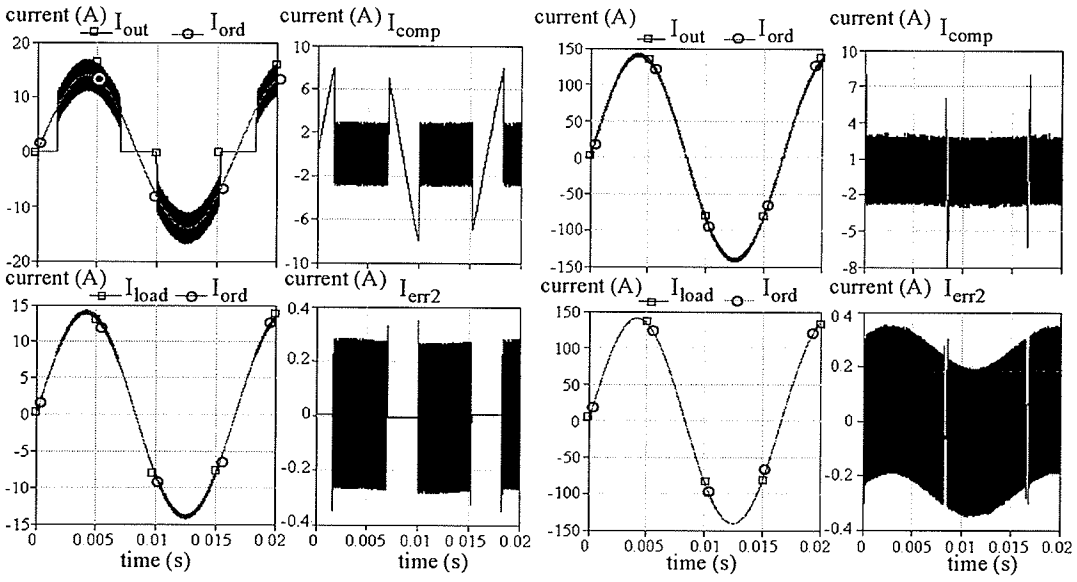
By implementing the low current cut-off technique to reproduce the test waveforms of Fig. 4.16, it is clearly shown in the simulation results of Fig. 4.17a, 4.17b, and 4.17c that the switching noise in the output waveforms could be eliminated. The resulting THD and noise level (I_{err2}) of the load current waveforms were extremely low. In addition, notice that both the VSC and analog source did not produce any current when I_{ord} returned to the zero level, thus solving the issue of high quiescent loss.

For the generation of load current waveforms with magnitude higher than $5.66A_{rms}$, the switchover irregularity will be compensated by the active filter. Hence, as shown in the

simulation results of Fig. 4.17d ($10A_{rms}$, 60Hz) and 4.17e ($100A_{rms}$, 60Hz), the operation of the low current cut-off scheme was transparent in the output waveforms.



a. Output current of $5A_{rms}$ at 60Hz. b. Output current of $5A_{rms}$ at 5kHz. c. Output current of $5A_{rms}$ at 20kHz.



d. Output current of $10A_{rms}$ at 60Hz. e. Output current of $100A_{rms}$ at 60Hz.

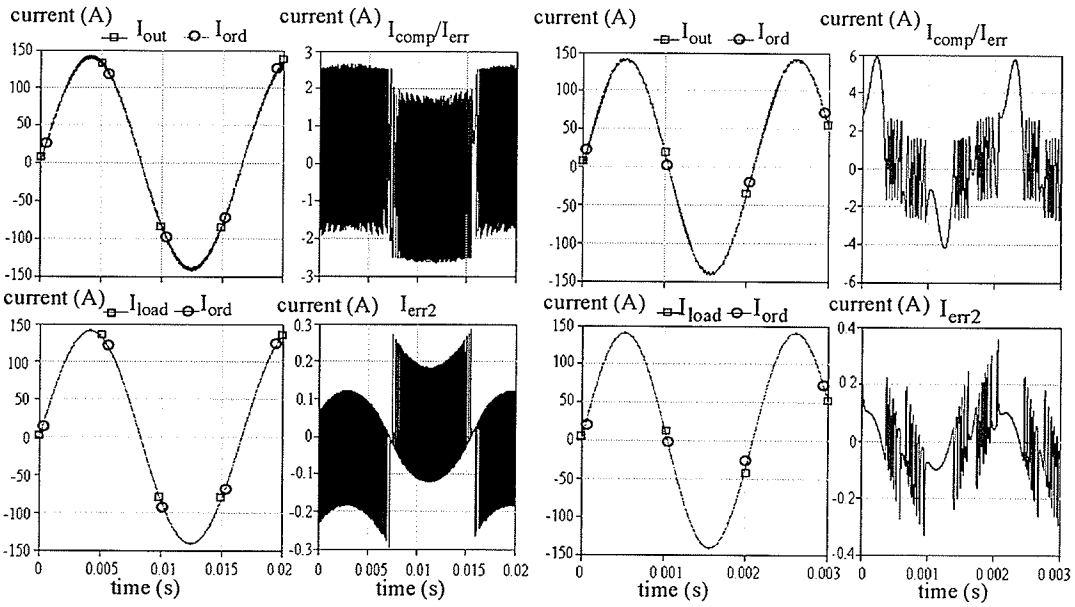
Fig. 4. 17 Simulation results of implementing low level cut-off control scheme.

4.7 Implementation of the Three-Level Switching Scheme

4.7.1 Simulation Results of the Three-Level Double Hysteresis Band Control Scheme

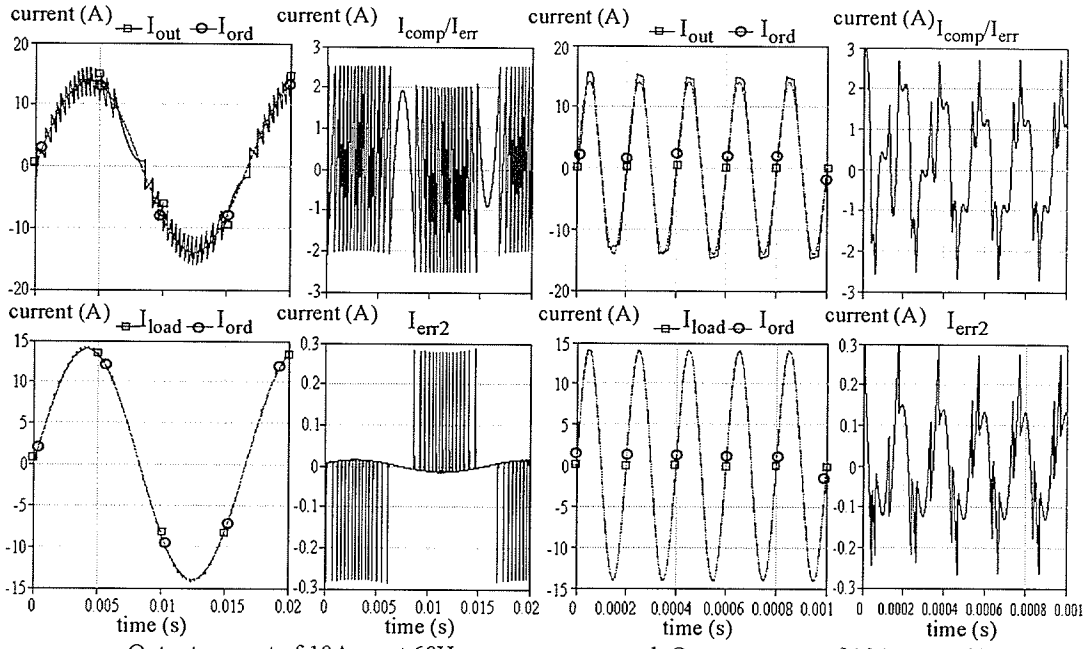
As discussed in Section 3.4.3, due to the poor quality output waveforms, it is not feasible to implement the three-level control scheme in the current amplifier design. However, by utilizing the hybrid filtering system, it is possible to reduce the low frequency switching ripple and DC offset produced by the double hysteresis band control technique. Hence, the issues of poor waveform quality can be addressed, and the three-level switching scheme can be applied in conjunction with the hybrid filter to further improve the dynamic switching performance of the VSC.

Fig. 4.18 illustrates simulation results of implementing both the double hysteresis band control scheme and the hybrid filtering system in the VSC circuit.



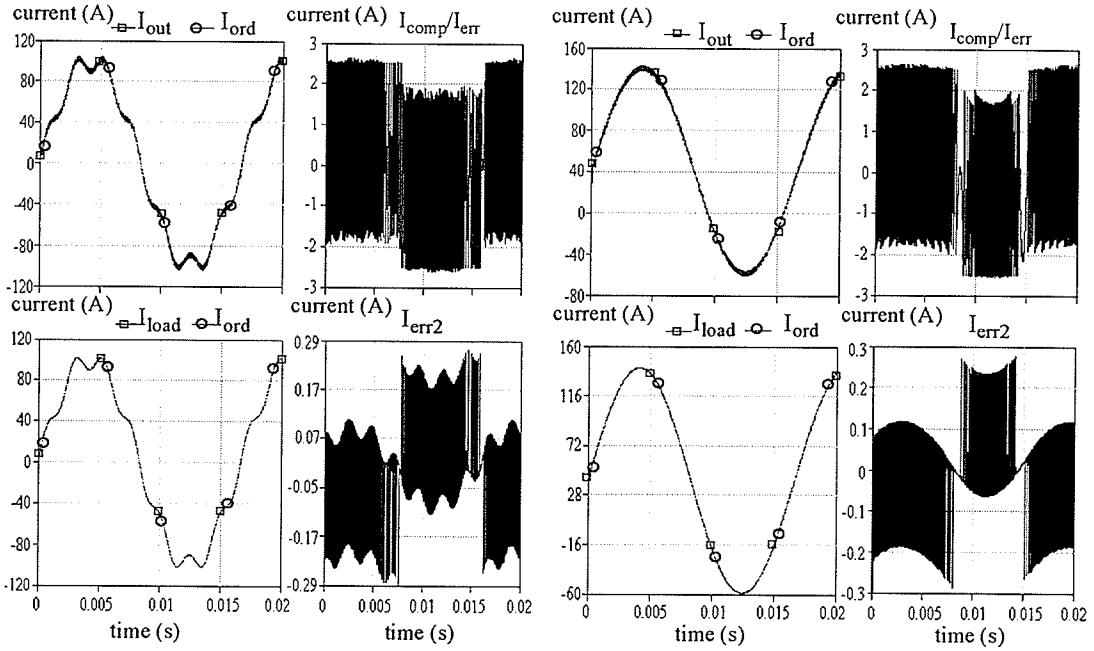
a. $100A_{rms}$ output current at 60Hz.
Peak I_{err2} value: 0.3A.

b. $100A_{rms}$ output current at 480Hz.
Peak value of I_{err2}: 0.33A.



c.Output current of $10A_{rms}$ at 60Hz.
Peak value of I_{err2}: 0.286A.

d. Output current of $10A_{rms}$ at 5kHz.
Peak value of I_{err2}: 0.331A.



e. Output current of 100A at 60Hz + 10% of its 7th harmonics. Peak value I_{err2}: 0.305A.

f. Output current of 100A 60Hz + 41A DC offset.
Peak value of I_{err2}: 0.285A.

Fig. 4. 18 Simulation results of three-level double band hysteresis control scheme.

By executing the three-level scheme with w_{hys} of 4.5A and offset of 1A, the input (I_{ord}), pre-filtered (I_{out}), and filtered (I_{load}) waveforms of injecting various test currents into a 0.1Ω load are presented. These test currents are: $100A_{rms}$ at 60Hz and 480Hz, $10A_{rms}$ at 60Hz and 5kHz, 100A at 60Hz plus 10A at 420Hz, and 100A at 60Hz plus DC 41A.

It is clearly demonstrated by the simulations that the VSC was capable of generating a wide range of output currents with high-speed response, while confining the switching error (I_{err}) within the 2.5A threshold. Compared to the CRPWM control scheme with the same threshold level, the operating frequency of the three-level control scheme was found to be much lower, ranging from 360Hz to 22kHz. As a result, the dynamic switching loss of the VSC can be reduced significantly. Furthermore, as shown in the figure, the low frequency ripple and the 1A DC offset introduced by the control scheme can also be reduced, thus allowing the generation of high quality output waveforms.

4.7.2 Performance Improvements: Two-Level versus Three-Level Control Schemes

To evaluate the waveform quality, the THD (Total harmonic distortion), noise factor, fundamental component value, and gain error of the load currents produced by using the CRPWM and double hysteresis band control schemes, implemented in conjunction with the hybrid filter, are both listed in Table 4.1. It is clearly shown that average THD of the waveforms produced by the three-level scheme is 55% lower than that of two-level scheme. In general, the noise factor is also lower, and noise level of -53dB can be achieved for the rated current of $100A_{rms}$ at 60Hz. The reduction of THD and noise level

is mainly due to the low operating frequency of the three-level scheme, which allows for a much more effective filtering task.

Table 4.1. Summary of load current waveform quality.

Control Scheme	Load Currents	THD	Noise Factor	Fundamental Component Value	Gain Error
Two-level CRPWM control scheme	$100A_{rms}$ at 60Hz	0.17%	-52dB	141.01A	0.007%
	$100A_{rms}$ at 480Hz	0.13%	-47dB	141.01A	0.007%
	$10A_{rms}$ at 60Hz	1.97%	-34dB	14A	0.71%
	$10A_{rms}$ at 5kHz	1.24%	-27dB	14.12A	0.14%
	100A at 60Hz + 10A at 420Hz	10%	-49dB	100A	0%
	100A at 60Hz + DC 41A	---	-50	100A	0%
Three-level double hysteresis band control scheme	$100A_{rms}$ at 60Hz	0.09%	-53dB	140.99A	-0.007%
	$100A_{rms}$ at 480Hz	0.08%	-52dB	141.01A	0.007%
	$10A_{rms}$ at 60Hz	0.37%	-34dB	14A	-0.71%
	$10A_{rms}$ at 5kHz	0.84%	-33dB	14.07A	-0.21%
	100A at 60Hz + 10A at 420Hz	10%	-50dB	100A	0%
	100A at 60Hz + DC 41A	---	-51dB	100A	0%

To compare the power performance of the two-level (CRPWM) and three-level (double hysteresis band) control schemes, the high current injection test of Section 4.4.4 was performed. Given the capacitance of 0.1F, 0.2F, 0.4F, and 0.5F, maximum operating time curves of the two control schemes, t_{CRPWM} and t_{3level}, were obtained from the simulation of injecting DC current of 100A to various resistive loads.

The plot of t_{CRPWM} and t_{3level} with respect to load value (output power) of the VSC is presented in Fig. 4.19. As shown in the figure, the VSC implemented with the three-level scheme can perform the current injection test, particularly at low load resistance values, for a much longer duration. Thus, it is confirmed through the simulation results that the

power performance and waveform quality of the current amplifier can be further improved by using the three-level switching scheme and the hybrid filtering system.

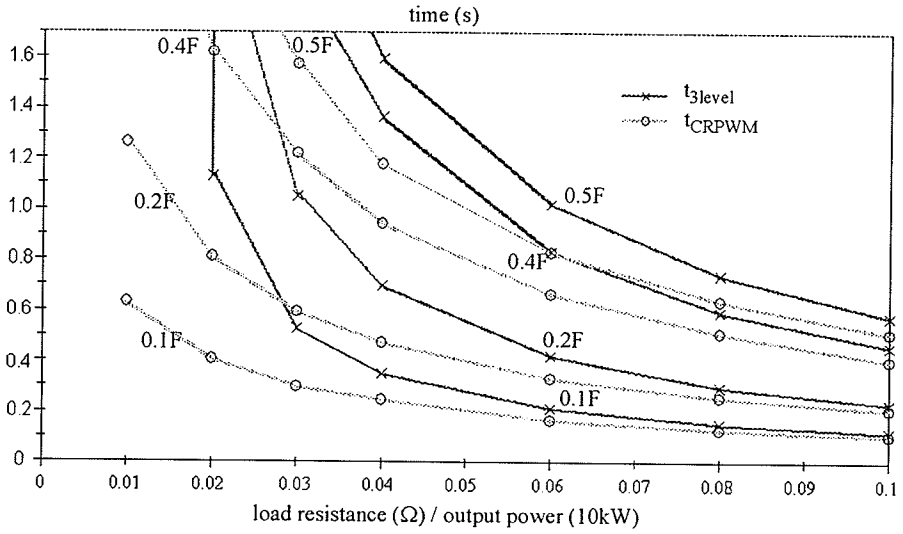


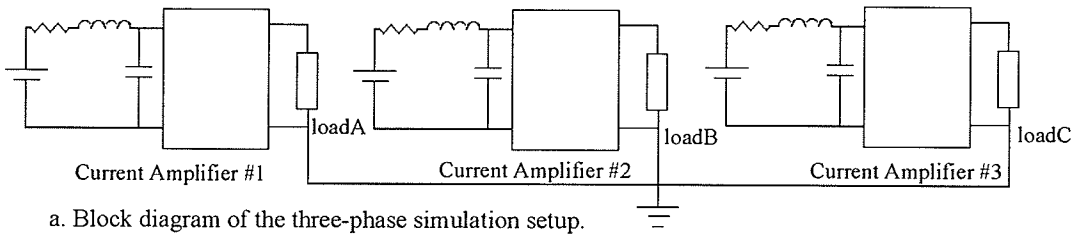
Fig. 4. 19 Maximum operating time of practical DC source using the two-level and three-level switching scheme.

4.8 Simulation of the Three-Phase Current amplifier

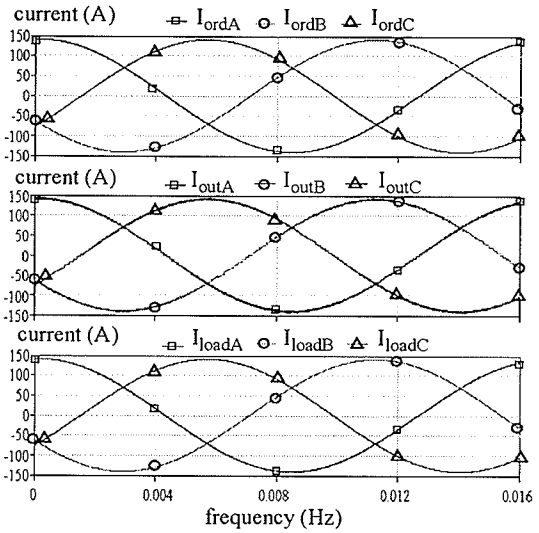
Finally, to ensure that the current amplifier design can also be applied to a three-phase application, simulations were performed using three sets of such amplifier to deliver various amount of test currents into a 0.1Ω star connected load.

A simplified diagram of the test layout is illustrated in Fig. 4.20a. The switching scheme implemented in this case is the three-level double hysteresis band technique, with the VSC output complemented by the hybrid filtering system. The resulting input (I_{ordA}, I_{ordB}, I_{ordC}), pre-filtered (I_{outA}, I_{outB}, I_{outC}), and filtered (I_{loadA}, I_{loadB}, I_{loadC}) waveforms are

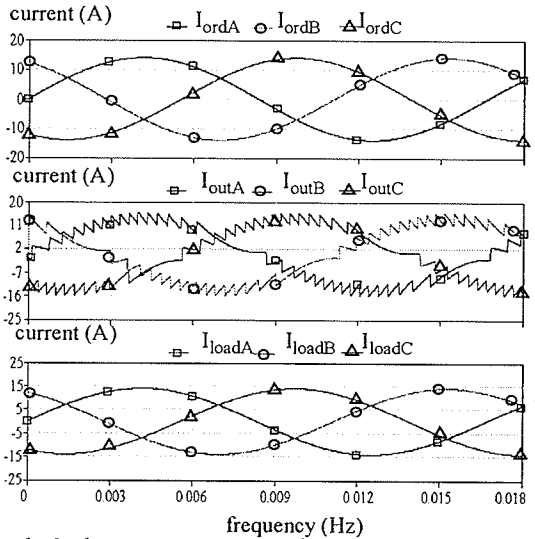
provided in Fig. 4.20b and 4.20c. As clearly shown in the simulation results, high quality three-phase transient currents can be generated by the current amplifiers.



a. Block diagram of the three-phase simulation setup.



b. 3-phase output current of $100A_{rms}$ at 60Hz.



b. 3-phase output current of $10A_{rms}$ at 60Hz.

Fig. 4. 20 Implementation and simulation results of three-phase current amplifier.

4.9 Summary of the Various Design Measures

By implementing the various design measures proposed in this chapter, the performance of a full bridge VSC can be substantially improved, to a point where it is possible to achieve the desired specifications as outlined in Chapter 2. Based on the simulation results, the effects of these design measures are summarized as follows:

- The ten-cycle rating of $100A_{rms}$ at 15V can be easily achieved with an energy storage capacitor of 0.155F if the VSC is controlled by a double band hysteresis scheme, and 0.172F if the control scheme is CRPWM.
- By using the hybrid filter, the THD, noise factor, and gain error of the $100A_{rms}$, 60Hz output waveform can be suppressed to as low as 0.09%, -53dB, and -0.007%, respectively, which are much lower than the specified ratings of 1%, -66dB, and 0.2% in some cases.
- Due to the low current cut-off scheme, high fidelity, small signal waveforms at frequency ranging from DC to 20kHz can be generated at the amplifier output. The problem of high quiescent loss during the switching operation can also be overcome.
- Finally, by executing the three-level control scheme, not only a fast acting and robust response can be achieved, the dynamic performance of the VSC can also be improved. It is clearly shown in the simulation results that the switching loss of the power converter, as well as the THD in the output waveforms, can be reduced significantly,

CHAPTER 5 Hardware Design and Experimental Results

5.1 Introduction

As discussed in the earlier chapters, the full bridge VSC (Voltage source converter), implemented with PWM (Pulse width modulation) switching technology, offers a promising design alternative to constructing a high performance relay testing current amplifier. In order to transform the VSC into such an amplifier, a number of design measures were proposed and simulated with PSCAD/EMDTC in Chapter 4. The feasibility of constructing an efficient, high fidelity current amplifier was clearly demonstrated by the positive simulation results. Consequently, based on the proposed design concepts, a single-phase prototype of the current amplifier was developed.

In this chapter, hardware considerations and circuit design issues encountered during the development of the prototype will be elaborated. Firstly, a practical schematic diagram of the full bridge VSC will be presented. A brief discussion will be provided on the selection of the power electronics components. Following that, preliminary experiment results obtained using the prototype will be presented and discussed. Finally, based on the

experimental findings, conclusion on the performance of the current amplifier will be drawn.

5.2 Final Full Bridge VSC Schematic Diagram

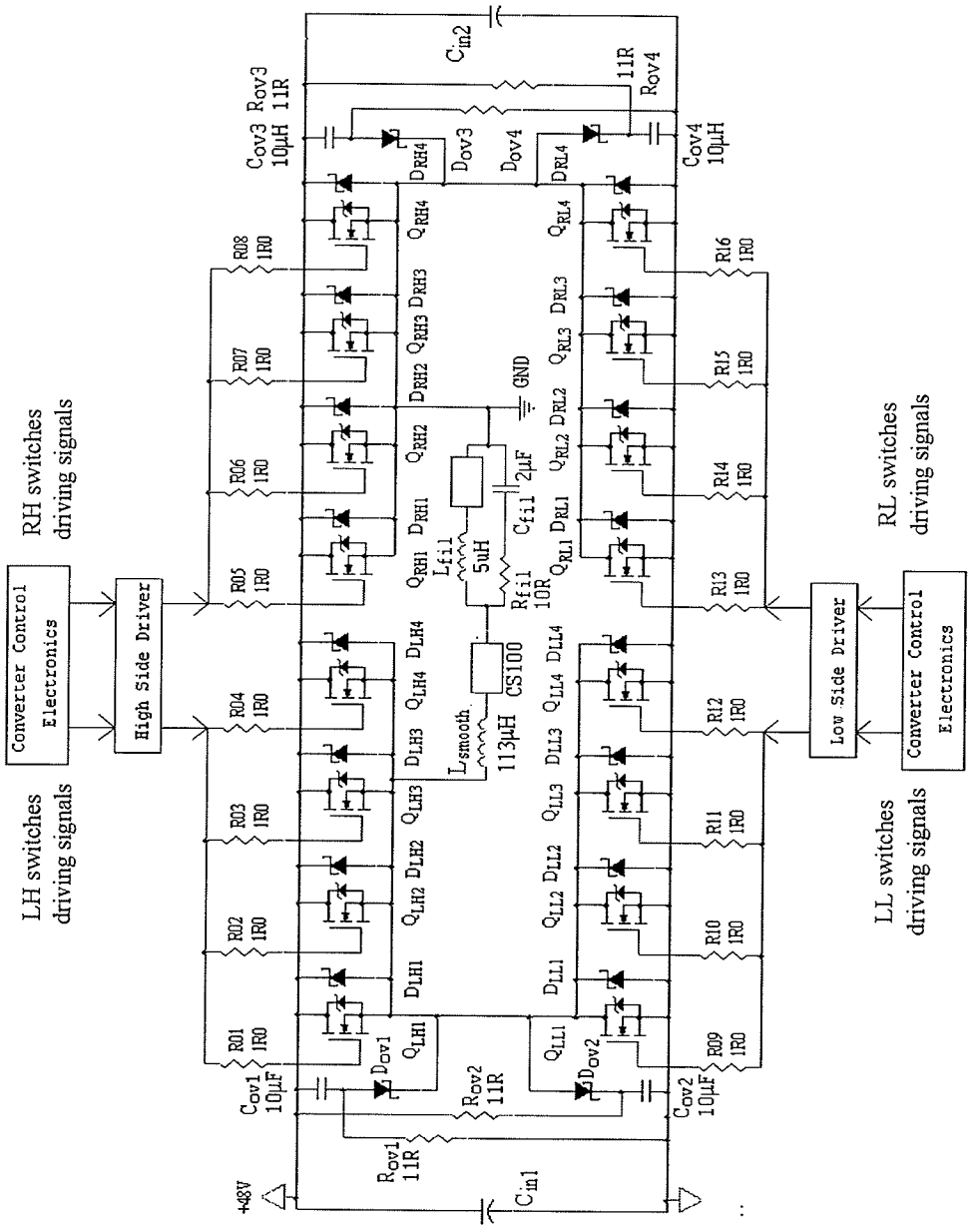


Fig. 5. 1 Schematic diagram of full bridge voltage source converter.

Based upon extensive research efforts and countless trial and error attempts, a more functional and practical schematic diagram of the full bridge VSC was finalized and presented in Fig. 5.1. As shown in the figure, in addition to the existing VSC components introduced in the previous chapters, there are several new elements implemented in the converter circuit. These hardware components will not alter the fundamental operating principle of the VSC. Rather, some of these components are essential for proper functioning of the converter, whereas others are used to alleviate the various problems encountered during the switching operation. Detailed discussions of these electrical components are provided in the following sections.

5.3 Efforts to Reduce Hardware Losses of the Full Bridge VSC

Significant improvements in overall power efficiency can be achieved with simple hardware changes. This is because most of the losses experienced in the switching converter originate from poor selection, layout, and placement of the power electronics components, as well as the circuit design.

For example, when conducting a $100A_{rms}$ current, a 0.1Ω resistive loss accumulated from improper selection of connection leads will lead to 1kW of power loss. Hence, hardware losses of the converter system need to be carefully examined and minimized. By minimizing these losses, the power requirements of the DC source and energy storage capacitors, as well as the physical size of the current amplifier, can be reduced.

Referring to Fig. 5.1, electrical components connected along high current path of the VSC contribute majority of the power loss. Detailed discussion of these components are provided as follows:

- Practical power capacitors are lossy because of their internal ESR (Equivalent series resistance). High internal losses will diminish the effective capacitance and ripple current rating of the capacitors. Hence, given the specified capacitance and voltage rating, capacitors with the lowest possible ESR should be used in the VSC circuit.

In this project, the best available off the shelf product was the 50VDC, 0.1F low loss aluminum electrolyte capacitor supplied by United Chemi-Con [47]. As shown in the schematic diagram, two such capacitors (C_{in1} and C_{in2}) were chosen and connected in parallel. The parallel connection was used to further reduce the ESR losses to 6.8mΩ and double the overall capacitance to 0.2F, so that the minimum required capacitance of 0.172F (referring to Section 4.4.4) could be obtained.

- There are two types of losses associated with the power electronics switches: static and dynamic. Using a better switching scheme, slower switching speed, or snubber circuit can reduce the dynamic losses. Similarly, using quality hardware components with lower conduction resistance can minimize the static losses.

In this project, fast switching HEXFETs from International Rectifier [48] were used in the VSC circuit. The MOSFET switches are rated for 75V and have a nominal conduction resistance of 7.8mΩ. These switches are packaged with surface mount technology (SMT),

which has a much lower parasitic resistance and inductance in the wire leads than conventional through-hole products.

Because of the positive thermal coefficient and self-compensating nature in a current sharing network, multiple units of MOSFETs can be connected in parallel without suffering the effects of thermal runaway. Hence, as seen in the schematic diagram, the parallel configuration (Q_{LH1}, Q_{RH1}, Q_{LL1}, and Q_{RL1} to Q_{LH4}, Q_{RH4}, Q_{LL4}, and Q_{RL4}) was used to further reduce the overall static losses and junction to case thermal resistance of the MOSFET switches. In doing so, assuming that the MOSFET switches have equal on-state resistance, conduction resistance as low as 3.9mΩ can be achieved.

- Although most power MOSFETs do come with an intrinsic anti-parallel pn junction diode and conduction time of the diode is extremely short during the switching operation, it is still advantageous to connect the MOSFET switches with a external freewheeling diode. This is because the parasitic body diode has much higher junction voltage and exhibits a "reverse recovery" characteristic. The higher junction voltage will bring forth higher conduction loss, while the reverse recovery condition will increase the dynamic losses and generate voltage overshoot when the diode is turned off.

By using Schottky diode (D_{LH1}, D_{RH1}, D_{LL1}, and D_{RL1} to D_{LH4}, D_{RH4}, D_{LL4}, and D_{RL4}), which in general has a much lower on-state voltage than an equivalent rating junction diode, the conduction loss resulting from the body diode of the MOSFET can be further reduced. Since the Schottky diodes are majority-carrier devices, they can be switched on and off faster because there are no stored minority carriers that must be injected into the

device during turn-on and pulled out during turn-off. The various reverse recovery problems associated with the pn junction diodes can also be addressed because the operation of the Schottky diodes does not involve minority carrier charges.

- The design of the slew rate limiting and filtering inductors (L_{smooth} and L_{fil}) is discussed in Section 5.4.2.2. Since these inductors contribute most of the power loss during the VSC switching operation, their design parameters should be carefully examined. To illustrate this, consider that the overall power loss of the inductors used in the prototype is approximately 130W when conducting a current of $100A_{rms}$ at 480Hz. The power loss of 130W is roughly 54% of the VSC static losses during the switching operation.

- There are a number of devices that can be used to measure both AC and DC current waveforms: resistive current shunt, coaxial shunt, closed-loop Hall effect current sensor, and DCCT (DC current transformer). In this project, a closed-loop Hall effect current sensor (CS100) was used in the VSC circuit. Due to its extremely low insertion loss, the power loss generated by the Hall effect sensor can be considered as negligible.

- In the hardware prototype, the various high current components were connected with soldering leads, quick-connect snap-in connectors, and terminal blocks via hook-up wires or PCB (Printed circuit board) traces. In order to reduce the amount of conduction loss and voltage spikes during the switching operation, the stray resistance and inductance resulting from the connection must be minimized. This was achieved by placing all the high current components in closed proximity, making the interconnecting wires as thick

and as short as possible, using connectors with high current rating, and fabricating the PCB with gold plated and heavily weighted traces for the high current paths.

- Finally, it is impractical to obtain the actual converter power losses through analytical calculations or simulation. There are too many unknown parameters, such as dynamic characteristics of the semiconductor switches, imperfections in the electrical components, impedance variations due to temperature and mechanical stresses, and high frequency skin effects. Hence, in order to assess the actual performance and efficiency of the current amplifier, the best approach is to conduct the physical tests by using the hardware prototype.

5.4 PWM Current Amplifier Hardware Design Considerations

In the following sections, hardware design considerations contributing to the successful construction of the current amplifier are discussed. These practical issues include the selection of a suitable current measuring device, the design of filter inductors, the selection of the DC power supplies, the selection of snubber circuits, and the requirements of the active filter design.

5.4.1 Selection of Current Measurement Device

The objective of the current amplifier is to deliver an output current closely resembling the input reference signal. This requires an accurate measurement of the output current waveforms, which conformity with the reference generates the firing order for the switching controller of the VSC. Any discrepancy between the actual load current and the

measured waveform will produce undesired phase and amplitude errors. Hence, it is important to implement a current sensor that is accurate and fast acting.

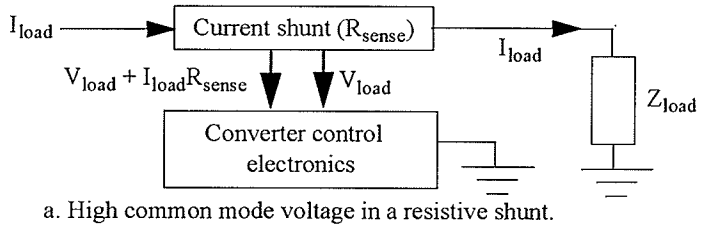
There are a number of devices that can be adopted for current measurement applications, the simplest being a shunt resistor. Ideally, any current flowing through the resistor will develop a voltage directly proportional to the current magnitude. The generated voltage signal can be scaled up or down according to the actual current level by using a gain adjusting buffer.

Though it is easy and cost effective to implement, such a resistive shunt has several shortcomings. Firstly, insertion loss of the resistive element will lower the overall power efficiency of the amplifier. If the resistance is reduced to minimize the losses, inherent parasitic inductance of the current shunt will become a dominant factor to affect accuracy of the current measurement. The resulting low voltage signal obtained from the current shunt is also susceptible to noise and requires additional filters and amplifiers for further processing. Finally, since the resistance of the current shunt is dependent on the temperature and the mechanical mounting stresses, it will be difficult to obtain a highly stable and accurate measurement.

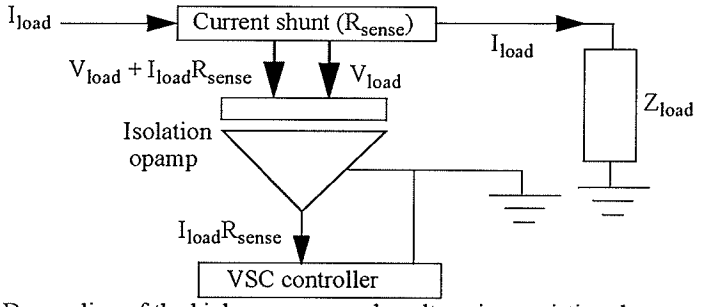
It is possible to construct the resistive element into a loop or coaxial configuration, thereby reducing the effects of parasitic inductance while retaining a low resistance value. The coaxial shunt, for example, has a frequency bandwidth of at least several MHz and is capable of measuring currents in the range of several kA. However, the cost of such

device is much higher than the simple resistive shunt, because it demands a more complicated construction technique and precision signal processing circuit.

Due to the direct-coupling connection, high frequency emi (electromagnetic interference) noise resulting from the switching operation can propagate to the control electronics of the VSC via the current shunt. Furthermore, as shown in Fig. 5.2a, if the voltage across the current shunt exceeds the common-mode voltage rating of the control electronics, it will saturate or even damage the low power circuit components.



a. High common mode voltage in a resistive shunt.



b. Decoupling of the high common mode voltage in a resistive shunt.

Fig. 5. 2 Isolation of current measurement device.

As a result, a dedicated isolation channel, implemented using an isolation operational amplifier as illustrated in Fig. 5.2b, is required to decouple the measured signal from the current shunt. However, the isolation circuit will increase overall complexity and cost of the current shunt, limit frequency bandwidth of the output waveform, and introduce additional measurement error.

Current transducers such as current transformer, DCCT (DC current transformer), Rogowski coil, and Hall effect sensor are often preferred whenever extensive isolation is needed. Though based on different working principles, constructions of these transducers are similar: a magnetic core wound with a primary and secondary winding, with the current to be measured passing through the primary winding and a scaled down representation of the primary current reflected in the secondary winding. Since both windings are electrically isolated from one another, the purpose of signal decoupling can be achieved.

The measurement device used in this project was a closed loop Hall effect sensor. There are numerous benefits for using such a sensor: low cost, extremely low insertion loss, off the shelf availability, ease of implementation, fast response, highly linear output, capability of measuring pure DC current, and isolation from the primary circuit. The current sensor is based upon the Hall effect theory, which states that when a current carrying conductor is placed in a magnetic field, a voltage perpendicular to the direction of the field and the flow of the current is generated, as depicted in Fig. 5.3 and Eqn. 5.1.

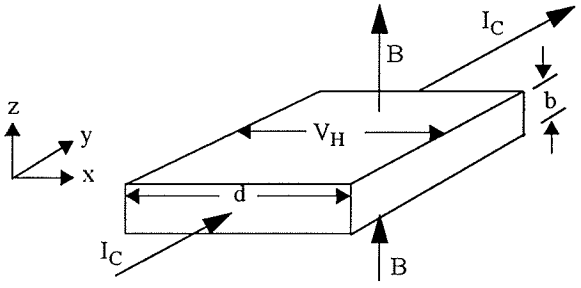


Fig. 5. 3 Hall effect theory illustration.

$$V_H = k \times I_C \times B\sin\theta \qquad \text{(EQ 5.1)}$$

Here V_H is the Hall effect voltage, k is a constant dependent on the geometry of the current carrying conductor (Hall element), the ambient temperature, and the mechanical stress on the element. I_C is the magnitude of the control current, and Bsinθ is the component of the magnetic field perpendicular to the Hall effect voltage. In a typical closed loop Hall effect sensor, I_C is maintained at constant level. Hence, the Hall voltage will be proportional to the strength of the applied magnetic field.

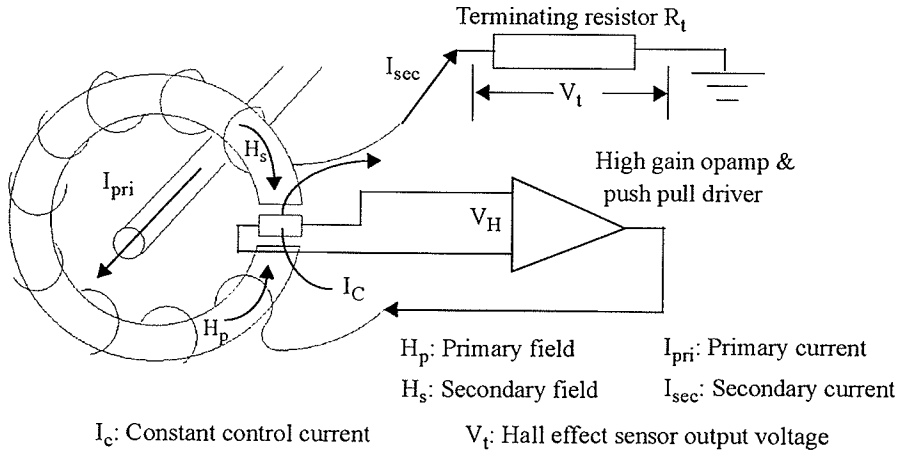


Fig. 5. 4 Simplified circuit diagram of closed loop Hall effect current sensor.

A simplified circuit diagram of the closed loop current sensor is provided in Fig. 5.4. The magnetic core is gapped and inserted with a Hall effect element. The current to be measured (I_{pri}) flows through the primary winding and produces a magnetic flux proportional to the current magnitude. At the same time, the output of the Hall element, bolstered by a high gain push-pull driver, drives the secondary coil with current I_{sec} in an attempt to balance the flux produced by the primary current. The secondary winding is

wound in series opposition on the magnetic core to achieve the purpose of flux cancellation. Consequently, the total flux in the magnetic core will be maintained at near zero level, and I_{sec} will be a scaled down representation of I_{pri}, with its magnitude decided by the turn ratio of the windings.

By using the closed loop configuration, the effects of non-linearity and saturation in the magnetic core can be eliminated, and the temperature sensitivity in the Hall effect element can be reduced. The sensor must be terminated with a resistor, thus converting I_{sec} to voltage (V_t). The resistor value should be selected such that V_t will not exceed the output rating of the push-pull driver. Finally, the equation of V_t is given as:

$$V_t = I_{sec} \times R_t = \frac{N_{pri}}{N_{sec}} \times I_{pri} \times R_t \qquad \text{(EQ 5.2)}$$

where R_t is the terminating resistance, and N_{pri} and N_{sec} are the respective turn number of the primary and secondary windings.

5.4.2 Design of Slew Rate Limiting and Filtering Inductors

The full bridge VSC requires two inductors to operate: the slew rate limiting inductor (L_{smooth}) and the filtering inductor (L_{fil}). The selection criteria of suitable magnetic cores, as well as the inductor design procedure, are discussed in the following sections.

5.4.2.1 Selection of Inductor Cores

Considering the available types of core material: air, iron alloy (magnetic steel), ferrites, powder irons, and amorphous alloy, and the wide variety of core shapes and sizes: toroids,

gapped toroids, pot cores, rob cores, U cores, E cores, I cores and RM cores, selecting a suitable magnetic core for inductor design can be somewhat confusing. Hence, to simplify the selection process in this project, a general guideline based on the following criteria was adhered to:

- The magnetic cores used to construct the inductors must achieve the specified inductance values. Practical magnetic-core inductors are nonlinear and will saturate if subjected to a high DC bias current. The saturation is caused by alignment of the microscopic magnetic moments under the presence of strong magnetic field created by the DC bias current. Hence, the constructed inductors should be able to tolerate a high current stress without being substantially saturated.

- The inductors should be reasonably lightweight and of a small size, so that the current amplifier will have a compact profile after incorporating these inductors. Additionally, the assembly of the inductors should be straight forward, in the sense that recoiling and modification of the turn number can be performed easily.

- Finally, and most importantly, the cost and availability of the magnetic cores should be factored into the selection considerations. High power magnetic cores are often expensive and require special ordering and long lead-time for custom fabrication. Hence, it is cheaper and more convenient to obtain cores that are in common use, even if these cores might only loosely fit the desired specifications.

By using the above selection criteria, the best option was to use the powder iron toroidal cores manufactured by Magnetic Inc. [49]. These powder iron cores were fabricated with distributed air gaps technology, which improves the core performance substantially by having a much lower eddy current loss and a higher operating current rating without leading to saturation. Coupled with the advantage of having a low leakage flux with a toroidal shape, the magnetic cores are particularly suitable for high current and high frequency switching converter applications.

5.4.2.2 Design Procedure of Filtering Inductor

Though possible to implement with an analytical approach, it is more convenient to design the inductors by utilizing the formulas and empirical data [50] compiled from the core manufacturer, Magnetic Inc. The detailed procedure of designing the filtering inductors (L_{smooth} and L_{fil}) is discussed below:

- The first step is to compute the required power handling capacity of the magnetic core, LI_{DC}^2, where L is the inductance (mH) and I_{DC} is the DC bias current (A). The correct core size can be located from the core selector charts compiled by the core manufacturer using the computed power capacity value.

- Once the core has been selected, the estimated turn number of inductor winding can be calculated by using Eqn. 5.3 and the Al value ($nH/turns^2$) provided from the core data sheet. The Al value of a magnetic core is defined as the amount of inductance (nH) that can be obtained for every square number of winding turns.

$$N = \sqrt{\frac{L}{AL}} \qquad \text{(EQ 5.3)}$$

- DC magnetizing force H (Aturn/cm) of the inductor can be acquired from Eqn. 5.4:

$$H = 0.4\pi \times N \times \frac{I_{DC}}{l_e} \qquad \text{(EQ 5.4)}$$

where N is the turn number of the winding, I_{DC} is the DC bias current (A), and l_e is the effective path length (cm) of the inductor. The permeability loss of the inductor, due to the high DC bias current, can be obtained by using the permeability versus DC bias curves of the chosen inductor core. Subsequently, the saturated inductor value can be estimated.

- In order to keep the copper loss to a minimum, magnet wire with the biggest conductor size should be used to wind the inductor core. However, if the conductor size gets bigger, it will become stiffer to bend, thereby causing the problem of core winding. Fortunately, the winding problem can be overcome by using multiple parallel-connected conductors with finer core size. The resulting wire is more flexible, but has the same conduction loss of the original single core wire. By referring to the property table of the magnet wire, the estimated winding resistance of the inductor can be obtained.

- Given the calculated magnetizing force value, the corresponding flux density of the magnetic core can be obtained from its magnetization curves.

Base on the above procedure and the core datasheet obtained from the manufacturer, the specifications of the inductors used in this project are provided in Table 5.1:

Table 5.1. Specifications of filtering inductors.

Descriptions	L_{smooth}	L_{fil}
Output Rating	141A	141A
Inductance	108μH	5μH
LI_{DC}^2	2147mHA^2	99mHA^2
Best Available Core	HI-FLUX 58908-A2	HI-FLUX 58550-A2
Permeability	26	26
Al value	27nH/turn^2	28nH/turn^2
Winding turn number	54	14
Effective path length (l_e)	19.95cm	8.15cm
DC Magnetizing force (H)	480Aturn/cm	30Aturn/cm
% of Initial permeability at 141A	31.1%	51.2%
Inductance at 141A	33.6μH	2.56μ
Winding wires	2x12awg magnet wires	2x13awg magnet wire
Resistance of the winding wires	0.00261Ω/m	0.00328Ω/m
length/turn of the winding wire at 20% window factor	6.8cm/turn	3.91cm/turn
Winding resistance	9.58mΩ	1.80mΩ
Copper loss at 141A	95.8W	18W
Flux Density	0.732 Tesla at 480Aturn/cm	0.528 Tesla at 30Aturn/cm
Core loss density at 141A, 480Hz	325mW/cm^3	144mW/cm^3
Nominal core volume	45.3cm^3	5.48cm^3
Worst case core loss	14.72W	0.79W
Total Operating Loss	110.52W	18.79W

5.4.2.3 Final Notes on the Inductor Construction

As discussed in previous sections, the design measures of implementing toroidal shaped and distributed air gap cores were adopted in order to contain the leakage flux of the inductors. However, operating at very high flux density, these inductors are still a major source of magnetic interference. Consequently, in the hardware design, the high power inductors were enclosed in magnetic shielding material and mounted at a far distance from the Hall effect sensor, analog interface circuit of the amplifier, and control electronics of

the VSC. By adopting such preventive measures, the interference noise induced by the magnetic field of the inductors can be minimized.

5.4.3 Requirements of Power Supply

The DC power supplies used in the current amplifier prototype were selected to satisfy the following conditions:

- Switch mode power supplies are extremely efficient when compared to their analog counterparts of equivalent rating. Consequently, these supplies have a much smaller profile and lower price tag. When these power supplies are incorporated into the amplifier design, significant saving in size, weight, and cost can be achieved.

- In this project, the continuous power rating of the current amplifier is 159W ($15A_{rms}$ at 15V) for the VSC and 60W (8A at 15V) for the analog current source. Upon considering operating losses, the rating of the power supplies must exceed these values. In addition, the DC supply of the VSC must be capable of withstanding frequent charge-discharge actions of the energy storage capacitors during the switching operation.

- If the output current of the power supply exceeds its nominal rating, overload protection will be activated to protect the supply from damaging. In this project, the constant current control is a preferred protection scheme to limit the capacitor inrush current and the high current surge during the injection tests. The protection scheme operates by reducing the supply voltage during the overloading conditions, in an attempt to keep the supply current below its maximum rating.

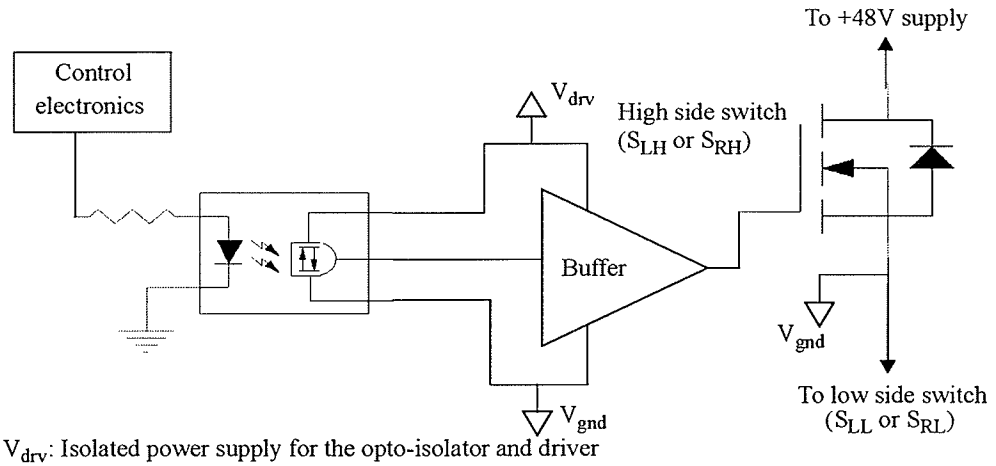
- Finally, as discussed in Section 3.3.3, in order to prevent DC side short circuit, it is also necessary to use a power supply with an electrically isolated output in the VSC circuit.

In addition to the high power DC supplies, the current amplifier also requires other low power sources to support proper functioning of its measurement and control circuits. Off the shelf switching power supplies with adequate ratings were selected for this purpose.

5.4.4 Discussion of MOSFET Driver Circuit

In order to turn on and off the MOSFET switches, a driving voltage in the range of 10V to 15V and 0V to 1.5V, respectively, needs to be applied across the GS (gate and source) terminals of the MOSFET. Referring to Fig. 5.1, the MOSFET switches (Q_{LH1}, Q_{LL1}, and Q_{RL1}) are generally not referenced to the ground potential. Thus, the driving signals issued from the control electronics have to be floated at the same potential of the source terminal. This can be accomplished by using dedicated gate drive circuit incorporating opto-isolators, charge pump controllers, or isolation pulse transformers.

Due to the ease of implementation and its extremely fast response, the opto-isolation approach was adopted in this project. As shown in Fig. 5.5, the centerpiece of such a design approach is the opto-isolator IC (Integrated circuit), which consists of an input LED (Light emitting diode) and an optical sensing unit. A high current gate drive buffer is also required to source and sink the gate charges of the MOSFET in the shortest possible time, so that the performance of high-speed switching can be achieved.



V_{drv}: Isolated power supply for the opto-isolator and driver
V_{gnd}: Ground return for the isolated power supply

Fig. 5. 5 Block diagram of opto-isolation driver.

As shown in the above figure, the LED and the optical sensing unit are both electrically isolated, and so does the DC source used to power the sensing unit and its output buffer. As a result, the output of the opto-isolator driver can be referenced to any potential and conveniently used to control any of the MOSFET in the VSC circuit.

The operating principle of the driver circuit is straightforward. If it is required to turn on the MOSFET, the control electronics will first assert a logic signal to activate the appropriate LED of the opto-isolator. Upon detecting the LED signal, the optical sensor responds by applying a gate drive voltage across the GS terminals of the MOSFET to turn on the switch. Conversely, as soon as the control electronics deactivates the LED driving signal, the optical sensor will cause the buffer to sink the gate charges of the MOSFET, thereby resulting a zero voltage applied across its GS terminals and forcing the switch to turn off.

5.4.5 Snubber Circuit Design

There are three basic types of snubber circuits, namely turn-on, turn-off, and overvoltage snubbers, which can be applied to improve switching performance of the MOSFET. The turn-on and turn-off snubbers are used to reduce the dynamic switching losses of the MOSFET, and the overvoltage snubber is used to suppress the high voltage stresses across the switch.

5.4.5.1 Practical Switching Waveforms

As shown in Fig. 5.6a, a practical VSC always has stray inductors (L_1 to L_9) in various parts of the circuit. To illustrate the effects of these inductors, the turn-on and turn-off processes of Q_{LL} are described below with some simplified assumptions.

The typical turn-off waveforms are illustrated in Fig. 5.6b. Initially, Q_{LL} is conducting the load current (I_{load}). If the MOSFET is turned off at t_0, the voltage across its drain and source terminals (V_{DS}) will begin to rise. When V_{DS} exceeds VDC at t_1, the freewheeling diode (D_{LH}) is forward biased, and it will start to conduct current. Due to the commutation of I_{load} to the diode, the MOSFET current (I_{DS}) will begin to decrease at a rate dictated by the properties of Q_{LL} and its gate driver. In this case, V_{DS} can be expressed as:

$$V_{DS} = VDC - L_{SUM} \times \frac{dI_{DS}}{dt} \qquad \text{(EQ 5.5)}$$

where L_{SUM} is the total value of the stray inductors along the path of I_{DS}.

Due to the decrease of I_{DS}, the value of $L_{SUM}dI_{DS}/dt$ is negative. Thus, an overvoltage beyond VDC is induced by the stray inductors, until I_{DS} drops to the zero level at t_2. If V_{DS} exceeds the maximum drain-source rating of Q_{LL} during the turn-off process, it will result in avalanche breakdown of the MOSFET's body diode and invite catastrophic failure to the VSC operation.

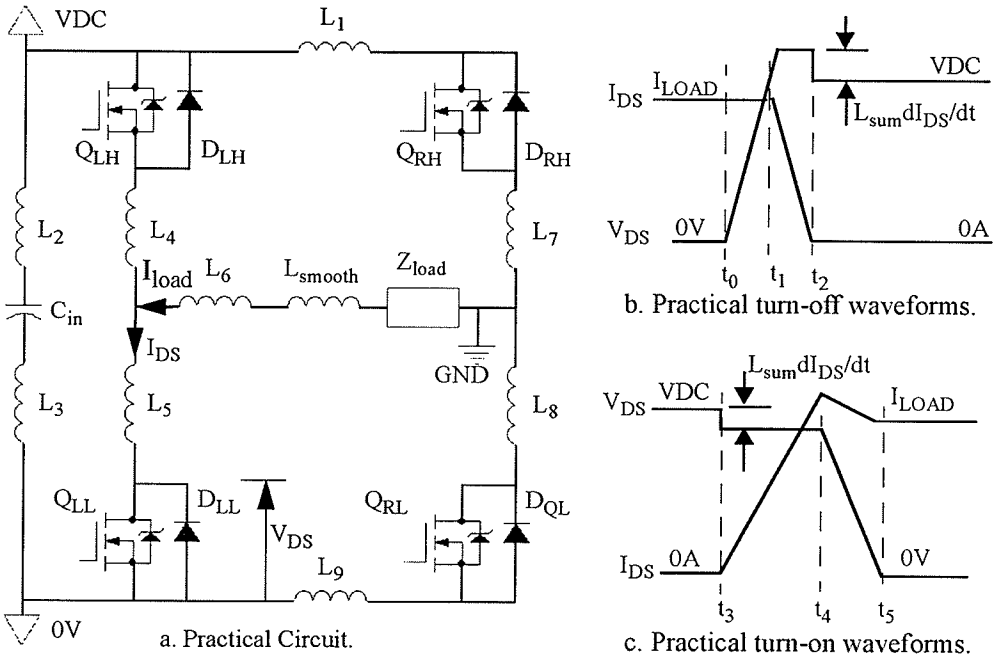


Fig. 5. 6 Practical VSC circuit and its switching waveforms.

As shown in Fig. 5.6c, if Q_{LL} is turned on again at t_3, I_{DS} will begin to rise at a rate dictated by the MOSFET properties and its gate driver. Due to the increase of I_{DS}, the value of $L_{SUM}dI_{DS}/dt$ is positive, and the resulting V_{DS} is less than VDC according to Eqn. 5.5. Because of the reverse recovery characteristic of D_{LH}, I_{DS} continues to rise above I_{load}, until the freewheeling diode recovers at t_4. At this moment, V_{DS} will start to

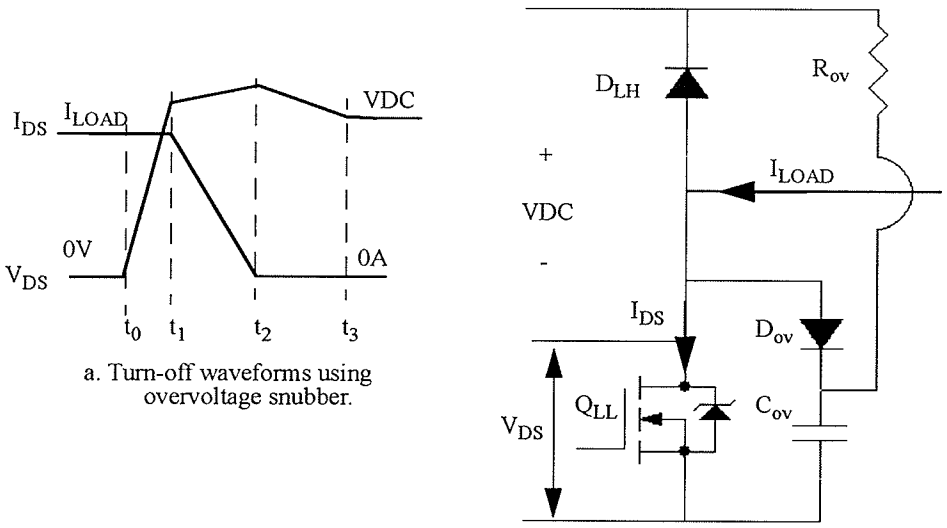
decrease at a rate decided by the device properties, and it will return to its steady state value of 0V at t_5.

As shown in the switching waveforms, there is a brief moment when Q_{LL} has to conduct I_{DS} while being subjected to a nonzero voltage, thereby causing a high instantaneous power loss during the switching transitions. The power loss, which is the product of I_{DS} and V_{DS}, is proportional to the switching frequency of the VSC. Furthermore, there are also overvoltage and overcurrent stresses resulting from the turn-off and turn-on process, respectively. Hence, snubber circuits should be implemented to improve the dynamic performance of the VSC switching operation.

5.4.5.2 Implementation of Overvoltage Snubber Circuit

Due to the presence of stray inductance and fast switching of current as high as 141A, significant overvoltage spikes and the resulting oscillation will be generated during the VSC switching operation. Hence, in order to protect the switching devices, overvoltage snubber circuits as seen in the schematic diagram of Fig. 5.1 were implemented in the VSC circuit.

Operating principle of the overvoltage snubber circuit can be explained by using the switching example of Q_{LL}. As illustrated in Fig. 5.7a, prior to the turning off of Q_{LL}, the snubber capacitor (C_{ov}) of Fig. 5.7b is charged to the bus voltage level (VDC). If Q_{LL} is turned off at t_0, V_{DS} will begin to rise rapidly. If the value of V_{DS} is higher than VDC, the freewheeling diode D_{LH} will be forward biased, and it will start to conduct current at t_1.



a. Turn-off waveforms using overvoltage snubber.

b. Overvoltage snubber Circuit.

Fig. 5. 7 Overvoltage snubber circuit and its waveforms.

The RCD (Resistor, capacitor, and diode) snubber circuit of Fig. 5.7b is essentially a voltage clamp for Q_{LL}. If V_{DS} is higher than VDC, the snubber diode (D_{ov}) will be forward biased, and the energy trapped within the stray inductors of the VSC circuit will be diverted toward charging C_{ov}. The charging of C_{ov} continues until I_{DS} drops to zero and D_S stops conducting at t_2. Subsequently, the capacitor discharges its built-up voltage through the snubber resistor R_{ov} to the DC supply rail. The time constant $R_{ov}C_{ov}$ should be small enough to allow the capacitor voltage to return to VDC at t_3 before the next turn-off process.

It is clearly shown in the improved switching waveforms of Fig. 5.7b that the voltage overshoot can be reduced by utilizing the voltage clamping snubber circuit. Due to the unknown stray inductance value, the analytical design of the snubber is difficult. Hence,

the values of R_{ov} and C_{ov} were obtained from laboratory experiments, and they were found to be 11Ω and 10μF, respectively.

5.4.6 Requirements of Current Source

As discussed in Chapter 4, analog current source is required in the amplifier design to compensate the switching error and to provide the high quality output waveforms at low current level. In order to achieve the best error canceling results, the current source must have good accuracy, high frequency responses, and minimum phase delay, and it should remain stable when subjected to external disturbances, such as the load value changes or supply voltage fluctuation.

The current source can be constructed using a number of analog designs, such as the modified Howland current pump, current mirror, and conventional class AB amplifier. In this project, the design approach of utilizing a high power operational amplifier in conjunction with a negative feedback controller was considered. The monolithic power opamp was chosen because it would simplify the design process, by saving the time and efforts used to design a high current output stage and its biasing circuit. By implementing the negative feedback design with PI (Proportional and integrated) compensation, it ensures that the analog current source will provide a precise, high-speed output response to perform the task of noise cancellation.

5.5 Performance Evaluation of the Current Amplifier

A working unit of the single-phase current amplifier, based upon the block diagram of Fig. 5.8, was successfully constructed in the laboratory. The hardware prototype consists of several power supplies and four modules. The four modules are: a full bridge VSC to efficiently deliver the high level switching current, an analog current source and a passive filter to compensate the switching error and provide high frequency waveforms at low level current, a DSP based controller to implement the switching algorithm and provide the driving signals for the MOSFET switches, and an analog interfacing unit to perform various conditioning and scaling tasks for the amplifier signals.

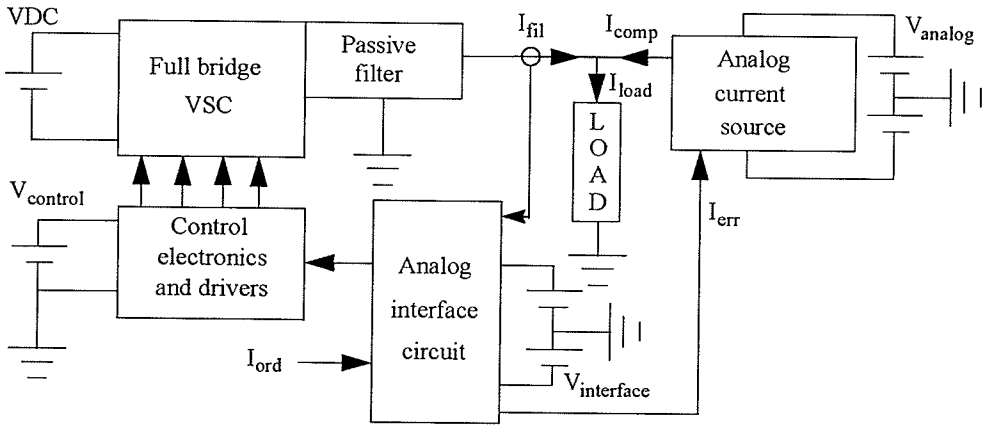


Fig. 5. 8 Block diagram of current amplifier

The control module was programmed with the two-level CRPWM control scheme using a 5A hysteresis bandwidth. The low current cut-off control scheme was also incorporated into the switching operation, with the turn-on and turn-off thresholds specified at +/-8A and +/-5A, respectively.

By implementing the various design measures, the current amplifier prototype was found to be capable of generating a wide range of high fidelity transient current waveforms: ranging from a few mA to as high as $100A_{rms}$ at frequency of DC to 20kHz. To illustrate examples of these output waveforms, the oscilloscope screenshots of the current injection tests are presented as follows.

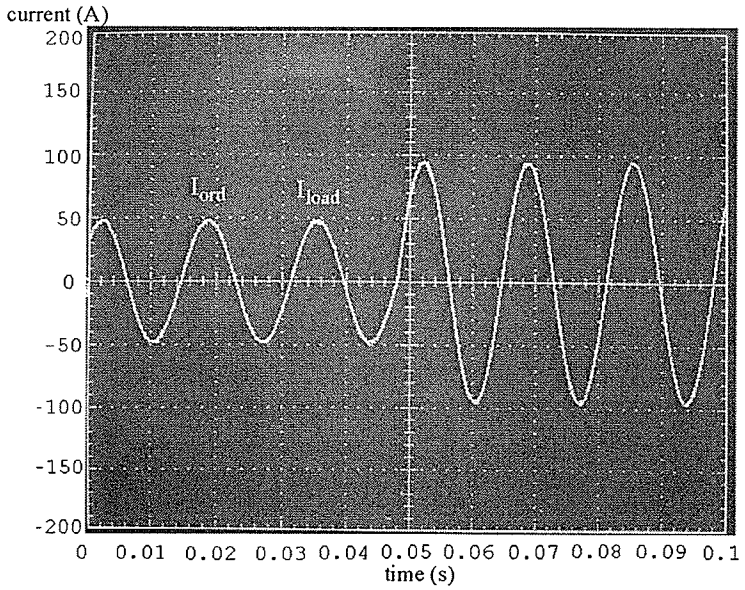
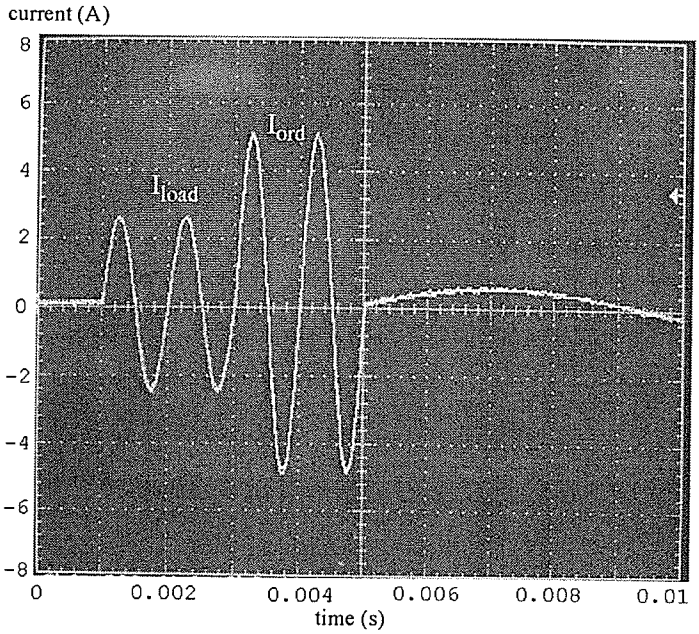
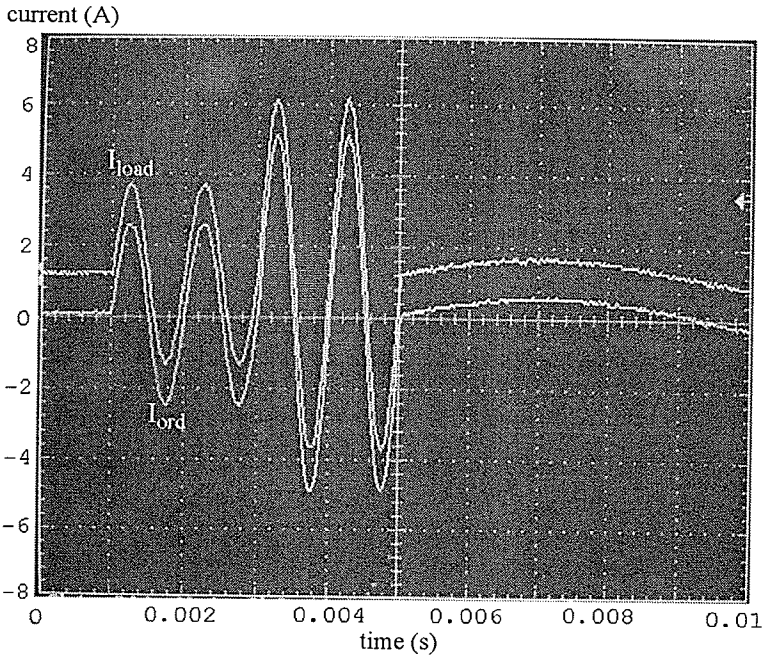


Fig. 5. 9 Experiment results of generating 48A, 95A at 60Hz.

The test results of injecting currents of 48A, 95A at 60Hz into a SEL protective relay are presented in Fig. 5.9. The two overlapping waveforms shown in the figure are the input reference signal (I_{ord}) generated by the RTP (Real time playback) system and measured output waveforms (I_{load}) obtained from a current probe. It is clearly shown that these two waveforms are almost identical. The test results also confirm the effectiveness of the hybrid filtering system, as the switching noise resulting from the converter operation is barely noticeable in the output waveform.



a. Overlapped input and output waveforms.



b. Input and output waveforms with an offset.

Fig. 5. 10 Experiment results of generating 2.5A, 5A at 1kHz.

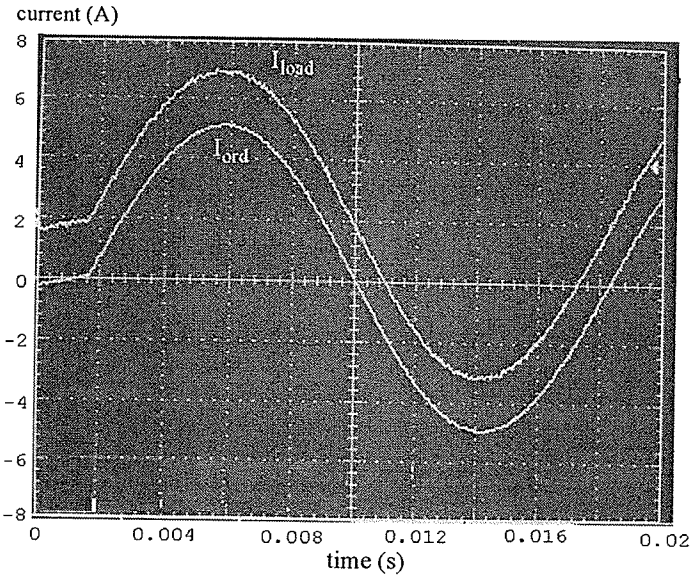
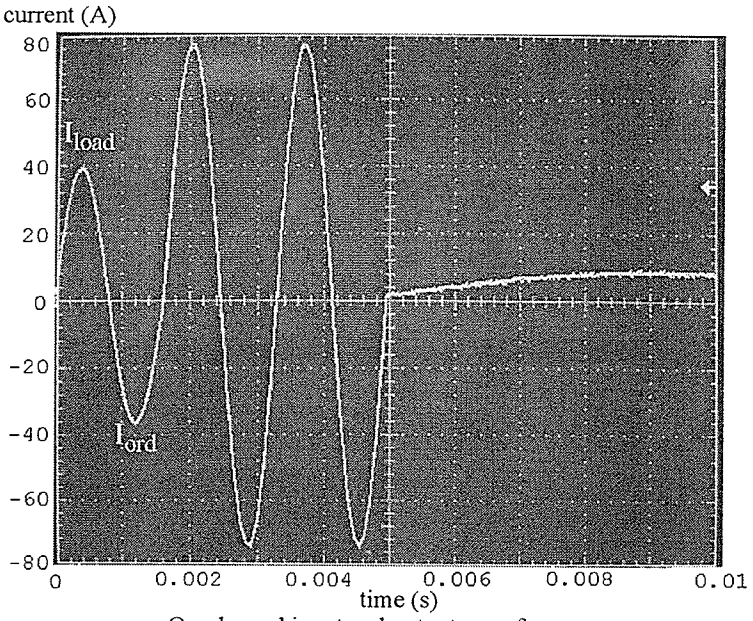


Fig. 5. 11 Experiment results of generating 5A at 60Hz.

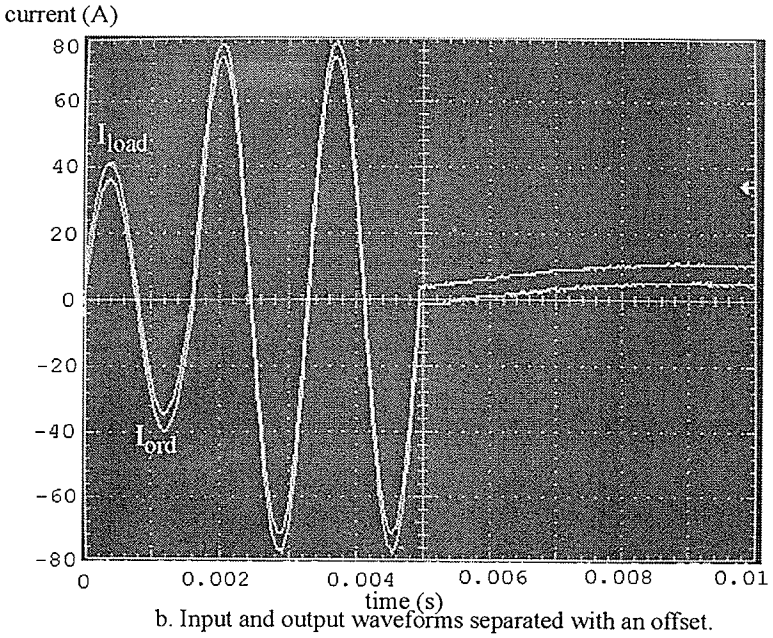
Both Fig. 5.10 and 5.11 show the test results of generating low level currents into the SEL relay. Due to the low current cut-off scheme, the output currents of 2.5A, 5A at 1kHz and 5A at 60Hz were drawn entirely from the analog current source. As seen in the simulation results, the resulting output waveforms (I_{load}) are exactly equal to the input waveforms (I_{ord}). As shown in Fig. 5.10b and 5.11, the input and output waveforms are purposely separated with an offset in the oscilloscope. It is clearly shown that the load current waveforms (I_{load}) are of high quality and free of any switching ripple. Thus, base on these experiment results, it is demonstrated that the current amplifier can produce highly accurate and low noise output waveforms at the small signal level.

The test results of delivering currents of 38A, 75A at 500Hz into the SEL relay are provided in Fig. 5.12. Fig. 5.13 illustrates the input (I_{ord}) and output (I_{load}) waveforms of

Fig. 12 in detail by using a smaller time scale. The two waveforms are presented overlapped, as well as separated vertically, in order to illustrate their differences.



a. Overlapped input and output waveforms.



b. Input and output waveforms separated with an offset.

Fig. 5. 12 Experiment results of generating 38A and 75A at 600Hz.

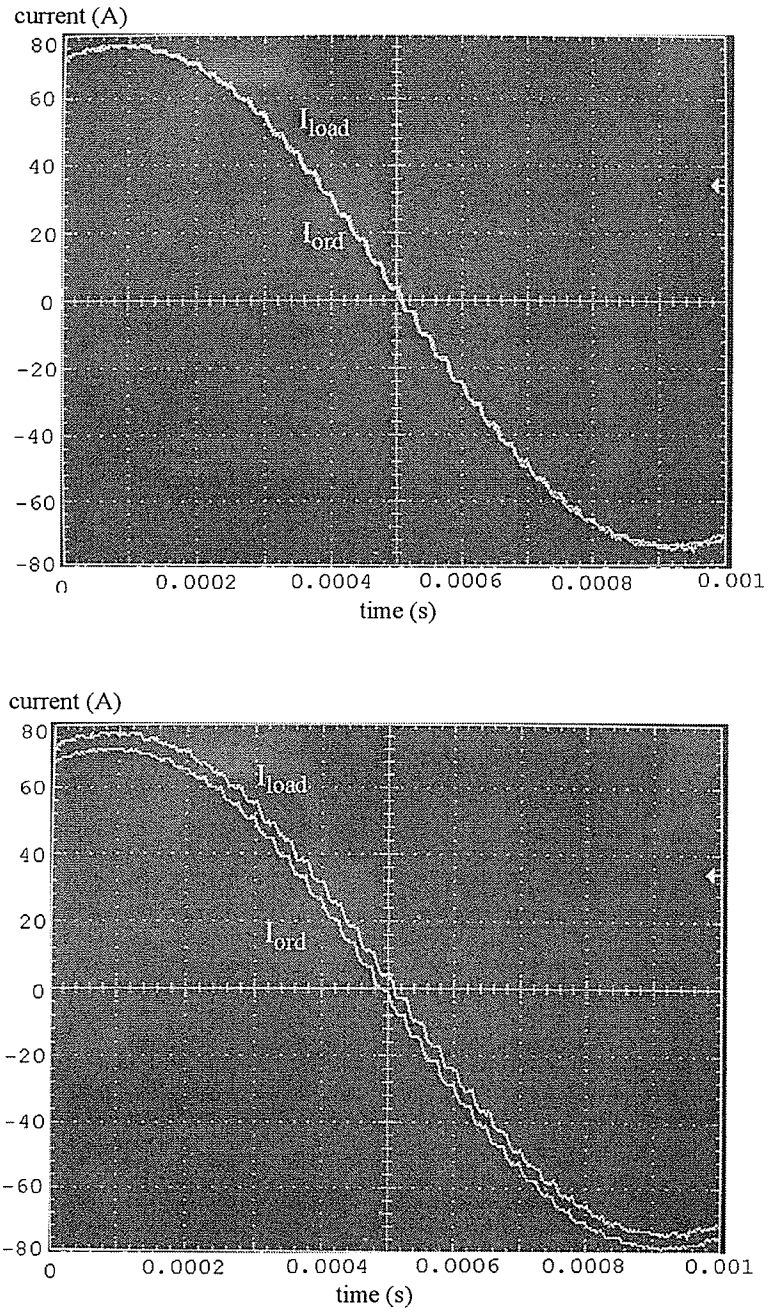


Fig. 5. 13 Experiment results of generating 38A and 75A at 600Hz, with smaller time scale.

As demonstrated by the experiment results, the current amplifier is able to deliver high current output at frequency as high as 500Hz. The measured load current waveform (I_{load})

is almost identical to the input reference signal (I_{ord}). Furthermore, notice that the high frequency ripple contained in the input reference signal, which is the D/A (Digital to Analog) converter noise introduced by the RTP system, can also be reproduced faithfully by the current amplifier.

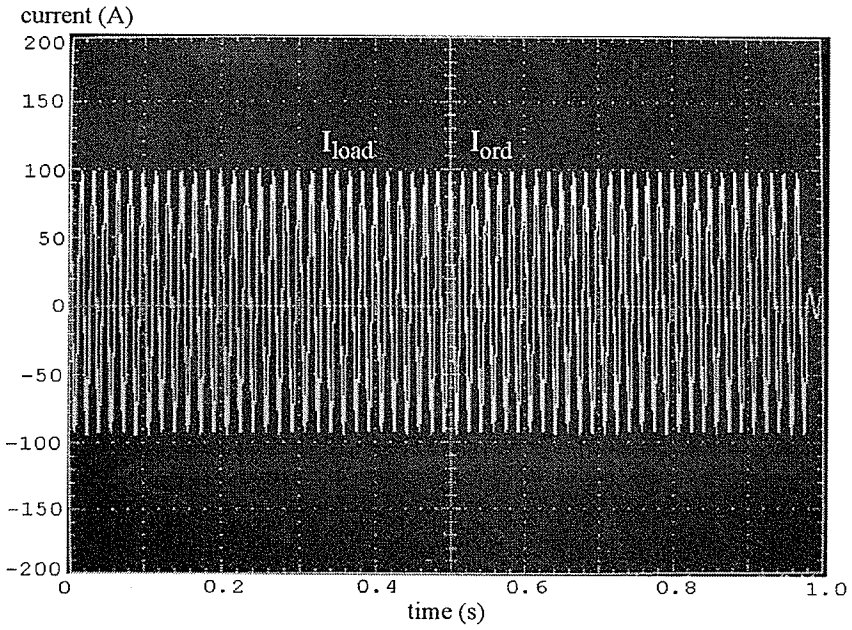


Fig. 5. 14 Experiment results of generating 95A at 60Hz for 1 second.

Finally, in order to demonstrate the capability to produce high level transient current for a substantial duration, a current of 95A at 60Hz was successfully generated by the current amplifier and injected into a short circuit load for one second. The resulting input (I_{ord}) and output (I_{load}) waveforms are presented in Fig. 5.14.

Preliminary experimental results of the PWM current amplifier, as seen from the above figures, are encouraging. By utilizing the PWM switching technology, the current amplifier was capable of generating a wide range of output current. The load current

waveforms were almost a replica of their input reference signals with barely noticeable switching noise. Moreover, high current output was produced to a short circuit load for a substantial duration. Thus, the purpose of constructing a proof-of-concept current amplifier suitable for relay testing applications has been achieved.

CHAPTER 6 Conclusion

6.1 Conclusion

The research objective of this thesis is to develop a relay testing current amplifier to serve as the output stage of a digital power system simulator. The amplifier was designed based on the PSCAD/EMTDC simulations. The simulations demonstrated that a highly efficient current amplifier could be developed by utilizing full bridge voltage source converter and several design measures, which include implementation of energy storage capacitor, execution of the CRPWM or three-level switching technique, incorporation of active and passive filtering system, and adoption of the low current cut-off control scheme.

Based on the design concepts and simulation results, hardware prototype of the current amplifier was successful constructed. The amplifier was tested to be capable of delivering high quality current output of up to $100A_{rms}$ with a frequency response of DC to 20kKz, while having a compact and portable package size. By completing a functional amplifier prototype and demonstrating its operation in relay testing applications, the objectives of this thesis has been achieved. The remaining tasks of transforming the prototype design

into a commercially marketed current amplifier remain to be address. These future tasks are briefly discussed in Section 6.2.

The contributions of this thesis include the following:

- Successful implementation of relay testing current amplifier by using power electronics based switching technology, which offers the advantages of high efficiency and a compact package, as compared to the conventional analog design.

- Unique use of transient simulation, which allows the determination of suitable converter topology, switching method, and control design to be implemented in the amplifier design. In addition, output rating and waveform quality of the amplifier can also be obtained by the simulation.

- Significant improvement of the VSC waveform quality by using various design measures, including implementation of the novel active and passive filtering system and allowing only the analog compensator to operate at low current output level.

- Implementing of energy storage capacitor and two-level CRPWM switching scheme that allows the current amplifier to operate with a low power DC source.

- Finally, as demonstrated by simulation, further improvement of the current amplifier waveform quality and reduction of switching losses by implementing the three-level control scheme with low switching losses.

6.2 Future Recommendation

Further improvements recommended for the relay testing current amplifier are discussed below:

There is a potential for further improvement in terms of increasing power efficiency of the existing amplifier design. Alternative hardware solutions should be investigated, in order to ensure that the current amplifier would have higher efficiency rating. In addition, it was clearly shown in the simulation results of Chapter 4 that the implementation of the three-level control scheme would reduce dynamic operating losses and increase output waveform quality of the VSC. Incorporation of the double hysteresis band technique would require some hardware modification. The control scheme should be implemented in the future amplifier design.

To produce a commercial product, additional performance tests for the current amplifier should be performed. Examples of these tests include measurement of the phase and group delay, frequency and phase responses, THD (Total harmonic distortion), gain accuracy, noise level, and emi emission level. The effects of ambient temperature and humidity on the operating performance of the amplifier should also be investigated. Finally, vibration tests should be conducted to ensure that the various high power components, power supplies, and printed circuit boards were properly assembled and securely mounted in the amplifier enclosure.

To protect the current amplifier from experiencing unexpected disturbances, which could easily lead to the breakdown of the amplifier circuit components, appropriate protection

measures to monitor and prevent occurrence of these disturbances should be implemented. Examples of protection measures include overvoltage of the amplifier output and power supplies, undervoltage of the power supplies, overcurrent of the amplifier output and power supplies, and overtemperature of the MOSFET switches and power opamps.

To perform the three-phase transient testing of protective relays, it is necessary to construct at least three units of such amplifiers and package these amplifiers, preferably, into the same enclosure. The eventual size and weight of the three-phase amplifier test set should be compact and portable enough to allow for easy carrying and maneuvering for the purpose of field-testing.

Finally, the current amplifier enclosure should be equipped with indicators to illustrate operating status of the amplifier, control buttons to trigger the on-off function and adjust the amplifier gain and offset settings, and labels to clearly identify the designated function of the indicators, input and output terminals, and control buttons.

Appendix A Specifications of Relay Testing Amplifiers and Protective Relays

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Introduction

The documents provided in this appendix are organized in the following fashion:

1. Recommended specification of the relay testing current extracted from "Digital Simulator Performance Requirements for Relay Testing," *IEEE Transactions on Power Delivery*, Vol. 13, No. 1, pp. 78-84, Jan 1998.

2. Recommended specifications of the relay testing amplifiers provided in "Understanding Conditioning Amplifier Response," J.A. Jodice, L. Allfather, R. Ryan, *ICDS'95*, pp.305-313, Apr 1995.

3. Hardware specifications of SEL 701 motor protection relay.

Table III. Typical Power Amplifier Specifications

		Voltage Amplifiers	Current Amplifiers
Input Characteristics			
1	Input Impedance	>10 k Ω	>10 k Ω
2	Input Range	±10 Vpk	±10 Vpk
3	Common-mode Input Range	±10 Vpk	±10 Vpk
4	CMRR	60 dB	60 dB
5	Gain	30 V/V	10 A/V
Output Capabilities			
6	Maximum Output Voltage	±300 Vpk	±50 Vpk
7	Maximum Output Current	±1 Apk	±100 Apk
8	Continuous Output Power	150 VA	2500 VA
AC Performance			
9	Frequency Response	0 – 10 kHz	0 – 10 kHz
10	Accuracy ($\lvert Gain^{*}V_{in} - V_{out}\rvert$)	<1% error, dc–1kHz <3% error, 1kHz–3kHz <5% error above 3kHz	
11	Group Delay	<50 μs	<50 μs
12	Group Delay Variation (0 – 3 kHz)	±1μs	±1μs
13	Slew Rate	> $10V/\mu s$	> $2.5V/\mu s$
14	Power Bandwidth	0 – 10 kHz	0 – 10 kHz
15	Output Impedance (0 - 3 kHz)	< 0.5Ω	> 250Ω
16	Output Offset	<0.1 V	<0.05 A
17	THD+N	<0.1%	<0.1%
18	IMD	<0.1%	<0.1%
Load Constraints			
19	Worst Case Load Impedance	70 Ω – inf. *	0 – 5 kΩ **
Environmental			
20	Operating Temperature	10 – 40 C^o	10 – 40 C^o
21	Output Offset Drift @ 20 C^o	<0.05% / C^o	<0.05% / C^o
22	Power Consumption	600 VA	10 kVA

Fig. A. 1 Recommended Specifications of Relay Testing Amplifiers.

H. Recommended Specifications for Switched-Mode, Direct Coupled Conditioning Amplifiers

Input Signal: 6.4 Volts RMS for full scale output on any range
Input Mode: Differential
Input Impedance: > 10 kΩ
Power output::
Current: 450 VA continuous, 675 VA for 1.5 seconds
Voltage: 150 VA continuous, 225 VA for 1.5 seconds
Output Range:
Current: 0–7.5/15/22.5/30/45/90A, continuous ac/dc 200% over range for 1.5 seconds
Voltage: 0–75/150/300V continuous ac/dc
Slew rate:
Current: 4 Amps per microsecond on 90 Amp range
Voltage: 10 volts per microsecond on 75 volt range
Frequency Response: dc to 20 kHz $\pm$ 3dB
Gain Accuracy @ 50/60 Hz = 0.2% of value
Phase error 50/60 Hz < 0.2°
Line/Load regulation: < 0.5% maximum, zero to full load @ 50/60 Hz, including $\pm$ 10% line variation
Noise: 10 Hz to 20 kHz < -66 dB
Common Mode Rejection Ratio > 66 dB
Harmonic Distortion as percentage of RMS full scale @ 50/60 Hz: Any one component < 0.5%, Total Harmonic Distortion < 1.0%
Error Indication:
Error annunciated when output deviates in amplitude or distortion from set value greater than specifications. Audible and visual indication persisting for at least one second with logical or communication signal to controller for test abort use.

Fig. A. 2 Recommended Specifications of Relay Testing Amplifiers.

Detailed Specifications

Standard Relay Features & Functions

Phase Current Inputs

Nominal Current, I_{NOM}:	1 A or 5 A
Range:	0.05–20.00 • I_{NOM}
Burden:	0.14 VA @ 5 A, 5 A tap 0.06 VA @ 1 A, 1 A tap
Continuous:	3 • I_{NOM}
200 Second Thermal:	10 • I_{NOM}
10 Second Thermal:	20 • I_{NOM}
1 Second Thermal:	50 • I_{NOM}
Measuring Error:	±1%, ±0.01 • I_{NOM}

Neutral/Ground Current Input

Nominal Current, IN_{NOM}:	1 A or 5 A
Range:	0.005–2.000 • IN_{NOM}
Burden:	0.28 VA @ 5 A, 5 A tap 0.19 VA @ 1 A, 1 A tap
Continuous:	0.3 • IN_{NOM}
1 Second Thermal:	5.0 • IN_{NOM}
Measuring Error:	±1%, ±0.01 • I_{NOM}

Motor Thermal Model

Locked Rotor Time:	1.0–240.0 s
Locked Rotor Current:	2.5–16.0 • I_{NOM}
Service Factor:	1.0–1.5

Setting Modes:
- 45 standard curve shapes
- Nameplate ratings
- Custom curve shape

Pickup Error:	<±1%, ±0.01 • I_{NOM}
Timing Error:	±2% ±15 ms

Independent Stop/Run Cooling Rates
Thermal estimate retained through relay power cycle.

Overcurrent Elements (Phase, Residual, Negative-Sequence)

Setting Range:	0.05–20.00 • I_{NOM}
Time Delays:	0.00–400.00 s

Neutral Ground Overcurrent Element

Setting Range:	0.005–2.000 • IN_{NOM}
Time Delays:	0.00–400.00 s

Current Unbalance Element

Alarm and Trip Elements	
Setting Range:	2%–80%
Time Delays:	0.00–400.00 s
Error:	<±1%

Definitions:

For $I_{av} > FLA$: $UB\% = 100\% \cdot |I_m - I_{av}|/I_{av}$

For $I_{av} < FLA$: $UB\% = 100\% \cdot |I_m - I_{av}|/FLA$

Where:
- I_{av} = Avg phase current
- I_m = Phase most different from I_{av}
- FLA = Motor rated full load amps

Load-Loss/Load-Jam Function

Load-Loss Alarm and Trip	
Setting Range:	0.03–1.00 • FLA
Load-Jam Trip	
Setting Range:	0.5–6.0 • FLA
Time Delays:	0.00–400.00 s

Starts Per Hour, Time Between Starts

Max. Starts/Hour:	1–15 starts
Min. Time Bet. Starts:	1–150 minutes

Start data retained through relay power cycle.

Phase Reversal Tripping

Phase reversal tripping based on current or optional voltage inputs.

Meter Accuracy

Current Metering:	±1%, ±0.01 • I_{NOM}
Demand Current Metering:	±1%
Optional Voltage Metering:	±1%, ±0.2 V
Optional Power Metering:	±2%
Optional Power Factor Metering:	<±4%
Optional Frequency Metering:	±0.01 Hz
Optional kW, kVa, kVAR Demand:	±2%

Analog Output

Single Analog Current Output

Settable Range:	0–1 mA 0–20 mA 4–20 mA
Max Load:	8 k or 400 ohms
Error:	<±0.5%, Full Scale

Select From:
%FLA, %Thermal Cap, Hottest RTD, Avg phase current, Max phase current

Contact Inputs

6 Self-Wetted Contact Inputs, Programmable Function

Contact Outputs

1 Trip Contact, 3 Programmable Contacts, Relay Self-Test Alarm
Form C Contacts
Make/Carry/Interrupt Ratings

Make:	30 A
Carry:	6 A
Interrupt:	8 A Resistive @ 250 Vac 0.75 A, L/R = 40 ms @ 24 Vdc 0.50 A, L/R = 40 ms @ 48 Vdc 0.30 A, L/R = 40 ms @125 Vdc 0.20 A, L/R = 40 ms @250 Vdc

Serial Ports

Front-Panel

EIA-232 Port:	300–19200 baud

ASCII text communication

Rear Panel

ASCII EIA-232 port:	300–19200 baud
Or Modbus® EIA-485 port:	300–19200 baud
EIA-485 port isolation:	500 V

Optional Features & Functions

Optional Phase Voltage Inputs

Nominal Voltage:	0–300 Vac

Four-Wire Wye or Open-Delta Voltages

Burden:	<2 VA at 300 V
Measuring Error:	±1%, ±0.2 V

Over/Undervoltage Elements

Setting Range:	1–300 Vac

Two Phase Overvoltage Elements
Two Phase Undervoltage Elements
One Residual Overvoltage Element

Power Factor Element

Alarm and Trip Levels	
Setting Range:	0.05–0.99 pf
Time Delays:	0.00–400.00 s
Measuring Error:	<±4%

Reactive Power Element

Alarm and Trip Levels	
Setting Range:	30–2000 VAR, 5 A tap 6–400 VAR, 1 A tap
Time Delays:	0.00–400.00 s
Measuring Error:	<±2%

Underpower Element

Alarm and Trip Levels	
Setting Range:	30–2000 W, 5 A tap 6–400 W, 1 A tap
Time Delays:	0.00–400.00 s
Measuring Error:	<±2%

Over/Underfrequency Elements

Three Settable Levels	
Setting Range:	20.00–70.00 Hz
Time Delays:	0.00–400.00 s
Error:	<±0.01 Hz

Optional Internal RTD Inputs

11 Internal RTD Inputs
Monitor Winding, Bearing, Ambient, or Other Temperatures
PT100, Ni100, Ni120, and Cu10 RTD-Types Supported, Field Selectable

Trip and Alarm Temperatures

Setting Range:	0°–250°C
Error:	<±2°C

Open and Short Circuit Detection
Trip Voting
Thermal Model Biasing
Motor Cooling Time Learning

Optional External RTD Module

12 Remote RTD Inputs
Trip, Alarm, and Thermal features, as with Internal RTDs.
Up to 500 m Away Using Fiber-Optic Cable
Adds Remote Contact Input

Reporting Functions

Event Summaries/Event Reports

14 Latest Summaries and 15-Cycle Oscillographic Records	
Resolution:	4 or 16 samples/cycle

Load Profile Function

Stores up to 17 quantities every 15 minutes for 48 days (without voltage option) or 34 days (with voltage option).

Sequential Events Records

512 Latest Time-Tagged Events

Motor Start Reports

5 Latest Starts	
Report Length:	3600 cycles

Quantities stored every 5 cycles during and immediately after each start.

Motor Start Trend

Stores 30-day averages of starting data for each of the past eighteen 30-day periods.

Ratings, Type Tests, & Certifications

Operating Temperature Range

–40°C to +85°C
–40°F to +185°F

Power Supply Voltage Range

20–250 ±20% Vdc
95–240 ±10% Vac 50/60 Hz
<15 VA Total Burden

Hold-Up Time:	50 ms @125 Vdc 150 ms @ 120 Vac

Type Tests

Front Panel:	NEMA12/IP54
Dielectric:	2.5 kV rms, 1 minute
Environmental:	IEC 68-2-1 : 1990 IEC 68-2-2 : 1974
Damp Heat Cycle:	IEC 68-2-30 : 1980
Impulse:	IEC 255-5 : 1977, 5 kV 0.5 j
Electrostatic Discharge:	IEC 801-2 : 1991, Level 4 IEC 255-22-2 : 1989 Level 4
Radio Frequency Immunity:	IEC 801-3 : 1984 IEC 255-22-3 : 1989
Fast Transient Burst:	IEC 801–4 : 1988, Level 4 IEC 255-22-4 : 1992, Level 4
Surge Withstand:	IEC 255-22-1 : 1988 IEEE C37.90.1 : 1989
5 kV Impulse:	IEC 255-5 : 1997
Magnetic Field Immunity:	EN 61000-4-8 : 1993, Level 5
Vibration:	IEC 255-21-1 : 1988
Endurance:	Class 1
Response:	Class 2
Shock and Bump:	IEC 255-21-2 : 1988
Bump:	Class 1
Shock Withstand:	Class 1
Shock Response:	Class 2
Seismic:	IEC 255-21-3 : 1993, Level 2

Certifications

ISO: Relay is designed and manufactured to an ISO-9001 certified quality program.
UL/CSA: UL recognized to the requirements of UL-508; CSA C22.2, N.14 for Industrial Control Equipment; and UL-1053, "Ground-Fault Sensing and Relay Equipment."
CE: CE Mark.

Fig. A. 3 Hardware Specifications of SEL 701 Motor Protection Relay.

Appendix B References

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