Neural Network Controlled Optimal Pulse Width Modulation for a Voltage Source Converter

by

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NEURAL NETWORK CONTROLLED OPTIMAL PULSE WIDTH MODULATION FOR A VOLTAGE SOURCE CONVERTER

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Abstract

This study is aimed at the application of feed-forward artificial neural networks to the on-line calculation of the optimal firing angles of a voltage source converter. Optimal pulse width modulation (OPWM) is a method to determine the switching instants of the power electronic switches in a voltage source converter (VSC) such that the current harmonics at its ac terminals are minimized while the number of switching actions per cycle remains constant. To achieve this, the converter switches must operate (or fire) at certain angles, which are dependant on the magnitude of the fundamental frequency component of the output voltage. Practical implementation of this technique is impeded partially due to the difficulties of the on-line calculation of the firing angles. Artificial neural networks (ANN) with their ability to provide nonlinear input-output relationships can serve as an appropriate tool to determine the firing angles in real time as the required magnitude of the fundamental varies. In this study a feed forward ANN is employed for this purpose. To verify the basic ideas, in addition to the extensive number of simulations, a hardware prototype was built. This prototype includes the inverter, the firing circuits and the controller and was successfully used as an induction machine drive.

This thesis is organized in six chapters. After a short introduction in Chapter 1, the basic ideas related to the ac to dc and dc to ac converters are presented in

Chapter 2, with a clear focus on the harmonic reduction methods. Chapter 3 briefly introduces the artificial neural networks. The focus here will be on the particular methods used in the following chapters. Chapter 4 contains the theoretical background for the optimal PWM voltage source converter, the proposed method for controlling the firing angles and details of the hardware implementation of a prototype converter. Chapter 5 explains the application of the same technique to an ac to dc converter and a STATCOM. The conclusions and suggestions for further study are presented in Chapter 6.

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My deepest thanks goes to my beloved wife for her understanding, sacrifice and love.

To my family

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CHAPTER 1

INTRODUCTION

Power electronic converters are a set of devices that deal with the conversion and control of electric power by supplying voltage and current in a form which is optimal for the load. Typical applications of power electronic converters include heating and lighting control, electrochemical processes, dc and ac regulated power supplies, induction heating, dc and ac electrical machine drives, electrical welding, active power line filtering, static VAR compensation, series transmission line compensation, HVDC transmission, and many more.

Utility systems produce power in 50 or 60 Hz sinusoidal form at fixed voltage. But many loads need the electric power in dc form, or in ac form but at different voltage or frequency. Quite often this power must be controlled precisely. A power electronic system converts the power from its original form to a form which is best for the given load.

Sometimes power is generated in dc form (by batteries, fuel cells, dc generators or MHD generators) or in ac form but with variable frequency (like wind turbines) or even at a fixed frequency, but different from that of the electrical network. A power electronic system usually interfaces these generating units to the rest of the electrical system.

At the centre of each power electronic converter there is usually a set of switching devices which are switched on and off by signals from a control system. The main reason for using switching devices is that an ideal switch has either a zero voltage across its terminals (on state) or zero current flowing through it (off state) and in both cases there is ideally no power dissipation in the device. Although real power electronic switches have some power loss, these are much less than in comparable linear devices. Rapid changes in the voltage or current caused by switching devices, on the other hand, produce unwanted voltage and current harmonics in the load and the source. The presence of harmonics in the voltage and/or current has

many negative impacts on the loads and power system equipment: in electric machines and transformers it produces extra heat and noise forcing the system to operate below its rated power, in cables it increases the insulation stresses, interferes with the operation of protective relays and so on. The growing number of power electronic converters in the power systems and therefore the rising level of the harmonics has forced a number of utilities to install active and passive filters in their systems at great costs. All of these make the reduction of harmonics a major concern for the power electronic converter designers. One common conventional method for reducing the harmonics generated by converters is to make several smaller converters instead of one large converter. These smaller converters are then connected to each other by specially designed transformers to share the output power. The net effect of the transformer connection is the cancellation of certain harmonics due to the introduction of appropriate phase shifts. This method used to be the natural choice in the past because making high power converters was subject to many technical difficulties and designers preferred to use several smaller converters. But this is not true any more with the great improvements in the recent years in the ratings and the speed of the switching devices and in the methods to connect them in series or parallel.

Using smart techniques for turning the switching devices on and off can reduce the size of harmonics and/or move them to the areas of frequency spectrum

where they are less harmful for the other systems connected to the converter. The most common technique for this purpose is the Pulse Width Modulation (PWM) where the ON and OFF times of the switches are determined by the instantaneous values of the desired output voltages or currents. In the basic sinusoidal PWM (see section 2.3.3) devices are switched at constant frequency but within each cycle the ON time depends linearly on the desired magnitude of the output. Many improvements to this basic PWM technique have been introduced (sections 2.3.4 to 2.3.7) to consider the mutual effects of the phases in three phase converters, the effect of triplen harmonics, advantages of multiple converters connected by transformers and other effects.

A promising improved PWM technique is the "optimal PWM" which totally removes certain selected harmonics from the output with the minimum number of switchings per cycle. Despite this clear advantage this method is not very popular yet for a number of reasons including the difficulty of implementation and relatively poor transient behaviour. This project's major aim is to find a convenient way for implementation of this technique. It will also be shown that superior results can be obtained with this method in a number of applications, particularly the Synchronous Static VAR Compensator (STATCOM), provided that the proper control scheme is employed.

The difficulty in the implementation of this technique comes mainly from the complexity of the equations that determine the switching angles of the inverter. These are a set of coupled nonlinear algebraic equations which can not be easily solved in real time. But to be able to use this PWM method we need a new solution for these equations every time the output voltage of the Voltage Source Converter (VSC) is changed. Our suggested implementation method is based on using an artificial neural network for solving these equations in real time. An artificial neural network is essential a set of simple nonlinear transfer functions connected to each other through constant gains. Despite the simplicity of its building blocks, a neural network can mimic almost any continuous multi input-multi output transfer function. Another important advantage of the neural networks is that they "learn" the transfer function between their input and outputs by examples of input-output pairs. In our application a set of solutions to the optimal PWM equations is used to train a neural network. Once the training is complete, the neural network can provide the switching angles for the voltage source converter for any desired level of the output voltage. The practicality of this method was examined by making a hardware prototype. The hardware prototype basically confirmed the simulation results and proved that a neural network-based controller for a VSC can be easily made by a fair amount of circuitry.

CHAPTER 2

POWER ELECTRONIC DEVICES AND CONVERTERS

The purpose of this project is to introduce a new technique for reducing harmonic content in the output of a voltage source converter. To provide the necessary background, this chapter will first briefly review the properties of some common semiconductor devices used in power electronic systems (section 2.1), then will discuss fundamental operational principles of ac to dc and dc to ac converters and some more recent achievements in these areas (sections 2.2 and 2.3). The focus will be

always on different ways of reducing the harmonics generated by the converters. The last section is dedicated to the power electronic systems used for reactive power compensation with more emphasis on the static synchronous compensator (STAT-COM). These devices are also based on voltage source converters and use similar techniques for harmonic reduction.

2.1 POWER SEMICONDUCTOR DEVICES

Power semiconductor devices are the key elements of a power electronic system. The first solid state high power device that replaced the vacuum tubes was the thyristor. Despite its great success and continuing popular use, the inability of the thyristors to interrupt the current makes its application difficult in many systems such as voltage source converters. But the tendency toward using voltage source converters has been growing because of their many advantages specially the relative simplicity of reducing their output harmonics. The development of improved devices that can be turned off when carrying current has been the recent focus of power electronics research.

2.1.1 Thyristor

The *thyristor* is probably the most commonly used power semiconductor device. A thyristor has three terminals: the anode (A), the cathode (K) and the gate

(G). The operating principles of the thyristor are simple: it starts conduction only if its anode has a higher potential than the cathode and a positive triggering pulse (V_{KG}) is applied to the gate. It will then remain conducting even if the gate pulse is removed, until the anode current falls under a certain value I_h.Thyristors are widely used over the entire power electronics spectrum, including dc and ac motor drives, lighting and heating control, HVDC conversion, static VAR compensation and solid state circuit breakers. The maximum rating of thyristors is significantly larger than most other power semiconductor components, typically above 5kA and 5-7kV. They are also less fragile than many other devices and can tolerate large surge currents. The main difficulty in using thyristors is that they can not be turned off by applying a control signal to the gate.

2.1.2 Triac

The *triac* has a complex multi-layer structure, but functionally it is like an antiparallel pair of thyristors. Like the thyristor, the triac has three terminals: T_1, T_2 and gate. When T_1 is positive the triac is turned on by a positive gate current and when T_2 is positive by a negative gate current. In both cases it remains on until the terminal current goes below the holding current. The triac is more economical than a pair of thyristors and is also easier to control, but it is more sensitive to rate of change of voltage (dv/dt), less sensitive to gate current variations and has a longer

turn-off time. The maximum rating of triacs is around 800V and 40A. The triac is usually used in 60Hz phase-controlled resistive loads such as heating and lighting.

2.1.3 Gate turn-off thyristor (GTO)

The *Gate turn-off thyristor* (GTO) is a device similar to the thyristor; however it can be turned off by applying a negative gate current pulse (Fig. 2-1). The turn-on characteristic is similar to the thyristor, but the current gain is much lower in turn off (typically 4 to 5). This means that a GTO needs a gate current of about 1/4 of the anode current to be turned off. GTOs usually need large snubber circuits[1] to limit the rate of voltage rise during the turn-off. This leads to a considerable snubber loss and limits their operation frequency to 1 to 2 kHz. GTO's ratings currently reaches to 6kV and 6kA which is comparable to that of the larger thyristors.

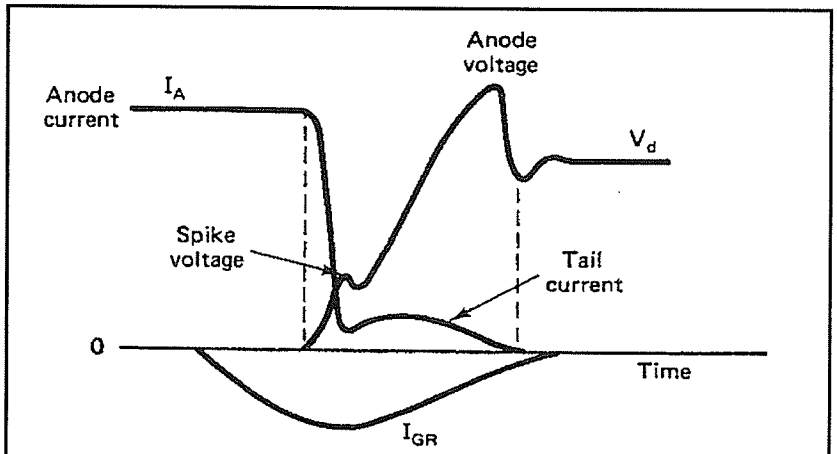


Fig. 2-1 Typical turn-off current waveforms of GTO [2]

2.1.4Power MOSFET

The *power MOSFET*'s structure and characteristics are similar to the low power MOSFETs. It is a voltage driven device and has a negligible gate current in the steady state. High switching frequency and easy gate control are the main advantages of this device and the relatively low power ratings is its major limitation. Because of very fast switching, this device has very little switching power loss, but since it has a relatively high voltage drop in the on-state the conduction loss is high. The positive temperature coefficient makes it easy to parallel MOSFETs in contrast to bipolar junction transistors (BJT). Power MOSFETs are popular in low-voltage, low-current high-frequency applications. The highest ratings available now are about 500V, 50A and 100kHz.

2.1.5 Insulated Gate Bipolar Transistor (IGBT)

The *insulated Gate Bipolar Transistor* (IGBT) combines the features of a MOSFET and a BJT. The power handling part of the device is a bipolar transistor (BJT), but the input stage is like that of a field effect device (Fig. 2-3), resulting in a negligible steady state gate current. Like BJTs, IGBTs inherently tolerate relatively high di/dt and dv/dt and therefore their snubber circuits are somewhat simpler. IGBTs usually have a diode connected across them in the reverse direction as they can not tolerate significant reverse voltages. This feature makes them more attrac-

tive to use in voltage source converters. The simplicity of the gate drive, ease of protection, and switching speed have made IGBTs one of the most popular power electronic switching elements in recent years. As a result several manufacturers have invested in producing higher rating IGBTs. The highest ratings that are commercially available now are 5kV and 1.5kA), with the switching frequencies up to 25kHz. More over, unlike BJTs, IGBTs can be easily paralleled to achieve higher current ratings. The IGBT's weaknesses come from its high conduction losses (because of the relatively high voltage drop) and its incapability of handling large over currents and over voltages.

2.1.6 Gate Commuted Thyristor (GCT)

The GCT is a newly introduced semiconductor which is based on the GTO structure [3]. Similar to GTO, the GCT is turned on by a positive gate-cathode

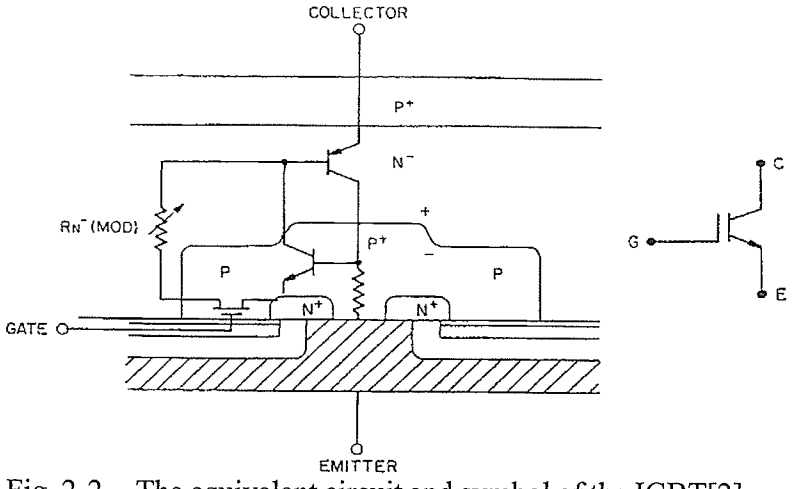


Fig. 2-2 The equivalent circuit and symbol of the IGBT[2]

pulse, but its gate current is larger and the anode-cathode voltage drop waveform is sharper and smoother. The device can be turned off while conducting by applying a negative current pulse to the gate, which is equal to the anode current. This will cause a quick turn off and removes the tail current which is typical for the GTOs. GCTs can tolerate a very high dv/dt and therefore do not need a dv/dt snubber, but they still need a snubber circuit to limit their di/dt. As the GCTs are mainly designed to be used in voltage source converters, they usually come with a monolithicly integrated anti parallel fast recovery diode. Thanks to the thyristor based structure, the GCT has a much lower conduction losses in comparison with the IGBT. Recent improvements in GCT design has reduced the conduction losses up to 25% below the

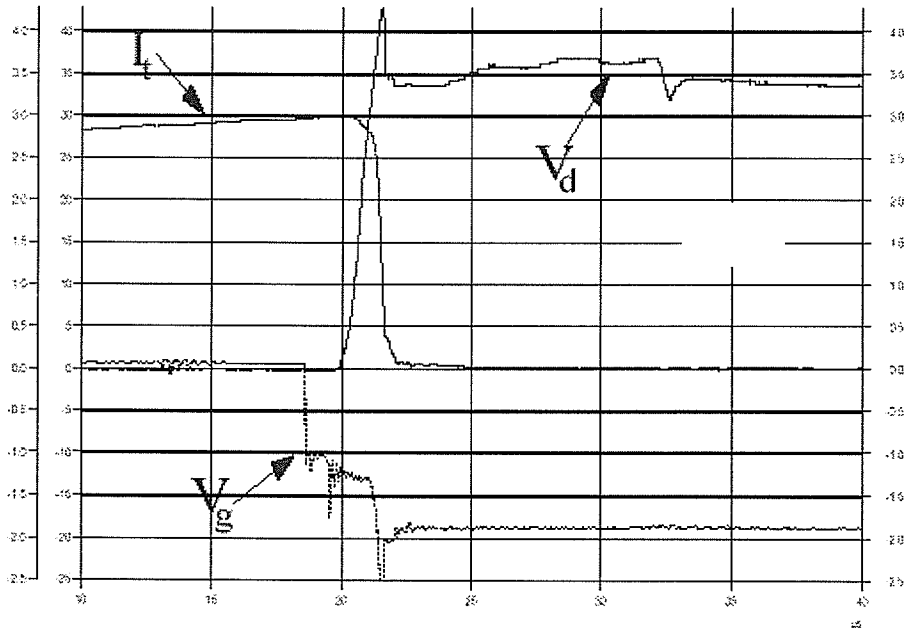


Fig. 2-3 Snubberless turn-off of a 3kA/4.5kV IGCT[3]

normal thyristors [4]. This reduces the cooling requirements in high power applications and effectively reduces the overall cost of the converters. The highly demanding gate circuit of the GCT has encouraged manufacturers to assemble the GCT and its gate drive in one module which is sometimes called Integrated Gate Commuted Thyristor or IGCT. The highest ratings currently available for IGCTs are 6kV, 5kA and 3kHz.

2.2 AC TO DC CONVERTERS (RECTIFIERS)

Rectifiers are widely used in countless applications requiring ac to dc conversion, from home electronics in the miliwatts range to large aluminium and copper mills in the megawatts range. The ac harmonic currents generated by the rectifiers is a matter of concern for the power utilities because it is directly injected into their system and can adversely affect other consumers as well as the transmission and distribution equipment. In this section we introduce a number of common rectifier circuits and the harmonic reduction techniques used in them. The author's contribution in this field by applying the method of neural network controlled optimal pulse width modulation will be explained in the following chapters.

The simplest three phase rectifier is the diode bridge shown in Fig. 2-4. This rectifier is simple and inexpensive, but it has several disadvantages. The output dc

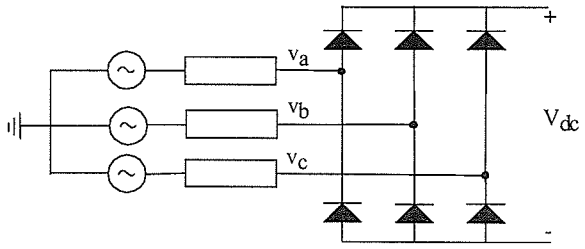


Fig. 2-4 The simple (6-pulse) three phase rectifier bridge

voltage has considerable ripple and is not controllable, its ac input current is contaminated by lots of harmonics, and the power factor at the ac terminals is low. The three phase diode bridge can be improved in several ways to reduce these negative effects. The next few sections will briefly introduce the most common types of improved ac to dc converters.

2.2.1 Thyristor 6-pulse converter

The first step toward a better rectifier is to replace the diode bridge with a thyristor bridge. Using a half thyristor bridge we can control the dc output voltage in the $[0\text{-}V_{lmax}]$ range by changing the firing angles of the thyristors. A full thyristor bridge allows even a wider range of control from $-V_{lmax}$ to $+V_{lmax}$ if there is a source at the dc side to keep current flowing in the same direction. In this case the bridge can also send the power from the dc to ac side and act like an inverter.

2.2.2 Thyristor 12-pulse converter

The dc voltage ripple and ac current harmonics can be reduced by connecting two bridges in series and feeding them from different secondary windings of a YYΔ transformer (Fig. 2-5). The 30 degree phase shift caused by the Δ connection combined with the same phase shift in triggering signals of the thyristors makes the output voltage of the second bridge to be 30 degrees out of phase with respect to the

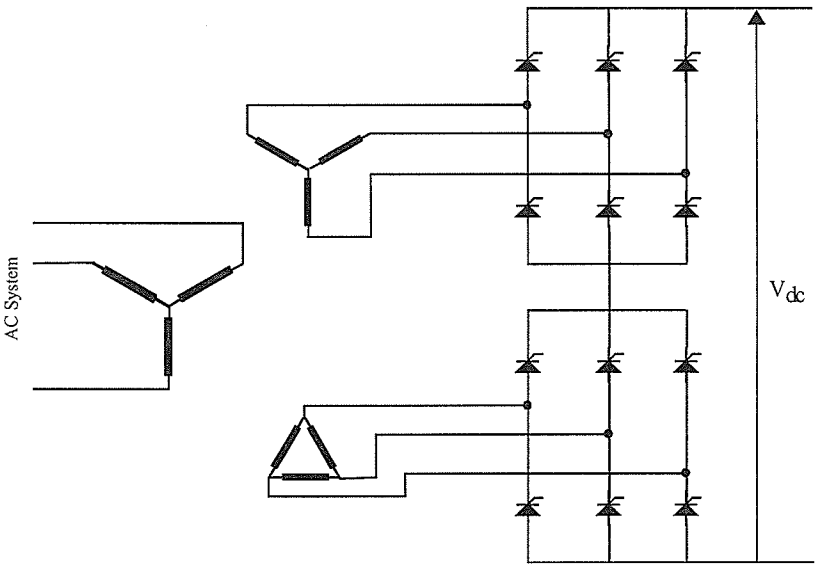


Fig. 2-5 The 12pulse converter configuration

first one. As a result, the total output voltage will have a ripple at a higher frequency (12 times the ac system frequency) and lower amplitude. There is also 30 degrees (or -30 degrees for negative sequence currents) phase difference between the line currents at the two sides of the YΔ transformer. Note that the phase shift caused by the transformer connection is the same at all frequencies. The ac side current phase shift caused by the converter on the other hand is n x 30^{o} where n is the harmonic number. As a result the total phase shift for 5th and 7th harmonics is equal to 180^{o} (note that the 5th harmonic current is negative sequence and the 7th is positive sequence) which means they will be cancelled out by the 5th and 7th harmonic currents from the YY transformer. This configuration is usually called a 12-pulse

configuration and is quite common in HVDC systems. Using the same idea, we can build higher pulse number systems like 24 and 48 pulse configurations to further reduce the dc and ac side harmonics, but this will require expensive zigzag transformers to produce the necessary phase shifts.

2.2.3 Parallel 12-pulse converter

The two thyristor bridges in Fig. 2-5 can also be connected in parallel to provide higher dc current. In this arrangement an interphase reactor is necessary to ensure the independent operation of the two rectifier bridges.The output voltage is the

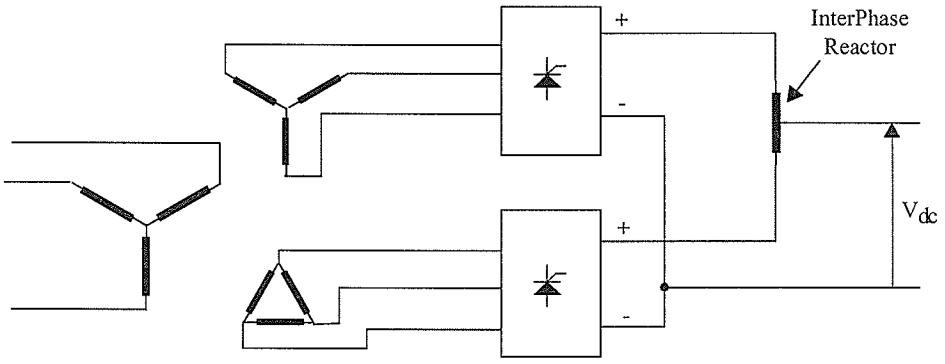


Fig. 2-6 12-pulse rectifier with parallel converters

average of the output voltages of the two converters and the output current is the sum of the two currents. The ac current's harmonic content remains the same as in

the series connected 12-pulse converter.

2.2.4 Parallel 12-pulse rectifier with multi-tap interphase reactor

The 12-pulse rectifier can also be improved by replacing Y and Δ windings with extended delta connections in the secondary side of the transformer and using two taps for the interphase reactor [6] as shown in Fig. 2-7.The extended delta ar-

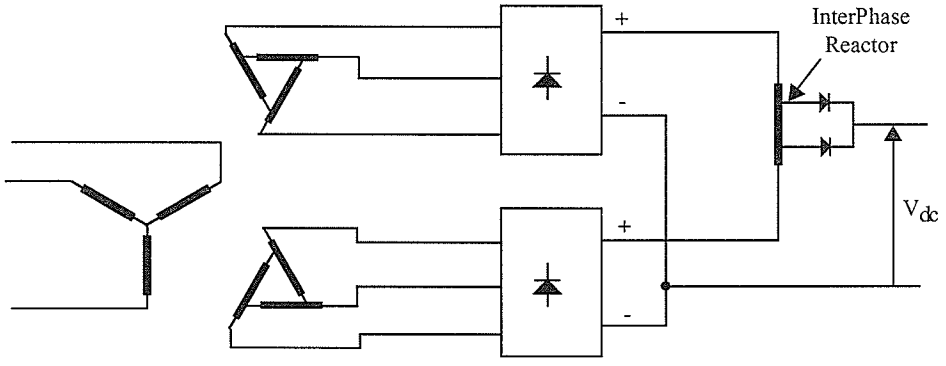


Fig. 2-7 12-pulse rectifier with extended delta connections and modified interphase reactor

rangement guarantees equal leakage reactances for the two secondary windings. The tapping ratio for the two taps can be selected such that the eleventh and thirteenth harmonics are eliminated from the input ac current. The fifth, seventh, seventeenth, nineteenth etc. harmonics will be cancelled as usual by the transformer. Thus from the input current point of view, this rectifier behaves like a 24-pulse ar-

rangement without using additional switching devices.

In the basic rectifier bridge, if diodes are replaced with self-controlled switches such as GTOs or IGBTs, better control over the dc voltage and ac current could be achieved. Switches can be turned on and off at appropriate times to substantially reduce a large number of harmonics both on the dc and ac sides. This will reduce the number of required switches and eliminates the need for complicated transformers. This method will be further discussed in future chapters.

2.2.5 Two-step rectifiers

Two step rectifiers are the most popular arrangements especially at lower powers. In these rectifiers usually a simple diode bridge is used to generate an unfiltered dc voltage. Then a dc-dc converter (e.g. buck or boost converter) shapes the final output voltage and current at the load to be to the desired level and with minimum lower order harmonics. The two step arrangement enables the designer to fo-

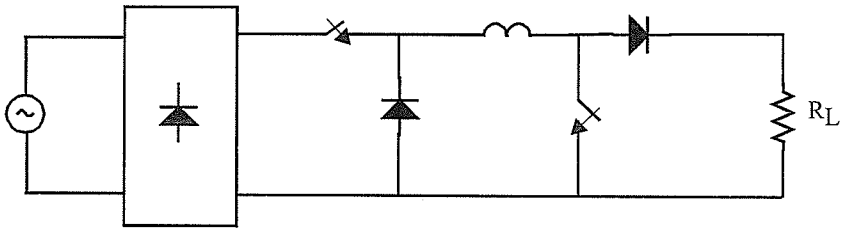


Fig. 2-8 Cascade Buck-Boost converter scheme

cus on the quality of the ac current (power factor and harmonics) drawn from the network in the first stage and leave the dc voltage regulation to the second stage. Several different switching schemes could be used to improve the ac side current waveform and power factor. For instance, in the buck-boost [7] converter presented in Fig. 2-8 the current drawn from the diode bridge is controlled to be almost in proportion to its dc side voltage, i.e. a full wave rectified sinusoid. As a result the ac current is nearly a sine wave with low harmonic content and near unity power factor[8].

As another example consider the two-step rectifier shown in Fig. 2-9. In this rectifier (sometimes called Ditcher rectifier) the main switch turns on and off the current in the primary winding of the transformer at a constant frequency much higher than the ac system frequency [9]. During the short "on" period the dc terminals of the diode bridge are connected only to the primary winding of the transformer. This raises the current to a level proportional to the ac voltage at the switching

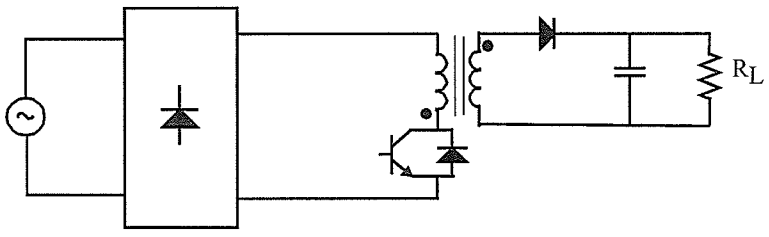


Fig. 2-9 Basic configuration of a single phase Ditcher rectifier

instant, because the length of the on period is constant. Then when the main switch turns off, the energy stored in the transformer's magnetic field is discharged into the load via the secondary winding. The dc current drawn from the rectifier bridge consists of a train of pulses with different amplitudes. The fundamental component of this pulse train is proportional to the rectified sinusoidal voltage at the bridge terminals. As a result the fundamental component of the ac current is also in phase with the ac voltage. Since the switching frequency is usually high, a moderate passive filter can be used at the ac terminals to remove excessive harmonics.

2.3 DC TO AC CONVERTERS

The class of power electronic equipment that convert dc to ac are known as inverters. Similar to the rectifiers, we are here concerned with the quality of converter's output waveforms. In this section we will introduce a number of most common inverter configurations and the harmonic reduction methods used in them.

Inverters can be classified into voltage fed and current fed (also called voltage source and current source) types. A voltage fed inverter is fed by a constant dc voltage source such as a battery or a regulated or unregulated rectifier, while a current fed inverter is fed by a constant dc current source such as a super conductor energy storage device or a controlled rectifier with a large series inductor at the output. A voltage fed inverter can operate in current controlled mode, i.e. its output voltage can be controlled in a way that the output current follows a specified reference value, regardless of the changes in load impedance or back emf. Similarly a current-fed inverter can operate in voltage controlled mode to provide the specified voltage at the ac terminals. Obviously in all these cases the output voltage and/or current waveforms of the inverter must be as close as possible to a sine wave and therefore reducing the output voltage and current harmonics is a major concern. As the first step, voltage source inverters usually use series inductors at their ac outputs to reduce the current harmonics, while current source inverters use parallel capacitors to

filter voltage harmonics. Different multi pulse and modulation techniques are also widely used for this matter. The most common types of the voltage source inverters and harmonic reduction techniques are shortly introduced in the following paragraphs.

2.3.1 Square-wave voltage fed inverter

The most simple voltage source three phase inverter is perhaps the *square-wave voltage fed inverter* (six-step inverter) shown in Fig. 2-10 (a). In this circuit transistors can be replaced by IGBTs, MOSFETs, GTOs or any other self-controlled electronic switch that suits the application. Theoretically during each cycle the upper and lower switches in each leg conduct for 180^{O} (in practice a short dead time between two successive switchings is necessary to avoid short circuitting the dc source). Switches in each leg are turned on and off with 120^{O} phase shift with respect to the other two legs. The resulting output voltage is a three phase symmetrical squarewave output as shown in Fig. 2-10 (b). In this simple inverter the frequency of the output ac voltage is controlled by the inverter, i.e. by the frequency of the firing pulses. But the amplitude of the output ac voltage is determined by the dc source. Therefore if the amplitude of the output voltage is to be controlled, the dc source has to be controllable. The other major drawback of this inverter is that its output voltage contains a large amount of harmonics and therefore needs strong fil-

tering. Low cost and relatively low losses are the main advantages that make the square wave inverter attractive in some applications.

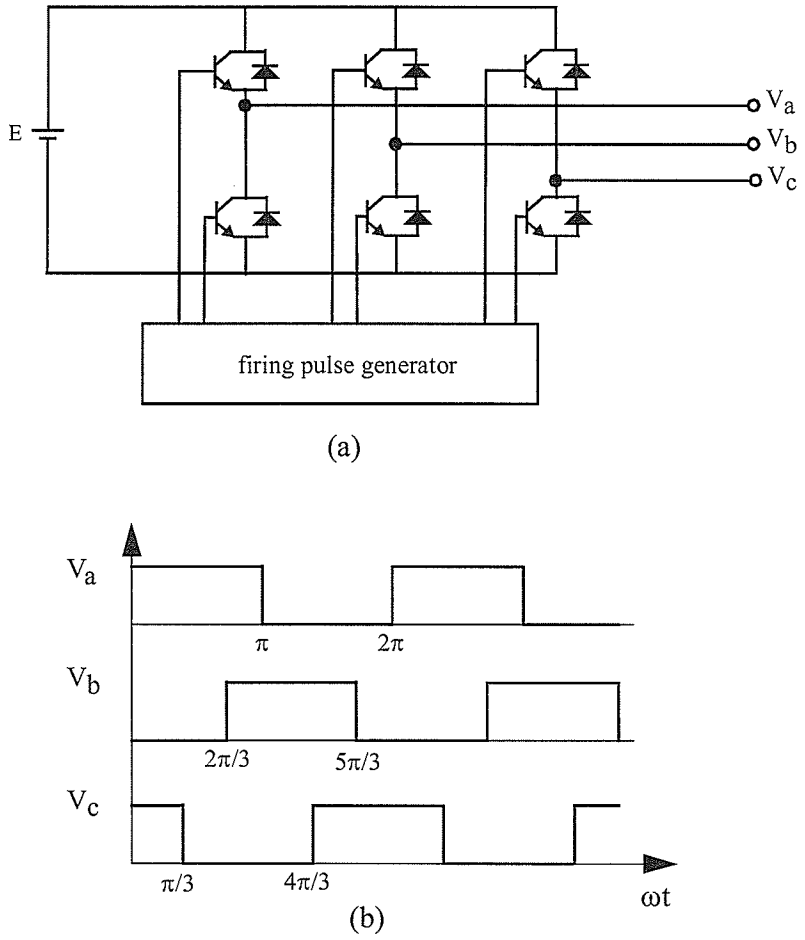


Fig. 2-10 Three phase square-wave voltage-fed inverter bridge;
a) Circuit diagram, b) The output voltage waveforms

2.3.2 Pulse Width Modulation

The output voltage of a voltage source converter can change only as pulses, for instance the phase voltages of the inverter shown in Fig. 2-10 can be either E or zero. Modulating the width of these pulses provides a way to change the average output voltage such that it contains a dominant fundamental component with harmonics as small as possible. Pulse width modulation (PWM) techniques have been improved over the time to provide the lowest harmonic levels with lower number of switchings and best transient performance for different applications. The following sections introduce a number of most common PWM methods.

2.3.3 Sinusoidal PWM

The above mentioned problems with the square wave inverter can be addressed by using a *Pulse Width Modulation* (PWM) scheme. Using PWM shifts the output voltage harmonics to higher frequencies which makes the filtering much easier. PWM also allows the output voltage to be controlled inside the inverter and therefore eliminates the need for the dc source to be controllable. Fig. 2-11 shows how the switching pulses are generated in the conventional sinusoidal PWM technique (also called the suboscillation PWM technique). Here a reference sine wave is compared with a triangular carrier wave. The frequency of the triangular carrier is much higher than the reference sine wave. Whenever the reference signal is great-

er than the carrier, the PWM trigger signal is high, otherwise it remains at the low level. For a three phase inverter like the one shown in Fig. 2-10(a), three separate reference sine waves with the same magnitude and frequency and 120^{o} phase shifts are required to be compared with three triangular carriers. When a trigger signal is high, the upper switch in the corresponding leg of the inverter is turned on and the lower one is turned off. Similarly, when the trigger signal is low, the upper switch is turned off and the lower one is on. This makes an output voltage at each terminal of the inverter that switches between zero and the full dc voltage in a similar fashion to the trigger signal.

The signal generated this way has a fundamental component at the same frequency as the reference sine wave and with an amplitude proportional to it (as long as the amplitude of the sine wave is below the peak value of the triangular wave). The harmonic voltages at the output of this inverter are mainly concentrated around the frequency of the triangular carrier, i.e. characteristic harmonics with closest frequency to the carrier have the largest magnitudes. As a result a higher carrier frequency will reduce the size of lower order harmonics and facilitate filtering, but at the same time it will increase the inverter losses because of the higher number of switchings. The *modulation index*, defined as the ratio of the magnitude of fundamental for a given scheme to the magnitude of fundamental for the six step in-

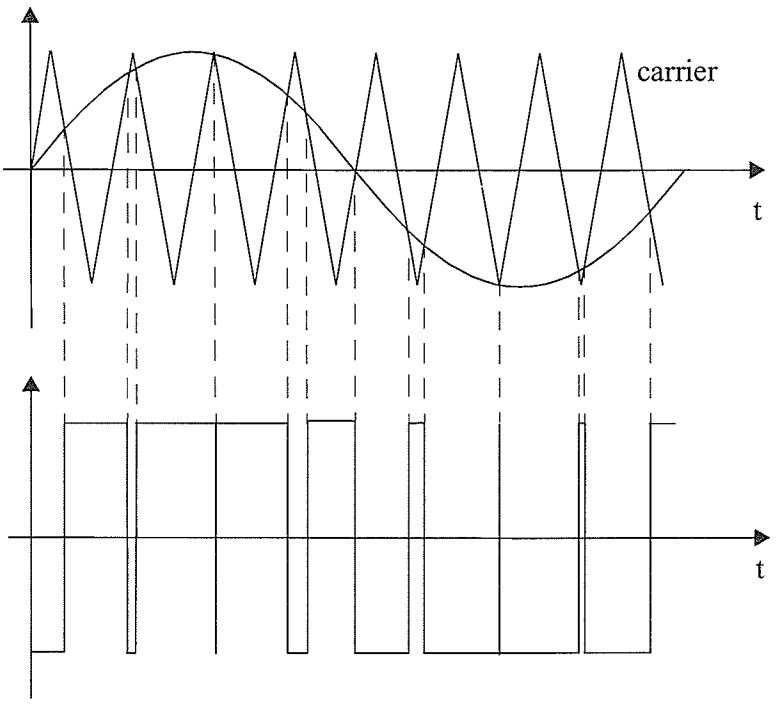


Fig. 2-11 Generation of sinusoidal PWM waveform

verter (note this is different from the ratio of the amplitude of the reference sine wave to the carrier which is sometimes also defined as modulation index), is a measure to compare the amplitude of the fundamental in different PWM methods. For the sinusoidal PWM the modulation index can reach its maximum value of $\pi/4=0.785$ when the amplitudes of the reference sine wave and the triangular carrier are equal [12]. Increasing the amplitude of the reference signal beyond this level (over modulation) will increase the amount of harmonics in the output voltage.

2.3.4 Harmonic injection PWM

Harmonic injection PWM [13] is a simple technique to increase the maximum modulation index while reducing harmonics in the output at the same time. Since the triplen harmonics do not appear in line currents in a three wire system, they can be added to the modulating signal in a pulse width modulator to elevate the maximum modulation index. The optimal amplitude and phase of each harmonic can be found by optimization techniques. This will increase the maximum modulation index to $\sqrt{3}\pi/6 = 0.907$. This scheme also reduces the total harmonic content of the output and its sensitivity to the dead times.

2.3.5 Space vector PWM

Space vector PWM is a very effective PWM technique. In this method at each moment of time the desired voltages for all three phases are considered together and then the state of each switch in the inverter is decided such that the output voltage of all three phases are as close as possible to the desired values. Looking at all three phases at the same time makes this method different from the previous methods that consider each phase independently. A brief explanation about the fundamentals of this method is given in the following paragraphs.

Each switch in the inverter can have two states: on and off. Therefore the

switches of the three phase bridge of Fig. 2-10 can have eight possible states (two for each arm). Here we assume that exactly one switch in every branch is on at any time. Obviously both switches being on will cause a dc bus short circuit and must be disallowed. We also do not allow isolation of the load from the dc bus as would happen with both switches off. For each arm of the inverter if the upper switch is on (and the lower is off) the output voltage of the corresponding phase is equal to the dc source voltage and if the upper switch is off the output voltage of that phase is zero. The output voltages of the three phases can be represented by three vectors at zero, 120^{o} and 240^{o}. For each possible state of the inverter switches, the three output voltage vectors can be added to make a unique vector that represents the output voltage of that state. Fig. 2-12 shows the 8 voltage vectors for the above inverter that are calculated according to the following equation:

$$V=2/3\ (\ v_a + \alpha v_b + \alpha^2 v_c\ ) \qquad (2\text{-}1)$$

where $\alpha = e^{j2\pi/3}$, and v_a, v_b, and v_c are either zero or equal to the dc source voltage. In this figure the vector V_1 represents the state of the inverter when v_a is high and v_b and v_c are low while V_2 shows that v_a and v_b are high and v_c is low. For the two states where all the upper switches or all the lower switches are on, we have V=0. These two states, V_0 and V_8, are called null states.

When the inverter is working, a controller provides a set of three reference

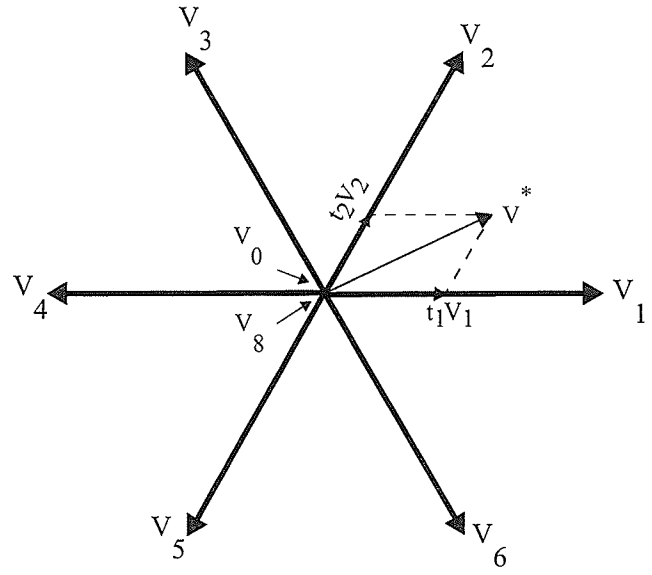


Fig. 2-12 Vector diagram for SVPWM

values for the three phase voltages. These three reference voltages are usually sampled at a constant rate with a sampling period T_s. At the time step k, the values of desired (reference) phase voltages are v_a^*, v_b^* and v_c^*. Similar to the inverter output voltages, these three values can be combined (using Eq. 2-1) to create the reference output voltage vector V*. Usually the inverter can not produce this voltage, but it can stay in the two adjacent states (say V_1 and V_2) for t_1 and t_2 seconds and also in one of the null states for t_n such that its average output voltage vector over the sampling period is equal to the reference voltage. This requires the following equation to be satisfied:

$$T_s V^* = t_1 V_1 + t_2 V_2 + t_n V_n \quad (2\text{-}2)$$

where $T_s = t_1 + t_2 + t_n$ is the sampling period. Fig. 2-12 shows how t_1 and t_2 can be calculated from the projection of V^* on the two adjacent voltage vectors. Since the sum of t_1 and t_2 is less than the sampling period T_s, the inverter must stay in null state for the rest of the sampling time. The null state time t_n can be evenly divided between the beginning and the end of the period T_s. In each case the null state is selected such that the transition from the previous state to null state and from the null state to the next state can be done with the minimum number of switching actions (usually only one switching). SVPWM method provides fast response to changes in the reference voltage and can produce less harmonics than the SPWM at the same frequency.

2.3.6 Synchronous PWM

The above PWM methods operate at constant carrier or sampling frequency, while the fundamental frequency of the reference signal is changing. Hence the switching sequence can be non-periodic which means that the Fourier spectrum of the output voltage is continuous and contains frequencies lower than the lowest carrier sideband as shown in Fig. 2-13. This problem is particularly important for smaller f_s/f_1 ratios where f_s is the carrier or sampling frequency and f_1 is the fundamental frequency of the reference. Synchronization of the sampling frequency and

the reference voltage can remove this problem. In *synchronized PWM* the ratio $N=f_s/f_1$ takes only integral values and is called *pulse number*. When the required modulation index or the frequency of the reference signal varies it is sometimes necessary to change the pulse number. These changes occur instantaneously and can generally produce current transients especially when the pulse number is low.

2.3.7 Improved space vector PWM methods

Several suggestions to improve the various aspects of SVPWM inverters have been given [14,15]. One interesting suggestion is to add a random part ΔT to T to spread the harmonics over a bandwidth [16]. This method reduces the power of harmonic voltage at each particular frequency to a very low level and therefore reduces the possibility of excitation of natural frequencies of the load. The *optimal subcycle method* is another variation of the space vector PWM in which the duration

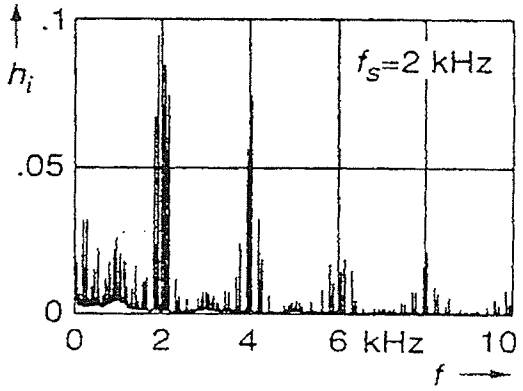


Fig. 2-13 Measured frequency spectrum for an asynchronous SVP-WM inverter [12].

of the sampling periods are not constant. The length of sampling period is considered as an optimization variable and is calculated for each sample in a way that some objective function is optimized [17]. This method exhibits high dynamic performance and can be used for synchronized and asynchronous modulation in a wide range of switching frequencies. The optimization reduces the harmonic currents at given frequencies and the frequency spectrum lacks dominant carrier frequencies.

2.3.8 Sampled SPWM techniques

The sinusoidal (suboscillation) PWM is easy to implement using analog integrators and comparators for generation of the triangular carrier and the switching

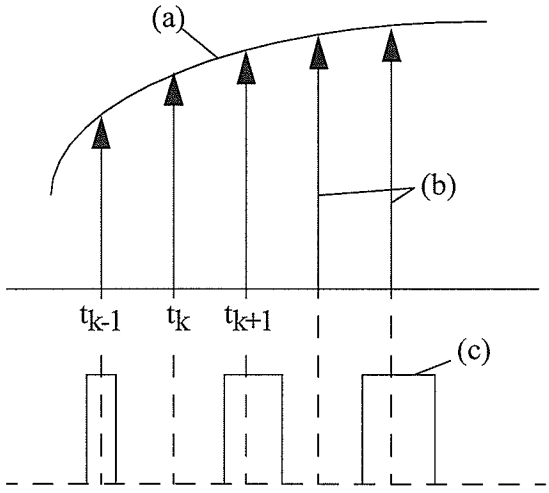


Fig. 2-14 Regular sampled PWM (a) reference signal (b) regular-sampled waveform (c) PWM waveform

pulses. Problems such as thermal drift, component tolerances, dc offsets, etc. associated with analog circuits have made the microprocessor based SPWM controllers more desirable. In a digital controller the reference signal can be sampled and the crossing instant between the reference and carrier signals calculated in real time. This method which is called *natural sampling* requires solving transcendental equations and therefore is not suitable for software implementation. In the *regular sampling* technique [18,19] on the other hand, the reference signal is sampled at regularly spaced intervals as shown in Fig. 2-14. For each carrier cycle two samples are generated, the first sample is used to calculate the time instant for the leading edge of the PWM pulse and the second is used for the trailing edge. The PWM signal generated this way is sometimes referred to as "asymmetric" regular sampled PWM because the two edges of each pulse are modulated with different samples of the reference signal and therefore it is asymmetric with respect to the sampling impulse. It is also possible to use only one sample to modulate both edges of the PWM pulse equally and produce a "symmetric" PWM signal [20].

2.3.9 Multilevel inverters

In *multilevel inverters* instead of using a single dc source a number of dc sources are connected in series to provide a way for applying different voltages to the load. Alternatively, a single dc source can be connected across a chain of series

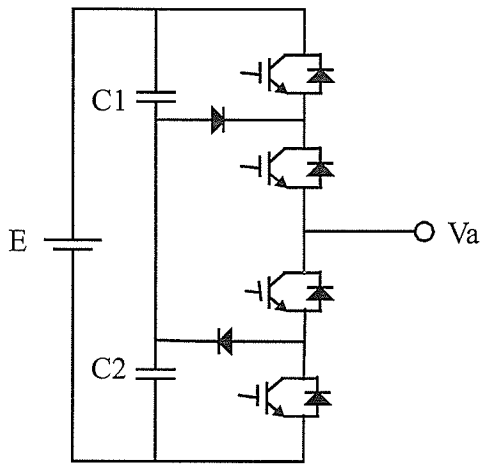


Fig. 2-15 One pole of a three-level inverter

connected capacitors (Fig. 2-15). In this case an additional control loop should be added to the system to keep the capacitor voltages at a constant level. At the output terminal, depending on which IGBTs are on, voltage Va can be equal to E, E/2 or zero. IGBTs can switch on and off only once per fundamental frequency cycle to produce a staircase waveform. This method of operation is called Fundamental Frequency Modulation (FFM). Different types of pulsewidth modulation schemes can also be used to further improve the output waveform. The harmonic distortion at the output of multilevel inverters is much less than two level inverters, especially when higher number of levels are used. The higher number of components, higher losses and more complicated control are the main disadvantages of this type of inverter[21].

2.3.10 Current-controlled inverters

Current-controlled voltage-source inverters [23] are often used in drive systems. Here a voltage-source inverter works in closed loop to maintain the output current as close as possible to a reference (time varying) value. Several different methods for controlling current can be used but the most common methods are linear control, hysteresis control, space vector current control, predictive current control and trajectory tracking control.

The *linear current control* (also called ramp comparison and suboscillation current control) consists of three independent proportional-integral (PI) controllers

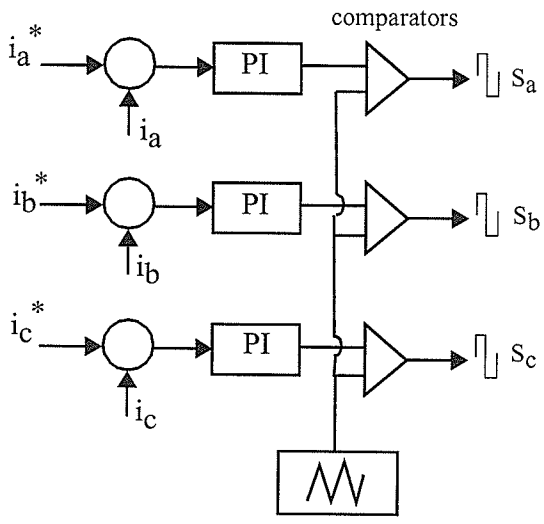


Fig. 2-16 Linear current regulator

that are employed to receive the current error and derive the reference voltage for a pulsewidth modulator. As usual the reference voltages are compared with a triangular carrier signal to produce three switching signals that control the three limbs of the inverter. This scheme has a fast response, but it has a steady-state current error (tracking error) when the reference currents are not constant. Fig. 2-16 shows the block diagram for a basic linear current controller.

In the *hysteresis-band control* scheme the current errors in the three phases are detected independently and when each of them exceeds an assigned band the corresponding inverter switches are commanded to change their state (Fig. 2-17(a)).

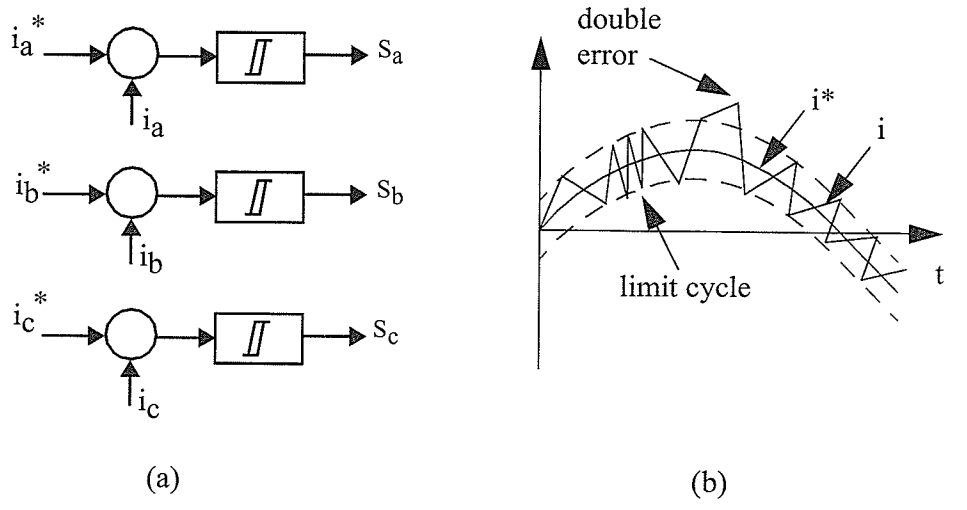


Fig. 2-17 Basic hysteresis current control: (a) controller block diagram, (b) waveforms

This control method is simple to implement and has a very good dynamic performance. The independent operation of the three phases and lack of any strategy to generate zero voltage vectors increases the switching frequency especially at lower modulation indices. Moreover, the current error is not strictly limited. The current can leave the hysteresis band whenever the zero vector is turned on and the load's back-emf vector has a component that opposes the previous active switching vector. At maximum the current error can be twice the size of the hysteresis band (Fig. 2-17(b)).The inverter has also a tendency to lock into limit cycle high-frequency oscillation when the frequency of the reference current signal is low.

The *space vector current control*, like the linear current control, compares the reference and actual currents to produce a reference voltage through a PI controller. This reference voltage is then sampled and applied to a space vector controller which will in turn control the inverter. Similar to the linear current control, there is a steady-state current error here. This error can be reduced by using a model of the load (usually a machine) to estimate the back-emf. The function of the current controller is then basically reduced to correct minor errors caused by a mismatch of model parameters or the model structure [24].

Another possibility in the space vector scheme is to use a look-up table instead of the PI controller. In this method the objective is to either limit the magni-

tude $|\Delta i|$ and angle $\arg(\Delta i)$ of the current error vector or its components Δi_α and Δi_β. Once a limited quantity reaches its boundary value the current switching state is terminated. The next state is then read from a look-up tableaus table is addressed by the error vector and/or the actual switching state vector [25].

The *predictive current control* method has common elements with the look-up table method discussed above. The time of switching is determined by suitable error boundaries. When the current error vector touches the boundary line, the inverter changes its switching state. To select the optimal switching state, trajectories of the current vector in the next time step and the time required to reach the next error boundary is predicted for all potential switching state vectors. Predictions are based on a simplified model of the load (usually a machine). Finally the switching state vector which produces the maximum on-time is selected. This procedure minimizes the switching frequency.

The *trajectory tracking control* method combines an off-line optimization for steady state operation and an on-line optimization during the transients. When the system is in steady state, the actual current vector is compared to its reference value and the error is fed to a PI controller to produce a reference voltage vector. The magnitude of this vector is used to select an optimal switching pattern from a look-up table. This look-up table contains a set of pre-calculated switching patterns

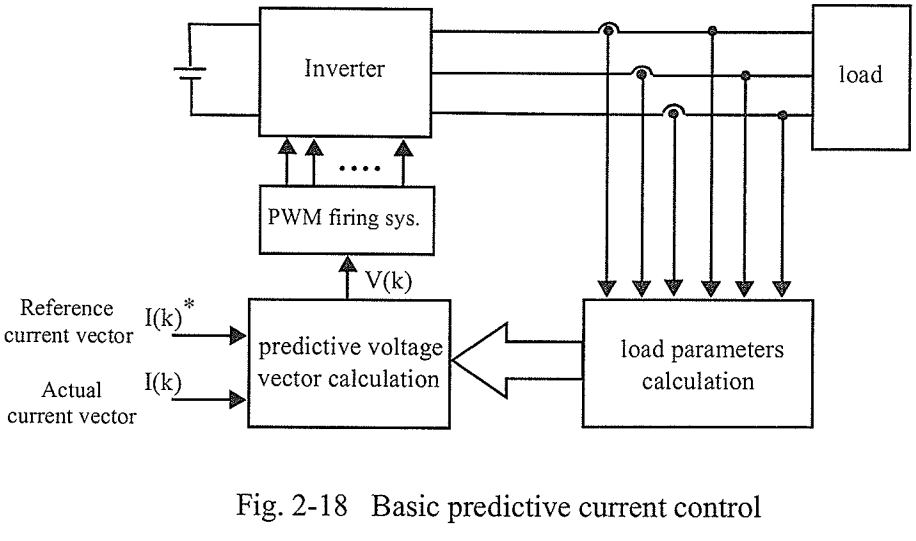


Fig. 2-18 Basic predictive current control

for different values of voltage magnitudes which will minimize the harmonic distortion of the load current under the steady state. Using a simplified model of the load and the selected switching pattern, the steady state harmonic current is calculated and compared to the actual value to detect transients. During the transient an on-line optimal tracking procedure modifies the switching patterns to minimize the transient harmonic current [27-28].

2.4 STATIC VAR COMPENSATORS

Reactive power compensation is one of the major applications of voltage source converters in the power transmission and distribution industry. Power utilities are particularly sensitive about the harmonics injected into their networks as it can affect a large number of consumers as well as the utility's equipment. Therefore it is important to reduce the harmonic content of the compensator output by adapting improved switching techniques. The neural network controlled optimal PWM technique suggested in this project was applied to advanced static VAR compensator and showed considerable improvement (chapter 5). This section briefly introduces the basic operation principles of the most common types of static VAR compensators.

Reactive power compensators are used in power transmission and distribution systems primarily to control the voltage level. They can also facilitate the active power transmission control and power oscillation damping. Reactive power compensation can be achieved by connecting reactors or capacitor banks to the system via circuit breakers. But this type of control has two drawbacks: circuit breakers are not fast enough to respond to the fast system transients and the reactive power can only be changed in steps. Using a synchronous condenser solves both of these problems as it is faster and can change its reactive power output linearly over a wide

range of capacitive and inductive values. But this is actually a rotating machine and like other electromechanical equipment needs expensive maintenance. Availability of modern power electronic switches has made it possible to replace these equipment with fast, reliable reactive power compensators that are less expensive and can be controlled more easily.

2.4.1 Conventional Static Var Compensator (SVC)

A conventional Static VAR Compensator (SVC) consists of one or more Thyristor Switched Capacitors (TSC) and one or more Thyristor Controlled Reactors (TCR) as shown in Fig. 2-19. TCR simply consists of a reactor and a thyristor valve. The reactor is usually divided into two parts with the thyristor valve in be-

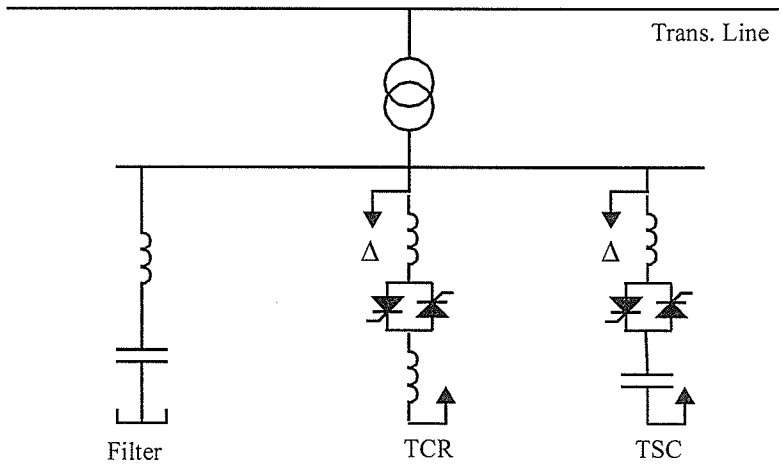


Fig. 2-19 Conventional Static Var Compensator

tween. This is to limit the fault currents flowing through the valve if a short circuit occurs at the reactor's terminals. TSC is basically a capacitor bank which is connected to the network by a thyristor switch. A small inductor is usually put in series with the capacitor to limit the valve current when there is a considerable difference between the capacitor voltage and the bus voltage when the thyristors are fired (in-rush current). The capacitor bank is fully connected to the network once the thyristors are fired, and is disconnected as soon as the firing pulses are stopped. Since current leads the voltage in a capacitor, it is impossible to change the capacitor current through the firing angles of the thyristors unless GTOs are used instead of thyristors. For the TCR on the other hand, the amount of the absorbed reactive power can be controlled continuously between zero and full capacity by changing the firing angles of thyristors from 90^{O} to 180^{O}. When the TCR operates at firing angles between the two limits, its currents are not sinusoidal and contain large amounts of 5th, 7th, 11th etc. harmonics necessitating the use of a number of filters. When a TSC and a TCR are installed in parallel, the reactive power can be controlled continuously from full capacitive to full inductive levels. When the required reactive power is capacitive and less than the TSC capacity, the TSC is connected to the network and the firing angle of TCR is controlled to absorb the difference between the required reactive power and the TSC capacity.

2.4.2 Static Synchronous Compensator (STATCOM)

The STATCOM is an electronic equivalent of the synchronous compensator which controls reactive power by means of adjusting a voltage source behind a synchronous reactance [29]. A STATCOM is basically a three-phase voltage source inverter which is connected to a small capacitor on the dc side. The ac side is connected to the ac network through an inductance which is usually the leakage inductance of a transformer. Fig. 2-20 shows the basic configuration of a STATCOM.

Under steady-state conditions the inverter converts the dc voltage of the capacitor into three ac voltages. The fundamental frequency component of these voltages are kept in phase with the ac network voltages (after considering the possible

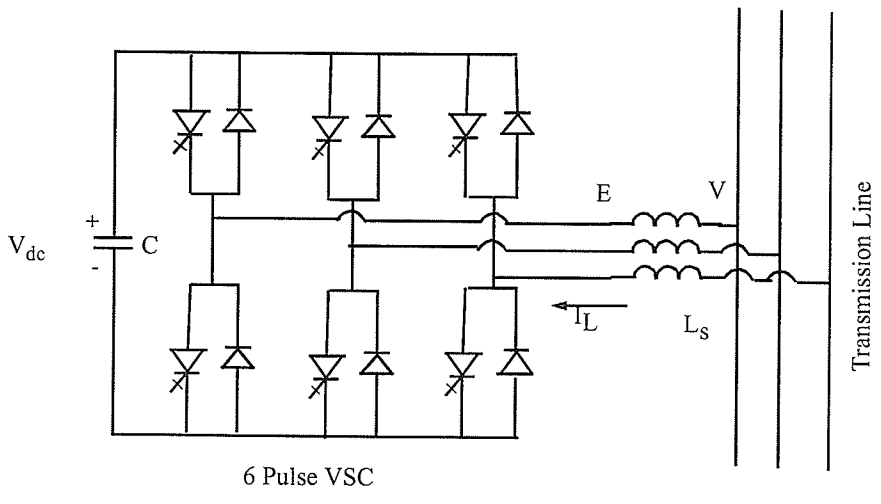


Fig. 2-20 Basic configuration of a STATCOM

phase shift caused by the transformer). If the line side magnitude of the inverter voltage (fundamental frequency component) is less than the transmission line voltage, the current flowing into the inverter will lag the transmission line voltage. In fact if the resistances of the inductors are neglected, this current will be pure inductive and lag the voltage by exactly 90 degrees. Similarly, if the magnitude of the inverter voltage is larger than the transmission line voltage, a capacitive current will flow into the inverter. The difference between the magnitudes of the inverter voltage and the line voltage determines the magnitude of the STATCOM current and therefore the amount of the reactive power generated or absorbed by it. When the inverter voltage is small, the STATCOM absorbs a large amount of reactive power. As the inverter voltage becomes larger, it absorbs less and less reactive power until the point where the magnitudes of the inverter and line voltages are equal and the reactive power is zero. Further increase in the inverter voltage will cause an increase in the STATCOM reactive power. These conditions are quite similar to the operation of the synchronous compensator in under-excitation and over-excitation modes and hence the rational for the name STATCOM. Fig. 2-21 shows the phasor diagrams for a STATCOM with negligible losses in the inductive and capacitive modes of operation. Here V is the transmission line voltage phasor, E is the fundamental frequency component of the inverter voltage, I_L is the fundamental frequency component of the STATCOM current (positive when flowing into the

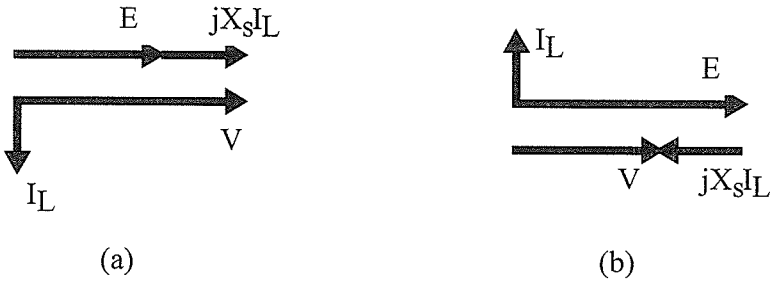


Fig. 2-21 Phasor diagrams for a STATCOM in the steady state. (a) inductive mode, and (b) capacitive mode

STATCOM) and X_SI_L is the voltage drop over the inductors (usually the leakage inductance of the transformer).

As long as the inverter and transmission line voltages are in phase, the STATCOM current remains at right angles with respect to these voltages and no active power is exchanged between the STATCOM and the system. But if E leads V by a small angle (less than 90^o), the angle between V and I_L will be more than 90^o and therefore real power will flow from the STATCOM into the transmission line. This will reduce the voltage across the dc capacitor as it is the only source of power in the STATCOM. Similarly, if the inverter voltage E lags the line voltage V, the STATCOM absorbs real power from the line and the dc capacitor will be charged. Fig. 2-22 shows the phasor diagrams for the STATCOM in two extreme situations where it absorbs or delivers pure active power.

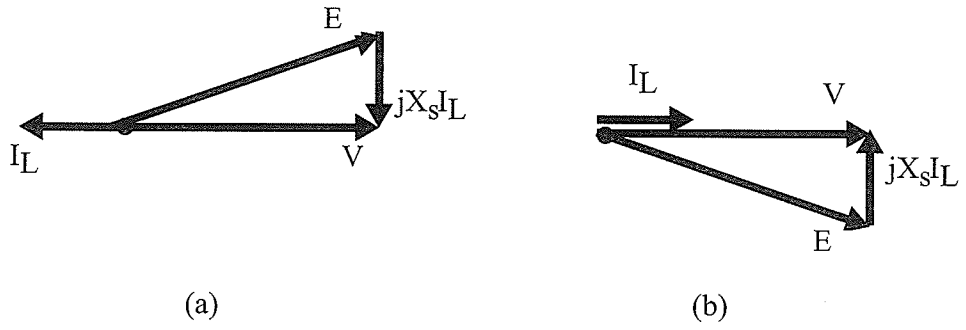


Fig. 2-22 Phasor diagrams for the STATCOM when it is (a) delivering pure active power, and (b) absorbing pure active power

Increasing or decreasing the dc voltage will affect the magnitude of the ac side voltage E of the inverter, which in turn controls the amount of the reactive power generated or absorbed by the STATCOM. This mechanism of charging and discharging the dc capacitor is used in most STATCOM control schemes as the principal mechanism of controlling the reactive power output. Pulse-width modulation is an alternative method to change the inverter output voltage and hence the reactive power without changing the capacitor voltage. This method will be discussed in more detail in the following chapters.

2.4.3 Comparison between SVC and STATCOM

In conventional SVC reactive power is generated or absorbed by energy-

saving components i.e. capacitors and inductors. The amount of the reactive power output of the SVC is limited by the ratings of these components. In the STATCOM on the other hand, it is not the energy-saving components that generate or absorb the reactive power. Here the reactive current is actually "exchanged" between the three phases such that in the ideal case there is no current flowing into the dc capacitor. The dc capacitor's function is to keep the voltage ripples at an acceptable level. This is a great advantage for the STATCOM in terms of the size and cost of the components. But the drawback is that the voltage source inverter in the STATCOM depends on GTO or other self-controlled electronic switches. Compared to thyristors, these switches are generally more expensive, more difficult to control and have lower ratings and more losses. Furthermore, series connection of self-controlled switches is generally more difficult than for thyristors.

From the power system point of view, the major difference between the SVC and the STATCOM is in their voltage-current characteristics in the over-voltage and under-voltage regions. As shown in Fig. 2-23, the maximum current that an SVC can draw from the network depends linearly on the network voltage. This is because at the extreme operating points, the SVC is essentially a constant impedance and therefore its current depends linearly on the voltage. A STATCOM on the other hand can carry its rated current over a wide range of under-voltage and over-

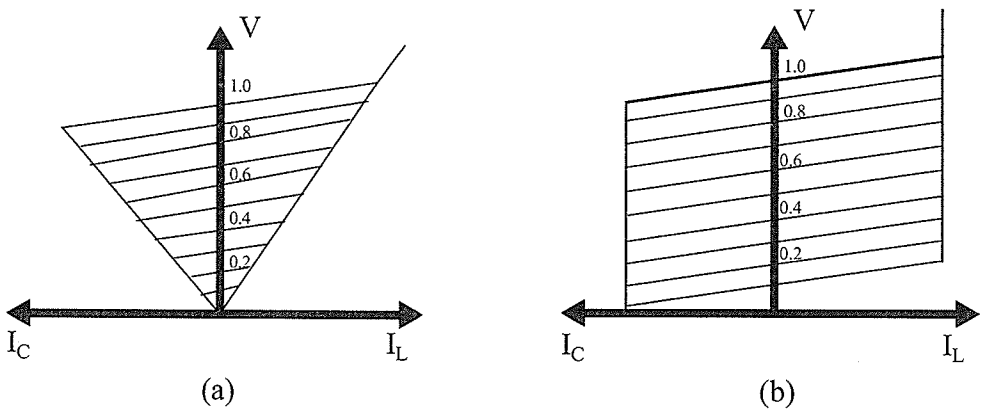


Fig. 2-23 Voltage-Current characteristics for (a)SVC and (b)STATCOM

voltage conditions. If the network voltage drops, the output voltage of the inverter in the STATCOM can be reduced accordingly, so that its current remains at the desired level.

2.4.4 Multi-pulse and quasi multi-pulse STATCOMs

The voltage-source inverter used in the STATCOM generates some harmonic voltages at its ac outputs. This causes some harmonic currents to be drawn from the network. Modern day STATCOMs utilize the harmonic cancellation techniques discussed earlier (multi-pulse or quasi multi-pulse) so that no significant ac filtering is required. Note that if ac filters are introduced, they could impact negatively on the dynamic performance of the device.

The simplest multi-pulse scheme is used in the 12-pulse STATCOM. In this scheme two 6-pulse square wave inverters are connected to a common capacitor on the dc side as shown in Fig. 2-24. On the ac side, inverters are connected to the secondary windings of two separate YY and YΔ transformers. This arrangement is very similar to the 12-pulse rectifier that introduced in section 2.2.2, but here the primary sides of the transformers are connected in series to allow adding the two voltages rather than the two currents. The firing pulses of the upper and lower inverters are phase shifted by 30^{o} with respect to each other so that the fundamental frequency voltages at the primary sides of the transformers are in pheasants causes the 5th and 7th harmonics of the inverter voltages are also phase shifted with respect to each other by 150^{o} and 210^{o} respectively. The YΔ transformer adds an extra 30^{o}

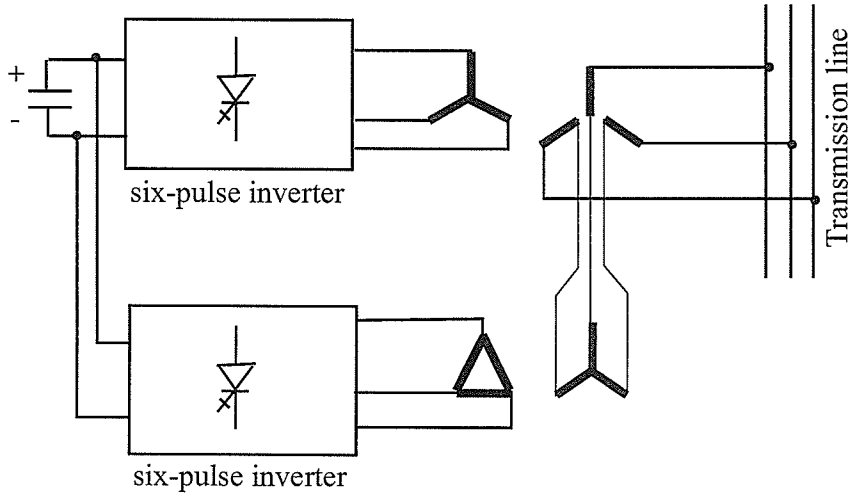


Fig. 2-24 Twelve-pulse STATCOM

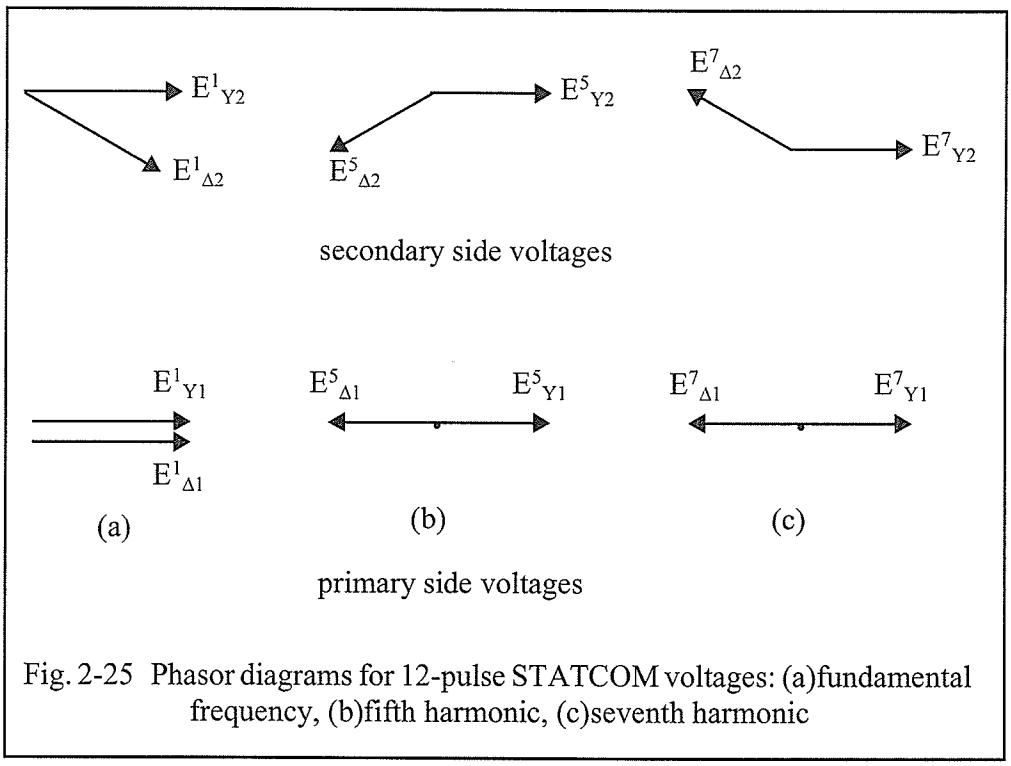


Fig. 2-25 Phasor diagrams for 12-pulse STATCOM voltages: (a)fundamental frequency, (b)fifth harmonic, (c)seventh harmonic

phase shift to the 5th harmonic but for the 7th harmonic it reduces the phase shift by 30^{O}. This is because the three phase 5th harmonic voltages are in negative sequence while the 7th harmonic voltages are in positive sequence, and the transformer's phase shift is in the opposite direction for the positive and negative sequence voltages. Thus on the primary side of the YΔ transformer both the 5th and 7th harmonic voltages are 180^{O} out of phase with respect to the YY transformer as shown in Fig. 2-24. As a result, the 5th and 7th harmonics generated by the two inverters cancel each other and the fundamental components add up.

Similar to the 12-pulse STATCOM, four six-pulse inverters can be connected to each other to make a 24-pulse STATCOM that contains no 5th, 7th, 11th and 12th harmonics in its output. In this case the firing pulses of each inverter must be 15^{o} phase shifted with respect to the next one. To make sure that the fundamental voltages of the inverters add up and the above harmonics are truly cancelled out at the network side, the transformers should provide similar phase shifts between their primary and secondary voltages. Zero and 30^{o} phase shifts can be achieved by using YY and YΔ transformers, but for other phase shifts the zigzag configuration must be used. The leakage reactance of all four transformers must be equal to guarantee their equal contribution to the reactive power generated (or absorbed) by the STATCOM. This is hard to achieve with zigzag transformers. The 48-pulse STATCOM similarly consists of eight six-pulse inverters with firing pulses phase shifted by 7.5^{o} with respect to each other and transformers that provide similar phase shifts between their primary and secondary voltages. The harmonic contamination at the output of this STATCOM is very low, because all the characteristic harmonics up to the 47^{th} are removed. The 48-pulse STATCOM is particularly attractive in high-power applications because compared to lower-pulse-number arrangements, it can use inverters with lower ratings. This reduces the need for series connection of switches (usually GTOs) and therefore reduces the cost and power losses in inverters. But using zigzag transformers with different phase shifts is the main problem

with this type of STATCOM.

The quasi multi-pulse technique [30] eliminates the need for the complicated transformers, but the drawback is that it allows a small amount of the characteristic harmonics to appear in its output voltage. In this approach, the harmonic

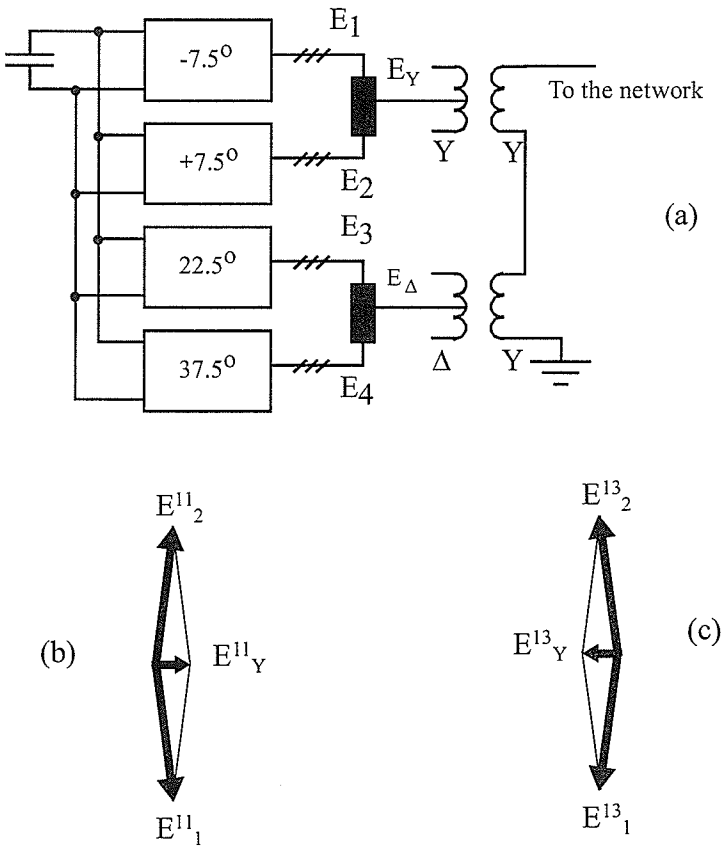


Fig. 2-26 The structure and phasor diagrams for a quasi 24-pulse STATCOM (a) converter connections with inter-phase inductors, (b) eleventh harmonic and (c) thirteenth harmonic phasor diagrams

voltages generated by the inverters do not cancel completely when the inverter voltages are added up, but the magnetic system is much simpler in this case. Fig. 2-26 shows one possible structure for the quasi 24-pulse STATCOM. The firing pulses of the first two converters are phase shifted by + and -7.5^{O} with respect to the network voltages. Therefore the eleventh harmonics are at ±7.5x11= ±82.5^{O}and the thirteenth harmonics are at ±7.5x13=97.5^{O} with respect to the same reference. The output voltages of the two inverters are added together by means of inter-phase inductors. Two YY transformers with series connected secondaries could also be used instead of these inductors. At the output of the inter-phase inductors the magnitude of the 11th and 13th harmonic voltages are only 13% (cos82.5^{O}=0.13) of their original values. The same technique is used in the third and fourth inverters to reduce the magnitude of the 11th and 13th harmonics, but the firing pulses of these inverters are 30^{O} ahead of the first and second ones. This in combination with the YY and YΔ transformer arrangements will remove the fifth and seventh harmonics just like in the 12-pulse STATCOM. Higher pulse number STATCOMs can be constructed similarly, i.e. a quasi 48-pulse STATCOM which adds up the output voltages of eight inverters to effectively reduce the magnitude of all harmonics up to the 47th to negligible levels [32].

2.5 CONCLUSIONS

In this chapter we studied the most commonly used power electronic devices including the thyristor, the triac, the GTO, the IGBT, the power MOSFET and the IGCT. The advantages and drawbacks of each component was briefly discussed along with the maximum ratings and common applications. Then a number of rectifier configurations, including the multipulse and two-step converters, were introduced and the waveform quality in each case was discussed. The main emphasis of the chapter was on the dc to ac converters (inverters) and the harmonics reduction methods used in them. Several variations of pulse width modulation technique was explained and their relative advantages were discussed. This paves the ground for a better understanding of the optimal PWM method which is the main technique used in this project. The operating principles of STATCOM was also briefly discussed as we will use our neural network controlled optimal PWM technique in this particular application in the following chapters. The next chapter will briefly introduce the basic principles of neural networks. This will provide the required background for the following parts of this thesis that are dedicated to the voltage source converters with the neural network controlled optimal PWM as the switching method.

CHAPTER 3

ARTIFICIAL NEURAL NETWORKS

Artificial neural networks have been used in a broad range of applications. These include pattern classification, pattern completion, function approximation, optimization, prediction, and automatic control. In this project an artificial neural network has been used to control the switching angles of a voltage source converter in such a way that certain selected harmonics are eliminated from the output voltage. This chapter provides a short introduction to the artificial neural network with emphasis on the particular type of the network and training methods used in this project.

A large number of network paradigms, each with its own distinctive name, have been introduced. But despite appearances, all artificial neural networks perform essentially the same function: They accept a set of inputs (an input vector) and produce a corresponding set of outputs (an output vector), an operation called vector mapping. Likewise, all neural network applications are special cases of vector mapping [33].

A neural network essentially consists of a number of interconnected processing cells, usually called neurons. Neurons receive inputs from each other and from the outside world (the input vector) and send their outputs to the other neurons and to the outside world (the output vector). Each neuron applies a simple mathematical function like a polynomial or a sigmoid or just a scaling factor to its inputs. The link between each pair of neurons has a weight, i.e. the output of each neuron is multiplied by a factor before being applied to the next neuron. These weights act as free variables in the network that by assuming a certain set of values cause the network to do a particular mapping. Fig. 3-1 shows the block diagram of a typical neuron with sigmoid characteristic.

The mapping relationship between input and output vectors may be static, where each application of a given input vector always produces the same output vector, or it may be dynamic, where the output produced depends upon previous, as

well as current, inputs and/or outputs. Different network paradigms vary greatly in the range of mappings that they can represent. Determining the representational limits for each network type is currently an active area of research. However, it has been proved that for the feed-forward networks with one hidden layer the functional relationship between the input and output vectors may be, for all practical purposes, arbitrarily complicated [34]. In other words, without changing internal topology, this kind of network is capable of producing any functional relationship likely to be encountered by changing its weights. However, this proof doesn't determine any limit on the number of hidden units required to achieve a certain mapping.

Artificial neural networks learn from experience. This characteristic, perhaps more than any other, has created the current interest in these methods. Learning offers a powerful alternative to programming. Learning methods may be broadly grouped as *supervised* and *unsupervised*, with a great many paradigms implementing each method. In supervised learning, the network is trained on a training

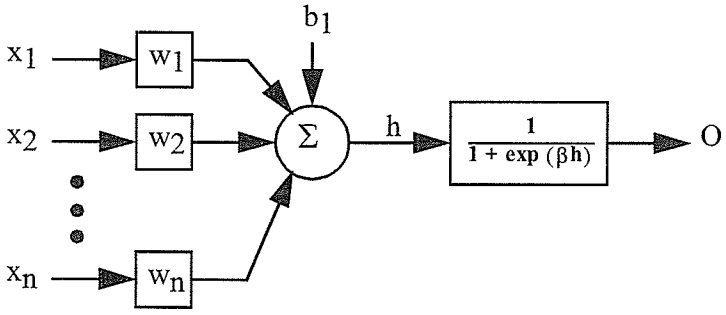


Fig. 3-1 A typical sigmoid neuron

set consisting of vector pairs. One vector is applied to the input of the network; the other is used as a 'target' representing the desired output. Training is accomplished by adjusting the network weights so as to minimize the difference between the desired and actual network outputs. This process may be an iterative procedure, or weights may be calculated by closed-form equations. Unsupervised learning, sometimes called self-organization, requires only input vectors to train the network. Here the neural network is presented with sets of input data, and the network classifies these input sets into categories. This classification is achieved by an algorithm that extracts statistical regularities from the training set, representing them as the values of network weights.

The *feed-forward* ANN trained by the *back propagation* method (or one of its many variations) is the most commonly used neural network. As shown in Fig. 3-2, in this type of ANN neurons are arranged in several layers. Each neuron receives input from all the neurons in the previous layer(s), but not from the other neurons in the same layer or those in the next layers. The first layer, usually called the input layer, receives the input vector and simply transfers that to the next layer without making any changes. The outputs of the neurons in the last layer are considered as the output vector. There are usually one or two layers of neurons between the input and output layers which are called hidden layers. Transfer functions of the neu-

rons of the output layer and hidden layer can be different, but the backpropagation method requires them to be differentiable in their whole range except possibly for a countable number of points.

3.1 THE BACKPROPAGATION TRAINING METHOD

Training of a feed-forward network means minimizing an error measure between the output vector and the target vector over the whole training set. The backpropagation method is essentially a computationally simple technique of calculating the gradient of the output error with respect to the network weights. Assume that x is the input vector to the network and $\mathbf{W_1}$ is the matrix of all the weights

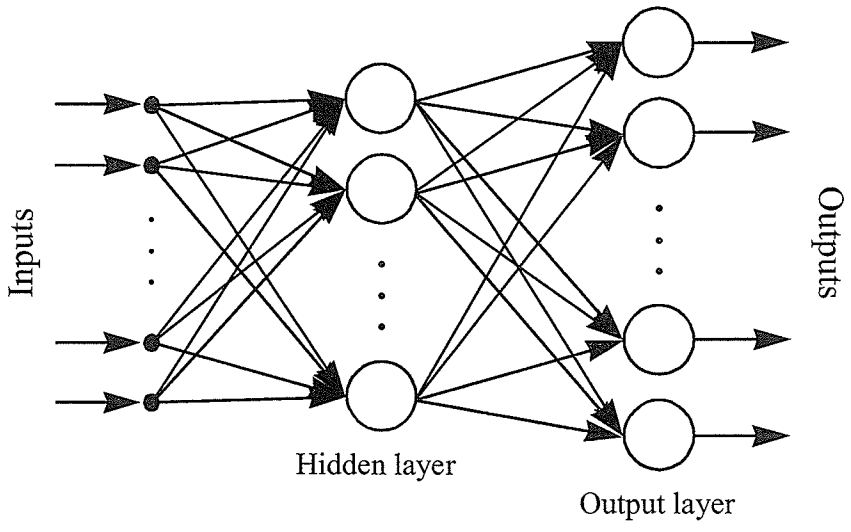


Fig. 3-2 A feed-forward neural network with one hidden layer

between the input layer and the first hidden layer. The subscript 1 shows that the weights are connected to the first layer. Then the output of the hidden layer is given by:

$$\mathbf{y}=f(\mathbf{x}\mathbf{W}_1) \tag{3-1}$$

where $f(.)$ is the vector of transfer functions of neurons in the hidden layer and operates on the product in a component-by-component fashion. To simplify the analysis we assume that the outputs of the final layer neurons are linear combinations of the hidden layer outputs. Therefore the output of the network is

$$\mathbf{out}=f(\mathbf{x}\mathbf{W}_1)\mathbf{W}_2 \tag{3-2}$$

where $\mathbf{W}_2$ is the matrix of all weights between the hidden and output layers.

The error measure for the output vector **out** is defined as

$$\text{sse} = \sum_i \left[(\mathbf{t}_i - \mathbf{out}_i)^2 \right] \tag{3-3}$$

where i is the number of components in the output vector and **t** is the target vector. Alternatively, the error may be averaged over the entire training set, in which case the error measure is

$$\text{sse} = \frac{1}{n}\sum_n \sum_i \left[(\mathbf{t}_i - \mathbf{out}_i)^2 \right] \tag{3-4}$$

where n is the number of training vectors in the training set. Now the gradient of the error with respect to the weights in the output layer is

where y_j is the output of the j^{th} hidden neuron. For the weights in the hidden layer

$$\nabla jk = \partial sse/\partial w_{2,jk} = (\partial sse/\partial out_k)\,[\partial out_k/\partial w_{2,jk}]$$
$$\partial sse/\partial out_k = -2\,(t_k - out_k)$$
$$\partial out_k/\partial w_{2,jk} = y_j$$
$$\nabla jk = -2\,(t_k - out_k)\,y_j \qquad (3\text{-}5)$$

the gradient is calculated as follows:

$$\nabla ij = \partial sse/\partial w_{1,ij} = \sum_k (\partial sse/\partial out_k)\,(\partial out_k/\partial y_j)\,(\partial y_j/\partial w_{1,ij})$$
$$\partial sse/\partial out_k = -2\,(t_k - out_k)$$
$$\partial out_k/\partial y_j = w_{2,jk} \qquad (3\text{-}6)$$
$$\partial y_j/\partial w_{1,ij} = f'\left(\sum_i w_{1,ij}\,x_i\right)\cdot x_i$$

This method can be easily extended to any number of hidden layers.

Once these gradients are in hand, many different optimization techniques can be adopted to minimize the error. In the original backpropagation method weights are updated at each iteration according to the following rule:

$$w_{jk}(n+1) = w_{jk}(n) - \eta \nabla jk \qquad (3\text{-}7)$$

where $w_{jk}(n)$ is the value of weight at n^{th} iteration and η is the learning rate. This method can, on certain problems, cause weights to oscillate rather than converge to a solution. To alleviate this, usually a momentum (similar to the acceleration factor used in load flow algorithms) is added to the weight update to make the weight change a function of the previous changes as follows:

$$w_{jk}(n+1) = w_{jk}(n) - \eta \nabla jk + \alpha\,(\Delta w_{jk}(n-1)) \qquad (3\text{-}8)$$

here $\Delta w_{jk}(n-1)$ is the change in the weight in the previous step.

The backpropagation method is a very slow training method. A large number of improved versions of backpropagation have been suggested to increase its speed and to reduce other problems associated with this method. However, since these methods are heuristic, their effectiveness is highly problem dependant. Here we present a few of these methods that are well tested on a large variety of problems and generally accepted to be beneficial in a wide range of applications.

The *Self-Adapting Backpropagation* (SAB) method [35] associates a separate step size (μ) to each weight which is adjustable during the training. At each training step, if a weight is changed in the same direction as the previous change its step size is increased. But if the direction of change is different from the previous step, the step size for that weight should be decreased. The Super SAB method is also based on the same rules, with an additional rule: if the direction of the current change is the opposite of the previous one, do not make this change and reverse the previous weight change. Using these simple rules, Super SAB can achieve training speeds 10-100 times faster than the original backpropagation.

The *conjugate gradient descent* methods [36], unlike the previous methods, do not proceed in the opposite direction of the gradient, but instead they proceed in

a direction which is *conjugate* to the direction of the previous step (preferably to all previous steps). The gradient on the current step stays perpendicular to the direction of the previous step. Such a series of steps is noninterfering, i.e. the minimization performed in one step is not partially undone by the next. Conjugate gradient methods approximate this conjugate direction by taking into account second derivative information that is not used by the backpropagation. The original conjugate gradient method requires the calculation of the second derivative matrix (Hessian) which is a computationally heavy task in addition to solving a set of n linear equations (where n is the number of weights). Instead, a number of clever methods have been devised to approximate a series of conjugate steps. These methods generally move in the direction of the gradient vector, but not with a fixed step size. Instead they do a line search to minimize the error function to find how far to move in this direction. For the quadratic surfaces this method converges to the minimum in n steps. In the areas close to the minimum usually the surface can be considered quadratic. But in the areas far from the minimum the behaviour is less predictable. Nevertheless conjugate gradient methods are generally much faster than backpropagation [33].

The original backpropagation suffers from a number of serious problems like requiring user to provide parameters like training rate and momentum that there is little theory for their determination, the high possibility of network paralysis i.e.

getting trapped in local minima or a flat area during the training, and long training time. The improved versions of the backpropagation method like super self-adapting and conjugate gradient descent are much faster and more reliable than the original method, but there are still two basic problems facing this method: there is no way to ensure that a solution is the best possible, and unpredictability of the network's output when an input vector is unlike any vector in the training set. Despite these problems, the feed-forward network trained by the backpropagation method is the base of most successful neural network applications.

CHAPTER 4

THE NEURAL NETWORK CONTROLLED OPTIMAL INVERTER

As mentioned earlier, minimizing the harmonic content of the output voltage (or current) is one the major concerns in the inverter design. In this chapter, design and implementation of an inverter will be discussed that eliminates the selected harmonics using optimal PWM. The control algorithm is implemented using ANN techniques as suggested by the author.

4.1 THE OPTIMAL PWM INVERTER

In a two-level PWM voltage source inverter the sum of the squares of all harmonics (including the fundamental) is always the same (Fig. 4-1):

$$\int_0^T V^2 dt = \sum_{i=1}^{\infty} V_i^2 = E^2 T \qquad (4\text{-}1)$$

where V_i is the RMS value of the i^{th} harmonic. So to improve the harmonics in the output voltage two approaches are possible:

1. Shift the harmonics to higher frequencies where it is easier to filter them out.

2. Increase, as much as possible, the amplitude of triplen harmonics in three phase systems without a neutral line. Since the triplen harmonics do not appear in the line voltage and current in these systems, this will not affect the load, but, as equation (4-2) suggests, this will reduce the amplitude of the other harmonics.

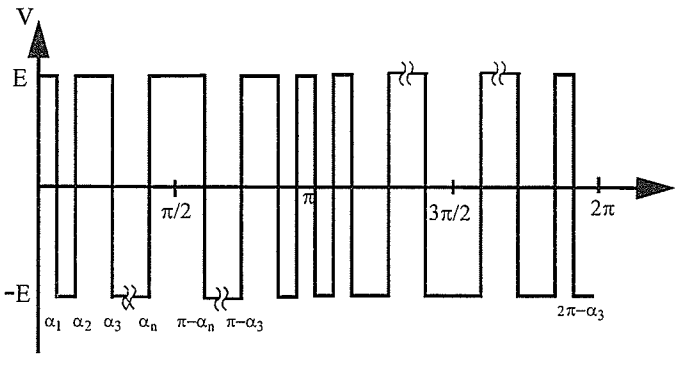


Fig. 4-1 A typical PWM waveform

In the optimal PWM technique [37] used in this project the first method is employed, however the optimization procedure does not put any constraint on the magnitude of the triplen harmonics, allowing them to attain whatever value which requires the elimination of the selected harmonics. The method is optimal in the sense that it uses the minimum number of pulses to achieve these goals. A great portion of power loss on the inverter switches happens during the switching actions because neither the voltage across nor the current through the switch is zero at this time. Therefore reducing the number of switching actions generally reduces the loss in the switches. This is of major concern especially in high power inverters.

In optimal PWM we normally select a waveform with odd and halfwave symmetries. This guarantees that there will be no even harmonics and simplifies the calculation of the amplitudes of the other harmonics. The amplitude (peak value) of the odd numbered harmonics for a PWM waveform with the above symmetries is obtained from the following equations.

$$\begin{aligned} V_1 &= \frac{4E}{\pi}\left[1-2\cos\alpha_1+2\cos\alpha_2-\ldots 2\cos\alpha_n\right] \\ V_3 &= \frac{4E}{3\pi}\left[1-2\cos 3\alpha_1+2\cos 3\alpha_2-\ldots 2\cos 3\alpha_n\right] \\ &\vdots \\ V_k &= \frac{4E}{k\pi}\left[1-2\cos k\alpha_1+2\cos k\alpha_2-\ldots 2\cos k\alpha_n\right] \end{aligned} \qquad (4\text{-}2)$$

where α_i is the i^{th} switching angle in the first quarter cycle (Fig. 4-1), V_1 is the amplitude of the fundamental and V_K is the amplitude of the k^{th} characteristic harmonic. To achieve the optimal PWM, in general we should set V_1 to the desired value, and the magnitude of all unwanted harmonics equal to zero and solve the resulting set of equations for $\alpha_1, \alpha_2, ..., \alpha_n$. Thus with n switchings per quarter cycle we will be able to determine the magnitude of fundamental and remove up to n-1 harmonics. An attempt to eliminate more harmonics will result in a set of equations where there are more equations than variables which most likely will not have a solution. On the other hand if the number of the eliminated harmonics is less than n-1, the number of equations is less than variables. This will give us the possibility to employ the unused degrees of freedom for other optimization purposes.

For a three phase system without a neutral line, the magnitude of the triplen harmonics are normally left floating. Analysis of the above set of equations using the Walsh Transform [38] shows that, if the number of the equations and number of switchings per quarter cycle are equal, then there are only two possible sets of solutions. The only difference between these two sets of solutions is the phase of the fundamental and harmonics, i.e. from the practical point of view they are equivalent. This means that the magnitude of the triplen harmonics will remain the same regardless of which set of solutions is selected. The triplen harmonics can also be

eliminated like other harmonics by adding the corresponding equations to the set of equations to be solved. The advantage of doing this is a reduction in the neutral point voltage of the transformer as explained later, but the disadvantages are higher switching frequency and possibly higher total harmonic distortion in the output ac current. This latter effect is because eliminating the triplen harmonics will increase the magnitude of the harmonics that are not eliminated as shown in equation (4-1).

The necessary and sufficient mathematical conditions for existence of a solution for equations (4-1) are not known to the author, but in most practical cases it is possible to find a solution. When the number of equations and unknowns are equal, many different algorithms can be used to solve the set of nonlinear algebraic equations (4-2). When solving a set of nonlinear equations, selection of the initial point is not always easy, as it has a considerable effect on the final solution and even on the convergence of the algorithm. Some authors [38] have suggested techniques based on the Walsh Transform to guarantee the convergence of the solution algorithm. The approach to this problem in this instance is to use the initial point $V_1=0$, $\alpha_i=\alpha_{i+1}=i\pi/2n$, i=1,3,...,n-1 if n is even (a similar result could be obtained if n is odd), then increase V_1 in small steps. At each step the solution of the previous step is used as the initial point. Fig. 4-2 shows a set of solutions obtained by the Newton-Raphson method and the above technique when n=5 and 5^{th}, 7^{th}, 11^{th} and 13^{th} har-

monics are eliminated, i.e. when in the following equations V1/E is set to different values from 0.01 to 1.16 in 0.01 steps and the set of five equations is solved each time for $\alpha_1 \ldots \alpha_5$:

$$\begin{aligned} V_1 &= \frac{4E}{\pi}\left[1-2\cos\alpha_1+2\cos\alpha_2-\ldots 2\cos\alpha_5\right] \\ V_5 &= \frac{4E}{5\pi}\left[1-2\cos 5\alpha_1+2\cos 5\alpha_2-\ldots 2\cos 5\alpha_5\right] \\ V_7 &= \frac{4E}{7\pi}\left[1-2\cos 7\alpha_1+2\cos 7\alpha_2-\ldots 2\cos 7\alpha_5\right] \\ V_{11} &= \frac{4E}{11\pi}\left[1-2\cos 11\alpha_1+2\cos 11\alpha_2-\ldots 2\cos 11\alpha_5\right] \\ V_{13} &= \frac{4E}{13\pi}\left[1-2\cos 13\alpha_1+2\cos 13\alpha_2-\ldots 2\cos 13\alpha_5\right] \end{aligned} \tag{4-3}$$

As can be seen in the typical graph of Fig. 4-2, when the magnitude of fundamental is increased beyond some limit, the adjacent firing angles reach each other and no solution can be found for the optimal PWM equations. The exact value of V_{1max} depends on the harmonics chosen to be eliminated. It was observed that in most of our cases (eliminating all harmonics except the triplens up to a certain order) the equations do not have a solution for the values of V_1 greater than 1.16pu, which is equivalent to a modulation index of 0.91. The problem of narrow pulses also appears for the values of V_1 close to zero. Therefore for practical usage of the optimal PWM we must set the upper and lower limits of V_1 to certain values lower than 1.16 and greater than zero respectively. The exact limits are calculated based

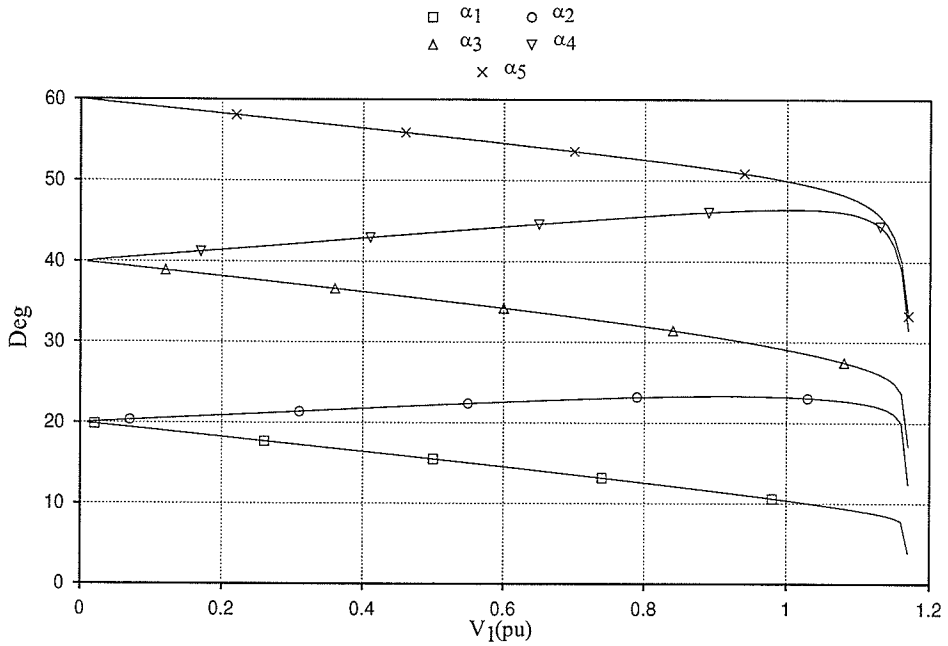


Fig. 4-2 Variation of α's as a function of V_1/E for n=5

on the capabilities of the switching devices and controller. The main limitations comes from the fact that a switching device must remain in on (or off) state for a certain time before it can be switched again. A short period of dead time is also necessary between switching off a device and switching on the opposite device on the same phase to avoid short circuitting the dc source. For high voltage converters the minimum on and off times for the valves and the minimum time between the switchings are in the range of tens of microseconds which implies a minimum pulse width in the range of 0.2 to 2 degrees in a 50Hz system. Obviously the firing pulse

controller can also add to this limitation if it is not of a higher speed. For a modulation index above 0.9 the governing equations do not have a solution and therefore it is not possible to eliminate the selected harmonics.

4.2 ACHIEVING OPTIMAL PWM USING AN ARTIFICIAL NEURAL NETWORK

The previous section showed that it is possible to completely remove a set of selected harmonics from the output of a PWM inverter. For real world implementation of this inverter we need a firing system that, for any desired value of V_1, alters the state of the switches at the corresponding angles obtained from Eq. 4-2. As can be seen from Fig. 4-2, firing angles α_i for an optimal PWM inverter are nonlinear functions of the fundamental component amplitude V_1. A few methods have been proposed to build a controller that changes the firing angles with V_1 according to these nonlinear functions. The first method is to approximate these functions with piecewise linear functions [38]. The method suggested in [39] uses the regular sampling PWM with a particular switching function to obtain a relatively good approximation of the optimal PWM. Another approach is to use a look-up table that associates each value of V_1 to a set of firing angles. To achieve the desirable level of accuracy, the look-up table must have a relatively large number of entries and use some kind of interpolation to deal with the inputs that fall between two table entries. In this thesis a new method is proposed that uses a feed-forward artificial neural network to map the normalized values of the fundamental component amplitude to the optimal switching angles. The training process of this network can be done off-line and only once; therefore the training time is not a matter of concern. Compared to

the common look-up table method, the neural network approach requires much less memory space but if a normal sequential processor is used for its implementation, its processing time is higher than the look-up table. A precise measurement of the processing time for the two methods is not included in this thesis because practical means to measure the processing times were not available at the time. Nevertheless, a rough comparison between the two method is possible based on the number of mathematical operations required in each case. Processing of a piecewise linear neuron consists of n+1 additions and n+1 multiplications and a few comparisons (n is the number of neurons in the previous layer) to find the weighted sum of the outputs from the previous layer, select the correct portion of the transfer function, and to apply the transfer function to the input. For a look up table on the other hand calculation of the outputs requires a comparison (to find the proper entry in the table) and two additions and a division for each output. Although floating point division is a time consuming operation for most processors, it seems that the neural network requires a longer processing time because all the above calculations must be performed for every neuron in the network. It is predicted that with the availability of low-cost parallel processing neural network chips in the near future, the processing time of the ANN will also be reduced. Although in principle the neural network processing time can put a limit on the maximum switching frequency of the PWM converter, the main limitation is imposed by the converter switching de-

vices. The maximum switching frequency for a single IGBT is currently 25kHz. For an IGBT valve consisting of several devices the maximum switching frequency is drastically reduced.

4.2.1 Firing angle control using a sigmoid ANN

The number of harmonics to be eliminated depends on the requirements of the load and the properties of the switching device used in the inverter. As the number of eliminated harmonics increases, the output current becomes closer to a pure sine wave, but the number of the switching actions increases at the same time and therefore the switching losses go higher. The higher number of pulses also means that they are shorter and hence breach the limit of the switching device when the frequency and amplitude of the fundamental component are lower. For the test cases used in this project we decided to eliminate all harmonics up to the 29^{th}. As explained in section 4.1, to be able to remove the eight non-triplen harmonics in this range and also determine the magnitude of the fundamental we require a minimum of nine switchings per quarter cycle of fundamental. The corresponding firing angles are found by solving nine equations as in Eq. 4-2 for k=1, 5, 7, 11, 13, 17, 19, 23 and 25. The switching frequency is therefore $59f_n$ where f_n is the fundamental frequency. This allows us to raise the fundamental frequency in our hardware prototype inverter up to 150Hz at maximum modulation index.

Fig. 4-3 shows the structure of a three-phase, two-level PWM inverter with the neural network firing angle control. The amplitude and frequency orders for the fundamental component of the inverter's output voltage are determined by a higher level controller. The neural network receives the desired amplitude and produces a set of firing angles that guarantee the elimination of unwanted harmonics while the amplitude of the fundamental remains at the ordered level. The firing circuit uses its frequency input and an internal time base oscillator to convert the firing angles to the actual firing times. The time base oscillator works at 33MHz and is an integral part of the processor board. These firing times are then used to generate the actual gate pulses. In power system applications (e.g. STATCOM) a phase-locked loop can be used to keep the inverter synchronized to the ac system.

As mentioned earlier, training of the neural network is carried out off-line. To provide the network with a proper set of input-output pairs as the training set, equations 4.2 were solved for values of V_1 from zero to 1.16E (highest possible value) with 0.01E steps. The set of all the solutions as well as the corresponding values of V_1/E form the training set for the neural network. Several other step sizes were also tried, but it was found that larger steps (less entries in the training set) will not give the desired accuracy and smaller steps (more entries in the training set) are not necessary as the accuracy criterion was met with the current step size. To evaluate

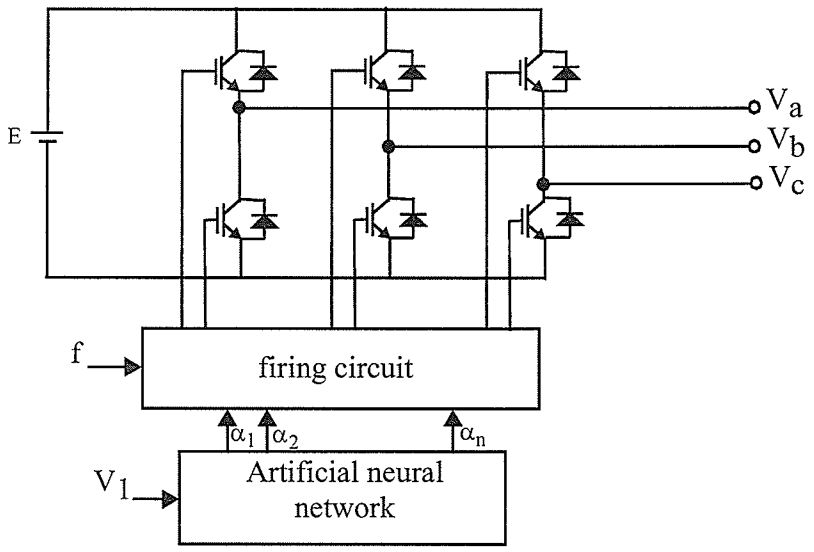


Fig. 4-3 Neural network controlled optimal PWM inverter

the network's behaviour, a set of one thousand input-output pairs were used as the test set.

It is well known that the optimal structure for a neural network that fits the requirements of a particular problem can only be found through experiment as there are no established methods to find this structure at the present time. Therefore in this project a number of neural networks with one or two hidden layers and different number of neurons in each layer were trained to find the simplest network with acceptable performance. Training of each network was repeated several times with

randomly selected initial weights to reduce the probability that the final error is a local minimum and not the global optimum and not a local minimum. The desired performance was that the maximum absolute error on the test set should be less than 0.1 degrees. In a 60Hz system this is equivalent to a maximum absolute error of 4.6 microseconds in turn-on and turn-off times of the inverter switches which is of the same order as the switching time of a GTO.

After experimenting with several neural network structures, the three layer (one hidden layer) network with five hidden neurons (i.e. five neurons in the second layer) was found to provide satisfactory results with the minimum number of neurons. Also results were best when a sigmoid characteristic was selected for the functional non-linearity. Direct connection from input to output neurons was also tested, but it did not improve the network's behaviour. The software tool used for training and testing the network was the Xerion software package which is a Unix based program developed by the University of Toronto [31].

From the many different training algorithms available in Xerion, the conjugate gradient method gave the fastest convergence and lowest possibility to get trapped in local minima. Conjugate gradient descent (see section 3.1) is a second order optimization method that does not proceed down the gradient of the objective function, but instead in a direction which is conjugate to the direction of the previ-

ous step (and preferably to all previous steps). Therefore the steps taken by this method are noninterfering, in the sense that the minimization performed in one step is not partially undone by the next step. Conjugate gradient methods approximate this conjugate direction by taking into account the second derivative information that is not used by back propagation [33].

Using the above training set and optimization method, a neural network was constructed that accepts normalized magnitude of the fundamental voltage of the inverter and provides the optimal firing angles at its outputs. Fig. 4-4 shows the theoretically exact values of two firing angles α_1 and α_2 and their calculated values from the neural network $\hat{\alpha}_1$ and $\hat{\alpha}_2$ as functions of normalized voltage magnitude. Note that the theoretically exact values can only be obtained after solving a complex, multi-order non-linear optimization problem, a process that is not easily implemented on line. Although the ANN takes a long time to train, once implemented, it produces these values very fast when presented with the fundamental voltage order. As can be seen there is a close match between the accurate and the estimated values and the criterion for the network accuracy is well satisfied.

To study the behaviour of the proposed neural network controlled optimal inverter, a complete three phase system including the inverter, firing circuit, neural network and load was simulated and analysed by the EMTDC/PSCAD transient

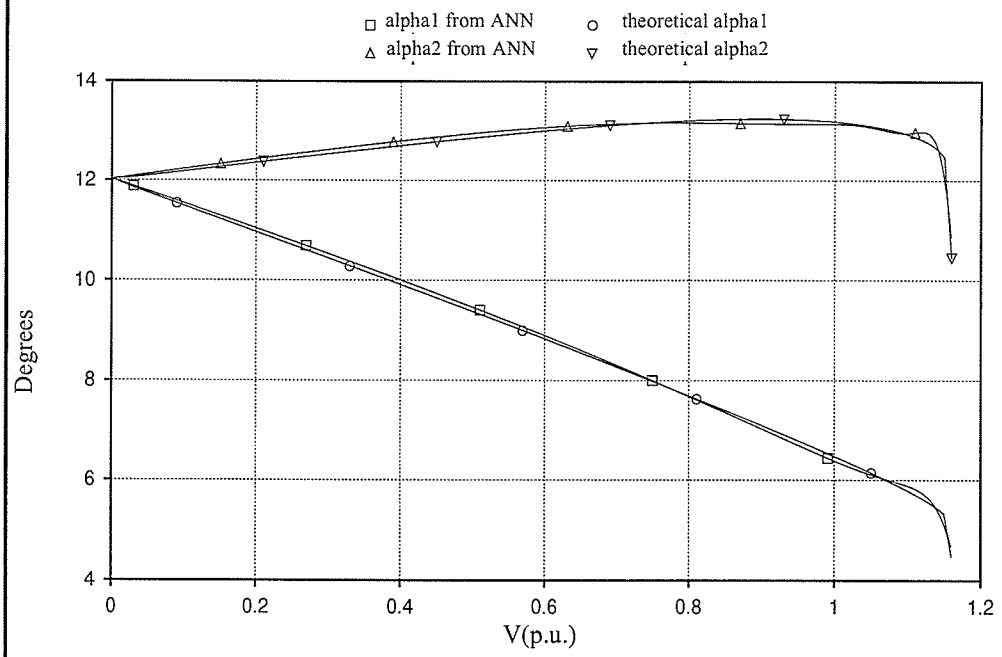


Fig. 4-4 Examples of the outputs of ANN along with the theoretical values of firing angles

simulation software package. This software package provides a library of ready-to-use models for most common electrical and control components such as those needed for constructing the inverter and firing circuit models. It also allows the user to easily add new models to this library in the form of FORTRAN subroutines. To be able to simulate an artificial neural network, a new component model for EMTDC/PSCAD was developed which receives the number of the input, output and hidden neurons as well as a set of weights as parameters (weights are read from a text file) and then calculates the firing angles based on its input voltage order.

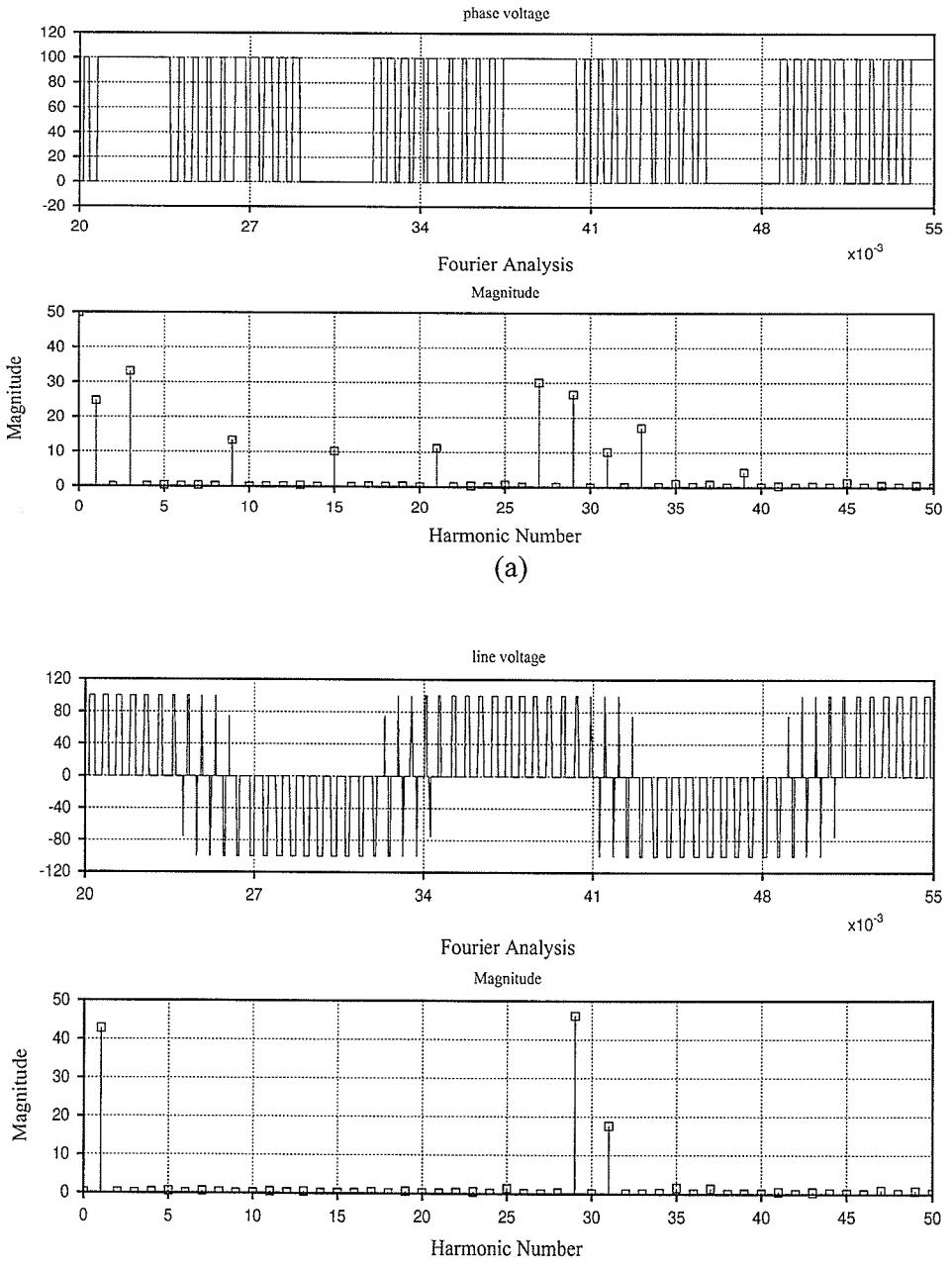
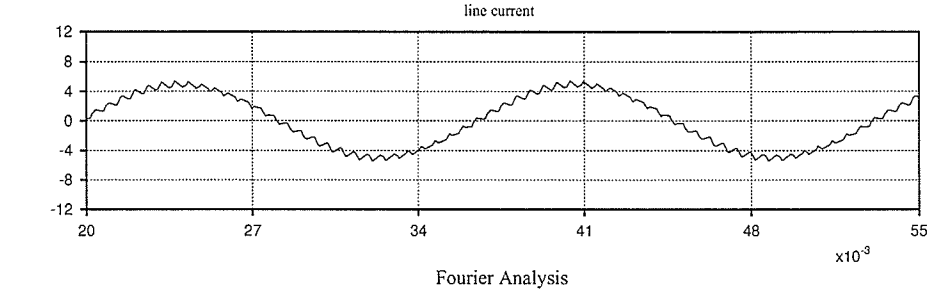
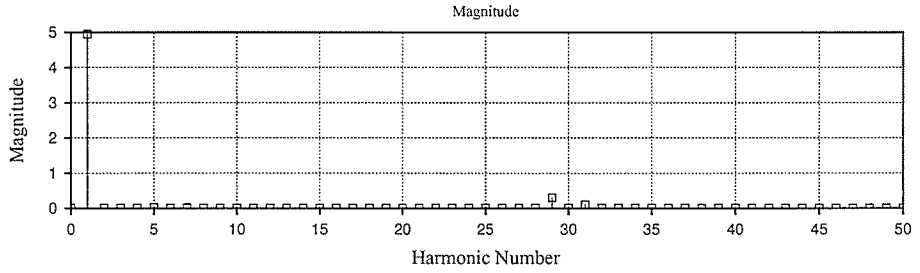


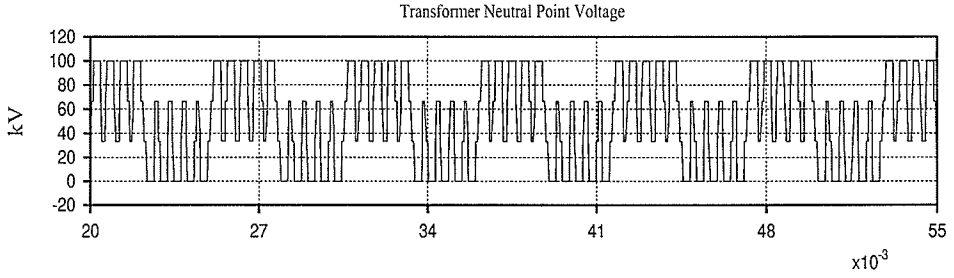
Fig. 4-5 Simulation results for ANN controlled optimal inverter when V_1=0.5pu: a) Phase voltage and Fourier analysis, b) Line voltage and Fourier analysis



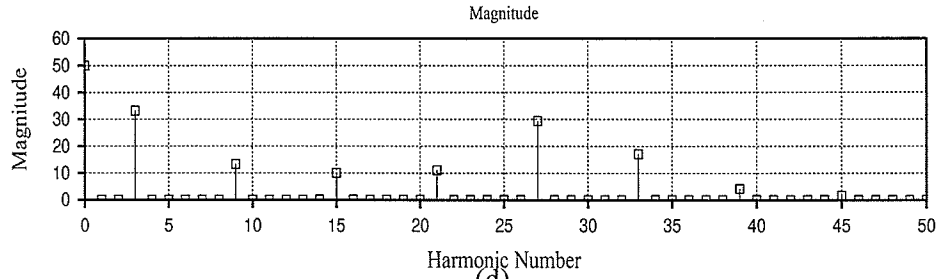
Fourier Analysis



(c)



Fourier Analysis



(d)

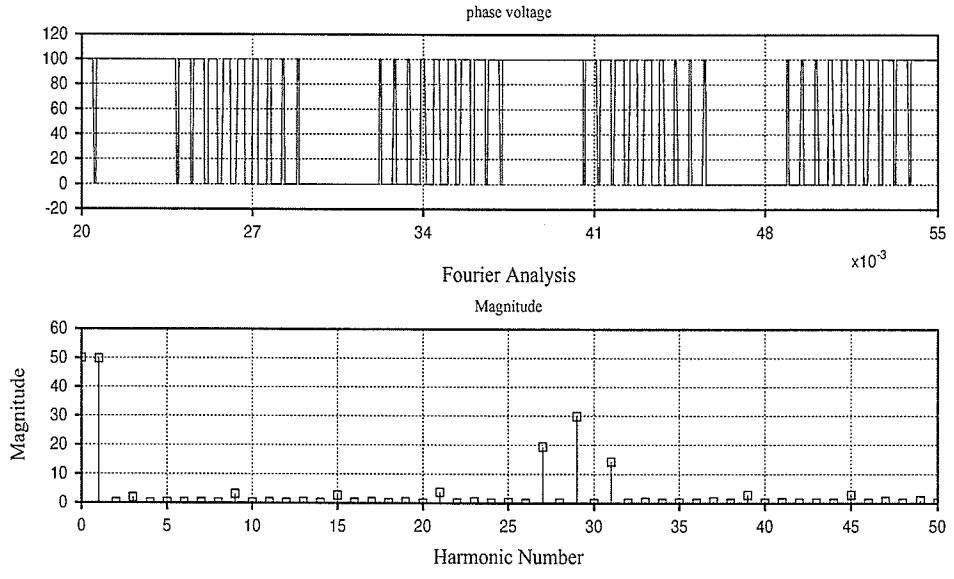
Fig. 4-5 Cont. c) Line Current and its Fourier analysis,
d) Neutral point voltage and its Fourier analysis

A number of simulations with different types of loads were conducted to verify the validity of the proposed method of harmonic reduction. Fig. 4-5 and Fig. 4-6 show the output voltage and current of the inverter and their Fourier analysis under steady state conditions for two sample values of V_1 of 0.5pu and 1.0pu respectively. The inverter load is modelled as a simple inductive impedance with a power factor of 0.8. The neural network with five hidden neurons mentioned earlier in this section is used to generate the required firing angles to remove non-triplen harmonics up to the 29^{th}. Since 9 switching per quarter cycle is used, the switching frequency is (9x2+1).(60)=1140Hz. As can be seen in these figures, all the non-triplen harmonics up to the 29th are totally cancelled in the phase voltages. Note that the middle point of the square markers are the actual values of the harmonics in these graphs. In the line voltages triplen harmonics disappear as expected and the lowest order non-zero harmonics are the 29th and 31st. Because of the inductive nature of the load, higher order harmonic voltages see larger impedances compared to the fundamental and therefore the harmonics are filtered out to a large extent. This causes the line current to have much less harmonic content than the voltage as can be seen in Fig. 4-5c and Fig. 4-6b. As mentioned at the beginning of this chapter, the sum of the squares of the amplitude of all harmonics is a constant value for a two level PWM signal. This is the reason that in Fig. 4-6, where magnitude of the fundamental is increased, voltage harmonics are much smaller.

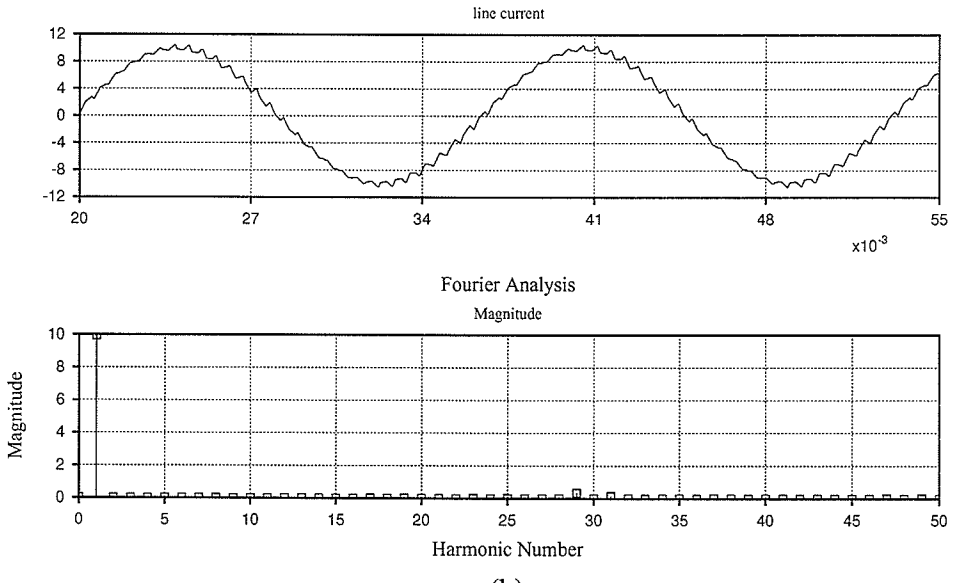
The voltage at the neutral point of the transformer secondary winding is the sum of all triplen harmonics in the three phases. Assuming that the low voltage side of dc capacitor is grounded, either directly or through an impedance, this voltage is equal to zero when the lower switching devices of all phases are on, and is equal to the capacitor voltage when all the upper devices are on. If two of the upper devices and one of the lower ones are on the neutral point voltage is 2/3 of the dc voltage and if two lower devices and one of the upper devices are on it is equal to 1/3 of the dc voltage. Fig. 4-5(d) shows the neutral point voltage and its Fourier analysis. As the magnitude of V_1 is reduced, the triplen harmonics become larger and the average neutral point voltage is increased.

4.2.2 Firing angle control using a piecewise linear ANN

The final goal in this project is to actually implement in hardware the optimal voltage source inverter with the proposed control scheme. As the special hardware in the form of an ANN chip which is able to perform the neural network computations in parallel was not available to us at the time the research was going on, we were forced to implement our neural network by conventional sequential processing units. Real time implementation of the sigmoid function will involve a large number of floating point operations including division and floating point exponent calculations. An alternative to this method is to replace the sigmoid charac-



(a)



(b)

Fig. 4-6 Phase voltage and current for V_1=E (1.0pu)

teristic function for neurons by a piecewise linear approximation of it (see Fig. 3-1 for neuron characteristic). The piecewise linear function does not need floating point exponential function and division calculations and therefore requires less processing time when implemented in real time. Obviously better results are expected when more line pieces are used. In this project using seven linear pieces showed satisfactory results. Adding more line pieces will reduce the error between the two characteristics, but at the same time will increase the amount of computations required to implement the new neurons in real time. Slopes and lengths of the line pieces were selected in a way that the integral of the square of the error between the sigmoid and piecewise linear graphs is minimized. Fig. 4-7 shows part of the sigmoid function and its piecewise linear approximation between -5 and +5.

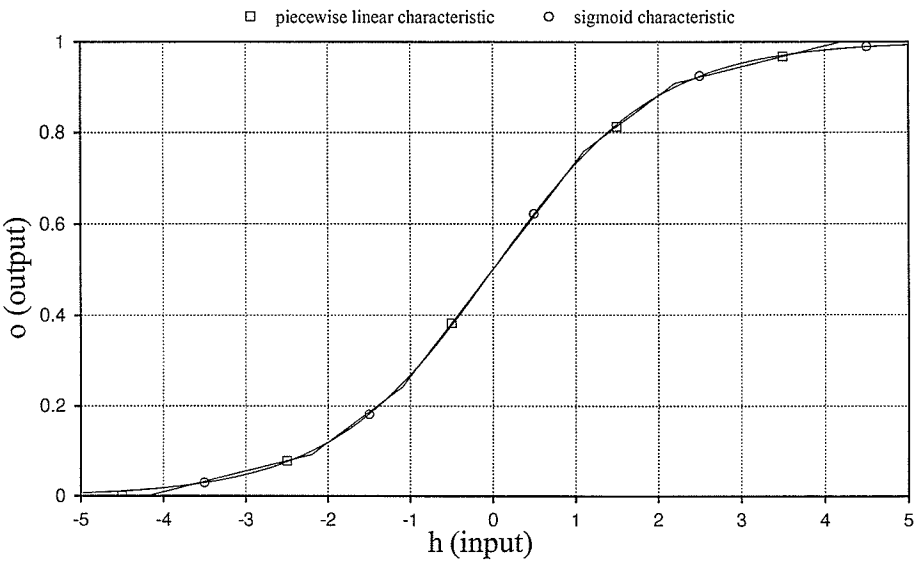


Fig. 4-7 Sigmoid and piecewise linear characteristics

The sigmoid characteristic was then replaced by the new piecewise linear characteristic for the neurons in a network which was already trained. As can be seen in Fig. 4-8, the resulting output firing angles are fairly close to the original values, but since the magnitude of harmonics in the output voltage is sensitive to changes in the α's, we have unacceptably large harmonics in the output. Fig. 4-9 shows the output voltage waveform and its spectrum for the system shown in Fig. 4-5 with the same magnitude for fundamental, but with the above piecewise linear characteristic for the neurons. As can be clearly seen, using this new characteristic causes an increase in the 5th, 7th, etc. harmonics from less than 1% to a maximum

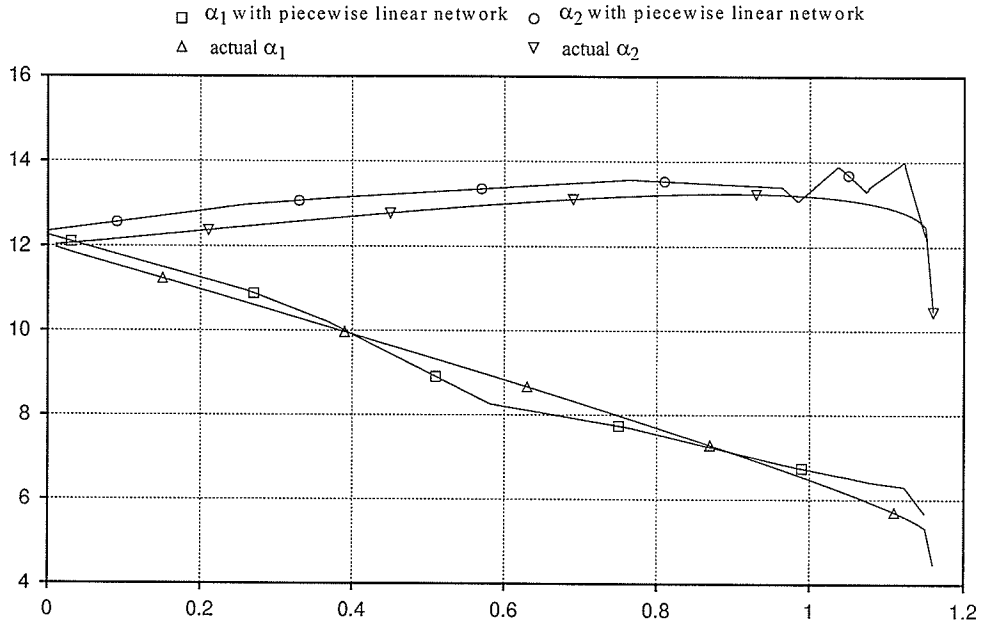


Fig. 4-8 α_1 and α_2 when the sigmoid function is approximated by a piecewise linear curve

of about 10%. This level of harmonics can not be tolerated in many applications and therefore another solution to this problem must be found.

On further reflection, our process has consisted of the following steps:

1) Training the network assuming sigmoid neurons.

2) Replacing the neurons with piecewise linear units in the actual implementation.

Alternatively one could use the following modified process:

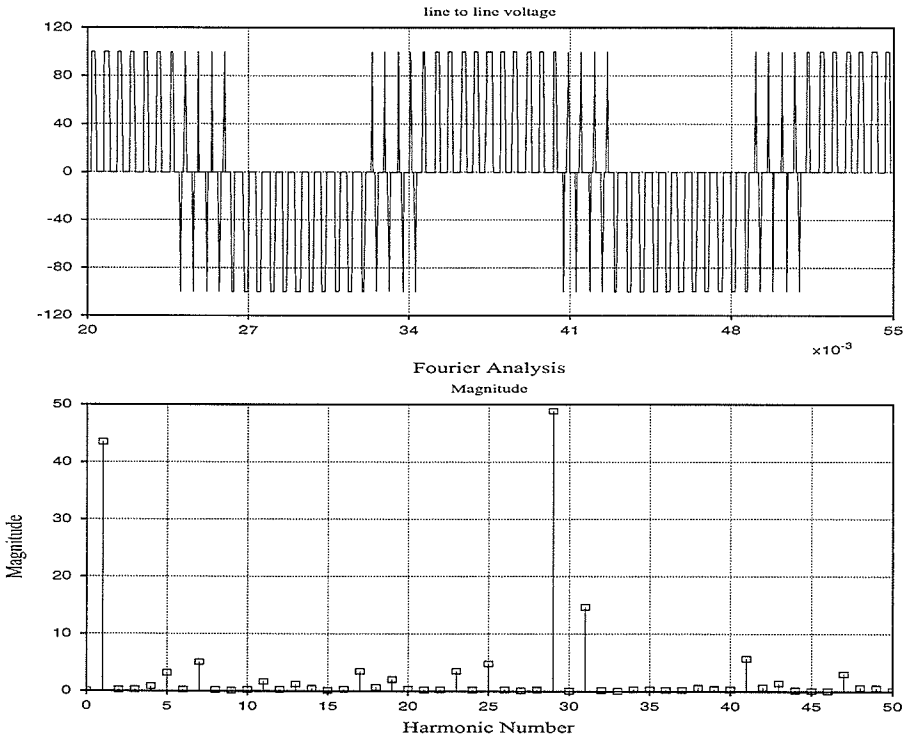


Fig. 4-9 Line voltage and its spectrum for the piecewise linear network with the same weights as the sigmoid-characteristic network

Assume piecewise linear characteristic for the neurons in the training process itself.

In this way, no approximation is made at all between the model and its implementation as both assume piecewise linearity. Theoretically this is possible, because the new characteristic function for the neurons is a continuous, monotonously increasing function, and differentiable except in a countable number of points e.g. the vertices where the lines join [41]. Obviously, the existing ready-to-use neural network training softwares could not be used to train this network and therefore a customized training program had to be developed. This is one of the contributions of this thesis. The developed training program uses the plain back propagation algorithm for its simplicity and therefore needs the first derivative of all neuron characteristics at each iteration of training. This derivative happen to be the slope of the appropriate piece of line, depending on the operating point of neuron at that iteration. In the rare case that the derivative at the breaking point of the characteristic is required, we can choose either the left or right derivative, with no significant effect on the final results.

As the plain back propagation method is very slow, it is important to choose a starting point as close as possible to the final solution. Since it is expected that the optimal weights for the piecewise linear network to be close to the weights of the

sigmoid network, it is reasonable to select these weights as the starting point for the new training program. This in fact reduces the training time considerably and prevents the simple training program from being stuck in local minima of the error function.

A neural network with a structure similar to those used in the previous examples was trained with the above method and was employed to generate the firing times for the same system. Fig. 4-10 shows the simulated voltage and current waveforms and their spectra for this system. As can be seen in this figure, results are almost identical to Fig. 4-5: the magnitudes of the 5^{th}, 7^{th} etc. harmonic voltages are all less than 1%, magnitude of 29^{th} harmonic is about 48% (compared to 45% in Fig. 4-5) and magnitude of 31^{st} harmonic is about 16% which is close to 17% in case of sigmoid network. This considerable improvement is due to the fact that in this case we are not "approximating" the neuron's characteristic with a piecewise linear function, but we are conducting the training with the a-priorie knowledge of the piecewise linear characteristic.

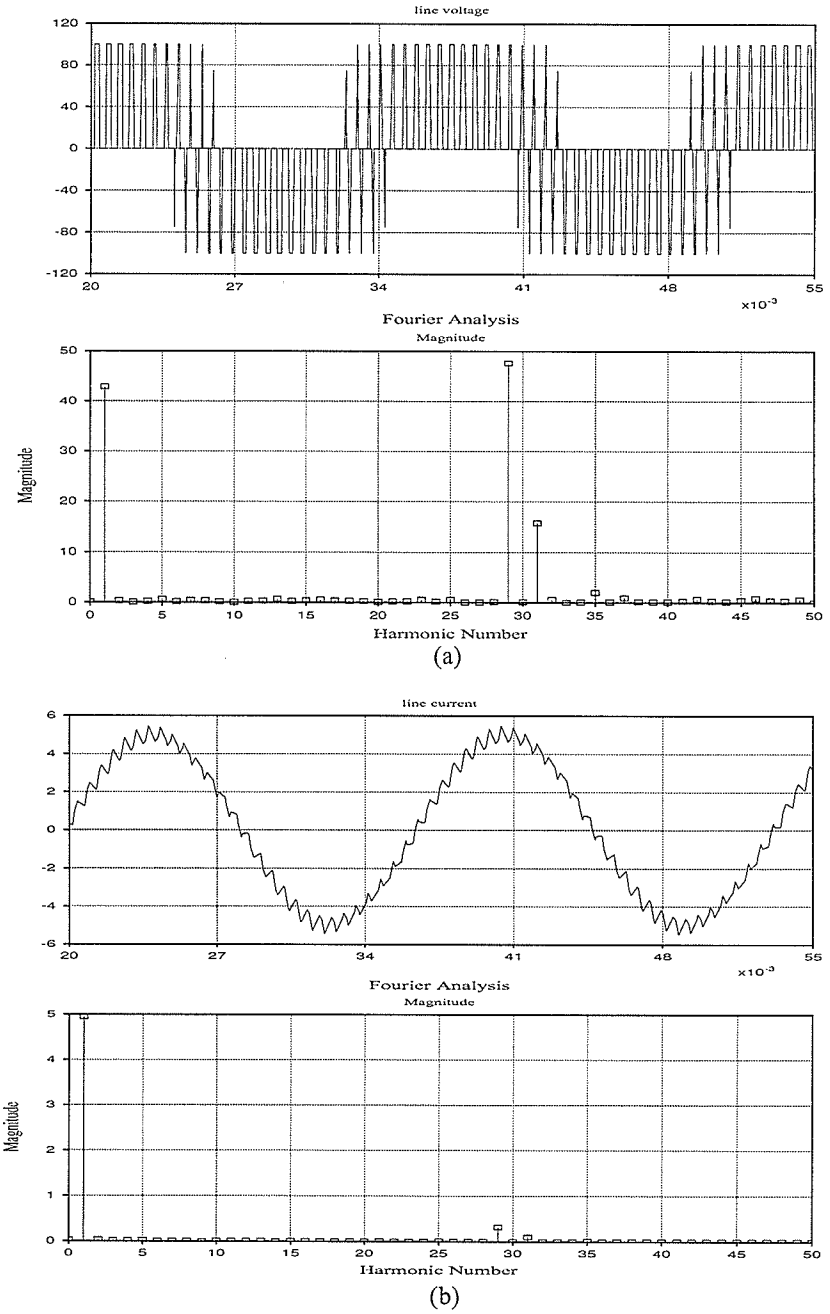


Fig. 4-10 a) Line voltage and b) Line current and their spectra for the new piecewise-linear network

4.3 HARDWARE IMPLEMENTATION OF THE OPTIMAL PWM INVERTER

The hardware implementation of the optimal PWM inverter can be divided into two parts: the inverter bridge and the firing controls. The inverter bridge comprises of the IGBT power electronic switches, the free-wheeling diodes and the snubber circuit. The firing controls are implemented on a Digital Signal Processing (DSP) board that communicates with a Personal Computer (PC) host. The PC provides a Graphical User Interface (GUI) that allows the user to change the magnitude and frequency of the output voltage in real time. This inverter system was used to drive an induction machine in a simple open-loop constant-volts-per-hertz (V/f) arrangement. The open loop control was chosen because of its simplicity, higher speed and robustness compared to the closed loop scheme. For a converter connected to a well regulated dc source this scheme works properly if accurate speed control is not necessary. Closed loop control allows additional improvement in the accuracy and can be used when the dc bus voltage variations are considerable. The following subsections explain the details of the various parts of the hardware and some typical test results.

4.3.1 The inverter bridge

The inverter is basically made of three double IGBT modules. Each module contains two IGBTs with the emitter of one IGBT connected to the collector of the

other one as shown in Fig. 4-11. Gates, collectors and emitters of both transistors are accessible from the terminals. The modules used in this project have 50A and 600V ratings. The three modules were mounted side-by-side on a heat sink. The three collectors of the upper IGBTs, and also the three emitters of the lower ones, were connected to each other by very short pieces of wire to keep the inductance of the dc link as low as possible.

The dc power was supplied by a six-pulse diode rectifier which was fed by a three phase auto transformer. This arrangement provides an adjustable dc voltage in the range of zero to 300V. But because of the relatively large inductance of the autotransformer, fast changes in the rectifier's output dc current may cause very large over-voltages. To protect the inverter against these over-voltages, a dc capacitor (3000uF) was put across the dc terminals of the rectifier. To suppress very fast voltage impulses where the large electrolytic capacitor is not effective (because of its internal inductance), a smaller ceramic capacitor was connected in parallel to the

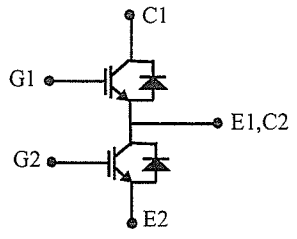


Fig. 4-11 A double IGBT module

electrolytic capacitor.

4.3.2 The snubber circuit

During the operation of the PWM inverter, the dc source current experiences fast changes. This is particularly true when fast IGBT switches are used that can turn off in a fraction of a microsecond. A quick drop in the dc current will cause the small inductance of the dc link wires to produce a large voltage impulse at the inverter dc terminals. It is imperative to protect the inverter switches against these impulses as the IGBTs can not tolerate such over voltages even for very short periods of time. A small circuit, usually called a snubber, will considerably reduce these over voltages by connecting a capacitor across the inverter when an overvoltage occurs. It should be mentioned that in a voltage source inverter like the one used in this project, the ac load inductance does not cause any transient overvoltages. This is because the fast anti-parallel diodes, which are part of the IGBT modules, provide a path for the load current to flow even when the IGBT's are turned off.

The simplest snubber circuit is a small capacitor (non electrolytic) connected directly across the IGBT module dc terminals. Although effective in reducing the transient over voltages, this capacitor may start resonating with the dc link inductance and therefore is not commonly used. A snubber circuit consisting of a capaci-

tor, a diode and a resistor as shown in Fig. 4-12 will avoid the resonance problem. Here the capacitor is charged to the dc line's normal voltage when the dc line is energised. Now, if the dc line voltage rises due to a quick drop in the dc current, the diode will start conducting and the capacitor will absorb the stored energy in the dc line inductance. When the dc line voltage is back to normal, the capacitor is discharged to the normal dc voltage level through the resistor. We chose this snubber circuit for its simplicity, although there are other more complicated snubber circuits that offer features like reduced power loss and protection against under voltages.

4.3.3 The driver circuit

The IGBTs used in this project need a gate-to-emitter voltage of +15V to fully turn on and -8V to securely turn off while the gating signals generated by the controller computer are at the TTL level, i.e. 0 to 0.5V for logic 0 and 3.5 to 5V for logic 1. Therefore there is a need for a driver circuit that translates the output of the controller to the voltage levels required by the IGBT's gate. It is also a common

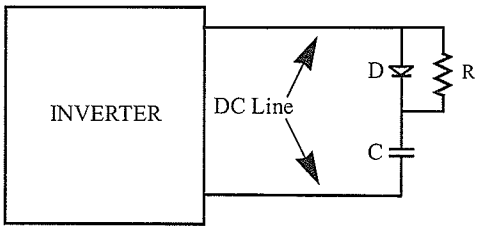


Fig. 4-12 The snubber circuit

practice to isolate the gate signals generated by the controller, from the high power inverter by using opto-couplers. A ready-to-use hybrid integrated circuit provided by the IGBT manufacturer can do both these jobs by receiving TTL signals at the input and transferring them through an opto-coupler to a driver circuit which provides the proper voltages for the IGBT gate. The driver also monitors the collector-emitter voltage of the transistor to detect serious over current conditions and reduce the gate voltage if necessary.

The above mentioned driver requires a +15V,0,-8V power supply. The drivers for the three upper IGBTs must have separate power supplies with independent 0V terminals. This is because these terminals are connected to the emitters of the IGBTs and if they are not independent the ac outputs of the inverter can be shorted out. In this project we used six separate supplies for the six drivers (instead of the minimum four supplies) to keep all the six drivers identical. Each of these power supplies actually consists of a dc/dc converter and a voltage regulator. The dc/dc

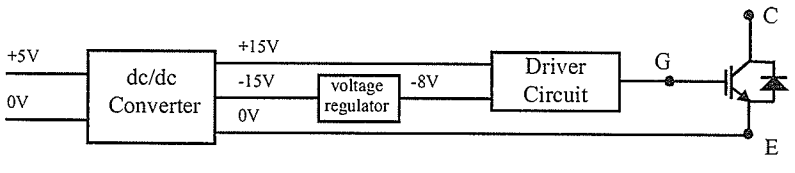


Fig. 4-13 The power supply for the gate driver of one IGBT

converters receive power from a common 5V source and provide isolated +/-15V at their outputs. A voltage regulator then converts -15V to -8V which is required by the driver circuit. Fig. 4-13 shows the power supply for IGBT gate drivers.

4.3.4 The TMS320C30 processor

The family of TMS320 Digital Signal Processing chips manufactured by Texas Instruments, is widely used in a variety of industrial applications such as image processing, speech processing, digital filtering, communications and real time control. The TMS320C30 belongs to the third generation of these processors which were first introduced in 1990. It is a 32-bit CMOS floating-point device which is able to process up to 33.3 million floating-point operations per second (MFLOPS). This performance can be achieved through using two parallel Arithmetic Logic Units (ALU) with 60ns single cycle instruction execution time. In addition to the Central Processing Unit (CPU), this chip contains a limited amount of memory (4Kx32-bit ROM, 2Kx32-bit RAM, and 64x32-bit Cache), Direct Memory Access (DMA) unit, two independent serial ports, two external interface ports and two 32-bit timers.

SPTMS320C30 is a ready-to-use DSP board from Spectrum Inc. with C30 processor, additional on-board memory and buffered input/outputs. This board can

be inserted in a PCI slot in any X86 based PC. The PC then serves as a host for the DSP board that can load a program into its memory and communicate with it while it is running the program. The PC host can also operate as a user interface for the DSP application. To do this, two programs must run at the same time: the application program on the DSP processor and the interface program on the PC. These two programs communicate with each other through a dual port memory on the DSP board (Fig. 4-13). The PC program can receive information from the user and pass it to the DSP program and/or receive information from the DSP program and display it for the user.

The manufacturer provides a number of effective development tools such as

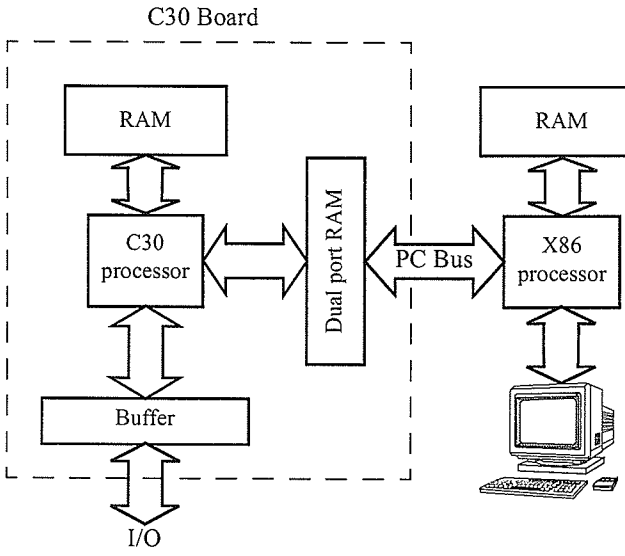


Fig. 4-14 Basic structure of the C30 board and its connection to the PC

C language and assembly language compilers, a C30 emulator and simulator that greatly facilitate programming and debugging of the applications. The C compiler can optimize the final code to utilize the parallel processing facilities of the C30 as much as possible. Through the use of the emulator, one can run the program in steps and monitor the contents of the registers and memory. The simulator does a similar job without requiring a DSP board to be present. It is actually a piece of software that runs on PC and simulates the behaviour of the DSP chip.

The two serial ports are able to either send or receive 8, 16, 24 or 32 bit data words independently. In addition, if the serial communication is not required, the serial port pins can be programmed to behave as general purpose I/O pins. This gives the user the opportunity to send and receive a limited number of binary signals (6 pins for each serial port) without requiring any additional circuitry. The data is sent and received through these pins by writing into, or reading from, certain memory mapped registers.

The two timer modules are general-purpose, 32-bit time/event counters with two signalling modes and internal or external clocking. They can be used to signal to the C30 or the external world at specified intervals, or to count external events. Timers can be used to interrupt the CPU or DMA (Direct Memory Access unit) or send a signal to the outside. Three memory mapped registers control the operation

of each timer. The global control register determines the operating mode of the timer, the period register specifies the timer's signalling period and the counter register contains the current value of the incrementing counter. The content of this register is incremented by one every time an input clock pulse is received. Once the value of this register equals the period register, it is set to zero and an output signal is generated that can be used to interrupt the CPU or DMA or sent to the outside.

4.3.5 The Graphical User Interface (GUI)

As mentioned before, in most applications the C30 board is dependent on a personal computer (PC) to initialize it and load its program into its memory. The PC can also provide a convenient way for the user to send and receive information to and from the DSP board. In this project the inverter is used in an open loop control system that receives the voltage and frequency orders from the user and applies the proper three phase PWM voltages to the load (induction machine) terminals. Therefore the only information that is needed to be passed to the DSP board are voltage magnitude and frequency. In this project since we do not use the C30's on-chip ROM, the ANN's weights have to be stored in the PC's hard disk and be loaded into the DSP board's RAM along with the firing control program.

The first interface program to be developed was a DOS based program

(written in C language) that, after initializing the DSP board and loading its program, copies the neural network weights into its memory and then waits for new voltage and frequency entries from the user. Once a new value for the voltage or frequency is entered by the user, this PC program writes them in certain addresses in the DSP board memory and then sets a flag (by writing 1 in another memory address). The firing control program (running on the DSP board) then uses these new voltage and frequency orders to generate new firing pulses.

To facilitate the data entry by the user, another Windows 3.1 based program was developed that basically does the same job as the DOS based program, but has a more advanced graphical user interface. This program was written in the C++ language using the Borland C++ V4.5 which was the most up-to-date C++ compiler at the time. Fig. 4-15 shows the GUI for the Windows based PC program. This program allows the user to change the voltage and frequency orders either independently or proportionally as would be required for constant V/f control of an induction machine. Each value can be changed either by moving the corresponding slider or by writing in the text window. In the proportional mode the ratio of voltage to frequency can also be selected.

Another important function of the PC program is to send proper signals to the firing control program for a smooth shut down when the program is terminated.

During the shut down the three upper IGBTs should be OFF and the three lower IGBTs should be ON. This is necessary to make sure that all three phase voltages are zero and a free wheeling path exists for the currents. The lower IGBTs should remain ON until the load current is zero. Since in this project the load currents are not measured, the firing signals to the upper IGBTs are kept at "low" and to the lower IGBTs at "high" level until the PC program is started again and the DSP board is initialized.

4.3.6 The firing control (DSP) program

The firing control program is the main part of the firing system which is responsible for issuing the proper ON and OFF signals for all six IGBTs at the pre-

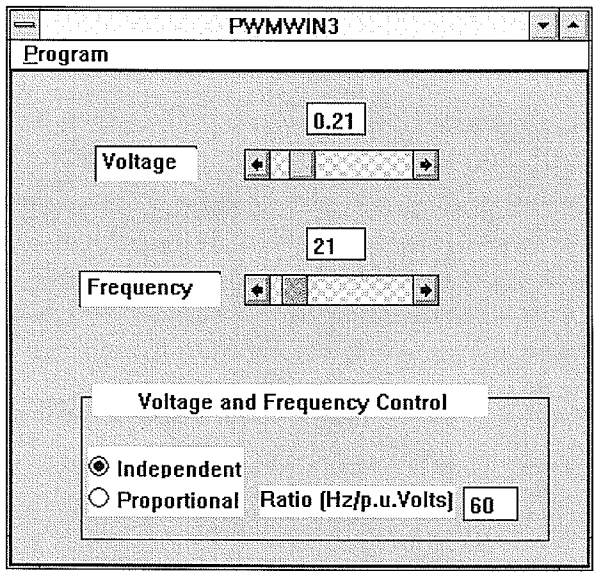


Fig. 4-15 The graphical user interface for the PC program, designed by the author

cisely calculated times to make sure that the selected harmonics are removed from the output voltage of the inverter. For this purpose the firing control program depends on a neural network subroutine that takes the per-unit voltage order as input and returns the firing angles that ensure the elimination of the selected harmonics. In this project two different neural network subroutines were developed, the first subroutine uses the sigmoid neurons and the second is based on the piecewise-linear neurons. Both subroutines work well with the current application that does not require a quick response from the neural network, although the linear implementation requires less processing time.

The neural network subroutine only provides the primary firing angles, i.e. those required for the first quarter of phase A. The secondary firing angles, i.e. other firing angles for phase A and the firing angles for the other two phases, can be easily calculated once the primary firing angles are available. Calculation of the secondary firing angles for phase A is straight forward because the output PWM voltage has odd and half wave symmetries. The same assumption has been used in the derivation of the basic optimal PWM equations. Based on this assumption, if $\alpha_1,\alpha_2 \ldots \alpha_n$ are the firing angles for the first quarter, the firing angles for the second quarter are $\pi-\alpha_n$, $\pi-\alpha_{n-1}$, ... $\pi-\alpha_1$, π. The firing angles for the second half cycle are the same as those for the first half cycle with a delay of π, i.e. $\pi+\alpha_1,\pi+\alpha_2 \ldots \pi+\alpha_n$, $2\pi-\alpha_n$,

$2\pi-\alpha_{n-1}$, ... $2\pi-\alpha_1$, 2π (see Fig. 4-1). Firing angles for the other two phases can be obtained by phase shifting those of phase A by $2\pi/3$ and $4\pi/3$.

Fig. 4-16 shows the flowchart of the firing control program. The program starts running once the DSP board is initialized and the firing control program is loaded into it by the PC program. The first thing to be done is the initialization of the serial port and the timer. Initializing the timer includes setting it to use the C30's internal clock, resetting its counter and period registers and enabling the corre-

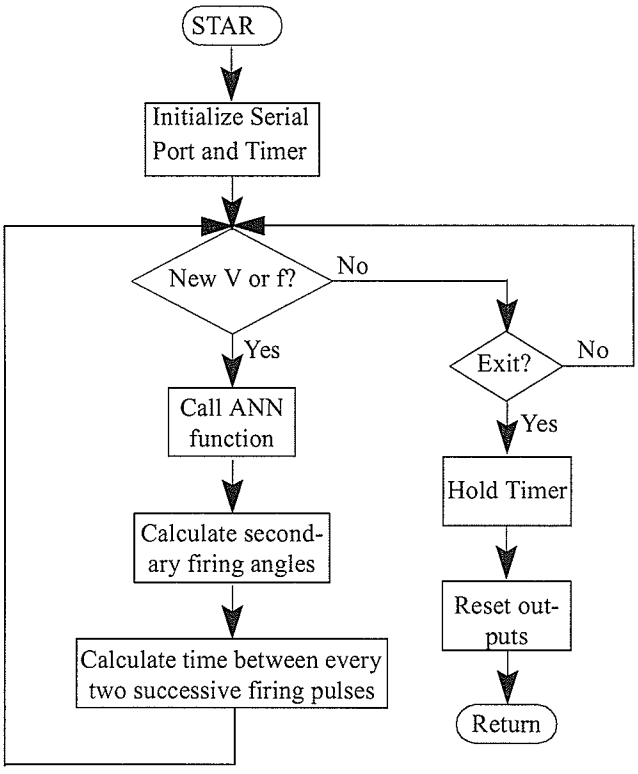


Fig. 4-16 Flow chart for firing control program

sponding CPU interrupt. When initializing the serial port, we define DX0, DX1, CLKX0, CLKX1, FSX0 and FSX1 pins as general purpose output pins. These pins are then used for sending firing orders to the IGBT driver circuits.

After the initialization, the program enters an infinite loop, waiting for either new values for V and F, or the exit command. Once a new value for V is received, the neural network function is called to calculate the new primary firing angles. The secondary firing angles are calculated at the next step. Note that for applications like STATCOM the converter voltages must be synchronized with the ac system voltages and therefore a phased locked loop is required. For a machine drive application like this case synchronization is not required and the output frequency is entirely determined by the converter itself. Then the firing angles for the three phases are merged and the time interval between each firing pulse to the next one is calculated based on the given frequency order. Knowing the period of the C30 processor's clock, we can convert these time intervals into the number of timer clock pulses. The converted time intervals are then put into an array of 114 elements called "pulsewidth". Another array of the same length called "Phase" holds indicators that show to which phase each firing pulse is related. For instance phase[k]=2 shows that at the end of the k^{th} time interval the IGBTs of phase B must be switched. The information stored in these two arrays is used by the timer and the interrupt routine

to determine the correct switching times of each IGBT. After updating the "pulsewidth" and "phase" arrays, this loop of the program is complete and program goes back to the waiting loop. If the exit command is received, the timer is stopped and "ON" and "OFF" signals are sent to the lower and upper IGBTs respectively. The C30 program then exits the main routine which leaves the output signals at this position until the C30 board is reset.

Every time the counter register equals the period register, an interrupt signal is sent to the CPU. This will cause the CPU to leave its current routine and jump to the specified interrupt routine. Fig. 4-17 shows the flow chart of the timer interrupt routine. The interrupt routine first stops the timer from counting to prevent it from sending another interrupt signal to the processor before it returns to the main routine. Without taking this precaution, if a second timer interrupt is received before the processor returns from the first call, the program will enter an infinite number of nested calls which will eventually cause an overflow in the stack and cause the processor to halt. The next step is to load the period register with a new value from the "pulsewidth" array. Then the corresponding element of the phase array is examined to find out which phase should be switched.

To make sure that the upper and lower switches of one phase do not conduct at the same time which will cause a dc bus short circuit, we have to make sure that

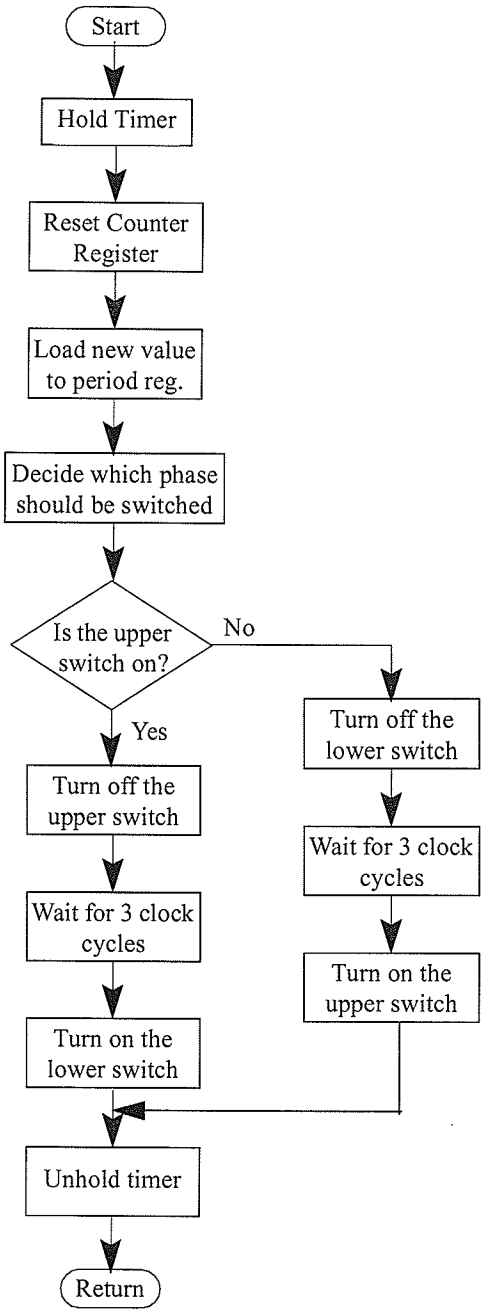


Fig. 4-17 Flow chart of the timer interrupt routine

every time the status of a phase is changed, the conducting switch is turned off first and after a short waiting period the other switch is turned on. This is done in the interrupt routine function by looking at the global variables "stat1", "stat2" or "stat3" to check the current status of the switches for the changing phase. Based on this, the currently "on" switch is turned off and after waiting in a loop for a short period the other switch is turned on. Our tests showed that waiting in a "for" loop for only one cycle which takes about 100ns is quite enough to prevent any short circuitting of the dc bus via simultaneous conduction of both IGBTs in a bridge arm. The interrupt routine then updates the "stat" variable and the counter for the "pulsewidth" and "phase" arrays and unholds the timer before returning the control to the main routine.

4.3.7 Test results

The above mentioned prototype inverter was used to feed a 3hp 6-pole, 208V squirrel cage induction machine. A dc generator was coupled to the induction machine to act as a mechanical load. Fig. 4-21 shows a photograph of the inverter, the PC host, the ac and dc machines and the resistive load for dc machine. The machine was run with different speeds under different loads and speeds and the line currents were measured and analysed by a digital oscilloscope. Fig. 4-18 and Fig. 4-19 show the machine current waveforms and their Fourier analysis under the

0.7p.u. load and for inverter frequencies and voltages of 1pu and 0.5 pu respectively. As can be seen in these two figures, the proposed scheme has been able to remove all the lower order harmonics and the first harmonic that appears in the output is the 29th. As previously explained, the current waveform improves significantly when the frequency and the magnitude of the fundamental component are increased. Precise measurements show that the actual output frequency of the system is slightly below the ordered frequency. This is because the actual width of each pulse in the output voltage is increased from the originally calculated value as a result of holding the timer while the interrupt routine is being processed. This deviation from the desired response can be easily compensated for by adopting a more

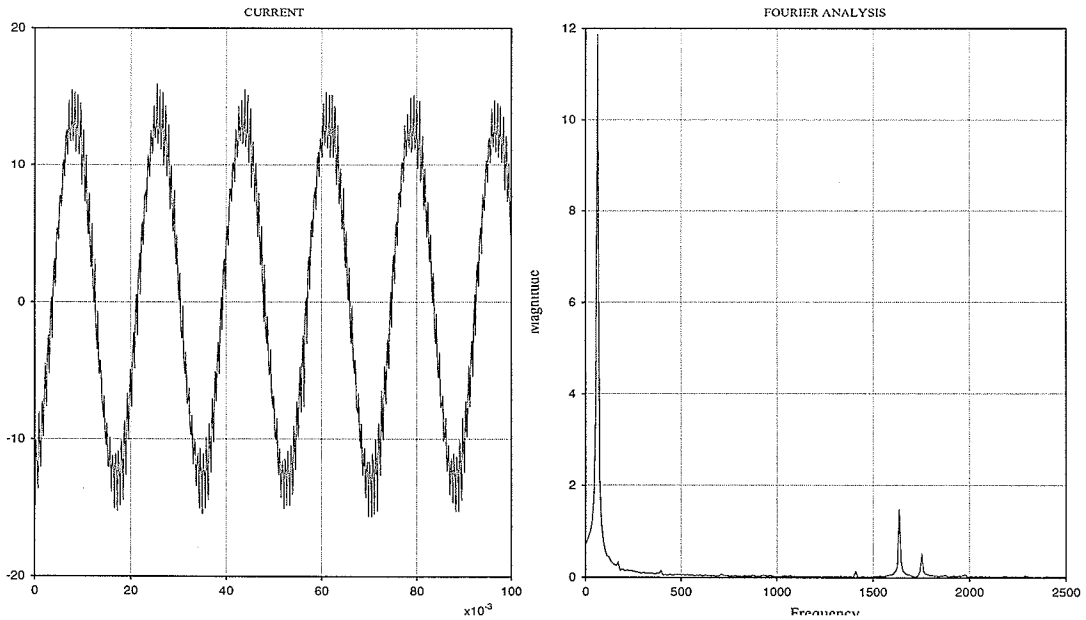


Fig. 4-18 Experimental results showing current waveform and its spectrum for the induction machine under 0.7p.u. load, V=1p.u and f=60Hz.

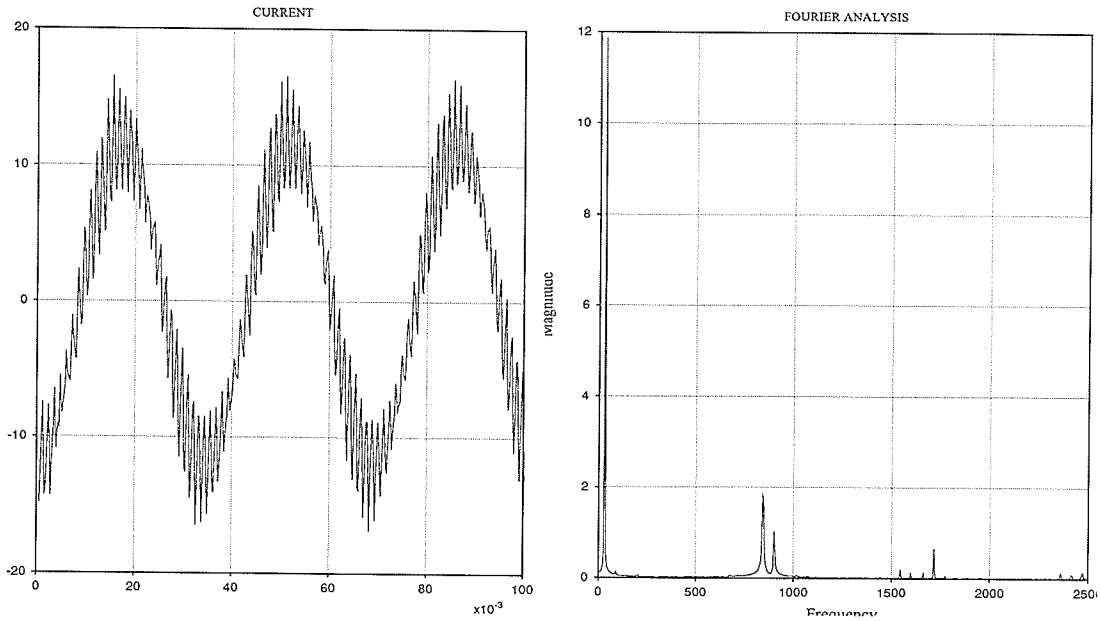


Fig. 4-19 Experimental results showing current waveform and its spectrum for the induction machine under 0.7p.u. load, V=0.5p.u and f=30Hz.

accurate method for calculating the length of each pulse. In this project though this was not implemented, as the purpose of the project was to show the feasibility of the proposed control scheme for the inverter. When using the proposed inverter as a machine drive, one should note that quick changes in frequency and/or the magnitude of the voltage may cause large current transients. This is both because of the larger slip in the machine and the non-optimal voltage waveform. Fig. 4-20 shows the current waveform after a step change in frequency.

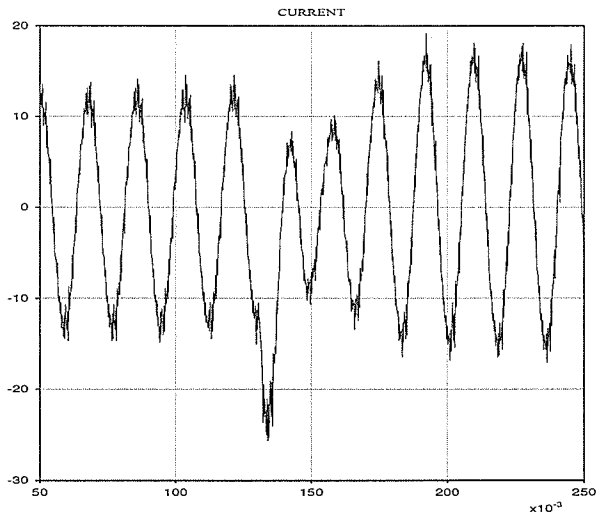


Fig. 4-20 Experimental results showing Current transient after 1Hz step change in frequency

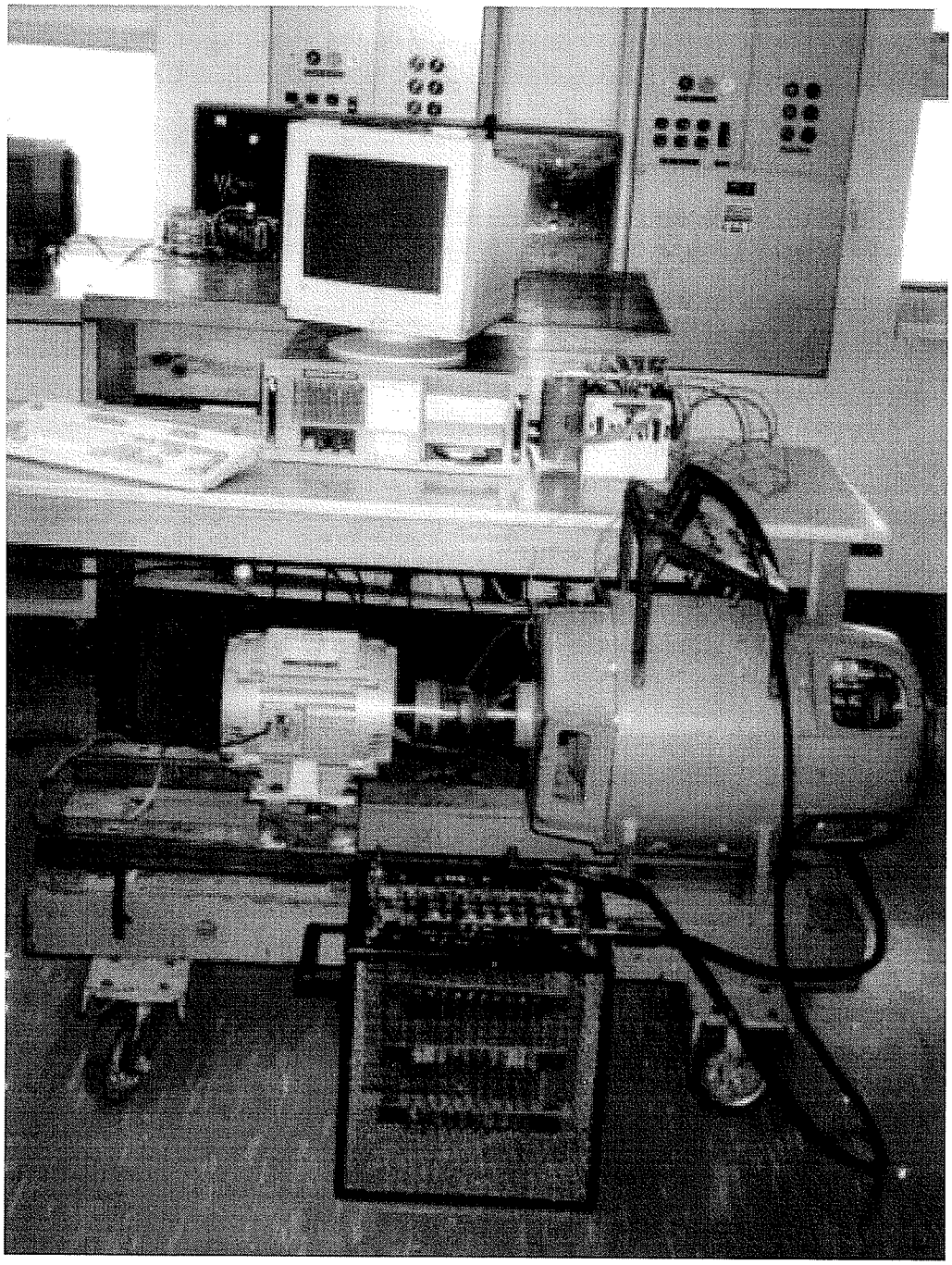


Fig. 4-21 A photograph of the inverter test set up

4.4 CONCLUSIONS

The optimal PWM method can be used in practical inverters to eliminate the selected harmonics from the output ac voltage and current. The precise firing orders for the inverter electronic switches can be generated by a neural network based circuit as proposed by the author. The neural network offers a fast, reliable and computationally inexpensive alternative to the on-line calculation of firing angles. Compared to a look-up table, it requires comparable memory and CPU time, while its flexibility to accommodate several optimization factors as inputs is an advantage. The method was validated by extensive simulation studies and by building a hardware prototype. This prototype uses a signal processing board (TMS320C30) to emulate the artificial neural network and a PC to serve as a user interface. To reduce the computation time for the ANN, the author replaced the sigmoid characteristic functions of the neurons by piecewise linear functions and trained the ANN with this a-priori knowledge. This method was also validated through a number of simulation and experimental tests.

CHAPTER 5

APPLICATION IN AN AC-DC CONVERTER AND STATCOM

The neural network controlled voltage source inverter can be used (with minor modifications) in an AC to DC converter (also known as PWM rectifier) to provide DC power to a load and at the same time regulate the reactive power exchange to the AC system. When used without a dc source or load, the device is a STATCOM with the function of regulating the reactive power supply. This chapter presents the details of design and results of simulation studies for two applications: i) an AC-DC converter with a single 2-level bridge and ii) a STATCOM with two bridges.

5.1 THE AC-DC CONVERTER

In Chapter 2 we stressed that it is highly desirable for a rectifier to draw a clean sinewave current at unity power factor from the ac lines. Utilities are particularly concerned about the harmonics as they can propagate in the system and increase the losses in transmission and distribution equipment; cause the misoperation of protective relays, and deteriorate the quality of the power delivered to consumers. As the number of rectifiers in the system increases the problem of harmonics becomes more serious. Several national and international standards, notably IEEE 519, now limit the amount of harmonics that a consumer can inject into the power system.

The ideas used in the previous section to design the optimal voltage source inverter can be used to design an AC-DC converter. The converter would be able to perform the task of AC-DC conversion and introduce very little harmonics into the power system. The reactive power can also be controlled in a wide rang of positive and negative values. Active power control is realized through closed loop regulation of the phase angle between the converter output and the ac system voltages. To be able to control the reactive power, the magnitude of the converter output voltage is controlled in a closed loop while the dc voltage is kept at a fixed reference level.

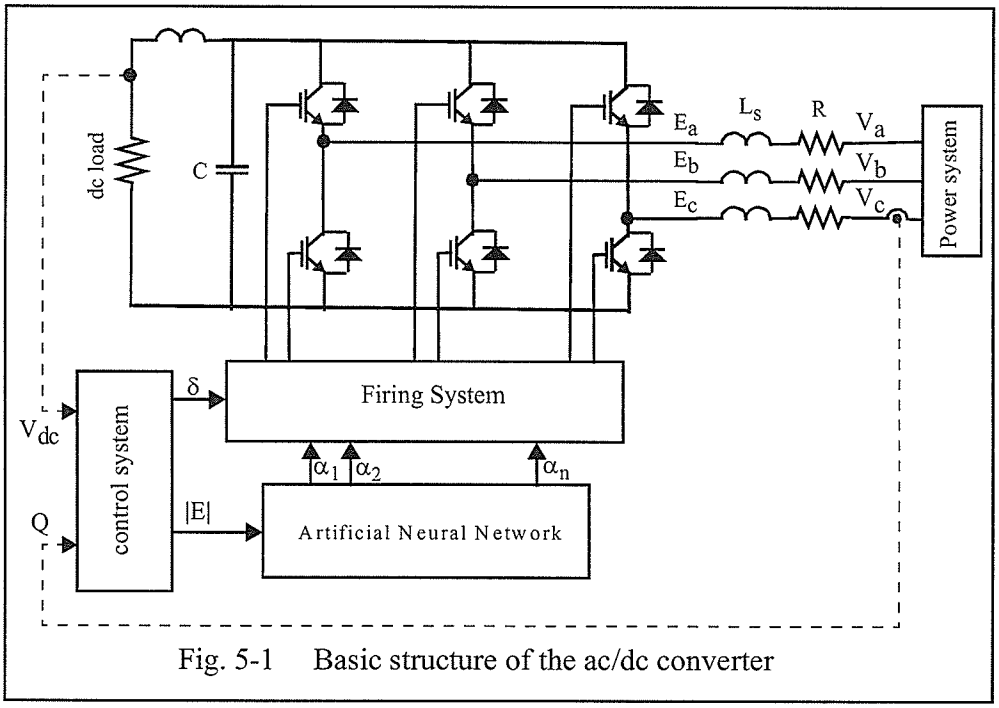


Fig. 5-1 Basic structure of the ac/dc converter

Fig. 5-1 shows the basic structure of the converter. During steady state operation there is a constant voltage V_{dc} at the dc terminals. The capacitor C is large enough to prevent sudden changes in the dc voltage. So for the purposes of approximate analysis it could be considered as a voltage source. The three phase bridge operates exactly the same way as the inverter used in the previous chapter to produce a terminal voltage E which is devoid of lower order harmonics. L_S and R_S represent the transformer and system impedances. The current flowing into these elements is governed by E and the ac system voltage V:

$$\left(R + \frac{dL_s}{dt}\right) i = V - E \qquad (5\text{-}1)$$

Considering that V is a pure sinusoidal waveform, the harmonic content of the ac current depends only on the harmonic content of E and the size of L_S. By applying the optimal PWM scheme, only the higher order harmonics exist in E which are readily filtered by the system inductance. The amplitude and the phase angle of the fundamental component of E can be controlled to regulate the active and reactive power flow into the converter such that the dc load voltage and the power factor (leading or lagging) at the ac terminals remain at the desired levels, regardless of the changes in the load resistance or the source voltage. The next two subsections explain the structure of the control system for this converter.

5.1.1 d-q representation of the phase quantities

The active and reactive powers at the terminals of a voltage source converter can be controlled independently as long as the currents and voltages are within the limits. This requires the control system to separate the active and reactive (also called d and q) components of the ac current. This subsection explains the principles of the d-q decomposition technique that is used in the converter controller.

In a three-phase three-wire system the sum of the three line voltages (and currents) is always zero. Therefore only two of these voltages (currents) are independent variables. Neglecting the zero sequence component, this is also true for the

phase voltages. This is acceptable as the zero sequence voltage does not have any effect on the active and reactive power in this case. Thus a set of such voltages (currents) can be uniquely represented by a vector (not phasor) on a plane [42] as illustrated in Fig. 5-2. For a balanced system with pure sinusoidal voltages the voltage

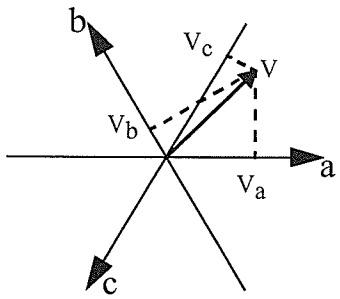


Fig. 5-2 Instantaneous voltage vector

vector will rotate at the angular velocity of ω on a circular trajectory with a radius equal to the magnitude of the three phase voltages. In general this vector contains all the information of the three phase set, including the steady state, unbalancies, harmonic waveform distortions and transient components. In Eq. 5-3 the new static direct and quadrature axes d_s and q_s and voltages V_{ds} and V_{qs} are introduced. The transformation from phase variables to ds-qs coordinates is as follows:

$$\begin{bmatrix} V_{ds} \\ V_{qs} \\ 0 \end{bmatrix} = T_s \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \qquad (5\text{-}2)$$

where

$$T_s = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{5-3}$$

The inverse transformation can be obtained from the following equation:

$$T_s^{-1} = \frac{2}{3} T_s^T \tag{5-4}$$

The above transformation, although useful, can be improved by choosing a rotating frame where the d-axis always coincides with a voltage vector. The advantage of this definition is that now the d-axis current component i_d accounts for active power (instantaneous) and i_q for reactive power. The transformation matrix in

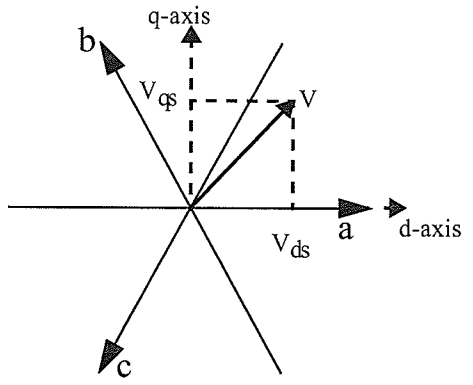


Fig. 5-3 Representation in ds-qs axis

this case is:

$$T = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta-\frac{4\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{4\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \qquad (5\text{-}5)$$

where $\theta=\tan^{-1}(V_{qs}/V_{ds})$ is the angle between the V vector and the stationary d-axis. The phase quantities and the transformed quantities are related as follows:

$$\begin{aligned} \begin{bmatrix} i_d & i_q & 0 \end{bmatrix}^T &= T\begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \\ \begin{bmatrix} V_d & V_q & 0 \end{bmatrix}^T &= T\begin{bmatrix} V_a & V_b & V_c \end{bmatrix}^T \end{aligned} \qquad (5\text{-}6)$$

Active and reactive powers are expressed in terms of the d and q quantities as follows:

$$\begin{aligned} P &= \frac{2}{3}|V|i_d \\ Q &= \frac{2}{3}|V|i_q \end{aligned} \qquad (5\text{-}7)$$

where |V| is the magnitude of the voltage vector.

5.1.2 System modelling and control

The system model and the structure of the control system we use here and for the STATCOM are based on the model first presented by Shauder and Mehta

[42]. This subsection briefly describes this model.

The instantaneous phase current and voltages in Fig. 5-1can be represented by the following vectors:

$$\mathbf{i}_p = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \qquad \mathbf{E} = \begin{bmatrix} e_a & e_b & e_c \end{bmatrix}^T \qquad \mathbf{V} = \begin{bmatrix} V_a & V_b & V_c \end{bmatrix}^T$$

Using these vectors, the current-voltage relations at the AC terminals of the converter are described by the following equation:

$$\frac{d\mathbf{i}_p}{dt} = -\frac{1}{L_s} \cdot \mathbf{R}\mathbf{i}_p + \frac{1}{L_s}(\mathbf{E} - \mathbf{V}) \tag{5-8}$$

where:

$$\mathbf{R} = \begin{bmatrix} R & 0 & 0 \\ 0 & R & 0 \\ 0 & 0 & R \end{bmatrix}$$

Transforming phase quantities to the d-q system and after some algebra we have:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R/L_s & \omega \\ -\omega & -R/L_s \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} e_d - |V| \\ e_q \end{bmatrix} \tag{5-9}$$

where $\omega = d\theta/dt$. If the losses in the converter and the series resistances are ne-

glected, the active power at the ac and dc sides are equal, hence:

$$V_{dc} \cdot i_{dc} = \frac{3}{2}|V|\, i_d \tag{5-10}$$

The above equation implies the important conclusion that the dc voltage is controlled only by i_d. Eq. 5-9 shows that changing either of the control inputs e_d or e_q will affect both i_d and i_q. It is highly desirable to control i_d and i_q (and hence P and Q) independently. This can be done by changing e_d and e_q in a way that decouples the two equations. In particular changing e_d and e_q according to the following equations will decouple i_d and i_q:

$$\begin{aligned} e_d &= |V| - L_s\, \omega\, i_q + u_d \\ e_q &= L_s \omega i_d + u_q \end{aligned} \tag{5-11}$$

This can be seen by substituting Eq. 5-10 in (5-9):

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} = \begin{bmatrix} -R/L_s & 0 \\ 0 & -R/L_s \end{bmatrix}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \frac{1}{L_s}\begin{bmatrix} u_d \\ u_q \end{bmatrix} \tag{5-12}$$

Now by controlling i_d and i_q through u_d and u_q, we can control the dc voltage and reactive power independently. But the only variables which are accessible are the amplitude and frequency of the fundamental component of E. Therefore the control system must first calculate |E| and the phase angle δ between E and the d-

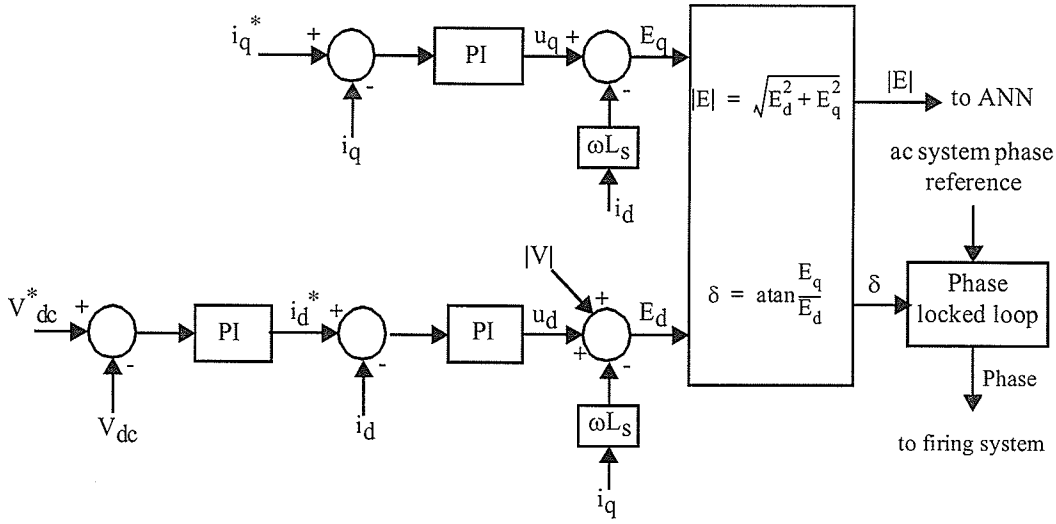


Fig. 5-4 Block diagram of the control system

axis and then a separate control loop should set δ at the desired level. It should be noted that since the actual controlled variables are the direct and quadrature axis projections E_d and E_q of the fundamental frequency component of E and not the actual d and q-axis components of E, there will be still some coupling between i_d and i_q. Fig. 5-4 shows the block diagram of the control system.

5.1.3 Simulation results

To examine the validity of the above analysis, a small system consisting of the neural network, the control and firing systems, and the converter was simulated using the PSCAD/EMTDC electromagnetic transient simulation software. The dc capacitor was 1000μF which is a typical size to keep the dc ripples at an acceptable

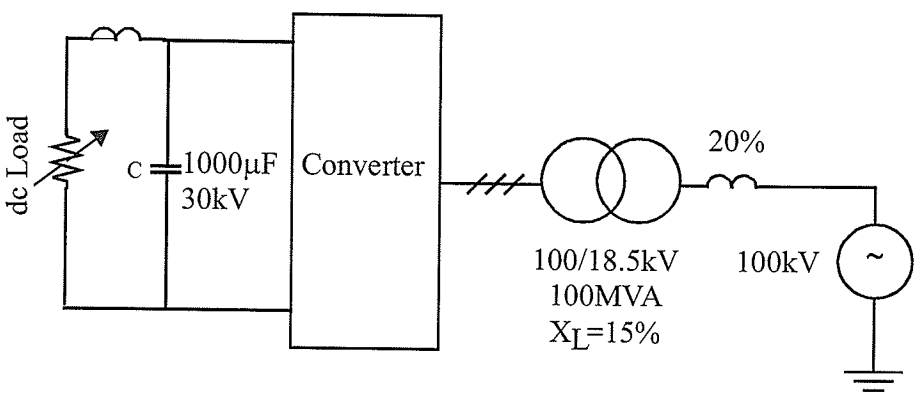


Fig. 5-5 AC-DC converter model used in simulation study

level (+/- 5%). The series inductance L_s was 0.35p.u. which consists of the transformer leakage inductance (0.15p.u.) and an additional series inductor (see Fig. 5-5). Extra series inductance was added to reduce the magnitude of the largest harmonic to about 5%. Alternatively a parallel high pass filter can be connected at the system side of the transformer to remove the remaining higher order current harmonics (29th and above) and reduce the total harmonic distortion of the AC current. Fig. 5-6 shows the phase voltage and current waveforms and the current spectrum when the reactive power exchange is zero and the active power is 1p.u. As can be seen, the first harmonic which appears in the phase current is the 29th and all the lower order harmonics are effectively cancelled. Higher order harmonics can be further attenuated by increasing the series reactance, but this will also increase the system's response time to changes in P and Q orders. Responses of the system to a

step changes in load and i_q^* are shown in Fig. 5-7 and Fig. 5-8 respectively. The response time is of the order of 1-2 cycles which is acceptable in most applications. Faster response can be achieved if the series inductance is decreased, but this will result in larger harmonic currents unless a higher pulse number is used.

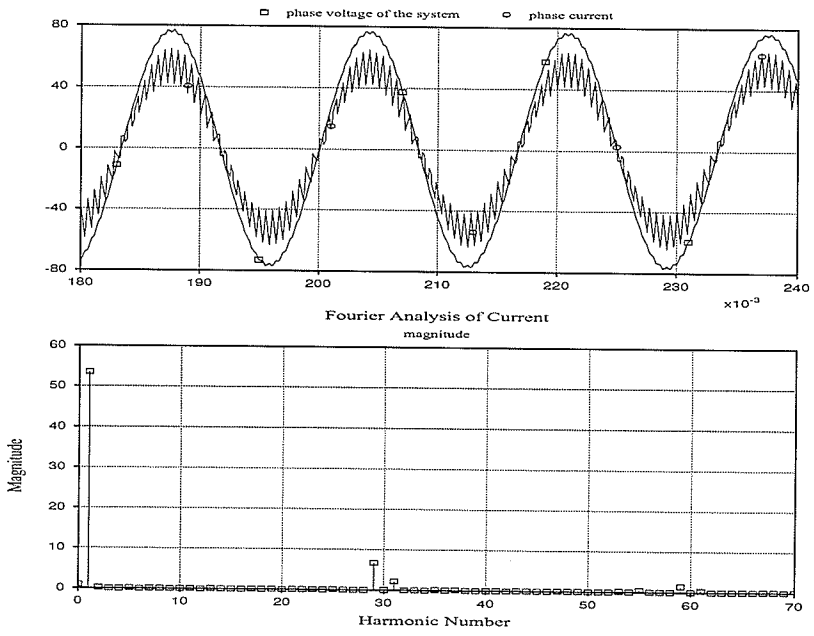


Fig. 5-6 The voltage and current waveforms when $Q^*=0$ & $P_{dc}=1$p.u. Note that the voltage and current are not in the same scale.

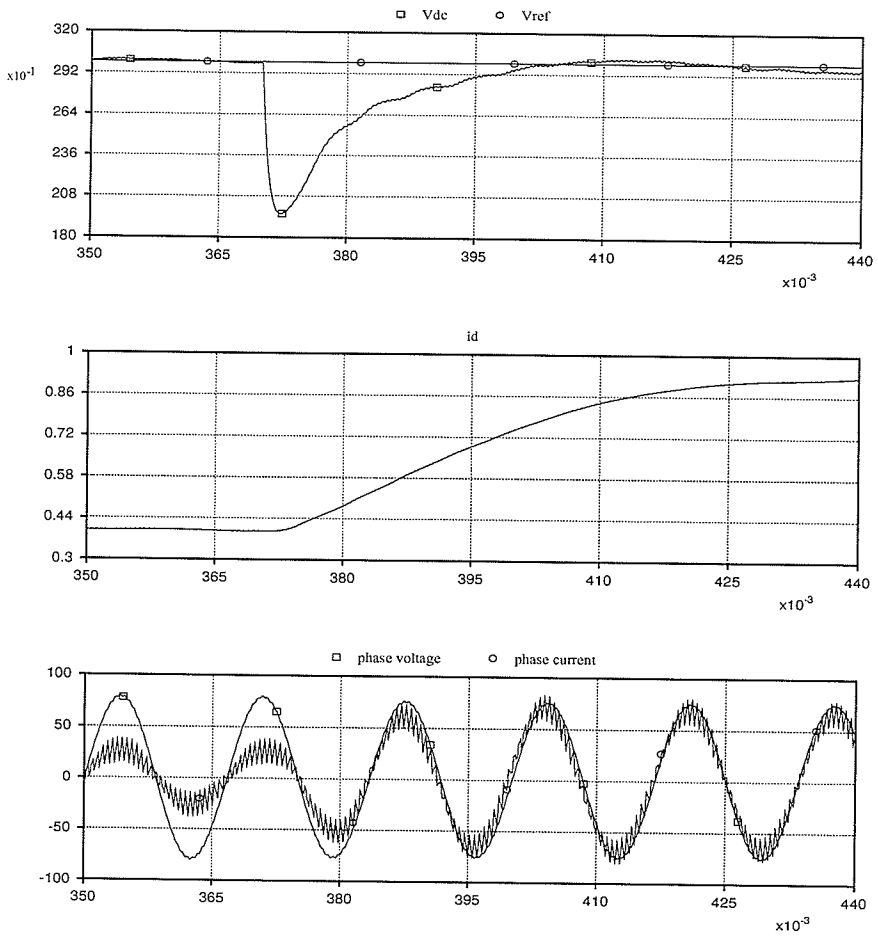


Fig. 5-7 Response of the AC-DC converter to a step change in load

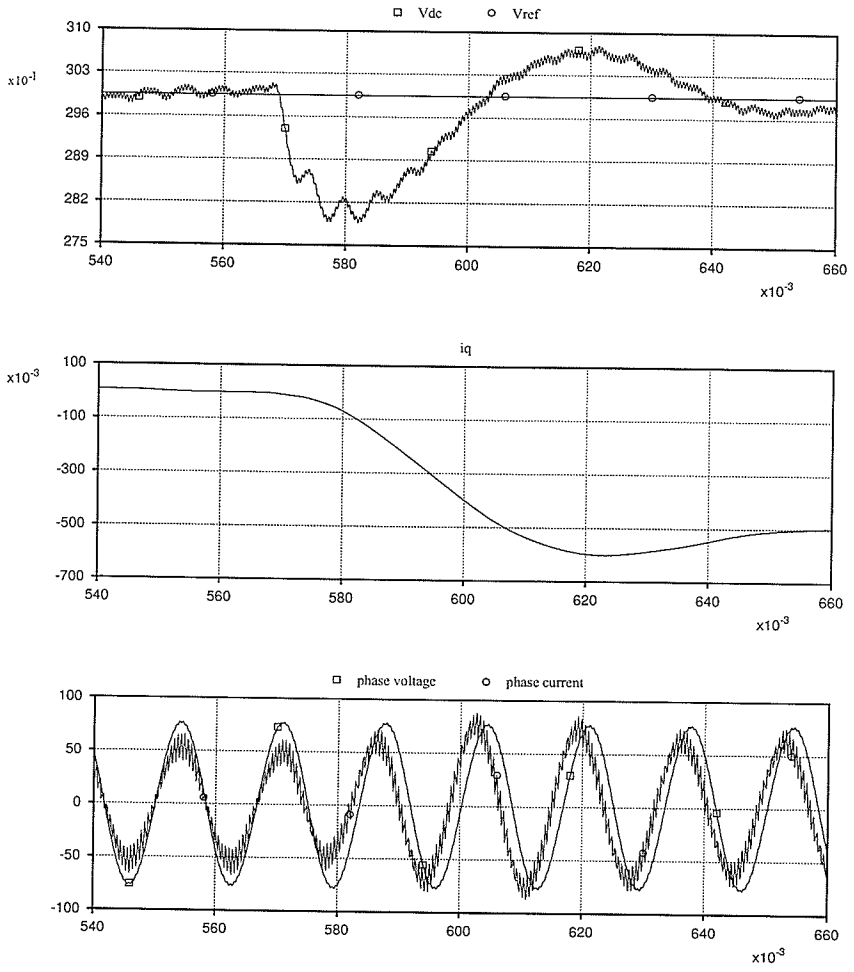


Fig. 5-8 Response of the AC-DC converter to a step change in i_q^*

5.2 TWO-CONVERTER STATCOM

As explained earlier, the optimal PWM method when applied to a 2-level converter can only push the harmonics to higher frequencies so that they are filtered more effectively by the series inductance. In a 2-converter configuration (Fig. 5-9) on the other hand, the 5^{th}, 7^{th}, 17^{th}, 19^{th} etc. harmonic voltages generated by the two converters actually cancel each other because of the YY and YΔ transformers. This is done in exactly the same way these harmonics are cancelled in a conventional 12-pulse STATCOM as explained in section 2.4.4. This mechanism considerably reduces the total harmonic distortion in the AC output voltage of the converter as 5^{th}

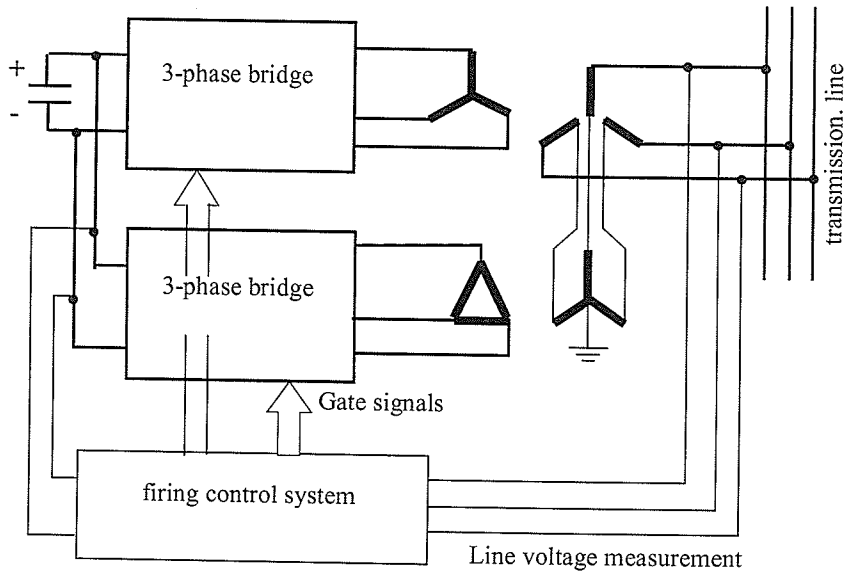


Fig. 5-9 The structure of the 2-converter STATCOM

and 7^{th} are typically the dominant harmonics. The optimal PWM technique can then be used to further improve the current waveform by eliminating 11^{th},13^{th} etc. harmonics. This way waveforms comparable to conventional multipulse STATCOMs can be obtained with only a few switchings per cycle. The 12-pulse operation of the STATCOM can be achieved by only one switching per quarter cycle (Fundamental Frequency Modulation) to determine the magnitude of fundamental and is not considered here. To remove all harmonics up to the 23^{rd} and achieve a waveform similar to a 24-pulse STATCOM with FFM, we need an optimal PWM pattern that only removes 11th and 13th harmonics. This requires only 3 switchings per quarter cycle: 2 for removing the harmonics and an extra one for being able to adjust the modulation index. Similarly, waveforms comparable to 36 and 48-pulse STATCOMS can be achieved by only 5 and 7 switchings per quarter cycle. This means the average switching frequency of the converter will be 11 times the fundamental (60Hz in 60Hz systems) for 36-pulse and 15 times the fundamental (900Hz in 60Hz systems) for the 48-pulse STATCOMs. The switching function of the second converter must be 30^{o} phase shifted with respect to the first one to guarantee the cancellation of the 5^{th} and 7^{th} harmonics.

The control scheme for the STATCOM can be based on either constant or variable PWM patterns. If the constant PWM pattern scheme is selected, the reac-

tive power is controlled through the control of the capacitor voltage. In this case only one set of switching angles is required that provides the maximum magnitude for the fundamental component and eliminates the selected harmonics. In the variable PWM pattern method on the other hand, the capacitor voltage is either kept constant or is controlled independently of the reactive power order to fulfil other requirements. Here the reactive power is controlled by regulating the magnitude of the fundamental component of the converter voltage by selecting different PWM patterns. The Universal Power Flow Controller (UPFC) and Voltage Source Converter based HVDC systems (e.g. HVDC LITE and HVDC PLUS) are examples of cases where the reactive power can not be controlled only by regulating the capacitor voltage. Systems based on the variable PWM pattern also have a faster response because under this control scheme the system does not need to wait for a change in capacitor voltage to be able to change its output reactive power. In both cases the active and reactive power exchange between the converter and the ac system must be controlled using a closed loop control system.

5.2.1 Simulation Results

To study the outcomes of the application of the neural network based optimal PWM scheme to the 2-converter STATCOM, a detailed simulation model was developed for this system, with a control loop similar to the AC/DC converter ex-

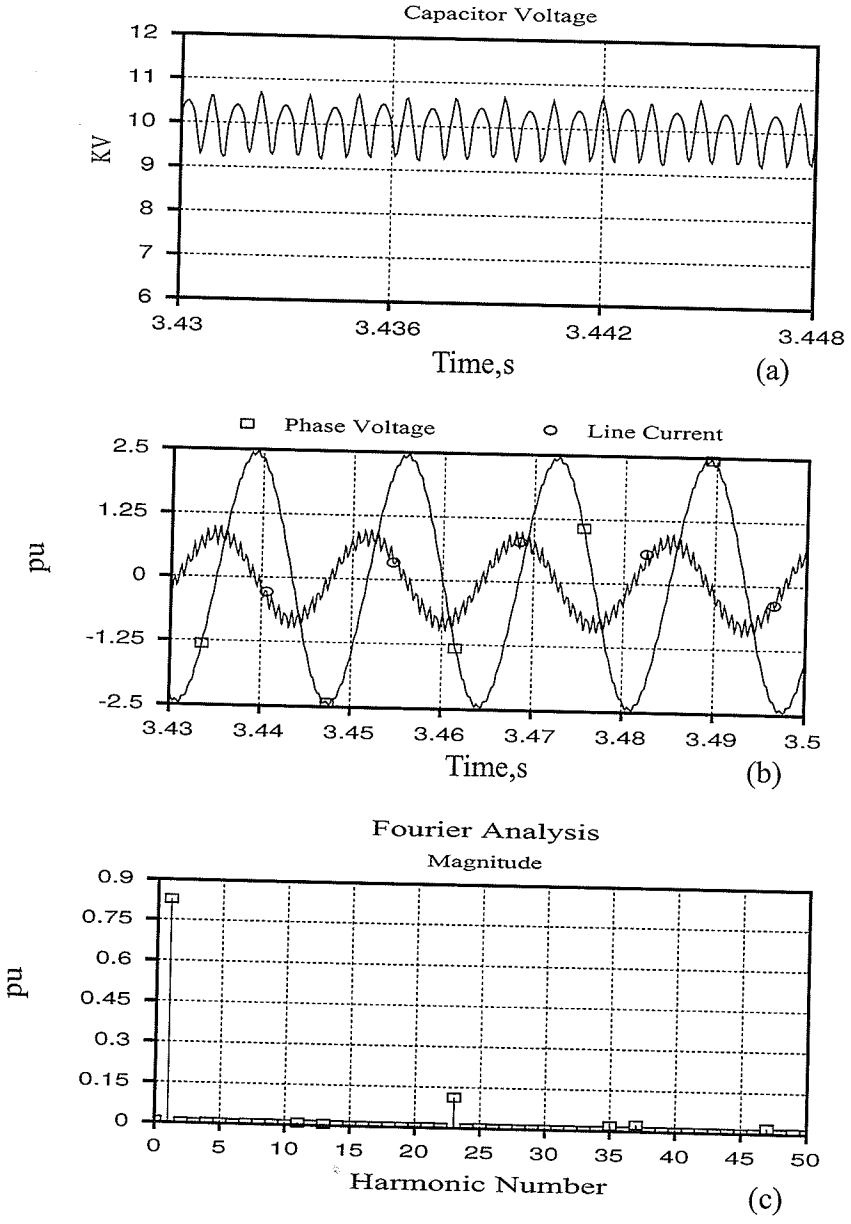


Fig. 5-10 24-Pulse STATCOM a) Capacitor Voltage, b) Phase Voltage and Current (voltage scaled to 3kV, current in pu) when iq=0.8 and c) the Fourier Analysis of the Phase Current

plained in section 5.1. Two cases where the first harmonics to appear are 23rd and 35th (similar to conventional 24 and 36-pulse STATCOMS) were studied. In the first case only 11^{th} and 13^{th} harmonics have to be removed by the PWM switching function while in the second case 23^{rd} and 25^{th} harmonics should also be removed in addition to the 11^{th} and 13^{th}. Similar to the previous systems, the optimal PWM equations (Eq. 4-2) were solved in each case for more than 100 equidistant values for the magnitude of the fundamental component and solutions were used to train a separate neural network.

Both simulated STATCOMs have 100MVar capacity and are connected directly to a 100kV source with a series impedance of 0.05p.u. The converter transformers are rated 55MVA each, 100/6.75kV with 0.1pu leakage reactance. The dc capacitor is 5000μF and its nominal voltage is 10kV. Fig. 5-10 shows the dc voltage and ac voltage and current for the 24-pulse STATCOM along with the Fourier analysis for the ac current. As expected the first harmonic appearing in the current is the 23rd and all lower order harmonics are effectively cancelled. Response of the 24-pulse STATCOM to a large step change in i_q order is shown in Fig. 5-11. As can be seen, i_q can catch up with the ordered value in about three cycles. Although the decoupling in the control system reduces the effect of change in i_q on i_d, there are still some variations in i_d and V_{dc} for a short time after the transient. This is mainly be-

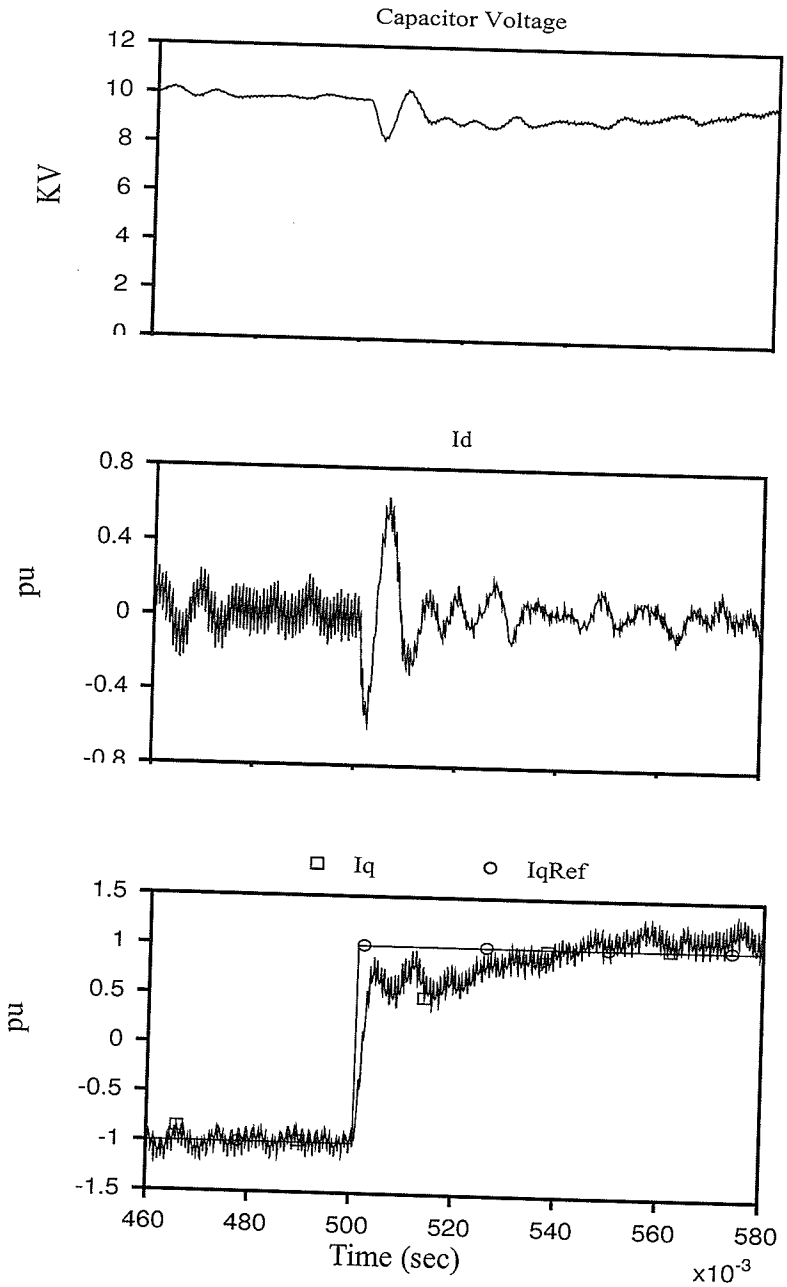


Fig. 5-11 Response of the 24-Pulse STATCOM to a Step Change in I_q Order

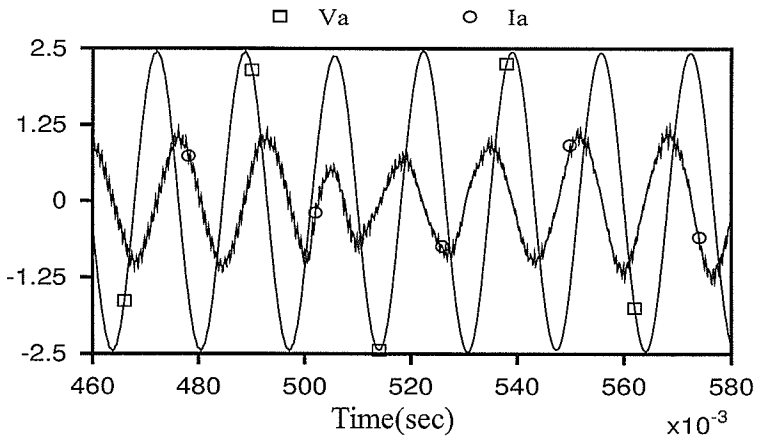


Fig. 5-11 Cont. Response of the 24-Pulse STATCOM to a Step Change in I_q Order (line current is in pu and phase voltage is scaled by a factor of 0.03)

cause of the finite response time of the control system and the quite large harmonics produced by the converter during the transient.

Fig. 5-12 shows dc and ac voltages, ac current and its Fourier analysis for the 36-pulse STATCOM under the steady-state conditions. Here the first harmonic appearing in the ac current is the 35th which has been highly suppressed by the transformer leakage reactance. As a result the ac current is much cleaner than in the 24-pule case. The dc voltage is also smoother due to the reduced magnitude and higher frequency of the harmonics in ac currents and switching functions. These results generally show considerable improvement over those from the single inverter

converter presented in the previous section. This agrees with expectations that the cancellation of 5th and 7th harmonics rather than shifting them to higher frequencies has a great impact on the final harmonic content of the ac current.

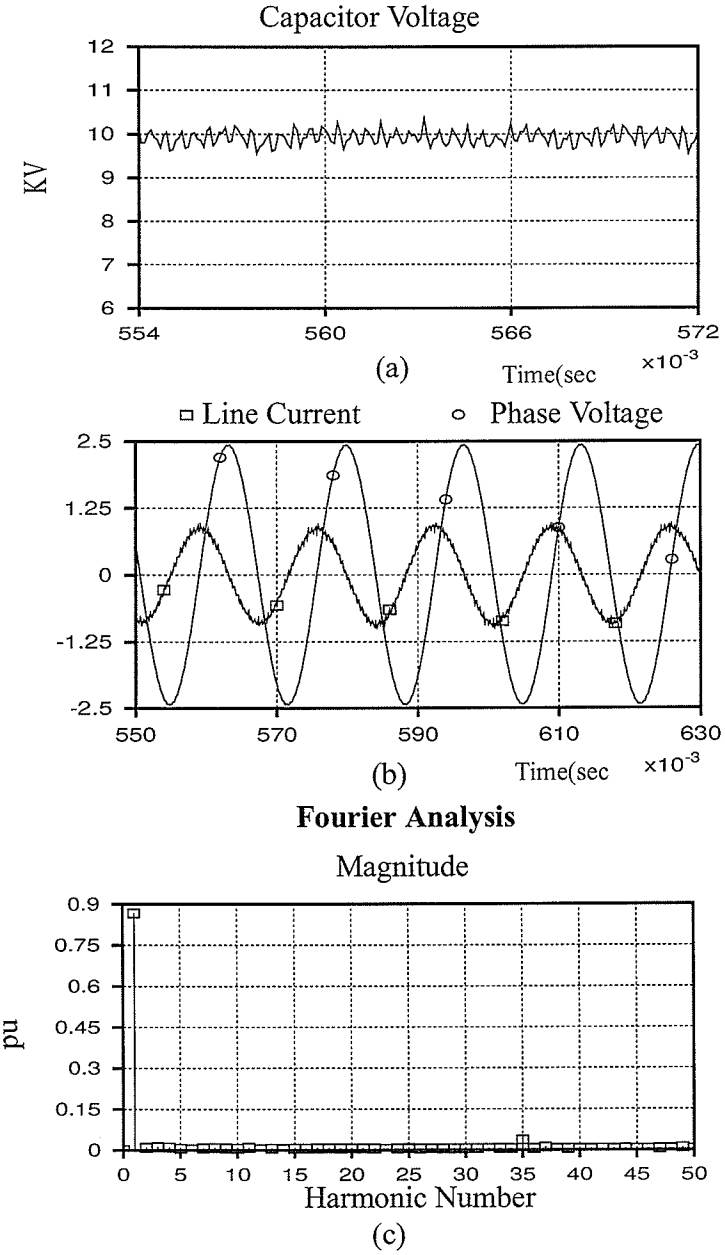


Fig. 5-12 36-Pulse STATCOM a) DC Capacitor Voltage, b) AC Voltage and Current (current is in pu and voltage is scaled by a factor of 0.03), c) Fourier Analysis of the AC Current

5.3 CONCLUSIONS

In this chapter the neural network controlled optimal PWM technique suggested by the author was used in two other applications: the AC-DC converter and the synchronous static VAR compensator (STATCOM). In the first application a single two-level converter was used that is connected through a three phase transformer to the ac system on one side and through a smoothing reactor to a dc load on the other side. A controller was developed for this converter which is based on the d-q decomposition of the ac current. An optimal PWM scheme with nine chops per quarter cycle was used for this system to eliminate all the ac current harmonics up to the 29^{th}. Simulation study shows that the system is able to keep the dc voltage at the ordered level with small ripple (less than 0.2%), and provide the ordered reactive power at the ac terminals. Extra series reactance is required to keep the current harmonics below 5%.

In the second application two converters are used that are connected in parallel at the dc side. On the ac side converters are connected to the power system through YY and YΔ transformers with series connected primaries. This arrangement is much more effective in reducing the ac current harmonics: the magnitude of the harmonics can be reduced to under 2% by using a PWM scheme with only five chops per quarter cycle and without extra series inductance. In general, the

studies show that the PWM technique suggested in this project can be successfully used in a variety of applications with different demands.

CHAPTER 6

CONCLUSIONS AND FURTHER WORK

Voltage Source Converters (VSC) are increasingly used in power conditioning applications such as uninterruptable power supplies, rectifiers, active filters, reactive power compensators, high voltage direct current power transmission, machine drives and many others. Reducing the harmonics generated by the VSC and its operating frequency (and the switching losses) are two major concerns specially in high power applications. Optimal pulse width modulation effectively reduces the VSC harmonics with the minimum number of switchings and hence

minimizes switching losses.

Principal Contribution

Although the optimal PWM method has been known for a long time, its application is limited partly because of the difficulties in implementation. The main contribution of this thesis is to show that a simple feed-forward artificial neural network can facilitate the implementation of the optimal PWM technique. Using the artificial neural network makes it possible to solve the governing equations of the optimal PWM and use the solutions to train the network all off line and without any time pressure. This method shows great advantages over solving the optimal PWM equations in real time. Compared to the conventional method of using look-up tables this method requires comparable amount of computational resources, but it is more flexible in accepting new input variables.

Validation

The validity of this method was studied through the extensive simulation studies of a number of applications including a voltage source inverter, PWM rectifier and a STATCOM. In all the studied applications the neural network was able to provide fast and accurate switching pulses for the inverter that satisfies the harmonic reduction requirements. The practicality of the proposed scheme was proved by building a hardware prototype that employs a digital signal processor board to

implement the neural network controller. This neural network provides the firing angles for the firing system which is another computer routine running on the same processor. Finally the firing signals are sent from the signal processing board to a driver circuit that controls a three phase IGBT bridge. The IGBT bridge is connected to a six pulse diode rectifier on the dc side and to an induction machine on the ac side. A personal computer was used as a host for the signal processing board and as a user interface. This prototype was used successfully to control the speed of the induction machine under a variety of load conditions, proving that the suggested method can be actually used under non-ideal work conditions where the dc voltage contains ripples, switching speed is limited, dead times between switching actions are required and so on. It was also shown that the processing time for the neural network can be reduced if necessary by using piece-wise linear characteristics for the neurons and a customized learning method.

Suggested topics for further work

The application of the neural network for generating optimal PWM waveform opens the door to a number of other applications that were considered beyond the scope of this project. Using a neural network to provide the optimal switching pattern for an active filter is a clear spin-off of the current project. Although active filters come in a variety of different arrangements, the core part of all of them is usually a voltage source converter that generates the specified harmonics at the ordered

magnitude and phase. These converters usually use standard sinusoidal PWM method with a high frequency triangular carrier. Using the optimal PWM for these converters can significantly reduce their operating frequency and switching losses.

Current controlled voltage source converters are widely used in machine drives and some other applications. These converters normally operate at very high switching frequency to be able to follow the reference current waveforms. Considering that in a normal induction or synchronous machine drive the machine current is sinusoidal most of the time, it seems to be possible to use the optimal PWM for these converters. This can reduce the switching frequency by up to two orders of magnitude. Obviously, to obtain a comparable transient response, proper controllers must be developed. The neural network also easily lends itself to on-line training and therefore is generally suitable for applications where the optimal switching pattern is selected intelligently based on the load and environmental conditions.

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APPENDIX A

THE FIRING CONTROL PROGRAM

A.1 THE PC PROGRAM

```
//This is just the same as pwmwin1 except that it is made possible to call
// PutV_F() from within the TMyEdit
#include <owl\framewin.h>
#include <owl\applicat.h>
#include <owl\scrollba.h>
#include <owl\edit.h>
#include <owl\groupbox.h>
#include <owl\radiobut.h>
#include <cstring.h>
#include <math.h>
#include <stdio.h>
#pragma hdrstop
#include "pwmwin3.rh"
#include "c30intfc.h"
#define Max_TextLen 5
#define MinVoltage 0.01
#define MaxVoltage 1.15
#define MinFrequency 1
#define MaxFrequency 200
//The Edit Window
class TMyEdit : public TEdit{
public:
  TMyEdit(TWindow* parent, int Id, const char far * text, int x, int y, int w, \
 int h, uint textLen,bool multiline, TScrollBar* scroller,char title);
  void EvKeyDown(uint key, uint repeatCount, uint flags);
  float val;
protected:
  TScrollBar* scrollPtr;
  float ScrollerMin,ScrollerMax;
  int scale;
DECLARE_RESPONSE_TABLE(TMyEdit);
};
DEFINE_RESPONSE_TABLE2(TMyEdit,TEdit,TStatic)
  EV_WM_KEYDOWN,
END_RESPONSE_TABLE;
```

```
//TMyEdit constructor
TMyEdit::TMyEdit(TWindow* parent, int Id, const char far * text, int x, int y,
int w, \
 int h, uint textLen,bool multiline, TScrollBar* scroller,char title)
:TEdit(parent,Id,text,x,y,w,h,textLen,multiline){
scrollPtr=scroller;
switch(title){
case 'V' : ScrollerMin=MinVoltage;
  ScrollerMax=MaxVoltage;
  scale=100;
  val=MinVoltage;
  break;
case 'F' : ScrollerMin=MinFrequency;
  ScrollerMax=MaxFrequency;
  scale=1;
             val=MinFrequency;
  break;
}
}
// The Main Window
class TScrollTest : public TFrameWindow {
public:
  TScrollTest(TWindow* parent, const char far* title);
  int c30init();
  static int PutV_F();
  int Round(double x);
protected:
  void SetupWindow();
  void Paint(TDC& dc,BOOL erase, TRect& rect);
  void EvHScroll(UINT scrollcode,UINT thumbPos,HWND hWndCtl);
  void EvEditResponse();
  void EvSize(UINT sizeType,TSize& size);
  void CmProgramExit();
private:
  TScrollBar* scroller1;
  TScrollBar* scroller2;
  static TMyEdit* Scroller1Value;
  static TMyEdit* Scroller2Value;
  TStatic*    Voltage;
  TStatic*    Frequency;
  TGroupBox*  radioGroup;
  TRadioButton* Indipendent;
  TRadioButton* Proportional;
  TStatic*  RatioTitle;
  TEdit*    RatioBox;
  static ulong Vinptr,Tptr,pwptr;
DECLARE_RESPONSE_TABLE(TScrollTest);
};
DEFINE_RESPONSE_TABLE1(TScrollTest,TFrameWindow)
  EV_COMMAND(CM_PROGRAM_EXIT,CmProgramExit),
```

```
  EV_WM_HSCROLL,
  EV_WM_SIZE,
END_RESPONSE_TABLE;
//initialization of static variables
TMyEdit* TScrollTest::Scroller1Value=0;
TMyEdit* TScrollTest::Scroller2Value=0;
ulong TScrollTest::Vinptr=0,TScrollTest::Tptr=0,TScrollTest::pwptr=0;
//FILE* TScrollTest::f2=0;
// constructor
TScrollTest :: TScrollTest(TWindow* parent, const char far* title)
  : TFrameWindow(parent,title),
 TWindow(parent, title)
{
  Attr.X=GetSystemMetrics(SM_CXSCREEN)/5;
  Attr.Y=GetSystemMetrics(SM_CYSCREEN)/7;
  Attr.H=Attr.Y*5;
  Attr.W=Attr.X*3;
  scroller1= new TScrollBar(this, ID_HScroll1, 150,50,125,20,TRUE);
  Scroller1Value= new TMyEdit(this,ID_EditBox1,"0.00",190,20,38,21,Max_TextLen,\
   FALSE,scroller1,'V');
  Voltage=new TStatic(this, ID_Voltage," Voltage",55,50,65,21,7);
  scroller2= new TScrollBar(this, ID_HScroll2, 150,130,125,20,TRUE);
  Scroller2Value= new TMy-
Edit(this,ID_EditBox2,"0.00",190,100,38,21,Max_TextLen,\
 FALSE,scroller2,'F');
  Frequency=new TStatic(this, ID_Frequency," Frequency",45,130,90,21,9);
  radioGroup=new TGroupBox(this,ID_RADIOGROUP,"       Voltage and Frequency Con-
trol      ",\
45,200,300,100);
  Indipendent=new TRadioButton(this,ID_INDIPENDENT,"Independent",\
50,240,100,25,radioGroup);
  Proportional=new TRadioButton(this,ID_PROPORTIONAL,"Proportional",\
50,260,100,25,radioGroup);
  RatioTitle=new TStatic(this,ID_RatioTitle,"Ratio (Hz/
p.u.Volts)",160,265,125,20);
  RatioBox=new TEdit(this,ID_RatioBox,"60",290,265,35,22,Max_TextLen,FALSE);
  AssignMenu(MENU_1);
  c30init();
}
//SetUp
void TScrollTest:: SetupWindow(){
TFrameWindow::SetupWindow();
scroller1->SetRange(MinVoltage*100,MaxVoltage*100);
scroller2->SetRange(MinFrequency,MaxFrequency);
   Indipendent->SetCheck(BF_CHECKED);
}
//Paint
void TScrollTest::Paint(TDC& dc,BOOL erase, TRect& rect){
TRect ClientRect, VoltageBox(54,48,120,71), FrequencyBox(44,128,135,151);
TFrameWindow::Paint(dc,erase,rect);
```

```
GetClientRect(ClientRect);
TBrush* brush=new TBrush(TColor::LtGray);
dc.SelectObject(*brush);
dc.Rectangle(ClientRect);
dc.RestoreBrush();
delete brush;
TPen* pen=new TPen(TColor::Black);
dc.SelectObject(*pen);
dc.Rectangle(VoltageBox);
dc.Rectangle(FrequencyBox);
dc.RestorePen();
delete pen;
}
// Size
void TScrollTest:: EvSize(UINT /*sizeType*/, TSize& /*size*/){
Invalidate();
}
//Definition of the Round function
int TScrollTest::Round(double x){
int integer=floor(x);
double frac=x-integer;
if(frac >= 0.5)
return (integer+1);
return integer;
}
// definition for the response function for scroller
void TScrollTest:: EvHScroll(UINT scrollcode, UINT thumbPos, HWND hWndCtl)
{
  char s1[Max_TextLen], s2[Max_TextLen],s3[Max_TextLen];
  // call ancestor
  TFrameWindow:: EvHScroll(scrollcode,thumbPos, hWndCtl);
  int p1=scroller1->GetPosition();
  double q1=p1/100.0;
  Scroller1Value ->GetText(s1,Max_TextLen);
  double qq1=atof(s1);
  if(fabs(qq1-q1)>=0.01){
sprintf(s1,"%.2f",q1);
Scroller1Value ->SetText(s1);
Scroller1Value ->val=q1;
if(Proportional->GetCheck() == BF_CHECKED){
RatioBox->GetText(s3,Max_TextLen);
double Ratio=atof(s3);
int p2=Round(q1*Ratio);
scroller2->SetPosition(p2);
      sprintf(s2,"%d",p2);
Scroller2Value ->SetText(s2);
Scroller2Value ->val=p2;
};
PutV_F();
return;
```

```
  };
  int p2=scroller2->GetPosition();
  Scroller2Value->GetText(s2,Max_TextLen);
  int pp2=atoi(s2);
  if(abs(pp2-p2)>=1){
sprintf(s2,"%d",p2);
Scroller2Value ->SetText(s2);
Scroller2Value ->val=p2;
if(Proportional->GetCheck() == BF_CHECKED){
RatioBox->GetText(s3,Max_TextLen);
double Ratio=atof(s3);
q1=p2/Ratio;
p1=Round(q1*100);
scroller1->SetPosition(p1);
sprintf(s1,"%.2f",q1);
Scroller1Value ->SetText(s1);
Scroller1Value ->val=q1;
};
PutV_F();
  };
}
//Response function for Exit command
void TScrollTest::CmProgramExit(){
  while( GetInt(NewDataFlag,DUAL) != 0)
;
 PutInt(NewDataFlag, DUAL,2);

//Hold();
CmExit() ;
}
//Response function for Edit Box
void TMyEdit:: EvKeyDown(uint key, uint repeatCount,uint flags){
char s[Max_TextLen];
TEdit::EvKeyDown(key,repeatCount,flags);
if(key == VK_RETURN){
this->GetText(s,Max_TextLen);
val=atof(s);
int p=val*(this->scale);
if(val<this->ScrollerMin){
val=this->ScrollerMin;
p=val*(this->scale);
};
if(val>this->ScrollerMax){
val=this->ScrollerMax;
p=val*(this->scale);
};
if(this->scale==100)
sprintf(s,"%.2f",val);
else
sprintf(s,"%d",p);
```

```
this->SetText(s);
(this->scrollPtr)->SetPosition(p);
TScrollTest::PutV_F();
 };
}
// The application class
class TScrollTestApp : public TApplication {
public:
  TScrollTestApp(const char far* name)
  : TApplication ( name) {};
  void InitMainWindow();
};
// Initialize program's main window
void TScrollTestApp::InitMainWindow(){
  MainWindow= new TScrollTest( 0,"PWMWIN3");
  MainWindow-> SetIcon(this,ICON_1);
}
#pragma argsused
// Main program
int OwlMain(int argc, char* argv[]) {
  TScrollTestApp app("Scroller");
  return app.Run();
}
//This function initializes the c30 board and sends the ANN's weights to it.
int TScrollTest::c30init()
{
 float w[100];
 int   nhid, nout, nweight, i;
 long int loadStat;
 ulong wptr,  nhidptr, noutptr/*,pwptr,Optr,a1ptr,a2ptr,a3ptr,phsptr*/;

//cout<<"in c30init";
/* reading weights from file */
 FILE* f1=fopen("weights.txt", "r");
  //f2=fopen("pwmout.txt","w");
 int end=fscanf(f1,"%d %d %d",&nweight,&nhid,&nout);

 if(end == EOF){
  printf("end of file!!");
  return -1;
 }

 for(i=0; i<nweight; i++){
  end=fscanf(f1,"%f",&w[i]);
  if(end == EOF){
   printf("end of file!!");
   return -1;
  }
 }
/* load DSP program */
```

```
 SelectBoard(BoardAdr);
 loadStat=LoadObjectFile("PwmDsp34.out") ;
 if(loadStat !=0){
  printf("unsuccessful load");
  return -1;
 }

 PutInt(PcProceedFlag, DUAL, 0);
 PutInt(NewDataFlag, DUAL, 0);
 Reset();                                /* start Dsp program */
 for(i=0; i<10000 && (GetInt(PcProceedFlag,DUAL) != 1); i++)
            ;  /* wait for PcProceedFlag. Dsp program is preparing
                  the address of w,Vin,... to be handed to the pc */
 if(i == 10000){
  printf("waiting too long for Dsp");
  return -1;
 }

 PutInt(PcProceedFlag, DUAL, 0);
 wptr=Get32Bit(wptradr,DUAL);          /* getting the location of */
 Vinptr=Get32Bit(Vinptradr,DUAL);      /*  various variables      */
 Tptr=Get32Bit(Tptradr,DUAL);
 nhidptr=Get32Bit(nhidptradr,DUAL);
 noutptr=Get32Bit(noutptradr,DUAL);
/*pwptr=Get32Bit(pwptradr,DUAL);
a1ptr=Get32Bit(a1ptradr,DUAL);
a2ptr=Get32Bit(a2ptradr,DUAL);
a3ptr=Get32Bit(a3ptradr,DUAL);
       phsptr=Get32Bit(phsptradr,DUAL);*/
 PutInt(nhidptr,DUAL,nhid);  /* putting information in Dsp memory */
 PutInt(noutptr,DUAL,nout);
 WrBlkFlt(wptr,DUAL,nweight,w);

}
//This function sends V and F to the DSP board   Aug 1/96
int TScrollTest::PutV_F(){

float Vin,freq,pw[115];
Vin=Scroller1Value->val;
freq=Scroller2Value->val;
  Vin=Vin*1.72-1.0;
  float T=(1/freq)/960e-9;
  while( GetInt(NewDataFlag,DUAL) != 0)      // wait until Dsp is ready to
;// recieve new data
  PutFloat(Vinptr,DUAL,Vin);
  PutFloat(Tptr,DUAL,T);
  PutInt(NewDataFlag,DUAL,1);
 /* while(GetInt(pflag,DUAL)!=1)
;
 PutInt(pflag,DUAL,0);
```

```
RdBlkFlt(pwptr,DUAL,114,pw);
for(i=0;i<114;i++){
fprintf(f2,"  %8.1f",pw[i]);
if(fmod(i,8)==0)
fprintf(f2,"\n");
}; */
  return 0;
}
```

A.2 THE DSP BOARD PROGRAM

```
/* Program PwmDsp33.c is the same as PwmDsp32.c except for returning the outputs
  to 0 when Comm1=2  */
#include <math.h>
#define PeriodReg          ((long *) 0x808028)
#define GlobalCtrlReg      ((long *) 0x808020)
#define CounterReg         ((long *) 0x808024)
#define InitTimer0         *GlobalCtrlReg=0x302L
#define HoldTimer0         *GlobalCtrlReg &=~0x80
#define UnHoldTimer0       *GlobalCtrlReg |=0x80
#define SetIntVect09       asm(" .sect \".int09\"");\
 asm(" .word _c_int09 ");asm(" .text")
#define en_int_8           asm(" OR 100h,IE")
#define dis_int_8          asm(" ANDN 100h,IE")
#define en_GIE             asm(" OR 2000h,ST")
#define DX0_for_output     *((long *) 0x808042) &=~0x10;\
 *((long *) 0x808042) |=0x60
#define togle_DX0          *((long *) 0x808042) ^=0x40
#define DX1_for_output     *((long *) 0x808052) &=~0x10;\
 *((long *) 0x808052) |=0x20
#define togle_DX1          *((long *) 0x808052) ^=0x40
#define FSX0_for_output    *((long *) 0x808042) &=~0x100;\
 *((long *) 0x808042) |=0x200
#define togle_FSX0         *((long *) 0x808042) ^=0x400
#define FSX1_for_output    *((long *) 0x808052) &=~0x100;\
 *((long *) 0x808052) |=0x600
#define togle_FSX1         *((long *) 0x808052) ^=0x400
#define CLKX0_for_output   *((long *) 0x808042) &=~0x1;\
 *((long *) 0x808042) |=0x6
#define togle_CLKX0        *((long *) 0x808042) ^=0x4
#define CLKX1_for_output   *((long *) 0x808052) &=~0x1;\
 *((long *) 0x808052) |=0x2
#define togle_CLKX1        *((long *) 0x808052) ^=0x4
#define FSR0_for_output    *((long *) 0x808043) &=~0x100;\
 *((long *) 0x808043) |=0x200
#define togle_FSR0         *((long *) 0x808043) ^=0x400
#define Reset_Outputs      *((long *) 0x808042) &=0x444;\
```

```
                *((long *) 0x808052) &=~0x444;
#define nrn(h)  1/(1+exp(-h))
#define min(A,B) ((A<B)? A:B)
int    nhid, nout, pulse,phase[115],stat1,stat2,stat3;
float  w[100],Vin,T,O[9],lasts-
witch,pulsewidth[115],alpha1[40],alpha2[40],alpha3[40];
extern float  *Comm2,*Comm3,*Comm7,*Comm9,*Comm10,*Comm11,*Comm12;
extern int    *Comm5,*Comm6;
extern long int Comm0,Comm1,Comm8;

void ANN(void);
main()
{
 int i,j,ij,k,i1,i2,i2j,i3j,i3;
 float mn,minn;
 /* transfer the addresses to pc */
 Comm2=w; Comm3=&Vin; Comm5=&nhid; Comm6=&nout; Comm7=&T,Comm9=pulsewidth;
 Comm10=alpha1;Comm11=alpha2;Comm12=alpha3;
 Comm0=1;
 Comm8=0;
 pulse=0;
 phase[0]=1;
 alpha2[38]=5;  /* to make sure that the last switching is for  */
 alpha3[38]=5;  /* phase 1 at alpha1=4 */
 stat1=1;stat2=0;stat3=1;
 SetIntVect09;
 InitTimer0;
 HoldTimer0;
 en_int_8;
 en_GIE;
 DX0_for_output;
 DX1_for_output;
 CLKX0_for_output;
 CLKX1_for_output;
 FSX0_for_output;
 FSX1_for_output;
 FSR0_for_output;
 *PeriodReg=100;
 while(1){
  while(Comm1 == 0)     /* wait for new data */
     ;
  if(Comm1 == 1){
   ANN();

   for(i=0;i<9;i++)      /* calculate all swtiching angles of phase 1 */
    alpha1[i]=O[i];      /* in one complete cycle                     */
   for(i=9;i<18;i++)
    alpha1[i]=2-alpha1[17-i];
   alpha1[18]=2;
   for(i=19;i<28;i++)
```

```
 alpha1[i]=2+alpha1[i-19];
for(i=28;i<37;i++)
 alpha1[i]=4-alpha1[36-i];
alpha1[37]=4;
for(i2=0;alpha1[i2]<2.66667;i2++) /* find the first switching angle after */
   ;                             /* 240 degrees                           */
for(i3=0;alpha1[i3]<1.33333;i3++) /* find the first switching angle after */
   ;                              /* 120 degrees                           */

for(j=0;j<38;j++){   /* calculate switching angles for phases 2 and 3*/
 i2j=i2+j;
 i3j=i3+j;
 if(i2j>37)
  i2j-=38;
 if(i3j>37)
  i3j-=38;
 alpha2[j]=alpha1[i2j]+1.333333;
 if(alpha2[j]>4)
  alpha2[j]-=4;
 alpha3[j]=alpha1[i3j]+2.666667;
 if(alpha3[j]>4)
  alpha3[j]-=4;
}
i1=0;i2=0;i3=0;lastswitch=0;  /* calculating the time interval between */
HoldTimer0;                   /* switching instant */
for(k=0;k<114;k++){
 mn=min(alpha1[i1],alpha2[i2]);
 minn=min(alpha3[i3],mn);
 if(minn == alpha1[i1]){
  pulsewidth[k]=(alpha1[i1]-lastswitch)*T;
  phase[k+1]=1;
  lastswitch=alpha1[i1];
  i1++;
 }
 else if(minn == alpha2[i2]){
  pulsewidth[k]=(alpha2[i2]-lastswitch)*T;
  phase[k+1]=2;
  lastswitch=alpha2[i2];
  i2++;
 }
 else{
  pulsewidth[k]=(alpha3[i3]-lastswitch)*T;
  phase[k+1]=3;
  lastswitch=alpha3[i3];
  i3++;
 }
}
Comm8=1;
 UnHoldTimer0;
 Comm1=0;
```

```
  }

  if(Comm1 == 2){
   HoldTimer0;
   Reset_Outputs;
   return 0;
  }
 }
}
void c_int09(void)
{
 int i,k=1;
 HoldTimer0;
 *PeriodReg=pulsewidth[pulse];
 *CounterReg=0;
 if(phase[pulse] == 1){
  if(stat1==1){
   togle_DX1;
   stat1=0;
   for(i=0;i<k;i++)
    ;
   togle_DX0;
  }
  else{
   togle_DX0;
for(i=0;i<k;i++)
    ;
   stat1=1;
   togle_DX1;
  }
 }
 else if(phase[pulse]== 2){
  if(stat2==1){
   togle_FSX1;
   stat2=0;
for(i=0;i<k;i++)
    ;
   togle_FSX0;
  }
  else{
   togle_FSX0;
   stat2=1;
for(i=0;i<k;i++)
    ;
   togle_FSX1;
  }
 }
 else{
  if(stat3==1){
   togle_CLKX1;
```

```
   stat3=0;
for(i=0;i<k;i++)
    ;
   togle_CLKX0;
  }
  else{
   togle_CLKX0;
   stat3=1;
for(i=0;i<k;i++)
    ;
   togle_CLKX1;
  }
 }

 pulse++;
 if(pulse == 56)
  togle_FSR0;
 if(pulse == 114){
  pulse=0;
  togle_FSR0;
 }
 UnHoldTimer0;
}

/* function ANN calculates the outputs of a neural network, given the
   number of neurons in each layer and weights in Xerion format */
void ANN(void)
{    int nh,no;
 extern float w[],O[],Vin;
 extern int nhid,nout;
 float Ohid[10],hhid[10],hout[10];
 int i,j,nx=-1;
 for(i=0; i<nhid;i++){
  nx++;
  hhid[i]=w[nx];

 }
 for(i=0;i<nout;i++){
  nx++;
  hout[i]=w[nx];

 }

 for(i=0;i<nhid;i++){
  nx++;
  hhid[i] += Vin*w[nx];
  Ohid[i]=nrn(hhid[i]);

 }
```

```
 for(i=0;i<nhid;i++){
  for(j=0;j<nout;j++){
   nx++;
   hout[j] += Ohid[i]*w[nx];

  }
 }
 for(i=0;i<nout;i++)
  O[i]=nrn(hout[i]);

}
```

APPENDIX B

THE NEURAL NETWORK PARAMETERS

In this appendix the weights and biases for the neural network used in Chapter 4 (Fig. 4-5 and Fig. 4-6) are presented. W1 is the matrix of weights between the input (V1) and the neurons in the hidden layer (five neurons) and B1 is the matrix of biases for them. W2 is the matrix of weights between the the hidden layer and output neurons (nine neurons) and B2 is the matrix of biases for output neurons.

$$W1 = \begin{bmatrix} -14.472779 \\ -76.712912 \\ -383.11309 \\ 0.10446498 \\ 22.067927 \end{bmatrix}$$

$$B1=\begin{bmatrix} 2.2067927e+001 \\ 9.3729853e+001 \\ 7.3796606e+000 \\ 4.4835525e+002 \\ -1.1472984e+000 \end{bmatrix}$$

$$W2=\begin{bmatrix} -9.4376434e-001 & 5.7701206e+000 & 1.4187515e+001 & 7.5706376e+000 & -2.6013973e+001 \\ 9.6613778e+000 & 2.1138645e+000 & 5.6744933e+000 & 9.9215435e+000 & 9.4934452e+000 \\ 6.7287376e+000 & 2.6605783e+000 & 6.1574415e+000 & 8.5449809e+000 & -1.5590635e+001 \\ 1.2630738e+001 & 2.8603460e+000 & 4.8405978e+000 & 9.9881710e+000 & 9.5091637e+000 \\ 1.1044512e+001 & 3.0521592e+000 & 4.8260510e+000 & 8.9067722e+000 & -1.2618835e+001 \\ 1.7373982e+001 & 6.6928080e+000 & 3.3739890e+000 & 9.9334807e+000 & 1.0109982e+001 \\ 1.7337490e+001 & 6.1921759e+000 & 3.0717608e+000 & 9.2441584e+000 & -1.2155914e+001 \\ 1.2442376e+001 & 2.2162922e+001 & 8.2079350e-001 & 9.7177541e+000 & 1.1074115e+001 \\ 1.3359061e+001 & 2.1697724e+001 & 6.2807957e-001 & 9.2401377e+000 & -1.3166383e+001 \end{bmatrix}$$

$$B2=\begin{bmatrix} -2.2174204e+001 \\ -3.1526206e+001 \\ -2.1340697e+001 \\ -3.3619178e+001 \\ -2.5191099e+001 \\ -4.0214074e+001 \\ -3.2780863e+001 \\ -4.7678262e+001 \\ -4.1059082e+001 \end{bmatrix}$$