A VLSI TACTILE SENSOR BUILDING BLOCK

by

Gerald Walter Klym

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ABSTRACT

Two CMOS VLSI circuits have been designed and manufactured to examine the viability of constructing a tactile sensor array which determines the edge point outline of an object. Several hardware algorithmic strategies were examined and features of each strategy were combined to implement the final design. The manufactured integrated circuits successfully carried out the required tasks of detecting a pressure stimulus, determining the object's edge outline, and transmitting the edge point array to a remote processor. The object outline is available in a format which could be used for object identification and orientation. In a hypothetical 100 x 100 pixel sensor using the selected design, a tactile image refresh rate in excess of 600 kHz. could be achieved. The determination was made that substantial speed improvements could be realized by implementing a custom designed operational amplifier in place of the biased inverter amplifier used in the test ICs. It was also concluded that future construction of tactile sensors could be made in a layered structure with the necessary computing circuitry placed underneath the metal contact pad. This implementation would lead to sensors with improved spatial resolution properties. The ICs were manufactured by Northern Telecom in a 3 μm dual metal layer process. The completion of the design work was made possible through the cooperation the University of Manitoba VLSI Laboratory and the Canadian Microelectronics Corporation.

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I would also like to express appreciation to Dr. H. C. Card for the use and access to the University of Manitoba VLSI laboratory facilities. Appreciation is extended to Dr. R. D. McLeod for participating in technical dicussions which aided in arriving at the implemented hardware design. A great appreciation is also extended to Messrs Peter Hortensius, Christian Schneider, and Roland Schneider for their invaluable guidance and assistance in the techniques of creating and arranging the manufacture of the VLSI design through cooperation with the Canadian Microelectronics Corporation and Northern Telecom.

Finally, I thank the Manitoba Telephone System for the time and financial support which was granted to complete this thesis.

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CHAPTER 1

INTRODUCTION

An intelligent tactile sense for a robotic gripper is necessary for a variety of manufacturing applications. A problem arises in the processing of a large amount of data from a high resolution sensor. Demand on a controlling computer would be excessive in order to carry out the required computations. An intelligent sensor would perceive a tactile stimulus and process the data into an image. In this thesis VLSI circuits are described which were developed to form the active elements in detecting a tactile stimulus, and to calculate the edge points of an object handled by a robotic gripper. The circuits have been designed as building blocks which can be physically laid out to construct a large array. The sensor would be implemented in the manufacture of a robotic gripper, thus enabling the gripper to detect and process a tactile pressure stimulus.

The characteristics of the human tactile sensory apparatus have been vigorously studied since the 1930s. An overview is presented in Chapter 2.

The algorithm which determines the edge points from raw pressure data was developed by Lee Luang Hong in her Master's thesis. [1] The four nearest neighbor edge point algorithm formed the basis for the hardware manipulation strategies developed in Chapter 3.

In Chapter 4 the features of three hardware strategies are combined to create the final hardware circuit configuration. Details of all sections of the design are highlighted along with a presentation of the operation of the complete design. To prove the viability of the design two hardware circuits were created to test the performance of the chosen strategy. Considerations are included concerning the operation of a large tactile array which could be constructed from the individual nine pixel VLSI circuits.

Chapter 5 contains ideas which would be necessary in implementing the tactile array edge processor into a working robotic gripper which would transmit an object's edge point outline.

The results of the circuit performance evaluation are highlighted in Chapter 6. The single-pixel circuit test examined the performance of the pressure detection, and the edge point determination. The nine-pixel circuit provided a basis for testing the complete system operation, and was used in a simulation of a larger working tactile array.

Chapter 7 documents the overall performance parameters of the manufactured design and makes recommendations for improvements and future work in the field of tactile system design and application.

CHAPTER 2

HUMAN TACTILE SENSORY APPARATUS [1]

2.1 Cutaneous Mechanisms

The most diffuse human sense known is located in the skin of man. The sense has been referred to as "touch", but serves many other purposes. Its diversity has lead to a dilemma on whether the sense should be classified as one sense or several. Although various cutaneous sensations are often considered together, this discussion will be confined to sensations which are originated in the skin. An attempt to quantify the mechanoreceptive processes will be carried out for comparison with tactile sensor resolution and tactile pixel size considerations.

The analysis will examine the properties behind the concept that cutaneous sensation responds to "stimuli vs. signal" in reacting to an action impressed upon it. All receptor types will be identified, and will be associated with the communication network which transmits the sensory information. The various locations in the human body will be examined where the sensory information is processed. The concept of threshold in the receptor firing mechanism will be analyzed with special attention to the mechanoreceptor sensors. Spatial resolution of all cutaneous sensors will

[1] Concepts and figures throughout this chapter are from references 2 and 3.

be presented. Finally, a comparison of human and mechanical systems will be done to establish a reference for engineering design considerations.

2.1.1 Receptor Types

There exist two main families of receptors in the skin, the 'free' terminals and the 'organized' corpuscular receptors. The free terminals are uniformly distributed over the entire body. The more specialized corpuscular receptors have a high concentration in various areas of the skin. The free terminals have often been identified as passive recipients of various stimuli. In contrast, the corpuscular receptors have very individual reactions to different applied stimuli. The four main stimuli to which the receptors react are: cold, heat, touch and damaging pressure. The thermoreceptors are a group which respond to variations in temperature. Mechanoreceptors react to touch, pressure, and vibration. Lastly, nociceptor units signal pain when a damaging stimulus is applied to the skin. Figure 2.1 shows a cross section of the first three layers of human skin. Observe the layered structure, the spatial distribution, and the multiple sizes of the various receptor units. Note also the connection method and path of nerve fibers which conduct the generated sensory signals.

This thesis, being concerned with the development of an intelligent electromechanical tactile sense, includes a

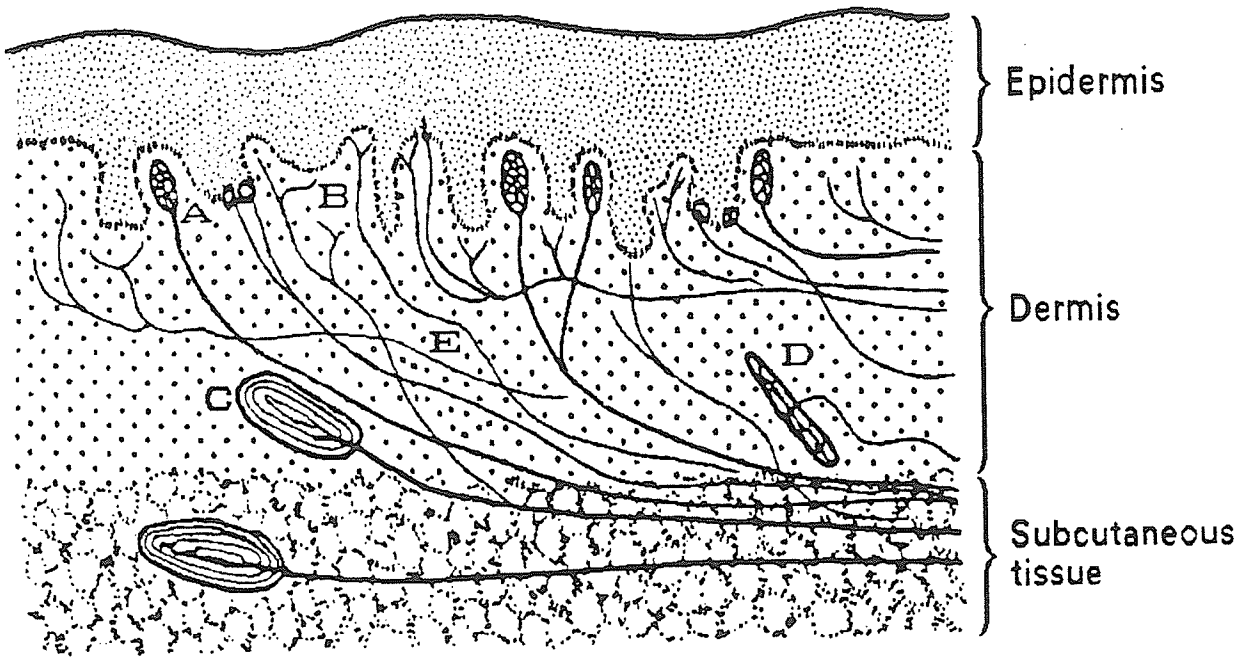


Figure 2.1. Cross section of the first three layers of human skin. Receptors A, C, and D are mechanoreceptors. Area B contains a Nerve Ending Bundle. Area E contains Nerve Fiber Pathways.

detailed analysis of the mechanoreceptors. The operation of these units will serve as a model to be emulated and possibly surpassed in sensor parameters such as spatial resolution, sensitivity, dynamic range, and physical durability.

2.1.2 Mechanoreceptor Units

Mechanoreceptors can be subdivided into three categories according to the reaction adaptation to touch. These are: slowly adapting, rapidly adapting, and very rapidly adapting. Adaptation is illustrated in that a reaction to a stimulus in a very rapidly adapting corpuscle will occur quickly and then decay very quickly to a steady state. In contrast, the reaction of a slowly adapting corpuscle rises less quickly but will maintain an output response for a longer period before returning to a steady state. See Fig. 2.4. Slowly adapting units detect the position and velocity of a stimulus, rapidly adapting units detect velocity, and vibration, and very rapidly adapting units detect transients in both position and velocity.

2.1.3 Stimulus Conduction

The growth or construction of the network which links the sensory receptors to the information processing areas of the body is called myelination. Both the mechanoreceptors and nociceptors communicate with the spinal column and the brain, which process the received tactile information. Both

types of receptors have both myelinated and unmyelinated channels of communication which tactile signals must traverse. Myelinated receptors are those cells which pass their signals along well structured paths, more generally known as large and small nerve fibers. Many such fibers can simultaneously detect signals from one or a group of receptor cells. See Fig 2.2.a for a representation of the multiple pathway nerve fiber myelinated system. These nerve fiber channels carry signals which report nearly in parallel to the spinal column. On the other hand, unmyelinated receptors depend upon intercell communication via physically larger sensory axons to pass the tactile information. Myelinated fibers are constructed of long, elastic, flexible cells, where sensory axons are made up from stacks of regularly shaped cells surrounded by a membrane.

A combination of receptors coupled to large and small myelinated fibers and sensory axons form a nerve trunk. When a stimulus is applied to a nerve trunk, the large myelinated fibers are aroused first, then the smaller myelinated fibers, and eventually the unmyelinated fibers. Figure 2.2.b shows a multiple nerve fiber reaction to a single pressure stimulus. Finally a stage of saturation is reached where no further increase in the stimulus activates more nerve fibers. The unmyelinated fibers transmit their signal by a physical deformation known as cable spread. Myelinated fiber conduction occurs in a

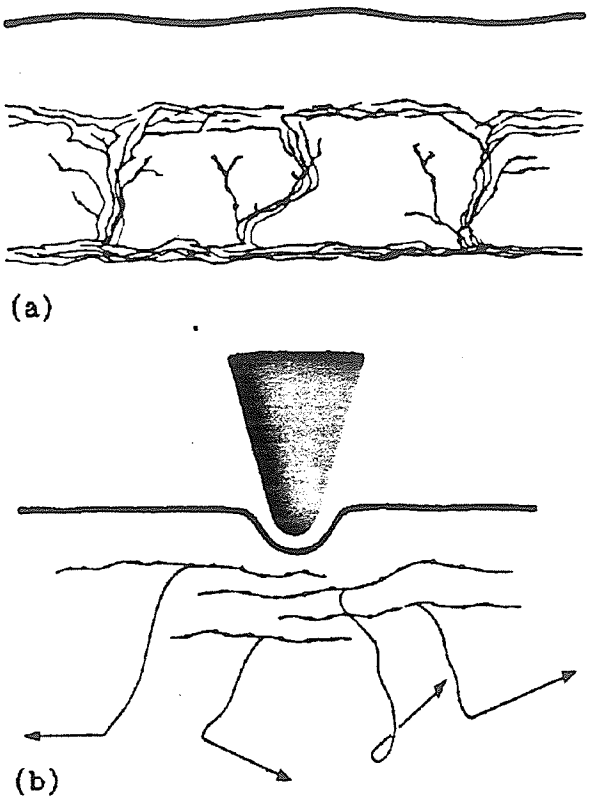


Figure 2.2. a. Multiple nerve fibers forming signal conduction trunks.

b. A multiple nerve path reaction to a single stimulus.

series of jumps through their elongated cells. This type of conduction is considerably faster than cable spread. When a stimulus is applied to a nerve trunk the resultant signal can be recorded some distance away as a series of electrical disturbances. The observed signals are of various intensity and are separated in time as each type of fiber in a sensory region has a different conduction velocity. The large myelinated fibers conduct faster than the small ones, and the unmyelinated fibers conduct the slowest of all.

There are various ways in which information about the texture, position, and hazard potential of an object are conveyed to the central nervous system. Firstly, certain sensory paths are dedicated to a specific type of information. Signals received on a specific path identify only one type of stimuli. Secondly, the number of impulses received per unit time and the timing between the pulses carry specific information. Finally, the virtual number of signals received on different paths will inform the nervous system about the nature of the object. Figures 2.3 and 2.4 show signals detected at a remote location in the human skin. These signals were generated by applying the pressure stimulus shown, to the index finger of a human subject.

2.1.4 Cutaneous Information Processing

The posterior horn of the grey matter of the human spinal cord provides the first opportunity for the sensory

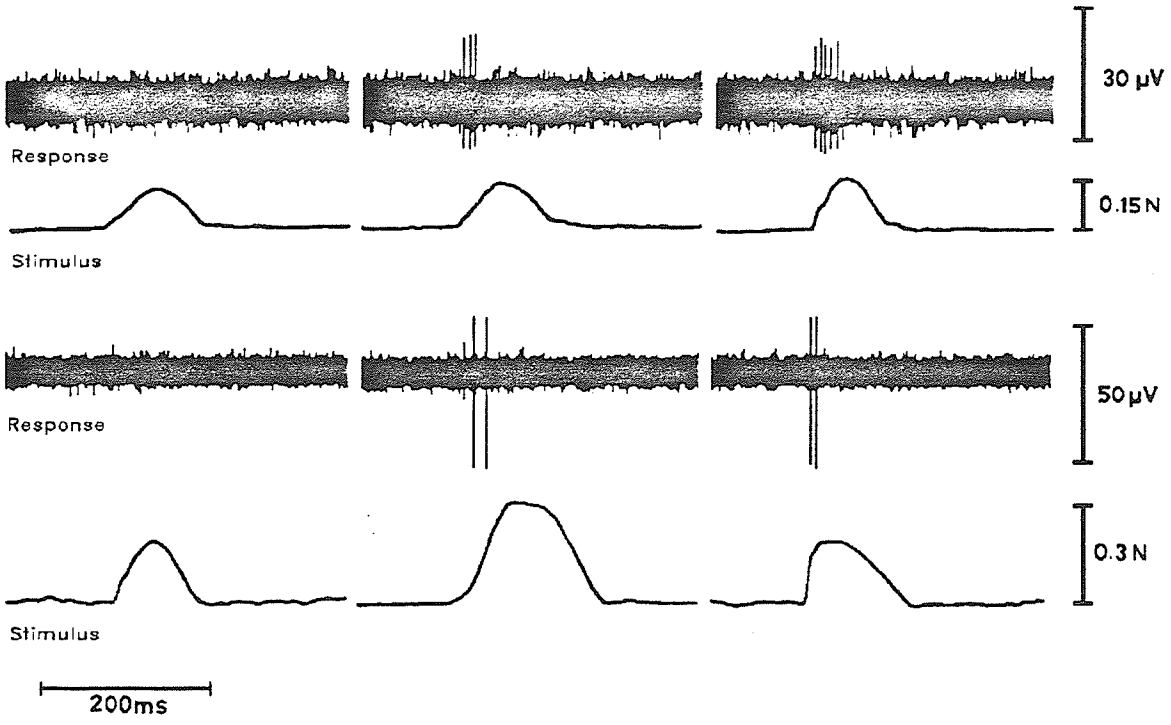


Figure 2.3. Remotely Detected Sensory Signals.

Notice that a certain pressure threshold must be crossed prior to a sensory signal being generated. Note the bottom right section showing that a lower pressure, but being applied quickly, will cause a response.

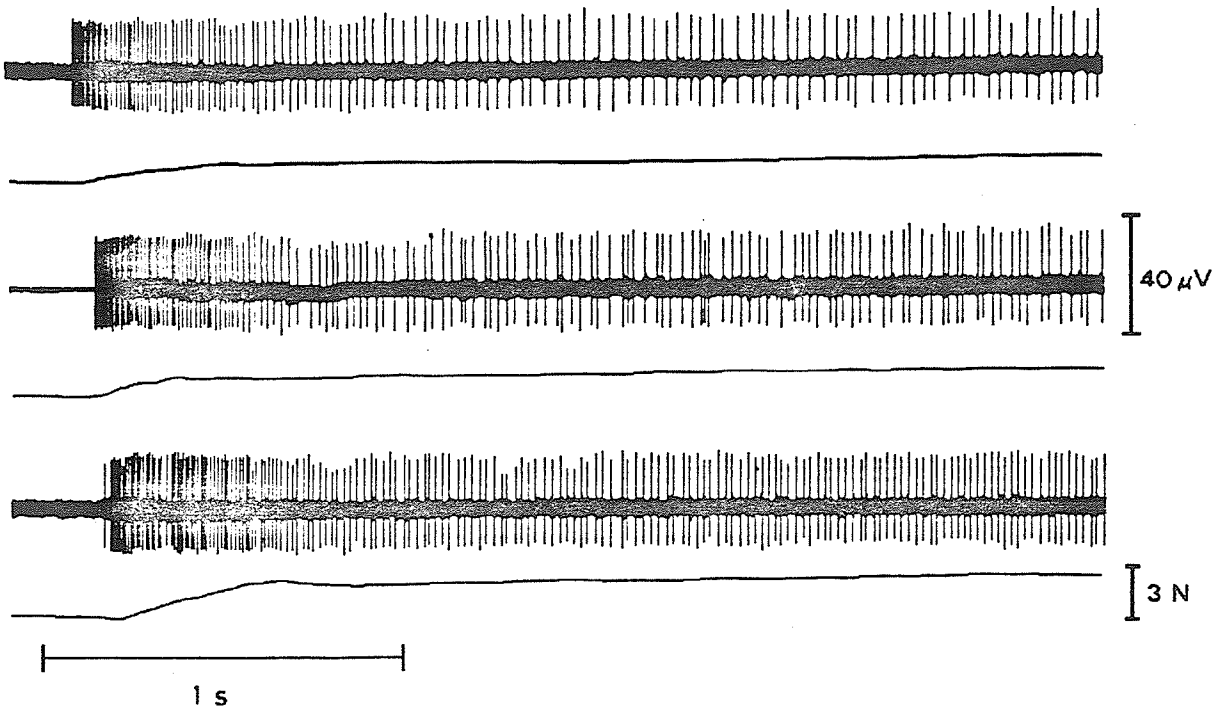


Figure 2.4. Remotely Detected Sensory Signals.

Highlighted are the threshold property of stimulus reaction and the tapering off of the response to a steady state pressure.

message to be modified. The cells it contains receive a wide variety of inputs and can either facilitate or inhibit further propagation of the stimulus. The response of the posterior horn to incoming stimuli can act to increase, reduce, or entirely suppress the sensory message. Suppression may occur if there is concurrent arrival of other messages, or if information originating in the brain is being distributed by the nervous system. In Fig. 2.5 signals applied to the editing node produce a resultant signal which is passed along.

The thalamus and the cerebral cortex form the major areas of the brain concerned with cutaneous sensation. The thalamus can be divided into two main regions of sensory impulse processing. One area is designated to the head region, while the other region handles all impulses from the body and limbs. Beyond the thalamus the anatomy of the sensory system becomes much more vague. The large number of myelinated fibers emerging from the thalamus to a great extent terminate in the primary sensory cortex. There also exists a secondary sensory area. Both sensory processing areas of the brain are closely coupled to the primary motor activity center as suggested in Fig. 2.6. This tight coupling is both in proximity and in the large number of interconnecting pathways.

Throughout the sensory pathway all information originating at any type of receptor is subject to the

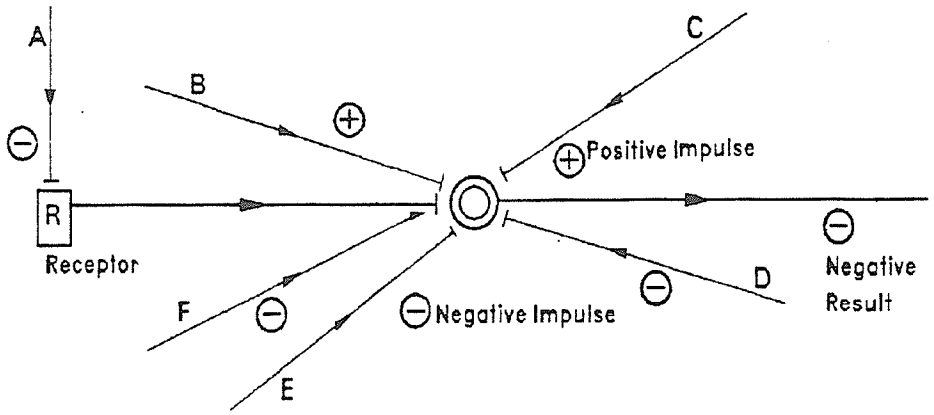


Figure 2.5. Stimulus Conduction or Suppression at a Signal Editing Node.

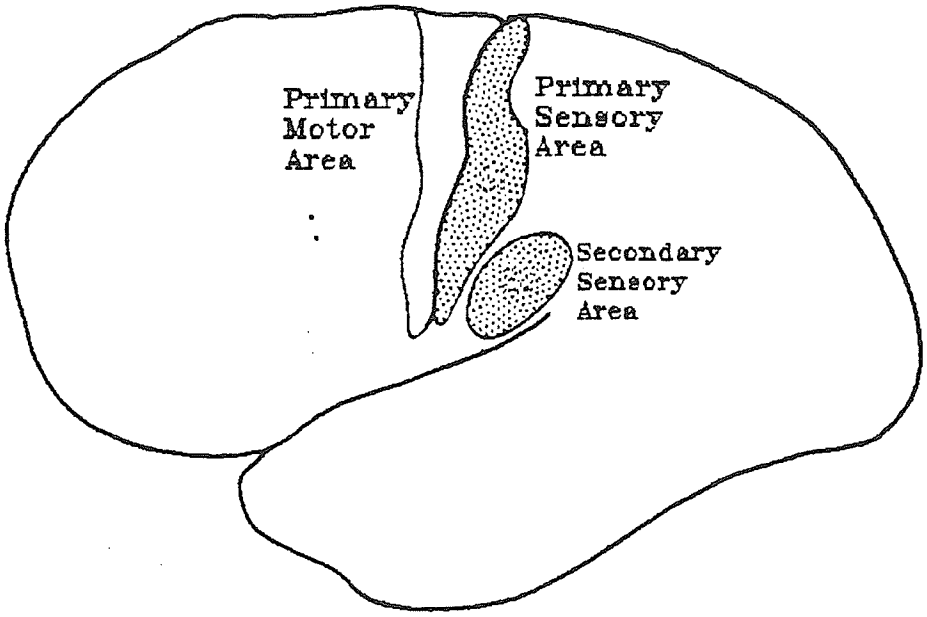


Figure 2.6. Left Cerebral Hemisphere.

Shown are the location of the Sensory and Motor Control processing areas of the brain.

concept of editing. Without this selective filtering of information at each exchange point in the system, the brain would be constantly bombarded with an overload of sensory input. The editing takes place at several locations along the complete sensory pathway. Many examples of the nature of sensory information editing exist. Receptors which are stimulated in a constant manner transmit briefly, and then no longer transmit further information. Concentrations of nerve fibers will not pass further signals until the number of received signals, or the intensity of these signals crosses a predefined threshold. The spinal column attenuates or amplifies impulses under the control of other activity present on the nervous system at that time. Finally, the brain allows selective attention to certain information controlled by the amount of conscious activity presently attributed to a specific region of the body. The brain is the editing control center, initiating appropriate reactions to the highest priority sensory inputs.

2.1.5 Detection Thresholds

As previously stated, several types of mechanoreceptors and nociceptors are capable of generating impulses as a result of tactile stimuli. In order to fire off a sensory receptor, the amount of stimulation energy applied to it must reach a certain prescribed level. Upon the application of a stimulus, the permeability of the receptor membrane changes and triggers a generator current. Then a

local depolarization in the receptor occurs causing the production of a generator potential. Eventually, a dedicated zone of the receptor-nerve fiber junction is triggered to fire off an impulse to be transmitted by the fiber. The required energy level to trigger a receptor is known as the excitation threshold. Every sensation aroused in the skin has a detection threshold which depends on many factors including the excitation threshold. The sensory thresholds of the skin are very much higher than those of the specialized senses. For detection of a cutaneous stimulus, energy levels must be one hundred million to one trillion times higher as compared to the arousal of vision or hearing.

Many factors affect the detection threshold of the skin. An area with a high density of receptors will naturally have a lower detection threshold than an area with more sparsely located receptors. The lower detection threshold is a direct result of the cumulative properties in the posterior horn which will detect a sensation purely upon the number of received impulses, even though the intensity of each individual impulse was too low to be detected. The physical thickness of the skin will affect the threshold. This fact is supported by the observation that detection thresholds are higher in the lower limbs where thicker skin is found in comparison with the upper limbs. A mechanical stimulus readily felt on the finger may not be noticed when applied to a toe.

The thresholds for intensity and duration of a stimulus vary independently and also vary with different subjects. A low energy stimulus may not create a response, but an increase in intensity or the size of applied area will arouse more receptors resulting in the experience of a sensation. A short application of a specific stimulus may not arouse any receptors where a more prolonged application at the same intensity may do so.

Thresholds vary with the frequency of stimulus application. A low intensity stimulus applied infrequently may not be detected. With the same stimulus applied at an continually increasing frequency, a point will be reached where a tactile sensation is generated.

2.1.6 Spatial Resolution

The spatial resolution of cutaneous receptors varies greatly throughout the human body. The density of touch or pain sensors is much greater than the density of other receptors such as those which detect heat or cold. If a physically small enough stimulus is used to examine a selected area of the skin, it will be found that thresholds are low in certain sensitive spots and are higher in the regions in between the spots. It is doubtful that sensory spots are really separate and discrete. It is more probable that gradients of sensitivity exist. The gradients are due to the overlapping arrangement of receptors with various

detection thresholds. Experimental results which show the existence of sensory spots may be explained by assuming the receptors are closer to the surface, or have lower detection thresholds.

External sensory experiments and physiological examinations have led to approximate receptor size and density values. The values vary throughout the body. In Table 2.1 receptor size values are presented as a range of the smallest and largest known bodies which perform the particular stated function. Density figures are given on average, and in relation to a specific location on the body.

Table 2.1 Size and Spatial Density of Mechanical Stimulus Receptors

Type of Receptor	Size	Density	Location
Slowly Adapting Mechanoreceptor	.1 x .4 mm - .15 x 2 mm	1 - 2 /cm^2 25 - 30 /mm^2	Throughout Fingertip
Rapidly Adapting Mechanoreceptor	30 x 80 µm - 1 x 4 mm	14 - 20 /mm^2 40 - 100 /mm^2	Throughout Fingertip
Very Rapidly Adapting Mechanoreceptor	.1 x .5 mm - 1 x 4 mm	1 - 2 /mm^2 5 - 10 /mm^2	Throughout Fingertip
Mechanical Nociceptor	.2 x .8 mm - .5 x 3 mm	0 - 1 /mm^2 3 - 20/mm^2	Throughout Fingertip

Figure 2.7 shows a schematic drawing of receptive fields mapped by single fiber stimulation. Below are histograms showing the distribution of the field sizes of

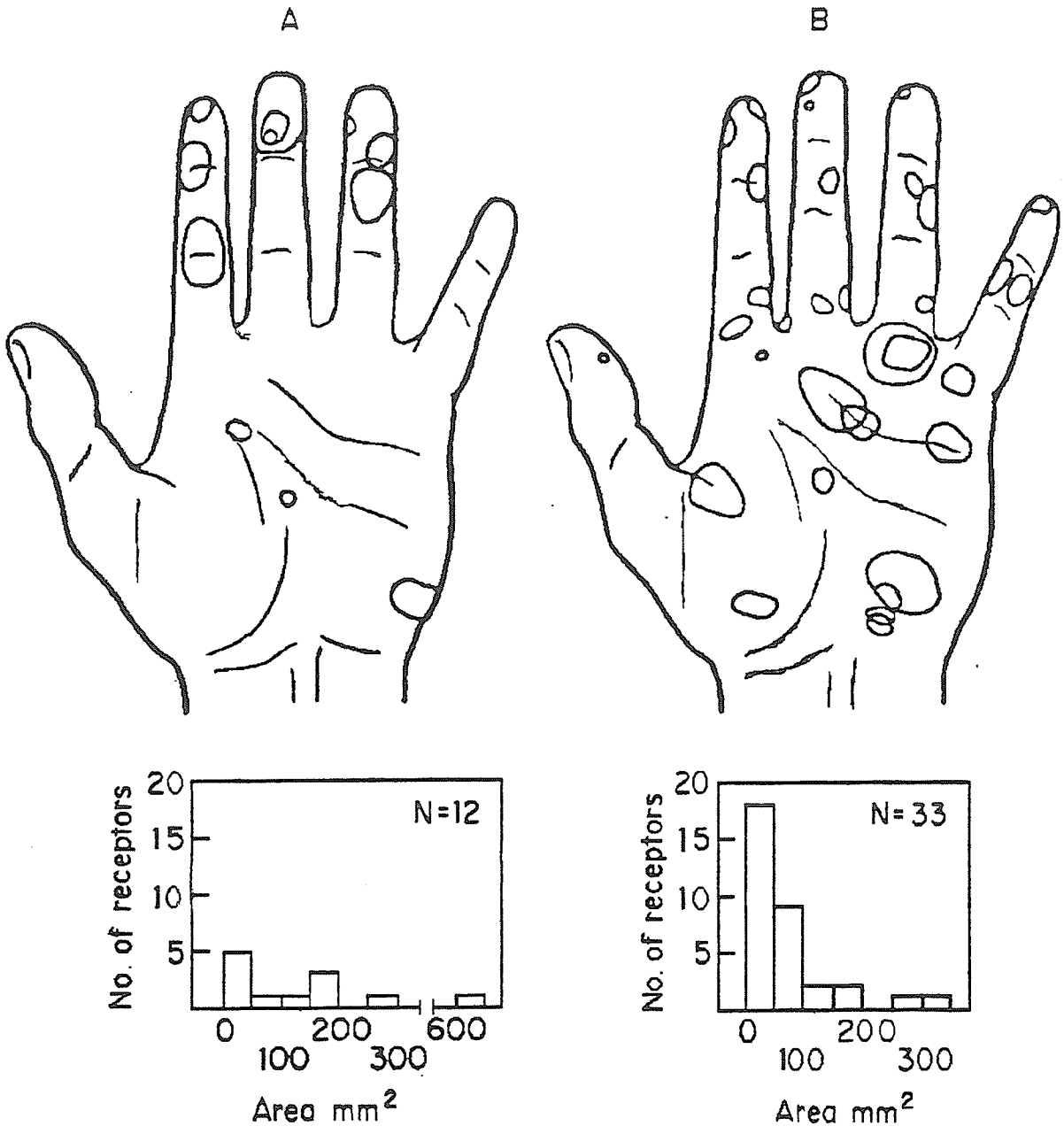


Figure 2.7. Distribution of the Field Sizes of the same type of Receptors (A - Rapidly Adapting B - Slowly Adapting) in the Human Hand.

the same units. Diagram A shows rapidly adapting units and diagram B shows slowly adapting units.

2.2 Comparison of Human and Engineering Tactile Properties

The human tactile sensory apparatus is compared to properties which will be incorporated into the engineering design of the electromechanical touch sensor system.

The human system operates with low level mechanical stimulation which results in the transmission of low amplitude electrical signals. These signals may stimulate areas of the nervous system which will act to amplify the signal if it is deemed necessary to pass along the information for processing. The touch sensor system also will operate with low level mechanical input by using a piezo electric film which generates low level electrical signals. Each individual touch sensor pixel will be equipped with an amplifier to bring the signal up to a standard TTL level prior to further processing.

In processing the information obtained from the receptors, the human system performs some of the task locally in the skin and nervous network. The remainder of the information processing is performed in the posterior horn of the spinal cord and the brain. For example when a damaging stimulus is detected by the hand, it is withdrawn nearly instantaneously. The determination to remove the offending stimulus is decided in the hand and the nervous

network connecting to the spinal cord. The kinesthetic signal generated to relieve the situation may also have originated in these areas without direct communication from the brain. It was not necessary for the complete signal to be received by the brain prior to an action being taken to remove the hand. It is also thought that some limited amount of pattern and object recognition is performed locally by the skin and nervous system. The human subject does not consciously have to think, to determine what is in his hand. The hand and nervous system cooperate to present the brain with a compiled image of whatever the hand is examining.

The sensor system attempts to duplicate the action of shared processing; a portion is carried out locally in the sensor which then transmits an outline of an image to be further processed elsewhere in the system. The local processing will be in the form of edge determination of the object in contact with the sensor and then the transmission, to the controlling computer, of information concerning only the location of edge points. The local processing will free a central computer from the task of receiving and then processing a vast amount of redundant data. By using this type of image transmission the central computer will directly concern itself only with object recognition and position.

In the human system many tactile receptors combine

their output to form a unified train of signals. This information is then transmitted over one or more links, to areas of the body which will make use of the information. The form of the complete tactile image is created and then transmitted. This process is replicated in the electromechanical touch system. All tactile pixels communicate with their neighboring pixels to determine the outline of an object. The transmission channel is one dedicated serial link. The controlling computer only receives the compiled outline in a format in which it can be quickly and easily interpreted.

The human hand is not well suited to work in a harsh environment. It can be easily crushed, punctured, or damaged by excessive pressure, sharp objects, chemical exposure or extreme temperature. It is, however, equipped for quick detection and release of a harsh stimulus to minimize damage. The human system does possess the ability of self healing to recover over time, from damage which is not too severe.

The delicate touch sensor system is also subject to damage from an extreme environment. Appropriate protection systems must be incorporated into the design to prevent damage. These protection systems will act to isolate the touch sensors and warn of impending destructive forces. The array of touch pads will have to be covered by a protective coating or an array of mechanical isolation devices which

will still maintain sufficient sensitivity for the task at hand. The isolation system must be easily replaceable in the event of damage. The sensor system will also be coupled with larger, less resolute, proximity or gross contact sensors. The purpose of these will be twofold. Firstly, the larger sensors will warn that contact with an object is imminent, and that the touch sensor system will soon be activated. Secondly, depending on the operating environment the large sensors must have the capability to recognize extreme temperature or a damaging chemical stimulus. If harsh stimuli are detected, processes will then have to occur to prevent damage to the more sensitive tactile array.

Incorporated in the human tactile system is the ability to detect and report upon a wide range of stimulation energy levels. This ability aids in the determination of texture, shape, and the location of edges of an object under examination. It also provides a feedback mechanism to the amount of pressure exerted on an object. The tactile system to be constructed only operates on a binary threshold principle indicating the presence or lack thereof of a portion of an object at that point. Other researchers have constructed a sensor system which operates with multiple thresholds. The design under discussion was created with a binary threshold system mainly due to VLSI real estate constraints and because access to analog circuitry for the construction of an analog to digital conversion circuit was not readily available.

The pixel resolution of the electromechanical tactile system will be targeted at 1 mm^2 pixels with as close a spacing as is possible. The spacing will be controlled by the size of associated amplification, edge detection, and data routing circuitry. The human system obviously operates with a much higher receptor density. What is given up in pixel resolution on the one hand is compensated for by an increased image acquisition rate. A high acquisition rate for an object while in a robotic gripper will allow for quick recognition of an object's position, and the detection of slip.

2.3 Objective Summary

The human system will serve as a model to be strived for in the construction of an electromechanical touch sensor device. At all points throughout the design cycle the human system will be looked to as a guideline of system performance to be replicated as closely as is allowed by the design tools at hand.

The following chapter will examine the mathematics of the edge detection procedure, and the communication system required for its execution. A detailed algorithmic analysis will be done to determine the most efficient methods of implementing edge detection and data communication in CMOS VLSI hardware.

CHAPTER 3

DESIGN STRATEGIES

3.1 Computational Alternatives

To carry out the process of edge point detection, three hardware computational strategies were considered. These included: a completely parallel scheme, a mixed parallel / serial scheme, and a completely serial scheme. The routines will be discussed, including advantages and disadvantages of each. The hardware schemes presented are based upon an IC being manufactured that will contain an array of nine individual tactile sensor pixels. The major design criterion was to efficiently detect and transmit edge point data on the three by three array of pixels. The IC will then serve as a building block for a larger tactile array which will maintain a minimum number of connections, yet still achieve efficient edge detection and data transmission. Each hardware routine presented will focus on a four-point edge point detection algorithm. Every point in the large array will compare pressure input data with its four nearest neighbors (North, South, East, West) to determine if it represents an edge point.

3.1.1 Four-Point Edge Point Detection

The location of sensor sites will be defined in a Cartesian X - Y coordinate system. Input information

concerning the shape and position of an object will be obtained through these points. If an object is located over a point and exerts sufficient pressure, a digital 1 will be recorded at this point indicating the object's presence. Conversely, if the object misses a point, or if there is insufficient pressure, a digital 0 will record the absence of the object at that point. Since the digital representation of the outline of an object is available in a two dimensional parallel array, edge detection will most accurately be achieved locally. In all hardware schemes considered, the data is inherently present in an X - Y array, so it will be efficient to determine the edge points prior to any manipulation or transmission of the data.

In a M. Sc. thesis by L. Luang Hong [1], three edge detection schemes were investigated. These included an eight-point scheme and a four-point scheme, both on a rectangular grid system, and a six-point scheme based on a triangular grid. The four point scheme being the simplest was also unexpectedly the most accurate in determining the best fit for the outline of an arbitrary object.

The essential condition for a point to be an edge point is that it must have a 1 as its input. Any point with an input value of 1 on the periphery of the sensing array is automatically an edge point. In the interior of the array a point is considered to be an edge point if it has an input

value of 1 and at least one of the four neighboring points has an input value of 0.

In the comparison between the three edge point schemes, two factors determined the efficiency of each scheme. The primary criterion was the best fit between the actual object outline and the outline determined from edge point detection. The other major consideration was the speed of data transmission. If a similar outline could be determined with fewer actual edge points, the amount of data to be transmitted would be reduced. An outline with the least number of points would be most desirable. The four-point edge detection scheme yielded the best outline fit with the fewest number of actual edge points in comparison to the other two that were investigated. The aforementioned investigation led to the four-point routine to be used in all hardware implementations of edge detection.

From a hardware point of view, a simple circuit must be created to determine the existence of an edge point. In the parallel methods of edge detection all points are tested simultaneously, though only points with an input value of 1 require testing. For each point with a 1 value, the data from the North, South, East, and West (N,S,E,W) points are required in the edge point determination. See Fig. 3.1. For a point of concern (C) with a value 1, two cases can occur. Firstly, all four neighbors could have a value 1, which would result in point (C) being classified as an

interior point. Secondly, one or more of the neighboring points could have a value 0, which would result in point (C) being classified as an edge point. A special case of the second classification occurs when all neighboring points have 0 value which would lead to the point being identified as isolated. A simple logic equation describes the edge point determination circuit.

$$\text{Result} = (\overline{N} + \overline{S} + \overline{W} + \overline{E}) \cdot C$$

If Result has a 0 value the point is either an interior point, or it has an input value 0. If Result is 1, the point is an edge point or possibly an isolated point, and its location must be noted. The comparative logic circuit can be implemented using a 4-input Nand gate and a 2-input And gate.

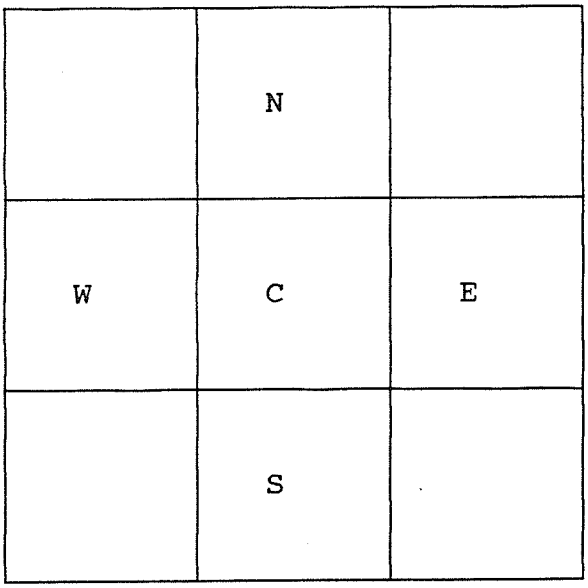


Figure 3.1. Nine Pixel Array Showing the Pixels Involved in the Edge Point Calculation.

3.1.2 Completely Parallel Edge Detection

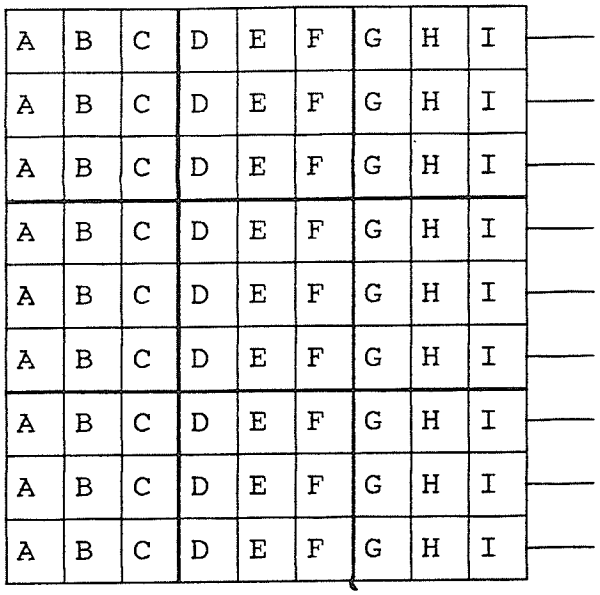
The fastest of all routines to be examined will be parallel edge point detection followed by parallel data transmission. To obtain the high throughput rate available with this scheme, a large number of connections are required. Internal to the sensor, each pixel must communicate with its four nearest neighbors. These pixels are located at intersecting lines in a grid-like communication system. Once edge data is determined, a data line is required for each row of pixels in the sensor. As resolution or size of the sensor array increases, the number of external lines would soon become unmanageable.

For the edge detection to be performed in parallel, each tactile pixel must have the capability of transmitting, and also retaining its input information. To meet this requirement each pixel must have a nonvolatile memory cell or latch. Each pixel must make available its input information to the four nearest neighbors and accept input information from its four nearest neighbors. The edge point determination is carried out in the two-gate logic circuit. The new edge data would replace the input tactile information in memory at that pixel. After this procedure the array will contain an outline of the object that exerted pressure on the sensors.

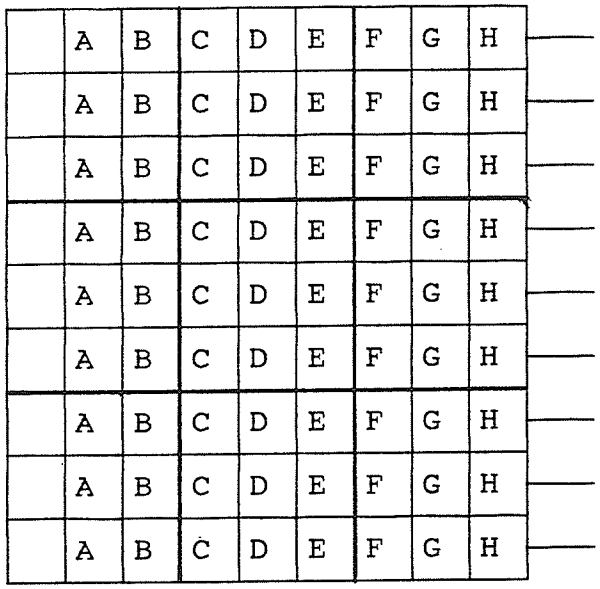
For the fastest realizable means of removing the

outline determined from the sensor, a parallel shift routine is applied. Data lines would be connected along one complete edge of the array. See Fig. 3.2. One data line is required for each row of pixels. The data could be shifted off the sensor in a number of clock cycles equal to the number of pixels in one dimension of the sensor. For example, if a large array was created using a grid of three-by-three ICs, in which each IC has a three-by-three pixel array, then 9 data lines would be required. The data could be shifted off the large array in 9 clock cycles. The information would be contained in a (9 x 9), 81 bit block of data.

The main problem with shifting all the data in this manner is that most of the information is redundant. The important data, the edge points, make up a very small portion of the whole array. If all the data is collected and transmitted, a waste of transmission bandwidth will occur. Some form of data compression, or logical filtering is required to only track the edge point locations. This consideration will be addressed in the following hardware routine proposals.



(a) - Alphabetic characters represent binary edge data.
- One data line is required for the transmission of each row of pixels in the sensory array.



(b) - Data is shifted out of the sensory array in a column by column manner.
- In this example, data would be completely scanned in nine clock cycles.

Figure. 3.2. Fully Parallel Data Scanning.

3.1.3 Mixed Parallel / Serial Edge Detection

A medium speed edge detection routine involves a combination of parallel and serial processes in determining and transmitting edge point data. The hardware layout of the scheme consists of a simple input sensor array in conjunction with a medium complexity edge point sequencer.

The input sensor array could be constructed with fewer communication lines because each pixel need only transmit to its nearest right side neighbor. The planned sensor structure allows for individual ICs to be constructed with nine active pixels. Due to the simple implementation of this design, higher resolution is a possibility with either sixteen or twenty-five pixels per input IC. As all data manipulation is performed in the associated processor, upper and lower connections between pixels are not required. This fact facilitates simple creation of large sensors due to the small number of connections that are required. Connections are required to the edge point sequencer, which involves one data line per row of pixels in the input sensor array. See Figs. 3.3 a - f. This number of communication lines does not present a great problem, because these connections can be made at the same time that the sensor array is constructed from individual ICs.

The edge point sequencer consists of three columns of shift register latches plus associated circuitry. The

columns are electrically as tall as the input sensor array plus an additional row of latches along the top and bottom. The additional rows are required to handle vertical shift overflow from the edge point processor. The processor must have the ability of operating under simple software control. Once the edge point routine for the array has been initialized, the processor operation will be controlled by a repetitive hardware sequencer. In development, one nine pixel shift register processor and the associated communication control would be created in hardware. The processors would then stack vertically with vertical connections, to accommodate any size sensor array. The center register of the nine-pixel processor will always contain the point being tested for the occurrence of an edge point. Through a sequence of horizontal and vertical data shuffling, each pixel from the input array will in turn become the point of concern. The shift register latches must be controllable to shift vertically and horizontally according to the sequencer instructions. Figures 3.3 a - f illustrate the mixed parallel / serial data manipulation.

After the input array has sampled an object and input pressure data has been latched, the sequencer can begin to extract the edge points. The processor column registers must be initialized to zero values. The sequence which examines all points and transmits edge point locations proceeds as follows;

Figure 3.3 b.

- begin by shifting two columns from the input array into the processing columns; this primes the processor to examine the rightmost column of the input array.
- determine if the points of concern (the center points of the nine register processing elements) contain a value of one.
- if a value of one is found at any of the points of concern, perform the edge point routine via the previously described logic circuit for that group of nine cells.
- if any of the examined points of concern are edge points, transmit or store their locations.
- the location of the edge point is determined according to the vertical position of the processing element, and number and direction of shifts that have been performed.
- the location of an edge point is transmitted or stored by sending the determined location data value.

Figure 3.3 c.

- shift the processing columns up one row; this places into the points of concern the pixels below the previously examined points.
- determine if the points of concern contain a value of one.
- if a value of one is found, perform the edge point

routine for that group of nine cells.

- if any of the examined points are edge points, transmit or store their locations.

Figure 3.3 d.

- shift the processing columns down two rows; this places into the point of concern the pixels above the points first examined.
- determine if the points of concern contain a value of one.
- if a value of one is found, perform the edge point routine for that group of nine cells.
- if any of the examined points are edge points, transmit or store their locations.

Figure 3.3 e.

- shift the processing columns up one row to restore input data to the original position as in Fig. 3.3 b to ready the processor columns for the next right shift from the input array.

Figure 3.3 f.

- shift to the right from the sensor array one column, into the processing columns, this allows the next column from the input array to be examined.

The above routine is repeated until all columns have been examined for edge points, and the edge point data has been transmitted or stored. The routine, in effect, performs column by column sifting of the edge points from the sensor array.

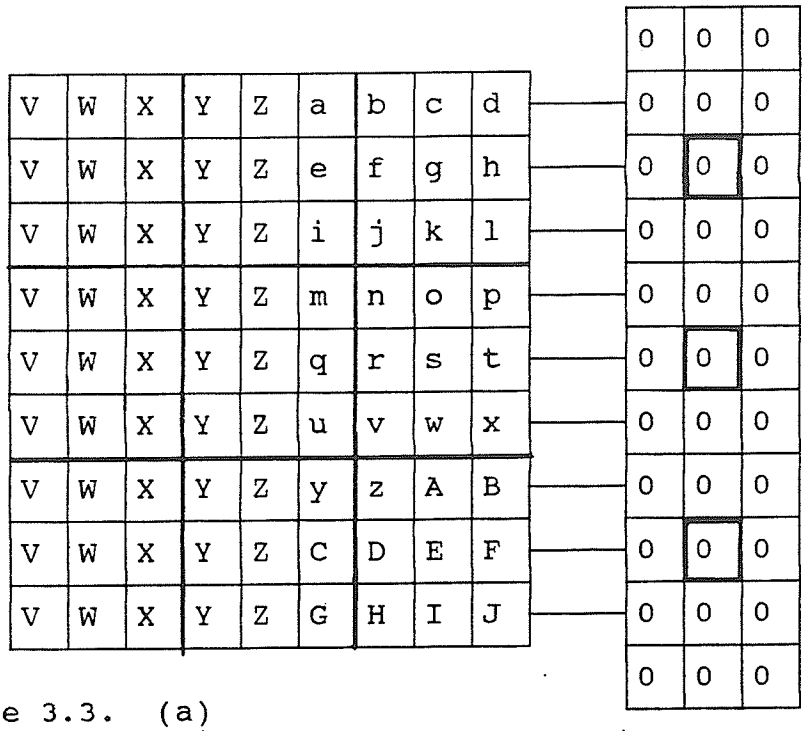


Figure 3.3. (a)
- Alphabetic characters represent raw pressure data.
- The diagram shows the data structure at the start of the edge point determination process.

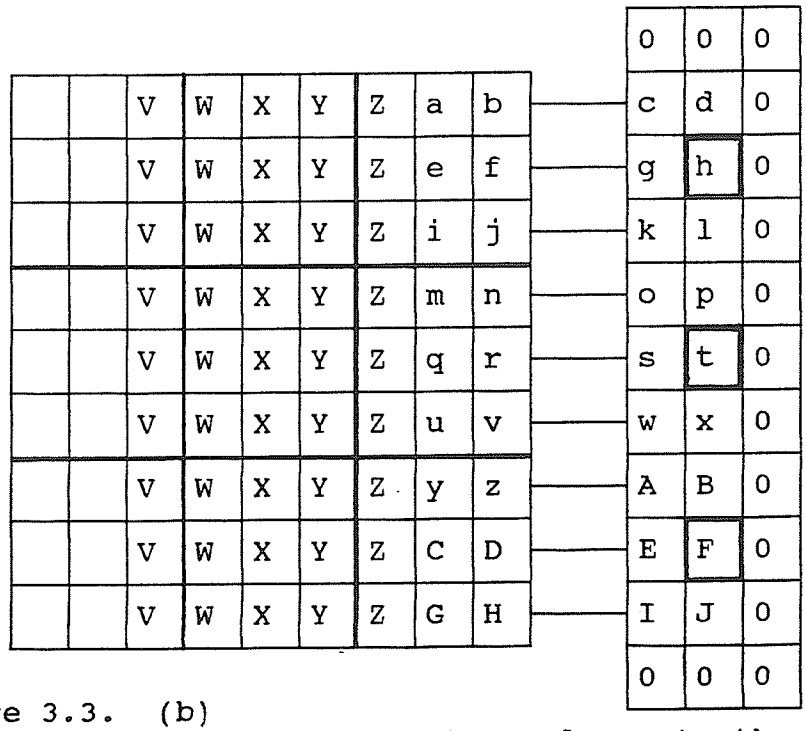


Figure 3.3. (b)
- Shift the array data two columns to the right.
- Determine if pixels h, t, or F are edge points.
- Store the location of any edge points found, in a scratch pad memory.

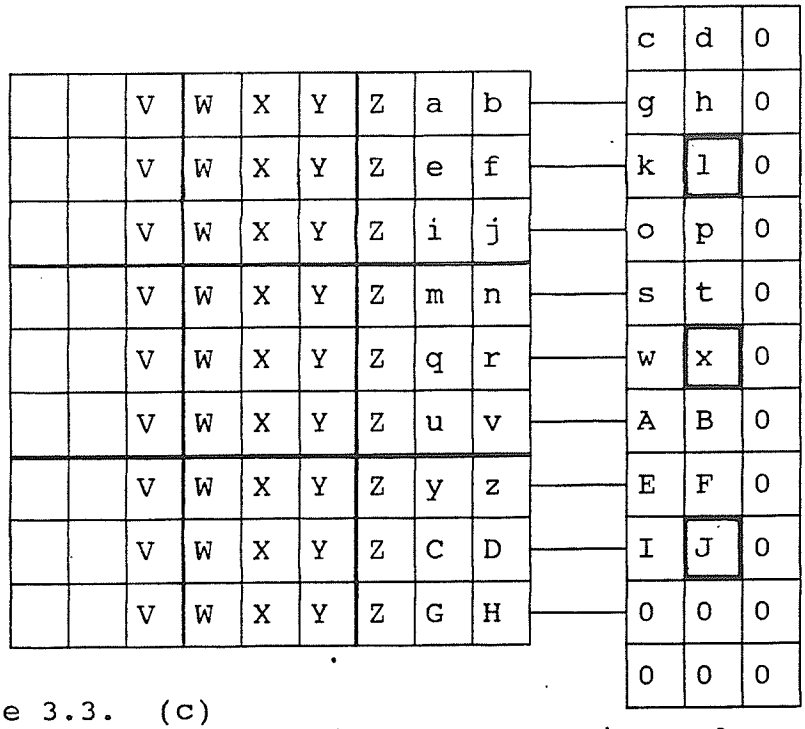


Figure 3.3. (c)
- Shift the data in the processing columns up one row.
- Determine if pixels l, x, or J are edge points.
- Store the location of any edge points found, in a scratch pad memory.

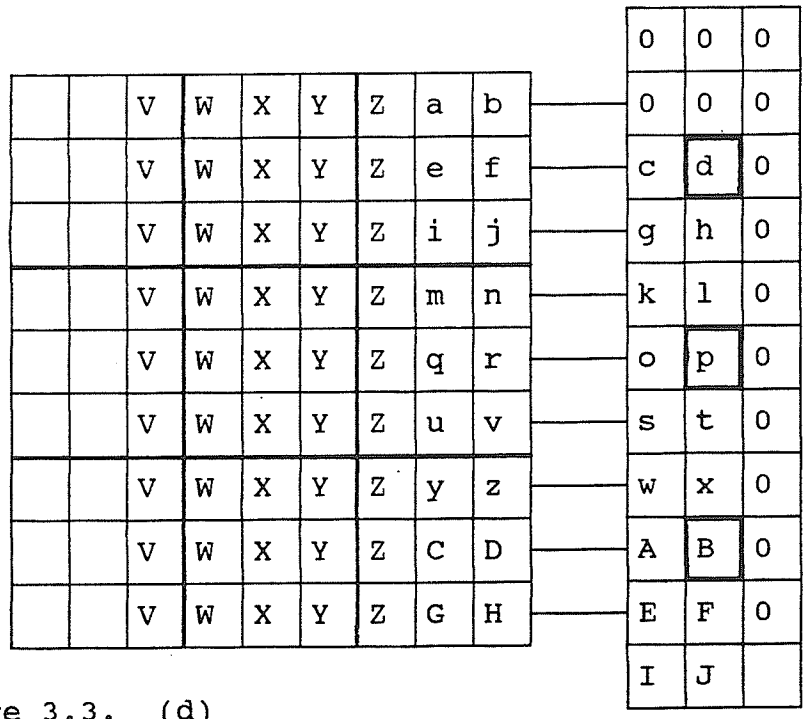


Figure 3.3. (d)
- Shift the processing column data down two rows.
- Determine if pixels d, p, or B are edge points.
- Store the location of any edge points found, in a scratch pad memory.

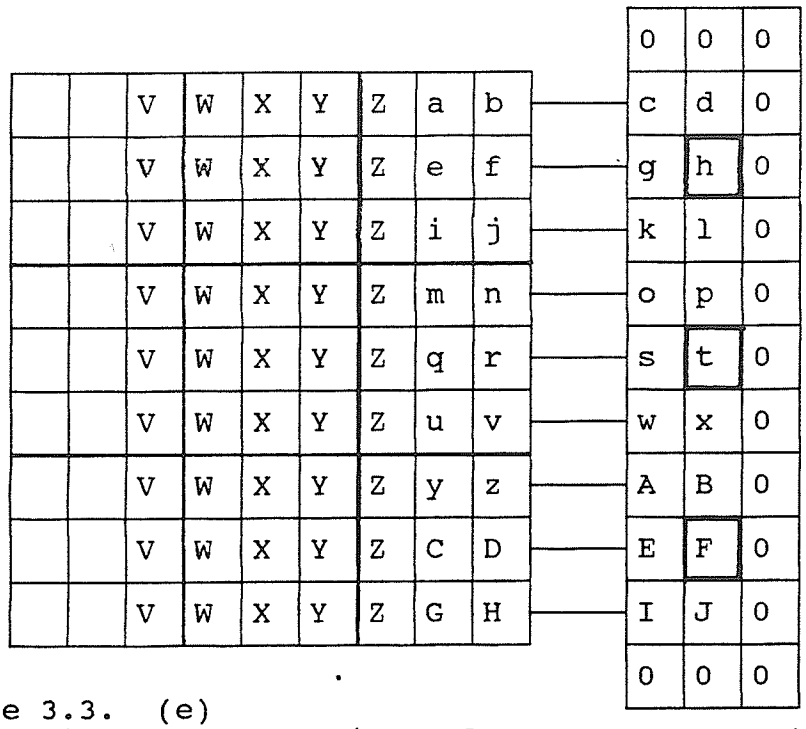


Figure 3.3. (e)
- Shift the processing columns up one row to restore the processing array to the state of Fig. 3.3 b prior to a right shift of raw data from the pressure array.

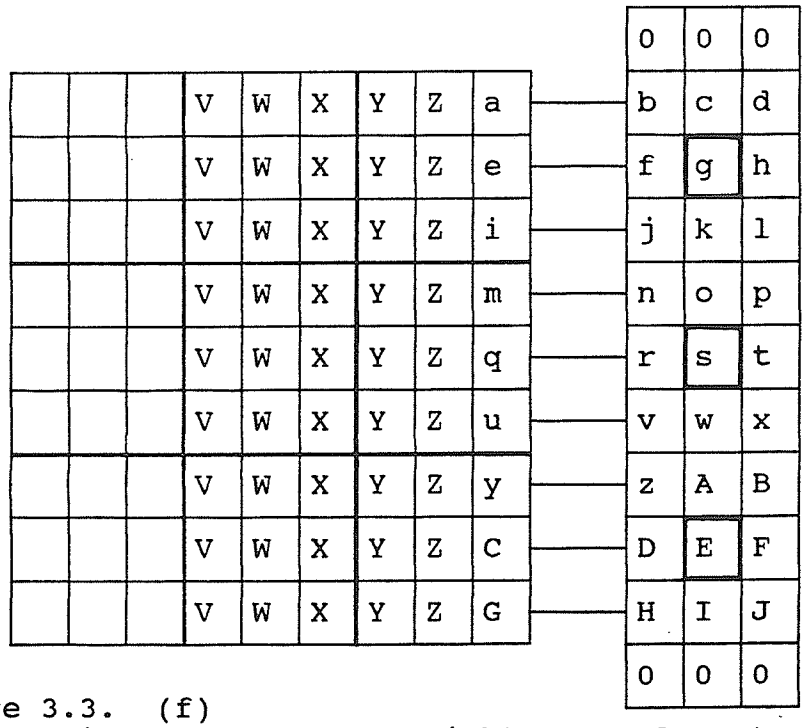


Figure 3.3. (f)
- Shift pressure data right one column to reinitialize the edge point determination process.
- Determine if pixels g, s, or E are edge points.
- Store the location of any found edge points in a scratch pad memory.

Figure 3.3. Mixed Parallel / Serial Data Manipulation

In using the partially parallel, partially serial edge determination, a great manufacturing advantage is realized in the construction of the input sensor array due to the simplicity of the interconnections. All the area of the input array can be optimized to perform high resolution pressure transduction and amplification, without any area used for additional computational or routing circuitry. All of the complex VLSI design will be confined to the processing columns. These columns would be physically small in comparison to the input array because the sensor pad area is not required. The small size of the processing columns would allow them to be placed alongside the input array when constructed. The simplicity of the input array allows the mixed parallel / serial scheme to adapt to increased tactile resolution more easily than the fully parallel design. The input pixel size could shrink to the size of the required amplification and local memory circuitry, thus creating an input array having a much finer resolution. The advantage that this design shares with the fully parallel design is that the edge point data is stripped off the input array column by column. Data in this format can be used in parallel by another processor for the purposes of pattern recognition and determination of an object's spatial orientation.

A disadvantage of this design is that it is slow in comparison to the parallel edge point determination. The connections required between the input array and the

processing columns create an additional task in the construction of this design. The processing columns must be located next to the sensor array because running a large number of lines to a remote location would be impractical. The complete processor input array plus edge point processor would require external software control to operate. This makes the system much less stand-alone and independent in comparison to the fully parallel processor.

3.1.4 Completely Serial Edge Detection (Cellular Automata)

The serial edge detection processor takes advantage of the Cellular Automaton structure in determining an edge point and its location. The input sensor array is similar in construction to the mixed parallel / serial design. The serial connection structure of the input array makes this design the slowest of the options considered. The array is connected in a manner which will allow scanning in a left to right, top to bottom raster fashion. This requires horizontal interconnection of each pixel in each row, plus vertical connections of the leftmost column. Each shift register present in the leftmost column must have the ability to switch between its row and the next row, when scanning of its row is completed. See Figs. 3.4 a - d. In a large sensor this switching action must be controlled externally from the sensor array. Hardware counters programmed with the size of the array would generate the required scanning control signals. Input pressure data is

removed from the array, one pixel at a time, starting at the top left hand corner. Data is scanned in a manner similar to the way a person reads the English printed page.

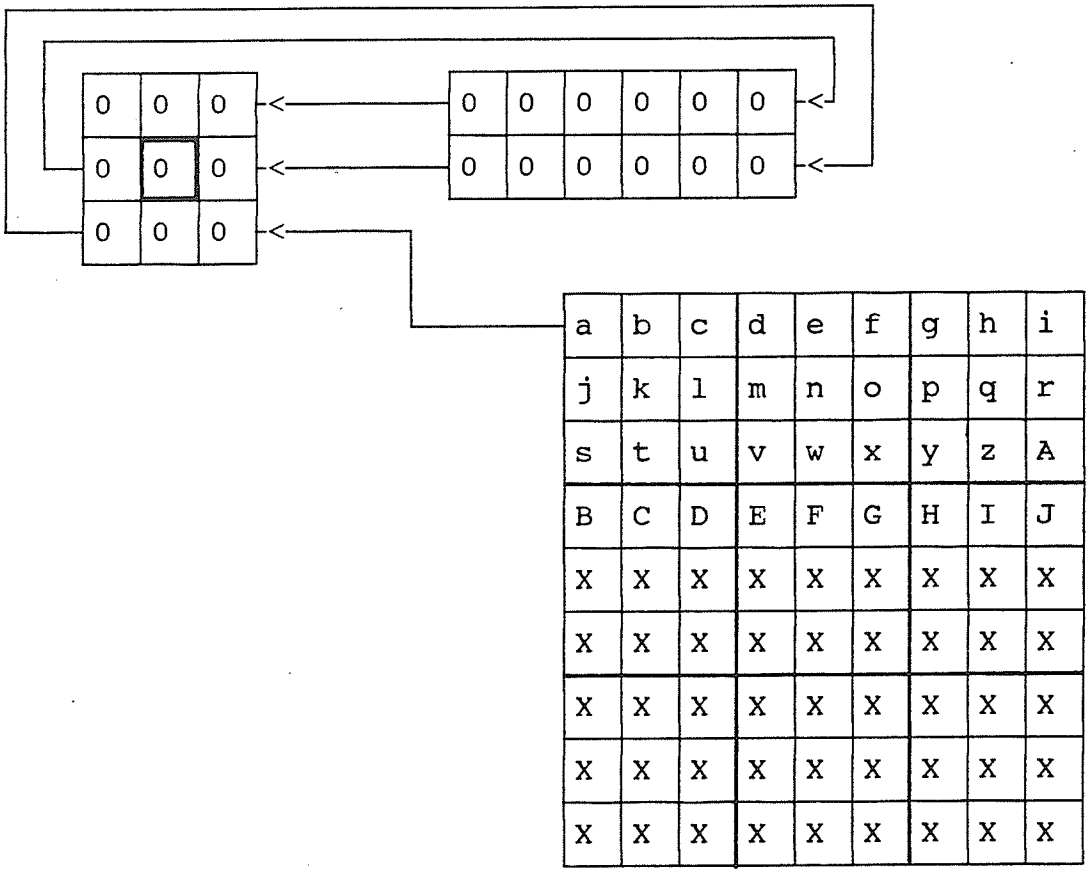


Figure 3.4. (a)
- Alphabetic characters represent raw pressure data.
- The diagram shows the data structure at the initialization of the edge point detection process.

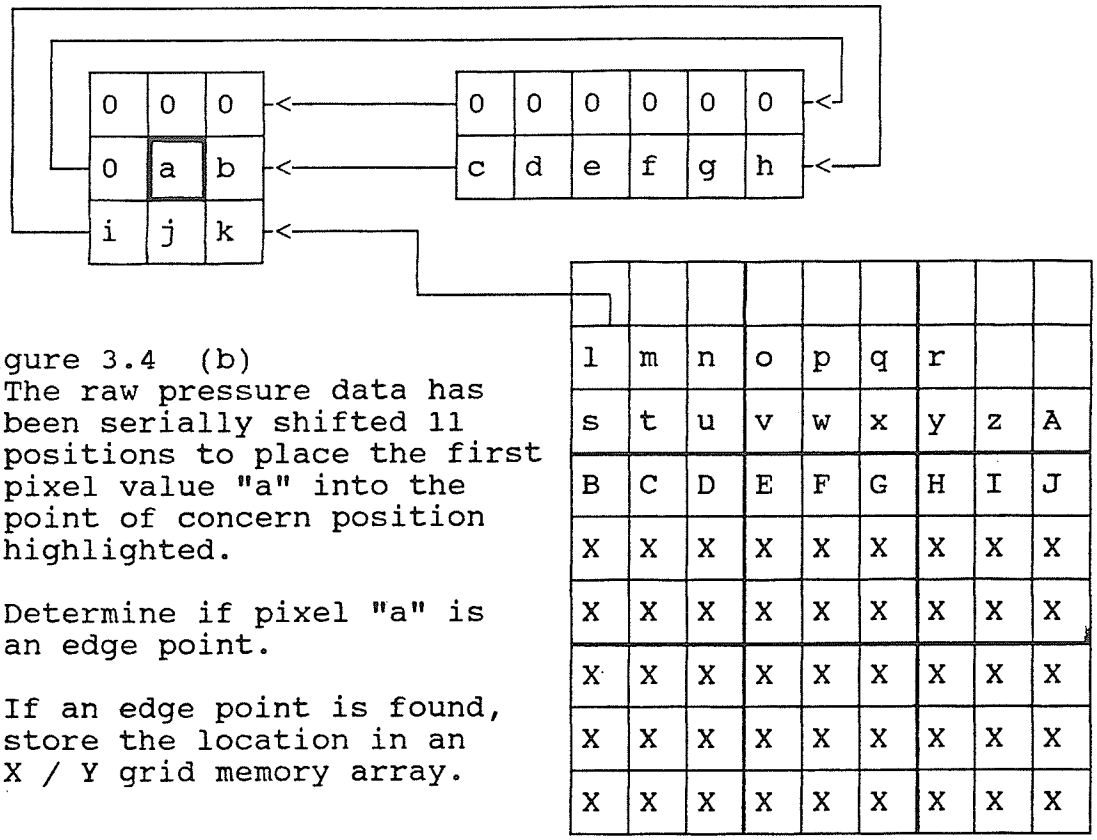


Figure 3.4 (b)
- The raw pressure data has been serially shifted 11 positions to place the first pixel value "a" into the point of concern position highlighted.

- Determine if pixel "a" is an edge point.

- If an edge point is found, store the location in an X / Y grid memory array.

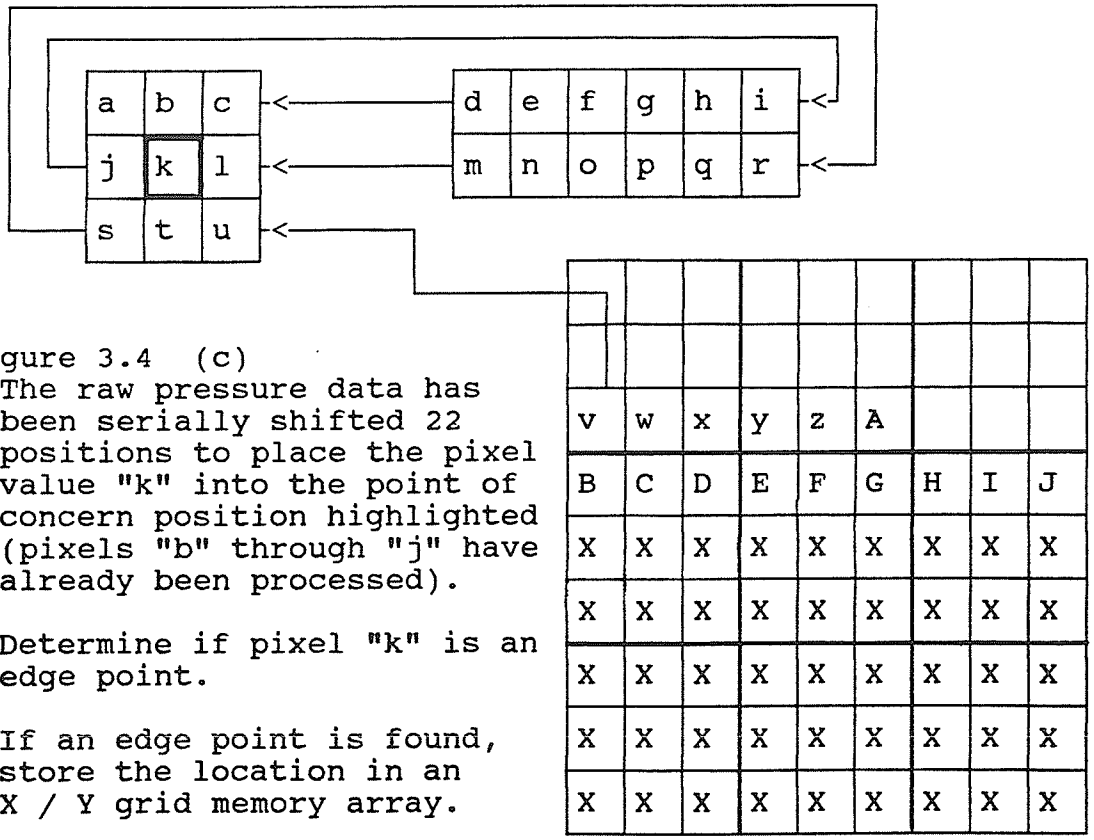


Figure 3.4 (c)
- The raw pressure data has been serially shifted 22 positions to place the pixel value "k" into the point of concern position highlighted (pixels "b" through "j" have already been processed).

- Determine if pixel "k" is an edge point.

- If an edge point is found, store the location in an X / Y grid memory array.

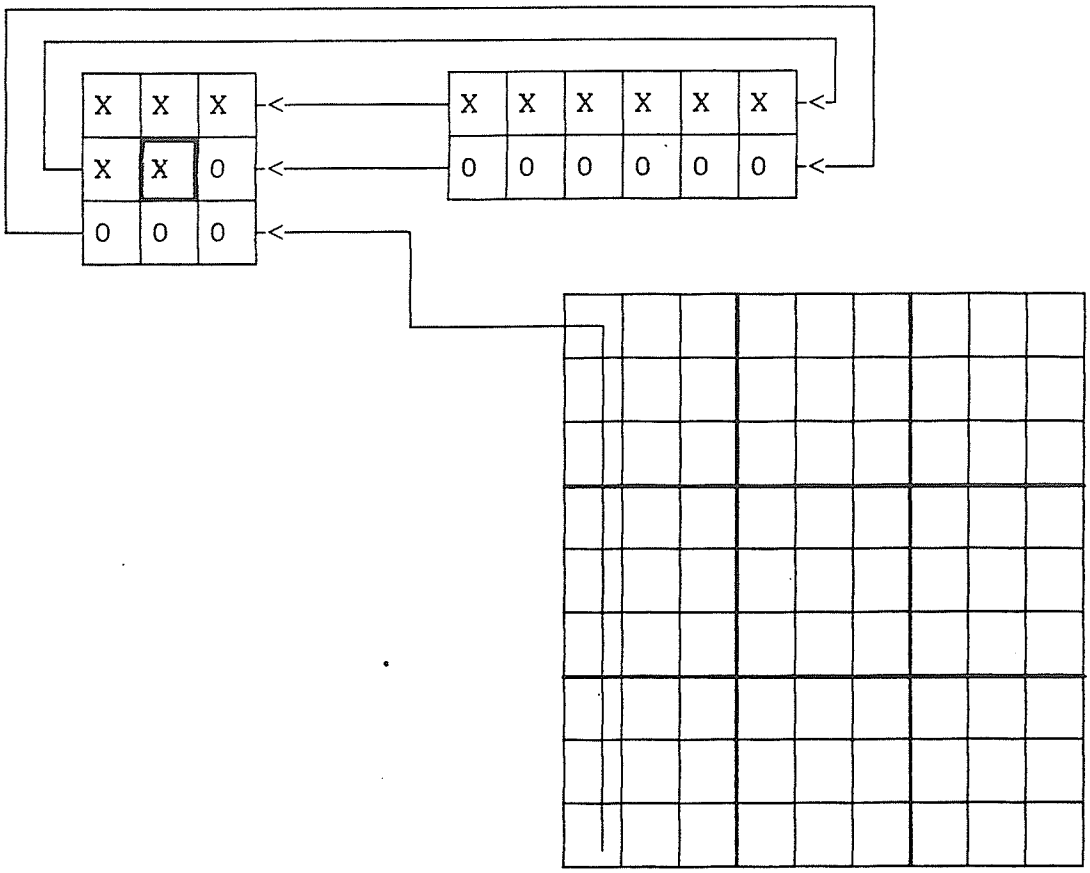


Figure 3.4. (d)
- The raw pressure data has been further serially shifted to place the last pixel value "X" into the point of concern position highlighted.
- Determine if the last pixel "X" is an edge point.
- If an edge point is found, store the location in an X - Y grid memory array.
- Notice that dummy zeroes have been inserted into the system in order to determine the existence of edge points in the bottom row.

Figure 3.4. Serial System Data Manipulation.

The edge detection processor is simple yet elegant. The serial data passes through a Cellular Automaton structure with its associated delay lines. The edge detection processor, equipped with the previously described logic circuit, is configured in a nine register block. The four-point edge detection routine is used. If the input

array contains n x n pixels, the delay lines required will be n - 3 registers in length. When the algorithm begins the processor must be initialized with (n - 3) + 3 + 1 = n + 1 dummy zeroes before edge points may be extracted. Also, at the end of the routine the data will have to be lengthened by (n - 3) + 3 + 1 = n + 1 dummy zeroes to complete the edge point determination. The transmitted location of an edge point will be determined by the number of shifts performed when that edge point has been detected. The values contained in the controlling hardware counters will track the location of a detected edge point.

The serial design maintains the simple input array structure observed in the mixed parallel / serial design. The limited number of connections required makes the array construction an easier task in comparison to the fully parallel scheme. As with the mixed design, pixel resolution could increase, i.e. the pixel size could decrease. The resolution is limited only by the size of the amplifier, logic, and shift register circuitry used which must perform their necessary detection and communication operations.

The one great advantage to the serial edge point processor is that it does not grow in size with increased sensor size or resolution. Once the processor design has been finalized, it will serve any input array constructed. The processor will be small enough to be located physically close to the input array. Due to the fact that only one

data line is required to transmit data from the input array, the processor could be located remotely if that need arises. Similar to the processing columns in the mixed parallel / serial design, the Cellular Automaton processor acts as an edge point filter in extracting edge points from the input sensor array. The edge data is extracted point by point in comparison to the quicker column by column extraction.

Of the designs considered, the serial design is slowest in cataloging the edge point data. In the other two cases, execution time only increases linearly with increased sensor size due to parallel scanning. When scanning serially, processing time increases according to a square law because the two dimensional array is being read one pixel at a time. The input array, despite having a simple interconnection structure, requires two different types of array building blocks in its design; one standard type in common with the mixed design array block, and a second specialized type with a switching shift register for placement on the left side of the array. The edge point data from the serial processor is available only one pixel at a time and may create a computational bottleneck if the image refresh data is required rapidly.

3.2 Computation Alternative Summary

Parallel, mixed parallel / serial, and serial designs have been presented in order of decreasing computational complexity and increasing execution time. Advantages and

disadvantages of each approach have been discussed. Each of the algorithms are based upon the four-point edge point determination routine. All designs used the two-gate logic circuit for the actual edge point calculation.

In the next chapter, features of each strategy are utilized in the finalized design. The chosen design will be presented, along with details concerning the VLSI implementation and considerations of manufacturing useful, practical sized tactile sensors.

CHAPTER 4

INTEGRATED CIRCUIT DESIGN

4.1 Design Procedure

Features of the aforementioned design alternatives are now highlighted and combined into the final design selection. The actual edge point determination strategy and method of pixel data transmission will be discussed in detail. This will be followed with considerations for implementing these routines in hardware. The methods for allowing the finalized pixel design to be used as a building block in a three by three (3 x 3) pixel array will be presented. Included will be the next building block hierarchy considerations, which will allow several nine pixel ICs to be combined in a larger sensor array. The hardware design from initial to final implementation will be discussed. Lastly, adaptation of Kynar film for use with the sensor is presented along with electrical properties of this piezoelectric film.

4.1.1 Selected Design

The edge point processing strategy chosen follows from the practical combination of design alternatives presented in the previous chapter. The raw data from the input pressure array is physically located in a two dimensional parallel array. The processing of the edge point data is efficiently executed in a parallel architecture. Therefore, local processing was chosen to compute the edge points.

A serial shift routine was chosen to transmit the data out of the sensor. The serial shifting routine can always operate at a much higher rate than that of the required mechanical action which creates input pressure data for the sensor. The serial shifting routine is the slowest option of removing the edge data from the array but the routine will operate many times faster than the mechanical response of the Kynar piezoelectric film. Therefore, the serial shifting routine will never cause a timing bottleneck in this method of data scanning. One output line will be required to transmit the data. This will keep the number of connections to the array to a minimum, regardless of its size.

The edge point determination follows the theory presented in the previous chapter. Each pixel must communicate with its four nearest neighbors. This communication is in the form of a two way information exchange. The pixel of concern is responsible for presenting its data to each of the four nearest neighbors and also to the local edge point logic circuit. This requires that each pixel must have the drive capability to five AND-gate inputs. The edge point calculation routine takes place as shown in Fig. 4.1;

- The process is initiated when the sampling clock (S_Clk) begins toggling the local one bit latch just after the application of mechanical pressure.

- A short duration sampling period is allowed for pressure data to charge the input pixel thus minimizing pressure detection error.
- The charge on the input pixel is isolated from the digital system by a two-stage biased inverter amplifier.
- The charge from the metal sensor pad is fed to the amplifier and results in a digital 1 or 0 being captured into the local one-bit latch indicating pressure or absence of pressure at that pixel, respectively.
- The sample period is terminated when the sampling clock stops toggling the latch.
- The output of each latch is then connected via a transmission gate, under control of Clk_2, to the local, and each nearest neighbor's edge point logic circuit.
- The local logic circuit determines whether the local pixel is an edge point.
- Once the pressure data has been presented to the edge point logic circuitry, the resultant edge point data is held on the output of the 2-input AND-gate.
- The edge data is then connected to the parallel load, serial shift, shift register via a transmission gate, under the control of Clk_1, Clk_3, and p/s_con to facilitate parallel data loading.

- Once edge data has been loaded, the network of serial shift registers, shown in Fig. 4.6 handles the edge point data transmission out of the sensor by toggling Clk_3.
- An off-sensor receiver scans the stream of edge point data looking for data with a logical 1 value which signals the location of an edge point.
- Upon detection of an edge point, the receiver stores the corresponding X - Y coordinates of that point.
- The edge point image is assembled, and then the process is reinitialized.

4.2 Implementation

4.2.1 Input Sensor Pad

The input sensor pad functions as the collector of charge generated when the piezoelectric film is compressed. The input sensor pad is a 990 μm x 990 μm square metal area. In the single-pixel design the sensor pad is physically located in the center of the circuit. In the nine-pixel final design, nine individual sensor pads report to their local amplification and logic circuitry.

Consideration must be paid to the protective overglass layer placed over the silicon chip in the manufacturing process. This layer guards against contamination from the

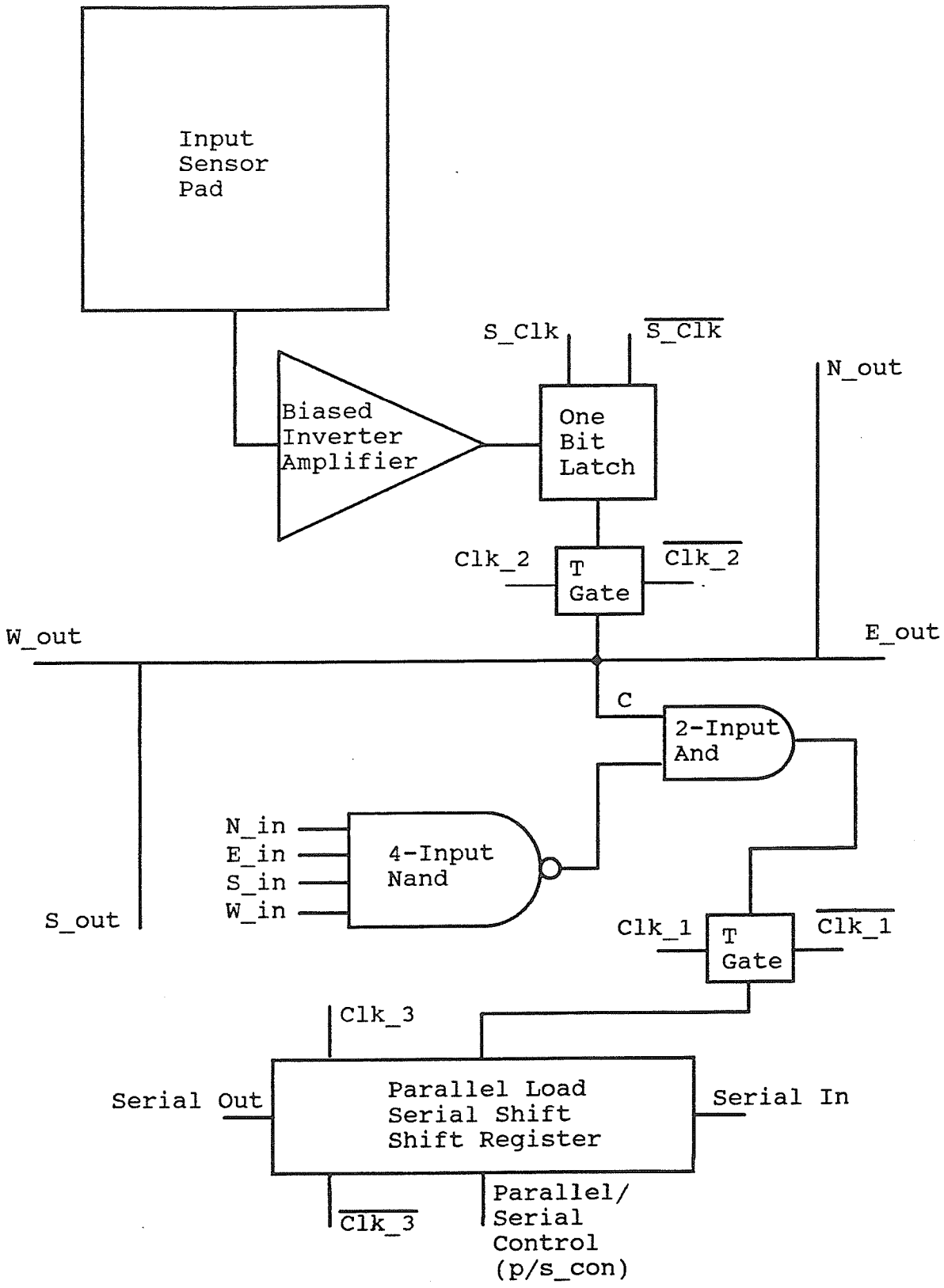


Figure 4.1. Single Pixel Tactile Sensor Schematic

environment. The input sensor pads will require that the protective overglass layer be removed to expose the metal area, and allow contact with the Kynar piezoelectric film, either directly or through a mechanical isolation system.

The overglass layer was specified to be removed from the sensor pads with a small overlapping area to conform to the design rules of the IC manufacturer. The overlap area required is 20 μm. wide on each side of the pad. This leaves an effective square metal contact region with sides of (1000 μm - 2 x 20 μm) = 960 μm. This is the finalized size of the sensor pad and must be considered when designing the Kynar film metal pad etching, or the probe size used in a mechanical pressure isolation system.

4.2.2 Biased Inverter Amplifier

The biased inverter amplifier is implemented in this circuit due to its relative ease of design in comparison to the design time required to construct a CMOS operational amplifier. A CMOS op-amp standard cell was not available at design time. Op-amp gain performance would have been superior compared to that of the biased inverter, but would

have used substantially more circuit area. The biased inverter had to be designed in a short and wide structure to fit below the sensor pad. This made effective use of circuit area and allowed the complete sensor structure to maintain an almost square shape.

The biased inverter input is designed to be held to a voltage which keeps the output in the 0 logic state. This input voltage value is just slightly below the trigger point which would render a logic 1 at the output of the amplifier. The sensor pad and the positive side of the Kynar film, are held at this same voltage. As the Kynar is compressed it adds a small pulsed voltage to the input of the biased inverter which triggers a logic 1 at the output.

The amplifier is constructed in two stages due to the inverting properties of each stage. This allowed the biasing of the amplifier to occur on the first stage, while the second stage corrected for the inverting nature of the circuit. The second stage also provides intermediate buffering between the high gain first stage and the one bit latch which must temporarily store the value detected on the sensor pad. The second stage of the amplifier provides unity gain. See Fig. 4.2 for a schematic representation of the amplifier design.

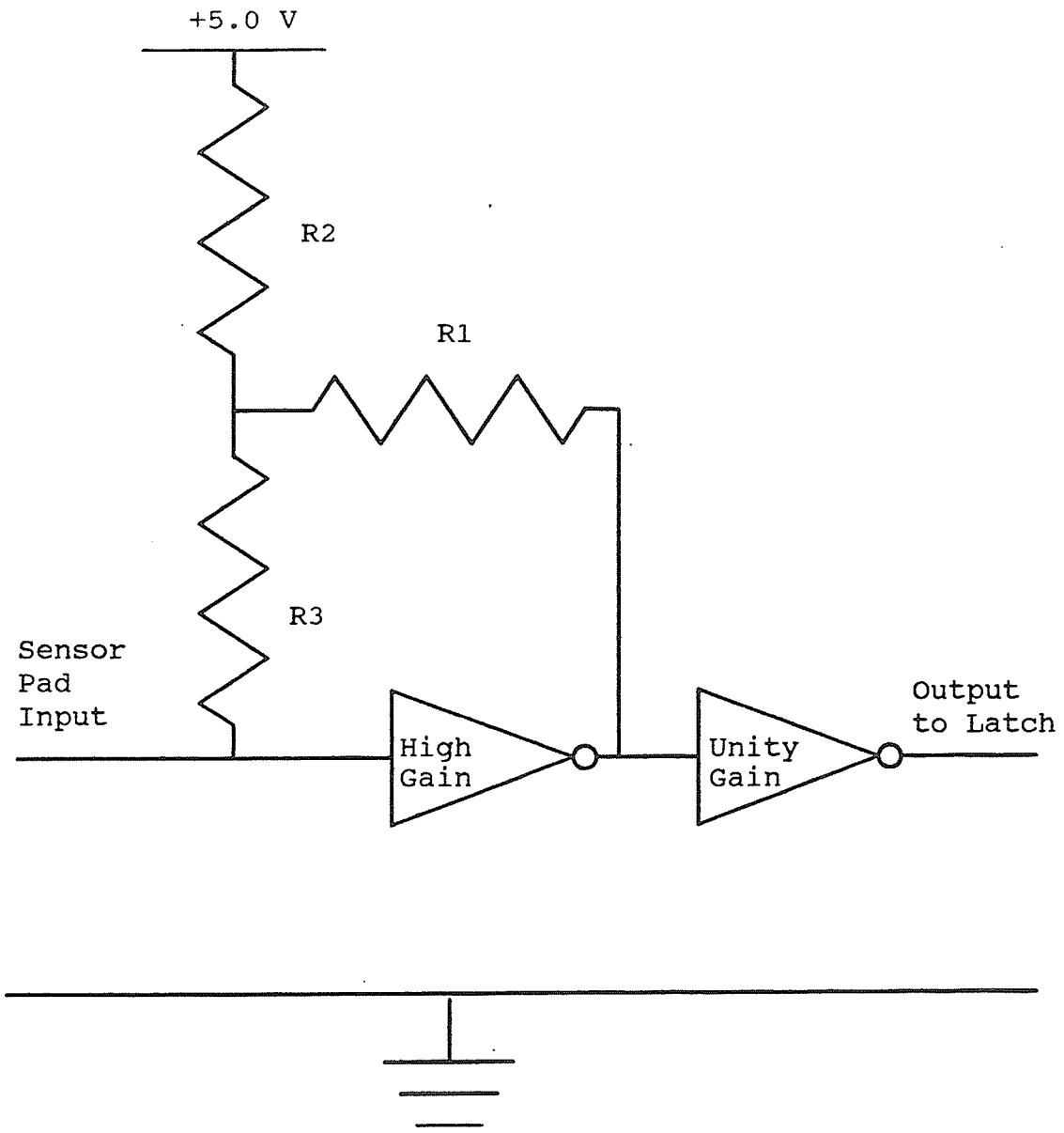


Figure 4.2. Biased Inverter Amplifier Schematic

The biased inverter amplifier went through two design iterations. The preliminary design achieved working performance as was proven through SPICE simulation. After placement of the amplifier in the complete pixel design, the observation was made that a substantial amount of circuit area remained unused. At this time it was decided that all resistors could be made physically larger, thus increasing their resistive values. Since the bias point of the amplifier depended upon the ratios of resistor values and not the values themselves, it was seen that larger resistors had less dependence upon manufacturing variances. Thus the larger resistor values ensured that the amplifier would be biased to the design value of 2.6 volts.

4.2.3 One Bit Latch

The latch holds the logic 1 or 0 which ripples out of the biased inverter under the control of the sampling clock (S_Clk). The one bit latch serves as short term memory for the input data value which will be presented to the edge detection logic. Data is clocked out of the latch to the edge detection logic via a transmission gate. The latch acts to debounce the switching action of the Kynar film, metal pad, biased inverter amplifier system. The noninverting latch is connected to the input of a transmission gate.

4.2.4 Transmission Gate Usage

The internal timing of the edge detection processor is regulated by transmission gates. The gate between the one bit latch and the edge point logic is controlled by Clock 2 (Clk_2). Clock 2, on a low to high transition, universally signals for stable pressure data to be passed from the latch to the edge logic for processing. The resultant data from each edge logic circuit is present on the input of the second transmission gate. This gate is located between the edge logic and the parallel load port of the shift register. It is controlled by Clock 1 (Clk_1). Clock 1, on a low to high transition, universally signals for all edge data to be loaded in parallel into the shift registers.

This type of data flow regulated by transmission gates simplified the design of the edge detection logic. Due to the fact that direct clocking of the logic was not required, the circuit was constructed using only static logic gates.

4.2.5 Edge Point Logic

As previously discussed, the determination of an edge point involves information from the point of concern and its four nearest neighbors. This operation occurs for all pixels in the sensor in parallel. The logic equation to be evaluated is as follows;

$$\text{Result} = (\overline{N} + \overline{S} + \overline{W} + \overline{E}) \cdot C \ .$$

The result of the equation has five distinct cases to be interpreted. The cases are highlighted in Table 4.1 below. Only cases 4 and 5 indicate that an edge point has been detected. If the local data is 1 and one, two, or three of the neighbours are 0, an edge point is determined.

Table 4.1. Logic Circuit Output States

Case	Neighbor Data				Local Data	Output Data
#	North	South	East	West	C	Result
1.	1	1	1	1	0	0
2.	1	1	1	1	1	0
3.	0	1	1	1	0	0
4.	0	1	1	1	1	1
5.	0	0	0	0	1	1

- Case 1 is an example of an Isolated non-pressure point.
- Case 2 is an example of an Interior point.
- Case 3 is an example of a General non-pressure point.
- Case 4 is an example of an Edge point.
- Case 5 is an example of an Isolated Edge point.

The equation can be implemented by a 4-input Nand-gate and a 2-input And-gate. The 4-input Nand-gate accepts input from the four nearest neighbors. The result from the

Nand-gate serves as one input to the 2-input And-gate. The other input to the And gate comes from the local pixel latch. The output of the And gate will only signal that an edge point has occurred if the local pixel contains a value 1. The result of the complete logic circuit determines the occurrence or nonoccurrence of an edge point at that local pixel.

Raw pixel data is presented to all five inputs of the logic circuit at the same time. The result simply ripples through the circuit in the period of three gate delays. The result is held on the output of the 2-input And gate until a transmission gate passes the edge data to the local parallel load / serial shift register.

4.2.6 Parallel Load / Serial Shift Register

The specialized shift register network handles all the edge point data routing. Once the edge data result has been determined by the logic circuit, this data can be presented to the parallel load port of the shift register via a transmission gate. The register loading is controlled by an input line (p/s_con) which instructs the register to accept data locally in parallel, or from a neighboring shift register to allow edge data clocking out of the sensor. When the p/s_con line is in the 0 state, the register is in the parallel load mode of operation. When the p/s_con line is in the 1 state, the register is in the serial shift mode.

The p/s_con line is normally in the high state and goes low only to facilitate parallel loading.

After Clock 1 changes from a low to high state, which opens the transmission gate between the edge point logic and the parallel load port of the shift register, parallel loading can occur. The p/s_con line goes low, and Clock 3 (Clk_3) toggles which signals universal parallel loading of all shift registers. The serially connected shift registers now contain all the edge point data.

Clock 1 now changes from a high to low state, which closes the transmission gate. During the same clock period the p/s_con line returns to the high state which enables the shift registers to begin the serial shifting routine. Clock 3 now universally toggles the network of shift registers to serially transmit the data out of the sensor.

The parallel load / serial shift register is constructed from a standard CMOS shift register cell. The front end of the shift register was modified to facilitate the parallel loading mode of operation. Extra circuitry was added to enable the shift register to be controlled by both Clock 3 and the p/s_con input lines. The serial load port was part of the standard cell design. The parallel load port was added. The standard cell noninverting output line is used.

4.2.7 Power and Ground Considerations

Highly redundant power and grounding has been a design consideration from the beginning of the design process. Each individual pixel has power and ground ports at the top left side, the left top side, the top right side, and the left bottom side. See Fig. 4.3. In the case of a power or ground connection failure during individual IC manufacture, each pixel has three redundant paths to obtain the required operating voltage.

In the 3 x 3 pixel implementation again four power and ground ports are implemented to provide universal sensor powering to all building blocks. This construction scheme allows surround style mesh powering in case of single or multiple faults in the power and ground connections. The mesh system would allow all separate sensor blocks to still receive power in the event of a fault. This redundant powering would virtually eliminate dead sensor areas in a real world sized sensor array. In Fig. 4.4, power and ground connections made to the 3 x 3 sensor array are in similar locations as those made to each individual pixel.

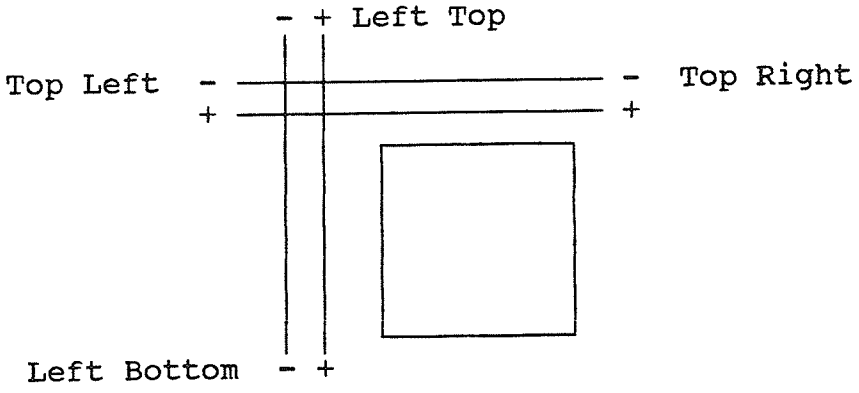


Figure 4.3. Single Pixel Power and Ground Ports.

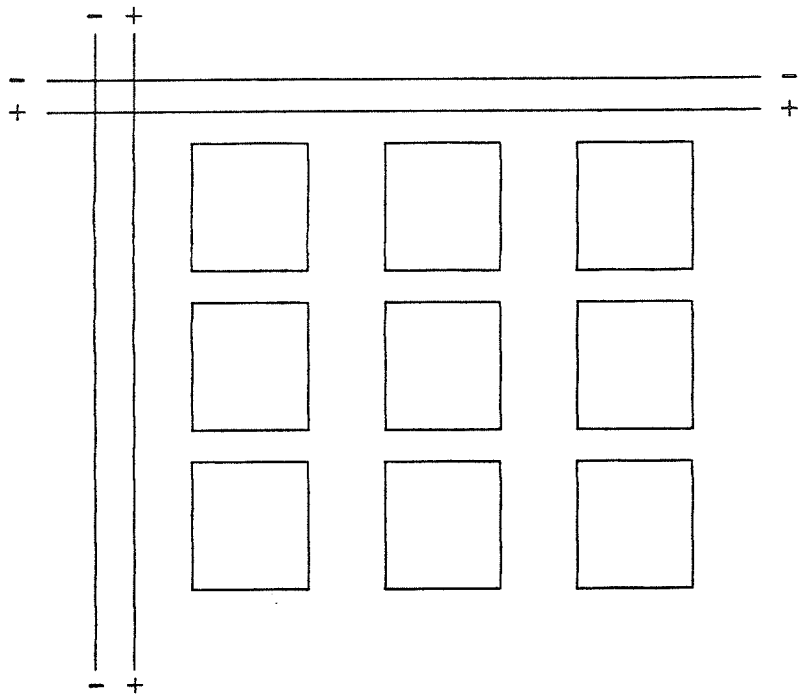


Figure 4.4. 3 x 3 Pixel IC Power and Ground Ports.

4.2.8 Clock and Timing Considerations

Four independent clock lines control the operation of the sensor and the associated edge detection logic. These are as follows;

S_Clk — The sampling clock operates on the one bit latch and controls the timing of incoming pressure data form the metal pad and amplifier system.

Clk_1 — Clock 1 operates on a transmission gate and controls the loading of processed edge data into the parallel load / serial shift register.

Clk_2 Clock 2 operates on a transmission gate and controls the loading of pressure data from the one bit latch to the edge detection logic of the local and four nearest neighbor pixels.

Clk_3 Clock 3 operates on the parallel load / serial shift register and controls the parallel loading of edge data into the shift register and the serial shifting of edge data out of the sensor array.

One control line, the parallel / serial control (p/s_con), signals the mode of operation of the shift registers. The two possible modes are the parallel load mode, and the serial shift mode.

An external clock and control signal sequencer generates the required clock and control signals. The frequency of operation of the sensor is controlled by this external signal generator. The drive capability of the sequencer will be designed to accommodate the load presented by the size of array used.

The timing diagram shown in Fig. 4.4 illustrates the sequence and timing of the sensor operation.

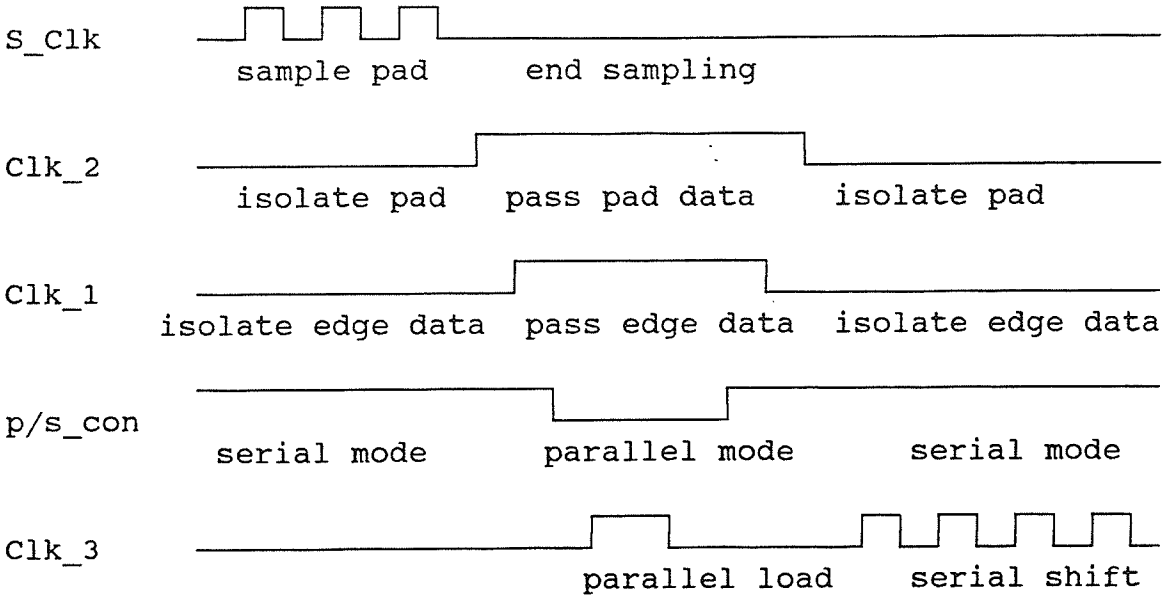


Figure 4.5. Tactile Sensor Timing Diagram.

4.2.9 Data Routing

Edge point data is resolved in parallel by each local pixel. The determined edge data is then loaded to shift registers in parallel to begin the serial shifting routine. In the nine pixel test IC the serial shift pattern occurs as shown in Fig. 4.6. For larger arrays to be built from 3 x 3 pixel ICs, several shift pattern structures would be required for the different positions that sensor building blocks would be placed in the array. These different shift pattern structures are shown in Fig. 4.7. The larger array shift pattern will be the same as that shown in Fig. 4.6 for the nine pixel test IC. The pixels are physically laid out in a grid pattern, but for data shifting are connected in one large data delay line. The number of data shifts required to scan the array is equal to the number of pixels in the array.

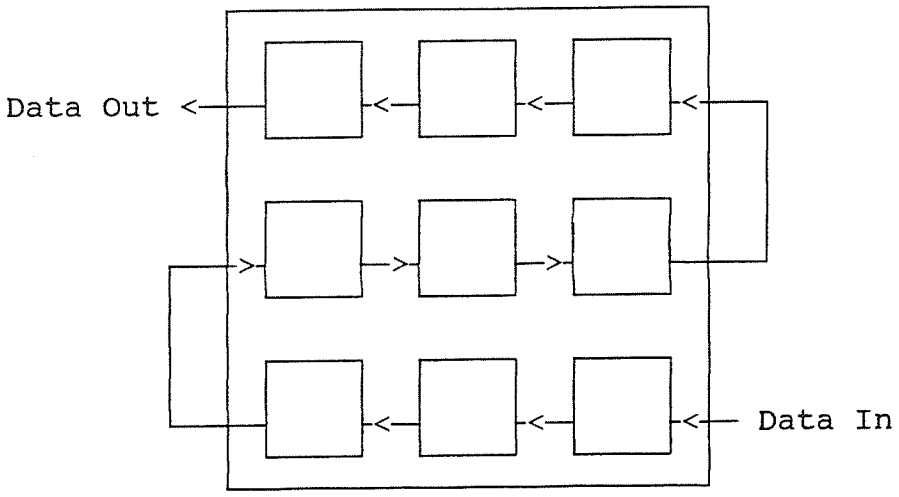


Figure 4.6. Nine Pixel Test IC Data Routing.

4.2.10 Data Receiver

The data receiver acts to assemble the edge point image prior to presenting the image to the controlling computer. The controlling computer may then access the compiled image by way of an interrupt for use in object recognition or determining the position of an object. The data receiver compiles an image in an X / Y grid coordinate system saving only X / Y data points which were determined to be an edge point from the sensor array. The X / Y coordinate image data can then be accessed for use.

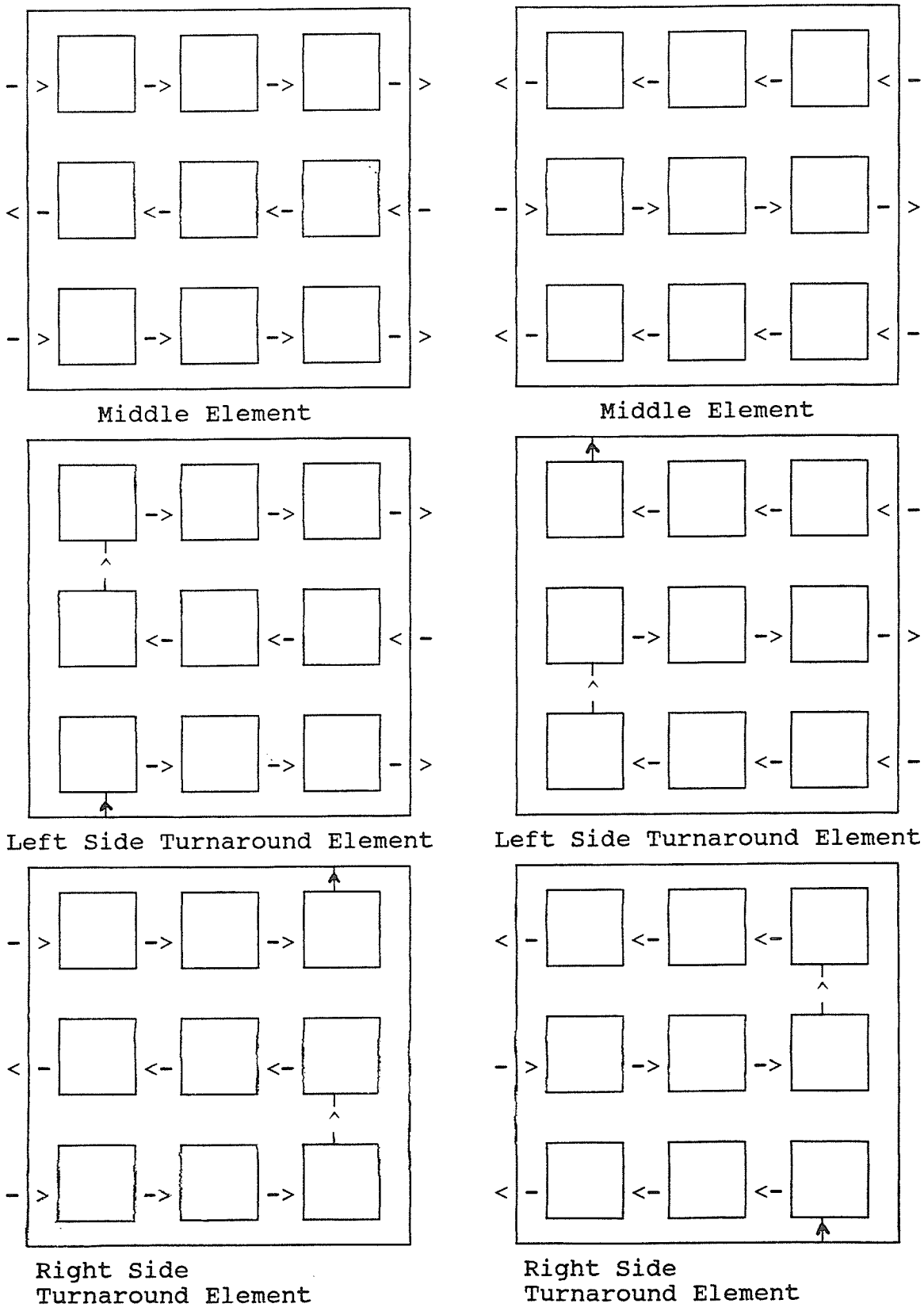


Figure 4.7. Large Sensor Shift Pattern Structures.

The origin of the sensor array is the top left corner which will have the coordinate value (0,0). The data receiver consists of two counters, memory, and control circuitry. One of the counters is required to track the X coordinate and the other one tracks the Y coordinate. The size of the counters will be dictated by the dimensions of the complete real world sized sensor array. The counters must be able to be reinitialized to zero. Due to the nature of the scanning, the counter which monitors the X coordinate must be an up / down counter. The counter which monitors the Y coordinate only has to be an up counter. The size and amount of memory required is, like the counters, dictated by the size of the complete sensor array.

The size of the sensor described will be assumed to be of dimension (n,m). The operation of the data receiver is as follows;

- Before edge data from the sensor array is scanned, the data receiver is initialized to receive data from the pixel at coordinate (0,0).
- Clk_3 controls the data scanning out of the sensor, and is also the controlling clock of the data receiver.
- As dictated by the scanning pattern the top row of data is received from left to right requiring that the X coordinate counter be incremented from 0 to n. The X / Y counter values will run from (0,0) to (n,0).

- The Y counter is incremented by one to make it ready for the second row of pixel data which will be received from right to left. The X coordinate counter is decremented from n to 0. The X / Y counter values will run from (n,1) to (0,1).
- This process is repeated until the complete sensor is scanned. This occurs when the Y coordinate value is equal to m + 1. The X / Y counter values will be either (0,m+1) or (n,m+1), when the image is completed.
- During scanning, the occurrence of a data value of 1 signals an edge point, causing the values of the X / Y counters to be stored in memory.
- The object outline is thus compiled in memory in a top down manner. At the end of the sensor scan the memory will contain the X / Y coordinates of each edge point detected.

Once the object outline is completely stored in memory, the X / Y coordinate data can be accessed in parallel directly from the memory registers. An interrupt could now be sent to the controlling computer signalling that an image is ready to be accessed. The computer would then read in the X / Y coordinate data until two consecutive zero values are read, this would signal that all valid edge point coordinates have been read and the process would end. Once all the data have been received, the computer could signal

the circuit to reinitialize the counters, and clear all memory registers.

The above description is for a data receiver which is implemented in a stand alone hardware circuit. This method will allow for the fastest possible scanning of the sensor structure. Scanning of the next image would be halted until the memory is read. If a higher image update rate is required by the controlling computer, two sets of memory could be used in a swinging buffer configuration. One memory array could be loading an updated image from the sensor while the other memory array is transmitting the last image to the controlling computer. This method would allow for continuous sensor scanning and the highest possible image update rate.

The major tasks of the data receiver are to filter out redundant sensor data and to compile the edge point image into a form which can be readily interpreted with little or no manipulation by the controlling computer.

4.2.11 System Simulation

In CSIM, a CMOS logic simulator, power and ground voltages, and data and clock signals can be applied to the design. Other data ports of the design can be monitored to verify the expected performance of the design.

The one pixel IC design performance was simulated first. Clock and control test vectors were created and

applied according to the timing diagram presented in Fig. 4.5. A special port was used at the input of the one bit latch to simulate data from the sensor input pad. Input data was applied to the serial_in input port. Appropriate data was applied to the North_in, South_in, East_in, and West_in data ports.

The serial_out output port was monitored to verify a correct data output signal. The North_out, South_out, East_out, and West_out pixel output data ports were monitored to verify that correct communication data was being generated for input to the neighboring pixels. Correct values were generated at the neighbor pixel output ports. Data applied at the input to the one-bit latch could be clocked through to the serial_out port. Data applied to the serial_in port could be clocked through to the serial_out port. The operation of the edge detection logic was verified by applying simulated neighbor pixel data to the one-pixel design.

The nine-pixel IC design performance was then simulated. Again power and ground voltages, and data, clock, and control vectors were applied to the design. Verification of the data shifting routine through all nine pixels was done. The output data vector equaled the input data vector. Simulated input pad data applied to any or all of the nine one bit latches could be clocked through to the serial_out port. Each of the nine pixels were examined in

this manner. Actual output data generated by neighboring pixels was applied to the center pixel to verify the edge detection logic. This verified that the inter-pixel communication and the complete edge detection system operated as designed. All troubleshooting which took place in the one-pixel IC testing carried through to the nine-pixel IC. Except for some data exporting problems which required solving, the simulation of the nine pixel IC generated expected results on the first attempt without any redesign being required.

4.3 Design Cycles

The ICs went through four design cycles prior to arriving at the final implementation. The initial cell size was 1380 µm x 1186 µm and was created using 5 µm design rules. A square shape was desired. In the final design the one pixel cell size was 1224 µm x 1176 µm and was created using updated 3 µm design rules.

The new technology offers two layers of metal and polysilicon whereas the original designs were created with only one layer of metal and polysilicon. This brings to light the point that future work in the area of tactile sensor design could be constructed with all necessary circuitry underneath the input sensor pad. The sensor pad could be constructed from the top layer of metal and any additional connections required could be implemented in the second layer of polysilicon. All required circuitry could

be designed in the lower levels of metal and polysilicon. Touch sensors constructed in this manner could have smaller sensor pads and be placed closer together. Pixel size would then be reduced, limited only by the size of the necessary processing circuitry laid out in a square arrangement.

4.4 Designing for Real World Use

Designing for real world use involves incorporating ideas which will be considered when constructing larger sensors from the 3 pixel by 3 pixel tactile sensor array. Some of the concepts were highlighted previously in the Power and Grounding section. Redundancy is provided for power and ground connections, giving the next level of sensor construction some degree of manufacturing fault tolerance. Other concepts of larger sensor design were shown in the section on Data Routing. The six versions in routing design will allow the data routing of a large sensor to follow the modified raster scanning method of serially transmitting the edge point data. The clock and control lines of the 3 x 3 IC are constructed to directly connect to the next 3 x 3 array placed above, below or on either side. All neighbor pixel communication lines are configured for the same type of connection to all neighboring 3 x 3 arrays.

In all stages of the design the IC was constructed to butt up against an adjacent IC in any direction without

further modification. In future work on larger sensor arrays the ICs would be manufactured with smaller connection pads. A manufacturing method for IC interconnection would have to be developed so that larger sensors could be constructed.

4.5 Kynar Film Considerations

The Kynar piezoelectric film is the active element in the sensor design, transforming mechanical force into an electrical voltage. The thin film performs the function of signal generation but is very susceptible to damage from the environment. Many types of protective coatings and mechanical isolation systems need to be evaluated to achieve a balance between overall durability and tactile sensitivity. A thin, easily replaceable, but strong rubber coating will be the protective answer for operations requiring a delicate touch system. A mechanical isolation system will be required for the sensor to eliminate the possibility of impact damage. See Figs 4.8 and 4.9 for cross sectional representations of two different IC isolation systems.

The Kynar film will be specially manufactured for the tactile sensor application with a continuous sheet of aluminum on one side and a pattern of aluminum or copper contact areas etched on the other side. The continuous sheet will be the electrical ground plane of the film input circuit. The patterned side of the film will match the

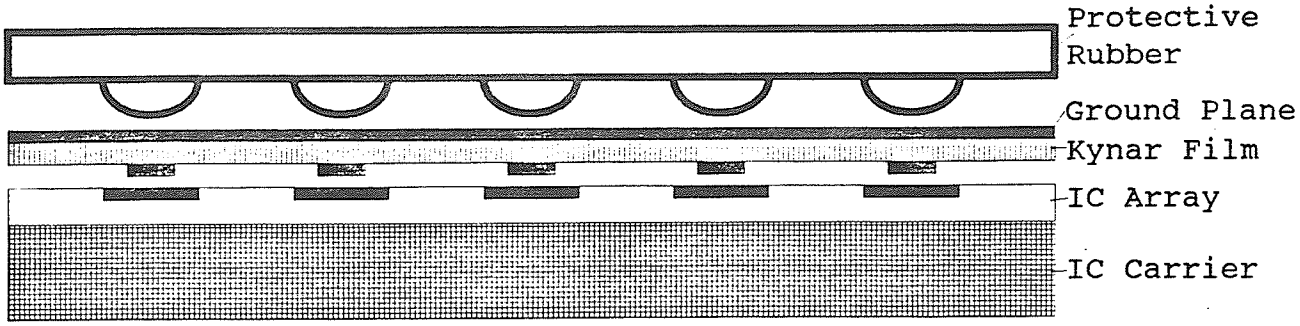


Figure 4.8. Direct Contact Protection System

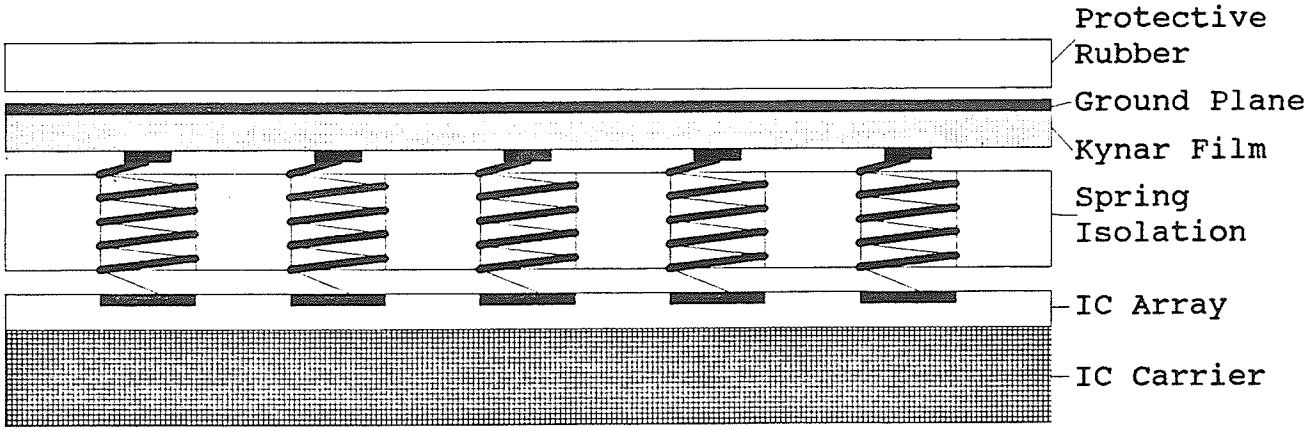


Figure 4.9. Spring Mechanical Isolation System

pattern of input pads on the sensor array. The etched areas will come into contact with the sensor pads of the VLSI sensor through various protective mechanical isolation systems. This electrical contact will bias the positive side of the Kynar film to the voltage present on the input of the biased inverter amplifier. A charge will develop between the ground plane and the etched pixel of the film when the piezoelectric material is compressed. This small generated voltage will add to the bias voltage and trigger the VLSI pixel below, thus indicating pressure at that point.

Testing of a piece of Kynar film was carried out to ensure its suitability for the required application. A sample piece of Kynar piezoelectric film with thickness of 110 μm was used. Experiments had to determine whether sufficient voltages were created by fairly low pressures in order to trigger the pixel input circuit. Results were encouraging. A piece of film with an area of approximately a 2.5 cm^2 was tested. With an object in contact with the film, moderate pressure was applied. Voltages of up to .8 volts were observed. When impact pressures were attempted, short duration transient impulses of up to 1.7 volts were detected.

Through SPICE simulations it was determined that voltages as low as .2 volts would be adequate to trigger the biased inverter amplifier. Voltages between .4 and .6 volts

generated by the Kynar film gave the most favorable results in successfully triggering a response by the VLSI sensor.

4.6 Design Summary

The one pixel and nine pixel designs have been fully described and implemented in silicon. All simulations of the designed sensor system show positive results.

In the next chapter, applications of the sensor for useful work will be discussed. Options for different Kynar piezoelectric film implementations will be presented. Considerations for a specialized multiple IC carrier will be discussed.

CHAPTER 5

LARGE SENSOR ARRAY CONSTRUCTION

5.1 Array Construction

In this chapter, ideas will be proposed to incorporate the touch sensor system into a useful device to carry out work. These ideas will be the forbearers in the construction of a working robotic gripper with a tactile sense. Considerations for the implementation of the Kynar piezoelectric film will be discussed. The mechanical design of a specialized IC carrier will be examined. The IC carrier will hold a large number of sensor circuits to be used in the construction of a useful sized tactile sensor..

5.2 Kynar Film Implementation

Methods of incorporating the Kynar piezoelectric film into the sensor system design will be discussed. These methods will highlight how the piezoelectric film will be mechanically attached to the sensor array.

The application of the piezoelectric film to the sensor array will involve an attachment by means of an adhesive. The film would be made in the normal three layers, two layers of metal sandwiching the piezoelectric material layer. One of the metal layers would then be chemically etched to have metal contact squares created to line up with the metal sensor pads of the sensor array. An adhesive could then be applied to the exposed piezo material areas of the film for contact with the overglass areas of the sensor circuit.

A similar attachment system would use a surrounding bracket to fasten down the piezo film to the sensor array. The construction of the film would be identical to that outlined in the adhesive method. The advantage to this system would be simple replacement of the piezoelectric film when necessary. The bracket would be constructed with precision alignment slots to allow the film to be accurately clamped in place over the sensor array.

5.3 Specialized Chip Carrier

In comparison to the sensor array the piezo material layer is inexpensive. If the working robotic gripper is in an environment where damage could occur, a mechanical system should be constructed to isolate the sensor array from that environment. The first step in creating a large, safe sensor array would be the construction of a rugged, durable chip carrier which will hold several of the individual ICs.

A material must be found which would offer sufficient rigidity to firmly hold the ICs in place and not allow the interconnecting wires to break due to motion or flexing. This material would also have the properties required to be able to absorb small impact shocks without breaking, while providing adequate protection to the IC sensor array.

As stated previously, the ICs which will be placed into the large array will have smaller connecting pads in comparison to normal IC connecting pads. The smaller pads are required to maintain the pixel spacing on one IC the

same across adjacent ICs. Each sensor chip would sit in a well and the connections would be made across small recesses in the well walls. The connections would then be covered with a layer of the chip carrier material.

5.4 Gripper System Operation

The constructed parallel plate gripper must provide a mechanical stimulus to the sensor array in order for it to operate. The piezoelectric film responds to a change in pressure and does not generate a charge under constant pressure. Due to this property of the piezoelectric material a vibrational stimulus must be applied once an object has been grasped. Integral to the mechanical design of the gripper jaws, a low amplitude, middle frequency resonator must be incorporated.

When an object is grasped and firmly held, the mechanical resonator begins to stimulate the parallel plates of the gripper. The design would be such that the two plates would compress and expand together. This mechanical stimulation would produce an electrical response in the piezoelectric film. The compression of the object would trigger the hardware routine which was detailed in the previous chapter. At the peak of compression the hardware would begin sampling the metal sensor pads for an induced voltage. The timing considerations dictate that the image refresh rate would be controlled by the frequency of vibration of the mechanical gripper.

CHAPTER 6

TESTING AND RECOMMENDATIONS

6.1 Testing Procedures

The hardware testing of the two ICs was performed to examine the operational limits of the manufactured design. Test procedures were designed and applied to both the one-pixel and nine-pixel ICs. The one-pixel IC had several test ports added in order to facilitate a detailed examination of the edge point determination algorithm. The testing of the nine-pixel circuit was focused upon the communication between pixels and the serial data scanning routine used to transmit the edge point data.

The test setup incorporated the use of the Hewlett Packard Data Generator (HP 8180A) and Data Analyzer (HP 8182A). A forty pin IC breadboard was used to physically hold the test circuits. Power and ground connections to the IC under test were supplied from the IC breadboard unit. Test vectors were programmed into the Data Generator for automated sequencing to the test circuits. Outputs and intermediate monitor points of the test IC were connected to ports on the Data Analyzer to observe the system operation. A block diagram of the test setup is shown in Fig. 6.1.

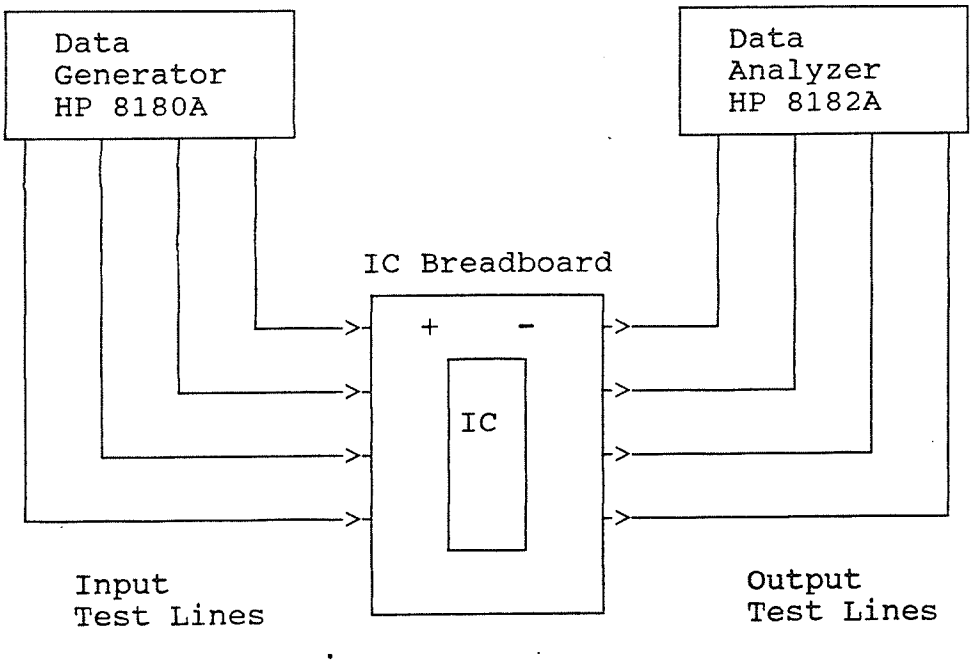


Figure 6.1. IC Test Setup.

The test procedures designed for the one-pixel IC included an examination of; the serial shifting operation, the edge point detection routine, and the input voltage threshold of the sensor pad amplifier. Test procedures designed for the nine-pixel IC included an examination of; the serial scanning operation, and a simulation of the edge point determination with external signals applied as would be generated by adjacently placed nine-pixel ICs.

The one-pixel serial shifting operation requires control of the five clock and control lines shown in the timing diagram of Fig. 4.5. A programmed pattern of serial data was applied at the Data_In port. The expected result was that the output data detected would follow the input data applied.

The one-pixel edge detection operation requires the use of the five clock and control lines, and the four adjacent pixel input lines. To simulate input from the Kynar piezo electric film, a low voltage signal was applied to the sensor pad test pin. The expected result was, when pad data and external pixel data were applied to the edge detection logic circuitry, the occurrence or nonoccurrence of an edge point could be detected at the Data_Out port.

To test the firing threshold of the biased amplifier assembly, incremental voltage signals were applied to the metal sensor pad. The applied voltages simulate the operation of the piezo electric film when pressure is applied. The one bit latch output data was expected to follow the low amplitude voltage changes applied to the sensor pad.

The nine-pixel IC serial scanning operation was examined. Test data was applied at the Data_In port. Monitoring was done at the Data_Out port. The output data was expected to follow the input data applied, after a delay of nine clock cycles.

The complete operation of the nine-pixel IC was examined. This system testing was done in three stages. The first stage involved applying test data to sensor pads and the N_in, S_in, E_in, and W_in lines via test pins of certain pixels. The selection of the test data was picked

to create the occurrence of edge points on the test IC. The test data was varied so that edge points could be created at selected points in the nine-pixel array. It was expected that edge data would occur in the positions predetermined by the test data applied.

The second stage of the testing was done in a similar manner, but with test data applied directly to the sensor pads using test probes. Again the test data was varied, and it was expected that edge data would occur in the positions predetermined by the test data applied.

The third and final testing stage involved simulating the operation of a larger sensor array than the single nine pixel IC. The data applied to the N_in, S_in, E_in, and W_in lines simulated pressure data from adjacently placed nine-pixel sensor circuits. The clock and control lines were programmed to carry out a continuously repeating routine of; sensor pad sampling, edge point determination, parallel loading of the shift registers, followed by serially scanning the edge data. During the scanning, test data was applied to the serial data input port. This test data simulated edge point data coming from adjacently placed nine-pixel ICs. The expected result was that data detected at the serial output port was firstly, locally generated edge data, followed by the externally generated edge point data.

6.2 Results

To begin each procedure, the designed test routines were implemented and made to operate at a clock frequency of 1.0 kHz Monitoring of output ports was done at similar clock speeds while expected data was observed. Once the test procedures provided the expected data, the operational clock speeds were increased. As the clock frequency increased the output data was monitored until errors in the expected data were observed. The clock frequency just before incorrect expected data began to appear, became the upper speed limit for system operation. Test results and the corresponding upper speed limit for each test routine and portion of the design will be presented. The IC pin designations are shown in the diagrams which were returned with the manufactured circuits. Refer to to Fig. 6.2 for the one-pixel pin out designation. Refer to to Fig. 6.3 for the nine-pixel pin out designation. The details of all the test routines are located in Appendix B.

The single pixel serial shifting routine was examined first. The results show that the output correctly tracked the input after a one clock period delay. The serial shifting operated error free at a 10 MHz clock frequency.

The single pixel edge point detection logic was tested. The results highlight that upon application of the programmed N_in, S_in, E_in, and W_in data and the internally created pressure data to the logic circuitry:

CMC MULTIPROJECT BONDING DIAGRAM

RETICLE CODE U285

BRAND ID LABEL IC3 / MB064

OTHER IDENTIFICATION FEATURES

WAFER NUMBERS

DESIGN FILE REFERENCE

PACKAGE	IDK40F1-192G		LID	C-493-175-35M	
WIRE ALLOY	99% Al/1% Si 99% Al/1% Si	DIA.	.001" .00125"	ELONG.	1.5 - 4% 1.5 - 4%
T.S.	14-16 gms 18-22 gms				
D/A PREFORM	ALLOY 98% Au/2% Si	RECOMMENDED SIZE		W/B METHOD	U.S.

BONDING DIAGRAM

NOTES: 1. DIE ATTACH PAD SIZE: .400 X .400

2. ZERO GROUND

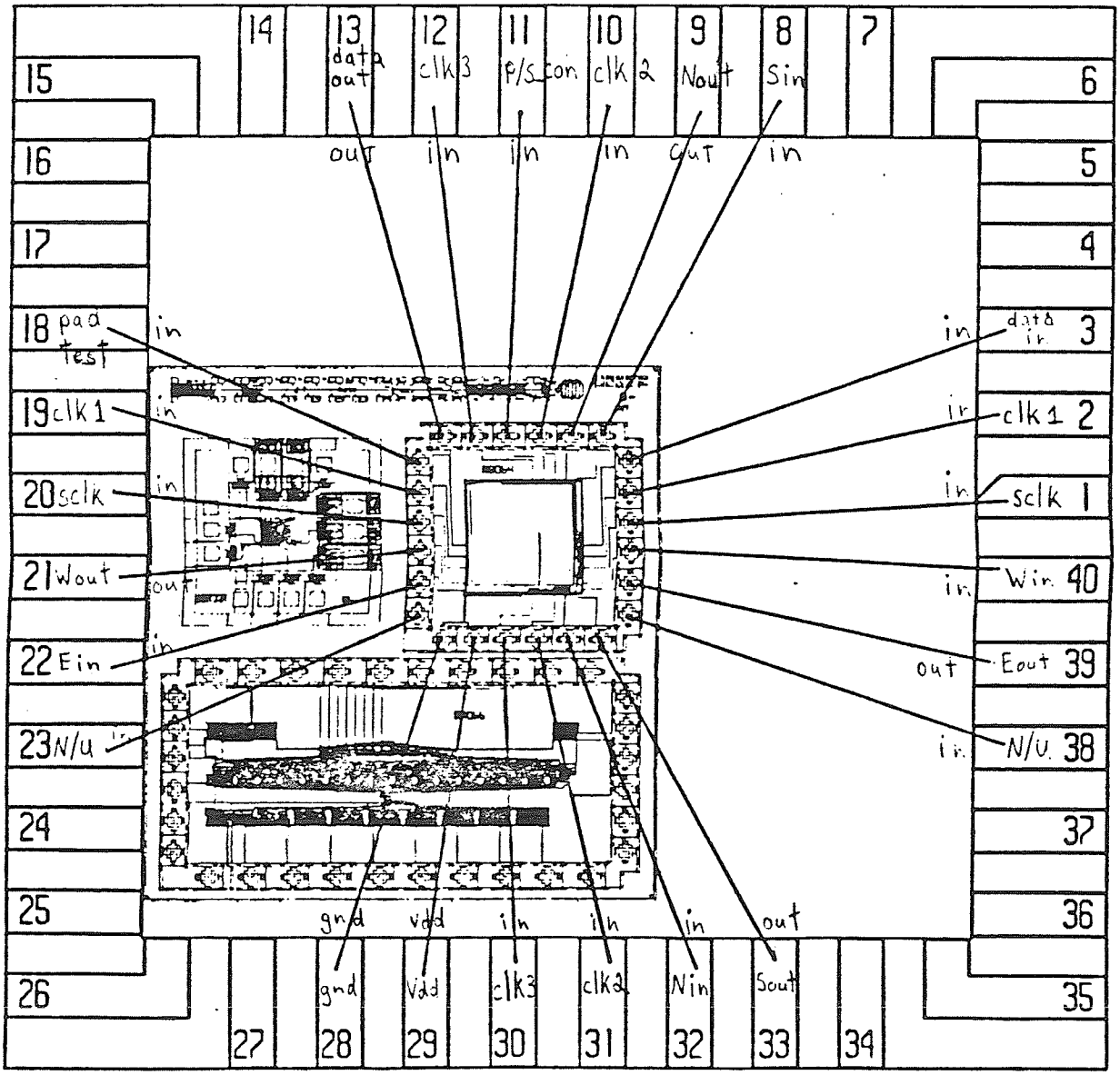


Figure 6.2. Single Pixel IC Pinout

~~CMC~~ MULTIPROJECT BONDING DIAGRAM

RETICLE CODE U28P

BRAND ID LABEL IC3 MB065

OTHER IDENTIFICATION FEATURES

WAFER NUMBERS

DESIGN FILE REFERENCE

PACKAGE	IDK40F1-192G			LID	C-493-175-35M		
WIRE ALLOY	99% Al/1% Si 99% Al/1% Si	DIA.	.001" .00125"	ELONG.	1.5 - 4% 1.5 - 4%	T.S.	14-16 gms 18-22 gms
D/A PREFORM	ALLOY 98% Au/2% Si	RECOMMENDED SIZE		W/B METHOD	U.S.		

BONDING DIAGRAM

NOTES: 1. DIE ATTACH PAD SIZE: .400 X .400

2. ZERO GROUND

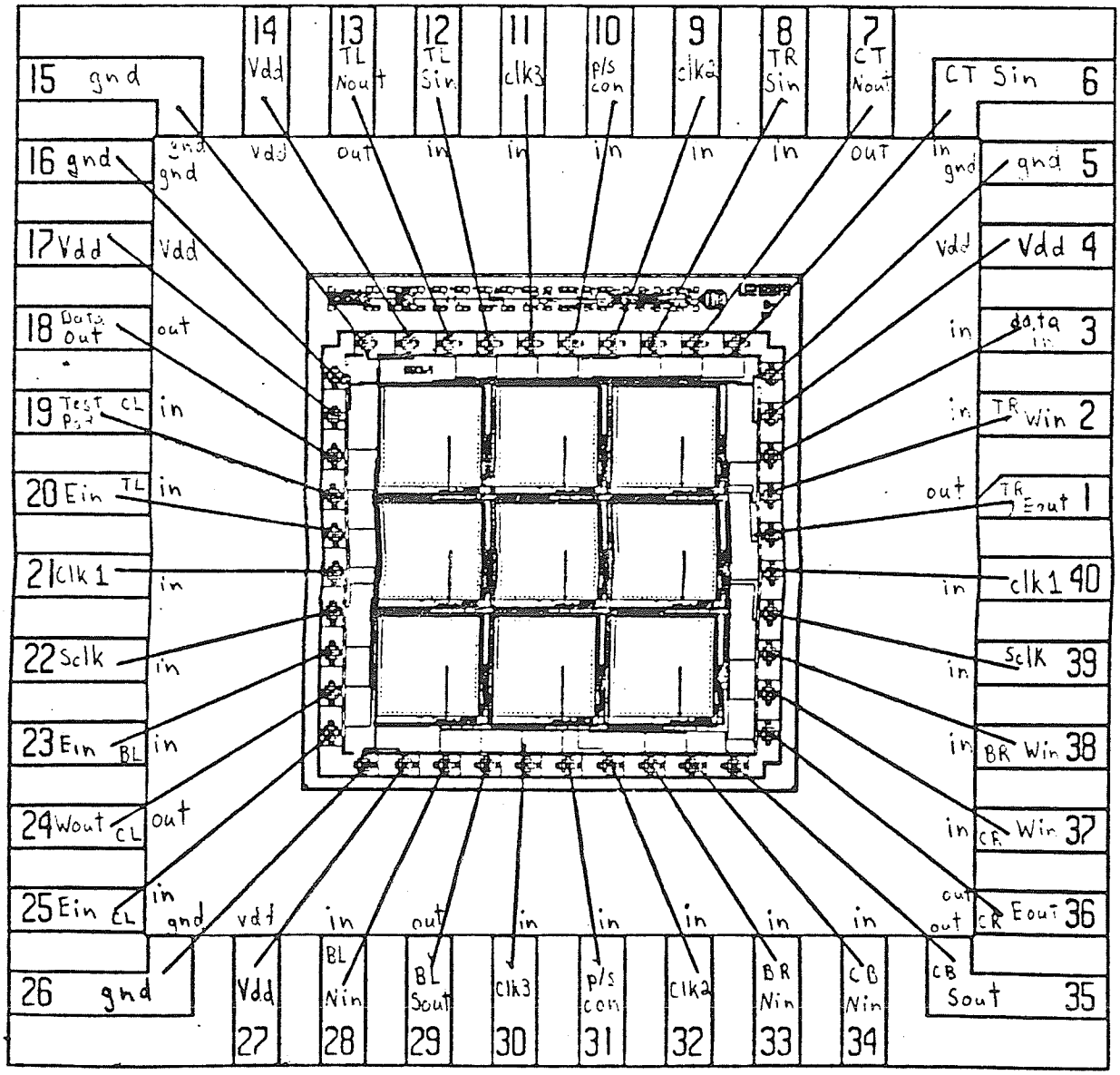


Figure 6.3. Nine Pixel IC Pinout

- a value of 1 signifying an edge point was detected when an isolated point was simulated.
- a value of 1 signifying an edge point was detected when an edge point was simulated.
- a value of 0 signifying an interior point was detected when an interior point was simulated.

The data supplied to the N_out, S_out, E_out, and W_out lines was correctly generated, signalling the presence or absence of simulated pressure data at the pixel under test. The edge detection logic could be clocked at 10 MHz without errors occurring.

The sampling requirements of a tactile pixel were examined. The results show that while sampling the amplifier output at 20 MHz, the number of sampling pulses could be reduced down to seven without the occurrence of errors. During further trials at a 10 MHz sampling rate, the number of sampling pulses could be reduced to three without the occurrence of errors.

The firing threshold of the biased inverter amplifier was tested. Small incremental voltage values were applied until the desired operation of the amplifier was observed. During the design stage the biased amplifier was calculated to be biased at 2.6 volts. In the preliminary testing of the single pixel IC it was found that the actual bias point of the amplifier was 2.7 volts. The results of the biased inverter amplifier threshold testing show that an

incremental application of .2 volts triggered the amplifier to the high output state. The sensor pad test data could be applied at 500 kHz without the occurrence of errors.

The nine-pixel serial scanning routine was examined. The serial scan testing highlights that the output correctly tracked the input after a nine clock period delay. The serial scanning operation was successful at a clock rate of 10 MHz.

The complete system operation of the nine-pixel IC was tested in three stages. The results of the first stage nine pixel IC testing show that after a parallel loading interruption, the edge data which was applied to the fourth pixel in the nine-pixel chain appeared in its correct position, preceded by three zeroes and followed by five zeroes. After resumption of the serial shifting, the locally generated data, was correctly followed by the input data applied. The system operation was successful at a clock rate of 2 MHz. The clock frequency was limited by the sampling procedure required to read the test data applied to the sensor pad.

The results of the second stage of the nine-pixel IC testing with pad data applied through a probe highlight that in each case after the parallel loading interruption, the edge data applied in the nine-pixel chain appeared in its correct position. All nine positions were examined with a correct response generated from each one.

The results of the third stage complete nine-pixel IC testing with adjacent IC simulation follow. The simulated edge data which was created by the combination of the sensor pad test pin, the test probe and the adjacent IC vectors appeared in their respective positions in the nine-pixel chain. The complete system operation was successful at a clock rate of 2 MHz, again limited by the sampling procedure.

The remaining system testing involves the etching of the Kynar piezo electric film to create sensor pad connections, and construction of a mechanical test apparatus. This test setup will allow direct pressure to be applied which will generate the voltage signals for the test ICs. The setup will test the system with pressure data for the sensor pads generated as it would be in actual system operation. The construction of this test apparatus is beyond the scope of this work, and is left to an undergraduate thesis project. The preliminary design work for the mechanical test setup has been completed by Gary Nelson in partial fulfillment of his undergraduate degree.

6.3 Recommendations

The test ICs were examined for proper functional performance and the highest error free operating frequency was determined. As is generally true when analog and digital systems are interfaced, the conversion of a signal

from an analog to a digital representation often becomes a speed bottleneck due to timing and sampling considerations. The designed sensor arrays are limited in image refresh frequency by the required amplification and sampling functions. The major throughput bottleneck of the implemented design is the biased inverter amplifier. The slow rise and fall time of the amplifier limits the frequency at which pressure data can be accurately detected.

A major improvement in tactile image throughput could be attained by the implementation of a stringently designed operational amplifier in place of the biased inverter amplifier. The op-amp would be designed to ensure that a zero voltage presented to the input will reset the output to the 0 state. The amplifier must be intolerant to the manufacturing process variation of resistor values. Also the amplifier should be capable of receiving and acting upon a universal reset signal which would initialize all amplifier outputs to a low state prior to detecting input pressure voltages. The op-amp would enhance the throughput rate of the IC but the mechanical operation of the Kynar film will remain the limiting factor in the complete system.

Further testing of an actual larger sensor array should be performed. In order to implement this testing, nine pixel ICs must be manufactured with pixel connection strategies as illustrated in Fig. 4.7. The larger sensor

array when constructed should be subjected to the same rigorous test routines as were described in the previous section for the one and nine-pixel ICs.

When an improved sensor array has been constructed and further testing of a physically larger array has been done, a hardware sequencer should be designed to control the system. The sequencer would control the timing of the system by generating the clock and control signals according to the timing diagram presented in Fig. 4.5.

CHAPTER 7

SUMMARY AND CONCLUSIONS

7.1 Summary

The design of the tactile sensor building block entailed several related studies. The human tactile system was analyzed in detail, examining the touch receptor size, density, and firing threshold. Several hardware algorithm design strategies, each implementing a four point edge determination scheme were considered. The different design strategies varied in construction and communication complexity. Key operating features of each design strategy were combined to create the final sensor array configuration.

The edge point determination was chosen to be executed in parallel because the sensor data did not have to be manipulated to achieve a data structure in which edge points could be solved for. A serial routing scheme was chosen to transmit the edge data because the shift register hardware could always be clocked faster than the required sensor pad sampling routine. This strategy would avoid possible processing bottlenecks. The serial communication system kept to a minimum the number of clock, input, and output lines required to operate the sensor array.

The hardware system was designed in CMOS VLSI, creating two test integrated circuits. A single pixel circuit with many additional test pins and a nine pixel building block to examine the complete system operation were designed and implemented in silicon. The chosen systems went through four computer design cycles prior to the final design being constructed. Upon return of the manufactured ICs, complete system testing was performed. The complete operation of a single pixel was examined for speed and firing threshold. The nine pixel block was tested for system operation, and a larger sensor array was simulated to examine the real world sized performance of the design.

7.2 Conclusions

A successful hardware implementation of the four point edge detection algorithm has been achieved. The designed integrated circuits performed as expected. As found in the testing stage, the performance of the biased inverter amplifier was the source of the tactile image processing bottleneck. The relatively slow response time of the amplifier was isolated as the limiting factor in the tactile image throughput. Sensor pad sampling rates as highlighted below dictate the tactile image refresh rate.

Table 7.1. Sensor Pad Sampling.

Sampling Frequency	No. of Samples	Sampling Duration	Total Period
2 MHz	3	.5 μs	1.5 μs
5 MHz	8	.2 μs	1.6 μs

While sampling the sensor pad at 2 MHz error free operation occurred when 3 samples of the pad voltage were taken. Using this sampling rate, an upper limit edge point image refresh rate of 666.6 kHz is attainable. While sampling the sensor pad at 5 MHz error free operation occurred when 8 samples of the pad voltage were taken. This sampling rate allows an upper limit edge point image refresh rate of 625.0 kHz.

The above data leads to the realization that the designed system could produce edge data images at an effective rate in excess of 600 kHz. A complete one hundred pixel array using a serial scan clock rate of 10 MHz could then transmit useful sized tactile images at a rate of 100 kHz. This image refresh rate is high enough to perform the desired task of object identification from a list of objects that the gripper could be exposed to, and also the object's position in the gripper. The image refresh rate is also sufficient to detect and correct for object slipping. The designed system may not however, have the processing throughput required for robotic kinesthesia which would be

required for real time object manipulation used possibly in automated manufacturing. These speeds could be easily achieved by implementing a specially designed operational amplifier in place of the biased inverter amplifier. With a more accurate amplifier creating improved rise and fall response times, and pushing the serial scan clock rate to 100 MHz, useful image refresh rates could be easily increased to beyond 1 MHz.

When the system design began, the manufacturing technology offered by Northern Telecom was a 5 μm single metal layer CMOS process. The edge detection processor was implemented with the metal sensor pad located physically in the middle of the tactile pixel with the required processing circuitry surrounding the pad. This strategy was dictated by the availability of only one metal layer which was used for the sensor pad and made the complete pixel size much larger than the metal pad itself. In the final design stage the IC manufacturing process offered by Northern Telecom was updated to a 3 μm dual metal layer CMOS process. Due to the change in technology a scaling process was used to translate the 5 μm design to a 3 μm implementation. A major redesign would have been required to fully take advantage of the improved manufacturing process and was not undertaken due to time constraints. The major fact that came to light was that a working system could be implemented in a single metal layer technology. This led to the realization that future tactile pixel systems could fully

exploit the dual metal layer manufacturing process by placing the edge point processing circuitry underneath the metal sensor pad. A future design using this layered strategy could be constructed with a substantially higher resolution. It was also observed that pixel size could then if required, decrease down to the area required to lay out the edge processing circuitry.

The future design possibilities discussed in the previous section could lead to tactile ICs being manufactured with more than nine pixels per chip. With the use of physically larger integrated circuits and placing the edge processing circuitry underneath the metal sensor pad, both pixel resolution and pixel count per chip could increase substantially. Using these ideas, and finding the balance between chip size and effective IC yield, could greatly simplify the later manufacturing detail required to construct useful sized tactile sensors.

A major problem to be overcome in constructing useful sized sensors from individual ICs is maintaining the pixel spacing at the junction of two ICs. Pixel spacing on one individual IC must be maintained across each junction when several ICs are connected to facilitate larger sensor construction. This problem can be solved by manufacturing the individual ICs with very small connection pads. Research is required to find the minimum sized pad which can serve as the platform to efficiently connect two ICs

together from a manufacturing viewpoint. Once this minimum connection pad size is determined, it will dictate the minimum spacing between pixels both on the individual ICs and across the junction of the edges of two ICs. Together with this work, a process must be developed to form the actual connections between the ICs. This process would would borrow ideas from the well established method of connecting an IC to its pin package.

As discussed in detail in Chapter 5, specialized chip carriers must be designed and constructed to hold, protect, and form the strength member of a useful sized sensor. Research into the type of material used, and the method of attaching the individual ICs to the chip carrier is required. The design must incorporate very accurate tolerances in IC placement and must facilitate and provide protection for the interconnection structure of the large sensor array. In an end to all the specialized chip carrier design, each separate application in which the sensor array will be used must be analyzed and optimized from a performance and threshold sensitivity perspective.

The use, attachment, and protection of the Kynar piezo-electric film must be examined in further detail. Several proposals for mechanical isolation of the piezo film, sensor pad system were suggested in Chapter 5. The potential for higher generating voltages from thicker or layered piezo-electric film should be tested in order to obtain a range of

voltage and threshold values to be applied to a specific application. A further possibility for the implementation of the piezoelectric film is that it could be grown on the metal sensor pad as a last stage in the VLSI manufacturing process. This process could be accurately controlled to produce specific performance parameters and would reduce the complexity of large sensor construction.

The design constructed in this thesis would easily lend itself to a multiple threshold implementation using A/D devices on the output of the amplifier. The pressure applied on different areas of an object could be read out on subsequent tactile images. The edge outline of a specific pressure threshold could be read by altering the firing threshold of the amplifier / analog to digital circuitry system. Edge point images would be constructed in a similar manner to the single threshold design, with subsequent images showing different pressure gradients.

Finally, the research carried out in this thesis could be applied to a wide variety of technologies. A proven process exists where detailed circuitry can be manufactured using a flexible medium. When the circuitry required to implement a tactile sensor array is simplified and finalized, the manufacture of a strong, flexible sheet of touch pixels would find a wide variety of uses. These would include a precursor to a robotic skin, and the active element in providing simple touch to a prosthetic limb to give limited tactile feedback to a human user.

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APPENDIX A

```
INPUT INVERTER FOR SENSOR PAD GAIN
*
* A Gain Biased CMOS Inverter
*
.OPTIONS LIMPTS=1E6 NODE
*
* Transistor Definition
*
M0 2 3 1 1 PENH L=5.e-06 W=150.e-06
M1 0 3 2 0 NENH L=5.e-06 W=50.e-06
*
* Source and Input Definition
*
VDD 1 0 DC 5V
*VIN 3 0
*
* Node Capacitance
*
CVDD 1 0 2.5071e-14
CINP 3 0 1.54538e-13
COUT 2 0 9.5792e-14
*
* Resistor Definition
*
R1 4 2 13499
R2 4 1 33389
R3 4 3 19469
*
* Transistor Models
*
.MODEL NENH NMOS (LEVEL=2.0 VTO=0.950 KP=24.8E-06 GAMMA=1.3
+ PHI=0.7 LAMBDA=1.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=4.0E-10 CGDO=4.0E-10
+ CGBO=2.0E-10 RSH=15.0 CJ=4.0E-4 MJ=2.0 CJSW=8.0E-10 MJSW=2.0
+ JS=1.0E-6 TOX=8.50E-8 NSUB=9.92E15 TPG=1.0 XJ=1.0E-6
+ LD=7.0E-7 UO=750 UCRIT=6.4E04 UEXP=0.139 VMAX=5.0E+4)
.MODEL PENH PMOS (LEVEL=2.0 VTO=-0.95 KP=8.4E-6 GAMMA=0.6
+ PHI=0.6 LAMBDA=3.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=4.0E-10 CGDO=4.0E-10
+ CGBO=2.0E-10 RSH=75.0 CJ=1.8E-04 MJ=2.0 CJSW=6.0E-10
+ MJSW=2.0 JS=1.0E-6 TOX=8.50E-08 NSUB=1.98E15 TPG=1.0
+ XJ=9.0E-7 LD=6.0E-7 UO=250.0 UCRIT=1.23E04 UEXP=0.022
+ VMAX=3.0E4)
*
* Analysis Definition
*
.TRAN 1NS 50NS
*
* Output Definition
*
.PRINT TRAN V(3)
.PRINT TRAN V(2)
.PRINT TRAN V(1)
.END
```

```
INPUT INVERTER FOR SENSOR PAD GAIN
*
* A Gain Biased CMOS Inverter
* With Second Latching Inverter
*
.OPTIONS LIMPTS=1E6 NODE
*
* Transistor Definition
*
M0 2 3 1 1 PENH L=5.e-06 W=150.e-06
M1 0 3 2 0 NENH L=5.e-06 W=50.e-06
M2 4 2 1 1 PENH L=5.e-06 W=20.e-06
M3 0 2 4 0 NENH L=5.e-06 W=20.e-06
*
* Source and Input Definition
*
VDD 1 0 DC 5V
VIN 3 0
*
* Node Capacitance
*
CVDD 1 0 2.5071e-14
CINP 3 0 1.54538e-13
COUT 2 0 9.5792e-14
CL   4 0 9.5e-14
*
* Resistor Definition
*
R1 3 2 6K
R2 3 1 15K
*
* Transistor Models
*
.MODEL NENH NMOS (LEVEL=2.0 VTO=0.90 KP=3.05E-05 GAMMA=1.592
+ PHI=0.695 LAMBDA=1.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=2.84E-10 CGDO=2.84E-10
+ CGBO=2.0E-10 RSH=15.0 CJ=3.44E-4 MJ=0.50 CJSW=1.09E-9 MJSW=0.50
+ JS=1.37E-5 TOX=8.50E-8 NSUB=9.92E15 TPG=1.0 XJ=1.0E-6
+ LD=7.0E-7 UO=750 UCRIT=6.4E04 UEXP=0.139 VMAX=4.92E+5)
.MODEL PENH PMOS (LEVEL=2.0 VTO=-0.90 KP=9.75E-6 GAMMA=0.634
+ PHI=0.612 LAMBDA=3.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=2.44E-10 CGDO=2.44E-10
+ CGBO=2.0E-10 RSH=75.0 CJ=1.54E-04 MJ=0.50 CJSW=4.37E-10
+ MJSW=0.50 JS=4.19E-10 TOX=8.50E-08 NSUB=1.98E15 TPG=1.0
+ XJ=9.0E-7 LD=6.0E-7 UO=240.0 UCRIT=1.23E04 UEXP=0.022
+ VMAX=7.33E4)
*
* Analysis Definition
*
.DC VIN 0 5.0 .1
*
* Output Definition
*
.PRINT DC V(3)
.PRINT DC V(2)
.PRINT DC V(4)
.END
```

```
INPUT INVERTER FOR SENSOR PAD GAIN
*
* A Gain Biased CMOS Inverter
* With Second Latching Inverter
* (Transient Analysis)
*
.OPTIONS LIMPTS=1E6 NODE
*
* Transistor Definition
*
M0 2 3 1 1 PENH L=5.e-06 W=155.e-06
M1 0 3 2 0 NENH L=5.e-06 W=60.e-06
M2 5 2 1 1 PENH L=5.e-06 W=20.e-06
M3 0 2 5 0 NENH L=5.e-06 W=30.e-06
*
* * Source and Input Definition
*
VDD 1 0 DC 5V
VIN 3 0 PULSE(2.3 2.9 5NS 2NS 2NS 4NS 25NS)
*
* Node Capacitance
*
CVDD 1 0 2.5071e-14
CINP 3 0 1.54538e-13
COUT 2 0 9.5792e-14
CL   4 0 9.5e-14
*
* Resistor Definition
*
R1 4 2 13499
R2 4 1 19469
R3 4 3 33389
*
* Transistor Models
*
.MODEL NENH NMOS (LEVEL=2.0 VTO=0.95 KP=24.8E-06 GAMMA=1.3
+ PHI=0.7 LAMBDA=1.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=4.0E-10 CGDO=4.0E-10
+ CGBO=2.0E-10 RSH=15.0 CJ=4.0E-4 MJ=2.0 CJSW=8.0E-10 MJSW=2.0
+ JS=1.0E-6 TOX=8.50E-8 NSUB=9.92E15 TPG=1.0 XJ=1.0E-6
+ LD=7.0E-7 UO=750 UCRIT=5.0E04 UEXP=0.14 VMAX=5.0E+4 NEFF=1.0)
.MODEL PENH PMOS (LEVEL=2.0 VTO=-0.95 KP=8.4E-6 GAMMA=0.6
+ PHI=0.6 LAMBDA=3.0E-2 RD=2.0E0 RS=2.0E0 CBD=2.0E-14
+ CBS=2.0E-14 IS=1.0E-14 PB=0.70 CGSO=4.0E-10 CGDO=4.0E-10
+ CGBO=2.0E-10 RSH=75.0 CJ=1.8E-4 MJ=2.0 CJSW=6.0E-10
+ MJSW=2.0 JS=1.0E-6 TOX=8.50E-08 NSUB=1.98E15 TPG=1.0
+ XJ=9.0E-7 LD=6.0E-7 UO=250.0 UCRIT=1.0E04 UEXP=0.03
+ VMAX=3.0E4 NEFF=1.0)
*
* Analysis Definition
*
.TRAN 1NS 50NS
*
* Output Definition
*
.PRINT TRAN V(3)
.PRINT TRAN V(2)
.PRINT TRAN V(4)
.PRINT TRAN V(5)
.END
```

```
MOS OUTPUT CHARACTERS
.OPTIONS NODE
VDS 3 0
VGS 2 0
M1 1 2 0 0 MOD1 L=4U W=6U AD=10P AS=10P
.MODEL MOD1 NMOS VTO=-2 NSUB=1.0E15 UO=550
VIDS 3 1
.DC VDS 0 10 .5 VGS 0 5 1
.PRINT DC I(VIDS) V(2)
.PLOT DC I(VIDS)
.END
```

DESIGN REFERENCE: MB064

TITLE: A SINGLE PIXEL TACTILE SENSOR

DESIGNER: Gerry Klym M.Sc.
Department of Electrical Engineering
University of Manitoba

DESCRIPTION: The IC is single pixel tactile sensor implemented for testing the tactile performance of the design. The IC facilitates exhaustive testing of a biased inverter amplifier and the single pixel's edge detection and data routing circuitry. The large metal pad accepts small voltages generated by a piezo electric film. This signal is amplified and conditioned for tactile image edge detection. Edge data is then loaded into a parallel load, serial shift register and read out of the pixel.

OTHER INFORMATION: The work is part of an M.Sc. thesis research project.

NOTE: The large metal pad has the protective layer of overglass removed for contact with a piezo electric film.

DESIGN REFERENCE: MB065

TITLE: A TACTILE SENSOR BUILDING BLOCK

DESIGNER: Gerry Klym M.Sc.
Department of Electrical Engineering
University of Manitoba

DESCRIPTION: The IC is nine pixel tactile sensor implemented for testing the tactile system performance of the design. The IC facilitates exhaustive testing of the nine pixel edge detection and data routing circuitry. The large metal pads accept small voltages generated by a piezo electric film. These signals are amplified and conditioned for tactile image edge detection. Edge data is then loaded in parallel and serially raster scanned out of the sensor.

OTHER INFORMATION: The work is part of an M.Sc. thesis research project.

NOTE: The large metal pad has the protective layer of overglass removed for contact with a piezo electric film.

APPENDIX B

TEST 1. One Pixel Serial Shift Test

IC Pin	Pin Designation	Connected To
28	Ground	IC Breadboard Ground
29	+ 5 V.	IC Breadboard Power
3	Data In	Port 0 0 Data Gen
11	P/S_Con	Port 0 2 Data Gen
12 or 30	Clock 3	Port 0 1 Data Gen
13	Data Out	Port 0 0 Data Anal

Table. B.1. One Pixel Serial Shift Test Wiring.

- Examine the operation of the parallel load / serial shift, shift register control line (p/s_con), and the serial shifting routine.
- Toggle Clock 3.
- Apply test data to the Data In port.
- Monitor the Data Out port
  - when the p/s_con line is low the shift register is in the parallel load mode.
  - test data applied to the Data In port is inhibited from reaching the Data Out port.
  - all zeroes should appear at the Data Out port.
  - when the p/s_con line is high the shift register is in the serial shift mode.
  - test data applied to the Data In port is connected and ready to be clocked to the Data Out port.
  - Data Out should equal Data In with one clock period delay.

- The results of the one pixel serial shift testing are as follows:
  - all zeroes appeared at the output when p/s_con was low.
  - the output correctly tracked the input after a one clock period delay when p/s_con was high.
  - the serial shifting operation was successful to a clock rate of 10 MHz.

TEST 2. One Pixel Edge Point Logic Test

IC Pin	Pin Designation	Connected To
28	Ground	IC Breadboard Ground
29	+ 5 V.	IC Breadboard Power
1 or 20	Sample Clock	Port 0 1 Data Gen
2 or 19	Clock 1	Port 0 3 Data Gen
10 or 31	Clock 2	Port 0 2 Data Gen
11	P/S_Con	Port 1 1 Data Gen
12 or 30	Clock 3	Port 0 1 Data Gen
18	Sensor Pad Input	Port 0 0 Data Gen
8	South In	Port 2 0 Data Gen
22	East In	Port 1 2 Data Gen
32	North In	Port 1 3 Data Gen
40	West In	Port 2 1 Data Gen
13	Data Out	Port 0 1 Data Anal
18	Sensor Pad Input	Port 0 2 Data Anal
39	East Out	Port 0 0 Data Anal

Table. B.2. One Pixel Edge Point Logic Test Wiring.

- Examine the operation of the edge point detection logic. Verify that edge data created internal to the pixel can be loaded into the parallel load port of the shift register and can then be serially shifted to the data output pin.
- Program the sampling clock, Clock 3, and the parallel / serial control lines into the Data Generator according to the system timing diagram presented in Fig 4.5.
- Hold Clock 1, and Clock 2 high so that sensor pad data can ripple through the amplifier, be sampled by the latch, and be passed directly through the edge detection logic to the parallel load port of the shift register.
- Apply small voltage change test data to the sensor pad test pin to simulate pressure data. Monitor this voltage to aid in observing the timing synchronization of the sensor pad sampling procedure.
- Create several test vectors for the N S E W input lines to make the single pixel under test; an isolated point, an edge point, and an interior point. Program these vectors into the Data Generator.
- Monitor one of the N S E W output lines to verify that pressure data to adjacent pixels is being properly generated corresponding to the low voltage test data applied.
- Monitor the Data Out port to observe the expected data being generated.

- the sampling clock applied to the one bit latch should enable the latch to successfully read pressure data being simulated on the sensor pad.
- the Clock 3 and p/s_con lines should operate the parallel loading, followed by the serial shifting of the shift register.
- Clock 1 and Clock 2 when held high, will allow edge data to flow directly through the transmission gates to the parallel load port of the shift register.
- the simulated pressure small voltage changes should trigger the biased amplifier to its high state, thus replicating the voltages which will be generated by the piezo electric film.
- the programmed N S E W test data should simulate data which will be generated from adjacent pixels under actual working sensor system conditions.

- The results of the one pixel edge detection logic operational testing are as follows:
  - the clock and control lines successfully operated the sampling and routing tasks required.
  - the applied small voltage test data triggered the biased inverter amplifier to the high state and returned the amplifier to a low state when the small voltage increment was removed.
  - upon application of the programmed N S E W input lines to the logic circuitry in conjunction with the internally created pressure data:

- a value of 1 signifying an edge point was detected when an isolated point was simulated.
- a value of 1 signifying an edge point was detected when an edge point was simulated.
- a value of 0 signifying an interior point was detected when an interior point was simulated.

- data supplied to the N S E W output lines was correctly generated, signalling the presence or absence of simulated pressure data at the pixel under test.
- the presence or absence of edge point data was detected at the output data port in accordance with the small voltage change test data and N S E W input data applied to the one pixel circuit.
- using a five clock period sampling interval of the sensor pad the operation of the edge detection logic could be driven to 10 MHz. without errors occurring.

TEST 3. Input Pressure Signal Duration Test

- Examine the time duration that the small voltage signal from the piezo electric film must be valid in order to successfully detect the pressure voltage on the sensor pad.
- Vary the clock speed and number of sampling pulses applied to the one bit latch while monitoring one of the N S E W output data lines to observe successful sampling.

- apply a constant small voltage value to the sensor input pad when the sampling routine begins to place the biased amplifier in its high output state.
- sample the amplifier output nine times while increasing the sampling rate until errors occur.
- after determining the maximum error free sampling rate decrease the number of sampling pulses until errors occur.

- The results of the sensor pad sampling duration testing are as follows:
  - using nine sampling pulses, successful amplifier sampling was achieved to a clock sampling rate of 20 MHz.
  - while maintaining the 20 MHz. clock rate, the number of sampling pulses could be reduced to seven without the occurrence of errors.
  - during further trials at a 10 MHz. clock rate, the number of sampling pulses could be reduced to three without the occurrence of errors.
- Vary the clock speed and pulse duration of the low voltage test data applied to the sensor pad test port, while sampling the amplifier at rates which did not cause error in the previous examination.
  - the trial began using 1 kHz. clock rate and a 50 % duty cycle for the test data into the sensor pad test port.

- observe one of the N S E W output lines for errors during the pulse duration testing.
- increase the clock rate and vary the duty cycle of the sensor pad test data to create error free sampling of the biased amplifier.

- The results of the piezo film simulation, frequency and pulse width testing are as follows:
  - sensor pad test data was applied at frequencies up to 500 kHz. with a minimum duty cycle of 75 % which means that the piezo film generator voltage must be valid for at minimum 1.5 µs.
  - sampling of the sensor test voltage could be done at 2 MHz. taking three samples per test pulse.
  - at a higher sampling frequency of 5 MHz., eight samples per test pulse were required for error free operation.

TEST 4. Biased Inverter Amplifier Threshold Test

IC Pin	Pin Designation	Connected To
28	Ground	IC Breadboard Ground
29	+ 5 V.	IC Breadboard Power
18	Pad Data In	Port 0 0 Data Gen
1 or 20	Sample Clock	Port 0 1 Data Gen
10 or 31	Clock 2	Port 0 2 Data Gen
39	E Out	Port 0 0 Data Anal

Table. B.3. Biased Inverter Amplifier Threshold Test Wiring.

- Examine the threshold voltages required to fire and reset the biased inverter amplifier. Verify also the upper clock frequency at which these voltages can be pulsed without errors in the operation.
- Apply small voltage increments to the sensor pad test pin and observe the operation of the amplifier by monitoring the E_out output pin. Due to restrictions inherent in the Data Generator, a voltage pulse generated must have at minimum a .5 volt difference between the upper and lower voltage extremes.
  - when the applied test data is in the low state the amplifier must put out a logical 0 value.
  - when the applied test data is in the high state the amplifier must put out a logical 1 value.
- The results of the biased inverter amplifier threshold testing are as follows:
  - the amplifier when sitting at the bias point of 2.7 volts was correctly found in the low output state in all one pixel ICs.
  - an incremental application of .2 volts triggered the amplifier to the high output state. The pad voltage monitored with an oscilloscope was 2.9 volts.
  - a decremental application of .3 volts reset the amplifier to the low output state. The pad voltage monitored with an oscilloscope was 2.4 volts.

- due to loading between the biased sensor pad and the Data Generator output line, the applied test pulse had an upper threshold of 1.2 volts which created the pad voltage of 2.9 volts, and a lower threshold of .7 volts which created the pad voltage of 2.4 volts.
- the application of this minimum value sensor pad test data could be generated at 500 kHz. without the occurrence of error.

TEST 5. Nine Pixel Serial Shift Test

IC Pin	Pin Designation	Connected To
26	Ground	IC Breadboard Ground
27	+ 5 V.	IC Breadboard Power
3	Data In	Port 0 0 Data Gen
10	P/S_Con	Port 0 1 Data Gen
11	Clock 3	Port 0 2 Data Gen
39	Data Out	Port 0 0 Data Anal

Table. B.4. Nine Pixel Serial Shift Test Wiring.

- Verify the operation of the nine pixel serial shifting routine.
- Toggle Clock 3.
- Apply test data to the Data In port.
- Monitor the Data Out port.
- Hold the p/s_con line high so that the chain of nine shift registers are in the serial shifting mode.

- test data monitored at the Data Out port should equal that data applied to the Data In port.

- The results of the nine pixel serial shift testing are as follows:
  - the output correctly tracked the input after a nine clock period delay.
  - it was observed that input data must be valid on the leading edge of the Clock 3 pulse for proper operation.
  - the serial shifting operation was successful to a clock rate of 10 MHz.

TEST 6. Nine Pixel Complete System Operation Test

IC Pin	Pin Designation	Connected To
26	Ground	IC Breadboard Ground
27	+ 5 V.	IC Breadboard Power
19	Pad Data In	Port 0 0 Data Gen
10	P/S_Con	Port 1 1 Data Gen
22	Sample Clock	Port 0 1 Data Gen
21	Clock 1	Port 0 3 Data Gen
9	Clock 2	Port 0 2 Data Gen
11	Clock 3	Port 1 0 Data Gen
39	Data Out	Port 0 0 Data Anal

Table. B.5. Nine Pixel Complete System Operation Test Wiring.

- Examine the complete operation of the nine pixel IC with pixel pressure data simulated through test pins.
- Verify the complete operation of the nine pixel IC. This entails the sampling, edge detection, parallel loading, and serial shifting, while observing the Data Out port for the appearance of edge point test data applied to the left center pixel.
- The left center pixel is chosen because test pins were provided to that pixel to enable the input of sensor pad data.
- Toggle Clock 3 to employ serial shifting.
- Apply test data to the Data In port.
- Monitor the Data Out port.
- Hold the p/s_con line high so that the chain of nine shift registers are in the serial shifting mode.
- Interrupt the serial shifting routine and perform the sampling, the edge detection, and parallel loading according to the timing diagram in Fig. 4.5. During the sampling, simulate edge data for the left center pixel.
- Resume the serial shifting routine after parallel loading, and observe that data from the fourth pixel signals the occurrence of an edge point.
  - while serial shifting is operating, test data monitored at the Data Out port should equal that data applied to the Data In port.

- after parallel loading and the resumption of serial shifting, the first three bits of data to appear at the Data Out port should be zero, followed by one data bit of one, followed by five data bits of zero, then the output should again track the input data applied at the Data In port.

- The results of the complete nine pixel IC testing are as follows:
  - the output correctly tracked the input after a nine clock period delay during serial shifting.
  - after the parallel loading interruption, the edge data which was applied to the fourth pixel in the nine pixel chain appeared in its correct position, preceded by three zeroes and followed by five zeroes.
  - after resumption of the serial shifting and the output of the locally generated data, the output correctly tracked the input data.
  - the complete system operation was successful to a clock rate of 2 MHz. limited only by the sampling procedure required to read the test data applied to the test sensor pad.

TEST 7.

- Examine the complete operation of the nine pixel IC with pixel pressure data simulated with test probes.

- This series of tests was done in a manner exactly like the previous test, but with a test probe making direct contact with a sensor pad in order to simulate sensor pad pressure data. Each pixel was examined in this way to verify the correct operation of all nine pixels in the sensor array.
- The test routine was carried out and monitoring of the Data Out port enabled the observation of the data generated locally, internal to the IC, preceded and followed by the input data applied to the input port. In each of nine trials the output data generated after the parallel loading should have an edge data value observed in the corresponding location according to the pixel that the test probe is connected to. The edge data bit in each case should be preceded and followed by the appropriate number of zeroes to indicate the absence of pressure data at the remaining pixels.
- The results of the complete nine pixel IC testing with pad data applied through a probe are as follows:
  - the output correctly tracked the input after a nine clock period delay during serial shifting.
  - in each case after the parallel loading interruption, the edge data which was applied by the test probe in the nine pixel chain appeared in its correct position, preceded by the appropriate number of zeroes and followed by the appropriate number of zeroes.

- after resumption of the serial shifting and the output of the locally generated data, the output correctly tracked the input data.
- the complete system operation was successful to a clock rate of 2 MHz. limited only by the sampling procedure required to read the pressure data applied by the probe to the test sensor pad.

TEST 8.

- Examine the operation of the nine pixel IC while simulating adjacently placed ICs by generating data which would originate from all sides of of the nine pixel array. This procedure will simulate how the nine pixel IC would operate as an element of a larger sensor array.
- Create several test vectors for the N S E W input lines to simulate certain pixels as edge points. In the nine pixel IC, a test pin was provided for each pixel allowing adjacent IC input to be applied. There are three N S E W input lines available for a total of twelve input lines to be used in simulating adjacently placed ICs. Program these designed vectors into the Data Generator. The wiring of these input lines is shown in Table B.6.

IC Pin	Pin Designation	Connected To
12	TL S_in	Port 1 2 Data Gen
6	TC S_in	Port 1 3 Data Gen
8	TR S_in	Port 2 0 Data Gen
2	RT W_in	Port 2 1 Data Gen
37	RC W_in	Port 2 2 Data Gen
38	RB W_in	Port 2 3 Data Gen
28	BL N_in	Port 3 0 Data Gen
34	BC N_in	Port 3 1 Data Gen
33	BR N_in	Port 3 2 Data Gen
20	LT E_in	Port 3 3 Data Gen
25	LC E_in	Avail Port Data Gen
23	LB E_in	Avail Port Data Gen

T = Top B = Bottom L = Left R = Right C = Center

Table. B.6. Adjacent IC Simulation Test Vector Wiring.

- This stage of the complete nine pixel IC operational testing is similar to the previous two stages but with more detailed local edge data created. Local pressure data applied to the pixels was provided through test pins and test probes. All nine pixels were examined for correct performance characteristics.
- Toggle Clock 3 to initialize and employ serial shifting.

- Hold the p/s_con line high so that the chain of nine shift registers are in the serial shifting mode.
- Apply random test data to the Data In port.
- Monitor the Data Out port.
- Interrupt the serial shifting routine by resetting the p/s_con line low and perform the sampling, the edge detection, and parallel loading according to the timing diagram in Fig. 4.5. During the sampling, apply certain programmed test vectors and sensor pad pressure data to simulate edge points for specific pixels in the nine pixel array.
- Resume the serial shifting routine after parallel loading, and observe the locally generated data at the output port. Observe the specific positions in the output where logical 1 data values are expected to appear to correctly signal the occurrence of edge points.
  - while serial shifting is operating, random test data monitored at the Data Out port should equal that random data applied to the Data In port.
  - after parallel loading and the resumption of serial shifting, the monitoring of the Data Out port enabled the observation of the data generated locally, internal to the IC, preceded and followed by the input data applied to the input port. In each trial the local output data generated should have an edge data value observed in the

corresponding locations according to the pixels that the test pin and/or test probes are connected to, in conjunction with the programmed test vector applied to the nine pixel IC. After local data is received the output should again track the random input data applied at the Data In port.

- The results of the complete nine pixel IC testing with adjacent IC simulation, are as follows:
  - the output correctly tracked the random input after a nine clock period delay during serial shifting.
  - after the parallel loading interruption was terminated, the serial shifting was resumed. The simulated edge data which was created by the combination of the sensor pad test pin, the test probe and the adjacent IC vectors appeared in their respective positions in the nine pixel chain. These edge points were correctly observed in each trial, preceded by the appropriate number of zeroes and followed by the appropriate number of zeroes.
  - after the local data was received, the output correctly tracked the random input data.
  - the complete system operation was successful to a clock rate of 2 MHz. limited only by the sampling procedure required to read the test data applied to the various sensor pads.