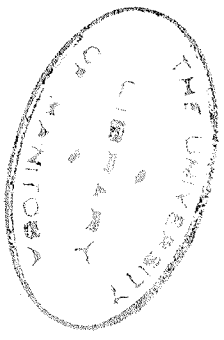
DEVELOPMENT OF A TRANSISTORIZED SINGLE CHANNEL PULSE HEIGHT ANALYZER

A Thesis Submitted to the
Department of Physics of the
University of Manitoba

In Partial Fulfillment
of the Requirements for the
Degree of Master of Science
in Engineering Physics



April 1, 1956

Submitted by:

O.C. Chaykowsky

PREFACE

In the few years since its invention, the transistor has become firmly established as a most important member of the rapidly increasing family of electronic devices. Even at present it is highly competitive and promises to surpass the vacuum tube in almost every field of electronics. Since 1948 when the original point-contact type was announced by Bell Telephone Laboratories, an intensive effort by the workers in the field has led to the development of many forms and shapes of transistors. Junction transistors, phototransistors, multi-electrode transistors, fieldistors, and transistors made from silicon have resulted and the field of application consequently has been broadened immensely.

This thesis is primarily concerned with the application of transistors to switching circuits and in particular the development of a transistorized single channel pulse height analyzer. In this field the point-contact transistor has no equal, primarily due to its inherent negative resistance characteristic and consequent greater than unity current gain. It exhibits extremely rapid switching action and can operate in the millimicrosecond region without the usual compensating circuitry required with vacuum tubes in that region. With the present rather heavy demands on subminiaturized electronic equipment, particularly in the field of computers, airborne radar and associated missile electronics, there is no doubt that in the very near future the tiny point-contact transistor will completely replace the vacuum tube in switching circuits.

The author wishes to extend his most sincere appreciation to Dr. K.I. Roulston, Department of Physics, University of Manitoba for his helpful suggestions, kind advice and interest on this project. The author also wishes to acknowledge with thanks the financial assistance received from the National Research Council of Canada, without whose co-operation this project would not have been possible.

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Winnipeg, Manitoba

April, 1956.

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ABSTRACT

A transistorized single channel pulse height analyzer has been developed and tested. The unit employs only three point-contact transistors and five crystal diodes greatly reducing space and power requirements associated with pulse height analyzers using vacuum tubes. Maximum regular counting rate is in excess of 500,000 per second, with the output pulse from the anticoincidence circuit of sufficient length to trigger the associated scaling circuit; about one microsecond long. Switching circuits which are used in this unit are discussed fully, both analytically from the equivalent circuit point of view, and practically from the experimental point of view. Time relationship problems arising from differences in triggering times of the upper and lower levels due to the finite rise time of the input pulse are also discussed. Finally, since stability of discrimination level, gate width and triggering level of the transistors are of extreme importance in pulse height analysis, considerable space is also devoted to this topic.

PART 1

INTRODUCTION

1.1 Pulse Amplitude Analysis

Any method of measuring a pulse amplitude spectrum resulting from random voltage pulses developed by a nuclear-radiation detector due to some nuclear process, has been found extremely useful by physicists in a great many nuclear experiments. This amplitude information is usually presented in the form of a pulse amplitude distribution curve.

(1, 2, 3.) If N(E), the number of pulses whose amplitude is greater than a particular voltage level E, is measured by some discriminating device and plotted as a function of E, an integral-bias curve is obtained as shown in Fig. 1.1

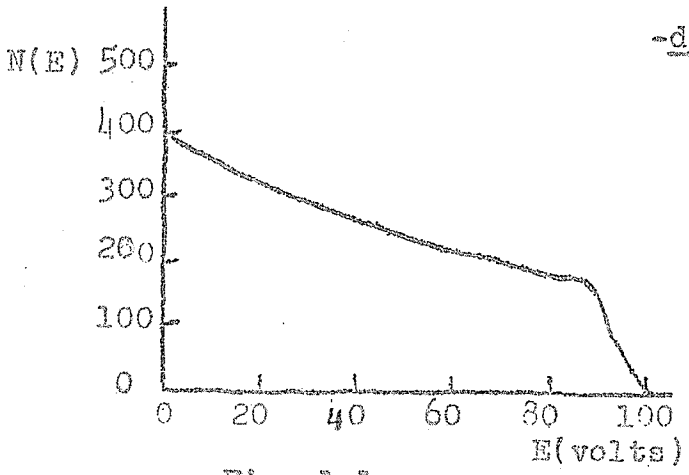

Fig. 1.1

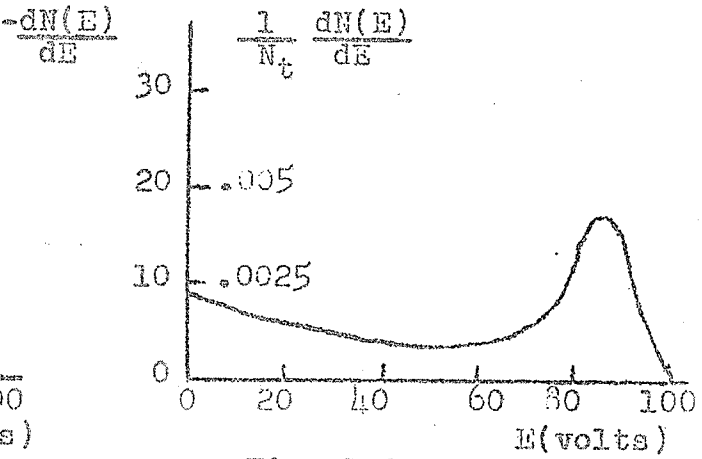

Fig. 1.2

If the negative derivative $\frac{-dN(E)}{dE}$ of the above function is plotted as a function of E, a so-called differential-bias curve is obtained giving the differential pulse-amplitude distribution curve, which determines the number of pulses lying within a unit channel width at a level E. (Fig. 1.2)

If $\frac{1}{N_t}\frac{dN(E)}{dE}$ is plotted versus E, then the fraction of pulses having amplitudes lying within a unit channel width at a level E can be determined. (Fig. 1.2) N_t is the value of N(E) at E = 0. Therefore we see that such a method can be employed by using an amplitude discriminator, and obtaining counts over a given time interval for various settings of the discriminator level.

The pulse amplitude distribution curve can never be a continuous curve since infinite data would be required; the actual representation of the results would be a histogram as shown in Fig. 1.3 which would approach a continuous curve if ΔE was made very small and a great many readings were taken.

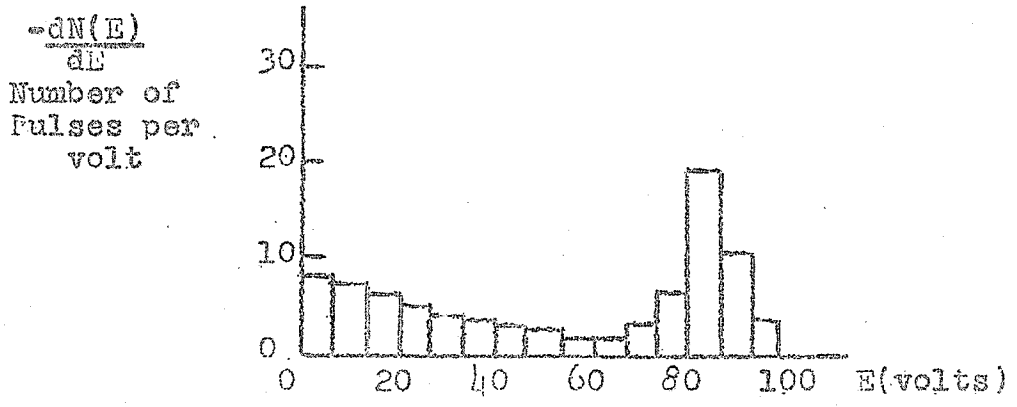

Fig. 1.3

The above means of obtaining a pulse-amplitude distribution curve is subject to considerable statistical error, because the process involves taking the difference between nearly equal statistically independent numbers, each of which is subject to a considerable statistical error in itself. It can be shown that a measurement of the average rate of events which occur randomly in time, obtained by counting the number of events N during an interval t has a probability 0.68 of lying

within the standard deviation range $(N_o - \sqrt{N_o}) < N < (N_o + \sqrt{N_o})$ where N_o is the "correct" answer --- provided N_o is sufficiently large so that the distribution can be assumed Gaussian. A measurement $N_1(E_1)$ thus is subject to an error whose standard deviation is approximately $\sqrt{N_1}$. A second measurement $N_2(E_1 + \Delta E) = N_2(E_2)$ has a standard deviation of approximately $\sqrt{N_2}$. Therefore the difference $\Delta N(E) = N_1 - N_2$ has a standard deviation $\sqrt{N_1 + N_2}$.

However, if direct measurements of those pulses with amplitude lying between E_1 and $E_2 = E_1 + \Delta E$ is made by means of a device having a window of amplitude acceptance rather than a threshold, the quantities N_1 and N_2 are not statistically independent and the standard deviation in the determination of $\Delta N = N_1 - N_2$ is merely $\sqrt{N_1 - N_2}$ (provided ΔN is adequately large). From these considerations we see the advantage of a device which automatically registers the number of pulses that pass through it in a channel width ΔE. Such a device is called a single channel pulse-amplitude analyzer or a single channel "kicksorter".

Two specific items of information must be determined in these units; (a) whether or not a specific input pulse has sufficient amplitude to cross the lower level and (b) whether or not the same specific input pulse has also crossed the upper level. The usual method employed in pulse-amplitude analyzers is for the unit to give an output pulse if and only if the lower level is crossed. If the upper level is also crossed, it produces a cancelling pulse which is used to suppress the lower level pulse, resulting in no output. Various time

relationship problems come into the design due to the finite rise time of the incoming pulse. This causes the upper level to trigger later than the lower level by a finite time Δt, which is dependent also upon the window width and discrimination level for any specific input pulse. Finally, the stability of window width and discrimination level is of utmost importance, and every design effort should be made to keep these within what is usually demanded for precision work; -- about one percent.

PART 2

TRANSISTOR SWITCHING CIRCUITS

2.1 Large-Signal Operation of Point-Contact Transistors

For large-signal operation the point-contact transistor is a highly non-linear device as can be seen by examining its static characteristic shown below in Fig. 2.1 and Fig. 2.4 Consider the circuit shown in Fig.2.3 with its performance governed by the load line drawn on the collector characteristics in Fig. 2.2. A negative input voltage causes a negative current to flow in the emitter circuit which offers a high resistance for negative currents and operation is limited to a very small region slightly to the left of the $i_e = 0$ curve and for all practical input voltages can be considered to remain almost stationary on the $i_e = 0$ curve. This region is known as the cutoff region.

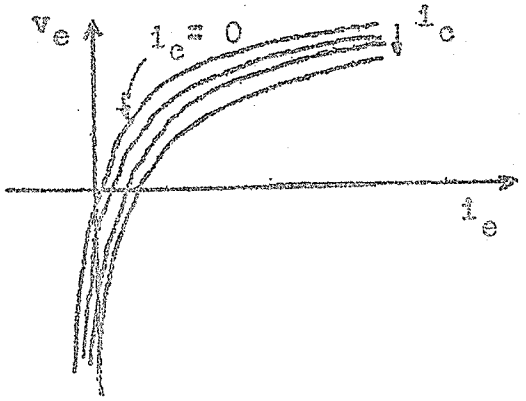

Fig. 2.1

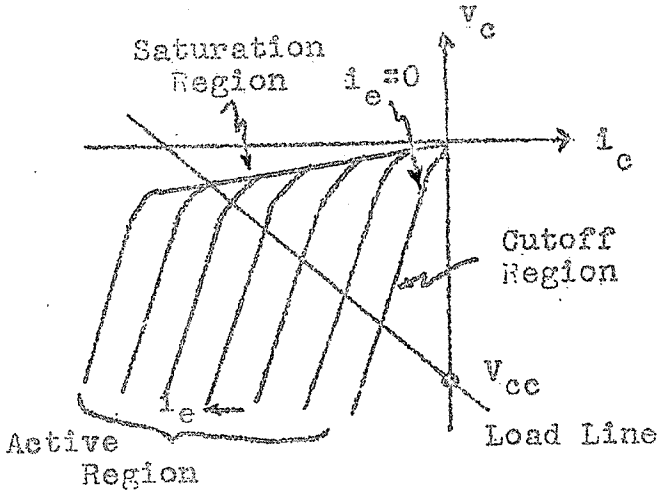

Fig. 2.2

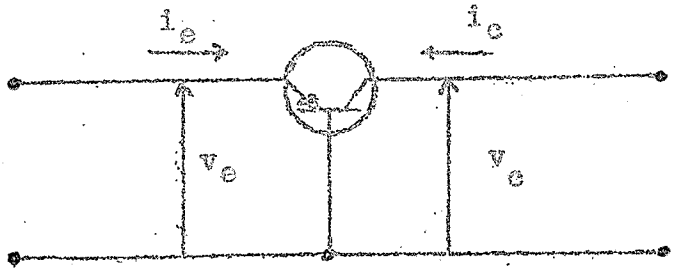

Fig. 2.3

For positive input voltage, i_e is greater than zero, and the collector current increases negatively with increase in emitter current; the transistor is said to be in its active region. When i_e becomes large enough, the operating point soon reaches the knee of the curve and further increase of i_e produces no further appreciable increase in i_c and the transistor is said to be in its saturation region.

In order to make the operating principles more readily understood, one can think of the transistor as being made up of two diodes.(an emitter to base diode, and a collector to base diode.) Equivalent circuit is shown in Fig. 2.4. For $i_e \leq 0$ (cutoff region) both diodes are operating in the reverse direction and the current generator in the collector arm is inactive. In the active region, for $i_e > 0$ and small , the collector diode is still biased in the reverse direction, while the emitter diode is conducting; the transistor acting like an active element. With further positive increase of i_e, the generator current $a'i_e$ becomes greater than the collector current and the collector-base diode closes with the result that the transistor enters the saturation region and both emitter and collector diode resistances are small; the collector resistance now shunting the generator and with a large load in the collector circuit, the transistor is again a passive element with low internal impedance.

The highly non-linear characteristics of the transistor make precise circuit analysis extremely difficult and usually the voltage-current relationships are represented by straight lines as with diodes; the slopes being the reverse and forward impedances of the diodes.

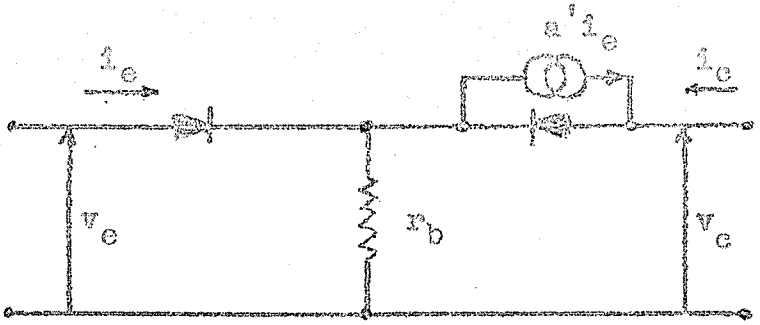

Fig. 2.4

We see therefore, that in order to utilize the small signal parameters and the small signal T equivalent circuit for large signal operation, it is necessary to assign one set of transistor parameters for each of the three regions and analyze each region separately.

2.2 Analysis of the Grounded Base Transistor Trigger Circuit

The equivalent T-network for a grounded base transistor can be set up as shown in Fig. 2.5

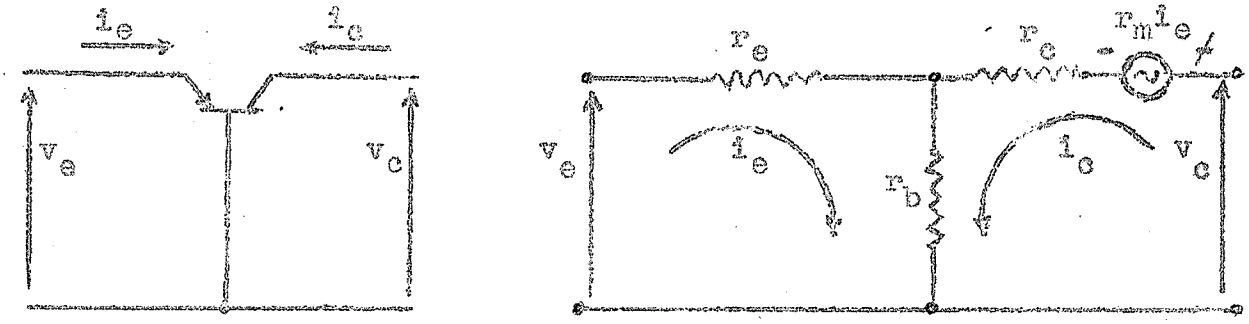

Fig. 2.5

$r_m i_e$ is a fictitious voltage generator that takes into account the current amplification properties of the transistor and transforms a passive T-network into an active transistor equivalent network. From four-pole network theory the equations for the above network can be set up as:

$$\begin{bmatrix} v_e \\ v_c \end{bmatrix} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix} \qquad (2.2.1.)$$

and substituting the respective parameters into the equation we get:

$$\begin{bmatrix} v_e \\ v_c \end{bmatrix} = \begin{bmatrix} r_e + r_b & r_b \\ r_m + r_b & r_b + r_c \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix} \qquad (2.2.2.)$$

For transistor trigger action the circuit must be loaded as shown in Fig. 2.6

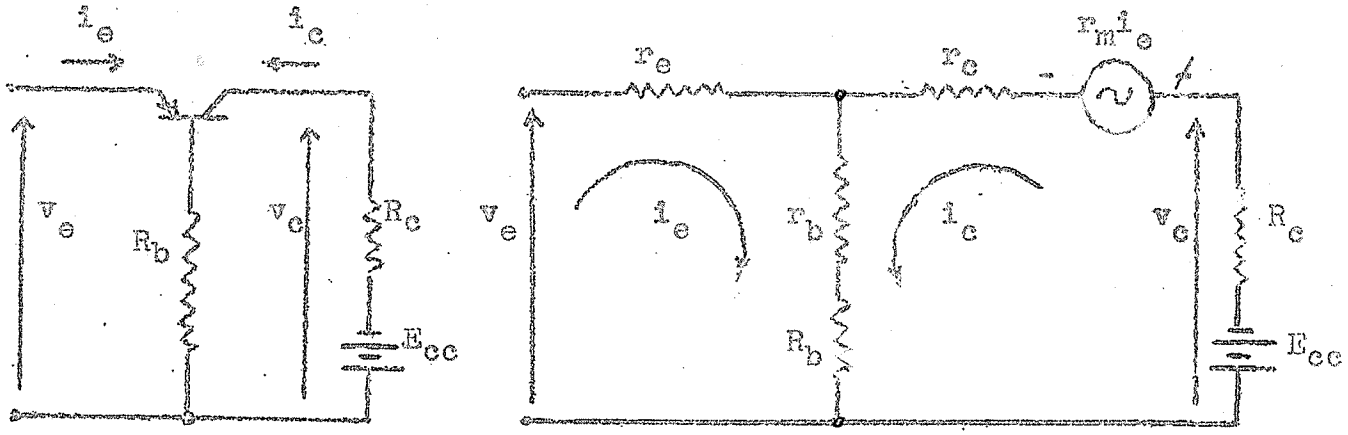

Fig. 2.6

The circuit equations are now given by:

$$\begin{bmatrix} v_e \\ v_c \end{bmatrix} = \begin{bmatrix} r_e + r_b + R_b & r_b + R_b \\ r_b + r_m + R_b & r_c + r_b + R_b \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix} \qquad (2.2.3.)$$

Also $$- E_{cc} = v_c + i_c R_c \qquad (2.2.4.)$$

To specify the performance of the circuit the emitter driving-point characteristic may be used most advantageously, and therefore it is desirable to obtain a relationship between v_e and i_e

If the expression for v_c from equation (2.2.3.) is substituted into equation (2.2.4.) the result is

$$- E_{cc} = i_e(r_b + r_m + R_b) + i_c (r_c + r_b + R_b + R_c) \qquad (2.2.5.)$$

Solving this for i_c and substituting back into equation (2.2.3.) one gets the desired expression for v_e as a function of i_e

$$v_e = i_e \left\{ r_e \not\parallel r_b \not\parallel R_b - \frac{(r_b \not\parallel R_b)(r_m \not\parallel r_b \not\parallel R_b)}{(r_b \not\parallel r_c \not\parallel R_b \not\parallel R_c)} \right\} - \frac{E_{cc}(r_b \not\parallel R_b)}{(r_b \not\parallel r_c \not\parallel R_b \not\parallel R_c)} \qquad (2.2.6.)$$

It is also very advantageous to obtain an expression for collector current i_c in terms of i_e termed the transfer characteristic. Rewriting equation (2.2.5.) we get:

$$i_c = - i_e \frac{(R_b \not\parallel r_m \not\parallel r_b)}{R_b \not\parallel r_b \not\parallel R_c \not\parallel r_c} - \frac{E_{cc}}{R_b \not\parallel r_b \not\parallel R_c \not\parallel r_c} \qquad (2.2.7.)$$

For circuit design purposes, the sectional linearization technique as outlined in section 2.1 may be adopted. The approximations that this method is based on are:

(1) R_b will be so chosen that it is much larger than r_b

(2) R_e in practice is always much larger than r_{ef} (The forward resistance of the emitter to base diode.)

(3) R_c in practice is always much larger than r_{cf} (The forward resistance of the collector to base diode.)

(4) r_m is assumed much larger than r_b ; r_c is assumed much larger than r_b ; and therefore $a = \frac{r_m \not\parallel r_b}{r_c \not\parallel r_b} \doteq r_m/r_c$ where a is the short circuit current amplification factor.

The three equivalent circuits for the transistor in each of the three regions are as shown in Fig. 2.7 (a) cutoff (b) active and (c) saturation.

If the above approximations are taken into account, equations (2.2.6.) and (2.2.7.) become:

$$v_e = i_e\left\{r_e \not\parallel R_b - \frac{R_b(r_m \not\parallel R_b)}{r_c \not\parallel R_b \not\parallel R_c}\right\} - \frac{E_{cc} R_b}{r_c \not\parallel R_b \not\parallel R_c} \qquad (2.2.8.)$$

$$i_c = -\frac{i_e(r_m \not\parallel R_b)}{r_c \not\parallel R_b \not\parallel R_c} - \frac{E_{cc}}{r_c \not\parallel R_b \not\parallel R_c} \qquad (2.2.9.)$$

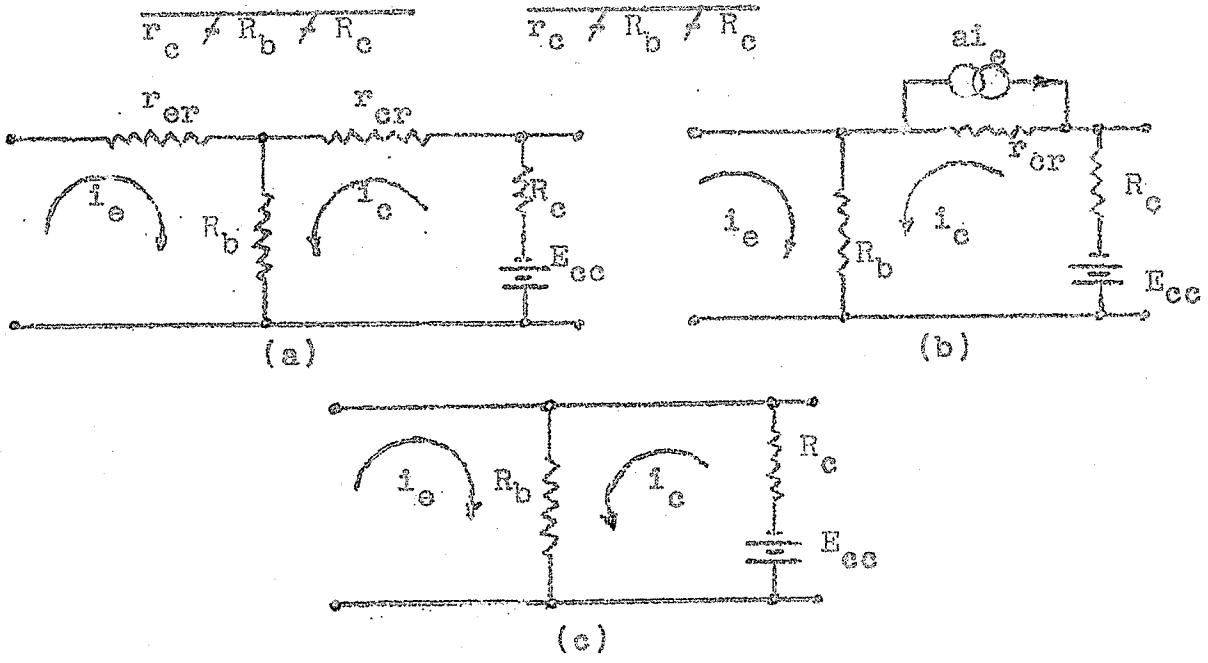

Fig. 2.7.

Note: Current generator ai_e in collector circuit in Fig. 2.7 (b) is absolutely equivalent to voltage generator $r_m i_e$ in Fig. 2.6.

(a) Cutoff Region : Both emitter-base and collector-base diodes are open, and the following conditions hold.

$r_e >> R_b$ and $a = 0$ ---- Imposing conditions yields

$$v_e = i_e r_e - \frac{R_b E_{cc}}{r_c \not\parallel R_b \not\parallel R_c} \qquad (2.2.10.)$$

$$i_c = -\frac{R_b i_e}{r_c \not\parallel R_b \not\parallel R_c} - \frac{E_{cc}}{r_c \not\parallel R_b \not\parallel R_c} \qquad (2.2.11.)$$

(b) Active Region : The transistor is an active network characterized by the current generator across r_c. The collector to base diode is still open but the emitter-base diode is conducting. Condition in this region is that $r_e << R_b$ and imposing this condition leads to

$$v_e = \frac{R_b\{R_c + r_c(1-a)\}}{R_b + r_c + R_c} i_e - \frac{E_{cc}R_b}{R_b + r_c + R_c} \qquad (2.2.12)$$

$$i_c = \frac{-(R_b + ar_c)i_e}{R_b + R_c + r_c} - \frac{E_{cc}}{R_b + R_c + r_c} \qquad (2.2.13)$$

Note that if R_c is less than $r_c(a-1)$ a negative emitter input resistance is obtained, and it is upon this principle that a point-contact transistor switching circuit operates.

(c) Saturation Region : Both emitter-base and collector-base diodes are conducting and the transistor once again becomes a passive network. The conditions to be imposed in this region are: $r_e << R_b$; $r_c << R_b$; $a \neq 0$. Therefore

$$v_e = \frac{R_bR_ci_e}{R_b + R_c} - \frac{R_bE_{cc}}{R_b + R_c} \qquad (2.2.14)$$

$$i_c = \frac{-R_bi_e}{R_b + R_c} - \frac{E_{cc}}{R_b + R_c} \qquad (2.2.15)$$

The preceeding equations may be solved for the points of intersection of the transition and saturation regions and the transition and cutoff regions.

P_1 $\quad i_e = 0 \qquad v_e = -\frac{R_bE_{cc}}{R_b + R_c + r_c}$ (2.2.16)

Q_1 $\quad i_e = 0 \qquad i_c = \frac{-E_{cc}}{R_b + R_c + r_c}$ (2.2.17)

P_2 $\quad i_e = \frac{E_{cc}}{a(R_b + R_c) - R_b} \qquad v_e = \frac{R_b(1-a)E_{cc}}{a(R_b + R_c) - R_b}$ (2.2.18)

Q_2 $\quad i_e = \frac{E_{cc}}{a(R_b + R_c) - R_b} \qquad i_c = \frac{-aE_{cc}}{a(R_b + R_c) - R_b}$ (2.2.19)

The calculated characteristics based upon the simplified analysis, and the characteristics obtained experimentally for two Northern Electric 2N22 point-contact transistors are shown in Figs. 2.8 and 2.9 . The theoretical characteristics were computed from typical values quoted by Northern Electric on their specification charts. For large pulse operation, where one is not too concerned about the exact position of the turnover points, design proceedure for any N.E. 2N22 type of transistor can be performed from the theoretically determined curves. However for accurate work, where one is triggering the circuit with small pulses, it can be seen that the experimental curves must be used and each circuit designed for the particular transistor under consideration. It was felt that this latter proceedure was necessary for this project.

Northern Electric type 2N22 were chosen as the type to be used primarily due to results of reliability tests performed by C.D. Florida[4] on various point-contact transistors, and because the 2N22 exhibited a fairly pronounced negative resistance characteristic with less fluctuations in triggering level than any other type tested in this investigation. (In this investigation, Northern Electric 2N24 and General Electric G-11 were also tested.) The two features mentioned above, while both highly desirable, are,however,obtained by directly opposite conditions and a good compromise is difficult to establish; (for good stability---R_b must be as small as possible; for a pronounced negative reistance region---R_b must be as large as possible.)

The two transistors displayed, W-57 and V-24 were chosen

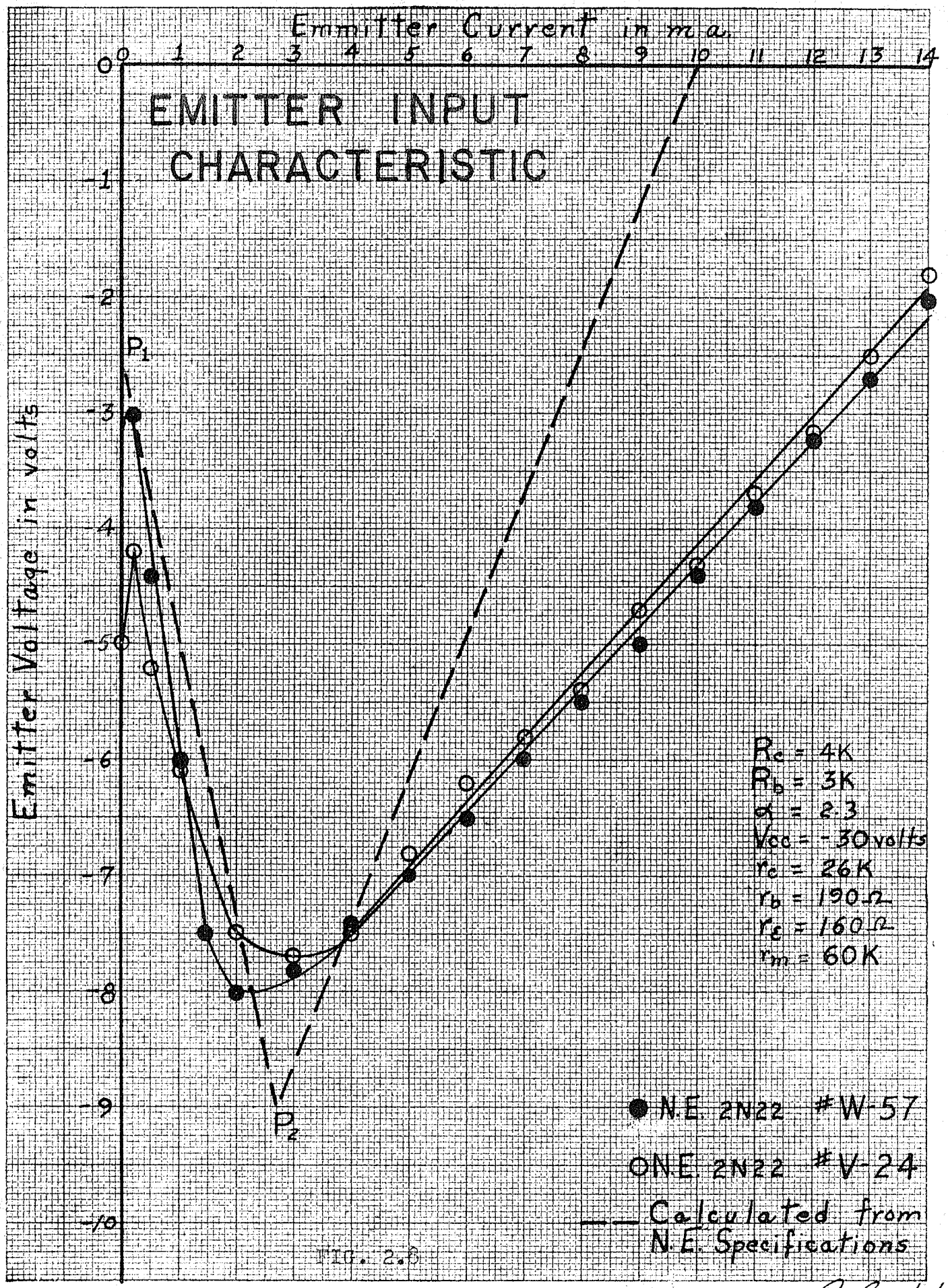

FIG. 2.8

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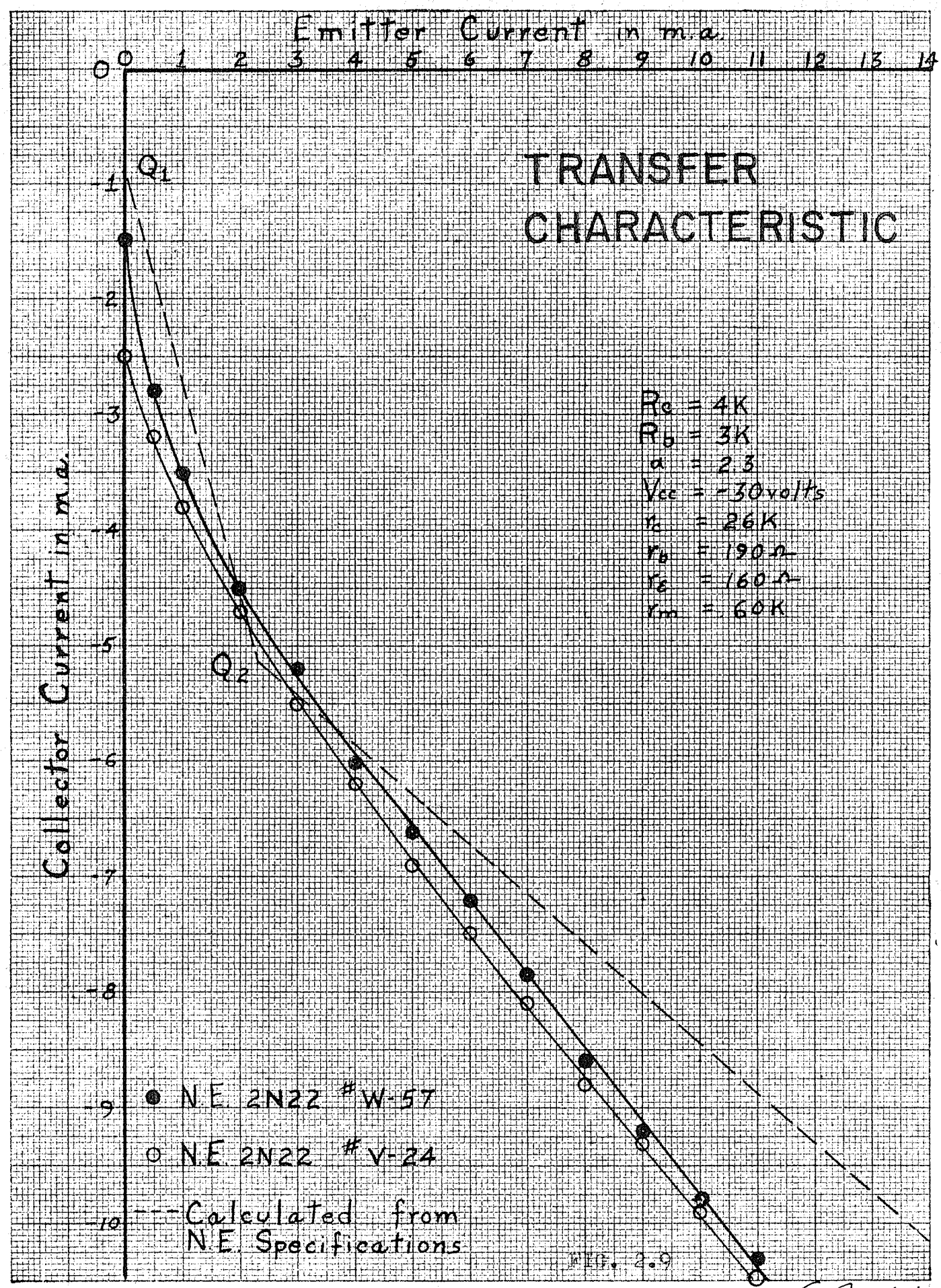


E.C. 4/1/55

for the trigger circuits from a batch of about twenty 2N22 type transistors. A characteristic curve was drawn up for each one and the stability of their triggering levels carefully investigated. W-57 and V-24 had characteristic curves which agreed fairly well with the theoretical curves, but the most important feature was that their fluctuations in triggering level were less than any other transistor of that type available. A further detailed discussion of stability will be given in a later section.

2.3 A Basic Monostable Transistor Trigger Circuit.

By proper choice of external loads, a negative resistance region is exhibited by a point-contact transistor. Various types of trigger circuits can be obtained by merely varying some of the external parameters. The bistable and astable trigger circuits were not used in this unit and therefore will not be discussed to any great extent. However a detailed discussion of the monostable trigger circuit will be extremely rewarding when the final assembled unit is to be analyzed, since the monostable triggering principle is involved throughout.

The basic monostable trigger circuit with its associated emitter input characteristic and transfer characteristic is shown in Fig. 2.10 The negative resistance region of the v_e vs i_e curve begins slightly to the right of the v_e axis.

In the quiescent state the capacitor C is fully charged and is effectively an open circuit. The operating point is therefore at M_1 , the d.c. load line being vertical. When a positive emitter voltage pulse sends into the emitter a positive

current greater than I_1, the circuit passes into its unstable negative resistance region. This voltage pulse must necessarily be of amplitude greater than v_t obviously.

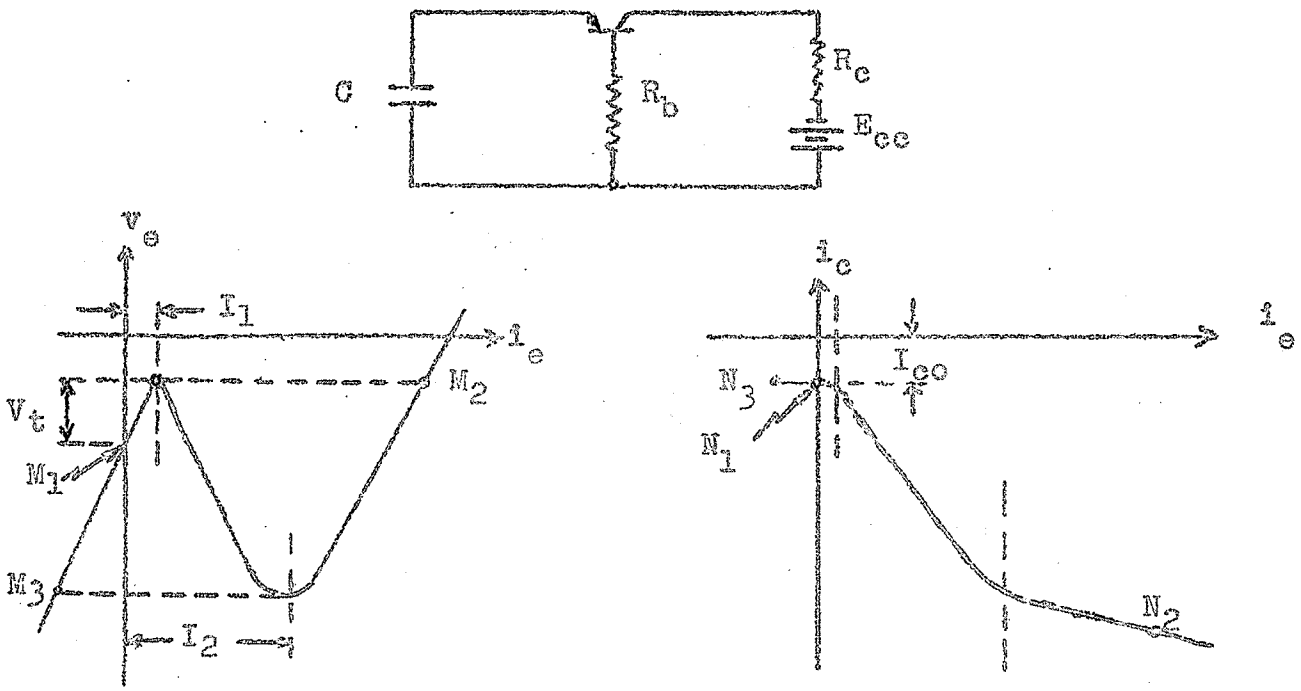


Fig. 2.10.

Because of the current amplification within the transistor and the positive feedback action afforded by the base resistance, the emitter and collector currents increase rapidly, and since the voltage across the condenser cannot change instantaneously the operating point will shift to the saturation region at constant voltage to point M_2. Now the capacitor is being charged in an opposite polarity to that of its quiescent state, and the operating point moves along the saturation curve until it reaches the valley point. When the unstable negative resistance region is again entered, the effect of diminishing emitter current and storing action of the capacitor is to shift the operating point at constant voltage to the cutoff region at M_3. The capacitor now discharges through the

reverse resistance of the emitter diode and the circuit returns to its original position M_1, and now is ready to repeat the cycle upon application of another trigger pulse.

The equivalent switching action circuits are shown in Fig. 2.11. (a) Equivalent circuit illustrating the trigger action (b) effect of closing switch (c) effect of opening switch.

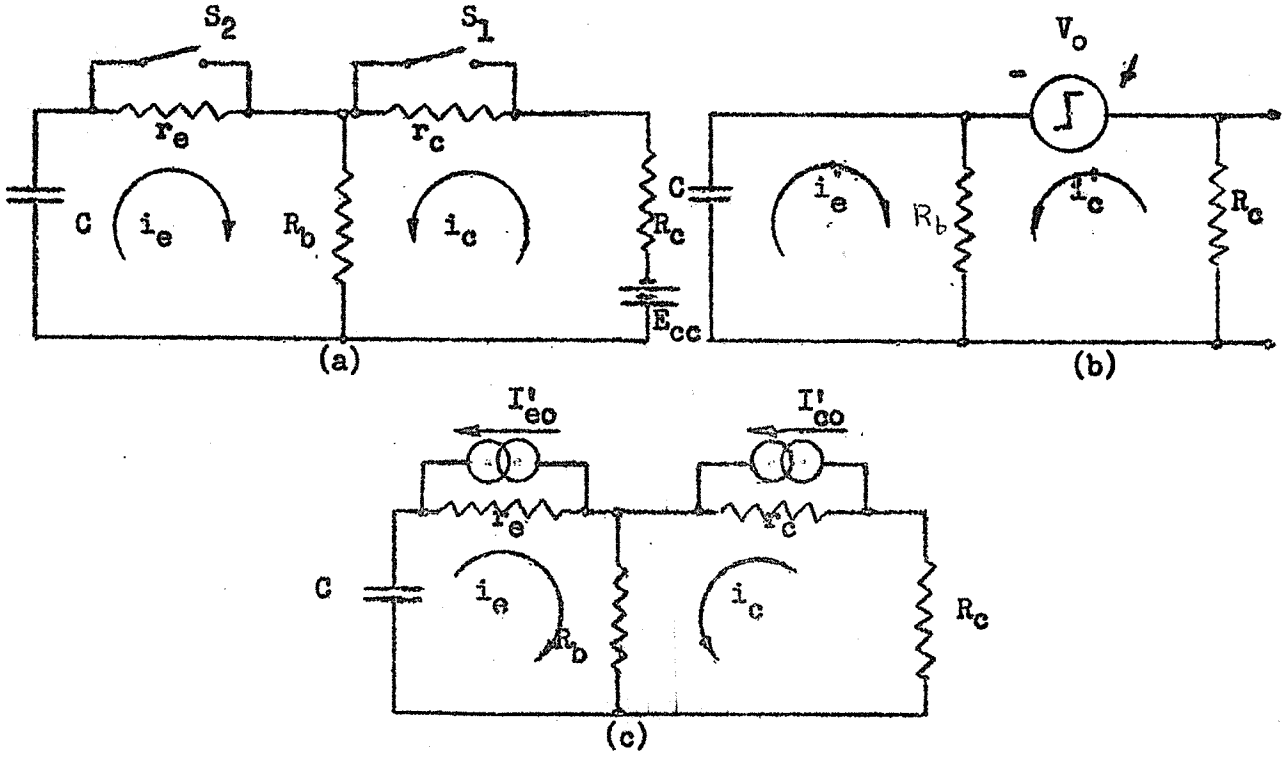


Fig. 2.11

Quiescently, with both S_1 and S_2 open, the currents in the emitter and collector loops are respectively

$$i_{eo} = 0 \qquad i_{co} = \frac{E_{cc}}{R_b \nparallel R_c \nparallel r_c} \tag{2.3.1}$$

At t = 0 both Switches are closed. Effect of closing switches is illustrated in Fig. 2.11 (b). V_o is a fictitious voltage source resulting from short-circuiting the quiescent voltage drop across r_c when S_1 is closed.

$$V_o = \frac{r_c E_{cc}}{R_b \nparallel R_c \nparallel r_c} \tag{2.3.2}$$

Loop Equations are:

$$0 = \frac{1}{C}\int i_e' \, dt + R_b i_e' + R_b i_c' \qquad (2.3.3.)$$

$$V_o = -R_b i_e' - (R_b + R_c) i_c' \qquad (2.3.4.)$$

Solving we get

$$i_e' = \frac{V_o}{R_c} \exp. -t/R_{11}C \qquad (2.3.5.)$$

$$i_c' = -\frac{V_o}{R_b R_c} R_{11} (1 - \exp^{-t/R_{11}C}) + \frac{V_o}{R_c} \exp^{-t/R_{11}C} \qquad (2.3.6.)$$

Where $R_{11} = \dfrac{R_b R_c}{R_b + R_c}$

Now taking into consideration the initial currents i_{eo} and i_{co} the total currents are:

$$i_e = i_e' + i_{eo} = \frac{V_o}{R_c} \exp. -t/R_{11}C \qquad (2.3.7.)$$

$$i_c = i_c' + i_{co} = \frac{-R_b V_o}{R_c(R_b + R_c)} \exp.^{-t/R_{11}C} - \frac{E_{cc}}{R_b + R_c} \qquad (2.3.8.)$$

The emitter current jumps from zero to V_o/R_c on the initiation of a triggering pulse and then decreases exponentially until i_e falls to I_2; the circuit then triggering back to low conduction. I_2 is given by (2.2.18.) as

$$I_2 = \frac{E_{cc}}{a(R_b + R_c) - R_b} \qquad (2.3.9.)$$

The second trigger action is equivalent to opening switches S_1 and S_2 at $t = T$, i.e. when i_e reaches I_2. This time T is given by

$$T = R_{11}C \ln \frac{r_c\{a(R_b + R_c) - R_b\}}{(R_b + R_c + r_c) R_c} \qquad (2.3.10.)$$

Currents i_e and i_c for $t > T$ may be calculated from considerations of opening switches S_1 and S_2 at $t = T$. This is equivalent to inserting fictitious current sources I_{eo}' and I_{co}' as shown in Fig. 2.11 (c).

$$I'_{eo} = \frac{V_o}{R_e} \exp.^{-(T+U)/R_{11}C} \qquad (2.3.11.$$

$$I'_{eo} = \frac{R_b V_o}{R_e(R_b+R_e)} \exp.^{-(T+U)/R_{11}C} - \frac{E_{cc}}{R_b+R_e} \qquad (2.3.12.$$

where $U = t - T$

The expressions for $t > T$ can be calculated in a similar manner but a qualitative analysis to a good approximation shows that the current waveforms return to their quiescent value almost instantaneously at $t = T$ except for the emitter current going very slightly negative due to the discharge current of the capacitor in the emitter circuit. The voltage across the capacitor however does not return to its quiescent state instantly at $t = T$ since the charge on it accumulated during the interval $0 < t < T$ must discharge through the high emitter back resistance. Analytically the voltage across the capacitor is:

$$v_e = \frac{-E_{cc}}{(R_b+R_c+r_e)} \qquad \text{for } t<0 \qquad (2.3.13.)$$

$$v_e = \frac{-R_b E_{cc}}{R_b+R_c} + \frac{R_b V_o}{R_b+R_c} \exp.^{-t/R_{11}C} \qquad \text{for } 0<t<T \qquad (2.3.14.)$$

$$v_e = \frac{-R_b E_{cc}}{R_b+R_c+r_c} + \left\{\frac{R_b(1-a)E_{cc}}{a(R_b+R_c)-R_b} + \frac{R_b E_{cc}}{R_b+R_c+r_c}\right\} \exp.^{-(t-T)/r_e C}$$

$$\text{for } T<t \qquad (2.3.15.)$$

The waveforms are shown in Fig. 2.12.

A graphical method of analysis utilizing the emitter input characteristic and the transfer characteristic may also be carried out assuming sectional linearization of the characteristics, and this method, although not quite as accurate as the analytical method is considerably simpler and gives good results especially if an experimental characteristic is used for each transistor being analyzed. The graphical method was used throughout this thesis for computing output pulse data from the various trigger circuits.

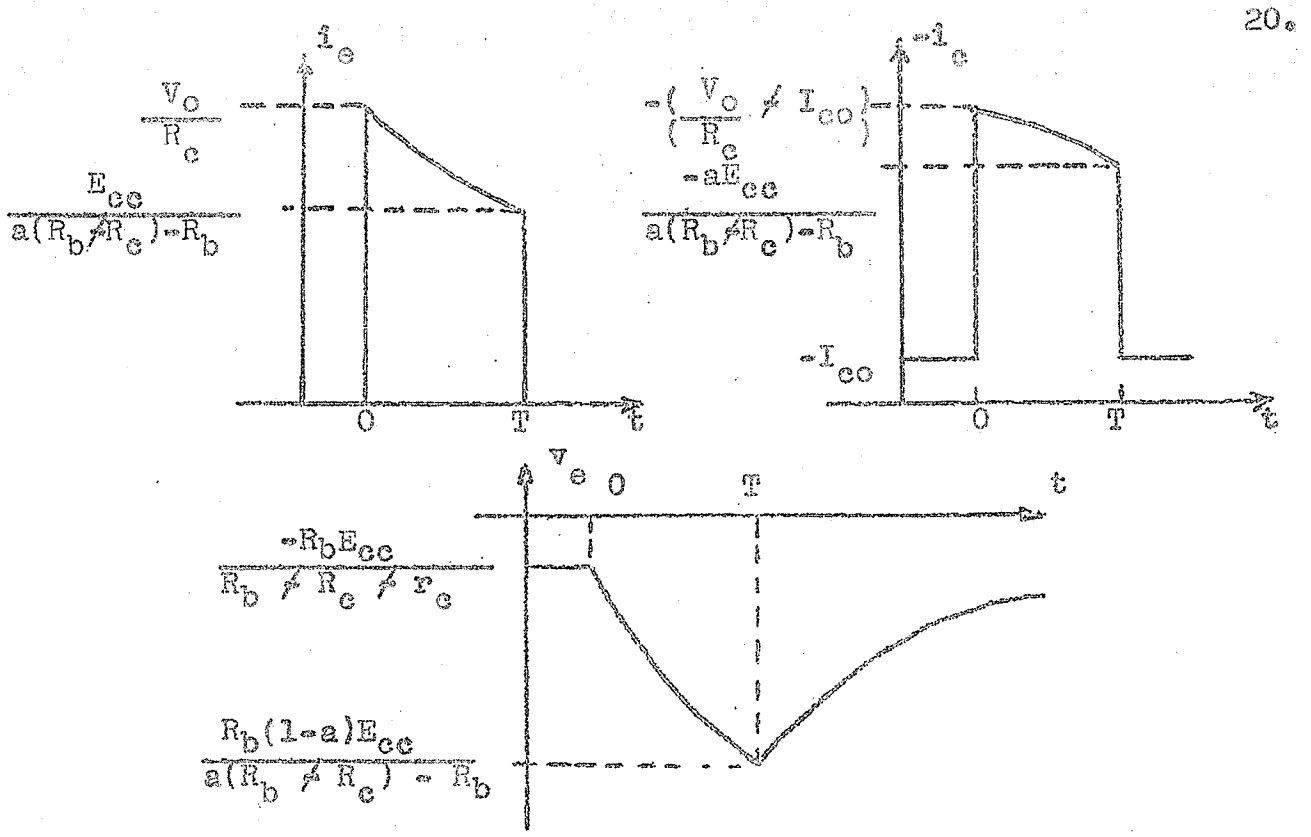


Fig. 2.12.

Consider Fig. 2.13 below

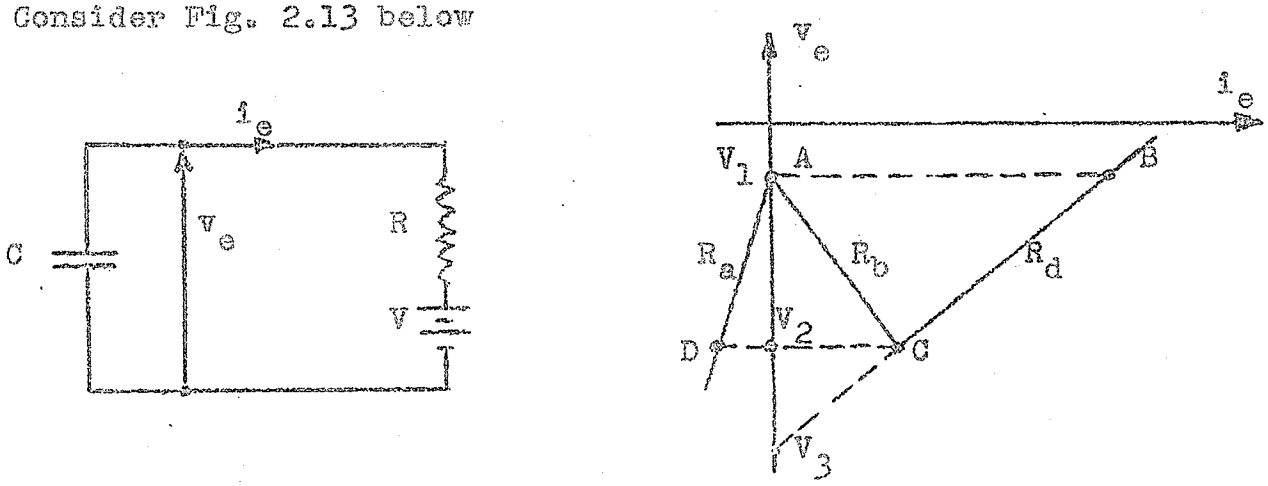


Fig. 2.13.

The two-terminal network defined by the v_e-i_e characteristic may be adequately represented by a resistance R in series with a direct voltage source V. R_a, R_b, R_d are the slopes of the linearized v_e-i_e curve and V_1, V_2 and V_3 the three associated voltages as shown above. The general expression for v_e and i_e are:

$$i_e = \frac{V_{eo}-V}{R}\ \exp.^{-t/RC} \qquad v_e = (V_{eo}-V)\exp.^{-t/RC} + V \qquad (2.3.14.)$$

where V_{eo} is the initial voltage across the condenser.

Operation may be summarized in the following manner

Time	Region	R	V
$t<0$	I	R_a	V_1
$t=0$	II	R_b	V_1
$0<t<T$	III	R_d	V_3
$t=T$	II	R_b	V_1
$T<t$	I	R_a	V_1

Therefore ;

$$i_e = 0 \quad \text{for } t<0 \qquad (2.3.15.)$$

$$i_e = \frac{V_1 - V_3}{R_e}\ \exp.^{-t/R_dC} \quad \text{for } 0<t<T \qquad (2.3.16.)$$

$$i_e = \frac{V_2 - V_1}{R_a}\ \exp.^{-(t-T)/R_aC} \quad \text{for } T<t \qquad (2.3.17.)$$

$$v_e = V_1 \quad \text{for } t<0 \qquad (2.3.18.)$$

$$v_e = (V_1 - V_3)\exp.^{-t/R_dC} + V_3 \quad \text{for } 0<t<T \qquad (2.3.19.)$$

$$v_e = (V_2 - V_1)\exp.^{(-t+T)/R_aC} + V_1 \quad \text{for } T<t \qquad (2.3.20.)$$

Set $v_e = V_2$ in Equation (2.3.14.)

$$T = \frac{1}{R_dC}\ln\frac{V_1 - V_3}{V_2 - V_3} \qquad (2.3.21.)$$

Similarly for i_c

$$i_c = I_{co} \quad \text{for } t<0$$

$$i_c = I_1 + K_d i_e \quad \text{for } 0<t<T \qquad (2.3.22.)$$

$$i_c = I_{co} \quad \text{for } t>T$$

where K_d is the slope of the transfer characteristic in region III.

PART 3

DESIGN AND TESTING OF THE SINGLE CHANNEL PULSE-HEIGHT ANALYZER.

3.1 A Practical Monostable Trigger Circuit

A practical monostable transistor trigger circuit due to A.W. Lo[5,6] is shown in Fig. 3.1 for both negative and positive input pulses, and in essence was the type used in this unit. Both circuits can be analyzed from the emitter input characteristic since a negative pulse on the base is equivalent to driving the emitter positive with respect to the base.

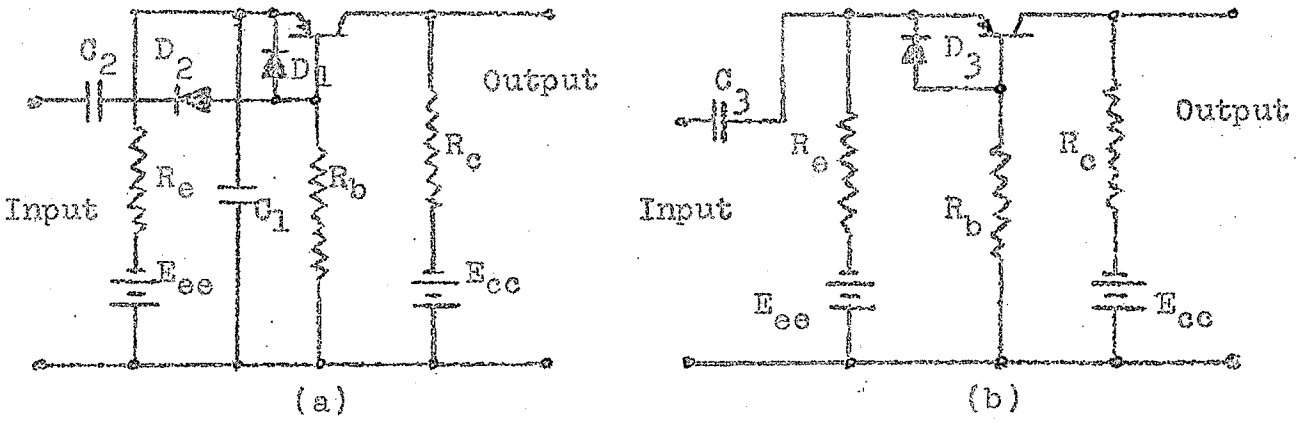


Fig. 3.1.

In Fig. 3.1 (b), a positive pulse applied to the emitter initiates trigger action. Capacitor C_3 acts as both the coupling capacitor for the input pulse and the feedback element for the trigger circuit. In this investigation it was determined that this " double duty" performed by capacitor C_3 slowed up the recovery time of the circuit (b) as compared to the same circuit (a). Using the same physical parameters and transistor the two circuits were compared for several operating features. Their performances were almost identical except for the difference in recovery times. The circuit as in Fig. 3.1.(b)

had a minimum recovery time of 1.2 u secs. with the output pulse 0.4 u secs. long. The circuit in Fig. 3.1.(a) had a minimum recovery time of 0.8 u secs. with the same output pulse length as stated above. It was therefore decided to use the negative input circuit wherever possible.

If we examine equation (2.3.10.) for T_1 we see that if the other external parameters involved are chosen and kept fixed, our choice of C_3 will determine the output pulse length. Since the other external parameters are usually chosen for correct operating conditions, stability etc. and are usually fixed, C_3 and C_3 alone can be used to control the output pulse length. (provided of course the internal parameters do not change due to temperature changes.)

In Fig. 3.1.(a) diode D_2 insures that the trigger circuit is isolated from the source except for the short time that the pulse is passing through. C_1 acts as the feedback element and controls the output pulse in this circuit.

It was shown in Section 2.3 that after the circuit triggers from its saturation state to its cutoff state, the capacitor C_1 starts to discharge through the high internal emitter resistance r_e: in this case it is actually $r_e \not / r_b \not / R_b$ in parallel with R_e. Since R_e is of the order of 20K in one of the trigger circuits this causes the emitter voltage to rise exponentially to its quiescent value rather slowly. This discharge time limits the repetition frequency at which the circuit can operate. To reduce the discharge time a second diode (D_1 and D_3) is placed between emitter and base to provide a low impedance path for the discharge of the capacitor. It now discharges through the forward impedance of the diode $\not / R_b$ in parallel with $r_e \not / r_b$, in parallel with

R_e. This is of the order of R_b ∴ forward resistance of the diode and could be as much as one tenth of the value of discharge resistance without the recovery diode. Using the above arrangement recovery times were improved 400 % over those obtained without the diodes, and up to a minimum of 0.8 u secs with a 0.4 u sec output pulse length. This is by no means the absolute minimum a transistor can be pushed to, but was the minimum obtainable with the pulse generator used due to violation of conditions (1) and (2) on the following page if attempts were made to reduce the recovery time any further.

It might be mentioned that the external emitter load R_e and emitter supply E_{ee} are not really necessary for monostable operation as has been shown when the basic monostable circuit was considered. They were added in this unit in order to obtain a control on the voltage required to trigger the circuit. Without R_e and E_{ee} the d.c. load line is vertical and operating point is at M_1 .(See Fig. 3.2. below) The voltage pulse required to trigger the circuit could be very small indeed, and this poses the threat of the circuit passing into the active region and oscillating due to small variations in the triggering level.

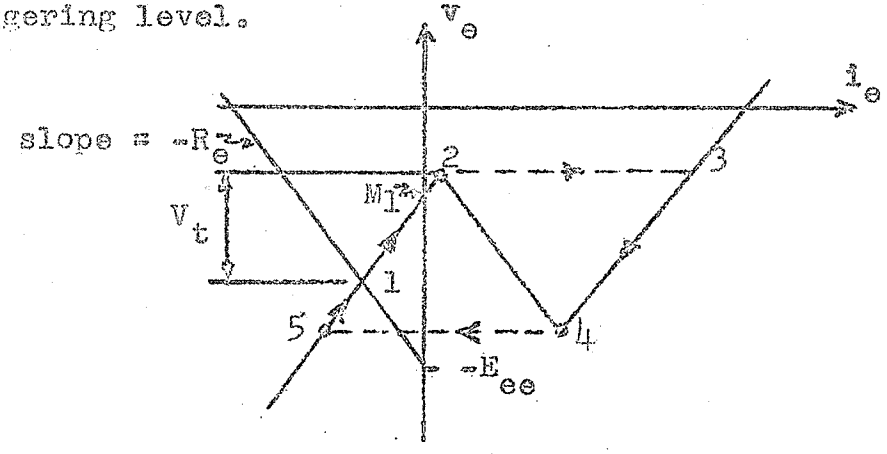


Fig. 3.2.

This was experienced many times during the course of testing, and therefore R_e and E_{ee} were added. The d.c. load line now has a slope $-R_e$ and an intercept of $-E_{ee}$ as shown in Fig. 3.2. and triggering voltage V_t can be precisely controlled. For monostable operation however R_e and E_{ee} are restricted to such values so that the load line intersects the emitter input characteristic only in the cutoff region.

The output pulse amplitude and width of either circuit (a) or (b) are independent of input pulse amplitude and width subject to the following conditions:

(1) If the input pulse width is greater than the output pulse width, the amplitude of the input pulse must not be so large that it will exceed the voltage required to trigger the circuit immediately after it has switched from the saturation to the cutoff region. If the input pulse is not restricted in this manner, an increase in the output pulse width would result.

(2) If the amplitude of the input pulse is just sufficient to trigger the circuit, the width of the input pulse must be slightly less than the recovery time of the circuit. If the input pulse width is equal to or greater than the recovery time of the circuit, multiple output pulses will result from the initiation of a single input trigger pulse.

3.2. Stabilization of the D.C. Operating Point.

For precise work it is very important that the triggering level of trigger circuits remain constant. It has been found that transistor parameters vary considerably due to ambient temperature changes, aging etc. Although these effects are primarily due to production methods and control, still, certain

circuit techniques may be employed to minimize them. In particular a and r_c vary with temperature considerably more than do the other parameters, and these changes in a and r_c cause the emitter input characteristic to shift as shown in Fig. 3.3.(b).

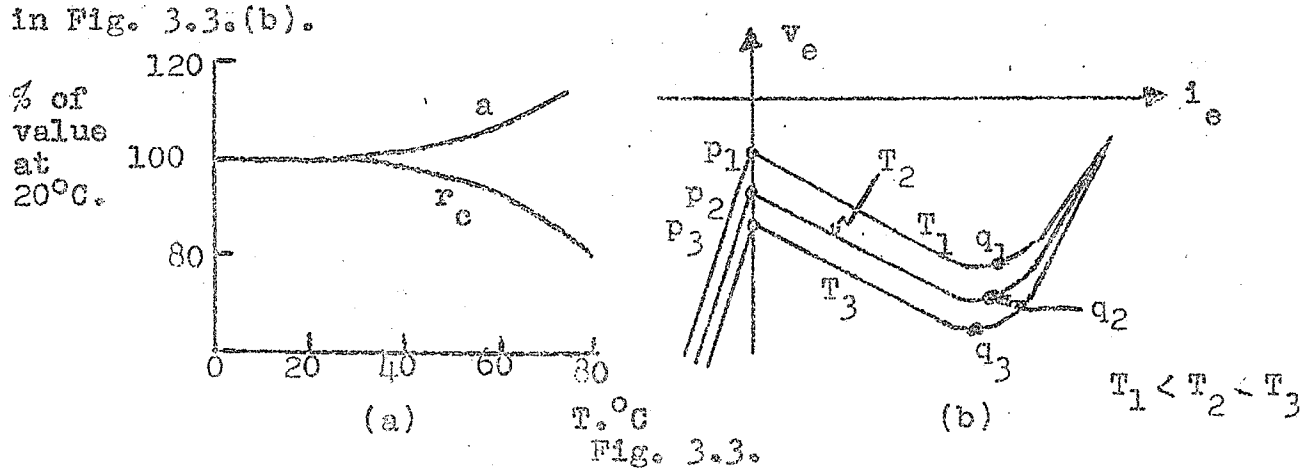


Fig. 3.3.

Variations in the triggering point (p) would cause the circuit either to free run or fail to trigger for any particular input pulse. Variations in the valley point (q) would cause changes in output pulse width.

For stability investigations, a special stabilized double pulse generator was constructed and stability tests were first performed on it. The circuit for the pulse generator is given in Fig. 3.4. It employs a multivibrator with variable repetition frequency to give the basic pulse. This pulse is then used to trigger a univibrator which gives out a delayed pulse relative to the triggering pulse; the time between pulse trains again being variable. The two trains of pulses then are fed into a mixer and through 1 stage of amplification. They are then fed through a biased diode stabilization circuit which only passes pulses of one specific voltage height. An amplitude control then taps off the required pulse amplitude and the pulses are sent out through a cathode follower of gain almost unity and low output impedance. This pulse generator gives out negative pulses

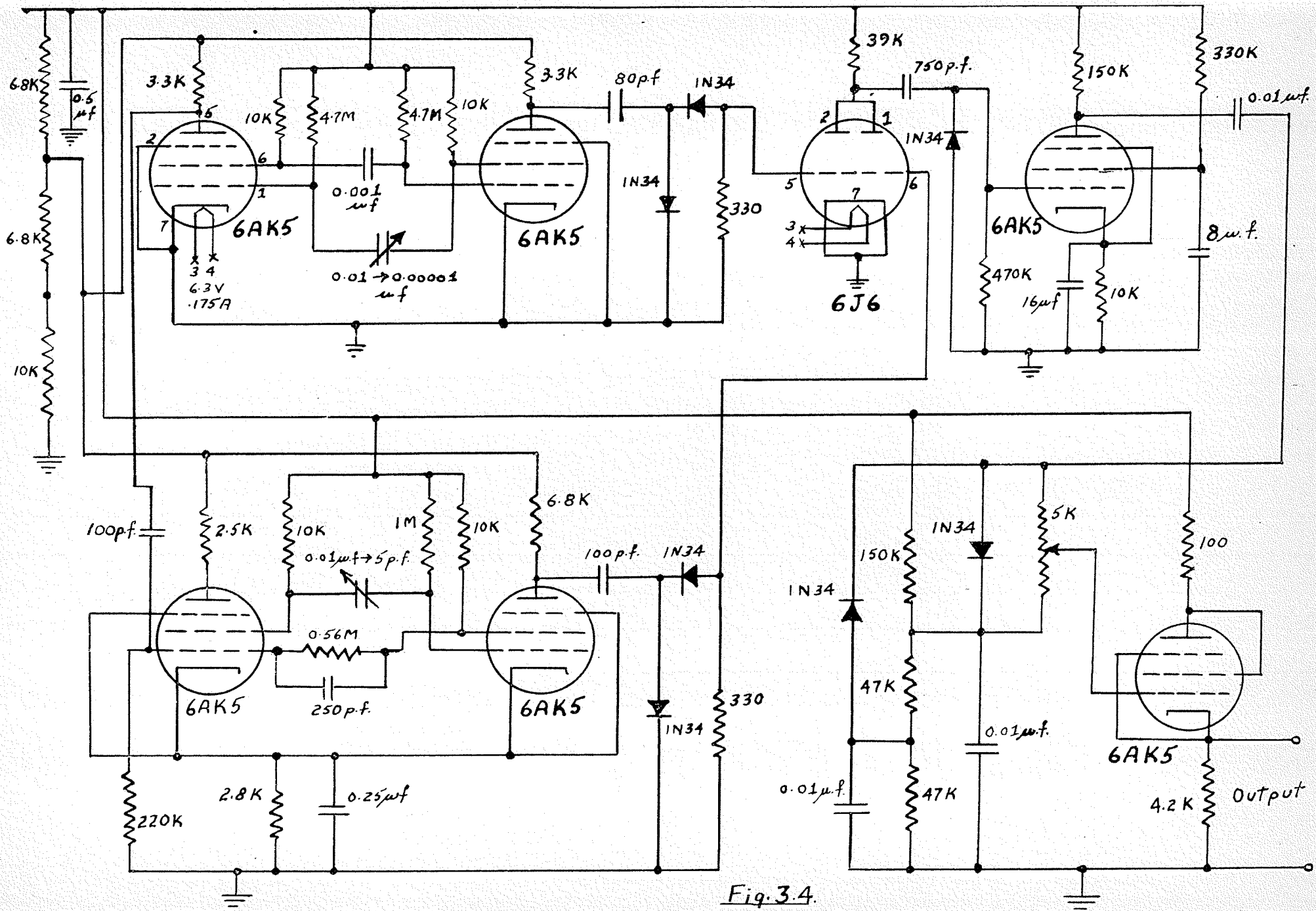


Fig. 3.4.

Stabilized Pulse Generator

C. Chaykowsky - Oct./55

0 to 40 volts, continuously variable. Basic repetition frequency is variable in 5 steps from 750 pulses per second to 12,500 pulses per second. Second train of pulses delayed relative to first by variable amounts in 5 steps: one from 0.6 u secs. to 1.4 u secs. continuously variable, and 4 steps up to 80 u secs. delay.

The circuit used to determine the stability of the pulse generator is shown in Fig. 3.5.

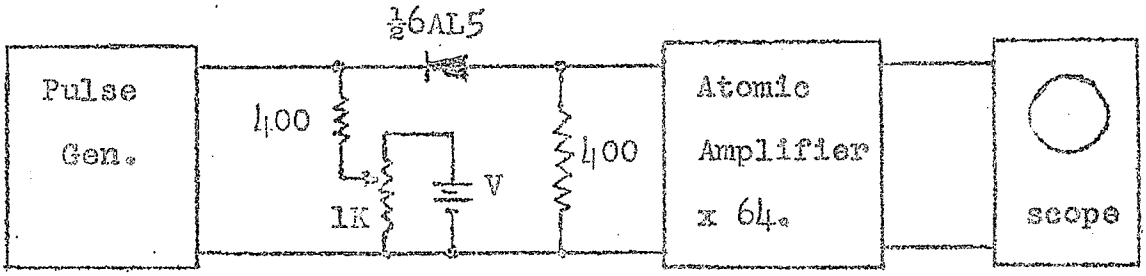


Fig. 3.5.

A pulse from the generator was passed through a diode, biased such that only a few millivolts were passed to the amplifier and such that the amplifier did not overload at maximum gain of 64. The output from the amplifier was then kept constant on an oscilloscope screen. Variations of $\pm$ 2 millivolts in the input pulse amplitude to the amplifier were easily detected. Two trials of 20 hours each were run and the results are shown in Figs. 3.6 and 3.7. Fig. 3.6 is for a discrimination level of 20 volts while Fig. 3.7 is for a discrimination level of only 3 volts. Note that between 10⅓ and 11⅓ hours a continuous check was kept on the stability, readings being taken every half-minute in order to ascertain whether or not there were any very short extreme fluctuations that did not follow the general trend. It was found that there were no "short fluctuations" and it was therefore assumed that the curve was rather smooth between experimentally determined points.

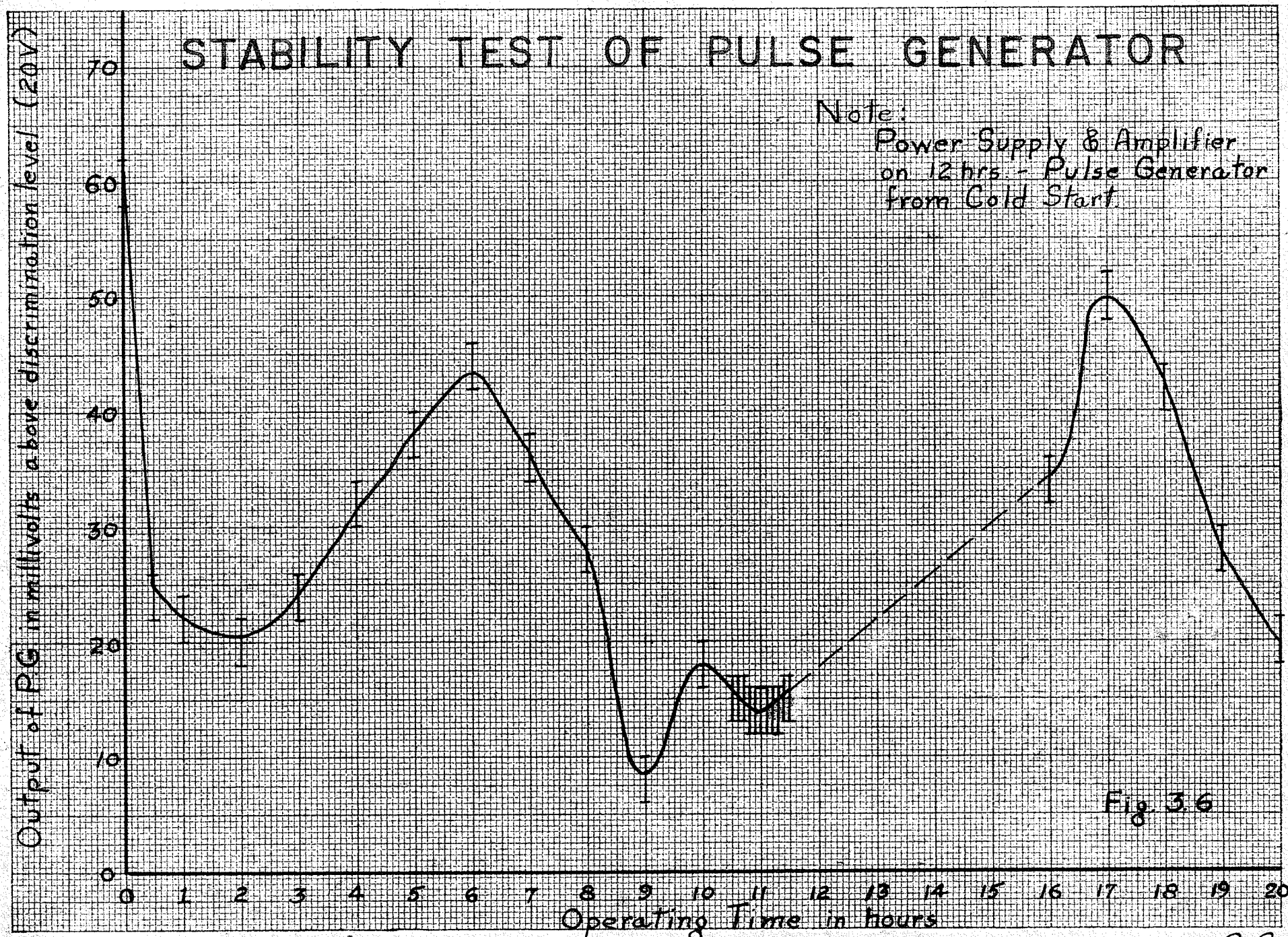


Fig. 3.6

C.P. 4/1/56

STABILITY TEST OF PULSE GENERATOR

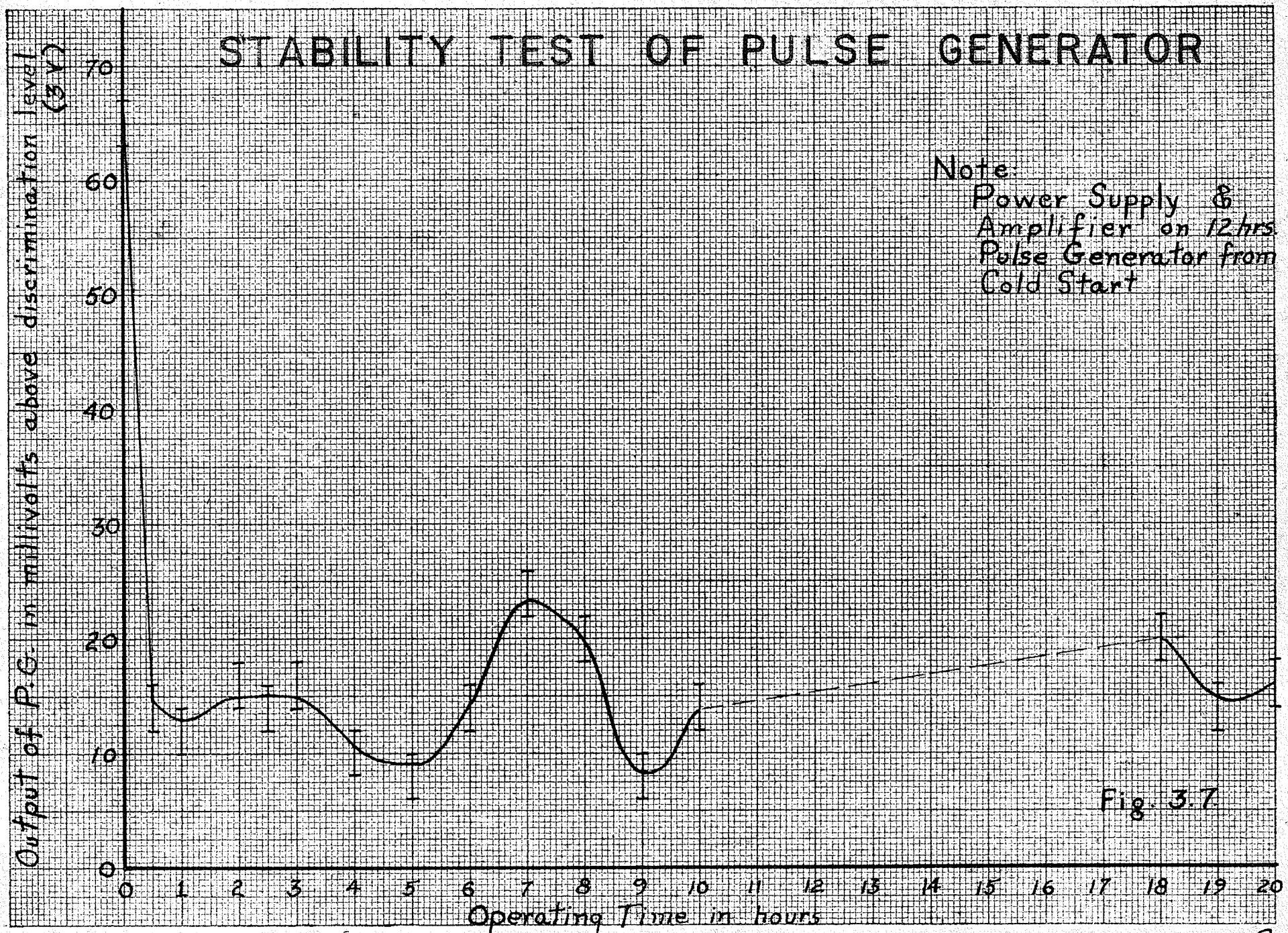


Fig. 3.7

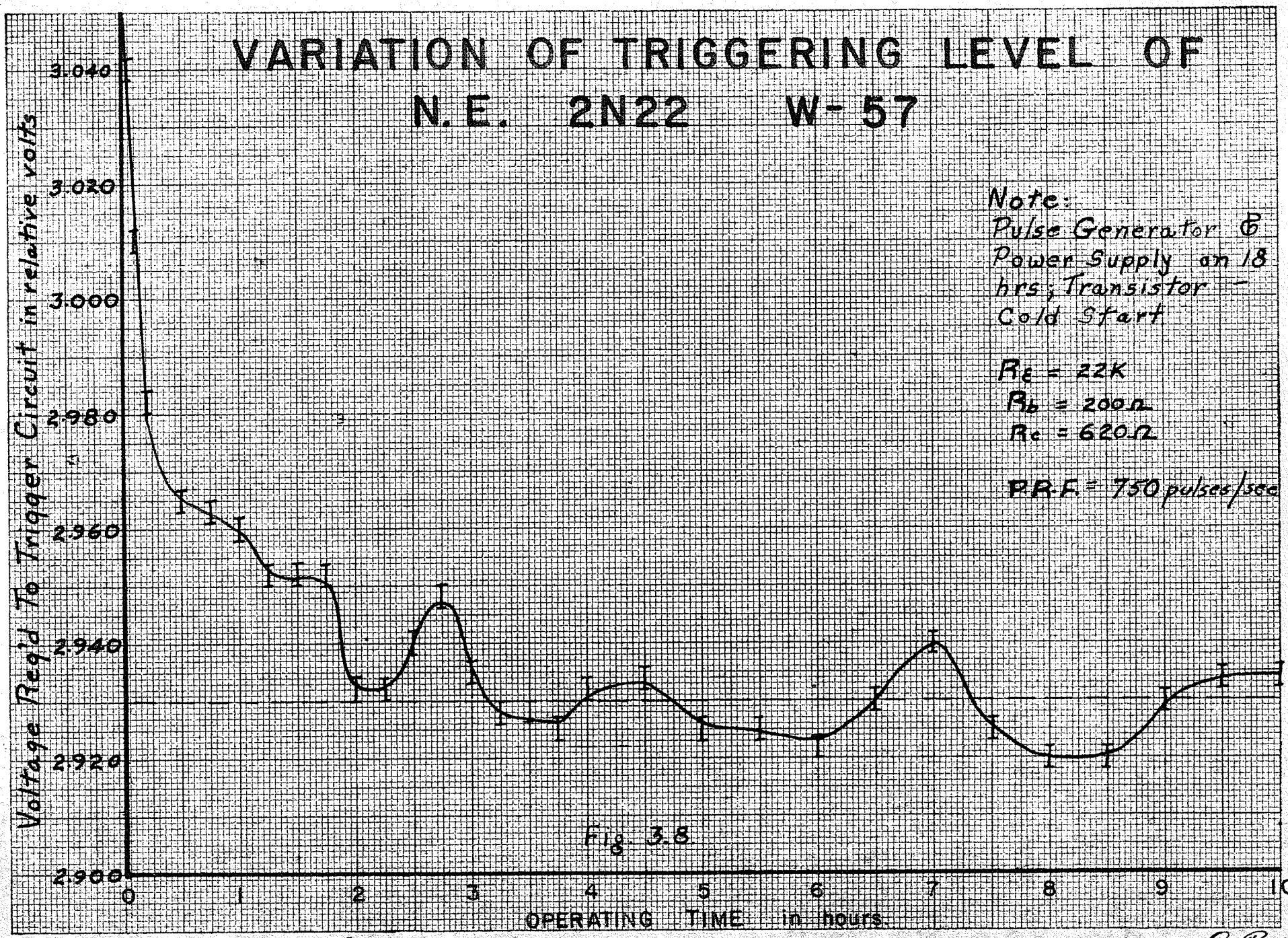
P.C. 4/1/56

The amplifier was determined to be well within the stability range being measured provided it had undergone a warm-up period of at least two hours before the experiment was undertaken. Fluctuations possibly due to variations in the associated power supplies were discounted by simply observing results when the supply voltages were varied by one percent. This caused no detectable change in the experimental results and since the supplies had a stability of 0.4 % or better it was therefore assumed that the fluctuations measured were those actually due to the pulse generator itself. The bias for the diode discriminating circuit was obtained from a battery and was assumed to be constant within experimental error. It was actually determined that the initial change in the curves for the stability tests of the pulse generator was due to the heating up of components, for when a fan was turned onto the components after a period of about two hours the curve almost rose to its intial value. We see from Figs. 3.6 and 3.7 therefore, that at worst, for output pulses of 20 volts the maximum fluctuation in this output pulse is only 42 millivolts. (after a warm-up period of at least one hour.) With a 3 volt output pulse the maximum variation after the same warm-up period is only 15 millivolts.

The stability of the triggering points of the transistors could now be investigated using the above mentioned pulse generator. See Figs. 3.8. , 3.9 , 3.10 , and 3.11.

The method was effectively the same as employed with the stability tests of the pulse generator. The input pulse to the trigger circuit was adjusted so that the transistor just triggered. (A few variations in the pulse amplitude

VARIATION OF TRIGGERING LEVEL OF N.E. 2N22 W-57



Note:
Pulse Generator & Power Supply on 18 hrs; Transistor - Cold Start

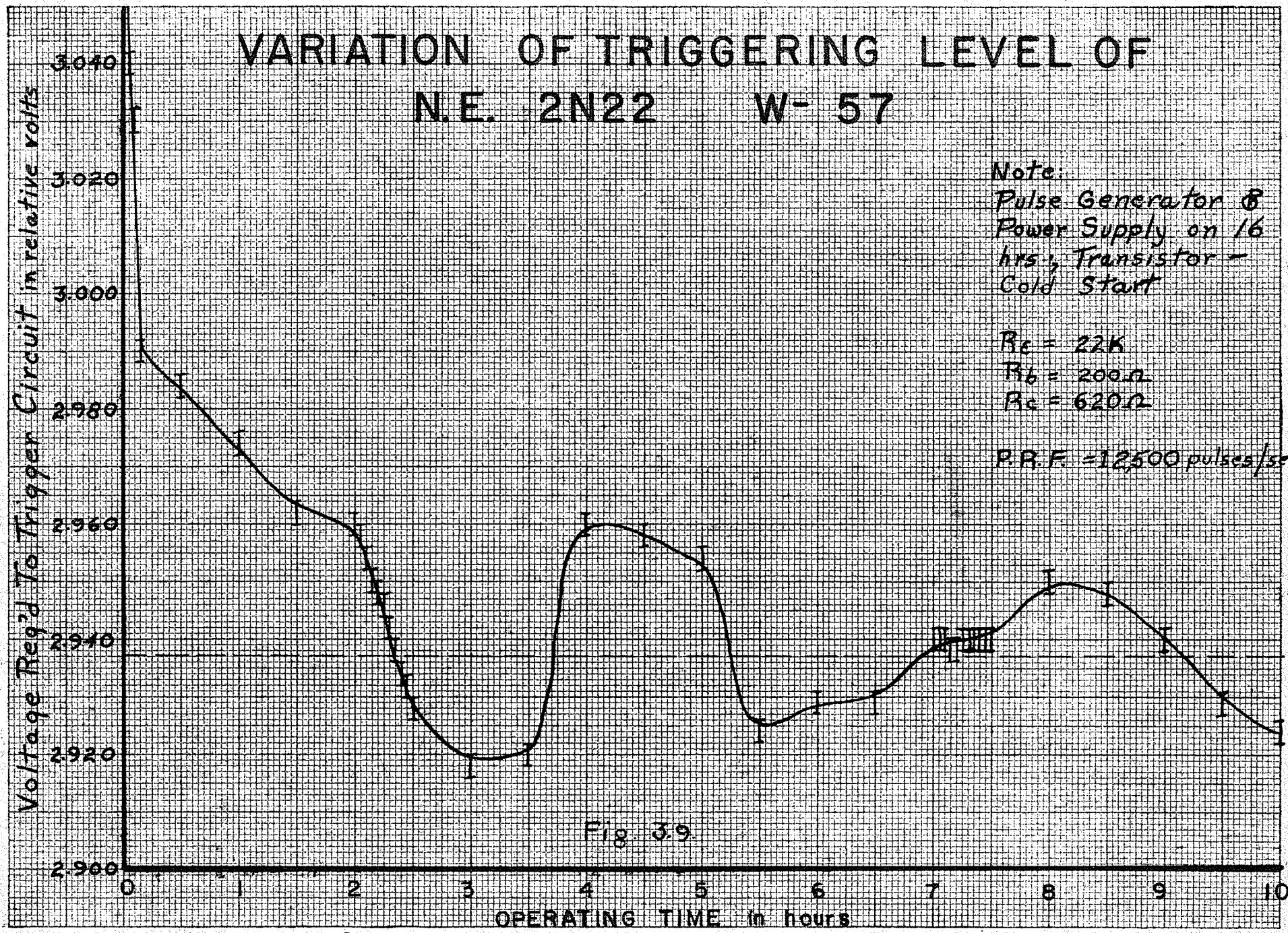
R_E = 22K
R_b = 200Ω
R_c = 620Ω

P.R.F. = 750 pulses/sec

Fig. 3.8

C.E. 4/1/56

VARIATION OF TRIGGERING LEVEL OF N.E. 2N22 W- 57



Note:
Pulse Generator ON
Power Supply on 16 hrs ; Transistor - Cold Start

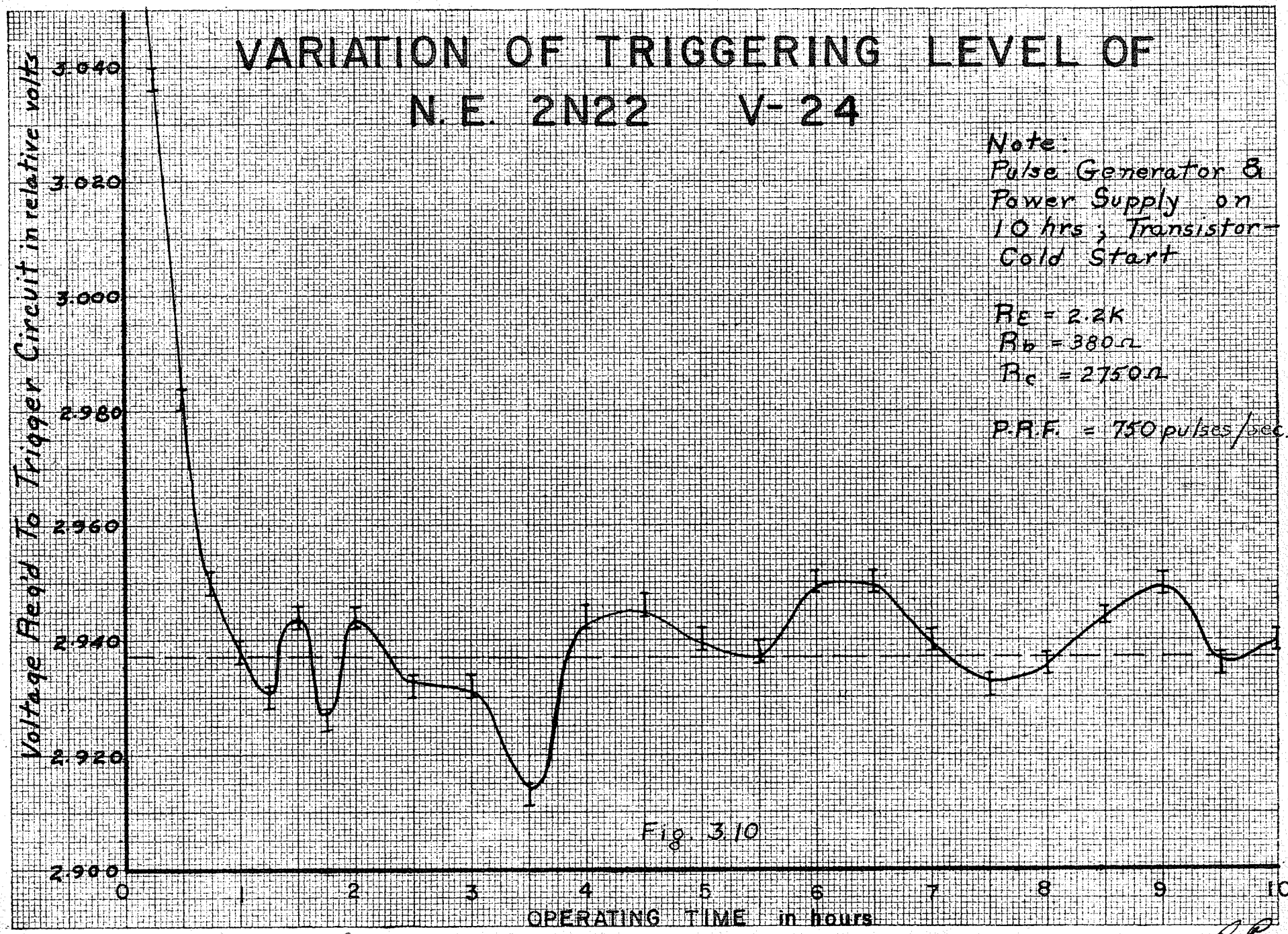
R_c = 22K
R_b = 200Ω
R_c = 620Ω

P.R.F. = 12,500 pulses/sec.

Fig 3.9

E.E. 4/1/56

VARIATION OF TRIGGERING LEVEL OF N.E. 2N22 V-24



Note:
Pulse Generator & Power Supply on 10 hrs ; Transistor - Cold Start

R_E = 2.2K
R_b = 380Ω
R_c = 2750Ω

P.R.F. = 750 pulses/sec.

Fig. 3.10

C.C. 4/1/56

VARIATION OF TRIGGERING LEVEL OF N.E. 2N22 V-24

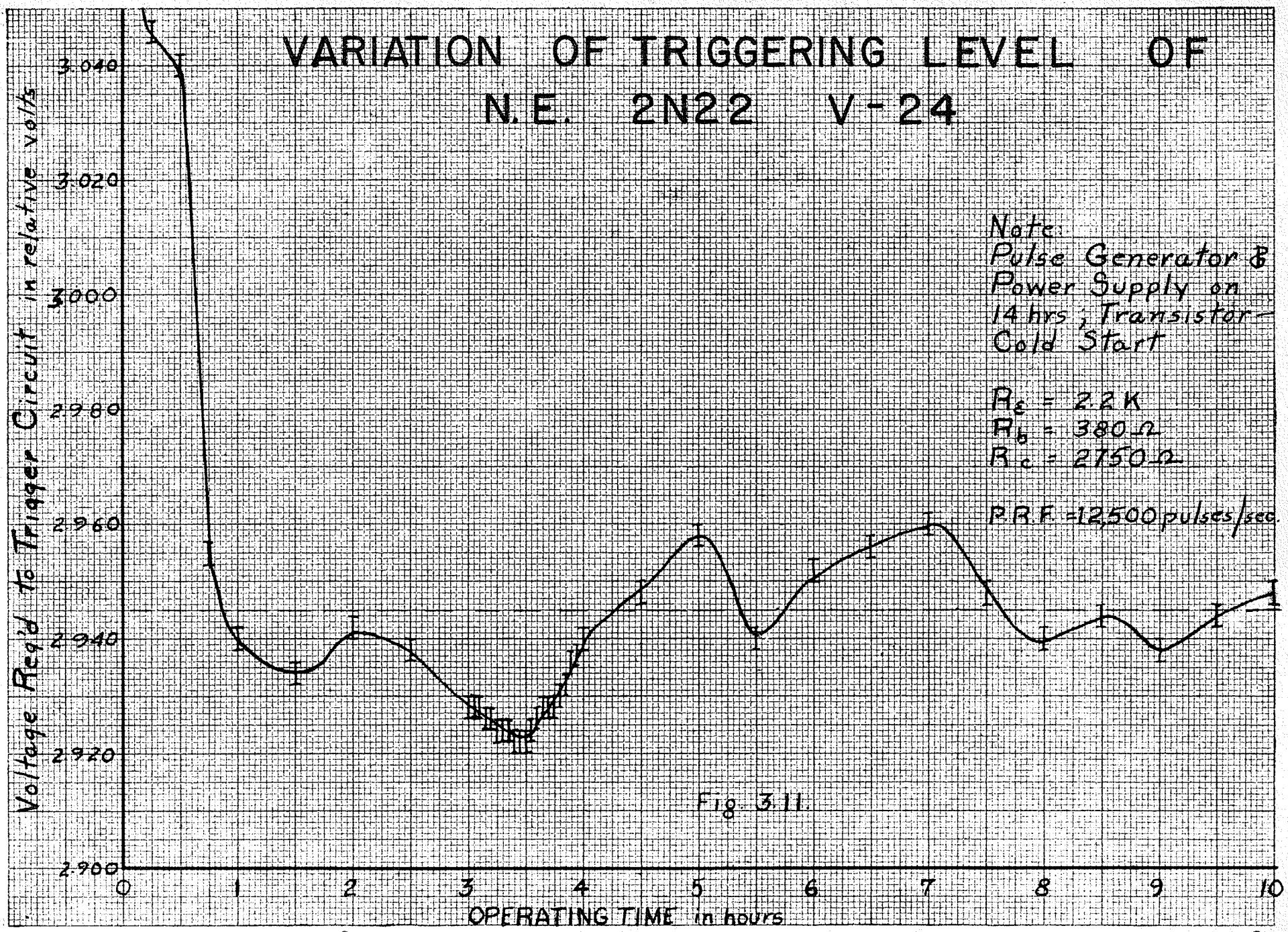


Fig. 3.11

C.B. 4/1/56

control circuit of the pulse generator were made in order to get the desired accuracy in measurements of output pulse height.) The uncertainty in whether or not the transistor was actually triggering took in $\pm$ 2 millivolts and made up the observational error. Two ten hour checks on each of the two transistors used for the trigger circuits were obtained at two different pulse repetition frequencies, in order to determine whether or not the heating of the transistor due to it being in the high conduction region more often for the higher repetition frequencies affected the triggering levels.

For W-57 it was determined that the higher p.r.f. caused greater variations in triggering level.

At 25,000 pulses/sec. --- fluctuations were 40 m.v. maximum

At 750 pulses/sec. --- fluctuations were 27 m.v. maximum

For V-24 no difference was detected for the different pulse repetition frequencies. Both varied by approximately 35 m.v. maximum. (All of these values quoted above are maximum variation after a two hour warm-up period has been discounted.)

All four tests were run on an input pulse of approximately 3 volts and fluctuations in the pulse generator were only 15 m.v. Sometimes this would subtract from the level and sometimes this would add to the level. As an absolutely worst possible case the author estimates the maximum variations in triggering levels to be :

For W-57 ---- 25 m.v. variation
For V-24 ---- 20 m.v. variation

} for as high p.r.f. as 25,000 pulses/sec and less for any smaller p.r.f.

Thus by careful selection of base resistance and transistors it was felt that the stability of the triggering levels was obtained to a satisfactory degree. It was also decided that to employ the usual diode clamping circuits, for clamping down the triggering points to specified voltages would not improve results sufficiently to warrent the use of two extra diodes and an extra supply voltage. Secondly, there would have been difficulties encountered in obtaining reliable measurements to any higher degree of stability since fluctuations in the pulse generator itself were already of the order of the measurements being taken. However, in future designs they most certainly may be required. The two transistors used here were painstakingly selected and it is interesting to note that none of the other 18 transistors tested were within 10 % of these two as far as stability goes. Some triggering points varied as much as 280 m.v. even after 4 hours of operation. Clamping circuits would most certainly have to be used with most of those transistors, especially if applied to similar circuits requiring similar degrees of stability as in this project.

The diode clamping technique suggested above is illustrated in Fig. 3.12.

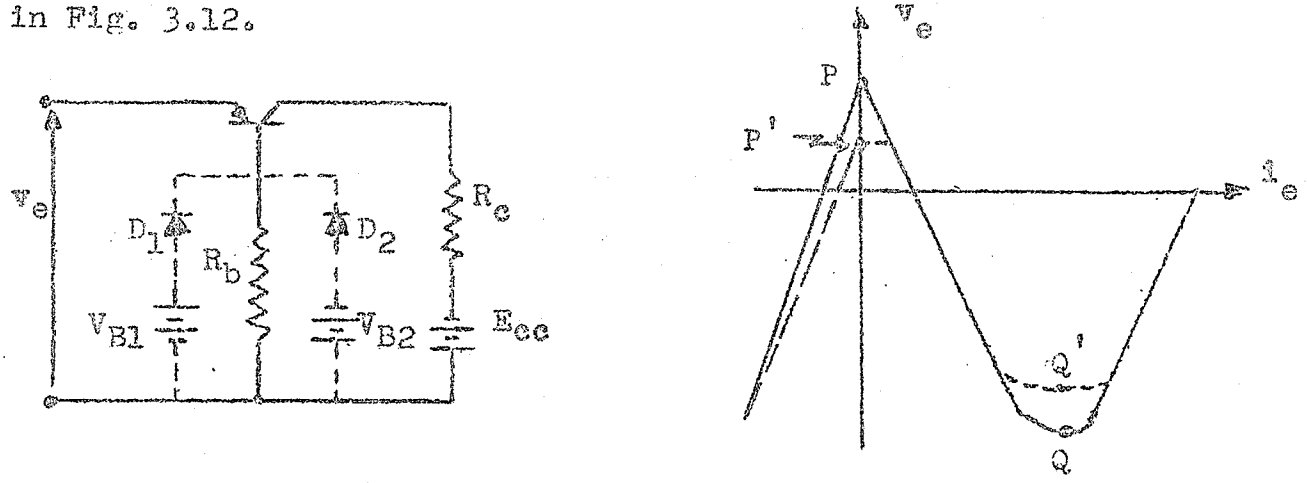


Fig. 3.12.

Without the clamping diodes the turnover points are P and Q, whose positions fluctuate with variations in transistor parameters. With the diode D_1 the first turnover point is clamped approximately at a voltage V_{B1}, and the second diode D_2 clamps the second turnover point at approximately V_{B2}. The stabilized turnover points are now P' and Q'.

3.3. Anticoincidence Mixing Circuit.

The schematic diagram for an anticoincidence circuit is shown in Fig. 3.13

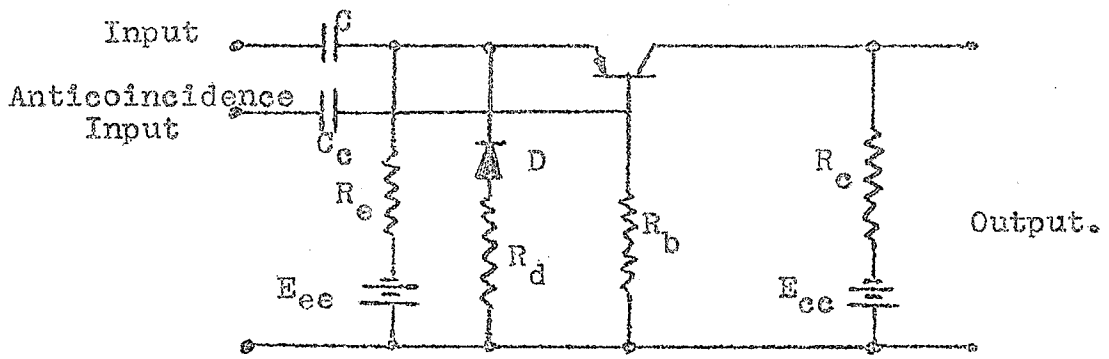


Fig. 3.13

The circuit gives an output pulse if and only if a single positive pulse is applied to the emitter input. If two positive pulses arrive simultaneously at the emitter and base, both being of almost equal amplitude, there will be no trigger action since the base is driven positive as hard as the emitter is and therefore no relative change in potential occurs between them. It is preferable that the input pulse to the base be slightly greater in amplitude than that to the emitter in order to insure complete cancellation.

Note that the stability of the triggering level of the transistor used in the anticoincidence circuit is not as important as for the transistors used in the trigger circuits.

Considerably more fluctuations can be tolerated since fairly large pulses are used to operate the circuit, (on the emitter 12 volts; on the base 23 volts). As an extra precaution, the emitter is biased rather heavily negative so that a pulse of about 6 volts is required to trigger the circuit. Thus even fluctuations of $\pm$ 5 volts, which are highly unlikely, will not hinder the operation of the circuit. (Eight hour stability test on # 51-24 showed a maximum fluctuation of 60 millivolts.) Note also, that a single positive pulse on the base will not trigger the circuit, no matter how large. However, this situation does not occur in pulse-height analysis, since the base is fed from the upper level trigger circuit, and if the upper level has triggered, then certainly the lower level must have also triggered.

The recovery diode from base to emitter must be removed in this circuit in order to prevent the positive pulse on the base from adding to the positive pulse on the emitter, and having the circuit trigger from the combined effect, whereas a cancellation should have resulted. In order to reduce the recovery time in this circuit, the diode may be placed as shown in Fig. 3.13. with a small series resistance to ground. This replacement effectively changes the emitter bias arrangement, and R_e may have to be adjusted. The diode is necessary in some cases for isolation where a value of R_d is such that an appreciable amount of signal is lost across it and where R_e is set high for triggering sensitivity. However, in this unit R_e was arranged to be only 700 ohms and R_d was chosen for correct emitter bias , in conjunction with R_e, such that a 6 volt pulse was required to trigger the circuit. No

appreciable loss of signal was encountered without the diode, and therefore it was unnecessary. Recovery time tests were made with and without the diode and no appreciable difference was detected. This of course was to be expected since R_e was already of the order of the forward impedance of the diode, and the discharge time constant was effectively CR_e. Photographs of the output pulses from the anticoincidence circuit showing recovery times are given in Figs. 3.23 and 3.22.

3.4 Delay Techniques

Because the input pulse has a finite rise time, there is a difference in triggering time Δt between the upper and lower level trigger circuits as indicated in Fig. 3.14.

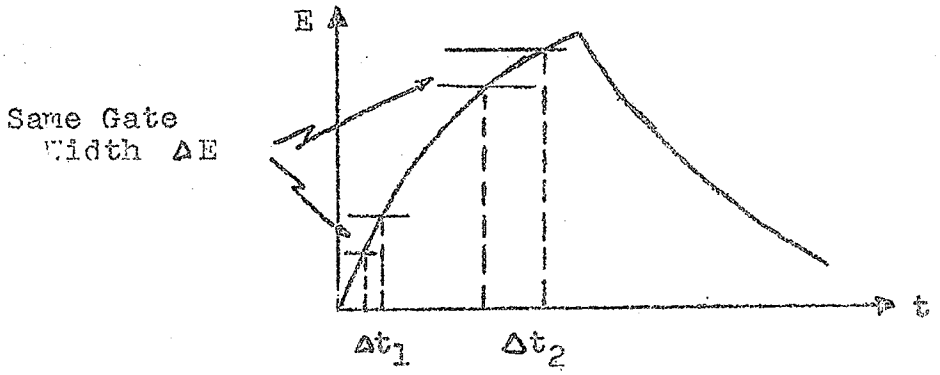


Fig. 3.14.

This difference in triggering time depends also upon the gate width and discrimination level as well as upon the rise time of the input pulse. We see therefore that the lower level pulse must be delayed in such a way so that it arrives at the mixer for all discrimination levels, gate widths and rise times expected, completely overlapped by the upper level pulse. Two types of delay methods were tried in this investigation, and the following one was accepted.

A piece of G.E. continuous delay line (nominal impedance 1000 ohms; nominal delay, 0.7 u secs./ ft; rise time 0.06 u secs. / 2.7 ft; and 167.0 ohms / ft d.c. resistance) was used in the lower channel. Since this unit was specifically designed for use in conjunction with equipment now being employed in scintillation spectrometer set-ups at the University of Manitoba, the delay circuit design to follow was based on the pulse rise times obtainable from the Atomic Amplifier (type 204-C) presently being used to feed vacuum tube pulse height analyzers. The output pulses from the amplifier have a rise time of approximately 0.25 u secs. Therefore, maximum difference in triggering time between lower and upper levels could not be more than 0.25 u secs. even for the worst possible case. i.e. discrimination level at zero and gate width equal to the pulse height.

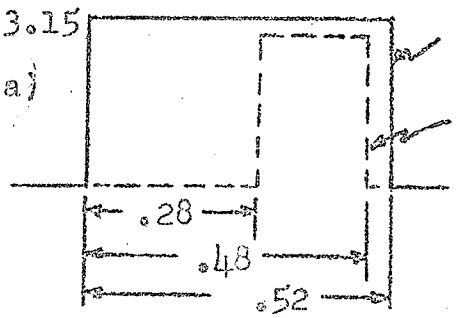
The lower level pulse length at the emitter of the mixer i.e. after it has passed through the delay line, should not differ from the lower level trigger circuit output pulse length by any appreciable amount if the delay line is properly matched, and therefore the output pulse length from the trigger circuit was used to compute the required upper level cancelling pulse shape. However, when the unit was assembled, perfect cancellation was not taking place due to reflections in the delay line. The pulse shapes were then fabricated experimentally on a "bread-board".

The delay was chosen as 0.28 u secs. in order to completely encompass the worst possible case mentioned above, and then the external parameters of the mixing circuit and the upper level trigger circuit were adjusted for proper pulse cancellation.

pulse amplitude, pulse shape, circuit recovery time, and delay line matching. Needless to say, a good deal of compromise had to be adopted, and wherever possible the parameters where chosen to favor conditions whereby a minimum possible recovery time could be obtained, reflections in the delay line being tolerated to a certain extent.

The pulse length at the emitter of the mixer was effectively just less than 0.2 u secs. If one looks at the photographs in section 3.5, it can be seen that the total length is about 0.35 u secs but the secondary pulse due to reflections in the delay line is of negligible amplitude compared to the first and definitely will not trigger the anticoincidence circuit since it is biased heavily negative. Thus we see that the upper level pulse must have at least a 0.48 u sec. flat top to take into account the worst possible case. (0.2 + 0.28) Actually it was adjusted to have a flat top of about 0.52 u secs and a total length of 0.9 u secs. The two extreme possiblities are illustrated below with idealized pulse shapes.

Fig. 3.15 (a)



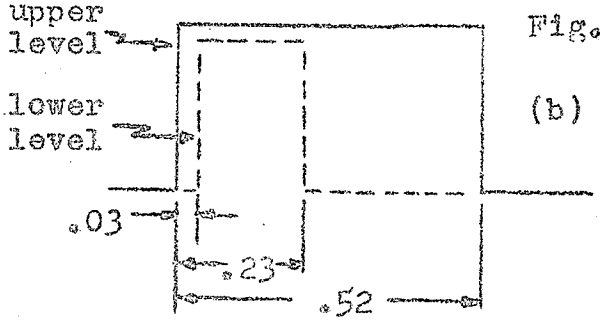


Fig. 3.15 (b)

(a) Both upper and lower levels trigger at exactly the same time.
(b) Lower level triggers 0.25 u secs before upper level

A control was incorporated in the final assembled unit to vary the output pulse length from the upper level as may be required with faster amplifiers, thus reducing the recovery time. R_b was made variable rather the C as is the usual method

because it was experimentally determined that in order to obtain a range for total output pulse lengths from 0.4 to 1.4 u secs. a large range of values for C had to be covered, whereas only a small range of values of R_b would give the same results. It was also considerably more convenient to employ a potentiometer rather than a variable capacitor from a space limitation point of view. The range of R_b that had to be incorporated was only 160 ohms, and this change made no detectable difference in the stability tests of triggering levels. The same principle was used in the mixing circuit to control the output pulse, except that R_c was varied rather then R_b. This had to be the case because R_b in the mixing circuit was chosen in a compromising manner from the point of view of operating conditions and delay line matching and once chosen, it had to remain constant.

The other method investigated for incorporating a delay made use of a transistor and is illustrated below.

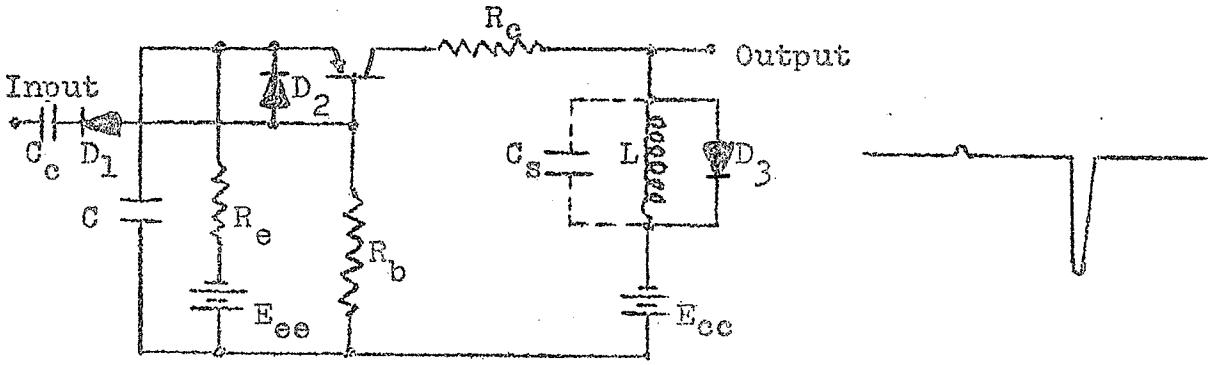


Fig. 3.16.

The diode across the choke absorbs all the energy except for the small negative "pip" at the trailing edge of the output pulse, which would be observed across R_c. By varying C or R_b the output pulselength could be varied and therefore the

delayed negative "pip" could be also varied in time. The main disadvantage with the circuit as applied to the problem under consideration was that the delayed pulse was nagative and could not be applied directly to the mixing circuit. Also to obtain delays of less than 0.5 u secs, very small chokes had to be used and the delayed pulse was very small; less than one volt in amplitude. An extra transistor for amplification and phase reversal would have to be used. It was felt that the ordinary transmission line delay would be a better choice from the point of view of simplicity and if a proper match could be obtained, its performance would be considerably better than the transistor delay scheme in the regions required. The photographs in section 3.5 show that a little mismatch is present but the reflected pulses have very little effect on the operation of the unit.

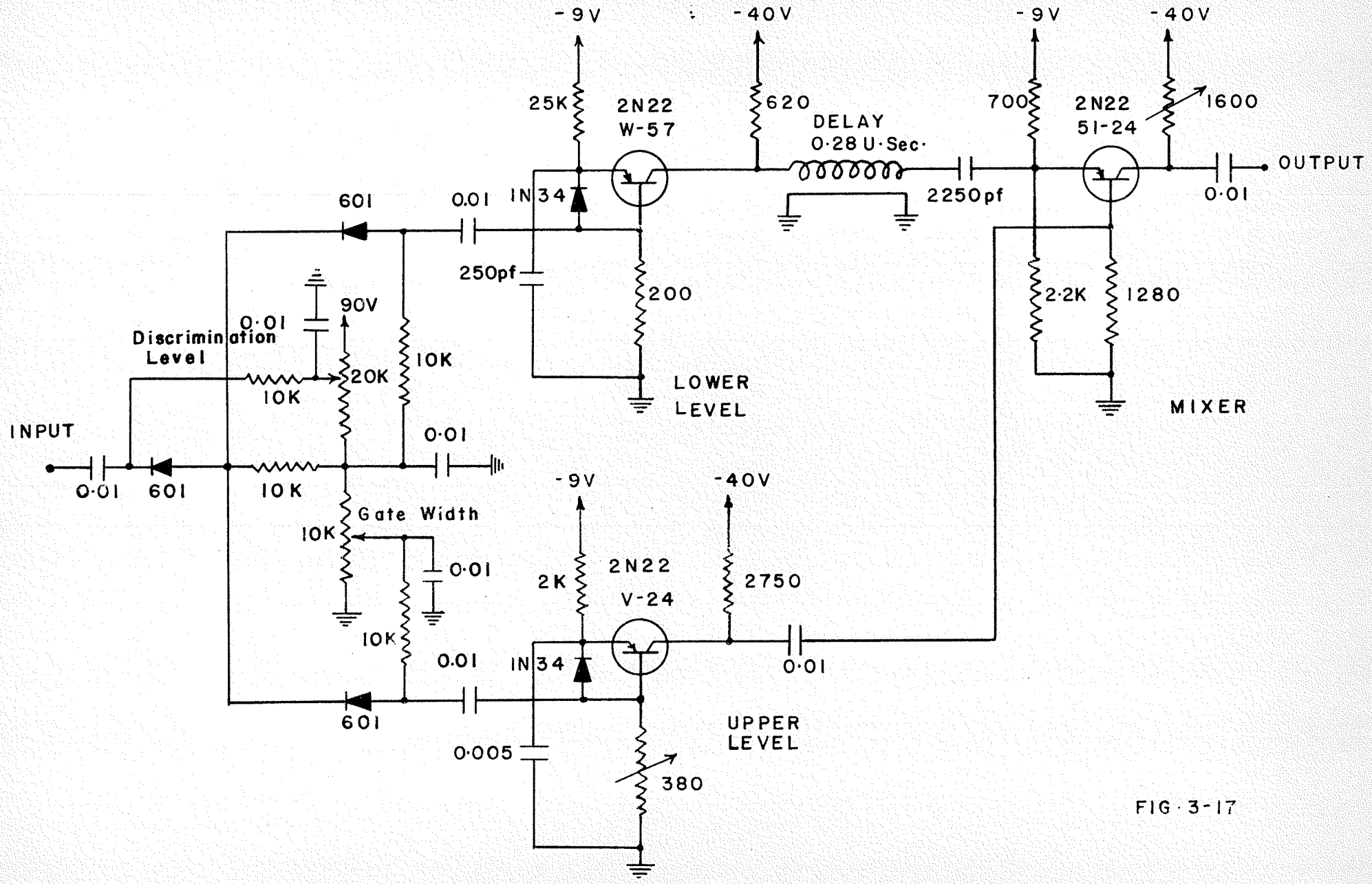
3.5. Performance of the Single Channel Pulse-Height Analyzer.

Complete circuit diagram of the transistorized single channel pulse-height analyzer is given in Fig. 3.17. For future monitoring purposes the following table is included.

D.C. Operating Conditions

	W-57	V-24	51-24
I_c	2.6 m.a.	3.0 m.a.	1.7 m. a.
V_c	37.5 v	30.0 v	35.0 v
I_e	0.6 m.a.	2.4 m.a.	3.1 m.a.

All resistors are 1%, $\frac{1}{2}$w, carbon and all potentiometers except the two helipots in the discriminating circuits are carbon. Wire wound potentiometers must not be used in this unit, except if absolutely unavoidable, in dead parts of



FIG·3-17

SINGLE CHANNEL PULSE-HEIGHT ANALYZER

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the circuit, as the helipots are used here. The stray inductance associated with the wire wound potentiometers caused slight distortions in pulse shapes, especially if used in the base circuit.

The stability of gate width and discrimination level was tested for two different pulse rise times, 0.3 and 0.03 u secs. The results are tabulated below for a range of discrimination levels from 0 to 60 volts.

rise time of input pulse	gate width	Variations in gate width
0.03	1 v	1/40 v
0.3	1 v	5/20 v
0.03	2 v	1/20 v
0.3	2 v	7/20 v
0.03	3 v	1/20 v
0.3	3 v	9/20 v

We see that for pulses having relatively long rise times the results are not very good, and since the amplifiers presently being used in our particular set-up give pulses with rise times of this order, any results obtained in conjunction with this unit would not be very reliable. However with the fast rise time pulses, results are indeed acceptable; gate width varying by only about 1.6% over a range of discrimination levels of 60 volts.

It should be mentioned that the relatively poor results at the pulse rise times for which the delay and transistor circuits were especially designed are not due to either of these circuits, but due to the operation of the discriminating diodes in the discriminating circuit. High back impedance diodes (Texas Instruments 601) were chosen for use in the discriminating circuit. Several types were tested (1N34, 1N38 and T.I.601) but it was found difficult to match the 1N34 and 1N38 diodes due to small differences in their

back impedances between any two particular diodes. At voltage levels above 15 volts, noticable differences in the amount of current each diode drew were easily detected because potential differences were observed across points that were supposed to be at the same d.c. potential. The silicon 601 diodes have a much higher forward resistance than the other two mentioned (undesirable) but also have considerably higher back resistances (desirable) and it was relatively a simple matter to select a few that drew almost identical currents at the same voltage levels.

In order to try and improve the results for the 0.3 u sec. rise time pulses, small trimmer capacitors were placed across each diode in turn in order to ascertain whether or not the pulses were leaking more through one diode than through the other due to stray capacitive coupling across the diodes. Very slight improvements were noticed but it was concluded that the major fault was elsewhere, since the effect should have been more pronounced for the sharper pulses but wasn't.

The author feels that in order to make the unit applicable to the slower rise pulses, a different method of discrimination will have to be used, possibly a biased transistor amplifier. This possibility was not examined due to a lack of time and was left to be completed at a future date. It is hoped that possibly a faster vacuum tube amplifier will be obtained in the near future so that this unit could be sucessfully incorporated into the scintillation spectrometers at the University of Manitoba.

We will concern ourselves from here on therefore only with the results as obtained with the "fast" pulses.

The pulse shapes as obtained from the various points of interest in the unit are shown in Figs. 3.18, 3.19, 3.20, 3.21, 3.22, and 3.23.

The minimum recovery time of the unit is just less than 2 u secs. Therefore, maximum regular counting rate is slightly in excess of 500,000 per second. For no more than a 1% loss maximum counting rate should not exceed 5,000 pulses per second. This value was computed from the expression $N = \frac{n}{(1 - nt)}$

where N = the number of events occuring per second

n = the number of events counted per second

t = recovery time of the circuit

(the circuit of course being of the non-paralysable type.) The 2 u sec. recovery time is governed by the recovery time of the upper level which itself is just 2 u secs. All other trigger circuits have recovery times less than this and down to a minimum of 0.8 u secs. The rather long recovery time in the upper level is due to the trigger circuit having to give out a rather long pulse (0.9 u secs.) in order to completely enclose the lower level pulse at the mixer for all gate widths, discrimination levels, and rise times encountered. The photographs show all the minimum recovery times obtainable; the results are from input pulses obtained from the double pulse generator described earlier. The rise times of the output pulses in Figs. 3.18, 3.19, and 3.20 were measured on the Tektronix millimicrosecond sweep scope and determined to be 30 m u secs. in all cases.

The output pulse length is variable from 1 to 2 u secs as may be required with associated scaling equipment; some scalers requiring at least pulses 1 u sec long above the

discrimination level of the scaler. The double rise effect in these output pulses from the mixer could not be eliminated without causing excessive distortion to the input pulses due to further mismatching of the delay line and it was decided to tolerate this effect, since it really does very little harm if any at all.

The last three references listed under section 3.6, although not referred to specifically, were included because general ideas were obtained from them and used freely throughout this thesis.

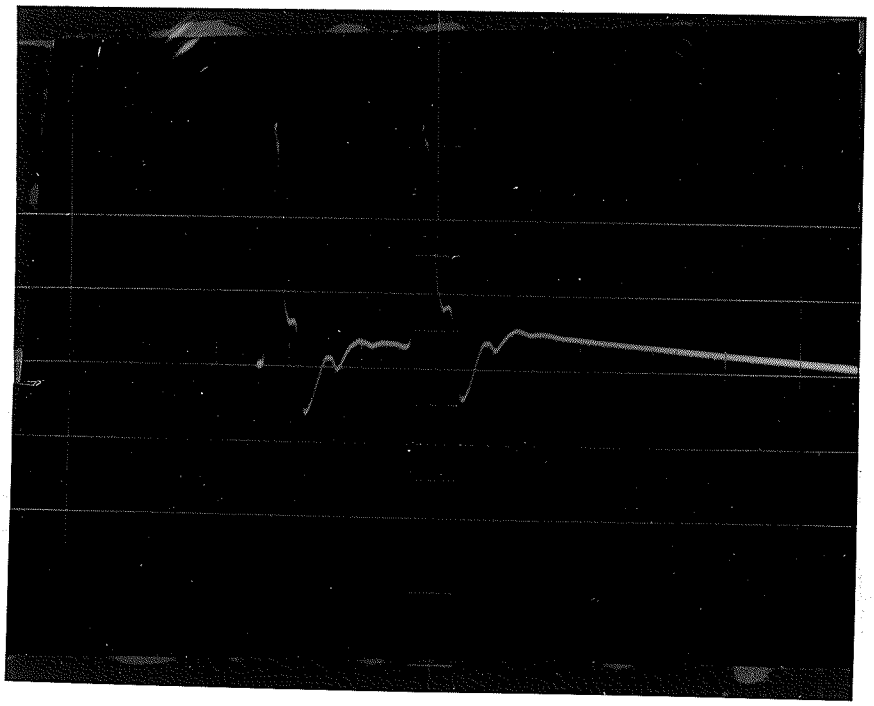

Fig. 3.18.

Output from Lower Level.

Scale: 0.4 Microseconds / Horizontal Division (1 cm.)

7 volts / Major Vertical Division (1 cm.)

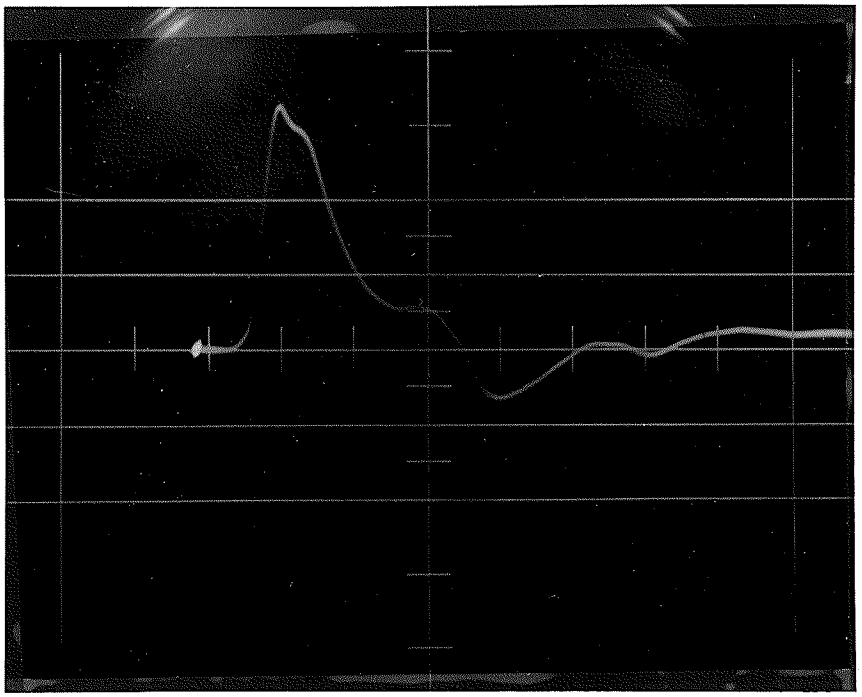

Fig. 3.19.

Output from Lower Level

Scale: 0.1 Microseconds / Horizontal Division (1 cm.)

7 volts / Major Vertical Division (1 cm.)

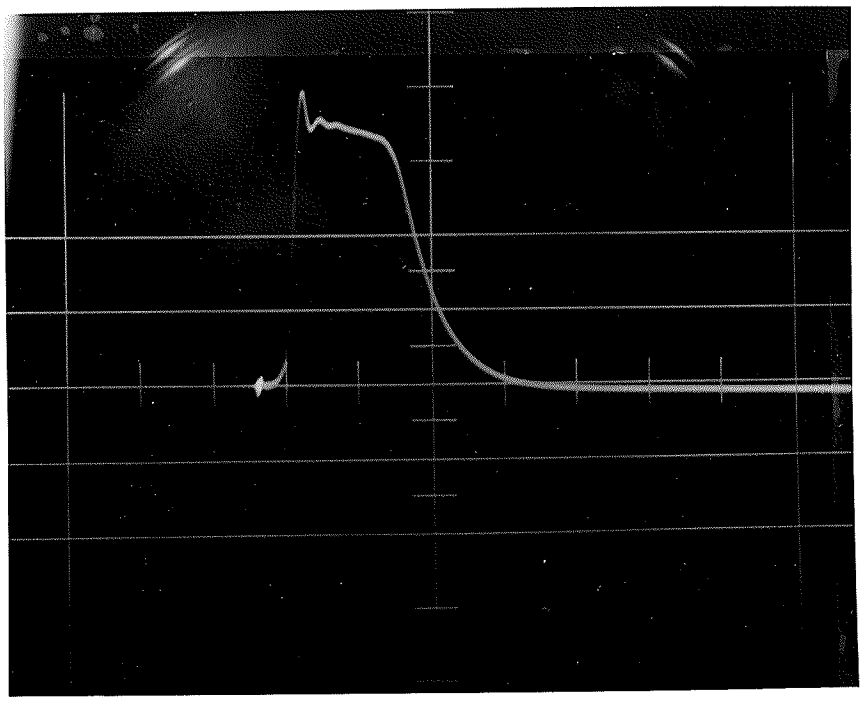

Fig. 3.20.

Output from Upper Level.

Scale: 0.3 Microseconds / Horizontal Division (1 cm.)

7 volts / Major Vertical Division (1 cm.)

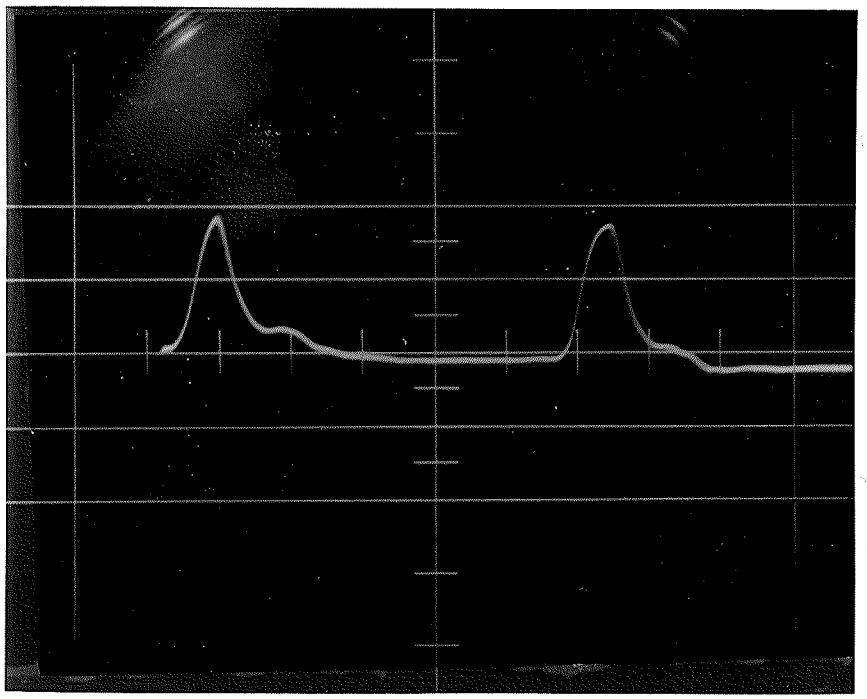

Fig. 3.21.

Output from Delay Line.

Scale: 0.2 Microseconds / Horizontal Division (1 cm.)

7 volts / Major Vertical Division (1.cm.)

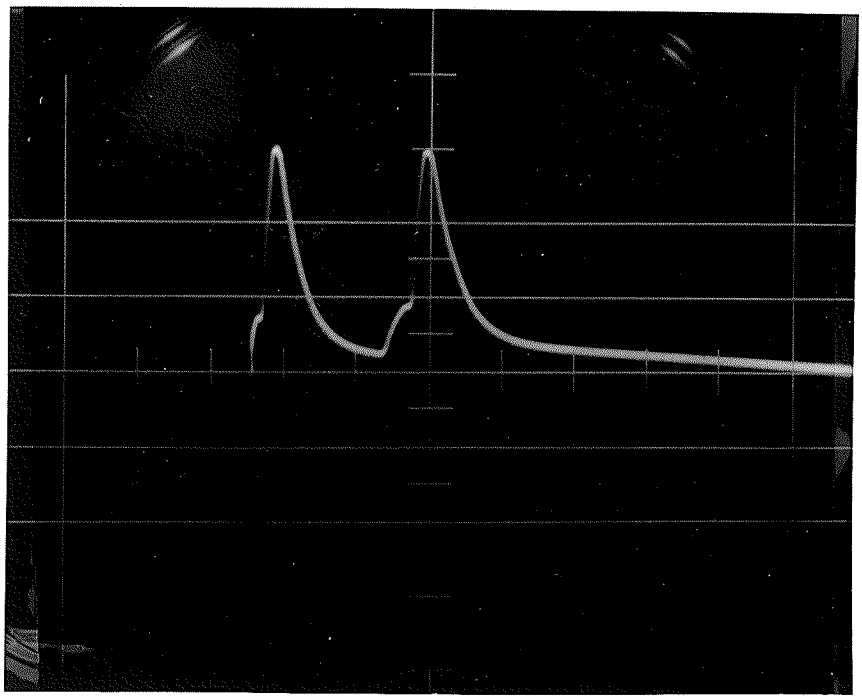

Fig. 3.22.

Anticoincidence Output from Mixer.

Scale: 1 Microsecond / Horizontal Division (1 cm.)

2 volts / Major Vertical Division (1 cm.)

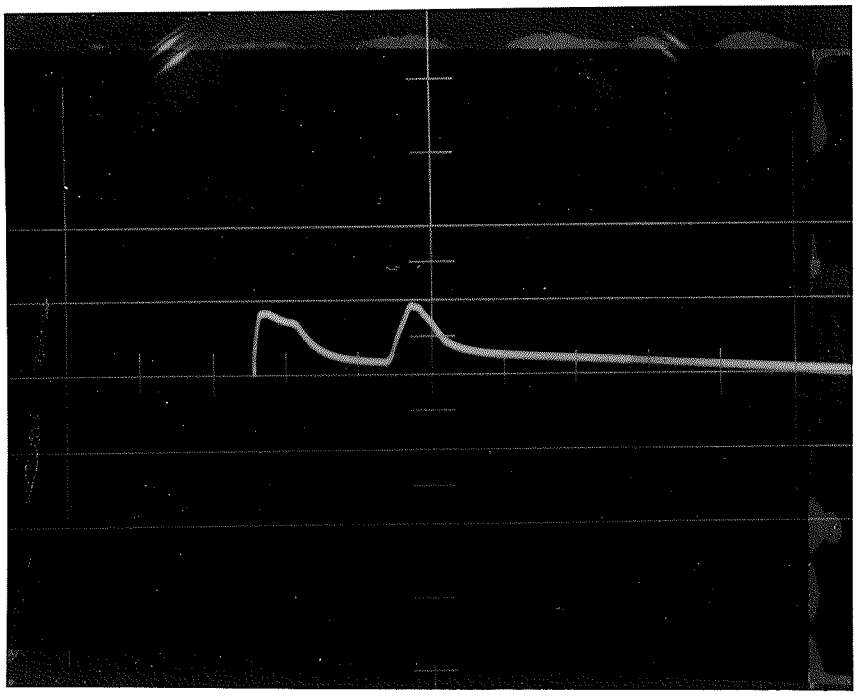

Fig. 3.23.

Cancelled Output from Mixer.

Scale: 1 Microsecond/ Horizontal Division (1 cm.)

7 volts / Major Vertical Division (1 cm.)

3.6 References:

1. C. H. Westcott and G.C. Hanna , " A Pulse Amplitude Analyzer for Nuclear Research using Pretreated Pulses," Rev. Sci. Instr. 20, 181(1949).

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9. V.G. Khartmon et al, " A Pulse Height Analyzer with an Electron Beam Tube " , Soviet Physics, # 3, 537 (1955).

Part 4

CONCLUSIONS

4.1. Conclusions

A single channel transistorized pulse height analyzer has been designed and built, having a recovery time of slightly less than 2 u secs. The circuitry has been considerably simplified and reduced in comparison to vacuum tube single channel pulse height analyzers of similar performance, and the overall power requirements have also been substantially decreased.

The author feels that considerably better recovery times can be obtained with transistor units if used in conjunction with faster amplifiers than were available for this investigation. A complete transistorization of the electronic equipment associated with scintillation spectrometers would undoubtedly lead to a general improvement of results. With the recent announcement of surface barrier tetrode transistors of frequency range in excess of 10 Mcps. it appears that a transistor amplifier could be built with much better rise time response than is presently being obtained from the model 204-C Atomic Amplifiers.

The next logical step as a follow up to this project would be the design and building of a transistorized amplifier or even a transistorized multichannel analyzer. The single channel unit described here could be used as a basic circuit for as many channels as desired, and the only forseeable complications which might arise would be in the channel mixing and stabilities of channel levels with respect to each other.