Design and Experimental Evaluation of a High-Efficiency Wireless EV Charging System with Aging- and Tolerance-Aware ZVS

by

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Abstract

Wireless Power Transfer (WPT) has gained significant attention as a promising technology for electric vehicle (EV) charging, offering convenience, safety, and the potential for widespread adoption of electrified transportation. Achieving high efficiency and long-term reliability, however, remains a major challenge due to the strong dependence on coil design, resonant compensation, and the robustness of soft-switching operation under component degradation.

This thesis presents the design and experimental validation of a 2 kW series-compensated WPT system for EV charging applications. A systematic methodology was developed to optimize Archimedean spiral coil, focusing on maximizing power transfer efficiency while avoiding bifurcation. The proposed design approach is novel in that it simultaneously ensures high efficiency and bifurcation-free operation, enabling the selection of coil turn count and load resistance that achieve optimal performance under the provided design constraints.

The 2 kW prototype was experimentally tested, demonstrating high efficiency and stable, bifurcation-free operation across the studied operating conditions. These results validate the effectiveness of the coil design methodology and highlight the advantages of the proposed approach compared with conventional design guidelines.

The thesis specifically examines how capacitor aging and manufacturing tolerances affect Zero-Voltage Switching (ZVS) and overall system efficiency. Experiments demonstrated that deviations in primary capacitance reduce the ZVS window and can lead to additional switching losses if dead time is selected based only on nominal conditions. A dead-time selection strategy that accounts for these deviations—along with careful capacitor selection to minimize tolerance and aging drift—was proposed and experimentally validated. This ensures that ZVS is preserved and high efficiency is maintained even as component values shift over time.

Overall, this work provides a practical framework for the design and experimental evaluation of efficient, bifurcation-free, and reliable WPT systems for electric vehicle charging, addressing both immediate performance optimization and long-term operational stability.

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Dedications

To my beloved wife, Methma, whose unwavering love, support, and encouragement have been my greatest strength throughout this journey.

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Nomenclature

AC	Alternating current
DC	Direct current
EV	Electric vehicle
WPT	Wireless Power Transfer
IPT	Inductive Power Transfer
ZPA	Zero Phase Angle
PFC	Power factor correction
SS	Series-Series
SP	Series-Parallel
PS	Parallel-Series
PP	Parallel-Parallel
ZVS	Zero voltage switching
ZCS	Zero current switching
EMF	Electromotive force
EMC	Electromagnetic compatibility
ESR	Equivalent series resistance

RMS	Root Mean Square
PoPs	Polarized pads
NPoPs	Non-polarized pads
DDP	Double D pads
DDQP	Double D quadrature pads
BP	Bipolar pads
FB	Full bridge

Chapter 1

Introduction

1.1 Background

Among the various innovations being explored, wireless charging has emerged as a promising solution to address the limitations of conventional wired charging. First, range anxiety—stemming from the comparatively limited driving range of Electric vehicles (EVs) relative to internal combustion engine vehicles—can be mitigated through opportunity charging, which enables brief, frequent energy top-ups at strategic locations such as intersections, bus stops, or parking lots. Second, by enabling opportunity charging, the required battery capacity can be reduced without sacrificing driving range, leading to lower upfront costs for end users. Third, wireless charging eliminates the need for manual plug-in connections, significantly improving safety and operational reliability [1]. As there are no exposed cables or connectors and the primary components can be installed underground, the system is less susceptible to environmental hazards such as rain or snow, thereby reducing maintenance needs and enhancing long-term durability [2–4].

Although wireless power transfer (WPT) has been demonstrated using various methods [5]—including acoustic [6], optical [7], capacitive [8], inductive [9], laser [10], and microwave-based systems [11]—literature consistently identifies inductive WPT as the most suitable approach for medium- to high-power applications [12]. Consequently, this thesis will focus exclusively on inductive WPT, and the term "WPT" used henceforth will refer specifically to this method.

WPT is a well-established concept with historical roots dating back to the late 19th and early 20th centuries. One of the earliest and most notable pioneers in wireless power transmission was Nikola Tesla, who conducted numerous experiments involving high-frequency oscillators, particularly for therapeutic and medical applications [13]. Tesla's work was influenced by Heinrich Hertz, whose experiments in 1888 provided the first empirical confirmation of electromagnetic wave propagation. These early experiments were among the first to demonstrate power transfer through a resonant inductive link, laying the foundational principles for most modern WPT systems. Although the fundamental technology has been known for over a century, it was only with recent advancements in materials science, power electronics, and semiconductor technology that its practical and widespread implementation became feasible. In response to the 1970s energy crisis, academic interest in EVs and inductive power systems was renewed, leading to initiatives such as the PATH program at the University of California, Berkeley during the 1980s [14]. In 1991, a research team at the University of Auckland, New Zealand, led by Boys and Green, directed their efforts toward high-power inductive power transfer (IPT) applications, particularly for powering movable systems [15]. Their work encompassed a comprehensive investigation into key aspects of IPT, including primary resonant converter topologies, compensation techniques for both primary and secondary circuits, optimal control strategies for the pickup unit, and the development

of multi-phase elongated primary tracks. They also examined complex dynamic behaviors in a WPT system, such as bifurcation phenomena [16, 17], where multiple zero phase angle (ZPA) frequencies can occur due to small variations in system parameters, leading to sudden qualitative changes in system behavior. More recently, the group has contributed significantly to the design of optimized charging pads for stationary EV applications [18].

The commercialization of stationary charging systems began between 1997 and 1998, initiated by the German company Conductix-Wampfler [19]. Following these foundational efforts, research in WPT has expanded substantially, with a focus on enhancing efficiency, reducing system costs, enabling dynamic charging, improving misalignment tolerance, optimizing charging pad geometries, exploring various compensation topologies, and developing advanced control strategies.

All WPT systems consist of a transmitter and a receiver separated by a gap. The transmitter is typically interfaced with power electronic circuitry that regulates power delivery, while the receiver is connected to secondary electronics that condition the received power before supplying it to the load. WPT operates fundamentally based on Ampère's circuital law and Faraday's law of electromagnetic induction. According to Ampère's law, an electric current flowing through a coil generates a magnetic field along a closed path surrounding the conductor. When the current in the primary coupler (transmitter) varies with time, it produces a time-varying magnetic flux that links with the secondary coupler (receiver). Faraday's law states that this changing magnetic flux induces an electromotive force (EMF) in the secondary coupler. The magnitude of the induced EMF can be expressed as $\mathcal{E}_s = -\frac{d\Phi}{dt}$, where $\Phi = MI_1$ is the magnetic flux linked with the secondary coil, M is the mutual inductance between the primary and secondary coils, and I_1 is the current in the primary coil. The rate of change of magnetic flux is proportional to the operating frequency of the pri-

mary coupler. Unlike conventional transformers, WPT systems operate under loose coupling conditions. In transformers, the primary and secondary windings are tightly wound around a shared magnetic core, resulting in minimal leakage flux and a high coupling coefficient. In contrast, WPT systems, especially for EV applications, typically feature a significant air gap between the transmitter and receiver coils, which increases leakage flux and reduces the mutual inductance M, generally resulting in a coupling coefficient of less than 0.5 [4]. Consequently, a high-frequency current is required in the primary coupler to generate a sufficiently high induced EMF in the secondary coupler.

Due to the inherently loose coupling in WPT systems, power transfer efficiency is often reduced. To mitigate this, capacitive compensation networks are employed on both the primary and secondary sides to offset the effects of leakage inductance, thereby enhancing the overall efficiency of power transfer as seen in Fig.2.1 [20]. The primary-side compensation circuit is designed to align the voltage and current phases at the input, thereby minimizing the apparent power (VA) rating and reducing the size requirements of the high-frequency power converter. Additionally, this compensation network serves as a band-pass filter, attenuating unwanted frequency components produced by the converter. As a result, the current in the primary coil approaches a near-sinusoidal waveform, which facilitates soft-switching operation of the primary-side converter and improves overall system efficiency. On the secondary side, compensation is also employed to counteract the inductive reactance of the receiver coil, thereby maximizing power transfer capability and improving overall efficiency [21–23].

Based on the configuration of compensation capacitors in the primary and secondary circuits, four fundamental compensation topologies are commonly used in WPT systems. These configurations are denoted using two-letter abbreviations, where the first letter represents the compensation type on the primary side and the second letter denotes the secondary

side. The four standard topologies are Series-Series (SS), Series-Parallel (SP), Parallel-Series (PS), and Parallel-Parallel (PP) [24]. Among these compensation strategies used in WPT systems, series compensation on the primary side—particularly in the SS topology—offers notable advantages. It eliminates the need for additional inductive components, reduces the voltage stress on the power supply by compensating the coil voltage drop, and maintains compensation characteristics independent of load variations [19]. This results in a simpler, more compact, and cost-effective system with high efficiency and minimal control complexity, making SS topology a preferred choice for many applications. On the other hand, topologies employing primary-side parallel compensation, such as PP and PS, enable high primary current operation with reduced semiconductor current stress. Despite this advantage, they introduce several practical challenges. These include the necessity for an external series inductor to regulate inverter current, leading to increased system size and cost [25]. Furthermore, the presence of circulating currents in the resonant tank diminishes efficiency under partial load conditions. Another critical drawback of PP and PS is the variability of the primary compensation capacitance with changes in mutual inductance and load, requiring advanced control techniques to maintain power factor correction [26]. While the SP topology can be advantageous in dynamic scenarios due to its flexibility, it demands higher capacitance under strong coupling conditions and typically achieves lower peak efficiency compared to the SS configuration [27]. Therefore, considering trade-offs between performance, complexity, and cost, the SS topology stands out as the most balanced and efficient approach for practical WPT system design and hence would be adopted in this study.

In recent years, several standards have been introduced to support the deployment of WPT technologies for EVs, among them, SAE J2954 [28] provides a comprehensive framework for light-duty plug-in EVs, specifying industry-accepted guidelines for interoperability,

electromagnetic compatibility (EMC), electromagnetic field (EMF) exposure, safety, performance benchmarks, and testing procedures. This standard specifically covers stationary charging scenarios, where the vehicle remains parked during power transfer. For wireless charging of heavy-duty vehicles, the SAE J2954/2 extension applies [29], while dynamic wireless charging—where vehicles receive power while in motion—is being addressed under the forthcoming SAE J2954/3 standard.

1.2 Problem Definition

Efficiency enhancement in WPT systems can be achieved through several approaches, with two primary focus areas: reducing transmission losses associated with the WPT coils; minimizing losses in power electronic components and converters Reducing transmission losses in WPT coils primarily involves optimizing key coil design parameters— such as geometry, size, and inter-coil spacing—to enhance magnetic coupling efficiency [30,31]. In addition, the use of appropriately selected litz wire is critical to minimizing AC resistance by mitigating both skin and proximity effects. Thoughtful design and implementation of electromagnetic shielding materials further reduce interference and related losses, contributing to improved overall performance [32].

Although considerable research has been devoted to the optimal design of coils for WPT-systems [33], [34], these studies generally overlook the impact of bifurcation, a phenomenon that can significantly reduce both efficiency and power transfer capability. In contrast, one widely referenced design approach focuses primarily on avoiding bifurcation, but does not explicitly aim to maximize efficiency [35]. Consequently, there remains a noticeable gap in the literature regarding coil design strategies that simultaneously address both objectives:

maximizing efficiency and avoiding bifurcation.

To bridge this gap, the present study proposes a design methodology that incorporates both efficiency optimization and bifurcation avoidance. Furthermore, this work compares the proposed approach with the widely adopted bifurcation-avoidance strategy to evaluate whether higher efficiency can be achieved while still preventing bifurcation.

To minimize losses in power electronic systems, several key strategies are employed, including the selection of components with low equivalent series resistance (ESR) and the reduction of switching losses. The latter can be achieved through soft-switching techniques such as zero-voltage switching (ZVS), zero-current switching (ZCS), and the adoption of advanced control methodologies [36, 37]. Among these, ZVS is particularly effective, as it significantly reduces switching losses in high-frequency converters—commonly used to achieve high power density—making it a preferred technique in modern high-efficiency designs. Consequently, significant research has been devoted to ensuring ZVS across the entire operational range of power converters. In this study, existing dead-time setting techniques are first experimentally verified on a high-power WPT setup to evaluate their effectiveness in sustaining ZVS and maximizing efficiency. Beyond this, the impact of capacitor tolerance and long-term aging in the primary compensation network is examined, with particular attention to how these variations influence both efficiency and the robustness of dead-time selection.

1.3 Research objectives

The primary goal of this thesis is to design and implement a 2 kW WPT prototype with a focus on enhancing overall power transfer efficiency. Given the broad range of factors that

influence efficiency in WPT systems—including coil design, power converter topology, control strategy, and magnetic shielding—it is impractical to address all these aspects within the scope of a single study. Therefore, this work focuses on two key areas: optimizing coil design and ensuring ZVS in the power electronic converters. These aspects are explored in detail in the subsequent chapters. To achieve this goal, the following objectives are formulated:

- Formulate and validate a systematic design approach for Archimedean spiral coils that optimizes power transfer efficiency while inherently mitigating bifurcation effects.
- Develop an experimental evaluation platform based on a 2kW series-compensated WPT system, facilitating detailed assessment of coil performance, efficiency enhancement strategies, and overall system behavior.
- Experimentally verify ZVS performance, examining the impact of capacitor tolerance and aging on efficiency and dead-time settings to provide actionable insights for maintaining reliable ZVS operation.

1.4 Thesis Organization

This thesis is organized into five chapters, structured to address the stated objectives and provide a logical progression from theoretical foundations to experimental validation and long-term reliability considerations.

- **Chapter 1: Introduction**

  This chapter introduces the motivation, scope, and objectives of the research. It outlines the challenges in achieving high-efficiency WPT and highlights the specific focus of this work on coil optimization and on the experimental verification of ZVS

performance, including the effects of capacitor tolerance and aging on efficiency and dead-time selection.

- **Chapter 2: Theoretical Background of Resonant Wireless Power Transfer**

  This chapter presents the fundamental principles of inductively coupled resonant WPT systems. It summarizes existing models and relationships for power transfer and efficiency under ideal conditions, establishing the theoretical foundation for subsequent coil design and performance studies.

- **Chapter 3: Coil Optimization and Experimental Verification Platform Development**

  This chapter details the design and optimization of identical Archimedean spiral coils with series compensation. The methodology focuses on selecting coil parameters to maximize efficiency while avoiding bifurcation. The proposed design approach is novel in that it simultaneously achieves high efficiency and bifurcation-free operation, addressing a gap in conventional coil design methods. The chapter also describes the development of a 2 kW experimental platform that allows detailed evaluation of coil performance and overall system behavior under realistic operating conditions.

- **Chapter 4: Zero-Voltage Switching Performance under Capacitor Aging and Tolerance Effects**

  This chapter develops a methodology to ensure reliable ZVS in resonant converters by explicitly considering the impacts of capacitor aging and manufacturing tolerances. Experimental investigations are used to evaluate dead-time selection and compensation design, ensuring sustained ZVS and efficient operation throughout the system's lifetime.

- **Chapter 5: Concluding Remarks**

The final chapter summarizes the key contributions and findings of the thesis. It reflects on the effectiveness of the proposed novel coil optimization approach and aging/tolerance-aware ZVS methodology, and outlines potential directions for future research to further improve the efficiency, robustness, and scalability of WPT systems.

Chapter 2

Theoretical Background of Resonant Wireless Power Transfer

2.1 Overview of Common Coil Geometries

In recent years, WPT has gained considerable traction as a viable solution for EV charging, offering the potential for safe, efficient, and user-friendly energy transfer without the need for physical connectors. A critical component in any WPT system is the pair of charging pads—comprising transmitter and receiver coils—that form the wireless link. The geometry, structure, and placement of these coils directly impact the overall system efficiency, coupling strength, misalignment tolerance, and suitability for vehicular integration. Earlier WPT designs often relied on magnetically structured cores, such as EE type cores, UU type cores, and pot cores, to enhance magnetic coupling [38–40]. While these core-based configurations can deliver strong coupling performance, they introduce several challenges in the context of EV applications. Notably, achieving sufficient magnetic flux with these structures typically

requires increased core thickness, which compromises the ground clearance of the vehicle and may necessitate significant structural modifications to the EV chassis. Moreover, such cores are generally heavy, expensive, and mechanically fragile, making them unsuitable for practical deployment in dynamic or mobile environments. They are also highly sensitive to horizontal misalignments, leading to degraded performance under real-world usage conditions [41].

In contrast, WPT systems for transportation applications predominantly use planar coils, as they offer clear advantages over core-based designs. Because planar coils are lightweight and structurally simple, they typically forego bulky magnetic cores, and their distributed winding geometry provides improved tolerance to lateral and angular misalignment. The absence of a magnetic core, together with the inherently flat coil structure, enables a low-profile design that preserves vehicle ground clearance—an important secondary advantage in EVs. As a result, planar WPT coils have become the preferred solution in modern EV charging systems, addressing many of the shortcomings of earlier core-based designs while aligning with the demands of mass-market electric mobility.

Planar coils are typically categorized into two main types: non-polarized pads (NPoPs) and polarized pads (PoPs). Each category has unique characteristics that affect coupling behavior and system performance. NPoPs, such as circular and square coil structures, use a single coil to produce magnetic flux primarily in the vertical direction. These designs are structurally straightforward and less costly to implement. While NPoPs may have limited tolerance to misalignment, they are generally sufficient for stationary charging setups, where vehicles are parked within a predictable alignment window.

On the other hand, PoPs incorporate multiple coils to create flux components in both vertical and horizontal directions, enhancing their ability to maintain power transfer under

misalignment. Designs like the Double D (DDP), Double D Quadrature (DDQP), and Bipolar (BP) pads fall into this category [42, 43]. These configurations offer improved lateral and longitudinal misalignment performance, making them better suited for dynamic charging scenarios.

However, PoPs introduce several design challenges. They typically require complex control schemes, dual inverter/rectifier circuits, and precise synchronization, all of which add cost and system complexity. Additionally, their performance is more sensitive to angular misalignments, which can significantly reduce coupling efficiency [44].

For static EV charging, where the vehicle is stationary and alignment can be controlled to a reasonable degree (though not perfectly), using manual guidance aids or assisted parking systems, NPoPs offer a practical and cost-effective solution. Their simplicity, adequate performance, and ease of integration make them ideal for such applications, despite having a narrower tolerance for positional errors.

2.2 Electrical Modeling of a Series-Compensated WPT System

Fig. 2.1 illustrates the system model of a single-phase SS compensated WPT system. The primary side is typically powered by a DC source, which may be derived through a power factor correction (PFC) stage interfaced with the AC grid. This DC link voltage is then modulated using a high-frequency inverter, which drives the series-compensated primary coil. The magnetic field generated is wirelessly coupled to the series-compensated secondary coil, where the induced AC voltage is subsequently rectified by a full-bridge rectifier and filtered by a capacitor, C_r. The resulting DC power is then supplied to the load—typically

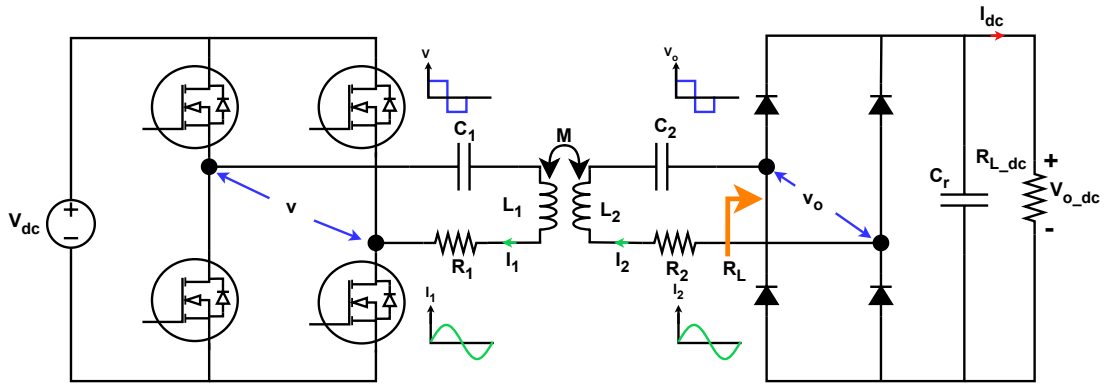

Fig. 2.1: Series–Series compensated wireless power transfer model

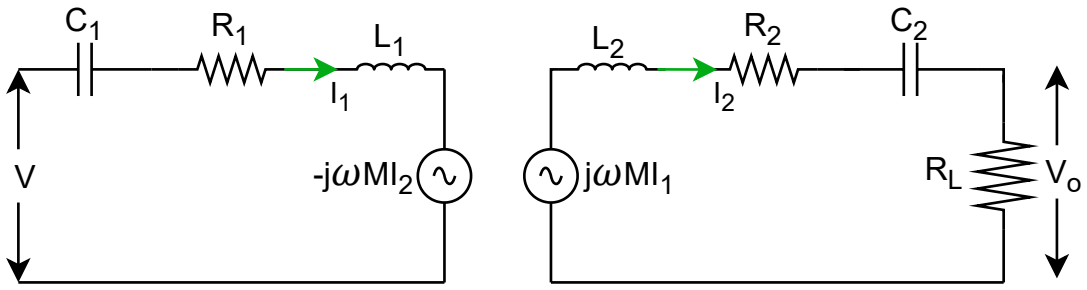

Fig. 2.2: Equivalent circuit of the Series–Series compensated wireless power transfer model

the EV battery—either directly or through an additional power conversion stage, depending on system requirements. Fig. 2.2 shows it's equivalent circuit. The variables in Fig. 2.1 are presented in Table 2.1. Subscripts "1" and "2" denote the primary and secondary sides, respectively.

The DC voltage on the primary side is typically modulated by an inverter, resulting in a square-wave voltage waveform at the switching frequency, as illustrated in Fig. 2.1. This waveform contains an infinite number of harmonics, as described by its Fourier series representation.

Table 2.1: Variables used in WPT model

Symbol	Description
V_{dc}	Primary DC supply voltage
v	High-frequency primary input voltage
v_o	High-frequency secondary output voltage
C_1	Primary compensation capacitance
C_2	Secondary compensation capacitance
L_1	Primary coil self-inductance
L_2	Secondary coil self-inductance
R_1	AC equivalent series resistance (ESR) of primary coil
R_2	AC equivalent series resistance (ESR) of secondary coil
M	Mutual inductance between coils
I_1	Primary resonant tank current
I_2	Secondary resonant tank current
C_r	DC output filter capacitance
I_{dc}	Output DC current
R_{L_dc}	Load resistance
v_{o_dc}	DC output voltage
R_L	AC equivalent load resistance

As discussed in Section 1.1, a series compensation capacitor is introduced on the primary side to align the voltage and current phases, thus minimizing the apparent power (VA) requirement. This is achieved by selecting a capacitor bank such that the self-inductance of the primary coil is fully compensated at the chosen switching frequency, as defined by (2.1).

$$\omega_s = \frac{1}{\sqrt{L_1 C_1}} \tag{2.1}$$

In other words, the compensation capacitance is selected so that the primary coil and the compensation network form a resonant circuit tuned to the switching frequency. Additionally, this primary-side compensation capacitance attenuates the unwanted harmonics generated

by the inverter, effectively functioning as a sharply tuned band-pass filter. As a result, the current in the primary-side resonant tank becomes nearly sinusoidal.

Similarly, on the secondary side, the self-inductance of the secondary coil is tuned to resonate at the switching frequency using compensation capacitor banks. This resonance removes reactive impedance at the selected switching frequency, thereby maximizing power transfer capability. The relationship between the self-inductance of the secondary coil and the secondary-side compensation capacitance is defined by (2.2).

$$\omega_s = \frac{1}{\sqrt{L_2 C_2}} \tag{2.2}$$

For the purpose of simplifying the analytical derivation process, the following set of assumptions has been adopted. These assumptions, which are widely recognized and well-established within the existing body of literature, facilitate the formulation of the governing equations while maintaining sufficient accuracy for the intended analysis.

- Both the primary and secondary sides operate at ideal resonance; that is, for the fundamental frequency, the impedance on each side is purely resistive, as the reactive impedance of the coils is fully compensated by the respective compensation capacitors.
- Only the fundamental component of the voltage waveforms v and v_o is considered, while the influence of all higher-order harmonics are neglected.
- All switching devices are ideal, exhibiting zero on-state resistance (no conduction losses) and instantaneous switching with no commutation delay. Furthermore, parasitic capacitances across the switches are neglected.
- All diodes within the rectifier bridge, as well as the output filter capacitor, are consid-

ered ideal components without any parasitic resistance, resulting in a lossless operation.

From Fourier series analysis, the high-frequency primary input voltage can be derived as (2.3) [45].

$$v = \frac{4V_{dc}}{\pi} \sum_{a=1,3,5...} \frac{1}{a} \sin(aw_s t) \tag{2.3}$$

Therefore, the root mean square (RMS) value of the fundamental component of the primary voltage, v_{rms}, can be derived as (2.4).

$$v_{rms} = 2\sqrt{2}\frac{V_{dc}}{\pi} \tag{2.4}$$

As outlined in [46], when a DC resistive load is supplied through a diode rectifier followed by a capacitive output filter, its AC equivalent can be represented by (2.5). This equivalent corresponds to the effective resistance observed from the secondary side of the WPT system, as shown in Fig. 2.2.

$$R_L = \frac{8}{\pi^2} R_{L\_dc} \tag{2.5}$$

Furthermore, for a given output power P_o, this can be expressed as (2.6).

$$R_L = \frac{8}{\pi^2} \frac{V_{o\_dc}^2}{P_o} \tag{2.6}$$

Under the assumption $\omega_s = \frac{1}{\sqrt{L_1 C_1}} = \frac{1}{\sqrt{L_2 C_2}}$ and applying Kirchhoff's voltage law to the equivalent circuit shown in Fig. 2.2, we obtain equations (2.7) and (2.8).

$$v = I_1 R_1 - j\omega M I_2 \tag{2.7}$$

$$j\omega M I_1 = I_2(R_2 + R_L) \tag{2.8}$$

Solving (2.7) and (2.8) to find I_2, we derive

$$|I_2| = \frac{\omega M v}{R_1(R_2 + R_L) + \omega^2 M^2} \tag{2.9}$$

Based on the aforementioned assumptions, for a given output power P_o, (2.10) holds true.

$$P_0 = |I_2|^2 R_L \tag{2.10}$$

From (2.9) and (2.10) we can derive (2.11)

$$P_0 = \frac{\omega^2 M^2 v^2}{[R_1(R_2 + R_L) + \omega^2 M^2]^2} R_L \tag{2.11}$$

In a similar manner, by making use of the relationships expressed in (2.7) and (2.8), the expression for the primary current, I_1, can be derived and is shown in (2.12).

$$|I_1| = \frac{(R_2 + R_L)v}{R_1(R_2 + R_L) + \omega^2 M^2} \tag{2.12}$$

Referring to the equivalent circuit illustrated in Fig. 2.2, the expression for the input power drawn from the DC source can be derived. This resulting formulation is presented in (2.13).

$$P_{in} = v|I_1| \tag{2.13}$$

From (2.12) and (2.13), the expression in (2.14) is obtained.

$$P_{in} = \frac{(R_2 + R_L)v^2}{R_1(R_2 + R_L) + \omega^2 M^2} \tag{2.14}$$

By utilizing the derived mathematical expressions for both the input power supplied to the system and the output power delivered to the load, the overall system efficiency (η) can be formally defined. In this context, efficiency is expressed as the ratio of output power to input power as presented in (2.15).

$$\eta = \frac{P_o}{P_{in}} \tag{2.15}$$

By substituting the expressions from (2.11) and (2.14) into the efficiency formulation, the resulting relationship is obtained and presented in (2.16).

$$\eta = \frac{R_L}{[R_L + R_2 + R_1 \frac{(R_L+R_2)^2}{\omega^2 M^2}]} \tag{2.16}$$

From (2.11), it can be observed that, for a fixed switching frequency ω, mutual inductance M, and AC-equivalent load resistance R_L, the output power is governed primarily by the magnitude of the input high-frequency voltage. This is due to the fact that the parasitic resistances R_1 and R_2 are considered constant throughout the power transfer process, thereby not influencing the variability of the output power under these operating conditions. Consequently, the output power becomes a function of the input DC voltage V_{dc} and the duty ratio of the inverter, since these parameters directly determine the amplitude of the high-frequency voltage applied to the primary side of the WPT system.

Furthermore, from the relationship expressed in (2.16), it can be observed that the system efficiency is independent of the input voltage. Accordingly, when considered alongside the

previously discussed findings, it can be concluded that the efficiency is also independent of the amount of power transferred. This implies that, under the stated assumptions, variations in the transferred power—resulting from changes in the input voltage—do not influence the efficiency of the WPT system.

2.2.1 Optimal Load Resistance for Efficiency Maximization

In a typical WPT system, the switching frequency and the mutual inductance are generally fixed during the power transfer process. Under these conditions, as indicated by the relationship in (2.16), the system efficiency becomes predominantly dependent on the load resistance R_L. To determine the specific value of R_L that maximizes efficiency, the standard approach involves differentiating the efficiency expression in (2.16) with respect to R_L and setting this derivative equal to zero. This optimization condition is mathematically expressed in (2.17), which yields the load resistance value corresponding to the peak efficiency of the system $R_{L\_\eta m}$ as presented in (2.18).

$$\frac{d\eta}{dR_L} = 0 \tag{2.17}$$

$$R_{L\_\eta m} = \sqrt{\frac{R_2\omega^2 M^2}{R_1} + R_2^2} \tag{2.18}$$

By substituting (2.18) into (2.16), the maximum efficiency attainable for a given switching frequency and mutual inductance, η_m can be obtained as shown in (2.19).

$$\eta_m = \frac{R_{L\_\eta m}}{[R_{L\_\eta m} + R_2 + R_1\frac{(R_{L\_\eta m}+R_2)^2}{\omega^2 M^2}]} \tag{2.19}$$

The variation of output power delivered to the selected load resistance, corresponding

to the maximum efficiency $R_{L\_\eta m}$, as a function of v,ω,M,R_1,R_2 can be expressed as (2.20).

$$P_{0\_\eta m} = \frac{\omega^2 M^2 v^2}{[R_1(R_2 + R_{L\_\eta m}) + \omega^2 M^2]^2} R_{L\_\eta m} \tag{2.20}$$

Based on (2.20) and (2.4), DC input voltage required for a set output power can be given by (4.9)

$$V_{dc} = \frac{\pi}{2\sqrt{2}} \frac{[R_1(R_2 + R_{L\_\eta m}) + \omega^2 M^2]}{\omega M} \sqrt{\frac{P_{0\_\eta m}}{R_{L\_\eta m}}} \tag{2.21}$$

2.2.2 Optimal Load Resistance for Output Power Maximization

To determine the value of R_L that yields the maximum output power, a similar procedure to the efficiency optimization process can be employed. In this approach, the standard method involves differentiating the output power expression given in (2.11) with respect to the load resistance, R_L. For convenience in simplifying the mathematical operations, a new variable A is defined as in (2.23), allowing (2.11) to be reformulated into the equivalent form shown in (2.24). Differentiating this reformulated expression with respect to R_L results in the derivative presented in (2.25). To determine the condition for maximum output power, this derivative is then set equal to zero. By solving the resulting equation for R_L and carrying out the algebraic simplifications, as illustrated in ((2.26)–(2.28)), the final expression for the load resistance that maximizes the output power, $R_{L\_p_o m}$ is obtained, as presented in (2.29).

$$A = R_1(R_2 + R_L) + \omega^2 M^2 \tag{2.22}$$

$$B = \omega^2 M^2 v^2 \tag{2.23}$$

$$P_o = \frac{B}{A^2} R_L \tag{2.24}$$

$$\frac{dP_o}{dR_L} = \frac{A^2 B - B R_L 2 A R_1}{A^4} \tag{2.25}$$

$$\frac{A^2 B - B R_L 2 A R_1}{A^4} = 0 \tag{2.26}$$

$$A = 2 R_1 R_L \tag{2.27}$$

$$R_1 R_2 + R_1 R_L + \omega^2 M^2 = 2 R_1 R_L \tag{2.28}$$

$$R_{L\_p_o m} = R_2 + \frac{\omega^2 M^2}{R_1} \tag{2.29}$$

Substituting (2.29) in (2.11), the maximum output power obtainable for a given switching frequency, mutual inductance, and voltage, P_{0_m} can be expressed as (2.30).

$$P_{0\_m} = \frac{\omega^2 M^2 v^2}{[R_1 (R_2 + R_{L\_p_o m}) + \omega^2 M^2]^2} R_{L\_p_o m} \tag{2.30}$$

By comparing $R_{L\_p_o m}$ and $R_{L\_\eta m}$, as presented in (2.29) and (2.18) respectively, it is evident that the value of load resistance that maximizes the output power transfer is not the same as the load resistance that maximizes efficiency. This distinction highlights that the optimal load resistance is dependent on the design objective. In practice, the designer must select the appropriate R_L value based on the specific performance target—whether

the priority is maximizing power transfer or achieving the highest possible efficiency. Since one of the primary objectives of this thesis is to maximize efficiency, the load resistance corresponding to the efficiency-maximizing condition has been selected, as determined from (2.18), for use in the design process described in the following chapter.

2.2.3 Efficiency Maximization with Identical Archimedean Spiral Coils

Starting from the load resistance expression given in (2.18), it can be reformulated as (2.31).

$$R_L = R_2\sqrt{1+\frac{\omega^2 M^2}{R_1 R_2}} \tag{2.31}$$

Introducing a normalized variable u as defined in (2.32), the load resistance can be expressed more compactly as (2.33).

$$u = \frac{\omega^2 M^2}{R_1 R_2} \tag{2.32}$$

$$R_L = R_2\sqrt{1+u} \tag{2.33}$$

The denominator of the efficiency expression in (2.16) can be rearranged into the form given in (2.34).

$$D = (R_L + R_2)\left[1+\frac{R_1}{\omega^2 M^2}(R_L+R_2)\right] \tag{2.34}$$

Furthermore, (2.31) can be manipulated to yield the quadratic relation in (2.35), which in turn gives the simplified form of (2.36).

$$(R_L - R_2)(R_L + R_2) = R_2 \frac{\omega^2 M^2}{R_1} \tag{2.35}$$

$$\frac{R_1}{\omega^2 M^2}(R_L + R_2) = \frac{R_2}{(R_L - R_2)} \tag{2.36}$$

Substituting (2.36) into (2.34), the efficiency expression simplifies to the well-known form in (2.37), and in terms of u, as (2.38).

$$\eta_m = \frac{R_L - R_2}{R_L + R_2} \tag{2.37}$$

$$\eta_m = \frac{\sqrt{1+u} - 1}{\sqrt{1+u} + 1} \tag{2.38}$$

For planar Archimedean spiral coils, the inductance and resistance can be approximated as

$$L_i \approx a N_i^2, \quad R_i \approx p N_i \quad (i = 1, 2) \tag{2.39}$$

The mutual inductance is expressed as

$$M = k\sqrt{L_1 L_2} = k a N_1 N_2 \tag{2.40}$$

which gives

$$M^2 = k^2 a^2 N_1^2 N_2^2 \tag{2.41}$$

and

$$R_1 R_2 = p^2 N_1 N_2 \tag{2.42}$$

Thus, the normalized variable u becomes

$$u = \frac{\omega^2 k^2 a^2}{p^2} N_1 N_2 = C N_1 N_2 \tag{2.43}$$

Defining $t = \sqrt{1+u} > 0$, the efficiency can be rewritten as

$$\eta_m = \frac{t-1}{t+1} \tag{2.44}$$

The derivative of efficiency with respect to u is

$$\frac{d\eta_m}{du} = \frac{1}{t(t+1)^2} > 0 \tag{2.45}$$

indicating that efficiency is a strictly increasing function of u.

Now, imposing the constraint of a fixed total turn count

$$N_1 + N_2 = T \tag{2.46}$$

and applying the AM–GM inequality, we obtain

$$N_1 N_2 \leq \left(\frac{N_1 + N_2}{2}\right)^2 = \left(\frac{T}{2}\right)^2 \tag{2.47}$$

with equality if and only if $N_1 = N_2 = T/2$. Since $u = C N_1 N_2$, it follows that u is maximized when $N_1 = N_2$, thereby maximizing efficiency.

$$\eta_m^{\max} \quad \text{when} \quad N_1 = N_2 \tag{2.48}$$

It can therefore be concluded that, under the assumptions of fixed coil geometry, planar Archimedean spiral layout, linear resistance scaling with turn count, and constant coupling coefficient k, maximum power transfer efficiency is achieved when the coils are identical, i.e., $N_1 = N_2$. In particular, identical Archimedean spiral coils maximize the product $N_1 N_2$ and thereby the coupling-dependent parameter u, yielding superior efficiency compared to asymmetric coil configurations. This derivation provides a novel analytical proof of a principle that is often assumed in WPT literature but rarely formally justified, and it forms the theoretical basis for the coil optimization adopted in this thesis.

2.3 Summary

This chapter laid out the theoretical groundwork and analytical models essential for understanding an inductively coupled WPT system. The analysis was built around an ideal resonant system where the reactive components of both the primary and secondary sides are perfectly compensated, so that only resistive elements affect power transfer. To simplify the study, parasitic resistances were treated as fixed, and only the fundamental frequency of the inverter's output voltage was considered, disregarding higher harmonics.

The discussion focused on two primary metrics: system efficiency and output power. Under stable operating conditions—specifically a fixed switching frequency and mutual inductance—it was demonstrated that efficiency depends mainly on the load resistance, not on the input voltage or the absolute power level. By analyzing how efficiency varies with load resistance, the value that leads to peak efficiency was determined. Similarly, the load

resistance that maximizes output power was identified by examining how power changes with load.

This comparison revealed an important design consideration: the load resistance that maximizes power transfer is different from the one that optimizes efficiency. Therefore, the selection of load resistance must align with the system's intended goal. If the priority is maximizing efficiency, the load resistance should be set accordingly, even if this means sacrificing some power delivery. Conversely, if the main goal is to maximize power output, a different load resistance value should be chosen.

In addition, by analyzing the dependence of efficiency on coil parameters, it was shown that for a fixed total number of turns, efficiency is maximized when the transmitting and receiving coils are identical. This is because identical coils maximize the product of turn numbers, thereby maximizing the coupling-dependent parameter and improving efficiency. Consequently, this thesis adopts identical Archimedean spiral coils as the foundation for optimization. Notably, while the principle of using identical coils is often assumed in WPT literature, the analytical proof presented here provides a novel formal justification that has not been explicitly demonstrated before.

The standard equations presented in this chapter have been extensively validated in existing literature, while the analytical derivation showing that identical coils maximize efficiency under a fixed total turn constraint is a novel contribution. Together, these results establish a solid theoretical foundation that supports the analysis and design decisions discussed in the next chapter, ensuring that the system is optimized according to the specified performance criteria.

Chapter 3

Coil Optimization and Experimental Verification Platform Development

3.1 Bifurcation Phenomena and Existing Approaches for Coil Optimization in WPT Systems

3.1.1 Bifurcation Phenomena

A SS WPT arrangement constitutes for doubly tuned network, formed by placing reactive compensation capacitors across both the primary and secondary coils to create two distinct resonant tanks. In such dual-resonant systems it is possible for the input impedance phase to cross zero at more than one frequency; this multiplicity of zero-phase-angle (ZPA) frequencies is commonly referred to as bifurcation or pole splitting [16], [17], [47], [48]. Because the theory and derivation of pole splitting are well established in existing literature, they are not reproduced in detail here. Practically, however, avoiding bifurcation is important for

preserving both stable power transfer and high efficiency. A commonly used design constraint to prevent pole splitting is to keep the coupling coefficient below a threshold value [35], i.e.

$$k < k_{\text{crit}}$$

where,

$$k = \sqrt{\frac{M}{L_1 L_2}}$$

which for SS resonant systems can be expressed in terms of the secondary quality factor as (3.1), where Q_2 is the loaded quality factor of the secondary circuit, defined as (3.2).

$$k \ < \ \frac{1}{Q_2}\sqrt{1 - \frac{1}{4Q_2^2}} \tag{3.1}$$

$$Q_2 \ = \ \frac{\omega L_2}{R_2 + R_L} \tag{3.2}$$

Designing to satisfy these inequalities helps ensure a single, well-defined resonant response and thus reliable power-transfer performance.

3.1.2 Review of Existing Coil Optimization Approaches

[34] presents a coil–coil efficiency maximization framework based on a particle swarm optimization (PSO) algorithm, supported by analytical expressions for AC resistance and mutual inductance tailored to identical coil geometries. The optimization enforces practical design limits such as required output power, specified load resistance, and a fixed outer coil diameter. [33] proposes a complementary strategy that maximizes the receiver quality factor under constraints on the receive-coil size. By prioritizing a high Q in the receiver, this latter

approach effectively reduces the critical coupling threshold, increasing the likelihood that the operating coupling exceeds k_{crit} and thereby induces pole splitting (bifurcation) at lower overall efficiency. Neither work, however, explicitly incorporates bifurcation avoidance as an objective during the design phase; consequently, both methods may yield designs that are vulnerable to reduced power-transfer capability and degraded efficiency when operated beyond the critical coupling coefficient.

In contrast, the design procedure proposed in [35] emphasizes bifurcation avoidance rather than explicit maximization of power-transfer efficiency. In this method the input and output voltages and the required output power are prescribed, and the load resistance is determined based on (3.3). A receiver quality factor Q_2 is then selected—typically between 2 and 10—and the secondary inductance L_2 is computed from the chosen Q_2 and the calculated load, determined based on (3.4). The target mutual inductance M is subsequently obtained using (3.5)–(3.7), and the critical coupling k_{crit} corresponding to the selected Q_2 is evaluated using (3.1). A working coupling satisfying $k < k_{\text{crit}}$ is then prescribed to avoid pole splitting, and the primary inductance L_1 is chosen so that the required mutual coupling M can be realized, as given by (3.8).

$$R_L = \frac{v_{o\_rms}^2}{P_0} \tag{3.3}$$

$$L_2 = \frac{Q_2 R_L}{\omega_0} \tag{3.4}$$

$$I_{2\_rms} = \frac{v_{o\_rms}}{R_L} \tag{3.5}$$

$$I_{1\_rms} = \frac{P_o}{v_{rms}} \tag{3.6}$$

$$M = \frac{I_{2\_rms} R_L}{I_{1\_rms} \omega} \tag{3.7}$$

$$L_1 = \frac{M^2}{L_2 k^2} \tag{3.8}$$

In practice, coils are fabricated to the specified inductances and the intercoil air gap is adjusted post-fabrication to achieve the computed mutual inductance, with the air gap serving as the principal degree of freedom [35]. While this workflow reliably prevents bifurcation by design, it does not directly optimize for maximum efficiency and can therefore yield conservative designs with suboptimal power-transfer performance. Additionally, in the context of EV charging—where the intercoil spacing is often constrained by vehicle ground clearance rather than by coil design—the air gap required to ensure $k \leq k_{\text{crit}}$ (i.e., the minimum spacing that guarantees bifurcation-free operation) may exceed the vehicle's available clearance. Consequently, the charger may be forced to operate in the over-coupled (bifurcation) regime, resulting in reduced power-transfer capability and lower efficiency.

Therefore, it is evident that existing approaches either emphasize efficiency or focus on bifurcation avoidance, but rarely address both objectives concurrently. This highlights a gap in the current literature for coil design methodologies that simultaneously maximize efficiency while ensuring bifurcation-free operation at the design stage.

3.2 Proposed Efficiency Optimization Approach Subject to Bifurcation Avoidance $(k/k_{\text{crit}} < 1)$

3.2.1 Parameter Sensitivity Analysis for Bifurcation Avoidance

From the relationships in (3.1) and (3.2), it is clear that in optimization approaches where the coupling coefficient k cannot be directly controlled, bifurcation can still be suppressed by increasing the critical coupling k_{crit}, which corresponds to reducing the quality factor Q_2. Examining (3.2), four parameters influence Q_2. In practice, the operating frequency ω is fixed to meet system specifications, while the secondary inductance L_2 is difficult to adjust after coil fabrication. In contrast, R_2 and R_L can be easily modified by adding series resistance, making them the practical variables for adjusting Q_2.

Increasing either of these resistances, however, comes at the cost of reduced efficiency. A higher R_2 increases conduction losses, thereby lowering efficiency as indicated in (2.16). Conversely, increasing R_L shifts the operating point away from the optimal load resistance R_{L,η_m}, which is typically selected in efficiency-oriented design methodologies, thus also reducing efficiency.

Consequently, to achieve a balance between bifurcation avoidance and efficiency maximization, it is necessary to evaluate the relative impact of varying R_2 versus R_L on system performance. The parameter with the lesser adverse effect on efficiency should then be selected as the adjustment variable to suppress bifurcation while maintaining high efficiency.

From (2.16), let us define

$$S = R_L + R_2, \quad \beta = \frac{R_1}{\omega^2 M^2}. \tag{3.9}$$

Then the denominator of the efficiency expression can be written as

$$D = S + \beta S^2 = S(1 + \beta S), \tag{3.10}$$

so that the efficiency becomes

$$\eta = \frac{R_L}{D} = \frac{R_L}{S(1 + \beta S)}. \tag{3.11}$$

The derivative of η with respect to R_L is

$$\frac{d\eta}{dR_L} = \frac{D - R_L(1 + 2\beta S)}{D^2} = \frac{S(1 + \beta S) - R_L(1 + 2\beta S)}{D^2} = \frac{R_2 + \beta S(R_2 - R_L)}{D^2}, \tag{3.12}$$

and the derivative with respect to R_2 is

$$\frac{d\eta}{dR_2} = -\frac{R_L(1 + 2\beta S)}{D^2}. \tag{3.13}$$

To compare the relative impact of R_L and R_2 on efficiency, the derivatives are normalized using the relative sensitivity,

$$S_x = \frac{x}{\eta}\frac{d\eta}{dx}. \tag{3.14}$$

Hence, the relative sensitivities are

$$S_{R_L} = \frac{R_L}{\eta}\frac{d\eta}{dR_L} = \frac{R_2 + \beta S(R_2 - R_L)}{D}, \quad S_{R_2} = \frac{R_2}{\eta}\frac{d\eta}{dR_2} = -\frac{R_2(1 + 2\beta S)}{D}. \tag{3.15}$$

Comparing the magnitudes of the sensitivities gives

$$\frac{S_{R_L}}{-S_{R_2}} = \frac{R_2 + \beta S(R_2 - R_L)}{R_2(1 + 2\beta S)}. \tag{3.16}$$

Subtracting numerator from denominator yields

$$R_2(1+2\beta S) - [R_2 + \beta S(R_2 - R_L)] = \beta S^2 \geq 0, \tag{3.17}$$

with equality only if $\beta = 0$, i.e., $R_1 = 0$. For any physical system where $R_1 > 0$ ($\beta > 0$), it follows that

$$\frac{S_{R_L}}{-S_{R_2}} < 1 \quad \Rightarrow \quad |S_{R_2}| > S_{R_L}. \tag{3.18}$$

Therefore, efficiency is more sensitive to changes in R_2 than to changes in R_L. Consequently, in order to minimize the impact on efficiency while ensuring bifurcation is avoided, it is preferable to increase R_L rather than R_2.

3.2.2 Proposed Efficiency Optimization Approach Incorporating Bifurcation Avoidance

In EV WPT systems, the load resistance R_L is typically much larger than the primary and secondary coil resistances (R_1 and R_2), reflecting the high-power delivery requirements relative to coil losses. Furthermore, as established in Section 2.2.3, the use of identical coils for efficiency maximization leads to $R_1 = R_2$. Under these conditions, (2.18) simplifies to (3.19), and similarly, (2.19) reduces to (3.20).

$$R_{L_{\eta m}} \approx \omega M \tag{3.19}$$

$$\eta_m \approx \frac{1}{[1 + R_1(\frac{R_{L\_\eta m}}{\omega^2 M^2})]} \tag{3.20}$$

By substituting (3.19) into (3.20), (3.21) is derived.

$$\eta_m \approx \frac{1}{1 + \frac{R_1}{\omega M}} \tag{3.21}$$

From (3.21), it can be observed that, within a specified operational frequency range, system efficiency varies with the switching frequency. Selecting the upper end of this range, i.e., maximizing the switching frequency, further enhances efficiency. For a fixed frequency, efficiency is also improved when the ratio R_1/M is minimized. After minimizing this term and selecting the optimal frequency within the design constraints, it is necessary to verify that bifurcation is avoided by ensuring the operating coupling satisfies $k < k_{\text{crit}}$. If this condition is not met, as discussed in Section 3.2.1, the load resistance R_L can be increased to suppress bifurcation, thereby enabling both maximum efficiency and bifurcation-free operation by design. In the context of WPT systems for EV charging, increasing R_L for a fixed output power corresponds to raising the output voltage, which can be readily achieved and fine-tuned through a supervisory control loop if required.

3.2.3 Fixed parameter selection

Typically, when designing a WPT system for an EV, some parameters are predetermined and fixed, while others can be selected based on the design objectives. In the design procedure proposed in [35], which emphasizes bifurcation avoidance, the input and output voltages are treated as fixed parameters, while the intercoil air gap is adjusted to achieve the desired coupling. For practical applications such as EV wireless charging, it is more effective to treat the minimum air gap as a fixed design parameter and allow the input and output voltages to vary within safe limits. This approach is preferable because adjusting the voltages via power converters is significantly easier than altering the physical air gap – which is constrained by

vehicle ground clearance – to ensure bifurcation-free operation.

Based on the considerations outlined above, the following parameters were selected as fixed for the design:

- **Rated output power** — SAE J2954, which covers WPT for light-duty vehicles, defines Power Class WPT1 as ranging from 0 to 3.7 kVA. For this work, an input power level of 2 kW was selected to align with the WPT1 class while balancing safety and practicality in the laboratory. This level is sufficient to demonstrate meaningful performance characteristics—such as efficiency variation and magnetic coupling behavior—without requiring specialized high-power test equipment or introducing excessive electrical hazards to personnel.

- **Air gap between coils** — An air gap of $15cm$ was selected to align with typical ground clearances observed in light-duty EVs. For instance, the Tesla Model 3 has a ground clearance of approximately $140mm$ [49], and the BYD Atto 3 reports a ground clearance of around $175mm$ [50]. Selecting $150mm$ ensures compatibility with most vehicle platforms while maintaining efficient magnetic coupling under realistic installation constraints.

- **Switching frequency** — SAE J2954 for light duty vehicles recommends a switching frequency range of 79 kHz to 90 kHz for WPT systems [28]. Typically, switching losses remain low because of soft switching implemented through ZVS or ZCS. Therefore, the efficiency improvement gained by increasing the switching frequency according to (3.21), outweighs the efficiency loss due to switching losses. Consequently, a switching frequency of 90 kHz was selected to maximize efficiency while staying within the standard's specified limits.

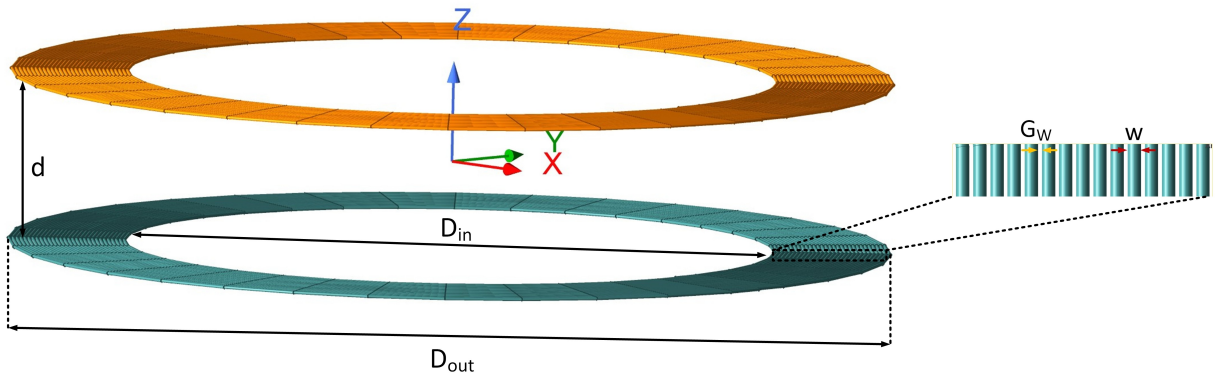

Fig. 3.1: Archimedean spiral coil arrangement for WPT setup

- **Maximum DC input voltage** — Typical DC fast-charging stations for EVs operate with DC bus voltages in the range of approximately $400V$ to $1000V$ [51]. In this work, the maximum DC voltage was conservatively limited to $600V$ ensuring a safe margin below the upper extreme. Nonetheless, the system design permits operation at any input voltage up to this maximum threshold, providing flexibility in adapting to varying conditions.

After selecting the fundamental fixed parameters, the next step is to choose the design-specific fixed parameters. This thesis focuses on the optimization of non-polarized planar identical Archimedean spiral coils. Identical coils were selected, as they have been shown to maximize efficiency, as demonstrated in Section 2.2.3.

As illustrated in Fig. 3.1, several key geometrical parameters define Archimedean spiral coils. These include the outer diameter D_{out}, inner diameter D_{in}, air gap between coils d, diameter of the wire w, number of turns N, and the spacing between each turn G_w. Each of these parameters influences the ratio R_1/M, which directly impacts system efficiency, and must therefore be carefully considered in the design process. Since it is impractical to

vary all geometrical parameters simultaneously to observe their effects, this study focuses on determining the number of turns N that minimizes the R_1/M ratio, thereby maximizing efficiency. The remaining parameters were selected to support efficiency maximization while satisfying additional constraints, including adherence to voltage safety margins and physical limits.

[18] and [52] report that, for circular pads, the fundamental flux path height is approximately one-quarter of the pad's outer diameter. This implies that, in order to maintain adequate coupling at larger air gaps, the pad diameter should generally be at least four times greater than the air gap distance. In this work, a pad diameter of 78 cm was selected to satisfy this requirement and to ensure sufficient coupling even at larger air gaps, thereby accommodating potential experimental verifications.

The selection of Litz wire diameter is typically guided by the methodology outlined in [53]. The process begins by estimating the maximum RMS current expected in both the primary and secondary coils. This current can be approximated using the desired maximum output power P_o, the anticipated DC-to-DC system efficiency η_{dc}, and the minimum operational RMS input and output voltages, v_{rms_m} and $v_{o\_rms\_m}$, as constrained by the design specifications. These estimates do not require extreme precision; a safety margin, Mar_s, is generally incorporated to account for potential future system upgrades and to provide operational reliability.

Once these quantities are determined, the required input power can be computed using:

$$P_{in} = \frac{P_o}{\eta_{dc}} \tag{3.22}$$

The corresponding RMS currents in the primary and secondary coils are then obtained

as:

$$I_{1\_rms} = \frac{P_{in}}{v_{rms\_m}} \tag{3.23}$$

$$I_{2\_rms} = \frac{P_o}{v_{o\_rms\_m}} \tag{3.24}$$

The larger of these two currents is selected:

$$I_{max} = \max(I_{1\_rms}, I_{2\_rms}) \tag{3.25}$$

Finally, the expected maximum current for the conductor is determined by applying the safety margin:

$$I_{final} = I_{max} \times Mar_s \tag{3.26}$$

For conventional cooling conditions, the recommended range of average current density—based on continuous operation and allowable temperature rise—is typically between $3\,\text{A/mm}^2$ and $6\,\text{A/mm}^2$ [54]. A conservative value of $4\,\text{A/mm}^2$ is selected in this study. Using this current density, the required wire cross-sectional area can be calculated as:

$$\text{Cross-sectional area of wire } (\text{mm}^2) = \frac{I_{final}}{4\,\text{A/mm}^2} \tag{3.27}$$

From this calculated area, the appropriate American Wire Gauge (AWG) can then be chosen for the Litz conductor.

Applying this methodology with an assumed system efficiency of $\eta_{dc} = 90\%$, a minimum RMS input voltage v_{rms_m} equal to 50% of the maximum voltage, and a safety margin $Mar_s = 1.5$, results in a minimum required conductor diameter of 1.83 mm (13 AWG).

Consequently, the Litz wire already available in the laboratory, with a diameter of 2.7 mm, was selected for use in the experiments.

Previous studies have consistently shown that increasing the spacing between adjacent coil turns G_w leads to a reduction in mutual inductance [18, 41]. This reduction occurs because wider gaps allow more magnetic flux to disperse between turns, which in turn weakens the net magnetomotive force (MMF) linking the coils.

Therefore, the turn spacing G_w should be minimized as much as possible. To achieve this while also ensuring geometric accuracy during coil winding, a coil track was designed and 3D printed as a guide. Maintaining precise spacing reduces flux dispersion between turns, thereby contributing to higher mutual inductance. However, the minimum achievable turn spacing G_w was limited to 0.8 mm due to the 3D printer's nozzle size, which restricts the minimum printable layer thickness.

Once chosen through the process described in this section, all selected parameters are treated as fixed parameters during the optimization process. A summary of these fixed parameters is provided in Table 3.1

Table 3.1: Fixed parameters selected for WPT coil design

Parameter	**Value**
D_{out}	78 cm
d	15 cm
G_w	0.8 mm
w	2.7 mm
P_o	2 kW
Switching frequency (ω)	90 kHz

With all other parameters fixed, the inner diameter becomes a function of N. With the outer diameter held constant, the number of turns is increased inward, starting from an

initial condition where the outer diameter equals the inner diameter at $N = 0$ ($D_{in} = D_{out}$). The relationship between the inner diameter and the number of turns is described by (3.28).

$$D_{in}(N) = D_{out} - [2(G_w + w)N] \tag{3.28}$$

Using these fixed parameters as a foundation, the optimization process seeks to evaluate how the number of turns in identical Archimedean coils influences the ratio R_1/M and thereby the overall efficiency, with the goal of establishing a criterion for determining the optimal turn count. The approach begins with analytical calculations and simulation studies to define the selection rule that yields the maximum efficiency, followed by experimental validation to confirm the results.

3.3 Formulation of coil turn count optimization conditions

For any given design of Archimedean spiral coils, the parasitic AC resistance R_1, R_2 can typically be expressed as (3.29) [55]. Here, γ_{ac} is the AC resistance factor, which is considered constant for a selected conductor at a given frequency, and R_{dc} is the DC resistance of the conductor, which is proportional to its total length, L_{total}. Based on (3.28), the relationship between L_{total} and N can be estimated using (3.30) and further simplified to yield (3.31).

It is evident from (3.31) that the first term ND_{out} increases linearly with N, while the second term, $-(G_w + w)N(N-1)$, varies quadratically with N and is subtracted from the total length. Therefore, for smaller values of N, the total length increases approximately linearly, whereas for larger N, the negative quadratic grows rapidly, reducing the rate of

increase from what would otherwise be a linear trend. In both cases, however, the total length still increases with N. As the conductor length increases with the number of turns N, R_{dc} increases, and consequently R_1, R_2 also increases. Therefore, it can be concluded that R_1 and R_2 will always increase with N, as expressed in (3.32), where R_{pu} denotes the per unit length AC resistance of the selected conductor at the specified switching frequency.

$$R_1 = R_2 = (1 + \gamma_{ac})R_{dc} \tag{3.29}$$

$$L_{total} \approx \pi \sum_{n=1}^{N} D_n = \pi \sum_{n=1}^{N} [D_{out} - 2(G_w + w)(n-1)] \tag{3.30}$$

$$L_{total} \approx \pi [N D_{out} - (G_w + w)N(N-1)] \tag{3.31}$$

$$R_1 = R_2 \approx R_{pu}\pi [N D_{out} - (G_w + w)N(N-1)] \tag{3.32}$$

The mutual inductance M may either increase or eventually saturate with the number of turns N, depending on the selected geometrical design parameters of the coil such as the turn spacing G_w and the ratio $\frac{D_{in}}{D_{out}}$ [31]. When M saturates with N, the series resistance R_1 continues to increase with additional turns, causing the ratio R_1/M to rise. According to (3.21), this increase in R_1/M directly reduces the achievable efficiency at a fixed switching frequency.

However, for a design in which M continues to increase with the number of turns N, examining (3.21) shows that, for a set switching frequency ω, if the ratio R_1/M decreases from turn i to turn $i+j$, where j is the step size between simulations, then the overall system

efficiency η_m will improve. In other words, as long as R_1/M continues to decrease with each additional turn, it remains beneficial to increase the number of turns.

$$\frac{R_1(N_{i+j})}{M(N_{i+j})} < \frac{R_1(N_i)}{M(N_i)} \tag{3.33}$$

Therefore, it can be concluded that increasing the number of turns as long as the condition in (3.33) holds will improve the efficiency of the system.

Under the same assumptions as Section 3.2.2, namely $R_L \gg R_1, R_2$, $R_1 = R_2$, and using (3.19), (2.11) can be simplified as (3.34)

$$P_0 \approx \frac{v^2}{\omega M} \tag{3.34}$$

From (3.34), it follows that for a fixed output power and switching frequency, an increase in mutual inductance M requires a proportional increase in the input voltage. Thus, in a design where M increases with the number of turns N, achieving the same output power demands a higher input voltage. As a result, increasing the number of turns also raises the required input voltage and voltage ratings of all components in the WPT system.

Based on these observations, it can be concluded that, for a design objective of maximizing efficiency, a higher number of turns N is generally preferable. The designer can increase N until one of the following conditions is reached:

Condition 1: The maximum N beyond which the requirement stated in (3.33) is violated.

Condition 2: The maximum value of N beyond which the system's maximum input voltage is exceeded.

This approach can be summarized as shown in the flowchart in Fig. 3.2.

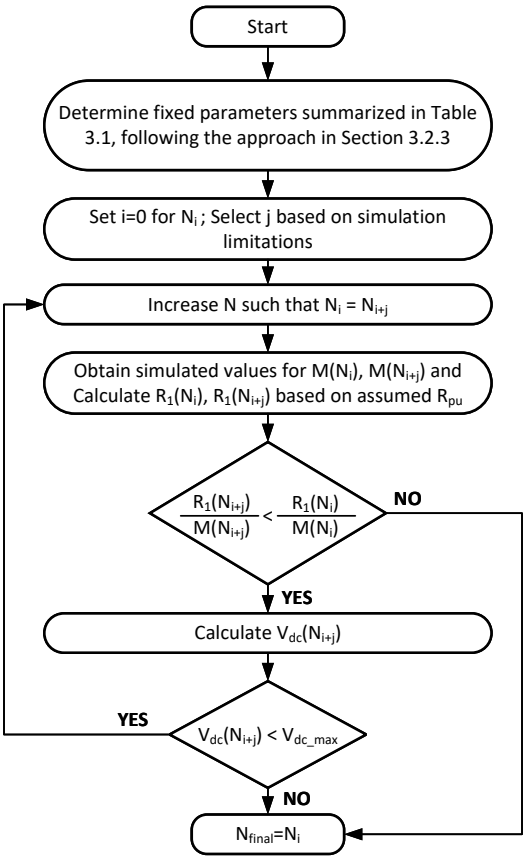

Fig. 3.2: Flowchart summarizing the proposed approach for selecting the optimal N for identical Archimedean spiral coils.

3.4 Optimization of Coil Turns and Efficiency Analysis

Using the geometrical parameters of the coil described in Section 3.2.3, an identical Archimedean spiral coil pair was modeled in ANSYS Maxwell. The software was primarily employed to simulate the self-inductance of each coil (L_1, L_2) and the mutual inductance between the coils (M) at a fixed air gap of $15cm$, while varying the number of turns.

The Magnetostatic simulation mode in ANSYS Maxwell provides sufficiently accurate

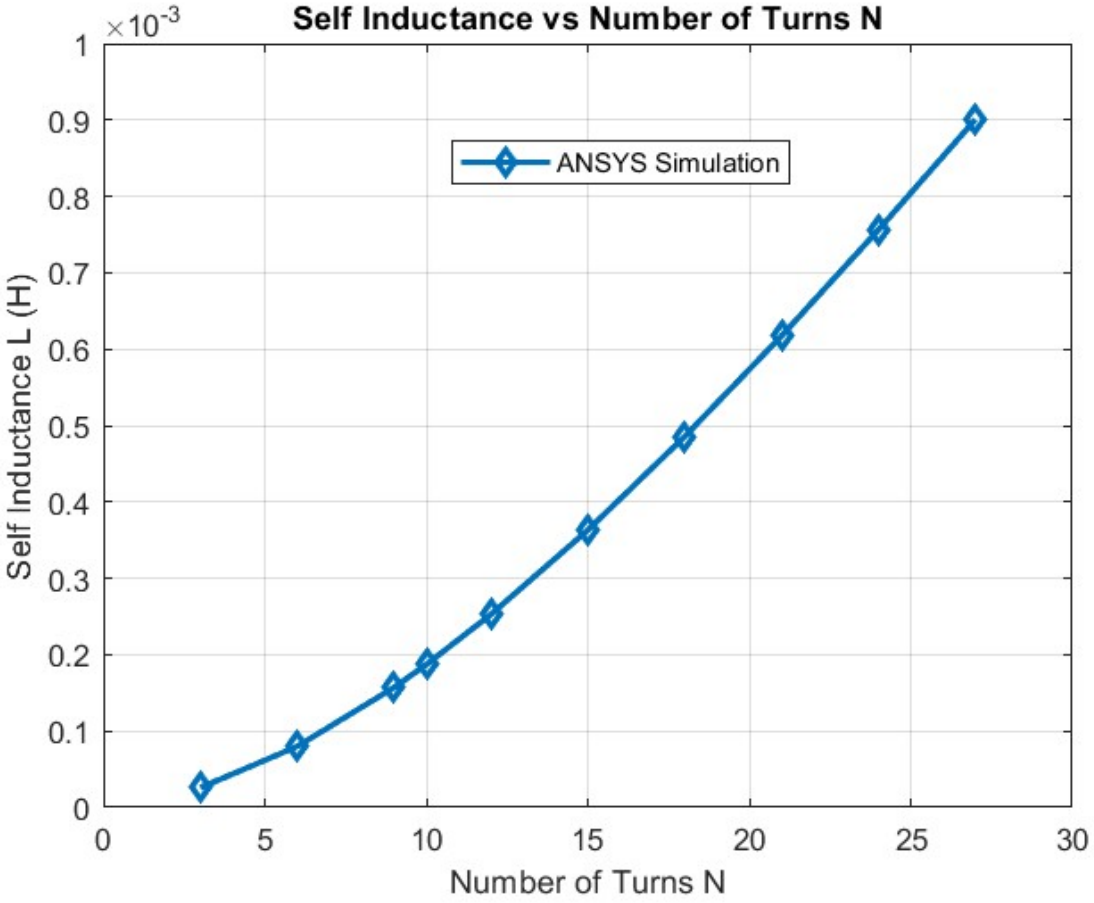

Fig. 3.3: ANSYS simulation results for self inductance variation with N

estimates of self-inductance and mutual inductance, and was hence employed for the simulations. Given the significant computational time required for ANSYS simulations, and considering that the primary goal was to observe the general trend of mutual inductance—whether it increases or reaches saturation with varying turn counts—the simulations were performed only for select discrete values of N, specifically $N = 3, 6, 9, 10, 12, 15, 18, 21, 24$ and 27. This approach allowed for efficient analysis while capturing the essential behavior of the system without exhaustive simulation of every possible turn count.

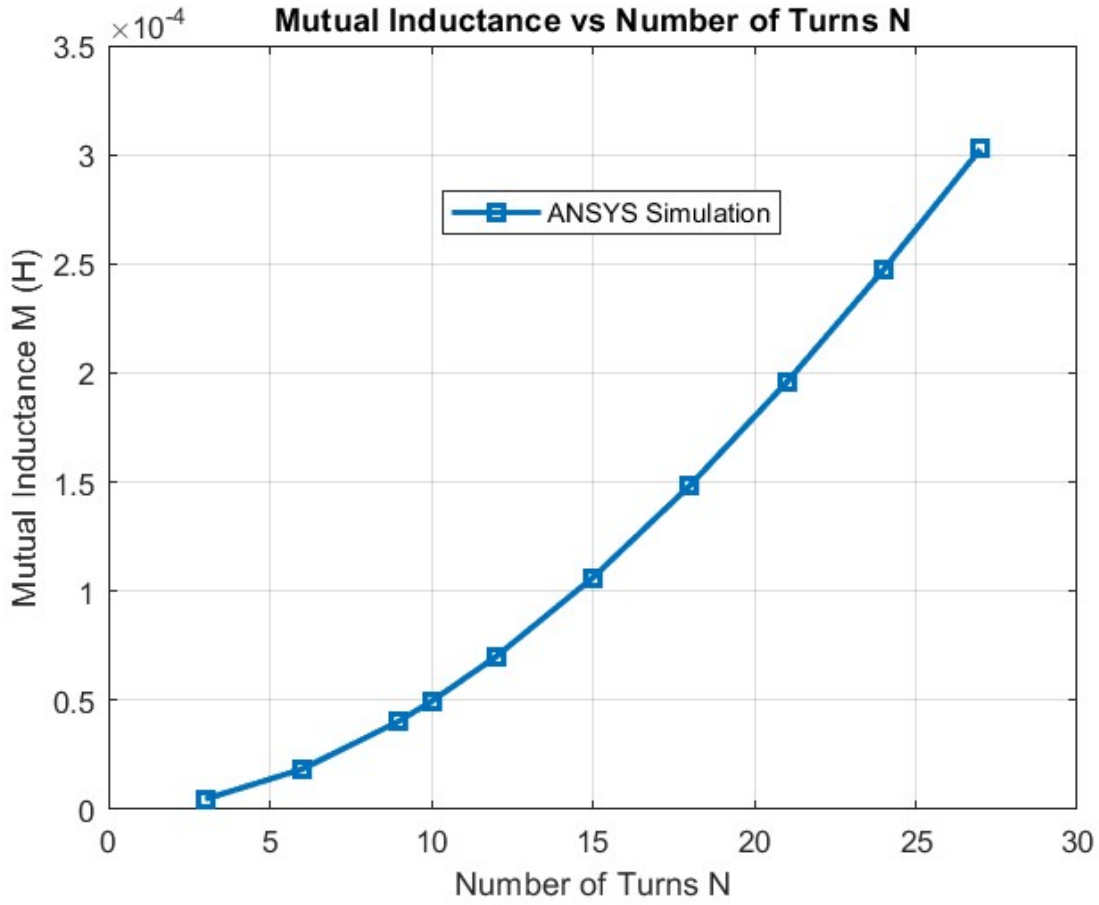

Fig. 3.4: ANSYS simulation results for mutual inductance variation with N

The results showing the variation of self-inductance with respect to the number of turns N based on ANSYS simulation is presented in Fig. 3.3. Since the coils are identical, the self-inductance values for a given number of turns are equal; that is, $L_1 = L_2$ for each corresponding N.

Fig. 3.4 illustrates the variation of mutual inductance as a function of the number of turns, based on results obtained from ANSYS simulations. As observed, both self-inductance and mutual inductance increase with the number of turns for the chosen design parameters.

Furthermore, the rate at which they increase also grows as the number of turns becomes larger.

Next, based on these simulation results and the analytical equations derived in Section 2.2, the efficiency was calculated for each simulated value of M. Since it is difficult to accurately determine the per-unit-length AC resistance R_{pu} in (3.32), an estimated value was used to compute R_1 for each N. This approach is justifiable because the primary objective of the analytical expressions is to identify the trend of efficiency variation—i.e., whether the efficiency increases, decreases, or saturates with N. This reasoning is further supported by Fig. 3.5, where efficiency is calculated using different R_{pu} values. The results clearly show that, although the absolute efficiency values change, the overall trend of efficiency variation with N remains consistent for all selected R_{pu} values.

MATLAB was used to solve the analytical equations and generate the plots in Fig. 3.5. First, the coil resistances R_1 and R_2 were calculated using (3.32) with the estimated value of R_{pu}. Next, the load resistance that maximizes efficiency $R_{L\_\eta m}$ was calculated based on (2.18); this was done to obtain comparable values, ensuring that the maximum efficiency attainable for each corresponding N could be calculated and fairly compared. If the load resistance were selected arbitrarily, the comparison across different numbers of turns would not be meaningful. Finally, the efficiency was determined using (2.19). This procedure was repeated for each number of turns N, using the simulated mutual inductance values M.

As the efficiency increases with the number of turns N, as observed in Fig. 3.5, it is evident that Condition 1 is not violated. To verify this, the variation of the R_1/M ratio with N was examined. Fig. 3.6 illustrates this variation, confirming that Condition 1 is not reached across the entire range of N considered. Consequently, the limiting factor for further optimization is determined by Condition 2, which will be analyzed next.

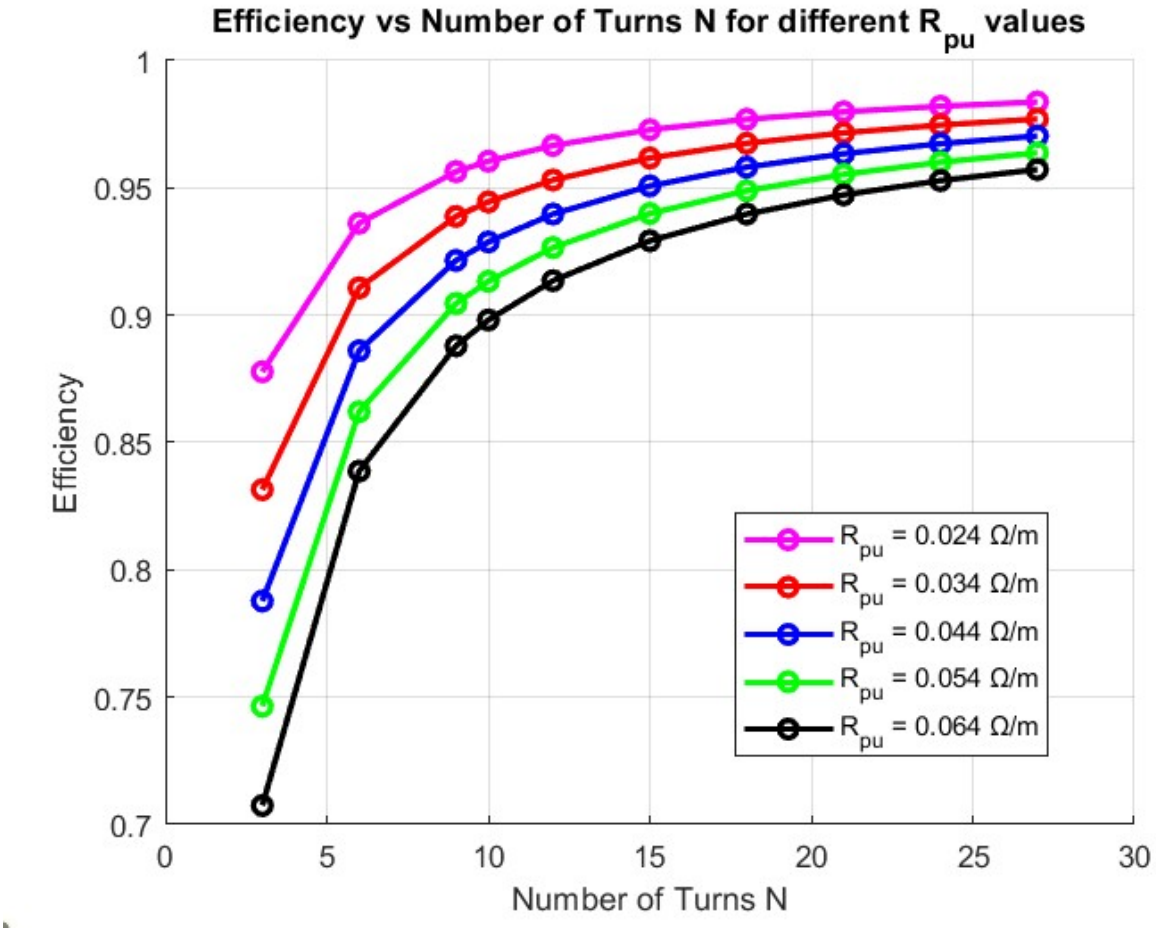

Fig. 3.5: Efficiency variation with number of turns for different per-unit-length resistances using ANSYS simulated mutual inductance and analytical calculations.

To identify the limiting factor based on Condition 2 discussed in Section 3.3, the variation of the DC input voltage with the number of turns for different R_{pu} values was plotted in Fig. 3.7 for 2 kW output power, using the simulated mutual inductance values and the analytical expression in (4.9). It can be observed that the influence of R_{pu} on the required input voltage is minimal. This is because $R_L \gg R_1, R_2$ for the selected R_{pu} values.

Therefore, based on the maximum input DC voltage limit of 600 V detailed in Section 3.2.3 and as specified in Condition 2 of Section 3.3, the maximum number of turns for

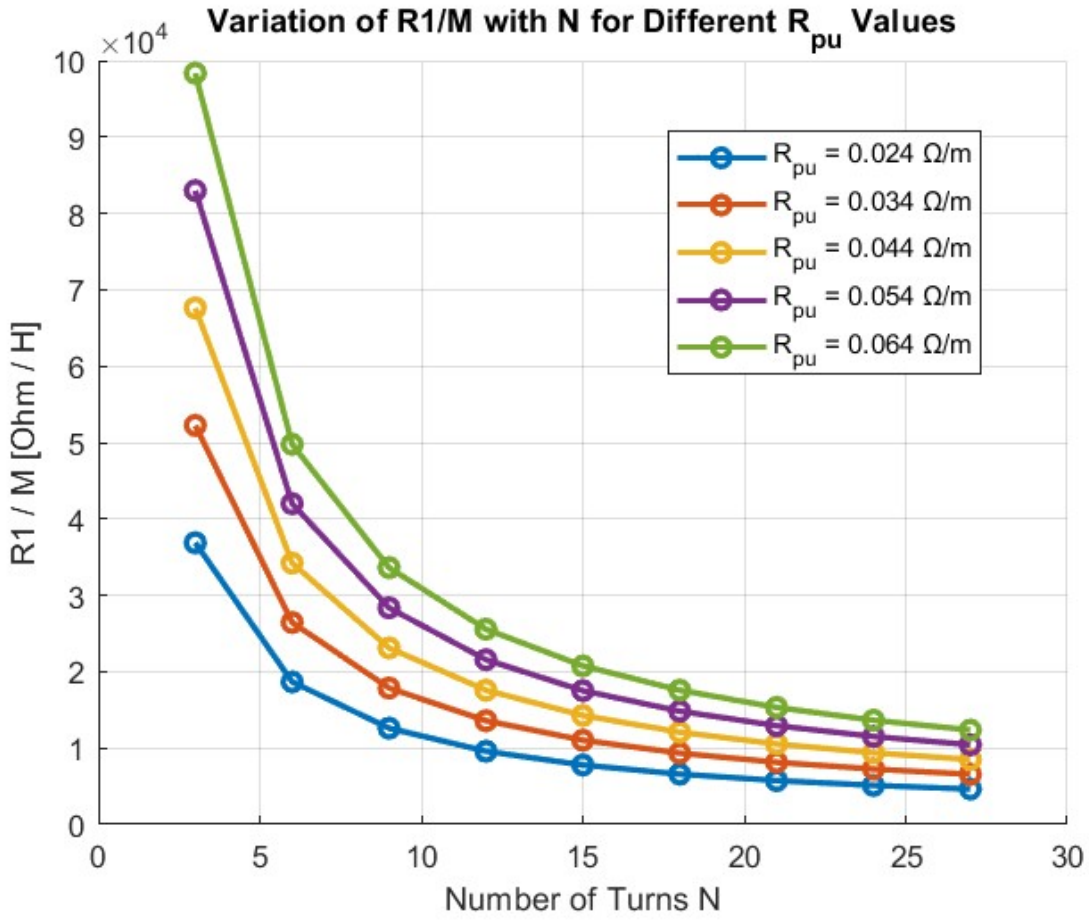

Fig. 3.6: Variation of the R_1/M ratio with the number of turns N for different per-unit resistances

the given design was selected as 24 to enable practical implementation.

Next, the WPT model was implemented in PLECS, as shown in Fig. 3.8. For ease of modeling, the transformer was represented using the T-model simplification. Accordingly, the inductance values in the model were set as (3.35) and (3.36). A pulse generator operating at the switching frequency with a 50% duty ratio was used to invert the DC voltage. The primary and secondary compensation capacitors were chosen such that the self-inductance values were fully compensated at the given switching frequency, as described by equations

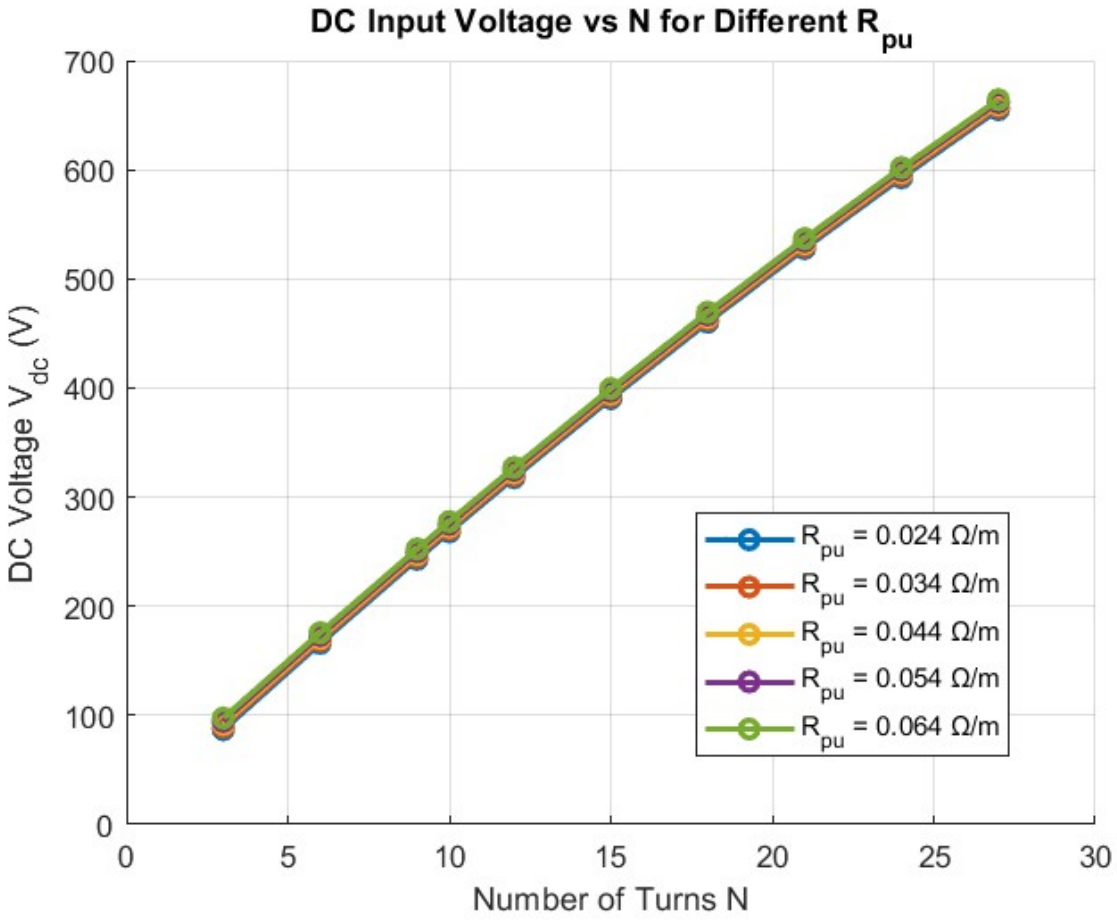

Fig. 3.7: DC input voltage variation with number of turns for different per-unit-length resistances using ANSYS simulated mutual inductance and analytical calculations

(3.37) and (3.38).

The simulation results obtained from the PLECS model were used to verify the analytically derived efficiency values and to determine the voltage ratings of the primary and secondary compensation capacitors.

Since the procedure for comparing PLECS-simulated and analytically calculated values is identical for all R_{pu} values, the comparison was performed only for $R_{pu} = 0.044$ Ω/m. Using this R_{pu} value, R_1 and R_2 were calculated for each value of N. The simulated mutual

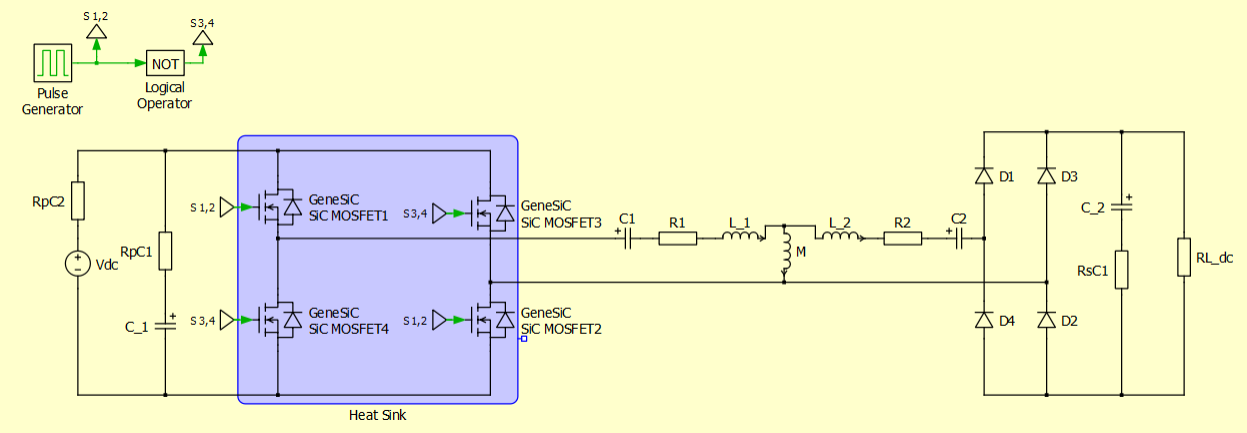

Fig. 3.8: Simulation model in PLECS

inductance values M obtained from ANSYS for each N were then used, along with the calculated $R_{L_{\eta m}}$ from (2.18) and V_{dc} from (4.9), to perform PLECS simulations and determine the efficiency. The results are presented in Fig. 3.9. The case for $N = 3$ is not shown, as the current rating of the SiC MOSFET was exceeded and the configuration was therefore omitted.

Fig. 3.10 compares efficiencies obtained for ANSYS + PLECS simulation results and ANSYS + Analytical calculations. The close agreement between the two sets of results confirms the validity of the analytical equations.

$$L\_1 = L_1 - M \tag{3.35}$$

$$L\_2 = L_2 - M \tag{3.36}$$

$$C_1 = \frac{1}{\omega^2 L_1} \tag{3.37}$$

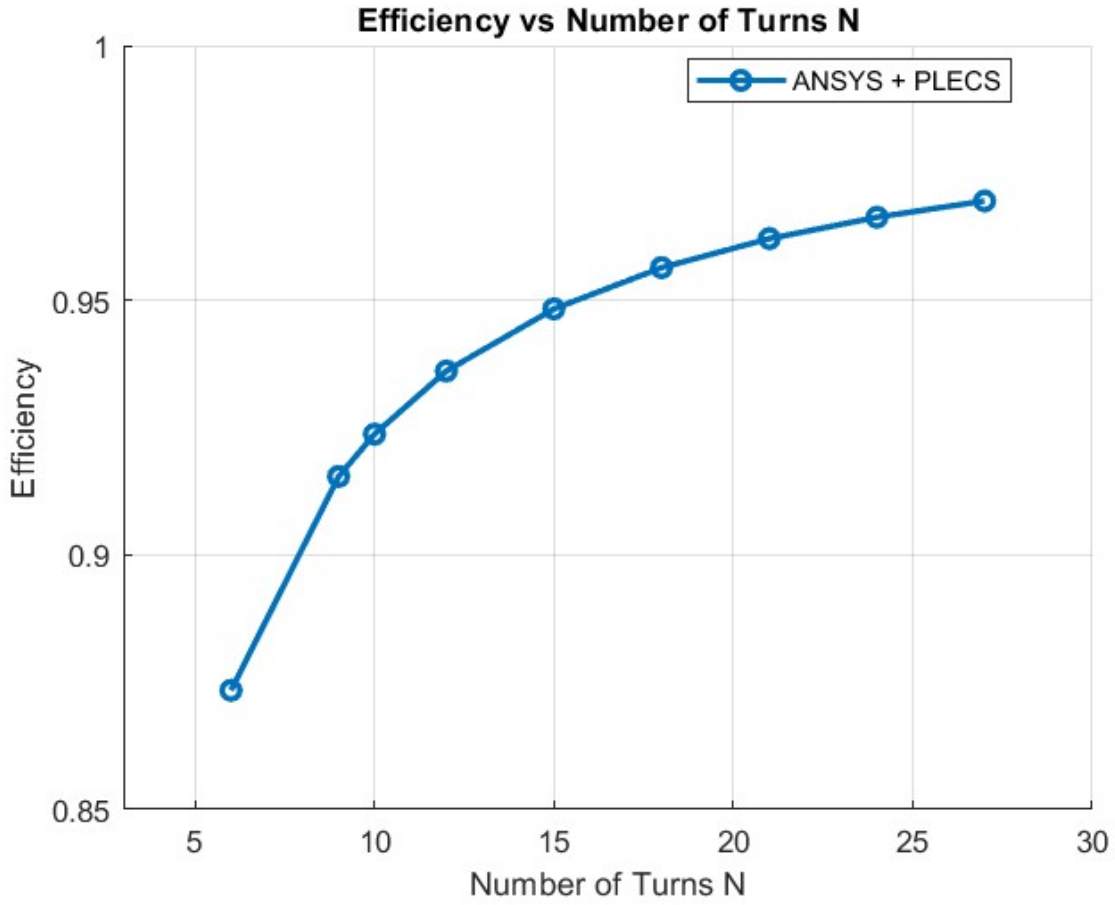

Fig. 3.9: Efficiency variation with number of turns using ANSYS simulated mutual inductance and PLECS simulation

$$C_2 = \frac{1}{\omega^2 L_2} \tag{3.38}$$

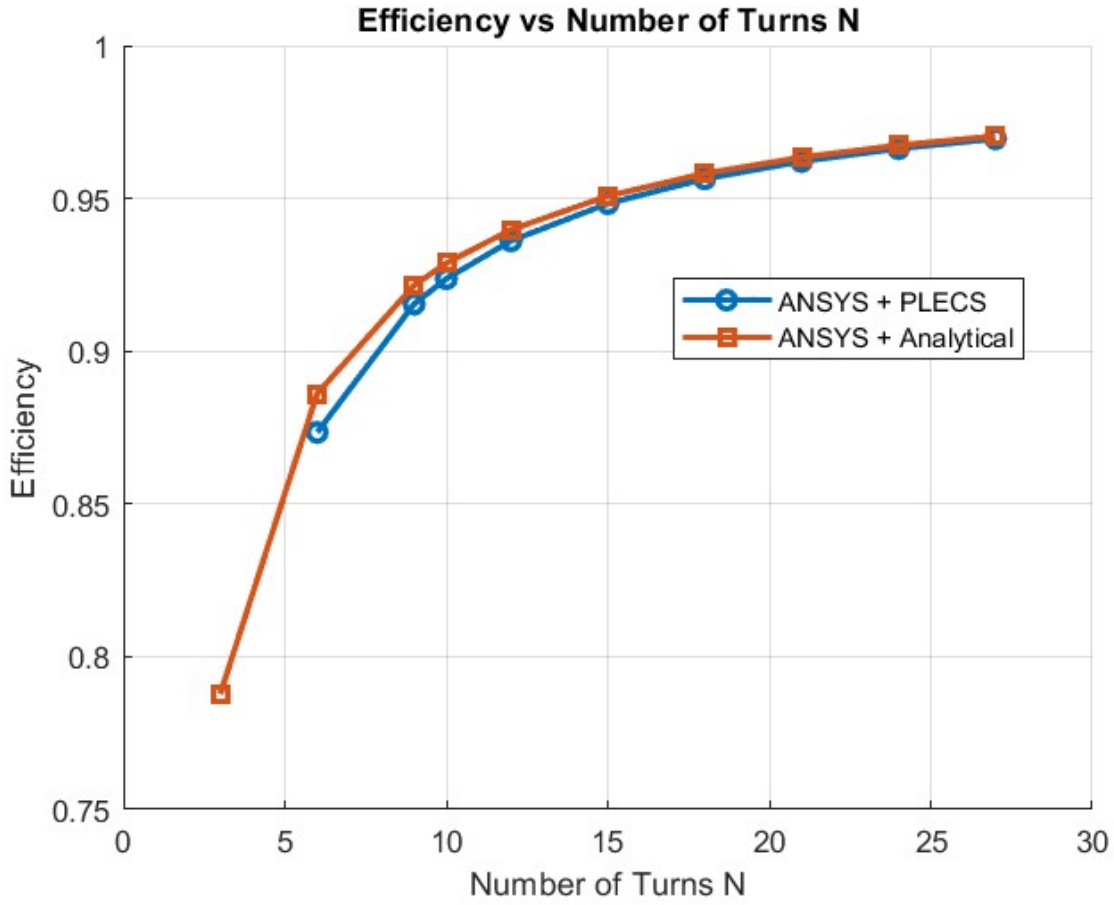

Fig. 3.10: Efficiency variation with number of turns for ANSYS + PLECS simulation results and ANSYS + Analytical calculations

3.5 Proposed Bifurcation Avoidance Strategy and Comparative Analysis

3.5.1 Proposed Bifurcation avoidance strategy

Once the optimum number of turns is determined using the procedure detailed in the preceding sections, the critical coupling coefficient k_{crit} should be adjusted to achieve the desired

operating ratio k/k_{crit}. This ratio can be selected based on the specific design requirements, such as required safety margin to ensure bifurcation-free operation.

First, R_1 and R_2 are calculated based on the selected per-unit-length resistance R_{pu} and the optimum number of turns N using (3.32).

Next, the load resistance that maximizes efficiency, $R_{L\_\eta m}$, is determined using (2.18) along with the simulated mutual inductance M.

The coupling coefficient k is then obtained from the simulated self-inductances and mutual inductance as

$$k = \frac{M}{\sqrt{L_1 L_2}}. \tag{3.39}$$

Based on the design-specified k/k_{crit} ratio, the required k_{crit} is computed.

To achieve the desired k/k_{crit} ratio while minimizing the impact on efficiency, an additional load resistance R_{L_add} is added to $R_{L\_\eta m}$, as highlighted in Section 3.2.1. The required R_{L_add} is determined iteratively by solving

$$Q = \frac{\omega L_2}{R_{L\_\eta m} + R_2 + R_{L\_\text{add}}}, \quad k_{\text{crit}} = \frac{1}{Q}\sqrt{1 - \frac{1}{4Q^2}}. \tag{3.40}$$

This procedure ensures that the selected k/k_{crit} ratio is achieved while maintaining high system efficiency.

Following this procedure, the efficiency was evaluated for different per-unit resistance values and different k/k_{crit} ratios. The obtained results are shown in Fig. 3.11. As can be observed, the efficiency deviates slightly from the optimum value when the k/k_{crit} ratio is lower, i.e., when the operating coupling k is well below the critical coupling k_{crit} which grantees bifurcation free operation.

In the experimental setup, a similar iterative process as in (3.40) should be followed,

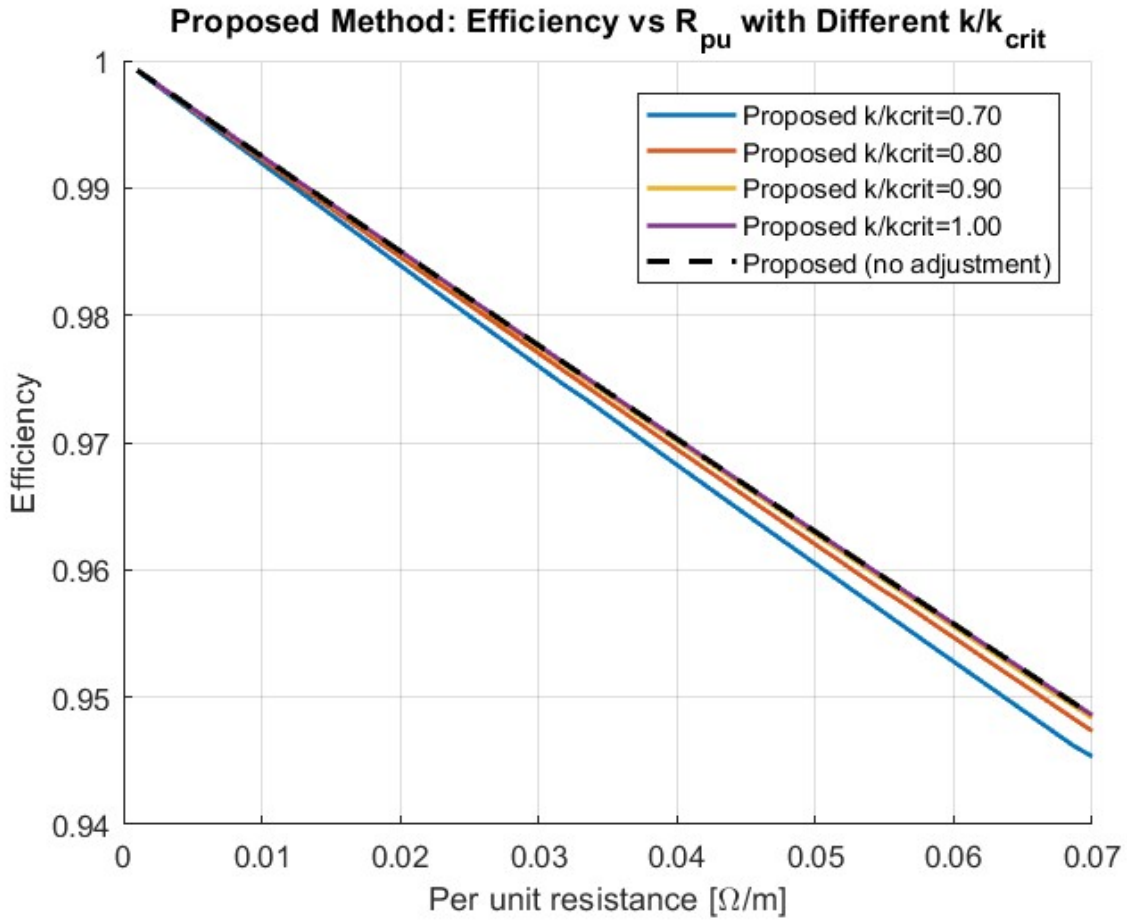

Fig. 3.11: Proposed method: efficiency variation with per-unit resistance for different k/k_{crit} ratios, based on ANSYS simulation results + analytical calculations.

based on the measured parameters, in order to obtain the desired k/k_{crit} ratio.

3.5.2 Efficiency Assessment:Proposed Optimization Approach vs. Existing Bifurcation Avoidance Design guideline

Following the well-referenced design guidelines for bifurcation-free coil design in [35], the efficiency was estimated for a comparable setup in order to verify which method provides

superior performance.

First, the input and output DC voltages were both fixed at 600 V. This adheres to the DC voltage limits defined in Section 3.2.3 and ensures that the primary and secondary coils remain nearly identical, since for identical coils the input and output voltages are expected to be similar. Considering a 2 kW output power, the load resistance R_L was determined according to (3.3). Using this value, the mutual inductance M was calculated as 258 μH based on (3.5), (3.6), and (3.7).

The next step is to determine the quality factor Q_2. Although this relationship is not explicitly discussed in [35], it can be inferred that Q_2 directly influences the minimum airgap required between the coils. For a given load resistance R_L and switching frequency, Q_2 is proportional to the coil inductance L_2. Therefore, a higher Q_2 corresponds to a larger L_2, which allows the same mutual inductance M to be achieved at a greater coil separation.

To ensure a meaningful comparison with the proposed method, the airgap must be kept similar between the two designs. From simulation results in Fig. 3.3, Fig. 3.4, it was observed that for identical coils at $N = 24$ turns the self-inductance is 756 μH and the mutual inductance is 247 μH at an airgap of 15 cm. Based on the preceding analytical calculation, the design requires a mutual inductance of 258 μH. Using linear interpolation between the simulated values, the required self-inductance was estimated as $L_2 \approx 789$ μH, which yields a quality factor of $Q_2 \approx 3.06$. Hence, $Q_2 = 3.06$ was selected for the comparison.

With Q_2 specified, k_{crit} was determined, and the operating coupling k was calculated from the desired k/k_{crit} ratio. Using this value and (3.8), the required L_1 was obtained. The coil resistances R_1 and R_2 were then evaluated by estimating the number of turns for L_1 and L_2 through linear interpolation of the simulated self-inductance values. From these turn counts and the per-unit resistance R_{pu}, the winding resistances were computed. Based on

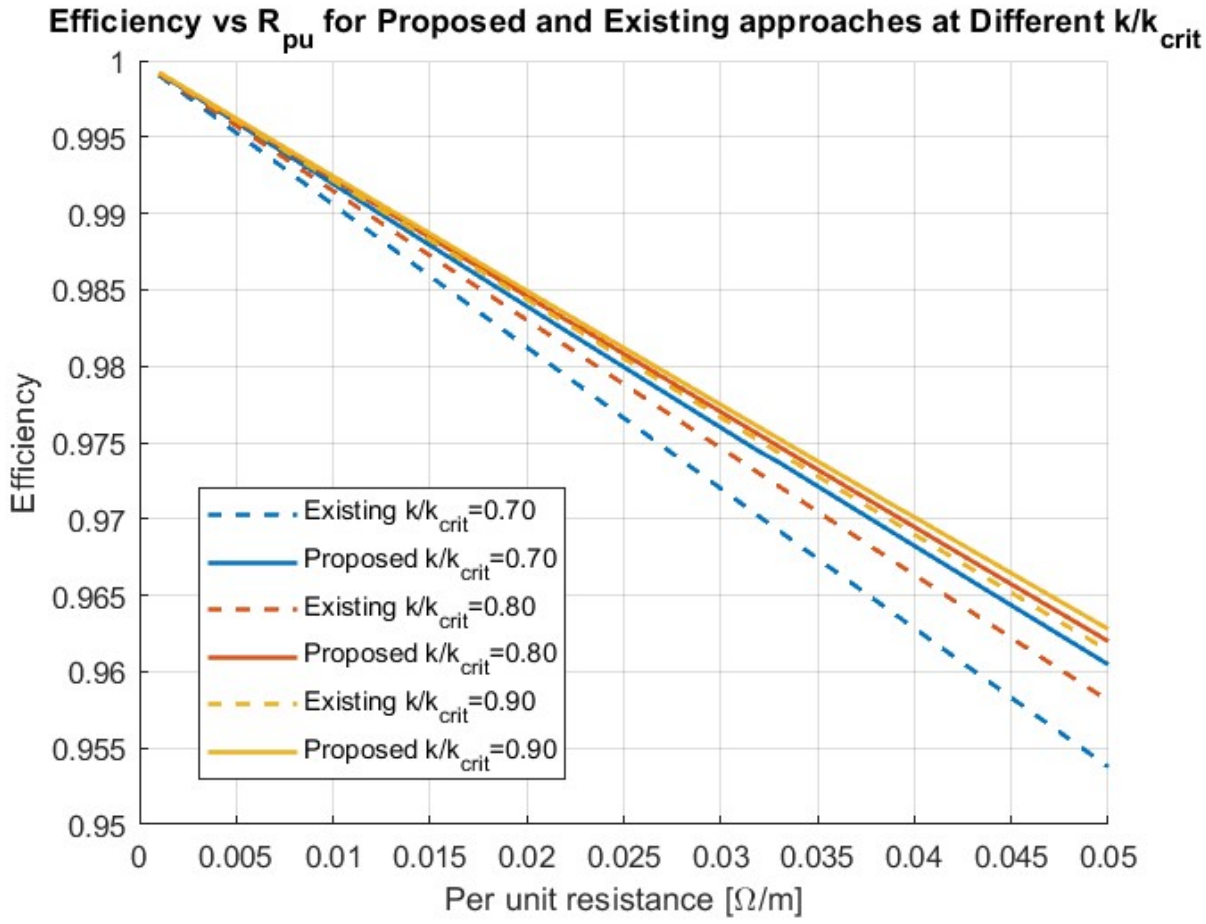

Fig. 3.12: Comparison of efficiency between the proposed optimization method and existing bifurcation avoidance guidelines across varying k/k_{crit} ratios.

these parameters, the final efficiency of the design was estimated.

Fig. 3.12 shows the comparison of efficiency between the proposed optimization method and the existing bifurcation avoidance guideline as per [35] across varying k/k_{crit} ratios, based on this approach. It can be seen that the proposed method provides better efficiency.

3.5.3 Impact of Coil Inductance Deviations on Bifurcation and Efficiency

In practice, it is generally difficult to achieve the exact simulated self-inductance values due to parasitic effects, manufacturing non-idealities, and the influence of surrounding metallic structures, particularly for unshielded coils or coils constructed without ferrite materials. Therefore, in addition to reducing efficiency, such deviations can cause the system to operate in the bifurcation region, significantly impacting power transfer capability, overall efficiency, and controllability.

In the proposed method, any variation in the self-inductance values can be accommodated by adjusting the load resistance R_L according to (3.40), thereby preventing operation in the bifurcation region. In contrast, the design approach presented in [35] does not provide a mechanism to mitigate bifurcation once the system is physically implemented. Consequently, if the operational coupling is designed close to the critical coupling, i.e., k/k_{crit} near 1, and L_1 decreases from its simulated value during experimental implementation while L_2 remains unchanged, the effective coupling k increases while k_{crit} remains constant. This can result in k/k_{crit} exceeding 1, causing the system to enter the bifurcation region. The value of k_{crit} remains constant because, in this design methodology, the input and output voltages are fixed, and for a given output power the load resistance R_L is therefore also fixed. Hence, according to (3.4), Q_2 remains constant, leading to a constant k_{crit}. On the other hand, k increases because, in this approach, the mutual inductance M is maintained at a fixed value determined by the required input and output voltages and power. This value of M is achieved experimentally by adjusting the air gap. Therefore, according to (3.8), when L_2 and M are constant, a decrease in L_1 results in an increase in k.

For example, as shown in Fig. 3.13, a 9.8% reduction in L_1 relative to the simulated

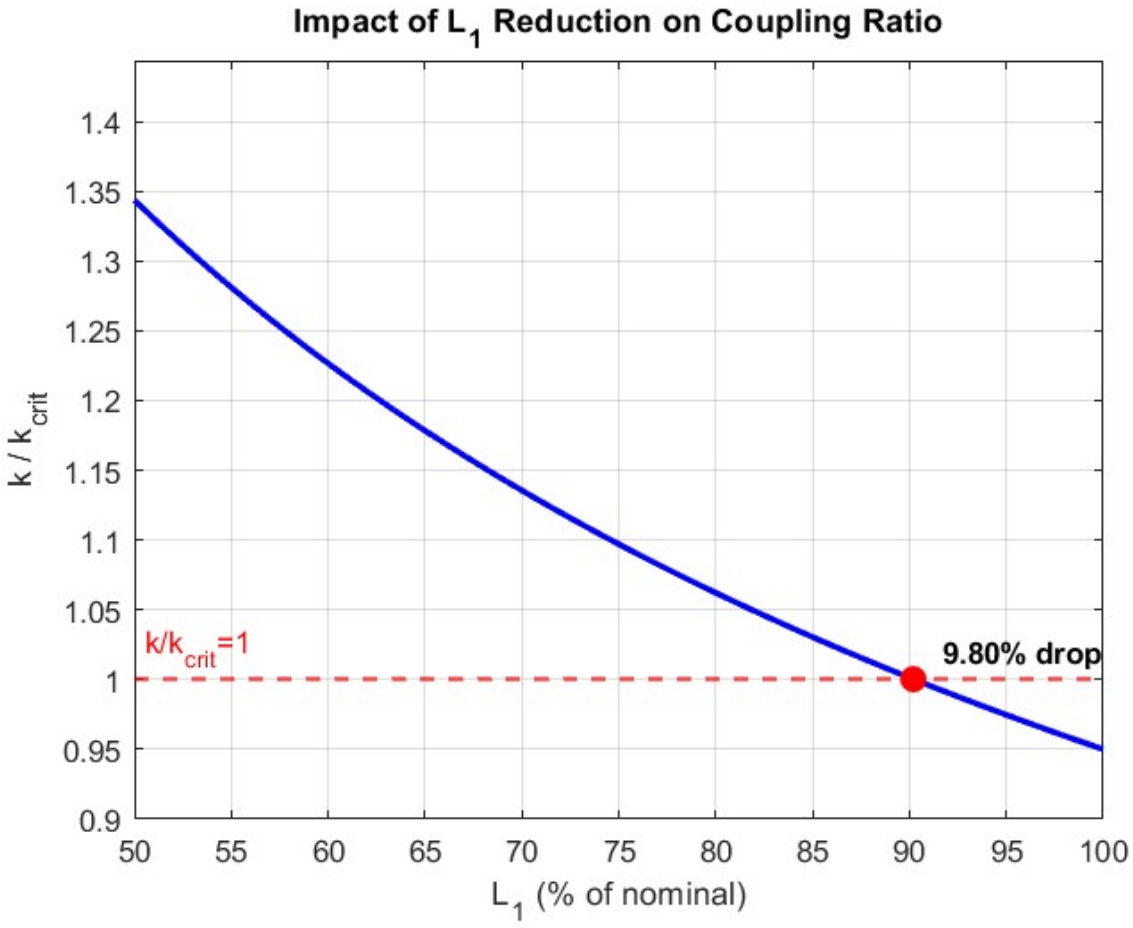

Fig. 3.13: Impact of L_1 deviation from simulated value on the coupling ratio k/k_{crit}.

value, with L_2 held constant and an initial k/k_{crit} of 0.95, can lead to $k/k_{\text{crit}} = 1$. Therefore, to ensure bifurcation-free operation while accounting for self-inductance tolerances, the approach in [35] requires that the design k/k_{crit} include a sufficient margin below 1. However, as observed in Fig. 3.12, efficiency is maximized when k/k_{crit} is close to 1. This implies that, under this method, a trade-off must be made by intentionally operating at a lower coupling ratio to maintain bifurcation-free operation, resulting in reduced efficiency by design.

In contrast, the proposed method allows operation near the optimal k/k_{crit} by simply

Table 3.2: Comparison between the proposed approach and existing bifurcation-avoidance design guidelines.

Aspect	**Proposed Approach**	**Existing Bifurcation-Avoidance Guidelines [35]**
Bifurcation Avoidance	Achieved via load resistance R_L adjustment, either during design or post-implementation, ensuring bifurcation-free operation.	Achieved by adjusting primary self-inductance L_1 during design; post-fabrication tuning is constrained by the physical coil structure, making adjustments impractical.
Airgap	Fixed airgap design is possible.	Considered a degree of freedom; depends on other set parameters.
Efficiency	Higher efficiency in a comparable design setting.	Lower efficiency in a comparable design setting.
Robustness to Parameter Variations	Can tolerate variations in self-inductances without entering the bifurcation region, by adjusting R_L if necessary.	Highly sensitive to variations in L_1 or L_2; such deviations can induce bifurcation. A conservative design margin for k/k_{crit} is required, which reduces achievable efficiency.

adjusting R_L, providing greater flexibility and improved overall performance. Table 3.2 presents a comparative summary of the proposed approach and the existing bifurcation-avoidance design guidelines, highlighting key aspects.

3.6 Hardware implementation and experimental results

Based on the analytical and simulated results obtained in the previous sections, it is evident that high efficiency can be achieved for identical Archimedean spiral coils with the selected geometrical parameters when using 24 turns. Furthermore, the analysis indicates that a maximum input voltage of 600 V will be applied. Therefore, special attention must be given to component voltage ratings and insulation requirements. In light of these considerations,

the experimental setup was carefully designed and fabricated to ensure safe operation while maintaining the desired performance.

3.6.1 Coil design and fabrication

In order to ensure consistency of the fabricated coil with the fixed parameters specified in Table 3.1, and to maintain a sufficient gap between each turn—thereby avoiding unintended turn-to-turn short circuits (a potential risk given the high operational voltage)—a decision was made to 3D print a track to guide the litz wire in place. The 3D model was designed in SolidWorks, with each coil track divided into four segments, as shown in Fig. 3.14, to accommodate the limitations of the 3D printer. Once printed, the segments were assembled to form the complete coil track. Once the tracks were fabricated, the coils were inserted into the tracks and securely fastened to prevent deformation after assembly. This ensured that the coil remained in place and fully adhered to the parameters listed in Table 3.1, as illustrated in Fig. 3.15.

Litz wire is made up of numerous fine conductors as seen in Fig. 3.16, each coated with its own layer of insulation and bundled together to form a single composite wire. The diameter of each strand is chosen to be smaller than the skin depth [56], allowing the conductor's cross-section to be utilized effectively at high frequencies. The strands are braided or woven in such a way that their positions periodically shift between the wire's core and its outer surface. This weaving pattern equalizes the influence of the proximity effect and skin effect on all strands, enabling them to share the current uniformly.

Once coil fabrication has been completed, the next critical step is to carefully remove the insulation from each individual strand of the litz wire. It is essential to perform this task with great caution, as any damage to the strands or incomplete removal of the insulation

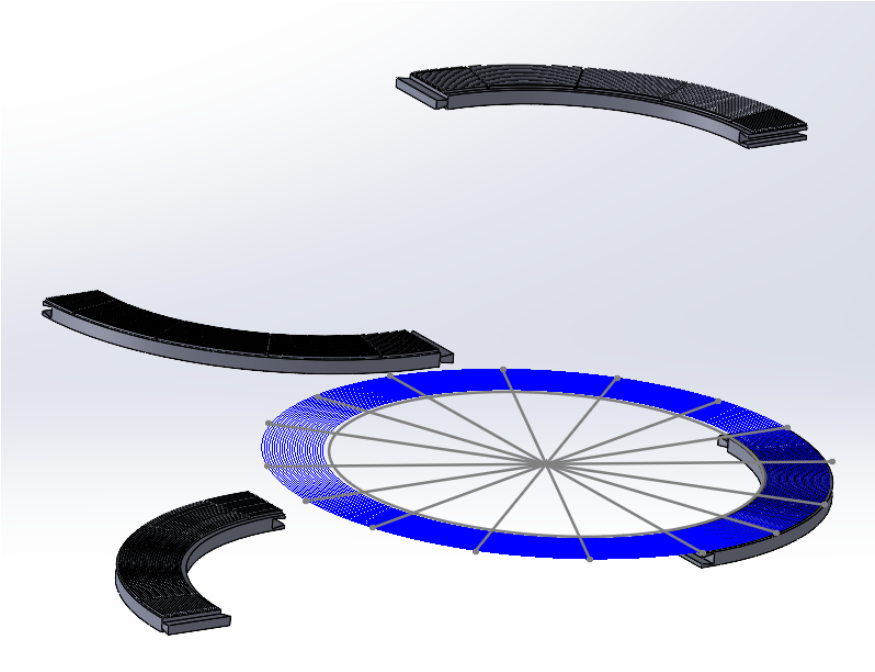

Fig. 3.14: SolidWorks 3D model of the coil track, segmented into four parts for fabrication due to 3D printer size limitations.

can lead to an increase in the AC resistance of the coil. Such an increase in resistance would, in turn, result in a reduction in the overall efficiency of the WPT system, potentially undermining the performance gains achieved through careful coil design and fabrication.

There are three primary approaches for removing the insulation from conductors: mechanical, chemical, and thermal methods [57]. Mechanical techniques, such as using brushes or cutters, carry a high risk of damaging the delicate strands and were therefore not considered. Chemical methods involve the use of acids or bases to strip the enamel coating; however, limited access to appropriate chemicals prevented the adoption of this approach. Thermal methods, which include the use of gas burners or laser processing, can also potentially harm individual strands. For these reasons, a specialized thermal technique known as tinning was selected for this work. In this process, a solder pot was used to contain molten

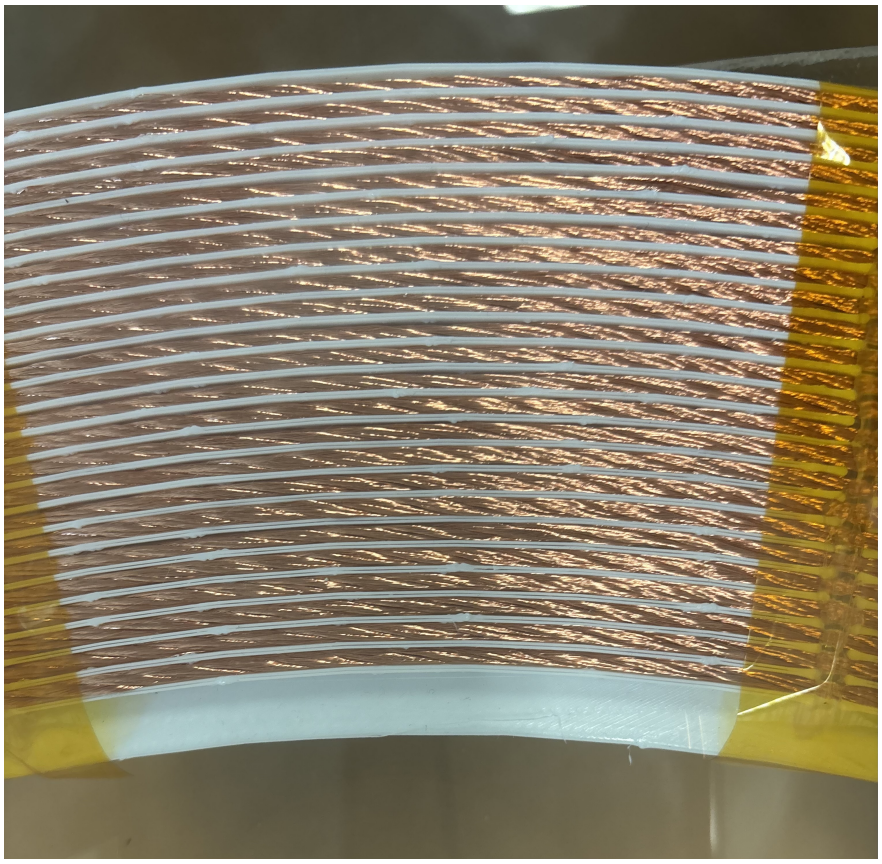

Fig. 3.15: Fabricated 3D-printed coil track with the litz-wire coil secured in place to maintain geometry and turn spacing.

solder, and the insulated end of the litz wire was dipped into the pot until the enamel was burned off. This not only removes the insulation from each strand but also bonds them together at the tip to form a solid conductor as shown in Fig. 3.17. This method was found to be the most effective by the author, as it ensures minimal strand damage while completely removing the insulation from all strands.

Fig. 3.16: Litz wire made of numerous individually insulated thin conductors

3.6.2 Compensation capacitor bank design and fabrication

As mentioned in Chapter 2, series compensation was selected for the experimental setup due to its advantages. Several key parameters must be carefully considered when designing the capacitor bank. The capacitance value is critical, as it primarily determines the resonant frequency, making it essential to use capacitors with stable capacitance. The ESR is another important factor, since higher ESR increases conduction losses in the primary and secondary resonant tanks, reducing overall efficiency. Finally, the voltage rating of the capacitor bank must account for the high voltage stress experienced at or near the resonant frequency. Capacitors should therefore be selected with a sufficient safety margin to ensure reliable and safe operation. In addition to these factors it should be noted that the maximum rms AC withstand voltage of capacitors drops significantly with higher frequency, this should also be taken into consideration when designing the capacitor banks.

The first step in designing capacitor banks is to select the capacitance values for the pri-

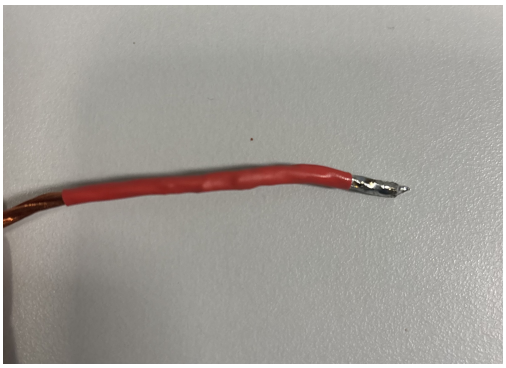

Fig. 3.17: Tinned end of the litz wire after the enamel insulation has been removed, with all strands bonded together to form a solid conductor

mary and secondary compensation banks. The self-inductances of the primary and secondary coils were measured as described in Section 3.6.3. Although, in the initial design phase, both capacitances are chosen to resonate at the switching frequency, typically only the secondary is tuned to the switching frequency. The primary is selected to resonate slightly below the switching frequency, providing an inductive reactance that facilitates ZVS, as discussed in Chapter 4. This is done to minimize the switching losses, thus improving the efficiency. For experimental verification, multiple primary compensation banks and one secondary capacitor bank were designed and fabricated. Once the capacitance values were determined, the maximum voltage stress across the capacitor banks was evaluated using PLECS simulations. However, caution is required when interpreting these results, as PLECS reports the stress across the entire capacitor bank and does not account for individual capacitor variation. In practice, the smallest capacitor in a series string can experience a disproportionately higher voltage, meaning that PLECS may systematically underestimate the true worst-case voltage stress, particularly under large component tolerances.

The three primary capacitor banks were designed to resonate at 88 kHz, 86.5 kHz, and 80.5 kHz, respectively, while the secondary capacitor bank was tuned to the switching

frequency of 90 kHz. The voltage across the primary and secondary capacitor banks was evaluated under the worst-case scenario, corresponding to a coupling coefficient of 0.2 (for increased air gap testing) and the largest R_L that produces the maximum output voltage at the rated output power, calculated as $800^2/2000 = 320\ \Omega$. The resulting waveforms are shown in Fig. 3.18, Fig. 3.19 and Fig. 3.20.

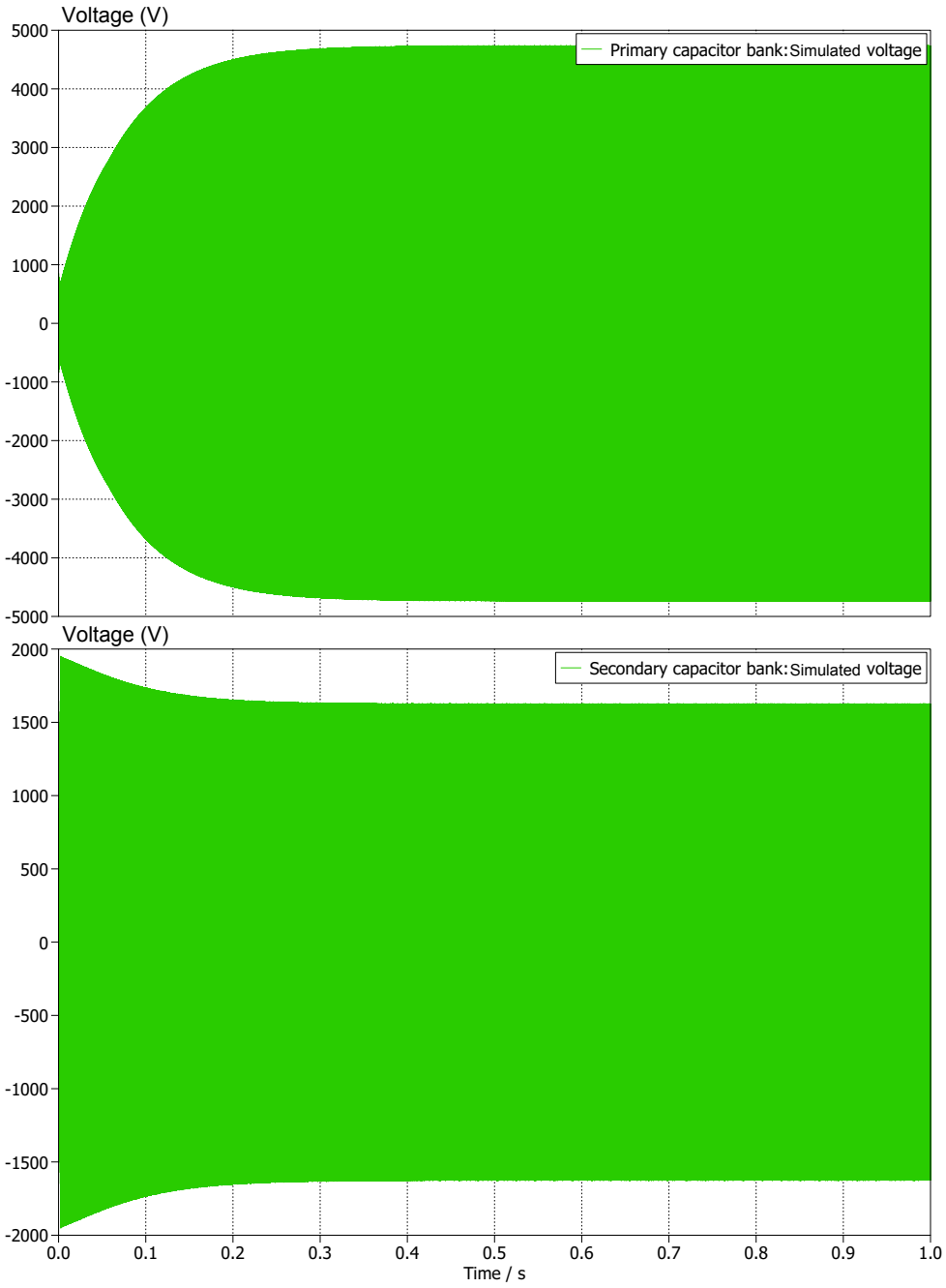

Fig. 3.18: Simulated capacitor voltages with primary tuned to $88kHz$ and secondary to $90kHz$ under worst-case operating conditions.

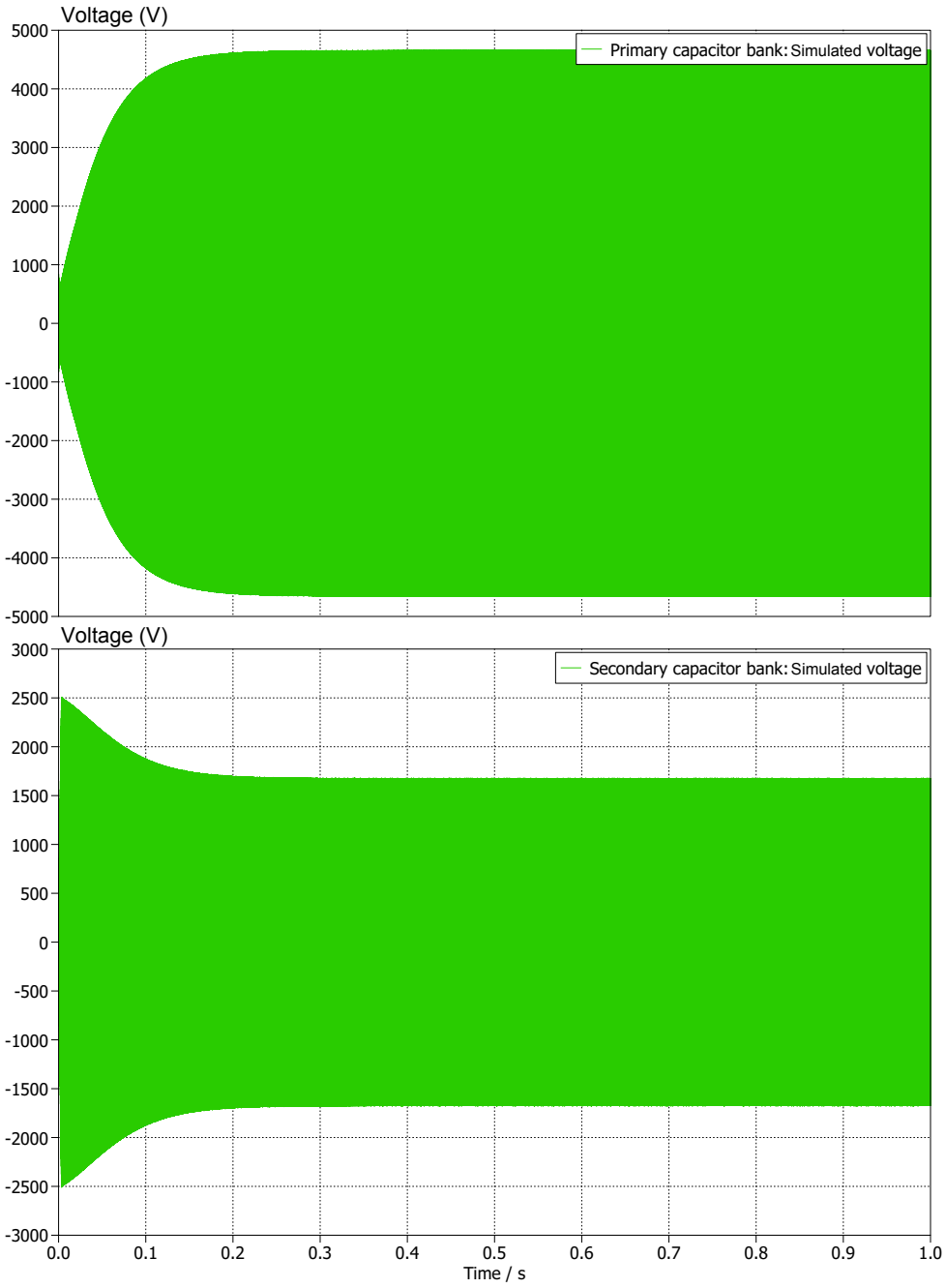

Fig. 3.19: Simulated capacitor voltages with primary tuned to $86.5kHz$ and secondary to $90kHz$ under worst-case operating conditions.

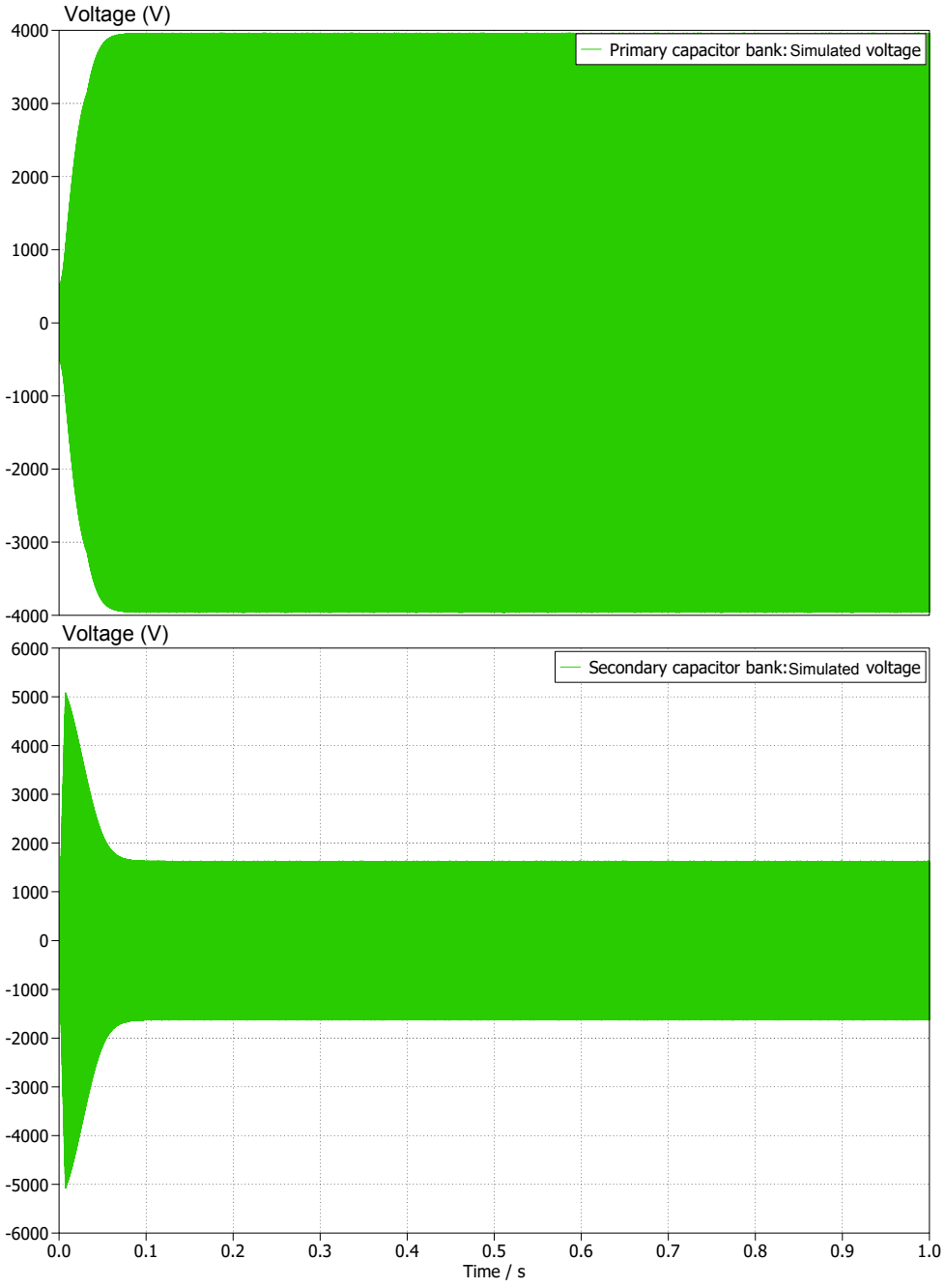

Fig. 3.20: Simulated capacitor voltages with primary tuned to $80.5kHz$ and secondary to $90kHz$ under worst-case operating conditions.

From the simulation results, the first two primary capacitor banks (88 kHz and 86.5 kHz) and the secondary capacitor bank experience peak voltages approaching 5 kV. With a 50% safety margin, these banks should be rated for at least 7.5 kV. The final primary capacitor bank (80.5 kHz) experiences a peak voltage of approximately 4 kV, requiring a rating of at least 6 kV with the same safety margin. Accordingly, all capacitor banks were designed to safely operate above these calculated voltage levels, ensuring sufficient margin during operation. A single capacitor bank is shown in Fig. 3.21.

3.6.3 Component characterization and measurement procedures

After fabricating the coils and compensation capacitors, they were characterized using an R&S HM8118 LCR meter. Mutual inductance was measured following the technique illustrated in Fig. 3.22. The coils were first connected in series with their magnetic flux aligned in the same direction to measure the series aiding inductance, L_{aiding}. They were then connected in series with opposing flux directions to measure the series opposing inductance, L_{opposing}. The mutual inductance, M, was subsequently calculated using Fig. 3.22.

$$M = \frac{L_{aiding} - L_{opposing}}{4} \tag{3.41}$$

Table 3.3 summarizes the simulated and measured values for the self- and mutual inductances of the coils. The measured values deviate from the simulated results due to limitations in simulation accuracy caused by time constraints: the finite region defined around the coil in ANSYS was restricted in size and the maximum element size in the mesh was not sufficiently small to achieve very high accuracy. This deviation is acceptable, since the primary objective of the simulation, as discussed earlier, was to study the directional variation of

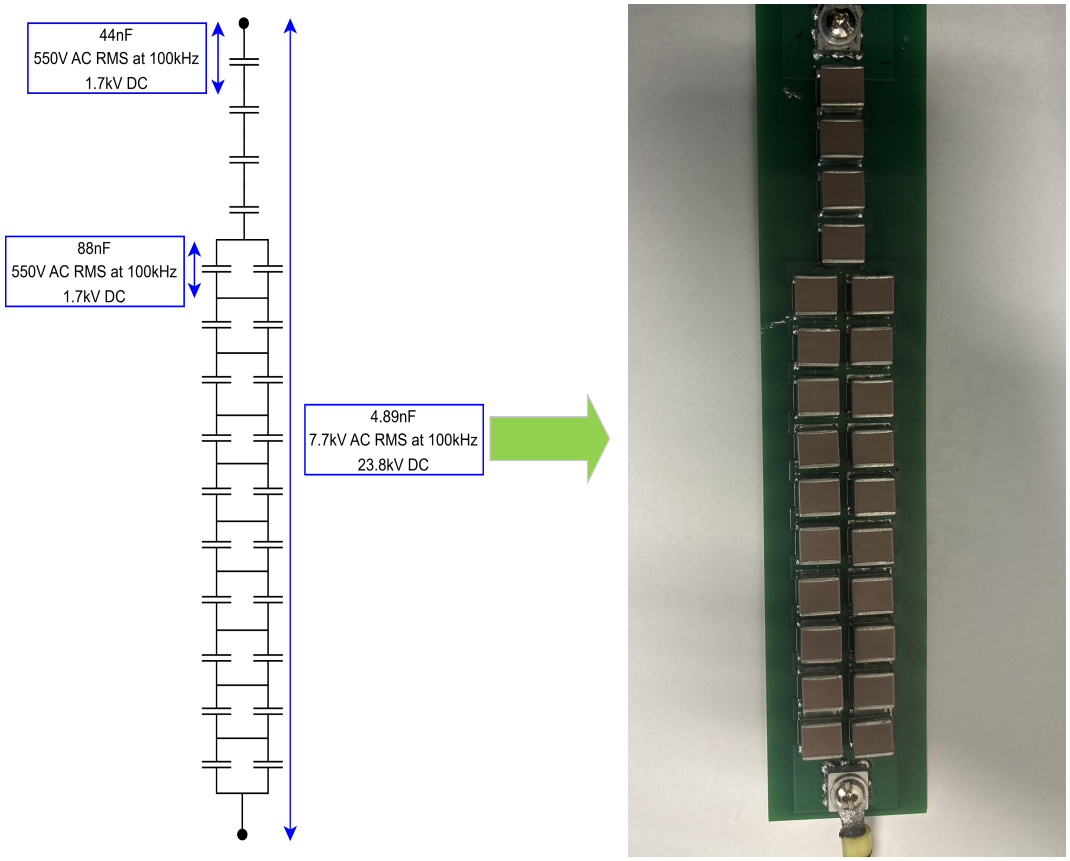

Fig. 3.21: Primary capacitor bank fabricated for $88kHz$ resonance, rated for over $7.7kV$ RMS voltage at $100kHz$.

mutual inductance with the number of turns rather than to obtain exact values of M.

The two measured self-inductance values also differ, even though the coils are geometrically identical. This is mainly because no shielding or ferrite was incorporated, making the coils more susceptible to environmental influences such as nearby rebars in the building's concrete structure and the metallic parts of the XYZ positioning table. In practice, ferrite bars are often used to minimize such variations; however, they were not included in this study in order to focus on the intrinsic behavior of unshielded air-core coils, which better isolates the impact of geometry on the coupling characteristics.

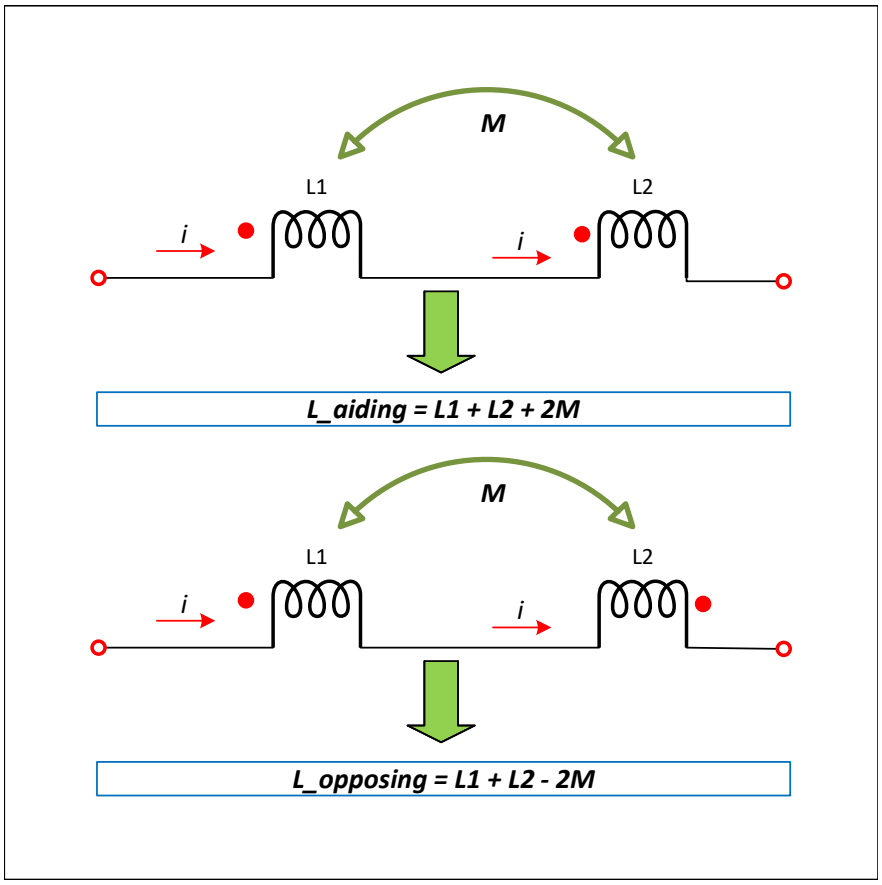

Fig. 3.22: Measurement setup for determining mutual inductance using series aiding and opposing coil connections.

Based on the measured self-inductance values, the primary and secondary compensation capacitor banks were designed with the objective of achieving a resonant frequency of 90 kHz on the secondary side, and 88 kHz, 86.5 kHz, and 80.5 kHz for the three primary capacitor banks. Since each capacitor has a capacitance of 44 nF and an AC voltage rating of 550 V_{rms} at 100 kHz, the capacitor bank values were determined through appropriate series and parallel combinations of these capacitors. These combinations were selected based on two design objectives: (1) achieving a resonant frequency as close as possible to the target values, and (2) ensuring that the capacitor banks could withstand the anticipated voltage

Table 3.3: Comparison of simulated and experimental self and mutual inductance values

Parameter	Simulated Value	Experimental Value
L_1 (Self-inductance of primary coil)	756.2 μH	669.5 μH
L_2 (Self-inductance of secondary coil)	756.2 μH	729.0 μH
M (Mutual inductance at 15 cm air gap)	247.3 μH	207.0 μH

stress, as explained in Section 3.6.2. The selected series and parallel configurations yielded capacitance values that resulted in resonant frequencies closely matching the design targets, as summarized in Table 3.4.

Table 3.4: Designed and measured parameters of compensation capacitor banks.

Capacitor Bank	Target Resonant Frequency (kHz)	Measured Capacitance (nF)	Experimental Resonant Frequency (kHz)
Primary Capacitor Bank 1	88.0	4.89	87.96
Primary Capacitor Bank 2	86.5	5.03	86.73
Primary Capacitor Bank 3	80.5	5.86	80.30
Secondary Capacitor Bank	90.0	4.36	89.27

3.6.4 Experimental results

Using the designed and fabricated primary and secondary coils together with the corresponding compensation capacitor banks, the experimental setup was constructed as shown in Fig. 3.23. The primary coil was positioned on the bottom surface of the XYZ table, while the secondary coil was mounted on the movable arm of the same table, thereby emulating the motion of a vehicle carrying the secondary coil as it approaches a stationary primary coil installed on the ground. Once the coils were positioned, the compensation capacitor banks were connected in series configuration, a choice made to enhance the overall power transfer capability and to maximize the system efficiency.

On the primary side, the coil was interfaced with a Taraz Technologies SPM-FB-SIC single-phase inverter, which is equipped with GeneSiC G3R75MT12D SiC MOSFETs and responsible for carrying out the voltage inversion. The inverter was powered by a Chroma 62050H-600S programmable DC power supply, which provided a stable DC link voltage necessary for reliable inverter operation. The secondary side, in turn, was connected to another Taraz Technologies SPM-FB-SIC single-phase inverter. In this case, the rectification of the received AC power was carried out through the body diode of the GeneSiC SiC MOSFET. Following rectification, the output was directed to a resistive load designed to dissipate the transferred power as heat.

The switching signals required to operate the inverters were generated using a Texas Instruments LAUNCHXL-F28379D development board. For performance evaluation, input and output DC power values, along with the overall DC-DC system efficiency, were recorded using a YOKOGAWA WT332E digital power analyzer. Furthermore, the voltage and current waveforms at critical nodes in the system were captured and analyzed using a Tektronix MDO3024 mixed-domain oscilloscope.

Components used and their ratings are summarized in Table 3.5. Switching pulses were provided to the inverter through the onboard gate driver integrated within the inverter. The gate driver supports two distinct modes of operation, which can be selected via a switch embedded on the driver board. The first mode is the PWM mode, in which the user is required to provide only the UH and VH signals; the UL and VL signals are automatically generated by the dead time generation logic. In this mode, the dead time can be adjusted within the range of 0.39579 μs to 8.3 μs using the onboard dead time programming trimmer, which varies from 1 kΩ to 21 kΩ.

The second mode is the dual-input mode, where all four switching signals—UL, VL, UH,

Table 3.5: Components and their technical specifications for 2 kW charger.

Circuit Configuration	**Component**	**Ratings**
Full-Bridge Inverter	Taraz Technologies SPM-FB-SIC single-phase inverter	800V, 41A
Full-Bridge Rectifier	Body diodes of GeneSiC G3R75MT12D SiC MOSFETs	800V, 20A (per MOSFET)
Primary Compensation Capacitor Bank 1	KEMET KC33C443KJGLCAUTO	4.89nF, 7.7kV (AC), 23.8kV (DC)
Primary Compensation Capacitor Bank 2	KEMET KC33C443KJGLCAUTO	5.03nF, 7.7kV (AC), 23.8kV (DC)
Primary Compensation Capacitor Bank 3	KEMET KC33C443KJGLCAUTO	5.86nF, 6.6kV (AC), 20.4kV (DC)
Secondary Compensation Capacitor Bank	KEMET KC33C443KJGLCAUTO	4.36nF, 8.25kV (AC), 25.5kV (DC)
Gate Drivers for Inverter Switches	Integrated in SPM-FB-SIC inverter	+18V / 0V, peak drive current = 2A, Isolation voltage = 1.2kV, fast switching
DC Power Supply	Chroma 62050H-600S Programmable DC Power Supply	600V, 8.5A, 5kW
Power Analyzer	YOKOGAWA WT332E Digital Power Analyzer	600V RMS, 20A RMS, 12kW

and VH—must be provided by the user. This mode was selected during implementation because, through adjustment of the CCS (Code Composer Studio) code for the LAUNCHXL-F28379D development board, the dead time could be easily and accurately controlled, providing greater flexibility and precision in operation.

Based on the above-described setup, a 2 kW power transfer was demonstrated at an air gap of 15 cm, resulting in a maximum DC–DC efficiency of 94.86%, measured using the power analyzer as shown in Fig. 3.24, and a maximum AC–AC (resonant tank) efficiency of 97.09%,

Table 3.6: Comparison between simulated and measured coil parameters.

Parameter	Simulated / Estimated Value	Measured Value
R_1	2.32 Ω	1.5 Ω
R_2	2.32 Ω	1.8 Ω
M	247 μH	207 μH

as illustrated in Fig. 3.27. Furthermore, to verify that the maximum efficiency is achieved at the calculated $R_{L\_\eta m}$ of 158 Ω (based on (2.18) and measured values), experimental efficiency was evaluated for different R_L values, as shown in Fig. 3.25. The results confirm that efficiency is maximized at the calculated value of 158 Ω. Additionally, the k/k_{crit} ratio remains well below 1 for all considered load conditions, as calculated from experimental measurements (see Fig. 3.26), ensuring bifurcation-free operation.

The efficiency in Fig. 3.10 is calculated considering only the resonant tank, without accounting for switching losses. Accordingly, it is compared with the resonant tank efficiency obtained experimentally for $N = 24$, as shown in Fig. 3.27. A discrepancy is observed between the experimental and simulated results, since the simulated value of M and estimated values of R_1, and R_2 differ from the measured values as shown in Table 3.6. When the efficiency is recalculated using the measured parameters, the results align closely with the experimental values, as shown in Fig. 3.28.

The results clearly demonstrate that the proposed optimization approach enables substantially higher efficiency while maintaining bifurcation-free operation.

3.7 Summary

This chapter details the design, optimization, and experimental validation of a 2 kW WPT system operating across a 15 cm air gap, using identical Archimedean spiral coils with series

compensation. The focus is on achieving high efficiency while maintaining bifurcation-free operation.

The chapter introduces a novel design methodology for Archimedean spiral coils that simultaneously maximizes efficiency and ensures bifurcation-free behavior. The methodology guides the selection of coil parameters and compensation capacitances, supported by simulation and experimental studies. ANSYS Maxwell and PLECS simulations were used to evaluate coil performance, while the experimental platform enabled detailed assessment under realistic operating conditions.

Primary and secondary coils were fabricated using litz wire and 3D-printed tracks to ensure precise turn spacing and consistent geometry. Compensation capacitor banks were designed to resonate at the desired frequency while accounting for voltage stresses and ESR. The experimental platform allowed measurement of coil characteristics, resonant frequency, and voltage stresses, verifying the efficacy of the proposed coil design methodology.

The results confirm that the proposed design approach achieves high DC–DC efficiency, maximizes power transfer, and avoids bifurcation across the tested load and air-gap conditions. Unlike existing bifurcation-avoidance design guidelines, which often reduce efficiency or lack a systematic approach, the proposed methodology provides a practical, repeatable framework for optimizing coil design in high-power WPT systems.

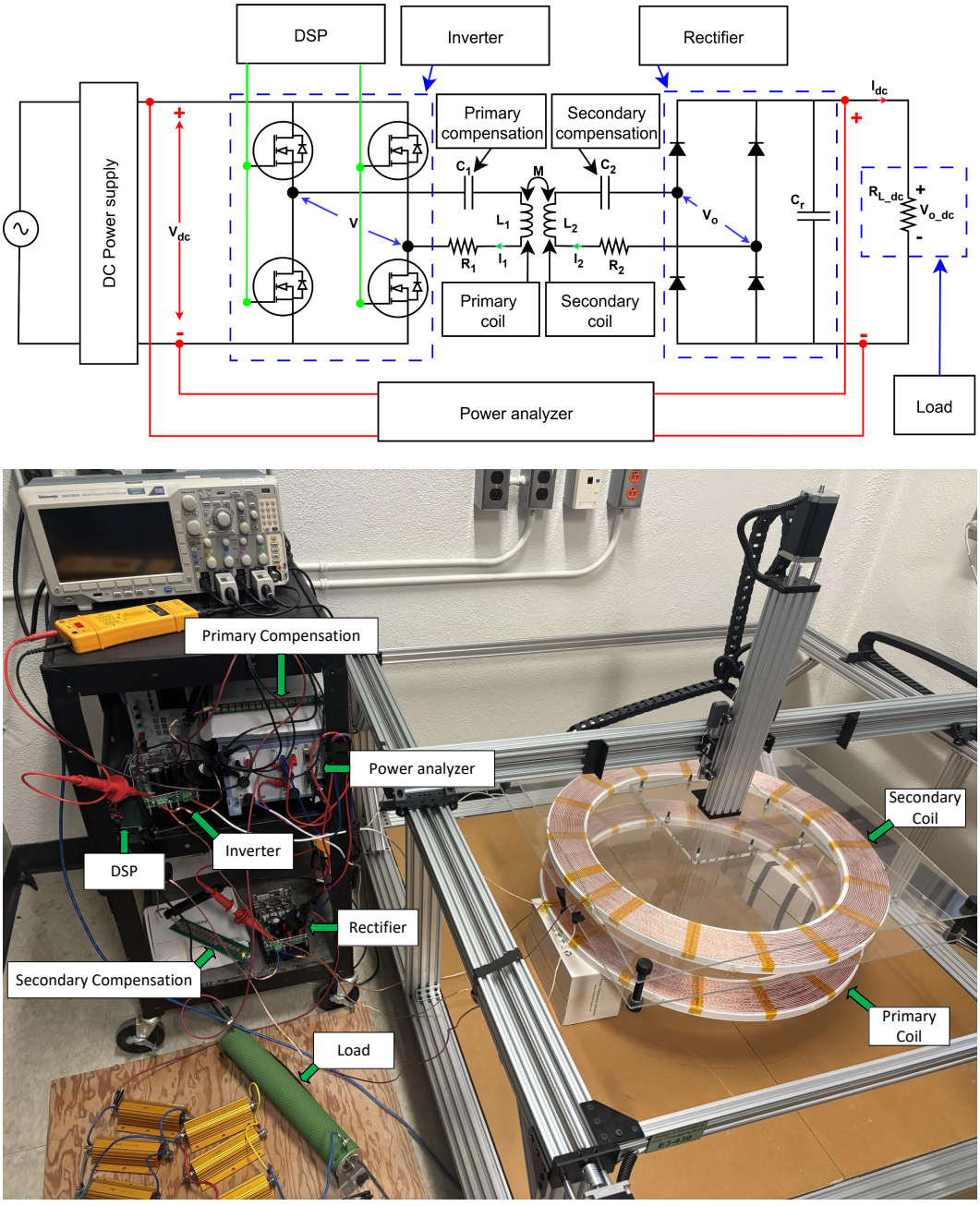

Fig. 3.23: Experimental wireless power transfer system incorporating primary and secondary coils, compensation capacitor banks, power electronics interfaces, and measurement instruments.

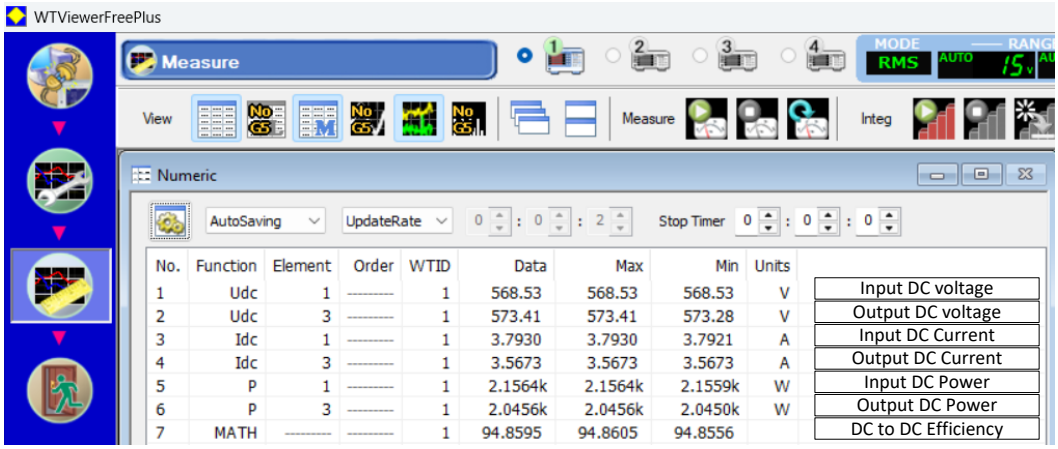

Fig. 3.24: Power analyzer output showing DC–DC efficiency and power delivery at 2 kW output power for a 15 cm air gap.

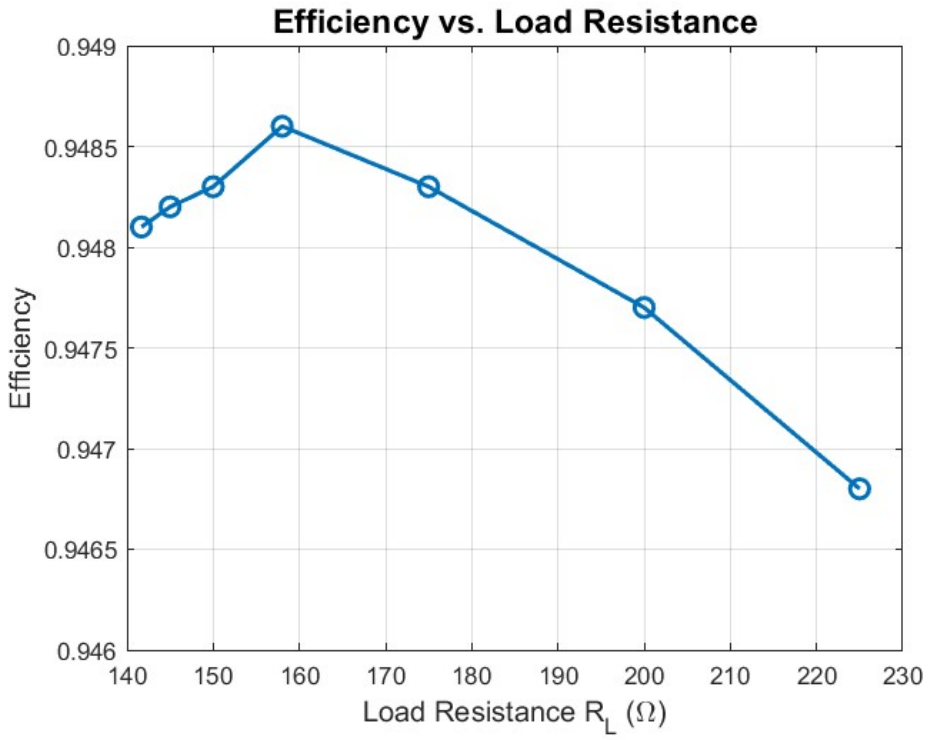

Fig. 3.25: Experimental DC-DC efficiency variation with R_L at 2 kW output power for a 15 cm air gap.

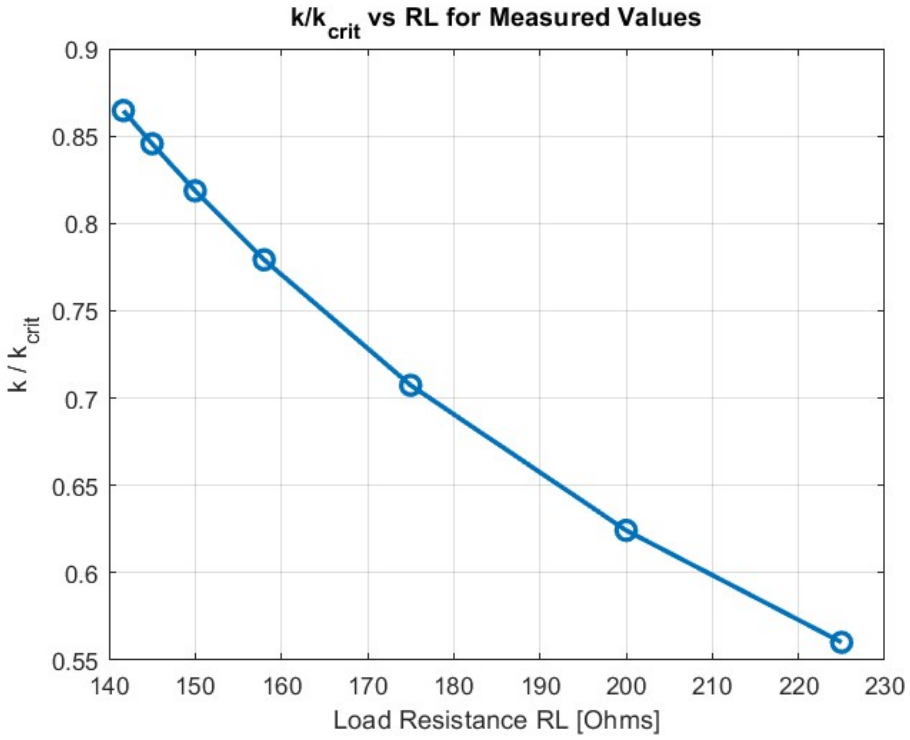

Fig. 3.26: k/k_{crit} ratio derived from measured coil characteristics across different load conditions.

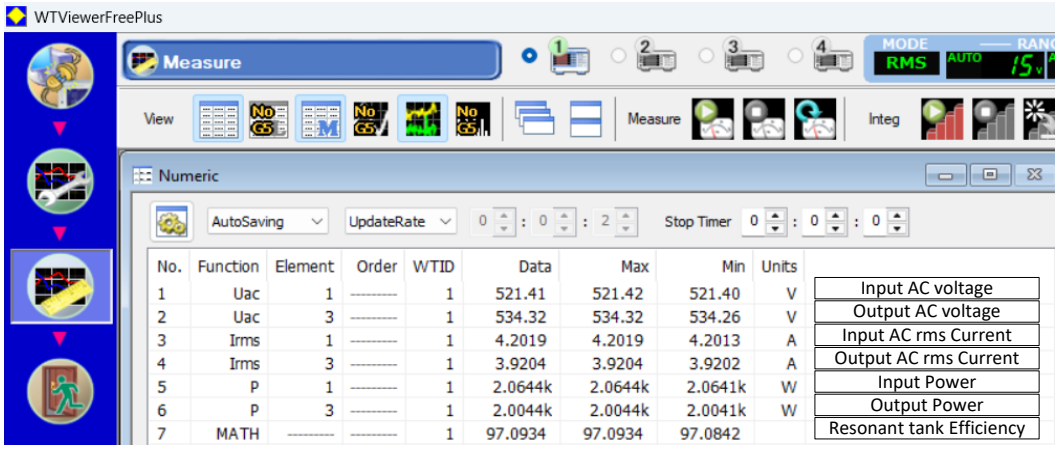

Fig. 3.27: Experimental resonant tank maximum efficiency at R_{L_nm}.

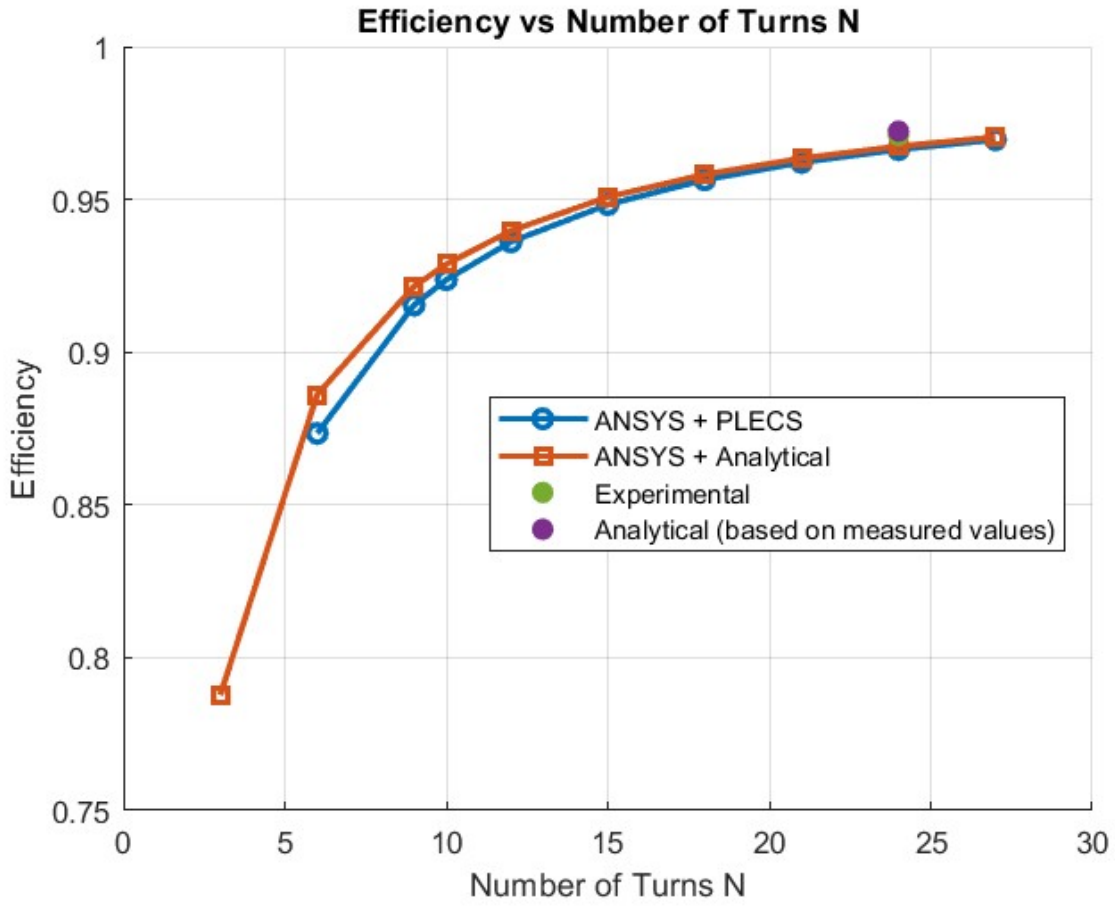

Fig. 3.28: Comparison of resonant tank efficiency variation with coil turn number N, showing simulated and analytically obtained results alongside experimental measurement and recalculated efficiency based on measured coil parameters.

Chapter 4

Zero-Voltage Switching Performance under Capacitor Aging and Tolerance Effects

4.1 Theoretical Background of ZVS for Full-Bridge Wireless Power Transfer

WPT systems designed for high-power applications frequently require high power density to enable more compact power electronic components and to promote improved as well as more cost-effective manufacturability. Achieving this objective is commonly facilitated by the use of elevated switching frequencies [58]. However, the use of higher switching frequencies inherently increases switching losses, necessitating the implementation of soft switching techniques. These techniques help minimize losses and mitigate the limitations on operating frequency imposed by the power dissipated during the on/off transitions of the

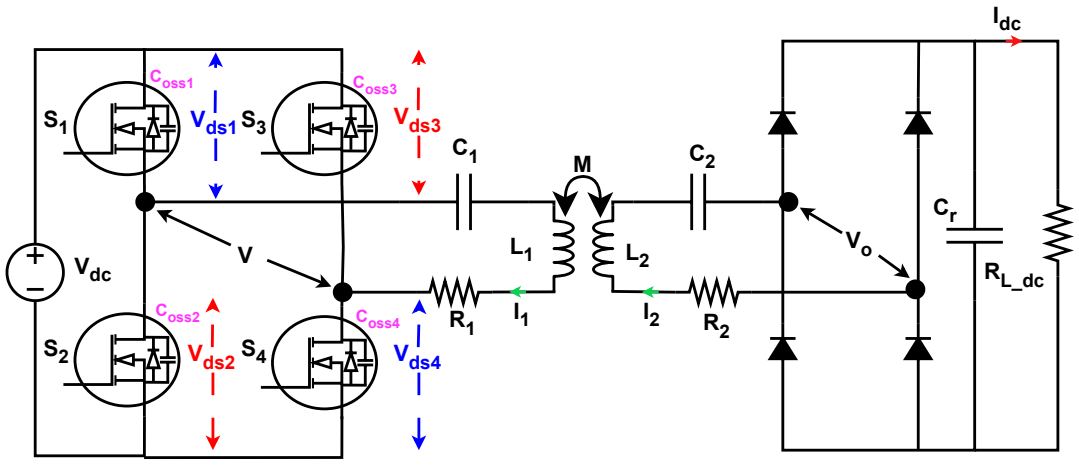

Fig. 4.1: Detailed Series - Series compensated WPT circuit representation with inclusion of MOSFET output capacitances

switches at elevated frequencies.

Soft-switching in power electronic converters is commonly achieved through techniques such as ZCS or ZVS. In this thesis, ZVS operation was adopted, as it is particularly well-suited for MOSFET-based inverters, reducing switching losses and stress on the devices [59].

In order to realize ZVS, the inverter must operate with an effective inductive load [60]. This condition is obtained by choosing the switching frequency slightly above the natural resonant frequency of the system. Accordingly, the secondary coil is tuned to match the switching frequency, while the primary coil remains tuned to the fundamental resonant frequency. Under this arrangement, the overall impedance of the WPT network appears inductive to the inverter.

Fig. 4.1 shows the detailed SS compensated WPT circuit representation including the MOSFET output capacitances. All components retain the same definitions as in Section 2.2. In addition, C_{oss1}, C_{oss2}, C_{oss3}, and C_{oss4} denote the nonlinear, voltage-dependent parasitic

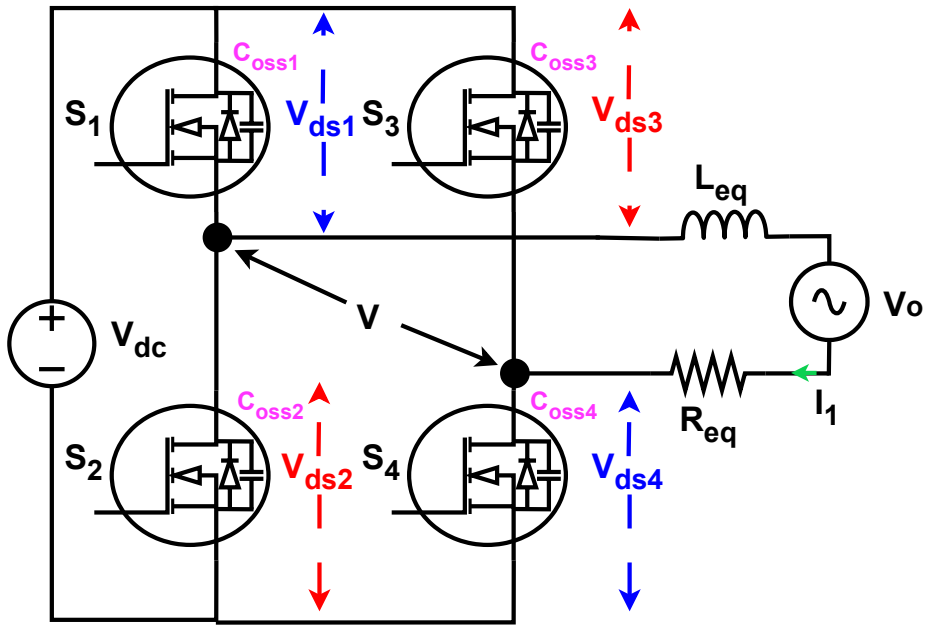

Fig. 4.2: Series - Series compensated equivalent WPT circuit representation with inclusion of MOSFET output capacitances

capacitances of MOSFETS 1, 2, 3, and 4, respectively. Similarly, V_{ds1}, V_{ds2}, V_{ds3}, and V_{ds4} represent the drain-to-source voltages across MOSFETS 1, 2, 3, and 4 at any given instant.

With the assumption that the secondary side is tuned to the switching frequency, while the primary side remains slightly inductive at this frequency, the equivalent circuit shown in Fig. 4.2 can be derived. In this representation, L_{eq} denotes the equivalent self-inductance of the primary side at the selected switching frequency, and R_{eq} represents the combined effect of the AC ESR of the primary coil together with the reflected AC ESR of the secondary coil at the set switching frequency.

In a conventional full-bridge (FB) modulation scheme, switches S_1 and S_4 are turned on and off simultaneously, while S_2 and S_3 operate in a complementary manner with respect to S_1 and S_4. This switching strategy is typically employed to avoid shoot-through faults (short circuits within a phase leg) and to minimize conduction losses that would otherwise arise if both the upper and lower switches in the same leg, such as S_1 and S_2, were conducting simultaneously.

With this type of switching scheme, the drain-to-source voltage of the non-conducting MOSFET pair increases toward the DC-link voltage V_{dc} as their parasitic output capacitances are charged. In order to minimize significant turn-on switching losses, these parasitic capacitances must be fully discharged prior to the next turn-on transition, ensuring that the voltage across the switches becomes zero. This condition, known as ZVS, effectively reduces power dissipation during the turn-on event. ZVS is typically achieved by introducing a sufficient dead time t_d during the switching transition period, during which both the upper and lower devices of a phase-leg are kept OFF. During this interval, the current flowing through the equivalent inductance L_{eq} discharges the parasitic capacitances of the previously non-conducting switch pair to zero, while simultaneously charging the capacitances of the previously conducting pair up to the DC-link voltage V_{dc}.

In this switching scheme, the drain-to-source voltage of the non-conducting MOSFET pair rises toward the DC-link voltage V_{dc} as their parasitic output capacitances are charged. To avoid significant turn-on switching losses, these capacitances must be completely discharged before the devices are turned on again, ensuring that the voltage across the switches is zero at the instant of turn on. This condition, referred to as ZVS, minimizes power dissipation at turn-on. ZVS is realized by introducing a sufficient dead time t_d in the switching transition interval, where both the upper and lower devices of a phase-leg remain OFF. In

this interval, the current flowing through the equivalent inductance L_{eq} forces the parasitic capacitances of the non-conducting switch pair to discharge to zero, while at the same time charging the capacitances of the previously conducting pair up to the DC-link voltage V_{dc}.

The time required for the parasitic capacitance to fully discharge is denoted as t_{dis} in this thesis. In general, to ensure ZVS operation, the applied dead time t_d must be greater than t_{dis} at each switching transition. Furthermore, t_{ZVS} is defined as the interval between the falling edge of the control signal and the instant when $I_1 = 0$. These definitions are illustrated in Fig. 4.3, which presents the typical operational waveforms of the WPT system.

When the dead time is excessively long, i.e., $t_d > t_{ZVS}$, a voltage notch can occur, a phenomenon also referred to as voltage polarity reversal [61, 62]. This phenomenon occurs when current reversal forces the discharged parasitic capacitors to recharge, resulting in a temporary voltage reversal across the load. This appears as a notch in the waveform and leads to distortion, extra switching losses, and increased device stress.

Considering these factors, it can be concluded that achieving ZVS without encountering the voltage notch phenomenon requires maintaining the dead time t_d within the limits specified in (4.1) for each switching transition.

$$t_{dis} \leq t_d \leq t_{ZVS} \tag{4.1}$$

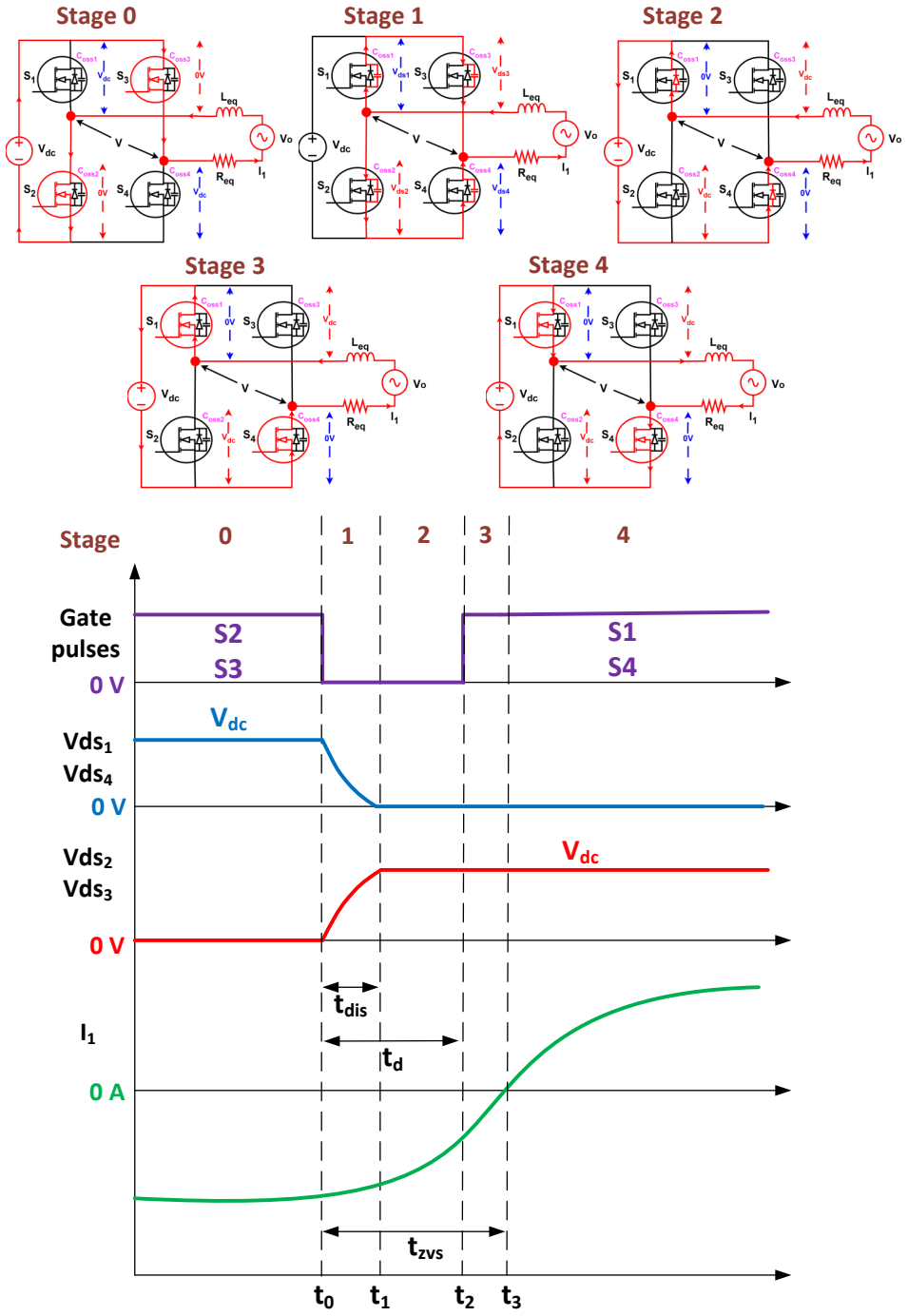

Fig. 4.3: Typical operational waveforms of the WPT system illustrating dead time (t_d), discharge time (t_{dis}), and ZVS interval (t_{ZVS}).

4.2 Review of dead time selection Techniques

4.2.1 Theoretical Background and dead time Selection Principles

t_{dis} and t_{ZVS} are not fixed, but vary with operating conditions, including M, V_{DC} and R_{L_dc}. This implies that a t_d value chosen for a particular operating condition may not be universally valid. Under different conditions, it can either be too short, leading to incomplete discharge of the parasitic capacitance and loss of ZVS, or too long, resulting in the voltage notch phenomenon when t_d exceeds the ZVS interval. Therefore, careful consideration is required when selecting the t_d to ensure reliable ZVS operation across the entire operating range. Given this necessity, extensive research has been conducted to determine optimal methods for selecting the dead time.

The existing literature on dead time selection can be broadly categorized into two main approaches: *fixed dead time* and *variable dead time* schemes. Fixed dead time schemes account for the variation of t_{dis} over the entire operating range and select a constant dead time value slightly greater than t_{dis_M}, the maximum discharge time across all operating conditions. In contrast, in variable dead time schemes, the dead time is adaptively adjusted at each switching instance based on measured parameters such as the input DC voltage and the turn-off current, $I_1(t_0)$, which corresponds to the current in the WPT circuit at the instant of switch turn-off.

Fixed dead time strategies differ primarily in the way t_{dis} is estimated. Two main analytical approaches are commonly reported in the literature: charge-based and energy-based methods [63]. In [64] a charge-based analytical approach is employed for dead time determination. Within this method, it is assumed that the stored charge in the parasitic capacitance must be completely discharged by the turn-off current, $I_1(t_0)$, within the dead

time interval. To simplify the analysis, both the turn-off current $I_1(t_0)$ and the MOSFET output capacitance, C_{oss}, are treated as constants throughout the dead time duration. Based on these assumptions, the discharge time t_{dis} can be derived, as shown in (4.2). However, practical operation deviates from these simplifications. As illustrated in Fig. 4.3, the turn-off current $I_1(t_0)$ does not remain constant during the dead time but instead varies dynamically. Furthermore, C_{oss} is inherently nonlinear and strongly dependent on the drain-to-source voltage of the MOSFETs [65,66]. As a result, these assumptions introduce inaccuracies, and the ZVS condition cannot be reliably evaluated using this method.

$$t_{dis} = \frac{2C_{oss}V_{dc}}{I_1(t_o)} \tag{4.2}$$

In [63], a modified energy-based analytical approach is proposed for determining the dead time. This method assumes that the energy stored in the equivalent inductance L_{eq} of the WPT system is sufficient to completely discharge the parasitic output capacitances of the MOSFET switches. The relationship can be mathematically expressed as shown in (4.3).

$$\frac{1}{2}L_{eq}[I_1^2(t_0) - I_1^2(t_1)] \geq 2Q_{oss}(V_{dc})V_o \tag{4.3}$$

Here, $Q_{oss}(V_{dc})$ denotes the total charge stored in the parasitic output capacitance of a MOSFET for a given V_{dc}. When switches S_1 and S_4 are operated simultaneously, their output capacitances C_{oss1} and C_{oss4} appear in series. As a result, the total charge stored across C_{oss1} and C_{oss4} is equal to $Q_{oss}(V_{dc})$. In the same manner, C_{oss2} and C_{oss3} undergo an equivalent discharge process. As discussed in [67], for the purpose of simplifying MOSFET modeling, a linear charge-equivalent capacitance C_{eq} can be defined. This capacitance corresponds to

the same stored charge as that of the nonlinear C_{oss} at a particular drain–source voltage V_{ds}, and is represented mathematically in (4.4).

$$C_{eq}(V_{ds}) = \frac{Q_{oss}(V_{ds})}{V_{ds}} \tag{4.4}$$

Based on (4.4), (4.3) can be updated to obtain (4.5).

$$\frac{1}{2}L_{eq}[I_1^2(t_0) - I_1^2(t_1)] \geq 2V_{dc}C_{eq}(V_{dc})V_o \tag{4.5}$$

With (4.5) established, and referring to Fig. 4.2 and Fig. 4.3, the discharge time for a given operating condition can be determined using (4.6) and ZVS interval t_{ZVS} can be determined by (4.7). In this context, ω represents the switching frequency, which is considered constant, while $I_{1,\max}$ denotes the peak instantaneous value of the primary current I_1, as defined in (4.8). The input voltage V_{dc} corresponding to a given output power P_{out} can be obtained from (4.9). Furthermore, $I_1(t_0)$ and $I_1(t_1)$ are derived using (4.10) and (4.11), respectively.

$$t_{dis} = \left| \frac{arcsin[\frac{I_1(t_1)}{I_{1\_max}}] - arcsin[\frac{I_1(t_0)}{I_{1\_max}}]}{\omega} \right| \tag{4.6}$$

$$t_{ZVS} = \left| \frac{arcsin[\frac{I_1(t_0)}{I_{1\_max}}]}{\omega} \right| \tag{4.7}$$

$$I_{1\_max} = \left| \frac{\sqrt{2}V_{dc}}{R_1 + \frac{\omega^2 M^2}{R_2+R_L} + j\omega L_{eq}} \right| \tag{4.8}$$

$$V_{dc} = \frac{\pi}{2\sqrt{2}} \sqrt{\frac{P_{out}(R_2+R_L)^2[(R_1 + \frac{\omega^2 M^2}{R_2+R_L})^2 + \omega^2 L_{eq}^2]}{\omega^2 M^2 R_L^2}} \tag{4.9}$$

$$I_1(t_0) = I_{1\_max} sin[arctan(\frac{\omega L_{eq}}{R_1 + \frac{\omega^2 M^2}{R_2 + R_L}})] \tag{4.10}$$

$$I_1(t_1) = \sqrt{\frac{2[\frac{1}{2} L_{eq} I_1^2(t_0) - 2V_{dc} C_{eq}(V_{dc}) V_o]}{L_{eq}}} \tag{4.11}$$

This method provides a more accurate estimation compared to the charge-based approach. However, it is not entirely precise, as practical factors such as parasitic effects in the experimental setup introduce deviations. In addition, the estimation of parasitic capacitances is typically derived from datasheet specifications, which may not accurately represent the actual device behavior under operating conditions.

In the variable dead time strategy presented in [68], the discharge time of the parasitic capacitance, t_{dis}, is experimentally determined offline for various operating points, defined by the drain-to-source voltage V_{ds} and the turn-off current $I_1(t_0)$. These experimentally obtained values are then stored in the microcontroller's memory. During real-time operation, V_{ds} and $I_1(t_0)$ are sampled in every switching cycle using sensors. The controller determines the appropriate dead time by referencing a preconstructed lookup table. Since it is impractical to experimentally measure the optimal dead time for every possible combination of V_{ds} and $I_1(t_0)$, linear interpolation is employed to estimate the minimum required dead time for intermediate operating points.

This method is adopted to achieve higher accuracy, as demonstrated in [68], where it is shown that selecting the dead time solely from analytically estimated t_{dis} can result in either underestimation or overestimation. Such inaccuracies may cause efficiency degradation, either through the loss of ZVS or the occurrence of the voltage notch phenomenon. Although this approach improves precision, it requires more sophisticated control and incurs higher

implementation costs compared to fixed dead time schemes.

4.2.2 Experimental Verification of dead time Selection Methods

The claims presented in the existing dead time selection approaches were subsequently verified experimentally. First, the Energy-based analytical dead time estimation, as described in [63], was implemented to assess whether it provides reasonably accurate dead time values that closely align with experimental measurements. Next, the assertion from [68] that the dead time should be minimized at all times to reduce efficiency loss was experimentally verified. Specifically, it was examined whether excessive dead time leads to increased losses due to conduction in the diodes, as opposed to conduction losses across the MOSFETs at higher power levels, thereby confirming the practical impact of dead time selection on overall system efficiency.

Experimental Verification of Energy-Based Analytical dead time Estimation

To evaluate the accuracy of the Energy-based analytical dead time estimation, both analytical and experimental assessments were conducted for an air gap of 15 cm, representing the nominal operating distance, as well as for reduced gaps of 14 cm and 13 cm to simulate the effects of vehicle loading or decreased tire pressure. The evaluations were performed using load resistances of 175 Ω, 200 Ω, and 225 Ω, corresponding to different operational regions of the system.

Analytical equations from (4.6) to (4.11) were employed to calculate the dissipation time t_{dis} under the various operating conditions described above. The equivalent capacitance, C_{eq}, required for these calculations was estimated based on the nonlinear variation of the parasitic capacitance (C_{oss}) with V_{ds}, as shown in Fig. 4.4 of the G3R75MT12D SiC MOSFET

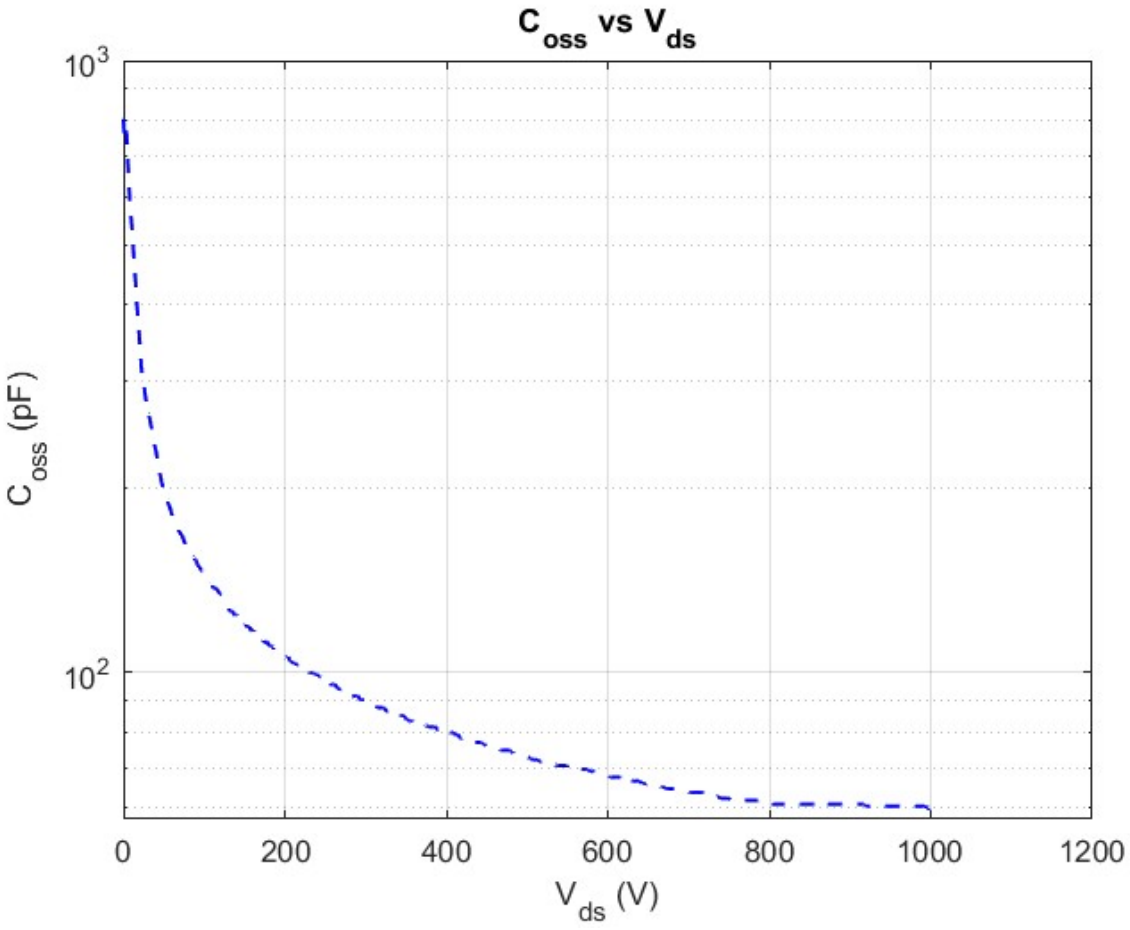

Fig. 4.4: Nonlinear variation of the parasitic capacitance C_{oss} with V_{DS} for the G3R75MT12D Si MOSFET, as provided in the datasheet.

datasheet, which was used for experimental verification. To facilitate analytical modeling, the charge-equivalent capacitance C_{eq} shown in Fig. 4.5 was derived using

$$C_{\text{eq}}(V_{\text{ds}}) = \frac{\int_0^{V_{\text{ds}}} C_{\text{oss}}(v)\, dv}{V_{\text{ds}}} \tag{4.12}$$

as described in [67].

The experimental setup described in Section 3.6 was used to experimentally obtain the

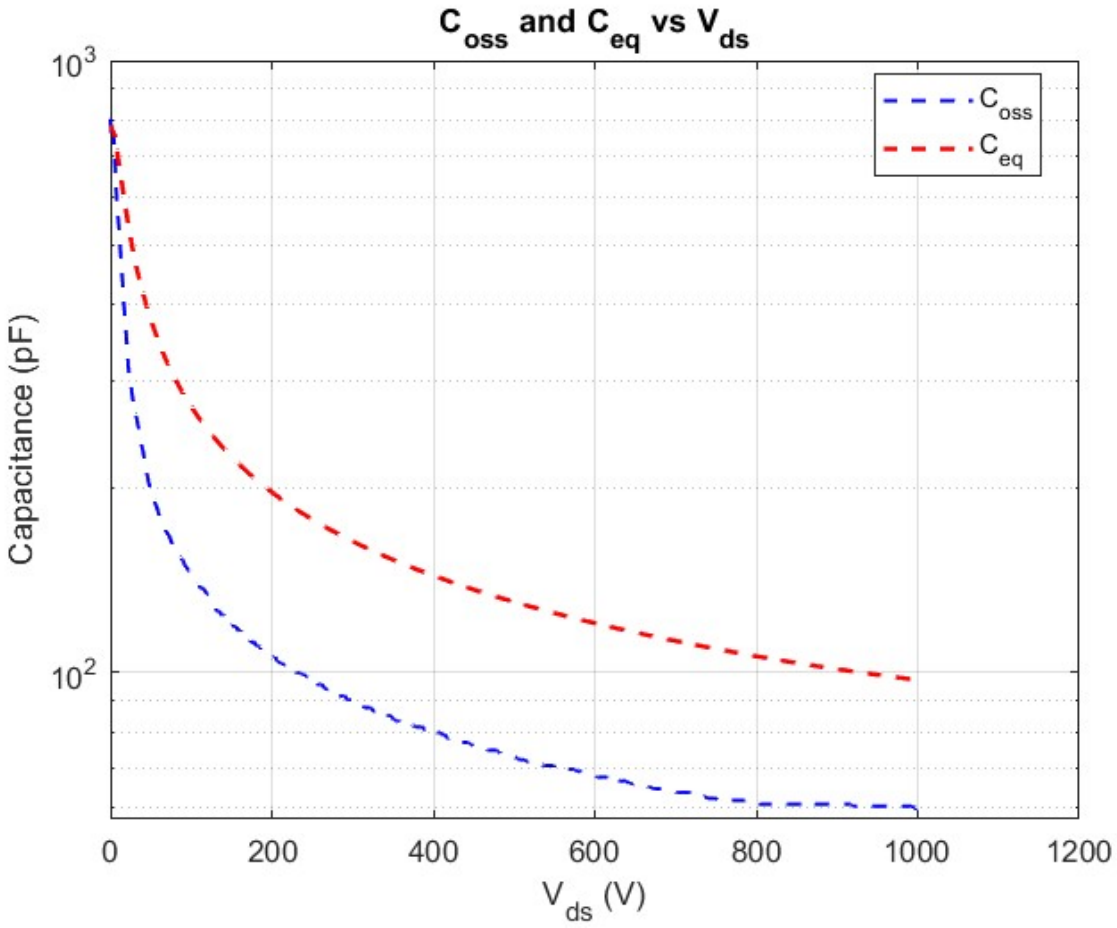

Fig. 4.5: Charge-equivalent capacitance C_{eq} used for analytical calculations, derived from the C_{oss} characteristics

discharge times t_{dis}, which were then compared with the energy-based analytical values, as shown in Fig. 4.6. Consistent with the observations reported in [68], noticeable deviations were observed. The primary cause of these deviations is that the C_{eq} estimated from the datasheet information is not sufficiently accurate. Therefore, it can be concluded that relying solely on this method to estimate the dead time may result in insufficient duration to fully discharge the capacitance, potentially leading to a loss of ZVS.

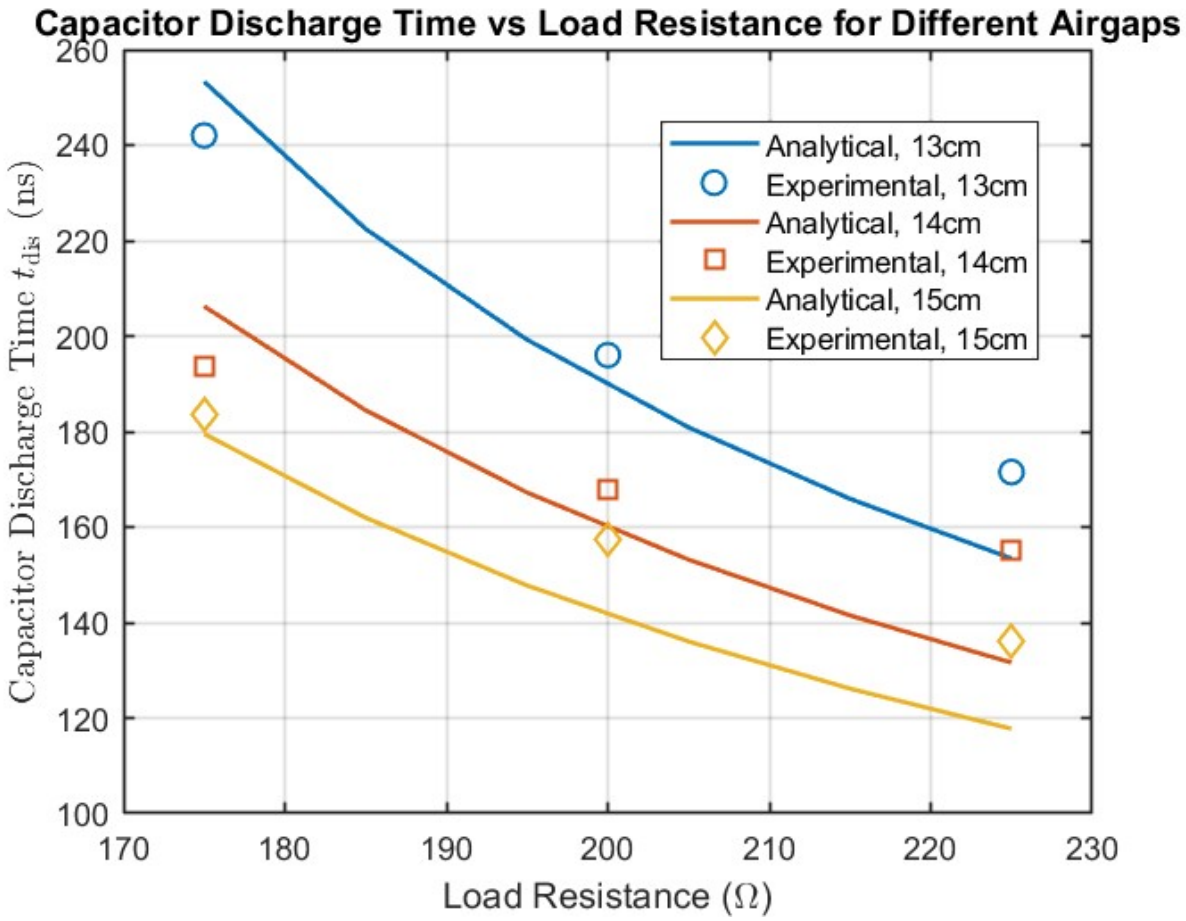

Fig. 4.6: Analytical and experimental capacitor discharge time t_{dis} versus load resistance for different airgaps.

Experimental Verification of Efficiency Impact of Excessive Dead Time

[68] highlights the importance of minimizing dead time to maximize efficiency. Beyond the obvious efficiency loss caused by ZVS violation when the condition in (4.1) is not satisfied, the study also claims that excessive dead time can lead to additional losses. This is because, during excessive dead time, current flows through the body diodes instead of the MOSFETs, and since body diodes generally have higher conduction losses, the total loss increases. While

this claim is theoretically valid, it has not been experimentally quantified to assess the practical impact on efficiency. To investigate this, experimental measurements were conducted under the same conditions as the preceding section. Two dead times, 220 ns and 310 ns, both ensuring ZVS is maintained, were tested. As shown in Fig. 4.7 and Table 4.1, the impact on efficiency is minimal. Therefore, for the conditions investigated in this study, it can be concluded as a novel finding that, as long as ZVS is maintained, operating with a slightly longer dead time does not significantly reduce efficiency. This result indicates that the commonly stated assumption in the literature—that dead time must always be minimized—does not hold in all cases. Consequently, the primary focus should be on ensuring ZVS rather than minimizing dead time at the cost of increased control complexity.

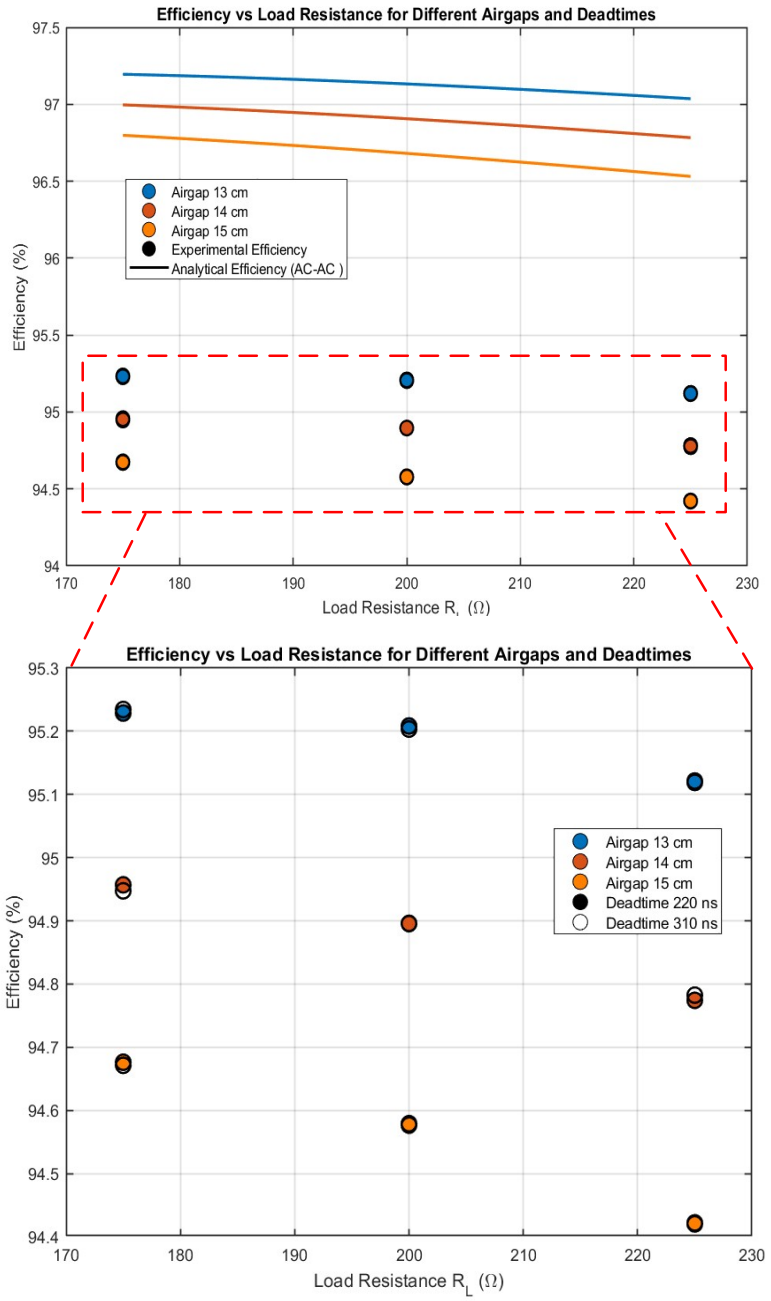

Fig. 4.7: Experimental comparison of system efficiency (DC-DC) for two dead time settings (220 ns and 310 ns) evaluated across multiple air-gap distances and load conditions.

Airgap (cm)	Deadtime (ns)	175 Ω	200 Ω	225 Ω
13	220	95.23 %	95.21 %	95.12 %
	310	95.23 %	95.20 %	95.12 %
14	220	94.96 %	94.90 %	94.77 %
	310	94.95 %	94.90 %	94.78 %
15	220	94.68 %	94.58 %	94.42 %
	310	94.67 %	94.58 %	94.42 %

Table 4.1: Summary of measured efficiencies (DC-DC) for different air-gap distances, load conditions, and dead time settings.

4.3 Experimental Investigation of Capacitor Tolerance and Aging Effects on ZVS

As discussed in Section 4.2, conventional methods of selecting the optimum dead time generally assume that the values of the primary and secondary compensation capacitors remain constant. In practice, however, this assumption is not valid. Compensation capacitors are subjected to high voltage stress, as demonstrated in Section 3.6, which accelerates aging and leads to changes in their capacitance values. Furthermore, practical factors such as manufacturing tolerance and long-term aging both contribute to variations in capacitance, which can significantly influence the resonant conditions and the corresponding ZVS behavior.

To evaluate the impact of capacitance tolerance and aging on the discharge time (t_{dis}) and ZVS interval (t_{ZVS}), this study considers a scenario where only the primary compensation capacitance is affected. The secondary capacitance is assumed to remain unchanged; however, in practice, both primary and secondary capacitors would be influenced. This simplification is made to isolate and clearly illustrate the effect on t_{dis} and t_{ZVS}, acknowledging that in a practical system the combined impact would be more pronounced.

The degree of capacitance variation arising from tolerance and aging can differ substantially depending on the capacitor technology, dielectric material, and operational stress

conditions. While stable Class I or II ceramic capacitors generally exhibit only moderate degradation, more pronounced variations can occur under prolonged high-voltage and high-temperature operation, as well as across different capacitor types.

Capacitors with highly stable dielectrics, such as the KEMET CKC33C103GJGAC7210, which uses a C0G (NP0) dielectric, demonstrate minimal combined aging and tolerance effects of less than 3% [69]. These capacitors are particularly well suited for WPT applications, where resonant network performance and efficiency are highly sensitive to capacitance deviations. As noted in industry literature, high-stability C0G MLCCs are commonly employed in magnetic resonance-based WPT systems to maintain precise resonance conditions and ensure reliable power transfer [70].

In practical WPT systems, however, general-purpose ceramic or film capacitors may also be used, which typically exhibit considerably higher tolerance and aging effects compared to high-stability C0G types. To ensure a comprehensive assessment of system robustness, two representative scenarios were examined: one reflecting a realistic case, where tolerance and aging effects are modest (3% for the purposes of this study), and another representing an extreme condition, where a combined impact of 19.8% is considered. This approach allows the evaluation of WPT performance, capturing the potential effects of both modest and severe variations in the compensation capacitance.

4.3.1 Analysis Under Moderate Capacitance Deviation (3%)

Primary capacitor bank 2, with a capacitance of 5.03 nF, was considered as the baseline design value (nominal), while primary capacitor bank 1, with a capacitance of 4.89 nF, represented the condition after the combined effects of capacitor tolerance and aging, corresponding to an approximate 3% reduction. In this context, the chosen margin provides

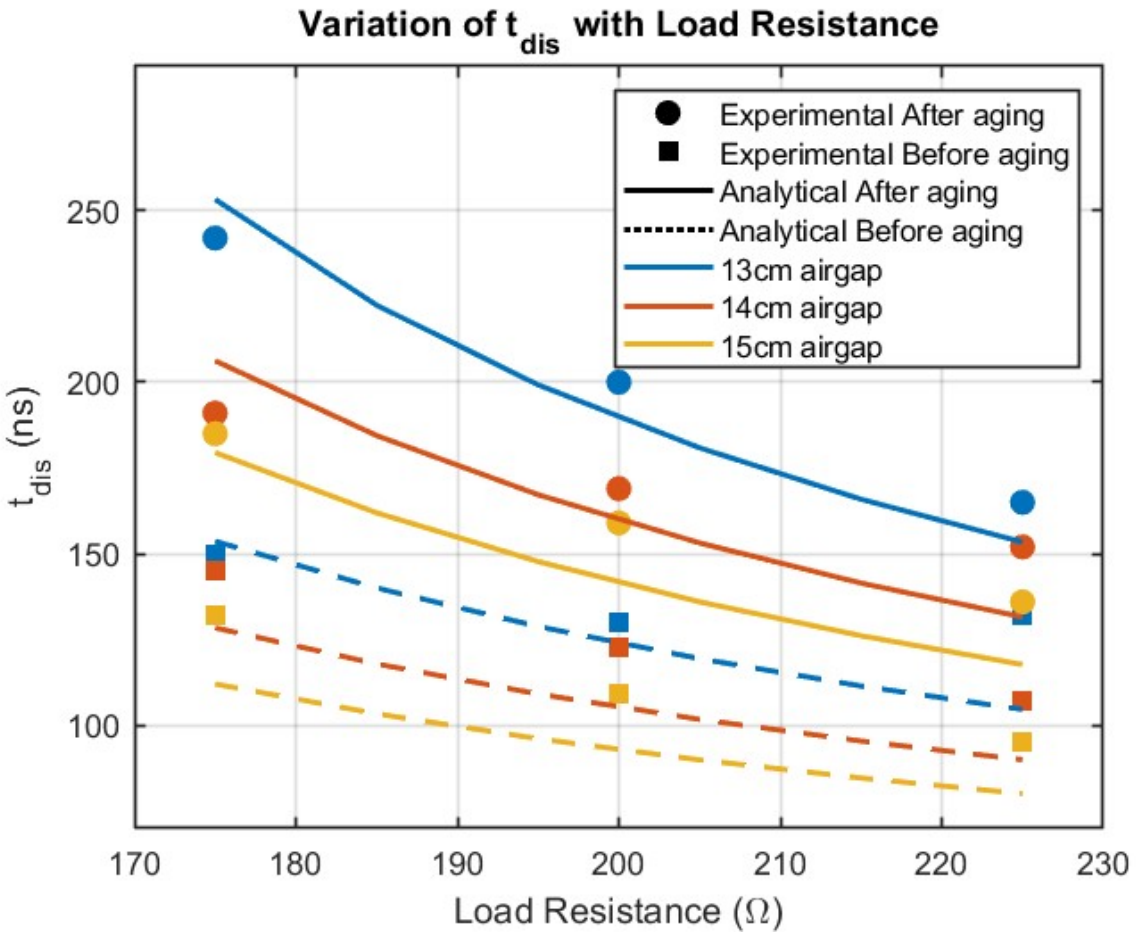

Fig. 4.8: Experimental variation of t_{dis} under different operating conditions, illustrating the impact of aging and tolerance.

a practical and conservative allowance, ensuring robust system performance under realistic operating conditions. The same operating regions considered in Section 4.2.2 were used for this analytical evaluation.

t_{ZVS} and t_{dis} were measured from oscilloscope waveforms under various operating conditions. The variation of t_{dis} across different operating points and with different primary capacitor banks, emulating the combined effects of aging and tolerance, is presented in Fig. 4.8. Similarly, the variation of t_{ZVS} under the same conditions is shown in Fig. 4.9.

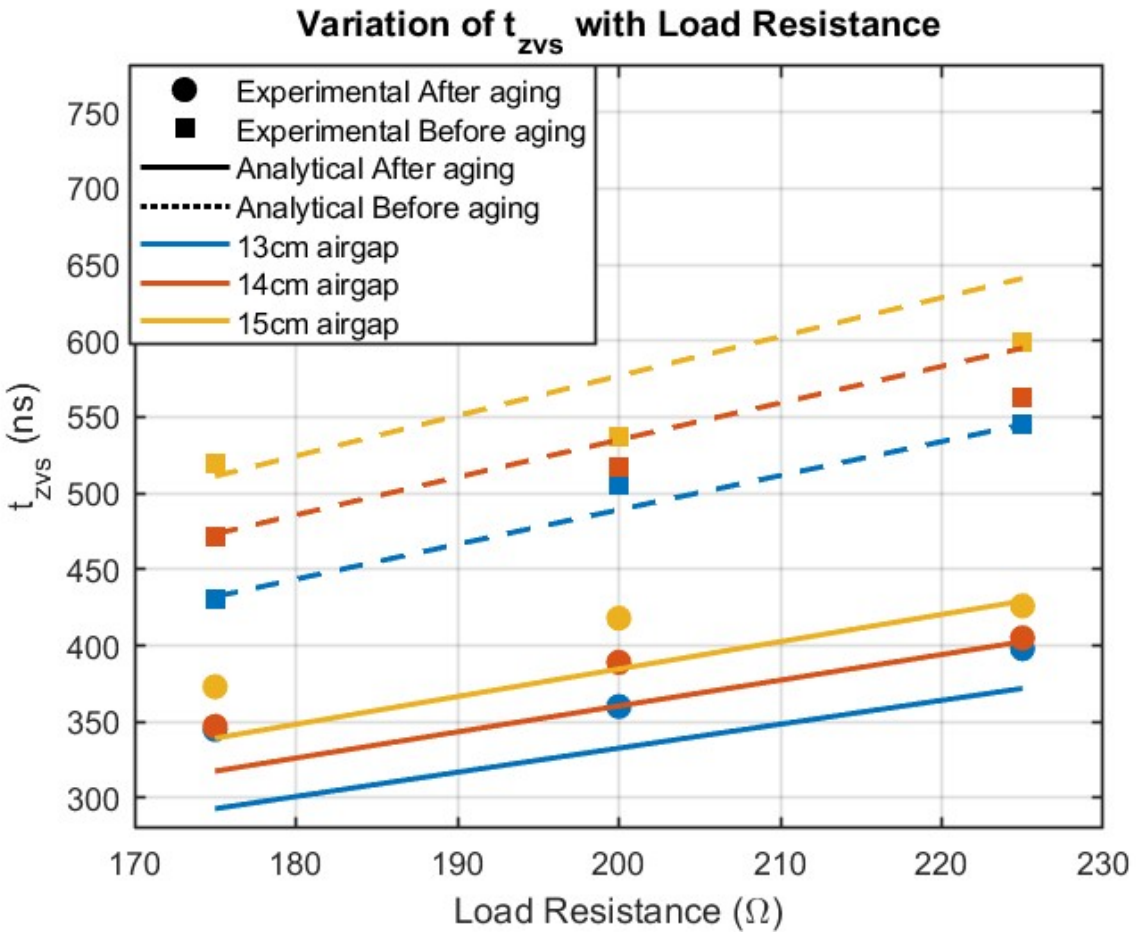

Fig. 4.9: Experimental variation of t_{ZVS} under different operating conditions, illustrating the impact of aging and tolerance.

Given that t_{ZVS} and t_{dis} vary with the operating conditions, (4.1) can be modified as (4.13), where $t_{\mathrm{dis\_M}}$ denotes the maximum t_{dis} over the entire operational range, and $t_{\mathrm{ZVS\_m}}$ denotes the minimum t_{ZVS} interval across the full operational region.

$$t_{dis\_M} \leq t_d \leq t_{ZVS\_m} \tag{4.13}$$

Based on the experimental results presented in Fig. 4.8 and Fig. 4.9, along with (4.13), it

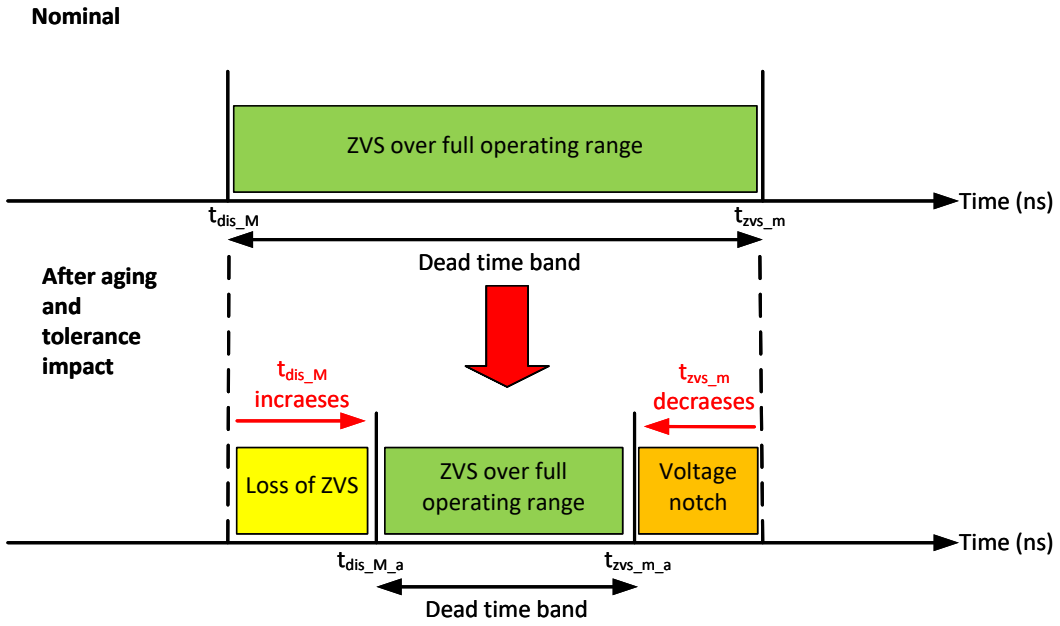

Fig. 4.10: Shrinking of the dead time band with aging and tolerance, as determined from experimental results under different operating conditions.

is evident that the lowest load and smallest air gap correspond to both $t_{\mathrm{dis\_M}}$ and $t_{\mathrm{ZVS\_m}}$ under both aging and tolerance conditions. Additionally, for each operating point, t_{dis} increases with aging and tolerance while t_{ZVS} decreases. Therefore, it can be concluded that the dead time band defined by (4.13) shrinks with aging and tolerance, as illustrated in Fig. 4.10. $t_{\mathrm{dis\_M\_a}}$ corresponds to the $t_{\mathrm{dis\_M}}$ value after aging and tolerance, and $t_{\mathrm{ZVS\_m\_a}}$ corresponds to the $t_{\mathrm{ZVS\_m}}$ value after aging and tolerance.

The observations in Fig. 4.10 indicate that, due to the combined effects of aging and tolerance, a dead time that ensured ZVS (yellow region) before these effects may no longer maintain it afterward. Likewise, a dead time that initially achieved ZVS (orange region)

prior to aging and tolerance may result in voltage notches and increased switching losses once these effects take place.

From the preceding findings, it can be inferred that setting the dead time equal to or close to the t_{dis} value calculated using nominal capacitance value, while assuming no impact of aging or tolerance as suggested in [63,68], may result in loss of ZVS in practical operation where aging and tolerance effects are present. To quantify the resulting efficiency loss, experimental verification was performed to compare the system efficiency when the dead time is set according to the methods in [63, 68] versus when the dead time is adjusted to account for the effects of aging and tolerance, i.e., set slightly longer within the dead time band that remains valid after considering aging and tolerance (green region in the lower subplot of Fig. 4.10).

To ensure a fair comparison, the critical operating point that defines the dead time boundary, as expressed in (4.13), was considered. This operating point corresponds to the minimum load and minimum air gap, namely 175 Ω and 13 cm, respectively.

The dead time estimated using the Energy-based analytical method from [63] was 154 ns. The experimentally measured minimum discharge time for this operating point, which corresponds to the recommended dead time according to [68], was 150 ns. Both values were obtained assuming the nominal primary capacitance of 5.03 nF remains fixed. In contrast, when the dead time is set considering the effects of tolerance and aging, the dead time band was identified experimentally using the aged primary capacitor (Primary capacitor bank 1) with a capacitance of 4.89 nF. From this experimental evaluation, the resulting dead time band was determined as

$$247 \text{ ns} \leq t_d \leq 345 \text{ ns}. \tag{4.14}$$

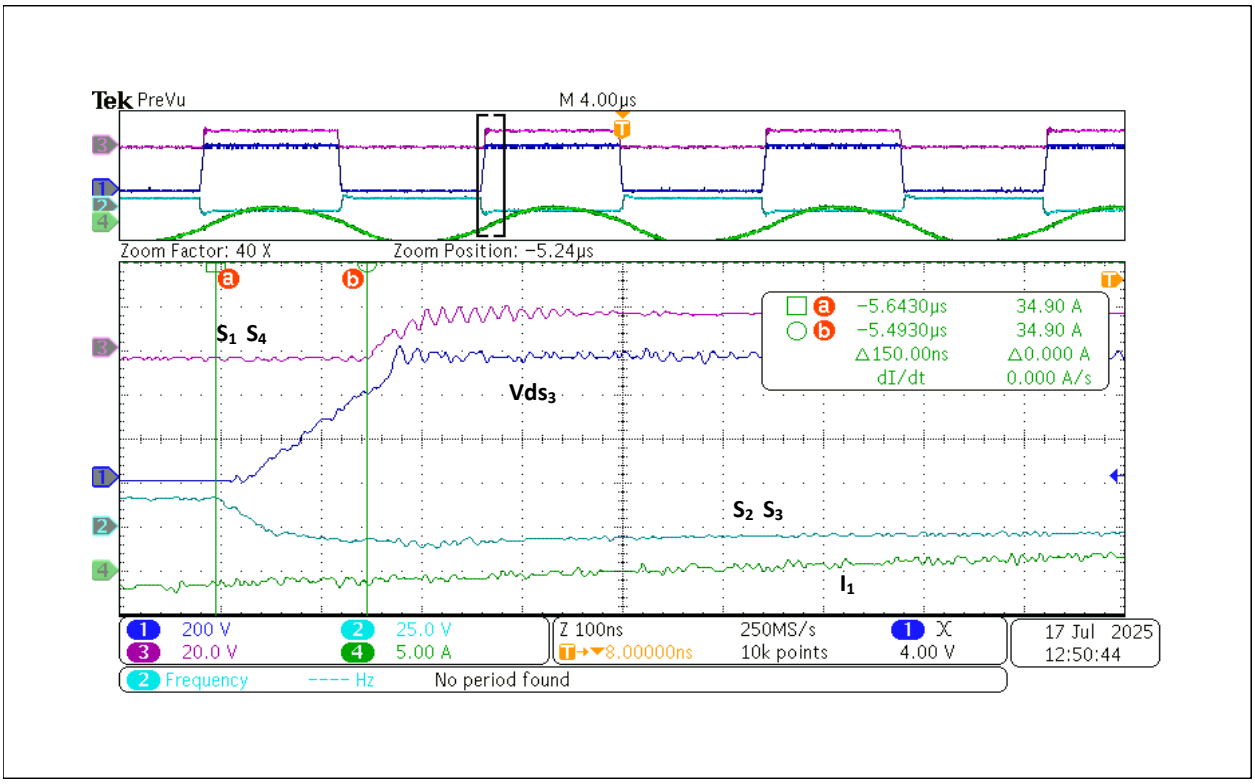

Fig. 4.11: Experimental waveforms for the aged and tolerance-affected capacitance case ($C_1 = 4.89$ nF) under a dead time of 150 ns, illustrating the impact of aging and tolerance on ZVS behavior.

Since the microcontroller resolution was insufficient to reliably distinguish between the 150 ns dead time and the 154 ns dead time —and given that these values are very close— experimental testing was performed only at 150 ns, representing both cases. The corresponding waveforms for this case are presented in Fig. 4.11, while the power analyzer output is shown in Fig. 4.12.

In Fig. 4.11, S_1 and S_4 represent the measured gate-to-source voltages of switches 1 and 4, while S_2 and S_3 correspond to the gate-to-source voltages of switches 2 and 3. V_{ds3} denotes the drain-to-source voltage across switch 3, and I_1 represents the measured primary current.

From the waveforms, it can be observed that when all switches are turned off, V_{ds3} begins

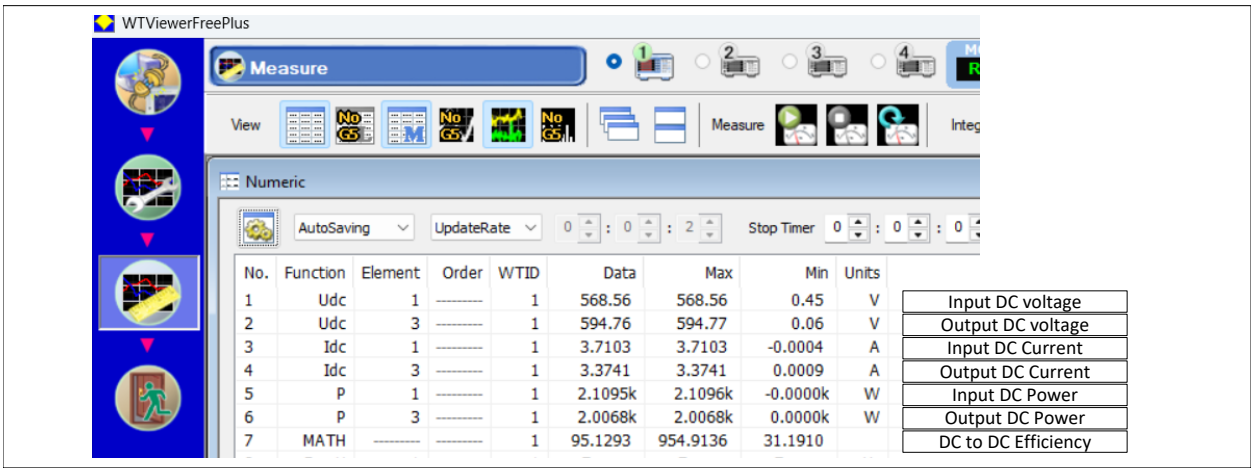

Fig. 4.12: Power analyzer measurements for the capacitance case affected by aging and tolerance ($C_1 = 4.89$ nF) with 150 ns dead time.

to rise due to the charging of its parasitic capacitance, while simultaneously the parasitic capacitances of switches 1 and 4 are being discharged. However, before V_{ds3} maximum is reached—meaning the parasitic capacitances across switches 1 and 4 are not completely discharged and the voltage across them has not yet reached zero—switches S_1 and S_4 are turned on. As a result, ZVS is not achieved, leading to switching losses that reduce the overall efficiency.

The measured DC-DC efficiency under this condition is 95.13%, as shown in Fig. 4.12. For the method considering the impact of aging and tolerance, since the viable dead time range was found as indicated in (4.14), a dead time of 308 ns was chosen for experimental verification. The corresponding waveforms for this case are presented in Fig. 4.13, while the power analyzer output is shown in Fig. 4.14.

As observed from the waveforms in Fig. 4.13, V_{ds3} reaches its maximum—indicating that the parasitic capacitances across switches 1 and 4 are fully discharged and the voltage across them has reached zero—before switches 1 and 4 are turned on. Therefore, ZVS is

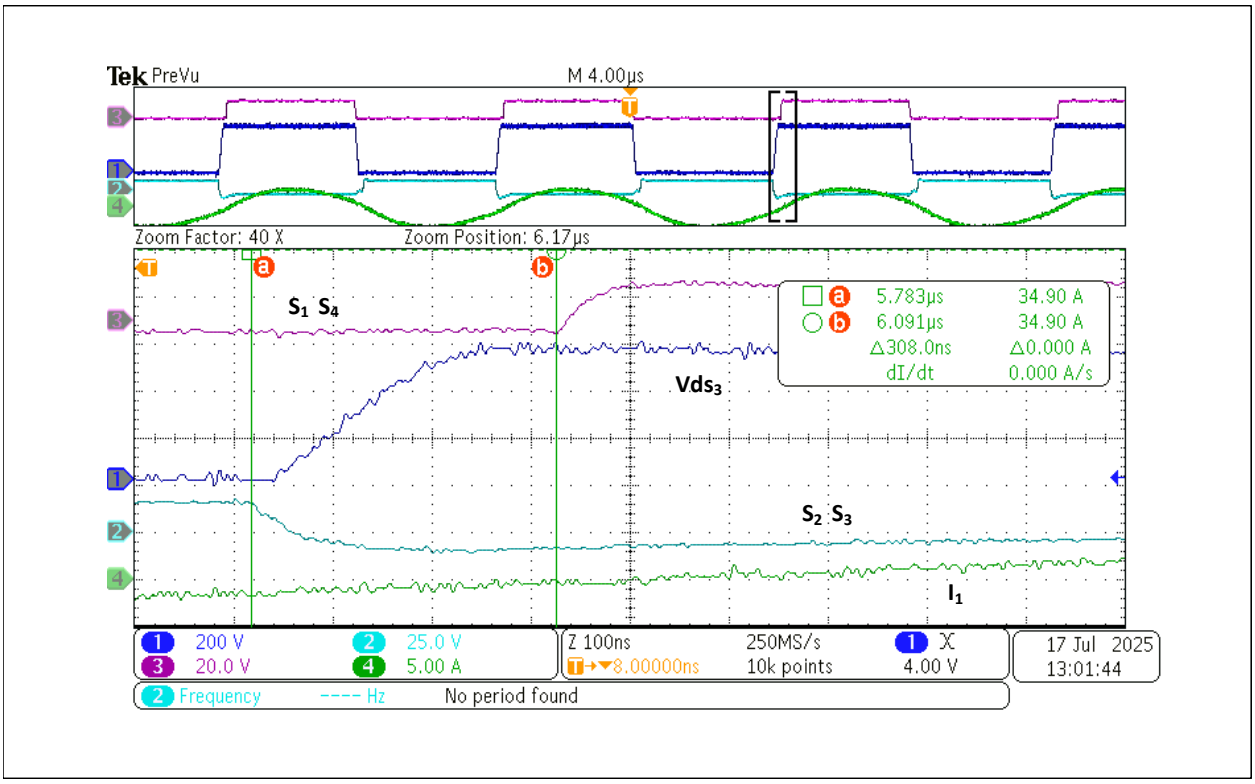

Fig. 4.13: Experimental waveforms for the method considering the impact of aging and tolerance with a dead time of 308 ns, demonstrating ZVS under the tolerance and aging affected primary capacitance condition.

maintained, resulting in lower switching losses and a higher DC–DC efficiency of 95.23% as shown in Fig. 4.14.

Table 4.2 summarizes the dead time selection methods, the corresponding estimated dead times t_d, and the measured efficiencies for the critical operating point ($R_{L\_dc} = 175\ \Omega$ and 13 cm air gap). It can be seen that the method accounting for the impact of aging and tolerance achieves the highest efficiency, emphasizing the importance of considering these effects when setting dead time.

It follows that a buffer can be incorporated in the nominal primary capacitance to account for worst-case tolerance and aging effects. Specifically, the primary capacitance can be

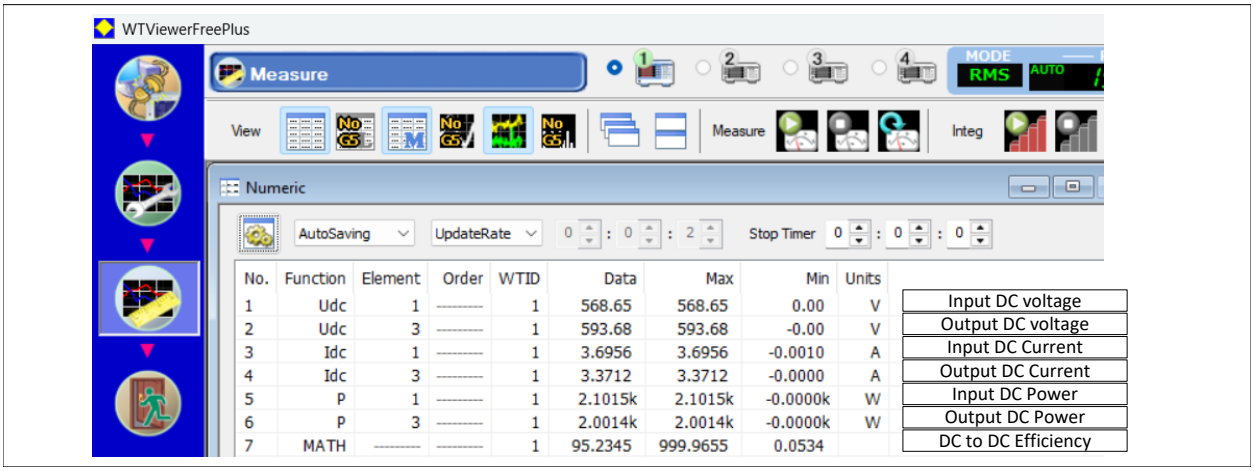

Fig. 4.14: Power analyzer measurements for the method considering the impact of aging and tolerance with 308 ns dead time.

Table 4.2: Comparison of dead time Selection Methods and Resulting Efficiencies after aging and tolerance effects, for $R_{L\_dc} = 175\ \Omega$ and 13 cm air gap

	t_d based on	t_d (ns)	Measured Efficiency
This study	Tolerance and aging reflected measured values	308	95.23%
[68]	Measured values	150	95.13%
[63]	Analytical values (energy based)	154	95.13%

selected with a slightly higher nominal value, ensuring that even after degradation due to aging and variations caused by component tolerances, ZVS operation is still reliably maintained.

4.3.2 Analysis Under Severe Capacitance Deviation (19.8%)

It is important to note that the margin introduced to account for aging and tolerance should be relatively small, similar to the previously considered case of approximately 3%. If the combined tolerance and aging margin is excessively large—such as when general-purpose ceramic or film capacitors are used, which typically exhibit considerably higher variation—it

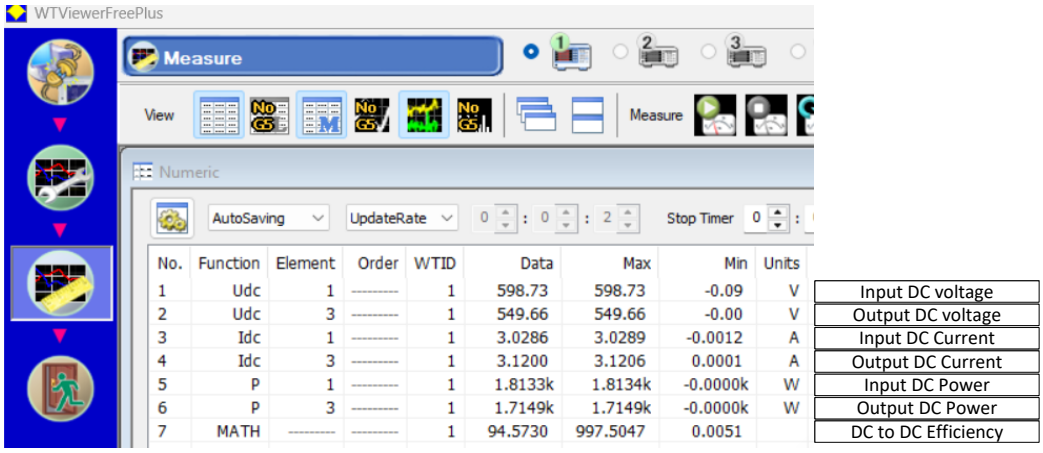

Fig. 4.15: Power analyzer measurements for the primary capacitor bank with increased nominal capacitance (5.86 nF) under nominal operating conditions, illustrating the impact on output power and DC–DC efficiency.

can adversely affect the power transfer capability and efficiency even under nominal operating conditions. To experimentally investigate this, a primary capacitor bank with 5.86 nF (capacitor bank 3) was selected, corresponding to a margin of approximately 19.8% over the expected final aged and tolerance-impacted capacitance of 4.89 nF (capacitor bank 1). This allows assessment of the impact of an intentionally oversized primary capacitance on ZVS maintenance, power transfer, and overall system efficiency.

Fig. 4.15 shows the power analyzer output for this capacitor bank under nominal operating conditions. It can be observed that at the maximum allowable DC input voltage of 600 V, the output power is limited to 1.7 kW and the DC–DC efficiency decreases to 94.57%.

These results indicate that while accounting for the effects of capacitance aging and tolerance is essential when setting dead time to prevent loss of ZVS, the use of capacitors with minimal aging and tolerance variations is equally critical to achieving maximum efficiency during WPT operation, both at the implementation stage and over the long term.

4.4 Summary

This chapter first reviewed the theoretical background of ZVS for full-bridge, SS resonant WPT systems, including the mechanism by which the parasitic MOSFET output capacitances are discharged during the dead time interval and the definitions of the discharge time t_{dis} and the available ZVS interval t_{ZVS}. The importance of maintaining ZVS to minimise switching losses and device stress was emphasised, together with the basic condition for safe dead time selection ($t_{dis} \leq t_d \leq t_{ZVS}$).

Established analytical dead time method (energy-based formulations, using a charge-equivalent capacitance derived from the device $C_{\text{oss}}(V_{ds})$ characteristic) was then evaluated experimentally across representative operating points (air gaps and load resistances). Experimental verification showed systematic deviations between analytically predicted and measured discharge times. The dominant source of discrepancy was identified as inaccuracies in the datasheet-derived charge-equivalent capacitance: the nonlinear $C_{\text{oss}}(V_{ds})$ behaviour in practice does not match the simplified equivalent used in the analytical models, leading to under- or over-estimation of t_{dis}.

The chapter also experimentally tested the recurring recommendation to minimise dead time wherever possible. A novel aspect of this study is that measurements at multiple air gaps and loads indicate that, provided the applied dead time lies inside the dead time band that guarantees ZVS, modest increases in dead time have negligible effect on DC–DC efficiency. In other words, once ZVS is preserved, operating with a somewhat longer dead time (within the valid band) does not always produce a significant efficiency penalty.

A focused experimental investigation then examined the impact of manufacturing tolerance and long-term aging on ZVS. For clarity, only degradation of the primary compensation capacitor was studied (the combined primary and secondary case would be more severe in

practice). Even a small reduction (3%) in primary capacitance due to tolerance and aging was shown to increase t_{dis}, reduce t_{ZVS}, and therefore shrink the viable dead time band. At a representative critical operating point (minimum load, minimum air gap), dead time settings derived from nominal (pre-aging/tolerance) methods failed to ensure full ZVS after aging/tolerance effects; in contrast, selecting the dead time from the experimentally determined post-aging/tolerance dead time band restored ZVS and produced a small measured improvement in DC–DC efficiency.

The trade-off between adding a capacitance margin (to ensure post aging/tolerance ZVS) and its impact on nominal performance was also examined. An intentionally oversized primary bank (representing a capacitor with large manufacturing tolerance and aging degradation) reduced the maximum deliverable power and lowered DC–DC efficiency at nominal conditions. This demonstrates that large nominal oversizing to preclude future tolerance and aging effects can be detrimental to power-transfer capability and power transfer efficiency.

From these findings, the chapter draws practical recommendations consistent with the experimental results: (i) dead time selection should explicitly account for post-aging and tolerance conditions to ensure ZVS is maintained throughout the system's lifetime; in practice, this means selecting a slightly longer dead time within the valid post-aging/tolerance band, as moderate excess dead time does not cause measurable efficiency loss; and (ii) capacitor selection should prioritise components with low tolerance and minimal aging drift, rather than relying on large nominal capacitance margins to ensure post-aging/tolerance ZVS is maintained, since excessive oversizing can reduce power-transfer capability and power transfer efficiency.

Chapter 5

Concluding Remarks

5.1 Conclusions

This thesis presented the design, experimental validation, and performance evaluation of a 2 kW WPT system, focusing on maximizing power transfer efficiency and ensuring reliable operation over the system's lifetime. The study concentrated on two key aspects: (i) coil design optimization under realistic design constraints and (ii) maintaining robust ZVS in the presence of capacitor aging and manufacturing tolerances.

A systematic methodology was developed to optimize Archimedean spiral coils for high efficiency while avoiding bifurcation. Analytical expressions from existing literature for self-inductance, mutual inductance, and AC resistance were employed to guide coil design, and the resulting coils were validated experimentally for efficiency and bifurcation-free operation. The results demonstrated that identical primary and secondary coils maximize coupling and overall system efficiency, providing a practical foundation for coil design in series-compensated WPT systems.

The 2 kW series-compensated prototype was experimentally validated, confirming the accuracy of analytical and simulation-based predictions. The system achieved a maximum DC–DC efficiency of 94.86% at a 15 cm air gap while maintaining bifurcation-free operation. This experimental platform enabled detailed assessment of coil performance, compensation design, and overall system behavior, fulfilling the objectives of validating the proposed design methodology.

The work further addressed the long-term reliability challenge of maintaining ZVS under the effects of capacitor aging and manufacturing tolerances. Experimental investigation revealed that even small deviations in primary capacitance reduce the available ZVS interval, potentially causing voltage notches and increased switching losses. To mitigate these effects, the study proposes two key strategies: (i) Selecting the dead time based on expected post-aging and component tolerance levels from manufacturer datasheets, in order to preserve ZVS throughout the system's lifetime, while allowing a slightly longer dead time within the valid band without measurable efficiency loss; and (ii) choosing capacitors with low tolerance and minimal aging drift, rather than relying on large nominal capacitance margins, to prevent reductions in power-transfer capability and efficiency.

In summary, the contributions of this thesis directly align with the research objectives and are threefold:

1. A validated methodology for optimizing Archimedean spiral coils to maximize WPT efficiency while avoiding bifurcation under realistic design constraints.

2. Experimental validation of a 2 kW series-compensated WPT platform, enabling assessment of coil performance, efficiency enhancement strategies, and overall system behavior.

3. An approach for maintaining ZVS under capacitor aging and manufacturing tolerances, including practical guidelines for dead time selection and capacitor choice to ensure long-term reliable operation.

Collectively, these outcomes provide a systematic foundation for designing high-efficiency, robust WPT systems, offering both theoretical insights and practical techniques applicable to academic research and industrial deployment.

5.2 Future Work

This thesis experimentally validated a 2 kW WPT system for EV charging, with a focus on optimizing Archimedean spiral coil design for high efficiency and bifurcation-free operation, and ensuring robust ZVS under capacitor aging and manufacturing tolerances. While the study provides significant insights into efficient and reliable WPT operation, further research can extend these findings and explore additional aspects of system performance:

- **Higher power levels:** Experimental investigation of WPT systems beyond 2 kW, exploring challenges related to higher current stress, thermal management, and efficiency scaling.
- **Misalignment tolerance:** Study the effect of lateral and angular misalignment between primary and secondary coils on power transfer efficiency, voltage stresses, and ZVS performance.
- **Dynamic load conditions:** Evaluate system performance under variable load scenarios representative of real EV battery charging profiles, including start-stop conditions and rapid load changes.

- **Impact of ferrite integration:** Investigate the effect of adding ferrite materials to the coils on optimal turn count, efficiency, and leakage inductance, and validate improvements experimentally.
- **Impact of shielding:** Examine the influence of magnetic or conductive shielding on coil performance, efficiency, and stray field reduction in practical deployment scenarios.
- **Bidirectional power transfer:** Extend the WPT system to support bidirectional energy flow, enabling vehicle-to-grid (V2G) applications, and assess efficiency and control challenges.
- **Integration with EV systems:** Evaluate real-world deployment scenarios, including vehicle-side integration, ground coil design, and coupling with battery management systems to validate system feasibility and reliability in operational conditions.

These studies can provide deeper understanding and practical guidance for designing robust, high-efficiency WPT systems suitable for commercial EV charging applications.

References

[1] T. M. Fisher, K. B. Farley, Y. Gao, H. Bai, and Z. T. H. Tse, "Electric vehicle wireless charging technology: a state-of-the-art review of magnetic coupling systems," *Wireless Power Transfer*, vol. 1, no. 2, pp. 87–96, 2014. [Online]. Available: https://doi.org/10.1017/wpt.2014.8

[2] H. H. Wu, A. Gilchrist, K. Sealy, P. Israelsen, and J. Muhs, "A review on inductive charging for electric vehicles," in *2011 IEEE International Electric Machines Drives Conference (IEMDC)*, 2011, pp. 143–147.

[3] A. Khaligh and S. Dusmez, "Comprehensive topological analysis of conductive and inductive charging solutions for plug-in electric vehicles," *IEEE Transactions on Vehicular Technology*, vol. 61, no. 8, pp. 3475–3489, 2012.

[4] S. Li and C. C. Mi, "Wireless power transfer for electric vehicle applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 1, pp. 4–17, 2015.

[5] K. Agarwal, R. Jegadeesan, Y.-X. Guo, and N. V. Thakor, "Wireless power transfer strategies for implantable bioelectronics," *IEEE Reviews in Biomedical Engineering*, vol. 10, pp. 136–161, 2017.

[6] M. G. L. Roes, J. L. Duarte, M. A. M. Hendrix, and E. A. Lomonova, "Acoustic energy transfer: A review," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 1, pp. 242–248, 2013.

[7] Z. Zeng, S. Fu, H. Zhang, Y. Dong, and J. Cheng, "A survey of underwater optical wireless communications," *IEEE Communications Surveys Tutorials*, vol. 19, no. 1, pp. 204–238, 2017.

[8] J. Dai and D. C. Ludois, "A survey of wireless power transfer and a critical comparison of inductive and capacitive coupling for small gap applications," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6017–6029, 2015.

[9] G. A. Covic and J. T. Boys, "Modern trends in inductive power transfer for transportation applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 1, pp. 28–41, 2013.

[10] K. Jin and W. Zhou, "Wireless laser power transmission: A review of recent progress," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3842–3859, 2019.

[11] K. Huang and X. Zhou, "Cutting the last wires for mobile communications by microwave power transfer," *IEEE Communications Magazine*, vol. 53, no. 6, pp. 86–93, 2015.

[12] Z. Zhang, H. Pang, A. Georgiadis, and C. Cecati, "Wireless power transfer—an overview," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 2, pp. 1044–1058, 2019.

[13] N. Tesla, "High frequency oscillators for electro-therapeutic and other purposes," *Proceedings of the IEEE*, vol. 87, no. 7, pp. 1282–, 1999.

[14] S. C. Technology, "Roadway powered electric vehicle project parametric studies: Phase 3d final report," Institute of Transportation Studies, UC Berkeley, Institute of Transportation Studies, Research Reports, Working Papers, Proceedings qt0gr200hv, Jan 1996. [Online]. Available: https://ideas.repec.org/p/cdl/itsrrp/qt0gr200hv.html

[15] G. Covic, G. Elliott, O. Stielau, R. Green, and J. Boys, "The design of a contact-less energy transfer system for a people mover system," in *PowerCon 2000. 2000 International Conference on Power System Technology. Proceedings (Cat. No.00EX409)*, vol. 1, 2000, pp. 79–84 vol.1.

[16] A. Green and J. Boys, "10 khz inductively coupled power transfer-concept and control," in *1994 Fifth International Conference on Power Electronics and Variable-Speed Drives*, 1994, pp. 694–699.

[17] G. Elliott, G. Covic, D. Kacprzak, and J. Boys, "A new concept: Asymmetrical pickups for inductively coupled power transfer monorail systems," *IEEE Transactions on Magnetics*, vol. 42, no. 10, pp. 3389–3391, 2006.

[18] M. Budhia, J. T. Boys, G. A. Covic, and C.-Y. Huang, "Development of a single-sided flux magnetic coupler for electric vehicle ipt charging systems," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 1, pp. 318–328, 2013.

[19] A. Mahesh, B. Chokkalingam, and L. Mihet-Popa, "Inductive wireless power transfer charging for electric vehicles–a review," *IEEE Access*, vol. 9, pp. 137 667–137 713, 2021.

[20] S. Li, W. Li, J. Deng, T. D. Nguyen, and C. C. Mi, "A double-sided lcc compensation network and its tuning method for wireless power transfer," *IEEE Transactions on Vehicular Technology*, vol. 64, no. 6, pp. 2261–2273, 2015.

[21] W. Zhang and C. C. Mi, "Compensation topologies of high-power wireless power transfer systems," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 6, pp. 4768–4778, 2016.

[22] C.-S. Wang, O. Stielau, and G. Covic, "Design considerations for a contactless electric vehicle battery charger," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 5, pp. 1308–1314, 2005.

[23] W. Zhang, S.-C. Wong, C. K. Tse, and Q. Chen, "Design for efficiency optimization and voltage controllability of series–series compensated inductive power transfer systems," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 191–200, 2014.

[24] Y. H. Sohn, B. H. Choi, E. S. Lee, G. C. Lim, G.-H. Cho, and C. T. Rim, "General unified analyses of two-capacitor inductive power transfer systems: Equivalence of current-source ss and sp compensations," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6030–6045, 2015.

[25] F. Lu, H. Zhang, H. Hofmann, and C. C. Mi, "An inductive and capacitive combined wireless power transfer system with lc-compensated topology," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8471–8482, 2016.

[26] W. Zhang, S.-C. Wong, C. K. Tse, and Q. Chen, "Load-independent duality of current and voltage outputs of a series- or parallel-compensated inductive power transfer converter with optimized efficiency," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 1, pp. 137–146, 2015.

[27] B. Esteban, M. Sid-Ahmed, and N. C. Kar, "A comparative study of power supply architectures in wireless ev charging systems," *IEEE Transactions on Power Electronics*, vol. 30, no. 11, pp. 6408–6422, 2015.

[28] S. International, "Wireless power transfer for light-duty plug-in/electric vehicles and alignment methodology," https://doi.org/10.4271/J2954_202408, Aug. 2024, accessed: 2025-05-01. [Online]. Available: https://doi.org/10.4271/J2954_202408

[29] ——, "Wireless power transfer for heavy-duty electric vehicles," https://doi.org/10.4271/J2954/2_202212, Dec. 2022, accessed: 2025-05-01. [Online]. Available: https://doi.org/10.4271/J2954/2_202212

[30] A. P. Sample, D. T. Meyer, and J. R. Smith, "Analysis, experimental results, and range adaptation of magnetically coupled resonators for wireless power transfer," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 2, pp. 544–554, 2011.

[31] Y. Wang, W. Liu, and Y. Xie, "Design and optimization for circular planar spiral coils in wireless power transfer system," in *2019 22nd International Conference on Electrical Machines and Systems (ICEMS)*, 2019, pp. 1–4.

[32] J. Kim, J. Kim, S. Kong, H. Kim, I.-S. Suh, N. P. Suh, D.-H. Cho, J. Kim, and S. Ahn, "Coil design and shielding methods for a magnetic resonant wireless power transfer system," *Proceedings of the IEEE*, vol. 101, no. 6, pp. 1332–1342, 2013.

[33] J. Sampath, A. Alphones, and H. Shimasaki, "Coil design guidelines for high efficiency of wireless power transfer (wpt)," in *2016 IEEE Region 10 Conference (TENCON)*, 2016, pp. 726–729.

[34] G. Wei, X. Jin, C. Wang, J. Feng, C. Zhu, and M. I. Matveevich, "An automatic coil design method with modified ac resistance evaluation for achieving maximum coil–coil efficiency in wpt systems," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6114–6126, 2020.

[35] K. Aditya and S. S. Williamson, "Design guidelines to avoid bifurcation in a series–series compensated inductive power transfer system," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 3973–3982, 2019.

[36] Y. Jiang, L. Wang, Y. Wang, J. Liu, X. Li, and G. Ning, "Analysis, design, and implementation of accurate zvs angle control for ev battery charging in wireless high-power transfer," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 5, pp. 4075–4085, 2019.

[37] J. Shin, S. Shin, Y. Kim, S. Lee, B. Song, and G. Jung, "Optimal current control of a wireless power transfer system for high power efficiency," in *2012 Electrical Systems for Aircraft, Railway and Ship Propulsion*, 2012, pp. 1–4.

[38] C.-G. Kim, D.-H. Seo, J.-S. You, J.-H. Park, and B. Cho, "Design of a contactless battery charger for cellular phone," *IEEE Transactions on Industrial Electronics*, vol. 48, no. 6, pp. 1238–1247, 2001.

[39] T. Nishimura, K. Hirachi, Y. Maejima, K. Kuwana, and M. Saito, "Characteristics of a novel energy transmission for a rechargeable cardiac pacemaker by using a resonant dc-dc converter," in *Proceedings of IECON '93 - 19th Annual Conference of IEEE Industrial Electronics*, 1993, pp. 875–880 vol.2.

[40] D. Pedder, A. Brown, and J. Skinner, "A contactless electrical energy transmission system," *IEEE Transactions on Industrial Electronics*, vol. 46, no. 1, pp. 23–30, 1999.

[41] M. Budhia, G. Covic, and J. Boys, "A new ipt magnetic coupler for electric vehicle charging systems," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2487–2492.

[42] A. Zaheer, H. Hao, G. A. Covic, and D. Kacprzak, "Investigation of multiple decoupled coil primary pad topologies in lumped ipt systems for interoperable electric vehicle charging," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1937–1955, 2015.

[43] G. A. Covic, M. L. G. Kissin, D. Kacprzak, N. Clausen, and H. Hao, "A bipolar primary pad topology for ev stationary charging and highway power by inductive coupling," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 1832–1838.

[44] T.-D. Nguyen, S. Li, W. Li, and C. C. Mi, "Feasibility study on bipolar pads for efficient wireless power chargers," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 1676–1682.

[45] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*, 3rd ed. Hoboken, NJ: John Wiley & Sons, 2003.

[46] R. Steigerwald, "A comparison of half-bridge resonant converter topologies," *IEEE Transactions on Power Electronics*, vol. 3, no. 2, pp. 174–182, 1988.

[47] C.-S. Wang, G. Covic, and O. Stielau, "Power transfer capability and bifurcation phenomena of loosely coupled inductive power transfer systems," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 1, pp. 148–157, 2004.

[48] D. C. Galbraith, M. Soma, and R. L. White, "A wide-band efficient inductive transdennal power and data link with coupling insensitive gain," *IEEE Transactions on Biomedical Engineering*, vol. BME-34, no. 4, pp. 265–275, 1987.

[49] I. Tesla, "Model 3 owner's manual," https://www.tesla.com/ownersmanual/model3/en_us/GUID-56562137-FC31-4110-A13C-9A9FC6657BF0.html, 2023, accessed: 2025-08-11.

[50] B. Auto, "Byd atto 3 specifications," https://www.byd.com/content/dam/byd-site/en-th/product/atto3/atto3-th.pdf, 2023, accessed: 2025-08-11.

[51] U. D. of Transportation, "Charger types and speeds – ev basics," https://www.transportation.gov/rural/ev/toolkit/ev-basics/charging-speeds, 2025, accessed: 2025-09-18.

[52] J. M. Miller, C. P. White, O. C. Onar, and P. M. Ryan, "Grid side regulation of wireless power charging of plug-in electric vehicles," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 261–268.

[53] A. Kunwar, "Design and implementation of an inductive power transfer system for wireless charging of future electric transportation," PhD Thesis, Ontario Tech University, 2016, accessed: 2025-10-01. [Online]. Available: https://ontariotechu.scholaris.ca/items/3e528c04-af10-4846-9588-8b7dfcc24bf0

[54] J. Sallan, J. L. Villa, A. Llombart, and J. F. Sanz, "Optimal design of icpt systems applied to electric vehicle battery charge," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 6, pp. 2140–2149, 2009.

[55] U. Pratik, B. J. Varghese, A. Azad, and Z. Pantic, "Optimum design of decoupled concentric coils for operation in double-receiver wireless power transfer systems," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1982–1998, 2019.

[56] C. Sullivan, "Optimal choice for number of strands in a litz-wire transformer winding," *IEEE Transactions on Power Electronics*, vol. 14, no. 2, pp. 283–291, 1999.

[57] A. Riedel, R. Hahn, A. Kuehl, and J. Franke, "Evaluation of different methods for removing the conductor insulation of stranded conductors," in *2021 12th International Symposium on Advanced Topics in Electrical Engineering (ATEE)*, 2021, pp. 1–7.

[58] D. J. Perreault, J. Hu, J. M. Rivas, Y. Han, O. Leitermann, R. C. Pilawa-Podgurski, A. Sagneri, and C. R. Sullivan, "Opportunities and challenges in very high frequency power conversion," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 1–14.

[59] E. Yang, F. Lee, and M. Jovanovic, "Small-signal modeling of series and parallel resonant converters," in *[Proceedings] APEC '92 Seventh Annual Applied Power Electronics Conference and Exposition*, 1992, pp. 785–792.

[60] W. Li, H. Zhao, J. Deng, S. Li, and C. C. Mi, "Comparison study on ss and double-sided lcc compensation topologies for ev/phev wireless chargers," *IEEE Transactions on Vehicular Technology*, vol. 65, no. 6, pp. 4429–4439, 2016.

[61] B. Zhao, Q. Song, W. Liu, and Y. Sun, "Dead-time effect of the high-frequency isolated bidirectional full-bridge dc–dc converter: Comprehensive theoretical analysis and experimental verification," *IEEE Transactions on Power Electronics*, vol. 29, no. 4, pp. 1667–1680, 2014.

[62] U. D. Kavimandan, V. P. Galigekere, B. Ozpineci, and O. Onar, "Analysis of deadtime in a single phase wireless power transfer system," in *2019 IEEE Transportation Electrification Conference and Expo (ITEC)*, 2019, pp. 1–8.

[63] C.-T. Truong and S.-J. Choi, "Improved zvs criterion for series resonant converters," *IEEE Access*, vol. 12, pp. 5333–5344, 2024.

[64] L. Barragan, J. Burdio, J. Artigas, D. Navarro, J. Acero, and D. Puyal, "Efficiency optimization in zvs series resonant inverters with asymmetrical voltage-cancellation control," *IEEE Transactions on Power Electronics*, vol. 20, no. 5, pp. 1036–1044, 2005.

[65] I. Zeltser and S. Ben-Yaakov, "On spice simulation of voltage-dependent capacitors," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 3703–3710, 2018.

[66] D. Costinett, D. Maksimovic, and R. Zane, "Circuit-oriented treatment of nonlinear capacitances in switched-mode power supplies," *IEEE Transactions on Power Electronics*, vol. 30, no. 2, pp. 985–995, 2015.

[67] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "Zvs of power mosfets revisited," *IEEE Transactions on Power Electronics*, vol. 31, no. 12, pp. 8063–8067, 2016.

[68] F. Xu, J. Liu, and X. Zhang, "Analysis of deadtime effects and optimum deadtime control for bidirectional inductive power transfer converters," *IEEE Transactions on Industrial Electronics*, vol. 71, no. 7, pp. 6929–6937, 2024.

[69] K. E. Corporation, "Ckc33c103gjgac7210 datasheet," https://www.digikey.ee/en/products/detail/kemet/CKC33C103GJGAC7210/11692593, accessed: 2025-10-20.

[70] T. Corporation, "High voltage mlccs with c0g characteristics and replacement solutions – application to wireless power transfer," https://product.tdk.com/en/techlibrary/solutionguide/mlcc04.html, TDK Tech Library, Tech. Rep., 2017.