# Adaptive Control Using Pulse-Frequency Modulation and Phase-Locked Loops

bу

Lawrence E. Draho

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presented to the University of Manitoba
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# ADAPTIVE CONTROL USING PULSE-FREQUENCY MODULATION AND PHASE-LOCKED LOOPS

BY

#### LAWRENCE E. DRAHO

A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

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#### ABSTRACT

This thesis describes the realization and testing of an all digital adaptive controller that uses the concepts of integral pulse frequency modulation and phase-lock loops to regulate first and second order plants. The plants, which respond the 'best' at high gains, operate at a point very near their critical gain. The adaptiveness of the controller maintains the system near its critical point even for sudden plant changes.

The proposed design also incorporates a scheme to provide a 'well-behaved' transient response by operating the system from the outset in the open-loop mode for a short time. This scheme is based on the observation that the feedback in the system causes a poor plant response during the start-up transition period.

Examples are submitted displaying how the plant responds to the transient improvement scheme and the adaptiveness of the digital controller. These examples are used to judge the performance of the proposed design.

#### ACKNOWLEDGEMENTS

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#### Chapter I

#### INTRODUCTION

#### 1.1 BACKGROUND

Phase-lock loops (PLL) are most commonly found in the communications area. They are used in receivers for various applications [2,3].

Recently, PLL have been used in control applications [4,5] where the plant to be controlled replaces the voltage controlled oscillator in the communications applications. The plant's response to a PLL controller shows a marked improvement over the responses to other types of controllers.

Another technique used in control systems is pulse frequency modulation (PFM) [6,7,9,10,11,12,13]. For PFM, the signal is a series of identical pulses, with the spacings between the pulses (or pulse frequency) containing the information [6]. The non-idealness of the pulses, and problems with noise corruption, caused researchers to look for an improved modulating technique.

One technique proposed is integral pulse frequency modulation (IPFM) where the pulse frequency is now dependent on the integral of the particular signal and a pre-determined integral threshold value. IPFM has the advantages of better noise immunity [7] and ease of analysis [8].

C.S.W. Woo [1] combined the concepts of PLL and IPFM to create a controller that utilizes the advantages of both methods. He found that this system has a locking range with respect to the gain of the system, i.e., there is a minimum  $gain(\neq 0)$  and a maximum gain for which the system would be in phase-lock. For any value of gain above this range, the system would not be in lock and it would exhibit an unstable oscillatory behavior. If the gain was below this range, the system would just not lock.

# 1.2 RECENT DEVELOPMENTS

With the advent of medium- and large-scale integration circuitry, more devices are being designed using digital instead of analog components [5,9,10]. This change in designs is due mainly to the low cost, decreased size, and better reliability of the digital circuits [14]. The digital designs are either hardware or a combination of hardware and software; the latter, in general, considered to be the better of the two.

For the hardware/software combination it is generally accepted that the best combination is to implement specific software packages in general purpose hardware [15]. Designing systems this way gives the designer more flexibility in accommodating the device to a given situation. Usually it is easier to rewrite and test software than it is to redesign and check hardware. Professor H. A. Barker stated that,

"...in future, software will be the key to electronic system design..." [15].

The relative ease in changing software, and the ability of micro-processor systems to react to situations in a programmed way have aided engineers in the area of adaptive control. Invariably, a controlled plant will change its characteristics over time. These changes could be due either to physical variations of the plant, or a change in the plant's environment. A fixed controller may not be able to handle these changes satisfactorily [16]. A variable controller, one that uses a micro-processor system, for example, would be able to adapt to these changes so that the plant operates at a satisfactory level.

# 1.3 STATEMENT OF PROBLEM

The PLL-IPFM controller investigated by Woo [1] is the bases of this thesis. Fig. 1.1 is a block diagram of the regulator control system using this analog regulator controller. Because pulses are a major component of the design, this kind of controller lends itself readily to a digital implementation. This kind of approach is very appealing because of the advantages digital circuitry has over analog circuits.

For this thesis, a digital controller composed of the two modulators, the phase comparator, and the gain adjustment will be realized using a Z-80 micro-processor system.

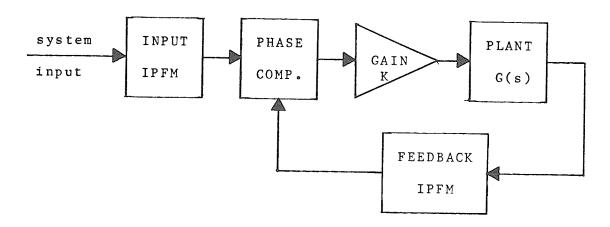


Figure 1.1: Control system investigated by Woo

The results of the digital design are compared with the analog design, then improvements are made in the digital controller.

The major improvement in the digital controller is to make it adaptive. Results will be presented to show that, when the system is in phase-lock, the best plant response occurs when the gain is as high as possible. An adaptive controller is designed to vary the gain in such a way that, regardless of the circumstances, the system gain will always be as high as possible, even when the plant changes.

Improvements are also made in the transient response of the plant. It will be shown that the digital implementation of the analog PLL-IPFM controller gives a poor transient response. A solution is proposed where the system is operated in the open-loop mode for a short time. This results in a much better transient response.

# 1.4 OUTLINE OF ANALYSIS

The relevant background on phase-lock loops and integral pulse frequency modulation, and the recent development and uses of digital components in control applications have been outlined in Chapter I. This information points to the possible advantages of a digitally implemented PLL-IPFM controller.

Chapter II briefly describes the analog controller investigated by Woo. Important results are also included.

Chapter III deals with the actual digital realization of the controller. The problems with and improvements made to the controller are also discussed.

Results of tests performed on the controller are covered in Chapter IV. The controller's improvements are examined as different programs are added to the initial design.

Finally, in Chapter V, the conclusions and recommendations are presented.

# Chapter II

#### EXISTING PLL-IPFM DESIGN

#### 2.1 GENERAL

The only PLL-IPFM controller known to this author is the unity feedback analog design described by Woo [1]. A block diagram of this design is shown in Fig. 2.1.

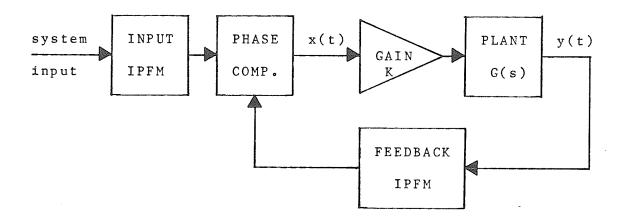


Figure 2.1: Existing analog PLL-IPFM control system

In this figure, the Integral Pulse Frequence Modulators, which are identical in design, convert their respective analog input signals into a series of pulses. The information contained in the modulated analog signals is now carried in the spacing between the pulses.

The IPFM is designed to continuously integrate its analog input signal. When the value of this integral reaches a pre-determined threshold value, a pulse is emitted and the value of the integrator is reset to zero. The process then repeats itself thus creating a series of pulses.

Notice, that because the threshold value is constant, the spacing between the pulses is dependent only on the size of the IPFM input signal. For large input signals, the value of the integral reaches the threshold value in a shorter time and the pulse spacing is smaller. Conversly, for small input signals, the amount of time it takes the integral to reach the threshold is large which makes the spacing between the pulses large.

For convenience, a one volt step function is used as the system input and the integrators' threshold value is chosen to be one volt-second. Therefore, the series of pulses coming from the input IPFM are spaced one second apart.

Looking at Fig. 2.1, the pulse sequences emitted by the feedback and input IPFMs are the phase comparator's inputs. One of the comparator's functions is to detect the initiation of these pulses. By using these pulses, the comparator is then able to produce the plant excitation signal.

This plant excitation signal is the resultant of an integrator within the comparator. Whenever the phase comparator detects an input pulse, this integrator resets its out-

put to zero and starts generating a unit ramp signal. When a feedback pulse is detected, the integrator is interrupted and it maintains a constant output at a level which is the highest integrated value attained just prior to the detection of the feedback pulse. The next detection of an input pulse resets the integrator to zero and the cycle repeats.

The time(phase) difference between the input pulse and the feedback pulse which immediately follows is referred to as the inter-pulse interval(IPI). In steady state, if the IPI is constant then the system is deemed to be in phase-lock.

The ramp portion of the phase comparator output depends on the phase difference between the detection of the input pulse and the feedback pulse which immediately follows. If there is a feedback pulse between successive input pulses, the comparator output is a trapezoidal type of signal. When the system is in phase-lock, the output of the comparator is a periodic series of identical trapezoids (see Fig. 2.2).

If there is no feedback pulse between two successive input pulses, the output of the phase comparator is a sawtooth wave. This absence of the feedback pulse is most common in the transient response of the system. Typically, unless the gain is very large, the control signal is of the form shown in Fig. 2.3. The sawtooth in the first interval is due to the fact that for this interval, the output of the plant is still small. This causes the feedback IPFM to take

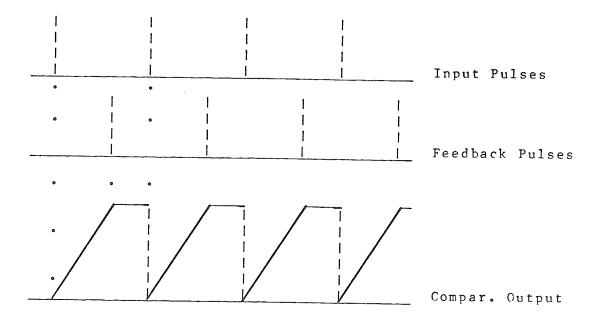


Figure 2.2: Phase comparator steady state output

more than one interval to reach its threshold value. When this threshold value is attained, the resultant feedback pulse causes the creation of the small trapezoid seen in the second interval of Fig. 2.3. As will be shown in Chapter 4, the "sawtooth followed by a small trapezoid followed by a large trapezoid ..." signal emitted by the phase comparator has a detrimental effect on the plant response.

A similar effect occurs when the system gain is very small. In this case though, the phase comparator output in steady state is a combination of sawtooth and trapezoidal waveforms.

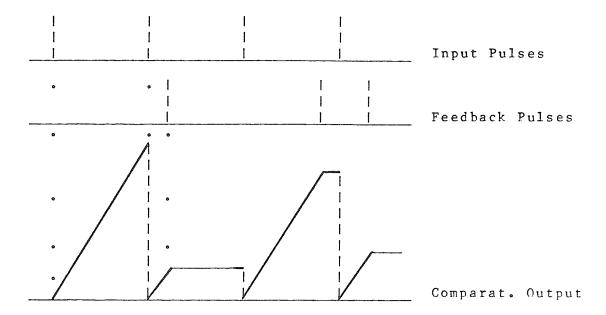


Figure 2.3: Typical transient control signal

#### 2.2 ANALOG DESIGN ANALYSIS

#### 2.2.1 Control Signal Characteristics

Examining Fig. 2.1, the trapezoidal signal that is emitted by the phase comparator is gain adjusted before it goes to the plant. Therefore each trapezoid in the plant excitation signal is characterized by the gain value, K, the inter-pulse interval, T, and the interval between two successive input pulses,  $T_0$  as shown in Fig. 2.4. For this thesis,  $T_0$  is a constant one second interval, but the gain and IPI are variable.

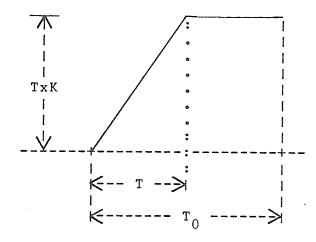


Figure 2.4: Control signal characteristics

# 2.2.2 <u>Locking</u> Relationship

Intuitively, as the gain increases, the plant output also increases in magnitude. This means that the time between successive feedback pulses decreases. If the increase in gain does not force the system out-of-lock, then obvious-ly the IPI also decreases. In other words, for a system in phase-lock at least, the gain and IPI values are inversely related.

Alternatively, for a system in phase-lock if the gain is decreased, the plant output also decreases, and so the time between successive feedback pulses increases. Eventually the gain is so small that the IPI value is greater than  $T_0$  and the system is out-of-lock. Therefore, there is a minimum gain  $(\neq 0)$  and a corresponding maximum IPI value for the system to be in phase-lock.

In order to analyze the locking relationship between gain and IPI, an expression for the plant output is needed. If one describes the linear plant by the following  $n^{\frac{th}{}}$  order linear differential equation,

where  $t_p$  is the time the first input pulse is initiated and the  $f_i$ 's are constant, an expression for the plant output can be formulated. If the system is stable and in phase-lock then the output of the linear plant is continuous and periodic. Therefore the mathematical description of this output is required for only one period. For a period beginning at time  $t_r$  then, without going into the derivation (see [1]), the output of the linear plant is completely described by:

$$y(t-t_{r}) = \underline{H} | e^{\underline{A}(t-t_{r})} \underline{Y} - (t-t_{r})\underline{A}^{-1}\underline{Q} | u(t-t_{r})$$

$$+ \underline{H} | \underline{A}^{-2}e^{\underline{A}(t-t_{r})} \underline{Q} - \underline{A}^{-2}\underline{Q} | u(t-t_{r})$$

$$+ \underline{H} | \underline{A}^{-1}(t-t_{r}-T)\underline{Q} | u(t-t_{r}-T)$$

$$- \underline{H} | \underline{A}^{-2}e^{\underline{A}(t-t_{r}-T)} \underline{Q} - \underline{A}^{-2}\underline{Q} | u(t-t_{r}-T)$$
....(2.2)

where  $\underline{H} = [1 \ 0 \ 0 \ \dots \ 0]$ 

$$\underline{Q} = \begin{bmatrix} 0 \\ 0 \\ \cdot \\ \cdot \\ K \end{bmatrix} = \begin{array}{c} \text{gain} \\ \text{vector} \\ \vdots \\ 0 \end{array}$$
 
$$\underline{Y} = \begin{bmatrix} y \\ 0 \\ \cdot \\ \cdot \\ 0 \end{bmatrix} = \begin{array}{c} \text{initial} \\ \text{conditions} \\ \text{vector} \\ \vdots \\ 0 \end{array}$$

where  $-a_i$  is a pole location, and

$$y_0 = -\frac{THA}{-1} \frac{Q}{Q} + \frac{HA}{-1} \frac{Q}{Q} + \frac{HA}{-1} \frac{Q}{Q} + \frac{A^TQ}{-1} \frac{Q}{Q} + \frac{A^TQ}{-1} \frac{Q}{Q} + \frac{A^TQ}{Q} + \frac{A^TQ}{-1} \frac{Q}{Q} + \frac{A^T$$

In Fig. 2.5, the feedback IPFM integrates the plant output, y(t), from t to t +T 0. At this time a pulse is emitted because the value of the feedback integral equals the threshold value, E, i.e.,

$$E = \begin{cases} t_s + T_0 \\ y(t) dt \end{cases}$$

$$t_s$$

Also, the gain, K, is an explicit parameter of y(t), therefore equation (2.4) can be rewritten as:

where

$$G(T) = \begin{cases} t_r^{+T} 0^{+T} \\ y(t) dt \\ t_r^{+T} \end{cases}$$

Hence, equation (2.5) relates the gain to the IPI for a given threshold value E. It can be shown (see [1]) that for a first order linear plant with a pole at -a (a>0), equation (2.5) becomes:

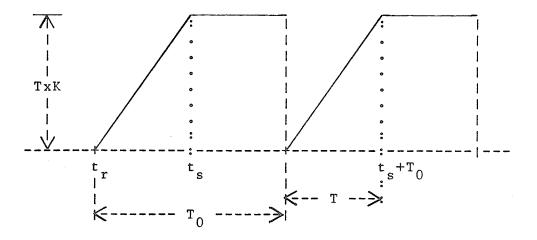


Figure 2.5: Plant excitation signal

# 2.2.3 Stability Relationship

If this control system is phase-locked and the gain is increased, it is observed that the feedback pulse positions oscillate around the "theoretical value" at a critical value of gain. As the gain is increased further, the system comes out-of-lock and the steady state response is observed to be unstable. Therefore, the value of gain used in the system must be less than this critical gain, K<sub>c</sub>, for the system to be stable.

The feedback pulse positions oscillating at the critical gain affect the IPI value. Therefore, there is a critical IPI value,  $T_{\rm c}$ , corresponding to the critical gain.

For a first order system, the stability relationship between gain and IPI, without going into the derivation is (see [1]):

$$K = a(1 + e^{-aT_0})$$

$$\frac{---aT}{(e^{-aT_0} - e^{-aT_0})}$$
.....(2.7)

where -a is the pole location.

# 2.2.4 Control System Example

Equations (2.6) and (2.7) are the expressions for the locking and stability relationships between gain and IPI for a first order system. The curves shown in Fig. 2.6 are graphical representations of these expressions for a general first order plant. The locking curve illustrates the lock-

ing relationship, i.e., the inter-pulse interval (IPI) corresponding to a given gain for the system to be in phaselock. The stability relationship, i.e., the maximum value
of gain and corresponding IPI for the system to remain stable, is shown by the stability curve.

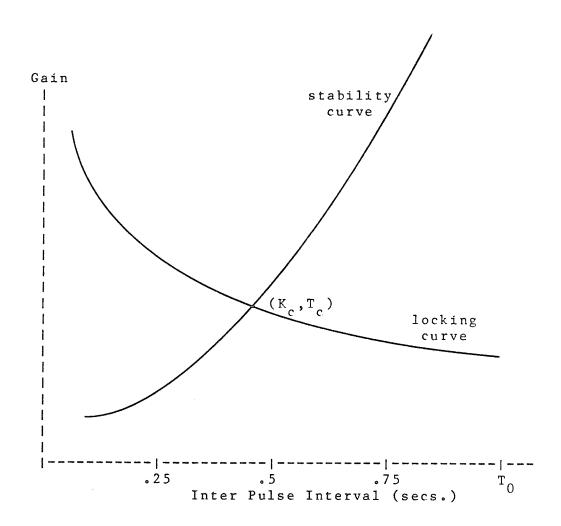


Figure 2.6: Typical relationship between gain, K and interpulse interval, T ( $T_0$ =1 sec.)

The critical values of gain and IPI are found at the point where the two curves intersect, i.e.,  $(K_c^{},T_c^{})$ . For

The minimum value of gain and the corresponding maximum value of IPI occurs when  $T=T_0$ . From Fig. 2.6 then, there is a range over which the system will be in phase-lock, i.e., the gain must be in the range,

$$K_c > K > K(T_0)$$

and the corresponding value of IPI must be in the range,

$$T_c < T \leq T_0$$

where the values of K and T are related by equation (2.6) (i.e. curve 1).

As an example, consider the first order linear plant with a pole at -5. The stability and locking relationships result in the theoretical range on the gain :

Simulating the system on a computer for comparison purposes results in the following table. This example shows that the predicted results agree with those from simulations.

Using this analog design investigated by Woo as the bases, the realization and testing of a digital PLL-IPFM controller has been accomplished and is presented in the following chapters.

TABLE 2.1

	T (calculated)	
2.5	- 0.9 0.7 0.5 0.3 0.2	No   No   No   No   No   No   No   No

#### Chapter III

#### REALIZATION

There are three components for the digital realization: the digital controller, the analog plant, and an interface between the two. The controller (the IPFMs, the phase comparator, and the gain adjustments) is realized with a Z80 micro-processor system. The plant is simulated on an analog computer (TR-20).

# 3.1 THE DIGITAL CONTROLLER

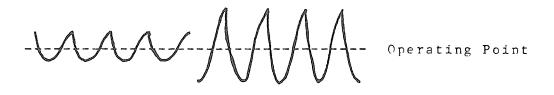
The controller is composed of three parts; the main program, initialization, and an interrupt routine. The adaptive nature of the controller and the closing of the feedback loop are handled by the main program. For the most part, the PLL-IPFM implementation is in the interrupt routine. The initialization program starts the system in the open-loop mode. Appendices P and C contain the flowchart and actual program listing, respectively.

#### 3.1.1 Main Program

The main program is composed of two parts: the adaptability routine, and the feedback-loop closing routine. The controller becomes adaptive after the feedback loop is closed.

As will be shown in the next chapter, the larger the gain is (at least up to the critical value), the smaller the ripple, and subsequently the better the performance. Ripple is defined here as the size of the oscillations about the operating point. Fig. 3.1 shows an exaggerated example of this.

ripple



high gain low gain

Figure 3.1: Effects of gain on the ripple

Having the gain as high as possible then, will be the criterion for chosing the gain. Using this criterion in the adaptation routine, the controller inspects the plant output every tenth period and determines if the system is stable. If it is stable, the gain is increased.

The system is also checked for stability every fifth .

period. If the system is found to be unstable during these checks, the gain is decreased. In this way, the plant has

had time to adjust to the new gain value if it had just been changed and produce a stable output. If the plant cannot adjust to the gain because the gain is too large, the five period check will hopefully be a short enough time so that the plant oscillations don't become too great.

The other part of the main program is the feedback-loop closing routine. Because it is very closely related to the initialization program, the feedback-loop closing routine will be explained in the following section.

#### 3.1.2 Initialization Program

Examples in the next chapter will point out the fact that the design outlined in Chapter 2 creates a problem in the transient response of the plant. The reason for the poor transient response is the plant's slowness in reacting to the sudden change in the input signal brought about by the step function. This is reflected by the feedback IPFM's The effect is explained in Section 2.1. Fig. 2.3 is a typical example of this problem. This problem is solved by programming the controller to ignore the feedback pulse, i.e., operate in the open-loop mode. Instead of a plant excitation signal like that of Fig. 2.3 being emitted from the controller, it is forced to emit a signal like that of Fig. 2.2. Then, when the plant response is 'near' the desired operating point, the controller is made to use the feedback pulse to characterize the plant excitation signal by closing the loop.

To operate in the open-loop mode, the characteristics of the signal we want to force the phase comparator to generate must be chosen. From Chapter 2 we know that any gain/
IPI(inter-pulse interval) pair on the locking curve of Fig.
2.6 such that the gain does not exceed the critical gain, will keep the system stable, therefore the question is which pair of values is to be used.

It was pointed out earlier that the higher the gain, the better the system performance (see Fig. 3.1). The critical gain best satisfies this criterion. In the open-loop mode then, the system will be forced to operate very near its critical point.

There are two ways to find the critical point. The first way uses the equations from Chapter 2 for the locking and stability relationships. From these relationships, a computer can find the critical point by trial and error, or graphically as in Fig. 2.6.

The problem with this first method is that, as the plant becomes more complex (i.e., third order, fourth order, etc.), the equation for the system locking becomes extremely complex. For this reason, another method is devised.

The second method uses the stability relationship and the plant (or a simulation) itself. The equations for stability are relatively easy to solve even for the more complex plants. Using a computer, a list of gain/IPI pairs that adhere to the stability relationship can be made. Using tri-

al and error then, the plant, in open-loop mode, is controlled by a signal with these gain/IPI characteristics. The required pair will correspond to the intersection point of the locking and stability curves (see Fig. 3.2), i.e. the point  $(K_{\mbox{\scriptsize C}},T_{\mbox{\scriptsize C}})$ .

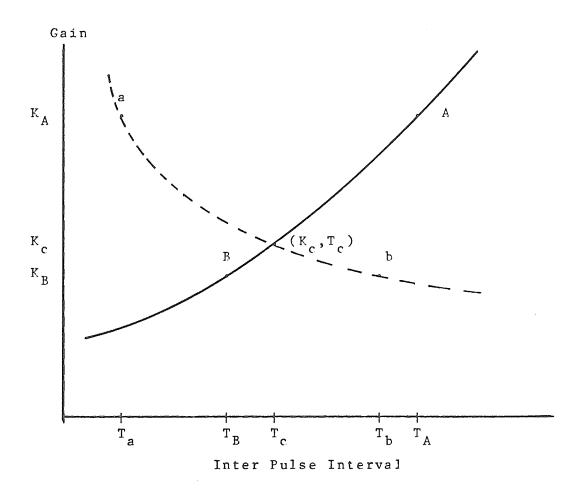


Figure 3.2: Using the stability relationship only method

For a step input there will be, at most, one intersection point. For a first order system, points on the stabil-

ity curve are calculated using equation (2.7) from Chapter 2. The location of the locking curve is uncertain. From Chapter 2 though, one can see that the equation for locking, equation (2.6), depends on the input to the system (a step function in this case). (A different input would produce a different locking curve.) Every point on the locking curve of Fig. 3.2 causes the average plant output to be the same as the input signal therefore this will also be true at the point were the two curves intersect. The method for finding the critical point is now explained by example and using Fig. 3.2.

Let the system have a one volt step input, and let point A be the test point. From the locking curve, to get a plant response with a one volt average, the pair  $(K_A, T_a)$  should be used. Using  $T_A$  instead will make the phase error too large and so the trapezoidal signal will be too large. This will make the plant average signal larger than one volt.

A similar problem occurs if point B is the test point. Now,  $\mathbf{T}_{B}$  is too small and so the plant output will have an average less than one volt. Examples of this will be shown in the next chapter.

The obvious problem with this method is that the plant, or a simulation of it, is needed. If neither is available, this method cannot be used.

Regardless of which method is used in finding the critical point, there is the question of when to close the feedback loop. The criterion used is: the loop will be closed when the average plant output is within a given range of the input signal.

Due to quantization of the analog values for gain and IPI, the values used by the controller may not be the exact counterparts of the analog values, so the voltage range has to be greater than zero. If the voltage range is too large, the loop will be closed too early, resulting in a poor transient response. If the range is too small, and the values used are not very accurate, the loop may never close. After experimenting with three different ranges,  $\pm 1$ ,  $\pm 2$ , and  $\pm 3$  quantum levels, it was decided that a range of  $\pm 2$  quantum levels should be used (one quantum level corresponds to about 20 my, i.e., 1/256 of 5 volts).

#### 3.1.3 Interrupt Routine

The last part of the controller is the interrupt program which contains the PLL-IPFM implementation. It consists of three integration routines, i.e., the input integral, the output integral, and the feedback integral. The integral, I, of a signal, y(t), is approximated by the equation,

where n is the number of sections over the integration period [17], i.e., n =  $T_{0}/\Delta t$ .

The integrators are in the interrupt routine so that the t in equation (3.1) will be small and constant (a requirement of equation (3.1)). The interrupt is controlled by a timer (a CTC) which is programmed to interrupt the microprocessor once every 1/256 of a second. This gives an essentially constant, and small, t relative to the period.

The value produced by the output integral is analogous to the phase comparator output signal discussed in Chapter 2 This signal, after being multiplied by the gain (using the technique suggested in [18]), controls the plant.

### 3.2 THE INTERFACE

Due to the different signal requirements, interfacing between the two computers is needed. These interfaces are composed of A/D converters, a D/A converter, and associated hardware.

The D/A converter translates the digital word from the micro-processor system, into a current signal. An operational amplifier is then used to change this current into a voltage suitable for the analog computer.

The A/D converter continuously converts the particular signals (input and plant output) into digital words. In this conversion mode, a slight delay is needed between the end of a conversion cycle and the beginning of the next conversion. Shift register circuitry is employed to accomplish this.

Also, the maximum clock frequency the A/D converter will operate at is less than the available system clock. A divide-by-six circuit slows the 4 MHz system clock to 667 kHz, which is within the range of the A/D converter.

These circuits and necessary timing diagrams are shown in Appendix A.

## 3.3 SOURCES OF ERROR

Most of the errors that plague other digital systems, plague this controller. These problems are mainly in the form of constraints placed on the system, either by the plant or by the digital controller itself [16].

The major problem with this digital controller is due to the fact that the micro-processor system being used is only an 8-bit machine. Because of this, errors are created by the quantization of the analog signals and the gain value, and by the rounding process in the multiplication subroutine. These errors, along with the fact that there is probably noise present, will make "... perfect locking always with zero error impossible."[14].

There are other problem areas in this digital controller. The error created by the integration approximation is slight; a value of  $\Delta y(t) \propto \Delta t/2$  [17] ( $\Delta y(t)$  and/or  $\Delta t$  are very small).

A problem with digital controllers in general, is the minimum cycle time required. Minimum cycle time refers to

the minimum amount of time needed for the program to function correctly. For this controller, the minimum cycle time is governed mainly by the slowest time it takes the interrupt routine to execute. Time is also needed for the main program to run but this is a small amount in comparison to the interrupt routine time. The program is interrupted once every 1/256 of a second, so the minimum cycle time has to be less than 3.9 msec.. Fortunately, for this digital implementation, the minimum cycle time is about 0.6 msec., so the minimum cycle time is not a problem.

Considering these sources of error, slight as they may be, a system will be considered stable if the maximum controller output voltage varies (randomly) by no more than one quantum value about an obvious average quantization level.

# 3.4 INCREMENTAL GAIN VARIATION

As was explained in Section 3.1.1, the adaptive controller varies the gain to suit the situation the system is in. In this section, an expression is developed to show how sensitive the gain is with respect to changes in the plant response. By using this sensitivity expression, any 'undesirable' changes in the plant response can be counteracted by an appropriate change in gain. This should keep the system operating very near its critical point for all time.

Theoretically, this sensitivity analysis which is about to be developed, works. Unfortunately, the final expression

Theoretically, this sensitivity analysis which is about to be developed, works. Unfortunately, the final expression includes exponential and square root terms. Evaluating these terms on the micro-processor system being used would create innumerable errors and take too much computer time, i.e., this analysis is useful if a more powerful machine were used but it is just not practical for use with this digital controller.

# 3.4.1 <u>Sensitivity Analysis</u>

The incremental amount the controller varies the gain by is a major determining factor on how well the system performs. For cases when the plant change is very gradual (if at all), a very small gain increment is desired; just enough change in the gain to allow the controller to follow the plant variations and keep the plant at the critical point. The increment cannot be so large though, as to send the system into instability. If there is the possiblity of very abrupt changes, a larger gain increment would be better. A large increment means a faster response by the controller which would have the system operating at the critical point in a shorter time.

From the previous sections, it was shown that the system will be operating very near its critical point when adaptability is invoked. Therefore, any plant variations will cause one of two things to happen to the system: either

If the plant variations cause the system to become more stable, the ripple will increase in size, assuming the system remains phase-locked. This situation creates no real problem with the system. The system response is just not as good as it could be.

Problems arise when the plant variation causes the system to go to its critical point. As was explained in Section 2.2.3, these plant variations cause the feedback pulses to oscillate about some theoretical value. These oscillations cause the average system response to oscillate about the system input value (this will be seen in the next chapter).

For the sensitivity analysis, the controller observes the plant output at the start of every interval, i.e., whenever an input pulse is detected. By observing the plant output at these points, the controller is able to decide if the system is going unstable or remaining stable. (If the points do not oscillate about some value, but instead are equivalued, then the system is stable.)

Equation (2.2) mentioned in Chapter 2 for the plant response is the starting point of the analysis. This equation was derived assuming that the system was in steady-state and so a further assumption is that, for this analysis, the system is stable until time  $t=t_{i-1}$ . For convenience, let j=i-1 and so  $t_{i-1}=t_j$ . For simplicity, it is also assumed that the incremental gain variation is constant over a given interval,  $T_0$ , and if the gain variation is changed, it is done instantaneously at the beginning of the interval.

incremental gain variation is constant over a given interval,  $\mathbf{T}_0$ , and if the gain variation is changed, it is done instantaneously at the beginning of the interval.

Symbollically then, for the  $i\frac{th}{t}$  interval extending over the time  $t_i$  to  $t_i+T_0$ , the controller will use the plant response occuring at the time  $t_i$  to decide if the system is stable. For time  $t>t_j$ , the system is assumed to be on the verge of instability. The controller senses this and instantaneously changes the gain in accordance with the sensitivity expression for the interval  $t_i < t \le t_{i+1}$  so that the system is again stable.

For a first order plant then, equation (2.2) which relates the plant response at a time t, i.e.  $y(t-t_j)$ , to the gain K, and IPI, T, for a given period  $T_0$ , becomes:

$$y(t-t_{j}) = [e^{-a(t-t_{j})} \cdot y_{t}] u(t-t_{j}) +$$

$$\begin{bmatrix} K^{\circ}(t-t_{j}) + K(e^{-a(t-t_{j})}-1) \\ ----_{a} & a \end{bmatrix} u(t-t_{j}) -$$

$$\begin{bmatrix} K(t-t, -T) + K(e^{-a(t-t, -T)} - 1) \\ ----i \\ a \end{bmatrix} u(t-t, -T)$$

where -a is the pole location

and 
$$y_t = K(e^{-aT_0} + aT - e^{-a(T_0-T)})$$
  
 $a^2(1-e^{-aT_0})$ 

The sensitivity of the plant response with respect to the gain then is given by:

$$\frac{\partial y(t-t_{j})}{\partial K} = \begin{bmatrix} e^{-a(t-t_{j})} \cdot \partial y_{t_{j}} \\ ---- \\ \partial K \end{bmatrix} u(t-t_{j}) +$$

$$\begin{bmatrix} (t-t_{j}) + e^{-a(t-t_{j})} - 1 \\ ---\frac{1}{2} & ---\frac{1}{2} \end{bmatrix} u(t-t_{j}) - 1$$

$$\begin{bmatrix} (t-t, -T) + K & (t-t, -T) \\ ---, j & ---, --- \\ a & a & K \end{bmatrix} u(t-t, -T) -$$

$$\begin{bmatrix} (e^{-a(t-t_j-T)}-1) \\ ----\frac{2}{a^2} \end{bmatrix} u(t-t_j-T) -$$

$$\begin{bmatrix} K & \partial(e^{-a(t-t_j-T)}-1) \\ -\frac{1}{2} & \partial K \end{bmatrix} u(t-t_j-T) \qquad \dots (3.2)$$

where,

$$\frac{\partial}{\partial K} (t-t_j-T) = -\frac{\partial T}{\partial K}$$

$$\frac{\partial}{\partial K} (t-t_j-T) = -\frac{\partial T}{\partial K}$$

$$\frac{\partial}{\partial K} (t-t_j-T) = -\frac{\partial T}{\partial K}$$

and,

$$\frac{\partial}{\partial K} \left( e^{-a(t-tj^{-T})} - 1 \right) = \frac{\partial}{\partial K} \left( e^{-a(t-tj)} \right) \cdot e^{-aT} + \frac{\partial}{\partial K}$$

$$e^{-a(t-t_j)} \cdot \partial (e^{aT})$$

= 
$$0 \cdot e^{aT} + a \cdot e^{-a(t-t j^{-T})} \partial T$$
 .....(3.4)

To continue this analysis, an equation relating IPI to gain is needed. Rearranging equation (2.6) of Chapter 2, one gets,

$$K = \underbrace{2 \cdot a \cdot E}_{2 \cdot T \cdot T_{0} - T^{2}}$$

where E=threshold value. This becomes:

$$T^{2} - 2 \cdot T \cdot T_{0} + 2 \cdot a \cdot E = 0$$

$$K$$

or,

$$T = T_0 + \int T_0 - 2 \cdot a \cdot E / K$$
 ....(3.5)

For  $0 \le T \le T_0$ , equation (3.5) becomes:

$$T = T_0 - \int T_0 - 2 \cdot a \cdot E / K$$
 .....(3.6)

For this thesis,  $T_0=1$  and E=1, therefore equation (3.6) becomes:

$$T = 1 - \sqrt{1 - 2 \cdot a / K}$$

From this one gets,

$$\frac{\partial T}{\partial K} = \frac{\partial}{\partial K} \begin{vmatrix} 1 - \sqrt{1 - 2 \cdot a} \\ - - - \end{vmatrix} \begin{vmatrix} 1 - \sqrt{1 - 2 \cdot a} \\ - - - \end{vmatrix} \begin{vmatrix} 1 - \sqrt{1 - 2 \cdot a} \\ - - - \end{vmatrix} \end{vmatrix}$$

= 
$$\frac{\partial}{\partial K}$$
 [ - ( 1 - 2 · a / K )  $^{1/2}$  ]

$$= -a$$
 ....(3.7)  

$$K^{2} (1 - 2 \cdot a / K)^{1/2}$$

Substituting equation (3.7) into equations (3.3), and (3.4) respectively, one gets:

$$\frac{\partial}{\partial K} (t-t_j-T) = \frac{a}{\sqrt{2} \cdot (1-2 \cdot a / K)^{1/2}}$$

$$\partial (e^{-a(t-tj^{-T})}-1) = -a^2 \cdot e^{-a(t-tj^{-T})}$$
  
 $\partial K \qquad K^2 \cdot (1-2 \cdot a/K)^{1/2}$ 

Substituting these equations into equation (3.2) gives:

$$\frac{\partial y(t-t_{j})}{\partial K} = \begin{bmatrix} e^{-a(t-t_{j})} \cdot \partial y_{t_{j}} \\ ---- \\ \partial K \end{bmatrix} u(t-t_{j}) + \frac{1}{2}$$

$$\begin{bmatrix} (t-t_{j}) + e^{-a(t-t_{j})} - 1 \\ ---\frac{1}{2} & ----\frac{1}{2} \\ a & a^{2} \end{bmatrix} u(t-t_{j}) - 1$$

$$\begin{bmatrix} (t-t_{j}-T) + 1 & & & \\ ---j & & & \\ a & & K(1-2a/K)^{1/2} \end{bmatrix} u(t-t_{j}-T) -$$

$$\begin{bmatrix} e^{-a(t-t j-T)} - 1 \\ ----\frac{2}{a^2} \end{bmatrix} u(t-t j-T) +$$

$$\begin{bmatrix} e^{-a(t-t_{j}-T)} \\ e^{-\frac{1}{2}} \\ K(1-2a/K) \end{bmatrix} u(t-t_{j}-T) \qquad \dots (3.8)$$

Equation (3.8) is an expression for all time greater than  $t=t_j$ , that relates changes in the plant response to changes in gain. For the sensitivity analysis, the relationship between the changes in plant response and gain is wanted at time  $t=t_i$  or  $t_j+T_0$ . The time  $t=t_j$  has passed and so the plant response at that time, i.e.  $y_{t_j}$ , has already occured. Therefore, evaluating expression (3.8) at  $t=t_j+T_0$  gives:

$$\begin{bmatrix} T_0 - T + & 1 & - \\ -a & K(1 - 2a/K)^{1/2} \end{bmatrix} -$$

$$\begin{bmatrix} e^{-a(T_0-T)} - 1 \\ ----\frac{1}{2} - --- \end{bmatrix} +$$

$$\begin{bmatrix} e^{-a(T_0-T)} \\ -\frac{1}{2} \\ K(1-2a/K) \end{bmatrix}$$
 .....(3.9)

Recombining, one gets:

$$\frac{\partial y(t_i)}{\partial K} = e^{-aT_0} (1 - e^{-aT}) + aT + e^{-a(T_0 - T)} - 1 \\ -\frac{1}{2} \times K(1 - 2a/K)^{1/2}$$

$$= X$$

By approximating the partial derivative in equation (3.10) by the discrete amounts  $\Delta y(t_{\underline{i}})$  and  $\Delta K$ , one gets:

$$\Delta y(t_i) = X \cdot \Delta K$$

Or, solving for  $\Delta K$ :

$$\Delta K = [X]^{-1} \cdot \Delta y(t_i)$$
.....(3.11)

Even though the resulting equation (3.11) is for a first order system, the expression is far too complex to be solved by the 8-bit microprocessor being used. The exponentials would have to be approximated by the first few terms of their series expansion. Using any more than the first two terms in the series would introduce multiplication rounding errors. The other multiplications and divisions in the expression would introduce more rounding errors to the resultant. The algorithm used to solve the square-root term will also introduce rounding errors. With all of these errors and approximations, the result of the expression would not be a very good estimate for the sensitivity.

The expression would also take a lot of computer time to solve even if, some how, the errors and approximations were not too much of a problem. This would probably make the program execution time greater than the minimum cycle time which was defined in the previous section. If this happens, then the controller will not work properly.

With all of these problems of timing constraints, approximations, and rounding errors, using the sensitivity analysis equation to change the incremental gain is not practical for the micro-processor system being used. If a more powerful machine were used, then this analysis could be useful.

Therefore, for this thesis, the incremental gain variation will be a constant one quantum increase or decrease in the gain. Using this smallest variation possible will insure that the system is not suddenly operating way beyond the critical point; the system will be operating, at most, one gain quantum past the critical.

Unfortunately, using the smallest incremental gain variation possible means that the system reacts very slowly to sudden plant changes. It will be seen in the next chapter though, that the one quantum variation gives good results, even for the case when the plant pole location is suddenly changed.

### Chapter IV

#### RESULTS

### 4.1 PREFACE

This chapter deals with the actual testing of the controller. The controller is first made to operate similar to the design discussed in Chapter 2. The performance of the digital implementation can then be compared to the results found in Chapter 2. A problem, called the loss-of-lock phenomenon [19], occurs with this design. An example showing this phenomenon is given.

The rest of the chapter is devoted to the improvements made on the controller, starting with the addition of the open/closed feedback routine. A method for finding the critical gain and inter-pulse interval(IPI) values when the locking relationship is unknown is demonstrated. Finally, the adaptive controller (with the open/closed feedback routine) is tested for various systems.

Fig. 4.1 shows a block diagram of the proposed digital control system. The plants to be controlled are simulated on the analog computer. Recordings are made of the control signal and the plant response. The input to the system is a one volt step function which is shown as a dashed line on the recordings. Also, the integrators have a threshold value

of one volt-second, which makes each interval one second in duration.

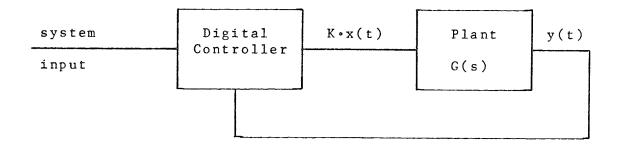


Figure 4.1: Digital control system

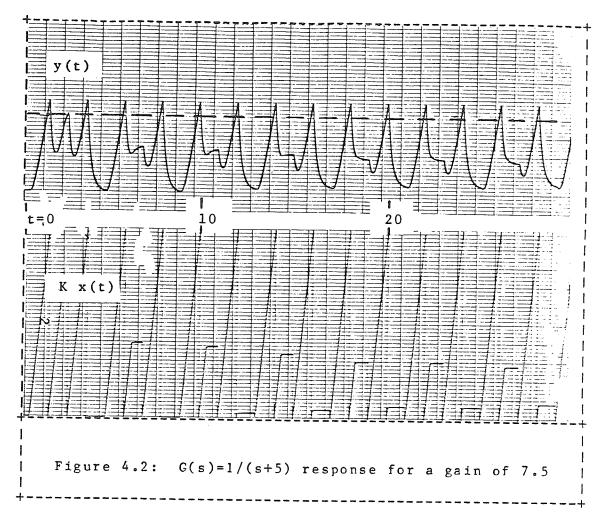
### 4.2 DIGITAL DESIGN

To compare the digital implementation to the analog design, we will test the controller on a first order plant where G(s)=1/(s+5). It was pointed out in Chapter 2 that theoretically the range of gains this system should be phase-locked for is:

 $10.0 \le K < 20.8$ 

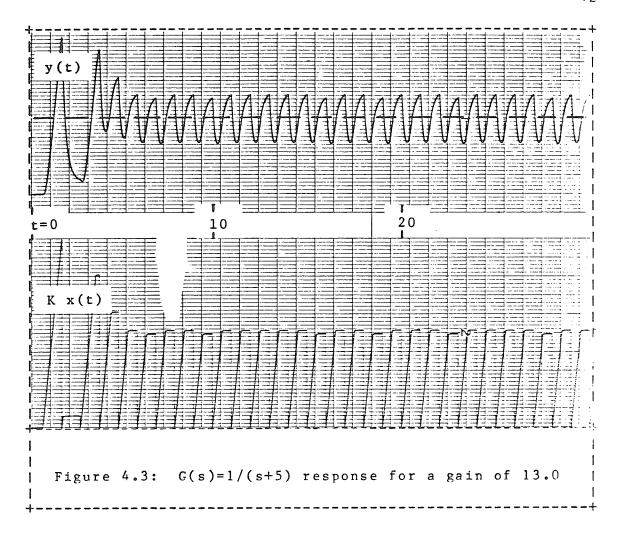
Figs. 4.2, 4.3, 4.4, show a sampling of the test results.

In Fig. 4.2, the gain used is 7.5. The system should be, and is, out of phase-lock because the controlling signal is not large enough. Looking at the first interval, the control signal has a sawtooth waveform. This is the strongest signal the controller will inject into the plant, yet it is

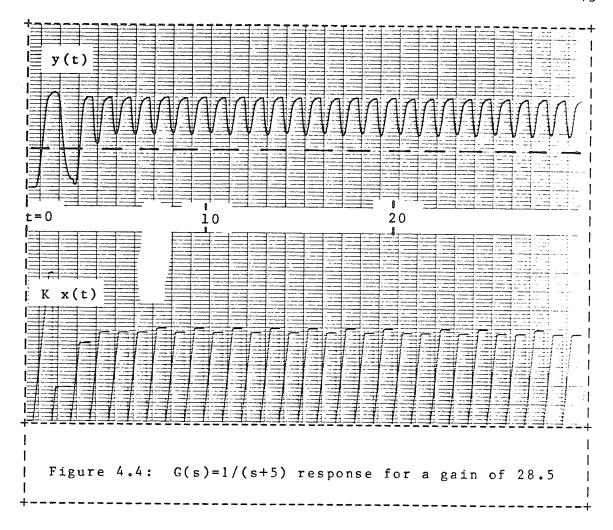


just barely enough to force the system above one volt. For the ensuing intervals the feedback causes signals of less strength to be produced by the controller, and therefore the system cannot get into phase-lock.

The gain in Fig. 4.3 is 13.0. The system, after about five intervals, is in phase-lock and stable. There are a few things to notice in this figure, the transients being the most obvious problem with the plant response.



These transients are caused by the sawtooth signal in the first interval and then the very small trapezoid in the next interval. This trapezoid is created because the feedback integrator, which stops the ramp signal thereby creating a trapezoid, takes more than one interval to reach the threshold value. In other words, the trapezoid is created by the input integrator reaching threshold for the second time as the feedback integrator reaches threshold for the first time. This effect is typical of this controller design.



Notice too, in Fig. 4.3, the staircase effect on the ramp portion of the trapezoids, and the apparent imperfect locking; the maximum amplitude of the trapezoids, when the system is in phase-lock, varies by one quantum level sometimes. Both of these effects are due to quantization.

Fig. 4.4 shows the loss-of-lock phenomenon. The gain used is 28.5, well above the critical gain for this plant, yet the system appears to be in phase-lock.

This phenomenon can be explained by first examining equation (2.6) in Chapter 2. Rearranging it:

$$K = E \cdot a / [t \cdot (T_0 - t/2)]$$
 ....(4.1)

where, -a = pole location (= -5)

$$T_0 = interval (= 1 sec.)$$

E = threshold level

Rearranging equation (4.1):

$$t^2 - 2 \cdot t + 2 \cdot E \cdot 5 / K = 0$$

or:

$$t = 1 - \sqrt{1 - 2 \cdot E \cdot 5 / K}$$
 ....(4.2)

because  $t \leq T_0 = 1$  sec.

Substituting values for E(=1), a, and K(=28.5) into equation (4.2) gives t=0.19 seconds. Obviously, this is not the IPI value in Fig. 4.4 the value is approximately 0.5 seconds.

If the threshold is two volt-seconds though, equation (4.2) gives an IPI of 0.45 seconds which agrees with Fig. 4.4. What has happened is, there are actually two feedback pulses for every one input pulse (see Fig. 4.5). The second feedback pulse is ignored by the controller, so that the controller views the plant as if it were responding to a one volt step input, while the plant responds to an apparent two volt step input. The plant is forced up to the two volt level and held there by the size of the gain.

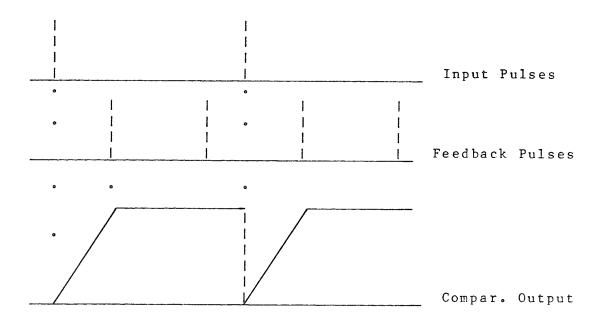
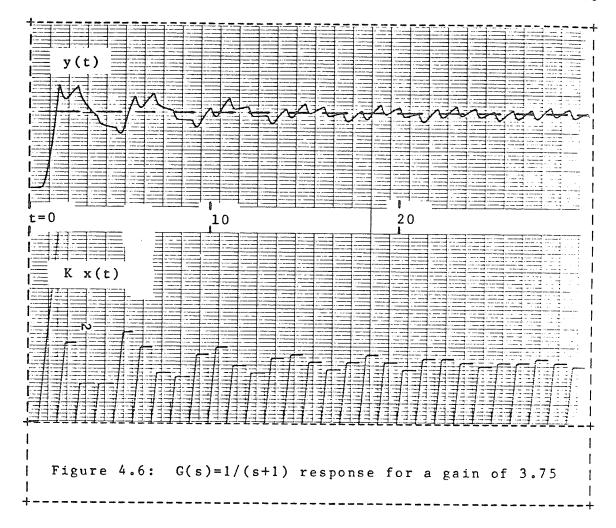


Figure 4.5: Loss-of-lock phenomenon situation

Comparing the results of the digital controller to those of the analog controller, it appears there is agreement between them (see Table 1 in Chapter 2). The only disagreement is with the loss-of-lock phenomemon case. Woo did not observe this result only because he simulated the entire system on a computer and did not make allowances in the program for the plant to lock at other than one volt.

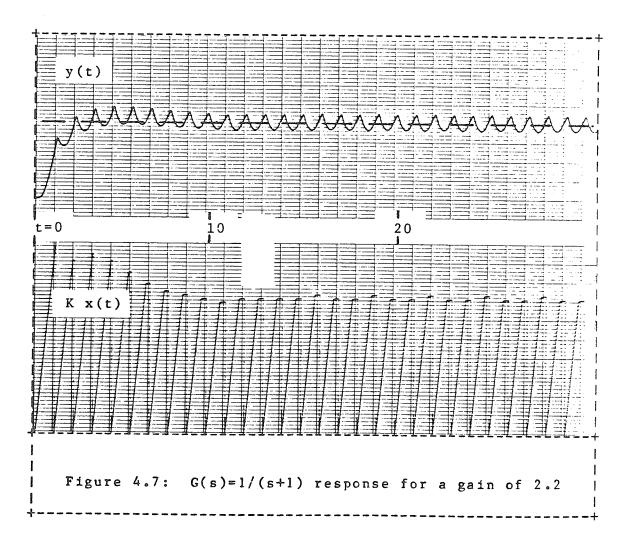
From these comparisons then, one must conclude that the digital implementation operates in a way similar to that of the analog controller.

Testing the same digital controller on a different plant, G(s)=1/(s+1), produces the results shown in Figs. 4.6 and 4.7.



The gain used for Fig. 4.6 is 3.75. Being this close to the critical gain causes problems for the controller. Notice the first interval sawtooth that drives the system to the one volt level. The transients, caused by this sawtooth, do not appear to he as bad as they were for the previous plant. The present system though, does not approach phase-lock for at least twenty intervals, and even then there is an oscillation on the control signal for another twenty intervals. Then, finally the system is locked.

In Fig. 4.7 the gain used, 2.2, is very close to the minimum locking gain of 2.0. At this low gain, the transients are not too much of a problem. The ripple (defined earlier) though, is twice the size of the ripple in Fig. 4.6. Because the ripple is less (a prime objective) for higher gains, the system will operate with as high a gain as possible.



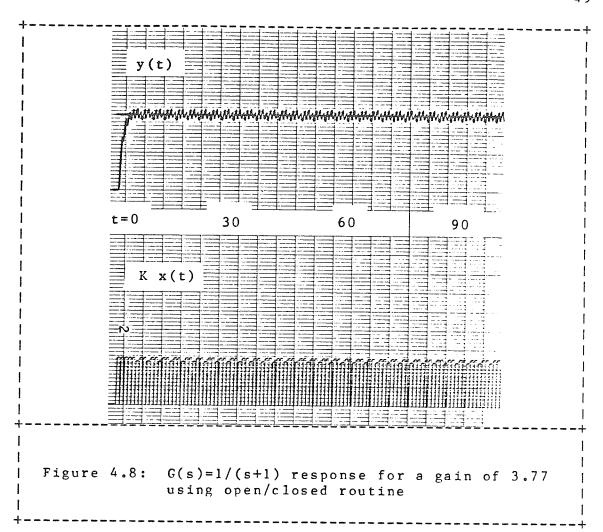
# 4.3 OPEN/CLOSED FEEDBACK LOOP DESIGN

The previous discussion has made the transient response problems with the design quite clear; the transients are too large and/or too long. In this section one will see that incorporating an open/closed feedback loop routine, like the one detailed in Chapter 3, improves the transient response.

Fig. 4.8 shows the results of the same 1/(s+1) plant, but with the open/closed-loop routine added to the controller. The controller is forced, in the open-loop mode, to emit a trapezoidal signal to the plant. These trapezoids are characterized (see Fig. 2.4) by the critical values of gain and IPI, i.e.,  $K_c=3.77$ ,  $T_c=0.375$  seconds. The vast improvement in the plant response is obvious; the system is in phase-lock in about five intervals and there is no overshoot or undershoot.

Fig. 4.9 shows the results of a plant characterized by G(s)=1/(s+2) to the same controller routine. In the open-loop mode, the critical values of gain and IPI for this plant ( $K_c=6.64$ ,  $T_c=0.370$  seconds) are again used to characterize the trapezoidal signal. This plant response is almost as good as the response of the plant G(s)=1/(s+1). The slightly poorer response (seven intervals to lock) of the present plant is due mainly to the error in digitizing the analog gain and IPI critical values.

The critical values used for the plant G(s)=1/(s+2) are derived from equations (2.6) and (2.7) of Chapter 2. The



open-loop response of the plant to these values of gain and IPI is shown in Fig. 4.10. One can see that the average of the plant response is about one volt. As was explained in Chapter 3, if only the stability equation is available, then, by testing different points on the stability curve and observing the average plant response, a fairly good estimate for the critical gain and IPI can be obtained. This trial and error method is made use of on the second order plant, G(s)=1/[(s+1)(s+2)].

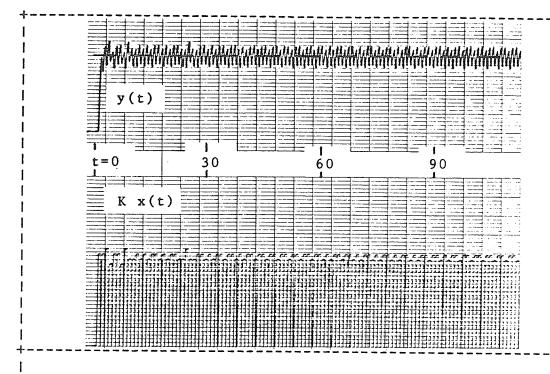


Figure 4.9: G(s)=1/(s+2) response for a gain of 6.64 using open/closed routine

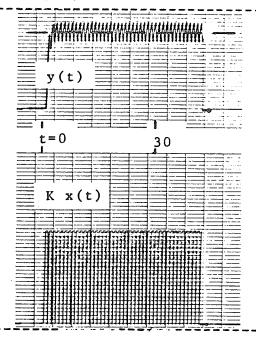


Figure 4.10: G(s)=1/(s+2) response for a gain of 6.64 in open-loop mode

Figs. 4.11, 4.12, 4.13 show this second order system's open-loop response to different gain/IPI pair values that satisfy the stability equation only.

Fig. 4.11 shows the resulting response when the pair is greater than the critical gain/IPI pair values; the average value of the plant output is about 1.2 volts. If the pair is smaller than the critical pair, the result is Fig. 4.12: the average plant output for this case is about 0.9 volts.

The gain/IPI pair used in Fig. 4.13 gives the best result with the plant average about 1.04 volts. It is not necessary to be completely accurate in chosing the values to be used because the rest of the program will take care of any minor discrepancies. Therefore, the pair used in Fig. 4.13 will be used as the critical values.

If the gain/IPI pair used in the program does not give a very good open-loop response, the system has a great deal of difficulty adjusting itself when the loop is closed. This can be seen in Fig. 4.14 where the gain/IPI pair of Fig. 4.11 is used, and the open/closed-loop routine is incorporated.

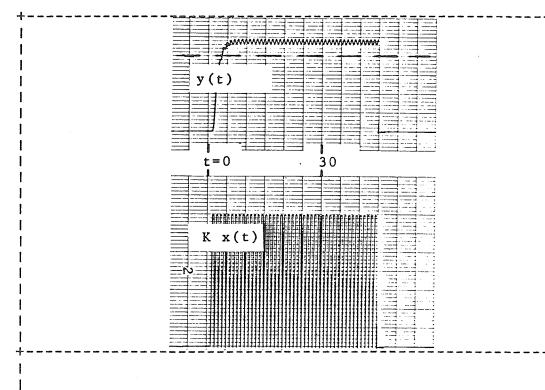


Figure 4.11: G(s)=1/[(s+1)(s+2)] open-loop response for a gain greater than critical

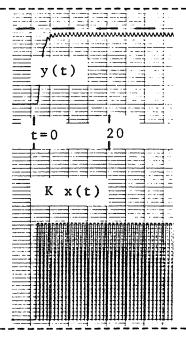
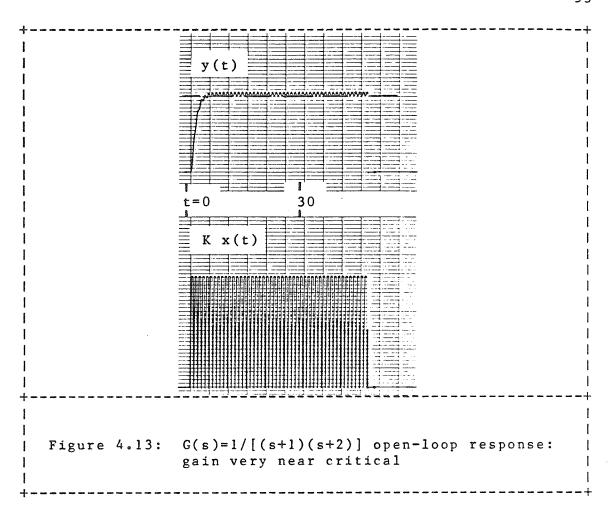
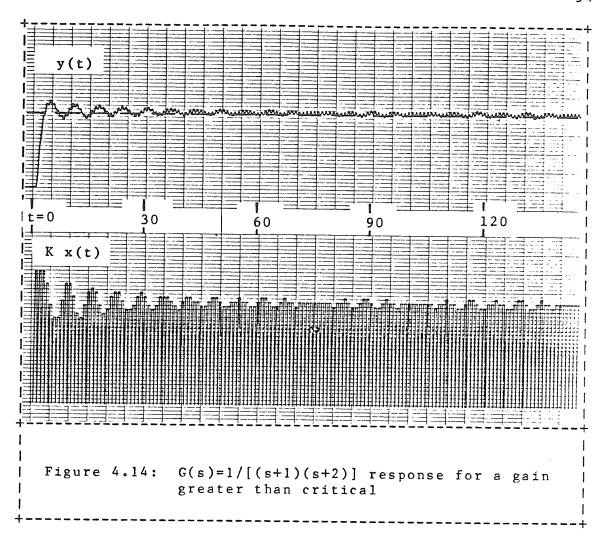


Figure 4.12: G(s)=1/[(s+1)(s+2)] open-loop response for a gain less than critical



When the loop closes, the controller takes over sixty intervals to get the system into phase-lock. Then, because the gain used in Fig. 4.14 is greater than the critical gain, phase-lock is lost after ten intervals. Therefore, even though it is not crucial that the open-loop values used for the critical pair are not the actual values, the closer the values are to the actual critical values, the better the plant response will be.

The symbols K and T will be used from now on to denote the respective open-foop critical values of gain and inter-pulse interval.



## 4.4 ADAPTIVE CONTROLLER

All the systems that have been discussed up to now have been fixed, i.e., the controller gain was constant and the pole location(s) of the different plants did not vary. In this section, the adaptability of the controller will be tested. The ability of this controller to vary the gain to suit the plant is what makes this controller so much more versatile than the previous designs.

Before any test results are examined, a criterion for varying the gain is needed. For this particular controller, the gain is varied such that the plant yields its best response, and the gain is as high as possible. "Best" response means the ripple is as small as possible, and the average value of the plant response is exactly the same as the input signal (one volt in this case).

The adaptive controller is tested under two different conditions. The first set of tests uses a fixed plant and the controller varies the gain to yield the best possible response. In the second set of tests, the plant changes its pole location and the controller varies the gain to follow the change and give the best possible response.

The fixed first order plant, G(s)=1/(s+2), is used to compare the fixed controller's response (Figure 4.9) to the adaptive controller's response shown in Figs. 4.15 and 4.16. Examining the control signal in Fig. 4.9 a slight periodicity is noticed. There is no such periodicity in Fig. 4.15. The control signal is more random in nature.

The periodicity of Fig. 4.9 super-imposes a three hertz signal on the average value of plant output. To the adaptive controller, this variation of the average value is taken as an unstable system response. To prevent instability, the gain is reduced until no oscillations in the control signal are noticable. This is why the control signal of Fig. 4.15 appears random. After twenty-two intervals phase-lock is

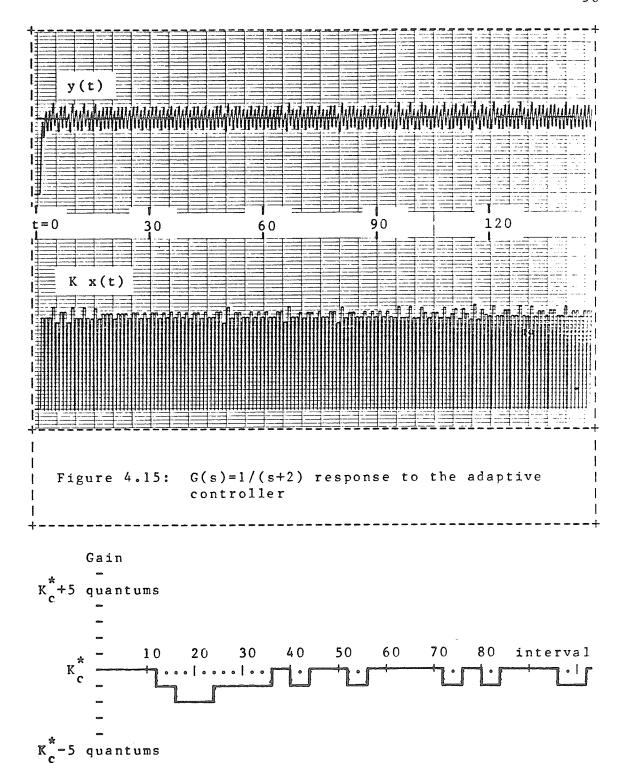


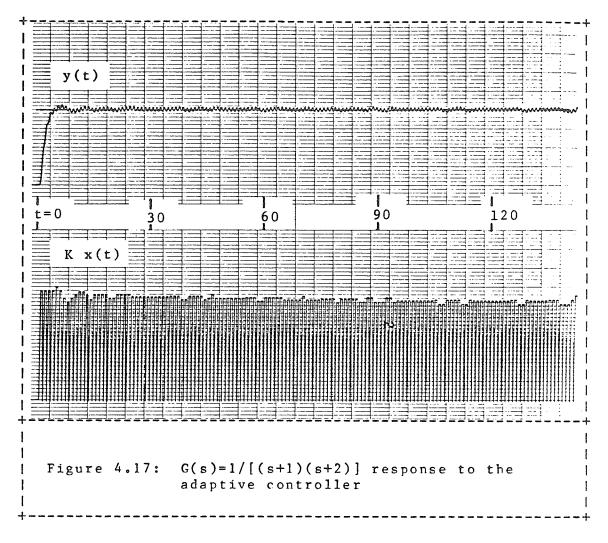
Figure 4.16: G(s)=1/(s+2) gain variations corresponding to the above response

achieved; the controller has reduced the gain from 6.61 to 6.44, a three quantum level decrease.

After reaching phase-lock, the controller constantly tries to increase the gain to get a better response. Twelve periods in phase-lock elapse before the gain is increased by one quantum value. The system becomes unstable and so the gain is decreased to 6.44 again. From Fig. 4.16, which shows the actual gains used in Fig. 4.15, one can see that the controller is always trying to push the gain higher.

Figs. 4.17 and 4.18, and Figs. 4.19 and 4.20 show the system responses of the plants G(s)=1/[(s+1)(s+2)], and G(s)=1/[(s+1)(s+3)] respectively. From the gain variation plots of the respective plants (Figures 4.18 and 4.20), one can see that, unlike the first order plant just discussed, the gain for these plants increases. This increase implies that the starting values of gain and IPI were less than the critical values. As was pointed out earlier, it is not important to start at the critical values because the controller varies the gain to get the best response.

The insensitivity of the system to the starting value of gain can be further recognized by starting the plant G(s)=1/[(s+1)(s+2)] at the apparent critical gain just found for this system (from Fig. 4.18). This gain, and corresponding IPI value, gives the response shown in Fig. 4.21. The overshoot makes the controller decrease the gain for a short time. The gain is then increased until the same final



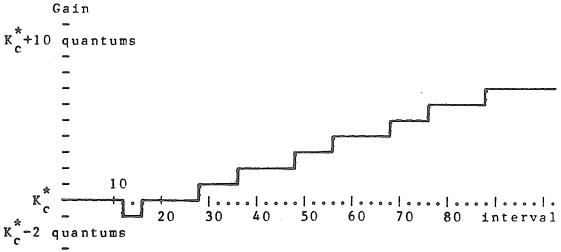


Figure 4.18: G(s)=1/[(s+1)(s+2)] gain variations corresponding to the above response

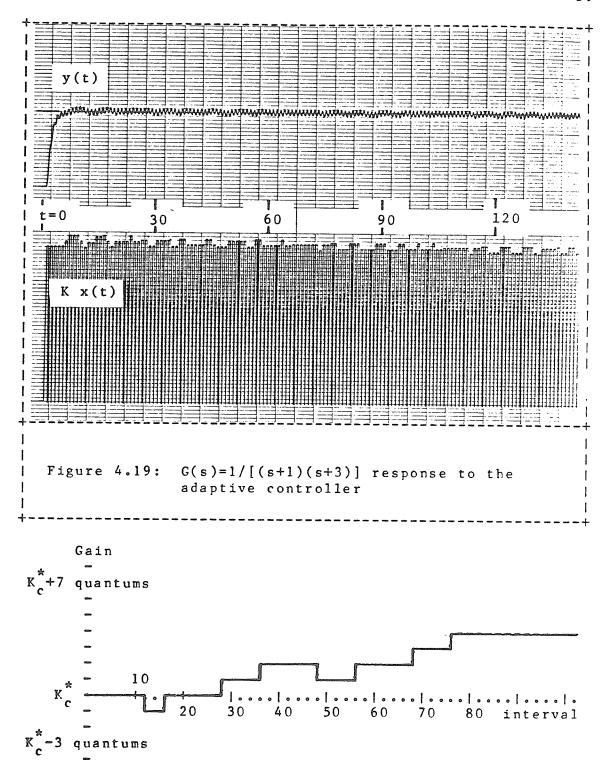


Figure 4.20: G(s)=1/[(s+1)(s+3)] gain variations corresponding to the above response

gain that was reached previously is achieved. (Compare Fig. 4.18 with Fig. 4.22). This shows how the controller is insensitive to the values of gain and IPI used to start the system, when the values used are close to the critical values.

The adaptability of the controller to plant variations is now tested. In a real application, changes in the plant are very possible. If plant changes occurred, a fixed controller would not be able to give the best response possible without some manual tuning. An adaptive controller though, would be able to adjust to these changes accordingly.

Fig. 4.23 shows how the adaptive controller responds as the plant G(s)=1/(s+2) changes its pole location from -2 to -1.75. Comparing Figs. 4.24 and 4.18, the gain variations at the beginning of the test are about the same, as they should be. About thirty intervals after start-up, the plant is suddenly changed to the form G(s)=1/(s+1.75). The change is too fast for the controller to make a smooth transition, but it eventually does get the new system into a stable phase-lock. The gain, when stability is attained (K=6.08), is only 4% higher than the critical gain for this plant predicted by the equations ( $K_c=5.84$ ). (Similar results are obtained when the change is more gradual.)

The result of a similar situation occuring with the same plant, but with a fixed controller, is shown in Fig. 4.25. The starting gain for a first order plant with its

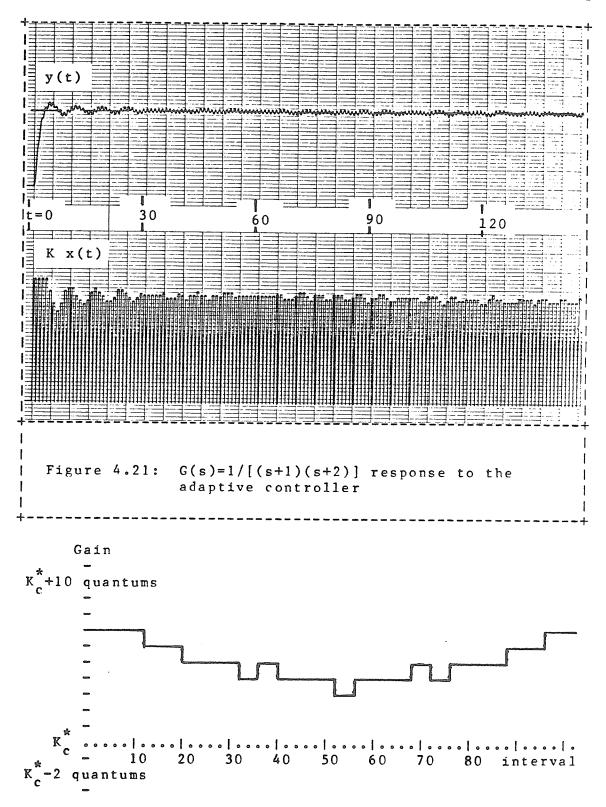


Figure 4.22: G(s)=1/[(s+1)(s+2)] gain variations corresponding to the above response

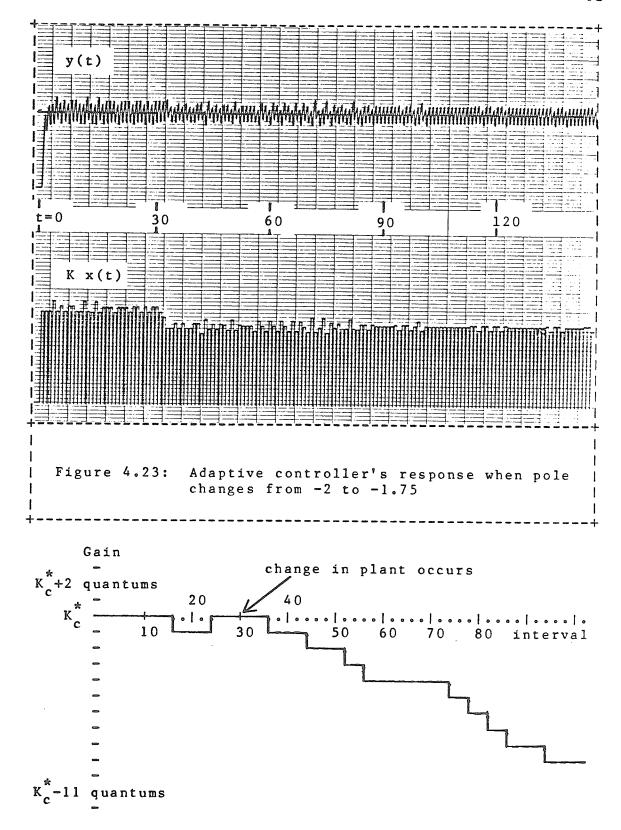


Figure 4.24: Gain variations corresponding to the above response

pole at -2 is used throughout. When the plant suddenly changes its pole location, the gain is greater than the critical gain for a 1/(s+1.75) plant. Because the gain is too high, the trapezoids of the plant excitation signal oscillate about the theoretical value which causes the average plant response to oscillate about one volt. Recall, during steady state the excitation signal stays within one quantum; however, in this case it's oscillating by at least two quantum levels. This oscillation indicates that the system is unstable.

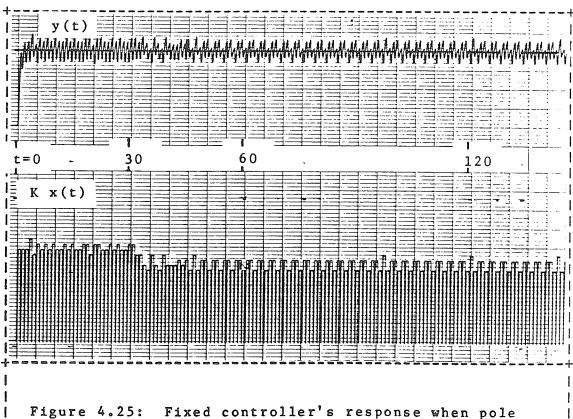


Figure 4.25: Fixed controller's response when pole changes from -2 to -1.75

If the pole location of the plant is changed even more, the advantage of using an adaptive controller becomes obvious. Fig. 4.26 shows the system response of a first order plant with its starting pole at -2 when the adaptive controller is used. Thirty intervals after start-up, the pole location is changed to -1.5. It takes the controller about 140 intervals but eventually the system is back in phase-lock. When the system is in phase-lock the gain used (K=5.31) is just 4% higher than the theoretical critical gain ( $K_c=5.09$ ) for the plant 1/(s+1.5).

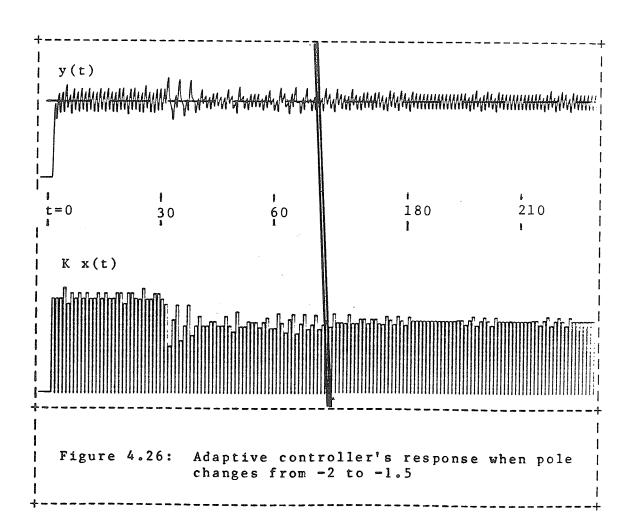
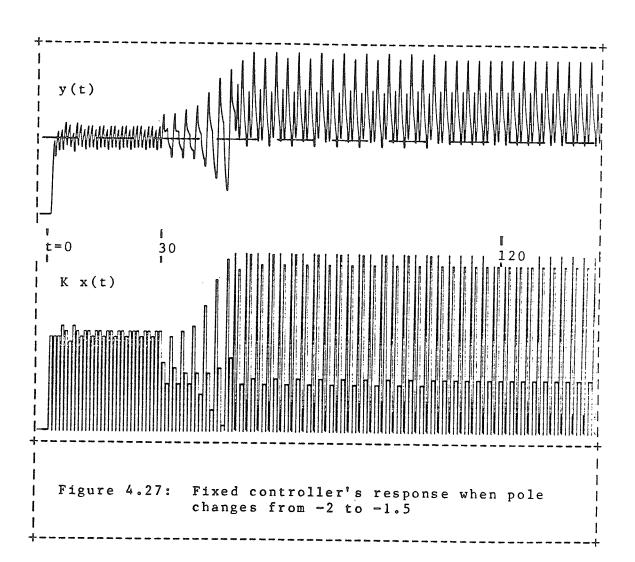


Fig. 4.27 shows the fixed controller's response to the same situation. Immediately after the change in the pole location, the system goes unstable because the gain being used is much to large for the 1/(s+1.5) plant.



## 4.5 PROBLEMS WITH DESIGN

The major cause of the problems with this digital controller is the resolution of the micro-processor system being used. Because of the coarse resolution, some of the methods used and criteria chosen for this design are not optimal, but they are the best under the given circumstances.

The resolution problem is most evident in the adaptability criteria. As was explained in Section 3.3, if the micro-processor system used had better resolution and more computing power, the sensitivity equations developed in Section 3.4.1 could be used to vary the gain. Using these sensitivity relationships would give better results.

Instead, less than optimal criteria have to be used.

These criteria require the following decisions be made.

- 1. The increment by which to increase/decrease the gain by.
- 2. The time between system checks to see if the gain needs to be changed.
- 3. The properties to look for when the system is checked.

For the plants previously discussed, the values used for these three criteria gave superb results. For at least one plant though,  $G(s)=1/[(s+1)^2]$ , these criteria caused the system to fall out-of-lock.

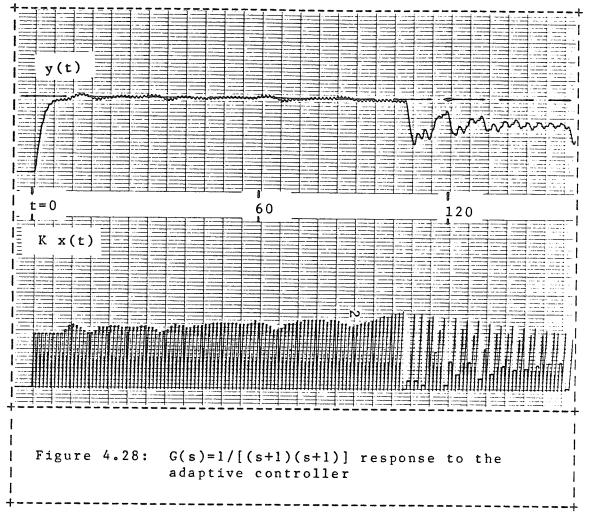
The response and gain variations for the G(s)=1/[(s+1)(s+1)] plant are shown in Figs. 4.28 and 4.29,

respectively. One can see that, after about one hundred intervals, the gain is less than the minimum gain needed for locking. There are a couple of points within these one hundred intervals where it appears that the controller is able to stabilize the gain and improve the plant response. Eventually though, due to the three criteria just mentioned, the gain is too low for the controller to operate properly.

This problem occurs because the adaptive algorithm in this controller is written with the assumption that the system is operating at, or near the critical gain. Usually for this plant, when the controller compares the average plant response value to that of the input value, they are not the same. This means that the system is unstable and the controller reduces the gain.

Eventually, the minimum locking gain is reached. Because the controller cannot distinguish between an unstable response due to a high gain, and a response due to a gain that is less than the minimum locking gain, subsequent gain reductions below the minimum locking gain causes inability of the controller to ever regain phase-lock.

If the time between checks on the system had been longer, the response of this plant would have probably been better. Eighteen intervals after start-up, the system is stable at a high gain (K=2.30), and stays that way for another ten intervals. The controller, trying to induce the system into giving the best response, tries to increase the gain. This



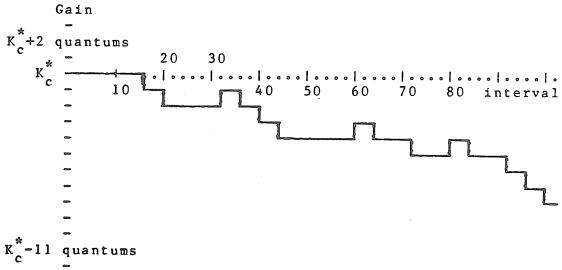


Figure 4.29: G(s)=1/[(s+1)(s+1)] gain variations for above response

causes an oscillation in the system from which the controller recovers, but at a lower gain.

Another attempt at increasing the gain causes another oscillation in the system which is its demise. The controller, trying to correct for the oscillation, decreases the gain too fast until finally, the gain is less than the minimum locking gain. If the controller had given the plant more time to react between gain changes, the system might not have failed.

One solution to the above problem would be to program the controller such that the gain used in the system is not less than the minimum locking gain. For a given plant it would mean evaluating equation (2.5) at  $T=T_0$ . Including this solution into the adaptive controller algorithm would mean the above result would never happen.

Increasing the time between "gain decreases" would also solve the above problem, but would create another. Take, for example, a system that is stable very near the critical gain. The controller increases the gain trying to get a better response, but actually causes the system to go unstable. The gain should be reduced immediately because the longer the gain is held above the critical point, the harder it is for the controller to restabilize the system. For this situation, the time between gain decreases should be small, and not large which is what is suggested by the previous situation.

The limited resolution also causes problems with the critera used for closing the loop. This includes the  $\pm 2$  quantum levels discussed in Chapter 3. By changing this criterion, one risks the possibility of not being able to close the feedback loop if the quantum range is made too small, or closing the loop too early if the range is made too wide. Decreasing the quantum band from  $\pm 2$  would make the system more sensitive to the starting values of gain and IPI used; they would have to converge to the critical values of gain and IPI as the band decreased in size. Alternatively, increasing the band size makes the system less sensitive to the starting values, but would mean that the loop would close too soon creating harmful transients. From the tests performed, the  $\pm 2$  quantum range appears to give the best results.

From the results and problems presented in this chapter, one can see that the adaptive controller, as it is now, produces good system responses for certain plants. The goodness of the response depends mainly on the adaptability criteria which were chosen to give a good response for a range of plant types.

In practice, the controller would be regulating one particular plant, and not several different kinds of plants as it is here. This would solve the problem of deciding what to make the adaptability criteria so that the controller could handle the range of plant types. Instead, because the

plant characteristics would be known, the adaptability criteria could be "fine tuned" to get the optimal response from the plant.

### Chapter V

### CONCLUSIONS AND RECOMMENDATIONS

In this thesis, a digital controller is realized and tested. The initial design is based on an analog controller which uses Integral Pulse Frequency Modulation and Phase-Lock Loop control. By comparing the digital controller and its analog counterpart, it can be concluded that the digital controller works about as well as the analog controller. Improvements are made in this controller design which include the development of a routine that makes the controller adaptable. Also the controller has the ability to start in the open-loop mode and then close the feedback loop at an appropriate time.

In the closed-loop mode, the controller is adaptive in nature, keeping the gain as large as possible. It is shown that maximizing the gain, when the system is in phase-lock, results in the best plant response. It is also shown that if the plant changes, the adaptive controller is able to bring the system back into phase-lock and operate the system very near its critical gain. It is concluded that this reaction by the adaptive controller produces a much better plant response than does the fixed controller.

The transient response is improved by having an open-loop/closed-loop routine in the controller. In the open-loop mode, the control signal is characterized by predeter-mined constants of gain and inter-pulse interval, chosen to be at, or near, their critical values. A new method for finding these critical constants is explained. If this method can be used for the more complex plants, it is concluded that this would be an easier method for finding the critical constants as compared to the old.

There is still a lot of work that can be done on this controller to improve its performance. A case is shown where the adaptive controller is inept at controlling a certain plant due to incorrectly chosen criteria in the adaptation algorithm. Further work in this area might discover the optimal criterion for a given class of plants.

Another line of research that would improve the controller's performance, would investigate the possibility of the controller "analyzing" the consecutive plant responses. Presently, the computer makes a decision on whether to change the gain by checking only one or two points over a certain time interval. A decision is made and carried out depending only on the plant response at these few points. By having the computer examine previous responses over ten intervals, say, could help the controller make a better decision as to whether to increase or decrease the gain, thereby improving the adaptability.

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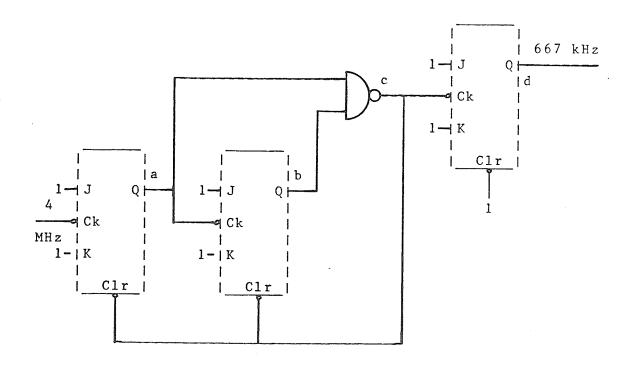
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## Appendix A

### HARDWARE

# Divide-by-Six Circuit

The divide-by-six circuit shown below is used to obtain a 667 kHz signal from the 4 MHz system clock. This 667 kHz clock signal is used to run the A/D converter which can operate at a maximum clock frequency of 800 kHz only.

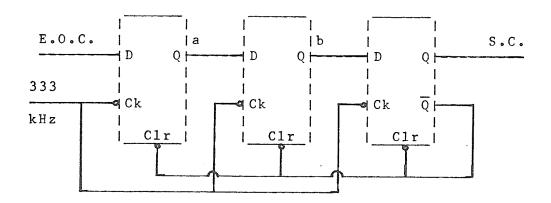


# Divide-by-Six Timing Diagram

4   MHz	           	             	             	 	1 1		       	             	 
a 	     	       		     	       		     	       	
b 		     			     	       		       	       
c						         	· · · · · ·		
d			     			   			

### 3-Stage Shift Register

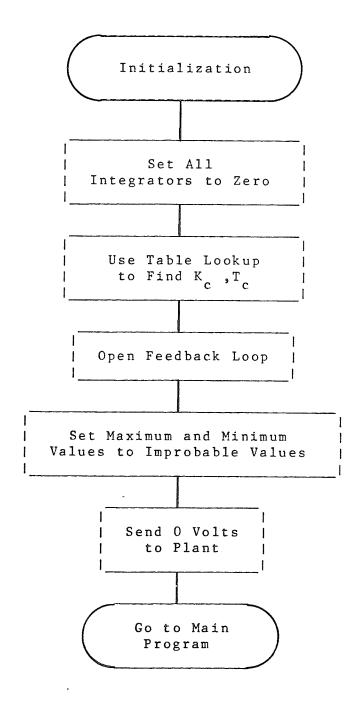
The 3-stage shift register circuit shown below is needed in the continuous A/D conversion mode. According to the A/D converter specifications, after every conversion, the A/D converter requires at least 4 clock cycles to elapse before the start of a new conversion, and so the End Of Conversion pin cannot be directly connected to the Start Conversion pin. Also, according to the specifications, the start conversion pulse must be at least one, but no more than three and one-half, clock periods long. The timing diagram below shows that these criteria are met by this shift register circuit.

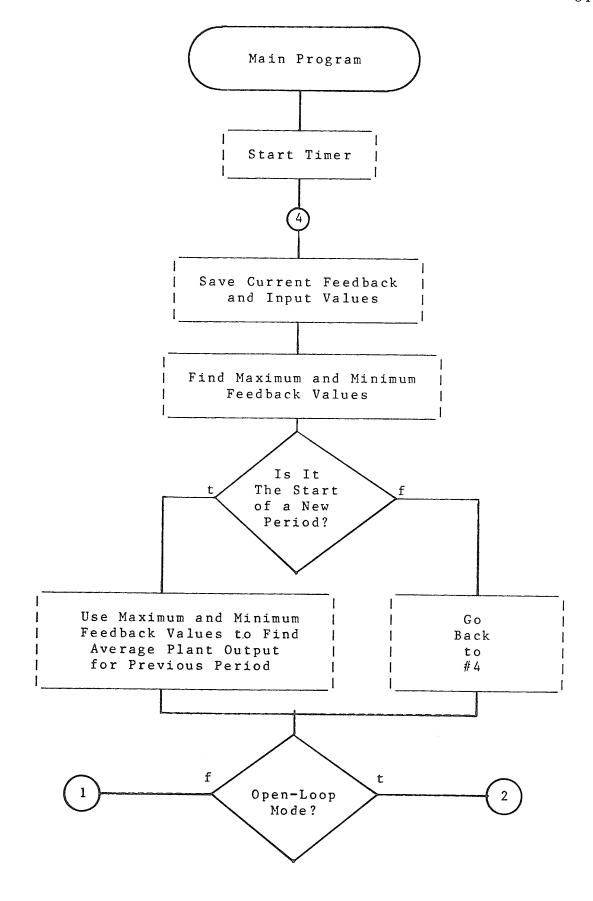


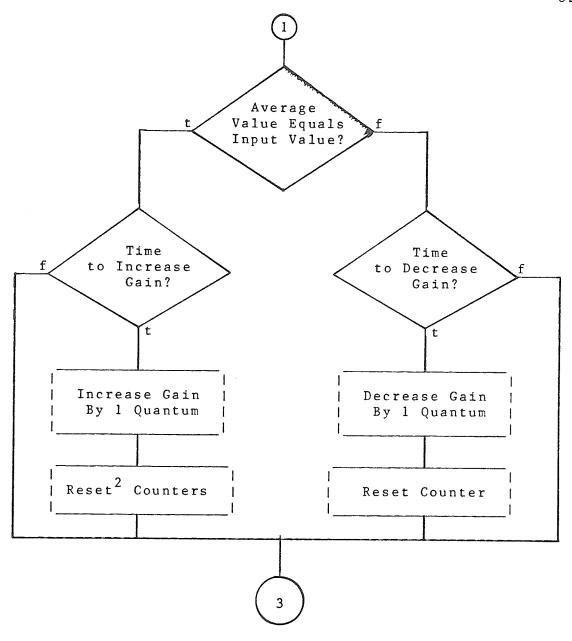
# Shift Register Timing Diagram

667   kHz	-       	1					     	               -	     	-	         
333 kHz	       	       	     	 ! ! -		 ! !	       	-     		-       	   
E.O.C.						     		<b>-</b>		<del>-</del>	*** *** ***
a 	     					-     					<b></b>
ъ 						-     				·	
S.C.					   		· ••• ••• ••	     			

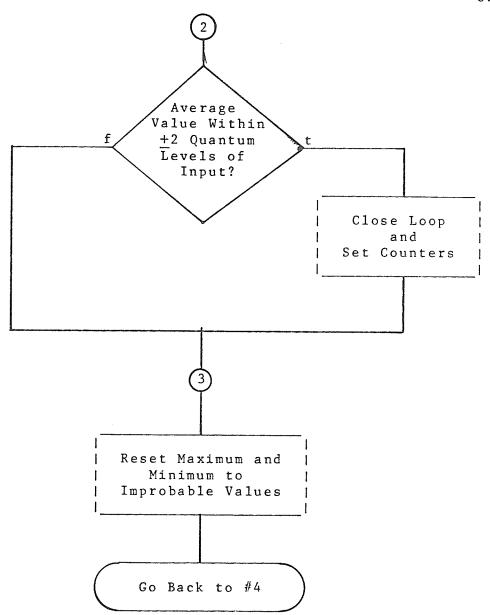
Appendix B
CONTROLLER FLOWCHART

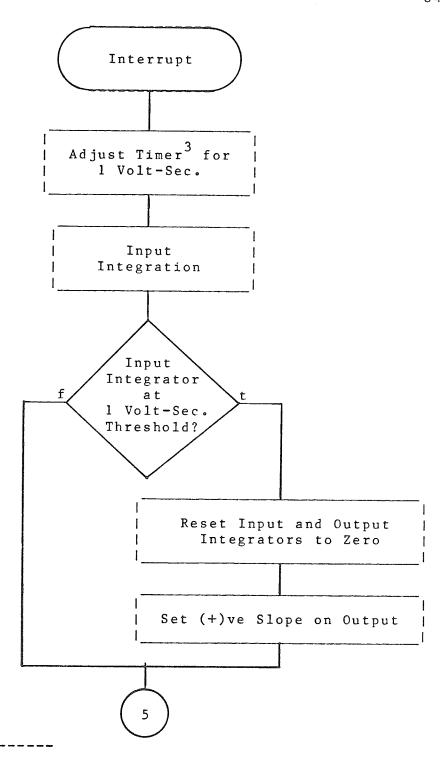




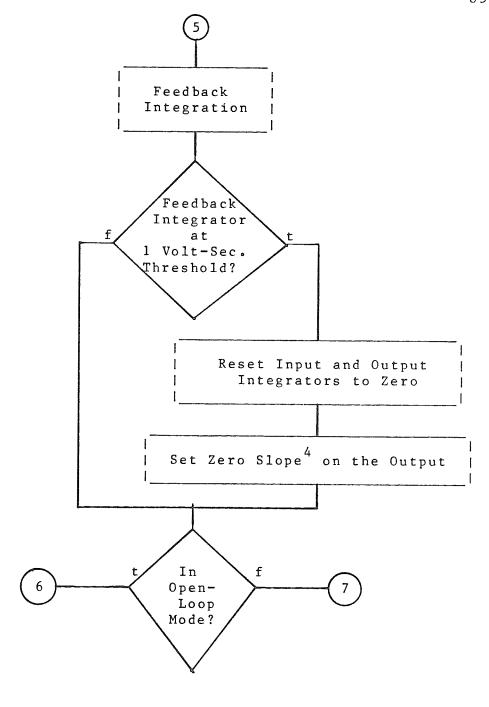


The counters are for the stability checking times referred to in Chapters 3 and 4

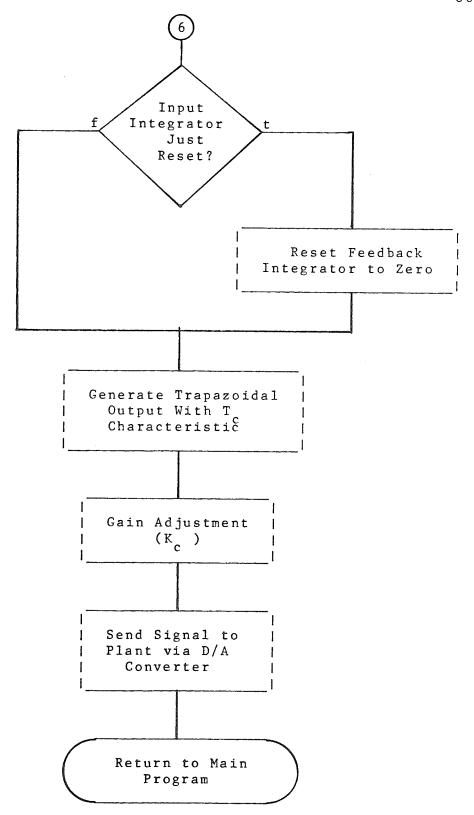


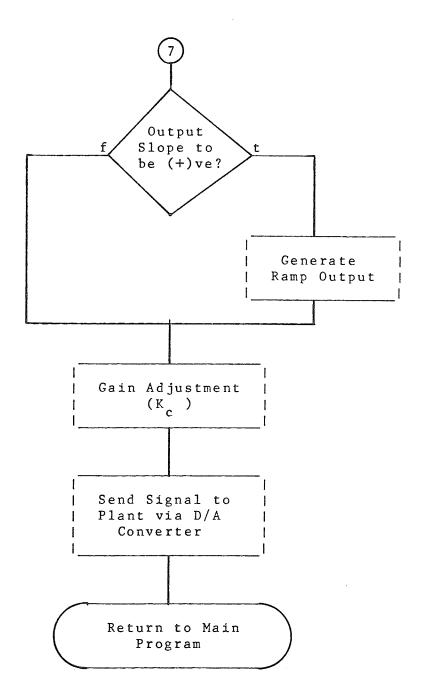


The program is interrupted 256 times a second (T = 1 sec.) or 3.906 msec.. The CTC can be programmed to interrupt either once every 3.846 msec. or 3.974 msec.. Adjusting the timer means alternating the interrupt between the above two times to give an average interrupt time of 3.910 msec. or a period of 1.001 secs..



This step does not affect the output in the open-loop mode.





### Appendix C

## PROGRAM LISTING FOR ADAPTIVE CONTROLLER

Comments

Mem- | Mneum-

```
ory | onics
Loca-
tion |
                     INTERRUPT
'''''' 1 SECOND ADJUSTMENT ''''''''''''''
2100
      8 0
                      ΕX
      3E A5
                      LD A,A5
      D3 84
                      OUT(84),A
      3E 1E
                      LD A, 1E
      В9
                       CP C
                       JR if NON-ZERO to SEC
      20 01
      3 C
                      INC A
      D3 84
                SEC
                      OUT(84),A
      4 F
                      LD C,A
 Input Integral
      D9
                      EXX
      21 80 21
                      LD HL,2180
2112
      11 8A 21
                      LD DE, 218A
      1 A
                      LD A, (DE)
      86
                      ADD A, (HL)
      77
                      LD(HL),A
      3E 00
                      LD A,00
      2 C
                      INC L
      8 E
                      ADC A, (HL)
      77
                      LD(HL),A
      FE 33
                      CP 33
      FA 31 21
                      JP if(-)ve to FBINT
2122
      D9
                      EXX
      57
                      LD D, A
      D9
                      EXX
      97
                      SUB A
      77
                      LD(HL), A
      2 D
                      DEC L
      77
                      LD(HL), A
      2E 85
                      LD L,85
```

```
77
                            LD(HL),A
        2 D
                            DEC L
        77
                            LD(HL),A
        2E 87
                            LD L,87
        4 E
                            LD C,(HL)
                      Feedback Integral
2131
        1 C
                   FBINT
                           INC E
        21 82 21
                           LD HL,2182
        1 A
                            LD A, (DE)
        86
                            ADD A, (HL)
        77
                           LD(HL),A
        3E 00
                           LD A,00
        2 C
                            INC L
        8 E
                           ADC A, (HL)
        77
                           LD(HL),A
        FE 33
                           CP 33
        FA 47 21
                           JP if(-)ve to OINT
2142
        97
                           SUB A
        77
                           LD(HL),A
        2 D
                           DEC L
        77
                           LD(HL),A
        00/4F
                           NOP / LD C, A
                        Output Integral
        97
                   OINT
                           SUB A
        В9
                           CP C
        28 26/10
                           JR if ZERO to CLEAR/PLANT
        3 D
                           DEC A
        В9
                           CP C
        28 OC
                           JR if ZERO to PLANT
        0D/00
                           DEC C / NOP
2150
        1 D
                           DEC E
        2E 84
                           LD L,84
        1 A
                           LD A, (DE)
        86
                           ADD A, (HL)
        77
                           LD(HL),A
        3E 00
                           LD A,00
        2 C
                           INC L
        8 E
                           ADC A, (HL)
        77
                           LD(HL),A
        2E 85
                   PLANT
                           LD L,85
        5 E
                           LD E, (HL)
        2 C
                           INC L
        7 E
                           LD A, (HL)
2160
        CD 60 23
                           CALL MULT
        06 04
                           LD B,04
        CB OC
                   SHFT2
                           RRC H
        1 F
                           RRA
        10 FB
                           DJNZ to SHFT2
        88
                           ADC A, B
       D3 80
                           A, (08) TUO
       08
                           EX
       D9
                           EXX
```

2171		ED 4D		RETI
77 LD(HL), A 2D DEC L 77 LD(HL), A 0D DEC C C3 5B 21 JP to PLANT	2171	2E 83	CLEAR	LD L,83
2D DEC L 77 LD(HL), A 0D DEC C C3 5B 21 JP to PLANT		77		
OD DEC C C3 5B 21 JP to PLANT		2 D		•
OD DEC C C3 5B 21 JP to PLANT		77		LD(HL),A
C3 5B 21 JP to PLANT		OD		•
		C3 5B 21		
	217A	00		
2180 Input Sum	2180			Input Sum
2182 Feedback Sum	2182			
2184 Output Sum	2184			_
2186 K Value	2186	<del></del>		•
2187 T Value	2187	***************************************		
				Present Maximum Value
		-		Present Minimum Value
218A Input Value				
218B Plant Output				-
218C Possible Plant Output		-		<del>-</del>

### TABLE LOOK-UP AND OPENING LOOP ROUTINE FOR GIVEN POLES

```
2190
        l,x
                           CRITICAL
2192
        1,1
                            T AND K
2194
       1,2
                           CONSTANTS PAIRS
       1,3
2196
                           FOR ONE
       1,4
2198
                           POLE
219A
       1,5
                            AT - 1
219C
       1,6
21A0
       91
                   POLE 1 SUB C
       30 02
                           JR if NO CARRY to AHEAD
       ED 44
                           NEG A
       3 D
                   AHEAD
                          DEC A
       07
                          RLCA
       C6 F0
                          ADD A, FO
       18 03
                           JR to SWITCH
       07
                   POLE=1 RLCA
       C6 90
                          ADD A,90
       16 21
                   SWITCH LD D,21
   Table look-up for K and T.
21BO
       5 F
                          LD E, A
       1 A
                          LD A, (DE)
       77
                          LD(HL),A
       2 D
                          DEC L
       7 B
                          LD A,E
       3 C
                          INC A
       00
                          NOP
       5 F
                          LD E,A
       1 A
                          LD A, (DE)
       77
                          LD(HL),A
       DD 21 01 20
                          LD IX,2001
   Opening the loop routine.
       2E 4F
                          LD L,4F
21CO
       36 OD
                          LD(HL), OD
       2E 46
                          LD L,46
       36 00
                          LD(HL),00
       2E 4A
                          LD L,4A
       36 26
                          LD(HL),26
       21 90 22
                          LD HL,2290
       36 92
                          LD(HL),92
       25
                          DEC H
       C3 25 22
21D0
                          JP to MAX
       91
                  POLE=C SUB C
       3 C
                          INC A
       07
                          RLCA
       C6 FA
                          ADD A, FA
       18 D4
                          JR to SWITCH
21DA
       00
                          NOP
21F0
       2,3
                          CRITICAL
21F2
       2 , x
                           T AND K
```

21F4	3,x	CONSTANTS PAIRS
21F6	4 , x	FOR ONE
21F8	5,x	POLE
21FA	1,J2	AT OTHER
21FC	1,J	THAN
21FE	2 , J	AT -1

```
MAIN PROGRAM
                         INIALIZATION
2200
        ED 5E
                           IM 2
        F3
                           DΙ
        00
                           NOP
        11 00 00
                           LD DE,00
        31 8C 21
                           LD SP,218C
        D 5
                           PUSH DE
        D 5
                           PUSH DE
        D5
                           PUSH DE
        D5
                           PUSH DE
        D 5
                           PUSH DE
        D 5
                           PUSH DE
2210
        31 CO 23
                           LD SP,23C0
        FE 01
                           CP 01
        79
                           LD A, C
        00
                           NOP
        21 87 21
                           LD HL,2187
        CA AB 21
                           JP if ZERO to POLE=1
        78
                           LD A, B
        00
                           NOP
        FA D3 21
                           JP if (-) VE to POLE=C
2222
        C3 A0 21
                           JP to POLE 1
        3E 7F
                           LD A,7F
                   MAX
        32 89 21
                           LD(2189), A
        3E 23
                           LD A,H
        ED 47
                           LD I,A
        3E 88
                           LD A,88
2230
        D3 84
                           OUT(84), A
        3E A5
                           LD A, A5
        D3 84
                           OUT(84), A
        3E FF
                           LD A, FF
       D3 9E
                           OUT(9E),A
       D3 9E
                           OUT(9E), A
       D3 9F
                           OUT(9F), A
       D3 9F
                           OUT(9F),A
2240
       D3 82
                           OUT(82),A
        97
                           SUB A
       D3 82
                           OUT(82), A
       D3 80
                           OUT(80),A
       06 01
                           LD B,01
        57
                           LD D, A
       D9
                           EXX
       4 F
                           LD C, A
       D9
                           EXX
224D
       76
                           HALT
       00 00
                           NOP
```

```
INPUT
                                 LOOP
2250
        3E 33
                   INPUT
                           LD A,33
        32 8A 21
                           LD(218A),A
        3E 1F
                           LD A, 1F
        D3 84
                           OUT(84), A
        4 F
                           LD C,A
        2E 8B
                   AGAIN
                           LD L,8B
        DB 9C
                           IN A, (9C)
        EE 7F
                           XOR 7F
2260
        32 8C 21
                           LD(218C),A
        96
                           SUB A, (HL)
        FE 03
                           CP 03
        F2 5A 22
                           JP if (+)ve to AGAIN
        FE FE
                           CP FE
                           JP if (-)ve to AGAIN
        FA 5A 22
        FΒ
                           EI
        3A 8C 21
                           LD A, (218C)
2272
        77
                           LD(HL),A
        2E 88
                           LD L,88
        ΒE
                           CP(HL)
        FA 7A 22
                           JP if (-) VE to MIN
        77
                           LD(HL),A
        2 C
                   MIN
                           INC L
        ΒE
                           CP(HL)
        F2 80 22
                           JP if (+) VE to GAIN
        77
                           LD(HL),A
2280
        97
                           SUB A
                   GAIN
        ВΑ
                           CP D
        CA 5A 22
                           JP if ZERO to AGAIN
        7 E
                           LD A, (HL)
        2 D
                          DEC L
       86
                          ADD A, (HL)
       1 F
                           RRA
        77
                          LD(HL),A
        3A 8A 21
                          LD A, (218A)
       96
                           SUB A, (HL)
       00
                          NOP
       C3 92/C0 22
                          JP to OPEN/CLSD
                      Open-Loop Routine
2292
       FE 03
                   OPEN
                          CP 03
       F2 F0 22
                          JP if (+)ve to DUMP
       FE FE
                          CP FE
       FA FO 22
                          JP if (-)ve to DUMP
229C
       00
                          NOP
       2E 4F
                          LD L,4F
22A1
       36 00
                          LD(HL),00
       2E 46
                          LD L,46
       36 4F
                          LD(HL),4F
       2E 4A
                          LD L,4A
       36 10
                          LD(HL),10
       21 90 22
                          LD HL, 2290
       36 CO
                          LD(HL),CO
```

```
22BO
       25
                         DEC H
       1E 05
                         LD E,05
       C3 DE 22
                          JP to SKIP
22B6
       00 00
                          NOP
                    Closed-Loop Routine
       1 D
22C0
                  CLSD
                          DEC E
       C2 D0 22
                          JP if NON-ZERO to STBL
       87
                         ADD A
       1E 05
                         LD E,05
       CA DO 22
                          JP if ZERO to STBL
       2E 86
                         LD L,86
       35
                          DEC(HL)
22CD
       00 00 00
                          NOP
22D0
       10 3E
                  STBL
                         DJNZ to BEFOR
       87
                          ADD A
       C2 DE 22
                          JP if NON-ZERO to SKIP
       7 E
                          LD A, (HL)
       2 D
                          DEC L
       96
                          SUB A, (HL)
       C2 DE 22
                         JP if NON-ZERO to SKIP
       2 D
                         DEC L
       34
                          INC(HL)
       06 OA
                  SKIP
                         LD B,OA
22E0
       C3 F0 22
                         JP to DUMP
22F0
       2E 86
                  DUMP
                         LD L,86
       7 E
                         LD A, (HL)
       DD 77 00
                         LD(IX),A
       DD 23
                         INC IX
       97
                          SUB A
                  RESET
       57
                         LD D, A
       2E 88
                         LD L,88
       77
                         LD(HL),A
       В8
                          CP B
       C2 02 23
                          JP if NON-ZERO to NEXT
2301
       04
                          INC B
       2 C
                  NEXT
                          INC L
       3E 7F
                          LD A,7F
       77
                          LD(HL),A
       C3 5A 22
                          JP to AGAIN
2308
       00 00
                         NOP
2310
       78
                  BEFOR LD A, B
       3 D
                          DEC A
       C2 FO 22
                          JP if NON-ZERO to DUMP
       7 E
                         LD A, (HL)
       2 D
                         DEC L
       77
                         LD(HL),A
       C3 F0 22
                         JP to DUMP
231B
       00
                         NOP
```

SUBROUTINE MULT				
2360	A7 21 00 00 54	AND A LD HL,00 LD D,H		
	06 08	LD B,08 C ADC HL,HL RLA		
	D2 70 23 3F	JP if NO CARRY to CHECK CCF		
2370	ED 5A 10 F5 CHEC 7D C9	ADC HL, DE CK DJNZ to MULT LD A, L RET		
2374	00 00	NOP		
2387 2388 238A	00	RUPT ROUTINE ADDRESS NOP 2100 NOP		