Co-ordination of Converter Controls and an Analysis of Converter Operating Limits in VSC-HVdc Grids

By

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Abstract

This thesis presents an investigation into the power transmission limitations imposed on a VSC-HVdc converter by ac system strength and ac system impedance characteristics, quantified by the short circuit ratio (SCR). An important result of this study is that the operation of the converter is not only affected by the SCR's magnitude, but is also significantly affected by the ac system's impedance angle at the fundamental frequency. As the ac impedance becomes more resistive, the minimum SCR required at the rectifier side increases from that required for ideally inductive ac impedance, but it decreases at the inverter side. The finite megavolt ampere (MVA) limit of the VSC imposes a further limitation on power transfer, requiring an increase in the value of the minimum SCR. This limitation can be mitigated if additional reactive power support is provided at the point-common-connection.

A state-space VSC model was developed and validated with a fully detailed non-linear EMT model. The model showed that gains of the phased-locked-loop (PLL), particularly at low SCRs greatly affect the operation of the VSC-HVdc converter and that operation at low SCRs below about 1.6 is difficult. The model also shows that the theoretically calculated power-voltage stability limit is not attainable in practice, but can be approached if the PLL gains are reduced.

The thesis shows that as the VSC-HVdc converter is subject to large signal excitation, a good controller design cannot rely on small signal analysis alone. The thesis therefore

proposes the application of optimization tools to coordinate the controls of multiple converters in a dc grid. A new method, the "single converter relaxation method", is proposed and validated. The design procedure of control gains selection using the single converter relaxation method for a multi-converter system is developed. A new method for selecting robust control gains to permit operation over a range of operation conditions is presented. The coordination and interaction of control parameters of multi-terminal VSC are discussed.

Using the SCR information at converter bus, the gain scheduling approach to optimal gains is possible. However, compared to robust control gains setting, this approach is more susceptible to system instability.

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List of Abbreviations

ac	alternating current
CSC	current-source converter
dc	direct current
FACTS	flexible ac transmission systems
GTO	gate turn off
HVdc	high-voltage direct-current
IGBT	insulated-gate bipolar transistor
ISE	integral square error
LCC	line-commutated converter
MMC	modular multilevel converter
MVA	megavolt ampere
PCC	point-of-common-coupling
PI	proportional-integral
PLL	phase-locked loop
pu	per unit
PWM	pulse-width modulation
SCR	short-circuit ratio
SPWM	sinusoidal pulse-width modulation
THD	total harmonic distortion
ESCR	effective short-circuit ratio
VCO	voltage controlled oscillator
VSC	voltage-source converter
XLPE	cross-linked polyethylene

Chapter 1: Introduction

1.1 Background

The process of power generation, transmission, and distribution is undergoing a revolution, in which the amount of small size distributed power generations, such as wind, solar, etc., are significantly increasing. This transition is bringing changes to all aspects of power systems operation, from generation, transmission, distribution to utilization.

Until recently, power generators have usually been high-rating power plants that use fossil fuel, hydro power, or nuclear power. Most generators in such centralized power generation schemes are relatively easily controlled synchronous machines of constant power and constant frequency [1]. Because of energy requirements and concerns about greenhouse gas emissions, there has been significant development worldwide on new types of renewable energy sources, such as wind, solar power generation. Harnessing renewable power sources, particularly those utilizing wind energy, has become a major task for power companies and transmission system operators. The main driving forces for this development have been environmental and legislative [2].

Large offshore wind farms have been developing rapidly all over the world. The European Wind Energy Association estimates that 120 GW of offshore wind power will be installed in the next two decades [3] [4]. The Atlantic Wind Connection (AWC) backbone transmission project will provide approximately 6000 MW of offshore wind capacity, which is enough power to serve approximately 1.9 million households [5]. The

integration of such large amounts of remote offshore wind generation into existing onshore networks creates technical, economic, and environmental challenges for developers and system operators.

Development of High Voltage Direct Current (HVdc) technology has taken place over the past 50 years. HVdc technologies are often categorized by the power electronic switching devices used in the ac to dc converter. Line commutated, current source converter (LCC-CSC) technology has been commercially available since the mid-1950s. It has mainly been used for point-to-point, high-capacity bulk power transmission links over long distances and for interconnection of asynchronous ac grids. However, thyristor-based converters require a synchronous voltage source to operate due to the limited flexibility within the thyristor valve [6], with which the converters stations must consume large amount of reactive power.

Self commutated, voltage source converter (VSC) technology uses more-flexible power electronic devices within the converter (such as those utilizing insulated gate bipolar transistor (IGBT) technology), thereby allowing a more controllable unit. The advantages of VSC technology include the voltage polarity remaining the constant during power reversal which will significantly reduce the stress on the cable. The VSC HVdc also has very flexible control capability which brings the possibility to reliably operate multi-terminal HVdc network. VSCs have been used for many years in motor drives. In the past decade, it has been seen the emergence of the application of VSC in high-voltage power transmission, particular for use with submarine cables, underground cables, and multi-terminal HVdc links [7]. The application of VSCs to HVdc transmission has only been a reality since 1997, when the concept of VSC transmission for medium-power dc

transmission was first implemented. The power levels of VSC technology have increased from a very moderate rating of 3 MW in 1997 (the Hellsjon project), to a rating of 400 MW in 2010 (the TransBay Cable in service), to a rating of 500 MW in 2012 (the Ireland to the UK line). Plans and development work to increase the rating of VSC technology are ongoing [4] [8] [9].

The thyristor valve technology used for the conversion in LCC-HVdc technology can only switch off when the current through it passes zero; hence, it relies on the line voltage for commutation. VSC technology is based on controllable semiconductor switches, which means that the valves can be switched on and off by external low-voltage control signals that are independent of the main current passing through the valve. This difference in operation gives VSC transmission significant advantages over LCC-HVdc since the VSC can function when it is connected to an ac system with a very low short-circuit ratio, or even when it is connected to a passive ac system without any generation or short-circuit power [6].

A significant distortion in the ac voltage waveshape can lead to a commutation failure for an LCC-HVdc scheme, causing a short and a temporary interruption in power flow [10]. Because a VSC is self-commutating, it does not suffer from such commutation failures. Furthermore, the amount of the reactive power consumption for LCC-HVdc is about 50% to 60% of the active power in the normal operation of LCC-HVdc. In contrast, VSC-HVdc can generate or absorb reactive power as required. Moreover, the control of the reactive power of VSC is independent from the control of the active power, subject to overall design limits [7]. Very rapid and versatile reactive power control is available in VSC-HVdc, which can bring significant benefits to the ac network [3].

VSC transmission uses pulse-width modulation (PWM) with a switching frequency of several kilohertz or uses the valve acting as a controllable voltage source to synthesize a sinusoidal voltage on the ac side. Therefore, harmonic distortion of the ac-side voltage is lower and fewer auxiliary filters are required than are required by LCC-HVdc [10]. This smaller footprint installation technology is suitable for installation on an offshore platform, for example. In conventional thyristor based transmission systems, power reversal is always associated with changing the polarity of the DC voltage. Transient phenomena in the cable requires special design measures and higher insulation capability. A VSC system instead cannot change voltage polarity and power reversal can be accomplished by keeping the same voltage polarity. This enables the use of cross-linked polyethylene (XLPE) cables without the problems imposed by trapped space and surface charges [7].

The major drawback of VSC technology is the high converter loss, which is caused mainly by switching losses that depend on the switching frequency of the semiconductor devices [7]. Also, a VSC has diodes connected in anti-parallel to the insulated gate bipolar transistors (IGBTs) to ensure current capability in the reverse direction. In the event of a fault on an overhead dc line the VSCs at both ends must be disconnected by opening the ac circuit breakers and enabling the arc to extinguish. DC breakers must be used to isolate the faulted dc link from the rest of system [6]. In such a circumstance, an LCC-HVdc converter would suffer a shorter interruption because the valves can automatically block to stop the direct current flow and extinguish the arc without opening the breakers.

1.2 DC Grids

The planning and development of a transmission system is usually driven by the demand of power in the system. Typical HVdc transmission systems have been used for the interconnection of asynchronous ac networks, long cable links connecting offshore wind farms to shore, the connection of remote islanded loads, and the strengthening of existing ac networks [11]. These purposes can be achieved by a corresponding number of individual point-to-point HVdc links, which could be interconnected via ac nodes; however, this approach requires a large number of HVdc converter stations. This is feasible, but it is not necessarily the most beneficial approach due to the construction and maintenance costs of the converter stations, especially when they are located offshore. Reducing the number of converter stations makes interconnection through a multi-terminal dc system attractive [12].

The concept of developing a multi-terminal HVdc (MTDC) grid or a dc grid has re-emerged in recent years due to the increasing presence of renewable energy generation and the need for alternative power routes [13] [14] [15] [16]. A dc grid might be an attractive solution for the grid integration problem in the near future [17] [18]. Unlike ac transmission, HVdc transmission is not hampered by large inductive reactive power in long overhead lines or large capacitive reactive power in submarine or underground cables. A dc grid consists of several HVdc converters connected by a dc network with a meshed, radial, or ring structure. DC grids consisting of VSC only, of LCC only, and of both types of converters (a hybrid dc grid) have been suggested and studied in the literature [19]. VSC-based dc grids have been investigated the most because of the advantages of VSC technology. Hybrid dc grids have gained little attention, but that

technology will become important for the integration of already-existing point-to-point HVdc connections of both types into the dc grid [20] [21].

Generation based on renewable energy has a rapidly varying output, which requires complete control of the real power flows to the main ac grid as well as reactive power control at the transmission terminals. It also requires asynchronous interconnections between the main ac grids for security of supply and for power export. These challenges can be solved by FACTS, LCC-based HVdc systems, and VSC-based HVdc systems [22] [23]. VSC-based multi-terminal HVdc systems have great potential for harvesting wind power because they are fully controllable [4]. They can transmit power in spite of the generator frequency deviations. This advantage can solve the problem of wind generators running at non-uniform speeds. For the integration of large offshore wind farms it has been determined that a VSC scheme is superior to an LCC scheme [24] [25]. Moreover, a self-commutated converter, such as voltage sourced converter (VSC), permits integration into a weak ac system, and such a converter can change power flow direction by simply changing current direction instead of by changing voltage polarity. Unlike conventional HVdc converters, VSC-based HVdc converters can operate at very low power, even at zero power. The active power and reactive power are controlled independently, and at zero active power the full range of reactive power can be utilized. Due to the recent development of IGBT technology and the increased ratings and reduced losses of VSC valves, VSC-based multi-terminal HVdc has gained more and more attention [26] [27] [28].

The operation of a VSC-based Multi-Terminal Direct Current (MTDC) system requires its common dc link voltage to be maintained at the set value with limited variations.

Active power flow among the multi-generation and transmission terminals must be balanced under all conditions. DC overvoltage could cause damage to the converter equipment and dc cables, whereas dc under-voltage could result in the loss of converter control capability [28]. Thus, the main task for controlling a dc grid connected to offshore wind farms is to control the dc voltage to ensure that the collected energy from wind farms is transmitted to the onshore grid networks according to predefined power dispatch criteria. In a dc grid, power can be balanced instantaneously by the use of dc voltage droop control, which can be seen as the ability of a dc grid system to compensate power imbalances in the dc grid at the cost of dc bus voltage deviations. This is analogous to the frequency droop control used in ac grids [6] [19] [30] [31] .

Due to the rapid increase in the current and voltage ratings of IGBTs, utilization of VSC technology for HVdc transmission has attracted significant attention, and the advantages of VSC-HVdc technology compared to LCC-HVdc technology have made dc grids using VSC-HVdc possible.

In this thesis the term multi-terminal HVdc (MTDC) is used. This configuration is also referred to as dc grid. The research detailed in this thesis focuses on VSC-based dc grids. The main research objectives of this thesis were to determine how the ac system strength and impedance characteristics affect VSC-HVdc transmission and to determine how to set the control gains for multi-terminal VSC-HVdc converters.

1.3 Research Objectives

It is well-known that an LCC-HVdc converter has difficulty operating into a weak ac system, whereas the performance of a VSC-HVdc converter is relatively unaffected by system strength (which allows VSC-HVdc converters to be connected to very weak ac systems) [10]. It is also well-known that an LCC-HVdc transmission system requires a large amount of reactive power compensation at the converter ac bus terminal, whereas a VSC-HVdc system can operate capacitively or inductively in the inverter mode and in the rectifier mode, and therefore generally does not require additional reactive power compensation [10]. Research regarding the limitations that ac systems impose on VSC transmission has mainly focused on ac system strength; the effects of ac system impedance characteristics on VSC transmission have largely been ignored [32] [33] [34].

One of the purposes of this research is to investigate the minimum ac system SCR required for the VSC to transfer rated real power under different ac system strengths and under different impedance angles. When the finite MVA rating limit and voltage rating limit of the VSC is considered, an even higher minimum ac system SCR may be required because the VSC may not be able to provide the reactive power required. The research used analytical and simulation methods to investigate these issues.

When multi-terminal VSC-HVdc (dc grid) is used to harvest large-scale wind energy, a particularly difficult problem is to coordinate control systems among the many terminals. It is known that VSC-HVdc control can be faster, but it is also known that it is much more complicated compared to conventional HVdc control. Besides choosing proper control parameters for the individual VSC converters, the controllers at the different

terminals may need to be coordinated in order to obtain good performance of the overall systems. It is important to achieve good coordination among the multiple controllers, but it is difficult due to the complexity of each individual controller and the interactions between multiple controllers.

Optimizing the control system in nonlinear systems such as power systems is mainly achieved by trial and error. This approach may work when the number of parameters is not great [35]; however, this process requires a significant level of technical experience in the area, which most engineers may not have. There has been no systematic approach to choosing the control parameters in these types of nonlinear systems until recent years when optimization-oriented electromagnetic transient (EMT) simulation methodologies were developed [35]. The research on optimization-based EMT simulation was pioneered by the University of Manitoba and the knowledge gained has been successfully implemented in the commercial software PSCAD/EMTDC. However, it is still very challenging to apply this optimization method to multi-terminal VSC-based HVdc. There are at least two fundamental problems that need to be answered before the optimization method can be successfully used in designing multi-terminal VSC-based HVdc systems. The first problem is that, although the optimization method is successfully used in the design of some control systems, it has never been used to optimize more than one controller at a time. It is not known whether this method can be used to design the controls for a multi-terminal HVdc system. The second problem is that the simulation time required may be very long. VSC-based HVdc converters are normally operated by Pulse Width Modulation (PWM) controls, a process which requires a very small time step. Also, the size of the circuit could be large, as multi terminals are modeled in the system.

The multi-run for the optimization of such a simulation case would be very time-consuming and could even be impossible due to the time required. It is necessary to determine if there are any methodologies and procedures that can be used to reduce the computational time in the optimization process.

The purpose of the research discussed in this thesis was to investigate how to coordinate the controls of multi-HVdc converters in a VSC-based multi-terminal HVdc grid. The coupling mechanism among the controls of the multi-terminal converters was studied. The optimization methodology was used to design the multiple controllers. A guideline for the design of a coordinative optimal control in a VSC-HVdc grid was proposed.

A phase-locked-loop (PLL) is typically used for angle reference generation for both LCC-HVdc and VSC-HVdc transmission applications [36] [37]. However, for VSC-HVdc transmission the SCR of the connected ac system may be very low and a fast (i.e., high gain) PLL will have an adverse affect on system performance. A state-space VSC model was developed and validated with the non-linear EMT model. The relationship between the ac system SCR and the gains of the PLL were investigated to demonstrate the impact of PLL parameters on the behavior of the VSC HVdc system.

It has been demonstrated that the strength of an ac system has significant impacts on the behavior of the VSC-HVdc systems connected to it. The control of the VSC-HVdc system can be designed or adjusted to have optimal performance for ac systems with different strengths. Knowing the strength of the ac system at the converter bus provides very useful information for the operation of the VSC HVdc system [38]. One effort of

this thesis was to conduct an online control gains scheduling by using the SCR information at the converter ac bus.

1.4 Organization of this Thesis

This thesis investigates the limits of the VSC transmission imposed by ac system strength and impedance characteristics. It also investigates the application of optimization tools to coordinate the controls of a multi-terminal VSC-HVdc system in a power network used for harvesting wide area renewable energy generation.

Chapter 1 provides an introduction to the technology and an introduction to the topics of the thesis.

Chapter 2 provides an overview of VSC transmission operating principles and converter power capabilities as the background theory for the research topic. The methods used to determine sinusoidal ac voltage are given. This chapter describes the main components of VSC-based HVdc. The averaged and two-level valve bridge models are described in detail; these two models will be used and compared in this research. This chapter also reviews the theory of VSC-based HVdc. The synchronously rotating two-axis (d-q) reference frame control, which allows fully independent control of both the active power flow and the reactive power flow of the VSC system are introduced.

Chapter 3 investigates the limitations that ac systems impose on VSC transmission. An analytical model is used to quantitatively analyze the minimum ac system SCR required for the VSC to transfer real power under different ac system impedance angles. When the finite MVA rating limit and the voltage rating limit of the VSC are considered, a higher

minimum ac system SCR is required because the VSC may not be able to provide the reactive power required. This study also shows that if additional reactive power support is made available at the point-common-connection (PCC) the finite MVA limit of the VSC can be mitigated and the VSC is be able to operate into lower SCR ac system. The important impact of PLL gains on VSC control when it connects to a weak ac system is also investigated. A state-space VSC model was developed and validated with the non-linear EMT model. The analysis shows electromagnetic transient simulation must be used to determine whether the gains calculated with small signal analysis are compatible with the large signal behaviour before selecting the final gains. The model also shows that the PLL gains, particularly at low SCR values greatly affect the operation of the VSC-HVdc converter.

Chapter 4 focuses on the development of the improved simulation-based optimization methods for the design of dc grid control parameters. It reviews optimization-enabled electromagnetic transient simulation (OE-EMTS) and the inclusion of robustness in it. The relaxation optimization method for multiple converters control gains design is introduced. A six-terminal VSC-HVdc testing case for parameter selection and optimization are presented with the relaxation optimization methods. Using the relaxation method, the control variables are reduced to one converter and utilization of optimization algorithms are possible for control gains selection. However, the whole system optimization process takes too long and computation time required is not practical. In order to reduce the computation time, using the averaged valve bridge model for control parameters optimization is proposed. The detailed valve bridge model is then used to evaluate the parameters selected.

In Chapter 5, the single converter optimization and the robust single converter optimization for the overall performance on a range of operating points are introduced. The procedure and method of single converter optimization and of robust single converter optimization are validated using examples. A six-terminal VSC-HVdc testing case for parameter selection and optimization is presented with the single converter optimization methods. The control interactions of the optimization methods are investigated and recommendations given.

Chapter 6 introduces the off-line SCR estimation method that uses the breaker and line status and the on-line SCR estimation method using converter busbar voltage and current information. By using the gain scheduling approach to optimal gains for dc grid converters, the converter controller gains can be adjusted from the look-up table based on the SCR information. The robust control gains setting approach and the gain scheduling approach are compared and discussed. The objective of this chapter is to provide a new approach to control the VSC HVdc converter based on additional information from the SCR estimation.

Chapter 7 provides a summary of the research, lists the contributions, and discusses possible future research.

Chapter 2: VSC Transmission and Control of a VSC-HVdc System

2.1 Basic Operating Principles of VSC Transmission

A typical topology of a voltage source converter (VSC) showing its significant component parts is shown in Figure 2-1. In a point-to-point transmission scheme, the other half of the scheme would be a mirror image from about the midpoint of the dc link. The dc link may be a cable or an overhead line. The direction of the real power P and reactive power Q are as shown in Figure 2-1. A positive P means that real power flows from the converter into the ac network (inverter operation). A positive Q means that the converter has a leading power factor.

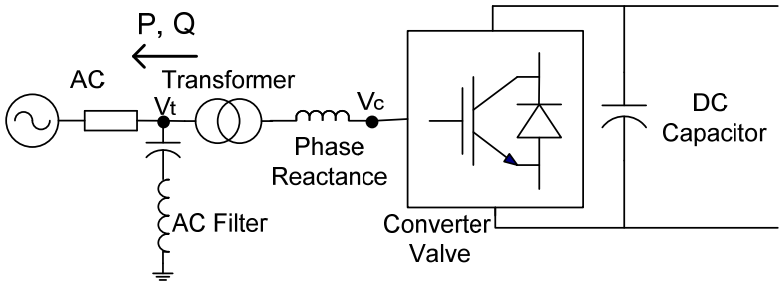


Figure 2-1: A typical configuration of a VSC converter terminal

The phase shift between the ac source fundamental voltages V_t and converter ac bus voltage V_c of both sides of the transformer and the phase reactance is mainly responsible for the active power flow, and the magnitude of V_c relative to V_t is mainly responsible for the reactive power flow. The magnitude and phase angle of converter output ac voltage V_c is controlled by the VSC-HVdc control system. The maximum fundamental frequency

voltage generated by the converter depends on the dc voltage. If the resistance of the transformer is ignored, the active power and reactive power are defined as (with the directions of power flow as in Fig. 2-1):

$$P = \frac{V_t \cdot V_c}{X} \sin \delta \qquad 2\text{-}1$$

$$Q = \frac{V_t (V_t - V_c \cos \delta)}{X} \qquad 2\text{-}2$$

where: δ = the phase angle between the fundamental voltages of V_t and V_c

V_t fundamental voltage at the source side

V_c fundamental voltage at the converter ac side

X = inductance of the transformer and the phase reactor

The direct current of the converter I_d can also be derived from the equality of power on the ac and dc sides:

$$I_d = \frac{\sqrt{6}}{\pi} \frac{V_t}{X} \sin \delta \qquad 2\text{-}3$$

2.2 Active and Reactive Power Capability

The VSC-HVdc converter can be operated as either an inverter, injecting real power into the ac system, or as a rectifier, absorbing power from the ac system. Both the rectifier and the inverter can be operated either capacitively, injecting reactive power into the ac system, or inductively, absorbing reactive power from the ac system. A simplified theoretical PQ diagram of a VSC-HVdc system at minimum (U_{min}) and maximum (U_{max}) ac system voltage is shown in Figure 2-2 [6]. The PQ diagram shows that the VA

capability of the VSC depends on the ac system voltage V_c. The increased reactive power output requires an increase of V_c and, correspondingly, an increase of dc voltage. Therefore, the interface transformer ratio can be used to optimize the PQ characteristic and steady-state power capability of the converter using an on-load tap changer. An additional benefit of a tap changer is that it can minimize the power losses of the VSC-HVdc transmission system. The Q limitation line indicates how the maximum dc voltage on the storage capacitor would impose a limit to the available capacitive output. The P design line corresponds to the designed rated power of the VSC.

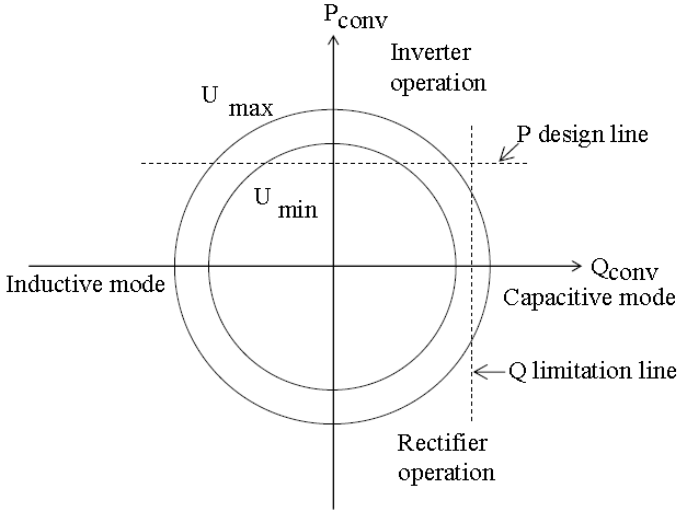


Figure 2-2: A basic simplified theoretical PQ diagram [6]

However, the actual PQ diagram provided by suppliers would be limited by the converter station ratings based on maximum currents and voltages. The reactive power capability is dependent on individual scheme parameters such as the ratio of ac voltage to dc voltage, the ac system fault level, the reactive power demand, etc. A typical VSC-HVdc PQ diagram is shown in Figure 2-3 as the solid curve, which illustrates that the ac system to which the converter is connected, will also have an impact on the converter var supply capability [39]. As the converter supplies (capacitive) or absorbs (inductive) vars from

the ac system the converter local ac bus voltage will change. For a very strong ac system (a high SCR) the change in local converter bus voltage will be negligible, but for ac connections with finite SCRs the change in ac bus voltage will reflect onto the converter valve winding, impacting the converter current limit in the inductive region and the converter voltage limit in the capacitive region, as shown by the dashed curve in Figure 2-3.

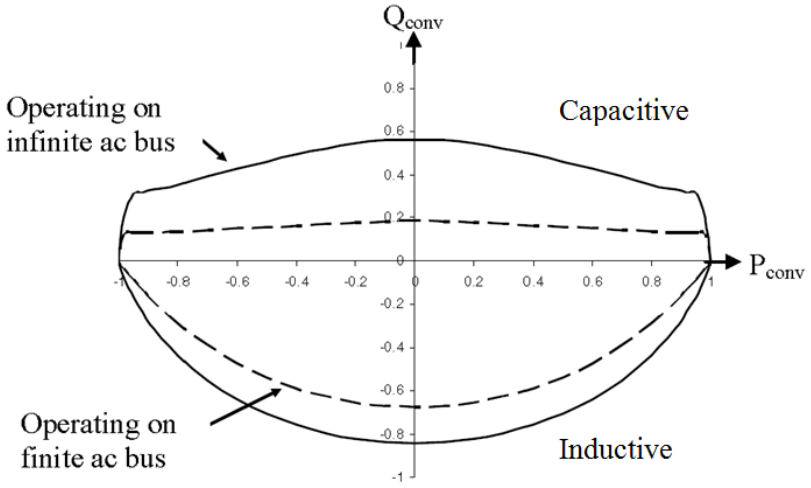


Figure 2-3: Comparison of a VSC converter operating against an infinite bus and a finite bus

2.3 Methods to Obtain Sinusoidal AC Voltages

As indicated above, the magnitude and phase angle of converter output ac voltage V_c is controlled by the VSC-HVdc control system. VSCs employ specialized control methods to generate sinusoidal ac waveforms. Typically, the approach is to eliminate low-order harmonics in the ac voltage waveform. Sinusoidal Pulse Width Modulation (SPWM) is one popular control method for reducing undesirable low-frequency harmonics [40]. Alternatively, specialized converter topologies that intrinsically create nearly-sinusoidal waveforms may also be used. The modular multilevel converter (MMC) is one such

topology [41] [42]. In this section, two converter topologies are discussed: two-level converter in which VSC valves act as a switch, and MMC in which VSC valves act as the controllable voltage source.

However the main focus of this thesis is to investigate the system level behavior between the VSC converter and the ac system, such as the VSC's maximum power transfer capability, optimal gain settings, etc. As long as the converter produces nearly-sinusoidal waveforms at the ac side (or waveforms with very small amounts of low-order harmonics) the type of converter does not make a big difference to the system level behavior. Hence, in this research the two-level converter and its averaged model have generally been used.

2.3.1 Sinusoidal Pulse Width Modulation

A two-level converter shown in Figure 2-7 is the simplest converter topology that can be used in a VSC system. The converter is typically controlled through sinusoidal PWM (SPWM), and the harmonics are directly associated with the switching frequency of each converter leg. Figure 2-4 presents the basic waveforms associated with SPWM and the line-to-neutral voltage waveform of the two-level converter [34].

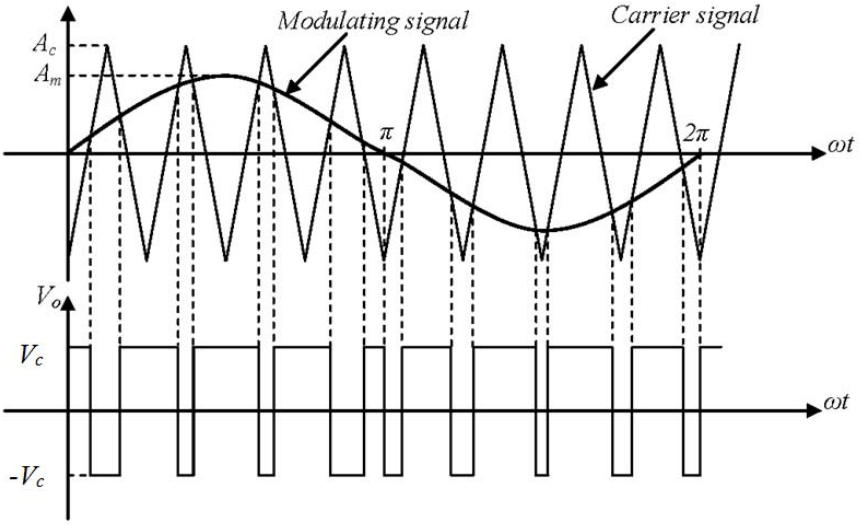


Figure 2-4: Bipolar SPWM waveforms

In order to generate the desired signal V_c, a high-frequency triangular *Carrier signal* is compared to a sinusoidal reference of the desired signal, the *Modulating signal*. The intersection of the two signals determines the switching instants. The square waveform in Figure 2-4 is the converter output voltage V_c, which consists of the fundamental component; and the high-frequency harmonic components depending on the carrier saw wave frequency. The high-frequency harmonic components can be prevented from appearing on the ac system by adding a high-pass filter.

When the modulating signal is a sinusoid of the amplitude of A_m and the peak of the triangular carrier signal is A_c, the ratio $m = A_m / A_c$ is known as the modulation index. The value m is normally in the range between *0* and *1*, so that the output voltage V_c does not contain the higher harmonic contents at lower frequencies. Over-modulation ($m > 1.0$) is possible, but will cause higher harmonic content at lower frequencies, which would degrade the quality of the voltage. Hence it is generally avoided. Another reason to avoid over-modulation [43] is because in the VSC converter, all valves consist of an IGBT

transistor with an anti-parallel diode. The diode automatically turns on if the peak of the ac bus voltage V_c exceeds the dc voltage (i.e. when $m > 1.0$), thereby resulting in uncontrolled conduction.

The fundamental frequency component of the converter output voltage is:

$$V_c(t) = m \cdot \frac{V_{dc}}{2} \sin(\omega t + \delta) \qquad 2\text{-}4$$

where: δ is the V_c phase angle relative to ac voltage V_t

V_{dc} is the dc voltage between the positive pole and the negative pole

ω is the fundamental angular frequency

By controlling the modulation index *m*, the amplitude of the applied output voltage can be controlled. Therefore, the reactive power output of the converter can be controlled. By controlling the modulating signal phase angle δ, the real power output of the converter can be controlled.

2.3.2 Modular Multilevel Converter

The recent introduction of a new topology, modular multilevel converter (MMC), is a major step forward in VSC converter technology for HVdc transmission. The converter arms act as a controllable voltage source with a large number of possible discrete voltage steps, which allows the formation of an approximate sine wave in terms of the adjustable magnitude of the voltage to the ac terminal. This principle is shown in Figure 2-5 [44].

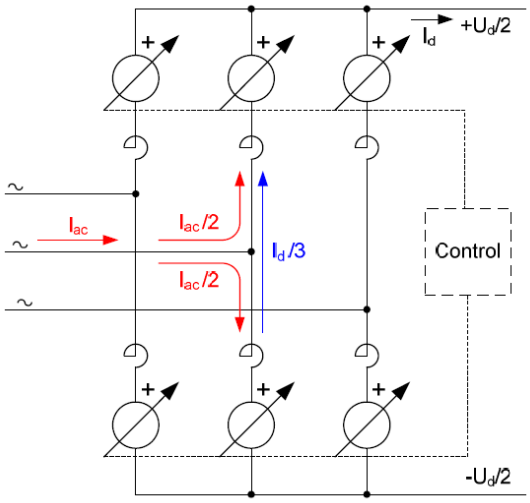


Figure 2-5: Converter in modular multilevel and its control principle [44]

Each of these variable voltage sources is designed with a number of identical but individually controllable sub-modules. Each sub-module is a two-terminal component that can be switched between a state with full module voltage and a state with zero module voltage in both current directions. In addition to auxiliary components and electronics, each sub-module consists of an insulated gate bipolar transistor (IGBT) half-bridge and a capacitor unit. Depending on the current direction, the capacitor can be charged or discharged. The main circuit arrangement is outlined in Figure 2-6. It is possible to individually and selectively control each of the individual sub-modules in a converter arm. The total voltage of the two converter arms in one phase unit equals the dc voltage; by adjusting the ratio of the converter arm voltages in one phase module, the desired sinusoidal voltage at the ac terminal can be achieved [44].

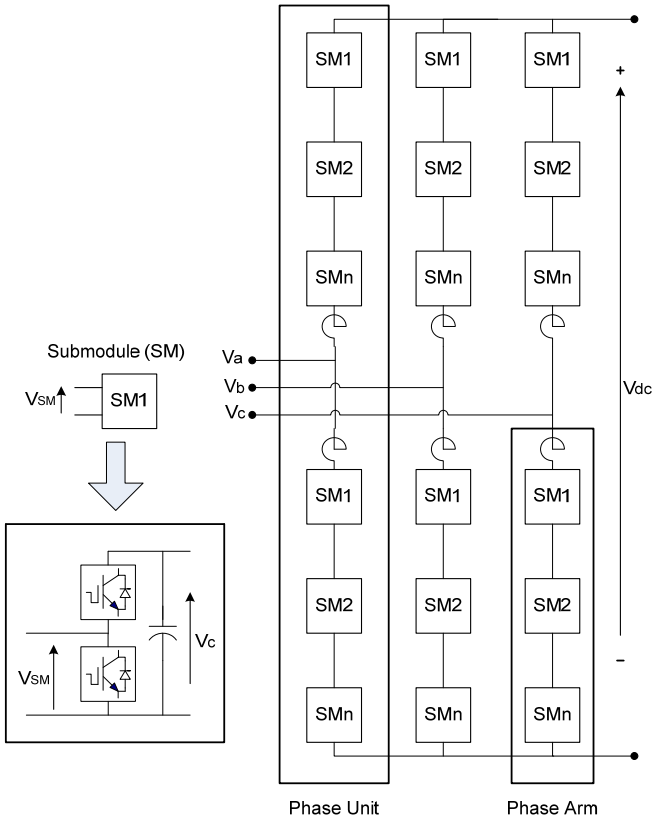


Figure 2-6: Main circuit of a modular multilevel converter

2.4 Main Components of a VSC System

The main function of the VSC-HVdc is to transmit constant dc power from the rectifier to the inverter. As shown in Figure 2-1, the main components of a VSC terminal comprise an interface transformer, a phase reactor, an ac filter, a valve bridge including a dc capacitor, and a dc cable [6].

2.4.1 Interface Transformer and Phase Reactor

The converters are normally connected to the ac system via transformers. The function of the transformers is to transform the voltage of the ac system to a value suitable to the converter and to provide electrical isolation between ac and dc sides. The transformer can

be an ordinary single-phase or three-phase transformer. The leakage impedance of the transformers is usually in the range of *0.1-0.2* pu based on the MVA rating of the transformer.

The converter reactor is one of the key components in a voltage source converter that permits continuous and independent control of active and reactive power. The main purposes of the converter reactor are to provide low-pass filtering of the PWM pattern to give the desired fundamental frequency voltage, to provide active and reactive power control (because the fundamental frequency voltage across the reactor defines the power flow [both active and reactive] between the ac and dc sides), and to limit the short-circuit currents. The short-circuit voltage (impedance voltage) of the converter reactor is typically *15%* of the rated dc power and rated ac voltage on the converter side.

2.4.2 AC Filter

Voltage sourced converters can be operated with different control schemes, most of which use pulse width modulation (PWM) to control the ratio between the fundamental frequency voltage on the dc side and the ac side. The voltage at the ac side converter terminal contains harmonic components resulting from the switching of the valve bridge. These harmonics have to be prevented from entering into the connected ac system. Depending on the filter performance requirements, the filter configuration may vary between schemes, but a typical filter size is somewhere between *10* to *30%* of the rated dc power. For MMC type VSC, since the high number of modules allows the construction of a stepped approximation to a sine wave, with a very large number of steps. It can be shown [41] that with only 40 levels, the total harmonic distortion (THD) can be

reduced below 3% with each individual harmonic below 1%. This is a typical requirement for most HVdc schemes; hence, ac filters can be omitted in many cases [44].

2.4.3 DC Capacitor

The objectives of the valve-side dc capacitor are to provide a low-inductance path for the turned-off current and to serve as energy storage. The capacitance will have a direct impact on dc-side ripple levels and on converter dynamic performance. In addition to stabilizing the dc voltage, the capacitor is also capable of filtering high-frequency current harmonics. Disturbances in the system will cause dc voltage variations. The ability to limit these voltage variations depends on the size of the dc side capacitor.

The dc capacitor size C_{dc} can be characterized as a time constant τ, defined as the ratio between the stored energy at the rated dc voltage V_{dc} and the nominal apparent power of converter S_{dc} as in equation (2-5). The time constant τ is typically selected to be less than 5 ms to satisfy small ripple and small transient overvoltage on the dc capacitor [45].

$$\tau = \frac{C_{dc} \cdot V_{dc}^{\ 2}}{2S_{dc}} \qquad \textbf{2-5}$$

2.4.4 Valve

A two-level phase unit is the simplest switching arrangement capable of producing ac output from a dc source in the form of a simple square-wave, and the two-level bridge is the most simple circuit configuration that can be used for building up a three-phase forced commutated VSC bridge. Several circuit topologies with varying levels of complexity exist for VSCs. Multi-level topologies generally generate voltage waveforms

of higher quality (e.g., improved harmonic spectrum) with fewer switching events, and hence, less switching losses. However, this is achieved at the expense of converter cost and control system complexity [6].

The two-level bridge can also be modelled using its averaged model [46]. The two-level IGBT and the averaged valve bridge models are shown in Figure 2-7. The valve bridge using the averaged model consists of one controlled ac voltage source on the ac side and one controlled dc current source on the dc side.

Using sinusoidal pulse width modulation (SPWM) control, the modulating signal in equation 2-4 can be represented as

$$m(t) = A_m \sin(\omega t + \delta) \qquad 2\text{-}6$$

By specifying the parameters A_m, ω, and δ in the modulating signal, the magnitude, frequency, and phase of $V(t)$ are controlled independently.

When the modulating signals to the three phases are $m_a(t)$, $m_b(t)$, and $m_c(t)$ and the ac currents are $i_a(t)$, $i_b(t)$, and $i_c(t)$, then the dc side current $i_{dc}(t)$ is

$$i_{dc}(t) = 0.5\frac{m_a(t)i_a(t) + m_b(t)i_b(t) + m_c(t)i_c(t)}{V_{tri}} \qquad 2\text{-}7$$

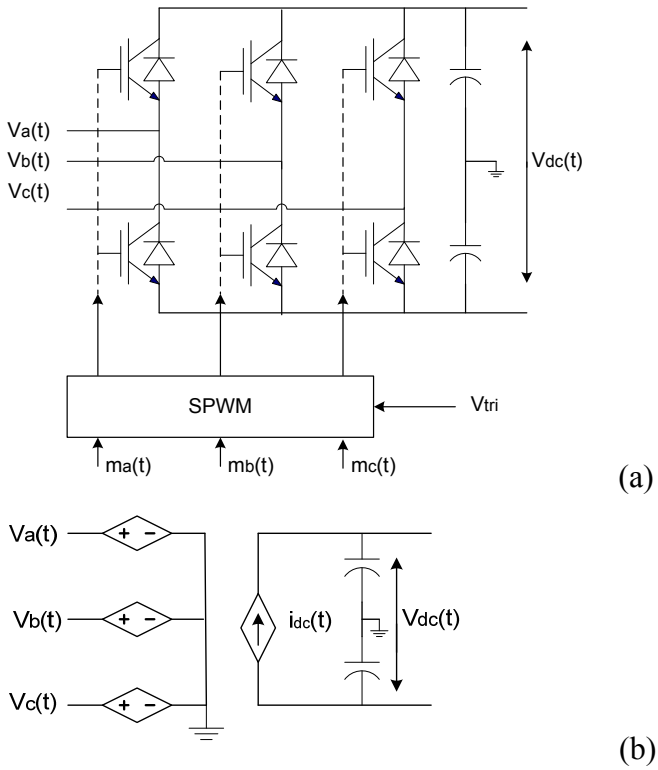


Figure 2-7: (a) Two-level IGBT valve bridge; (b) Averaged model of the valve bridge

Equation 2-7 is based on the assumption that the active power on the ac side is equal to the active power transmitted from the dc side at steady state with losses ignored. However, the switching losses cannot be ignored in the averaged model and the calculated dc current must be adjusted to consider the switching losses. In order to consider the losses in the dc current calculation, we assume the losses of a converter are a percentage of the converter rating at *loss%*. Equation 2-7 should be modified by multiplying *(1-loss%)* for rectifier operation and *(1+loss%)* for inverter operation. The *loss%* of *1.5%* is used in this thesis for IGBT switching loss. [6] shows for 2-level converter has a power loss of approximately 3% for the complete VSC substation, including IGBT, filter, and interface transformer losses.

2.4.5 DC Cable and Overhead Transmission Lines

Cables and overhead transmission lines can be used to transmit electric energy over a distance. Since a VSC allows only one dc voltage polarity, the cable does not need to be designed for voltage polarity reversal. This allows simple cable types such as extruded XLPE dc cables, to be used in long-distance VSC transmission systems [10] [47].

2.5 Control of a VSC-HVdc System

A single-line diagram of one VSC connected to an ac system is shown in Figure 2-8. The converter transformer and the phase reactor are represented as the resister R and the reactor L. By controlling the amplitude and phase of the generated voltage V_c, the VSC can be made to generate any given values of real and reactive currents on the ac side. The real part of the current is more sensitive to the phase angle δ of V_c, whereas the imaginary part of the current is more sensitive to the amplitude of V_c. In a converter operating with PWM, these quantities can easily be controlled by the modulating index (which is proportional to V_c) and the phase of the modulating signal.

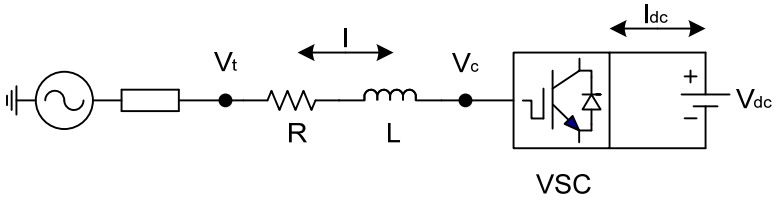


Figure 2-8 Single-line diagram of one VSC connect to an ac system

For VSC transmission applications, this control is usually achieved by direct control or vector control [6] [22] [38]. Direct control means that the modulation index m and the phase angle δ are directly adjusted by the parameters being controlled, typically with m

being responsible to set the desired voltage magnitude of V_c and δ being responsible for setting the real power flow. However, this leads to interactions between the loops, because the change of δ not only affects the real power but also indirectly the reactive power and hence the voltage. Vector control [48] is a current control strategy that permits the independent control of real power (P) and reactive power (Q) by the adjusting action of the modulation index and the phase of the modulating signal. The controller is decoupled in nature permitting a change in P without any effect on Q and vice versa. It also has the inherent advantage of being able to limit the VSC current thereby preventing overloading.

Other control strategies are also possible, such as Type II control by Schauder [49] and the power-synchronization control proposed by Zhang [50]. However, this thesis utilizes the vector control as an example because it is the well accepted and most widely used approach in the electric power industry. The vector control strategy consists of a cascade control system with faster inner current controllers and additional outer controllers that provide the reference values for the inner controllers. This section will give brief introduction of the vector control for VSC.

2.5.1 Inner Current Controllers

From Figure 2-8, the voltage and current relationship in three-phase instantaneous form is expressed as

$$L\frac{di}{dt} = -Ri + u_t - u_c \qquad 2\text{-}8$$

By applying the Park transformation shown in equation 2-9, the abc-frame in equation 2-8 can be converted to the synchronously rotating dq-reference frame, as shown in equations 2-10 and 2-11. The angle θ is in phase with the positive sequence of the fundamental frequency ac waveform V_t and is generated using a phase-locked-loop (PLL) to the system voltages V_t.

$$\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \qquad 2\text{-}9$$

$$L\frac{di_q}{dt} = -Ri_q - \omega L i_d + u_{tq} - u_{cq} \qquad 2\text{-}10$$

$$L\frac{di_d}{dt} = -Ri_d + \omega L i_q + u_{td} - u_{cd} \qquad 2\text{-}11$$

However, it can be seen from equations 2-10 and 2-11 that the two loops are not decoupled because a change in the real component of the current i_d via the parameter δ (the phase angle of V_c relative to V_t) would also immediately affect the reactive component of the current i_q and thus require a change in the magnitude of V_c in order to keep i_q at its set point.

Assuming the VSC output voltage V_c is determined by the following PI controller equations (equations 2-12 and 2-13), where i_d^* and i_q^* are reference values of i_d and i_q, and K_p and K_i are proportional and integral gains of the PI controller.

$$u_{cq} = -(K_p + \frac{K_i}{s})(i_q^* - i_q) - \omega L i_d + u_{tq} \qquad 2\text{-}12$$

$$u_{cd} = -(K_p + \frac{K_i}{s})(i_d^* - i_d) + \omega L i_q + u_{td} \qquad 2\text{-}13$$

Substituting equations 2-12 and 2-13 to equations 2-10 and 2-11, yields

$$L\frac{di_q}{dt} = -\left[R - (K_p + \frac{K_i}{s})\right] i_q - (K_p + \frac{K_i}{s}) i_q^* \qquad 2\text{-}14$$

$$L\frac{di_d}{dt} = -\left[R - (K_p + \frac{K_i}{s})\right] i_d - (K_p + \frac{K_i}{s}) i_d^* \qquad 2\text{-}15$$

It is clear that i_d and i_q are decoupled in equations 2-14 and 2-15. The vector control method removes the coupling between the real and the imaginary of the output current; hence, the real power and the reactive power can be independently controlled. Based on equations 2-12 and 2-13, the inner current controller loop is shown in Figure 2-9.

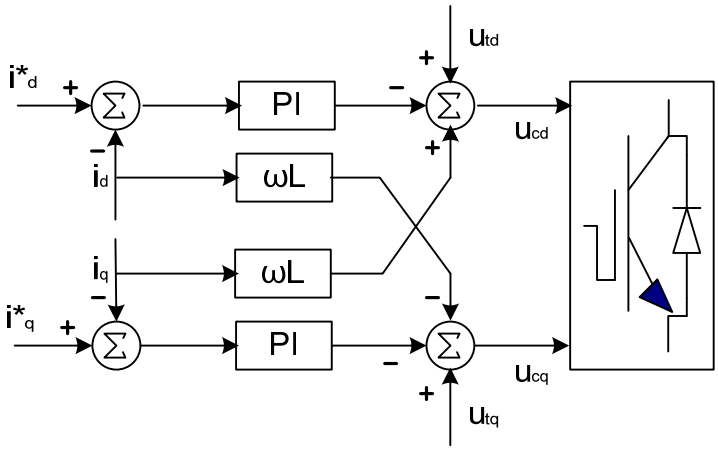


Figure 2-9: Inner current control loop

2.5.2 Outer Controller

The vector control is accomplished by additional outer controllers that provide the reference values for the inner current controllers. The outer controllers include the dc voltage controller, the ac voltage controller, the active power controller, the reactive power controller and the frequency controller. The reference value of the active current

i_d^* can be derived from the dc voltage controller and the active power controller; the reference value of the reactive current i_q^* can be obtained from the ac voltage controller and the reactive power controller.

2.5.2.1 DC Voltage Control

A dc voltage controller on one or more VSCs common to the dc voltage bus can regulate active power to maintain the required voltage level across the dc capacitor. The voltage across the capacitor is measured, filtered and compared to the dc voltage reference and the dc voltage error is obtained. A proportional controller, and sometimes a proportional-integral (PI) controller, can maintain the dc voltage within prescribed limits. The PI controller is used to eliminate steady state error; however, if a droop characteristic is required, a proportional controller should be used [4] [19] [30].

2.5.2.2 Active Power Control

This function controls the power transfer so that it goes in the direction determined by the operator and controls the power to the value that is determined by the operator. The power regulator function should be used as the primary means of regulating the flow of power between two ac networks. Power control is achieved by regulating the phase angle of the fundamental frequency component of the ac voltage at the converter side of the interface reactance.

2.5.2.3 AC Voltage Control

AC voltage control is achieved by regulating the magnitude of the fundamental frequency component of the ac voltage generated at the VSC side of the interface reactor and/or

transformer. With multilevel converters and two-level converters operating with PWM, the magnitude of the ac voltage is directly achieved by variation of the modulation index. The dc capacitor voltage is usually held constant.

2.5.2.4 Reactive Power Control

Control of the reactive power exchange with the ac system is achieved by modifying the amplitude output voltage waveform to make the convertor either absorb or provide reactive power. The reactive power control output for each end of the system can be set independently at any set point between the limits of the converter.

2.5.2.5 Frequency Control

The frequency control is essential when the power delivered to the ac system from the VSC is the dominant or perhaps the only source of power. Such is the case when a VSC supplies power to an isolated load. The frequency can be controlled by control of the frequency of the oscillator that determines the valve pulse firing sequence.

2.5.3 Phase Locked Loop (PLL)

The function of the PLL is to generate the angle reference to synchronize the VSC to the ac system and provide the angle information for Park transformation matrices. There is a wide range of PLL types currently in use in HVdc schemes worldwide [36] [51] [52] [81]. They follow the same operating principal, and differ mainly in the area of phase angle measurement. The D-Q-Z type PLL as presented in [53] and shown in Figure 2-10, is a widely used type in actual applications and is used in this thesis. The PLL uses an internal voltage controlled oscillator (VCO) to generate the reference angle θ that varies

between 0° and 360° for firing the converter valves. The phase angle error between the ac system voltage (positive sequence, phase-A) and the reference ramp θ is passed through a PI controller to change the frequency of the VCO. If properly designed, an equilibrium condition is rapidly achieved where the phase angle error goes to zero, ensuring that θ is in perfect synchronism to the angle of the phase-A positive sequence ac voltage of the input voltage V_t. The D-Q-Z type of grid control has excellent immunity from either loss of synchronizing voltage or harmonic distortion on the ac synchronizing voltage. This is useful for HVdc converters which are often required to operate with weak ac systems and are subjected to distorted synchronizing voltages [53].

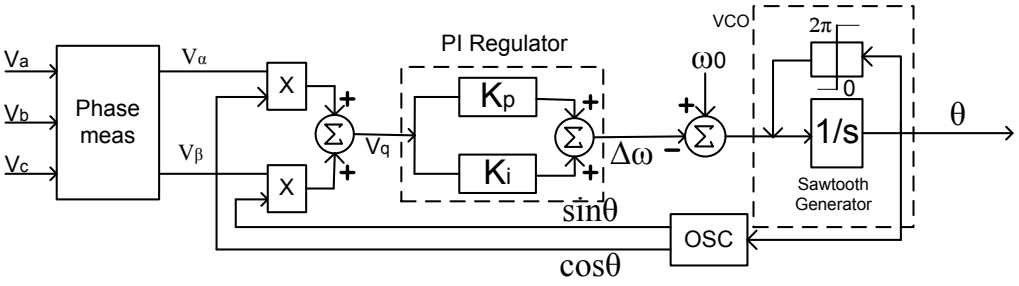


Figure 2-10: Block diagram of PLL

2.5.4 Overall VSC Vector Control

Each VSC converter has two degrees of freedom, namely the modulation index and phase angle. The choice of which kind of outer controller will be used to calculate the reference values of the converter current will depend on the application and may require some advanced power system study. One ac operating variable (either ac voltage or reactive power) and one dc operating variable (either dc voltage or dc power) can be controlled at each VSC converter. The ac voltage control is normally used to maintain the ac voltage at

the connected bus especially when the ac system is weak. If the ac connection is strong, the reactive power control strategy can be used. When the VSC connect to an isolated load, ac voltage control and frequency control can be used [54]. Each converter controls its reactive power flow independent of the other station. But it should be known that the active power flow into the dc link must be balanced and the dc voltage controller is necessary to achieve power balance. The converter controlling the dc voltage will act as a "slack bus" that will provide or absorb sufficient real power to achieve the power balance of the dc system. The balance is attained based on the measurement of the dc voltage. The other converters can set any active power value within the limits for the system. Under steady-state operation with only one converter, operating as a slack bus does not pose a problem. However, if the converter acting as a slack bus trips then the power balance on the dc grid cannot be achieved if all the other converters are trying to control their own dc power. To avoid uncontrolled power flow on the dc grid as a consequence of local dc voltage and current measurement errors, the steady-state dc voltage limits can be defined by an upper and lower droop line [30].

In this thesis, the dc grid system is used to demonstrate the concept of control parameters tuning. Only one converter controls the dc voltage and the other converters control dc power. The dc voltage droop concept is not employed.

The overall VSC vector control is shown in Figure 2-11 [40]. The frequency control for the VSC connected to an isolated load is not considered in this thesis.

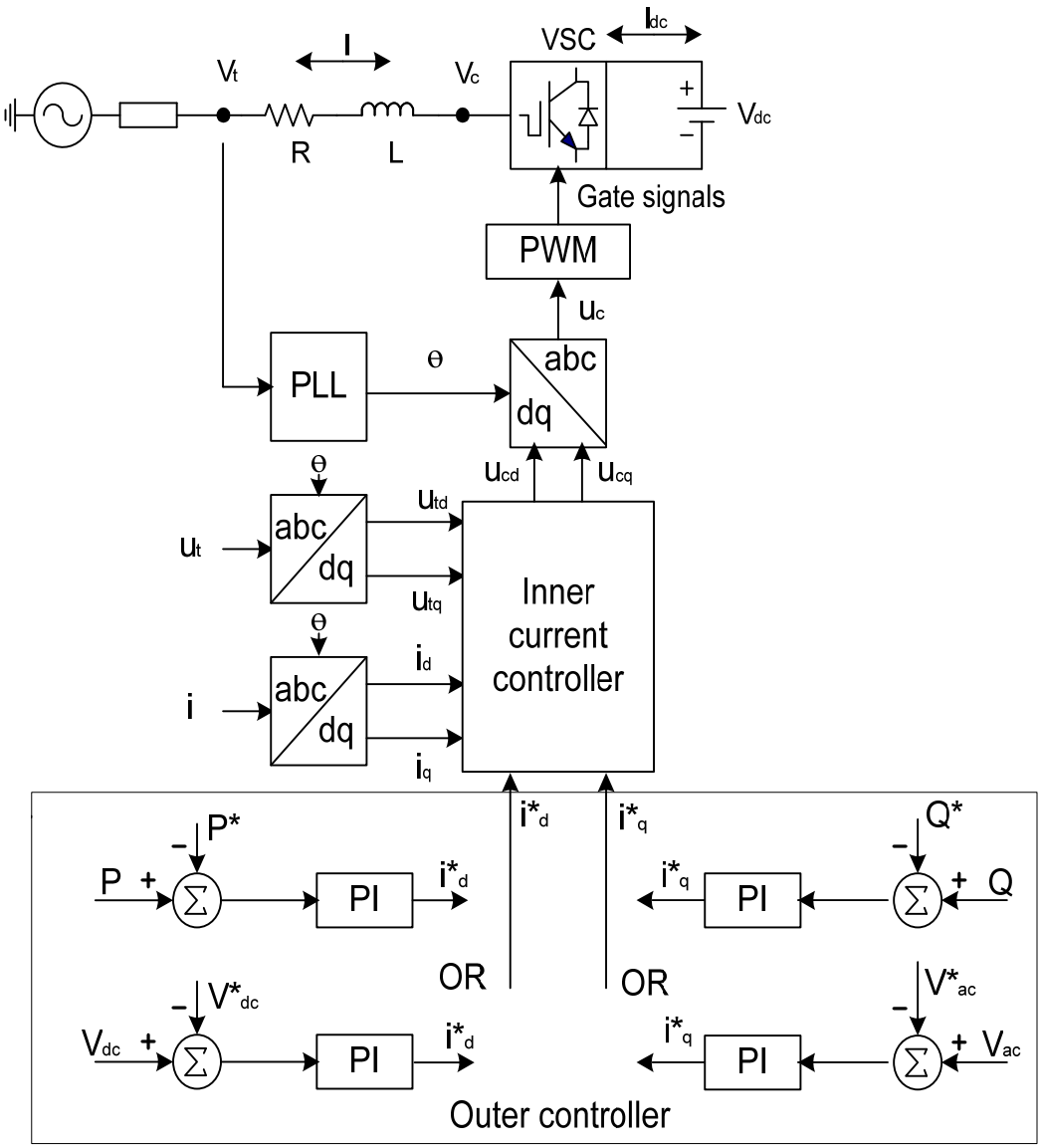


Figure 2-11: Complete VSC control structure including outer controllers

2.6 Summary

This chapter presented the basic operating principles of VSC transmission and the main components of a VSC transmission system. The real and reactive power capability of a VSC system was discussed. VSC transmission is limited by the finite converter current and voltage rating and by the finite ac system strength. For the purposes of simulation

modeling, the averaged and the two-level valve bridge model were given and the PWM control method was introduced.

The control system of a VSC-HVdc transmission system was discussed. The vector control mathematical model was provided, as was a block diagram of the control systems in the vector control technique.

Chapter 3: VSC Transmission Imposed by AC System Strength and AC Impedance Characteristics

3.1 Introduction

It is well-known that an LCC-HVdc converter has difficulty operating into a weak ac system, whereas the performance of a VSC-HVdc converter is relatively unaffected by system strength (which allows VSC-HVdc converters to be connected to very weak ac systems) [10]. It is also well-known that an LCC-HVdc transmission system requires a large amount of reactive power compensation at the converter ac bus terminal, whereas a VSC-HVdc system can operate capacitively or inductively in the inverter and rectifier modes [10] and is less dependent on external reactive compensation.

Research regarding the limitations that ac systems impose on VSC transmission has mainly focused on ac system strength; the effects of ac system impedance characteristics on VSC transmission have largely been ignored [32] [33] [34]. In this chapter, an analytical model is used to quantitatively analyze the minimum ac system SCR required for the VSC to transfer real power under different ac system impedance angles. The analytical results provide a key contribution to this thesis. Several other parametric relationships are explored, such as the impact of external reactive power support on the operating limits of the converter. The impact of the converter rating on the operating limits of the converter is also examined.

Analytical results are based on steady state calculation; however, an electromagnetic transients program (EMT) models the network in detail using the differential equations of the network. EMT simulation has become an acceptable validation tool for other methods of calculation because actual experimentation in real power systems is usually not possible [55]. In this thesis, the analytical analysis is compared with a system modeled on an Electromagnetic transient simulator (PSCAD/EMTDC). The PSCAD model was developed by the author and includes full EMT details of the system. Its converter ratings are loosely based on a proposed off-shore wind generation collector system. As testing against an actual system was not possible, the EMT model provided the most accurate model for validation purposes.

A phase-locked-loop (PLL) is typically used for angle reference generation for LCC-HVdc and VSC-HVdc transmission applications. A fast PLL will normally improve the dynamic transient performance for traditional LCC-HVdc [36]. However, for VSC-HVdc transmission, the SCR of the connected ac system may be very low. The simulation results show that if the VSC system is connected to a very low SCR ac system a fast (i.e., high gain) PLL will have an adverse affect on system performance, and the gains of the PLL need be reduced. In this thesis, a state-space VSC model was developed and compared with the non-linear EMT model. The impact of PLL gains on the system stability was discussed.

3.2 Comparison of LCC and VSC

This section will give a brief comparison between LCC HVdc transmission and VSC transmission.

The major difference between an LCC HVdc converter and a VSC converter arises because of the manner in which the converter valves are turned off. The LCC uses thyristor valves and thus depends on an ac voltage source in the ac system for the commutation process. A thyristor can only be turned on when forward biased, but cannot be turned off unless a reverse bias voltage is applied to it. The ac system voltage reversal is used for this purpose. When the next valve in the conduction sequence is triggered, the previously conducting valve sees a reverse voltage and hence begins the process of turning off. Note that the reverse voltage is available only for a 180° interval from the firing angle α =0° point of the conducting thyristor. Due to the inductance in series with the ac voltage, this process takes a certain amount of time – corresponding to the overlap angle. If the firing of this next valve is delayed too much, the commutation (transfer of current from outgoing valve to incoming valve) is not successful and this phenomenon is referred to as commutation failure. In contrast, the self –commutated VSC uses valves made with IGBTs or similar devices that can be turned off with a command pulse at any desired moment. Hence commutation failure is a non-event.

Also, the VSC appears to the ac side as a controllable voltage source, whose voltage is determined by the firing method and the dc side capacitor voltage. The dc side voltage in a VSC is essentially kept constant. The LCC on the other hand reproduces an ac current whose magnitude is proportional to the dc current. In the LCC, the dc current is

maintained constant due to smoothing or other inductances. Furthermore, polarity of valves has to be reversed in the LCC for power reversal. A VSC system instead can keep the same voltage polarity for power reversal. The same voltage polarity during power reversal makes the dc grid possible.

Table 3.1 summarizes the comparison between LCC and VSC converters.

Table 3.1: Summary Comparison between LCC HVdc and VSC HVdc [6]

Feature		LCC HVdc	VSC HVdc
Harmonic and filter requirement		Filter banks are designed to eliminate characteristic harmonics on the ac and dc side.	Smaller filters are required. MMC technology may eliminate the filter.
Overvoltages in the ac system		A sudden LCC HVdc stop can cause fundamental frequency overvoltages, sometimes exacerbated by resonance.	Due to the use of small ac filters and the ability to control ac voltage, the overvoltage can be eliminated or become significantly smaller.
Robustness against the ac system faults		The scheme may suffer a temporary commutation failure.	The scheme can not suffer from commutation failures and can continue to transfer some power.
Cost, losses, reliability and the availability of the large scale HVdc system		Better at present	The differences are decreasing because of improvements in VSC technology.
Protection against the dc system faults		Fast restart is possible	Fast restart is difficult without dc circuit breakers or full bridge converter.
Flexibility of power flow reversal in multi-terminal schemes		Power flow reversal at each terminal requires mechanical switching operation.	Power flow reversal at each terminal is easy.
Requirement for ac system	Dependence on an ac voltage source	An ac voltage source is mandatory	A voltage source is not required
	Reactive power consumption or generation	LCC HVCC consumes reactive power of 50% to 60% of the active power. Switchable shunt capacitor banks are necessary for reactive power compensation.	Reactive power can be generated or absorbed. Reactive power can be controlled independently from active power control at both ends of the VSC Transmission scheme.
	Short circuit ratio (SCR)	In general, a SCR of more than 2 is required for stable operation.	There is no special limit on SCR.[1]

Note [1] the requirement of SCR for VSC HVdc transmission will be studied in this thesis. Some new conclusions will be reported.

Shading indicates superior performance.

3.3 System Strength and Short Circuit Ratio

The interaction between ac and dc systems can be represented by the strength of the ac system relating to the dc system in the HVdc system. To quantify the strength of the ac system at the converter bus of an HVdc system, the concepts of short circuit ratio (SCR) and effective short circuit ratio (ESCR) were introduced for LCC applications [56]. The SCR is the ratio of the ac system's short circuit capacity and rated dc power. The ac/dc system strength is defined in IEEE guide [56] for LCC HVdc transmission as $V_t^2 / |Z_s|$, where V_t is the rated terminal voltage and $|Z_s|$ the ac system's impedance magnitude at fundamental frequency. The weaker the ac system, that is, the lower the SCR, the greater will be the propensity for undesired ac/dc interactions. The following SCR values can be used to classify an ac/dc system:

- Strong system: SCR > 3
- Weak system: 2 < SCR < 3
- Very weak system: SCR < 2

As ac filters are predominantly capacitive, they tend to increase the ac system's Thévenin reactance and thereby decrease the short circuit ratio, resulting in a smaller "Effective" Short Circuit ratio (ESCR). LCC schemes with low SCR can suffer from high temporary overvoltages on load rejection, and are more prone to power-voltage instability.

Figure 3.1 is a simple representation of an HVdc system connected to an ac network.

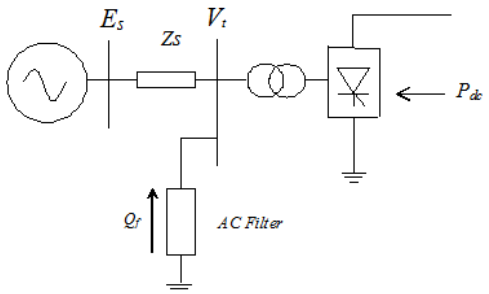


Figure 3.1: The converter connected to an ac bus

For the system shown in Figure 3.1, the ac system SCR at the converter bus is calculated as in equation 3-1, in which, Z_s is the Thévenin impedance of the ac system, P_{dc} is the rated dc power, and V_t is the rated line RMS voltage.

$$SCR = \frac{MVA_{sc}}{P_{dc}} = \frac{V_t^2 / |Z_s|}{P_{dc}} \qquad 3\text{-}1$$

ESCR can be calculated as in equation 3-2, in which Q_f is the fundamental Mvar of the shunt ac filter connected to the converter ac bus bar.

$$ESCR = SCR - \frac{Q_f}{P_{dc}} \qquad 3\text{-}2$$

The ESCR is thus smaller in magnitude than the SCR. Strictly speaking; the SCR (or ESCR) is a complex number inversely proportional to Z_s. However, as Z_s is usually highly inductive, the SCR is almost all imaginary. Hence, the phase of the SCR (or ESCR) is often ignored and only its magnitude is referred to.

The SCR (and/or ESCR) defined above is a widely-used terminology in the HVdc community. However, it is not strictly related to the actual short-circuit current. It is independent of the system voltage E_s, which is the voltage behind the Thévenin impedance that provides the current during the short circuit. In fact, the rated line voltage V_t and the rated dc power P_{dc} are constants for a specific HVdc system. Thus, in

equations 3-1 and 3-2, the SCR and ESCR are only determined by the Thévenin impedance Z_s.

It is well-known that a conventional line-commutated HVdc system cannot work properly if the connected ac system is weak because the commutation of the converter valve is dependent on the stiffness of the alternating voltage supplied by the ac system. A VSC-HVdc system has the potential to be connected to a weak ac system, as well as the capability to generate or consume reactive power; however, the research in this thesis demonstrates that the strength of an ac system has significant impact on the behavior of the VSC-HVdc systems connected to it.

3.4 Analytical Studies

The one-terminal VSC-HVdc system in Figure 3.2 was used for the analytical studies.

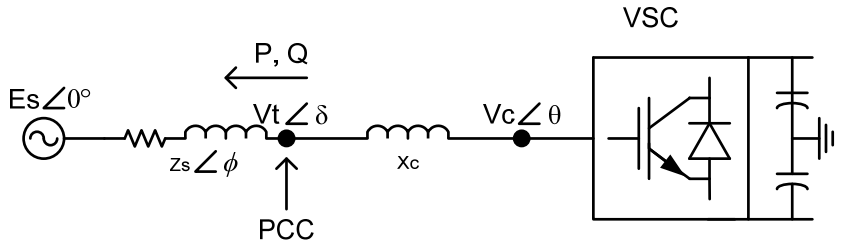


Figure 3.2: Analytical studies VSC-HVdc model

The ac system was represented in the analytical model by a simple equivalence, a Thévenin impedance $Z_s\angle\phi$ and a Thévenin voltage source E_s. This simplified equivalence is defined only at the rated frequency, which indicates that its impact on higher frequency switching transients and harmonics may not be entirely accurate. Nevertheless, as it is at present not possible to select the parameters of a "true" ac

network, the simplified network will have to do for the present. Note that a significant component of the studies using this equivalent are for determining steady-state behavior at rated frequency, such as maximum real power P and reactive power Q exchange between the ac and dc system, and determination of power - voltage stability limits, for which this representation gives correct results. For the VSC, commutation failure is no longer a problem, so that the harmonics ripple and switching-type transients are not a big concern, for which the simple representation is adequate. Also, the VSC requires either a small ac filter to absorb the higher order switching harmonics or no ac filter at all (in the case of topologies such as the MMC [41] [44]). In the current available publications [7] [19] [30] [33] [57], simple equivalents representations are widely used to analyze the behavior of HVdc systems. And this thesis follows in this tradition.

3.4.1 Limits to Operation Imposed by AC System Characteristics

3.4.1.1 AC System Neglecting Source Resistance

The well-known power-angle equation 3-3 assumes that the ac system impedance in Figure 3.2 is purely inductive, i.e., $Z_s = jX_s$. The effect of the impedance angle (ϕ) is not considered at this point. It is considered later.

$$P = \frac{V_t \cdot E_s}{X_s} \sin(\delta) \qquad 3\text{-}3$$

Assuming the magnitudes of E_s and V_t are both *1 pu*, if the ac system impedance X_s in equation 3-3 is replaced by the SCR in equation 3-1, theoretically, the maximum power that can be transferred can be written as $P_{max}(pu) = SCR$. The maximum power that can be transferred is proportional to SCR, which is inversely proportional to the connected ac

system Thévenin impedance. Note that the angle δ is now the angle of V_t with reference to E_s (which is assumed to be the angle reference, i.e $E_s \angle 0^o$). This use is different from Chapter 2, where δ was the angle between V_t and V_c.

3.4.1.1.1 A Note on Dead Loads

In the analysis, it was assumed that the converter was feeding into an ac network, and the Thévenin voltage of the network equivalent was E_s. Under these circumstances, the maximum power transferrable is close to the SCR value. This may be confusing to some readers who may argue that the VSC can feed a "dead load", i.e., a pure impedance, which they consider to be of SCR = 0. In the definition used here (equation 3-1), the SCR is really a measure of the Thévenin admittance of the system, and not a measure of the actual short circuit fault level. Hence a dead load does not mean SCR =0!

Nevertheless, the dead load must be handled differently. If E_s now represents the voltage across the load, it is no longer a constant, as it changes with load current. If E_s in Figure 3.2 is replaced by a "dead load" (Z_{load}) as shown in Figure 3.3, The apparent power at VSC terminal V_t is $S = V_t^2 / (Z_{load} + Z_s)$. If we assume the load Z_{load} is purely resistive ($Z_{load} = R_{load}$) and the impedance between the load and the VSC terminal V_t is purely inductive ($Z_s = X_s$), the real power transfer at V_t to the dead load is $P = R_{load} \cdot V_t^2 / (R_{load}{}^2 + X_s{}^2)$. We can see analytically, the maximum real power can be transferred is when $R_{load} = X_s$, which is $P_{\max} = V_t^2 / 2X_s$ or $P_{\max}(pu) = SCR / 2$.

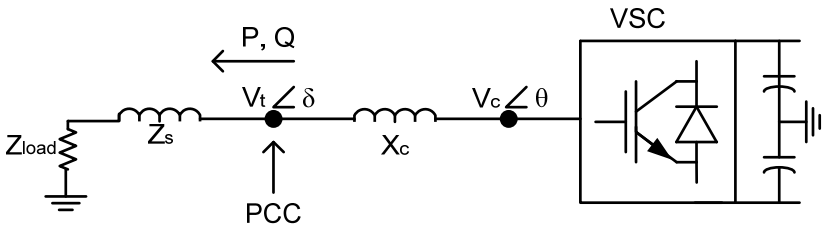


Figure 3.3: VSC connected to a dead load

3.4.1.2 AC System Considering Source Resistance

If the ac system impedance is represented as $Z_s = r_s + jx_s$, the real and reactive power transferred at the PCC for both directions (rectifier operation and inverter operation) can be derived as in equations 3-4 to 3-7, where δ is the phase difference between V_t and E_s (for inverter operation, δ is the angle by which V_t leads E_s; for rectifier operation, δ is the angle by which E_s leads V_t) and $\beta = 90° - \phi$, where $\phi = \tan^{-1}(x_s / r_s)$ is the angle of the ac system impedance:

$$P_{inv} = V_t^2 \frac{r_s}{|Z_s|^2} + \frac{V_t \cdot E_s}{|Z_s|} \sin(\delta - \beta) \qquad 3\text{-}4$$

$$P_{rec} = -V_t^2 \frac{r_s}{|Z_s|^2} + \frac{V_t \cdot E_s}{|Z_s|} \sin(\delta + \beta) \qquad 3\text{-}5$$

$$Q_{inv} = V_t^2 \frac{x_s}{|Z_s|^2} - \frac{V_t \cdot E_s}{|Z_s|} \cos(\delta - \beta) \qquad 3\text{-}6$$

$$Q_{rec} = V_t^2 \frac{x_s}{|Z_s|^2} - \frac{V_t \cdot E_s}{|Z_s|} \cos(\delta + \beta) \qquad 3\text{-}7$$

Hence, the maximum real powers that can be transferred for rectifier operation and inverter operation are given by equations 3-8 and 3-9. Here it is assumed that the converter's internal voltage V_c is large enough and that the series inductance X_c is small

enough to allow these powers. Also, at this time the MVA and voltage ratings of the VSC are not taken into consideration.

Inverter Operation: $$P_{inv\_\max} = \frac{V_t \cdot E_s}{|Z_s|} + V_t^2 \frac{r_s}{|Z_s|^2} \quad (3\text{-}8)$$

which happens for $\delta = [180° - \phi]$, and

Rectifier Operation: $$P_{rec\_\max} = \frac{V_t \cdot E_s}{|Z_s|} - V_t^2 \frac{r_s}{|Z_s|^2} \quad (3\text{-}9)$$

which happens for $\delta = \phi$

Under the above maximum power transfer condition, the VSC is required to supply the following reactive power:

$$Q_{inv\_P\max} = V_t^2 \frac{x_s}{|Z_s|^2} \quad \text{(inverter operation)} \quad (3\text{-}10)$$

$$Q_{rec\_P\max} = V_t^2 \frac{x_s}{|Z_s|^2} \quad \text{(rectifier operation)} \quad (3\text{-}11)$$

The ac system impedance angle ϕ is typically in the range of *70*° to *85*° [6] [56]. Equations 3-8 and 3-9 show that with the resistance present in the ac system the maximum power that can be transferred is different for rectifier operation than for inverter operation for the same ac system. For example, if the ac system impedance angle is *80*°, the maximum real power transferred for the VSC in rectifier mode occurs when the phase difference δ is *80*°; for the VSC in inverter mode it occurs when the phase difference δ is *100*°.

If the ac system strength is represented by the SCR, as shown in equation 3-1, assuming rated conditions, equations 3-8 and 3-9 can be more succinctly expressed in per-unit as:

$$P_{inv\_max}(pu) = \frac{P_{inv\_max}}{P_{dc}} = SCR \cdot (\frac{Es}{V_t} + \frac{r_s}{|Z_s|}) \quad 3\text{-}12$$

$$P_{rec\_max}(pu) = \frac{P_{rec\_max}}{P_{dc}} = SCR \cdot (\frac{Es}{V_t} - \frac{r_s}{|Z_s|}) \quad 3\text{-}13$$

Equations 3-10 and 3-11can be more succinctly expressed in per-unit as:

$$Q_{P\_max}(pu) = \frac{Q_{P\_max}}{P_{dc}} = SCR \cdot \frac{x_s}{|Z_s|} \quad 3\text{-}14$$

Assuming the magnitudes of E_s and V_t are both *1 pu*, equations 3-12 and 3-13 show that rated power can be transferred only when the SCR is in the neighbourhood of *1* (equal to *1* if $r_s = 0$). When $r_s > 0$, under the same ac system conditions, the maximum real power that can be transferred is higher when the VSC is in inverter mode (equation 3-12) than when it is in rectifier mode (equation 3-13). Interestingly, equation 3-14 shows that the reactive power required under maximum real power transfer is the same for rectifier operation as for inverter operation.

Figure 3.4 and Figure 3.5 show the maximum transferrable real powers as functions of the SCR for inverter and rectifier operation. Parametric plots are provided for different impedance angles ranging from *90°* to *70°*. Figure 3.6 shows the relationship between phase angle difference *δ (°)* and the real power *P (pu)* transferred at the PCC for SCR = 1, and Figure 3.7 shows the relationship between the real power *P (pu)* transferred and the reactive power *Q (pu)* required at the PCC for *SCR = 1*. In order to compare the maximum real power transfer and the reactive power requirement for both rectifier and inverter modes of operation the curves are extended to show both rectifier and inverter operation on the same plot. These are shown in Figure 3.6 and Figure 3.7 respectively.

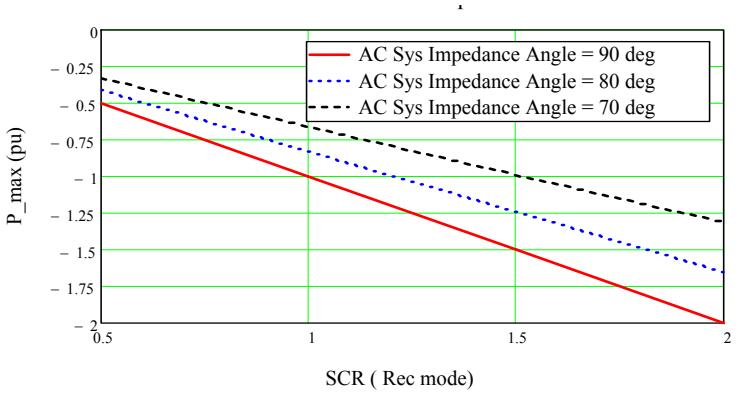


Figure 3.4: Rectifier SCR – P_max curve for different angle ϕ

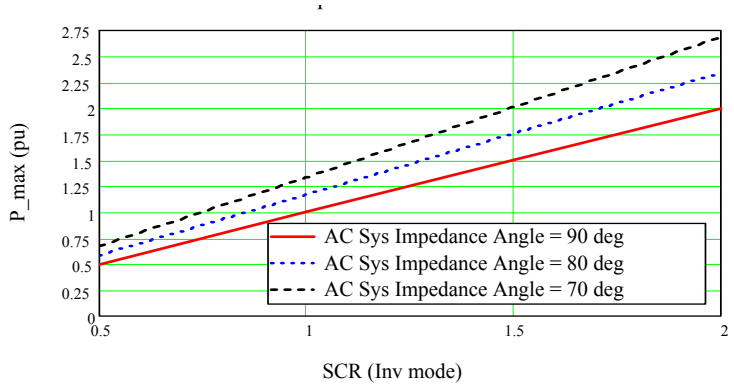


Figure 3.5: Inverter SCR – P_max curve for different angle ϕ

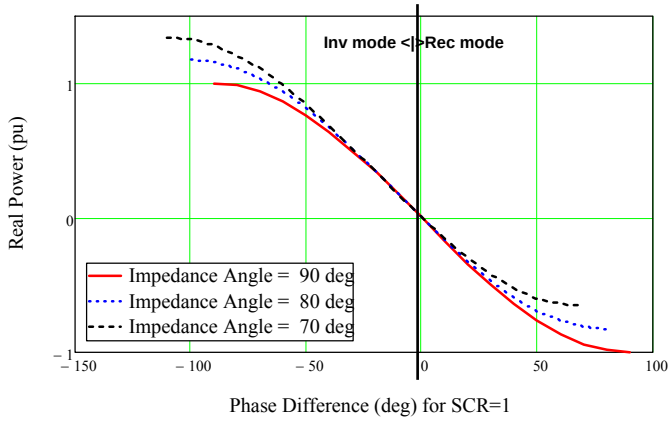


Figure 3.6: δ - P curve for different impedance angle ϕ

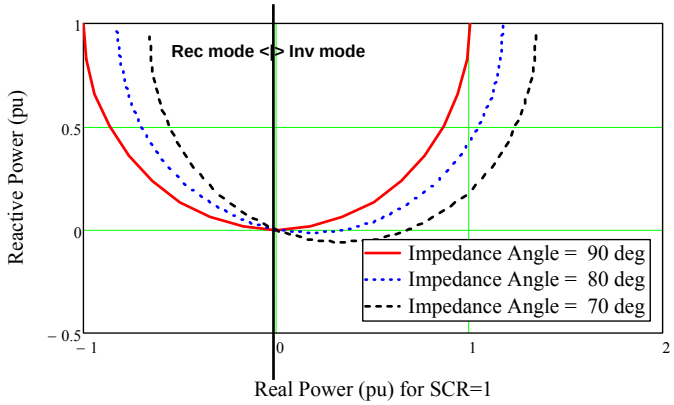


Figure 3.7: P - Q curve for different impedance angle ϕ

Table 3.2 shows the maximum real power that can be transferred and the reactive power required under different ac system impedance angles for *SCR = 1*. For example, if the ac system impedance angle is *80°* and *SCR = 1*, for rectifier operation the maximum real power that can be transferred is *0.826 pu*, and for inverter operation it is *1.174 pu*. The reactive power required under maximum real power transfer is *0.985 pu* for both rectifier and inverter operation.

Table 3.2: P_{max} Possible and Q Required for SCR = 1

ϕ (°)	P_{max} (pu) for SCR = 1		$Q_{\_Pmax}$ (pu) for SCR = 1	
	VSC as Rectifier	VSC as Inverter	VSC as Rectifier	VSC as Inverter
90	1	1	1	1
85	0.913	1.087	0.996	0.996
80	0.826	1.174	0.985	0.985
75	0.741	1.259	0.966	0.966
70	0.658	1.342	0.94	0.94

Table 3.3 shows, as a function of the system impedance angle ϕ, the smallest SCR ($SCR_{\_min}$) for which rated power can still be transmitted. It can be seen that the rectifier requires a larger $SCR_{\_min}$ than the inverter, and that the difference becomes larger as the impedance of the system becomes more resistive. The corresponding reactive power requirements at the PCC and the VSC rating requirement are shown in Table 3.3.

Table 3.3: $SCR_{\_min}$, Q and S_{vsc} Required for P = 1 pu Transfer

ϕ (°)	VSC as Rectifier			VSC as Inverter		
	$SCR_{\_min}$	Q(pu)	S_{vsc}(pu)	$SCR_{\_min}$	Q(pu)	S_{vsc}(pu)
90	1	1	1.414	1	1	1.414
85	1.095	1.091	1.48	0.92	0.916	1.356
80	1.21	1.192	1.556	0.852	0.839	1.305
75	1.349	1.303	1.643	0.794	0.767	1.260
70	1.52	1.428	1.743	0.745	0.7	1.221

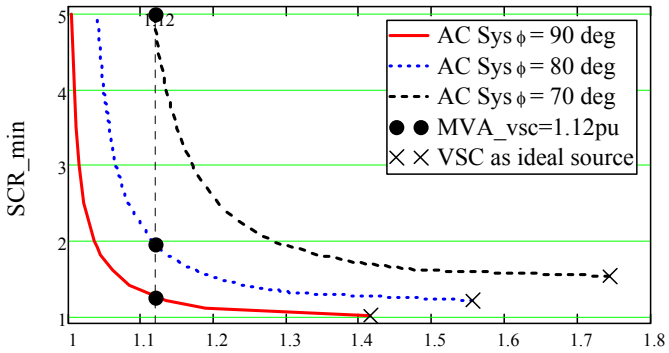
The results in Table 3.3 show (for different ac system impedance angles ϕ) the minimum ac system SCR that must exist if *1 pu* real power is transferred to the PCC. Table 3.3 shows that for the VSC in rectifier mode the required minimum SCR increases when ac system impedance angle ϕ decreases. It also shows that for the VSC in inverter mode the required minimum SCR decreases when ac system impedance angle ϕ decreases. The corresponding reactive power requirements at the PCC show the same trend. For example, if the ac system impedance angle is *80°*, when the VSC is in rectifier mode the minimum ac system SCR is *1.21* in order to transfer *1 pu* of real power at the PCC, and the required reactive power absorption at the PCC is *1.192 pu*. However, when the VSC is in inverter mode the minimum ac system SCR is *0.852* in order to transfer *1 pu* of real power at the PCC, and the required reactive power absorption at the PCC is *0.839 pu*.

3.4.2 Limits to Operation Imposed by VSC Ratings

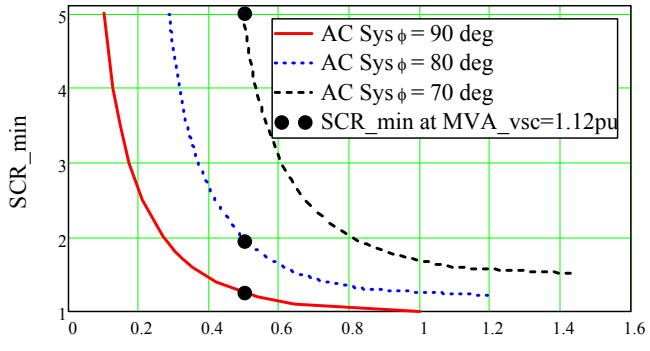
The analysis in the previous section did not consider the finite MVA ratings of the VSC as seen from the PCC. When these are considered, a higher $SCR_{\_min}$ than the one calculated in the previous section is typically necessary because the VSC may not be able to provide the reactive power required (see Table 3.3). Figure 3.8 (rectifier operating mode) and Figure 3.9 (inverter operating mode) show the variation of $SCR_{\_min}$ as a

function of the VSC's pu MVA rating and as a function of the reactive power requirement at the PCC when rated real power is transferred.

Consider that a VSC's MVA rating is *1.12 pu* (i.e., Q_{vsc} = *0.5 pu* at rated power). For rectifier operation, Figure 3.8 (a) shows that $SCR_{\_min}$ increases to *1.25, 1.95*, and *5.0* for ϕ=*90°, 80°*, and *70°*, respectively, as shown by the black dots. If the VSC rating is not constrained, the corresponding $SCR_{\_min}$ values are much smaller (*1.0, 1.21*, and *1.52*) (see Table 3.3), as indicated by the 'X's in Figure 3.8 (a).



(a)

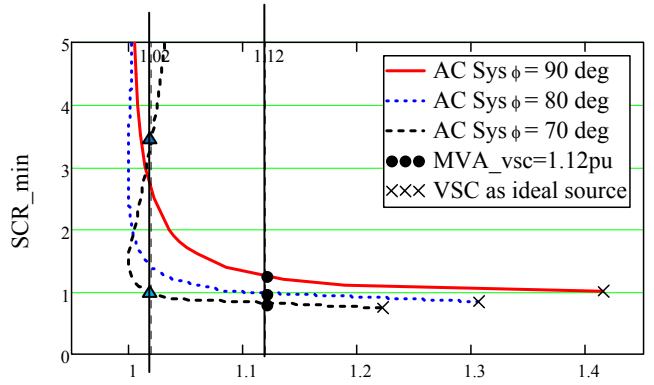


(b)

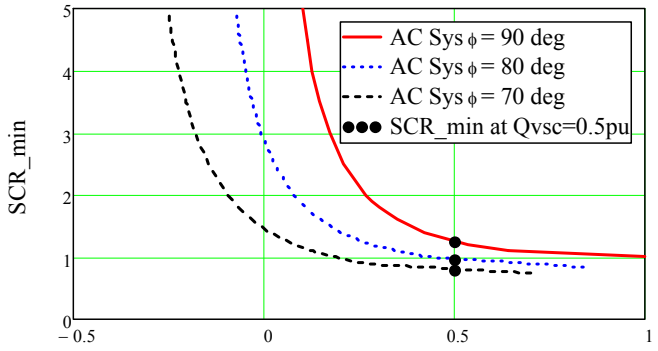
Figure 3.8: $SCR_{\_min}$ – MVA_{VSC} and Q curve for different ϕ (Rectifier operation)

For inverter operation, Figure 3.9 (a) shows that $SCR_{\_min}$ increases to *1.25, 0.95*, and *0.8* for ϕ=*90°, 80°*, and *70°*, respectively, as shown by the black dots. If the VSC rating is not

constrained, the corresponding SCR_min values are a little smaller (*1.0, 0.852*, and *0.745*), as indicated by the 'X's (see Table 3.3). As can be seen, the impact of the finite MVA rating of the VSC on the rectifier is more severe, especially for a VSC connected to a highly resistive ac system.



(a)



(b)

Figure 3.9: SCR_{min} – MVA_{VSC} and Q curve for different ϕ (Inverter operation)

It is interesting to see in Figure 3.9 (a) that for a high-resistance ac system (i.e., ϕ=70°) in inverter operation the SCR curve folds back on itself, indicating that the SCR must lie between a minimum and maximum value for a VSC in inverter operation. For example, if the VSC MVA rating is 1.02 pu, as shown by the vertical line in Figure 3.9 (a), the minimum SCR and maximum SCR required are 1 and 3.5 (as shown as blue triangles),

respectively. As can be seen from Figure 3.9 (b), the VSC will absorb instead of generate reactive power if it is connected to a high-resistance ac system (i.e., ϕ=70°). When the SCR is high the VSC MVA rating (i.e., 1.02 pu) will be exceeded. However, if the VSC MVA rating is higher (i.e., 1.05 pu) the maximum SCR constraint will not be applicable.

3.4.3 AC Voltage Considering off Nominal Values

Note that the above analysis considered the magnitudes of E_s and V_t are both *1 pu*. If an interface transformer is present between the ac system and the converter, the secondary voltage (the filter bus voltage) can be controlled with the tap changer to achieve the maximum active and reactive power from the converter, both consumption and generation.

For example, if a higher (i.e., *1.05 pu)* or lower (i.e., *0.95 pu*) voltage V_t at the PCC is controlled by the tap changer. Compared to Figure 3.4, Figure 3.10 shows the maximum transferable real powers as function of the SCR for rectifier operation. As can be seen, if a higher voltage at the PCC (i.e., *1.05 pu*) is controlled, the maximum transferable real power is higher (the upper dotted curves in each ϕ group). In contrast, if a lower voltage at the PCC (i.e., *0.95 pu*) is controlled, Figure 3.10 shows the maximum transferable real power is lower (the lower dotted curves in each ϕ group).

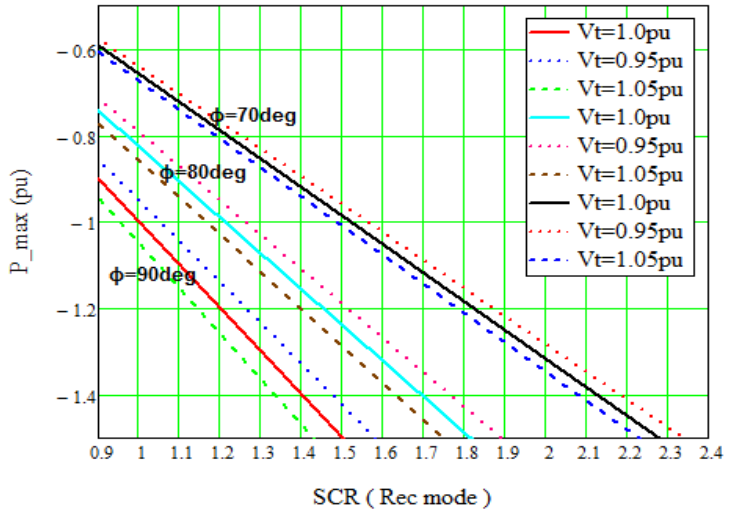


Figure 3.10: SCR – $P_{\_max}$ curve for different V_t (Rectifier operation)

However, for a lower controlled voltage at the PCC (i.e., *0.95 pu*), due to the consequent reduction in the required reactive power, the required minimum SCR ($SCR_{\_min}$ in Table 3.3) for which the rated power can still be transmitted can be reduced. Figure 3.11 shows the variation of $SCR_{\_min}$ as a function of the VSC's pu MVA rating at the PCC (S_{vsc} in Table 3.3) for the VSC to transfer rated real power at rectifier operating mode. As can be seen, for $V_t = 0.95\ pu$, the system can operate at lower SCRs (dotted curves) in comparison to the case in which $V_t = 1\ pu$ (solid curves). For example, consider a VSC rectifier with an MVA rating of 1.12 pu (i.e., Q_{vsc} = 0.5 pu at rated power), the minimum required SCR for transmitting rated power in rectifier operation decreases dramatically from 5 to 2.8 for ac system ϕ= 70°.

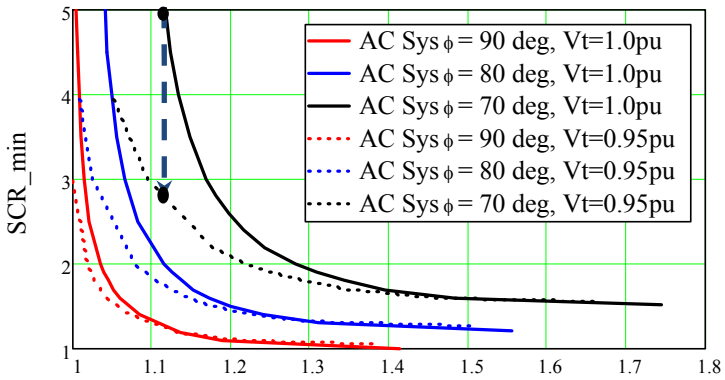


Figure 3.11: SCR – MVA_{vsc} curve for different V_t (Rectifier operation)

If the magnitude of the Thévenin equivalent voltage source E_s is higher than *1 pu*, the maximum real power that can be transferred is higher (compared to the values in Table 3.2), and the minimum SCR and reactive power required for transferring *1 pu* real power at the PCC are decreased (compared to the values in Table 3.3). Figure 3.12 shows the minimal SCR required at PCC for different impedance angle ϕ under different E_s magnitude (1.0 pu, 1.05 pu and 1.10 pu) for transferring rated power under rectifier and inverter operating conditions. As can be seen the higher the E_s magnitude, the lower the minimum SCR required for transferring the rated real power at the PCC.

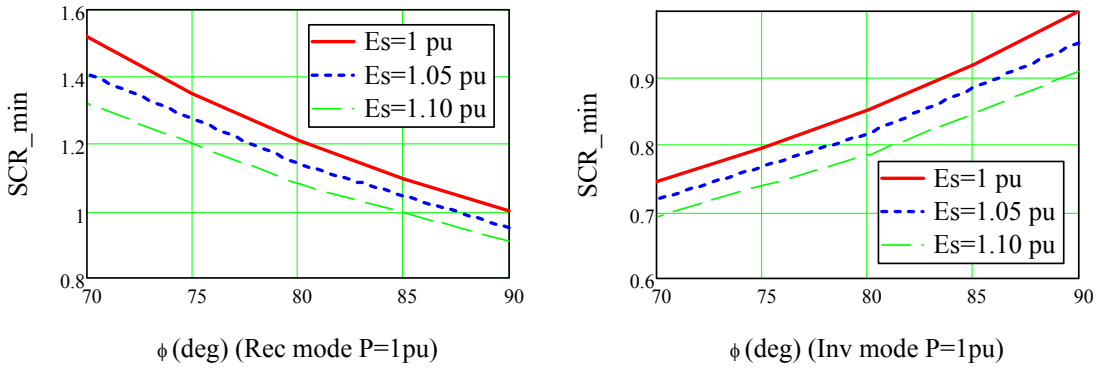


Figure 3.12: ϕ – SCR_{min} curve for different E_s

3.4.4 The Advantages of Reactive Support at the PCC

Generally, it is assumed that reactive power support is not needed for VSCs. However, particularly for weak ac systems, reactive power support may be necessary at the PCC if the MVA rating of the VSC is not sufficiently large. Figure 3.13 shows the equivalent circuit when reactive power support Q_c, using a fixed capacitor, is considered. Equations 3-4 to 3-7 can still be used, except that the impedance Z_s must be replaced by the Thévenin equivalent Z_{eq}, and E_s must be replaced by E_{eq}.

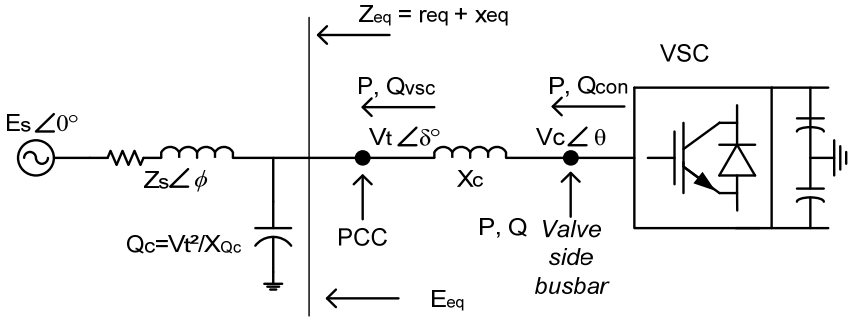


Figure 3.13: Analytical VSC-HVdc model

Here ESCR can be defined in a manner identical to that used for LCC as:

$$ESCR = \frac{V_t^2}{|Z_{eq}| \cdot P_{dc}} = SCR - \frac{Q_c}{P_{dc}} = SCR - Q_c(pu) \qquad 3\text{-}15$$

Assuming rated conditions, equations 3-4, 3-5, 3-6, and 3-7 can be more succinctly expressed in per-unit (based on the dc rated power) as:

$$P_{inv}(pu) = ESCR \cdot \frac{r_{eq}}{|Z_{eq}|} + ESCR \cdot \frac{E_{eq}}{V_t} \cdot \sin(\delta - \beta) \qquad 3\text{-}16$$

$$P_{rec}(pu) = -ESCR \cdot \frac{r_{eq}}{|Z_{eq}|} + ESCR \cdot \frac{E_{eq}}{V_t} \cdot \sin(\delta + \beta) \qquad 3\text{-}17$$

$$Q_{inv}(pu) = ESCR \cdot \frac{x_{eq}}{|Z_{eq}|} - ESCR \cdot \frac{E_{eq}}{V_t} \cdot \cos(\delta - \beta) \qquad 3\text{-}18$$

$$Q_{rec}(pu) = ESCR \cdot \frac{x_{eq}}{|Z_{eq}|} - ESCR \cdot \frac{E_{eq}}{V_t} \cdot \cos(\delta + \beta) \qquad 3\text{-}19$$

where

$$E_{eq} = E_s \cdot \frac{-jx_{Qc}}{Z_s - jx_{Qc}} = E_s \cdot \frac{SCR}{ESCR}$$

$$Z_{eq} = Z_s \,||\, (-jX_{Qc}) = Z_s \cdot \frac{-jx_{Qc}}{Z_s - jx_{Qc}}, \;\; Z_{eq}(pu) = \frac{1}{ESCR}$$

and

$$Q_{inv}(pu) = Q_c(pu) + Q_{VSC\_inv}(pu)$$

$$Q_{rec}(pu) = Q_c(pu) + Q_{VSC\_rec}(pu)$$

At rated power (i.e., *P = 1 pu* in equations 3-16 or 3-17), the relationship between Q_c and Q_{vsc} can be obtained by replacing the ESCR in equations 3-16 to 3-19 with equation 3-15. If the ac system is purely inductive (i.e., ϕ=90°) the per unit relationship of Q_c and Q_{vsc} can be derived analytically as:

$$Q_{vsc} = (SCR - Q_c) - \sqrt{\left(\frac{E_{eq}}{V_t}\right)^2 \cdot (SCR - Q_c)^2 - 1} - Q_c \qquad 3\text{-}20$$

As can be seen, the VSC reactive power support Q_{vsc} to the PCC (and hence, the VSC rating) can be reduced by adding fixed capacitor Q_c at the PCC. Figure 3.14 shows the relationship between Q_{vsc} and Q_c for different SCRs (ϕ=90°) under rated power transfer. Note that over-compensation Q_c will result in Q_{vsc} becoming negative (inductive) as seen in Figure 3.14, at which point the VSC rating will begin to increase once again. Hence, for the lowest VSC rating, Q_c should be selected so that $Q_{vsc} = 0$. For example, for *SCR = 2,* $Q_c = 0.14$, as indicated by the black dot.

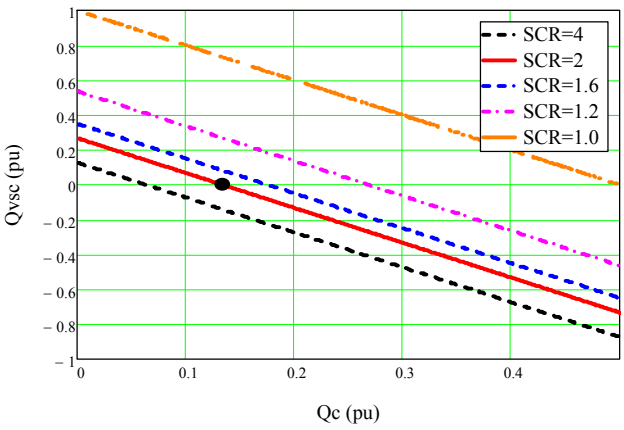


Figure 3.14: Q_c vs. Q_{vsc} curve for ac system ϕ = 90deg, P = 1 pu transfer

It has been shown in Table 3.3, if the ac system is not purely inductive, in order to transfer *1 pu* real power the requirements of the reactive power support at the PCC are different for rectifier operation than for inverter operation. Figure 3.15 shows the relationship between the ac system ($\phi = 80°$) SCR and the reactive power support Q_c required at PCC if complete compensation is required (i.e., no reactive power required from the VSC or $Q_{vsc}=0$). As can be seen, rectifier operation requires more Q_c support than inverter operation does. It also shows that the weaker the ac system (i.e., lower SCR), the more impact of Q_c support on reducing the VSC reactive power requirement.

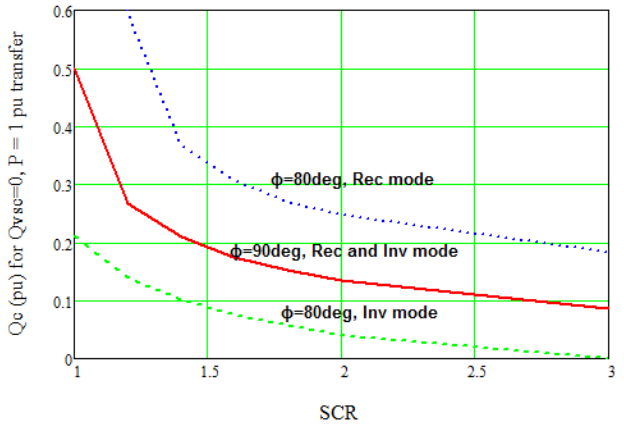


Figure 3.15: SCR – Q_c curve for complete compensation

Section 3.4.2 has shown that when the finite MVA ratings of the VSC are considered, a higher $SCR_{\_min}$ is typically necessary because the VSC may not be able to provide the reactive power required. However, the above analysis shows that the minimum required SCR ($SCR_{\_min}$) to transmit rated power can be decreased by adding the additional reactive power Q_c at the PCC. For example, consider a VSC rectifier with an MVA rating of *1.12 pu* (i.e., $Q_{vsc} = 0.5\ pu$ at rated power). If $Q_c = 0.1\ pu$ is supplied at the PCC, as in Figure 3.16 (see Figure 3.8 also), the minimum required SCR for transmitting rated power in rectifier operation decreases dramatically from 5 to 2.4 for ac system $\phi = 70°$. For other ac system conditions ($\phi = 80°$, $\phi = 90°$), the minimum SCR versus VSC MVA curves are also shown in Figure 3.16. As can be seen, if the finite MVA rating of the VSC is considered, the provision of such additional reactive power allows the system to operate at significant lower SCRs (the dotted curves) in comparison to the cases when no compensation is provided (the solid curves). Note that the reactive power in the above analysis refers to the total reactive power support at the point of common coupling. This will include the Mvar generation from any ac filters that are present.

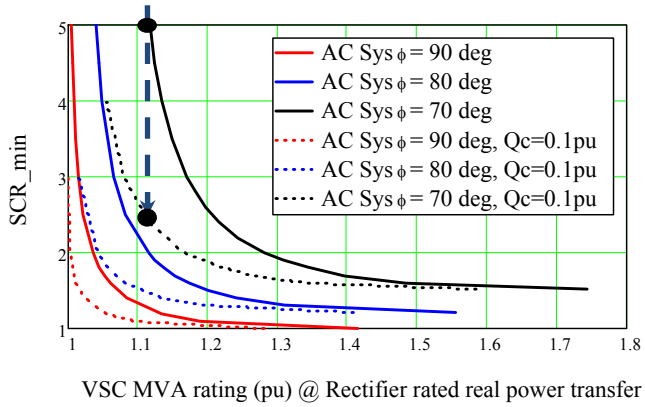


Figure 3.16: $SCR_{\_min}$ – MVAVSC curve for 0.1 pu Q_c (Rectifier operation)

3.4.5 Converter Valve MVA and Voltage Rating Requirement

The converter phase reactance needs be considered when calculating the converter valve MVA rating and voltage rating. The converter valve side rms ac bus voltage V_c from Figure 3.13 is shown in equation 3-21. This value will be used to determine the converter valve MVA rating and the voltage rating, and hence the value of the modulation index.

$$V_c \angle \theta = V_t \angle \delta + jX_c \cdot \frac{V_t \angle \delta - E_s \angle 0}{Z_s \angle \phi} \qquad 3\text{-}21$$

By controlling the phase angle and magnitude of the V_c, the real power P and the reactive power Q at the PCC can be controlled independently. The magnitude of V_c is directly related to the ac system characteristics and the converter reactance X_c. The modulation index m requirements and the converter MVA ratings requirements are based on the calculations of voltage V_c for the different converter reactances X_c. From equation 2-4, the relationship between the rms value of V_c and the modulation index m is given by $V_{c\_rms} = \sqrt{3/2} \cdot V_{dc} \cdot m$, where V_{dc} is the per unit dc voltage and V_{c_rms} is the per unit rms ac voltage on the valve side (as in Figure 3.13). In this section, all voltages are in per unit.

Based on the assumption that the magnitudes of E_s and V_t are both *1.0 pu*, Table 3.4 to Table 3.8 show the values of the valve side converter ac bus voltage V_c and the modulation index m under different ac system *SCRs*. Also shown in the tables are the required reactive power support Q at the PCC and the reactive power Q_{con} at the converter ac terminal. The VSC's MVA rating (including converter reactor/transformer) is defined as the apparent power into the VSC at the PCC, which is shown as $MVA_{\_vsc}$ in the tables. However, the MVA rating of the converter's IGBT valve bridge is the

apparent power entering the valve at the converter's valve side busbar. The converter's MVA rating is shown as $MVA_{\_con}$ in the tables. The resulting ratings consider two different values of the converter reactor/transformer (*0.15 pu* and *0.25 pu* based on the rated dc power and the rated ac voltage at converter side*)* for inverter and rectifier operations, respectively. The three ac system impedance angles, ϕ *=90°, 80°,* and *70°*, are considered.

Table 3.4: ϕ=90°, 1 pu Real Power, the same for Rectifier and Inverter Operation

VSC rating at PCC			Converter rating at converter bus							
			X_c = 0.15 pu				X_c = 0.25 pu			
SCR	Q (pu)	$MVA_{\_vsc}$ (pu)	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m
1.0	1.00	1.41	1.30	1.64	1.16	0.95	1.50	1.80	1.28	1.05
1.6	0.35	1.06	0.52	1.13	1.06	0.87	0.93	1.37	1.12	0.91
2.0	0.27	1.04	0.43	1.09	1.05	0.86	0.54	1.14	1.10	0.90
3.0	0.17	1.01	0.33	1.05	1.04	0.85	0.43	1.09	1.07	0.87
4.0	0.13	1.01	0.28	1.04	1.03	0.84	0.38	1.07	1.06	0.87

Table 3.5: ϕ=80°, 1 pu Real Power, Rectifier Operation

VSC rating at PCC			Converter rating at converter bus							
			X_c = 0.15 pu				X_c = 0.25 pu			
SCR	Q (pu)	$MVA_{\_vsc}$ (pu)	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m
1.21	1.19	1.55	1.56	1.85	1.19	0.97	1.80	2.06	1.32	1.08
1.6	0.61	1.17	0.82	1.29	1.10	0.90	0.96	1.39	1.18	0.96
2.0	0.49	1.11	0.68	1.21	1.08	0.88	0.80	1.28	1.15	0.94
3.0	0.37	1.07	0.54	1.14	1.07	0.87	0.65	1.19	1.12	0.91
4.0	0.32	1.05	0.48	1.11	1.06	0.87	0.59	1.16	1.11	0.91

Table 3.6: ϕ=80°, 1 pu Real Power, Inverter Operation

VSC rating at PCC			Converter rating at converter bus							
			X_c = 0.15 pu				X_c = 0.25 pu			
SCR	Q (pu)	$MVA_{\_vsc}$ (pu)	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m
0.85	0.84	1.31	1.1	1.49	1.14	0.93	1.27	1.62	1.24	1.01
1.0	0.42	1.09	0.6	1.17	1.07	0.87	0.72	1.23	1.13	0.92
1.6	0.15	1.01	0.3	1.04	1.03	0.84	0.40	1.08	1.07	0.87
2.0	0.08	1.00	0.23	1.03	1.02	0.83	0.33	1.05	1.05	0.86
3.0	-0.01	1.00	0.14	1.01	1.01	0.82	0.24	1.03	1.03	0.84
4.0	-0.05	1.00	0.1	1.01	1.00	0.82	0.20	1.02	1.02	0.83

Table 3.7: ϕ=70°, 1 pu Real Power, Rectifier Operation

VSC rating at PCC			Converter rating at converter bus							
			X_c = 0.15 pu				X_c = 0.25 pu			
SCR	Q (pu)	$MVA_{\_vsc}$ (pu)	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m
1.52	1.43	1.75	1.88	2.13	1.22	1.00	2.19	2.41	1.38	1.13
1.6	1.1	1.49	1.43	1.75	1.17	0.96	1.65	1.93	1.30	1.06
2.0	0.8	1.28	1.05	1.45	1.13	0.92	1.21	1.57	1.23	1.00
3.0	0.61	1.17	0.81	1.29	1.10	0.90	0.95	1.38	1.18	0.96
4.0	0.54	1.14	0.73	1.24	1.09	0.89	0.86	1.32	1.16	0.95

Table 3.8: ϕ=70°, 1 pu Real Power, Inverter Operation

VSC rating at PCC			Converter rating at converter bus							
			X_c = 0.15 pu				X_c = 0.25 pu			
SCR	Q (pu)	$MVA_{\_vsc}$ (pu)	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m	Q_{con} (pu)	$MVA_{\_con}$ (pu)	V_c (pu)	m
0.75	0.7	1.22	0.92	1.36	1.12	0.91	1.07	1.47	1.20	0.98
1	0.19	1.02	0.34	1.06	1.04	0.85	0.45	1.10	1.08	0.88
1.6	-0.03	1.00	0.12	1.01	1.01	0.82	0.22	1.02	1.02	0.83
2.0	-0.1	1.00	0.06	1.00	1.00	0.82	0.16	1.01	1.01	0.82
3.0	-0.18	1.02	-0.03	1.00	0.98	0.80	0.08	1.00	0.99	0.81
4.0	-0.22	1.02	-0.07	1.00	0.98	0.83	0.04	1.00	0.98	0.80

The results show that the converter MVA rating is higher than the entire VSC MVA rating due to the existence of the converter reactance. For the same VSC MVA rating, the

higher the converter reactance is, the higher the converter MVA rating is. Rectifier operation requires a higher MVA rating than inverter operation does.

The converter reactance/transformer is one of the key components in a VSC that permits continuous and independent control of active and reactive power, as indicated in Section 2.4.1. The typical reactance is in the range *0.1 pu* to *0.15 pu* for the converter transformer and converter reactance [39]. However, the results in the tables show that for a lower SCR, a higher resistive ac system, and a higher converter reactance, the required modulation index m will be over *1.0*, as shown by the red colour in the tables. For example, $\phi=70°$ with $X_c=0.25\ pu$ rectifier operation would have problems for $SCR < 2$. The over-modulation ($m > 1.0$) will cause higher harmonic content at lower frequencies. For a VSC valve bridge as shown in Figure 2-6 or Figure 2-7 (a), since there is a diode connected directly between the terminals of each sub-module of the VSC valve bridge and there is no ability to block forward current or to reverse the applied capacitor voltage. Consequently the peak of the valve side converter ac bus voltage V_c must remain below the dc voltage in order to keep the diode reverse biased. Hence over-modulation is not allowed in the VSC application [43].

If the power-electronic converter's MVA and voltage limits are both considered, the minimum SCR required needs to consider both of them. For example, consider the case in Figure 3.17 and Figure 3.18 (the variation of $SCR_{\_min}$ as a function of the converter's MVA rating and of its voltage rating, respectively) for $\phi=80°$ and rectifier mode at rated power operation. Assume the converter has an MVA limit of *1.2 pu* (i.e., $Q_{con} = 0.66\ pu$ at rated power) and a voltage limit of *1.1 pu*. For $X_c = 0.15\ pu$, considering the MVA limit, the minimum SCR is *2.1* (shown by the black dot in Figure 3.17); but considering

the voltage limit, the minimum SCR is *1.6* (shown by the black triangle in Figure 3.18). So, the applicable limit is dictated by the MVA and the $SCR_{\_min}$ is *2.1*. However, when $X_c = 0.25\ pu$, the MVA and voltage imposed limits are *2.9* and *5.0*, respectively. The $SCR_{\_min}$ is now dictated by the voltage, and it becomes 5.0.

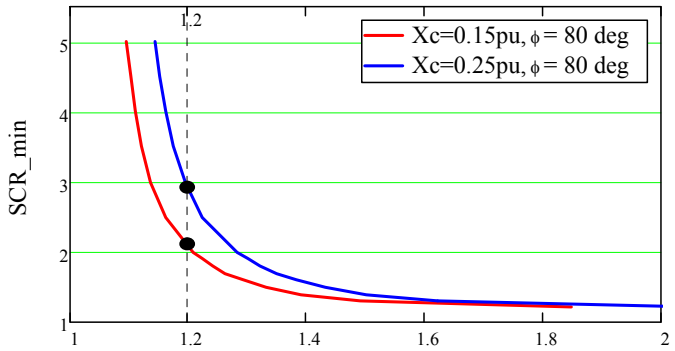


Figure 3.17: $SCR_{\_min}$ vs. $MVA_{\_con}$ for P = 1 pu (Rectifier operation)

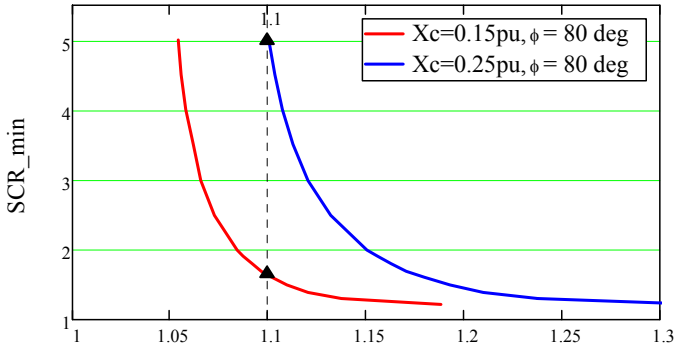


Figure 3.18: $SCR_{\_min}$ vs. V_{con} for P = 1pu (Rectifier operation)

Summary of the Analytical Studies:

- The ac system characteristics, the *SCR*, and impedance angle ϕ impose the limitations on the VSC real power transmission.

- The minimum ac system *SCR* is required to transfer *1 pu* of real power at the PCC. The minimum ac *SCR* at the rectifier side increases from that required for ideally inductive ac impedance, whereas for the inverter side it decreases.
- A finite VSC MVA rating increases the minimum *SCR* requirement. If there is reactive power compensation (filters) at the PCC point to support the ac voltage, the required VSC rating will be reduced. The minimum SCR required will decrease.
- The converter side ac bus voltage V_c magnitude is determined not only by the ac system SCR and the ac system impedance angle ϕ, but also by the converter reactance X_c. The higher the X_c is, the higher the magnitude of V_c is, and the higher the converter side ac busbar reactive support Q_{con} is.
- Compare the VSC operating to a resistive ac system (i.e., $\phi < 90°$) with the VSC operating to a pure inductive ac system (i.e., $\phi = 90°$), higher converter ac bus voltage V_c is required if the VSC operating in rectifier mode, but lower converter ac bus voltage V_c is required if the VSC is operating in inverter mode. Therefore, if the VSC is designed to operate in both rectifier mode and inverter mode, the optimum transformer tap ratio should be determined from analytical studies.
- If both the converter MVA rating and the voltage rating have limits, in order to meet both the limits the higher minimum SCR should be chosen as the minimum SCR requirement for the connected ac system.

3.5 EMT Validation

In this section, the analytical calculations of the previous sections are validated using detailed electromagnetic transients simulations. Only the cases with an ac network that includes a Thévenin source are considered. The dead load situation is peripheral to the thesis scope and is not simulated.

VSC transmission schemes include the symmetrical monopole, asymmetric monopole and bipolar configuration. In a symmetrical monopole the dc output voltages are of equal but opposite magnitude. The midpoint of the dc circuit is earthed, using capacitors as shown in Figure 3.2. This arrangement makes maximum use of the dc voltage rating of the conductor. In an asymmetrical monopole, the dc side output from the converter is asymmetrical with one conductor typically connected to earth. It is possible to operate the transmission system in metallic return or in earth return. Two asymmetrical converters can be connected together in a bipolar configuration either with earth or metallic return [58]. This topology may be more suitable for very large ratings.

Most existing VSC schemes are of the symmetrical monopole [6] type, and most reported literature uses symmetrical monopole configuration, which is also the topology used in this thesis. The widely-used EMT program PSCAD/EMTDC [59] was used to conduct the simulations.

Figure 3.19 shows the simulated VSC-HVdc model with the VSC converter rated at ±320 kV (dc) and 500 MW. The configuration of the VSC system is symmetric monopole. The nominal PCC voltage was 230 kV. The modeled VSC converter was connected by a 50 km dc cable to a dc voltage source representing the remote converter

(which was assumed to be in control of the dc voltage). The simulated system details are provided in Table 3.9 and Table 3.10. The control system of the VSC was based on a fast inner-current control loop controlling the ac current. A synchronously rotating two-axis (*d-q*) reference frame was used for the inner current control, which allowed fully-independent control of both the active and reactive power flows of the VSC system. The references of the inner current control, (i_d, i_q), were generated by the two outer controllers, real power control, and ac voltage control. The VSC control system had four PI controllers.

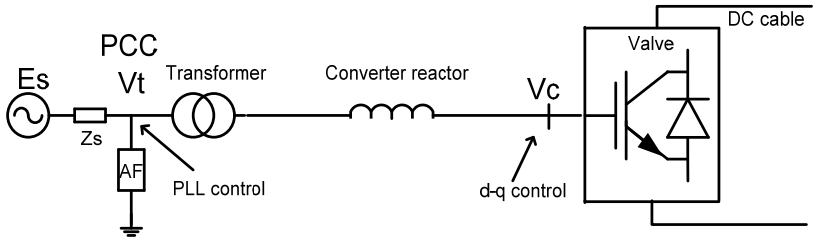


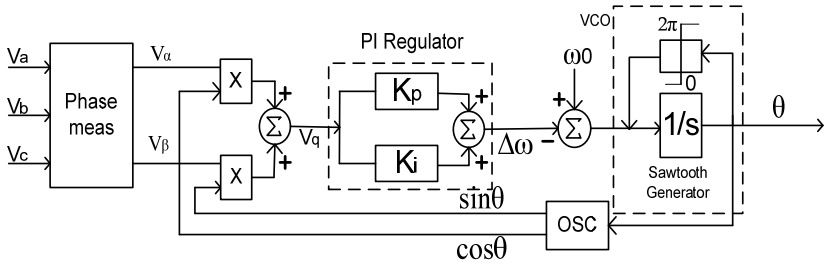
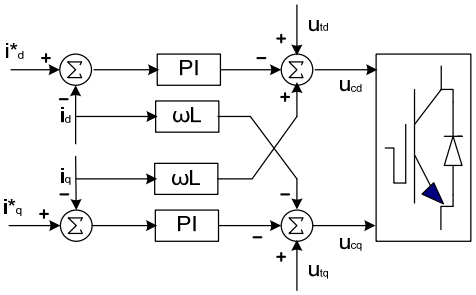
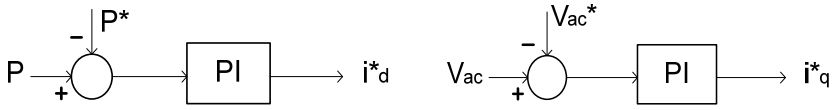
Figure 3.19: EMT simulation VSC-HVdc model

Table 3.9: VSC-HVdc System Parameters

Rated ac system voltage	230 kV, 60 Hz
Ac system impedance angle	80° Note 1
Rated dc power rating (base)	500 MW
DC voltage	±320 kV
Converter transformer rating	583 MVA
Converter transformer ratio	230 kV/333 kV
Converter transformer and reactor impedance	0.15 pu (0.088 H)
Passive high pass filter	75 Mvar (15%) Note 1
Converter	2-level PWM
DC capacitor	500 µF
Switching frequency	900 Hz
DC cable: 321.5 kV and 1563 A, copper	45 km, 2400 mm^2

Note [1] value changed in section 0

Table 3.10: Controller Parameters

PLL controller: K_p=10, K_i =50	
Inner controller: K_p=0.5, K_i=50	
Outer controllers: P controller: K_p=0.5, K_i=35 V_{ac} controller: K_p=0.6, K_i=50	

Note on the per unit (pu) quantities:

The rated ac voltage (V_{ac}) and rated dc power (P_{dc}) are used as the base quantities per unit quantities on the ac side of the converter. The impedance base is then P_{dc}^2/V_{ac}. For all converters in this thesis, the rated ac voltage is V_{ac}= 333 kV on the converter side of the converter transformer and V_{ac}= 230 kV on the ac system side. Rated dc power P_{dc} can be 500 MW or 1000 MW (e.g., multi-terminal study case in Chapter 4 and Chapter 5). The dc voltage is the base quantity on the dc side. The dc voltage used in this thesis is 320 kV.

The percentage quantities for the converter transformer is chosen 10% on its own MVA base and voltage base on the ac system side. Considering both real and reactive power,

the transformer MVA base is larger than the rated dc power P_{dc} of 500 MW or 1000 MW. In this thesis 1 pu real power and 0.5 pu reactive power are considered for the converter transformers. Therefore, transformer leakage reactance is based on MVA rating of 583 MVA for converter with 500 MW P_{dc} and 1166 MVA for converter with 1000 MVA P_{dc}.

3.5.1 SCR verse VSC MVA Rating Validation

Three ac system impedance angles, *70°, 80°,* and *90°*, and different SCRs were tested by changing system resistance and reactance. The validation approach used consisted of trying to reproduce, by simulation, the curves of $SCR_{\_min}$ versus the MVA at the PCC when rated real power is transferred, i.e., the curves shown in Figure 3.8 and Figure 3.9.

In the detailed switching simulation model, a 75 Mvar (15% of dc power rating) high pass filter was used to mitigate the higher order harmonics in the ac system. This is typical for 2 and 3-level VSC HVdc converters [39]. The curves presented in Figure 3.20 and Figure 3.21 for comparing analytical and simulation results use current measured in the converter inductor. As the ac filter is located on the system side of these measurements, it has theoretically no impact on these curves. Of course, it would affect the reactive power absorbed as a whole by the VSC and filter combination. The reactive power supply and its impact are discussed in a later Section 3.5.2. The $SCR_{\_min}$ values calculated in Section 3.4 are the theoretical minimums, and in a practical circuit, they can be approached closely, although reaching them exactly is a challenge, as doing so requires optimizing the controls [60]. This aspect is discussed in more detail in the next section.

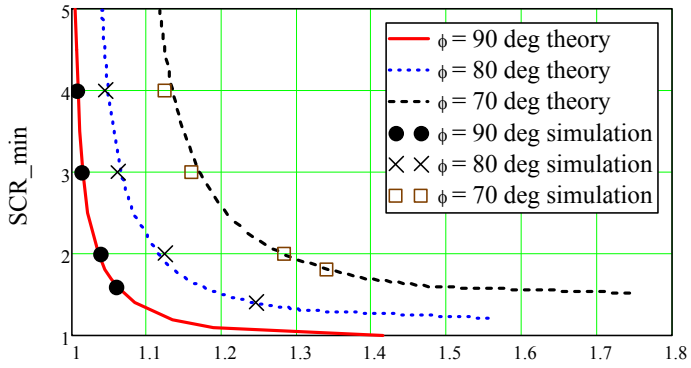


Figure 3.20: SCR –MVA$_{VSC}$ curve for different ϕ (Rectifier operation)

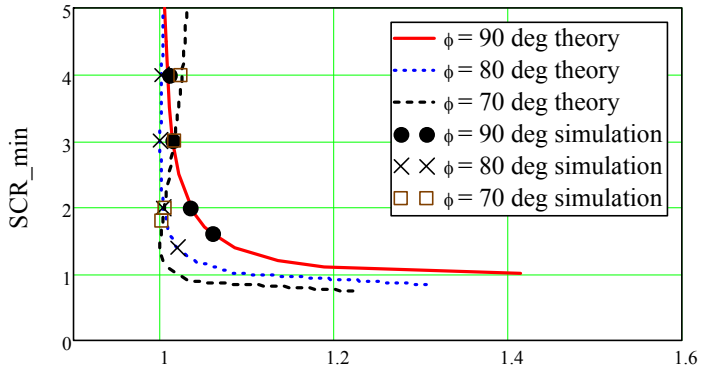


Figure 3.21: SCR – MVA$_{VSC}$ curve for different ϕ (Inverter operation)

Figure 3.20 and Figure 3.21 show a comparison of the simulation results and the analytical results when there is a transfer of *1 pu* of real power under rectifier operation and inverter operation for different ac system SCRs. The solid plots show the analytical results, and the markers (X, □, and •) represent EMT simulation results. As can be seen, the two are in agreement. The $SCR_{\_min}$ values are the asymptotic values attained when the MVA becomes larger. The simulations confirm that the analytical equations used in the previous section are accurate in predicting the behaviour of the VSCs.

3.5.2 Reactive Support at PCC Validation

Section 3.4.4 has shown that when the finite MVA ratings of the VSC are considered, the minimum required SCR ($SCR_{\_min}$) to transmit rated power can be decreased by adding the additional reactive power Q_c at the PCC. The validation used here is to reproduce, by simulation, the curve of *SCR* versus the percentage of reactive power Q_c support at the PCC considering a VSC with an MVA rating of *1.12 pu* (i.e., Q_{vsc} = *0.5 pu* at rated power).

The curve in Figure 3.22 shows a comparison of the simulation results and the analytical results when there is a transfer of *1 pu* of real power under rectifier operation for ac system $\phi = 80°$. The solid plots show the analytical results, and the triangle markers represent EMT simulation results. If no reactive power is supplied at the PCC, as in Figure 3.16 (see Figure 3.8 also), the minimum required SCR for transmitting rated power is *2*. However, when reactive power Q_c is supplied at PCC, the minimum required SCR can be reduced. For example, when the 7% reactive power support at PCC, the VSC can operate at as low SCR as *1.7*. The simulations confirm that the analytical equations used in the previous section are accurate in predicting the behaviour of the VSCs.

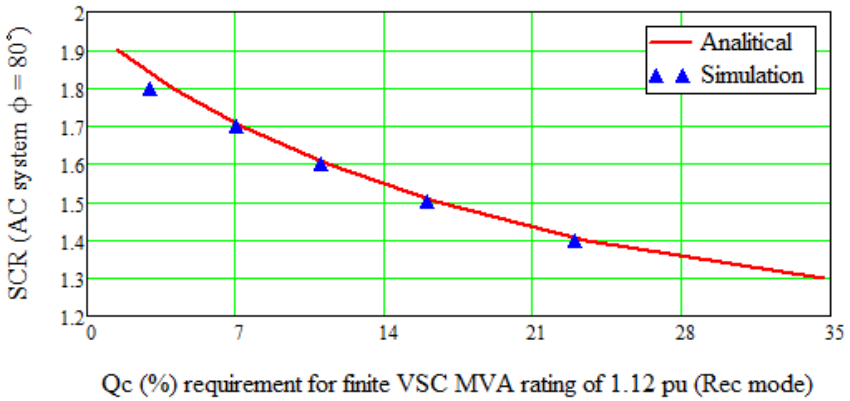


Figure 3.22: SCR – Q_C % curve for $\phi = 80°$ (Rectifier operation)

3.6 Impact of the SCR on PLL Gains

As mentioned in the previous section, as the SCR approaches its theoretical minimum limit, $SCR_{\_min}$, the converter becomes more difficult to control. The optimal controller gains of the VSC model were selected by using optimization enabled electromagnetic transient simulation (OE_EMTS). (More details on control parameter optimization using OE_EMTS will be introduced in Chapter 4). The EMT simulation studies showed that the parameters of the phase locked loop (PLL) play a very important role in system steady-state and system transient performance. However, stable operation was less sensitive to adjustments in the parameters of the outer loop controllers.

The PLL provides an angle reference for the generation of firing pulses. This angular reference varies from *0°* to *360°* and tracks the angle of the PCC voltage waveform. The effects were studied on the one-terminal VSC system in Figure 3.19 with the ac system impedance angle of *80°*. For this case, theoretically, $SCR_{\_min}$ was *1.21* (rectifier operation) and *0.85* (inverter operation). In the simulations, the SCR was varied from *1.4* to *4* for rectifier operation and from *1.0* to *4* for inverter operation (the absolute lower limits of *1.21* and *0.85* in Table 3.3 were not practically achievable even with reduced PLL gains as discussed in the next part of this section). Steady state operation at all SCRs in this range was possible.

To investigate the dynamics of the converter, two types of disturbances were considered:

a) A sudden change in the converter load from full rectification to full inversion, and vice versa

b) A sudden change in the system impedance (i.e., the SCR).

In the simulation, the controller gains for the outer loops (i.e., ac voltage control and power control) were selected using a non-linear optimization method, simplex optimization [61] coupled with EMT simulation [62] [63] for an SCR of *2.0*. The optimal gains were selected for dc power order (with a 100 ms ramp) from rated power import (500 MW) to rated power export (-500 MW) at t = 2.5 second and back to rated power import at t = 4.5 second. The study showed the four PI controller gains have a very limited effect on the system dynamic performance than the PLL gains, and hence are unchanged for the VSC connected to the different SCR ac systems. Many simulations were carried out, and a few representative cases are presented in this section.

The angular reference signal θ (shown as *theta* in the plots) generated by the PLL tracks the voltage V_t of the PCC and is shown in the plots. The phase angle (shown as *th* in the plots) of the infinite bus (Thévenin source) voltage of the E_s is also plotted. In the simulation, *th* is a known quantity and does not require measurement. The phase angle difference between the angles of V_t and of E_s, (i.e., *theta – th*, shown as *Delta* in the plots) is a measure of how quickly the system settles down into a stable steady state as it directly affects the active power transfer between V_t and E_s terminals.

In the first set of simulations, the dc power was ramped from *0* to *500 MW* or *1.0 pu* (rectifier operation), held there for *2 s*, then ramped to *-500 MW* (inverter operation), and then again ramped to *+500 MW* after *2 s*. Figure 3.23 shows the response of the power and the phase angle difference (*Delta*) for a strong system with *SCR = 4.0*. The large gains of $K_p = 100$ and $K_i = 500$ for the proportional and integral gains of the PLL were used (see Table 3.10 for the parameters and a diagram). The ac voltage waveforms E_s at the infinite bus (Thévenin source) and V_t at the PCC are also shown over a *100 ms*

interval starting at *2.5 s* (the instant where a step is applied), along with the tracked phase angles. As can be seen, the power response tracks the order very closely, and the phase angle difference also shows a fast response because the PLL is able to lock into the PCC voltage very quickly.

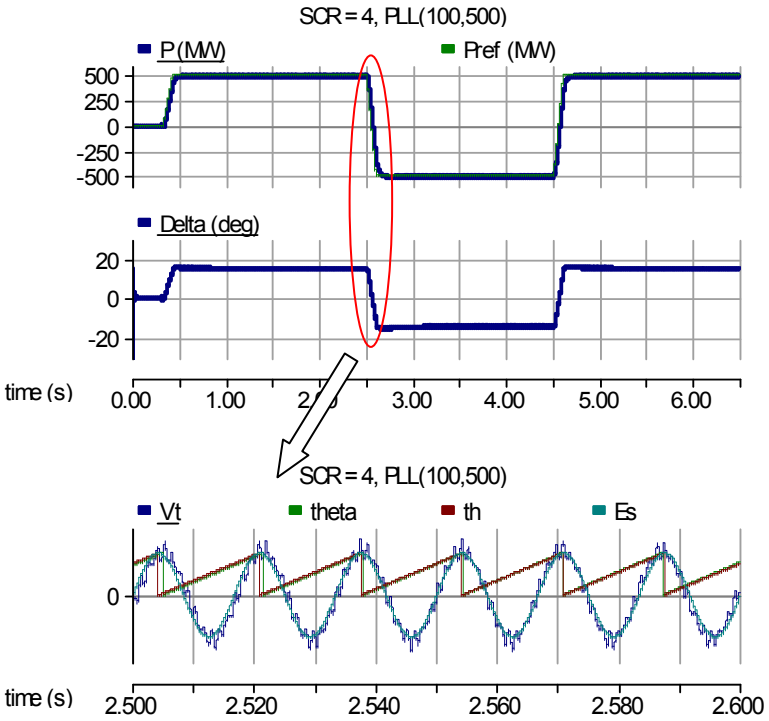


Figure 3.23: Load change for SCR = 4, PLL (K_p=100, K_i=500)

However, with the same large PLL gains, Figure 3.24 shows that for a weak system with *SCR = 1.6* the tracking is poor, and after the ramp changes the system becomes unstable and is unable to recover. The sudden power change causes a much bigger difference in *Delta* with the smaller SCR (43° to -36.8° for a SCR = 1.6 system) than in the case with the larger SCR (15.1° to -14.4° for a SCR = 4 system), so having too high a gain on the PLL results in the loss of the phase lock. The situation can be rectified by reducing the PLL gains by a factor of *10* to $K_p = 10$ and $K_i = 50$. The PLL is then able to maintain lock and power order changes can be accommodated, as shown in Figure 3.25. However,

as seen by the trace of *Delta*, there is an overshoot in the response, and also the settling time is larger than that for strong system with higher gains (0.6 s for a SCR = 1.6 system compared to 0.1 s for a SCR = 4 system).

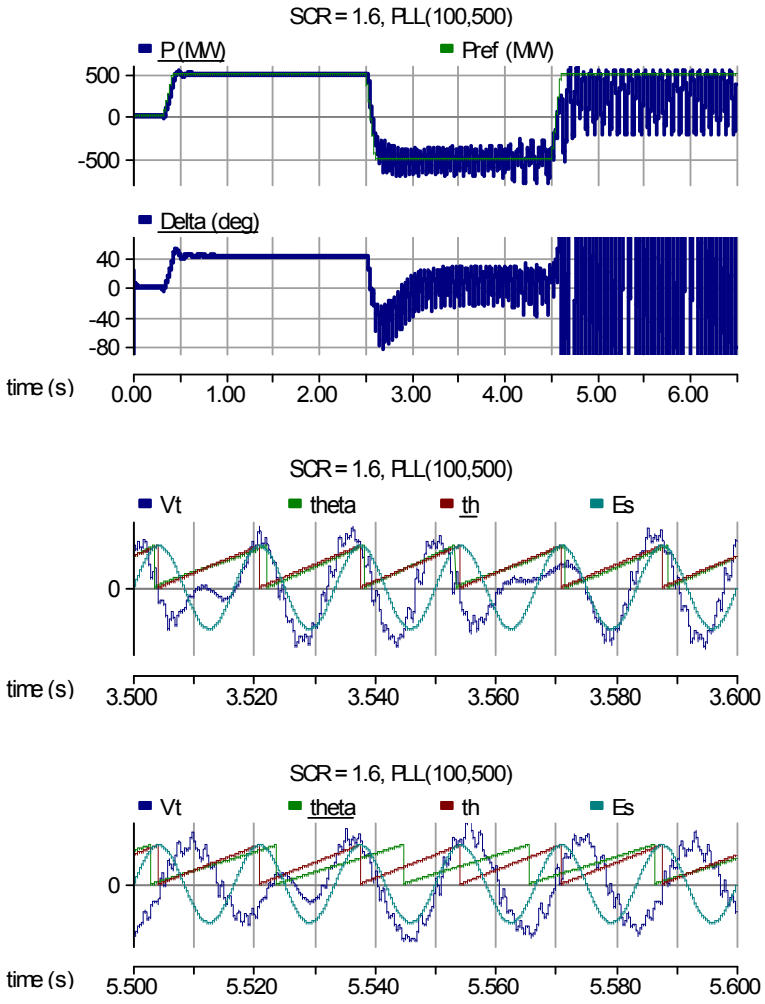


Figure 3.24: Load change for SCR=1.6, PLL (K_p=100, K_i=500)

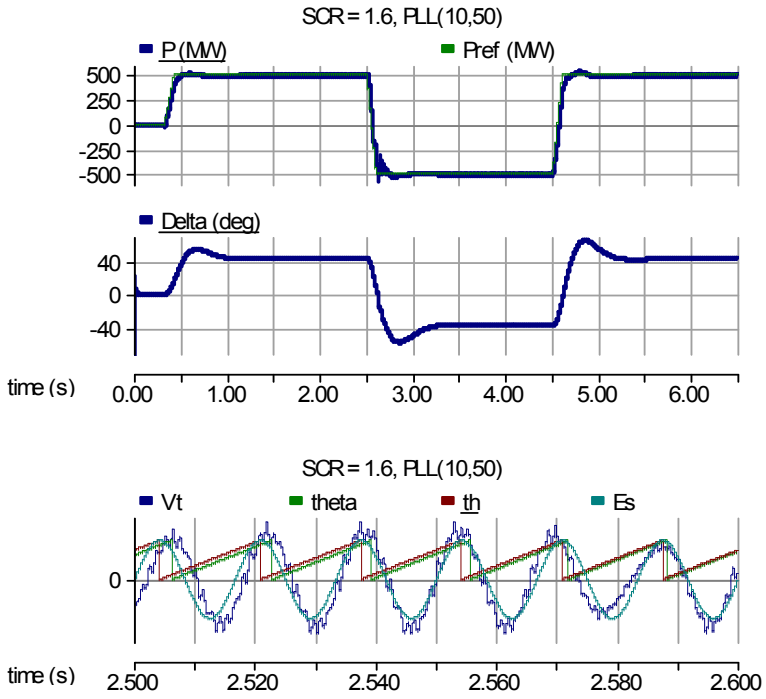


Figure 3.25: Load change for SCR = 1.6, PLL (K_p=10, K_i=50)

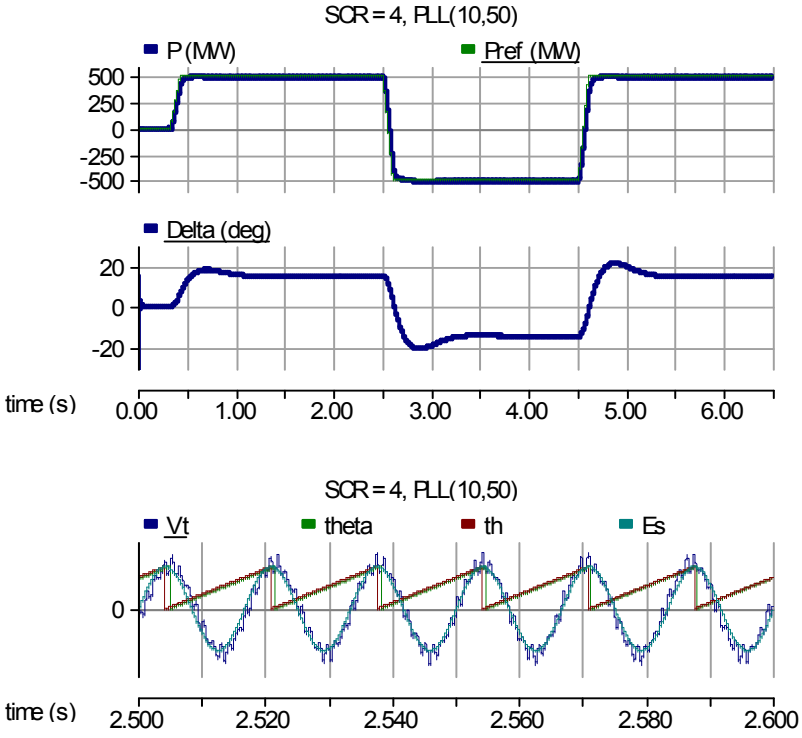


Figure 3.26: Load change for SCR = 4, PLL (K_p=10, K_i=50)

The above simulations suggest that one way of ensuring stable performance for all SCRs in the expected range of SCRs is to select the PLL gains that work with the lowest expected SCR. Figure 3.26 shows the performance of the higher SCR system (*SCR = 4*) with lower gains. The response is a little under-damped compared to the case in Figure 3.23 where the gains are higher. However, it is still adequate as seen by the crisp power response.

In the second set of simulations, the load was fixed and the ac system impedance was changed so that the SCR changed in steps from *4* to *1.6* to *1.8* to *2.0* and then back to *4*. The plots of Figure 3.27 and Figure 3.28 are for inverter operation. The dc power is *500 MW* or *1.0 pu*. The larger PLL gains (K_p *=100,* K_i *=500*) give good transient performance for SCRs higher than *2*, but unstable transient performance for SCRs lower than *2*. The smaller PLL gains (K_p *=10,* K_i *=50*) give moderate transient performance for both high SCR operation and low SCR operation.

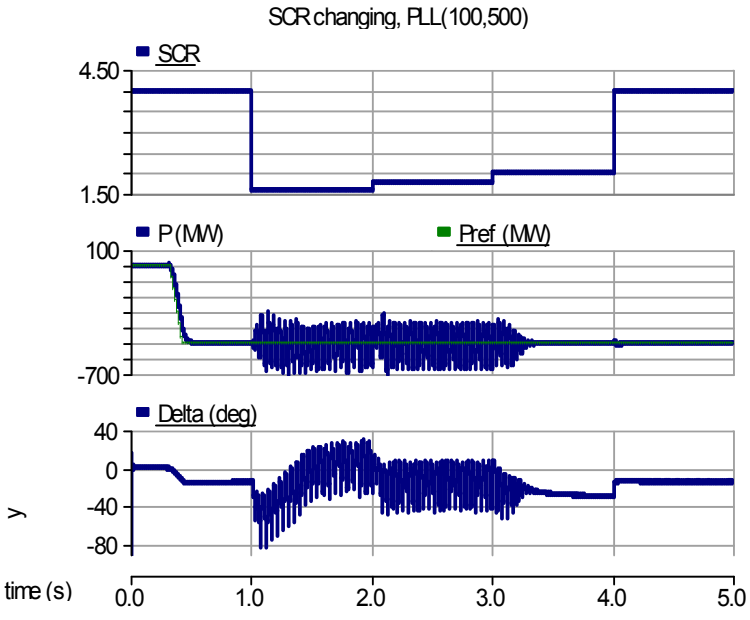


Figure 3.27: SCR change for PLL (K_p=100, K_i=500)

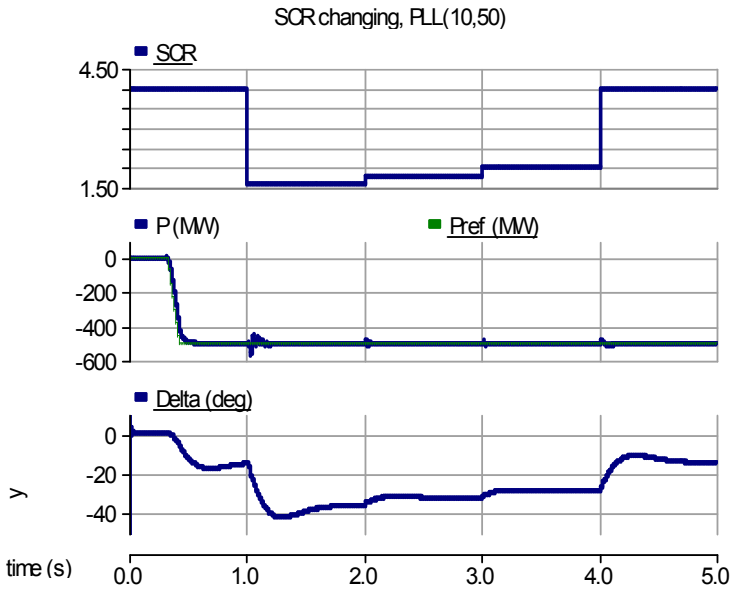


Figure 3.28: SCR change for PLL (K_p=10, K_i=50)

It should be noted that the transient performance shown in this section is an interesting observation based on many EMT simulation results. It is recognized that further research needs to be done to generalize this observation into a guideline for selection of the PLL gains or even the type of PLL. The work may be expanded by exploring more types of PLL algorithms, or conducting analytical study using frequency domain methods. The next section shows analytical approaches to selecting PLL gains, but the investigation of types of different PLL is outside the scope of the thesis.

3.7 Analysis of VSC PLL Transients Using Linearized State-space Analysis

In order to investigate the behaviour of PLL at different SCR levels, a small signal model is developed and discussed in this section. The analysis will show that the phenomena

discussed in the above section are large signal related, and cannot be correctly analyzed with the small signal model. The detail analysis and discussion are presented as follows.

3.7.1 State-space VSC Model

The methods in the linear system theory [78] are used to analyze the impact of PLL on the dynamic behaviour of VSC HVdc systems. Firstly the state-space equations of the system in Figure 3.29 is derived, in which the dynamics of the network, PLL, DQ decoupled control of VSC converter are all included. The ac network in Figure 3.29 is assumed to have a Thévenin impedance consisting of R_s and L_s; the capacitor C_f to represent the high pass filter. Although this form has been assumed in this thesis, if more detail is available, the formulation can easily be extended to handle this. The VSC side is modeled by a phase reactor L, a loss resistance R, and a source V_c representing the VSC's internal voltage.

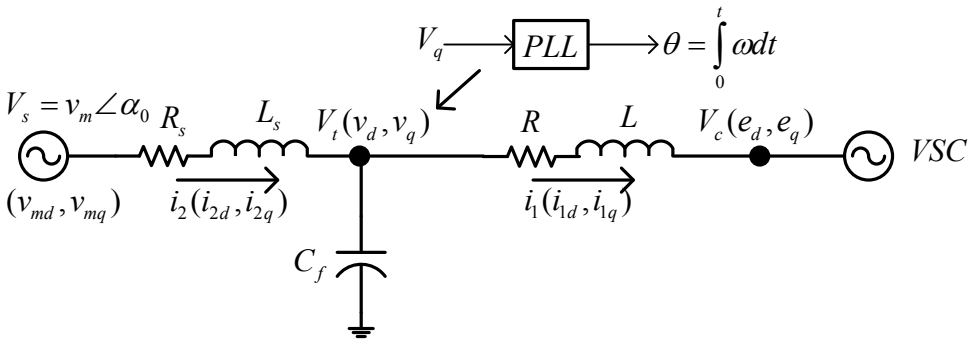
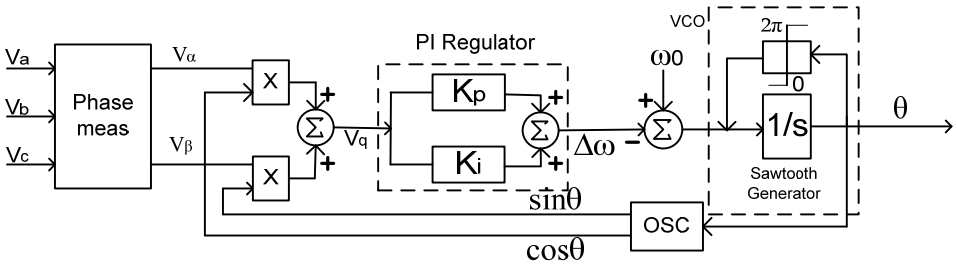


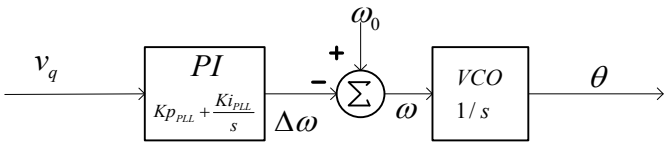
Figure 3.29: VSC system for linearization analysis

The control block diagram of the system can be represented as in Figure 3.30, which includes the PLL control, the voltage and the current measurement delay, the inner current (i_d, i_q) control loop and the outer power (P), ac voltage (v_{ac}) control loop. The PLL and its linearized model are shown in Figure 3.30 (a) [53] and (b), in which the P-I

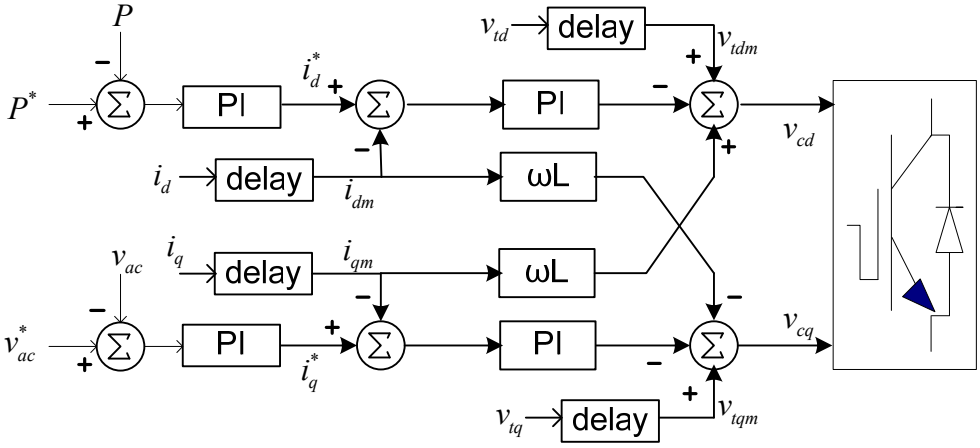
loop filter acts on the phase error signal and feeds the Voltage Controlled Oscillator (VCO). The VCO also has a free running frequency input ω_0. The phase error is actually v_q, the q-axis voltage at the PLL control point, which happens to be $v_t \sin(\theta)$, which is essentially proportional to the θ when θ is small. This PLL is based on the Siemens Transvektor control system discussed in [79] [80]. The inner and the outer control loop and the measurement delay blocks are shown in Figure 3.30 (c).



(a) PLL Topology [53]



(b) PLL Transfer Function



(c) dq decoupled control

Figure 3.30: Control block diagram of the VSC system

The state-space model derived in this thesis will include the ac system shown in Figure 3.29 and the VSC controls shown in Figure 3.30. The detailed procedure to develop the state-space model will be introduced as follows.

Firstly the ac system network equations in *abc* frame can be written as,

$$\begin{aligned} L\frac{di_{1abc}}{dt} + Ri_{1abc} &= v_{tabc} - v_{cabc} \\ L_s\frac{di_{2abc}}{dt} + R_s i_{2abc} &= v_{sabc} - v_{tabc} \\ C_f\frac{dv_{tabc}}{dt} &= i_{2abc} - i_{1abc} \end{aligned} \qquad 3\text{-}22$$

In order to represent the system equations in the same coordinates (*dq0* frame) as the VSC control, the Park transformation in equation 3-23 is used, in which the primary system *q* axis leads *d* axis,

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos\theta & \cos(\theta-\frac{2\pi}{3}) & \cos(\theta+\frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta-\frac{2\pi}{3}) & -\sin(\theta+\frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \qquad 3\text{-}23$$

The ac system network equations in *dq0* frame will become,

$$\begin{aligned} LT\frac{dT^{-1}i_{1dq0}}{dt} + Ri_{1dq0} &= v_{tdq0} - v_{cdq0} \\ L_sT\frac{dT^{-1}i_{2dq0}}{dt} + R_s i_{2dq0} &= v_{sdq0} - v_{tdq0} \\ C_fT\frac{dT^{-1}v_{tdq0}}{dt} &= i_{2dq0} - i_{1dq0} \end{aligned} \qquad 3\text{-}24$$

Hence, in a synchronous grid *dq0* reference frame with the *d* axis chosen aligned with the PLL control voltage v_t, the dynamic equations of the ac system network in Figure 3.29 can be written as,

$$\begin{aligned} L\frac{d}{dt}\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} &= \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} - \begin{bmatrix} v_{cd} \\ v_{cq} \end{bmatrix} - \omega L \begin{bmatrix} -i_{1q} \\ i_{1d} \end{bmatrix} - R\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} \\ L_s\frac{d}{dt}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} &= \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} - \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} - \omega L_s \begin{bmatrix} -i_{2q} \\ i_{2d} \end{bmatrix} - R_s\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} \\ C_f\frac{d}{dt}\begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} &= \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} - \begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} - \omega C_f \begin{bmatrix} -v_{tq} \\ v_{td} \end{bmatrix} \end{aligned} \qquad 3\text{-}25$$

Secondly the control equations are represented. Since the control loop inputs (the voltage v_t and current i_1 at the PLL control point in *dq* coordinates) are measured quantities from the physical variables in the network, for full accuracy, the dynamics of the measurement transducers must be included. In this thesis, they are taken as first order lags that provide high frequency noise filtering as shown in Figure 3.30, where v_{tdm}, v_{tqm} and i_{1dm}, i_{1qm} are the measured values for the actual values v_{td}, v_{tq} and i_{1d}, i_{1q} respectively. Thus, the transfer function can be written as equation 3-26, where T_{mvd}, T_{mvq} and T_{mid}, T_{miq} are the time constants for the measurement controls.

$$\begin{aligned} v_{tdm} &= (\frac{1}{1+sT_{mvd}})v_{td} \\ v_{tqm} &= (\frac{1}{1+sT_{mvq}})v_{tq} \\ i_{1dm} &= (\frac{1}{1+sT_{mid}})i_{1d} \\ i_{1qm} &= (\frac{1}{1+sT_{miq}})i_{1q} \end{aligned} \qquad 3\text{-}26$$

The outer loop controllers and inner loop controllers in Figure 3.30 can be written as equation 3-27 and equation 3-28 respectively, where *m* is the modulation index. Here the

controllers work on measured values rather than actual values as would be the case in real life. Here P_{ref} and v_{ref} are reference values for real power control and ac voltage control respectively, Kp_p, Ki_P and Kp_v, Ki_v are the PI control parameters for real power control and ac voltage control respectively.

$$\begin{aligned} i_d^* &= \left[P_{ref} - (v_{tdm} i_{1dm} + v_{tqm} i_{1qm}) \right] (Kp_P + \frac{Ki_P}{s}) \\ i_q^* &= (v_{ref} - \sqrt{v_{tdm}^2 + v_{tqm}^2})(Kp_V + \frac{Ki_V}{s}) \end{aligned} \tag{3-27}$$

$$\begin{aligned} v_{cd} &= \left[v_{tdm} + i_{1qm} \cdot \omega L - (i_d^* - i_{1dm})(Kp_1 + \frac{Ki_1}{s}) \right] m \\ v_{cq} &= \left[v_{tqm} - i_{1dm} \cdot \omega L - (i_q^* - i_{1qm})(Kp_2 + \frac{Ki_2}{s}) \right] m \end{aligned} \tag{3-28}$$

The dynamics of the PLL controller can be represented by equation 3-29, where θ is the phase error outputted from PLL and ω is the angular frequency. Here Kp_{PLL}, and Ki_{PLL} are the PI control parameters of the PLL.

$$\begin{cases} \theta = \int_0^t \omega dt \\ \omega = \omega_0 + v_{tq} (\frac{K_{I\,PLL}}{s} + K_{P\,PLL}) \end{cases} \tag{3-29}$$

In order to develop the state-space equations for the system, the above equations must be linearized around the operating point and converted to the state variable form. Some of the equations are already linear (such as 3-29), but others are nonlinear and must be linearized (such as 3-27). This will yield the state-space model [78] of the whole VSC system as in equation 3-30.

$$\begin{aligned} \dot{\mathbf{x}} &= \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \\ y &= \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \end{aligned} \tag{3-30}$$

Here the state vector will turn out to be of dimension 16 as discussed below, and the input variable $\mathbf{u} = \begin{bmatrix} P_{ref} & v_{ref} \end{bmatrix}$ is of dimension 2. Any other desired variables of interest (y) in the circuit or controls are now calculated as linear combinations of the state vector and inputs using suitable matrices C and D. The relevant equations are subsets of equation 3-30. Sometimes, the system can be simpler, i.e., when we are analyzing only the inner loop control behaviour using i_d^* and i_q^* as inputs. However, in order to analysis the whole system behavior, the outer loop control and the PLL are represented as well using P_{ref} and v_{ref} as inputs in this model.

Derivation of the full form of equation 3-30 is now discussed below, and is finally given in section 3.7.1.7.

3.7.1.1 Measurement control state variable equations

From transfer function equations 3-26, the state space equations related to the measurement controls can be written as equations 3-31 and 3-32, in which the state variables $x_{01}, x_{02}, x_{03}, x_{04}$ are chosen to convert the transfer function to state space equations.

$$\frac{v_{tdm}}{v_{td}} = \frac{1}{1+sT_{mvd}} = \frac{\frac{1}{T_{mvd}}}{s+\frac{1}{T_{mvd}}} = \frac{\beta_{001}}{s+\alpha_{001}} \rightarrow \begin{cases} \dot{x}_{01} = -\alpha_{001}x_{01} + v_{td} \\ v_{tdm} = \beta_{001}x_{01} \end{cases}$$

$$\frac{v_{tqm}}{v_{tq}} = \frac{1}{1+sT_{mvq}} = \frac{\frac{1}{T_{mvq}}}{s+\frac{1}{T_{mvq}}} = \frac{\beta_{002}}{s+\alpha_{002}} \rightarrow \begin{cases} \dot{x}_{02} = -\alpha_{002}x_{02} + v_{tq} \\ v_{tqm} = \beta_{002}x_{02} \end{cases} \qquad \text{3-31}$$

$$\frac{i_{1dm}}{i_{1d}}=\frac{1}{1+sT_{mid}}=\frac{\frac{1}{T_{mid}}}{s+\frac{1}{T_{mid}}}=\frac{\beta_{003}}{s+\alpha_{003}}\rightarrow\begin{cases}\dot{x}_{03}=-\alpha_{003}x_{03}+i_{1d}\\ i_{1dm}=\beta_{003}x_{03}\end{cases}$$
$$\frac{i_{1qm}}{i_{1q}}=\frac{1}{1+sT_{miq}}=\frac{\frac{1}{T_{miq}}}{s+\frac{1}{T_{miq}}}=\frac{\beta_{004}}{s+\alpha_{004}}\rightarrow\begin{cases}\dot{x}_{04}=-\alpha_{004}x_{04}+i_{1q}\\ i_{1qm}=\beta_{004}x_{04}\end{cases} \quad 3\text{-}32$$

3.7.1.2 Outer control state variable equations

The outer loop control equation 3-27 can be linearized around the operating point to yield the state-space equations 3-33 and 3-34 for i_d^* and i_q^* respectively, with x_1, x_2 being the state variables.

$$\begin{cases}u=P_{ref}-(v_{tdm}i_{1dm}+v_{tqm}i_{1qm})\\ i_d^*=u(Kp_P+\frac{Ki_P}{s})\end{cases}\rightarrow\frac{i_d^*}{u}=\frac{Ki_P}{s}+Kp_P=\frac{\beta_{01}}{s}+\lambda_1$$
$$\rightarrow\begin{cases}\dot{x}_1=P_{ref}-(v_{tdm}i_{1dm}+v_{tqm}i_{1qm})\\ i_d^*=\beta_{01}x_1+\lambda_1(P_{ref}-(v_{tdm}i_{1dm}+v_{tqm}i_{1qm}))\end{cases} \quad 3\text{-}33$$

$$\begin{cases}u=V_{ref}-\sqrt{v_{tdm}^2+v_{tqm}^2}\\ i_q^*=u(Kp_V+\frac{Ki_V}{s})\end{cases}\rightarrow\frac{i_q^*}{u}=\frac{Ki_V}{s}+Kp_V=\frac{\beta_{02}}{s}+\lambda_2$$
$$\rightarrow\begin{cases}\dot{x}_2=V_{ref}-\sqrt{v_{tdm}^2+v_{tqm}^2}\\ i_q^*=\beta_{02}x_2+\lambda_2(V_{ref}-\sqrt{v_{tdm}^2+v_{tqm}^2})\end{cases} \quad 3\text{-}34$$

3.7.1.3 Inner control state variable equations

The inner loop control equation 3-28 yields state space equations 3-35 and 3-36 for i_d and i_q respectively, with x_3, x_4 being the state variables.

$$(i_d^* - i_{1dm})(Kp_1 + \frac{Ki_1}{s}) = v_{tdm} + i_{1qm} \cdot \omega L - \frac{v_{cd}}{m} \rightarrow \begin{cases} u = i_d^* - i_{1dm} \\ y = v_{tdm} + i_{1qm} \cdot \omega L - \frac{v_{cd}}{m} \\ \frac{y}{u} = \frac{Ki_1}{s} + Kp_1 = \frac{\beta_{03}}{s} + \lambda_3 \end{cases} \quad 3\text{-}35$$

$$\rightarrow \begin{cases} \dot{x}_3 = i_d^* - i_{1dm} \\ v_{tdm} + i_{1qm} \cdot \omega L - \frac{v_{cd}}{m} = \beta_{03} x_3 + \lambda_3 (i_d^* - i_{1dm}) \end{cases}$$

$$(i_q^* - i_{1qm})(Kp_2 + \frac{Ki_2}{s}) = v_{tqm} - i_{1dm} \cdot \omega L - \frac{v_{cq}}{m} \rightarrow \begin{cases} u = i_q^* - i_{1qm} \\ y = v_{tqm} - i_{1dm} \cdot \omega L - \frac{v_{cq}}{m} \\ \frac{y}{u} = \frac{Ki_2}{s} + Kp_2 = \frac{\beta_{04}}{s} + \lambda_4 \end{cases} \quad 3\text{-}36$$

$$\rightarrow \begin{cases} \dot{x}_4 = i_q^* - i_{1qm} \\ v_{tqm} - i_{1dm} \cdot \omega L - \frac{v_{cq}}{m} = \beta_{04} x_4 + \lambda_4 (i_q^* - i_{1qm}) \end{cases}$$

3.7.1.4 PLL control state variable equations

The PLL control equation 3-29 yields the state-space equations 3-37, with θ, ω being the state variables.

$$\begin{cases} \frac{d\theta}{dt} = \omega \\ \frac{d\omega}{dt} = K_{IPLL} v_{tq} + K_{PPLL} \frac{dv_{tq}}{dt} \end{cases} \quad 3\text{-}37$$

$$\rightarrow \frac{d}{dt}\begin{bmatrix} \theta \\ \omega \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} \theta \\ \omega \end{bmatrix} + \begin{bmatrix} 0 \\ K_{IPLL} v_{tq} + K_{PPLL} \frac{dv_{tq}}{dt} \end{bmatrix}$$

3.7.1.5 Control state variable equations

Rearrange equations 3-31 to 3-37, the 10 control state space equations are,

$$\begin{cases} \dot{x}_{01} = -\alpha_{001} x_{01} + v_{td} \\ \dot{x}_{02} = -\alpha_{002} x_{02} + v_{tq} \\ \dot{x}_{03} = -\alpha_{003} x_{03} + i_{1d} \\ \dot{x}_{04} = -\alpha_{004} x_{04} + i_{1q} \\ \dot{x}_{1} = P_{ref} - (\beta_{001} x_{01} \beta_{003} x_{03} + \beta_{002} x_{02} \beta_{004} x_{04}) \\ \dot{x}_{2} = v_{ref} - \sqrt{(\beta_{001} x_{01})^2 + (\beta_{002} x_{02})^2} \\ \dot{x}_{3} = \beta_{01} x_1 + \lambda_1 (P_{ref} - (\beta_{001} x_{01} \beta_{003} x_{03} + \beta_{002} x_{02} \beta_{004} x_{04}) - \beta_{003} x_{03} \\ \dot{x}_{4} = \beta_{02} x_2 + \lambda_2 \left(v_{ref} - \sqrt{\beta_{001}^2 x_{01}^2 + \beta_{002}^2 x_{02}^2} \right) - \beta_{004} x_{04} \\ \dot{\theta} = \omega \\ \dot{\omega} - K_{PPLL} \dot{v}_{tq} = K_{IPLL} v_{tq} \end{cases} \quad 3\text{-}38$$

And the outputs of the controllers are,

$$\begin{cases} v_{tdm} = \beta_{001} x_{01} \\ v_{tqm} = \beta_{002} x_{02} \\ i_{1dm} = \beta_{003} x_{03} \\ i_{1qm} = \beta_{004} x_{04} \\ i_d^* = \beta_{01} x_1 + \lambda_1 (P_{ref} - (v_{tdm} i_{1dm} + v_{tqm} i_{1qm})) \\ i_q^* = \beta_{02} x_2 + \lambda_2 (v_{ref} - \sqrt{v_{tdm}^2 + v_{tqm}^2}) \\ v_{tdm} + i_{1qm} \cdot \omega L - \dfrac{v_{cd}}{m} = \beta_{03} x_3 + \lambda_3 (i_d^* - i_{1dm}) \\ v_{tqm} - i_{1dm} \cdot \omega L - \dfrac{v_{cq}}{m} = \beta_{04} x_4 + \lambda_4 (i_q^* - i_{1qm}) \end{cases} \quad 3\text{-}39$$

Where

$$\begin{cases} \beta_{01} = Ki_P \\ \lambda_1 = Kp_P \end{cases} \quad \begin{cases} \beta_{02} = Ki_V \\ \lambda_2 = Kp_V \end{cases} \quad \begin{cases} \alpha_{001} = \beta_{001} = 1/T_{mvd} \\ \alpha_{002} = \beta_{001} = 1/T_{mvq} \\ \alpha_{003} = \beta_{003} = 1/T_{mid} \\ \alpha_{004} = \beta_{004} = 1/T_{miq} \end{cases} \quad 3\text{-}40$$

$$\begin{cases} \beta_{03} = Ki_1 \\ \lambda_3 = Kp_1 \end{cases} \quad \begin{cases} \beta_{04} = Ki_2 \\ \lambda_4 = Kp_2 \end{cases}$$

3.7.1.6 AC Network State Space Equations

Dynamic equation 3-25 for the ac network must also be linearized around the operating point. Since v_{sd}, v_{sq} and v_{cd}, v_{cq} in equation 3-25 are not state variables, they need be replaced by state variables. Assume that α_0 is the angle of the Thévenin source V_m relative to V_t (assumed to be the bus for the voltage angle reference, i.e., $V_t \angle 0$) and θ is the angle error from the PLL. The Thévenin source v_{sd} and v_{sq} can be written as,

$$v_s = \sqrt{\frac{2}{3}} v_m (\cos \omega_0 t + \alpha_0) \rightarrow \begin{cases} v_{sd} = v_m \cos\left[\theta - (\omega_0 t + \alpha_0)\right] \\ v_{sq} = v_m \sin\left[(\omega_0 t + \alpha_0) - \theta\right] \end{cases} \quad 3\text{-}41$$

Replacing equations 3-25 with equations 3-38, 3-39 and 3-41, we can rewrite the 6 dynamic equations of the ac network in linearized form in equation 3-42. Here $i_{1d}, i_{1q}, i_{12}, i_{2q}, v_{td}, v_{tq}$ are the state variables.

$$\begin{aligned} L\frac{d}{dt}\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} &= \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} - \omega L \begin{bmatrix} -i_{1q} \\ i_{1d} \end{bmatrix} - R\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} - \begin{bmatrix} m\beta_{001}x_{01} \\ m\beta_{002}x_{02} \end{bmatrix} - \begin{bmatrix} m\lambda_3\beta_{003} & m\omega L\beta_{004} \\ -m\omega L\beta_{003} & m\lambda_4\beta_{004} \end{bmatrix}\begin{bmatrix} x_{03} \\ x_{04} \end{bmatrix} \\ &\quad + \begin{bmatrix} m\beta_{03}x_3 \\ m\beta_{04}x_4 \end{bmatrix} + \begin{bmatrix} m\lambda_3\beta_{01}x_1 \\ m\lambda_4\beta_{02}x_2 \end{bmatrix} + \begin{bmatrix} m\lambda_3\lambda_1 P_{ref} \\ m\lambda_4\lambda_2 v_{ref} \end{bmatrix} - \begin{bmatrix} m\lambda_3\lambda_1\left(\beta_{001}x_{01}\beta_{003}x_{03} + \beta_{002}x_{02}\beta_{004}x_{04}\right) \\ m\lambda_4\lambda_2\sqrt{\beta_{001}^2 x_{01}^2 + \beta_{002}^2 x_{02}^2} \end{bmatrix} \\ L_s\frac{d}{dt}\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} &= -\omega L_s \begin{bmatrix} -i_{2q} \\ i_{2d} \end{bmatrix} - R_s\begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} - \begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} + \begin{bmatrix} v_m \cos\left[\theta - (\omega_0 t + \alpha_0)\right] \\ v_m \sin\left[(\omega_0 t + \alpha_0) - \theta\right] \end{bmatrix} \\ C_f\frac{d}{dt}\begin{bmatrix} v_{td} \\ v_{tq} \end{bmatrix} &= -\begin{bmatrix} i_{1d} \\ i_{1q} \end{bmatrix} + \begin{bmatrix} i_{2d} \\ i_{2q} \end{bmatrix} - \omega C_f \begin{bmatrix} -v_{tq} \\ v_{td} \end{bmatrix} \end{aligned} \quad 3\text{-}42$$

3.7.1.7 Overall VSC system state variable equations

From equations 3-38, and 3-42, the overall VSC system state space equations with 16 state variables can be represented as $M\dot{X} = A'X + B'U$, where M is already linearized and is shown in equation 3-43. However the terms $B'U$ and $A'X$ are still not fully linearized. This is because $B'U$ contains non-linear functions and $A'X$ contains terms like ωi_{1d} (see equation 3-44 and 3-46) which are products of state variables.

In order to complete the linearization as $M\Delta\dot{X} = A''\Delta X + B''\Delta U$, further steps are needed as shown in equation 3-45 and 3-47. From this, the state variable form can be obtained as $\Delta\dot{X} = A\Delta X + B\Delta U$, where $A = M^{-1}A''$ and $B = M^{-1}B''$. Hence eigenvalues of A can be used to determine the stability of the system.

$$M = \begin{array}{c} \\ 1 \\ 2 \\ 3 \\ 4 \\ 5 \\ 6 \\ 7 \\ 8 \\ 9 \\ 10 \\ 11 \\ 12 \\ 13 \\ 14 \\ 15 \\ 16 \end{array} \begin{array}{c} \begin{array}{cccccccccccccccc} 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 9 & 10 & 11 & 12 & 13 & 14 & 15 & 16 \end{array} \\ \begin{bmatrix} 1 & & & & & & & & & & & & & & & \\ & 1 & & & & & & & & & & & & & & \\ & & 1 & & & & & & & & & & & & & \\ & & & 1 & & & & & & & & & & & & \\ & & & & 1 & & & & & & & & & & & \\ & & & & & 1 & & & & & & & & & & \\ & & & & & & 1 & & & & & & & & & \\ & & & & & & & 1 & & & & & & & & \\ & & & & & & & & 1 & & & & & & & \\ & & & & & & & & & 1 & & & & & & -K_{PPLL} \\ & & & & & & & & & & L & & & & & \\ & & & & & & & & & & & L & & & & \\ & & & & & & & & & & & & L_s & & & \\ & & & & & & & & & & & & & L_s & & \\ & & & & & & & & & & & & & & C_f & \\ & & & & & & & & & & & & & & & C_f \end{bmatrix} \end{array} \qquad 3\text{-}43$$

$$X=\begin{bmatrix} x_{01} \\ x_{02} \\ x_{03} \\ x_{04} \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ \theta \\ \omega \\ i_{1d} \\ i_{1q} \\ i_{2d} \\ i_{2q} \\ v_d \\ v_q \end{bmatrix} \qquad B'U=\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ \mathrm{P}_{ref} \\ v_{ref} \\ \lambda_1 \mathrm{P}_{ref} \\ \lambda_2 v_{ref} \\ 0 \\ 0 \\ m\lambda_3\lambda_1 \mathrm{P}_{ref} \\ m\lambda_4\lambda_2 v_{ref} \\ v_m \cos\left[\theta-(\omega_0 t+\alpha_0)\right] \\ v_m \sin\left[(\omega_0 t+\alpha_0)-\theta\right] \\ 0 \\ 0 \end{bmatrix} \qquad \text{3-44}$$

$$\Delta X=\begin{bmatrix} \Delta x_{01} \\ \Delta x_{02} \\ \Delta x_{03} \\ \Delta x_{04} \\ \Delta x_1 \\ \Delta x_2 \\ \Delta x_3 \\ \Delta x_4 \\ \Delta\theta \\ \Delta\omega \\ \Delta i_{1d} \\ \Delta i_{1q} \\ \Delta i_{2d} \\ \Delta i_{2q} \\ \Delta v_d \\ \Delta v_q \end{bmatrix} \qquad B''\Delta U=\begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \\ \lambda_1 & 0 \\ 0 & \lambda_2 \\ 0 & 0 \\ 0 & 0 \\ m\lambda_3\lambda_1 & 0 \\ 0 & m\lambda_4\lambda_2 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \Delta \mathrm{P}_{ref} & \Delta v_{ref} \end{bmatrix} \qquad \text{3-45}$$

$$A' =$$

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	$-\alpha_{001}$														1	
2		$-\alpha_{002}$														1
3			$-\alpha_{003}$								1					
4				$-\alpha_{004}$								1				
5	$-\beta_{001}\beta_{003}x_{03}$	$-\beta_{002}\beta_{004}x_{04}$														
6	$\frac{-\beta_{001}^2 x_{01}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$\frac{-\beta_{002}^2 x_{02}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$														
7	$-\beta_{001}\beta_{003}x_{03}\lambda_1$	$-\beta_{002}\beta_{004}x_{04}\lambda_1$	$-\beta_{003}$		β_{01}											
8	$\frac{-\beta_{001}^2 x_{01}\lambda_2}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$\frac{-\beta_{002}^2 x_{02}\lambda_2}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$		$-\beta_{004}$		β_{02}										
9										1						
10																$K_{I\,PLL}$
11	$-m\beta_{001}-m\lambda_3\lambda_1\beta_{001}\beta_{003}x_{03}$	$-m\lambda_3\lambda_1\beta_{002}\beta_{004}x_{04}$	$-m\lambda_3\beta_{003}$	$-m\omega L\beta_{004}$	$m\lambda_3\beta_{01}$		$m\beta_{03}$				$-R$	ωL			1	
12	$\frac{-m\lambda_4\lambda_2\beta_{001}^2 x_{01}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$-m\beta_{002}-\frac{m\lambda_4\lambda_2\beta_{002}^2 x_{02}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$m\omega L\beta_{003}$	$-m\lambda_4\beta_{004}$		$m\lambda_4\beta_{02}$		$m\beta_{04}$			$-\omega L$	$-R$				1
13													$-R_s$	ωL_s	-1	
14													$-\omega L_s$	$-R_s$		-1
15											-1		1			ωC_f
16												-1		1	$-\omega C_f$	

$$A'' =$$

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1	$-\alpha_{001}$														1	
2		$-\alpha_{002}$														1
3			$-\alpha_{003}$								1					
4				$-\alpha_{004}$								1				
5	$-\beta_{001}\beta_{003}x_{03}$	$-\beta_{002}\beta_{004}x_{04}$	$-\beta_{001}\beta_{003}x_{01}$	$-\beta_{002}\beta_{004}x_{02}$												
6	$\frac{-\beta_{001}^2 x_{01}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$\frac{-\beta_{002}^2 x_{02}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$														
7	$-\beta_{001}\beta_{003}x_{03}\lambda_1$	$-\beta_{002}\beta_{004}x_{04}\lambda_1$	$-\beta_{003}-\beta_{001}\beta_{003}x_{03}\lambda_1$	$-\beta_{002}\beta_{004}x_{02}\lambda_1$	β_{01}											
8	$\frac{-\beta_{001}^2 x_{01}\lambda_2}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$\frac{-\beta_{002}^2 x_{02}\lambda_2}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$		$-\beta_{004}$		β_{02}										
9										1						
10																K_{IPLL}
11	$-m\beta_{001}-m\lambda_3\lambda_1\beta_{001}\beta_{003}x_{03}$	$-m\lambda_3\lambda_1\beta_{002}\beta_{004}x_{04}$	$-m\lambda_3\beta_{003}-m\lambda_3\lambda_1\beta_{001}\beta_{003}x_{03}$	$-m\omega L\beta_{004}-m\lambda_3\lambda_1\beta_{002}\beta_{004}x_{02}$	$m\lambda_3\beta_{01}$		$m\beta_{03}$			$-mL\beta_{004}x_{04}+Li_{1q}$	$-R$	ωL			1	
12	$\frac{-m\lambda_4\lambda_2\beta_{001}^2 x_{01}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$-m\beta_{002}-\frac{m\lambda_4\lambda_2\beta_{002}^2 x_{02}}{\sqrt{(\beta_{001}x_{01})^2+(\beta_{002}x_{02})^2}}$	$m\omega L\beta_{003}$	$-m\lambda_4\beta_{004}$		$m\lambda_4\beta_{02}$		$m\beta_{04}$		$mL\beta_{003}x_{03}-Li_{1d}$	$-\omega L$	$-R$				1
13																
14									$-v_m\sin(\theta-\alpha_0)$	$L_s i_{2q}$			$-R_s$	ωL_s	-1	
15									$-v_m\cos(\alpha_0-\theta)$	$-L_s i_{2d}$			$-\omega L_s$	$-R_s$		-1
16										$C_f v_q$	-1		1			ωC_f
										$-C_f v_d$		-1		1	$-\omega C_f$	

3.7.2 Model Verification

In order to validate the small signal model, the time-domain response of the small signal model was obtained using MATLAB and compared with the time-domain response of the non-linear model simulated on the electromagnetic transient simulation program PSCAD/EMTDC.

The system shown in Figure 3.29 was used for the verification, with the VSC now replaced with a detailed 2-level pulse width modulated converter model. The system parameters are shown in Table 3.11 and the control parameters are shown in Table 3.12. The PLL gains are varied from low values to high values in order to evaluate the effect of PLL gains on the behavior of the VSC converter, while other controller gains are kept constant. Early section showed that the gains of the VSC inner and outer PI controllers have limited effect on system transient performance compared to the gains of the PLL.

Table 3.11: VSC-HVdc System Parameters

Equivalent ac system V_m(base)	1.0 kV, 60 Hz
Equivalent ac system SCR	1.6 or 4.0
Equivalent ac system impedance angle	80°
Rated dc power rating (base)	1.0 MW
PLL controlled voltage V_t	1.0 kV, 60 Hz
Converter reactance L	0.15 pu (0.398 mH)
Passive filter C_f	15% (398 μF)

Table 3.12: VSC-HVdc Control Parameters

PLL ($Kp_{PLL} = K_p$, $Ki_{PLL} = 5K_p$)	K_p varies from low to high values
Measurement (T_{mvd}, T_{mvq})	(0.02, 0.02)
Measurement (T_{mid}, T_{miq})	(0.0012, 0.0012)
Power controller (Kp_P, Ki_P)	(0.5, 50)
Ac voltage controller (Kp_v, Ki_v)	(0.5, 50)
Inner i_d controller (Kp_1, Ki_1)	(2, 100)
Inner i_q controller (Kp_2, Ki_2)	(2, 100)

3.7.2.1 Transient response of the VSC model

The small signal model was exhaustively compared with the full EMT simulation of the converter. A few sample results are shown here. In the figures, P_ss and Vac_ss are results from small signal model, P_EMT and Vac_EMT are results from EMT model. Results of of Figure 3.31 and Figure 3.32 show comparison of the power responses obtained from the detailed non-linear model and the small signal model for a power order step change from 1.0 pu to 0.95 pu and from -1.0 pu to -0.95 pu respectively. The simulations are for SCR = 1.6 and the lower PLL gain of $K_p = 10$, (i.e., $Kp_{PLL} = 10$ and $Ki_{PLL} = 50$). Figure 3.33, Figure 3.34 show the EMT and small signal time responses for higher PLL gain of $K_p = 100$, (i.e., $Kp_{PLL} = 100$ and $Ki_{PLL} = 500$).

Both figures show that the small signal model is highly accurate as the two traces are nearly identical. They also show that operations are stable for both lower and higher PLL gains and at the higher gains with a smaller settling time than that at the lower gains, but higher transient overshoot.

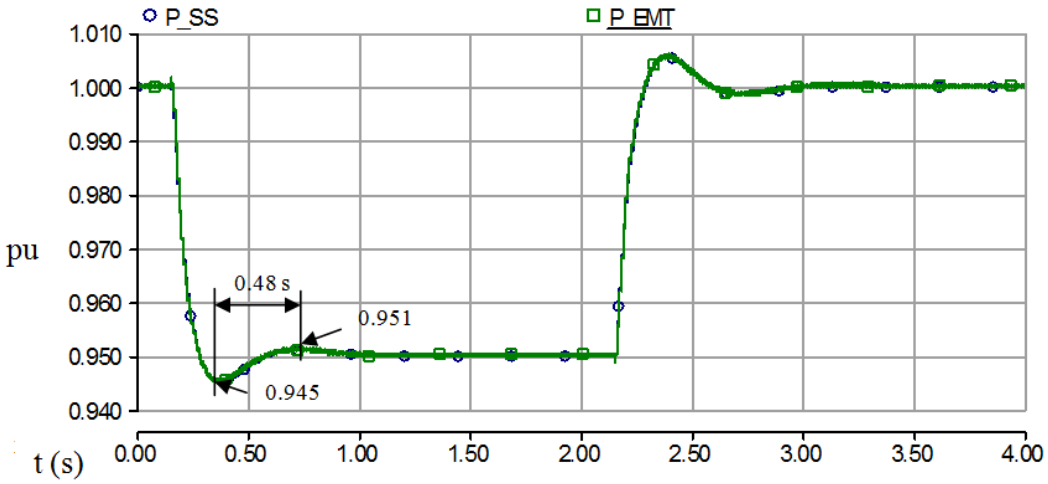


Figure 3.31: Power step change from 1.0 pu to 0.95 pu for SCR=1.6, PLL (10,50)

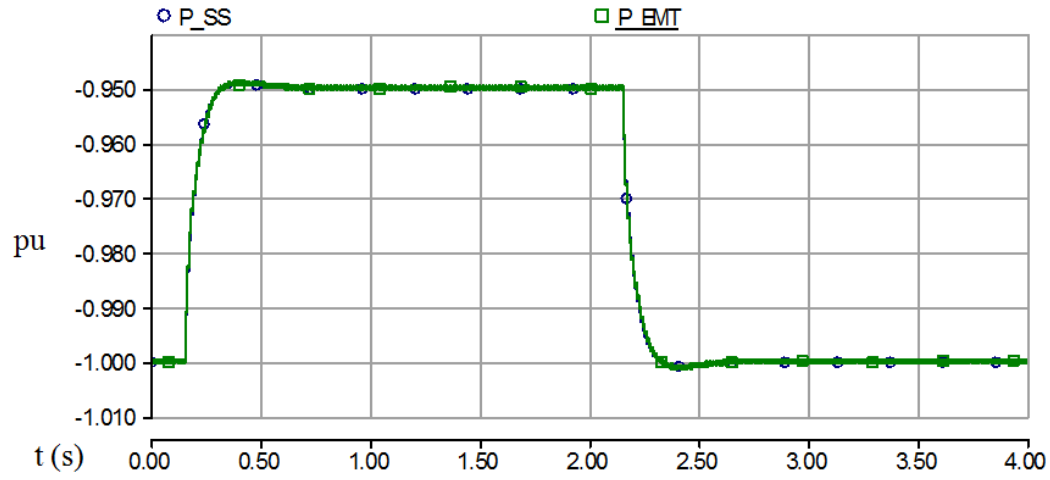


Figure 3.32: Power step change from -1.0 pu to -0.95 pu for SCR=1.6, PLL (10,50)

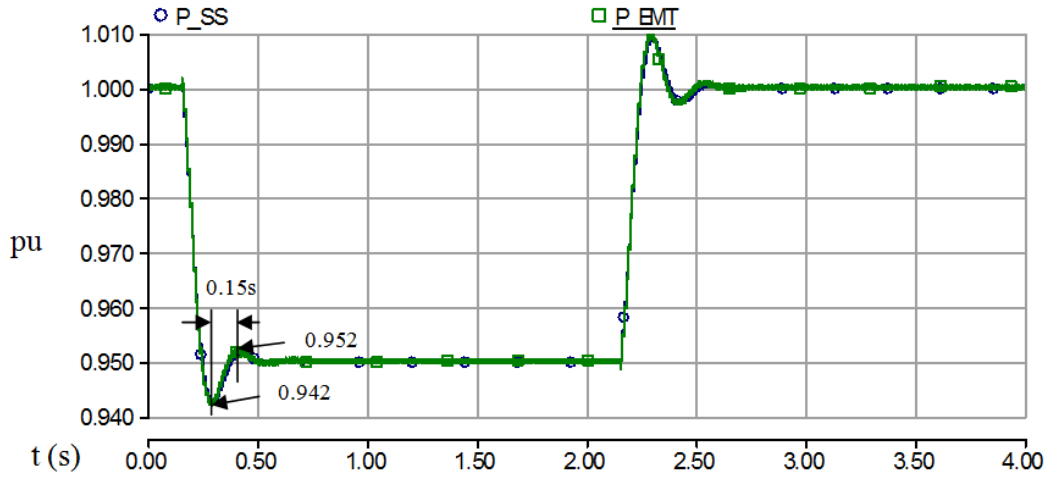


Figure 3.33: Power step change from 1.0 pu to 0.95 pu for SCR=1.6, PLL (100,500)

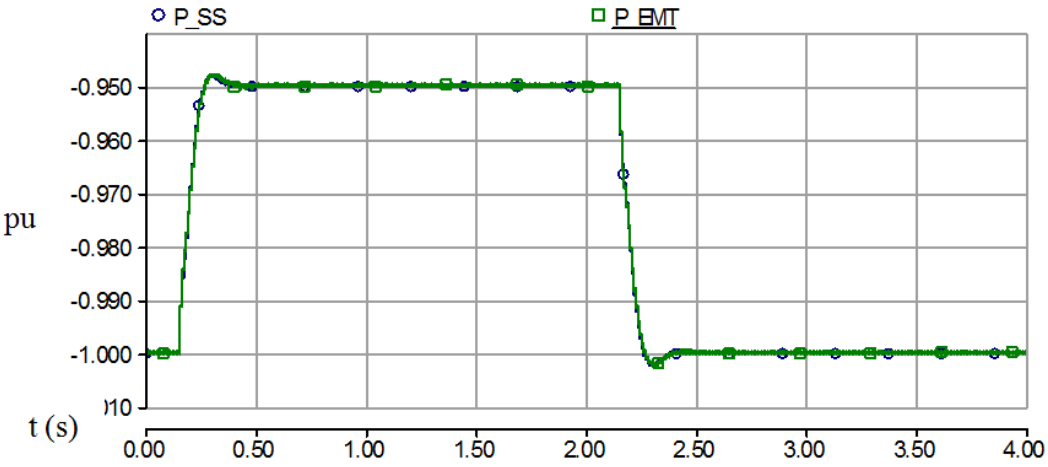


Figure 3.34: Power step change from -1.0 pu to -0.95 pu for SCR=1.6, PLL (100,500)

Similarly the small signal model response was validated using the EMT response for a voltage step change from 1.0 pu to 0.95 pu when the power order is 1.0 pu. The results are shown in Figure 3.35 and Figure 3.36 for lower and the higher PLL gain of K_p = 10 and K_p = 100. The transient responses of the model show the developed state-space model of the VSC system is in agreement with the EMT model.

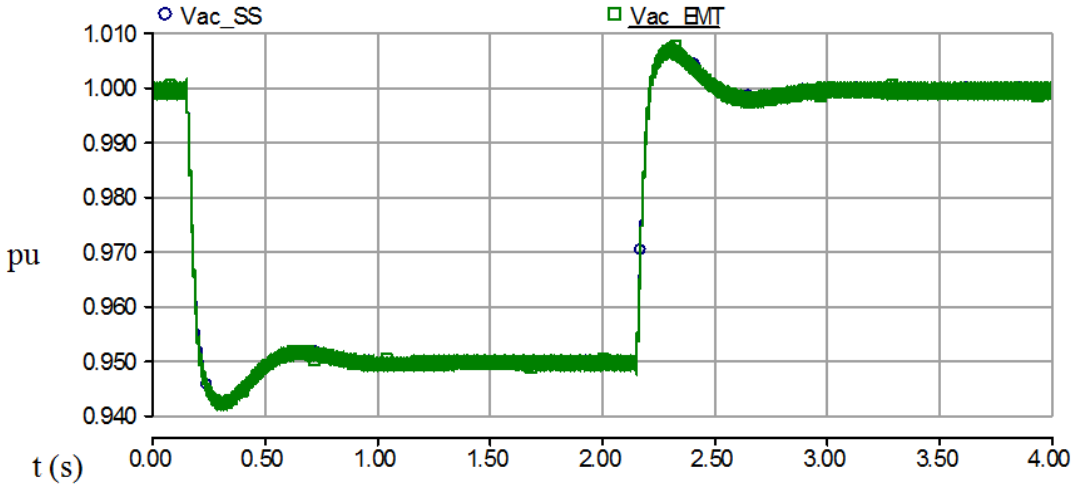


Figure 3.35: Voltage step change from 1.0 pu to 0.95 pu for SCR=1.6, PLL (10,50)

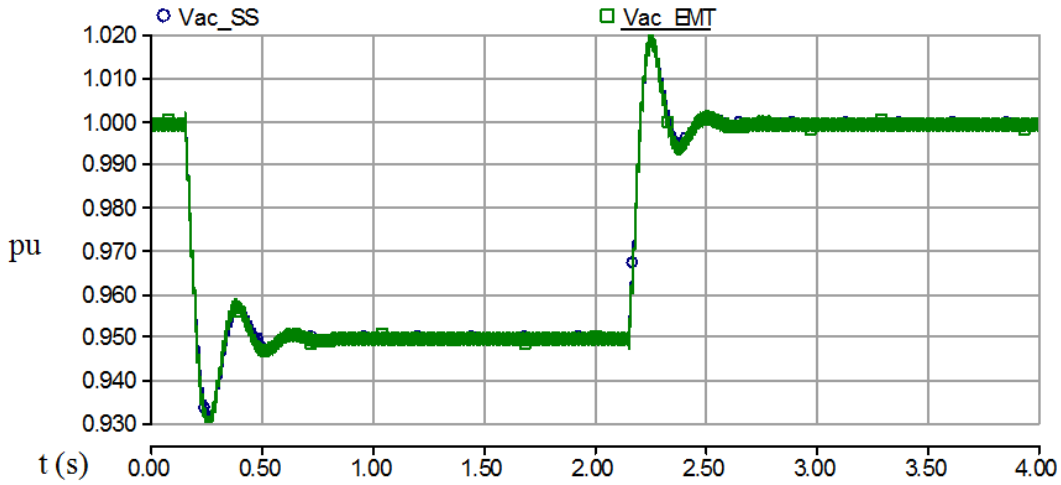


Figure 3.36: Voltage step change from 1.0 pu to 0.95 pu for SCR=1.6, PLL (100,500)

3.7.2.2 Eigenvalue analysis of the VSC model

The eigenvalues of the P =1.0 pu operating point are shown in Table 3.13 for both lower (K_p = 10) and higher (K_p = 100) PLL gain sets under ac system SCR = 1.6 and 4.0. The results indicate that the system is stable for the lower and higher PLL gains for both these SCRs. The calculated eigenvalues are consistent with the EMT simulations of the previous section. The eigenvalues in the table show, the dominant eigenevalue for the

lower gain set is $(-3.817 \pm j6.49)$. The simulated plot in Figure 3.31 shows a half period of oscillation of 0.48 s. This is in complete agreement with the half period derived from the natural frequency of the dominant mode of $(-3.817 \pm j6.49)$, for which the half period is also $0.5(2\pi/(6.49)) = 0.48s$. Likewise the decay rate of the amplitude in a half cycle is also consistent with the real part of the dominant eigenvalue.

Table 3.13: Eigenvalues of the test system for P = 1.0 pu

SCR=1.6		SCR=4.0	
PLL (Kp_{PLL}, Ki_{PLL}) (10,50)	PLL (Kp_{PLL}, Ki_{PLL}) (100,500)	PLL (Kp_{PLL}, Ki_{PLL}) (10,50)	PLL (Kp_{PLL}, Ki_{PLL}) (100,500)
$-184.006+3.811i\times 10^3$	$-185.909+3.817i\times 10^3$	$-150.274+4.038i\times 10^3$	$-154.585+4.045i\times 10^3$
$-184.006-3.811i\times 10^3$	$-185.909-3.817i\times 10^3$	$-150.274-4.038i\times 10^3$	$-154.585-4.045i\times 10^3$
$-141.311+3.16i\times 10^3$	$-158.606+3.175i\times 10^3$	$-116.427+3.367i\times 10^3$	$-130.011+3.381i\times 10^3$
$-141.311-3.16i\times 10^3$	$-158.606-3.175i\times 10^3$	$-116.427-3.367i\times 10^3$	$-130.011-3.381i\times 10^3$
$-242.678+1.01i\times 10^3$	$-232.062+1.019i\times 10^3$	$-283.813+1.392i\times 10^3$	$-278.211+1.396i\times 10^3$
$-242.678-1.01i\times 10^3$	$-232.062-1.019i\times 10^3$	$-283.813-1.392i\times 10^3$	$-278.211-1.396i\times 10^3$
$-270.975+452.829i$	$-267.107+480.304i$	$-281.369+883.164i$	$-269.188+893.937i$
$-270.975-452.829i$	$-267.107-480.304i$	$-281.369-883.164i$	$-269.188-893.937i$
$-56.46+47.701i$	$-80.579+45.637i$	$-61.753+21.296i$	$-78.762+22.572i$
$-56.46-47.701i$	$-80.579-45.637i$	$-61.753-21.296i$	$-78.762-22.572i$
$-35.627+23.768i$	$-10.149+21.516i$	$-36.965+13.694i$	$-41.909+18.817i$
$-35.627-23.768i$	$-10.149-21.516i$	$-36.965-13.694i$	$-41.909-18.817i$
-25.976	$-36.508+23.484i$	-20.883	-34.756
-12.606	$-36.508-23.484i$	-16.361	$-17.295+7.289i$
$-3.817+6.49i$	-34.708	$-4.043+5.075i$	$-17.295-7.289i$
$-3.817-6.49i$	-5.263	$-4.043-5.075i$	-5.334

The eigenvalue root locus of the P =1.0 pu operating point for the PLL gains K_p changing from 0 to 200 are plotted. The expanded root locus, showing poles closest to the imaginary axis, is shown in Figure 3.37, Figure 3.38, and Figure 3.39 for SCR=4.0,

SCR=1.6 and SCR = 1.3 respectively. For SCRs of 4.0 and 1.6, the system is stable for all K_p values. Indeed, by looking at the root locus, the poles for both these ac network strengths move more into the left half plane (LHP) as the gain increases. However, when the SCR is reduced to 1.3, the system becomes unstable for $K_p > 60$. This is opposite to the situation for higher SCRs, where the system poles move away from imaginary axis as K_p increases. A more detailed analysis shows that the SCR value below which unstable poles are possible is 1.32.

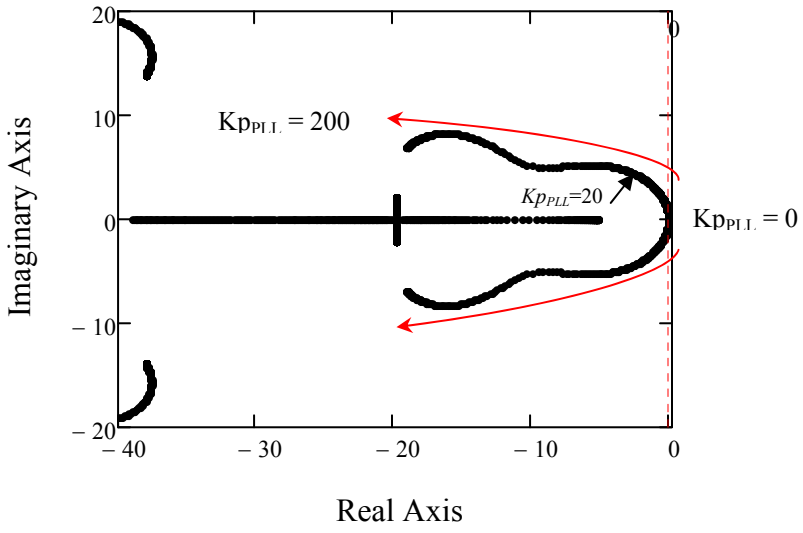


Figure 3.37: The root locus of the eigenvalue of the system SCR = 4.0, P=1.0 pu

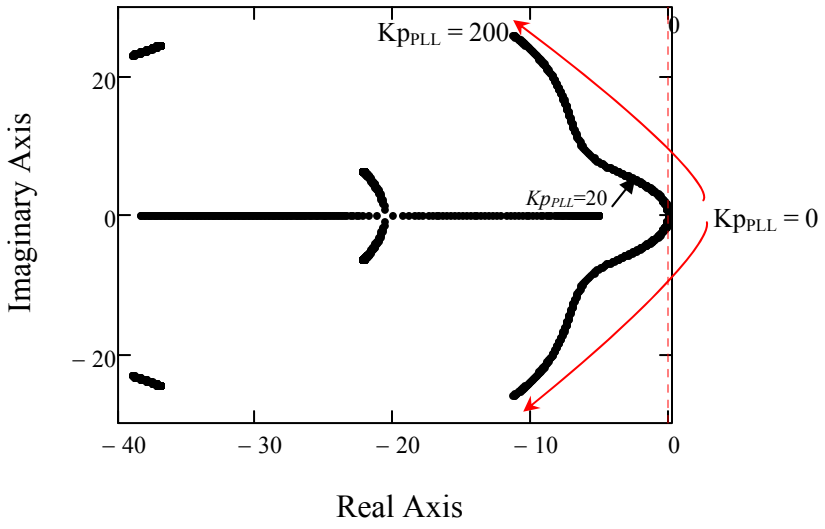


Figure 3.38: The root locus of the eigenvalue of the system SCR = 1.6, P=1.0 pu

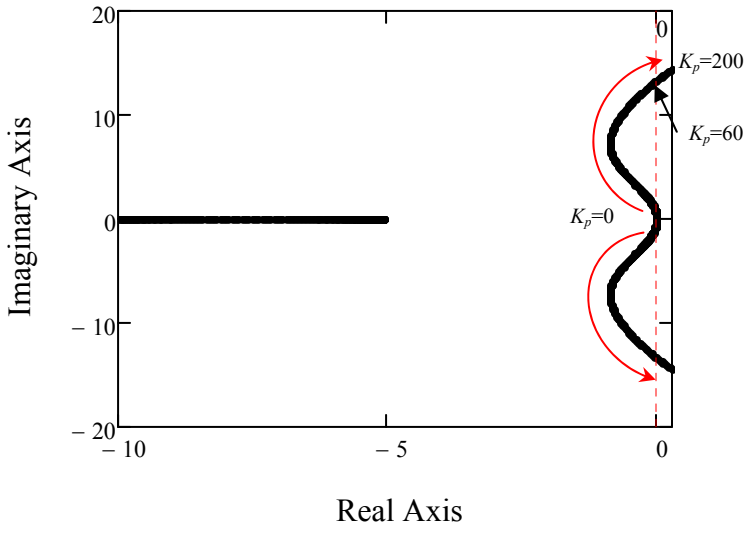


Figure 3.39: The root locus of the eigenvalue of the system SCR = 1.3, P=1.0 pu

Similarly the eigenvalues at the P= - 1.0 pu (inverter) operating point are shown in Table 3.14 and the root locus of system SCR=4.0, 1.6 and 1.3 are shown in Figure 3.40, Figure 3.41 and Figure 3.42 respectively. The results show the system is stable for both PLL gain sets and has improved stability at the higher gains.

Table 3.14: Eigenvalues of the test system for P = -1.0 pu

SCR=1.6		SCR=4.0	
PLL (Kp_{PLL}, Ki_{PLL}) (10,50)	PLL (Kp_{PLL}, Ki_{PLL}) (100,500)	PLL (Kp_{PLL}, Ki_{PLL}) (10,50)	PLL (Kp_{PLL}, Ki_{PLL}) (100,500)
$-170.591+3.81i\times 10^3$	$-177.847+3.805i\times 10^3$	$-138.429+4.037i\times 10^3$	$-147.288+4.031i\times 10^3$
$-170.591-3.81i\times 10^3$	$-177.847-3.805i\times 10^3$	$-138.429-4.037i\times 10^3$	$-147.288-4.031i\times 10^3$
$-134.491+3.153i\times 10^3$	$-151.571+3.142i\times 10^3$	$-108.676+3.361i\times 10^3$	$-121.598+3.348i\times 10^3$
$-134.491-3.153i\times 10^3$	$-151.571-3.142i\times 10^3$	$-108.676-3.361i\times 10^3$	$-121.598-3.348i\times 10^3$
$-253.556+1.013i\times 10^3$	$-243.26+1.003i\times 10^3$	$-295.366+1.396i\times 10^3$	$-289.631+1.391i\times 10^3$
$-253.556-1.013i\times 10^3$	$-243.26-1.003i\times 10^3$	$-295.366-1.396i\times 10^3$	$-289.631-1.391i\times 10^3$
−272.825+ 458.268i	−262.063+ 382.358i	−287.574+ 885.985i	−267.677+ 857.901i
−272.825− 458.268i	−262.063− 382.358i	−287.574− 885.985i	−267.677− 857.901i
−64.973+ 54.486i	−81.112+ 92.114i	−62.994+ 24.124i	−83.163+ 33.408i
−64.973− 54.486i	−81.112− 92.114i	−62.994− 24.124i	−83.163− 33.408i
−27.26+ 22.454i	−18.263+ 21.544i	−32.901+ 12.8i	−41.678+ 15.951i
−27.26− 22.454i	−18.263− 21.544i	−32.901− 12.8i	−41.678− 15.951i
−34.813	−37.077+ 17.78i	−34.086	−35.133
−17.792	−37.077− 17.78i	−12.516	−18.744+ 5.186i
−4.166+ 5.574i	−34.124	−4.026+ 5.155i	−18.744− 5.186i
−4.166− 5.574i	−5.304	−4.026− 5.155i	−5.326

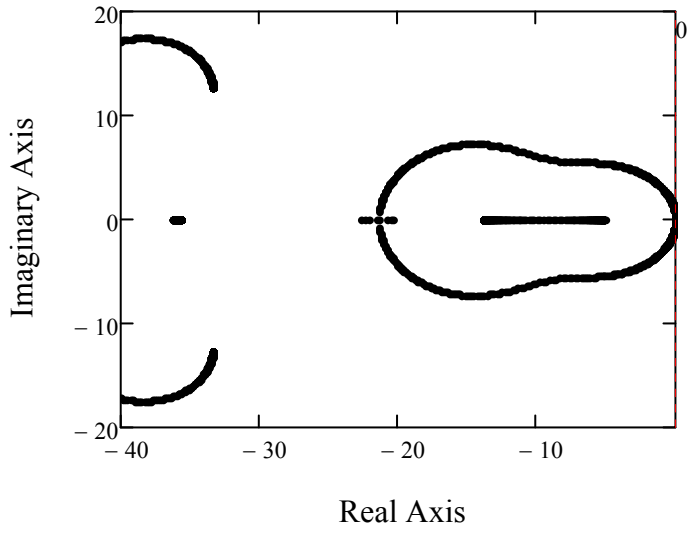


Figure 3.40: The root locus of the eigenvalue of the system SCR = 4.0, P= -1.0 pu

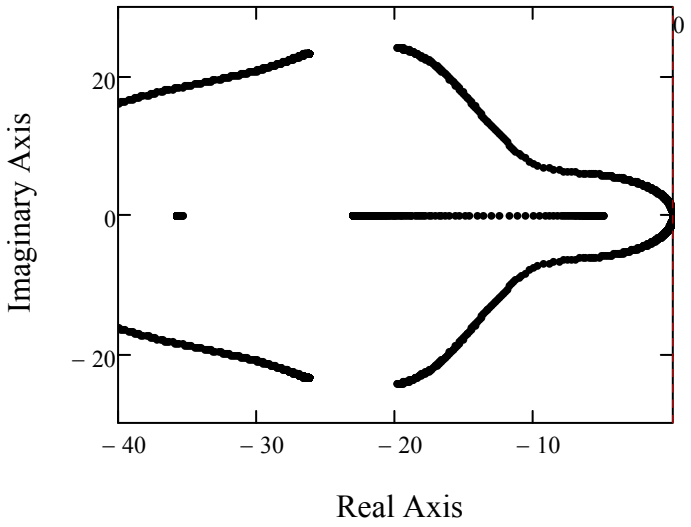


Figure 3.41: The root locus of the eigenvalue of the system SCR = 1.6, P= -1.0 pu

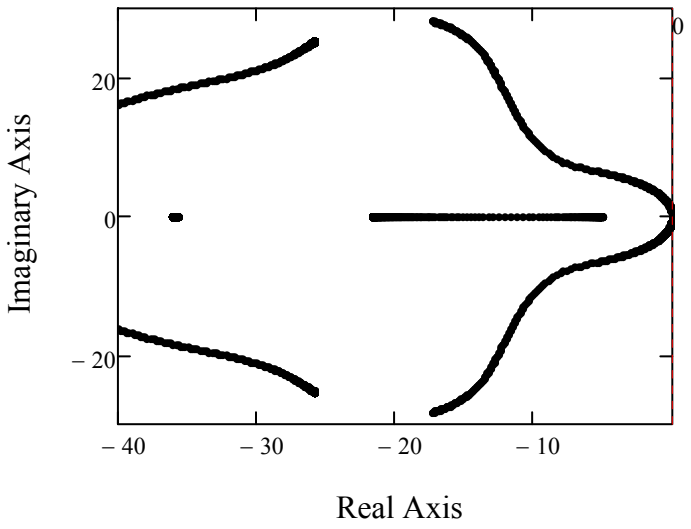
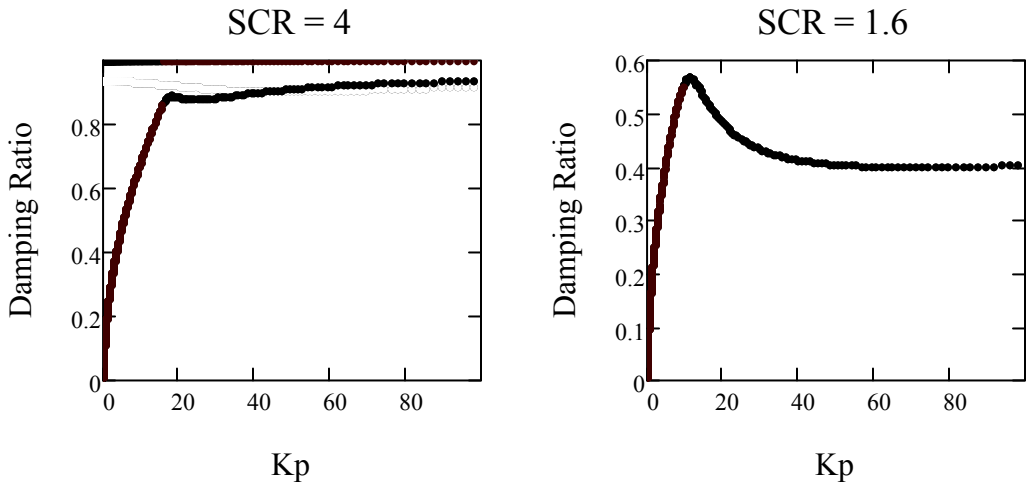


Figure 3.42: The root locus of the eigenvalue of the system SCR = 1.3, P= -1.0 pu

3.7.2.3 Damping Ratio Analysis of the VSC Model

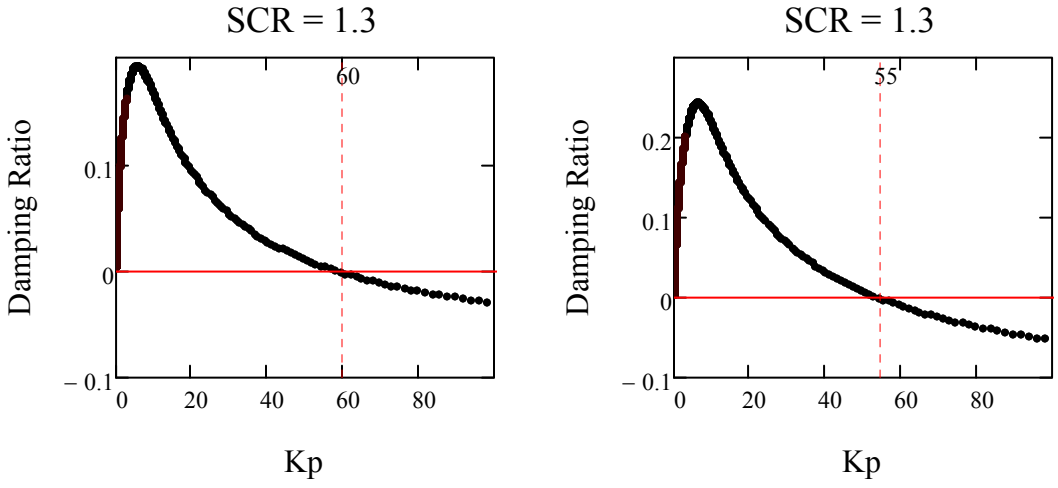
The damping ratio of an underdamped oscillation mode is defined as $\zeta = -\sigma / \sqrt{\sigma^2 + \omega^2}$ (where $\lambda = \sigma \pm j\omega$ is the eigenvalue of the mode). Damping ratios of 10% or more are considered suitable for power systems, as then the response is not too oscillatory [72]. If the damping ratio ζ is considered, the results shown in Figure 3.43 (a) and (b) indicate

that K_p should be large than around 20 for the stronger systems (SCR =4 or 1.6) as then the damping ratio is uniformly high. When the ac system becomes even weaker, e.g., SCR = 1.3, as shown in Figure 3.44 (c), the damping ratio becomes negative when PLL gain $K_P > 60$, indicating instability. This is also seen in the root locus plot of Figure 3.39.



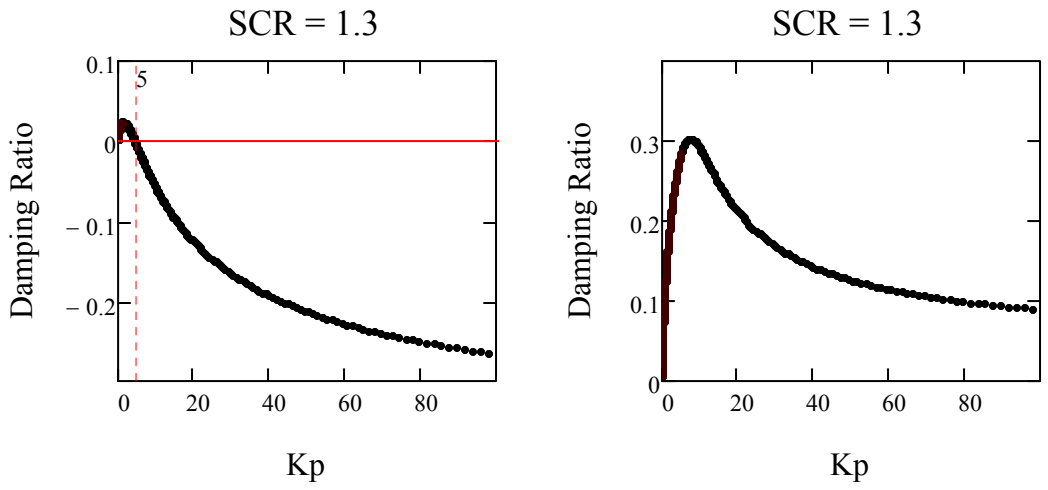
(a) C_f=15%, ϕ=80˚ (b) C_f=15%, ϕ=80˚

Figure 3.43: PLL gain verse damping ratio for stronger system



(c) C_f=15%, ϕ=80˚ (d) C_f=30%, ϕ=80˚

Figure 3.44: PLL gain verse damping ratio for weaker system



(e) C_f=15%, ϕ=78˚ (f) C_f=15%, ϕ=82˚

Figure 3.45: PLL gain verse damping ratio for different system impedance angles

In VSC-HVdc installations, additional reactive power support is often provided, in order to reduce the reactive power loading on the VSC valves. This can be in the form of a reactive shunt capacitor. For a larger shunt capacitor, e.g. one that provides 30% compensation (with rated dc power as base), Figure 3.44 (d) indicates that K_p must be below 55. However, Figure 3.44 (a) and (b) show that for the weaker system, the dominant poles of the system are much more poorly damped compared with the stronger systems of Figure 3.43 (a) and (b). Hence, it is expected that operation at very low short circuit ratios in the range 1.4 or below, will prove to be difficult. Another observation is that when the ac system impedance angle is smaller, e.g., *78˚* instead of *80˚* as in Figure 3.45 (a), the damping is poorer and instability is reached much sooner at K_p =5. For a larger impedance angle, i.e. *82˚*, Figure 3.45 (b) shows damping is much improved and there is no instability.

3.7.3 Maximum Power Transfer Capability and PLL gain Limitation on SCR Requirement

Power-voltage instability in dc converters limits the maximum power transfer capability (P_{max}) of the converter for both LCC and VSC type converters. Such analysis in Section 3.4 shows the P_{max} increases with the growing of SCR. However, such analysis does not take into account any control system parameters, and essentially is an absolute limit that can never be exceeded.

Using the small signal model developed above, the impact of PLL gains on the maximum power transfer is discussed in this section. An interesting result from such a study would determine how close one can come to theoretical limit P_{max} when such control system parameters are considered.

For a VSC rectifier it can be shown when the SCR has a resistive component (i.e., the Thévenin equivalent of the ac system has a resistive component, giving an impedance angle smaller than 90°), the P_{max} is reduced, whereas the inverter has the opposite trend. The relationship between P_{max} and SCR can be given as equation 3-48. Thus the more onerous case of a VSC rectifier connected to an ac system with impedance angle of 80° is considered in this section.

$$P_{\max}(pu) \approx SCR \cdot (1 \pm \frac{R_s}{|Z_s|}) \qquad 3\text{-}48$$

where $Z_s = R_s + j\omega L_s$ is the ac systems Thévenin impedance at fundamental frequency. The '+' sign is used for inverter operation and the '-' sign for rectifier operation.

Curves in Figure 3.46 show the relationship between the power transfer and the largest

real part $\sigma_{\max}$ of the eigenvalues, i.e, $\sigma_{\max} = \max(\mathrm{Re}(\lambda_i))$, $i \in \{1, 2...16\}$; for different SCRs (all with the impedance angle of 80°), when a PLL gain of K_p =100 is used. The curves indicate that for each SCR, there is a critical value of power P_{max*}, beyond which $\sigma_{\max}$ goes positive indicating the onset of instability. This value is the maximum achievable power P_{max*} considering the system eigenvalues.

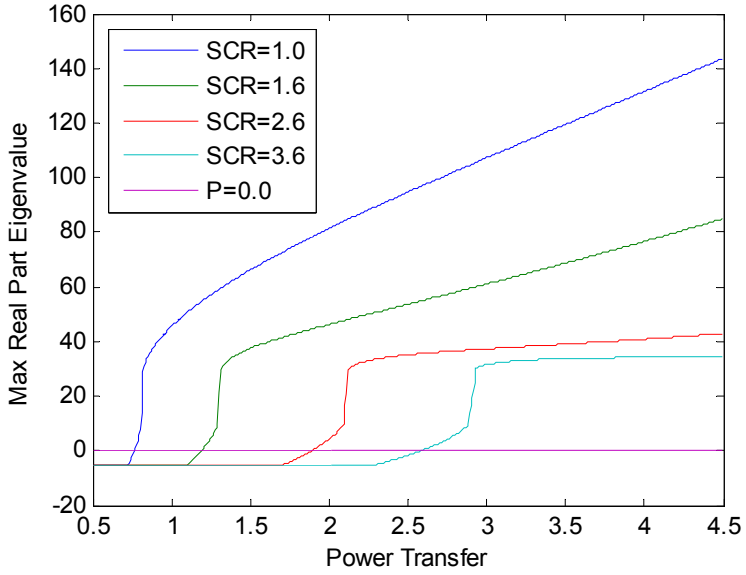


Figure 3.46: The real part of eigenvalue of the system $\sigma_{\max}$ vs. power transfer

Figure 3.47 shows the relationship between the SCR and P_{max*} for different PLL gains of K_p =1 and K_p = 100 respectively. The theoretical maximum power transfer P_{max} as derived in Section 3.4.1 and given by equation 3-48 is also shown in the figure. The results shows $P_{max*} < P_{max}$, as is to be expected. The enlarged curves at lower SCR clearly show that the theoretical limit is more closely approached as the PLL gain goes to very small values. The figure shows the larger gain (K_p =100), rated power can be transmitted only when the SCR is greater than 1.31; whereas, for the lower gain (K_p =1), the system can be weaker, with an SCR of 1.245 more closely approaching the theoretical

minimum SCR of 1.21 for the 80° ac system.

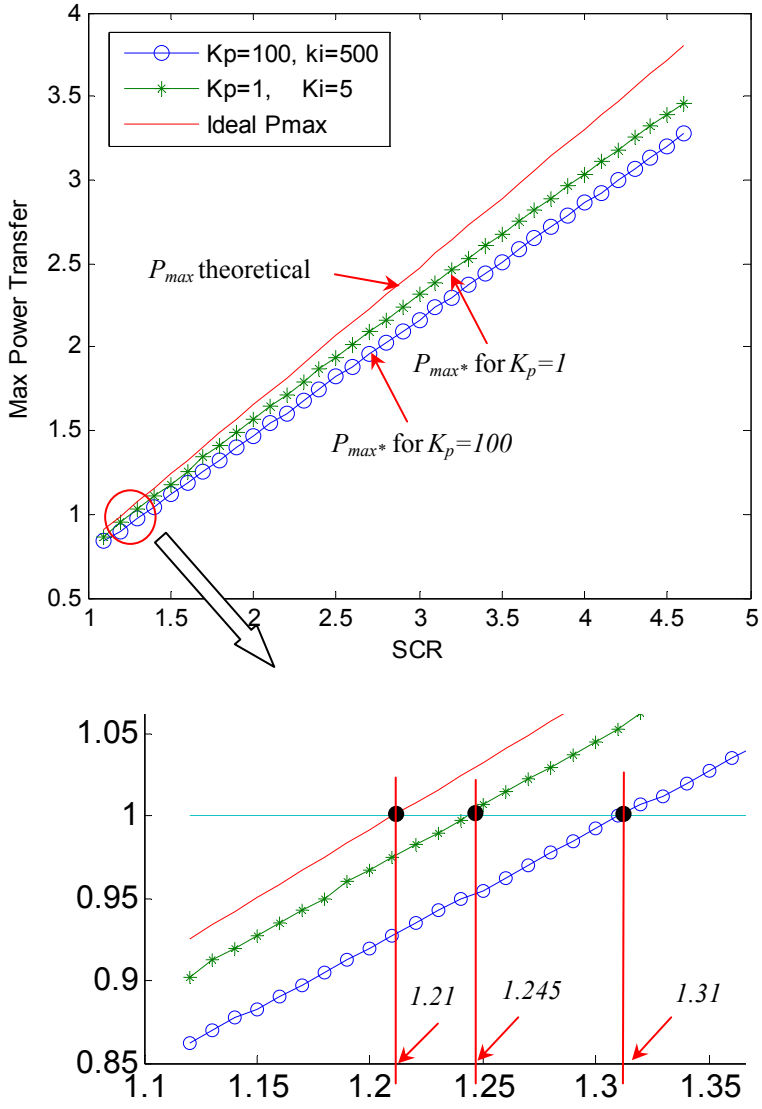


Figure 3.47: The maximum power transfer capability

Another useful way to quantify this phenomenon is to plot the allowed range of K_p versus the SCR with the aim of transmitting rated power as shown in Figure 3.48. The figure shows for a system SCR greater than 1.32, the high K_p no longer imposes a limitation on the stability. It must be noted however, that using too small a PLL gain gives poor damping, particularly at higher SCRs (see Figure 3.43), and will result in poor dynamic

performance. Hence it is unlikely that operation at such low gains will be attempted.

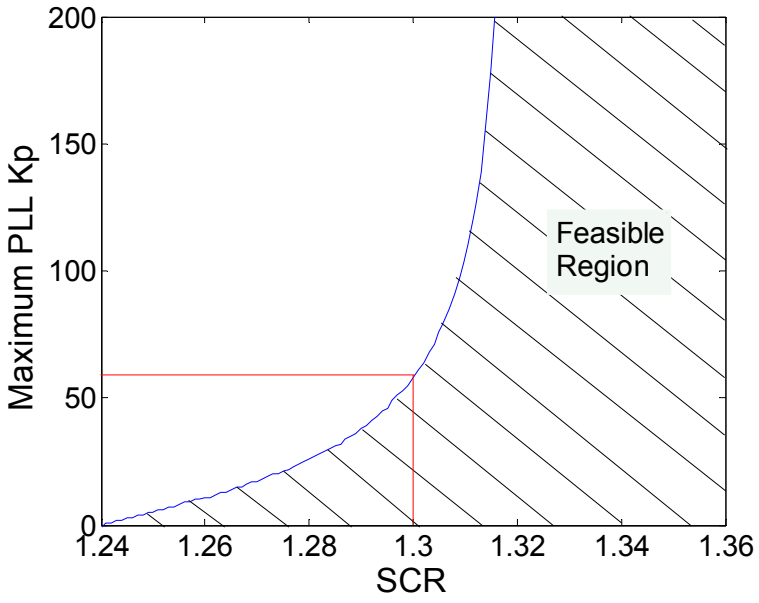


Figure 3.48: The SCRs vs. maximum PLL gain K_p

3.7.4 PLL Gain Effects: Large Signal Disturbances versus Small Signal Disturbances

As shown in Figure 3.31, to

Figure 3.36, the linearized model is entirely accurate for small changes around any one operating point. It also shows that operation at low SCRs requires reduced PLL gains. The same general conclusion is observed for the large step changes in Section 3.6 (see Figure 3.25), but the precise numerical values for threshold limits, etc. do not agree with the small signal analysis. For example, for power reversal, the system goes unstable for SCR = 1.6 at large gains (see Figure 3.24), whereas the small signal analysis says that the system should always be stable for SCR > 1.32 (rectifier). However, results in Section 3.6 were for large step changes in power reference. For such changes, the system

transition through a range of operating points, and so linearized analysis is not directly applicable.

The above discussion shows that relying on linearized analysis alone is dangerous, as it might suggest working at the high gains. Hence, electromagnetic transient simulation must be used to determine whether the gains calculated with small signal analysis are compatible with the large signal behaviour before selecting the final gains.

3.8 What Constitutes a Low SCR for VSC Systems?

In LCC systems, an ESCR of 2.5 is considered as a threshold between weak and strong systems. ESCRs greater than 2.5 make the converter susceptible to voltage changes from remote faults, load rejection overvoltages, poor damping and increased risk of commutation failure. Therefore when ac system has an ESCR < 2.5, we say that the system is "weak". ESCR ≥ 2.5 corresponds to a "strong" ac system.

The question can be asked, whether a similar threshold can be defined for the VSC. The analysis in this chapter makes a contribution to arriving at such a threshold. The analysis in this chapter shows that the rectifier operation is the most severe operation for VSC transmission; hence the values shown below are for rectifier operation. However, they will still be applicable to inverter operation if power reversal is considered.

The answer to the question can be answered in several stages. Assuming a typical impedance angle of 80°, the following thresholds apply:

1. SCR = 1.21 is an absolute theoretical limit below which operation at rated power is not possible. However, with controls present, the limit cannot be attained.

2. SCR =1.32 is the limit below which at least some of the poles can go into the right hand complex plane (RHP). Although stability is possible, the PLL gains are so low that the dynamic response may be poor.
3. As in item 2 above, when the SCR < 1.4, operation is not recommended, as the PLL gains have to be small.
4. If large transient, i.e., power reversal is required, the small signal analysis gives optimistic answers to retain system stability; a minimum SCR of about 1.6 is required.

So in conclusion, one can say that for a VSC HVdc system, SCR = 1.6 could be considered as the threshold between a weak and a strong system. However, the manifestation of effects is different from that in the LCC. For example, there is no load rejection overvoltage or commutation failure.

It should also be noted that comparing LCC and VSC options, an SCR of 1.6 for the VSC would result in SCR of 1.1 for the LCC, assuming filters providing 50% compensation. Hence one can say that the VSC can be used in situations where the ESCR for an LCC would be 1.1.

3.9 Conclusions

This chapter investigated power transmission limitations imposed by ac system strength and ac system impedance characteristics on a VSC-HVdc converter. An important observation is that the operation of the converter is affected by the angle of the ac system's impedance at the fundamental frequency. As the SCR becomes more resistive,

the minimum ac short circuit ratio (SCR) required at the rectifier side increases from that required for ideally inductive ac impedance, but it decreases at the inverter side. Also, the finite MVA limit of the VSC imposes a further limitation on power transfer, requiring an increase in the value of the minimum SCR. This limitation can be relieved if additional reactive power support is provided at the point-common-connection (PCC).

Another important observation is that the gains of the phase locked loop (PLL) used for angle reference generation must be reduced for lower SCR operating conditions (weak ac systems). Several tests were conducted for step changes in power order at different operating points and for different power order step magnitudes. It was observed that the gains of the VSC inner and outer PI controllers have a relatively limited effect on system transient performance compared to the gains of the PLL.

A state-space VSC model was developed and validated using detailed electromagnetic transients simulation. The small signal model can be used to analysis the system stability under both system and control parameters changes. However, the large signal transient cannot be analysed by the linearized model. Electromagnetic transient simulation must be used for selecting the final controller gains.

Results presented in this chapter show that the PLL works well in stronger ac systems, with short circuit ratios of 1.6 or larger as long as the proportional gain is kept sufficiently large to provide an adequate damping coefficient. However, result shows that gains of the PLL, particularly at low SCRs greatly affect the operation of the VSC-HVdc converter and that operation at low SCRs below about 1.4 is very difficult. Also, the damping ratio is much poorer (lower) than that for the higher SCRs. This indicates that

operation at such low SCR values, is not recommended. It is also seen that the provision of local capacitive reactive power via a shunt capacitor and the decreased ac system impedance angle will further lower the stability limit.

The chapter also showed that the maximum power transfer limit predicted by a power-voltage stability calculation is a theoretical upper limit that can never be attained in practice. Eigenvalue calculations show that it can only be approached closely when the PLL gains attain very small values.

Chapter 4:Relaxation Optimization Methods to Optimal Gains for DC Grid Converters

4.1 Introduction

Multi-terminal VSC-HVdc schemes (also called dc grids) are complex arrangements of ac and dc transmission networks interfaced through semiconductor switches. Accurate simulation of the relevant phenomena for the design of their controllers requires a detailed representation of the system that usually uses electromagnetic transient simulation programs (referred to as emtp-type programs). Designing controllers using analytical approaches, such as the root locus approach is difficult due to the complexity and nonlinearity of power systems. Traditionally, simulation-based design consists of a human being conducting several runs to reach the desired set of design parameters. However, the search process can become lengthy and some regions of the space may not contain the optimum. Recently, the use of optimization-enabled electromagnetic transient simulation (OE-EMTS) to design the control parameters of complex systems was introduced [64]. This method can automate the search process in a highly-efficient manner. It uses a mathematical approach that utilizes a nonlinear optimization algorithm to select the most likely parameters.

However, the increasing number of terminals in dc grids imposes a big challenge to controller design. The increasing number of control objectives and control variables is making the current optimization algorithms difficult to handle. In this chapter, OE-EMTS

will be briefly discussed, and then the focus will be on the proposed "relaxation optimization method" for the design of control gains for multi-terminal VSC-HVdc converters.

4.2 Optimization Enabled Electromagnetic Transients Simulation (OE_EMTS)

Using an emtp-type program in the controller design process requires conducting a number of runs, each with a different set of controller parameters, to determine the optimal values of the design parameters. Many of these programs contain a “multiple-run” feature which permits the user to conduct a series of runs with the parameter values varied in a random or sequential manner. The user then examines the results of these runs and selects the parameter values that provide the optimum results. However, this method deploys no intelligence in the way it spans the search space, and the search process can be very wasteful of computational time.

Optimization-enabled electromagnetic transient simulation (OE-EMTS) has been recently introduced for the design of control parameters for complex systems [64]. In OE-EMTS, a sequence of simulation runs is conducted with the trial parameter settings in each run selected by a nonlinear optimization algorithm [35]. During each run, an objective function (OF) is evaluated, which has the property that, the smaller it is, the closer to the achievement of the objectives it is. This strategic selection of parameters usually results in an orders of magnitude reduction in the number of emtp simulations required compared to the sequential and random searches of the multi-run approach. Figure 4-1 shows how the simulation program and the optimization algorithm are interfaced.

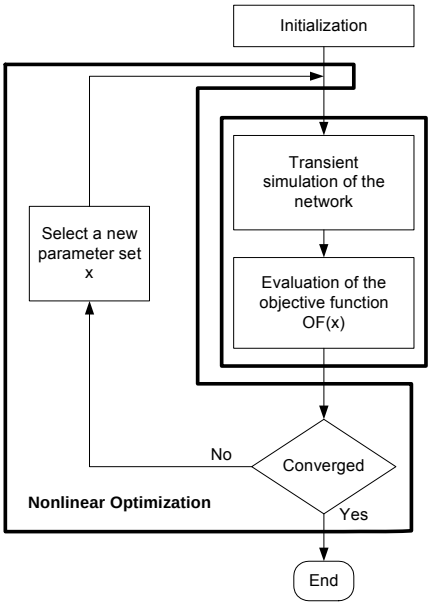


Figure 4-1: Schematic diagram of optimization-enabled transient simulation [35]

The optimized settings that may be optimal for a given operating configuration may be inadequate for a different configuration. The inclusion of robustness into the design using optimization-enabled transient simulation has been introduced [62] [65]; it enhances the design of optimal systems by searching for a parameter set that has the best overall performance over a range of operating points. The inclusion of robustness can also be implemented into each sub-parameter set search in Figure 4-1, as shown in Figure 4-2, where the weight distribution factor w_j indicates the importance of the operating point. As a consequence, care must be taken to assign higher relative weights to the most vital system conditions so as to not over-constrain the objective function. Selecting the final weights does require some trial and error [62].

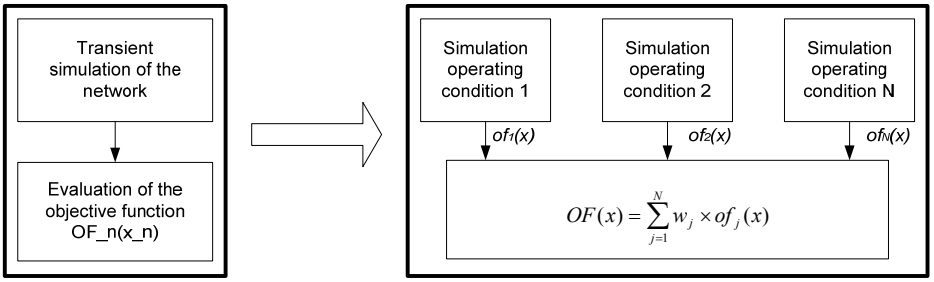


Figure 4-2: Inclusion of robustness in optimization-enabled transient simulation [65]

However, as the number of VSC converters in the VSC-HVdc grid increases, the number of operational conditions increases exponentially. For example, if the design is carried out using x different control variables and y different SCRs, xy different configurations result for the single converter. If there are n converters, the total number of cases to be considered can be as high as $(xy)^n$. In the case studies presented later, we have used $x = 4$ and $y = 4$, and we have used $n = 6$ converters in the grid. This gives a total number of cases equal to about *17* million. In addition, the entire system is n times as large, and hence takes much longer to simulate for each run. Hence optimization based on the whole dc grid and on all operational conditions becomes impractical. In order to have good overall performance over a range of operating points for multi-terminal VSC-HVdc converters, a new robust optimization procedure that optimizes one converter at a time and uses a manageable amount of computation time will be introduced later in this thesis.

4.3 Optimization Algorithm and Simulation Program

An optimization problem can be defined as finding the minimum (or maximum) of a mathematical function, commonly referred to as an objective function (OF), within a specified parameter space [66]. Although analytical solutions can be found for simple objective functions, it is very difficult to find solutions for nonlinear multivariable

functions. Optimization algorithms are usually used to find the optimal points of the objective functions by using the iterative search process.

From the viewpoint of mathematics, OE-EMTS solves a nonlinear optimization problem. The OE-EMTS can be written as a general optimization problem as:

$$\begin{aligned} &\min f(x) \\ &s.t. \quad g(x) = 0 \end{aligned} \tag{4-1}$$

The system performance is quantified by an objective function (OF) that quantifies the deviation of the system behavior (discerned from the system waveforms) from the desired behavior. Usually, the OF is selected as a positive function with zero indicating perfect conformance to the desired behavior. In traditional algebraic optimization, the OF is available as an equation in terms of the variables to be optimized. In a complex system no closed form equation of OF is available, so analytical determination of optimization is not possible. Using OE-EMTS the system is simulated and the OF is made from a function of the simulation waveform. In non-linear optimization techniques, several simulations are conducted, and in each the input parameters are perturbed and the impacts on the OF are computed. This gives an idea regarding what trial parameters should be attempted for the next run in the sequence. Eventually, the method converges to the optimal point.

Several different non-linear optimization methods are possible. These methods can be classified into three categories named direct search methods, gradient-based methods, and heuristic methods. The direct methods, such as Nelder-Mead, Hooke-Jeeves, and Powell's conjugate directions use the values of objective function (obtained at a limited number of sample points) in their search. The main advantage of direct search methods is their simplicity, in that they do not require explicit calculations of derivatives as required

in gradient based method. The heuristic method, such as genetic algorithm (GA), particle swarm optimization (PSO), simulated annealing (SA), and ant colony are based on evolutionary computing [67]. They are guaranteed to find the global minimum (in infinite time) but take a very long time to do so [35]. They are more suitable for combinatorial optimization such as models including binary switch states ('on'/'off') instead of continuous numbers (such as PI gains) [68]. Others use gradient information and usually attain a local minimum. They are generally faster, and although a global minimum is not guaranteed, there is a chance of finding it by using different initial starting points. In any case, even if a local minimum is obtained, the parameters will always be better than that of the initial set of parameters.

In this thesis the OE-EMTS approach uses the simplex method of Nelder and Mead [61]. The simplex optimization method is a geometry-based, non-linear optimization algorithm. It is usually very suitable for cases in which the number of variables is 10-20 or less [35][65][62][63][69], which is the case in this thesis. This method is based on successive intuitive re-shaping of an object called a simplex. In N-dimensional space, a simplex is a geometric object comprising N + 1 vertex. In two- and three-dimensional spaces, the simplex would be a triangle and a tetrahedron, respectively. The basic idea in the simplex method is to compare the value of the objective function at the N+1 vertices of a simplex and seek the optimum point in a direction. The method discards the worst vertex (i.e., the highest value) for a minimization problem; a new vertex is chosen, and gradually the optimum point is approaching during the iterative process. The method is described in the literature [35] [61]. It is fast, but it only guarantees a local minimum and does not guarantee a global minimum.

The OE-EMTS has been successfully implemented on PSCAD/EMTDC and used in optimizing the control systems of STATCOM, HVdc, dc-dc converters, etc. [35] [58] [62] [64] [70] [71]. In the research discussed in this thesis, the PSCAD/EMTDC electromagnetic transient simulation program has been selected as the simulation core.

4.4 Use of Relaxation Optimization to Set Gains for DC Grid Converters

Multi-terminal VSC-HVdc control systems have multiple objectives. Tuning such control systems sometimes requires a significant amount of expertise and time. Some research use the open loop transfer function of each control to choose the gains for the controller [54] [69]. In order to do so, the Laplace transformed equivalent of the physical systems must be identified. System transfer function is derived from the linearized differential equation of the respective state variable. However this linearized approach is only valid in the small neighbourhood around the specified operating point, and it remains a question whether the parameters defined by open loop control functions will work for close loop situations. In order to select the optimal control parameters under different operating conditions and under system transients, the OE-EMTS is used in this thesis for the controller gain selection.

Initially the intention was to use the OE-EMTS in a multi-terminal VSC HVdc system to tune the control parameters; however, investigation revealed two major challenges:

1) There are multiple objective functions due to more than one VSC terminal needing to be optimized. The single objective optimization algorithm is no longer valid and

multi-objective optimization algorithms need to be considered. One way to handle the multi-objective problems is to use the concept of Pareto optimality [72] [74]. The Pareto frontier, which is a set of all the Pareto optimums, is drawn in the space of all the sub-objective functions, and it permits the understanding of tradeoffs between competing sub-objectives. However the Pareto frontier is a graphic visualization method and requires human observation of a two dimensional graph, each dimension referring to one of the sub-objectives. Hence it is best suited for two dimensions (i.e. two sub-objectives). Extension to 3-dimensions is possible, but requires special software for handing 3-D visualization. As the OFs in this thesis have at least 3 sub-objectives, the Pareto method was not used.

2) A single objective optimization function algorithm can still be used if the objective function is defined by a linear combination of the multi-objective functions. If the linear multipliers are positive, it can be proven that the solution of the new single optimization problem is right on the Pareto Frontier of the multi-objective optimization problem [74][75]. This method seems to be simple and easy to implement; however, the dimension of the optimization problem increases linearly as the number of VSC HVdc terminals increases.

Two basic approaches can be used to solve the multi-objective optimization problem and the high dimension problem: one is mathematics-inspired and the other is engineering-inspired. One can seek better mathematic algorithms to solve multi-objective optimization; or, one can study the particular engineering problem and perhaps solve it in a simplified way, but with sufficient accuracy.

Investigating the optimization algorithm itself is beyond the scope of this thesis. The purpose of this research was to tune the controller and establish a necessary good operating condition of the multi-terminal VSC HVdc system. It is not absolutely essential to run the system at the theoretical optimal point. It is sufficient for all operating points to be stable, and all dynamic responses to be well damped. Keeping this in mind, the engineering-inspired approach was utilized, and a relaxation-based optimization method was developed.

4.4.1 Control Parameters Selection and Design Procedure

Normally, the initial control gains are selected manually to ensure the system starts up to steady state. The number of simulations required to achieve the optimal solution varies depending on this selection. In this section, a new design procedure is proposed, in which the averaged valve bridge model is used for initial control parameter values selection [46]; and the selection and optimization of a control parameter set for each individual terminal is used and evaluated by the designed objective function of the system.

Multi-terminal VSC-HVdc technology has made the integration of large offshore wind farms to a grid over distances possible. However, the increasing number of VSC terminals imposes big challenge to designing of the control system. Because the number of terminals increases, as does the number of optimization variables, the resultant problem takes a great deal of computer time.

Optimal design of the controls involves selection of suitable gains (K_p) and time constants (T_i) for the respective proportional-integral (PI) controllers at each VSC terminal. The VSC control shown in Figure 2-11 involves four PI controllers, two inner

controllers and two outer controllers. Hence, the total number of control parameters that must be selected and optimized is eight for one VSC terminal. With several VSC terminals in a VSC-HVdc grid, the number of design control parameters increases significantly, a situation that optimization algorithms may find difficult to handle.

The idea of relaxation-based optimization proposed in this thesis is to optimize each converter in the grid one by one. Although the final result may not be optimal, this is a practical approach. It is known that modeling based on averaged representations is useful for the analysis of the slow dynamic of the system. In this research, initial control parameter selection using the averaged model to represent the valve bridge was used. Without high-frequency switching of the IGBTs in each converter, the computational time was reduced substantially. The selected initial control parameters were then evaluated and confirmed by representing the valve bridge with the detailed model.

To summarize, the procedure is as follows:

1. The multi-terminal system is modeled, with all converters described by the averaged model (This allows faster simulation).
2. By trial and error, the controller parameters for all converters are selected so that the system runs stably at the prescribed operating condition. (The large number of control parameters for the multi-terminal VSC-HVdc system makes the manual selection very difficult.)
3. Pre-specified disturbances and sub-objective functions (described in next section) are constructed. The objective function is the weighted sum of the sub-objective functions; it will be optimized to make system response as good as possible given

the disturbances. There is a separated sub-objective function for optimizing the gains of each converter.

4. The control of the runs is handed over to a non-linear optimization algorithm, and the optimization proceeds. Several consequence optimization sequences are run, as follows:
    - In the first run, the parameters of the dc voltage controlling converter are optimized. The sub-objective function of the dc voltage controlling converter is given more weight.
    - In the second run, the parameters of the power controlling converter are optimized. The sub-objective function of the power controlling converter is given more weight. At the end this optimization stage, two converter parameter-sets have been optimized.
    - The process is repeated for the third converter, and so on until all converters are optimized.
5. The final parameter sets are recorded and a confirmatory simulation (no optimization process) with the multi-terminal system consisting of fully detailed converter models is conducted to make sure that the parameter sets obtained using the averaged model work as expected.

This approach has a number of drawbacks:

- The number of simulations is very large, and even with an averaged model the process takes a great amount of time.

- Because all the parameters were not optimized simultaneously, the result is sub-optimal.
- Simulations may become unstable and no results may be found.
- The robust controller parameters selection for different operation conditions is impractical with the whole system representation.

Normally, the response of the inner current controller is very fast and the response of the outer controller is much slower than the response of the inner current controller is. At the time scale of interest to the outer controller, the currents may thus be assumed to be equal to their reference value. Therefore, in order to reduce the total number of control parameters to be selected and optimized, this research proposes to fix the inner current controller control parameters for each converter. In this way, the number of control parameters to be selected and optimized is reduced from eight to four for one VSC converter.

The control system is required to operate satisfactorily when the system is subjected to power order change and disturbances. The system's response to these events is quantified into a single objective function (OF). Even though the design is to consider all aspects of the design specification in selecting the OF, the initial design cycle, which minimizes this OF, may yield unanticipated system behaviors. Therefore, a second design cycle has to be initiated, one with a more-refined OF. This procedure may have to be repeated several times to achieve a satisfactory design [62].

The process is shown in Figure 4-3.

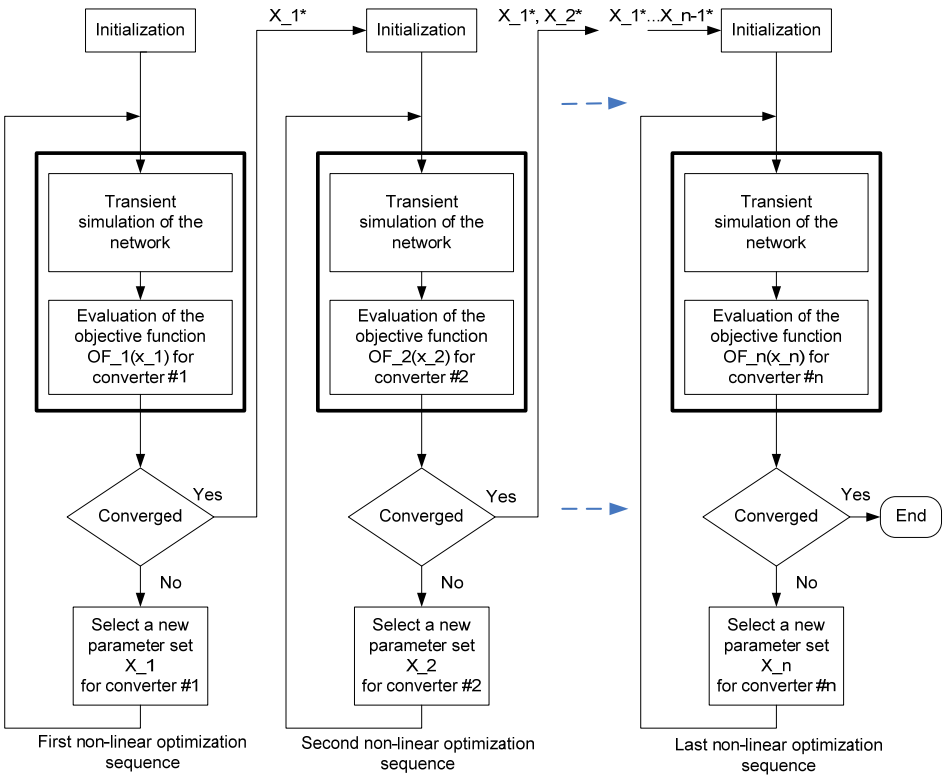


Figure 4-3: Schematic of an OE-EMTS interface for multiple devices

4.4.2 Development of the Objective Function

A single objective function can be generated based on the integral square error (ISE) measure frequently used in control systems, as shown in equation 4-2. The factor K_i can be used to give selective importance to the different objectives depending on which objective is most important to the control parameters design. The purpose of this objective function is to select and optimize the proportional and integral gains K_p and T_i of the two PI controllers in the outer controller of the j^{th} VSC converter. The number n denotes the number of partial objective functions for each of the operating conditions. In a multi-terminal VSC-HVdc system this number can be the number of terminals. Equation 4-3 shows the partial objective function of the VSC terminal with dc voltage and ac voltage control. Equation 4-4 shows the partial objective function of the VSC

terminal with power and ac voltage control. The first partial objective function penalizes any deviation of dc power or dc voltage from its reference. The second penalizes the ac voltage magnitude error; and the third the sum of the square of the ac harmonics, i.e., the square of the total harmonic distortion (THD). The last sub-objective function, ought not to be required, as the PWM algorithm should determine the THD. However, if the controllers act too fast, i_d and i_q are not quasi-constant, and can introduce ac voltage distortions. Adding the last term prevents this from happening. $T_{deblock}$ and T_{ss} represent the time when the converter de-blocked and the time when the system reached steady state. In order to penalize any deviation between the actual and the reference for the power order changes or the dc voltage, the weighting factor *w(t)* is added to reflect the importance of the change.

This multi-objective optimization problem often converges to a solution that is a compromise between the objectives. Therefore, selecting parameters in the simulation that minimize ISE provides the best fit of the desired objectives.

$$of_j(K_{p\_j1}, T_{i\_j1}, K_{p\_j2}, T_{i\_j2}) = \sum_{i=1}^{n} K_i \times ISE_i \tag{4-2}$$

$$ISE_{Vdc,Vac} = \int_{t=Tdeblock}^{t=Tss} w(t)[(V_{dcref} - V_{dc})^2 + (V_{acref} - V_{ac})^2 + V_{hm}{}^2]dt \tag{4-3}$$

$$ISE_{P,Vac} = \int_{t=Tdeblock}^{t=Tss} w(t)[(P_{ref} - P)^2 + (V_{acref} - V_{ac})^2 + V_{hm}{}^2]dt \tag{4-4}$$

4.5 Relaxation Optimization Method Evaluation

The relaxation optimization method was tested using a detailed electromagnetic transients simulation for a six-terminal VSC-HVdc system. In the cases in which an averaged valve bridge model were used, a 50 μs solution time step was utilized; however, in order to accurately simulate the switching of the IGBTs of the converters, in the case in which a 2-level valve bridge model was used, a 10 μs solution time step was used in the EMT simulation program.

4.5.1 Six-terminal System Description

A six-terminal ±320 kV VSC-HVdc grid, shown in Figure 4-4, was set up for the control parameter optimization study. In this thesis, it is assumed the electrical distance between the converters is large enough so that the interaction between the connected ac systems can be ignored. The converter nominal ratings used in the examples are listed in Table 4.1.

Table 4.1: VSC-HVdc System Parameters

Rated ac system voltage	230 kV, 60 Hz
AC system impedance angle	80°
Rated dc power rating (base)	500 MW (or 1000 MW)
DC voltage	±320 kV
Converter transformer rating	583 MVA (or 1166 MVA)
Converter transformer ratio	230 kV/333 kV
Converter transformer and reactor impedance	0.15 pu
Passive high pass filter	75 Mvar (or 150 Mvar)
Converter	2-level PWM
DC capacitor	500 μF
Switching frequency	900 Hz
DC cable: 321.5 kV and 1563 A, copper	2400 mm^2

The system operating conditions during the optimization process were as follows:

VSC 1, VSC3, VSC4, VSC5: (500 MW rating) P and V_{ac} control

Disturbance: Rec -> Inv -> Rec (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 2

VSC 6: (1000 MW rating) P and V_{ac} control

Disturbance: Inv -> Rec -> Inv (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 2

VSC 2: (1000 MW rating) V_{dc} and V_{ac} control

AC system SCR: 4

DC cable: Cable 1, 2: 80 km; Cable 3:160 km; Cable 4: 64 km.

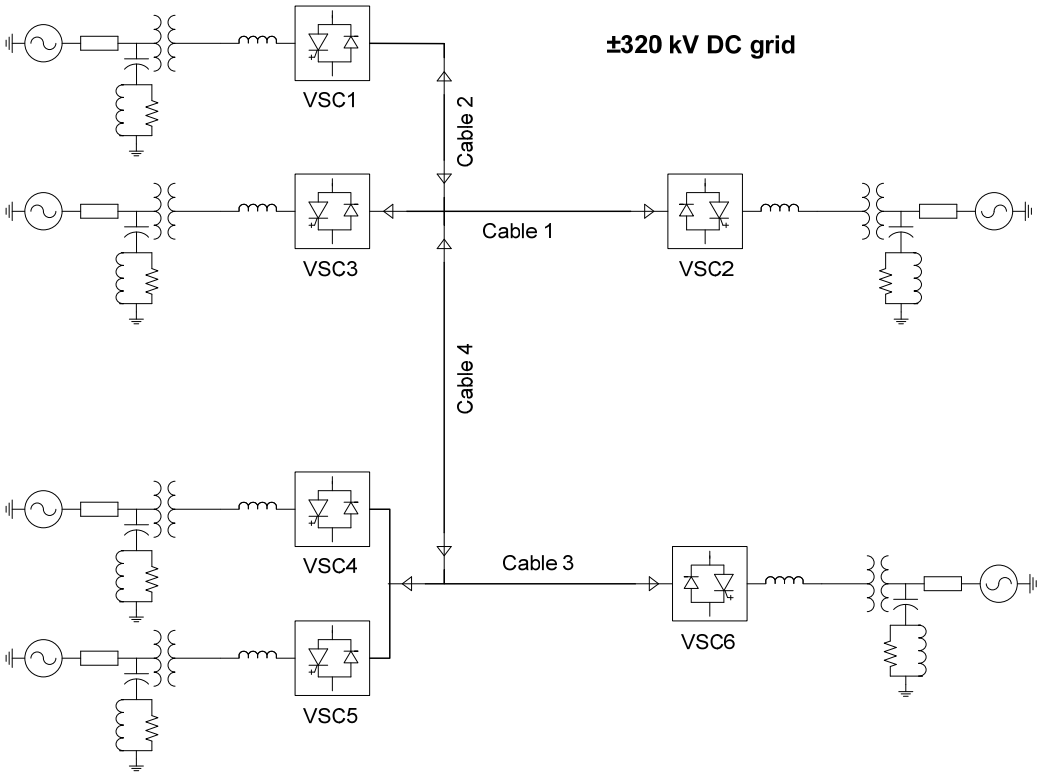


Figure 4-4: Six-terminal VSC-HVdc grid

The control system for the six-terminal VSC-HVdc grid comprises terminal controllers and a master controller. The main functions for controlling the active power, the reactive power, the ac voltage, and the dc voltage are incorporated in the terminal controllers as show in Figure 2-11. The master controller is provided with the minimum set of functions necessary for coordinated operation of the terminals, such as de-block and block, in a certain order to reduce the start-up dynamics. The master controller sends a de-block signal to the dc voltage controlling converter VSC2 to build up the dc voltage at 0.2 s and then sends signals to de-block other converters at 0.3 s.

4.5.2 Objective Function Selection

First, the terminal that controls dc voltage is selected for control parameter optimization. The objective function (equation 4-5) is used. The objective function consists of six sub-objective functions to reflect the six terminals, in which $ISE_{Vdc,Vac}$ and $ISE_{P,Vac}$ are sub-objective functions defined from equations 4-3 and 4-4. Several different weighting factor sets have been tried during the design cycle through trial and error, it is found the interactions from the other converters have limited influence on the dc voltage controlling converter performance. The relatively big weighting factor of 10 chosen for the VSC2 sub-objective function is used to penalize the error produced by the VSC that controls V_{dc} and V_{ac}.

$$of(K_{p\_Vdc}, T_{i\_Vdc}, K_{p\_Vac}, T_{i\_Vac}) = 10 \times ISE_{Vdc,Vac} + \sum_{i=1}^{5} ISE_{(P,Vac)i} \qquad 4\text{-}5$$

Next, the other terminals with P and V_{ac} that control VSCs are optimized on control parameter selection. Since two VSCs are at same dc bus, their controllers are assumed to be identical. Equation 4-6 is the designed objective functions for VSC1, VSC3, VSC4, and VSC6, in which $ISE_{Vdc,Vac}$ and $ISE_{P,Vac}$ are sub-objective functions defined from equations 4-3 and 4-4. As before, the relatively big weighting factor of 10 for the relative sub-objective functions is used to penalize the error produced by the respective terminal.

$$of(K_{p\_P}, T_{i\_P}, K_{p\_Vac}, T_{i\_Vac}) = ISE_{Vdc,Vac} + 10 \times ISE_{P,Vac} + \sum_{i=1}^{3} ISE_{(P,Vac)i} \qquad 4\text{-}6$$

The control system is required to operate satisfactorily when the system is subjected to power order change and disturbances. Using the selected initial control gains, the relaxation optimization can be used again to refine the control gains for different

objectives. The desired steady state and transient operation performance can be improved by adding the desired objectives in the objective functions and by the use of the relaxation method to select the refined control gains.

4.5.3 Study Results

By trial and error, controller parameters for all converters are selected so that the system runs stably at the prescribed operating condition. The losses in the system include 1.5% of converter rating switching loss and cable loss. Hence, VSC2 input and output is around 940 MW from, or to, the dc grid. The disturbance consists of power order changes at 2.5 s and at 4.5 s.

Figure 4-5 shows the real power P and the dc voltage E_{dc} of the VSC2 using the initial trial and error control parameters. The control parameters are not optimized at this stage. The results show that even though the system is stable at the initial operation condition, it will go to unstable when the system operation conditions are changed. The control parameters need to be optimized for different operating conditions.

By using the relaxation method, the VSC that controls dc voltage is optimized first; then the VSCs that control the real power are optimized one by one. The optimized control parameter values are listed in Table 4-2. The results show that when all ac system SCRs are the same, the optimized control gains are similar for all the VSCs with real power control. The interaction between control gains optimization and different VSC terminals is very minimal if the dc voltage of the grid is properly controlled. Figure 4-6 shows the results when the control parameters are optimized. When Figure 4-6 is compared to

Figure 4-5, it can be seen that the relaxation optimization method did a good job regarding control parameters selection for different operating conditions.

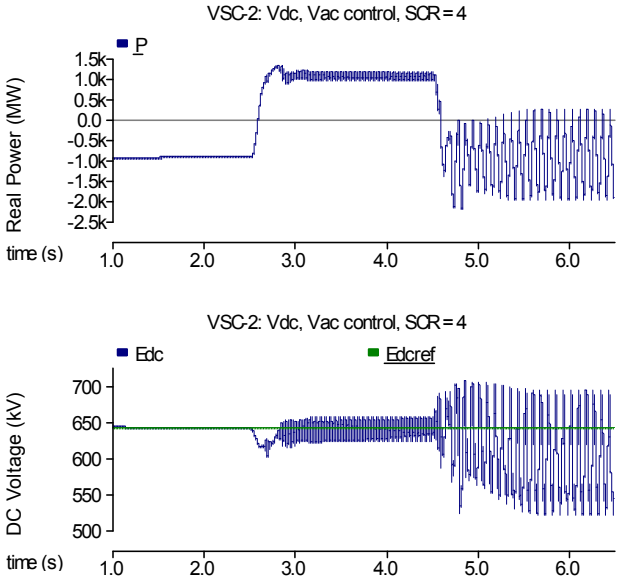


Figure 4-5: Real power and dc voltage for VSC2: pre-optimization (averaged model)

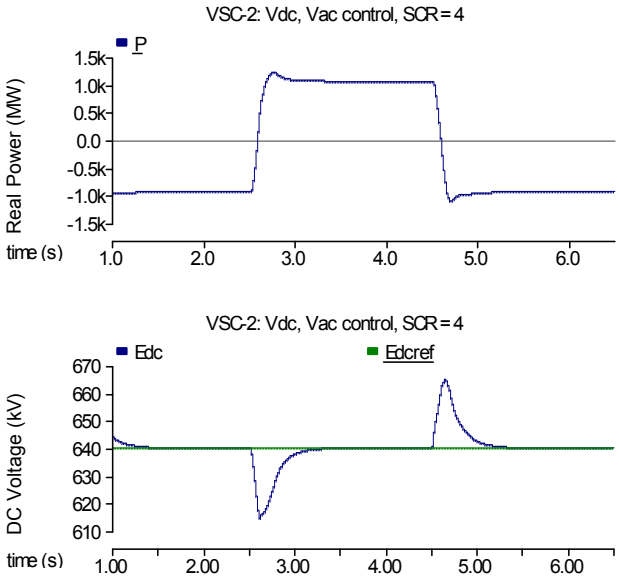


Figure 4-6: Real power and dc voltage for VSC2: after-optimization (averaged model)

Table 4-2: Optimized Control Parameter Values

Outer PI Controller	VSC2		VSC6		VSC1		VSC3		VSC4	
	K_p	T_i	K_p	T_i	K_p	T_i	K_p	T_i	K_p	T_i
V_{dc}	14.15	0.006	-	-	-	-	-	-	-	-
P	-	-	0.887	0.015	0.885	0.015	0.885	0.015	0.885	0.015
V_{ac}	4.444	0.029	0.553	0.018	0.553	0.014	0.553	0.014	0.553	0.014

In the simulation, it was found that when one converter is optimized, the sub-objective functions from other converters do not experience significant changes unless the case goes unstable. This indicates the relaxation optimization method in which the VSC terminals are optimized one by one has a good chance of working in a multi-terminal VSC-HVdc system.

In order to validate the selected control parameters, the averaged valve bridge model was replaced by the detailed two-level converter model. The control gains obtained from the averaged model in Table 4-2 were used in the detailed model. The objective functions and the sub-objective functions of the averaged model are compared to those of the detailed model in Table 4-3. The object functions for the detailed model are large due to the ac voltage harmonics caused by IGBT switching. However, for both averaged model and detailed model, it can be seen that when the ac system SCR is the same, the obtained objective functions are the similar for all the VSCs with real power control.

Table 4-3: Objective Functions of Averaged and Detailed Model Representation

	Obj for averaged model				Obj for detailed model			
	obj	$obj_{\_Vdc}$	$obj_{\_Vac}$	$obj_{\_Vhm}$	obj	$obj_{\_Vdc}$	$obj_{\_Vac}$	$obj_{\_Vhm}$
VSC2	0.854	0.811	0.004	0.039	2.085	0.010	0.016	2.059
	obj	$obj_{\_P}$	$obj_{\_Vac}$	$obj_{\_Vhm}$	obj	$obj_{\_P}$	$obj_{\_Vac}$	$obj_{\_Vhm}$
VSC6	0.236	0.089	0.015	0.133	2.796	0.451	0.023	2.322
VSC1	0.239	0.089	0.016	0.134	2.647	0.417	0.016	2.214
VSC3	0.239	0.089	0.016	0.134	2.675	0.423	0.020	2.232
VSC4	0.239	0.089	0.016	0.134	2.722	0.436	0.021	2.265

The dc voltage E_{dc} and the active power P of the detailed two-level valve bridge model of the VSC2 are shown in Figure 4-7. Compared to Figure 4-6, which shows the averaged model, there is no noticeable difference between the two representations.

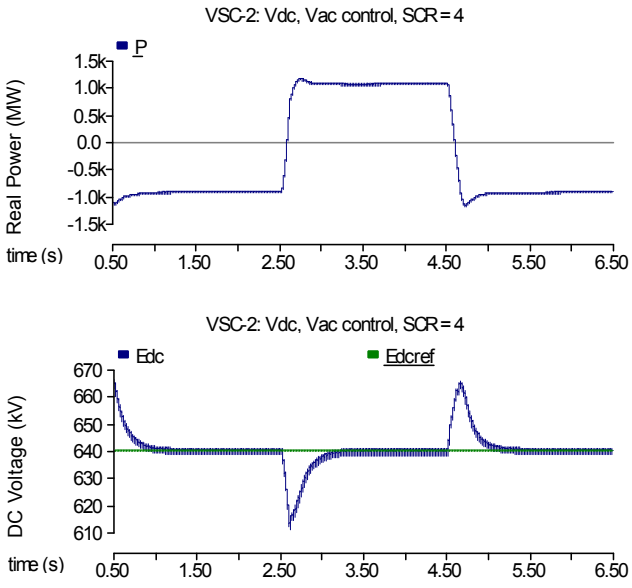


Figure 4-7: Real power and dc voltage for the VSC2: 2-level model

4.5.4 Computational Time Comparison

When the detailed two-level valve bridge model is used, the *6.5* s simulation with *10* μs time step and *100* μs plot step in PSCAD/EMTDC takes *240* minutes to run on an Intel® Core™2 Duo CPU computer with 1.96 GB of RAM running at 3.00GHz. The lengthy computational time makes the optimization process excessively slow and thus impractical for the detailed model representation. If the detailed two-level valve bridge model was replaced by averaged valve bridge model, the same *6.5* s simulation would take *25* minutes on the same computer, approximately 10 times less time.

4.6 Conclusions

Along with the increased number of converters in a dc grid, HVdc grids will impose a big challenge to the controller gains optimization process. In this chapter, an alternative approach that allows the optimizations of different converters to be conducted one at a time, the relaxation method, was introduced. Although the results are sub-optimal, the computational burden is manageable. By using the averaged valve bridge model in the initial control parameter optimization process, the computational time can be reduced substantially. The detailed valve bridge model can be used to evaluate the performance of the control parameter selection.

Even though the control variables are reduced to one converter by using the relaxation method, the computational time is lengthy if the whole system is represented by the detailed valve bridge model. The robust controller parameters selection for different operation conditions using the whole system detailed valve bridge model representation

is, therefore, impractical. An improved relaxation optimized method for multi-terminal VSC-HVdc system control parameter optimization is introduced in the next chapter.

Chapter 5: Single Converter Relaxation Method to Optimal Gains for DC Grid Converters

5.1 Introduction

As mentioned in Chapter 4, ideally, the full multi-terminal system should be optimized in one attempt. By using the relaxation approach, the large number of control variables can be reduced to the control variables for one converter. But, as demonstrated in Chapter 4, even with that simplification, the optimization process for the full system is too slow. In this chapter, a new method, the "single converter relaxation method", is proposed and validated.

The optimized settings that may be optimal for a given operating configuration may be inadequate for another. Selecting robust control gains for acceptable overall performance over a range of operating points (consider changing SCR of the ac system) is necessary. However, using the full system in the optimization process could be a challenge. In this chapter, a new method for the selection of robust control gains for acceptable overall performance on a range of the operating points of multi-terminal VSC-HVdc converters, the single converter relaxation method, is presented. Then, the full model relaxation method and the single converter relaxation method are compared and recommendations are made.

5.2 Using the Single Converter Relaxation Method to Set the Gains for DC Grid Converters

By doing multiple examples, it was observed that the performance of one VSC converter in the grid is really not significantly impacted by the others, as the dc voltage controlling converter maintains the grid voltage and insulates the converters from interacting with each other. This observation suggests a simpler way to conduct the optimization. This approach is described below.

Given a dc grid with one converter in dc voltage control and the other converters in dc power control, each of the dc power controllers (which may be connected to ac networks of different SCRs) is independently optimized. The principal behind this method is the observation that the optimal gains of a dc power controlling converter connected to a constant voltage dc grid are independent of the other converters on the grid. Although, impedances of transmission lines and other grid equipment may transiently cause the dc voltage to vary at any converter, they do not appear to affect the efficacy of this approach, as will be shown later in this section.

5.2.1 Control Parameters Selection and Design Procedure

Consider the six-terminal dc grid of Figure 5-1 with un-optimized control gain sets of G1, G2, G3, G4, G5, and G6, where G2 is the gain set of the voltage controlling converter and the others are the gain sets of the power controlling converters. The steps of the proposed single converter relaxation method are as follows:

Step A: First, the control gains G1 for the converter (including its connected ac network) with dc power control are optimized with it connected to a dc voltage source. The dc

source stands in for the nominally constant voltage of the dc grid, as shown in Figure 5-1 (a). The same procedure for optimizing the gains used for converter 1 is applied to the other dc power controlling converters, as shown in Figure 5-1 (a1), (a2), (a3), and (a4).

Step B: The dc voltage controlling converter is introduced together with its ac system and connected to the optimized converter 1 with optimized gains G1*, as in Figure 5-1 (b). The dc voltage controlling converter controller gains are now optimized. Now we have all converters optimized individually.

Step C: The dc grid is connected using the optimized gain sets G1*, G2*, G3*, G4*, G5*, and G6*, as in Figure 5-1 (c) and re-simulated as a check.

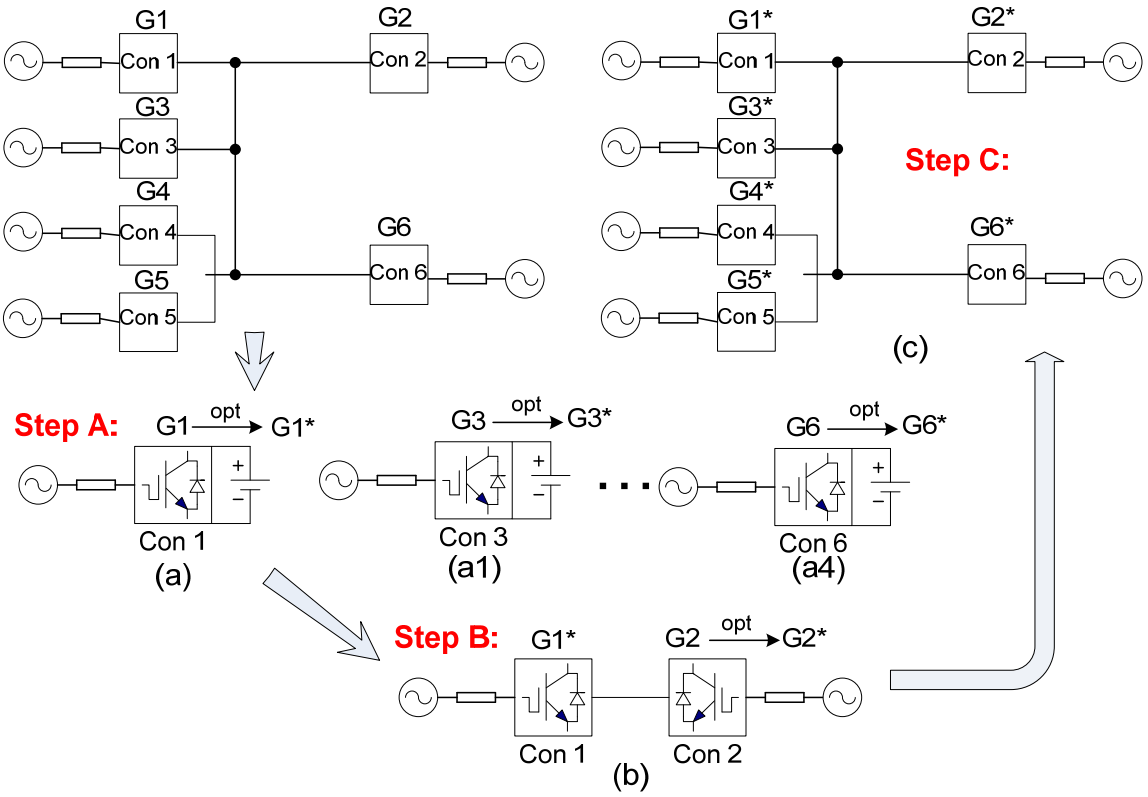


Figure 5-1: Procedure of the single converter relaxation method

5.2.2 Ensuring Robust Control Gains Selection

In the single converter relaxation method proposed in Section 5.2.1, it was assumed that each converter is connected its own ac network, which was assumed to be fixed. However, if the connected ac system changes, i.e., the SCR changes, the optimized control gains may be sub-optimal to the changed SCR, or may even result in unstable operation. Hence, the controller tuning process must be modified and a more robust approach in which the optimized gains work for the range of expected SCRs developed. One approach is the inclusion of robustness into the design using optimization-enabled transient simulation [65][62], as shown in Figure 4-2. Another approach proposed in this thesis is to optimize the converter to operate for the worst or near worst expected condition (usually the lowest SCR) and use those gains for all operating points, even though the performance may be sub-optimal for those points.

Approach #1: Selection using robust optimization:

The first approach used to select the robust gains is via the method of robust optimization [65][62]. Here, each optimization step with the trial parameter set has "n" simulations, for the "n" SCRs under consideration. Each run produces a sub-objective function, and the net objective function is evaluated at the end of the "n" simulations by totaling these sub-objective functions. Hence, a single objective function is assigned to the set of "n" runs, and for the purposes of the non-linear optimization (NLO) program, this constitutes one step. A new parameter set is selected by the non-linear optimization (NLO) program and tried out in the next set of "n" runs. It is clear that this optimization approach yields a parameter set that is optimized for the set of "n" SCRs as a whole, although it may not be optimal for any specific SCR. However, this approach is computationally demanding and

requires very long computer usage times. That is why it was not convenient to apply it in the simulation in which the entire dc grid was modeled in Chapter 4. Here it is possible to use this approach because only one converter is being optimized at a time. Nevertheless, it is still a computationally intensive task, and it is possible that many EMT simulators may not have a robust optimization algorithm.

Approach #2: Selection using engineering judgment:

Observation from repeated simulations has shown that gains designed for a weaker system with lower SCR do work reasonably well for a stronger system with larger SCRs, even though their performance may be somewhat sub-optimal. However, gains selected for a stronger system, often cause instability when the SCR is weaker. With these observations, an approach described below can be used:

1. Assume a range of operating SCRs (i.e., $SCR_1 < SCR_2 < \ldots < SCR_n$). Optimize the controller gains for the most likely operating condition SCR_k with gains as G^*_{SCRk}.
2. Check the converter operation at all the other SCR values (SCR_1, SCR_2, SCR_{k-1}, SCR_{k+1}, …, SCR_n) using the gain set G^*_{SCRk}. The gains will provide optimal operation for the most likely operating point $SCR = SCR_k$, but will be suboptimal at other SCRs. Also, from the observation, operation for a $SCR_j > SCR_k$, will be stable, although may be slower than that with optimized gains G^*_{SCRj}. However, there is a risk that for a smaller $SCR_m < SCR_k$, the converter may become unstable. If so, select the next lowest SCR, SCR_{k-1}, and repeat the procedure. If this works for all operating points, stop. If not, repeat, with next lowest SCR.

3. Carry out the same procedure for robust control gains selection for the other converters.

5.3 The Optimization Process using the Single Converter Relaxation Method

The overall optimization process, including the ensuring of robustness to SCR variation, is discussed in this section. Step A and Step B (detailed in Figure 5-1 of Section 5.2) of optimizing the controller gains of a power controlling converter and a dc voltage controlling converter are discussed for one-terminal and two-terminal examples. Step C of the final optimizing process in Figure 5-1 is discussed for a six-terminal system.

5.3.1 System Description and Objective Functions Selection

The converter nominal ratings used in the examples are the same as those listed in Table 4.1. The system operating conditions during the optimization process are the following:

<u>One-terminal system:</u>

VSC 1: (500 MW rating) P and V_{ac} control

Disturbance: Rec -> Inv -> Rec (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 1.6, 1.8, 2, 3, and 4

DC cable length: 45 km (check with 0 km and 110 km)

<u>Two-terminal system:</u>

VSC 1: (500 MW rating) P and V_{ac} control

Disturbance: Rec -> Inv -> Rec (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 2

VSC 2: (500 MW rating) V_{dc} and V_{ac} control

AC system SCR: 1.8, 2, 3, and 4

DC cable length: 45 km (check with 0 km and 110 km)

Six-terminal system:

VSC 1, VSC3, VSC4, VSC5: (500 MW rating) P and V_{ac} control

Disturbance: Rec -> Inv -> Rec (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 2

VSC 6: (1000 MW rating) P and V_{ac} control

Disturbance: Inv -> Rec -> Inv (full power ramping rate of *100 ms/1000 MW*)

AC system SCR: 2

VSC 2: (1000 MW rating) V_{dc} and V_{ac} control

AC system SCR: 4

DC cable: Cable 1, 2: 80 km; Cable 3:160 km; Cable 4: 64 km.

The controller gains optimization is based on per unitized system parameters. The optimization design objectives are:

- Control the real power to the desired value for the power controlling converter or control the dc voltage to the desired value for the dc voltage controlling converter
- Maintain the ac voltage at the desired value
- Keep the ac voltage with lower harmonics

The one-terminal system is used to optimize the control gains for the power controlling converter. A single objective function to be used as the function of four controller gains, named K_{p_P}, T_{i_P} (for real power control) and K_{p_Vac}, T_{i_Vac} (for ac voltage control), can be generated based on the well-known integral square error (ISE) measure. The objective function in equation 5-1 consists of three sub-objective functions for the three optimization design objectives. The two-terminal system is used to optimize the control gains for the dc voltage controlling converter. A single objective function to be used as the function of four controller gains, named K_{p_Vdc}, T_{i_Vdc} (for dc voltage control) and K_{p_Vac}, T_{i_Vac} (for ac voltage control) can be generated based on the well-known integral square error (ISE) measure. The objective function in equation 5-2 consists of three sub-objective functions for the three optimization design objectives. The different weights w_1, w_2, and w_3 for the three sub-objective functions are given to reflect the different importance of the sub-objective functions and to ensure their comparable contributions to the *ISE* based on the per unitized system parameters.

$$obj(K_{p\_P}, T_{i\_P}, K_{p\_V_{ac}}, T_{i\_V_{ac}}) = obj_{\_P} + obj_{\_V_{ac}} + obj_{\_V_{hm}} = ISE_{\_P} \qquad 5\text{-}1$$

$$\text{where, } ISE_{\_P} = \int_{t=T_{deblock}}^{t=T_{ss}} [w_1(t)(P_{\_err})^2 + w_2(t)(V_{ac\_err})^2 + w_3(t)(V_{hm})^2]dt$$

$$obj(K_{p\_V_{dc}}, T_{i\_V_{dc}}, K_{p\_V_{ac}}, T_{i\_V_{ac}}) = obj_{\_V_{dc}} + obj_{\_V_{ac}} + obj_{\_V_{hm}} = ISE_{\_V_{dc}} \qquad 5\text{-}2$$

$$\text{where, } ISE_{\_V_{dc}} = \int_{t=T_{deblock}}^{t=T_{ss}} [w_1(t)(V_{dc\_err})^2 + w_2(t)(V_{ac\_err})^2 + w_3(t)(V_{hm})^2]dt$$

5.3.2 Step A: Power Controlling Converter Optimization

An example of the new proposed procedure is now described. The one-terminal system is used to optimize where the control gains for the VSC with real power and ac voltage control are selected to permit operation over a range of operation conditions. The interaction between the control gains and the cable length change will also be evaluated. Figure 5-2 shows one VSC connected to a dc voltage source representing the remote converter (assumed to be in control of the dc voltage).

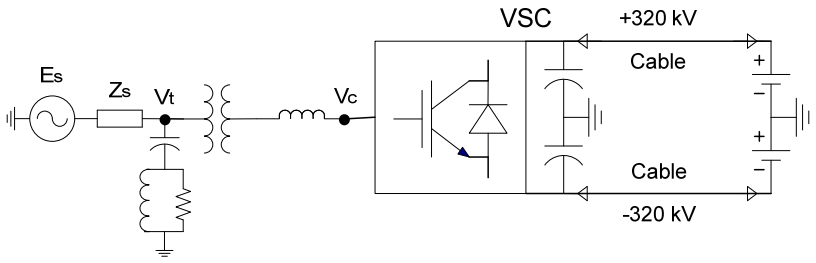


Figure 5-2: One-terminal VSC-HVdc system

5.3.2.1 Parameter Optimization for Operation over a Range of Different SCRs

In the one-terminal system, the controller gains are optimized for different ac system SCRs. The optimized gains for different ac system SCRs are shown in Table 5.1.

Table 5.1: Optimized Gains and OFs for a Power Controlling Converter

SCR	K_{p_P}	T_{i_P}	K_{p_Vac}	T_{i_Vac}
1.6	0.415	0.034	0.572	0.018
1.8	0.458	0.033	1.160	0.014
2	0.524	0.034	0.607	0.018
3	0.662	0.011	2.549	0.011
4	2.158	0.010	0.214	0.011

It can be seen that when the ac system SCR changes, a different set of controller gains will give optimal performance for that particular SCR ac system. This means that optimal

gains selected for one SCR may not be suitable when the ac system changes and has a different SCR. Two solutions are possible. In the first solution, a single set of gains is selected and checked by simulation to determine if the performance is still reasonable for other SCRs. This procedure, referred to as "robust gain selection", is discussed in this chapter. Alternatively if some way of estimating SCR is available (i.e., estimating the SCR from the status of breakers connected to transmission lines or by using a scanning approach), the optimal gains in Table 5.1 could be switched into the controllers as the SCR changes. This is discussed in the next chapter.

5.3.2.2 Robust Gains Selection for a Power Controlling Converter

The first approach (Approach #1), is of robust optimization. Here an aggregated OF is optimized, with simulations conducted at several ac system conditions. In this example, the optimization was conducted with ac system SCRs of 1.6, 2 and 4 respectively (weak to strong). The resultant gains are optimal for the full range of SCRs.

An alternative approach (Approach #2) is to use engineering judgement and select the parameters corresponding to a mid-range SCR from Table 5.1, and, via simulation, check to determine whether the performance at the other SCRs is still adequate. If the performance is adequate, this single set of parameters is entered into the controller for the entire operating range. It is likely that this gain will be closer to the lower end of SCRs because the lowest SCR is where the system is most fragile and the lowest SCR typically has the lowest numerical values for the gains. However, if the parameters corresponding to lowest SCR are selected, the system response may be very slow at the higher SCR values. So in Table 5.1, a good set of candidate gains are those for SCR = 1.8 or SCR = 2.

As per the above discussion, the lowest (SCR = 1.6) gains could have been used for all SCRs, but it was observed that the gains obtained when SCR = 2 worked adequately at the lower SCRs and the higher SCRs, but gave 100% optimized performance at SCR = 2, which is closer to the middle of the SCR range. The study showed that the higher SCR gains will not work for a lower SCR system. Hence, the gains obtained at SCR = 2 were chosen as the robust gains set for the power controlling converter.

The initial gains and the selected robust gains for both approaches are listed in Table 5.2, as are the optimization run numbers for the two approaches. The sub-objective functions (OF_i) for each of the three runs and the cumulative objective function (OF) are also shown. Compared to Approach #2, the robust optimization algorithm (Approach #1) reduces the OF from 9.411 to 8.944. The engineering-judgement-based Approach #2 results in only a slightly poorer OF of 9.411. Approach #1 does a much better job for the lowest SCR (SCR = 1.6) (OF_1=3.016) than Approach #2 (OF_1 = 3.702).

Table 5.2: Robust Gains and OFs for Power Controlling Converter

Approach	K_{p_P}	T_{i_P}	K_{p_Vac}	T_{i_Vac}	OPT Run #	SCR=1.6 OF_1	SCR=2 OF_2	SCR=4 OF_3	OF
Initial	1	0.04	1	0.016	-	102.6	3.077	2.683	108.3
#1	0.562	0.043	0.523	0.014	243	3.016	3.113	2.815	8.944
#2	0.524	0.034	0.607	0.018	67	3.702	3.018	2.691	9.411

Figure 5-3 to Figure 5-5 show the robust optimization in action. In these figures, the real power *P* and the RMS ac voltages at ac voltage terminal V_{ac} are shown.

With initial gains selected, as shown in Figure 5-3, the operation at the lower SCR of 1.6 is unstable.

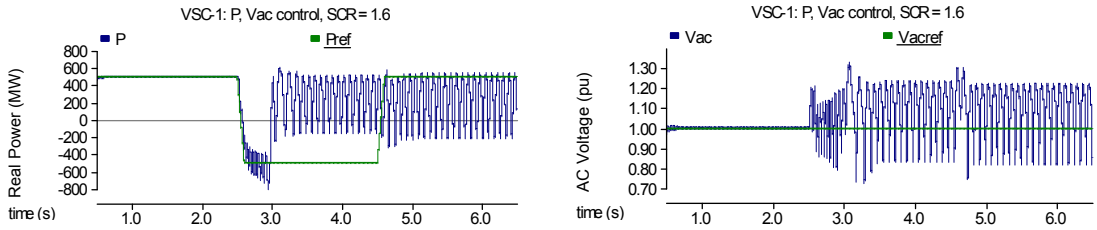


Figure 5-3: One-terminal VSC for robust gains selection (Initial gains)

However, performance with the optimized gains, as shown in Figure 5-4 (Approach #1), is good for all the SCRs considered. Figure 5-5 shows the results for the engineering-judgement-based Approach #2, where the response is stable and has minimal overshoot, being very similar to the optimized waveforms of Figure 5-4.

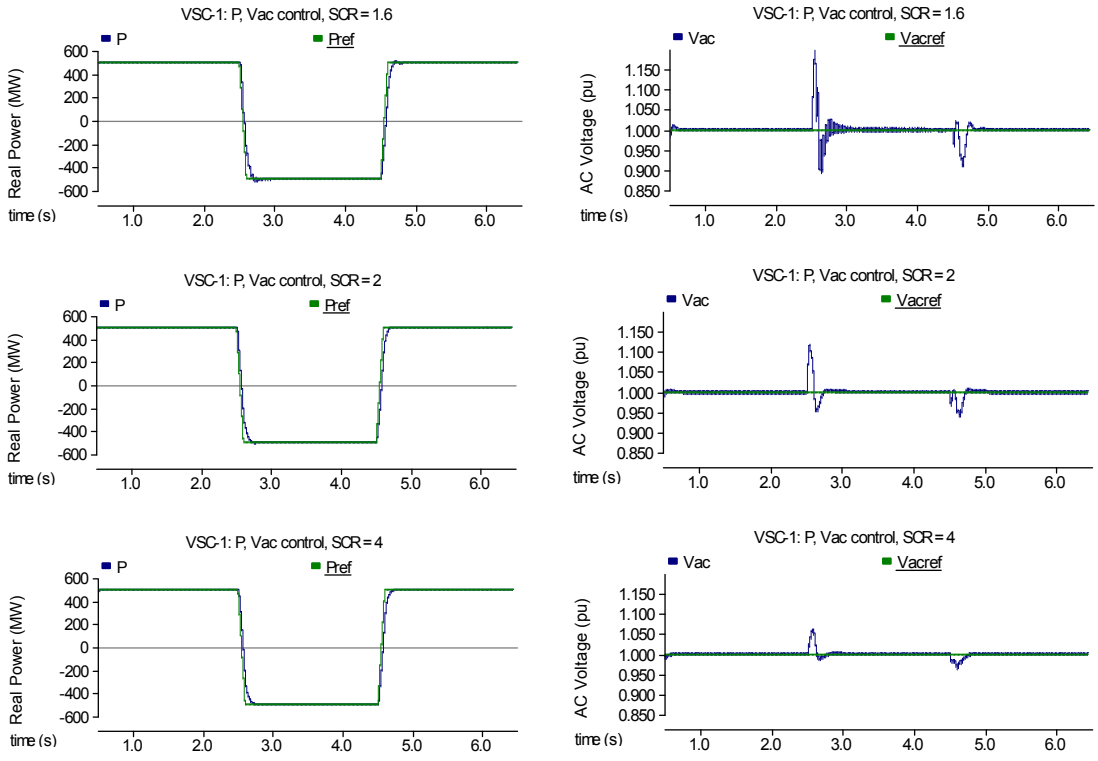


Figure 5-4: One-terminal VSC for robust gains selection (Approach #1)

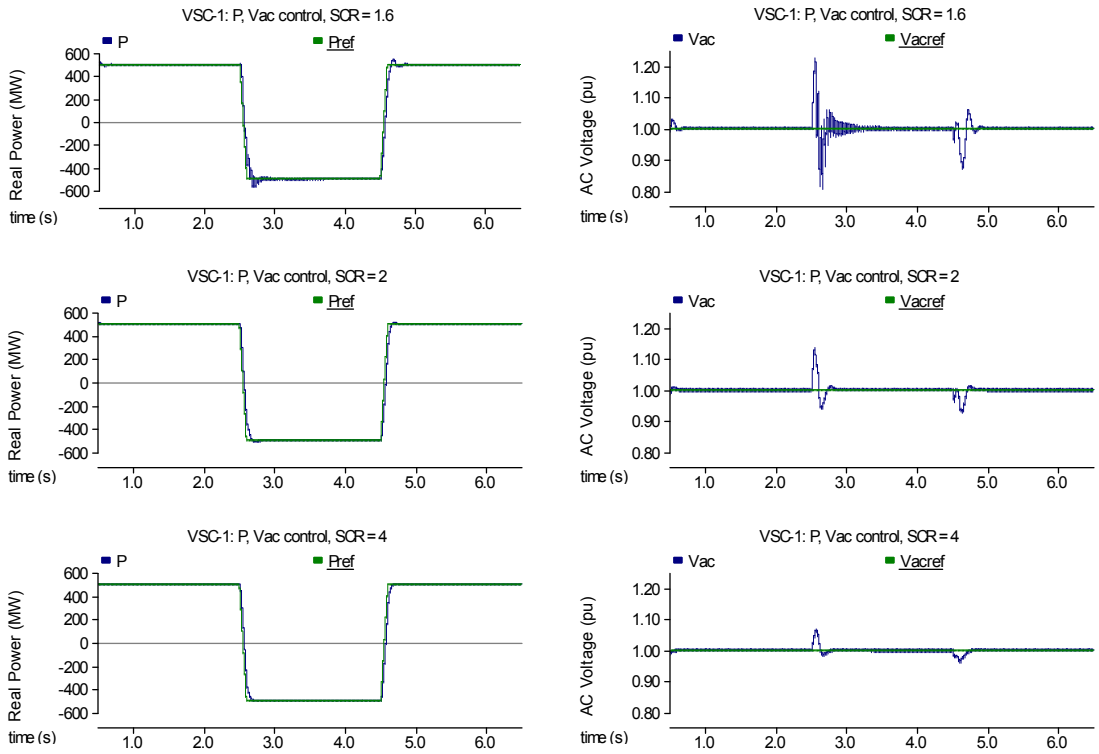


Figure 5-5: One-terminal VSC for robust gains selection (Approach #2)

The simulation results show both approaches will give the system acceptable performance; however, Approach #2 will use less computational time. Hence it is the method of choice.

5.3.2.3 Control Gains Interaction from Cable Length Change

The interaction between the cable length and the optimized control gains was studied by changing the cable length from 0 km to 45 km to 110 km. The study shows the objective function obtained will be essentially unchanged for different cable lengths. Therefore, the real power and ac voltage control gains optimization is not sensitive to cable length change if the dc voltage is controlled to a constant.

5.3.3 Step B: DC Voltage Controlling Converter Optimization

The next step in the proposed optimization procedure is to connect the dc voltage controlling converter VSC2 to the power controlling converter VSC1. In this step, the dc voltage controlling converter control gains will be optimized. Step A has already been carried out in Section 5.3.2. Unlike the optimal parameters of power controlling converters, the optimal parameters of voltage controlling converters were found to be dependent on the connecting dc cable length, which is shown in this section.

An example of the two-terminal system, shown in Figure 5-6, is used to optimize where the control gains for the VSC2 with V_{dc}, V_{ac} control are selected to permit operation over a range of operation conditions. The VSC1 with P, V_{ac} control is connected to a fixed ac system and uses the robust control gains obtained from Section 5.3.2.2.

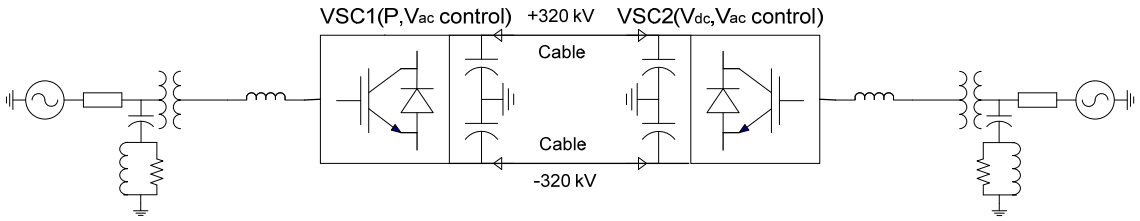


Figure 5-6: Two-terminal VSC-HVdc grid

5.3.3.1 Parameter Optimization for Operation over a Range of SCRs

In Step B, the control gains for the dc voltage controlling converter VSC2 are optimized for different ac system SCRs. The optimized controller gains for VSC2 are listed in Table 5.3. VSC1 was optimized in Step A. The objective functions (OFs) for VSC1 and VSC2 are also listed in the table. It can be seen from Table 5.3 that even though the dc voltage control converter (VSC2) connected ac system SCR is changed from 1.8 to 4, the objective functions for the power control converter (VSC1) are about the same, around

2.8. This validates the approach of tuning power controlling controllers separately. Section 5.4 contains detailed discussion regarding why the single converter relaxation method works.

Table 5.3: Optimized Gains for DC Voltage Controlling Converters and OFs

VSC2 (V_{dc}, V_{ac} control)						VSC1 (P, V_{ac} control)	
SCR	K_{p_Vdc}	T_{i_Vdc}	K_{p_Vac}	T_{i_Vac}	OFs	SCR	OFs
1.8	6.181	0.008	1.233	0.018	4.391	2	2.805
2	23.83	0.007	0.952	0.049	4.054		2.809
3	8.310	0.006	1.443	0.047	1.926		2.819
4	9.416	0.013	0.273	0.009	1.899		2.818

5.3.3.2 Robust Gains Selection for DC Voltage Controlling Converter

As in the case of the power controlling converter (Step A), Approach #1 uses the robust optimization method to optimize an aggregate objective function over three operating points, (i.e., the converter connects to an ac system with SCR = 1.8, 2, and 4).

Another approach, as in the case of the power controlling converter (Step A), is to use the engineering-judgement-based Approach #2, in which a single parameter set works for all anticipated SCRs for the dc voltage controlling converter VSC2. As before, this is specifically optimized for SCR = 2.

The initial gains and the selected robust gains for both approaches are listed in Table 5.4. The optimization run numbers for the two approaches are listed in the table. The sub-objective functions (OF_i) for each of the three runs and the cumulative objective function (OF) are also shown.

Table 5.4: Robust Gains and OFs for a DC Voltage Controlling Converter

Approach	K_{p_Vdc}	T_{i_Vdc}	K_{p_Vac}	T_{i_Vac}	OPT Run #	SCR=1.8 OF_1	SCR=2 OF_2	SCR=4 OF_3	OF
Initial	1	0.01	1	0.01	-	16.68	7.441	4.237	28.36
#1	25.45	0.006	1.143	0.053	165	6.009	4.888	2.633	13.53
#2	23.83	0.007	0.952	0.049	32	6.309	4.615	2.611	13.54

For the two-terminal system, the power controlling converter VSC1 power order P is shown in Figure 5-7. Figure 5-8 to Figure 5-10 show the robust optimization process. In these figures, the dc voltage E_{dc} and the RMS ac voltages at ac voltage terminal V_{ac} are shown. With initial gains selected, as shown in Figure 5-8, the performance is not satisfied. The result for Approach #1 is shown in Figure 5-9. The result for Approach #2 is shown in Figure 5-10. The simulation results show both approaches give the system acceptable performance. This confirms that using engineering judgment (Approach #2) and selecting gains optimized for a single SCR that is somewhat higher than the minimal SCR can ensure adequate performance over the range of SCRs.

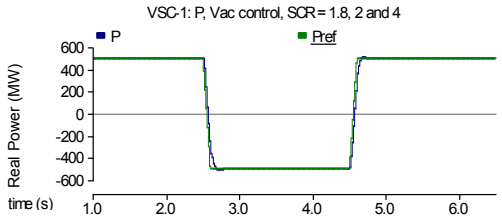


Figure 5-7: Two-terminal VSC system real power P order

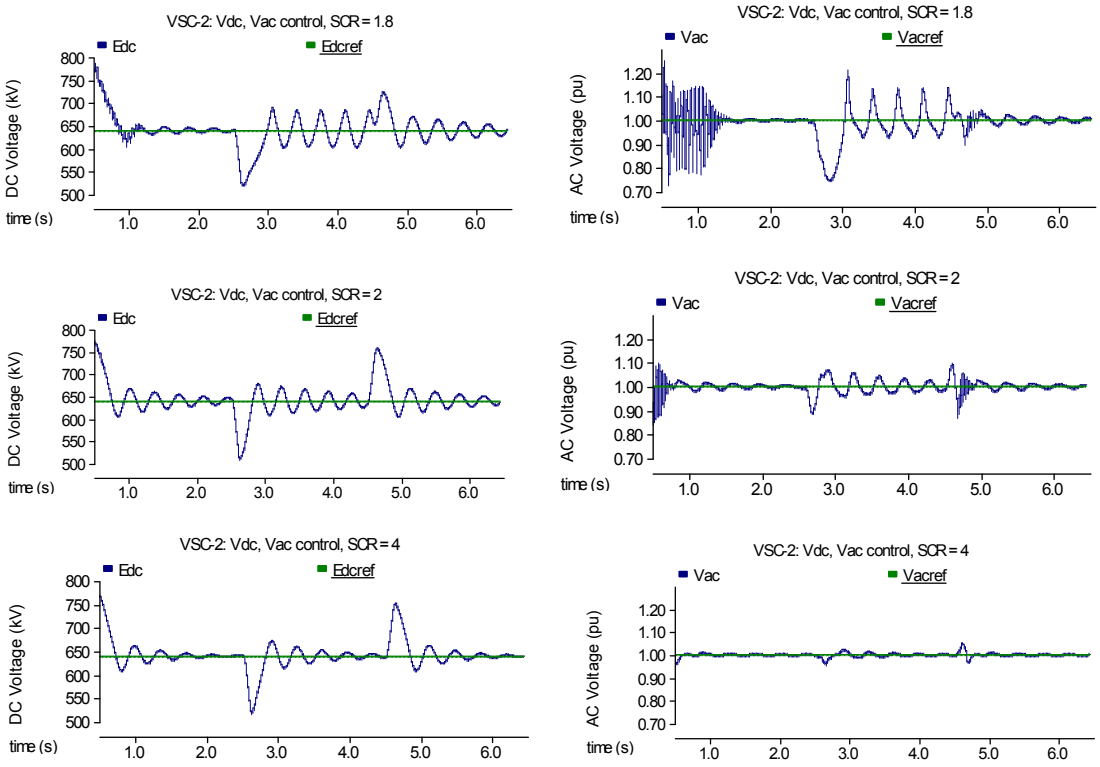


Figure 5-8: Two-terminal VSC for robust gains selection (Initial gains)

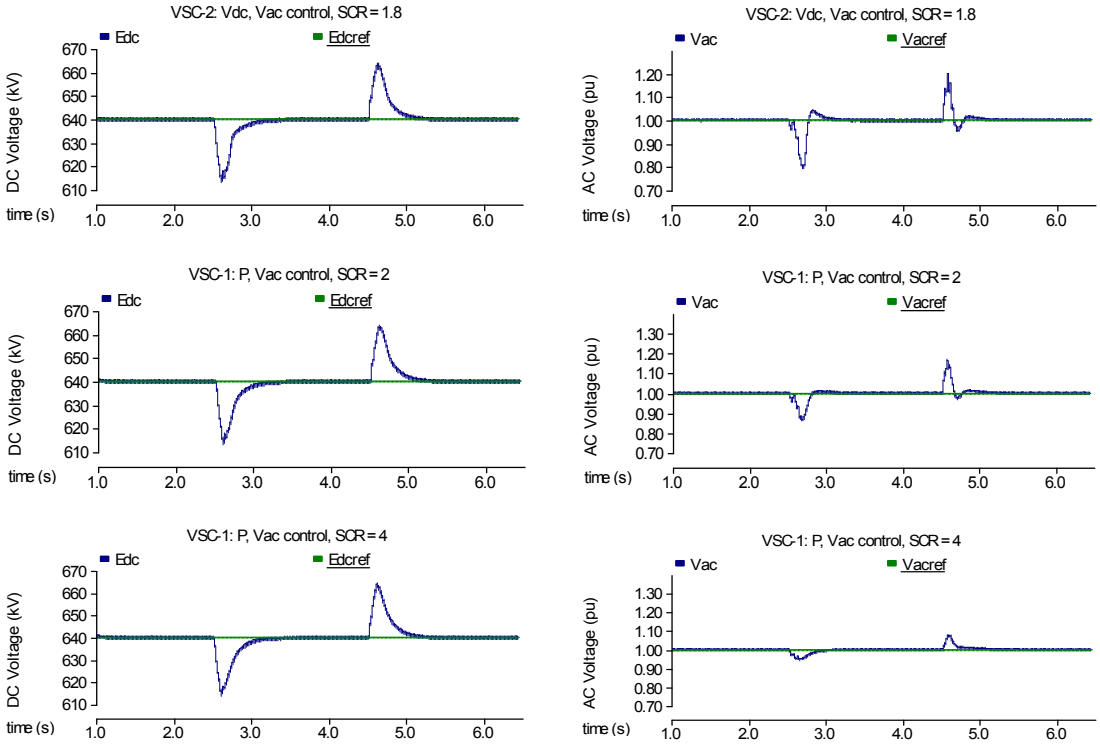


Figure 5-9: Two-terminal VSC for robust gains selection (Approach #1)

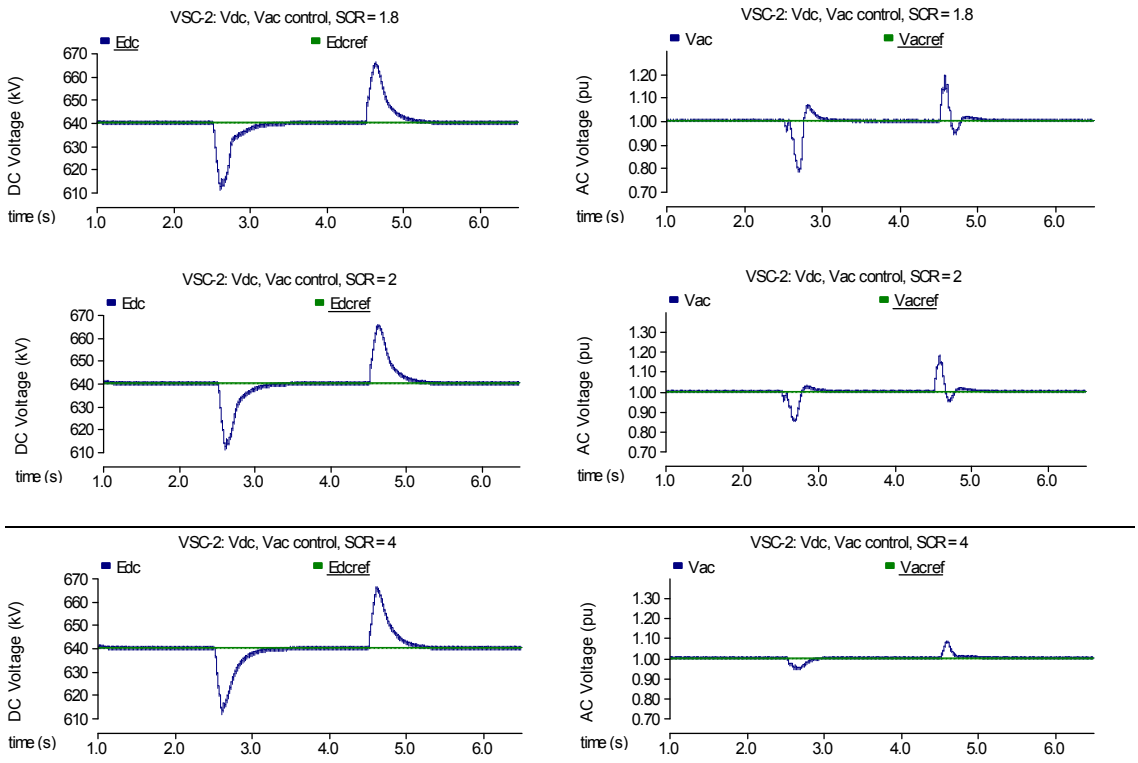


Figure 5-10: Two-terminal VSC for robust gains selection (Approach #2)

5.3.3.3 Control Gains Interaction Resulting from Cable Length Change

The interaction between the cable length and the optimized control gains was studied by changing the cable length. For the two-terminal system in Figure 5-6, the power controlling converter VSC1 was connected to an SCR = 2 ac system and the dc voltage controlling converter VSC2 was connected to an SCR = 2 or SCR = 4 ac system. The robust gains selected in Sections 5.3.2.2 and 5.3.3.2 were used. Table 5.5 shows the comparison of the objective functions when the cable length was changed.

If VSC2 is connected to an SCR = 2 ac system and the cable length is 110 km instead of 45 km, the obtained objective function increases from 4.054 to 9.452. Compared to Figure 5-9 (in which the cable length is 45 km), the performance of the system is adversely affected, as can be seen in Figure 5-11 (in which the cable length 110 km).

However, the robust control gains are still acceptable for the cable length reduction. It can be seen in Table 5.5 that the obtained objective function changes from 4.054 to 4.807 when the cable length decreases from 45 km to 0 km.

Table 5.5: Cable Length Change using Robust Controller Parameters

Cable length	VSC1 (P, V_{ac} control), SCR=2				VSC2 (V_{dc},V_{ac} control)				
	obj	$obj_{\_P}$	$obj_{\_Vac}$	$obj_{\_Vhm}$	obj	$obj_{\_Vdc}$	$obj_{\_Vac}$	$obj_{\_Vhm}$	SCR
45 km	2.809	0.451	0.023	2.336	4.054	0.012	0.127	3.915	2
110 km	3.087	0.458	0.023	2.606	9.452	0.013	0.144	9.295	
0 km	2.791	0.447	0.022	2.321	4.807	0.013	0.135	4.659	
45 km	2.796	0.451	0.023	2.322	2.085	0.010	0.016	2.059	4
110 km	2.808	0.458	0.023	2.327	2.150	0.010	0.016	2.124	

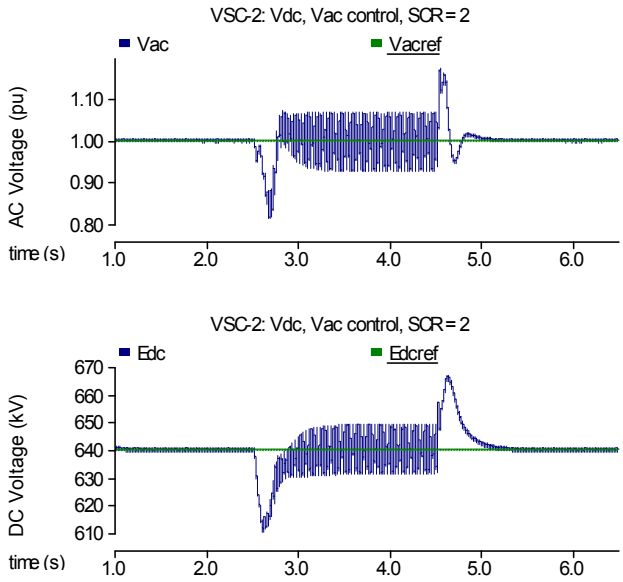


Figure 5-11: VSC2 connected to an SCR = 2 ac system, cable length 110 km

Assume an SCR = 4 system. Table 5.5 shows the comparison of the objective functions when the cable length is 45 km and 110 km (the bottom two columns). The objective functions will not be affected by the cable length change if the connected ac system is relatively strong (i.e., SCR = 4). The obtained objective function only has a minor change,

from 2.085 to 2.15, when the cable length increases from 45 km to 110 km. Figure 5-12 shows the dc voltage and the ac voltage when the connected ac system is SCR = 4 for the VSC with dc voltage control. The system has good performance.

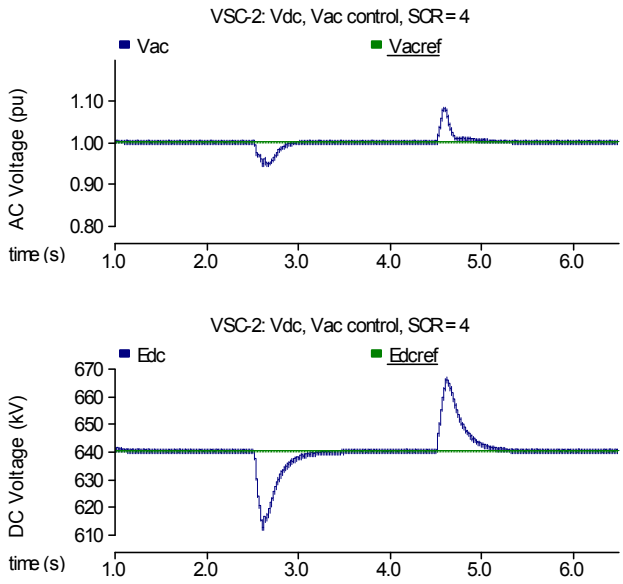


Figure 5-12: VSC2 connected to an SCR = 4 ac system, cable length 110 km

The study shows the robust control gains for a V_{dc}, V_{ac} controller are sensitive to the cable length increase if the VSC is connected to a relatively weak ac system. But the robust control gains will give better performance when the connected ac system is relatively strong. Hence, the voltage controlling converter should be optimized using the longest expected cable length in the dc grid. It is also suggested that given the choice, the VSC connected to a relatively strong ac system should be selected as dc voltage control.

5.3.3.4 System SCR Change

The selected robust control gains were evaluated by changing the ac system SCR using the two-terminal VSC system. In the study, the VSC with real power control was full rectifier operation and the connected ac system impedance changed so that the SCR

changed in steps from *4* to *1.6* to *1.8* to *2.0* and then back to *4*. The VSC with dc voltage control was connected to an SCR = 2 ac system. Figure 5-13 shows the SCR change, the real power *P*, and the RMS ac voltages at ac voltage terminal V_{ac} for VSC1. The results show the chosen robust control gains are acceptable for system SCR changes. For example, when the SCR suddenly changes from 4 to 1.6, the system impedance is changed from 0.25 pu to 0.625 pu. If we assume the voltage at PCC V_t is 1 pu when the connected ac system SCR = 4, the ac system equivalence source voltage E_s is $E_s = \sqrt{1^2 + 0.25^2} = 1.0308\,pu$. When the ac system SCR change to 1.6, assuming E_s is kept unchanged and no control action or reactive power support action occurs, the voltage at the PCC will become $V_t = \sqrt{E_s^{\,2} - 0.625^2} = 0.82\,pu$. In reality the control will respond to some extent so the voltage should be higher than the lowest possible value of 0.82 pu. In the simulation, there is a momentary ac voltage drop to 0.9 pu (i.e. > 0.82 pu) shown in Figure 5-13 during transient.

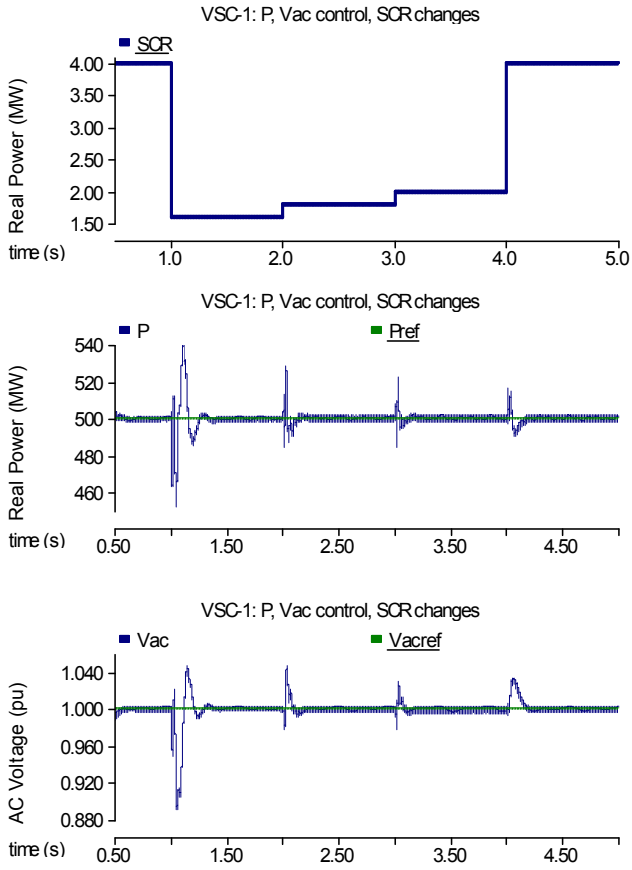


Figure 5-13: VSC1 connected to a variable ac system

5.3.4 Step C: Multi-terminal Converters Optimization

The final step of the single converter relaxation method for multi-terminal converter optimization is Step C of the optimization procedure in Figure 5-1. In this step, the individually optimized power controlling converters (i.e., converters 3, 4, 5, and 6) were connected to the two-terminal system consisting of converters 1 and 2 optimized in Step B. The resulting system is now the optimized six-terminal VSC-HVdc system in Chapter 4, Figure 4-4. As discussed in Sections 5.3.2.2 and 5.3.3.2, a single optimized gain for one low SCR was selected as the constant gain applicable to all SCRs in the range, and was demonstrated to give adequate performance. In the example, the optimized control

gains for the medium SCR, i.e., SCR = 2 were chosen as the robust control gains for the selected range of SCRs. Table 5.6 lists the controller gains for the PLL, inner current controller, and outer controllers.

Table 5.6: Controller Parameters for a Six-terminal VSC System

PLL controller	K_p	T_i	Inner current controller	K_p	T_i
	50	1/250		0.5	1/50
Outer controller	P,V_{ac} controller	K_{p_P}	T_{i_P}	K_{p_Vac}	T_{i_Vac}
		0.524	0.034	0.607	0.018
	V_{dc},V_{ac} controller	K_{p_Vdc}	T_{i_Vdc}	K_{p_Vac}	T_{i_Vac}
		23.83	0.007	0.952	0.049

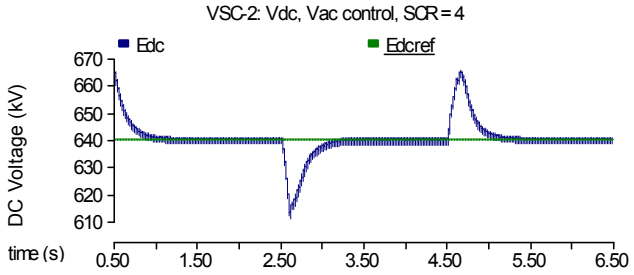
Once the controllers have been optimized, the behavior of the entire six-terminal system should be tested to determine if the individual tuning procedure gives acceptable performance for set-point changes as well as faults. The following objectives were tested in this study.

5.3.4.1 Power Set-point Change

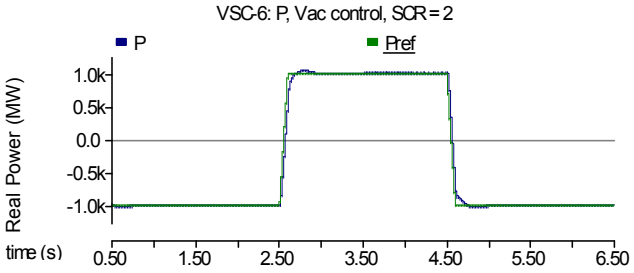
The operation conditions of the six-terminal system are described in Section 5.3.1. The power set-point is changed at 2.5 s and at 4.5 s in the example. The objective functions obtained for each VSC are listed in Table 5.7. The objective functions obtained are close to those obtained from the two-terminal system in Table 5.3. The dc voltage E_{dc} of the dc voltage controlling converter (VSC2) and the transferred real power P of the power controlling converters (VSC6 and VSC1) are shown in Figure 5-14. The robust control gains used for this system give good power set-point change performance, and the measured power essentially follows the *100 ms/1000 MW* power set-point ramping.

Table 5.7: Power Set-point Change for a Six-terminal VSC System

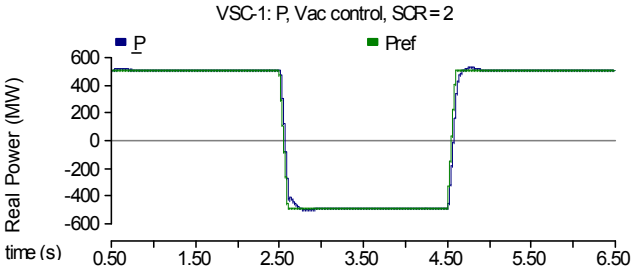
		obj	obj_P	obj_V_{ac}	obj_V_{hm}
P, V_{ac} control	VSC1	3.025	0.414	0.017	2.595
	VSC3	3.047	0.419	0.018	2.611
	VSC4	3.097	0.424	0.018	2.655
	VSC5	3.097	0.424	0.018	2.655
	VSC6	3.094	0.410	0.023	2.661
V_{dc}, V_{ac} control		obj	obj_V_{dc}	obj_V_{ac}	obj_V_{hm}
	VSC2	2.383	0.009	0.016	2.357



(a)



(b)



(c)

Figure 5-14: Power set-point change, six-terminal VSC system (a) VSC2 (b) VSC6 (c) VSC1

5.3.4.2 Faults

In order to verify the dynamic performance of the six-terminal VSC-HVdc system, different faults were applied in the system. Since the system will reach steady state at around *1.0* s in the simulation program, a snapshot was taken at *1.5* s and the fault was applied at *1.55* s. The dc voltage E_{dc}, the ac voltage waveform and the RMS ac voltage at ac source terminal V_{ac}, and the transferred real power P at ac source terminal were plotted to verify the dynamic performance of the selected robust control gains. The following disturbances were applied:

- Three-phase-to-ground ac fault at the ac source terminal
- One-phase-to-ground fault at the ac source terminal
- SCR change of the dc voltage controlling converter

Three- phase-to-ground Fault

A three-cycle three-phase-to-ground fault was applied at the dc voltage controlling converter VSC2 ac bus. The results are shown in Figure 5-15. The robust control gains selected gave good dynamic performance to the six-terminal VSC-HVdc system, with the power returning to normal within approximately 300 ms after fault clearance. Also, ac voltage was brought to 1.05 pu within 300 ms.

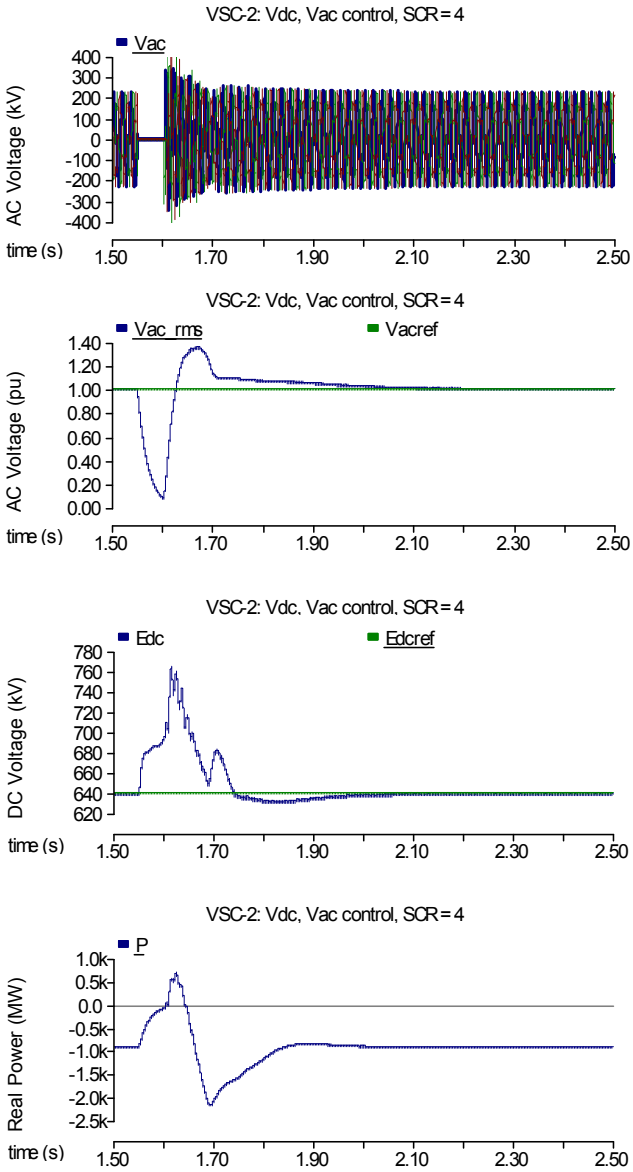


Figure 5-15: Three-phase ground fault at VSC2 ac bus terminal, six-terminal VSC system

One-phase-to-ground Fault

A nine-cycle one-phase-to-ground fault was applied at the VSC2 ac bus. The results are shown in Figure 5-16. The robust control gains selected gave good dynamic performance to the six-terminal VSC-HVdc system, with the power returning to normal within approximately 200 ms after fault clearance. The ac voltage was brought to 1.05 pu very quickly.

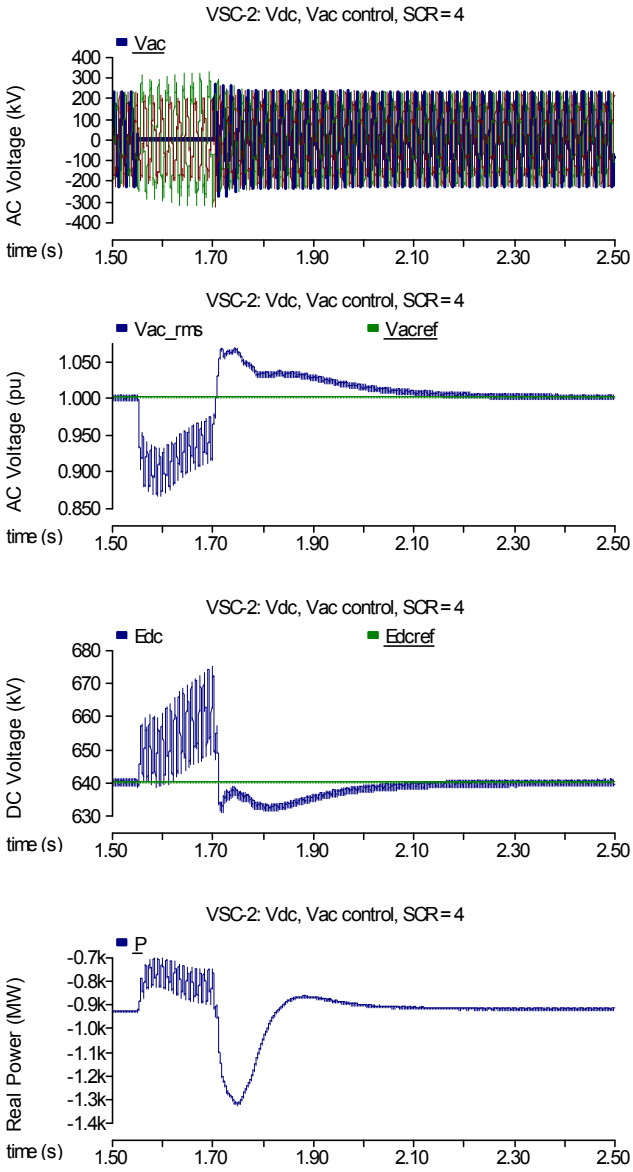


Figure 5-16: One-phase-to-ground fault at VSC2 ac bus terminal, six-terminal VSC system

5.3.4.3 AC System SCR Changes

If the ac system operates at different operating conditions, the equivalent impedance of the ac source the converter is connected to changes. This is equivalent to the ac system SCR change. The results of changing the dc voltage controlling converter VSC2 connected ac system SCR from 4 to 2 at 1.55 s and changing it back to 4 at 2.05 s, are shown in Figure 5-17. The robust control gains selected gave good dynamic performance

when the ac system operating condition changed. The dc voltage returned to the set-point within 200 ms when the SCR changed from 4 to 2 and within 100 ms when the SCR changed from 2 to 4.

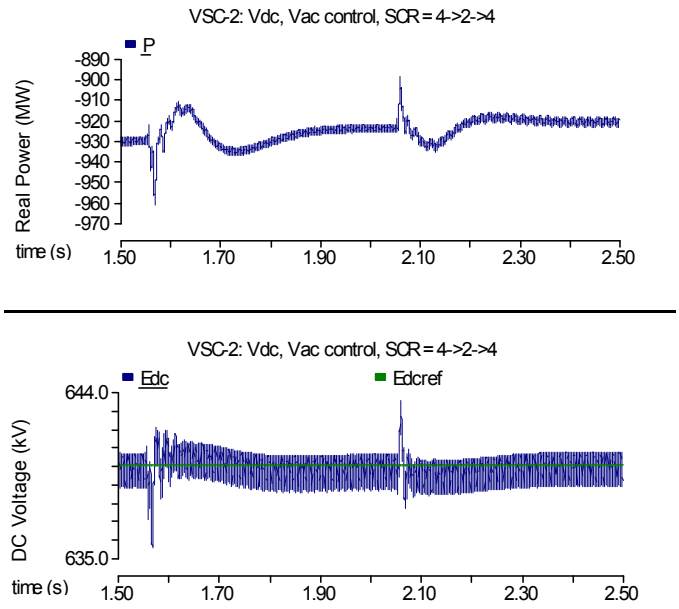


Figure 5-17: SCR change at VSC2 ac bus terminal, six-terminal VSC system

5.4 Why the Single Converter Relaxation Method Works

In order to prove that optimization of one converter does not affect the converter that has been already optimized, the two-terminal system in Step B was evaluated. Figure 5-18 shows the changing of the objective functions as the optimization proceeds when the VSC2 (under control gains optimization) was connected to an SCR = 1.8 ac system. The curves *Obj_VSC1* and *Obj_VSC2* are the objective functions of VSC1 and VSC2 obtained from equations 5-1 and 5-2, respectively. The curves were plotted as a function of the sequence number of the optimization run as the optimization process proceeded. The curves show the objective functions for VSC2 approached the minimum during the

optimization runs. However, the objective functions for VSC1 kept close to constant at around 2.8.

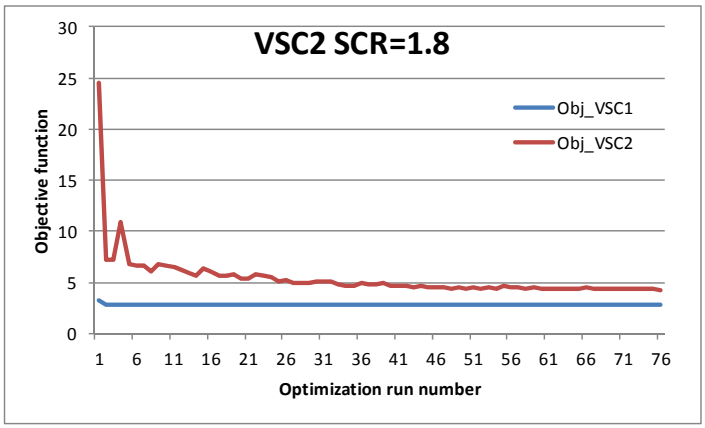


Figure 5-18: Objective function vs. optimization run number

The simulation evaluation confirms that the single converter relaxation method proposed in this research can be used for multi-terminal VSC-HVdc applications. Because of the independent control of the VSC system, whenever the dc voltage can be controlled the controller gains of VSCs in the dc grid can be individually optimized.

5.5 Summary and Comparison of the Two Optimization Methods

The single converter relaxation method for multi-terminal VSC-HVdc system control gains selection allows the optimization variables and the computational time to be minimal. The overall optimization process, including the ensuring of robustness to SCR variation, was discussed in this chapter. The coordination and interaction of control parameters of a multi-terminal VSC were discussed.

Several observations and recommendations are listed below:

- A one-terminal system can be used for real power control gains optimization.

- A two-terminal system can be used for dc voltage control gains optimization.
- Optimization can be achieved using a robust optimization procedure in which a single set of control gains captures the performance over the full range of SCRs. Alternatively; an engineering-judgment-based approach can be used in which the optimized gains for a specific SCR close to the lowest SCR in the range are used for all SCRs. This is generally easier to use than the robust optimization method and results in performance close to the fully-optimized system.
- The selected dc voltage control gains are sensitive to cable length if the connected ac system is relatively weak. However, they are not sensitive to cable length change if the connected ac system is relatively strong. Hence, the dc voltage control should be located at the VSC connected the relatively strong ac system.
- The longest cable length that dc power will transfer in the dc grid should be chosen for the dc voltage control gains optimization process.

Because of the characteristics of the independent control of each converter for multi-terminal converters, the interactions between the control gains and the impedance between the converters are very minimal. If the dc voltage of the dc grid can be maintained, each converter in the VSC-HVdc grid can be viewed as a dc voltage source. Hence, the control gains selection can be optimized individually.

The proposed relaxation optimization method detailed in Chapter 4 limits the optimized control variables to one converter. When optimizing the converter control gains, the objective function is evaluated by the whole system performance. This method works well, but the drawback is the optimization process is very slow, even with averaged valve

models. The single converter relaxation method detailed in Chapter 5 works very well for control gains design and is the most efficient way to design the optimal control gain in a multi-terminal VSC-HVdc system. Hence, this method is recommended for VSC dc grid applications.

Chapter 6: Gain Scheduling Approach to Optimal Gains for DC Grid Converters

6.1 Introduction

Chapter 5 showed that the optimal control gains of the converter are very dependent on the SCR of the ac system to which the converter is connected. Two methods of selecting the control gains can be utilized. One method, which was discussed in Chapter 5, is to select a single set of control gains that will work for all SCRs; however, this may result in sub-optimal performance if the SCR changes to a higher value. The other method is to estimate the ac system's SCR and select gains using a lookup table. This chapter discusses estimation methods that would be useful for this approach. In this approach, the SCR of the network is estimated and the gains are changed so that they are optimal for that setting; therefore, it is not necessary to work with gains optimized for just a single SCR, which would be sub-optimal for other SCRs. In the sections that follow, SCR estimation using monitored breaker status information and using the monitored converter bus voltage and current information are introduced.

6.2 The Motivation for using Monitored Information to Estimate the SCR

A PMU (a synchrophasor) measures the phase and magnitude of voltage or current waveforms on an electricity grid using a common time source for synchronization. Time

synchronization allows synchronized real-time measurements of multiple remote measurement points on the grid. PMUs measure voltages and currents at diverse locations on a power grid and produce accurately time-stamped voltage and current phasors. For 60 Hz systems, PMUs must deliver between 10 and 30 synchronous reports per second, depending on the application. Phasor data concentrators (PDCs) collect the information from the PMUs. The PDCs correlate the data and control and monitor the PMUs. A supervisory control and data acquisition (SCADA) system at the central control facility presents system-wide data on all generators and substations in the system every two to ten seconds. Such a network is used in wide area measurement systems (WAMS). The first, used by the Bonneville Power Administration, began operating in 2000 [77].

Calculating the Thévenin impedance is a simple circuit analysis exercise as long as all the relevant information regarding the power network is known (from a WAMS system or from another method). However, a SCADA system requires seconds to update the system information, and during this time the power network may experience unstable operations and may not be able to return to a steady state if the proper actions are not taken.

Hence, the monitored information should be used to estimate the SCR, and from the SCR the network changes can be reflected quickly and the proper actions can be taken in a more timely fashion. The SCR could be determined by off-line studies in which information regarding the status of breakers on various lines is used to consult a table that gives an estimate of the SCR. This could not be delegated to a SCADA system because the response times of SCADA are too slow (in the range of 2 to 10 s). In order to do an on-line change of the control gains based on the SCR information, a fast generation and breaker status monitoring system should be available. An alternative to using SCADA

status of breakers is to use a probing signal to directly measure the Thévenin impedance. Both methods are considered in next section.

6.3 SCR Estimation

AC system strength will vary depending on the system operating conditions. As in the application to LCC, the SCR and ESCR concepts have been used for VSC-HVdc in this thesis. However, as the filters (if any) are very small (low Mvar) for the VSC application the SCR and ESCR are essentially the same; hence, only the SCR has been used in discussions of VSC converters in this thesis. As discussed in Chapter 3, the SCR and ESCR are only determined by the Thévenin impedance Z_s, therefore, the problem of finding the system strength can be solved by calculating the Thévenin impedance at the converter bus.

6.3.1 SCR Estimation Off-line using Monitored Breaker Status Information

Most utilities maintain load flow stability program data (e.g., in the format used by the popular Siemens/PTI stability modeling tool PSS/E). This information can be used to estimate the SCR of the larger ac network by the procedure discussed below. SCR values could be tabulated for various key operating configurations corresponding to the statuses of generators and breakers in the region surrounding the converter. These statuses could be determined by monitoring and reporting using high-speed communication links. Hence, using a table look-up procedure, the reported breaker status data could be used to report the SCR value. As in Chapter 5, the optimal parameters for each SCR were calculated. Hence, from the reported SCR values the appropriate parameter set could be

switched in, an approach known as gain scheduling [76]. The procedure below shows how the SCR can be calculated for a given system configuration.

Once the SCR is known, the ac network can be fitted with a simple Thévenin equivalent. Note that in this approach it is assumed that the converter buses are sufficiently electrically distant that any direct ac connections can be ignored (i.e., ac connections between converters).

The relationship between network bus (node) voltages and currents may be represented by node equations. The effect of generators, nonlinear loads, and other devices (i.e., dynamic reactive compensators and HVdc converters) connected to the network nodes are reflected in the node current. The network equation in terms of the node admittance matrix can be written as follows:

$$\begin{bmatrix} Y_{11} & Y_{12} & \cdots & Y_{1n} \\ Y_{21} & Y_{22} & \cdots & Y_{2n} \\ \cdots & & & \\ Y_{n1} & Y_{n2} & \cdots & Y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \cdots \\ V_n \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \\ \cdots \\ I_n \end{bmatrix} \qquad 6\text{-}1$$

Assuming that the power system has n buses, m generators, k loads, and that the HVdc is connected to bus number n. The diagram of the system is shown in Figure 6.1. The relationship of node voltage and current at the boundary of the circle is represented by the (network) equation 6-1.

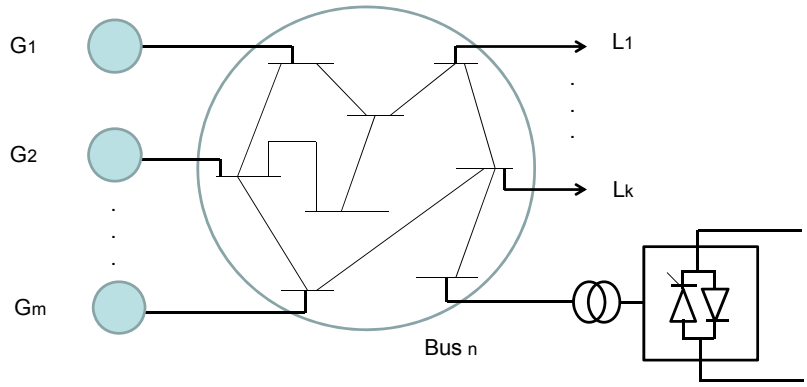


Figure 6.1: Converter connected to an n bus ac system

In per-unit terms, the SCR at bus *n* is the reciprocal of the impedance of the network observed from bus *n*. When SCR is calculated, it is commonly accepted that a generator is treated as a voltage source behind the transient impedance X_d' [72]. The loads can either be treated as impedance embedded in the network or as current sources representing nonlinear loads. The circuit diagram is changed to the one in Figure 6.2 based on these assumptions.

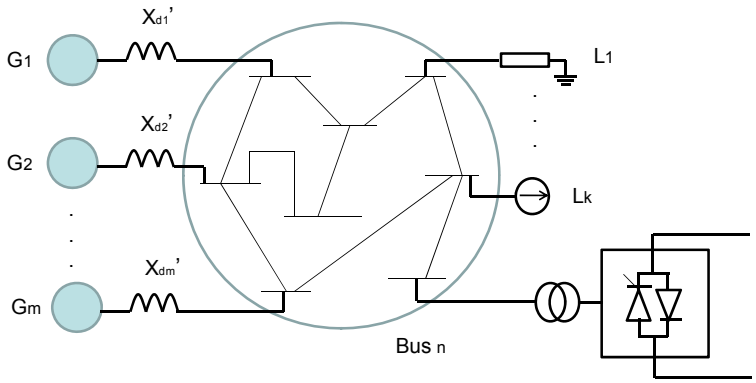


Figure 6.2: Circuit diagram of a converter connected to an n bus ac system

In order to calculate the Thévenin equivalent impedance at bus *n*, the voltage sources are treated as short circuit, and current sources are treated as open circuit, as in Figure 6.3. If a unit current source at bus *n* is applied, the voltage at that bus V_n is the Thévenin equivalent impedance.

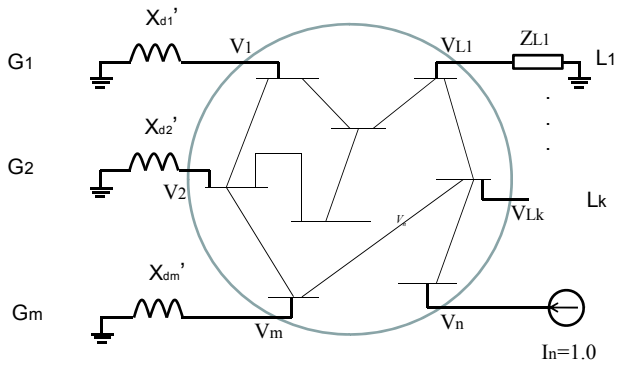


Figure 6.3: Thévenin equivalent impedance at the converter bus

The above computation can be described by the following equation:

$$\begin{bmatrix} \left(Y_{11}+\frac{1}{X'_{d1}}\right) & Y_{12} & \cdots & Y_{1m} & Y_{1(m+1)} & \cdots & Y_{1(m+k)} & \cdots & Y_{1n} \\ Y_{21} & \left(Y_{22}+\frac{1}{X'_{d2}}\right) & \cdots & Y_{2m} & Y_{2(m+1)} & \cdots & Y_{2(m+k)} & \cdots & Y_{2n} \\ \cdots & & & & & & & & \\ Y_{m1} & Y_{m2} & \cdots & \left(Y_{mm}+\frac{1}{X'_{dm}}\right) & Y_{m(m+1)} & \cdots & Y_{m(m+k)} & \cdots & Y_{mn} \\ Y_{(m+1)1} & Y_{(m+1)2} & \cdots & Y_{(m+1)m} & \left(Y_{(m+1)(m+1)}+\frac{1}{Z_{L(m+1)}}\right) & \cdots & Y_{(m+1)(m+k)} & \cdots & Y_{(m+1)n} \\ \cdots & & & & & & & & \\ Y_{(n-1)1} & Y_{(n-1)2} & \cdots & Y_{(n-1)m} & Y_{(n-1)(m+1)} & \cdots & Y_{(n-1)(m+k)} & \cdots & Y_{(n-1)n} \\ Y_{n1} & Y_{n2} & \cdots & Y_{nm} & Y_{n(m+1)} & \cdots & Y_{n(m+k)} & \cdots & Y_{nn} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ \cdots \\ V_{n-1} \\ V_n \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ \cdots \\ 0 \\ I_n \end{bmatrix} \quad 6\text{-}2$$

Denote the admittance matrix, the first matrix on the left in equation 6-2, as the extended admittance matrix, Y_{ext}. The Thévenin equivalent impedance can be solved by inversion of this matrix.

$$\begin{bmatrix} V_1 \\ V_2 \\ \cdots \\ V_{n-1} \\ V_n \end{bmatrix} = Y_{ext}^{-1} \begin{bmatrix} 0 \\ 0 \\ \cdots \\ 0 \\ I_n \end{bmatrix} \quad 6\text{-}3$$

Then the Thévenin equivalent impedance at the converter bus (bus n) is:

$$Z_{eq} = V_n = \left(Y_{ext}^{-1}\right)_{nn} \quad 6\text{-}4$$

And the SCR at the converter bus (bus *n*) is:

$$SCR = \frac{1}{Z_{eq}} = \frac{1}{\left(Y_{ext}^{-1}\right)_{nn}} \qquad 6\text{-}5$$

6.3.2 SCR Estimation On-line using Converter Bus Monitored Information

The closed-loop estimation method developed in this section uses the local converter ac bus voltage and current information to estimate the ac system SCR [77]. For example, a probing signal is ordered every few minutes at the converter bus by introducing a small step change in the dc current, which also changes the ac voltage and ac current entering the ac network. The algorithm below calculates the SCR based on the change of the voltage and current information at the converter bus on the application of this probing signal.

As we discussed in the previous section, estimation of SCR requires estimation of the Thévenin impedance. In order to understand the problem more clearly, let us analyze the Thévenin equivalent circuits with a phasor diagram. Assuming that the larger ac network can be approximated by a linear circuit, it can always be converted to a Thévenin equivalent circuit as shown in Figure 6.4, which preserves all the external characteristics of the original network. In general, the network would have a frequency-dependent Thévenin equivalent, but if it is evaluated only at fundamental frequency (i.e., 60 Hz as is the case here), it would provide the correct system response at 60 Hz.

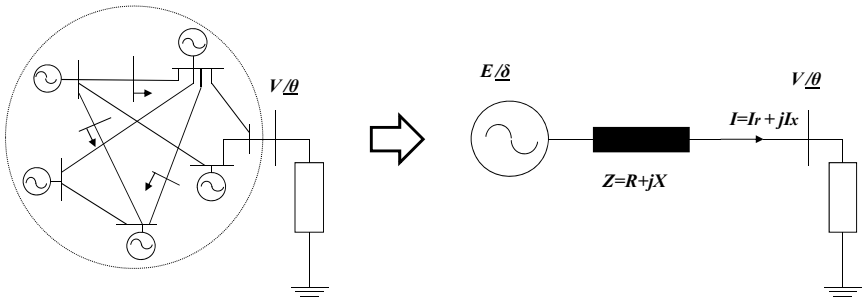


Figure 6.4 Thévenin equivalent circuit

In Figure 6.4, the following equation can be obtained directly according to Kirchhoff Voltage Law (KVL):

$$E = V + I \cdot Z \tag{6-6}$$

If we draw the phasor diagram of circuit and project the vector I and vector E on vector V as in Figure 6.5,

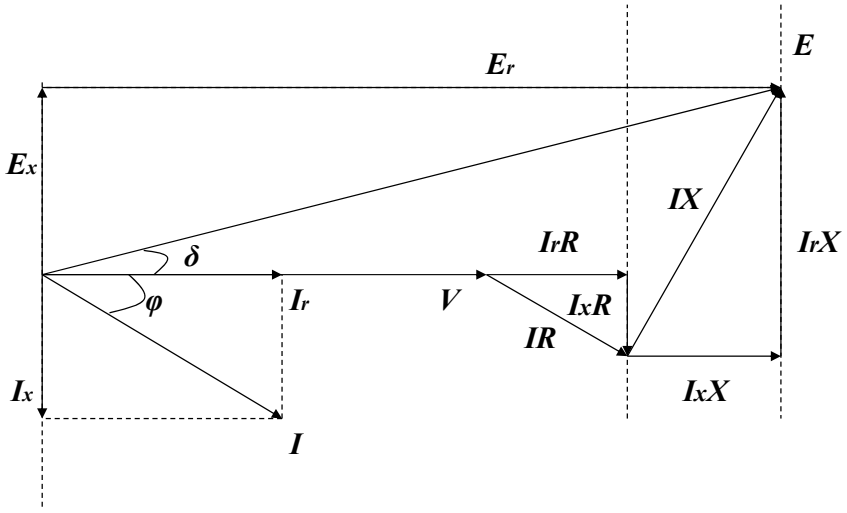


Figure 6.5 Phasor diagram of the Thévenin equivalent circuit

we will have: $$E = E_r + jE_x \tag{6-7}$$

and $$I = I_r - jI_x \tag{6-8}$$

equation 6-6 can be expanded as:

$$E_r + jE_x = V + (I_r - jI_x)\cdot(R + jX) \quad 6\text{-}9$$

If we separate the real and imaginary parts of equation 6-9, we can have two equations:

$$E_r = V + I_r R + I_x X \quad 6\text{-}10$$

$$E_x = I_r X - I_x R \quad 6\text{-}11$$

In these two equations, the ac busbar voltage V is used as the angle reference. V, I_x, and I_r can be measured at the converter ac bus terminal. There are 4 unknowns in the two equations, which are E_r, E_x, R and X. In order to solve the four unknowns, we require two additional equations. This can be done by including equations 6-10 and 6-11 at another measurement point afforded by the perturbation caused by the probing signal as shown in equations 6-12 and 6-13. It appears that there are 2 extra unknowns E_{x2} and E_{r2}. But if E is assumed constant, we can solve for the four unknowns.

$$E_{r2} = V_2 + I_{r2} R + I_{x2} X \quad 6\text{-}12$$

$$E_{x2} = I_{r2} X - I_{x2} R \quad 6\text{-}13$$

Although the E remains constant as a vector in the space, i.e., $|E_{x2}+jE_{r2}|=|E_x+jE_r|=|E|$, since the angle reference of the two measuring points V and V_2 are different, in order to solve the 4 unknowns, we can rotate the two frames by the angle difference between V and V_2. Figure 6.6 shows the phasor diagram of two measuring points with the constant E.

Assuming the angle difference between V and V_2 to be,

$$\Delta\theta = angle(V_2) - angle(V) \quad 6\text{-}14$$

the rotated V_2 and I_2 refer to the first measuring point V should be as following:

$$V_2{}' = \begin{bmatrix} V'_{r2} \\ V'_{x2} \end{bmatrix} = R(\Delta\theta) \begin{bmatrix} |V_2| \\ 0 \end{bmatrix} \quad 6\text{-}15$$

$$I_2{}' = \begin{bmatrix} I'_{r2} \\ I'_{x2} \end{bmatrix} = R(\Delta\theta) \begin{bmatrix} I_{r2} \\ I_{x2} \end{bmatrix} \quad 6\text{-}16$$

in which $$R(\Delta\theta) = \begin{bmatrix} \cos(\Delta\theta) & \sin(-\Delta\theta) \\ \sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix}$$

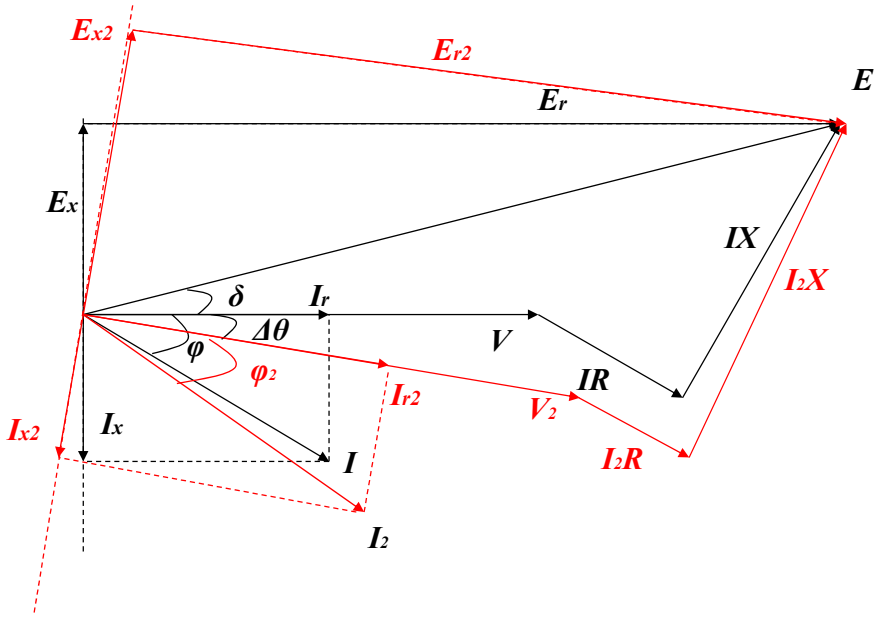


Figure 6.6 Phasor diagram of two measuring points with constant E

After the rotation the equations 6-12 and 6-13 become:

$$E_{r2} = E_r = V'_{r2} + I'_{r2}R + I'_{x2}X \quad 6\text{-}17$$

$$E_{x2} = E_x = V'_{x2} + I'_{r2}X - I'_{x2}R \quad 6\text{-}18$$

Re-arrange equations 6-10, 6-11, 6-17 and 6-18, we obtain the equation 6-19, in which the four unknowns E_r, E_x, R and X can be solved.

$$\begin{bmatrix} 1.0 & 0.0 & -I_r & -I_x \\ 0.0 & 1.0 & I_x & -I_r \\ 1.0 & 0.0 & -I'_{r2} & -I'_{x2} \\ 0.0 & 1.0 & I'_{x2} & -I'_{r2} \end{bmatrix} \begin{bmatrix} E_r \\ E_x \\ R \\ X \end{bmatrix} = \begin{bmatrix} V \\ 0.0 \\ V'_{r2} \\ V'_{x2} \end{bmatrix} \quad \text{6-19}$$

There are three basic assumptions in the algorithm described above, which is for the two measuring points:

(1) The equivalent voltage source of the Thévenin equivalent circuit is constant;

(2) The equivalent impedance of the Thévenin equivalent circuit is constant;

(3) The current measurements are different.

(1) and (2) assure there are 4 unknowns in the 4 equations while (3) assures the matrix in equation 6-19 is non-singular so that the equations are solvable.

In the real power systems (1) and (2) will not be satisfied during any disturbance. However, when the disturbance is settled down to steady state, the Thévenin equivalent circuit will be solvable again. (3) is not hard to satisfied when the probing signal is added which leads to different current measurements.

By using the above procedure, the SCR of ac system can be effectively estimated. The results of the estimation can be used as a base to adjust the control of VSC HVdc systems.

6.4 On-line Gain Scheduling EMT Simulation

Assuming that an SCR change can be determined, perhaps by using the proposed breaker monitoring method discussed above, this example demonstrates that the optimal gains of Table 5.1 can be selected so that the system uses the best gains for the operating

condition present. The two-terminal VSC system shown in Figure 5-6 was used and redrawn to the configuration in Figure 6.7. The system is a ±320 kV two-terminal VSC-HVdc system rated at 500 MW. The VSC with dc voltage control is in inverter operation and connected to an SCR = 2 ac system. The VSC with real power control is in rectifier operation at full rated power (500 MW) and connects to an SCR = 3 ac system. The ac network connecting the real power controlling converter is shown in Figure 6.8; the lines L1, L2, and L3 will be switched on and off during the simulation, thereby changing the SCR. The ac system SCR is, in consequence, changed from *3* (all lines switched on) to *1.6* (L1, L2, and L3 switched off) to *1.8* (L1 switched on) to *2.0* (L2 switched on) and then back to *3* (L3 switched on) in 3 seconds, as shown in Figure 6.8. The corresponding SCRs are calculated off-line based on the breaker status and the optimized control gains used are available in a look-up table. If the SCR lies between two table entries, the gains corresponding to the lower (more critical) SCR are used. For example, as the tabulated values are only for SCRs of 2 and 3, the gains corresponding to SCR = 2 would be used when the actual SCR is 2.5. In this study, the optimized control gains sets for different SCRs are from Table 5.1, as described in Chapter 5.

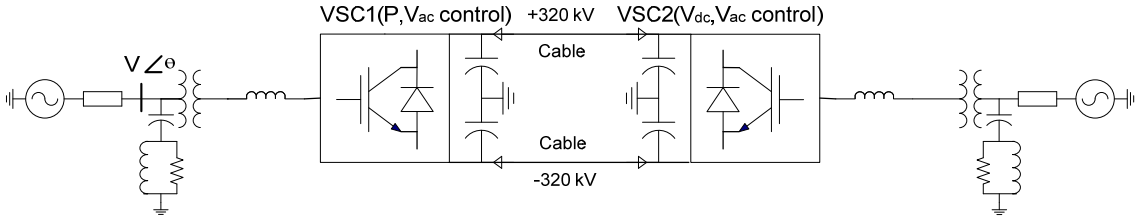


Figure 6.7: Two-terminal VSC-HVdc grid

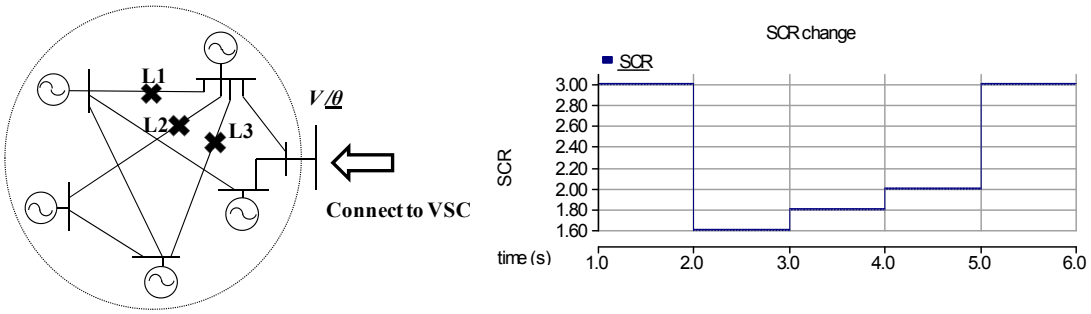


Figure 6.8: VSC1 connected ac network and SCR changes

In the first study, the control gains scheduling was set to activate at the instant when the SCR is changed, in which the fast generation and breaker status monitor system is available. However, in reality, even though the fast monitor system is available, a slight time delay is required to detect the SCR change. In the second study, the control gains scheduling was set to activate at various delay times as the SCR is changed. The results of a *200 ms* delay were reported in the thesis. Both of the studies discussed in this chapter were compared with the robust control gains setting method and the results are reported below.

The angular reference signal θ (shown as *theta* in the plots) generated by the PLL tracks the voltage V_t of the PCC and is shown in the plots. The phase angle (shown as *th* in the plots) of the infinite bus (Thévenin source) voltage of the E_s is also plotted. In the simulation, *th* is a known quantity and does not require measurement. The phase angle difference between the angles of V_t and of E_s, (i.e., *theta – th*, shown as *Delta* in the plots) is a measure of how quickly the system settles down into a stable steady state as it directly affects the active power transfer between V_t and E_s terminals.

As indicated in Chapter 3, the phase angle difference between the voltage E_s of the infinite bus (Thévenin source) and the voltage V_t of the PCC is a measure of how quickly

the system settles down into a stable steady state as it directly affects the active power transfer. Hence, the real power *P* and the phase angle difference *Delta* are shown in the figures below. The objective function measured is calculated using equation 5-1.

Base Case Operation with No Gain Change:

In Chapter 5, the robust approach, in which there is a single, unchanging set of gains for all SCRs, was presented. The robust control gains chosen are the gains as reported in Table 5.1. Figure 6.9 shows operation with a given set of gains that are not changed with the SCR. However, these gains correspond to the optimized gains for SCR = 3, and hence are not robust. The study results show the system goes unstable after the SCR changes.

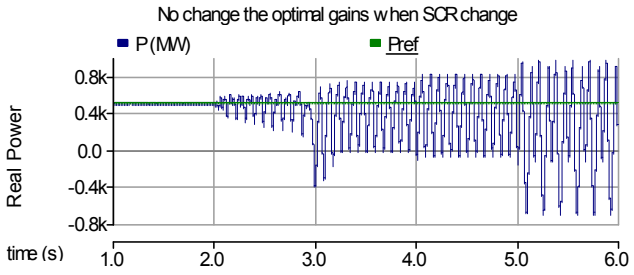


Figure 6.9: Performance with gains optimized for a specific SCR = 3

Operation with Gain Scheduling:

Unlike the above approach, here gain scheduling is conducted to match the gains to the actual SCR. For the first study, a *0 ms* delay was assumed between breaker opening and the change of gains, and the optimal control gains were set from the preset look-up table. Figure 6.10 shows that the system had good performance and that the calculated objective function was 2.861. However, for the second study, when the optimal gains were set *200 ms* after the SCR has been changed, the system was stable, as shown in Figure 6.11, but the calculated objective function was higher at 3.724. The length of delay time plays

a very important role in the system performance. If the delay time is too long, the system will go to unstable, as indicated in Figure 6.9, and the gains are not changed.

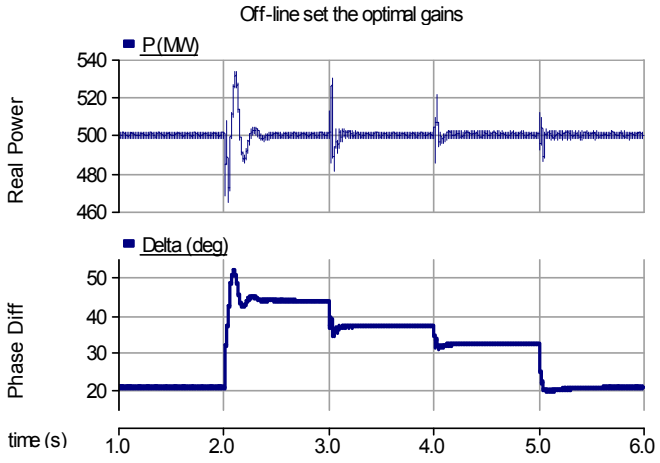


Figure 6.10: Control gains setting with no time delay

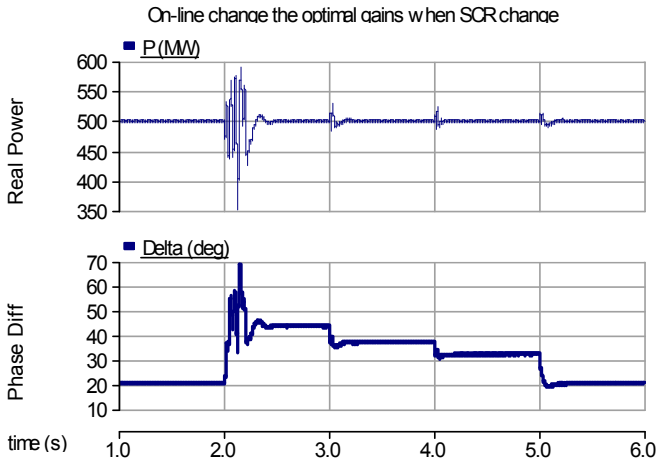


Figure 6.11: Control gains setting with a 0.2 s time delay

Operation with Robust Gain:

Figure 6.12 shows the results when robust control gains are used, i.e., the control gains are not changed during the system SCR changes. The system performance is satisfied and the calculated objective function is 2.578.

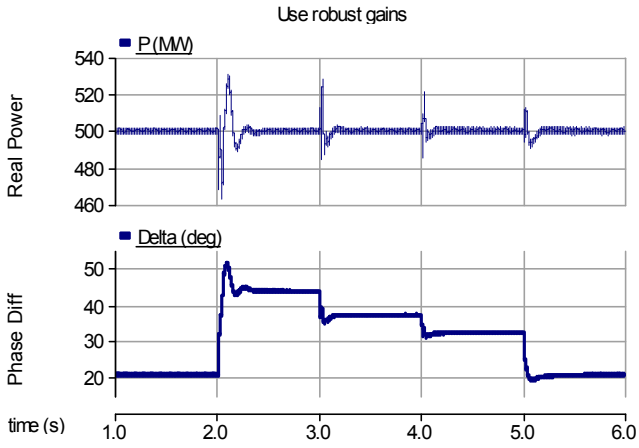


Figure 6.12: Performance with robust gains

The simulation results show that with delays included the on-line gain scheduling method (Figure 6.11) has a somewhat poorer performance compared to the robust control gains setting (Figure 6.12). Even with no delay (Figure 6.10), the robust gains still give a marginally better result. This unexpected behaviour can be attributed to the fact that the sudden changes of gains in the gain scheduling procedure introduce a disturbance to the system, which is particularly onerous for the weaker SCR systems. Hence, even though the optimal control gains can be scheduled on-line, it is suggested that the control gains that have the best overall performance on a range of operating points, the robust control gains, should be used.

6.5 Summary

This chapter introduced the off-line SCR estimation based on the pre-set switching status and on-line SCR estimation based on the measured information at converter busbar. Based on the calculation of the SCR, the control gains of the VSC HVdc system can be adjusted on-line to achieve optimal performance. However, when delays in changing the

gain are included, the on-line gain scheduling performance becomes poorer. In contrast, the fixed robust control gains give the system improved performance over the entire range of operating conditions, and are therefore recommended.

Chapter 7: Conclusions and Future Work

This thesis investigated power transmission limitations imposed on a converter by ac system strength and by ac system impedance characteristics. The finite converter rating limit and the reactive power requirement of VSC transmission were determined. A small signal model of the converter system and its controls were developed and the impact of PLL parameters on the transient and steady-state behavior of a VSC is investigated. Application of optimization tools to coordinate the controls of multiple converters in a dc grid were investigated, and the methods and procedures for setting control gains for a multi-terminal VSC-HVdc system were developed.

7.1 The Main Contributions of this Thesis

The main contributions of this thesis are the following:

- The operation of a converter is greatly affected by the angle of the ac system's impedance at the fundamental frequency. As the SCR becomes more resistive, the minimum ac short circuit ratio (SCR) required at the rectifier side increases from that required for ideally inductive ac impedance, but it decreases at the inverter side. The finite MVA limit of the VSC imposes a further limitation on power transfer, requiring an increase in the value of the minimum SCR. This limitation can be mitigated if additional reactive power support is provided at the point-common-connection (PCC).

- The gains of the phase locked loop (PLL) used for angle reference generation must be reduced for lower SCR operating conditions (weak ac systems). The gains of the VSC

inner and outer PI controllers have limited effects on system transient performance compared to the gains of the PLL.

- A state-space VSC model was developed and validated with the EMT model. However, the large signal transient cannot be analysed by the linearized model. Electromagnetic transient simulation must be used for selecting the final controller gains.

- Control gains optimization in a VSC-HVdc grid can be achieved by using a robust optimization procedure in which a single objective function (OF) captures the performance over the full range of SCRs. However, with the whole dc grid represented, this generally requires immense computing resources and is sometimes even beyond the handling capability of optimization algorithms. An approach called the "relaxation optimization method" was introduced in which the optimizations of different converters are conducted one at a time and, hence, it limits the optimized control variables to one converter.

- One of the key conclusions of this thesis is that a single converter could be optimized by itself in a VSC dc grid and then added to the grid. The interactions between the control gains and the impedance between the converters are very minimal if the dc voltage of the dc grid can be maintained. Each converter in the VSC-HVdc grid can be viewed as though it is connected to a fixed dc voltage source. Hence, the control gains selection can be optimized individually. This is much more practical and manageable in terms of required computing resources than the approach discussed above.

- For a power-control converter, the single converter could be connected to an ideal dc bus (constant voltage) for optimization. For a voltage control converter, a two-terminal dc system with the voltage controlling converter connected to an optimized power controlling converter via the longest cable length is recommended as the system to be used for gain optimization. This method for multi-terminal VSC-HVdc system control gains selection allows the selection of gains in a more manageable manner (with respect to computer time and resources) than would be the case if simultaneously optimizing all gains in the multi-terminal system was attempted.

- Optimization can be achieved using a robust optimization procedure in which a single set of control gains captures the performance over the full range of SCRs. Alternatively; an engineering-judgment-based approach in which the optimized gains for a specific SCR close to the lowest SCR in the range are used for all SCRs can be used. This is generally easier to do than the robust optimization, and results in performance close to that of the fully-optimized system.

- The selected dc voltage control gains are sensitive to cable length if the connected ac system is relatively weak. However, they are immune to cable length change if the connected ac system is relatively strong. Hence, the dc voltage control should be located at the VSC connected to the relatively strong ac system.

- The longest possible cable length the power will transfer over in the dc grid should be chosen for the dc voltage control gains optimization process.

- By using the monitored breaker status and voltage and current at converter busbar, the SCR can be determined and the gain scheduling approach to obtaining optimal gains

for dc grid converters is possible. However, when delays in changing the gains are included, the on-line gain scheduling performance becomes poorer. In contrast, the fixed robust control gains give the system improved performance over the entire range of operating conditions, and are hence recommended.

7.2 Recommended Future Research

The concepts and methodologies developed in this thesis have great potential for future research regarding dc grids. In this section, several topics that could be researched in the future using this thesis as a base to build on are discussed.

7.2.1 DC Grid Transmission Limitations Imposed by the Multi-infeed AC Systems Characteristics

The VSC transmission limitations imposed by the connected ac system characteristics and impedance angle were studied in this thesis. It was assumed that the ac connections between converters can be ignored. However, for grid integration purposes, more than two terminals of a dc grid will be connected to the same ac system. Therefore, the converter buses may not be sufficiently electrically distant, and the direct ac connections cannot be ignored. The transmission limits of the dc grid could be studied including the influences of the connected ac systems. Possible study areas are the following:

- How the electrical distance between the two ac systems impacts dc grid transmission?
- How do the two electrically close ac systems (one strong and one weak), impact dc grid transmission?

- How do the two electrically close ac systems with different impedance angles impact dc grid transmission?
- How do the two electrically close ac systems with one in rectifier mode and one in inverter mode impact dc grid transmission?
- How to define the transmission limits of the dc grid?
- How to define the transmission limits of parallel ac and dc lines?
- How to define the transmission limits of parallel VSC HVdc and conventional HVdc lines?

7.2.2 PLL Frequency Response Using Time Domain Software

In this thesis it was found that the PLL parameters are very important to the performance of the entire dc grid. It would be interesting to study how to set the PLL parameters of VSC-HVdc terminals connecting ac systems with different SCRs. Linear control system analysis with a Bode plot provides clear information regarding when the control parameters change. However, it is hard to obtain the analytical form of the entire multi-terminal VSC-HVdc systems. It is hoped that it is possible to find the frequency response of the entire system based on EMT simulation. When the excitation is small enough, the response should be linear as well. The relationship between the input and output may be used to produce the Bode plot. It is worth attempting to see if there is a possibility of carrying out linear system analysis based on EMT simulation results.

7.2.3 Relaxation Method on Control Gains Coordination within VSCs

In this thesis, relaxation methods were successfully used to obtain optimal solutions for multi-terminal VSC HVdc systems. It would be interesting to expand the application of relaxation methods to other power system applications.

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