A Transmission Line DC De-Icer Using a Single-Arm Modular Multilevel Converter

By

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Abstract

This thesis studies the operating principles, parameter design, and harmonics performance of an HVDC converter topology: SAMMC (single-arm modular multilevel converter), and develops a DC deicer system using this converter as a rectifier to melt ice on iced conductors. Ice formation on power lines is a common problem in cold climate jurisdictions. It could cause severe danger to power systems since the weight of ice could damage the power line or transmission towers. This thesis develops a portable DC deicer with SAMMC technology to convert AC power into DC power and use DC current to melt ice on the power line efficiently and economically. The SAMMC DC deicer system is firstly validated by EMT simulation models. Then, a scaled-down laboratory prototype is developed to validate the performance of the SAMMC rectifier and the harmonics suppression controller.

Acknowledgements

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Ziming Dong

Dedications

To my families

To my friends

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S. Fan, X. Jiang, L. Shu, P. He, P. Liu and H. Nie, "DC Ice-Melting Model for Elliptic Glaze Iced Conductor," in IEEE Transactions on Power Delivery, vol. 26, no. 4, pp. 2697-2704, Oct. 2011, doi: 10.1109/TPWRD.2011.2156433. ©2011 IEEE

Figure 1.6: Cross section profile for iced conductors.

S. Fan, X. Jiang, L. Shu, P. He, P. Liu and H. Nie, "DC Ice-Melting Model for Elliptic Glaze Iced Conductor," in IEEE Transactions on Power Delivery, vol. 26, no. 4, pp. 2697-2704, Oct. 2011, doi: 10.1109/TPWRD.2011.2156433. ©2011 IEEE

Chapter 1

Introduction

1.1 Background

Long-distance transmission lines are critical assets of electric utilities and form the backbone of electrical power systems. Without a reliable transmission system, the stability and security of power systems are at risk. In jurisdictions with a cold climate, transmission systems are prone to the formation of ice on the lines [1]. Ice formation on a line is a serious threat to its operation, as the weight of the ice can lead to excessive sagging of the line, which in turn may cause it to come into contact with other objects or lead to mechanical breakage of the line or transmission towers [2]. Utilities in Canada have had to deal with the consequences of excessive icing on transmission lines; examples include the massive disruptions that Hydro Quebec faced in 1998 [3] and more recently in Manitoba Hydro's system in October 2019 [4].

Knowing the harmfulness of ice accumulation on a power line, it is clear that developing effective and convenient ice removal methods is of great importance. Utilities adopt various methods for removing ice from transmission lines, including mechanical rolling of the ice, and electrical methods for heating [5]. The latter is preferable as it can melt ice off long segments of a transmission line from a single location before the ice-melter is moved to another place [6]. This method of deicing, i.e., using electric current to create controlled heat in segments

of a transmission line [7] is the focus of this thesis. For electric ice-melting, both AC and DC options may be used [8], of which the latter is considered here. Ice-melting based upon DC currents is preferred because the impedance of power lines' inductance is larger than the impedance of power lines' resistance. If AC current is applied, the power lines will absorb a large reactive power. However, if DC current is applied, the impedance of power lines' inductance is zero, so there will be no reactive power absorbed by the power lines. [9]. The downside of DC deiceris that an AC-DC converter (rectifier) needs to be employed to convert the typically-available AC voltages to a controlled DC voltage.

Compared with other ice-melting methods, DC deicing has significant advantages. Several research studies have been conducted regarding this method. The most typical DC deicing device, which is widely used nowadays, consists of a transformer and a thyristor rectifier (usually 12-pulse rectifier) as shown in Figure 1.1.

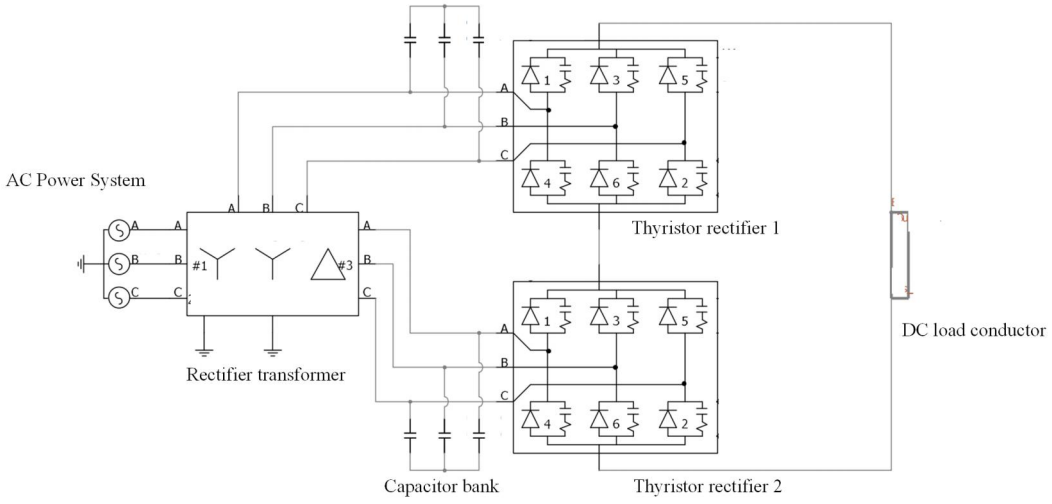

Figure 1.1: Thyristor-based DC deicer.

Limitations can be found in this typical DC deicing device. First of all, a significant amount of reactive power is absorbed by the rectifier, making the MVA-per-MW ratio much higher than unity; therefore, a larger transformer must be used. Secondly, the thyristor-based rectifier generates high current harmonics without a proper filter system; however, it is difficult to make the size of the deicing system compact if filters are included. In conclusion, a

relatively large space is needed to place the thyristor-based rectifier deicer, and the harmonic levels are concerning.

In order to reduce the cost, and increase the flexibility of the ice melting procedure, utilities prefer a portable DC deicer concept. A portable DC deicer is superior to a fixed DC deicer since there is no need to install one deicer at each AC substation; multiple AC stations can share one portable deicer to reduce costs. Also for those small stations that are not equipped with a deicer, the portable deicer can melt ice off their power lines when necessary.

The work process of a portable DC deicer is shown in Figure 1.2. Assume ice formation on power line occurs in the area between Transmission Tower 1 and Transmission Tower 3, and Transmission Tower 1 is connected to a substation. To melt ice with the Portable DC Deicer, the Portable DC Deicer truck should be moved to the substation which is connected with Transmission Tower 1 and obtain AC power from this substation. Before starting ice melting procedure, the transmission lines involved in ice melting procedure should be de-energized by switching off the disconnectors in substations. Two groups of crews are required to conduct the ice melting procedure. The first group should locate at the DC Deicer end substation, and the second group should be located at the end of melting power line.

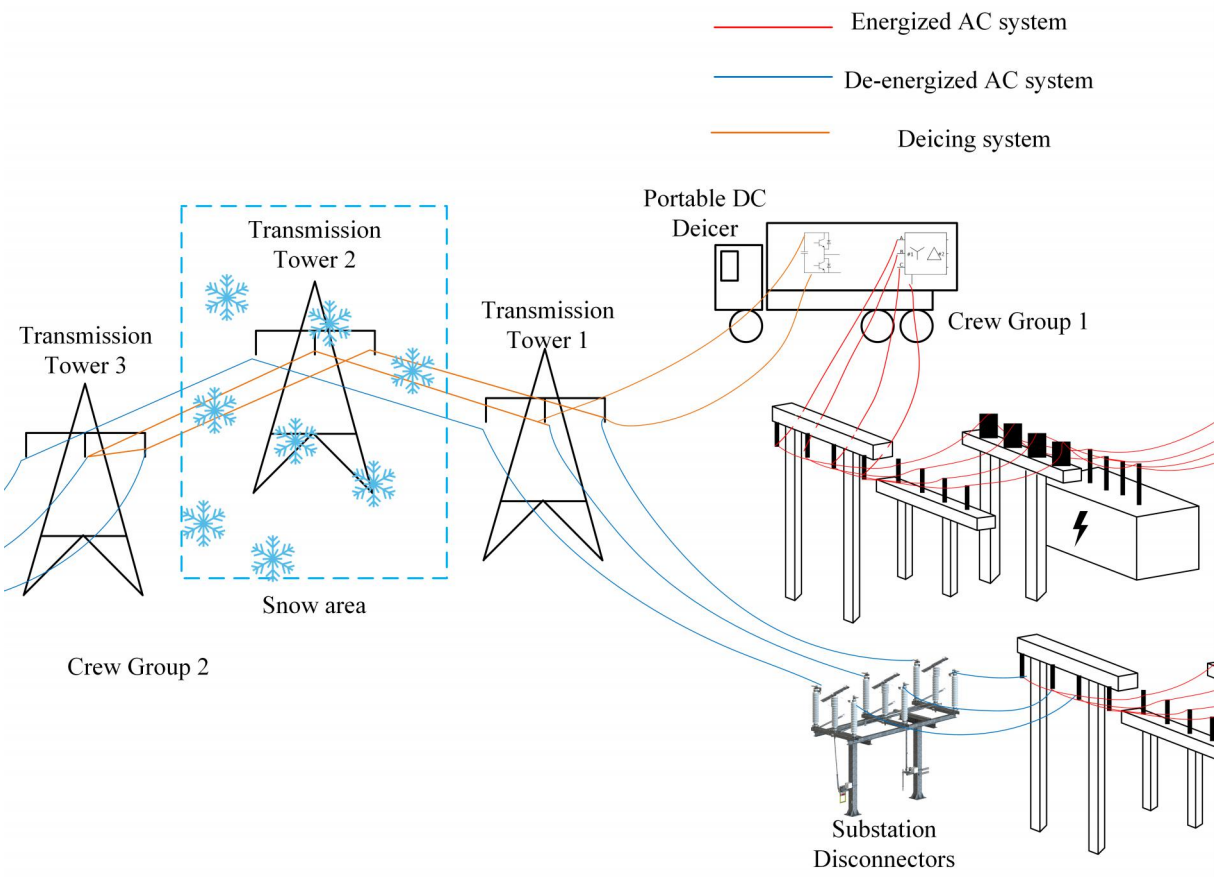

Figure 1.2: Portable DC deicer work process.

However, the design of a portable DC deicer could be challenging. Firstly, the size of the deicer device must be compact enough so that the whole system can be loaded on a vehicle. This requires a small transformer and converter. Secondly, the deicer must be suitable for melting different conductors under different conditions. This requires that the DC output voltage of the device must be highly controllable.

While it has been clearly stated that the performance of a thyristor-based rectifier cannot satisfy the requirements for a portable DC-deicer, to address this issue, researchers and utilities are interested in introducing fully controlled voltage-source converters (VSCs) in ice melting applications. Using VSCs, the problem of harmonics and reactive power consumption can be essentially remedied. Among different VSC topologies, a modular multilevel converter (MMC) is attractive. Compared with two-level or three-level VSC designs, MMCs have

several advantages, including higher voltage rating, no need for filter systems, lower switching losses, and better harmonic performance. To further reduce the size of the deicing system, a new MMC topology, namely single-arm modular multilevel converter (SAMMC), is selected in this thesis to be the rectifier of the DC deicer. The schematic diagram of SAMMC based DC deicer is shown in Figure 1.3.

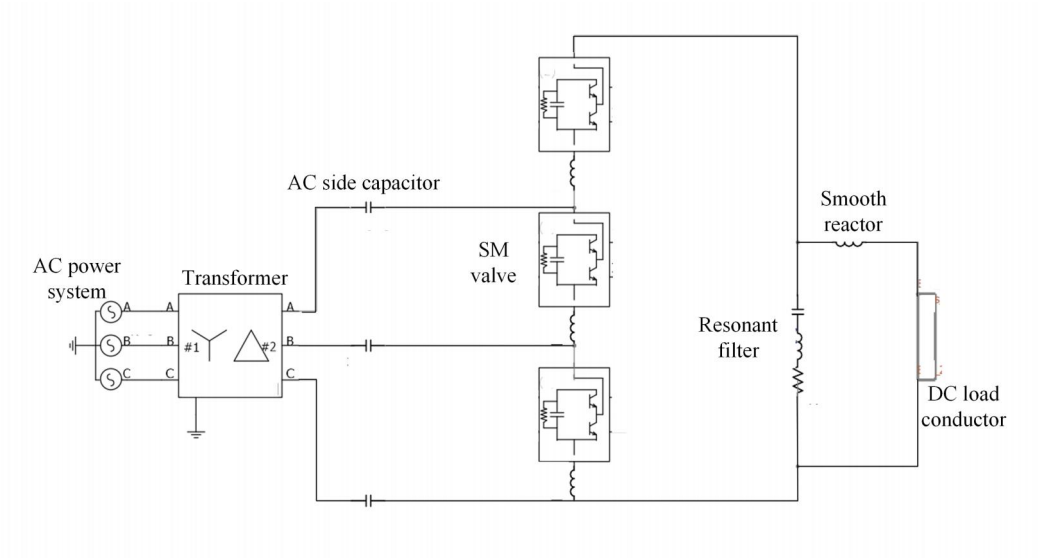

Figure 1.3: SAMMC DC deicer.

Similar to conventional MMCs, a SAMMC also uses a modular approach based upon half-bridge submodules (HB-SM); however, the three valves form a single string on the DC side with three tapping points to connect to an AC system. The primary benefit of a SAMMC is its relatively small size. Although some peripheral equipment, such as three AC-side capacitors and a resonant filter, are added to this new topology, the number of SM valves is reduced from six to three. This topology is originally intended for tapping small amounts of power off a DC line to energize small loads, thus operating as an inverter. In the proposed research it is used as a rectifier, i.e., to connect an AC source to a segmented line through which controlled amounts of DC current will flow. By introducing SAMMC, the size of both the rectifier transformer and the rectifier itself are made smaller.

As discussed before, the second requirement for a mobile DC deicer is that one device

should work with different conductors under different conditions. Although the design in Figure 1.3 can produce reasonably good result in some scenarios, when conductors with small resistance (typically 2Ω to 10Ω) are to be heated, the rectifier will absorb a large amount of reactive power. If this problem is solved, the reactive power absorbed from power system will be greatly reduced, and a smaller transformer can be used. In Figure 1.4, a DC-DC buck converter is proposed to be added to step down the voltage from rectifier's DC side to DC voltage on the conductor side.

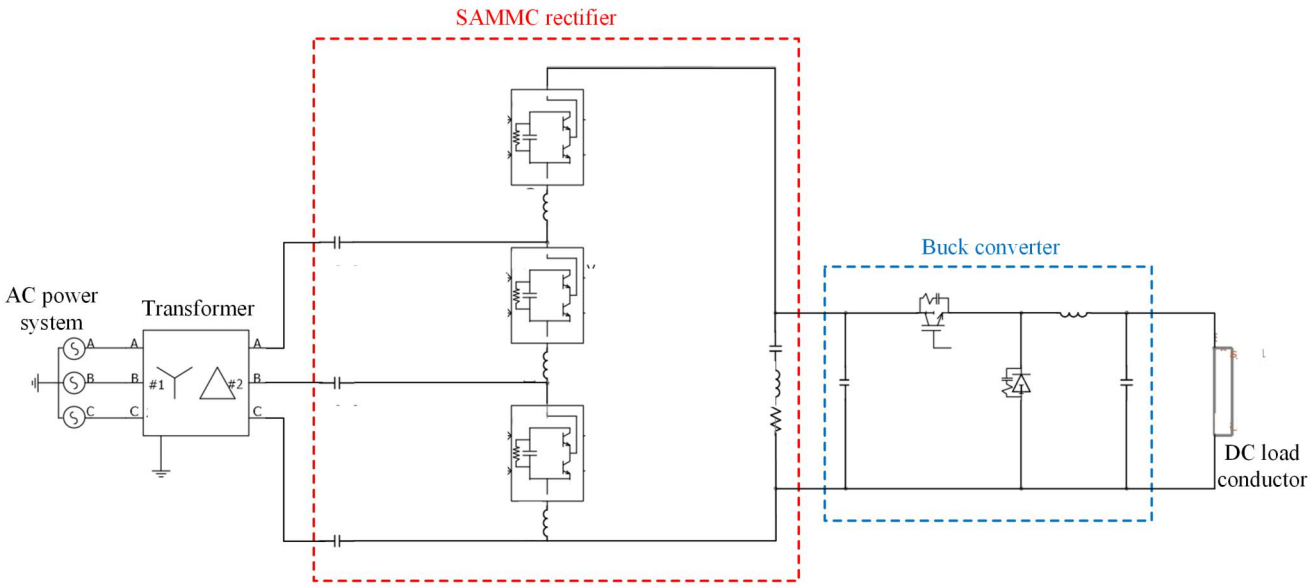

Figure 1.4: SAMMC DC deicer with a step-down DC-DC converter.

In short, introducing SAMMC as the rectifier makes it possible to design a compact, low-harmonic, and highly controllable DC-deicer. This thesis discusses the two designs (with and without the step-down DC-DC converter) and compares their merits and drawbacks.

1.2 Literature Review

This section will go through previous studies on several topics related to the design of DC deicers. The formation and melting process of ice on power conductors, characteristics of

different AC-DC converter types, and the control and principle of DC buck converter.

1.2.1 Ice formation and ice melting

To better understand the ice melting process and select a proper DC current rating for the DC deicer and plan the melting time, basic knowledge about ice formation and ice melting models will be first introduced.

For the ice formation on a power line, how frozen water accumulates on the conductor and what factors affect the shape and size of the ice layer are the points of interest in this thesis. Hydro-Quebec and other institutions have conducted several studies and experiments on conductor icing. A number of valuable models and conclusions are recorded in [10]. Generally there are two types of ice accretion on power conductors, namely precipitation icing and in-cloud icing. Precipitation icing refers to the conductor ice caused by glaze, wet snow, or dry snow. While dry snow can be easily removed, glaze (freezing rain) and wet snow are the main causes of iced conductors. In-cloud icing refers to conductor ice caused by super-cooled droplets within clouds.

Glaze/wet snow or super-cooled droplets can be modeled as a sticky droplet of liquid-to-frozen water mixing, which has a temperature around 0°C. The surface temperature of conductors is far below zero, so once the droplets touch the conductor, they will be frozen and become part of the ice layer on the power line. Several factors could affect the mass and shape of the ice layer, including air temperature, relative humidity, precipitation rate, wind speed, the angle between wind flow and conductor, and the conductor diameter [10][11].

In short, droplets move with air stream toward the conductor, stick to the conductor, and become ice. The location where the droplets touch the conductor is determined by the airflow nearby the power line and the inertia of droplets [12]. Furthermore, the location of droplets finally decide the shape of the ice layer on the conductor. Since the droplets tend to hit the upwind side of the conductor, in most cases, the cross-sector of the ice layer looks like an ellipse instead of a circle. To validate this theory, Chongqing University in China

built an icing station to capture the cross-section profiles of iced conductors [13]. Figure 1.5 shows the diagram of an elliptic iced conductor [13]. Figure 1.6 shows photos taken from field experiments [13].

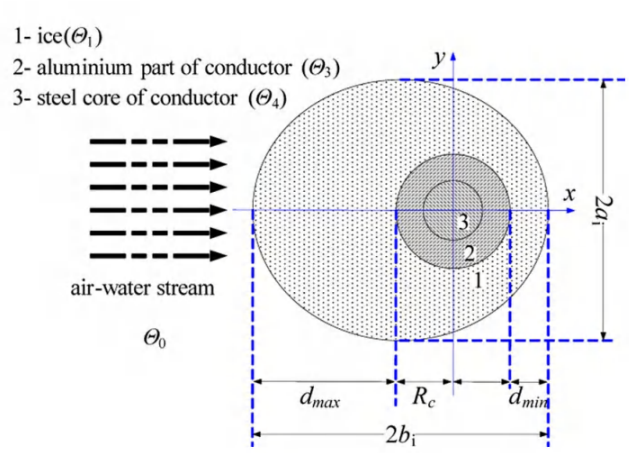

Figure 1.5: Elliptic iced conductor diagram. Source: from [13] ©2011 IEEE

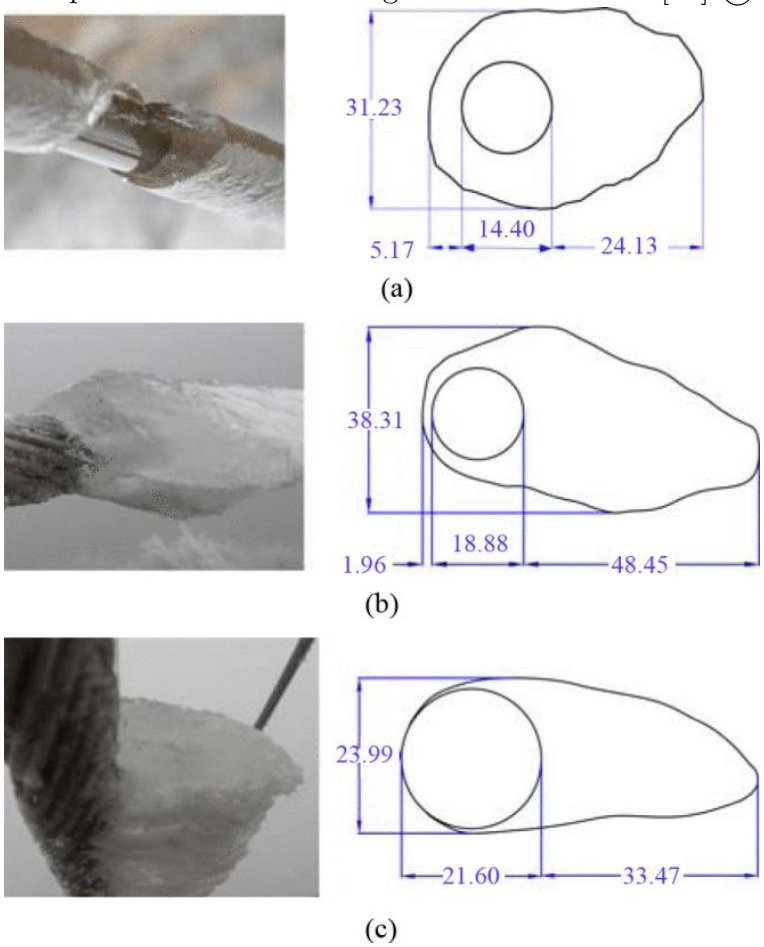

Figure 1.6: Cross section profile for iced conductors. Adopted from [13] ©2011 IEEE

After understanding the shape of the cross-section of the ice layer on the power line, one can study the ice melting process of the iced conductor. Reference [13] divides the melting

process of an elliptic iced conductor into three stages:

(1) Temperature Rising Stage: Before starting the melting process, the temperatures of both the conductor and ice layer are equal to the ambient temperature (far below 0°C). After DC current is applied, the temperature of the conductor starts rising, but the ice layer will not start to melt until the boundary between the conductor and ice layer reaches 0°C. The interval between the beginning of the melting process and the conductor-ice interface temperature reaching 0°C is defined as the temperature rising stage.

(2) Ice Rotating Stage: As discussed before, the ice layer tends to grow on the upwind side, so a cohesive force between the conductor surface and inner surface of the ice layer is needed to support the ice layer's gravitational torque. When the inner ice layer starts to melt, the cohesive force is weakened and finally becomes too weak to support the ice layer. Then the ice layer rotates until its center of gravity falls right below the conductor. It is worth mentioning that an air gap forms between the conductor and ice after the rotation.

(3) Ice Shedding Stage: After the second stage, the ice layer is supported by the ice on top of the conductor. As melting proceeds, the top part of the ice layer becomes increasingly thinner, and finally the ice is shed off.

To quantify the melting procedure above and find out the ice melting time in a certain scenario, a mathematical model is developed in [13]. As a conclusion, with a DC current of 800-1000 A, the melting process typically lasts for 30-180 minutes depending on the ambient temperature, the shape of ice layer, and other weather conditions.

1.2.2 AC-DC Converter types

To find a suitable AC-DC conversion method for the DC deicer application, the two dominant types of HVDC converters, line commutated converter (LCC) and voltage source converter (VSC) are reviewed in this subsection.

LCC converter

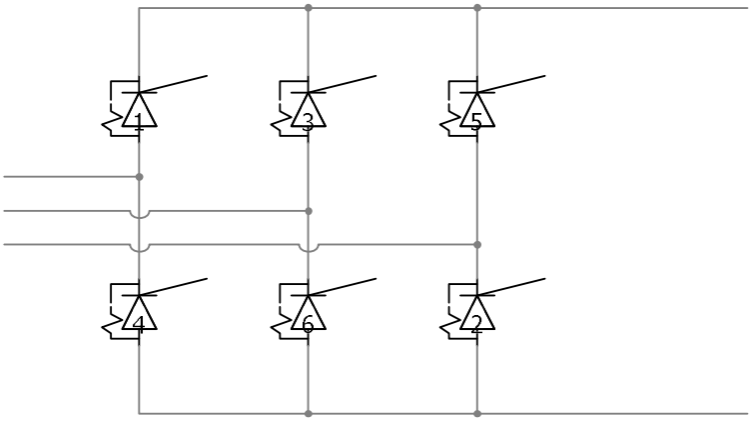

Figure 1.7: Diagram of a LCC converter.

As shown in Figure 1.7, the LCC utilizes thyristors as the power switch. A thyristor is a half-controlled power semicondcutor, so the LCC converter is controlled by adjusting the firing angles of its thyristors. Since the thyristor cannot be controlled to switch off as long as there is current flow, the commutation of LCC converter depends on the AC line voltage [14].

The advantages of the LCC technology is the high voltage and power rating and low complexity. Thyristor technology has the largest blocking voltage capability compared with other power semiconductors (for example IGBT, GTO, IGCT) [15][16]. Also, the topology and controlling strategy of an LCC is simple and reliable. The high power rating and low complexity make LCC technology especially suitable for high power DC transmission projects (for example a bulk power transmission system project).

However, there are also disadvantages of the LCC technology. The AC voltage of an LCC cannot be controlled arbitrarily, so the reactive power flow can be massive during operation. Furthermore, the current and voltage harmonics of LCC converter are high. To address these problems, LCCs usually operate with reactive compensation devices and filters, so the size

of LCC power conversion system is relatively larger.

VSC converter

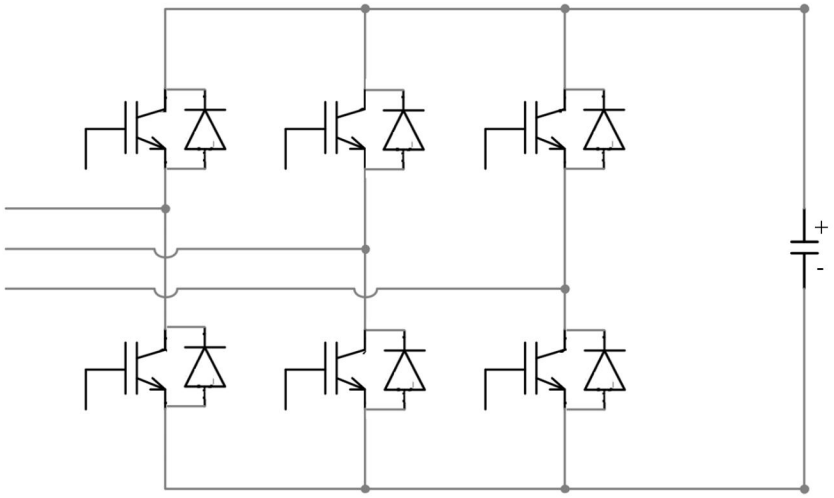

Figure 1.8: Diagram of VSC converter.

The diagram of a two-level VSC converter is shown in Figure.1.8. The voltage source converter uses IGBTs for switching. An IGBT is a fully-controlled power semiconductor so that the AC terminal can be freely switched to output $+V_{dc}/2$ or $-V_{dc}/2$ voltage depending on the firing pulses signal. The control of IGBTs in the VSC converter is achieved by pulse width modulation (PWM). With a high frequency carrier and 60 Hz modulation waveform, the AC terminals of VSC can output desirable AC voltage. The magnitude and phase angle of output AC voltage is controlled by the modulation index and phase angle of modulation waveform. A large capacitor is required to maintain the DC voltage on the DC side of the converter.

A VSC is a relatively new technology compared with LCC. VSC technology is studied and applied by many researchers due to its fully controllable AC output voltage. However, there are also disadvantages to VSC converter.

The first disadvantage for VSC converter is that a high capacitance and high voltage capability capacitor is required on the DC side of the converter. The second disadvantage is

that the AC output waveform of a two-level VSC converter is a bipolar waveform that contains massive harmonic components, so a filter is required on the AC side of the converter. The last disadvantage is that, controlled by PWM technology, it requires the IGBTs to switch at a very high frequency; thus the switching losses of the converter become an obvious problem [17]

To solve these problems, researchers aim to increase the voltage level of VSC converter, which leads to the prevalence of Modular Multilevel Converter (MMC) technology.

MMC converter

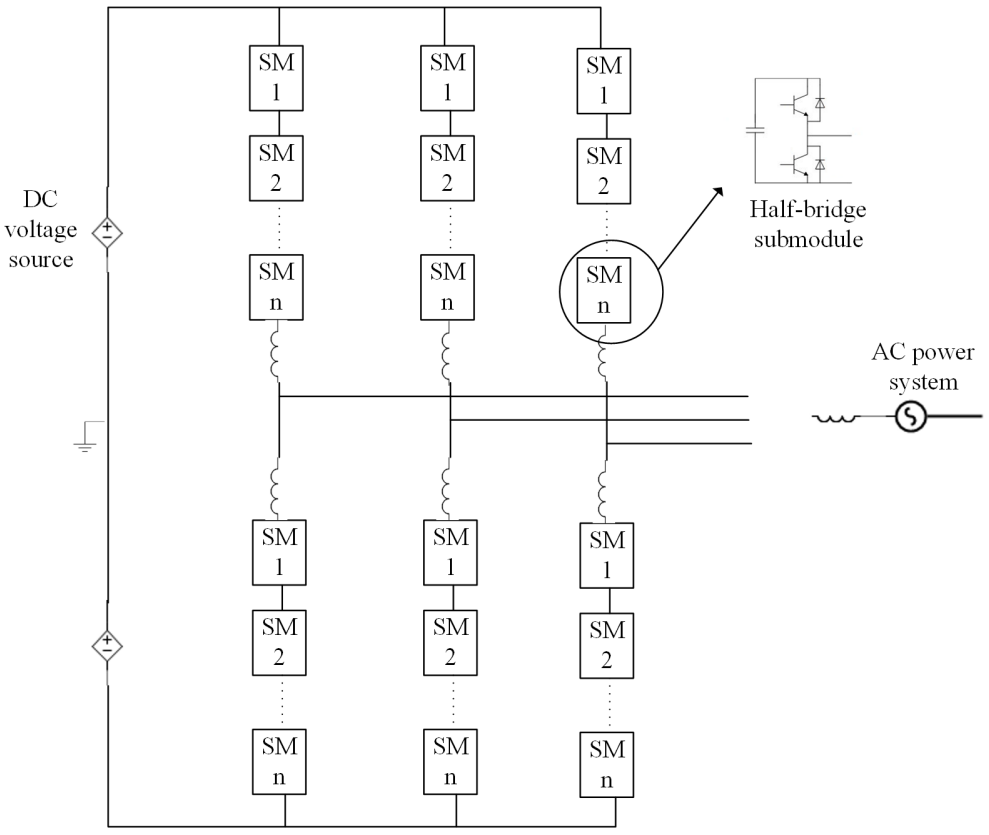

Figure 1.9: Conventional MMC converter with half-bridge submodules.

A Modular Multilevel Converter (MMC) with half-bridge submodule (SM) was proposed in 2002 by Prof. Marquardt [18]. MMC consists of three phases (six arms). Each arm contains N SMs. There are two types of SM, namely half-bridge SM and full-bridge SM. In a half-

bridge SM, there are two IGBTs for switching, two anti-parallel diodes and a small capacitor for energy storage.

The diagram of an MMC with half-bridge SM is shown in Figure 1.9. With N SMs installed in each arm, the converter is capable for outputting an $N + 1$-level AC voltage waveform. With a proper number of levels, the output voltage is close to a sinusoidal waveform, so there is no need for filters on the AC output terminals. Compared with two-level VSC converter, there is no need for a large DC side capacitor; instead, there are a number of small capacitors in every SM. Furthermore, the switching frequency for each IGBT in MMC converter is greatly reduced, the switching loss of MMC is much better than two-level VSC converter [19].

1.2.3 DC buck converter

A DC-DC buck converter converts a larger DC voltage into a smaller one. The converter is consists of two capacitors (input voltage capacitor C_{in} and output voltage capacitor C_{out}), a IGBT for power switch, an inductor, and a diode.

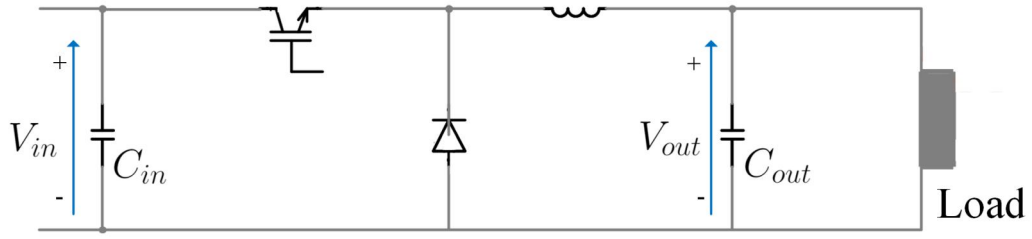

Figure 1.10: DC-DC buck converter.

There are two states of the buck circuit. By switching on and off the IGBT [20], the buck converter operates between on-state and off-state. The two operation states are shown in Figure 1.11.

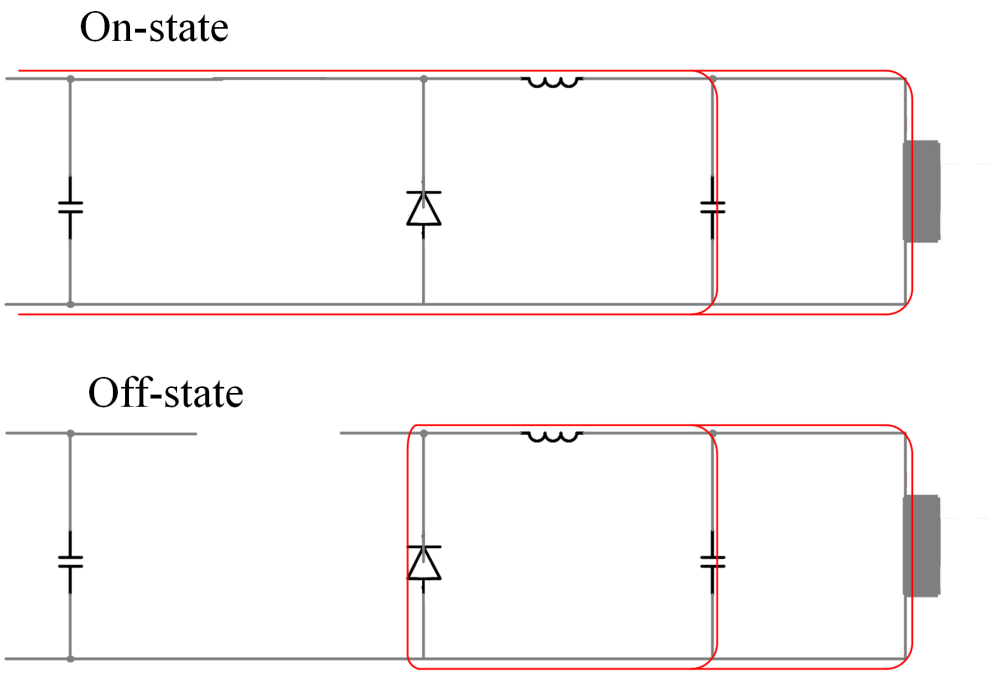

Figure 1.11: On-state (above) and off-state (below) of converter.

During on-state, the IGBT is switched on, input DC voltage provides energy for both the load and the energy stored in the inductor and output capacitor. During off-state, the IGBT is switched off, the inductor and output capacitor release the stored energy to maintain the load current.

The output DC voltage of buck converter is controlled by pulse-width modulation (PWM). PWM control is achieved by comparing a DC modulation signal with a switching frequency carrier. The IGBT switches on when the modulation signal is higher than carrier, vise versa switches off when the modulation signal is lower than carrier. The PWM schematic is shown in Figure 1.12.

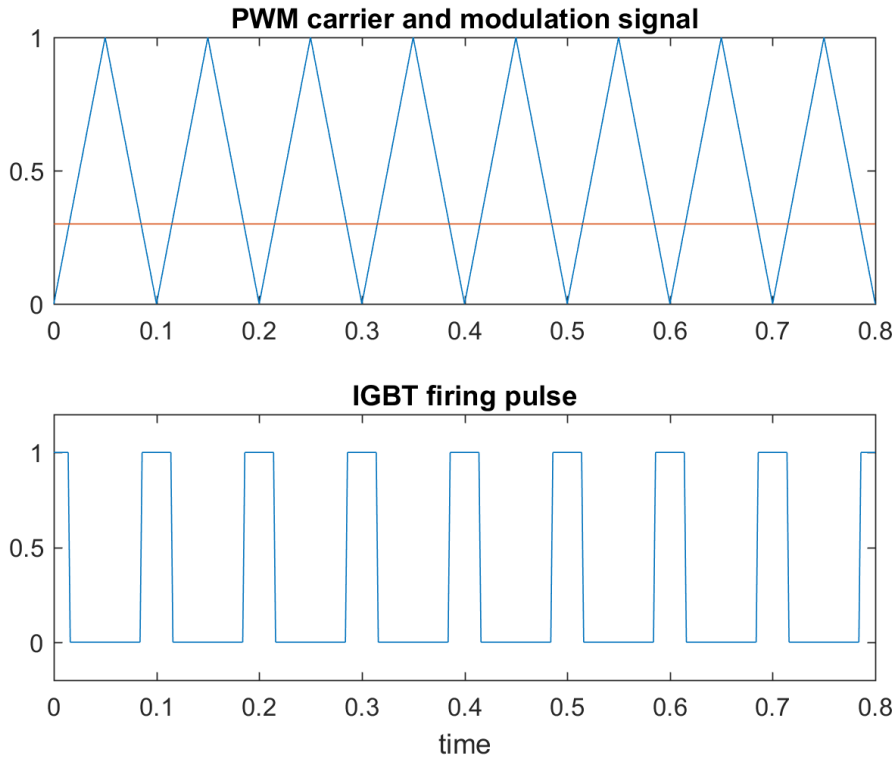

Figure 1.12: PWM carrier and modulation signal (top) Buck converter IGBT firing pulses (bottom).

The ratio of on-state operation time T_{on} to the whole switching period T_s (including on-state operation time and off-state operation time) is called the duty ratio [21].

The relation ship between buck converter input voltage V_{in} and output voltage V_{out} is described as (1.1):

$$V_{out} = \frac{T_{on}}{T_s} V_{in} \tag{1.1}$$

By changing the DC modulation signal, the duty ratio can be changed thus the output voltage is regulated to the desired value.

1.3 Thesis Motivation

It has been shown that a DC deicer is an efficient and economical way to melt ice on a long power line segment. To further reduce the cost and increase the flexibility of the deicer

device, utilities and researchers are looking for a portable DC-deicer design so that nearby AC stations can share one deicer. However, the conventional design of the DC deicer uses a thyristor-based LCC converter, and its size and performance are not suitable for a portable deicer. This provides the motivation to study the feasibility of applying a more up-to-date VSC technology in the design of a DC deicer. In this thesis, two DC deicer designs based on a single-arm MMC will be discussed, and both EMT (electromagnetic transient) simulation and hardware prototyping methods will be used to verify the design.

1.4 Objectives and Methodologies

Based on the presented background and motivation, this thesis will include the whole procedure of developing a compact-size, high-performance DC deicer, including the circuit topology design, parameter design, the validation of results, and performance analysis.

During this procedure, several new methods are introduced. Primarily, this deicer design aims to reduce the size of the device significantly. To achieve this goal, the two fundamental ideas are to reduce the size of the rectifier transformer and reduce the size of the converter itself. To reduce the transformer's size, trying to minimize the reactive power absorbed by the converter is one solution, so that a transformer with a small MVA rating can be deployed. This thesis addresses this issue by adding a DC-DC buck converter to fully control the rectifier DC voltage. To reduce the rectifier's size, SAMMC topology is utilized to reduce the SM valves by half; also, a 2HCSC (2nd harmonic current suppression controller) is designed for SAMMC, so that the SM capacitor size can be significantly reduced.

The design procedure consists of mathematical modeling, EMT simulations, and hardware validation. Firstly, a mathematical model of the circuit is developed to select the parameters and investigate the operating conditions. Secondly, another mathematical model is developed to calculate the harmonics and size the passive components accurately. Thirdly, the system is simulated in EMT simulation solvers (PSCAD/EMTDC and RSCAD-RTDS). Lastly, a

scaled-down prototype is developed to prove the feasibility of our design in reality.

The specific objectives and methodologies in this thesis are listed as follows:

(1) Propose two different designs for SAMMC-based portable DC deicer. The first design consists of a transformer and a SAMMC rectifier. For the second design, a DC-DC converter is added to the DC side of SAMMC. While one more converter is added in the second design, the transformer size is reduced.

(2) Develop the circuit's mathematical model. This model is developed for parameter design and finding the optimal operating conditions of the SAMMC rectifier. Several parameters need to be settled in the design procedure, such as transformer voltage rating, transformer MVA rating, and SM capacitor value. Also, as a highly controllable converter, the magnitude and phase angle of SAMMC's AC voltage can be controlled by its modulation waveform. So the design of the modulation index and phase angle is also an issue. To avoid a large number of time-consuming EMT simulations, this faster model is developed to design these parameters and modulation waveform for the first step in an approximate manner. This mathematical model is developed to approximately give out the device performance (for example, AC/DC side voltage and current, SM capacitor average voltage, and real power/reactive power absorbed by the rectifier) once a set of parameters and modulation waveform is selected. As a result, the optimal parameters will be obtained from this model to reduce the size of the transformer and the rectifier.

(3) Develop a mathematical model to analyze circuit harmonics. The values of arm inductors and SM capacitors are critical in deciding the current harmonics level. In order to control the harmonics level to satisfy IEEE standards, we need to develop a mathematical model to describe the relationship between SM capacitor value/arm inductor value and harmonics, and use this model to design the parameters accurately. Since the current harmonics cannot be obtained directly, an iterative method is used to solve this problem and give out the 2nd/3rd harmonics magnitudes.

(4) Develop an EMT model for the two designs of the DC deicer device. This thesis

uses the "detailed equivalent model" to simulate the SAMMC rectifier. This thesis will use RSCAD to simulate the device on a real-time simulator. This model will be used to validate the performance of the DC deicer device and validate the two proposed mathematical models.

(5) Propose a 2HCSC (2nd harmonic current suppression controller). No previous research has been done about the current harmonics suppression controller for SAMMC topology, and the 2HCSC for conventional MMC cannot work with SAMMC, and no 2HCSC method has been proposed to suppress the 2nd harmonics in SAMMC so far. A new 2HCSC method is developed for SAMMC and validated using EMT simulations. After deploying the 2HCSC controller, the size of the SM capacitor can be reduced.

(6) Develop a scaled-down hardware prototype for the DC deicer. A low-power laboratory setup is built to test the DC deicer device. An AC voltage source is provided by LabVolt and the SAMMC is driven by firing pulses generated by RTDS.

1.5 Thesis Outline

The remaining parts of this thesis are organized as follows:

Chapter 2 is an introduction to SAMMC. The operating principles, control diagrams, and parameter design principles of SAMMC are described. Chapter 3 focuses on the two different designs of SAMMC DC deicer. The parameter design and simulation results are included. Furthermore, this thesis will analyze and make the comparison of the two designs. In chapter 4, the RTDS hardware-in-loop validation is built and analyzed. Chapter 5 concludes this thesis and discusses conclusions, contributions, and recommendations for future research.

Chapter 2

Introduction to a Single-Arm MMC

2.1 Operation principle of a SAMMC rectifier

References [22] and [23] have discussed the operating principles of a SAMMC inverter. However, for the DC deicer application, the SAMMC converter is used as a rectifier. This section discusses the operating principles of an SAMMC rectifier. Several diagrams and equations regarding the steady state normal operating condition will be demonstrated. The AC current and DC current equivalent circuits are extracted to illustrate the AC-DC power conversion in SAMMC.

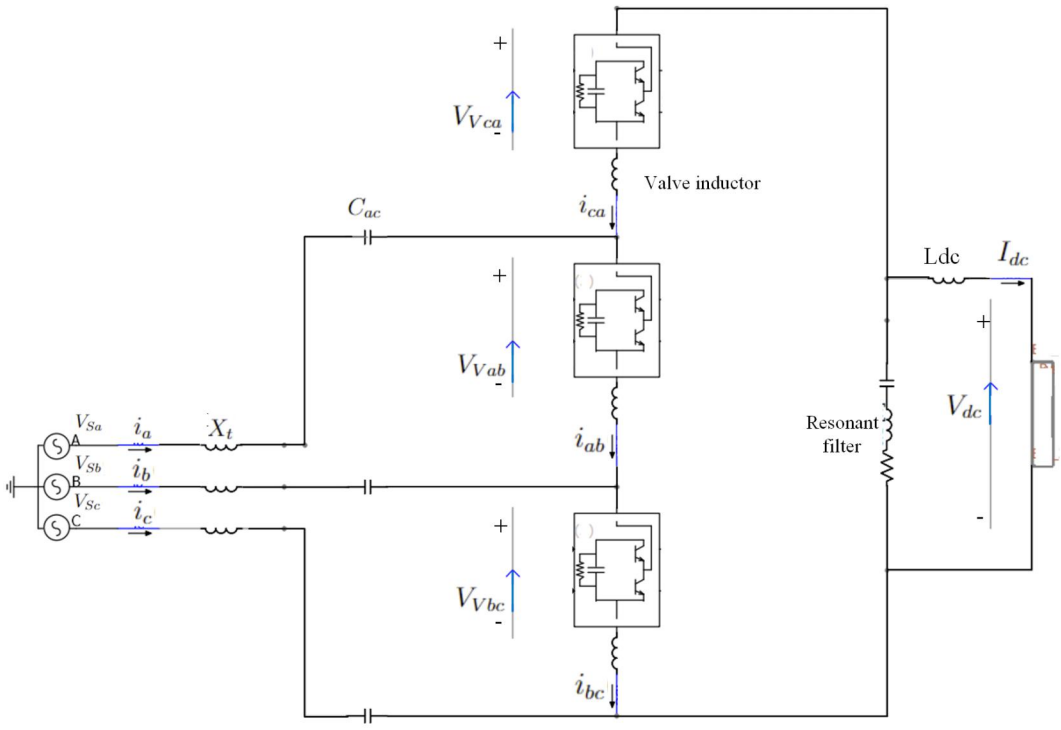

Figure 2.1: Diagram of a SAMMC rectifier.

Figure 2.1 is a diagram of a SAMMC rectifier with a DC load. This chapter introduces its operation by analyzing the voltage characteristic of the converter. The SAMMC converter consists of three valves. Each valve contains N submodules (SMs) whose nominal average voltage is noted as V_{csm}, so each valve is able to produce a voltage range from 0 to NV_{csm} on the AC side. In normal operation, the number of SMs inserted in the valve is controlled by a modulation waveform with a modulation index m and a phase angle θ, and the valve voltage becomes $\frac{1}{2}NV_{csm}(1 + m\sin(\omega t + \theta))$ if harmonics are ignored. The valve voltage mainly contains a fundamental component and a DC component. The fundamental component produced by each valve is the line-to-line (L-L) AC output voltage, and three AC-side capacitors block the DC voltage component. The converter is connected with the AC system via a transformer represented as the impedance X_t. On the DC side, since three valves are placed on one string, the summation of the total number of inserted SMs in all three valves

is $\frac{3N}{2}$. So the DC side voltage is kept constant at $\frac{3N}{2}V_{csm}$.

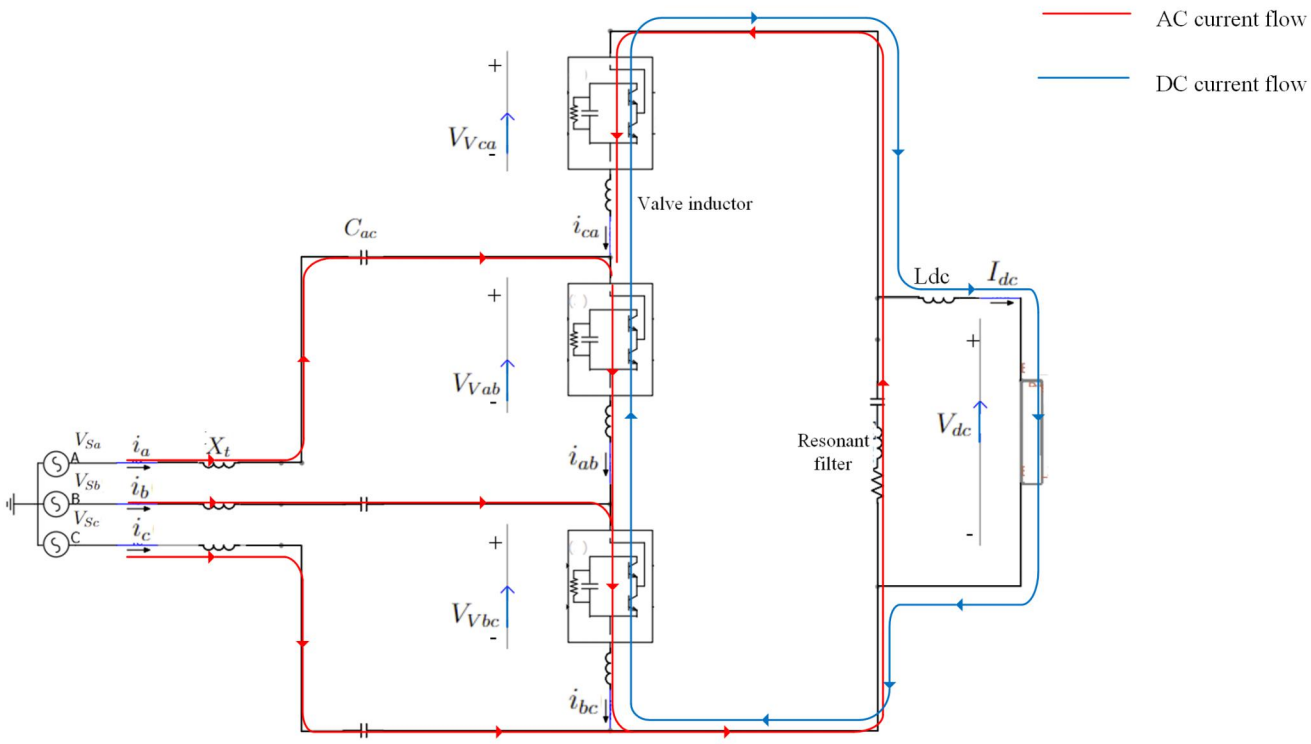

Figure 2.2: AC and DC current flow in a SAMMC.

Figure 2.21 shows the AC and DC current flow paths in a SAMMC. For AC currents, three-phase AC currents injected from the power system flow through the transformer and AC capacitors to charge SM capacitors; a resonant filter which is tuned to fundamental frequency is utilized to prevent AC current flow through the DC side. The DC current is blocked by the capacitor in the resonant filter so it will flow into the DC load. The current flow through the valve string contains both AC current component (charging current component) and DC current component (discharging current component), so that the SM capacitor voltage as well as DC side voltage can keep constant.

To quantify the above description, the equations regarding current, voltage, and power under steady-state normal operation are discussed next. Note that this analysis is not a fully detailed mathematical model; harmonics are ignored, and all components are assumed to be

ideal.

As illustrated in [24], the common strategies for the controlling MMCs are Phase Shifted PWM (PSPWM) and Level Shifted PWM (LSPWM), and the number of inserted SMs are controlled by sinusoidal modulation waveform.

AC power system phase voltage are given as follows :

$$\begin{aligned} V_{Sa}(t) &= \sqrt{2}V_{Sph}\sin(\omega t - \frac{\pi}{6}) \\ V_{Sb}(t) &= \sqrt{2}V_{Sph}\sin(\omega t - \frac{5\pi}{6}) \\ V_{Sc}(t) &= \sqrt{2}V_{Sph}\sin(\omega t + \frac{\pi}{2}) \end{aligned} \tag{2.1}$$

where V_{Sph} is the RMS value of the power system's phase voltage, and ω is the angular frequency of power system.

AC power system L-L voltage are as follows:

$$\begin{aligned} V_{Sab}(t) &= \sqrt{6}V_{Sph}\sin(\omega t) \\ V_{Sbc}(t) &= \sqrt{6}V_{Sph}\sin(\omega t - \frac{2\pi}{3}) \\ V_{Sca}(t) &= \sqrt{6}V_{Sph}\sin(\omega t + \frac{2\pi}{3}) \end{aligned} \tag{2.2}$$

Modulation waveforms for each valve are:

$$\begin{aligned} wv_{ab}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta)) \\ wv_{bc}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta - \frac{2\pi}{3})) \\ wv_{ca}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta + \frac{2\pi}{3})) \end{aligned} \tag{2.3}$$

The modulation index m ranges from 0 to 1.0, and θ is the phase angle between the modulation waveform and power system's AC voltage.

Equation (2.3) leads to the following expressions for the valve voltages:

$$\begin{aligned} V_{Vab}(t) &= \frac{NV_{csmAB}(t)}{2}(1 + m\sin(\omega t - \theta)) \\ V_{Vbc}(t) &= \frac{NV_{csmBC}(t)}{2}(1 + m\sin(\omega t - \theta - \frac{2\pi}{3})) \\ V_{Vca}(t) &= \frac{NV_{csmCA}(t)}{2}(1 + m\sin(\omega t - \theta + \frac{2\pi}{3})) \end{aligned} \tag{2.4}$$

where $V_{csmAB}(t)$, $V_{csmBC}(t)$, and $V_{csmCA}(t)$ are the average SM capacitor voltages in each valve. Thus the L-L output voltage of the converter can be expressed as follows:

$$\begin{aligned} V_{Cab}(t) &= \frac{NV_{csmAB}(t)}{2} m\sin(\omega t - \theta) \\ V_{Cbc}(t) &= \frac{NV_{csmBC}(t)}{2} m\sin(\omega t - \theta - \frac{2\pi}{3}) \\ V_{Cca}(t) &= \frac{NV_{csmCA}(t)}{2} m\sin(\omega t - \theta + \frac{2\pi}{3}) \end{aligned} \tag{2.5}$$

The DC voltages blocked by the AC-side capacitors are:

$$\begin{aligned} V_{Caca}(t) &= \frac{N\overline{V_{csm}}}{2} \\ V_{Cacb}(t) &= 0 \\ V_{Cacc}(t) &= -\frac{N\overline{V_{csm}}}{2} \end{aligned} \tag{2.6}$$

where $\overline{V_{csm}}$ is the DC component of $V_{csmAB}(t)$, $V_{csmBC}(t)$, and $V_{csmCA}(t)$.

Applying Kirchhoff's voltage law (KVL) to the three-valve string and DC load, DC side voltage can be obtained:

$$V_{dc}(t) = I_{dc}(t)R_{dc} = V_{Vab}(t) + V_{Vbc}(t) + V_{Vca}(t) + L_{arm}(\frac{di_{ab}}{dt} + \frac{di_{bc}}{dt} + \frac{di_{ca}}{dt}) \tag{2.7}$$

Ignoring current harmonics, i_{ab}, i_{bc} and i_{ca} contain DC current and symmetrical AC components. Also I_{dc} contains only a DC component ideally; therefore, $\frac{di_{ab}}{dt} + \frac{di_{bc}}{dt} + \frac{di_{ca}}{dt} = 0$.

Combined with (2.4), (2.7) can be rewritten as:

$$V_{dc} = \frac{3N\overline{V_{csm}}}{2} \tag{2.8}$$

The expression of the currents flowing in the SAMMC rectifier can be found by assuming the power factor of the converter as $\cos\varphi$. The arm currents (phase currents) flowing in three SM valves are as follows:

$$\begin{aligned} i_{ab}(t) &= -I_{dc} + \frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta - \varphi) \\ i_{bc}(t) &= -I_{dc} + \frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta - \frac{2\pi}{3} - \varphi) \\ i_{ca}(t) &= -I_{dc} + \frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta + \frac{2\pi}{3} - \varphi) \end{aligned} \tag{2.9}$$

where I_L denotes the RMS value of the line current. The three line currents (output currents) are:

$$\begin{aligned} i_a(t) &= \sqrt{2} I_L \sin(\omega t - \theta - \frac{\pi}{6} - \varphi) \\ i_b(t) &= \sqrt{2} I_L \sin(\omega t - \theta - \frac{5\pi}{6} - \varphi) \\ i_c(t) &= \sqrt{2} I_L \sin(\omega t - \theta + \frac{\pi}{2} - \varphi) \end{aligned} \tag{2.10}$$

In steady state operation, the input AC power and output DC power are equal, and so the average SM capacitor voltage (V_{csm}) is kept constant. The power balance implies that:

$$\begin{aligned} P_{dc} = I_{dc} V_{dc} = P_{ac} &= 3 V_{cL-L} I_{arm} \cos\varphi \\ P_{ac} &= \frac{\sqrt{3} V_{Sph} V_{cL-L} \cos\theta}{X_T - \frac{1}{jwC_{ac}}} \end{aligned} \tag{2.11}$$

where V_{cL-L} is the RMS value of the converter L-L voltage, and I_{arm} is the RMS value of the AC component in arm current. With (2.5) and (2.9), the expression of I_L and I_{dc} can be extracted from (2.11) as:

$$I_L = \frac{V_{Sph}\cos\theta}{(X_T - \frac{1}{jwC_{ac}}\cos\varphi)} \tag{2.12}$$

$$I_{dc} = \frac{mI_L\cos\varphi}{\sqrt{6}} \tag{2.13}$$

Finally, the equation for power angle φ needs to be obtained. The converter valves are connected to the AC system via a transformer (X_t) and AC side capacitor (C_{ac}). By ignoring the negligible impact of the arm inductor, then

$$\frac{V_{Sph}\angle -\frac{\pi}{6} - \frac{V_{cL-L}}{\sqrt{3}}\angle -\frac{\pi}{6} - \theta}{X_T - \frac{1}{jwC_{ac}}} = I_L\angle -\theta - \frac{\pi}{6} - \varphi \tag{2.14}$$

and φ can be expressed as:

$$\varphi = -\theta - 30^\circ - arcsin(\frac{V_{Sph}\sin(-\frac{\pi}{6}) - \frac{V_{cL-L}}{\sqrt{3}}\sin(-\frac{\pi}{6} - \theta)}{(X_T - \frac{1}{jwC_{ac}})I_L}) \tag{2.15}$$

To show the difference between the power transmission of SAMMC and conventional MMC, the following diagram in Figure 2.3 shows the PQ absorbing capability for SAMMC and MMC with the same semiconductors (4.5 kV, 1000 A) and the same voltage level (12 SMs per valve).

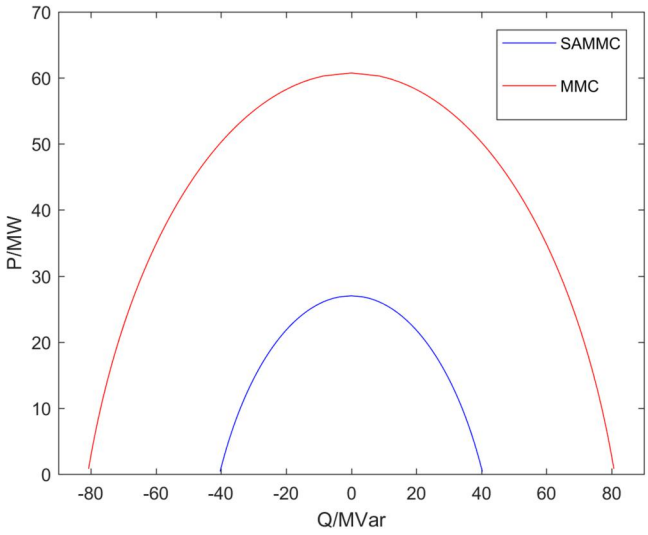

Figure 2.3: The PQ capability of SAMMC rectifier.

According to the PQ capability diagrams, the PQ absorbing range of SAMMC converter is significantly smaller than that of a conventional MMC. So the SAMMC topology is more suitable for low-power applications, especially those applications whose cost and size must be reduced.

Till now, the operating principle, power conversion principle, and key mathematical expressions at fundamental frequency have been clearly stated. This part serves as an introduction, and a more accurate mathematical model will be developed in Chapter 3.

2.2 The design of key parameters

Chapter 2 of [25] demonstrates the design of circuit parameters of a conventional MMC converter. This subsection briefly describes the procedure to design parameters for the SAMMC converter, including the number of SMs per valve, arm inductors, and AC-side capacitors. As the voltage rating and power rating of the system must be given before deciding converter parameters, this thesis assumes that the rated AC-side voltage is 13 kV, rated DC-side voltage is 6 kV, and the rated power is 5 MW. (These are not the system ratings of the DC-deicer system; they are rather for demonstrating parameter sizing procedure in this subsection.)

2.2.1 Number of SMs per valve

The first parameter to be decided is the number of SMs per valve. The number of SMs is related to semiconductor voltage rating and voltage harmonics. Similarly, with the design of a conventional MMC, the primary consideration for deciding the number of SMs is related to the voltage rating of the power semiconductor device.

The maximum voltage on SM capacitor should not exceed the voltage rating of the power semiconductors. From (2.8) the average SM capacitor voltage can be expressed as:

$$\overline{V_{csm}} = \frac{2V_{dc}}{3N} \tag{2.16}$$

The maximum voltage across each SM capacitor is the SM capacitor's peak voltage. This voltage can be calculated as the sum of the average SM capacitor voltage and half of the voltage ripple. Normally the voltage ripple of any VSC converter capacitor can be considered as $\pm 10\%$ as shown in [26]. Therefore, the voltage ripple equation can be rewritten as:

$$V_{rip} = 0.1\overline{V_{csm}} \tag{2.17}$$

where V_{rip} denotes the peak-peak value of the SM capacitor voltage ripple.

The voltage ratings of semiconductors are decided by the rating of a single IGBT and the arrangement of IGBTs. While IGBTs can be arranged as a series stack to withstand a much higher voltage, according to literature [27], [28], and [29], the series stack arrangement can introduce unbalanced voltages within the stack and lead to higher switching losses. To avoid unnecessary power losses and control complexities, it is possible to use a high enough number of SMs (N) so that the V_{csm} is lower than a single IGBT's voltage rating.

In conclusion, to avoid a series-stack IGBT arrangement, the first criterion to choose the number of SMs can be described as the following inequality:

$$V_{scr} < 1.1\overline{V_{csm}} = 1.1 \times \frac{2V_{dc}}{3N} \Rightarrow N > \frac{2.2V_{dc}}{3V_{scr}} \tag{2.18}$$

For low DC rating applications, for example, the DC deicer application proposed in this thesis, the rated DC voltage is only around 6 kV, and the voltage rating for commercial IGBTs can reach 6.5 kV nowadays [30]. So the number of SMs cannot be solely decided by the semiconductor ratings in low DC voltage applications.

The second consideration for choosing the right number of SMs is the voltage harmonics. When the number of SMs is relatively small, the nearest-level control cannot give out a satisfactory voltage waveform [31]. Therefore, controlling the SAMMC by a multicarrier-based PWM method is a better choice. When the modulation index is close to unity, the number of voltage waveform levels is equal to the number of SMs per valve. With a higher number of converter output voltage levels, voltage harmonics can be greatly reduced. The regulation for voltage harmonics limits at point of common coupling (PCC) can be found in the IEEE 519-2014 standard [32], note that some utilities may have stricter limits than IEEE 519-2014.

To quantify the relationship between voltage switching harmonics and the number of SMs per valve, Figure 2.4 shows the voltage waveform THD for different numbers of SMs (N), Figure 2.5 shows the schematic diagram of phase disposition pulse width modulation (PDPWM), and Figure 2.6 shows the output voltage waveform, and Figure 2.7 is the voltage harmonics spectrum. (Note that only switching harmonics are included when discussing the number of SMs per valve; the voltage ripple on SM capacitors is ignored.)

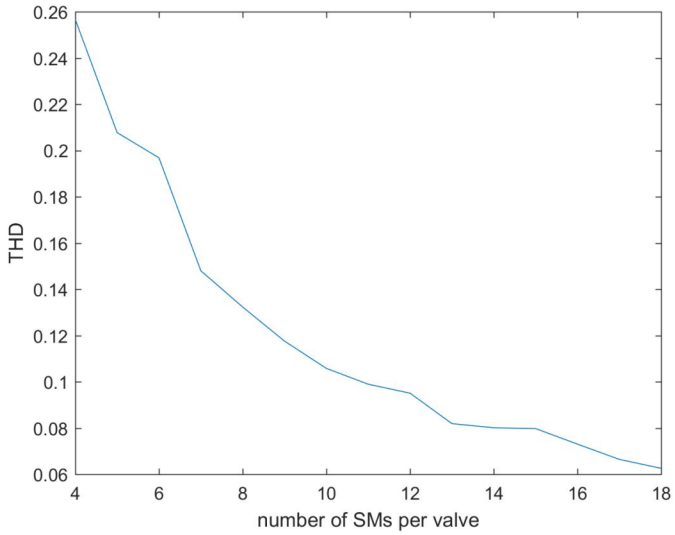

Figure 2.4: Voltage THD vs, the number of SMs (carrier frequency = $9f_0$, modulation index = 1.0).

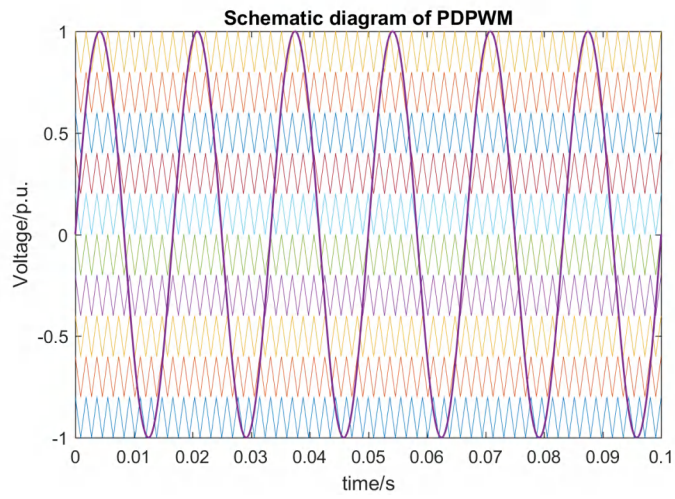

Figure 2.5: Schematic diagram of phase disposition PWM (PDPWM).

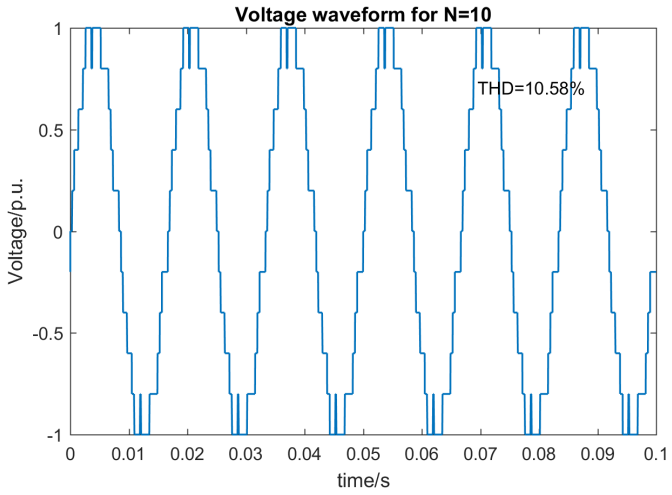

Figure 2.6: Voltage waveform for $N = 10$ (carrier frequency $= 9f_0$, modulation index $= 1.0$).

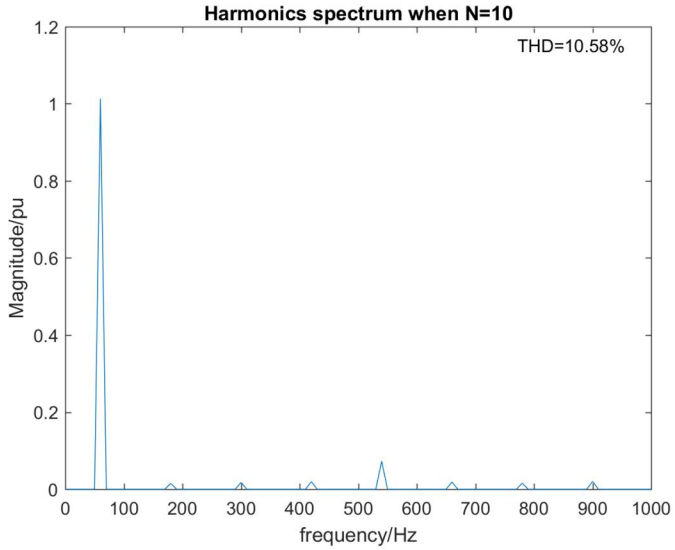

Figure 2.7: Voltage harmonics spectrum (including the first 15 harmonics).

As shown in Figure 2.4, at least 16 SMs are required in each valve to limit the voltage harmonics to under 7.5%. However, with a higher number of SMs in each valve, the size of SAMMC converter is significantly enlarged. The size of the converter is proportional to the number of SMs. The final decision on this parameter should be made based on two considerations: the voltage harmonics level must be acceptable, the size of SAMMC converter must be as small as possible. Specifically, in this portable DC deicer application, the converter

works with low power and is not a permanent load. It will only be connected to power system during emergency conditions, so a compromising voltage harmonics performance could be acceptable.

2.2.2 SM capacitor sizing

It is important to choose the right value for SM capacitance. A low value for the SM capacitance will cause a high voltage ripple on SM capacitor voltage during its charging and discharging process and causes a high level of voltage and current harmonics. On the contrary, an unnecessarily high SM capacitance will increase the cost and size of the converter. In the design of conventional MMCs, a common practice for capacitor design is that the energy stored in all capacitors should yield 30-40kJ/MVA [26] of energy storage. While this common practice provides an approximate range for SM capacitance design, it is insufficient to choose an accurate, optimal value for SM capacitance. To achieve this goal, this thesis finds out the theoretical relationship between SM capacitance and SM voltage ripple, and finds the right capacitance value to limit the voltage ripple to a certain level.

It is first noted that:

$$\begin{aligned}
\Delta V_{csmAB}(t) &= \frac{1}{NC_{sm}} \int_0^t n_{AB}(t) \cdot i_{ab}(t)\, dt \\
\Delta V_{csmBC}(t) &= \frac{1}{NC_{sm}} \int_0^t n_{BC}(t) \cdot i_{bc}(t)\, dt \\
\Delta V_{csmCA}(t) &= \frac{1}{NC_{sm}} \int_0^t n_{CA}(t) \cdot i_{ca}(t)\, dt
\end{aligned} \tag{2.19}$$

where $n_{AB}(t), n_{BC}(t)$, and $n_{CA}(t)$ are the number of SMs inserted in each valve at time t; their expressions can be found as:

$$\begin{aligned}
n_{AB}(t) &= N \cdot wv_{ab}(t) \\
n_{BC}(t) &= N \cdot wv_{bc}(t) \\
n_{CA}(t) &= N \cdot wv_{ca}(t)
\end{aligned} \tag{2.20}$$

where $wv_{ab}(t)$, $wv_{bc}(t)$ and $wv_{ca}(t)$ are the modulation waveforms for three valves. Substituting (2.3), (2.9) and (2.20) into (2.19), the final relationship between SM voltage ripple and C_{sm} can be described as:

$$\begin{aligned}
\Delta V_{csmAB}(t) =& \frac{1}{2C_{sm}}\left[-\frac{\sqrt{2}I_L}{\sqrt{3}\omega}\cos(\omega t-\varphi-\theta)+\frac{mI_{dc}}{\omega}\cos(\omega t-\theta)-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t-\varphi-2\theta)\right] \\
\Delta V_{csmBC}(t) =& \frac{1}{2C_{sm}}\left[-\frac{\sqrt{2}I_L}{\sqrt{3}\omega}\cos(\omega t-\varphi-\theta-\frac{2\pi}{3})\right. \\
&\left.+\frac{mI_{dc}}{\omega}\cos(\omega t-\theta-\frac{2\pi}{3})-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t-\varphi-2\theta+\frac{2\pi}{3})\right] \\
\Delta V_{csmCA}(t) =& \frac{1}{2C_{sm}}\left[-\frac{\sqrt{2}I_L}{\sqrt{3}\omega}\cos(\omega t-\varphi-\theta+\frac{2\pi}{3})\right. \\
&\left.+\frac{mI_{dc}}{\omega}\cos(\omega t-\theta+\frac{2\pi}{3})-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t-\varphi-2\theta-\frac{2\pi}{3})\right]
\end{aligned} \tag{2.21}$$

A conventional approach for sizing SM capacitance is to regulate the SM capacitor voltage ripple under a certain range (for example 10% of its average voltage value).

The accurate SM capacitor voltage ripple of valve AB can be obtained by finding out the maximum SM capacitor voltage and minimum SM capacitor voltage, as described below:

$$V_{rip} = \Delta V_{csmABmax} - \Delta V_{csmABmin} \tag{2.22}$$

where $\Delta V_{csmABmax}$ denotes the maximum value of SM capacitor voltage and $\Delta V_{csmABmin}$ denotes the minimum value of SM capacitor voltage. These two values can be found by finding out the time when the derivative of $\Delta V_{csmAB}(t)$ is equal to zero.

Substituting I_L by I_{dc} with relationship (2.13), the solution for $\frac{d\Delta V_{csmAB}(t)}{dt} = 0$ can be found as:

$$\frac{d\Delta V_{csmAB}(t)}{dt} = \frac{I_{dc}}{2C_{sm}}\left[-\frac{2}{m\cos\varphi}\sin(\omega t-\varphi-\theta)-m\sin(\omega t-\theta)-\frac{1}{\cos\varphi}\cos(2\omega t-\varphi-2\theta)\right] = 0 \tag{2.23}$$

Two periodical solutions, namely t_{Vmax} and t_{Vmin}, can be obtained by solving (2.23). At

the moment $t = t_{Vmax}$, $\Delta V_{csmAB}(t)$ reaches its maximum value $\Delta V_{csmAB}(t_{Vmax})$. Similarly, at the moment $t = t_{Vmin}$, $\Delta V_{csmAB}(t)$ reaches its minimum value $\Delta V_{csmAB}(t_{Vmin})$.

To regulate the SM capacitor voltage ripple under a certain percentage ($rippct\%$) of its average voltage value, (2.24) must be satisfied:

$$V_{rip} \leq rippct\% \overline{V_{csm}} \tag{2.24}$$

Manipulations of (2.22) and (2.16), (2.24) can lead to the size of SM capacitor C_{sm}:

$$\begin{aligned} C_{sm} \geq & \frac{3N}{4rippct\%V_{dc}} \left[\frac{2I_{dc}}{\omega m cos\varphi} (\cos(\omega t_{Vmax} - \varphi - \theta) - \cos(\omega t_{Vmin} - \varphi - \theta)) \right. \\ & + \frac{mI_{dc}}{\omega} (\cos(\omega t_{Vmax}) - \cos(\omega t_{Vmin})) \\ & \left. - \frac{I_{dc}}{2\omega \cos\varphi} (\sin(2\omega t_{Vmax} - \varphi - 2\theta) - \sin(2\omega t_{Vmin} - \varphi - 2\theta)) \right] \end{aligned} \tag{2.25}$$

SM capacitance is related to the converter's cost, size, and harmonic performance. Although (2.25) gives out a way to size the SM capacitor based on a voltage ripple percentage, this method is not accurate enough when designing converter to control the harmonics within a certain level. The impact of SM voltage ripple on current harmonics will be further demonstrated in section 2.3. After theoretically sizing the capacitance, EMT simulations are required to check the performance and finalize the design.

2.2.3 Valve inductor sizing

Similar to conventional MMCs, the valve inductor of SAMMC is responsible for absorbing voltage harmonics, suppressing current harmonics, and limiting DC fault current's rate of rise [33]. Since the DC deicer application is not a permanent load and is used under controlled conditions, this thesis will not discuss the fault condition and will focus on harmonics. While several papers have proposed the sizing of arm inductors for conventional MMCs [33], [34], the method of sizing SAMMC valve inductors is different. While in conventional MMCs

the arm inductor only contains even-numbered circulating current harmonics [35], all the harmonic components produced by the switching valve can be found in the valve inductor voltage and current of SAMMC.

To find out the relationship between harmonics level and valve inductor in SAMMC is not as direct as that of the conventional MMC. The reason is that, as shown in Figure 2.8, the AC harmonics' equivalent circuit of SAMMC is not a three-phase balanced circuit. The fundamental frequency resonant filter introduces an unbalanced impedance between valves AB and CA for harmonic currents. The method to calculate current harmonics will be discussed in section 2.3. Based on the current harmonics calculation model proposed in section 2.3, a proper valve inductor value can be chosen to achieve a certain current harmonics level.

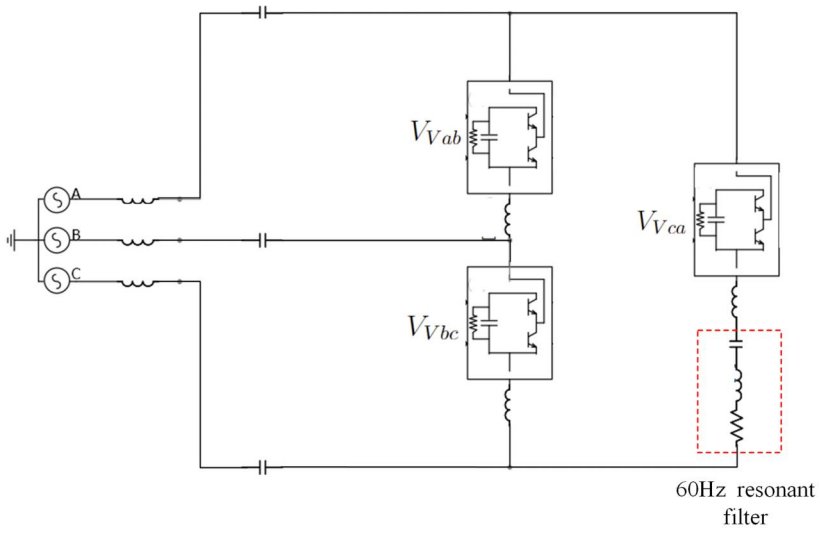

Figure 2.8: Unbalanced AC harmonics' equivalent circuit for SAMMC.

2.3 Current harmonics and their suppression

According to IEEE 519-2014 standard, the permissible THD level for a 120 V∼69 kV power system with a short circuit ratio of 20< I_{SC}/I_L <50 (I_{SC} is the maximum short-circuit current at PCC, I_L is the maximum demand load current) is 8%. When designing a SA-

MMC, a mathematical model used to estimate the current harmonics level is helpful to optimize the size of SM capacitors and valve inductors, in order to reduce the cost/size of the converter while controlling the current THD. Some previous studies have provided valuable methods for calculating the current harmonics and proposing solutions to suppress certain harmonic components for conventional MMCs [36], [37]. In a conventional MMC, each phase current is independent, and the current harmonics circulating in each arm can be found from the arm inductor's voltage. However, in the SA-MMC, the current harmonics flow is more complicated. Instead of circulating through the valve, the 2nd current harmonic (and other even-ordered current harmonics) leaves the valve string at AC terminals. Also, as stated before, the AC harmonics' equivalent circuit of SAMMC is not a three-phase balanced circuit, so the methods used to calculate a symmetrical power system cannot be used. This section introduces a mesh current-based iterative method to theoretically analyze current harmonics and a modified modulation method to reduce current harmonics.

2.3.1 Converter current harmonics calculation

As shown in Figure 2.8, the circuit of SAMMC is not symmetrical when studying harmonic currents. So instead of converting three-phase calculations into single phase calculations (which is a general approach for balanced three phase circuits), the mesh current method [38] is used to solve this circuit.

In the AC circuit shown in Figure 2.8, when the SAMMC rectifier is connected to an ideal AC power system with a transformer (which is represented as a series equivalent reactor), the fundamental current is the response of AC power system and the fundamental component of valve voltages, while an n-th order current harmonics is the response of n-th order component of valve voltage. The final result of current can be regarded as the summation of fundamental current component and harmonics components. By applying the superposition theorem, the AC circuit can be decoupled into a series of sub-circuits containing only one particular frequency component, as shown in Figure 2.9 and Figure 2.10.

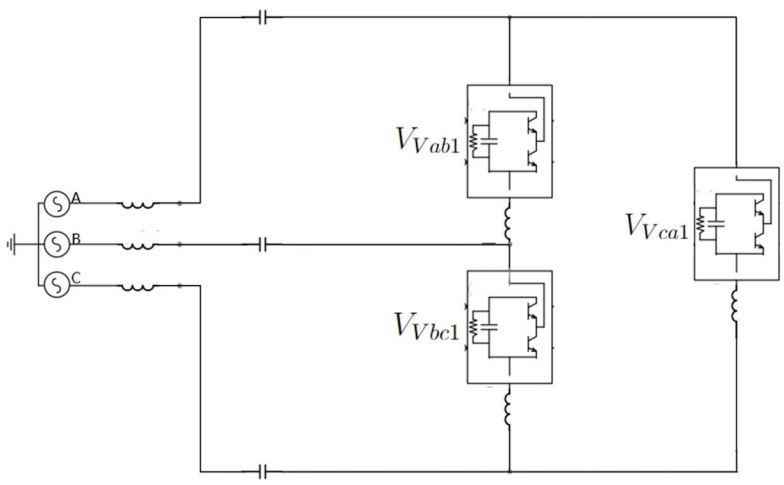

Figure 2.9: Fundamental current response equivalent circuit.

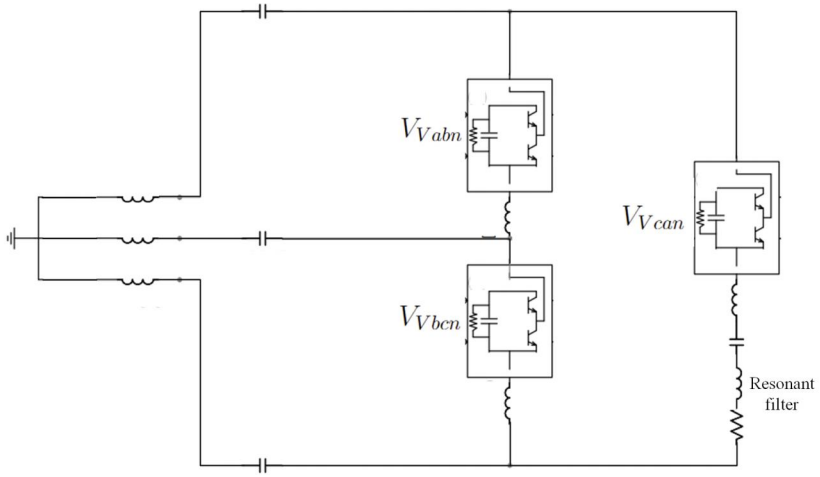

Figure 2.10: n-th harmonic current response equivalent circuit.

Figure 2.9 is the AC equivalent circuit of the fundamental frequency component, AC power system is a 60Hz ideal voltage source, and V_{Vab1}, V_{Vbc1}, V_{Vca1} are the fundamental frequency component of valve voltages. Figure 2.10 is the sub-circuit for any n-th order harmonic component. The AC power system is shorted as its voltage contains no harmonics component ideally, and V_{Vabn}, V_{Vbcn}, V_{Vcan} are the n-th order components in voltage V_{Vab},

V_{Vbc}, V_{Vca}.

To solve the harmonic current sub-circuits, three valve voltages and each frequency component of them need to be calculated. From (2.4), the valve voltage is decided by the average SM capacitor voltage in the valve and the modulation waveform. Moreover, the steady state average SM capacitor voltage is decided by the current flowing through the valve, can be described as:

$$\Delta Vcsm_k(t) = \frac{1}{NC_{sm}} \int_0^t N \cdot wv_k(t) \cdot i_k(t)\, dt \tag{2.26}$$

where k is the notation of each arm AB, BC, CA. From (2.3), $wv_{ab}(t)$, $wv_{bc}(t)$ and $wv_{ca}(t)$ are the modulation waveforms for three valves.

After obtaining the expression of the valve voltage, a certain current harmonic with the corresponding valve voltage component in the sub-circuit can be calculated using the mesh current method. The diagram for calculating n-th harmonic is shown in Figure A.3.

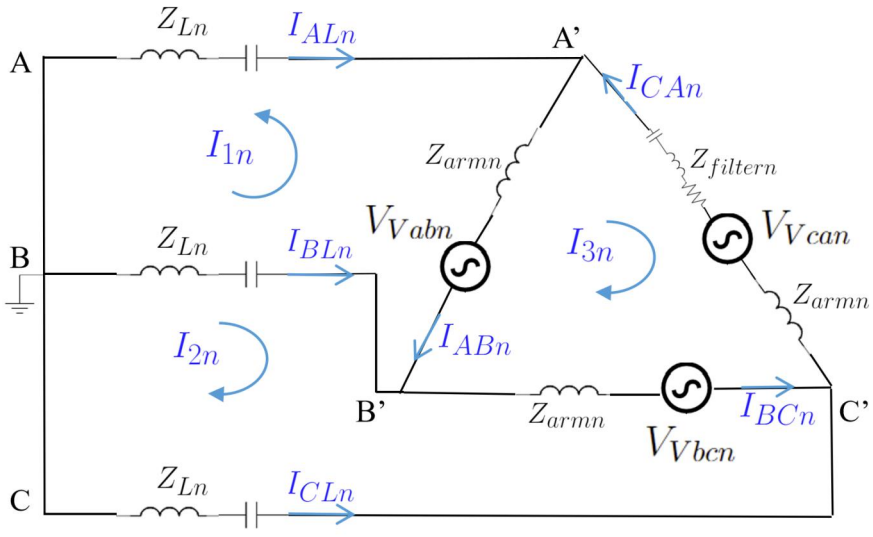

Figure 2.11: Mesh current diagram for the n-th order current equivalent circuit.

In this figure, Z_{Ln} is the impedance of transformer and AC capacitor for n-th order current; Z_{armn} is the impedance of valve inductor for n-th order current; $Z_{filtern}$ is the impedance of resonant filter for n-th order current. I_{1n}, I_{2n} and I_{3n} is the mesh current for the three meshes in the circuit. Three line current I_{ALn}, I_{BLn} and I_{CLn} are three line currents

which can be denoted as $-I_{1n}$, $I_{1n} + I_{2n}$ and $-I_{2n}$; and three arm currents I_{ABn}, I_{BCn} and I_{CAn} can be denoted as $-I_{1n} - I_{3n}$, $I_{2n} - I_{3n}$ and $-I_{3n}$.

The mesh current method is based on Kirchhoff's Voltage Law (KVL) and superposition theorem [38]. The circuit topology is divided into a few fundamental loops. The KVL equation for three loops in Figure A.3 is shown below:

$$\begin{aligned} &I_{1n} \cdot (2Z_{Ln} + Z_{armn}) + I_{2n}Z_{Ln} + I_{3n}Z_{armn} = V_{Vabn} \\ &I_{2n} \cdot (2Z_{Ln} + Z_{armn}) + I_{1n}Z_{Ln} - I_{3n}Z_{armn} = -V_{Vbcn} \\ &I_{3n} \cdot (3Z_{Ln} + Z_{filtern}) + I_{1n}Z_{armn} - I_{2n}Z_{armn} = V_{Vabn} + V_{Vbcn} + V_{Vcan} \end{aligned} \tag{2.27}$$

The n-th order current harmonic can be calculated by solving (A.2).

In summary, the current harmonic results are derived from valve voltage expressions. And valve voltages are obtained by valve currents $i_k(t)$ and modulation waveforms $wv_k(t)$ $(K = ab, bc, ca)$ (2.4) (A.1). However, the full expression of valve currents $i_k(t)$ is not known from the beginning of the calculation procedure, since we do not know their harmonics components.

The full expression of valve current $i_k(t)$ and V_{Vkn} with DC, fundamental components and harmonics can be obtained by an iterative method. Iterative method is used to solve functions with fixed-points. In mathematics, a function with a fixed point is a function by which independent variable can be mapped back to itself by the function. This kind of function can be described as $f(c) = c$. The equations and descriptions from (A.11) to (A.14) in Appendix A show how to fit the current harmonics problem into a fixed-point function problem.

The iterative method for solving the fixed-point function $g(x)$ is shown below. The DC and fundamental components of valve current (i_{k0}+i_{k1}) are selected as initial values for the iteration i_k^0. Then the result of $g(i_k^0) = i_k^1$ is selected as the independent variable for the next round of calculation. The results will converge gradually, and when the error $i_k^k - i_k^{k-1}$ becomes smaller than a certain threshold, the iterative procedure is stopped. The numerical

description for this iterative method is as follows:

$i_k^1 = g(i_k^0)$

$i_k^2 = g(i_k^1)$

$i_k^3 = g(i_k^2)$

.....

$i_k^k - i_k^{k-1} < err$

A fully detailed illustration about the mathematical model and implementation of this iterative harmonics calculation algorithm is demonstrated in Appendix A.

2.3.2 Validation of iterative SAMMC harmonics calculation method

A system-scale EMT testing model is built in RSCAD to compare the output current harmonics simulation results with the proposed mathematical model results, in order to validate this iterative converter harmonics calculation method. Comparisons of simulation result and calculation result of harmonics magnitude under five different operation states are shown with plots, the convergence of iterative method is also shown in another figure to demonstrate how iterative method helps to make the calculation results more accurate.

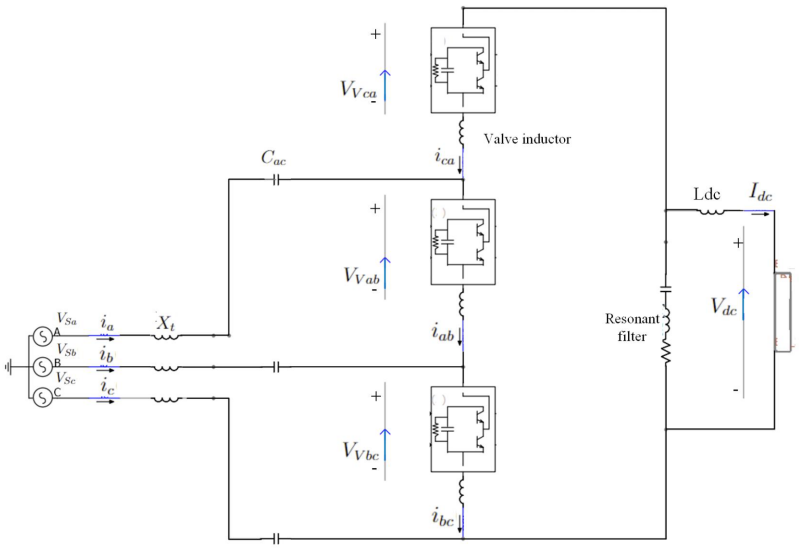

Figure 2.12: Harmonics testing system diagram

The diagram of the testing model is shown in Figure 2.12. The peripheral system is: AC power system is set to be 2 kV (L-L RMS value) at 60 Hz, the transformers equivalent leakage reactance is 0.85 mH. The converter parameter setting is as below: the AC side capacitor is 100 mF, number of SM per valve is 10, valve inductor is 0.5 mH and SM capacitor is 80 mF, the resonant filter is consists of a 1.04 mH inductor and a 6.76 mF capacitor, and a resistive load 4.8 Ω is connected to the SAMMC DC side. A PI controller controlling the phase angle of the modulation index is deployed to set the system to different operation points. Figure 2.13 snapshot of this testing model from RCSAD graphical interface.

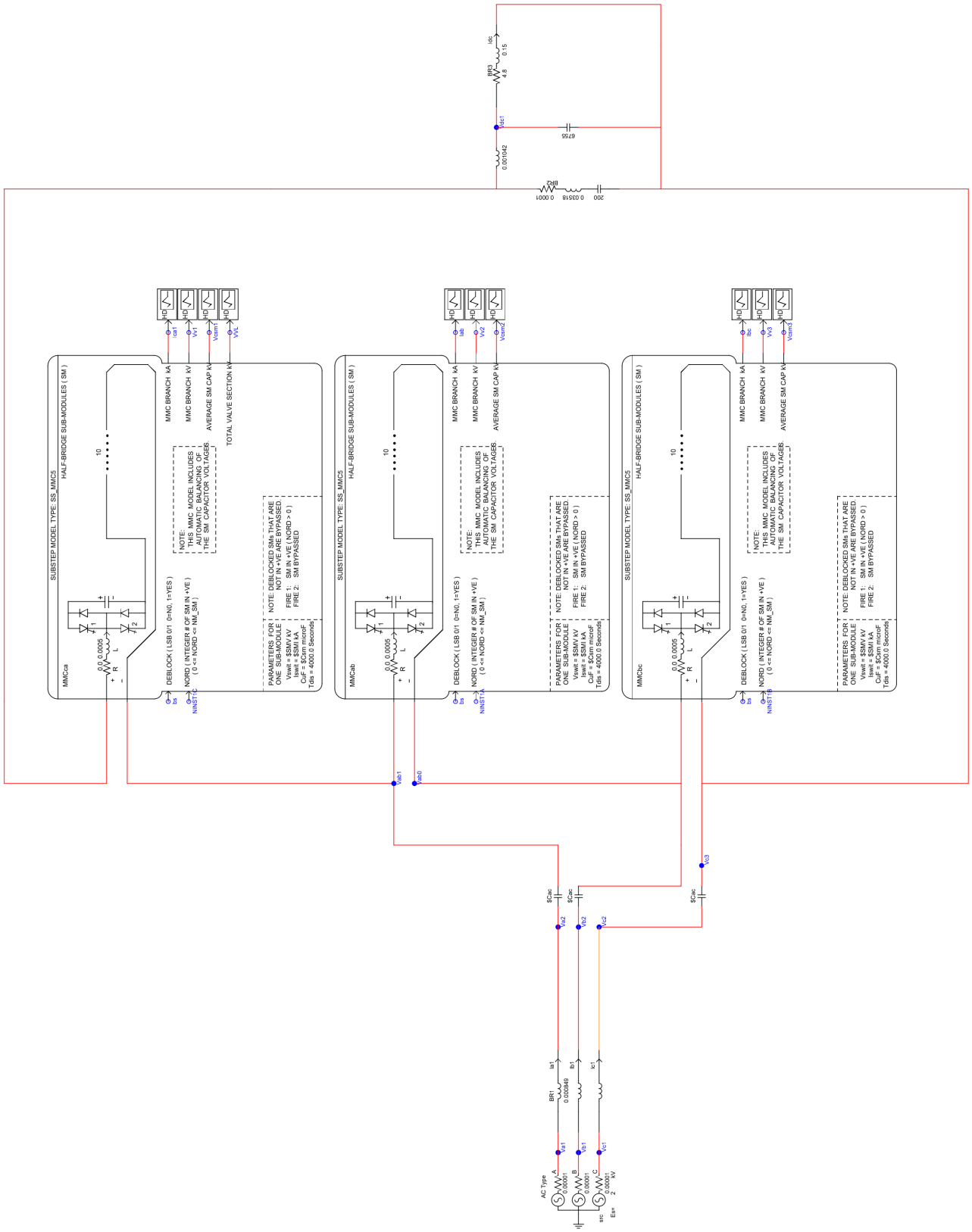

Figure 2.13: SAMMC harmonic testing setup in RSCAD, (Cac=100mF, Csm=80mF)

Five different simulation results at different operation points are recorded. The five different steady-state operation scenarios are listed in the table below:

Table 2.1: Key values for five operation points.

No. of Scenario	V_S (L-L,RMS)/kV	I_L (Line,RMS) /kA	I_{dc} /kA	θ/degree	φ/degree
1	2	2.8	1	51	60
2	2	2.6	0.8	37.8	68.6
3	2	2.61	0.6	26.8	79.93
4	2	3.5	1.2	70.9	56.1
5	2	2.85	0.4	16.94	86.2

In Table 2.1, θ denotes the angle by which the power system phase A voltage leads the modulation waveform wv_{ab}, and φ denotes the angle by which converter output line voltage leads converter output line currents.

To validate the proposed harmonics calculation method, this thesis compares three line current 2nd harmonic simulation results ($I_{A2^{nd}s}, I_{B2^{nd}s}, I_{C2^{nd}s}$) with three line current 2nd harmonic calculation results ($I_{A2^{nd}c}, I_{B2^{nd}c}, I_{C2^{nd}c}$). Figure 2.15 shows the theoretical results and simulation result comparison for line current 2nd harmonics in five different operation states.

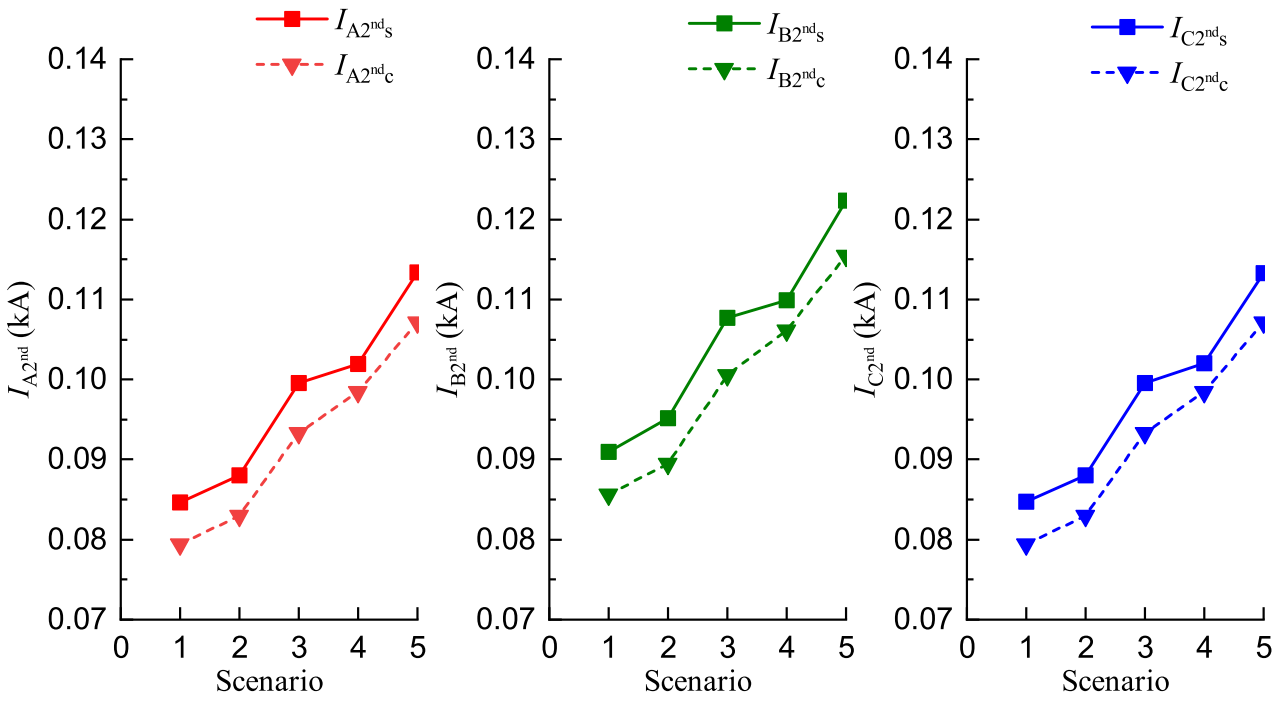

Figure 2.14: Theoretical results and simulation result comparison for line current 2nd harmonics in five different operation states

As shown in Figure 2.14, both simulation results and theoretical results show that the 2nd current harmonic in Phase B current is higher than the other two Phases, which confirms the statement that the SAMMC harmonics circuit is not three-phase balanced due to the impact of resonant filter. For the data of each scenario, the calculation results follows simulation results with some small error. These errors mainly come from two reasons: firstly, the number of inserted SM waveform is simplified to a sinusoidal waveform; secondly, higher level harmonics are ignored to reduce the computation cost.

Similarly, three line current 3rd harmonic simulation results ($I_{A3^{rd}s}, I_{B3^{rd}s}, I_{C3^{rd}s}$) with three line current 3rd harmonic calculation results ($I_{A3^{rd}c}, I_{B3^{rd}c}, I_{C3^{rd}c}$) are plotted in Figure 2.16.

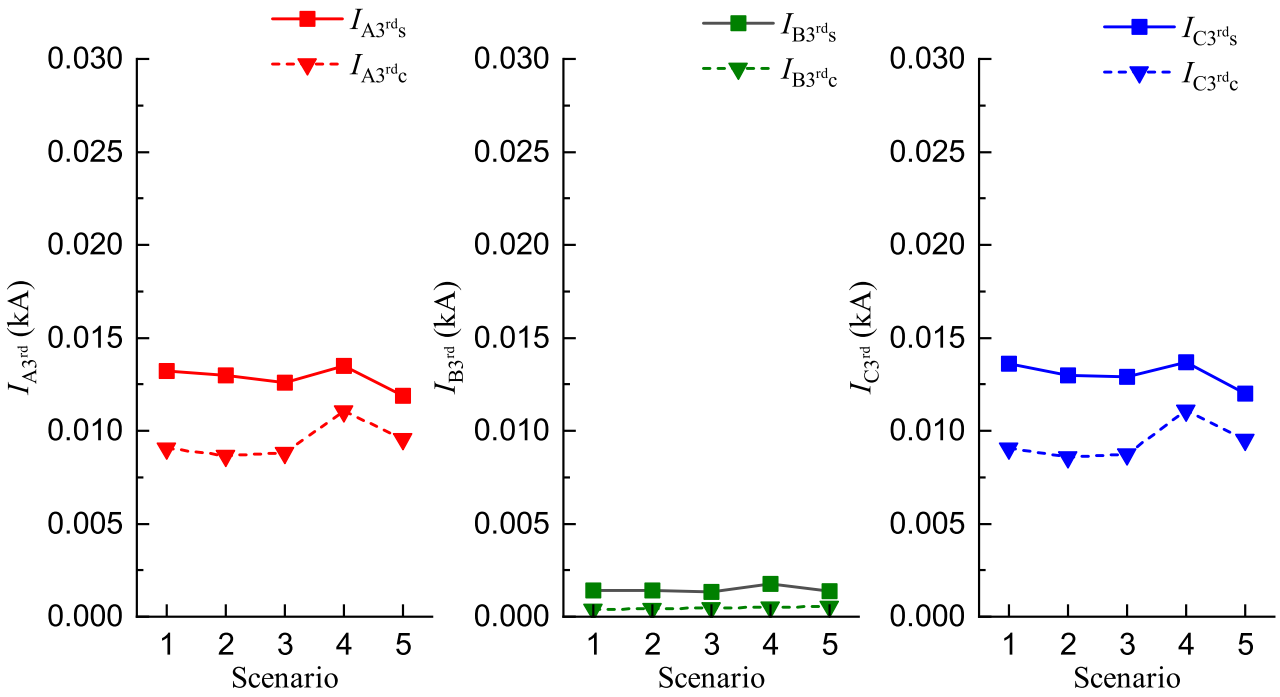

Figure 2.15: Theoretical results and simulation result comparison for line current 3rd harmonics in five different operation states

Figure 2.15 shows that phase A and phase C's third current harmonics are approximately the same, while phase B's third current harmonic is a very negligible value. This is again due to the unbalanced circuit. The reason for errors between calculation value and simulation value remains the same with 2nd harmonic.

To show the iterative method in a more intuitive way, Figure 2.16 shows the calculation result of Scenario 3's second current harmonic in each iteration.

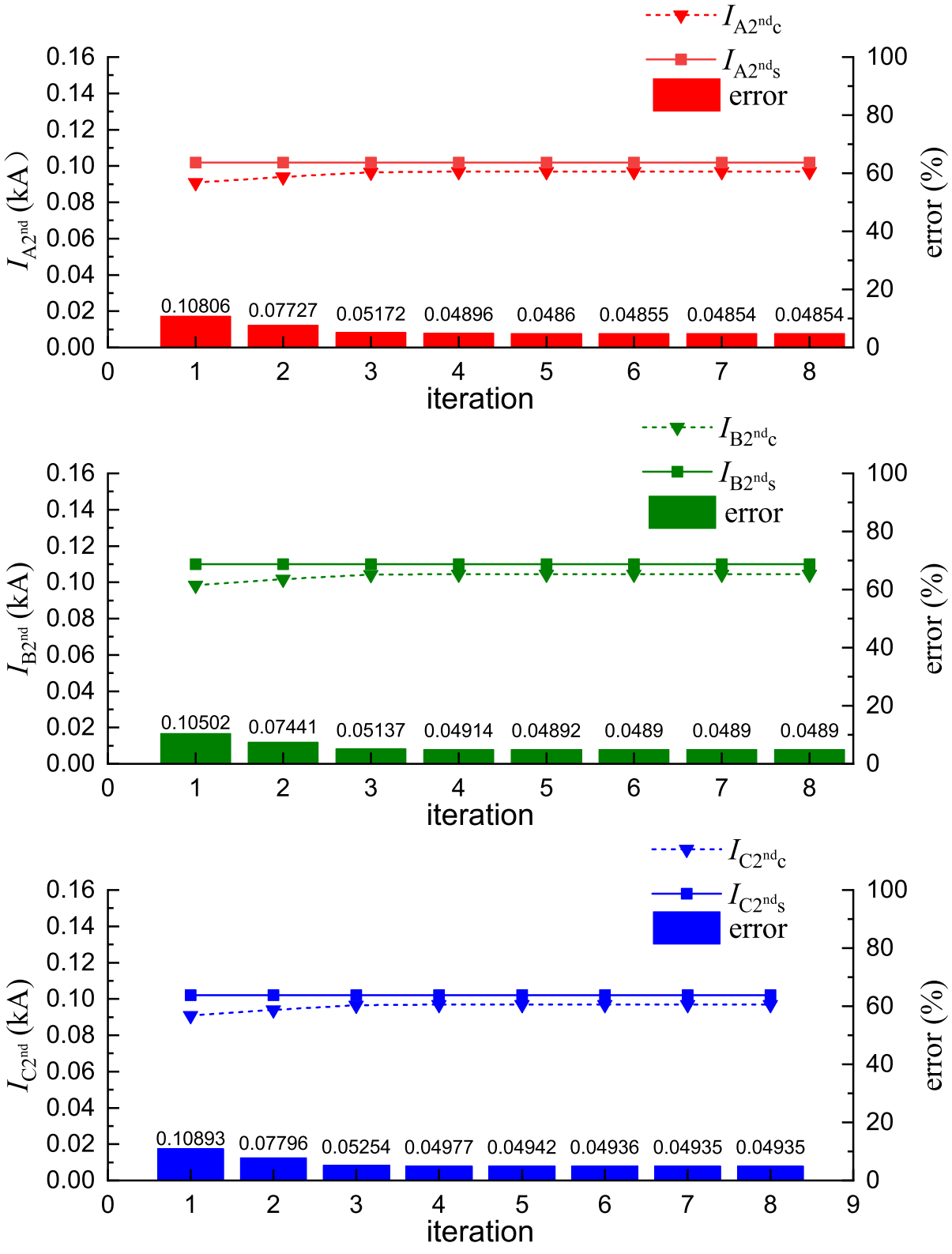

Figure 2.16: Convergence of three-phase second current harmonic in Scenario 3

The solid line is the simulation value results, and the dashed line is the calculation results from each iteration. A histogram is used to show the error between simulation results and calculation results. The errors for the calculation results at the first iteration are over 10%, then gradually reduced to less than 5%, and finally converge at the 7th iteration.

In conclusion, the proposed harmonics calculation method is tested with five different scenarios and give out convincing results. The iterative method effectively improved the accuracy of calculation results.

2.3.3 2nd current harmonic suppression controller

The current harmonics mainly consist of 2nd harmonic. If a way to eliminate 2nd harmonics from output current can be found, designers can use smaller SM capacitors to achieve the required current THD standard thus the size and cost of the SAMMC rectifier can be significantly reduced. This section will design a 2nd harmonic suppression controller based on the harmonics mathematical model proposed in the previous section and validate this controller in RSCAD EMT simulation.

The design of 2nd current harmonic suppression controller

From the previous section, it has been confirmed that the SAMMC converter's current harmonics are the response of valve voltage harmonics. The most significant magnitude of current harmonic is the 2nd harmonic. So, removing the 2nd harmonic from the output current can be an effective method to reduce the output current harmonics without increasing the SM capacitor size.

Since SAMMC is a variant of MMC converter, some performance is similar for both topologies. In conventional MMC topology, there exists methods to eliminate the 2nd harmonic current circulating in the MMC arms, the most commonly adopted one is 2nd harmonic injection method [39]. The principle of this 2nd harmonic injection method can be described as, by injecting a certain amount of 2nd order signal in the modulation waveform, the 2nd

order circulating current can be controlled to the desired value (normally zero) [37]. To obtain the exact amount of 2nd order signal, a Circulating Current Suppression Controller (CCSC) is designed. In CCSC controller, a PI controller is used to produce the 2nd order signal from the error of 2nd order current, while the 2nd order current is obtained simply by adding the current both upper arm and lower arm current. Figure 2.17 is a diagram showing CCSC controller for conventional MMC converter.

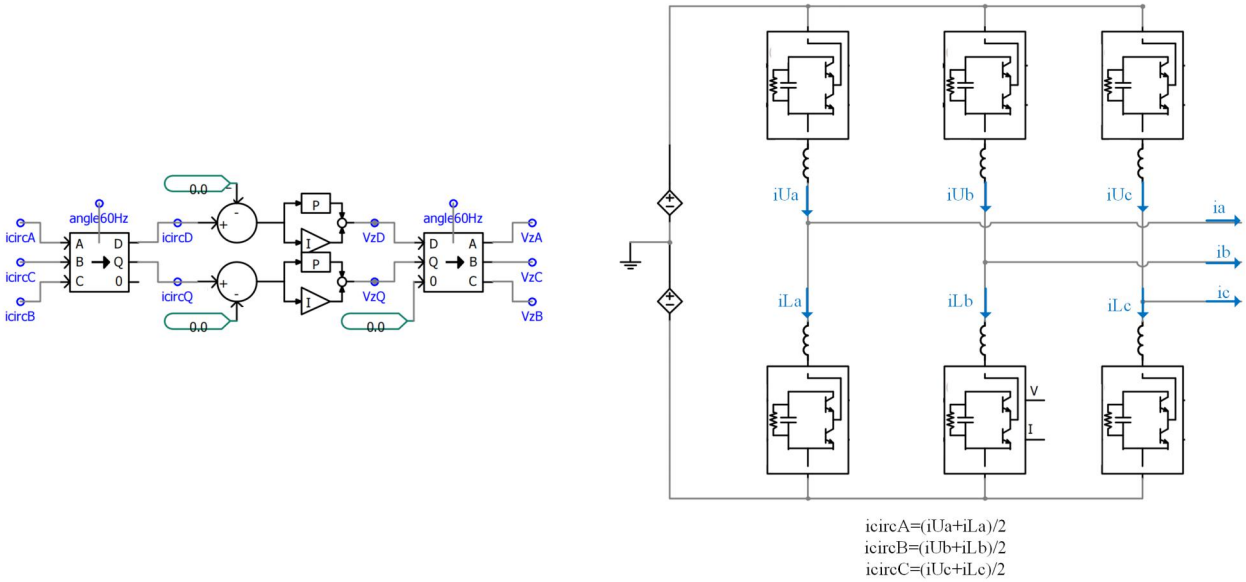

Figure 2.17: CCSC controller for a conventional MMC

However, this CCSC controller cannot be deployed on the SAMMC converter. The reason is that in the SAMMC converter the 2nd order currents leave the converter from AC terminals instead of circulating in the valve string, so the 2nd order current cannot be obtained by simply adding currents of two valves. Although the CCSC controller cannot be directly used to control SAMMC, it inspires the design of the 2nd harmonic current suppression controller (2HCSC) for the SAMMC converter. To design 2HCSC, two problems need to be solved: 1. Whether the 2nd current harmonic in SAMMC can be controlled by adding a 2nd order signal to the modulation waveform, and 2. If such a 2nd order signal exists, how to obtain the 2nd order signal.

Problem 1 can be solved by the current harmonics mathematical model proposed in

Appendix A. In Appendix A, it has already been validated that the 2nd current harmonic is the response of 2nd component of valve voltage. Equation 2.28 shows that the 2nd current harmonic can be obtained by a linear transformation of 2nd component of valve voltage.

$$\mathbf{IL}_2 = \mathbf{CL} \cdot \mathbf{Z}_2^{-1} \cdot \mathbf{CV} \cdot \mathbf{Vv}_2 \tag{2.28}$$

where $\mathbf{IL}_2$ is the vector of three phase 2nd current harmonics, $\mathbf{CL}, \mathbf{Z}_2, \mathbf{CV}$ are coefficient matrix proposed in Appendix A. $\mathbf{Vv}_2$ is the valve voltage vector for 2nd voltage component.

In order to find out a 2nd order signal V_z to control 2nd current harmonics, this procedure can be done by finding a V_z to eliminate the 2nd component of valve voltage. If the 2nd order harmonic can be removed from valve voltage, the 2nd order harmonic current will be eliminated.

First, a mathematical solution will be used to find out if the 2nd current harmonic in SAMMC can be controlled by adding a 2nd order signal to the modulation waveform. By adding a three phase balanced 2nd order signal to the modulation waveform, the modulation index changes from (2.3) into the new one (2.29):

$$\begin{aligned}
wv'_{ab}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta) - V_z \sin(2\omega t + \theta_z)) \\
wv'_{bc}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta - \frac{2\pi}{3}) - V_z \sin(2\omega t + \theta_z + \frac{2\pi}{3})) \\
wv'_{ca}(t) &= \frac{1}{2}(1 + m\sin(\omega t - \theta + \frac{2\pi}{3}) - V_z \sin(2\omega t + \theta_z - \frac{2\pi}{3}))
\end{aligned} \tag{2.29}$$

Combined with (2.4) and (2.19), the expression for valve voltage with the 2nd order signal Vz can be obtained. Take valve AB for example, the valve voltage is as (2.30):

$$\begin{aligned}
V'_{Vab}(t) &= Nwv'_{ab}(t)V_{csmAB}(t) \\
&= Nwv'_{ab}(t)(\frac{2V_{dc}}{3N} + \Delta V_{csmAB}(t)) \\
&= Nwv'_{ab}(t)(\frac{2V_{dc}}{3N} + \frac{1}{NC_{sm}}\int_0^t Nwv'_{ab}(t) \cdot i_{ab}(t)\, dt)
\end{aligned} \tag{2.30}$$

Since V_z is a very small signal compared with modulation index, (2.30) can be approximately expressed as:

$$\begin{aligned} V_{Vab}^{'}(t) &= Nwv_{ab}^{'}(t)(\frac{2V_{dc}}{3N} + \frac{1}{NC_{sm}}\int_0^t Nwv_{ab}^{'}(t)\cdot i_{ab}(t)\,dt) \\ &\approx Nwv_{ab}^{'}(t)(\frac{2V_{dc}}{3N} + \frac{1}{NC_{sm}}\int_0^t Nwv_{ab}(t)\cdot i_{ab}(t)\,dt) \end{aligned} \tag{2.31}$$

Extract the 2nd component from (2.31) and let the 2nd voltage component equal to zero:

$$\begin{aligned} &\frac{N}{4C_{sm}}\left(-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta) - \frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1}) + \frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\right) \\ &+\frac{Nm}{4C_{sm}}\left(-\frac{I_L}{\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta) + \frac{mI_{dc}}{2\omega}\sin(2\omega t-2\theta) + \frac{I_{3rd1}}{6\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\right. \\ &\left.-\frac{mI_{2nd1}}{4\omega}\cos(2\omega t+\theta_{2nd1}) - \frac{mI_{2nd1}}{12\omega}\cos(2\omega t+\theta_{2nd1})\right) - \frac{2V_{dc}}{3N}V_{z1}\sin(2\omega t+\theta_{z1}) = 0 \end{aligned} \tag{2.32}$$

Obviously, the 2nd order signal injected to valve AB modulation waveform to achieve zero 2nd component is:

$$\begin{aligned} V_{z1}\sin(2\omega t+\theta_{z1}) =& \frac{3N^2}{8V_{dc}C_{sm}}\left(-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta) - \frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1})\right. \\ &\left.+\frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\right) + \frac{3mN^2}{8V_{dc}C_{sm}}\left(-\frac{I_L}{\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta)\right. \\ &+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\theta) + \frac{I_{3rd1}}{6\omega}\sin(2\omega t+\theta_{3rd1}+\theta) \\ &\left.-\frac{mI_{2nd1}}{4\omega}\cos(2\omega t+\theta_{2nd1}) - \frac{mI_{2nd1}}{12\omega}\cos(2\omega t+\theta_{2nd1})\right) \end{aligned} \tag{2.33}$$

Similarly, the 2nd order signals injected to valve BC, CA modulation waveform to achieve

zero 2nd component are:

$$
\begin{aligned}
V_{z2}sin(2\omega t+\theta_{z2}) =& \frac{3N^2}{8V_{dc}C_{sm}}\left(-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta)-\frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1})\right.\\
&\left.+\frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\right)+\frac{3mN^2}{8V_{dc}C_{sm}}\left(-\frac{I_L}{\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta)\right.\\
&+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\theta)+\frac{I_{3rd1}}{6\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\\
&\left.-\frac{mI_{2nd1}}{4\omega}\cos(2\omega t+\theta_{2nd1})-\frac{mI_{2nd1}}{12\omega}\cos(2\omega t+\theta_{2nd1})\right)\\
V_{z3}\sin(2\omega t+\theta_{z3}) =& \frac{3N^2}{8V_{dc}C_{sm}}\left(-\frac{mI_L}{2\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta)-\frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1})\right.\\
&\left.+\frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\right)+\frac{3mN^2}{8V_{dc}C_{sm}}\left(-\frac{I_L}{\sqrt{6}\omega}\sin(2\omega t+\varphi-2\theta)\right.\\
&+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\theta)+\frac{I_{3rd1}}{6\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\\
&\left.-\frac{mI_{2nd1}}{4\omega}\cos(2\omega t+\theta_{2nd1})-\frac{mI_{2nd1}}{12\omega}\cos(2\omega t+\theta_{2nd1})\right)
\end{aligned}
\tag{2.34}
$$

From equation (2.33) and (2.34), it is clear that, theoretically, there exists such 2nd order signals to remove 2nd current harmonics. The next step is to design a controller to inject these 2nd order signals into modulation waveforms. Although it is possible to theoretically calculate the V_z signal and have it injected into modulation waveform, the high computational cost and calculation error may compromise the performance of 2HCSC controller. So a more practical approach is to deploy a PI controller to produce V_z signal.

Similar to the CCSC controller used in conventional MMCs, for SAMMC, the errors of current 2nd harmonics or 2nd component voltage is the ideal input for the controller. As stated before, the 2nd current harmonics in SAMMC are not circulating in the valve arm, so it is not easy to obtain 2nd valve current directly. This thesis used DQ transformation and filters to obtain the 2nd component from valve voltages.

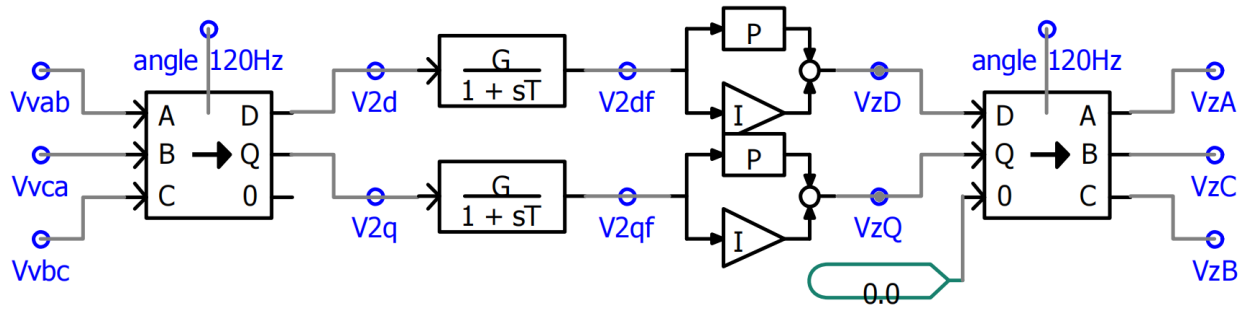

Figure 2.18: Diagram of 2HCSC controller.

Figure 2.18 is the diagram of the 2nd harmonic current suppression controller (2HCSC). DQ0 transformation is applied to three valve voltages in negative sequence V_{Vab}, V_{Vca} and V_{Vbc} with a 120Hz rotating angle. The result of the DQ0 transformation, denoted as V_{2d} and V_{2q}, contains a DC component representing the 2nd order component and other AC ripples representing other frequency components. A filter with a long enough time constant can get the DC components of V_{2d} and V_{2q}, as V_{2df} and V_{2qf}. V_{2df} and V_{2qf} are the projection of valve voltage 2nd order component on the d q axis, respectively. V_{2df} and V_{2qf} are the input of PI controllers to generate a proper V_{zD} and V_{zQ} to make V_{2df} and V_{2qf} to be zero. V_{zD} and V_{zQ} are transformed back to ABC domain with the same 120Hz rotating angle, and V_{zA}, V_{zB}, V_{zC} are subtracted by the modulation waveform.

Validation of 2nd current harmonic current suppression controller

To validate the proposed 2HCSC controller, a EMT simulation case is developed in RSCAD. The setting of this testing system is listed as the table below:

Table 2.2: Parameters and operation state of 2HCSC testing system.

Parameter	Value	Unit
Power system voltage (L-L,RMS)	1.5	kV
Transformers leakage inductance	0.85	mH
AC side capacitor	100	mF
Number of SM per valve	10	-
Valve inductance	0.5	mH
SM capacitor	30	mF
Idc	0.8	kA

Figure 2.23 shows the comparison of output line current before and after 2HCSC is enabled. After 2HCSC is enabled, the THD of current is reduced from 6.46% to 1.3%. A similar comparion is also make for valve voltage.

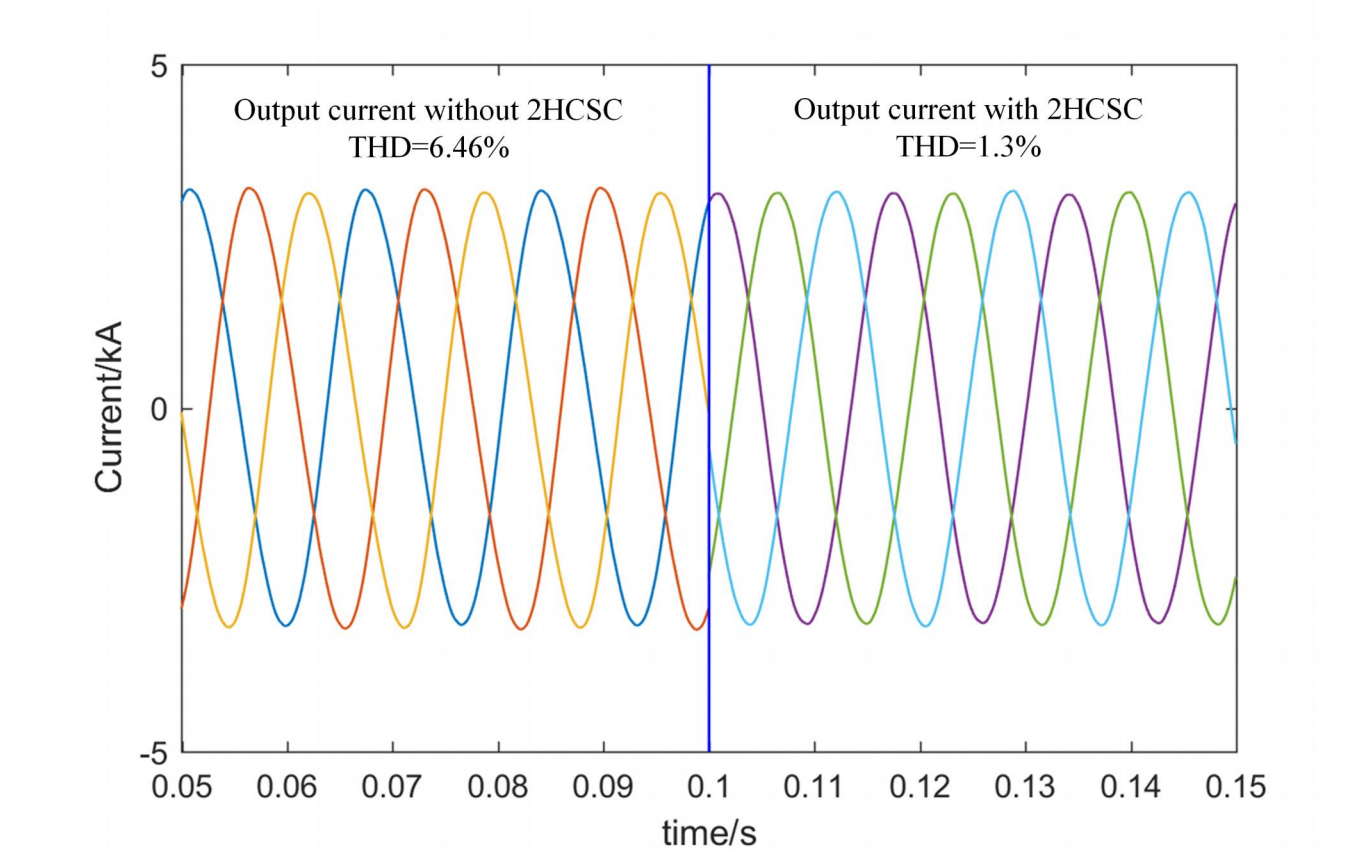

Figure 2.19: Output current with/ without 2HCSC.

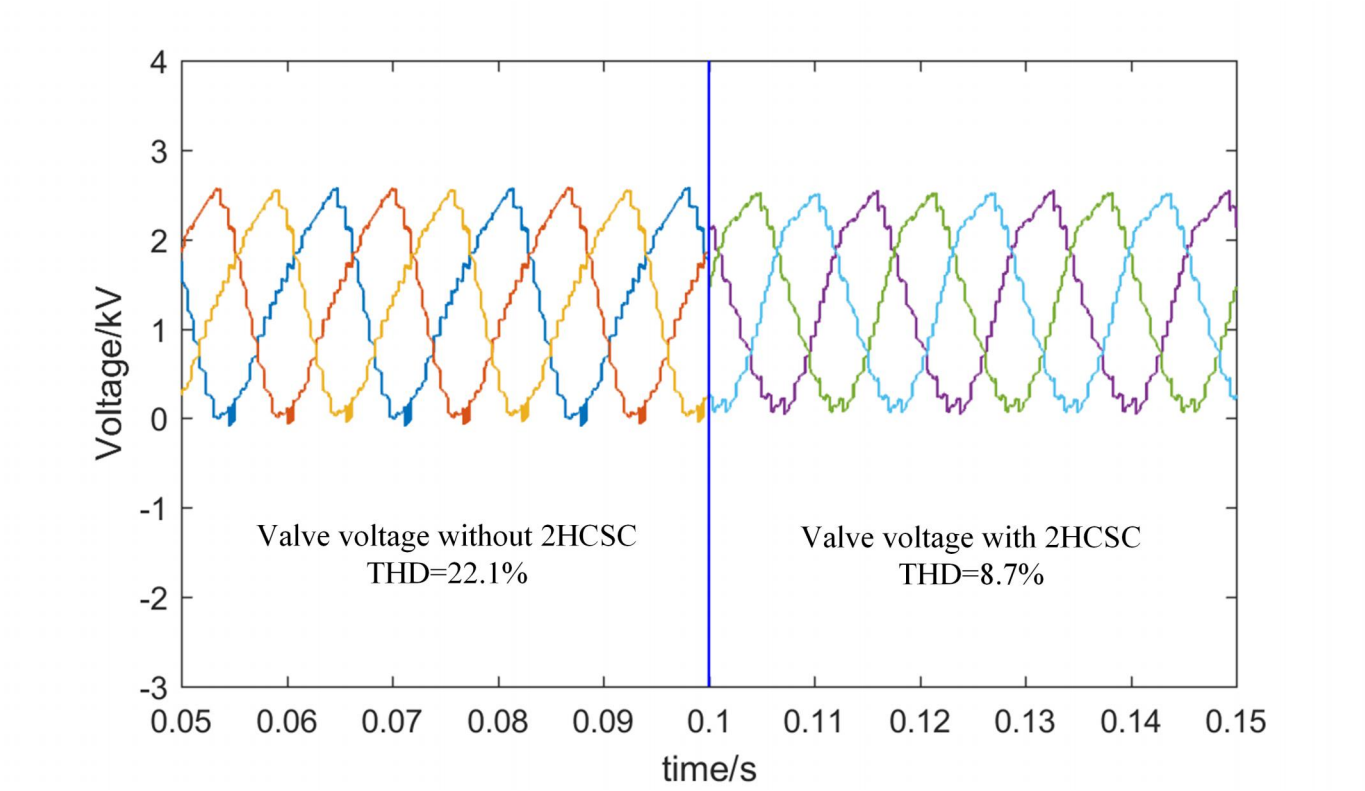

Figure 2.20: Valve voltage with/ without 2HCSC.

The harmonics spectrum of output currents can clearly illustrate how 2HCSC helps to reduce current harmonics.

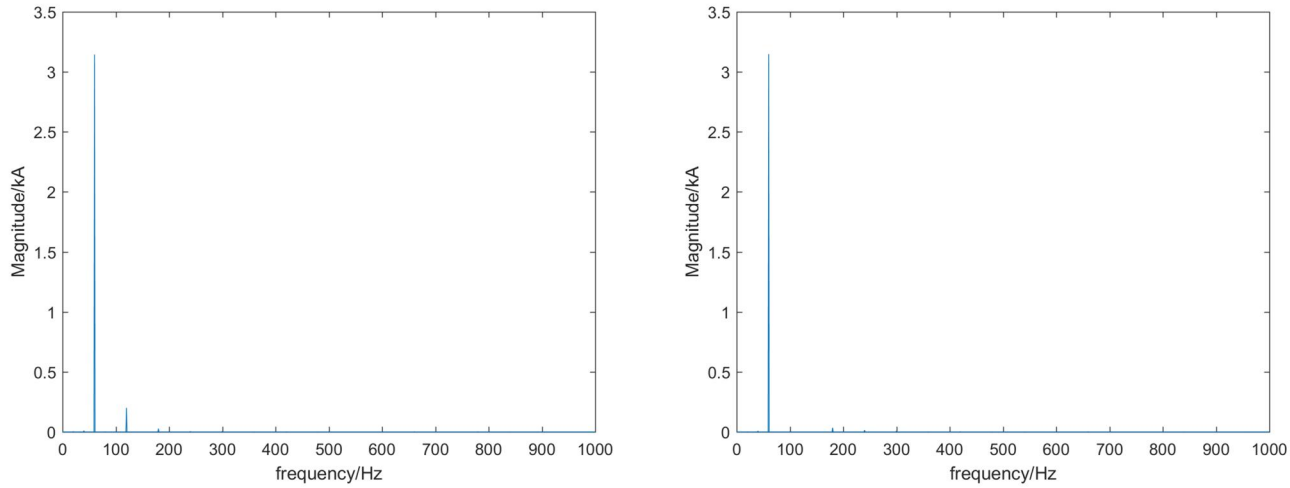

Figure 2.21: Output current harmonics spectrum without/ with 2HCSC.

On the left hand side is the harmonics spectrum of output current without 2HCSC, on

the right hand side is the harmonics spectrum of output current with 2HCSC enabled. The 2nd order current harmonics (120Hz component) is removed after 2HCSC is enabled, while the fundamental component is not affected by 2HCSC.

The injected 2nd order signal V_z is shown as Figure 2.22:

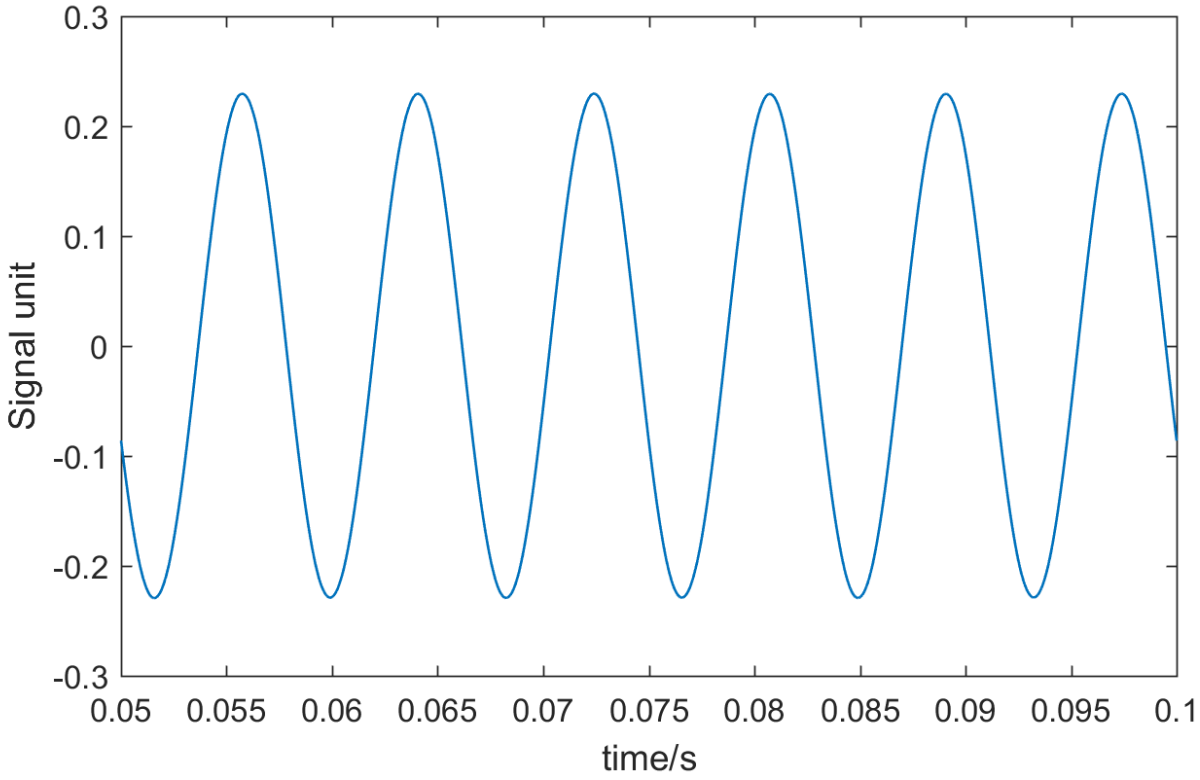

Figure 2.22: Injected 2nd order signal produced by 2HCSC.

Compared with modulation waveform index, the magnitude of signal V_z is much smaller than the magnitude of modulation index AC component (1 unit).

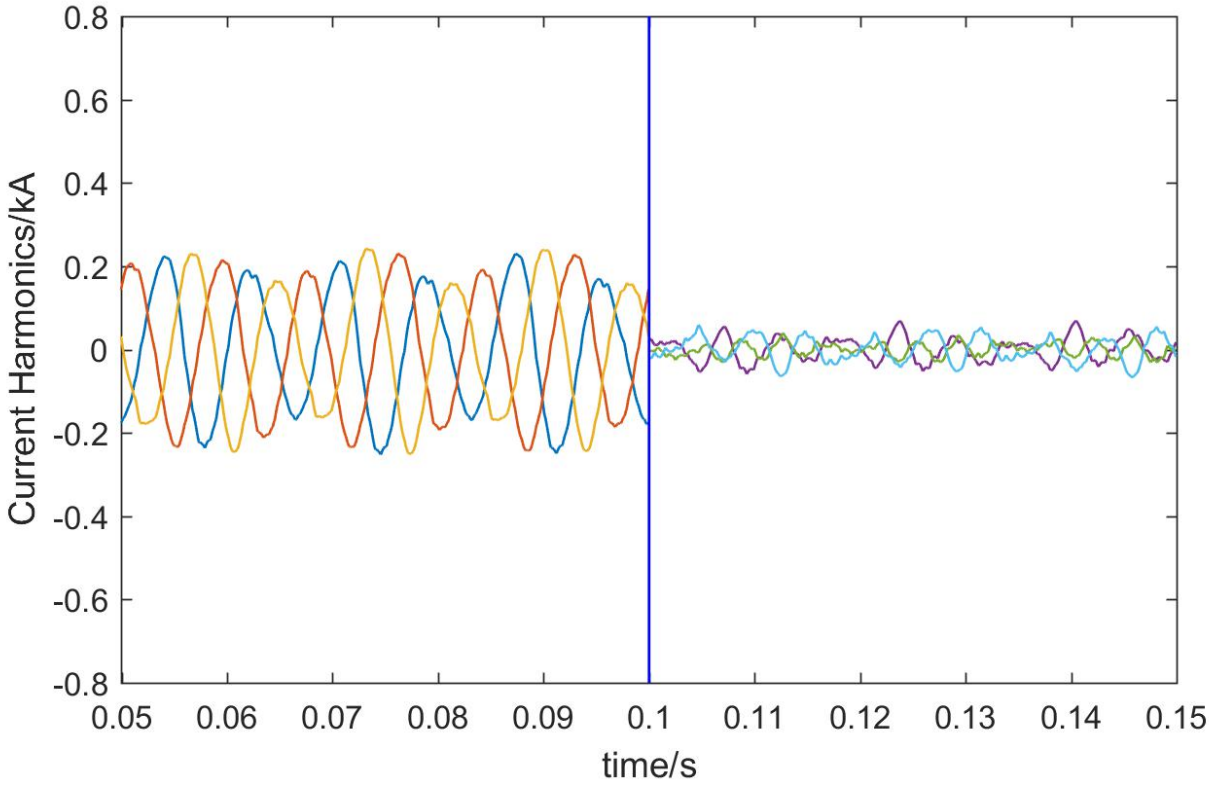

Figure 2.23: Current harmonics diagram 1.Without 2HCSC 2.With 2HCSC.

To show the result in a more direct way, the current harmonics are extracted from output current waveform. As shown in Figure 2.23, the 2nd component of output current is greatly reduced after 2HCSC is enabled.

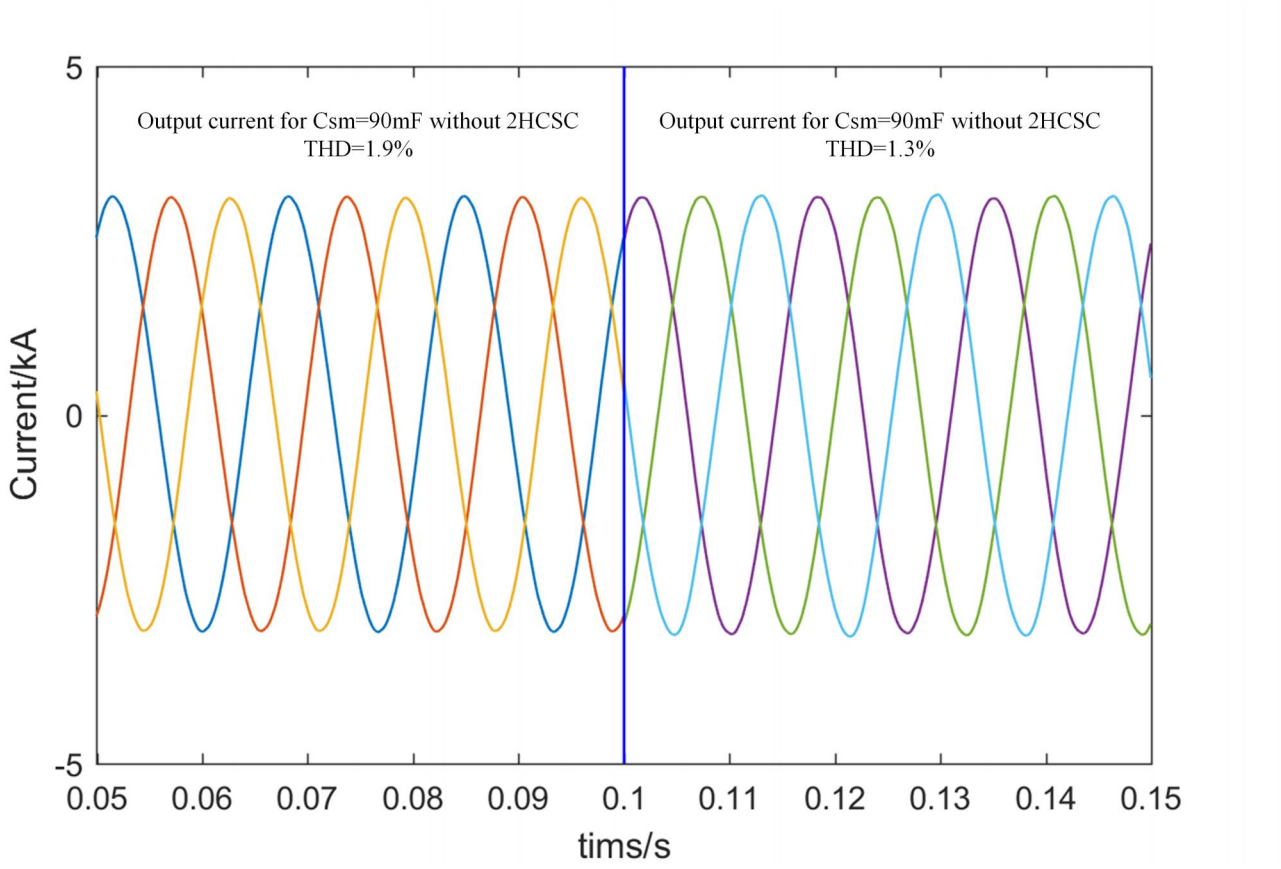

Figure 2.24: Output current comparison for 1.Csm=90mF without 2HCSC 2.Csm=30mF with 2HCSC.

The comparison of output current waveform of 30mF SM capacitor design with 2HCSC controller and the output current waveform of 90mF SM capacitor design without 2HCSC controller is shown in Figure 2.24. The design with 2HCSC controller has a much better current THD performance even if the SM capacitance is reduced by 2/3.

In conclusion, the deployment of 2HCSC can remove 2nd current harmonic. With 2HCSC, the SM capacitance can be reduced, so that the size and cost of the converter is reduced.

Chapter 3

Design of DC Deicer

After studying the ice melting procedure in Chapter 1 and SAMMC converter in Chapter 2, Chapter 3 design a SAMMC deicer working with 12.47 kV AC bus bar based on the previous studies. The design of SAMMC DC deicer includes the design of the converter, the design of AC transformers and the arrangement of frozen conductors. A mathematical model is developed to optimize the design to reduce the size and cost of the converter and improve the converter's performance. Two different approaches of the deicer design are proposed: the first design will use a larger transformer and the conductors to be melted are directly connected on SAMMC converter DC side; the second design uses a DC buck converter between the SAMMC converter and frozen conductors to step down the DC voltage so that a smaller transformer can be utilized. While both designs have advantages and disadvantages, this thesis will discuss the two designs and give out EMT simulation results in PSCAD simulator.

3.1 An overview of SAMMC based DC deicer design

A mobile SAMMC based DC deicer should consist of the following parts: a rectifier transformer, the SAMMC converter, control panel, insulators and connectors. Figure 3.1 is a diagram of this mobile SAMMC DC deicer.

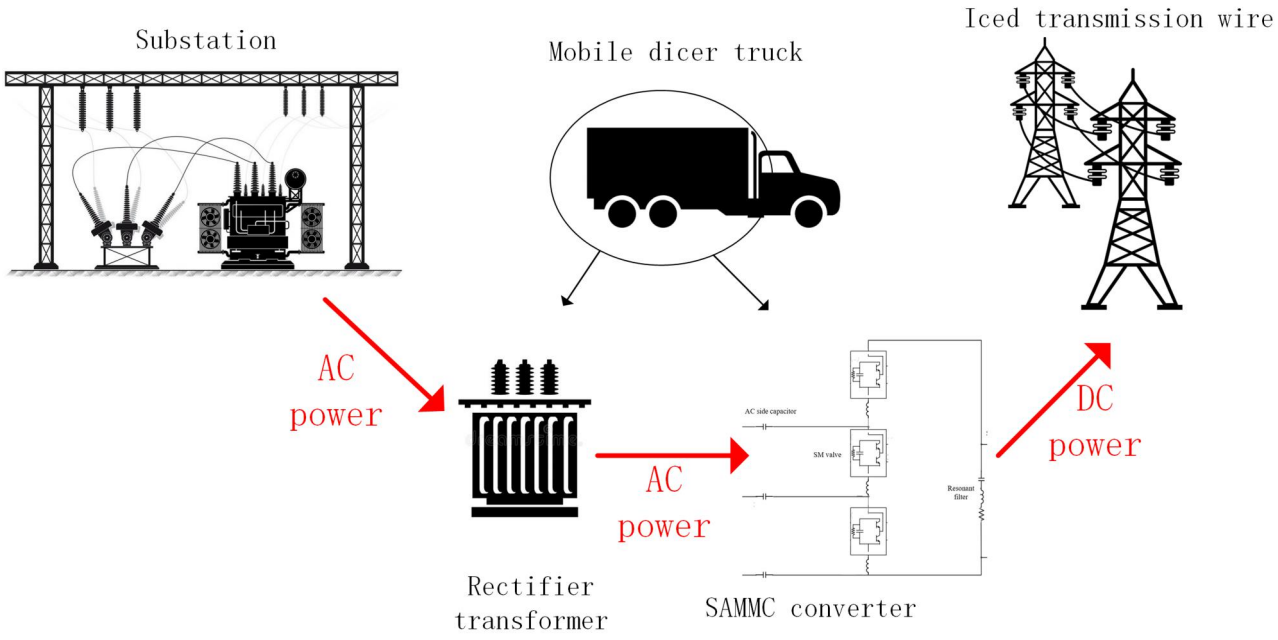

Figure 3.1: SAMMC based DC deicer diagram.

The transformer and SAMMC rectifier are loaded on a truck. When conducting the melting procedure, the transformer is connected to the AC power system, and SAMMC DC terminal is connected to the conductor to ne heated. The power flows from AC power system to the transformer, and converted into DC power in SAMMC to heat the transmission lines.

3.1.1 The choice of transformer

The rectifier transformer is a key component in this deicer system and should be chosen carefully. A delta-wye transformer should be used. Wye winding is connected to the AC power system side and delta winding is connected to the converter side to suppress 3rd current harmonics.

The voltage and MVA ratings of the transformer also need to be considered. While the primary side voltage is fixed at 66 kV, the secondary side voltage should match the converter's output AC voltage to reduce reactive power transmit from transformer to converter. The leakage reactance of the transformer is used to achieve a certain impedance between AC power system and SAMMC converter. If the reactance of the transformer is not enough,

additional reactors may be added in series. A larger reactance will help reduce the reactive power transmission, but will also limit the range of real power transmission. The transformer should have enough MVA rating to avoid core saturation.

3.1.2 Iced conductor arrangement scheme

The iced transmission line could have multiple wires, while only two terminals in SAMMC are available. Thus, arranging the wires and connecting them to two terminals is worth studying. Usually, the transmission line system includes three wires (phase A, B, and C) to carry power, and a ground wire to protect transmission lines from a lightning strike. Ideally, the four conductors can be arranged in series to fit the two DC terminals, such as shown in Figure 3.2.

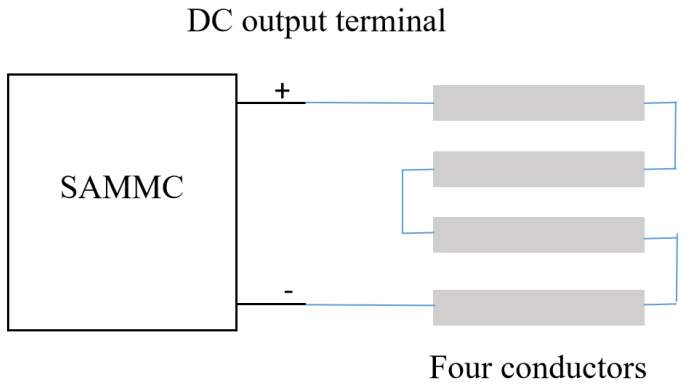

Figure 3.2: Ideal 4 conductors connection scheme.

However, nowadays, most ground wires use the OPGW (optical fiber composited overhead ground wire) technology. The OPGW ground wire has an optical fiber in it for communication purpose, and the optical fiber is very vulnerable to temperature rising [40]. So the ground wire cannot be melted with DC current unless a special wire called OPGW(M) is used in the transmission system [40]. Also, OPGW is often earthed by transmission tower [41], and hence the insulation must be modified before applying voltage. So this thesis will not consider the ground wire in the melting process. In conclusion, three conductors need to be connected on

two DC terminals.

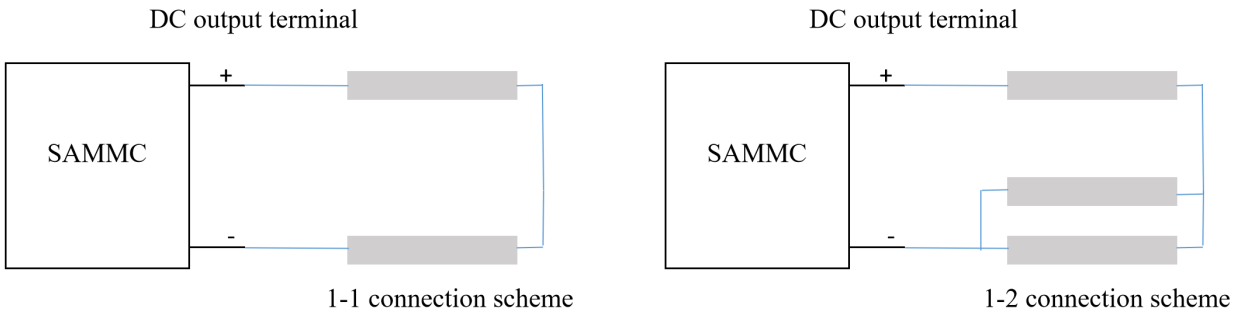

Figure 3.3: 1-1 connection scheme (left) 1-2 connection scheme (right).

Figure 3.3 shows two connection schemes that are widely adopted in DC deicing. The left-hand side is called 1-1 mode, and the right-hand side is called 1-2 mode [41]. In a 1-1 mode connection, two phase conductors are connected in series. Since only two conductors can be connected, the melting procedure need to be done twice to heat three conductors. In 1-2 connection, one conductor is in series with two parallel conductors, so only one melting action is required. But the downside of 1-2 connection is the two parallel conductors can only be heated by half of the maximum current.

When choosing the connection scheme, it is helpful to refer to the resistance of the connected conductors. The 1-1 connection scheme resistance is 33% larger than 1-2 connection scheme. In a SAMMC rectifier, the DC voltage is decided by the DC current I_{dc} and connection conductor resistance R_{com}:

$$V_{dc} = I_{dc} \cdot R_{con} \tag{3.1}$$

Also the output L-L RMS voltage of SAMMC is described as (3.2):

$$V_{acRMS} = \frac{mI_{dc}R_{con}}{6\sqrt{2}} \tag{3.2}$$

By combining (3.1) and (3.2), it can be found that when a certain I_{dc} is required, the converter

AC output voltage is decided by connection conductor resistance.

$$V_{acRMS} = \frac{V_{dc}}{6\sqrt{2}} \tag{3.3}$$

So by modifying the connection scheme, a suitable AC voltage can be set for the converter to reduce the reactive power transmission.

3.2 Mathematical model for SAMMC deicer design

In order to design the SAMMC system, the performance of this deicer system needs to be studied. The design of the converter has been studied in Chapter 2, but the choosing of transformer for this system is not studied. Moreover, different DC load resistance also affects the performance of this system. To optimize the deicer system design, the operating point of a certain case (for example, when system parameters are settled, to apply a certain DC current on the load conductor, what is the P Q output value and AC current of the system) need to be obtained; also the PQ capability of the system (what is the maximum power can the system transfer with a certain load conductor), and also how different transformer rating and load conductor resistance affect the performance of the system. This section builds a mathematical model for the deicer system to study the questions above and help design the SAMMC deicer system.

Since this mathematical model only focuses on steady-state power flow, only fundamental frequency component will be studied. This model analyzes the power conversion of SAMMC by extracting the AC circuit and DC circuit from the circuit diagram of SAMMC deicer system.

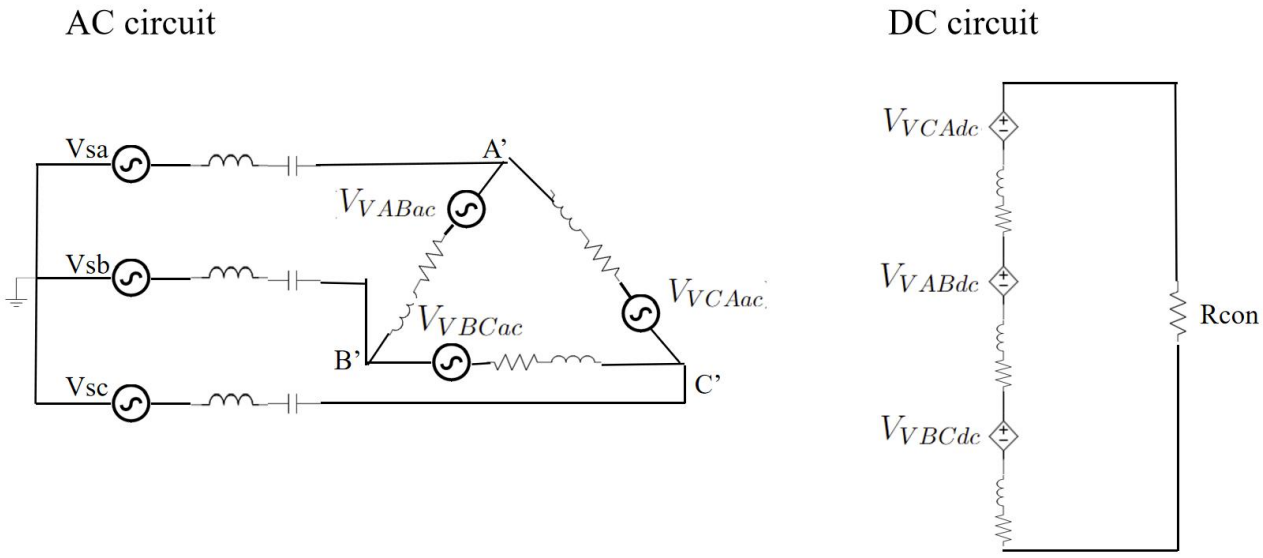

Figure 3.4: AC circuit and DC circuit of SAMMC deicer circuit.

As shown in Figure 3.4, three SM valves are connected in delta . Each valve can be modelled as an ideal AC voltage source and a series resistor. The series resistor represents the power semiconductor (IGBT and diode) turn-on resistance.

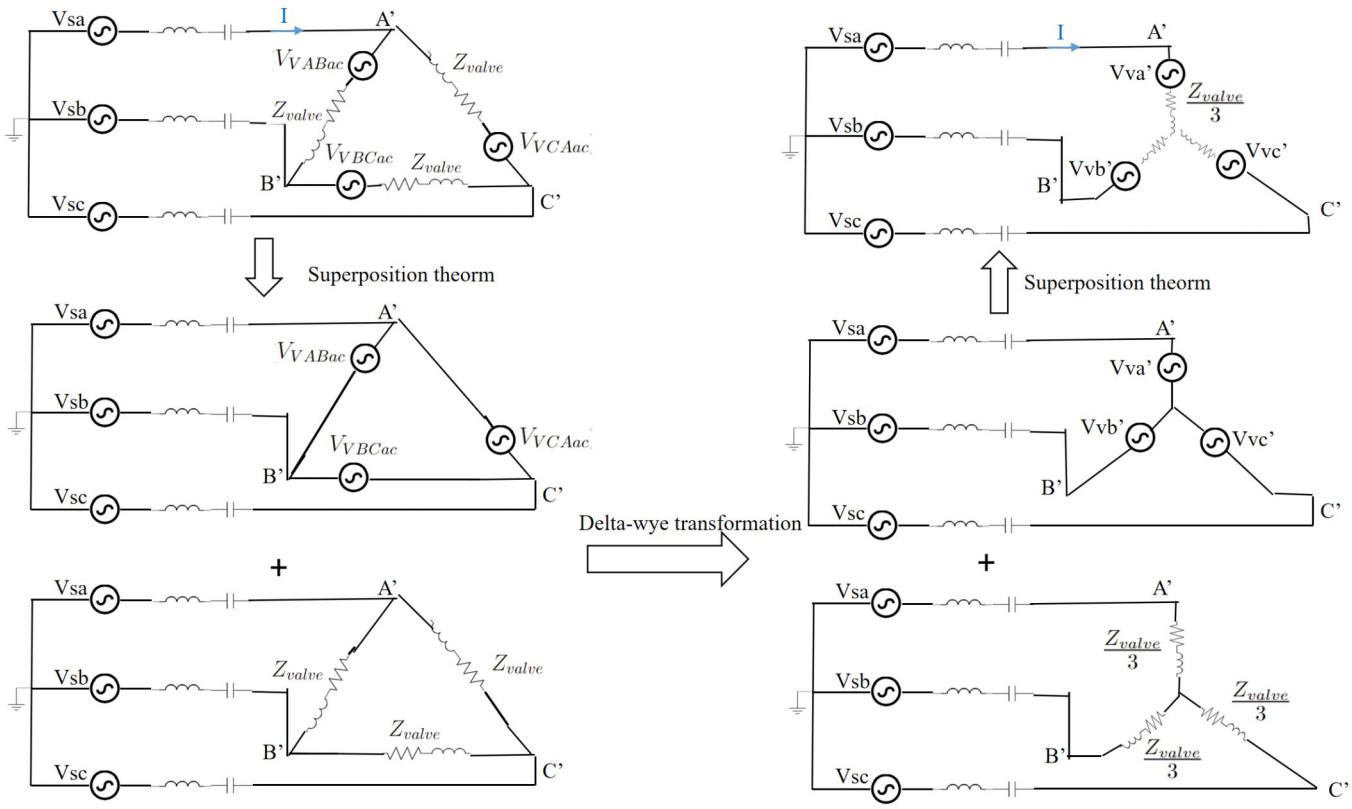

Figure 3.5: Delta-wye transformation of SAMMC deicer AC circuit

To study the power flow of the proposed AC circuit, a delta-wye transformation is applied to the AC circuit. As illustrated in Figure 3.5, first apply superposition theorem on the AC circuit to decouple the voltage source and passive components into two subcircuits, then apply delta-wye transformation to both subcircuit, finally combine the two transformed subcircuit based on superposition theorem.

After the delta-wye transformation, the wye equivalent voltages $(V'_{Va}, V'_{Vb}, V'_{Vc})$ become $1/\sqrt{3}$ times of the original AC valve voltage $(V_{VABac}, V_{VBCac}, V_{VCAac})$ with a 30°phase lagging. Z_{valve} is the impedance of the SM valve, after the delta-wye transformation, it becomes $\frac{Z_{valve}}{3}$ in the wye equivalent circuit.

In the case the L-L voltage of AC power system leads converter L-L voltage by δ degree,

the apparent power transmit from power system to converter can be expressed as:

$$\begin{aligned}
S_1 &= 3V_{sp}I^* \\
&= 3V_{sp}\angle\delta \left[\frac{V_{sp}\angle\delta - V_{Va}^{'}\angle 0}{jX+R}\right]^* \\
&= 3V_{sp}(\cos\delta + j\sin\delta)\left[\frac{V_{sp}(\cos\delta + j\sin\delta) - V_{Va}^{'}}{jX+R}\right]^* \\
&= \frac{3R(V_{sp}^2 - V_{sp}V_{Va}^{'}\cos\delta) + 3XV_{sp}V_{Va}^{'}\sin\delta}{R^2+X^2} + j\frac{3V_{sp}^2X - 3RV_{sp}V_{Va}^{'}\sin\delta - 3XV_{sp}V_{Va}^{'}\cos\delta}{R^2+X^2}
\end{aligned} \tag{3.4}$$

where $X = X_t - \frac{1}{j\omega C_{ac}} + j\omega\frac{L_{valve}}{3}$, and $R = \frac{R_{valve}}{3}$.

The real power and reactive power transmitted from power system to deicer system is the real part and imaginary part of apparent power S_1:

$$\begin{aligned}
P_1 &= \frac{3R(V_{sp}^2 - V_{sp}V_{Va}^{'}\cos\delta) + 3XV_{sp}V_{Va}^{'}\sin\delta}{R^2+X^2} \\
Q_1 &= j\frac{3V_{sp}^2X - 3RV_{sp}V_{Va}^{'}\sin\delta - 3XV_{sp}V_{Va}^{'}\cos\delta}{R^2+X^2}
\end{aligned} \tag{3.5}$$

Also, the apparent power received by the converter can be expressed as:

$$\begin{aligned}
S_2 &= 3V_{Va}^{'}I^* \\
&= 3V_{Va}^{'}\angle 0 \left[\frac{V_{sp}\angle\delta - V_{Va}^{'}\angle 0}{jX+R}\right]^* \\
&= 3V_{Va}^{'}\left[\frac{V_{sp}(\cos\delta + j\sin\delta) - V_{Va}^{'}}{jX+R}\right]^* \\
&= \frac{3R(V_{sp}V_{Va}^{'}\cos\delta - V_{Va}^{'2}) + 3XV_{sp}V_{Va}^{'}\sin\delta}{R^2+X^2} + j\frac{3XV_{sp}V_{Va}^{'}\cos\delta - 3RV_{sp}V_{Va}^{'}\sin\delta - 3V_{Va}^{'2}X}{R^2+X^2}
\end{aligned} \tag{3.6}$$

The real power and the reactive power absorbed by the converter are:

$$\begin{aligned}
P_2 &= \frac{3R(V_{sp}V_{Va}^{'}\cos\delta - V_{Va}^{'2}) + 3XV_{sp}V_{Va}^{'}\sin\delta}{R^2+X^2} \\
Q_2 &= j\frac{3XV_{sp}V_{Va}^{'}\cos\delta - 3RV_{sp}V_{Va}^{'}\sin\delta - 3V_{Va}^{'2}X}{R^2+X^2}
\end{aligned} \tag{3.7}$$

Next, the power flow of DC circuit need to be studied. The DC circuit power is the power

on load conductors R_{con} and valve resistance R_{valve}:

$$P_{dc} = I_{dc}^2 \left(R_{con} + 3R_{valve}\right) \tag{3.8}$$

The power balance equation is used to solve the operating point; the real power converter received from power system should be equal to the DC power output of the converter:

$$P_{dc} = P_2 \tag{3.9}$$

The procedure of solving the operation point for a certain melting case with the proposed mathematical model is shown in the flow chart in Figure 3.6:

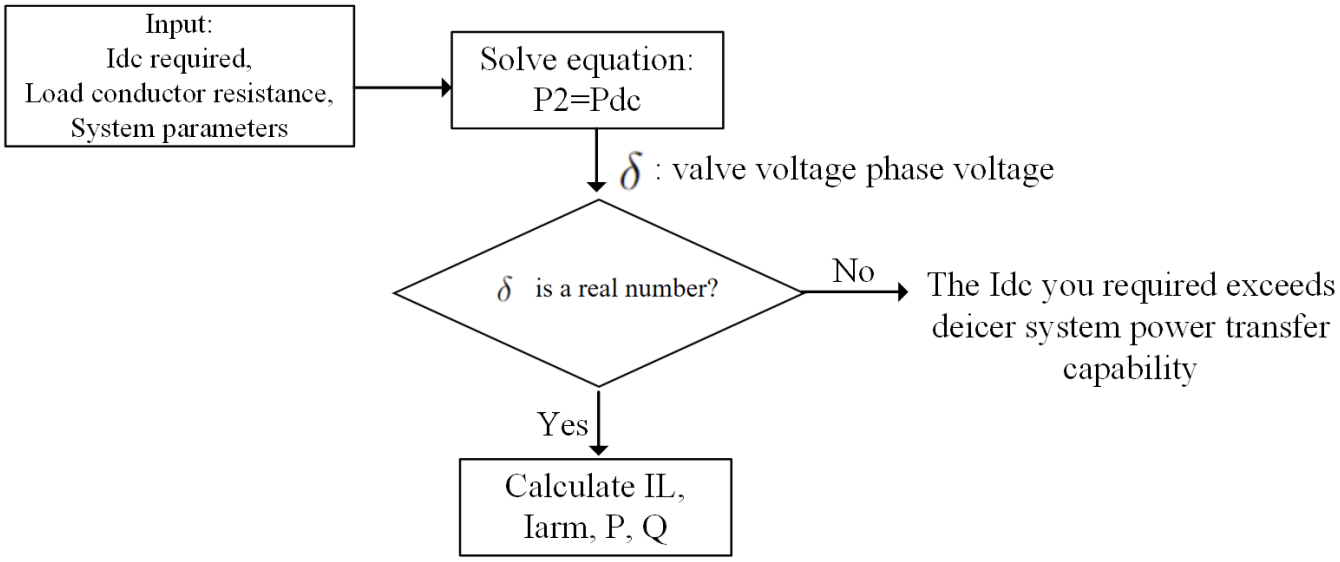

Figure 3.6: Diagram of solving deicer operation point

The inputs to the model are the system parameters (transformer's secondary side voltage and leakage impedance, converter parameters and modulation index), the resistance of load conductors, and the required I_{dc}.

All the inputs are used to solve the phase angle delay of valve voltage, δ, with the power balance equation (3.9). If δ is a real value, this value is used to calculate other operation values, like converter output currents and valve currents. If δ is a complex number, this

indicate $sin\delta > 1$, which means the required I_{dc} exceeds the maximum real power capability for this system.

3.3 Impact of parameters in SAMMC deicer design

After obtaining the mathematical model to calculate the operation point for a certain case, this section studies how different parameters affect the performance of the system. This will help to design the system wisely. The parameters needed to be discussed are: transformer secondary voltage rating V_{sp}, system total impedance $X = X_t - \frac{1}{j\omega Cac} + j\omega\frac{L_{valve}}{3}$, and modulation index for converter controlling m. The proposed the mathematical model is used to evaluate how these parameters affect the power output capability and PQ performance for a certain melting case.

3.3.1 The impact of modulation index (m)

The transformer's primary-side PQ diagram is shown as follows.

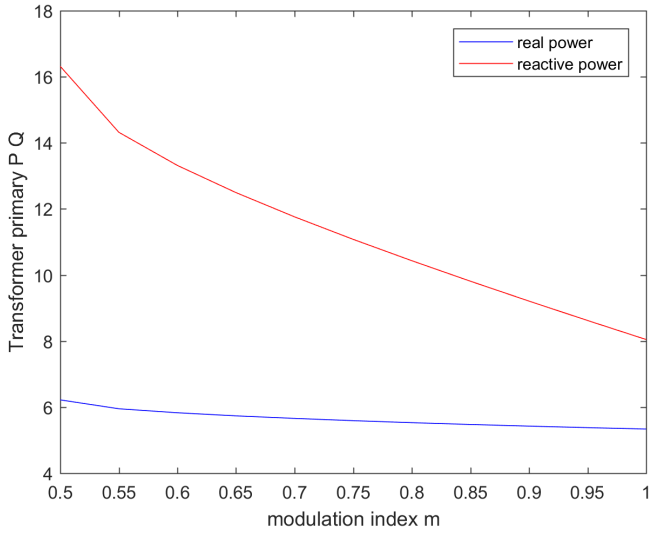

Figure 3.7: Transformer primary side PQ diagram with different modulation index

Since the conductor resistance is usually a very small value (4.8Ω in this case), (3.2) shows

that the converter's output AC voltage is also small compared with transformer secondary-side voltage. So an undesirable reactive power will flow from AC power system to the converter. From (3.2), a larger modulation index is used, the converter output voltage will be larger, so the reactive power flow can be reduced. In conclusion, the largest modulation index ($m = 1$) should be used in this system.

3.3.2 The impact of transformer's secondary-side voltage

Knowing that the modulation index should be $m = 1$ from the previous section, this subsection discusses the impact of transformer's secondary voltage rating. Since the transformer primary side voltage rating is fixed at 66 kV, this section will test the secondary voltage rating from 1 kV to 10 kV, and plot the PQ power capability when other parameters are fixed.

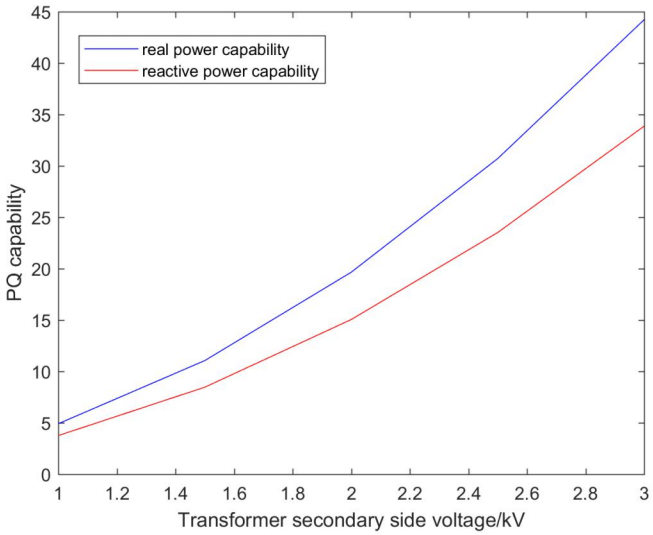

Figure 3.8: Converter PQ capability with different transformer secondary voltage rating

From Figure 3.8, to allow the converter to provide enough real power for conductor melting (typically. 5-10 MW), 1.5 kV 2 kV rating voltage on transformer secondary side is enough.

To study different transformer secondary voltage rating systems' performance in a certain case, the mathematical model is used to study different transformer secondary voltage ratings

and test their PQ output when apply a 1 kA DC current on 4.8Ω conductor. The results are plotted in Figure 3.9:

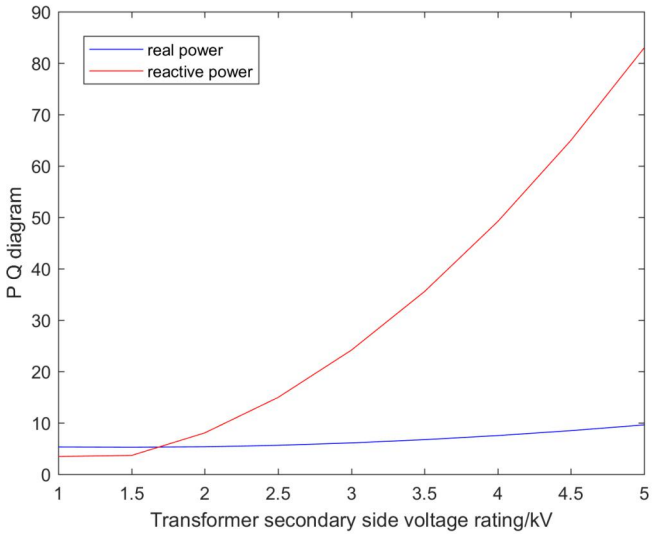

Figure 3.9: 1 kA melting case study for different transformer secondary voltage rating

If a larger transformer secondary voltage is chosen, the reactive power flow from power system to SAMMC converter is larger, thus requiring a larger MVA rating transformer. Also when transformer secondary voltage is larger, the valve current RMS value will be larger, thus causing more conduction loss on power semiconductors.

In conclusion, if transformer secondary voltage rating is too high, the reactive power flow will be excessive, thus a larger transformer need to be deployed. If transformer secondary voltage rating is too low, the system will be incapable to produce enough DC power.

3.3.3 The impact of system total impedance

The system total impedance is the impedance connecting the SAMMC converter with power system. As term $X = X_t - \frac{1}{j\omega Cac} + j\omega\frac{L_{valve}}{3}$ the system total impedance is made up with three parts, transformer leakage impedance, AC side capacitors and valve inductors. This subsection will study those three impedances as a whole, X, and study its impact on system power output capability and study their performance in a case study.

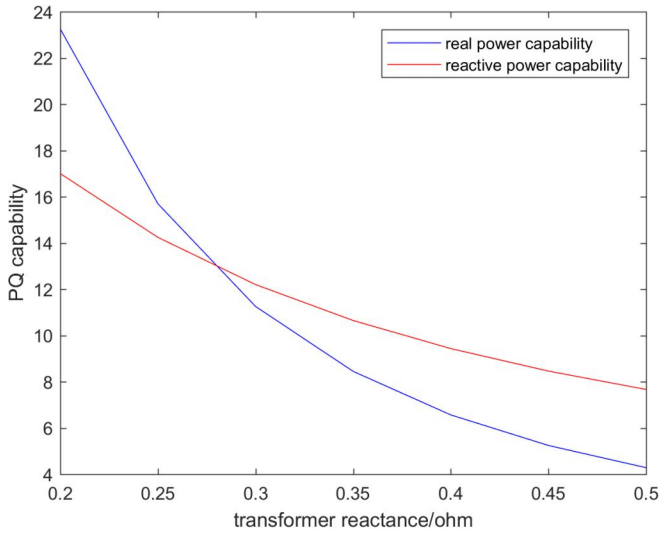

Figure 3.10: Converter PQ capability with different transformer reactance

Figure 3.10 shows the PQ capability of the system with different transformer reactance. If the transformer reactance is larger than 0.45Ω, the maximum real power output of the converter will be less than 5 MW.

Also the performance of different deicer systems with transformer of 0.2∼0.45Ω reactance when heating 4.8 Ω conductors with 1 kA DC current is studied. The results are plotted in Figure 3.11:

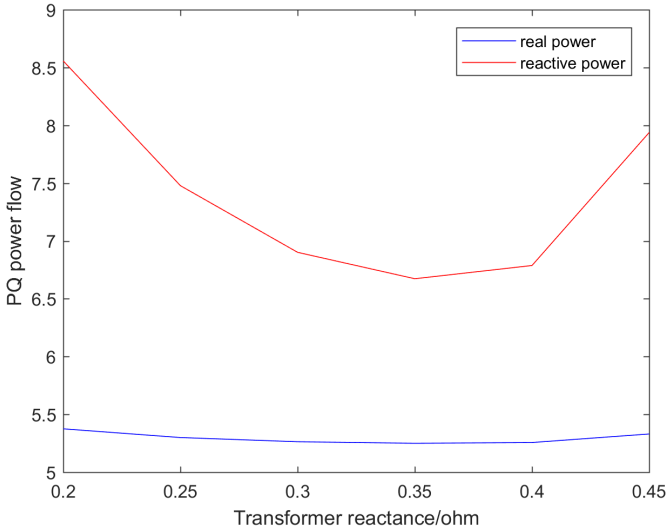

Figure 3.11: 1kA melting case study for different transformer reactance

As shown in Figure 3.11, the reactive power flow reaches its minimum value when transformer reactance is 0.35Ω in this case. If the transformer cannot provide enough reactance, series reactor may be used.

3.4 Design of SAMMC DC deicer: a case study

This section will design a DC deicer to melt a 50 km segment of 230 kV transmission line. The parameters of transmission line is listed as the following table:

Table 3.1: Parameters for load transmission line conductor

Line Designation	Voltage Class (kV)	X/R ratio	R_{ac} per km	X per km	R_{dc} per km
LineA 230	230	9.6	0.0629	0.4885	0.048

Table 3.2: Parameters for load transmission line conductor

In the deicer system, the load conductors to be melted can be described as a lumped model with a series resistor and reactor. In this case, to melt transmission lines in Table 3.2 with 1-1 connection scheme, the lumped model for two power line conductors in series is shown in Figure 3.12.

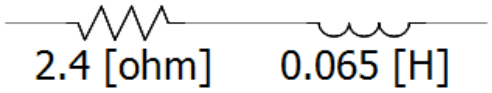

Figure 3.12: Lumped model for load transmission line conductor

This section will design a SAMMC deicer system to provide 0.8 kA DC current on the above transmission line.

3.4.1 System parameter design

Section 3.3 provides a method to choose modulation index and transformer for the deicer system, and section 2.2 provide method to design the SAMMC converter. Based on these previous study, the system parameters are designed as Table 3.2:

Table 3.3: Parameters for SAMMC DC deicer system design.

Parameter	Value	Unit
Transformer primary voltage	66	kV
Transformer secondary voltage	2	kV
Transformer MVA rating	10	MVA
Transformer leakage reactance	15%	pu
Series reactance	0.769	mH

The SAMMC converter parameters are designed as Table 3.3:

Table 3.4: Parameters for SAMMC Converter.

Parameter	Value	Unit
Number of SM per valve	6	-
SM capacitance	20	mF
Valve inductor	0.5	mH

3.4.2 Controller design

A simplified real power transmission equation can be expressed as (3.10):

$$P = \frac{V_1 V_2 \sin\delta}{X} \tag{3.10}$$

where V_1 is the L-L RMS value of transformer secondary side voltage, V_2 is the L-L RMS value of SAMMC, δ is the phase angle difference between V_1 and V_2, X is the impedance between power system and converter.

The real power flow is controlled by two variables, magnitude of converter output voltage V_2 and the converter phase delay δ. As discussed in subsection 3.3.1, in the deicer system, usually V_2 is much smaller than V_1, so the modulation index is fixed to be 1 to avoid larger

reactive power flow, which means the magnitude of converter output voltage V_2 is a constant. So real power can only be controlled by voltage phase delay δ.

A simple control of VSC converter DC current is depicted in Figure 3.13. In this dual-loop controller, the outer loop is DC current controller, output DC current is controlled by the active power flow; the inner loop is converter real power controller, the real power transmitted from power system to converter is controlled by voltage phase delay δ.

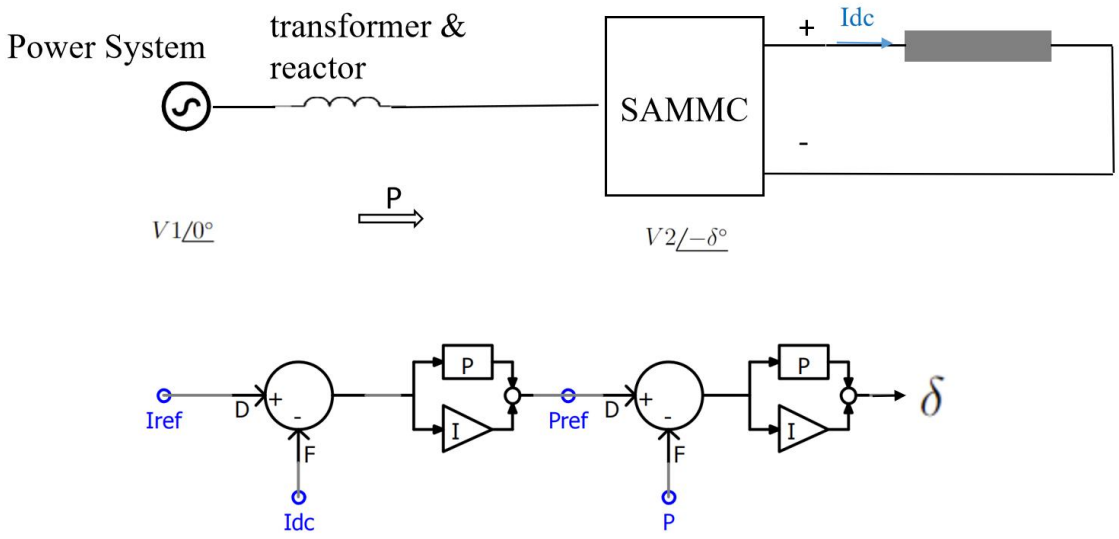

Figure 3.13: Dual-loop controller for SAMMC DC deicer

3.4.3 Simulation results

The proposed SAMMC DC deicer system is modeled in PSCAD; the converter is represented by detailed equivalent model (DEM) [42]. The converter three phase AC current, AC voltage, valve voltage, output DC voltage/current and the consumed real/reactive power is shown:

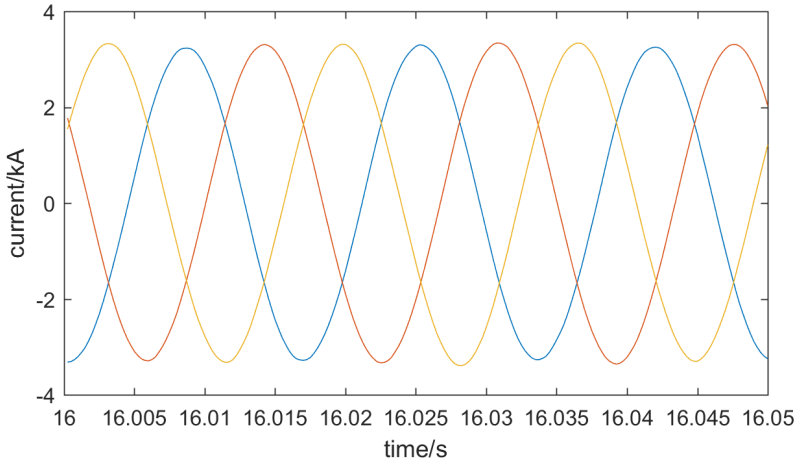

Figure 3.14: Converter AC output current I2.

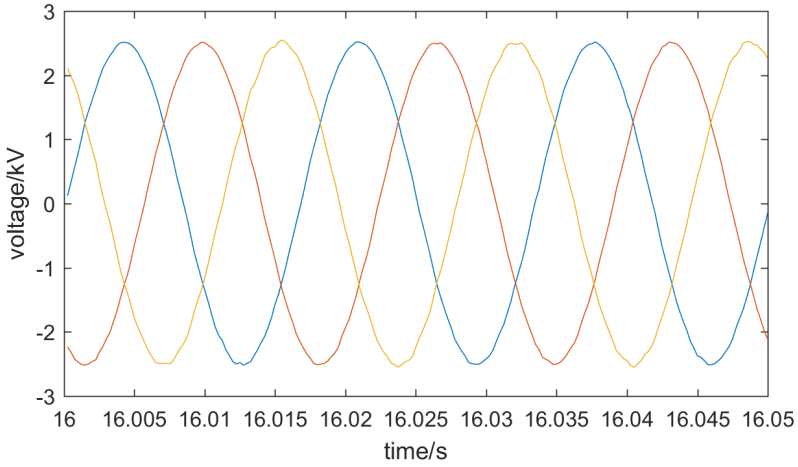

Figure 3.15: Converter AC output voltage V2.

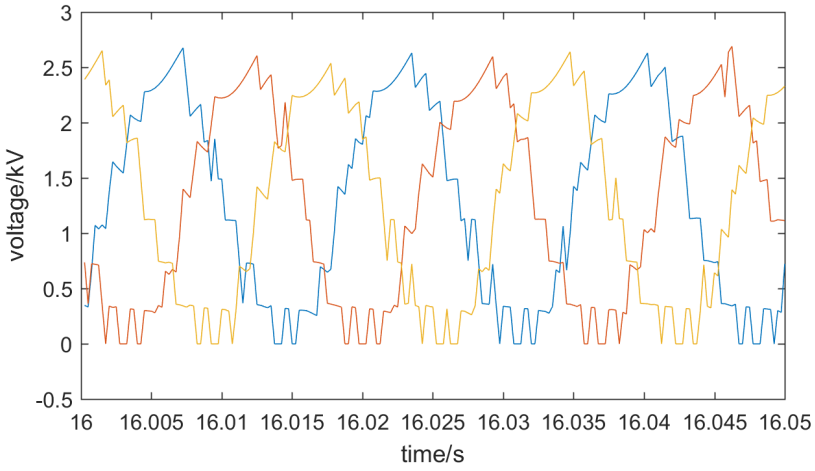

Figure 3.16: Converter valve voltage $V_{vab}, V_{vbc}, V_{vca}$.

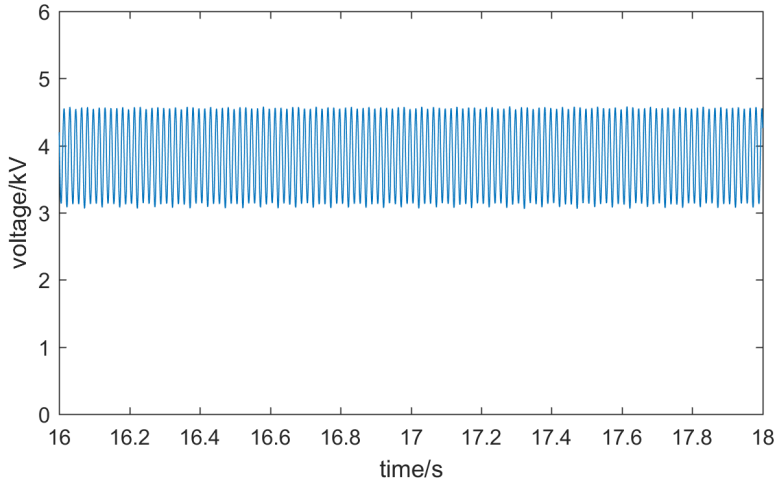

Figure 3.17: Converter output DC voltage V_{dcx}.

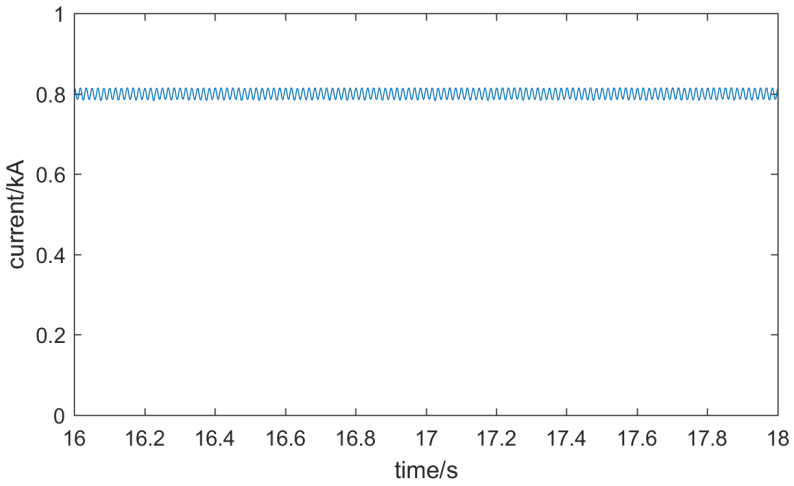

Figure 3.18: Converter output DC current I_{dc}.

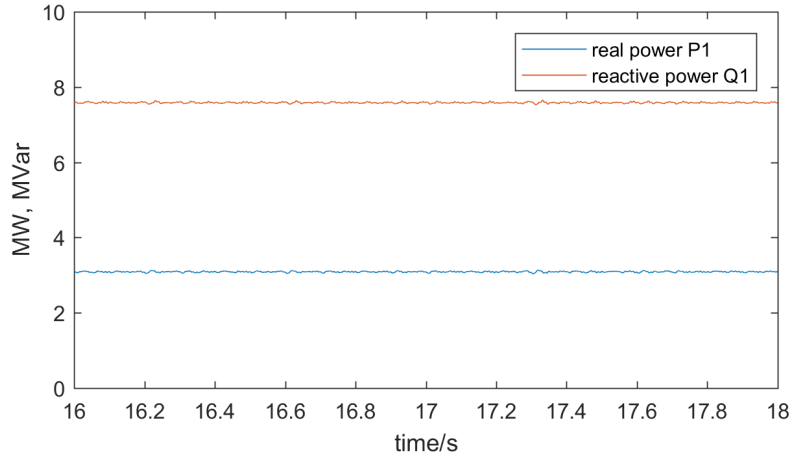

Figure 3.19: Real power (P1) reactive power (Q1) consumed by transformer primary side.

With the 2HCSC controller, The THD of three phase currents are controlled to be 0.96%, 0.58% and 0.91% for phase A, phase B and phase C. And the THD of converter output AC voltages are 2.82%, 2.82% and 2.96% for phase A, phase B and phase C.

3.5 Design of SAMMC DC deicer with DC buck converter

While section 3.4 gives out a design of SAMMC deicer, there are some disadvantages in this design. This section will evaluate the limitation of the design proposed in section 3.4 and give out an improvement by adding a DC buck converter on the DC side of SAMMC converter. A PSCAD simulation case study is given out at the end of this section.

3.5.1 Limitation of SAMMC DC deicer

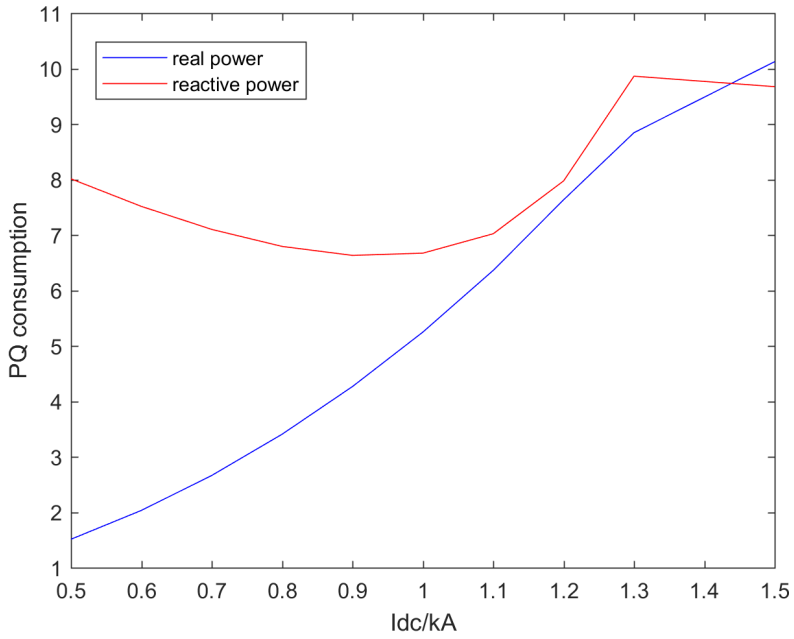

Figure 3.20: Deicer system PQ output with different magnitudes of DC current I_{dc}

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Section 3.4 presents a case study which a conductor is melted by 0.8 kA DC current. However, if different magnitudes of DC current are applied to melt the conductor, the operation condition will change, and may not be desirable.

Figure 3.20 shows how DC current affects the PQ output of the deicer system. When I_{dc} increases from 0.8 kA to 1 kA, the reactive power absorbed by the system will increase and

exceed the capacity of the 10 MVA transformer. In other words, the reactive power of the deicer system limits the operation flexibility of the SAMMC DC deicer system.

To address this issue, it is important to understand the reason of the reactive power flow. As shown in (3.2), the converter AC voltage is decided by DC load resistance and DC current. While the DC resistance of a conductor is a relatively small value, the converter side AC voltage is also small. The voltage magnitude difference between high transformer secondary side EMF (Electromotive force) and low converter AC voltage will cause a huge reactive power flow from power system to converter.

3.5.2 Design SAMMC DC deicer with DC buck converter

To reduce the reactive power flow, the converter AC voltage must be risen. From (3.3), to boost converter AC side voltage magnitude, the converter DC voltage must be increased. By adding a DC buck converter between converter DC side voltage and DC load voltage, the converter DC side voltage can be boosted up.

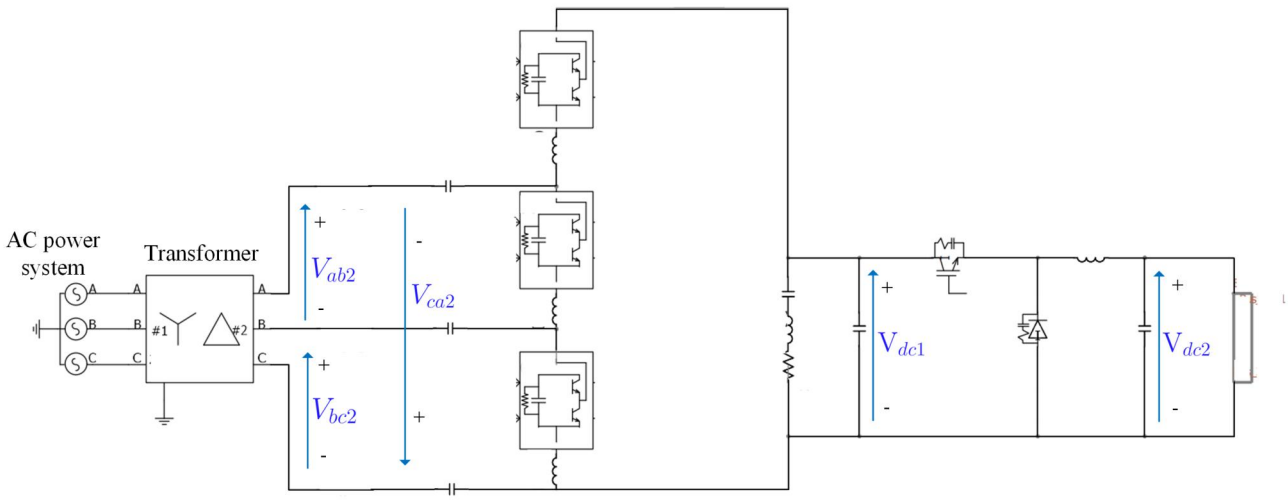

Figure 3.21: Diagram of SAMMC rectifier with DC buck converter.

The diagram is shown in Figure 3.21. Compared with the previous design in Figure 1.3, although one DC buck converter is added, the transformer size is reduced greatly, and there is no need for adding additional series inductors. By adding the DC buck converter, the size of DC deicer is reduced, also the load DC current can be increased. The next subsection will use simulation to validate the improvement.

3.5.3 Controller design

This subsection will discuss the controllers for both the SAMMC and DC-DC buck converter in the system.

The SAMMC is equipped with a real power controller and a reactive power controller. The simplified real power transmission equation can be expressed as (3.10), the real power controller remains the same with Figure 3.13. And the simplified reactive power transmission equation can be expressed as (3.11):

$$Q = \frac{V_1 V_2 \cos\delta - V_2^2}{X} \tag{3.11}$$

Where Q is the reactive power transferred from power system to SAMMC converter, V_1 is the L-L RMS value of transformer secondary side voltage, V_2 is the L-L RMS value of SAMMC, δ is the phase angle difference of V_1 and V_2, X is the impedance from power system to converter. When the phase angle difference between power system side voltage and converter side voltage delta is a small value, the control of real power flow and reactive power flow can be approximately decoupled as: P is controlled by δ, Q is controlled by converter side voltage magnitude V_{acRMS}. From (3.2), the control of voltage magnitude V_{acRMS} can be achieved by controlling the modulation index m.

The controller for SAMMC rectifier is shown in Figure 3.22.

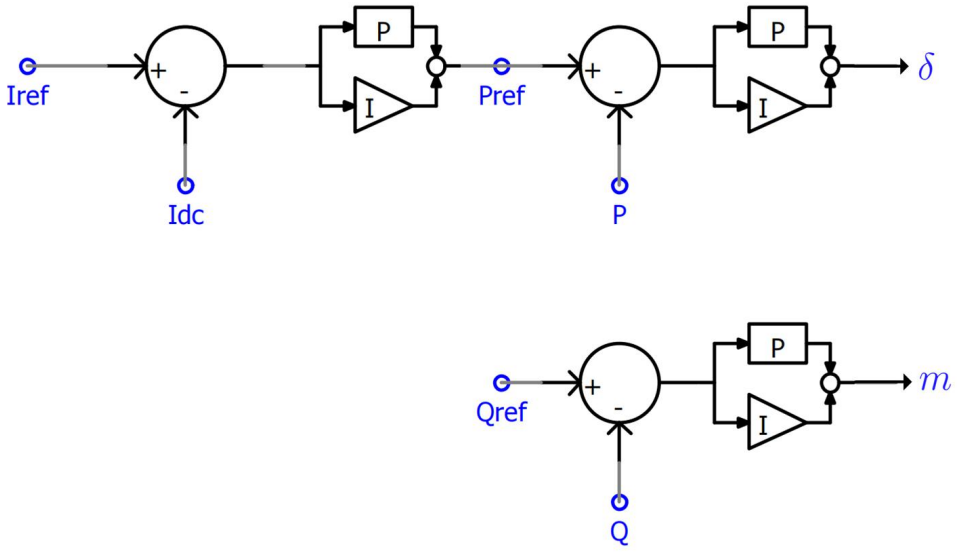

Figure 3.22: SAMMC rectifier PQ controller.

The real power controller is a dual-loop controller. The outer loop is the DC current controller, I_{dc} is the measured DC current on the DC side load and I_{ref} is the demanded DC current reference. The inner loop is the real power controller, the output power of the converter P is controlled by δ, which is the phase angle between transformer secondary side voltage and converter voltage. While the reactive power control loop is simple, the actual reactive power flow Q follows the reactive power reference Q_{ref} by controlling the modulation index m.

The controller of DC-DC buck converter is used to regulate the voltage ratio of input DC voltage V_{dc1} and output DC voltage V_{dc2}. As stated in subsection 1.2.3, the buck converter is controlled by PWM scheme. A modulation reference signal is used to control the buck converter. By regulating the modulation reference signal of buck converter *Buckmod*, the DC link voltage between SAMMC and DC-DC buck converter V_{dc1} is controlled as a constant 23kV. This controller is shown in Figure 3.23.

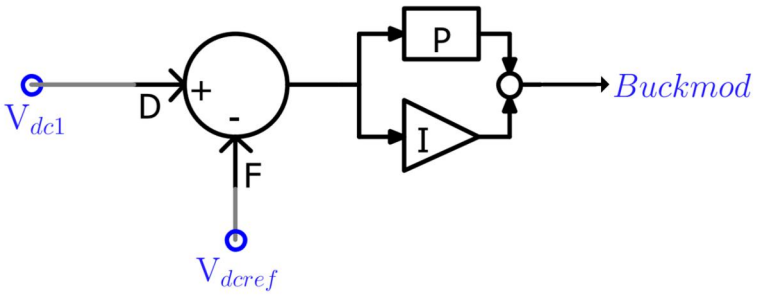

Figure 3.23: DC-DC buck controller.

When operators from the utility conduct deicing with the DC Deicer, they should set the DC current reference I_{ref} and the reactive power reference Q_{ref} from the control panel. Once the ice melting procedure finishes, shut down the converter and remove the connection between Deicer and power lines. The DC current reference I_{ref} need to be designed carefully by analysis the thermal dissipation model of the conductor so that the melting procedure can be done in a suitable length of time. The choice of DC current is affected by conductor type, shape and thickness of ice layer, ambient temperature and other environmental conditions.

3.5.4 Simulation results

The simulation of SAMMC DC deicer with DC buck converter system is built in RSCAD substep environment. The SAMMC converter is modelled by an average value model. The parameter setting of the simulation is listed in the table below:

Table 3.5: Parameters for SAMMC DC deicer system with DC-DC buck converter.

Parameter	Value	Unit
Number of SM per valve	6	-
SM capacitance	20	mF
Valve inductor	0.6	mH
Transformer primary side voltage	66	kV
Transformer 2nd side voltage	3	kV
Transformer MVA rating	5	MVA
Transformer leakage reactance	10.7%	p.u.
Buck converter input capacitor	6755	μ F
Buck converter output capacitor	10	mF
Buck converter inductor	0.1	mH

The simulation waveforms (with 2HCSC enabled) are shown below:

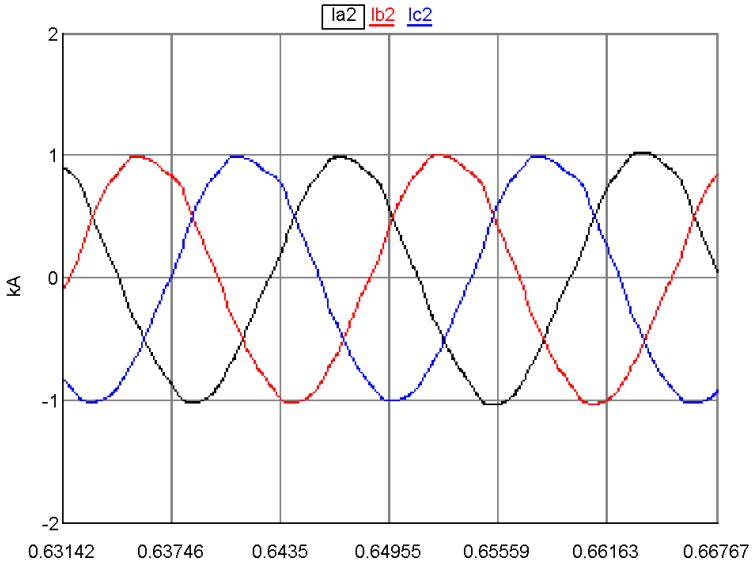

Figure 3.24: Converter output current

The THD of converter output current is 3.19%.

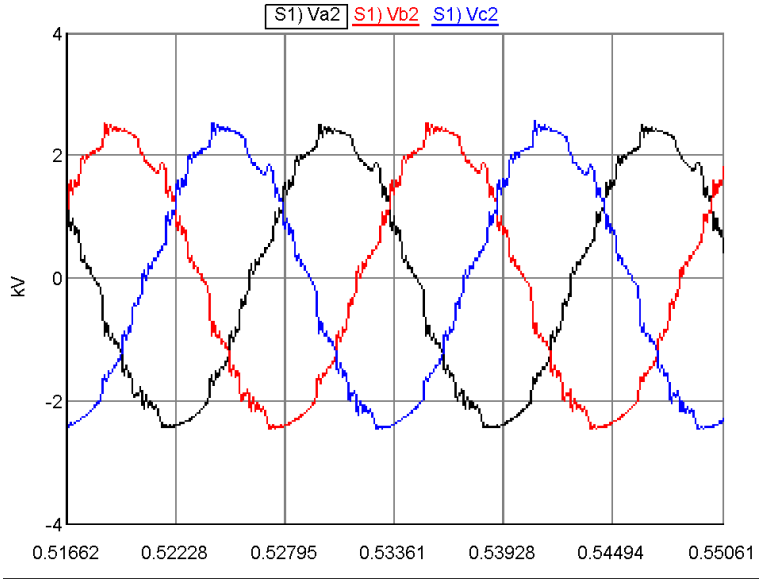

Figure 3.25: Converter output voltage

The THD of output voltage is 6.32%.

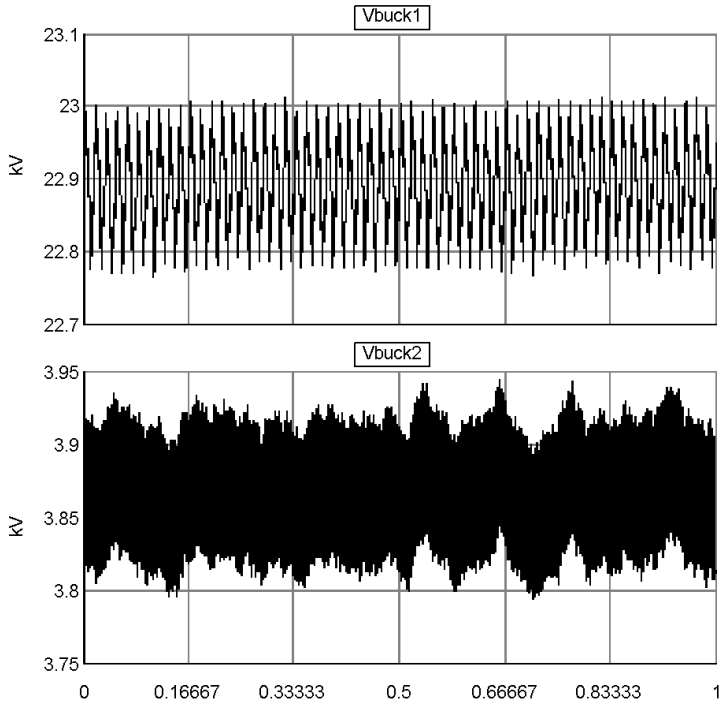

Figure 3.26: Converter DC voltage (Vbuck1) DC load voltage (Vbuck2)

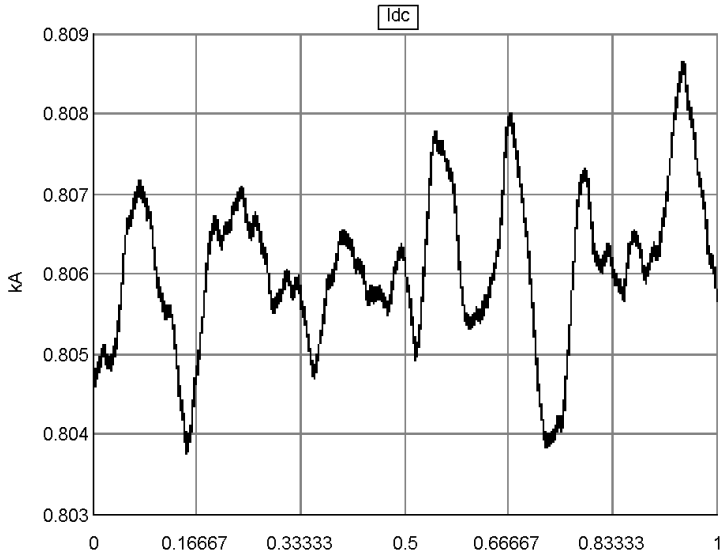

Figure 3.27: DC load current

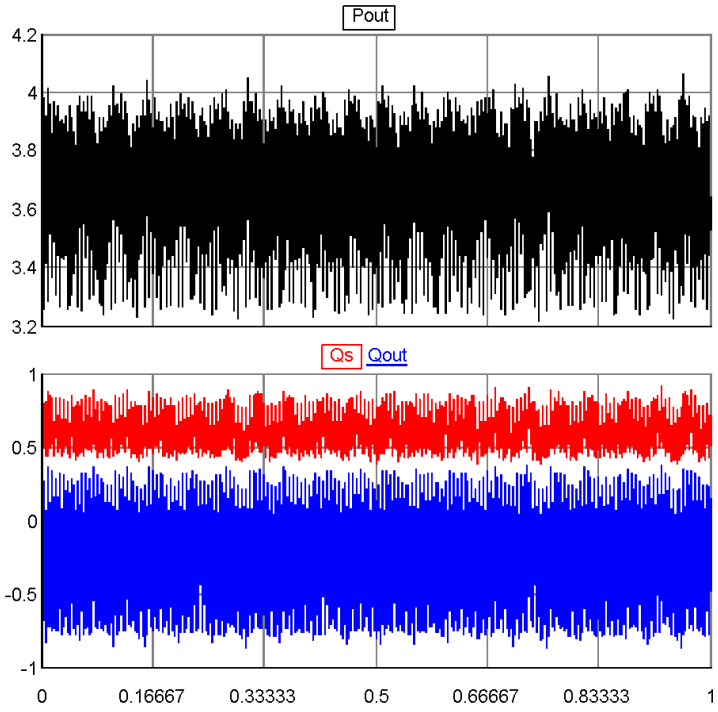

Figure 3.28: Deicer system absorbed real power and reactive power

Qs is the reactive power absorbed by transformer primary side, Qout is the output reactive power of transformer secondary side. Qs is 0.63MVar, Qout is -0.26MVar. Compared with the application of SAMMC DC deicer without DC-DC buck converter, the reactive power flow is reduced by 90%.

Chapter 4

Real-Time Hardware-in-Loop Validation of SAMMC Rectifier

The previous chapters have already theoretically analyzed the SAMMC converter and also designed and validated the SAMMC DC deicer in EMT simulations. To further test the proposed design in real world, a lab-scale MMC setup is used to build an SAMMC prototype, and operate it as a rectifier to heat up resistors. The design of this prototype converter and the result waveforms are shown in this chapter.

4.1 Design and parameters of SAMMC hardware

The RTDS Hardware-In-Loop (HIL) testing system for SAMMC rectifier is consists of following parts:

• MMC submodule setup is modified to be the converter.

• RTDS rack and GTIO cards are used to control the converter, send firing pulses to submodules and collect voltage & current data.

• A Lab volt is used to provide AC voltage.

• Some other peripherals are designed based on certain case.

• An oscilloscope is used to read voltage and current waveforms.

The core part of this lab-scale MMC prototype, the MMC submodule setup, is built by Dr. Xianghua Shi. Detailed information about the design and firing principle of the lab-scale submodules can be found in her report [43]. The table below lists some of the key parameters of the submodules:

Table 4.1: Key parameters of lab-scale submodules.

Parameter	Value	Unit
SM capacitance	4.7	mF
Nominal capacitor voltage	20	V
MOSFET maximum voltage	100	V
MOSFET rated current	137	A
MOSFET on-state resistance	4.5	mΩ
Diode maximum voltage	100	V
Diode rated current	30	A
Diode forward voltage drop	0.385	V

To emulate the SAMMC DC deicer with the lab-scale prototype, a test system is built under the design of Figure 4.1. Three SM valves are connected with a 60 Hz resonant filter, and AC capacitors are connected at the AC output terminals to make a SAMMC converter. Three reactors connect the Lab Volt AC voltage to the converter AC terminal as an equivalent of three phase transformer. A load resistor is connected at the resonant filter to be heat up. A RTDS GPC rack is used to generate firing pulses for SM semiconductors from input modulation waveform. Also an oscilloscope is used to read and record waveforms.

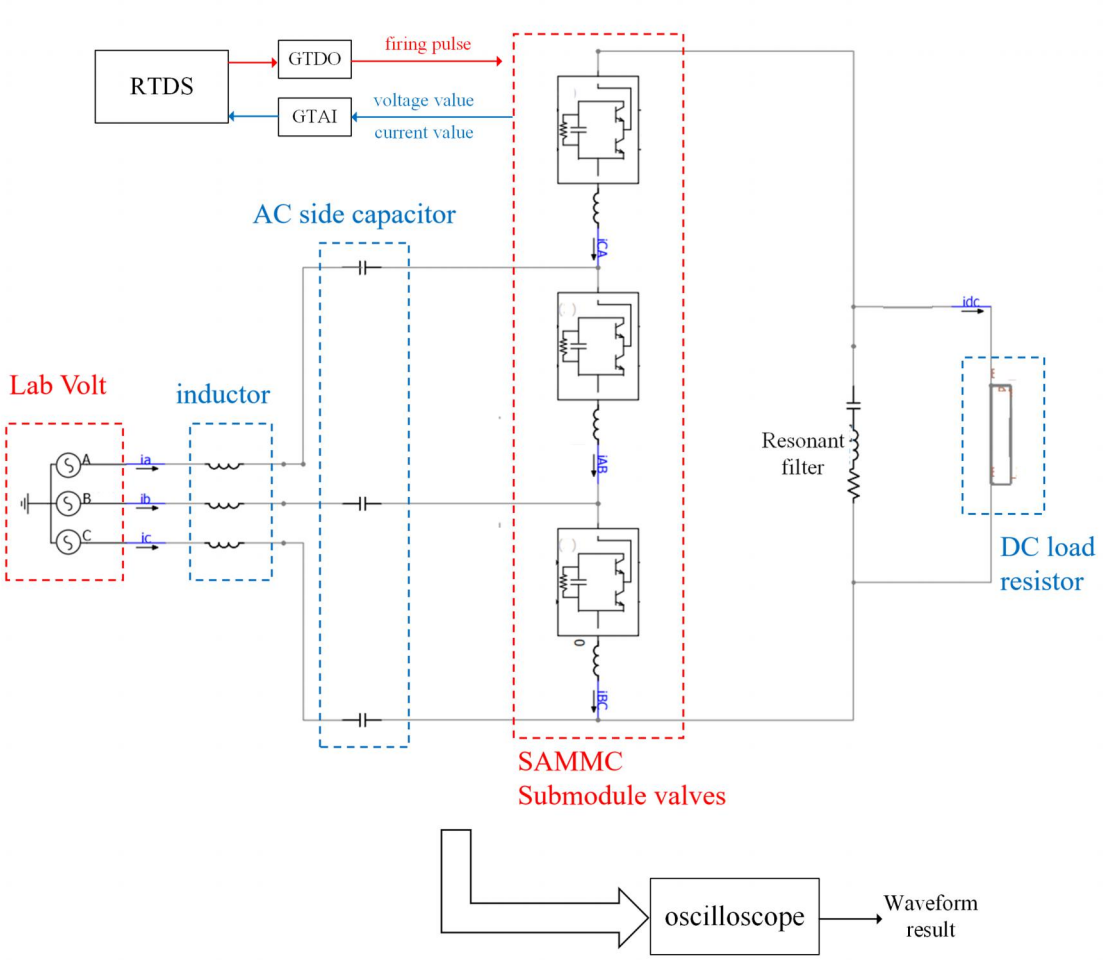

Figure 4.1: Diagram of the HIL testing system.

The design parameters of lab-scale SAMMC rectifier system is listed in Table 4.2:

Table 4.2: Lab-scale SAMMC rectifier system setup

Parameter	Value	Unit
Number of SM per valve	10	-
Valve inductor	5.1	mH
AC side capacitor	312	mF
DC resistive load	236	Ω
AC input voltage	36	V
Modulation index	1	-
Modulation waveform phase angle	50	degree

4.2 SAMMC hardware result waveforms

The SAMMC HIL hardware testing system is built and shown in Figure 4.2.

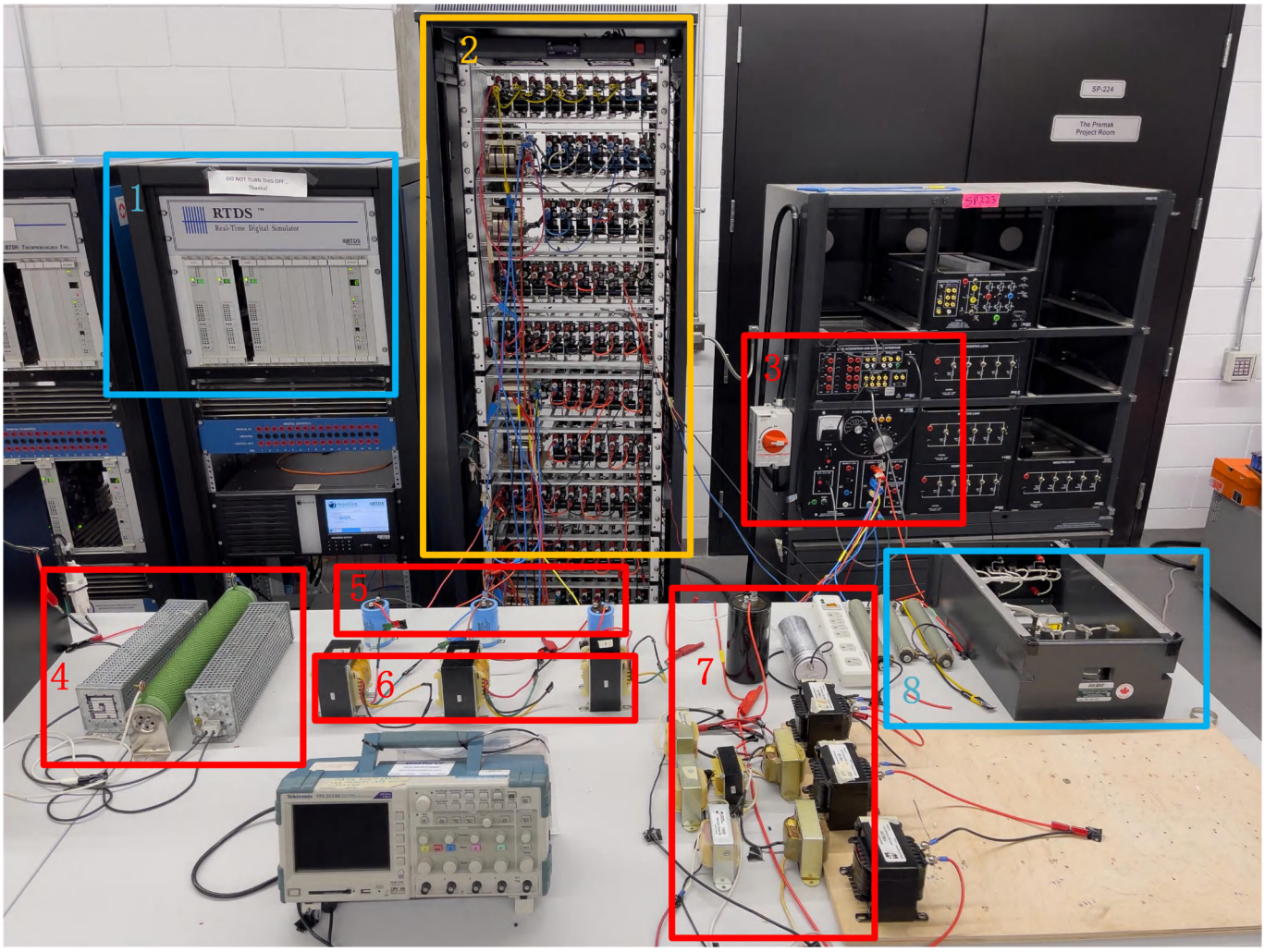

Figure 4.2: Lab-scale SAMMC rectifier system photo.

The devices shown in the photo Figure 4.2 are listed as: 1. RTDS rack, 2. Lab-scale half-bridge SM, 3. Lab volt, 4. DC load resistor Converter AC side capacitor, 5. System connect reactor, 6. Resonant filter 7. Phase lock loop (PLL) sample voltage divider.

The waveform results after reaching steady state are shown below:

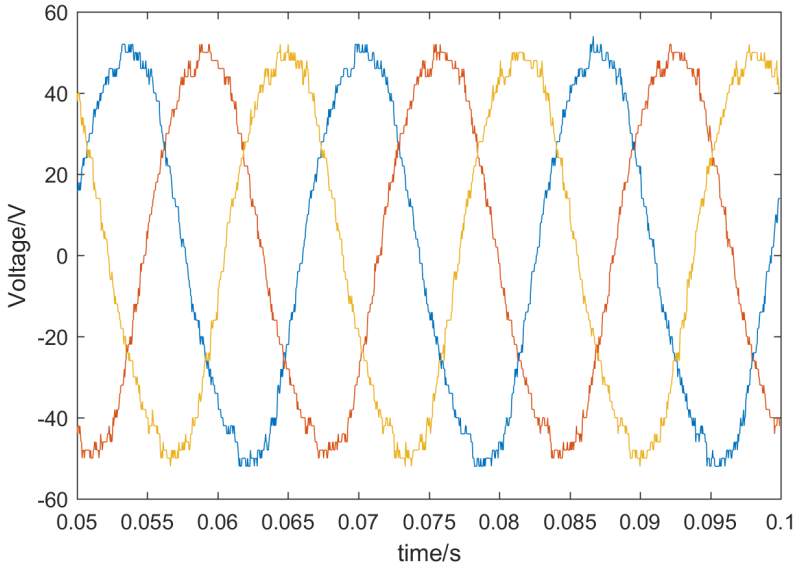

Figure 4.3: Converter output AC voltage.

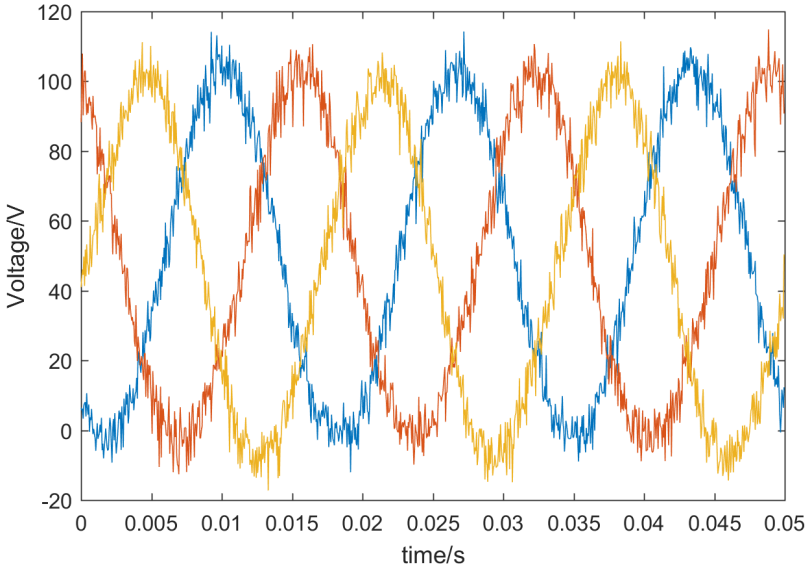

Figure 4.4: Converter valve voltage.

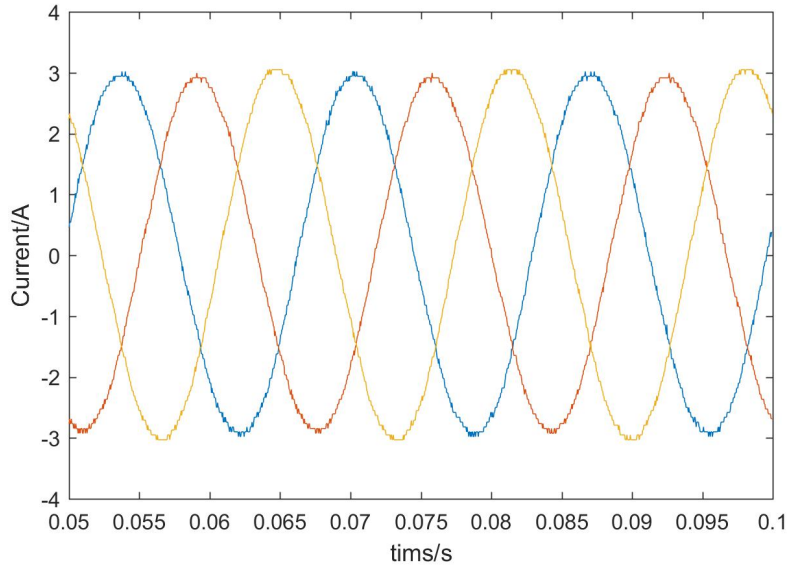

Figure 4.5: Converter output AC current.

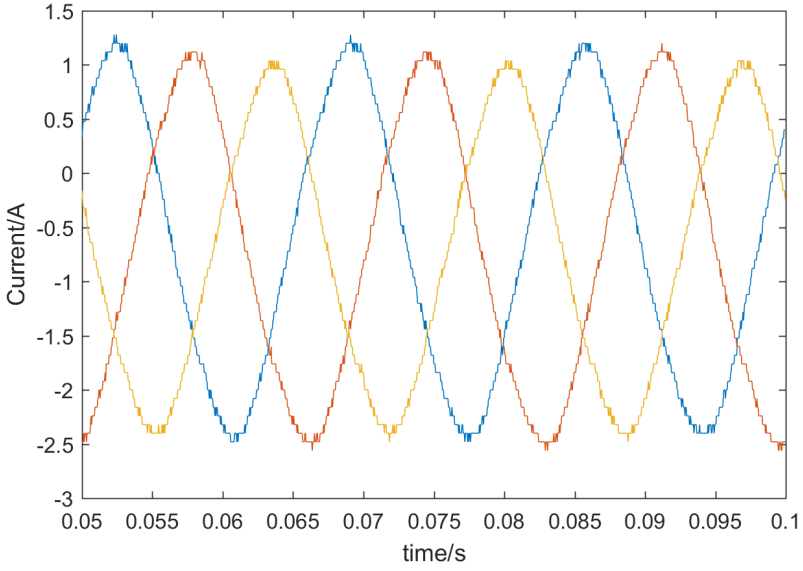

Figure 4.6: Converter valve current.

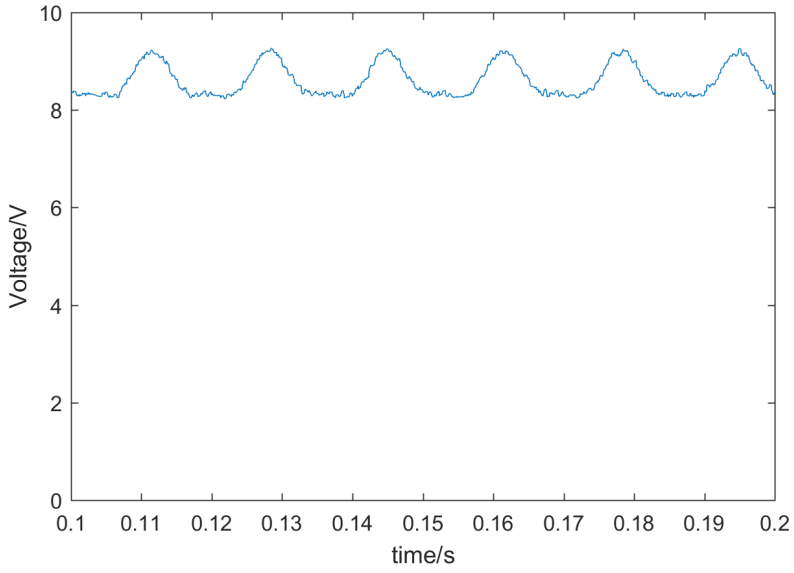

Figure 4.7: Average submodule voltage.

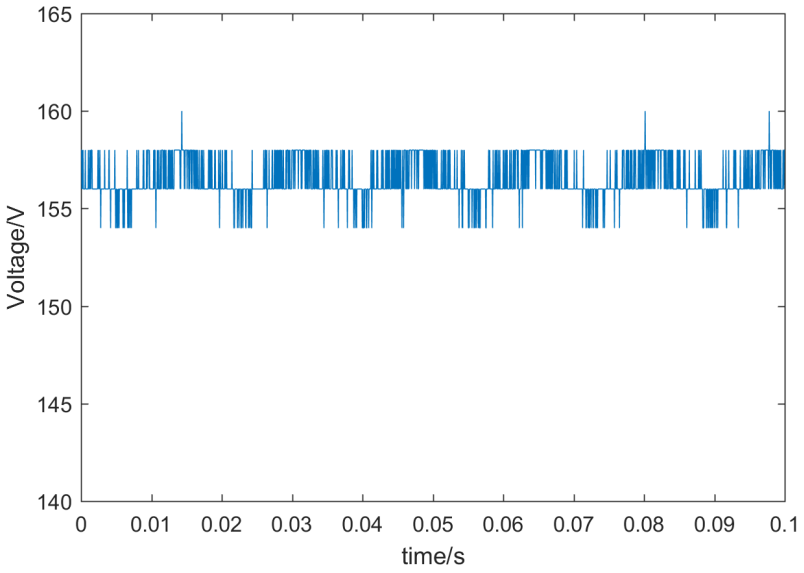

Figure 4.8: DC load voltage.

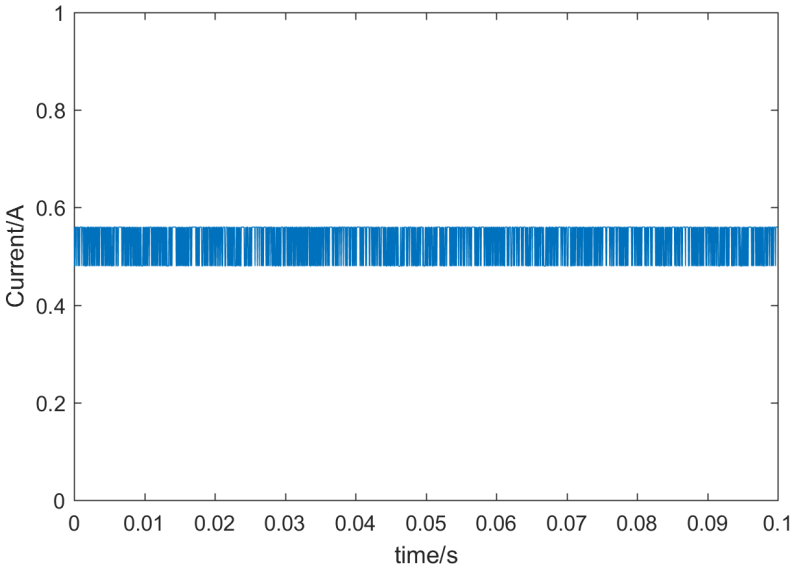

Figure 4.9: DC load current.

The temperature of DC load resistor is measured to monitor the heating process on the load. After reaching steady state, the load resistor temperature rises from 30°C to 40°C in 5 minutes as shown in Figure 4.10.

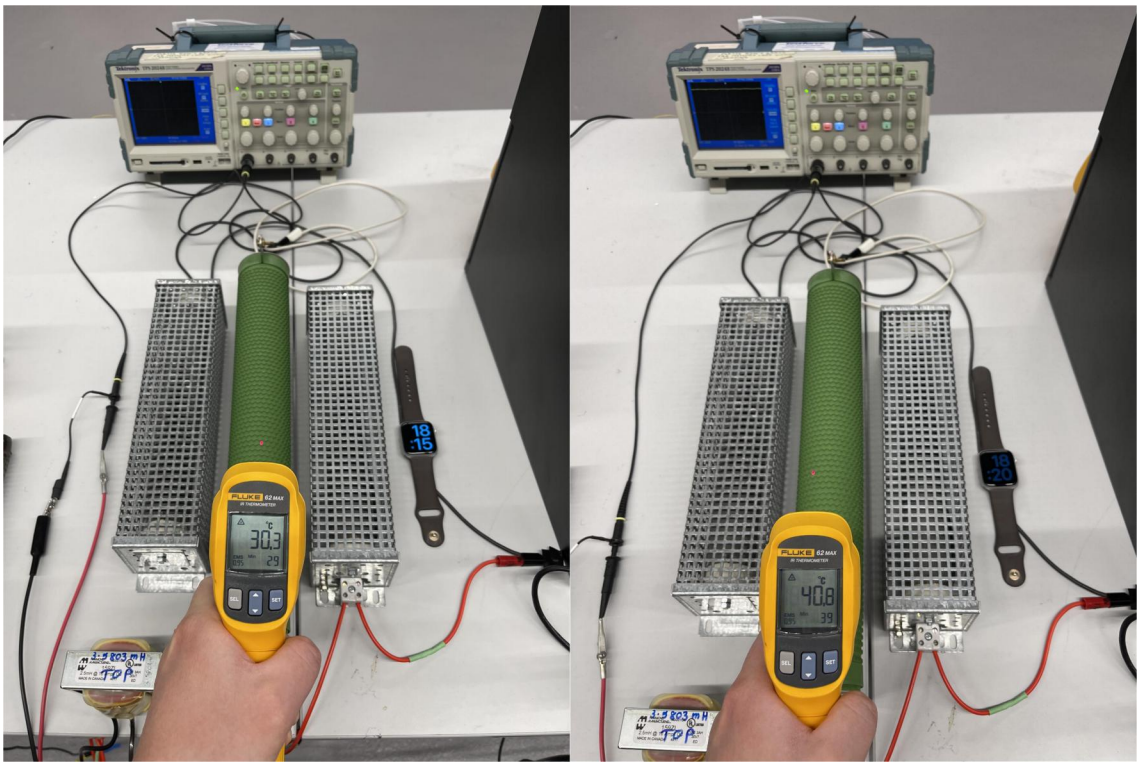

Figure 4.10: DC load resistor temperature before heating (left) and after heating (right).

4.3 Hardware validation of 2HCSC controller

This section will validate the 2nd harmonic current suppression controller (2HCSC) for SAMMC proposed in subsection 2.3.3.

The same Hardware-in-loop (HIL) testing system with RTDS introduced in the previous subsection is used to validate 2HCSC controller. SAMMC output line currents and phase voltages before and after 2HCSC controller is enabled are compared and analyzed to prove the proposed 2HCSC works in real-world hardware application.

Both of the two hardware cases with and without 2HCSC controller enabled run under the same operation point. This operation point is recorded by the table below, Table 4.3:

Table 4.3: Lab-scale SAMMC rectifier setup for 2HCSC hardware validation.

Parameter	Value	Unit
Number of SM per valve	10	-
Valve inductor	5.1	mH
AC side capacitor	312	mF
DC resistive load	236	Ω
AC input voltage	40	V
Modulation index	1	-
Modulation waveform phase angle	50	degree

A comparison between the converter output current before and after 2HCSC controller is enabled is shown in Figure 4.11:

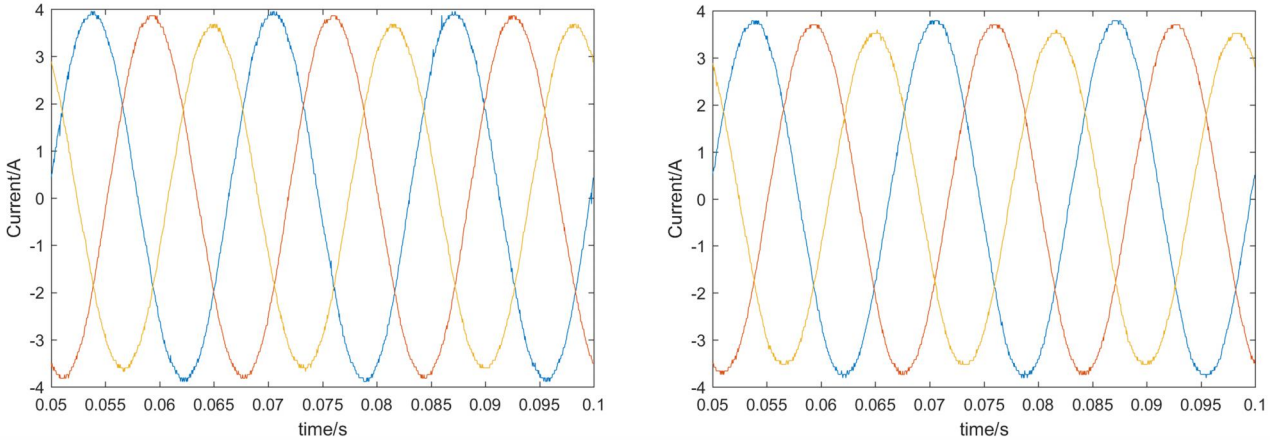

Figure 4.11: Comparison of SAMMC output current before 2HCSC enabled (left) and after 2HCSC enabled (right).

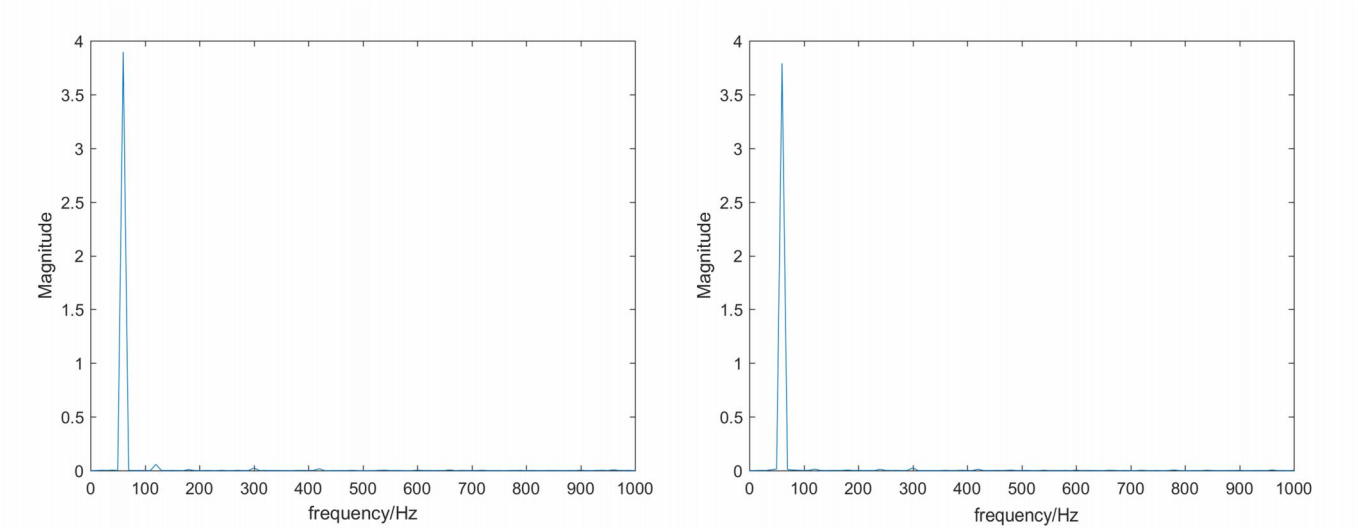

Figure 4.12: Harmonics spectrum of output current before 2HCSC enabled (left) and after 2HCSC enabled (right).

The THD of phase A output current before 2HCSC controller is enabled is 2.11%, while the THD of phase A output current before 2HCSC controller is enabled is 1.58%. In other words, after applying the 2HCSC controller, the 2nd component of output current is eliminated, the output current THD is reduced by 25%. The effectiveness of 2HCSC will increase when current increasing.

Chapter 5

Contributions, Conclusions and Future work

5.1 Contributions and conclusions

Proposed in 2018, SAMMC is a relatively new topology, so far, the characteristics of this converter topology are not well researched. This thesis discussed several details about this converter, including its operating principles, parameter designs, and harmonics performance. Compared with conventional MMCs, it is particularly suitable for low-power applications. So, a novel case study of SAMMC application: low power rectifier for DC deicing was given out. The major contributions and conclusions are:

1. Developed a harmonics calculation model to help design the converter's SM capacitance and valve inductor. An iterative calculation method is proposed to improve the accuracy. The model is validated by comparing calculation results and simulation results. The error of calculation results are less than 5%.

2. Proposed a 2nd harmonic current suppression controller (2HCSC) to eliminate the 2nd harmonics of the converter. The controller injects 2nd order signal to modulation waveform to remove 2nd order components from valve voltage. The controller is tested in both EMT

simulation and hardware-in-loop (HIL) test, results shows the output current THD can be reduced by up to 79% (depending on the operating condition).

3. Provided a guideline for SAMMC DC deicer system design. Using a mathematical model, the impact of several key parameters (transformer secondary side voltage rating, transformer impedance, AC side capacitor) are investigated on the deicer system.

4. Developed a Hardware-in-loop test with lab-scale MMC submodules and RTDS. The hardware is used to validate the operation and 2HCSC of SAMMC converter.

5.2 Future work

1. The small-signal stability of the controllers proposed in this thesis to control SAMMC converter are not studied. The PI controllers' gain and time constants may not be tuned to the best value to achieve optimal controlling performance.

2. The DC deicer rectifier is a very low power application (5-10 MVA). However, SAMMC is capable to transfer a much larger power (for example, as an HVDC power tap or grid connection inverter). So it is valuable to study the performance and dynamics of SAMMC in a standard power system in the future.

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Appendix A

Implementation of iterative SAMMC current harmonics calculation algorithm

A.1 Mathematical model of SAMMC iterative current harmonics calculation

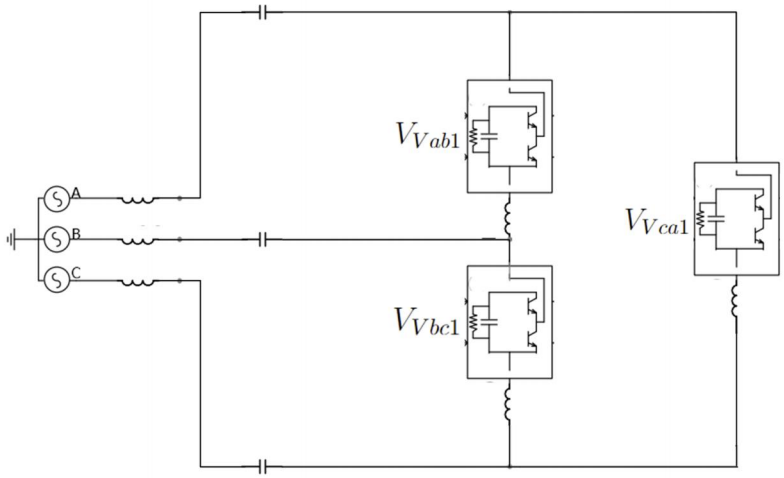

Figure A.1: Fundamental current response equivalent circuit.

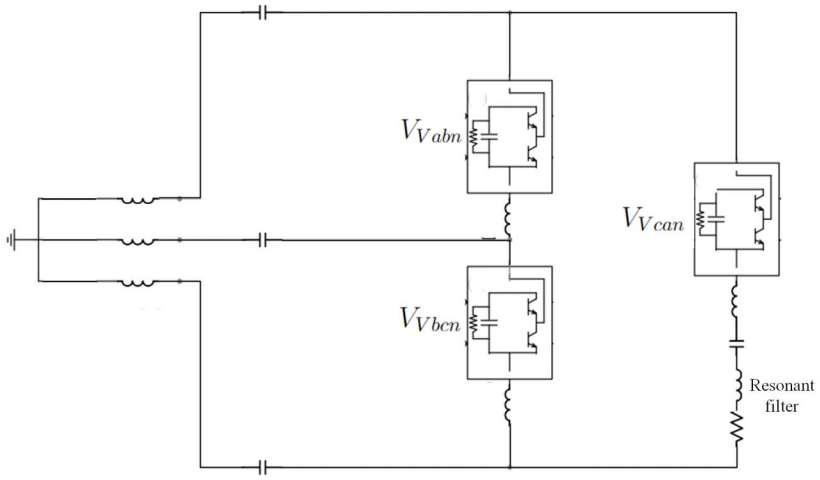

Figure A.2: n-th harmonic current response equivalent circuit.

Figure 2.9 is the AC equivalent circuit of the fundamental frequency component, AC power system is a 60Hz ideal voltage source, and V_{Vab1}, V_{Vbc1}, V_{Vca1} are the fundamental frequency component of valve voltages. Figure 2.10 is the sub-circuit for n-th order harmonic component, and V_{Vabn}, V_{Vbcn}, V_{Vcan} are the n-th order components in voltage V_{Vab}, V_{Vbc}, V_{Vca}.

To solve the harmonic current sub-circuits, three valve voltages and each frequency component of them need to be calculated. From (2.4), the valve voltage is decided by the average SM capacitor voltage in the valve and the modulation waveform. As for the modulation waveform, it is a purely sinusoidal waveform (for the condition without 2nd current harmonic suppression controller). Moreover, the steady state average SM capacitor voltage is decided by the current flowing through the valve, can be described as:

$$\Delta Vcsm_k(t) = \frac{1}{NC_{sm}} \int_0^t N \cdot wv_k(t) \cdot i_k(t)\, dt \tag{A.1}$$

where k is the notation of each arm AB, BC, CA. From (2.3), $wv_{ab}(t)$, $wv_{bc}(t)$ and $wv_{ca}(t)$ are the modulation waveforms for three valves.

After obtaining the expression of the valve voltage, a certain current harmonic with the corresponding valve voltage component in the sub-circuit can be calculated using the mesh

current method. The diagram for calculating n-th harmonic is shown in Figure A.3.

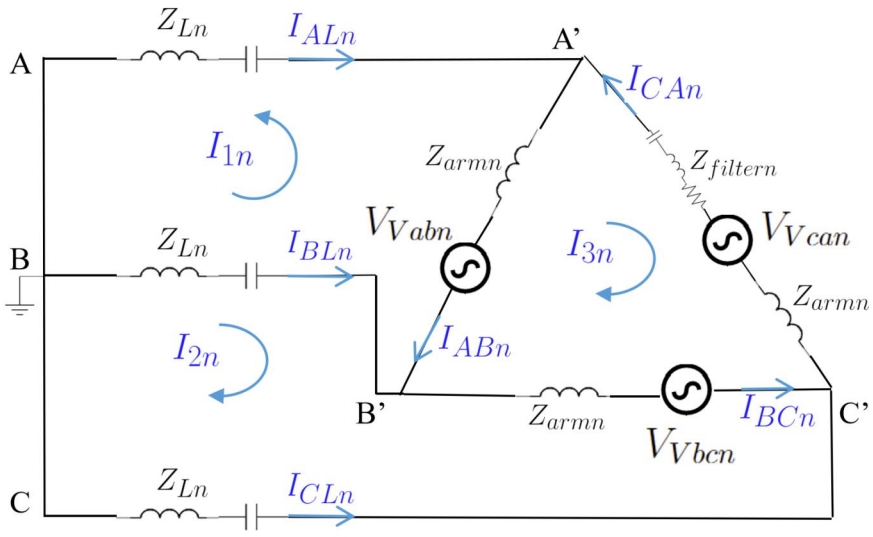

Figure A.3: Mesh current diagram for the n-th order current equivalent circuit.

In this figure, Z_{Ln} is the impedance of transformer and AC capacitor for n-th order current; Z_{armn} is the impedance of valve inductor for n-th order current; $Z_{filtern}$ is the impedance of resonant filter for n-th order current. I_{1n}, I_{2n} and I_{3n} is the mesh current for the three meshes in the circuit. Three line current I_{ALn}, I_{BLn} and I_{CLn} are three line currents which can be denoted as $-I_{1n}$, $I_{1n} + I_{2n}$ and $-I_{2n}$; and three arm currents I_{ABn}, I_{BCn} and I_{CAn} can be denoted as $-I_{1n} - I_{3n}$, $I_{2n} - I_{3n}$ and $-I_{3n}$.

The mesh current method is based on Kirchhoff's Voltage Law (KVL) and superposition theorem [38]. The circuit topology is divided into a few fundamental loops. The KVL equation for three loops in Figure A.3 is shown below:

$$\begin{aligned} I_{1n} \cdot (2Z_{Ln} + Z_{armn}) + I_{2n}Z_{Ln} + I_{3n}Z_{armn} &= V_{Vabn} \\ I_{2n} \cdot (2Z_{Ln} + Z_{armn}) + I_{1n}Z_{Ln} - I_{3n}Z_{armn} &= -V_{Vbcn} \\ I_{3n} \cdot (3Z_{Ln} + Z_{filtern}) + I_{1n}Z_{armn} - I_{2n}Z_{armn} &= V_{Vabn} + V_{Vbcn} + V_{Vcan} \end{aligned} \tag{A.2}$$

The three equations in (A.2) can be rearranged into matrix form as follows:

$$\begin{bmatrix} 2Z_{Ln}+Z_{armn} & Z_{Ln} & Z_{armn} \\ Z_{Ln} & 2Z_{Ln}+Z_{armn} & -Z_{armn} \\ Z_{armn} & -Z_{armn} & 3Z_{Ln}+Z_{filtern} \end{bmatrix} \cdot \begin{bmatrix} I_{1n} \\ I_{2n} \\ I_{3n} \end{bmatrix} = \begin{bmatrix} V_{Vabn} \\ -V_{Vbcn} \\ V_{Vabn}+V_{Vbcn}+V_{Vcan} \end{bmatrix} \quad \text{(A.3)}$$

Denote the matrix
$\begin{bmatrix} 2Z_{Ln}+Z_{armn} & Z_{Ln} & Z_{armn} \\ Z_{Ln} & 2Z_{Ln}+Z_{armn} & -Z_{armn} \\ Z_{armn} & -Z_{armn} & 3Z_{Ln}+Z_{filtern} \end{bmatrix}$ as $\mathbf{Z}_n$, matrix $\begin{bmatrix} I_{1n} \\ I_{2n} \\ I_{3n} \end{bmatrix}$
as $\mathbf{Iloop}_n$ and matrix
$\begin{bmatrix} V_{Vabn} \\ -V_{Vbcn} \\ V_{Vabn}+V_{Vbcn}+V_{Vcan} \end{bmatrix}$
as $\mathbf{Vloop}_n$ in the rest of this thesis. While $\mathbf{Vloop}_n$ can be described as a linear transformation of valve voltage vector

$$\mathbf{Vv}_n = \begin{bmatrix} V_{Vabn} \\ V_{Vbcn} \\ V_{Vcan} \end{bmatrix}$$

with

$$\begin{bmatrix} V_{Vabn} \\ -V_{Vbcn} \\ V_{Vabn}+V_{Vbcn}+V_{Vcan} \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{Vab} \\ V_{Vbcn} \\ V_{Vcan} \end{bmatrix},$$

where the coefficient matrix
$\begin{bmatrix} 1 & 0 & 0 \\ 0 & -1 & 0 \\ 1 & 1 & 1 \end{bmatrix}$
is denoted as $\mathbf{CV}$.

According to (A.3), the loop currents for the n-th order current can be easily obtained by:

$$\mathbf{Iloop}_n = \mathbf{Z}_n^{-1} \cdot \mathbf{Vloop}_n = \mathbf{Z}_n^{-1} \cdot \mathbf{CV} \cdot \mathbf{Vv}_n \tag{A.4}$$

Keeping in mind that the loop currents are not the final current results, the line currents and valve currents can be obtained from the equations below:

$$\begin{aligned} I_{ALn} &= -I_{1n} \\ I_{BLn} &= I_{1n} + I_{2n} \\ I_{CLn} &= -I_{2n} \end{aligned} \tag{A.5}$$

$$\begin{aligned} I_{ABn} &= -I_{1n} - I_{3n} \\ I_{BCn} &= I_{2n} - I_{3n} \\ I_{CAn} &= -I_{3n} \end{aligned} \tag{A.6}$$

(A.5) and (A.6) can also be rearranged into matrix equation format:

$$\begin{bmatrix} I_{ALn} \\ I_{BLn} \\ I_{CLn} \end{bmatrix} = \begin{bmatrix} -1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_{1n} \\ I_{2n} \\ I_{3n} \end{bmatrix} \tag{A.7}$$

and

$$\begin{bmatrix} I_{ABn} \\ I_{BCn} \\ I_{CAn} \end{bmatrix} = \begin{bmatrix} -1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 0 & -1 \end{bmatrix} \cdot \begin{bmatrix} I_{1n} \\ I_{2n} \\ I_{3n} \end{bmatrix} \tag{A.8}$$

To simplify the notations, denote the matrix $\begin{bmatrix} I_{ALn} \\ I_{BLn} \\ I_{CLn} \end{bmatrix}$ as $\mathbf{IL}_n$, the coefficient matrix

$\begin{bmatrix} -1 & 0 & 0 \\ 1 & 1 & 0 \\ 0 & -1 & 0 \end{bmatrix}$ as **CL**; matrix $\begin{bmatrix} I_{ABn} \\ I_{BCn} \\ I_{CAn} \end{bmatrix}$ as $\mathbf{Iarm}_n$, and the coefficient matrix $\begin{bmatrix} -1 & 0 & -1 \\ 0 & 1 & -1 \\ 0 & 0 & -1 \end{bmatrix}$ as **CA**. Thus (A.7) and (A.8) can be rewritten as:

$$\mathbf{IL}_n = \mathbf{CL} \cdot \mathbf{Iloop}_n \tag{A.9}$$

$$\mathbf{Iarm}_n = \mathbf{CA} \cdot \mathbf{Iloop}_n \tag{A.10}$$

In summary, the expressions of valve voltages for each harmonic component can be obtained from (2.4) and (A.1). Then, from (A.4)-(A.10), the current harmonic results are derived from valve voltage expressions. The input values for harmonic current calculation are: the topology of SAMMC circuit, SM capacitance C_{sm}, three-phase modulation waveforms $wv_k(t)$ and arm currents $i_k(t)$. However, when designing the SAMMC converter, only the DC ($i_{k0}(t)$) and fundamental components ($i_{k1}(t)$) of $i_k(t)$ are known. In other words, the full expression of input $i_k(t)$, including DC, fundamental component and other harmonics is an unknown value. However, according to (A.1), it can be shown that arm current harmonics do impact valve voltage harmonics. If this impact is ignored, the harmonics mathematical model will lose accuracy.

An iterative method is developed here to figure out the accurate expression of $i_k(t)$ with only DC and fundamental components. An iterative method is used to solve functions with fixed-points. In mathematics, a function with a fixed point is a function by which independent variable can be mapped back to itself by the function. This kind of function can be described as $f(c) = c$. The following equations and descriptions show how to fit the current harmonics problem into a fixed-point function problem. From (2.4) and (A.1), it is shown that valve voltages can be expressed as a non-linear function of valve currents. This thesis denote this relationship as a function:

$$\mathbf{Vv}_n = f_1(\mathbf{Iarm}_n) \tag{A.11}$$

Also from (A.3)-(A.8), the valve current is a linear function of the valve voltage:

$$\mathbf{Iarm}_n = f_2(\mathbf{Vv}_n) \tag{A.12}$$

Simultaneous functions (A.11) and (A.12) yield:

$$f_2(f_1(\mathbf{Iarm}_n)) = \mathbf{Iarm}_n \tag{A.13}$$

To simplify (A.13), this thesis uses $g(x)$ to denote $f_2(f_1(x))$. So the function of valve current vector **Iarmn** can be constrained by a fixed-point function:

$$g(\mathbf{Iarm}_n) = \mathbf{Iarm}_n \tag{A.14}$$

It is evident that function $g(x)$ have infinite fixed-points since there are infinite possible fundamental valve current $i_{k1}(t)$. When the operation point is fixed, for a concrete fundamental valve current $i_{k1}(t)$ input, there is only one fixed-point result: the full frequency valve current $i_k(t)$.

The iterative method for solving the fixed-point function $g(x)$ is shown below. The DC and fundamental components of valve current (i_{k0}+i_{k1}) are selected as initial values for the iteration i_k^0). Then the result of $g(i_k^0) = i_k^1$ is selected as the independent variable for the next round of calculation. The results will converge gradually, and when the error $i_k^k - i_k^{k-1}$ becomes smaller than a certain threshold, the iterative procedure is stopped. The numerical description for this iterative method is as follows:

$$i_k^1 = g(i_k^0)$$

$$i_k^2 = g(i_k^1)$$

$$i_k^3 = g(i_k^2)$$

.....

$$i_k^k - i_k^{k-1} < err$$

A.2 Implementation of iterative current harmonics calculation algorithm

From [44], the majority of valve current harmonics in an MMC valve consists of 2nd harmonic. Under this consideration, not all the harmonics will be considered in the mathematical model. Only 2nd and 3rd harmonics will be included when programming the harmonics mathematical model to simplify this problem.

As described in (A.14), to implement the iterative harmonics method, the expression of the fixed-point function $g(x)$, or $f1(x)$ and $f2(x)$ need to be found out. As stated before, the whole AC circuit of the SAMMC is divided into several sub-circuits, each of which only contains a single frequency component. Correspondingly, when focusing on 2nd and 3rd harmonics, function $g(x)$ can be decoupled into $g_2(x)$ and $g_3(x)$, which contains the numerical relationship for 2nd harmonics component and 3rd current harmonics, respectively.

From (A.13) and (A.14), $g_2(x)$ and $g_3(x)$ can also be written as $f_{22}(f_{21}(x))$ and $f_{32}(f_{31}(x))$. To find out $g(x)$, four functions: $f_{22}(x)$, $f_{21}(x)$, $f_{32}(x)$ and $f_{31}(x)$ need to be found out.

First find out $f_{22}(x)$ and $f_{32}(x)$. $f_{n2}(x)$ describes the function from valve voltage to arm current for n-th order harmonics. From (A.4) and (A.10), the expression of $f_{n2}(x)$ can be written as:

$$\mathbf{Iarm}_n = f_{n2}(\mathbf{Vv}_n) = \mathbf{CA} \cdot \mathbf{Z}_n^{-1} \cdot \mathbf{CV} \cdot \mathbf{Vv}_n \tag{A.15}$$

After obtaining $f_{n2}(x)$, $f_{n1}(x)$ ($f_{21}(x)$ and $f_{31}(x)$) need to be found. $f_{n1}(x)$ is the function from arm currents to valve voltages for n-th order harmonics, this relationship is described in (2.4) and (A.1). By denoting the DC component of valve currents as I_{dc}, the fundamental component of three-phase valve currents as $\frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta - \varphi)$, $\frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta - \frac{2\pi}{3} - \varphi)$, $\frac{\sqrt{2}}{\sqrt{3}} I_L \sin(\omega t - \theta + \frac{2\pi}{3} - \varphi)$, the three-phase 2nd harmonic component as $I_{2nd1} \sin(2\omega t + \theta_{2nd1})$, $I_{2nd2} \sin(2\omega t + \theta_{2nd2})$, $I_{2nd3} \sin(2\omega t + \theta_{2nd3})$, the 3rd harmonic component as $I_{3rd1} \sin(3\omega t + \theta_{3rd1})$, $I_{3rd2} \sin(3\omega t + \theta_{3rd2})$, $I_{3rd3} \sin(3\omega t + \theta_{3rd3})$. Substituting these terms into ((2.4) and (A.1), the full expression of valve voltages can be written as:

$$
\begin{aligned}
V_{Vab}(t) &= n_{AB}(t)\cdot\Big(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t n_{AB}(t)\cdot\Big(-I_{dc}+\frac{\sqrt{2}}{\sqrt{3}}I_L\sin(\omega t-\theta-\varphi)\Big)\\
&+ I_{2nd1}\sin(2\omega t+\theta_{2nd1})+I_{3rd1}\sin(3\omega t+\theta_{3rd1})\Big)\\
&= \frac{N}{2}(1+m\sin(\omega t-\theta))\cdot\Big(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t\frac{N}{2}(1+m\sin(\omega t-\theta))\cdot(-I_{dc}\\
&+\frac{\sqrt{2}}{\sqrt{3}}I_L\sin(\omega t-\theta-\varphi)+I_{2nd1}\sin(2\omega t+\theta_{2nd1})+I_{3rd1}\sin(3\omega t+\theta_{3rd1}))\,dt\\
&= \frac{V_{dc}}{3}(1+m\sin(\omega t-\theta))+\frac{N}{4C_{sm}}\Bigg[-\frac{\sqrt{2}}{\omega\sqrt{3}}I_L\cos(\omega t-\varphi-\theta)+\frac{mI_{dc}}{\omega}\cos(\omega t-\theta)\\
&-\frac{m}{2\sqrt{6}\omega}I_L\sin(2\omega t-\varphi-2\theta)-\frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1})-\frac{I_{3rd1}}{3\omega}\cos(3\omega t+\theta_{3rd1})\\
&+\frac{mI_{2nd1}}{2\omega}\sin(\omega t+\theta_{2nd1}+\theta)-\frac{mI_{2nd1}}{6\omega}\sin(3\omega t+\theta_{2nd1}-\theta)+\frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)\\
&-\frac{mI_{3rd1}}{8\omega}\sin(4\omega t+\theta_{3rd1}-\theta)\Bigg]+\frac{Nm}{4C_{sm}}\Bigg[-\frac{\sqrt{6}}{6\omega}I_L\sin(2\omega t-\varphi-2\theta)-\frac{\sqrt{6}}{6\omega}\sin(\varphi)\\
&+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\varphi)-\frac{mI_L}{4\sqrt{6}\omega}(\cos(\omega t+\varphi)-\cos(3\omega t-\varphi-3\theta))\\
&-\frac{I_{2nd1}}{4\omega}(\sin(3\omega t-\theta+\theta_{2nd1})-\sin(\omega t+\theta_{2nd1}+\theta))-\frac{I_{3rd1}}{6\omega}(\sin(4\omega t-\varphi+\theta_{3rd1})\\
&-\sin(2\omega t+\theta_{3rd1}+\theta))+\frac{mI_{2nd1}}{4\omega}(\cos(2\theta+\theta_{2nd1})-\cos(2\omega t+\theta_{2nd1}))\\
&-\frac{mI_{2nd1}}{12\omega}(\cos(2\omega t+\theta_{2nd1})-\cos(4\omega t+\theta_{2nd1}-2\theta))\\
&+\frac{mI_{3rd1}}{8\omega}(\cos(\omega t+\theta_{3rd1}+2\theta)-\cos(3\omega t+\theta_{3rd1}))\\
&-\frac{mI_{3rd1}}{16\omega}(\cos(3\omega t+\theta_{3rd1})\cos(5\omega t-2\theta+\theta_{3rd1}))\Bigg]
\end{aligned}
$$

$$
\begin{aligned}
V_{Vbc}(t) &= n_{BC}(t)\cdot(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t n_{BC}(t)(-I_{dc}+\frac{\sqrt{2}}{\sqrt{3}}I_L\sin(\omega t-\theta-\varphi-\frac{2\pi}{3})\\
&+ I_{2nd2}\sin(2\omega t+\theta_{2nd2})+I_{3rd2}\sin(3\omega t+\theta_{3rd2}))\\
&= \frac{N}{2}(1+m\sin(\omega t-\theta-\frac{2\pi}{3}))\cdot(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t\frac{N}{2}(1+m\sin(\omega t-\theta-\frac{2\pi}{3}))\cdot(-I_{dc}\\
&+ \frac{\sqrt{2}}{\sqrt{3}}I_L sin(\omega t-\theta-\varphi-\frac{2\pi}{3})+I_{2nd2}\sin(2\omega t+\theta_{2nd2})+I_{3rd2}\sin(3\omega t+\theta_{3rd2}))\,dt\\
&= \frac{V_{dc}}{3}(1+m\sin(\omega t-\theta-\frac{2\pi}{3}))+\frac{N}{4C_{sm}}\left[-\frac{\sqrt{2}}{\omega\sqrt{3}}I_L\cos(\omega t-\varphi-\theta-\frac{2\pi}{3})\right.\\
&+ \frac{mI_{dc}}{\omega}\cos(\omega t-\theta-\frac{2\pi}{3})\\
&- \frac{m}{2\sqrt{6}\omega}I_L\sin(2\omega t-\varphi-2\theta-\frac{4\pi}{3})-\frac{I_{2nd2}}{2\omega}\cos(2\omega t+\theta_{2nd2})\\
&- \frac{I_{3rd2}}{3\omega}\cos(3\omega t+\theta_{3rd2})+\frac{mI_{2nd2}}{2\omega}\sin(\omega t+\theta_{2nd2}+\theta+\frac{2\pi}{3})\\
&- \frac{mI_{2nd2}}{6\omega}\sin(3\omega t+\theta_{2nd2}-\theta-\frac{2\pi}{3})\\
&+ \left.\frac{mI_{3rd2}}{4\omega}\sin(2\omega t+\theta_{3rd2}+\theta+\frac{2\pi}{3})-\frac{mI_{3rd2}}{8\omega}\sin(4\omega t+\theta_{3rd2}-\theta-\frac{2\pi}{3})\right]\\
&+ \frac{Nm}{4C_{sm}}\left[-\frac{\sqrt{6}}{6\omega}I_L\sin(2\omega t-\varphi-2\theta-\frac{4\pi}{3})-\frac{\sqrt{6}}{6\omega}\sin(\varphi)+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\varphi-\frac{4\pi}{3})\right.\\
&- \frac{mI_L}{4\sqrt{6}\omega}(\cos(\omega t+\varphi-\frac{2\pi}{3})-\cos(3\omega t-\varphi-3\theta))-\frac{I_{2nd2}}{4\omega}(\sin(3\omega t-\theta+\theta_{2nd2}-\frac{2\pi}{3})\\
&- \sin(\omega t+\theta_{2nd2}+\theta+\frac{2\pi}{3}))-\frac{I_{3rd2}}{6\omega}(\sin(4\omega t-\varphi+\theta_{3rd2}-\frac{2\pi}{3})-\sin(2\omega t+\theta_{3rd2}+\theta+\frac{2\pi}{3}))\\
&+ \frac{mI_{2nd2}}{4\omega}(\cos(2\theta+\theta_{2nd2}+\frac{4\pi}{3})-\cos(2\omega t+\theta_{2nd2}))-\frac{mI_{2nd2}}{12\omega}(\cos(2\omega t+\theta_{2nd2})\\
&- \cos(4\omega t+\theta_{2nd2}-2\theta-\frac{4\pi}{3}))+\frac{mI_{3rd2}}{8\omega}(\cos(\omega t+\theta_{3rd2}+2\theta+\frac{4\pi}{3})-\cos(3\omega t+\theta_{3rd2}))\\
&- \left.\frac{mI_{3rd2}}{16\omega}(\cos(3\omega t+\theta_{3rd2})-\cos(5\omega t-2\theta+\theta_{3rd2}-\frac{4\pi}{3}))\right]
\end{aligned}
\tag{A.16}
$$

$$
\begin{aligned}
V_{Vca}(t) &= n_{CA}(t)\cdot(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t n_{CA}(t)(-I_{dc}+\frac{\sqrt{2}}{\sqrt{3}}I_L\sin(\omega t-\theta-\varphi+\frac{2\pi}{3})\\
&+ I_{2nd3}\sin(2\omega t+\theta_{2nd3})+I_{3rd3}sin(3\omega t+\theta_{3rd3}))\\
&= \frac{N}{2}(1+m\sin(\omega t-\theta+\frac{2\pi}{3}))\cdot(\frac{2V_{dc}}{3N}+\frac{1}{NC_{sm}}\int_0^t\frac{N}{2}(1+m\sin(\omega t-\theta+\frac{2\pi}{3}))\cdot(-I_{dc}\\
&+\frac{\sqrt{2}}{\sqrt{3}}I_L\sin(\omega t-\theta-\varphi+\frac{2\pi}{3})+I_{2nd3}\sin(2\omega t+\theta_{2nd3})+I_{3rd3}\sin(3\omega t+\theta_{3rd3}))\,dt\\
&= \frac{V_{dc}}{3}(1+m\sin(\omega t-\theta+\frac{2\pi}{3}))+\frac{N}{4C_{sm}}\left[-\frac{\sqrt{2}}{\omega\sqrt{3}}I_L\cos(\omega t-\varphi-\theta+\frac{2\pi}{3})\right.\\
&+\frac{mI_{dc}}{\omega}\cos(\omega t-\theta+\frac{2\pi}{3})\\
&-\frac{m}{2\sqrt{6}\omega}I_L\sin(2\omega t-\varphi-2\theta+\frac{4\pi}{3})-\frac{I_{2nd3}}{2\omega}\cos(2\omega t+\theta_{2nd3})-\frac{I_{3rd3}}{3\omega}\cos(3\omega t+\theta_{3rd3})\\
&+\frac{mI_{2nd3}}{2\omega}\sin(\omega t+\theta_{2nd2}+\theta-\frac{2\pi}{3})-\frac{mI_{2nd3}}{6\omega}\sin(3\omega t+\theta_{2nd3}-\theta+\frac{2\pi}{3})\\
&\left.+\frac{mI_{3rd3}}{4\omega}\sin(2\omega t+\theta_{3rd3}+\theta-\frac{2\pi}{3})-\frac{mI_{3rd3}}{8\omega}\sin(4\omega t+\theta_{3rd2}-\theta+\frac{2\pi}{3})\right]\\
&+\frac{Nm}{4C_{sm}}\left[-\frac{\sqrt{6}}{6\omega}I_L\sin(2\omega t-\varphi-2\theta+\frac{4\pi}{3})-\frac{\sqrt{6}}{6\omega}\sin(\varphi)+\frac{mI_{dc}}{2\omega}\sin(2\omega t-2\varphi+\frac{4\pi}{3})\right.\\
&-\frac{mI_L}{4\sqrt{6}\omega}(\cos(\omega t+\varphi+\frac{2\pi}{3})-\cos(3\omega t-\varphi-3\theta))-\frac{I_{2nd3}}{4\omega}(\sin(3\omega t-\theta+\theta_{2nd3}+\frac{2\pi}{3})\\
&-\sin(\omega t+\theta_{2nd3}+\theta-\frac{2\pi}{3}))-\frac{I_{3rd3}}{6\omega}(\sin(4\omega t-\varphi+\theta_{3rd3}+\frac{2\pi}{3})-\sin(2\omega t+\theta_{3rd3}+\theta-\frac{2\pi}{3}))\\
&+\frac{mI_{2nd3}}{4\omega}(\cos(2\theta+\theta_{2nd3}-\frac{4\pi}{3})-\cos(2\omega t+\theta_{2nd3}))-\frac{mI_{2nd3}}{12\omega}(\cos(2\omega t+\theta_{2nd3})\\
&-\cos(4\omega t+\theta_{2nd3}-2\theta+\frac{4\pi}{3}))+\frac{mI_{3rd3}}{8\omega}(\cos(\omega t+\theta_{3rd3}+2\theta-\frac{4\pi}{3})-\cos(3\omega t+\theta_{3rd3}))\\
&\left.-\frac{mI_{3rd3}}{16\omega}(\cos(3\omega t+\theta_{3rd3})-\cos(5\omega t-2\theta+\theta_{3rd2}+\frac{4\pi}{3}))\right]
\end{aligned}
$$

From (A.16), derive function $f_{21}(x) : \mathbf{Vv}_2 = f_{21}(\mathbf{Iarm}_0, \mathbf{Iarm}_1, \mathbf{Iarm}_2, \mathbf{Iarm}_3)$ for each valve

as:

$$
\begin{aligned}
V_{Vab2}(t) =& \frac{N}{4C_{sm}}\left(-\frac{3mI_{ph}}{2\sqrt{6}\omega}\sin(2\omega t-\varphi-2\theta)-\frac{I_{2nd1}}{2\omega}\cos(2\omega t+\theta_{2nd1})\right.\\
&+\frac{mI_{3rd1}}{4\omega}\sin(2\omega t+\theta_{3rd1}+\theta)+\frac{m^2I_{dc}}{2\omega}\sin(2\omega t-2\theta)+\\
&\frac{mI_{3rd1}}{6\omega}\sin(2\omega t+\theta_{3rd1}+\theta)-\frac{m^2I_{2nd1}}{4\omega}\cos(2\omega t+\theta_{2nd1})\\
&\left.-\frac{m^2I_{2nd1}}{12\omega}\cos(2\omega t+\theta_{2nd1})\right)\\
V_{Vbc2}(t) =& \frac{N}{4C_{sm}}\left(-\frac{3mI_{ph}}{2\sqrt{6}\omega}\sin(2\omega t-\varphi+120^\circ-2\theta)-\frac{I_{2nd2}}{2\omega}\cos(2\omega t+\theta_{2nd2})\right.\\
&+\frac{mI_{3rd2}}{4\omega}\sin(2\omega t+\theta_{3rd2}+\theta+120^\circ)+\frac{m^2I_{dc}}{2\omega}\sin(2\omega t-2\theta+120^\circ)\\
&+\frac{mI_{3rd2}}{6\omega}\sin(2\omega t+\theta_{3rd2}+\theta+120^\circ)-\frac{m^2I_{2nd2}}{4\omega}\cos(2\omega t+\theta_{2nd2})\\
&\left.-\frac{m^2I_{2nd2}}{12\omega}\cos(2\omega t+\theta_{2nd2})\right)\\
V_{Vca2}(t) =& \frac{N}{4C_{sm}}\left(-\frac{3mI_{ph}}{2\sqrt{6}\omega}\sin(2\omega t-\varphi-120^\circ-2\theta)-\frac{I_{2nd3}}{2\omega}\cos(2\omega t+\theta_{2nd3})\right.\\
&+\frac{mI_{3rd3}}{4\omega}\sin(2\omega t+\theta_{3rd3}+\theta-120^\circ)+\frac{m^2I_{dc}}{2\omega}\sin(2\omega t-2\theta-120^\circ)\\
&+\frac{mI_{3rd3}}{6\omega}\sin(2\omega t+\theta_{3rd3}+\theta-120^\circ)-\frac{m^2I_{2nd3}}{4\omega}\cos(2\omega t+\theta_{2nd3})\\
&\left.-\frac{m^2I_{2nd3}}{12\omega}cos(2\omega t+\theta_{2nd3})\right)
\end{aligned}
\tag{A.17}
$$

And function $f_{31}(x) : \mathbf{Vv}_3 = f_{31}(\mathbf{Iarm}_0, \mathbf{Iarm}_1, \mathbf{Iarm}_2, \mathbf{Iarm}_3)$ as:

$$
\begin{aligned}
V_{Vab3} =& \frac{N}{4C_{sm}} \left(-\frac{I_{3rd1}}{3\omega} \cos(3\omega t + \theta_{3rd1}) - \frac{mI_{2nd1}}{6\omega} \sin(3\omega t + \theta_{2nd1} - \theta) \right) \\
&+ \frac{Nm}{4C_{sm}} \left(\frac{mI_{ph}}{4\sqrt{6}\omega} \cos(3\omega t - \varphi - 3\theta) - \frac{I_{2nd1}}{4\omega} \sin(3\omega t - \theta + \theta_{2nd1}) \right. \\
&\left. - \frac{3mI_{3rd1}}{16\omega} \cos(3\omega t + \theta_{3rd1}) \right) \\
V_{Vbc3} =& \frac{N}{4C_{sm}} \left(-\frac{I_{3rd2}}{3\omega} \cos(3\omega t + \theta_{3rd2}) - \frac{mI_{2nd2}}{6\omega} \sin(3\omega t + \theta_{2nd2} - \theta - 120^\circ) \right) \\
&+ \frac{Nm}{4C_{sm}} \left(\frac{mI_{ph}}{4\sqrt{6}\omega} \cos(3\omega t - \varphi - 3\theta) - \frac{I_{2nd2}}{4\omega} \sin(3\omega t - \theta + \theta_{2nd2} - 120^\circ) \right. \\
&\left. - \frac{3mI_{3rd2}}{16\omega} \cos(3\omega t + \theta_{3rd2}) \right) \\
V_{Vca3} =& \frac{N}{4C_{sm}} \left(-\frac{I_{3rd3}}{3\omega} \cos(3\omega t + \theta_{3rd3}) - \frac{mI_{2nd3}}{6\omega} \sin(3\omega t + \theta_{2nd3} - \theta + 120^\circ) \right) \\
&+ \frac{Nm}{4C_{sm}} \left(\frac{mI_{ph}}{4\sqrt{6}\omega} \cos(3\omega t - \varphi - 3\theta) - \frac{I_{2nd3}}{4\omega} \sin(3\omega t - \theta + \theta_{2nd3} + 120^\circ) \right. \\
&\left. - \frac{3mI_{3rd3}}{16\omega} \cos(3\omega t + \theta_{3rd3}) \right)
\end{aligned}
\tag{A.18}
$$

After obtaining all the functions, the iterative converter harmonics calculation method is described as a flowchart: Figure A.4.

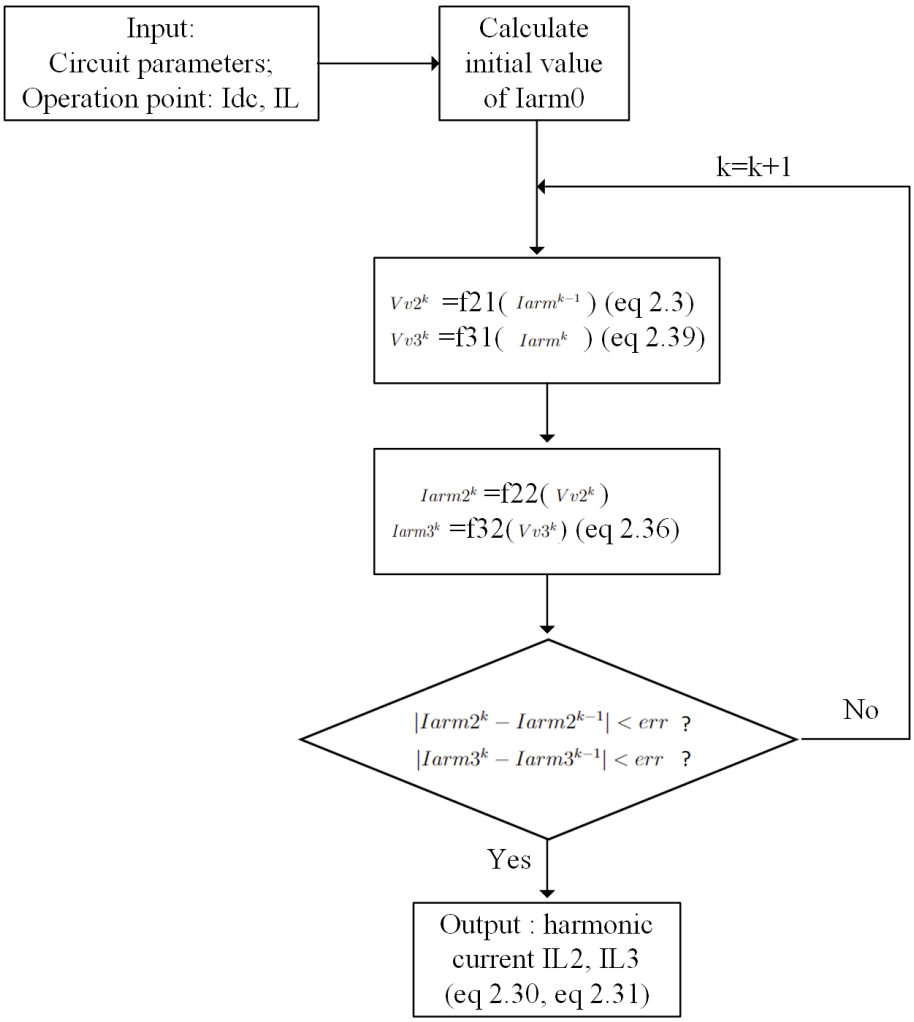

Figure A.4: Diagram of iterative converter harmonics calculation method procedure.