SATURATION CHARGE IN GRADED-BASE TRANSISTORS

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by

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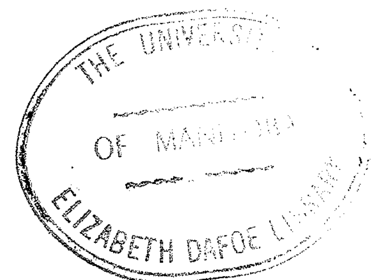

ABSTRACT

A new device configuration (called the inverted emitter-follower mode) is proposed in this thesis which gives remarkable reduction in saturation charge stored in bipolar transistors. Switching speed, loading capability, reliability, and stability are not affected by operating the transistor in this mode. Moreover, the active turn-on time is improved.

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To My wife Mradula

with affection and love.

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NOTATIONS

A	area of the emitter
A_C	area of the collector
b'	internal base contact
C	capacitance
c'	internal collector contact
C_B	base terminal capacitance
D_N	diffusion constant of electrons
D_p	diffusion constant of holes
ε	electric field
h_{FE}	common-emitter current gain
I, J	total current and current density
I_N, J_N	electron current and current density
I_p, J_p	hole current and current density
I_{pS}^*, J_{pS}^*	hole current and current density in the collector for $V_{C'B'} = 0$
I_{pS}, J_{pS}	hole current and current density in the collector region at the on-set of saturation
I_B	base current
I_{B_1}, I_{BS}	saturation base current
I_{BX}	excess base current
I_{B_2}	reverse base current
I_{CS}, I_{CM}	collector current at the edge of saturation
m	base-field factor
N_A	concentration of acceptor ions in the collector
$n(o)$	electron density in the collector at the edge of the collector depletion region
n_o	equilibrium electron density
$n(w_c)$	electron density at the collector contact

Notations (cont'd)

q	electron charge
Q	Active region charge in IEF-mode
Q_B	Active region base charge
Q_{BM}	Base charge at the edge of saturation
Q_{BS}	Base charge in saturation
Q_C	collector charge in saturation
Q_X	excess saturation charge
τ_F, τ_I	forward and reverse time constants
τ_x	excess storage time constant
t_s	saturation time
t_d, t_r, t_f	delay, rise and fall-time respectively
μ_N	mobility of electrons
μ_p	mobility of holes
w	base width
W_C	collector width
ω_F, ω_I	cut-off frequencies in forward and reverse mode.
α_F, α_I	forward and reverse common base current gains

CHAPTER I

INTRODUCTION

The importance of controlling saturation-charge storage in switching transistors is well recognized. The storage delay is caused by excess charge accumulation in the base and the collector regions of a saturated bipolar transistor. This saturation charge is related to the excess base current. Several circuit techniques have been developed either to eliminate this excess base current and thus, reduce saturation charge to zero, or to limit it below a known and controllable value. The use of limited-saturation devices and additional components in logic gates is more common to improve the switching speed [C.1]. But, reliability, cost, and loading capability are affected by these techniques. The saturation characteristics of a switching transistor can also be improved by using fabrication techniques. The gold doping is used to reduce the minority-carrier life time. But the technique lowers switching speed, current gain, and causes high leakage current. Heavily doped buried layers and collector contact improve the saturation characteristic. Moreover, capacitances increase as the area increases.

The proposed new circuit technique is a saturation charge control method. This technique does not need either extra fabrication techniques or any other additional components, nor are cost, reliability, and loading capability affected. Moreover, it reduces the saturation charge storage and improves the switching speed.

The physical model of a switching transistor is discussed in Chapter II. This physical model is similar to that proposed by BEALE and SLATTER [B.2]. Minority-carrier charge distribution, switching times and modes among other basic concepts are introduced in this chapter. Efforts are made in the next two chapters to deal with large-signal analysis of a graded base

transistor in the current saturation region and measuring techniques to determine saturation charge and excess storage time constant. Experimental results and discussion are the main theme in the fifth chapter. Mathematical proofs followed by discussions are introduced at each stage. The saturation charge, excess storage time constant, and speed in the inverted emitter-follower (IEF) mode are analysed in detail . Finally, the results and advantages of IEF mode are concluded in Chapter VI.

CHAPTER II

THE BIPOLAR TRANSISTOR AS A SWITCHING DEVICE

An ideal switching device has no power loss during switching operation and can change its state, say from the on to the off condition, in zero time. This simple definition requires that in the closed position the switch must have no voltage drop across its terminals. In the open position, the switch must suppress all current flow through the load. Finally, no time delay must exist between one switch setting and the other.

2.1 Static and Dynamic Properties:

A bipolar transistor switch is shown in Fig. 2.2a. Transistor limitation with respect to a perfect switch can easily be determined from the dc output characteristics in Fig. 2.1 and the waveform shown in Fig. 2.2b. It is evident from Fig. 2.1 that when the base current is zero, a small amount of collector current still flows in the circuit. This is called the collector leakage current and prevents full cut-off of load current. Similarly, the collector-emitter voltage is never zero in the on position of the switch. However, an application of reverse bias on the collector-base junction reduces the collector leakage current to its minimum value. And, secondly, advanced fabrication techniques give a very small collector-emitter voltage (called collector saturation voltage).

There are two situations in which an electronic device may have a zero power input requirement, yet still require a finite control signal. If the input impedance is infinite, a voltage is required for control. If the input impedance is zero, a current is required for control. In each case, no input power is required. A bipolar transistor has very low input impedance and is controlled by an input current signal. The input power requirements therefore, are very small.

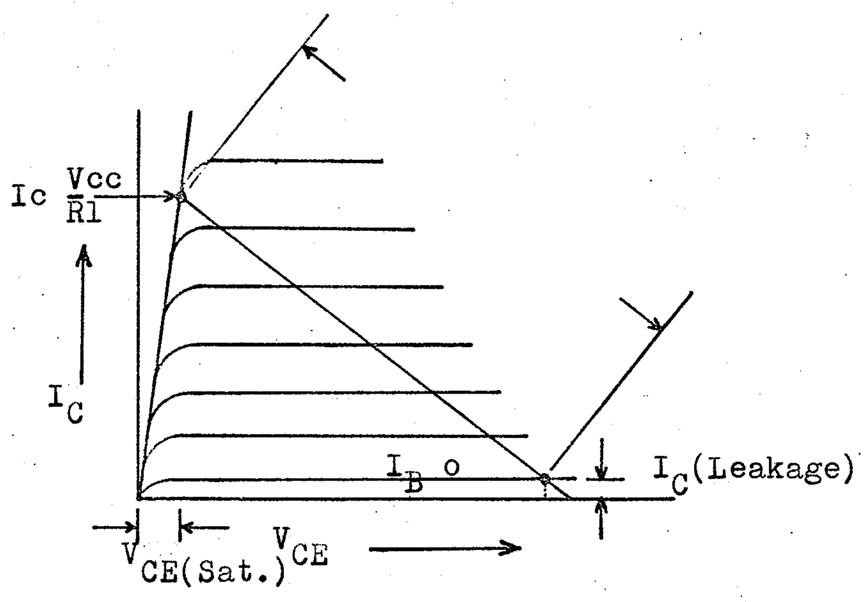


Fig.2.1- Transistor DC Output Characteristics.

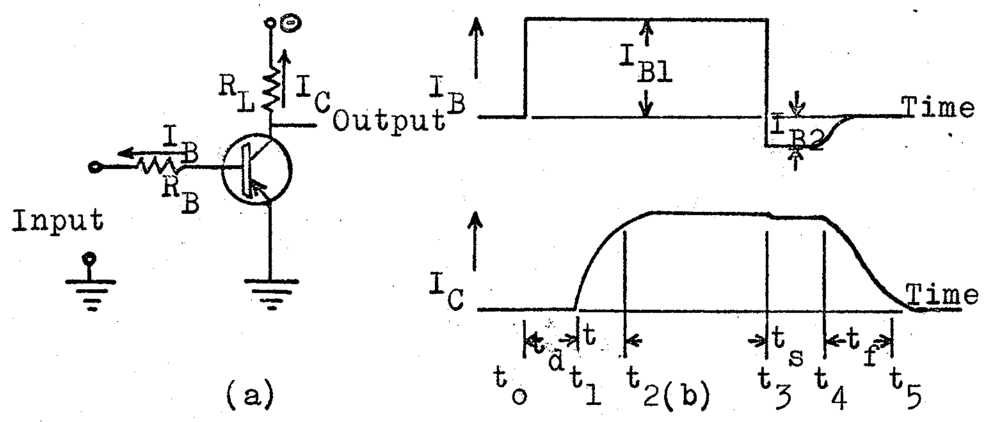


Fig.2.2 a- A Bipolar Transistor Switch.

Fig.2.2 b- Input and Output Response of Switch.

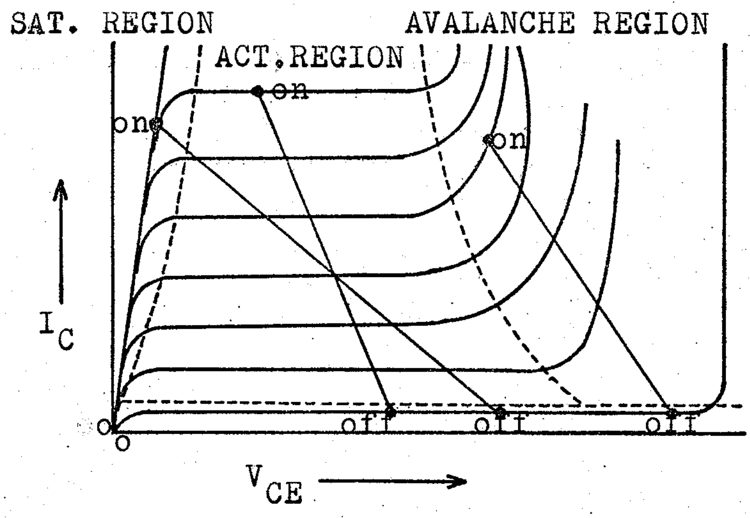


Fig.2.3- Operating Regions for Switching Modes.

In general, the dc characteristics of a bipolar transistor switch are very close to the ideal model, and it is possible to simulate the off and on conditions of a perfect switch even though it can never be realized as a perfect switch due to its dynamic limitations. These transient limitations are illustrated in Fig. 2.2b. This Figure presents the physical events which occur when a transistor is switched from off to on and then to off again.

As illustrated by the waveform, the output collector current pulse is far from being an exact replica of the input current pulse. At time t_o, a negative voltage pulse of sufficient amplitude is applied at the input and a base current I_{B1} starts to flow immediately. But it is to be observed that collector current does not begin to increase until time t_1. The interval between t_o and t_1 is called delay time (t_d) and is defined as the time required to bring the transistor from the initial off condition to the edge of conduction. At time t_1, the operating point of the transistor is at the beginning of the active region and the collector current starts to increase toward its saturation value. However, it takes a time to reach its maximum value. This time interval is shown from t_1 to t_2, and is defined as the rise time (t_r) of the collector current. The sume ($t_d + t_r$) is called turn-on time, t_{on}.

At time t_2, the operating point enters the current saturation region and the transistor will remain in this state as long as the input signal is maintained. At time t_3, the base current is reduced instantaneously to a value that effects cut-off of the device. It is observed that the collector current does not respond until time t_4. The time interval between t_3 and t_4 is referred to as the storage time (t_S). Finally, at time t_4, the transistor comes out of saturation and the collector current falls to its off value at t_5. The interval of time between t_4 and t_5 is defined as the fall time (t_f). The sum

$(t_s + t_f)$ is called turn-off time, t_{off}.

The delays in the output response are attributed to inherent properties of the bipolar transistor. These delays affect the switching speed of the device. This thesis is mostly concerned with the delay caused by storage time. The storage-time delay is contributed due to the excess minority-carrier charge storage and is a big limiting factor for high-speed switching operations. A new technique is proposed which gives reduced minority-carrier storage in the current saturation region.

2.2 Switching Modes

The bipolar transistor switching circuits generally fall into three basic categories, depending on their operating mode. These are broadly classified as saturated mode, current mode, and avalanche mode, and are determined by the portion of the transistor output characteristics utilized. Fig. 2.3 illustrates these operating regions.

The avalanche mode is seldom used due to operational difficulty in this negative resistance region and current mode never duplicates the perfect switch. In all current-mode circuits, transistor saturation is avoided by limiting the emitter current to a value that is less than the normal collector current limiting condition represented by Vcc/R_L. When designed for a specific load, excessive variations in load conditions could result in improper performance. If the load is too heavy, the available output voltage might be insufficient to assure proper turn-on of the succeeding stage, while if it is too light, it would be possible to enter the saturation region. Thus, the fixed load condition and complicated circuitry have limited the use of current mode switches in the logic circuits although they give a high switching speed.

The saturated mode is the only one which has enjoyed widespread popularity. It most nearly duplicate the function of an ideal switch. In the off condition, current through the switch is negligible. In the on condition, the transistor is driven into saturation and exhibits a virtual short circuit between emitter and collector terminals. It is capable of switching large amount of power with little device dissipation, i.e. it can withstand large voltages during the off condition and large currents during the on condition. It requires few parts and results in simple circuitry. However, because the transistor is driven into saturation, its switching speed is limited by minority-carrier storage delay time. Several techniques have been listed in the first chapter which reduce the minority-carrier charge storage. In each case, the aim is to overcome the storage time delay.

The most useful configuration for using a bipolar transistor in the saturated mode is the common-emitter configuration. The transistor has very large current and voltage gains in this configuration. It may be switched on with very little base drive and has negligible reverse saturation current. Fan-in and fan-out capabilities are large. Finally, the transistor can respond to driving signals instantaneously because it has a higher gain-bandwidth product in this configuration. The following switching modes can be realiaed in the same configuration:

(a) Normal mode,

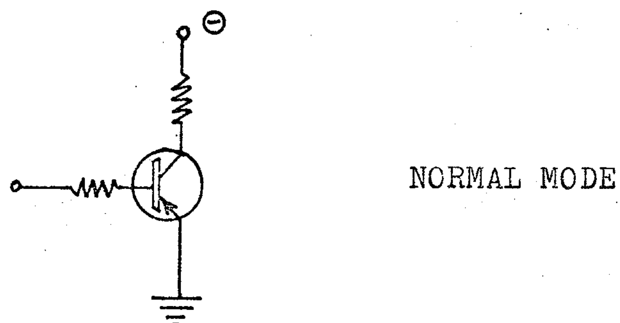
(b) Emitter-follower mode,

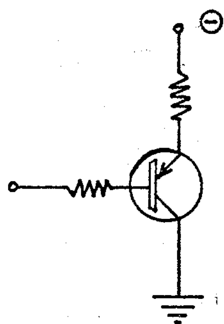
(c) Inverted mode, and

(d) Inverted emitter-follower mode.

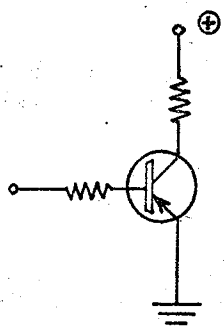
The circuit diagrams for these various switching modes are shown in Fig. 2.4.

The inverted emitter-follower mode is a new switching mode,

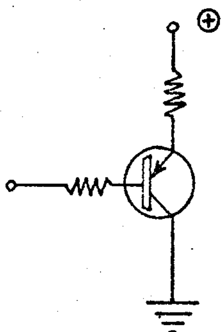




EF MODE



INVERTED MODE



IEF MODE

Fig.2.4- Switching Modes (Common-Emitter Configuration).

discovered by the author. It has a significant reduced charge storage and high switching speed.

2.3 Minority-Carrier Charge Distribtions

The operating range for a saturated bipolar transistor switch is illustrated in Fig. 2.3. Anderson [A.1] devided this large-signal operating range into three regions which are as follows:

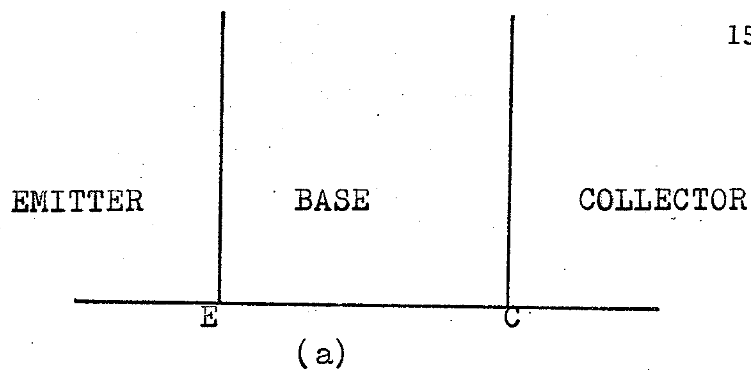
REGION I: (Collector current cut-off): Both the emitter and collector junctions are reverse biased. It is known as the off region.

REGION II: (Active): Emitter junction is forward biased and collector junction is reverse biased.

REGION III: (Collector current saturation or saturation): Both the emitter and collector junctions are forward biased.

It has been explained that storage time delay is caused by minority-carrier charge storage. Because this thesis is mainly concerned with the charge storage, the minority-carrier distribution in all the above operating regions are explained in detail. It is convenient to explain the dynamic behaviour of a bipolar transistor in terms of the charge distributions. As most of the modern switching transistors have graded-base structures, the charge distributions are considered only for this type of transistors. The charge distributions for other types of transistors can be found in the literature [B.4].

CUT-OFF REGION: The minority-carrier density in this regions is very nearly zero at both the emitter and collector junctions. Fig. 2.5b shows the charge distributions of a PNP transistor in the off state. It is assumed here that



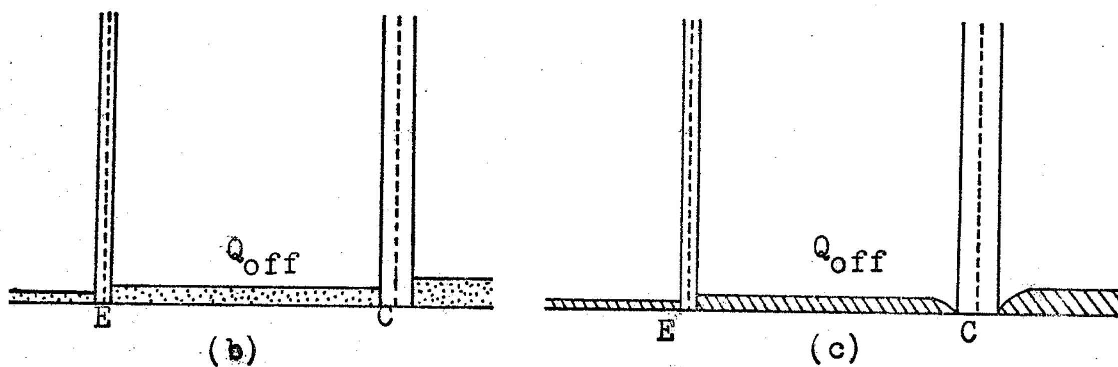


Fig.2.5- Minority-Carrier Charge Distributiob in Cut-Off Region.

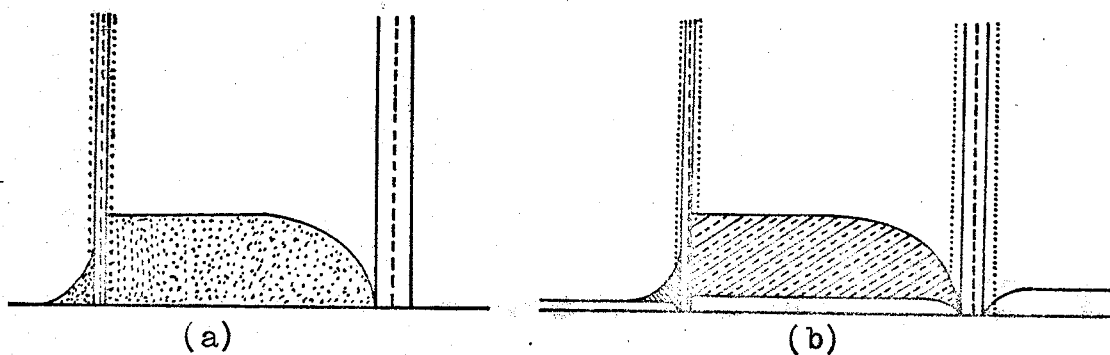


Fig.2.6- Minority-Carrier Charge Distribution in Active Region.

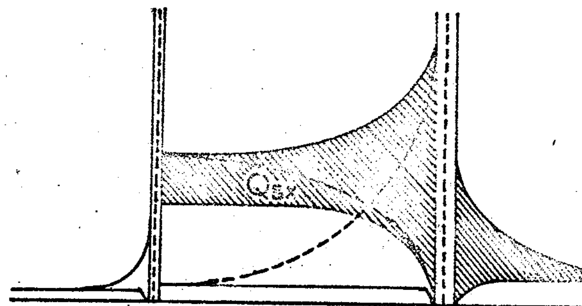


Fig.2.7- Minority-Carrier Charge Distribution in Saturation Region.

reverse saturation currents are zero for both junctions. If there is any reverse saturation (cut-off) current, a minority carrier gradient is maintained near the collector junction. This situation is shown in Fig. 2.5c.

ACTIVE REGION: Once the current starts to flow from emitter to collector, the minority-carrier injection takes place from emitter junction and a charge gradient is established in the base region. The current flow is directly proportional to this gradient. The charge constituted by minority carriers in the base region determines the internal dynamic behaviour of the transistor. If there is no recombination in the base region and the emitter injection efficiency is unity, a lossless injection of charge into the base will cause a continuous current flow from emitter to collector until the charge is removed. In practice, recombination occurs in the base region, and a base current is necessary to maintain the level of the base charge. All the terminal currents can be explained in terms of this base charge.

If the transistor is turned on into a short circuit load (constant collector voltage), the charge distributions shown in Fig. 2.6a are set-up. This charge stored in the base region (Q_B) gives rise to a collector current I_C, and a base current I_B. The amount of charge Q_B depends upon the type of distribution and the base width. The most useful 'ON' state for a bipolar transistor in switching applications is when the transistor is just bottomed. In this case the collector-base junction voltage (V_{CB}) is zero. The maximum amount of charge in the base is denoted by Q_{BM} and the base current to maintain it by I_{BM}. The collector current reaches its saturation value and is written as I_{CS}.

If a finite load resistance is connected to the collector terminal and the collector voltage drops during turn-on from $V_{CE(off)}$ to

$V_{CE(sat)}$, some extra charge is required to charge the collector depletion layer capacitance. This situation is illustrated in Fig. 2.6b. It is evident that the base charge with the finite collector load resistance is larger than that without load to maintain the same collector current.

CURRENT SATURATION REGION: If the value of base current I_B is increased beyond I_{BM}, the collector junction becomes forward biased and the transistor presents a very low impedance between the collector and emitter terminals. Consequently, the voltage across these terminals becomes very small. The collector saturation current is controlled by the external circuit and is essentially V_{CC}/R_L, where V_{CC} is the collector supply voltage and R_L is the load resistance.

As both junctions are forward biased in the current saturation region, minority-carrier injection into the base region takes place from both junctions. For any excess base current beyond I_{BM}, an excess charge Q_X is stored in the base and the collector regions. These excess charge components are shown in Fig. 2.7. It is absolutely difficult to separate these two excess charge components by experimental methods. The charge stored in the collector region can only be calculated theoretically, by knowing boundary conditions, transistor material parameters, and the geometry of the transistor [B.2].

CHAPTER III

LARGE-SIGNAL ANALYSIS OF SATURATION-CHARGE STORAGE

An appropriate way of studying transistor action in the current saturation region is by analysis of the physical model in this region. Basically a transistor consists of one rectifying P-N junction (emitter junction) separated from a second rectifying N-P junction (collector junction) by a thin semiconductor layer (base region). The thickness of the base region is much smaller than the minority-carrier diffusion length in it. In the active mode the emitter junction is forward biased and the collector junction is reversed biased. Because the thickness of the base region is much smaller than the minority-carrier diffusion length in the base, the minority carriers injected into it by the forward biased emitter junction are collected at the reverse biased collector junction almost without any loss in the base region.. The transport of minority-carriers across the base region involves both diffusion and drift. In modern bipolar switching transistors the minority-carrier transport across the base region is due to diffusion and drift in a built-in electric field.

Fig. 3.1 is an ideal cross-section of a P-N-P expitaxial diffused bipolar transistor. As most of the modern transistors are drift transistors, a detailed large-signal analysis is given only for this type of the transistors.

3.1 Basic Assumptions

Of the many assumptions made by previous workers only the most relevant assumptions are listed.

(i) The resistivities of the semiconductor regions are low [E.2].

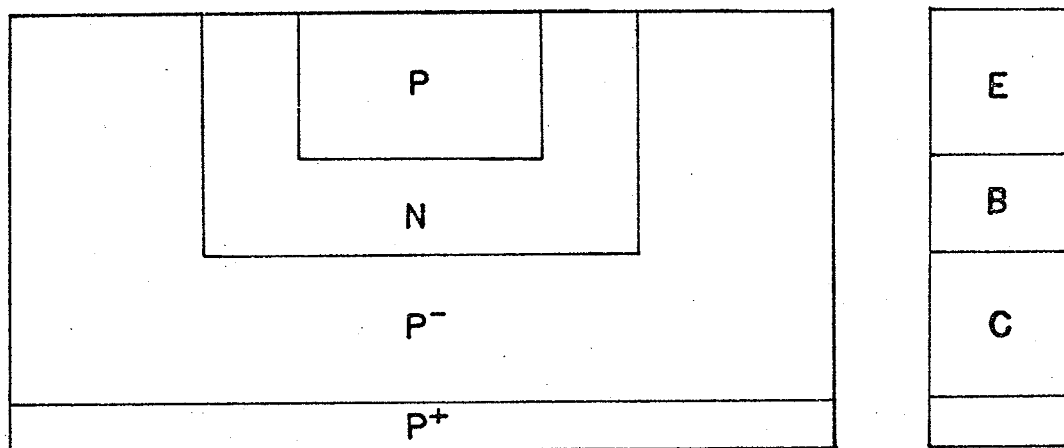


Fig. 3.1 - Cross-section of an epitaxial PNP transistor.

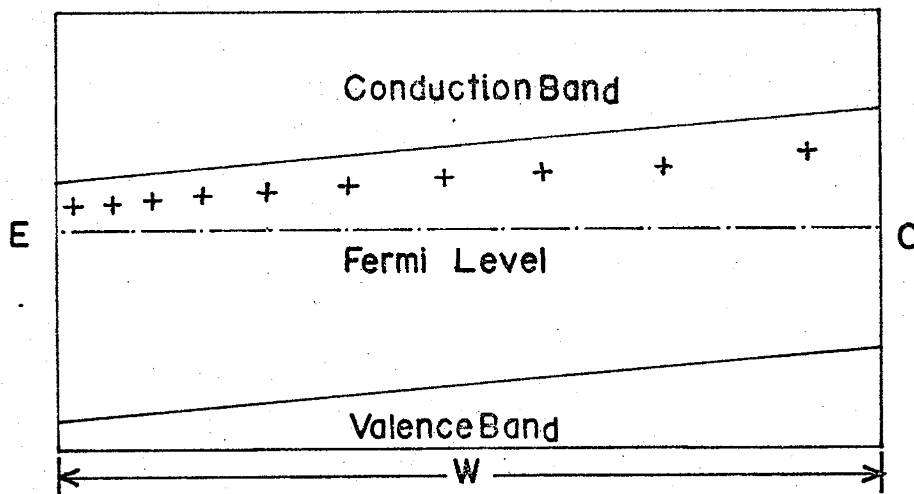


Fig. 3.2 - The graded-base region of a transistor showing the effect of doping level.

(ii) The minority-carrier injection densities are low enough in comparison with the doping levels of the semiconductor regions.

Assumptions (i) and (ii) insure that there are no voltage drops within the semiconductor other than those across the junctions and that the emitter efficiency is not a function of the emitter current. This assumption is not always true because the collector regions of all modern bipolar transistors have finite resistivity.

(iii) The base regions is graded with the highest doping level near the emitter-base junction. Fig. 3.2 [H.2] shows the graded base region and the physical origin of a built-in electric field.

(iv) The base is much more heavily doped than the collector region which is assumed homogeneous with an acceptor concentration (N_A). This assumption is quite different than that made by Eber's and Moll. These authors presented a theory of a saturated transistor in which the collector region is much more heavily doped than the base region.

(v) The collector region is wide enough for the whole collector-base voltage (V_{CB}) to be dropped across it without producing any significant heating of the holes. Assuming that hole mobility is unaffected even for high fields (2000 V/cm), it implies that collector region has an effective width $W(\text{in}\mu) > 5V_{CB}$. Van der Ziel and Agourdis [V.1] suggested a different condition which is approximately that $W(\text{in}\mu) \asymp V_{CB}$ and there is a $\bar{p}$-region between the heavily doped base region and p^+ collector region. This p^-region is quite narrow.

(vi) Even in saturation, there is a collector space-charge layer at the collector-base junction. Kirk's [K.1] assumptions (that in saturation a boundary layer associated with the collector-base junction migrates towards the collector contact, the potential on the base side of the boundary is close to the base potential, the boundary represents the collector edge of the

effective base region and the transistor simply behaves as though the width had been correspondingly increased), are incorrect.

(vii) Space-charge layer widening effects can not be neglected. Although the voltage drop across collector-space charge layer is small, its effect on carrier concentration is generally very large owing to their exponential dependence on voltage.

(viii) Saturation occurs as a result of the collector-base junction becoming forward biased. The voltage across the junction is then small enough for carrier heating in the space-charge layer to be negligible so the carrier densities on either side of the space charge layer are related by the normal Boltzman equation. Owing to assumption (iv), the electron density on the collector side of the layer $n(o)$ is much greater than the hole density on the base side, which is practically unaffected by saturation:

$$n(o) = n_o \exp (qV_{C'B'}/kT) \tag{3.1}$$

where n_o is the equilibrium electron density in the collector region.

(ix) The transit time of holes across the base region is unaffected by saturation. Thus, the saturated transistor characteristics are determined by the extra minority-carrier concentration in the base and collector regions. It must be remembered here that the most heavily doped region of the transistor is the emitter and there is no minority-carrier concentration on the emitter side of the emitter-space charge layer.

(x) Almost complete charge neutrality exists in the collector region where the hole concentration is

$$p = N_A + n \tag{3.2}$$

(xi) The steady state electron current in the collector region is negligible. This implies that the minority-carrier (electron) life time

τ_n is sufficiently large and that no electrons enter the collector from the p^+ contact. In other words, the electron current in the collector region is negligible in comparison with the hole current [B.2].

(xii) The geometry is one dimensional. This assumption seems inconsistent with assumption which states that the collector region is thick enough. In most of the transistors the emitter area is smallest and there is a pronounced lateral spreading of the current in the collector, so that a one-dimensional analysis appears over simplified. If the base current is not greatly exceeding the saturation value, the region of stored charge in the collector is shallow compared with the lateral dimensions of the emitter. The remainder of the collector acts as a series resistance.

(xiii) As long as the transistor operating point is in the current saturation region, the transistor impedances are so low that it is most convenient to consider that currents as independent variables. In addition, the operation is nearly linear with respect to currents, but is very non-linear with respect to voltage.

3.2 Saturation Charge Storage and Excess Storage Time Constant

Once the transistor is fully turned on, it remains in saturation because the driving base current I_{B1} is greater than the amount necessary to establish the collector current I_C, that is $I_{B1} > I_C/h_{FE}$. in saturation as shown in Fig. 2.7. In the base region, the total stored charge in saturation is denoted by Q_{BS}. Some of the minority charge is stored in the high-resistivity collector region and may be a significant portion of the total excess saturation charge. The saturation charge stored in the collector region is denoted by Q_C. There is no charge storage in the low

resistivity emitter region. Thus, the total stored charge is $Q_{BS} + Q_C$. If Q_{BM} is the amount of base charge required to bring the transistor to the edge of the saturation region, then the excess stored charge is

$$Q_X = Q_{BS} + Q_C - Q_{BM} \tag{3.3}$$

The shaded portion of the Fig. 2.7 shows this excess charge Q_X.

Thus, the storage time t_s is the time required to reduce the excess charge to zero. It happens when the collector forward potential is reduced to zero and starts to reverse polarity. The storage interval begins when the base current I_{B1} is reversed to a turn-off value I_{B2}. This situation is shown in Fig. 2.2b since the excess base current may be defined [B.4] as

$$I_{BX} = I_{B1} - I_{BM} \tag{3.4}$$

and the excess storage time constant as

$$\tau_x = \frac{dQ_X}{dI_B} = \frac{Q_X}{I_{BX}} \; . \tag{3.5}$$

The large-signal switching behavior of a transistor in the current saturation region is characterized by this excess storage time constant τ_x. In aid to the analysis of the transistor, Moll's [M.4] concept is utilized, that is, the base charge is made up of two components,

$$Q_{BS} = Q_{BSF} + Q_{BSR} \tag{3.6}$$

The first term on the righthand side corresponds to a forward emitter-to-collector current I_F and is the forward component of the total charge; the

second term is a reverse component of the total charge and is due to collector-to-emitter current I_R. Substituting the value of Q_{BS} into equ. (3.3), and finally into equ.(3.5), the excess storage time constant becomes

$$\tau_x = \frac{Q_{BSF} + Q_{BSR} + Q_C - Q_{BM}}{I_{BX}} \tag{3.7}$$

3.3 Saturation Charge Storage in the Base Region:

Transport of the minority-carriers across the base region in the absence of recombination can be described (for a PNP graded base transistor) by the relation

$$I_p(x) = qA\,[\mu_p \varepsilon p(x) - D_p \frac{dp(x)}{dx}] \tag{3.8}$$

Here, the constant built-in electric field ε [H.2 pp. 143] is positive since the holes are accelerated in the positive x-direction. The diffusion gradient of holes is directed to the right from emitter to collector, giving a diffusion current which enhances the drift current. The first-order linear differential equation may be written in terms of $p(x)$:

$$\frac{dp(x)}{dx} - \frac{\mu_p \varepsilon}{D_p} P(x) = \frac{I_{p(x)}}{qAD_p} \ . \tag{3.9}$$

Einstein's relation states that

$$\frac{D_p}{\mu_p} = \frac{KT}{q} = V_T \tag{3.10}$$

This linear differential equation can be written after integration as,

$$p(x) = [\exp(\frac{\varepsilon x}{V_T})]\ [\frac{I_{P(x)}}{qA\mu_p \varepsilon} \exp(-\frac{\varepsilon x}{V_T}) + C] \tag{3.11}$$

Here $x=0$ at the emitter junction and $x=w$ at the collector junction.

The total base charge is decomposed into two active region charge components [M.4] [E.2] a forward active charge component Q_{1S} and a reverse active component Q_{2S}. This decomposition is illustrated in Fig. 3.3. Writing $p(x) = p_1(x)$ for Q_{1S} and $p(x) = p_2(x)$ for Q_{2S}, the equ.(3.11) is solved for these two minority-carrier densities at any distance x along the base. In the forward active case, the collector is assumed reverse biased and the emitter forward biased. Solving for $p_1(x)$, the boundary conditions are $p_1(o) = p(\varepsilon)$ and $p_1(w) = 0$. It gives,

$$C = - \frac{I_{p_1}(x)}{qA\mu_p \varepsilon} \exp\left(- \frac{\varepsilon w}{V_T}\right). \qquad (3.12)$$

Now, $I_{p_1}(x) = I_1(w) = \text{constant}$. Equation (3.11) becomes,

$$p_1(x) = \frac{I_1(w)}{qA\mu_p \varepsilon} \left[1 - \exp\left(\frac{x-w}{V_T} \varepsilon\right)\right] \qquad (3.13)$$

The normalized base-field-factor m is defined as

$$m = \frac{w\varepsilon}{V_T} = \frac{t_D}{t_w} \qquad (3.14)$$

where $t_w = \frac{w}{\mu_p \varepsilon}$ is the time required for a hole to drift the distance w and $t_d = \frac{w^2}{2D_p}$ is the delay time required for a hole to diffuse a distance w. Equ. (3.13) has the final form,

$$p_1(x) = \frac{I_1(w)}{qAD_p m} \left[1 - \exp\left(\frac{x}{w} - 1\right)m\right] \qquad (3.15)$$

The excess hole density at the emitter side $(x=0)$ of the base is

$$p_1(o) = p_1(\varepsilon) = \frac{I_1(w)}{qAD_p m} \left[1 - \exp(-m)\right] \qquad (3.16)$$

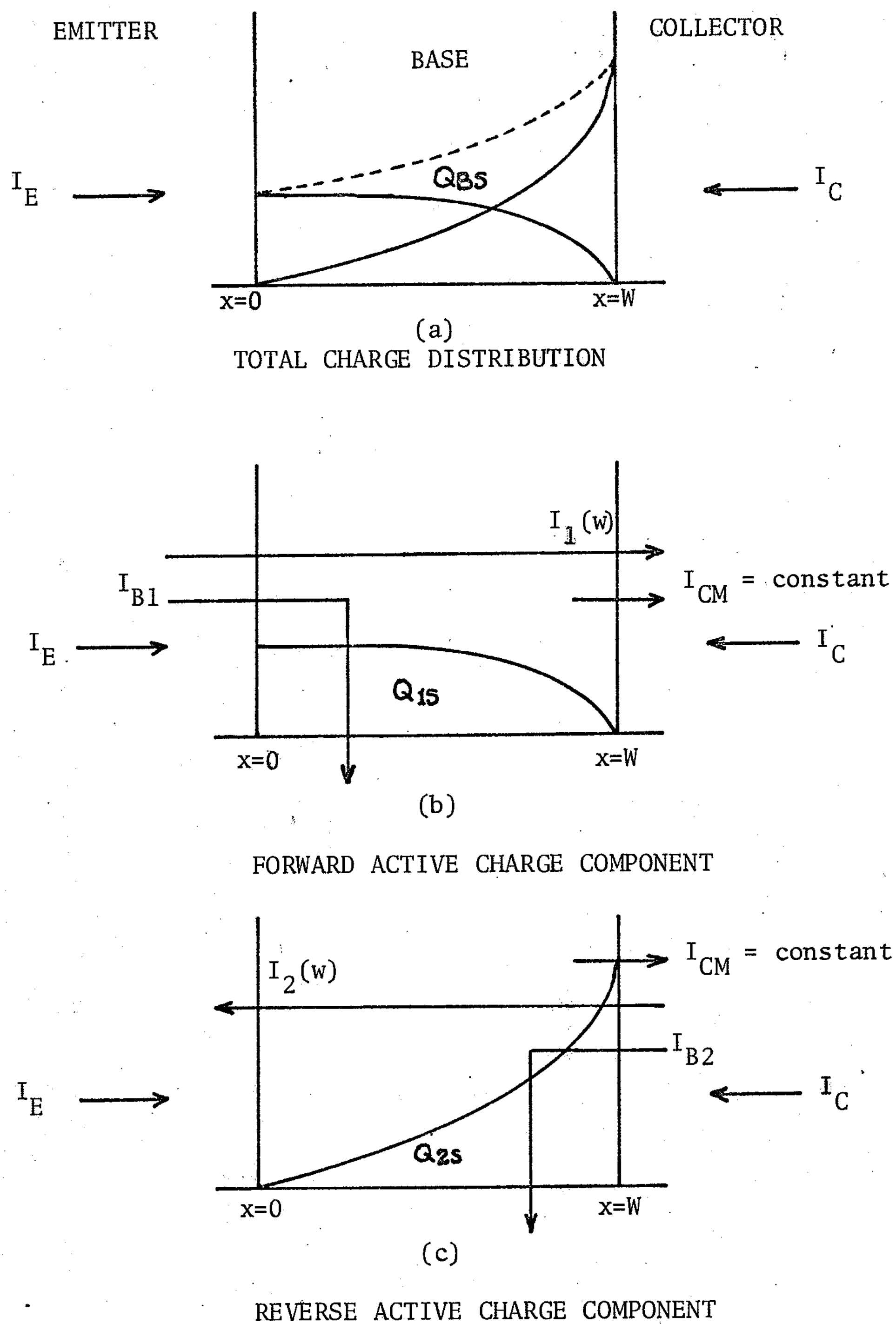


Fig. 3.3 - Charge components corresponding to forward and reverse currents.

Here $p_1(\varepsilon)$ designates the hole density at the emitter side of the base for the case of pure drift transport of holes across the base region.

There will be a marked difference in the base charge distribution in the reverse active case (when collector is forward biased and emitter is reverse biased). This reverse active charge distribution is shown in Fig. 3.3. The excess hole density is calculated with the help of boundary conditions $p_2(o) = 0$ and $p_2(w) = p_2(D)$, where $p_2(D)$ is the excess hole density at x = w due to diffusion only. $p_2(x)$ is calculated from equ. (3.11) as

$$p_2(x) = \frac{I_2(w)}{qAD_p m} [\exp (\frac{xm}{w}) - 1] \tag{3.17}$$

where the sign of the equation has been reversed to take care of the reverse operation and give the proper limit. The excess hole density on the collector side of the base is to be

$$p_2(D) = \frac{I_2(w)}{qAD_p m} [\exp (m) - 1] . \tag{3.18}$$

The total excess hole density at any point along the base is

$$\begin{aligned} p(x) &= p_1(x) + p_2(x) \\ &= \frac{I_1(w)}{qAD_p m} [1 - \exp (\frac{x}{w} - 1)m] \\ &+ \frac{I_2(w)}{qAD_p m} [\exp (\frac{xm}{w}) - 1] . \end{aligned} \tag{3.19}$$

The total stored charge in the base region during current saturation is calculated by integrating p(x) over the width of the base region:

$$Q_{BS} = qA \int_o^w p(x) \, dx$$

$$= qA \int_{o}^{w} [1 - \exp\ (\frac{x}{w} - 1)m]\ \frac{I_1(w)}{qAD_p m}\ dx +$$

$$[\exp\ (\frac{xm}{w})\ - 1]\ \frac{I_2(w)}{qAD_p m}\ dx$$

$$= \frac{1}{D_p m} \int_{o}^{w} I_1(w)\ \{1 - \exp(\frac{x}{w} - 1)m\}\ dx\ +$$

$$\int_{o}^{w} I_2(w)\ \{\exp\ (\frac{x}{w})m\ - 1\}\ dx$$

$$= \frac{w}{D_p m}\ [I_1(w)\ -\ I_2(w)] - \frac{w}{D_p m^2}\ [I_1(w)\ -\ I_2(w)]$$

$$+ \frac{w}{D_p m^2}\ [I_1(w)\ e^{-m}\ -\ I_2(w) e^{m}]$$

or

$$Q_{BS} = \frac{w}{D_p m}\ [I_1(w)\ -\ I_2(w)]\ -\ \frac{w}{D_p m^2}\ [I_1(w)(1 - e^{-m})$$

$$-\ I_2(w)\ (1 - e^{m})] \qquad (3.20)$$

The above total charge can also be calculated in terms of terminal currents $I_1(w)$ and $I_2(w)$ in saturation, which are related to the terminal currents as follows:

$$\begin{aligned} I_E &= I_1(w) - \alpha_I\ I_2(w) \\ -I_C &= \alpha_F(w) - I_2(w) \end{aligned} \qquad (3.21)$$

The direction of collector current flow is taken into the collector terminal. and is shown in Fig. 3.3. Expressing the saturation base charge Q_{BS} in terms of I_E, I_C

$$Q_{BS} = \frac{w}{D_p m} \frac{(1+\alpha_F) I_E - (1-\alpha_I) I_C}{1 - \alpha_F \alpha_I} - \frac{w}{D_p m^2}$$

$$\frac{I_E + \alpha_I I_C}{1 - \alpha_I \alpha_F} (1 - e^{-m}) - \frac{I_C + \alpha_F I_E}{1 - \alpha_I \alpha_F} (1 - e^{m}) \tag{3.22}$$

where I_E and I_C are the emitter and collector currents in saturation, respectively.

The maximum charge stored in the base region at the edge of saturation depends only on the current injected from the emitter junction. If this emitted current is I_{EM} and the hole density at the base side of the emitter junction due to this current is $p(\varepsilon)$, then

$$Q_{BM} = qA \int_0^w p(x)\, dx$$

$$= qA \cdot \frac{I_{EM}}{qAD_p m} \int [1 - \exp(\frac{x}{w} - 1)m]\, dx$$

$$= \frac{wI_{EM}}{D_p m} [1 - \frac{1}{m}(1-e^{-m})] \tag{3.23}$$

The excess saturation base charge Q_{BX} which must be removed before the transistor can come out of saturation is

$$Q_{BX} = Q_{BS} - Q_{BM}$$

$$= \frac{w}{D_p m} \left[\frac{(1-\alpha_F) I_E - (1-\alpha_I) I_C - I_{em}(1-\alpha_F \alpha_I)}{1 - \alpha_F \alpha_I} \right]$$

$$- \frac{w}{D_p m^2} \frac{I_E + \alpha_I IC}{1 - \alpha_F \alpha_I} (1-e^{-m}) - \frac{I_C + \alpha_F I_E}{1 - \alpha_F \alpha_I} (1-e^{m}) \qquad (3.24)$$

Thus, the excess saturation base charge can be calculated in terms of active region transistor parameters, and of course, knowing the value of base-field-factor m.

3.4 Saturation Charge Storage in the Collector Region:

Several authors have recently reported on the static collector saturation voltage and minority carrier storage phenomenon in lightly doped collector regions [B.2; C.3; P.1]. However, the analysis given here is based on Beale and Slatter's work. A one-dimensional analysis which defines the minority carrier storage phenomenon in lightly doped collector region of a graded-base transistor in terms of terminal currents and device parameters is given in this section.

As the doping density on the base side of the collector junction is much higher than on the collector side and the collector contact is an ohmic contact, the doping profile and net minority-carrier density distribution in the saturated collector region is assumed as in Fig. 3.4a. The analysis proceeds from the two transport equations and the requirement that the total current be continuous:

$$J_p = q\mu_p \varepsilon p - qD_p \frac{dp}{dx} \qquad (3.25)$$

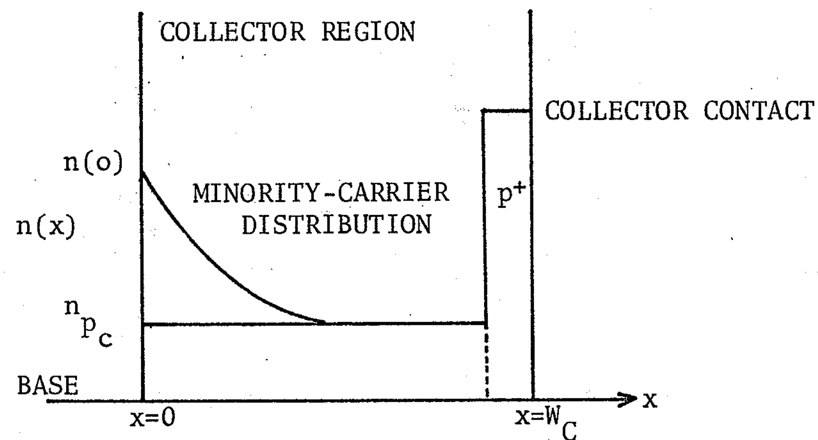


Fig. 3.4 - Collector doping profile and minority-carrier charge distribution in the saturated collector region.

$$J_N = q\mu_N \varepsilon n + qD_N \frac{dn}{dx} \tag{3.26}$$

$$J = J_p + J_N$$

Assuming charge neutrality in the collector region and no electron from the p+ collector contact, the total majority carrier density in the collector region is $p=n+N_A$ and $J_N = 0$. Equations (3.23) and (3.24) give:

$$\varepsilon = \frac{D_N}{\mu_N} \frac{1}{n} \frac{dn}{dx} \tag{3.27}$$

or

$$\begin{aligned} \varepsilon &= V_T \frac{1}{n} \frac{dn}{dx} \\ &= V_T \frac{1}{n} \left(\frac{-dp}{dx}\right) \end{aligned} \tag{3.28}$$

because N_A is constant and hence $\left|\frac{dp}{dx}\right| = \left|\frac{dn}{dx}\right|$.

Now,

$$J_p = -2q\, D_p \left(1 + \frac{N_A}{2n}\right) \frac{dp}{dx} \tag{3.29a}$$

$$= 2q\, D_p \left(1 + \frac{N_A}{2n}\right) \frac{dn}{dx} \tag{3.29b}$$

By integrating equ. (3.29b)

$$x = \frac{2qD_p}{J_p} [n(x)-n(o) + \frac{N_A}{2} \ln \left(\frac{n(x)}{n(o)}\right) \tag{3.30}$$

Equation (3.30) gives the relation between x and n in terms of collector current density J_p and electron concentration at the edge of the collector. It remains to find n(o) in terms of the applied terminal currents and voltages. This can be done by using assumption $J_N \to 0$ which allows n(x) to be related

to voltage by Boltzmann equation. It is convenient to assume $x = W_C$ in equ. (3.30) (where W_C is the effective width of the collector region) since the voltage at this point ($V=V_C$) is known. Thus from equ. (3.26)

$$V_{CB'} - V_{C'B'} = -\int_{0}^{W_C} \varepsilon \, dx$$

$$= -V_T \int_{0}^{W_C} \frac{dn}{n}$$

$$= -V_T \ln \left(\frac{n(W_C)}{n(o)}\right) \qquad (3.31)$$

From equ. (3.30) and assuming that $n(W_C) \rightarrow 0$, it follows

$$W_c = \frac{qD_p}{J_p} \left[- \frac{2n(o)}{N_A} - \frac{(V_{CB'} - V_{C'B'})}{V_T}\right] \cdot N_A$$

$$= \frac{-qD_p}{J_p} \left[\frac{2n(o)}{N_A} + \frac{(V_{CB'} - V_{C'B'})}{V_T}\right] \cdot N_A \qquad (3.32)$$

where B' and C' denote the internal base and collector contacts respectively. The hole current component in the collector region, when $V_{C'B'} \rightarrow 0$ and $n(o) \rightarrow 0$, is

$$J_{pS}^{*} = -q \, \mu_p N_A \, V_{CB'}/W_c \qquad (3.33)$$

Thus from equ. (3.32)

$$\frac{n(o)}{N_A} = \frac{1}{2V_T} \left[V_{CB'} \left(\frac{J_p}{J_{pS}^{*}} - 1\right) + V_{C'B'}\right] \qquad (3.34a)$$

Equation (2.1) can be substituted for $V_{C'B'}$ to find out the $n(o)/N_A$ in terms of measurable quantities. However, in saturation, $V_{C'B'}$ is approximately equal to -0.6V for a typical silicon transistor.

This gives a simplified form of equation (3.34), which is useful

in the saturation.

$$\frac{n(o)}{N_A} = \frac{u}{2}\left(\frac{J_p}{J_{pS}} - 1\right) \qquad (3.34b)$$

where

$$u = \frac{1}{V_T}(V_{CB'} - V_{C'B'})$$

and

$$J_{pS} = J_{pS}^{*}/(V_{CB'} - V_{C'B'})/V_{CB'}$$

Equations (3.30) and (3.34) can be used to find the electron distribution as a function of distance in the collector region. In actual calculation, it is seen that the electron charge in the collector is concentrated near the collector-base junction and can be so large that the resistivity of the collector is heavily modulated in this region [B.2]. The charge is kept close to the collector junction by the field produced by the hole current flowing through the collector. The charge spreads across the region as the hole current increases.

The total saturation charge stored in the collector region (Q_c) is calculated as follows:

$$Q_c = qA\int_{o}^{W_c} n(x)\ dx \qquad (3.35a)$$

Putting the value of $n(x)$ from equ. (3.29b)

$$Q_c = \frac{qA}{J_p}\int_{o}^{W_c} J_p\ n(x)\ dx$$

$$= \frac{qA}{J_p}\int_{o}^{n(o)} 2q\ D_p\ n(x)\ dn + \frac{qA}{J_p}\int_{o}^{n(o)} 2q\ D_p\ \frac{N_A}{2}\ dn$$

$$Q_c = \frac{q^2 A^2 D_p}{I_p} [n(o)^2 - N_A\, n(o)] \qquad (3.35b)$$

where A is the emitter area. Equ. (3.35b) in conjunction with equ. (3.34a) gives the charge stored as a function of current and voltage. In the deep saturation, $n(o) >> N_A$, and

$$Q_c = \frac{I_p W_c^2}{4D_p} [1 - \frac{I_{pS}}{I_p}]^2 \qquad (3.36).$$

Equation (3.36) can be used to determine the saturation charge stored in the collector region.

3.5 Saturation Charge Storage in the Case of Inverted Emitter-Follower mode:

In the inverted emitter-follower mode, current is emitted from the collector and collected at the reverse biased emitter junction. The emitter is grounded and the load resistance is connected to the collector terminal. During saturation, the transistor presents a virtual short circuit between the collector and emitter terminals. The total resistance in the collector circuit (resistance of low-resistivity collector region and load resistance) is much larger than the forward resistance of the emitter loop. Consequently, all excess base current flows across the emitter junction. The excess saturation charge stored in the base region is injected from the emitter and there is no saturation charge injection from the collector side. The above facts have been proved experimentally. As the I_{BX} is increased, current across the emitter junction is reduced first. When $I_{BX} = I_1(w)$, the current across the emitter junction is zero. If $I_{BX} > I_1(w)$, meter indicates current flow in the reverse direction.

The saturation charge storage and current conditions for the IEF mode in saturation, are shown in Fig. 3.5. The theoretical claculations of saturation charge require the knowledge of the current conditions across the junction and the physical parameters such as doping levels of all three regions of the transistor. Once these parameters with other boundary conditions are known, the analysis could be given in same way as in section 3.3. The complete analysis of the IEF mode in saturation requires controlled fabrication and knowlege of all material parameters. At present, no such facilities are available in our laboratories.

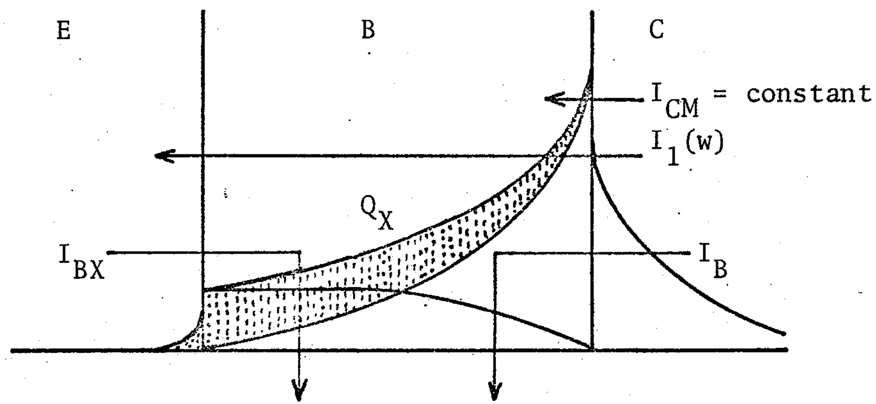


Fig. 3.5 - Saturation charge in the Inverted Emitter-Follower Mode.

CHAPTER IV

TECHNIQUES OF MEASURING SATURATION CHARGE AND EXCESS STORAGE TIME CONSTANT

There are numerous experimental procedures to measure saturation charge and saturation time constant. These are summarized well by Nanavati [N.4] whose conclusions seem supported by other workers in the field. A few are described in this chapter and considerable attention has been given to include only those which either give reasonable accuracy in measurements or are otherwise important.

4.1 Small-Signal Method:

On the basis of one-dimensional analysis of the two-diode model of a transistor in the saturation region, Moll [M.4] has found:

$$\tau_x = \frac{\omega_I + \omega_F}{\omega_I \omega_F (1-\alpha_F \alpha_I)} \tag{4.1a}$$

where ω_I and ω_F are the alpha cut-off frequencies of transistor in reverse and forward modes respectively; α_I and α_F are reverse and forward common base current gains. τ_x is the excess saturation charge storage time constant. Equation (4.1a) can be written as

$$\tau_x = \frac{\tau_F + \tau_I}{1 - \alpha_F \alpha_I} \tag{4.1b}$$

where $\tau_F = \frac{1}{\omega_F}$ and $\tau_I = \frac{1}{\omega_I}$.

Beaufoy and Sparkes [B.4], using a slightly different approach found

$$\tau_x = \frac{1.22 \, (\omega_I + \alpha_F \omega_F)}{\omega_F \omega_I (1-\alpha_F \alpha_I)} \tag{4.2}$$

$$= 1.22 \left(\frac{\tau_F + \alpha_F \tau_I}{1-\alpha_F \tau_I}\right)$$

A similar but more accurate formula was proposed later.

$$\tau_X = \left(\frac{\tau_F + \alpha_I \alpha_I}{1 - \alpha_F \alpha_I}\right) \alpha_F \qquad (4.3)$$

Hence, prediction of saturation charge storage time constant requires the measurement of four small-signal active region parameters. Two different test circuits to measure active region response time constant τ are given in Fig. 4.1a and 4.1b. All the test procedures that measure τ, only the quantity Q_{off} (charge required to turn-off the transistor) is measured. In the test circuit of Fig. 4.12 [G.1] a negative going pulse of sufficient amplitude is applied at the input base terminal. The transistor is switched on and brought at the edge of saturation ($I_{BX} = 0$), but does not enter into saturation region. The stored charge is extracted by capacitance C after the pulse termination. The amount of charge extracted is

$$Q_{off} = C \cdot \Delta V = \tau I_C + Q_V \qquad (4.4)$$

where $\Delta V = (V_1 - V_2)$ is the voltage change across capacitance C, and Q_V is the charge stored in the depletion layer. It is assumed that $Q_V \ll I_C\tau$ and does not change appreciable for different values of collector voltage swing, provided the condition $V_{CB} = 0$ exists. For such a condition

$$Q_{off} = \tau I_{C1} + Q_V = \Delta V_1 X C$$

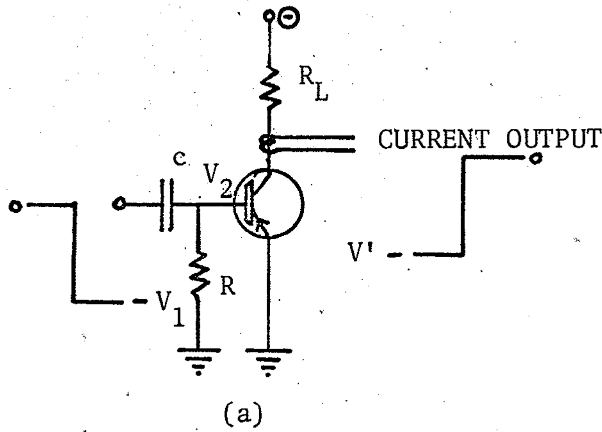
$$Q_{off} = \tau I_{C2} + Q_V = \Delta V_2 X C$$

and thus

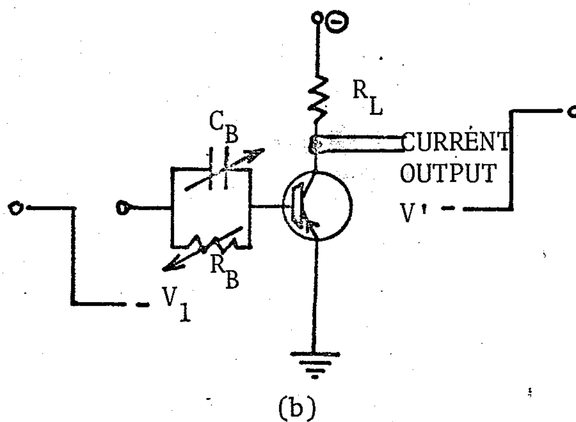
$$(Q_{off2} - Q_{off1}) = (I_{C2} - I_{C1})\ \tau$$

or

$$\tau = \frac{Q_{off}}{\Delta I_C} = \frac{C(\Delta V_2 - \Delta V_1)}{\Delta I_C} \qquad (4.5)$$



(a)



(b)

Fig. 4.1 - Test circuits for measurement of Active Region Time constant, V.

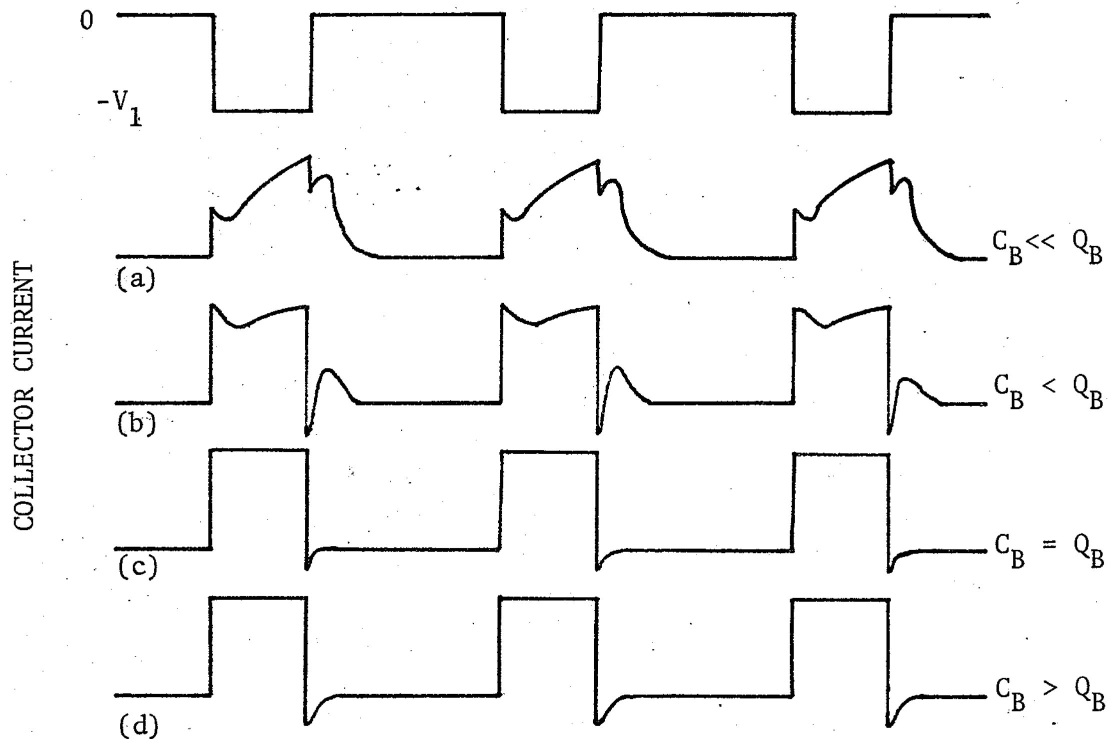


Fig. 4.1c - Output waveforms observed during adjustment of C_B in Fig. 4.1b

In the test circuit of Fig. 4.1b, first R_B is adjusted until, during the on-stroke, the transistor is just bottomed ($V_{CB} = 0$). This condition is achieved when $t_s = 0$ for output current pulse. When C_B has been adjusted to yield step collector response

$$Q_{off_1} = \Delta V\, C_{B1} = \tau I_{C1} + Q_V \qquad (4.6a)$$

For another setting of the collector current I_{C_2}, R_B is adjusted again until transistor is bottomed, and for step response

$$Q_{off_2} = \Delta V\, C_{B_2} = I_{C_2}\tau + Q_V \qquad (4.6b)$$

Hence,

$$(Q_{off_2} - Q_{off_1}) = V\,(C_{B_2} - C_{B_1}) = (I_{C_2} - I_{C_1})$$

and

$$\tau = \frac{\Delta V\,(C_{B2} - C_{B1})}{\Delta I_C} \qquad (4.6c)$$

where ΔV is approximately equal to input pulse amplitude, while a more accurate value of ΔV is the voltage swing across C_B. The waveforms observed during adjustment of C_B for a normal transistor are shown in Fig. 4.1c. By normal transistor is meant a 6db/octave current gain variations with frequency. Sparkes [S.5] has described this cut-off frequency dependence of alpha. A graph drawn for Q_{off} vs. collector current gives a straight line. The slope of this line is the time constant τ.

Thus, the active region time constant τ is measured both in the forward and reverse modes. In the reverse mode, the collector acts as a emitter and the emitter as a collector. The common-base current gain alpha (α) is

measured with the standard circuits described in most of the electronic text books. The steady-state short circuit output values of alpha are measured for different current conditions, in both reverse and forward modes. Putting the values of the four parameters τ_F, τ_I, α_F and α_I in equ. (4.3.), the value of τ_x may be calculated.

The above method of measuring excess saturation charge storage time constant is not particularly useful to the circuit designer, as it involves measurement of four parameters. The measured values of τ_x may vary as much as 100%.

4.2 Large-Signal Method:

If the transistor is driven into saturation, an electron current I_{BM} is drawn into base as a result of recombination of the active charge Q_{BM} having a life time τ. Another electron current I_{BX} is required to support recombination of the excess charge Q_X with a lift time τ_x. Thus the net current of $I_{B_1} = I_{BM} + I_{BX}$ would flow out of the base terminal.

Now suppose the transistor is switched into saturation by the application of a pulse at base terminal. At the termination of the pulse the input voltage is changed to positive for a PNP transistor. This potential cannot supply the electron currents required by recombination, instead it offers a field which repels the excess holes from the base to the emitter and collector causing a current I_{B_2} to flow into the base terminal. The above situation is shown in Fig. 2.2b. The continuity equation is written [H.1]

$$-I_{B_2} = \frac{dQ_X}{dt} + \frac{Q_B}{\tau_B} \tag{4.7}$$

where τ_B is the active region base time constant. Writting $Q_x = \tau_x I_{BX}$

and $I_{BX} = I_{B_1} - I_{BM}$, the storage time t_s for the condition $I_{BX} = 0$ is given

$$t_s = \tau_x \ln \frac{I_{B_1} + I_{B_2}}{I_{BM} + I_{B_2}}. \qquad (4.8)$$

This is the expression for storage time often described in the literature [M.4] [N.4].

The test circuit for measuring storage time t_s is shown in Fig. 2.2a. The conditions at the input are such that the input source is a constant current generator, i.e. the base lead resistance R_B is much greater than the forward resistance of the emitter base junction diode. A negative going pulse of sufficient amplitude switches on the transistor into saturation. The input and output current pulse transients appear on scope as shown in Fig. 2.2b. The amplitudes of I_{B_1}, I_{B_2} and the time t_s are measured. Now the pulse amplitude is reduced to a value for which $t_s=0$ and the transistor is just bottomed. In this condition, $I_{B_2} = 0$ and $I_{B_1} = I_{BM}$. The same procedure is repeated for different values of the collector current. The excess storage time constant is

$$\tau_x = \frac{t_s}{\ln \frac{I_{B_1} + I_{B_2}}{I_{BM} + I_{B2}}} \qquad (4.9)$$

and the saturation charge

$$Q_x = \tau_x (I_{B_1} - I_{BM})$$

$$= \tau_x I_{BX}. \qquad (4.10)$$

The values of τ_x and Q_x are in complete agreement with theory. In general, the values of τ_x are either low or high for

small values of base current I_{B_1}, i.e. for small value of excess saturation base current I_{BX} because there is greater probability to make errors in measuring small quantities. When the currents I_{B1} and I_{B_2} are of the same order and I_{BM} is either smaller than I_{B_1} or is of the same order, the sum of I_{B_1} and I_{B_2} becomes very important. Any error made in measuring I_{B1} is multiplied in the numerator of the logarithmic term.

4.3 Beaufoy and Sparkes Method:

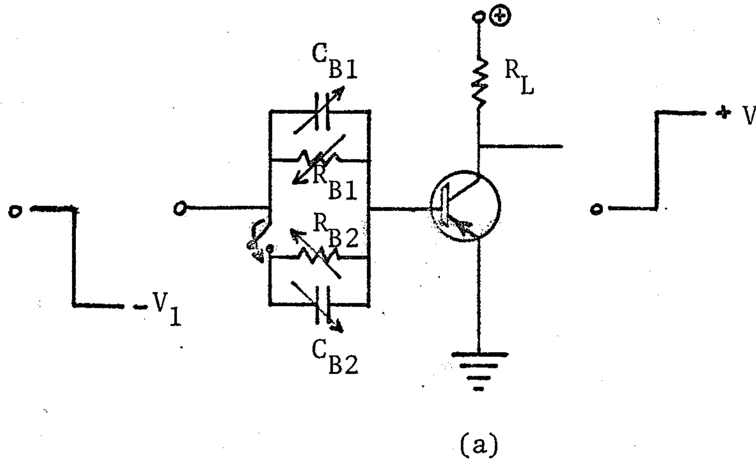
This procedure is just an extension of that described in section 4.1. Fig. 4.2 shows complete test sets for the measurement of excess saturation charge storage Q_X. In the circuit diagram of Fig. 4.2a first R_{B_1} is adjusted until, during the on stroke, the transistor is just bottomed (V_{CB}=0). When it has been adjusted for sharpest response (or squar-wave output) and for any desired collector current,

$$Q_{off} = Q_B = \Delta V \; C_{B_1} \tag{4.11}$$

where ΔV is the amplitude of the input pulse, assuming that transistor 'off' current is zero and that the collector-to-emitter voltage V_{CE} is negligible.

Next, if the load resistance value is restored to its original value of R_L and another resistance R_{B_2} is connected in parallel of R_{B_1}, an extra base current in excess of I_{BM} is passed through R_{B_2}. In fact, this base current passed through R_{B_2} will be the saturation base current I_{BX}, since R_{B_1} was previously set for just bottomed condition with load resistance R_L. Now C_{B_2} has the function of extracting the saturation charge stored in the base region. Both R_{B_2} and C_{B_2} are adjusted for sharpest output response, Q_X becomes

$$Q_X = \Delta V \; C_{B_2} \tag{4.12}$$



(a)

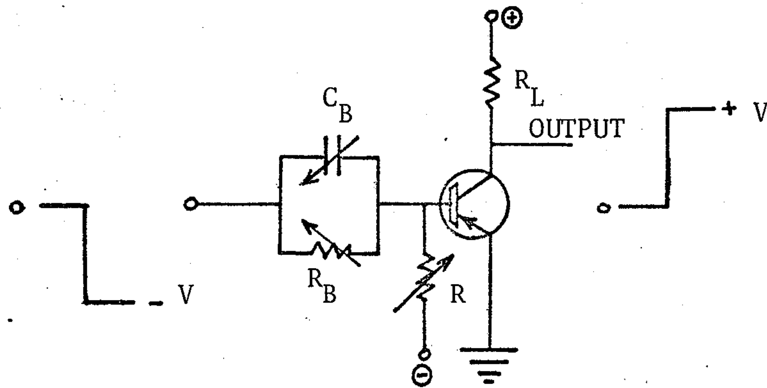


Fig. 4.2 - Test circuit for measuring Q_X and τ_x (Beaufoy and Sparkes Method).

and $$\tau_x = \frac{Q_x}{I_{BX}} = \frac{\Delta V X C_{B_2}}{I_{BX}}$$

$$= R_{B_2} \quad C_{B_2} \tag{4.13}$$

Thus the value of Q_x and τ_x are directly read in terms of R_{B_2}, C_{B_2}, and input voltage.

There is a variation of the above experimental procedure. In the circuit shown in Fig. 4.2b the resistance R is first adjusted so that the transistor just bottoms (V_{CB}=0) without the application of a pulse. If a train of negative-going pulses of predetermined amplitude is applied at the base terminal, an excess base current I_{BX} would start to flow due to this input and the transistor would then be driven into saturation. The next step is to adjust the variable resistance and capacitance R_B and C_B until the output pulse assumes a square-shap. In each case the combination of R_B and C_B is chosen which yields the sharpest response of the outpust pulse. Let R_B' and C_B' be the values so obtained for R_B and C_B respectively. Then

$$\tau_x = R_B' \quad C_B' \tag{4.14}$$

and $$Q_x = \tau V C_B' \tag{4.15}$$

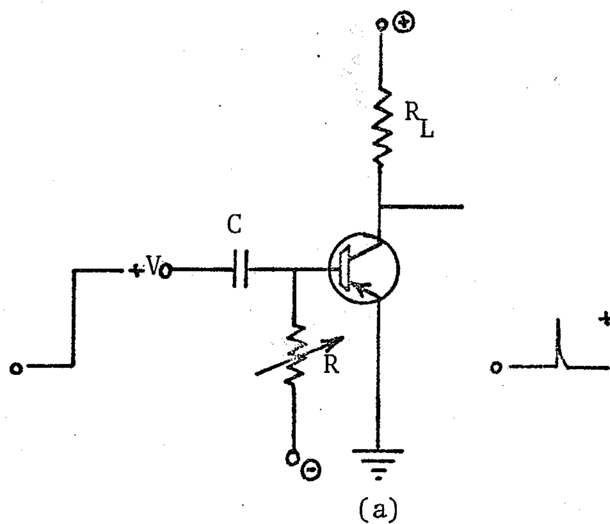
where ΔV is the amplitude of the input pulse. The pulse applied was a negative pulse starting from zero. The above measurements are performed for various values of collector current I_C and graphs are drawn for Q_x vs I_{BX}. The various values of input voltage ΔV for the same collector current I_C give different values of Q_x. τ_x may also be extrapolated from the slope of the Q_x vs I_{BX} curves.

The second method [B.4] [N.4] of this section is not so useful because it is very difficult to adjust the exact $V_{CB}=0$ condition. One can measure $V_{CB}=0$ only at the physical base and collector terminals. When $V_{CB}=0$ at the outer terminals it may be the case that collector junction is more forward biased. Next both these methods provide visual observation of the measurements. The setting of C_B for sharpest adjustment may depend on the observes. A pulse train is shown in Fig. 4.1. The values of C_B for pulse trains of Fig. 4.1b & 4.1c may differ by a factor of as much as two to three.

4.4 Nanavati's Method:

The test circuit is shown in Fig. 4.3a. First, R is adjusted until it puts the transistor into saturation by a known amount [N.4]. A train of positive going pulses is applied through a fixed value of coupling capacitor C. The amplitude of the pulse generator is varied and the output is observed in order to determine how large a pulse is required to take the transistor just out of saturation. In this method advantage is taken of the non-linearity at the edge of the saturation region. Once the pulse amplitude is greater than that required for just bringing the transistor out of saturation, the sudden increase in the output current pulse transient identifies the edge of saturation. This transient is observed at the instant of positive-going edge of the input pulse. The output current transient observed during the experiment is shown in Fig. 4.3b. The extrapolation of the edge of saturation can be done visually quite well, or it can be done graphically for a greater accuracy. The results reported in this work are based on visual extrapolation.

Let I_{BS} be the current when transistor is in saturation and I_{BM} the current which is just sufficient to put the transistor at the edge of saturation. Then, saturation current is $I_{BS}-I_{BM}$. If ΔV is the pulse height



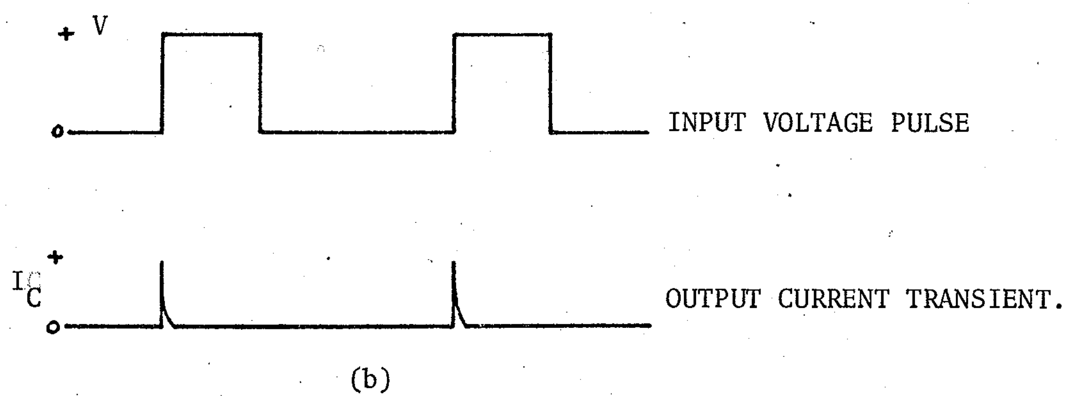


Fig. 4.3 (a) Nanavati's measuring circuit and

(b) Input and output pulse transients.

necessary to take the transistor just out of saturation, then ΔV is a measure of the excess saturation charge Q_x.

$$Q_x = \Delta V X C \tag{4.16}$$

and

$$\tau_x = \frac{Q_x}{I_{BX}} \tag{4.17}$$

A graph ΔQ_x vs I_{BX} is drawn. The slop of this characteristics is the excess saturation charge time constant τ_x.

This is the most useful and convenient method. There are fewer sources of errors.

CHAPTER V

EXPERIMENTAL RESULTS AND DISCUSSION

The experimental results for saturation charge (Q_X) and excess storage time constant (τ_X), are shown in Fig. 5.1 to Fig. 5.5. These data were taken with MMPS-6518 PNP-expitaxial graded-base transistor. Similar results were obtained for other graded-base transistors. For example, the normal and IEF mode performances of a NPN (2N3565) transistor are given in Fig. 5.7.

5.1 Saturation-Charge Storage:

It can be seen from Fig. 5.1 and Fig. 5.2 that the saturation charge varies with collector current. It may also be seen that Q_X is independent of collector current at low I_{BX}. Therefore, at the onset of saturation the initial saturation charges and charge distribution are invariant for different injection levels. If the transistor is driven further into saturation, the saturation charge (Q_X) increases with the base drive, but it decreases with increasing injection level.

The curves of Fig. 5.2 show the saturation charge variation with excess base current. It is evident, that normal, inverted and emitter-follower modes store equal amount of charges for most of the operating values of excess base current. Therefore, there is no advantage (over the normal mode) operating the transistor in either inverted or emitter-follower mode, since current gain and speed are sacrificed. But the charge Q_X stored in the case the of the inverted-emitter follower (IEF) mode is much smaller than that of the normal mode. There is about 60-70% reduction in saturation charge and improved switching speed (discussed in sect. 5.3) make the IEF mode superior to other operating modes.

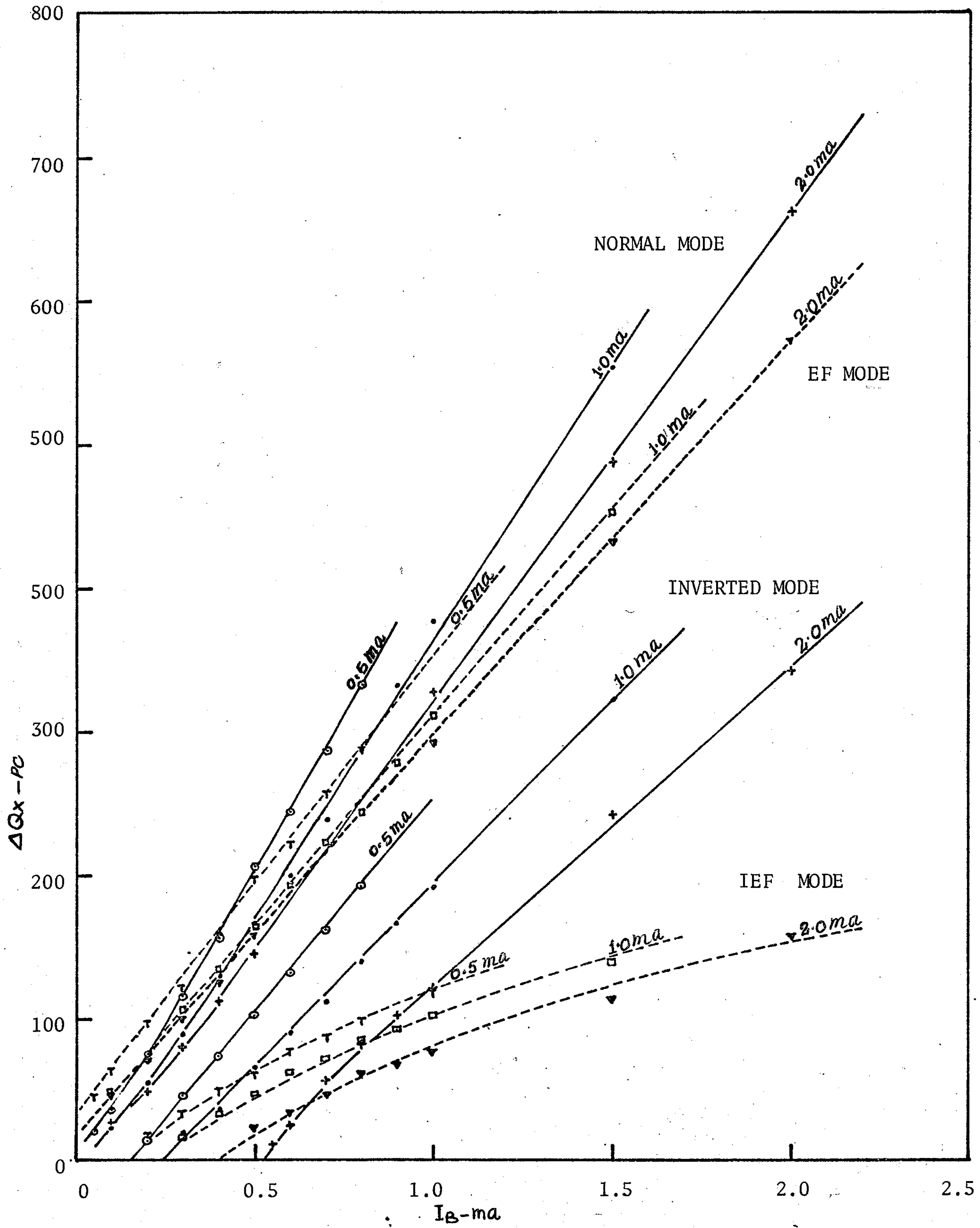


Fig. 5.1 - ΔQ_X vs I_B curves.

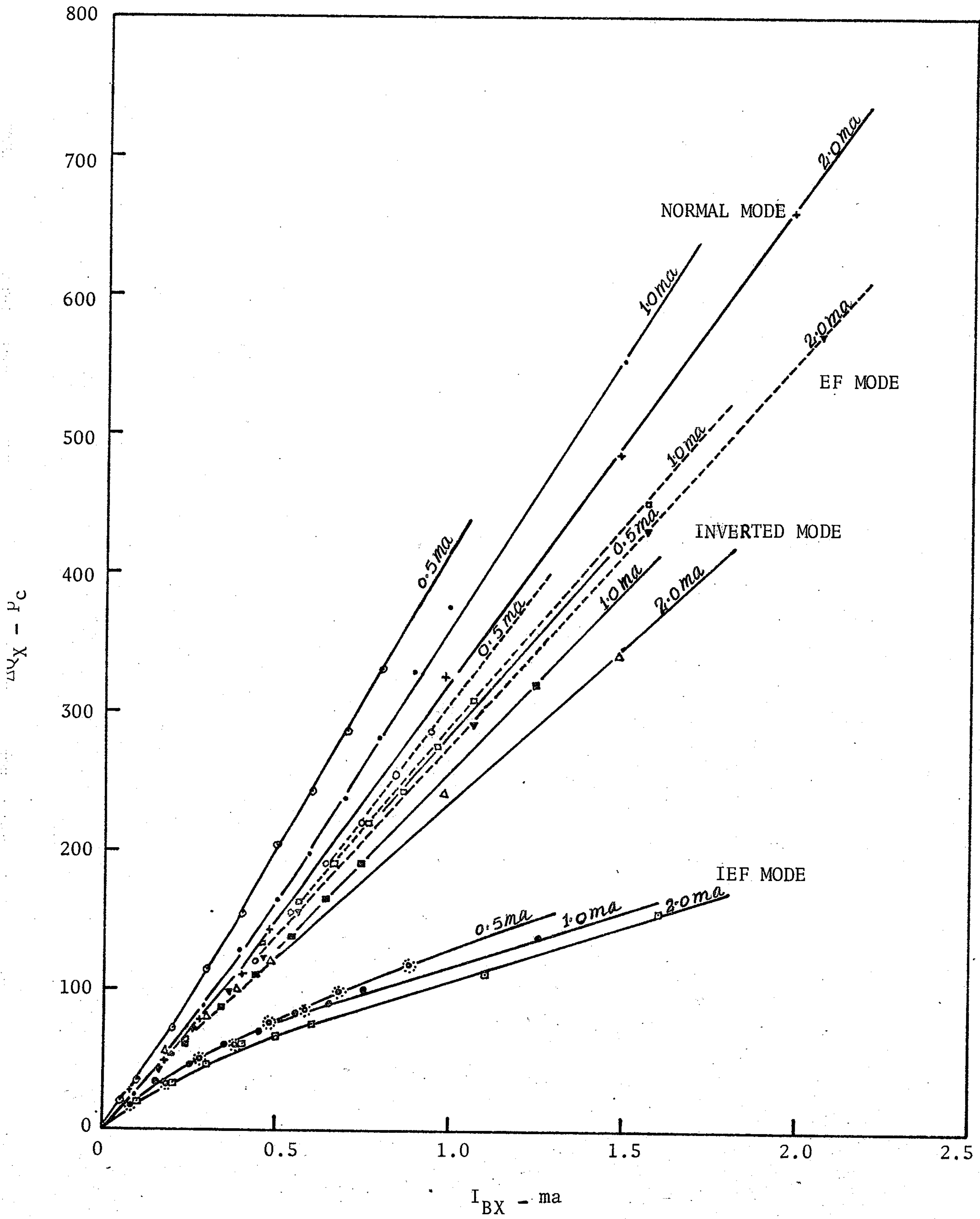


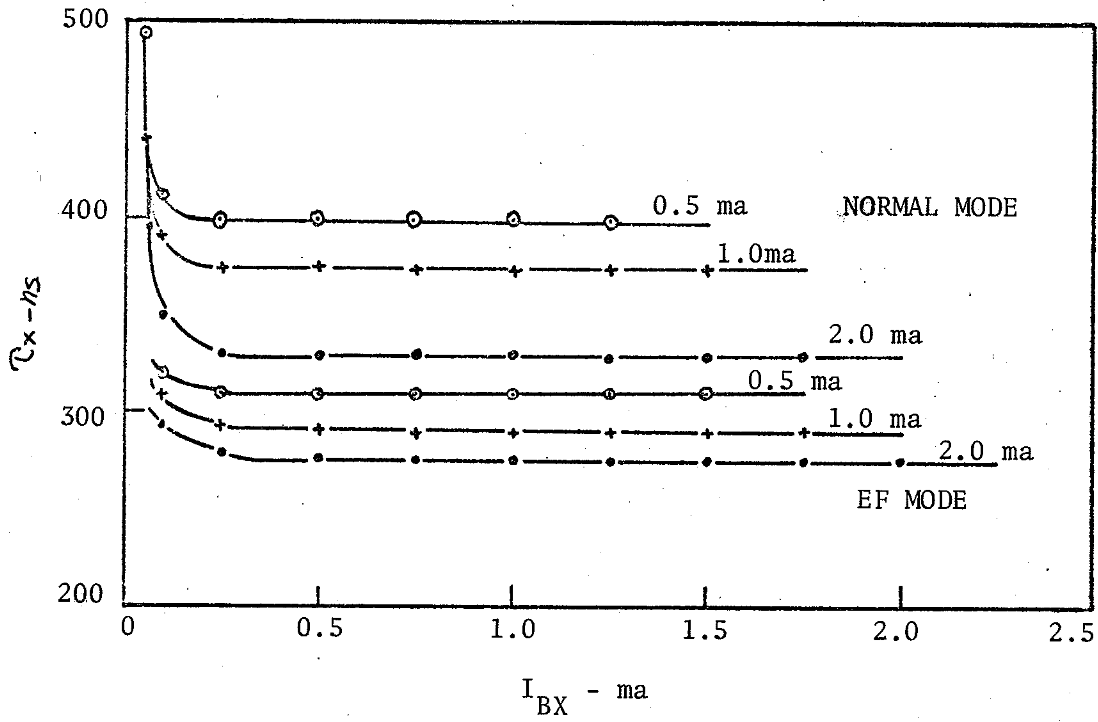
Fig. 5.1- ΔQ_X vs I_{BX} Curves.

In the case of the inverted emitter-follower (IEF) mode, the values of saturation charge are higher for low values of excess base current (I_{BX}) and decrease gradually with increasing I_{BX}. These values of Q_X become fairly constant for high values of I_{BX}. It is also evident from Fig. 5.2 that the saturation charge Q_X rises exponentially for low values of I_{BX}. This may be due to initial voltage adjustment across the depletion layer when the transistor enters saturation.

The saturation charge storage is almost independent of load resistance, except in the case of the emitter-follower mode where the operating range is limited for a particular value of load resistance. Hence, the emitter-follower mode is not suitable for switching purposes. The curves of Figs. 5.1 to 5.4 follow the same pattern for different values of load resistant. The variations in saturation charge (Q_X) with changing load resistance indicate that the charge stored in the depletion regions during saturation is much smaller than the total saturation charge. In other words, base-width modulation and depletion region variation do not affect the saturation charactereistics much. This is in agreement with assumption (V) of chapter III.

5.2 Excess Storage Time Constant

It is evident from Fig. 5.3 and 5.4 that the excess storage time constant varies with the injection level and the base drive. These variations of excess storage time constant (τ_X) are fairly complicated. Considering the effect of injection levels, three principal factors should be kept in mind. First, at low current levels, the change of depletion layer thickness as a transistor enters saturation, necessitate the injection of extra base charge, leading to higher values of τ_X. Second, the increase of current gain which occurs as the current level increases (shown in Table 5.1) will tend to lead to values of τ_X which rise with increasing current level, and third, the



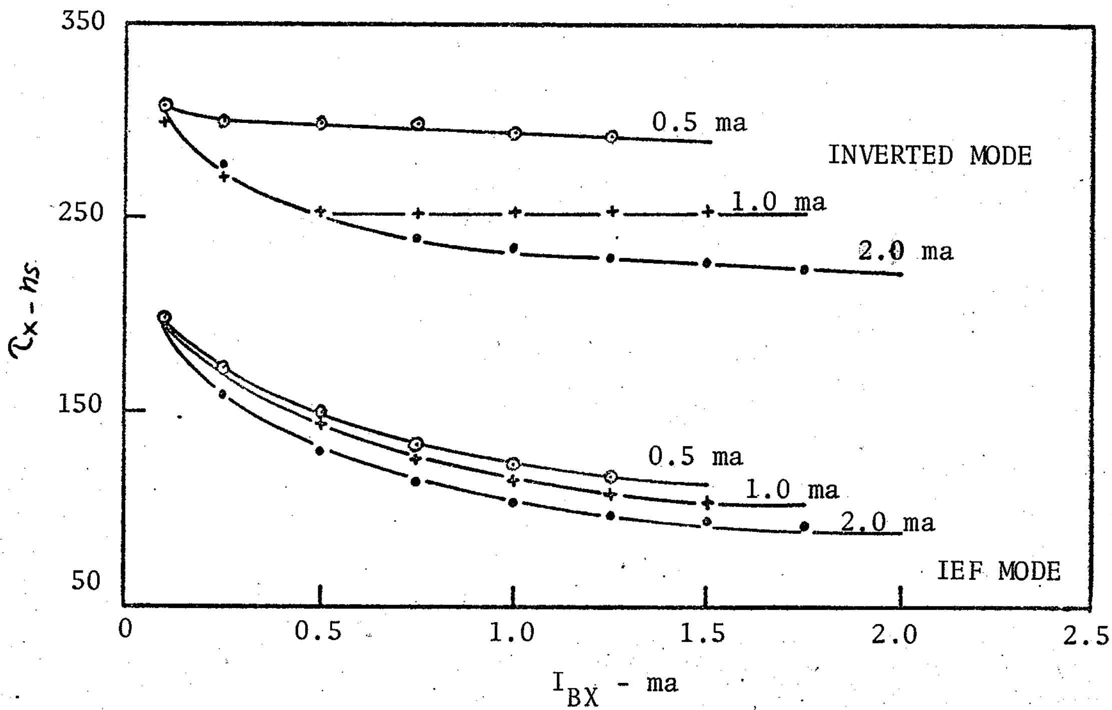
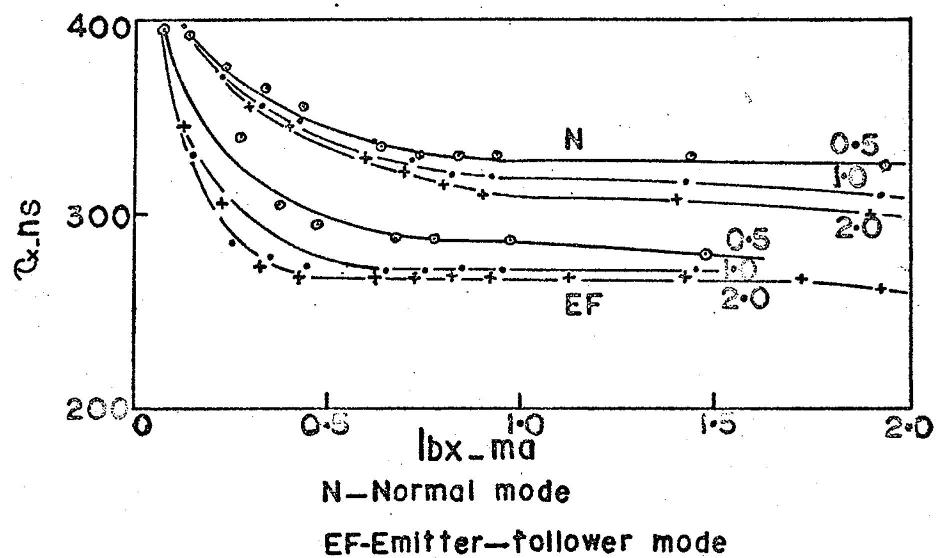


Fig. 5.3 - τ_X vs I_{BX} curves.



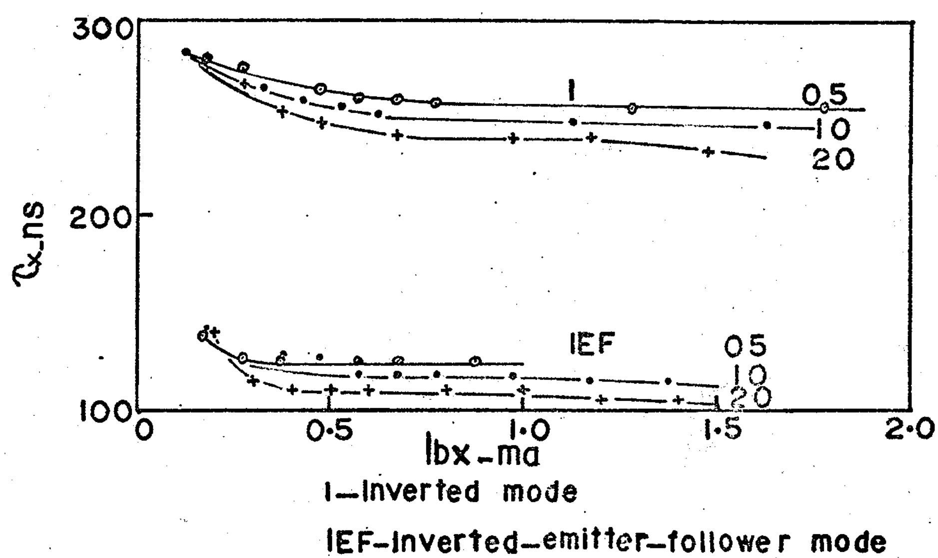


Fig. 5.4 - τ_x vs I_{BX} curves.

decrease in τ_F and τ_I (i.e. increasing in ω_F and ω_I) as a result of high injection level will cause a decrease in τ_x.

Typical curves of Fig. 5.3 and 5.4 are in good agreement with low-level and high-level injection effects. Both the large-signal and charge-control methods give identical values of τ_x. The values of τ_x decrease with increasing collector current. These variations are small in the case of the inverted emitter-follower mode, and τ_x is not so strongly dependent on collector current. In Fig. 5.5, τ_x has much higher values and increases with increasing injection level, i.e. increasing collector current. Thus, the small-signal method gives values of τ_x which are quite different than those of other methods. In Equ. (4.3) if α_F is very close to unity and has small variations with collector current (Table 5.1), then the expression for τ_x reduces to

$$\tau_x = \frac{\alpha_I \tau_I}{1 - \alpha_I} \tag{5.1}$$

where $\tau_F \ll \tau_I$.

It is also clear from Table. 5.1, that the inverted current gain α_I is a very non-linear parameter which increases with increasing injection level. Consequently, high values of τ_x are expected from the small-signal method.

The higher values of τ_x and disagreement of τ_x vs I_C characteristics with those by other method put the validity of small-signal method in doubt. At present, it seems that the small-signal method of measuring τ_x is inadequate.

Further, the diffused structures which possess relatively large collector regions with high resistivity and life-times often exhibit minority-

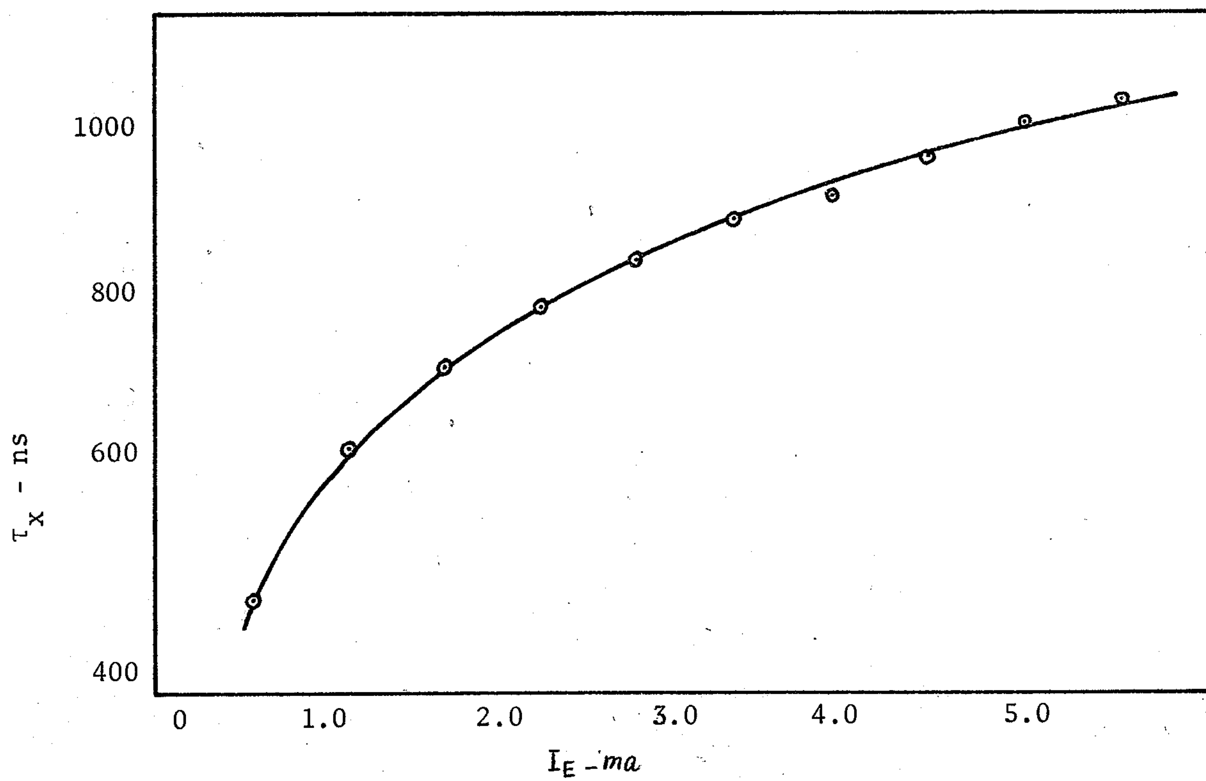


Fig. 5.5 - τ_x vs I_E curve.

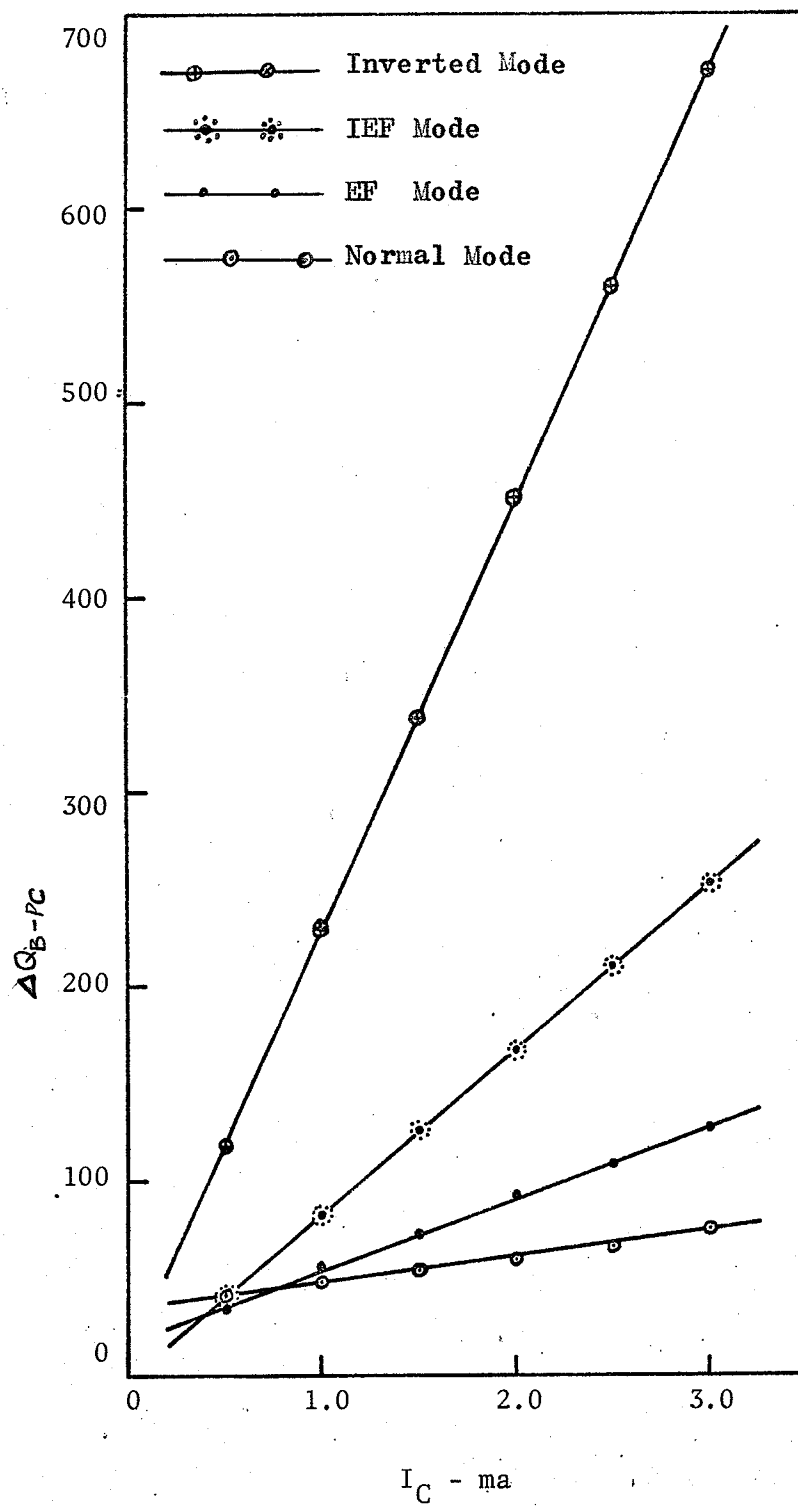


Fig. 5.6 - ΔQ_B vs I_C curves.

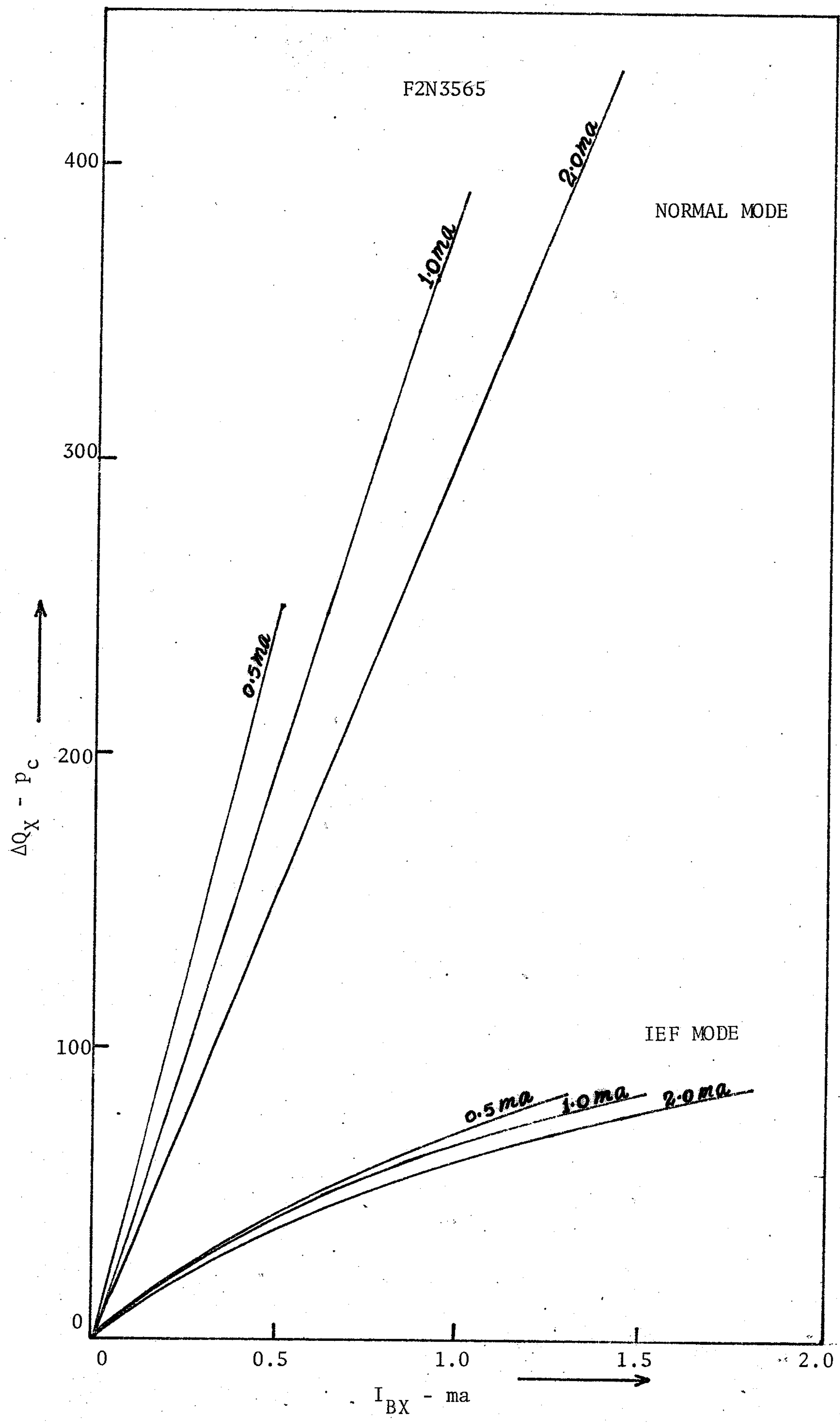


Fig. 5.7 - ΔQ_X vs I_{BX} curves

TABLE 5.1

Excess storage time (τ_x) evaluation by small-signal method.

I_E-(ma)	$\alpha_F = \frac{I_E - I_B}{I_E}$	$\alpha_I = \frac{I_{ER} - I_{BI}}{I_{EI}}$	$\tau_F = \frac{Q_{BF}}{I_{BI}}$	$\tau_R = \frac{Q_{BI}}{I_{BI}}$	$\tau_{XF} = \frac{(\tau_F + \tau_I \alpha_I)}{1 - \alpha_F \alpha_I}$	$\tau_{XI} = \frac{(\tau_I + \alpha_F \tau_F)}{1 - \alpha_F \alpha_I}$
0.2	0.984	0.737	12 ns	220 ns	620 ns	620 x
0.5	0.987	0.694	"	"	506 "	507
0.7	0.988	0.720	"	"	575 "	575
0.9	0.989	0.738	"	"	630 "	630
1.0	0.990	0.746	"	"	660 "	661
1.2	0.990	0.763	"	"	720 "	721
1.4	0.990	0.763	"	"	720 "	721
1.6	0.991	0.772	"	"	760 "	760
1.8	0.991	xxx	"	"	x "	x
2.0	0.992	0.780	"	"	798 "	798
2.5	0.992	0.792	"	"	846 "	845
3.0	0.992	0.800	"	"	890 "	890
3.5	0.992	0.805	"	"	915 "	916
4.0	0.992	0.812	"	"	955 "	956
4.5	0.992	0.816	"	"	985 "	985
5.0	0.992	0.820	"	"	1010 "	1012

carrier charge storage in this region when the transistor is driven into saturation. This has the effect of producing very large values of τ_x measured either by large-signal or charge-control methods. The small-signal method gives the values of τ_x corresponding to the charge stored in the base region only; and these values should be expected lower than those measured by other methods. But this is just opposite of what is observed. The small-signal method exhibits larger values for τ_x than the other methods. These values of τ_x will again be increased after introducing the correction factor for Q_c. These facts again place doubt on the validity of the small-signal method.

The theory of the small-signal method explains the behaviour of the transistor in normal and inverted modes only. It does not say anything about the inverted emitter-follower mode. Even for normal and inverted modes, the values of τ_x are the same, as is evident from Fig. 5.5 and Table 5.1. But the other experimental methods show different values of τ_x for each mode. The active-region time constants (Fig. 5.6) are also different in each case. The values of these time constants vary from tens of nano-seconds to hundreds of nano-seconds, indicating that each mode is different from others. Therefore, it is evident that small-signal transient behaviour characterization of transistor in current saturation is not completely described by Moll's [M.4] two diode model.

It may be possible because active region parameters do not hold good in current saturation region [B.3]. Secondly, the behaviour of graded base transistors is more complicated and demands improvement in small-signal theory. In conclusion, the small-signal method never gives satisfactory results.

The variations of τ_x with excess base current (I_{BX}) are shown in Fig. 5.4 and 5.5. Initially for low values of I_{BX}, the values of τ_x are

high. But they are approximately equal for different values of collector currents. As the I_{BX} is further increased τ_x decreases first and then becomes constant for moderate values of I_{BX}. The values of τ_x are quite low in the inverted emitter-follower (IEF) mode and follow the same pattern as in other modes. But the variations with I_{BX} are more prominent in the case of charge control method than those in large-signal method.

Thus, the inverted emitter-follower mode gives least values of τ_x and hence, relatively very small saturation charge storage. This gives improved switching speed and reduced saturation time delay without any extra fabrication technique and cost.

5.3 Active Region Performance:

The active region performance of inverted emitter-follower (IEF) mode are much superior to other operating modes for the identical operating conditions. It is clear from Table 5.2 that the IEF mode has minimum delay time. The normal mode has approximately 20-60 times and the inverted mode 10 times more delay in their responses than the IEF mode. There is remarkable reduction in rise-time too if the transistor is operated in IEF mode. Approximately, 50% reduction in rise time is evident (Table 5.3) from that in the normal mode and 30% from that in the inverted mode.

Hence, the inverted-emitter-follower (IEF) mode gives a reduced turn-on time (delay time + rise time) delay. The turn-on switching speed of the IEF mode is as much higher as 300% to 400% than the normal mode. It is about 150% to 400% greater than the inverted mode.

The active region turn-off time delay includes fall-time (t_f) only and it is clear from the Table 5.4 that this is the largest in the case of the inverted emitter-follower mode. Thus, the IEF mode has poor turn-off response.

TABLE 5.2

Delay time evaluation for MMPS-6518-PNP Transistor

Conditions		R_B = 6.8K, R_L = 1K, t_s=0		R_B = 6.8K, R_L = 1K, t_s = 100 ns	
I_C (mA)		1	2	1	2
Delay time (ns)	IEF-mode	4	4	4	4
	Normal-mode	240	190	80	80
	Inverted-mode	40	40	40	40
	EF-mode	It is not useful for switching action			

TABLE 5.3

Rise time evaluation for MMPS-6518-PNP Transistor:

Conditions		R_B=6.8K, R_L = 1K, t_s=0		R_B= 6.8K, R_L = 1K, t_s = 100 ns	
I_C(mA)		1	2	1	2
Rise Time (ns)	IEF-mode	240	200	60	70
	Normal-mode	680	640	100	170
	Inverted-mode	360	340	200	200

TABLE 5.4

Fall-time evaluation for MMPS-6518-PNP Transistor

Conditions		R_B= 6.8K, R_L = 1K, t_s=0		R_B= 6.8K, R_L = 1K, t_s= 100 ns	
I_C(mA)		1	2	1	2
Fall Time (ns)	IEF-mode	380	400	400	400
	Normal-mode	100	120	120	120
	Inverted-mode	250	360	250	340

TABLE 5.5

Total turn-on for MMPS-6518-PNP Transistor

Conditions		R_B= 6.8K, R_L= 1K, t_s=0		R_B=6.8, R_L=1K, t_s = 100ns	
I_C(mA)		1	2	1	2
Total Delay (ns)	IEF-mode	244	204	64	74
	Normal mode	920	830	180	250
	Inverted mode	400	380	240	240

CHAPTER IV

CONCLUSIONS

A new operating configuration (called inverted emitter-follower mode) has been proposed which reduces the charge stored in the graded-base transistors during the saturation regime. The experimental data confirm that the saturation charge Q_x is reduced to one third of that in the normal mode without sacrificing switching speed, loading capability, and stability. Thus the IEF mode has saturation characteristics superior to other operating modes.

The saturation charge Qx and excess storage time constant τ_x measured by various experimental techniques have been compared. The results of most methods are in good agreement with the only exception of the small-signal method. The theoretical and experimental limitations of the small-signal method have been outlined.

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