Grounded HVDC Grid Line Fault Protection Using Rate of Change of Voltage and Hybrid DC Breakers

By

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Abstract

Different HVDC grid types and the respective protection options are discussed. An earthed bi-pole HVDC grid was modeled in PSCAD, and using simulation results, the necessity of di/dt limiting inductors to contain the rise of fault currents within the capacity of current hybrid DC breakers is demonstrated. The impact of different inductor sizes on current rise was studied. A fault detection and localization scheme using the rate of change of voltage (ROCOV) measured at the line side of the di/dt limiting inductors is proposed. The protection system was modeled and tested under different fault types and locations. The results show that the proposed method of HVDC grid protection is feasible using the current hybrid DC breaker technology. A systematic procedure for setting the necessary protection threshold values is also demonstrated.

Acknowledgements

I would like to thank Dr. Athula Rajapakse for his advice and guidance which proved to be very valuable throughout this research project.

I would like to thank Dennis Woodford and Electranix Corporation for their encouragement and support and for a work environment that values life-long learning.

I would like to thank Ellie Sneath for editorial support provided during the writing of this thesis.

Dedication

This work is dedicated to Ellie, Chloe, Celia, Violet and Wyatt.

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List of Abbreviations

AC	-Alternating Current
DC	-Direct Current
HVDC	-High Voltage Direct Current
IGBT	-Insulated-Gate Bipolar Transistor
LCC	-Line Commutated Converter
LC	-Inductor Capacitor
MCOV	-Maximum Continuous Over-Voltage
MMC	-Multi-Module Converter
P-G	-Pole-to-Ground
P-P	-Pole to Pole
PWM	-Pulse Width Modulation
ROCOC	-Rate of Change of Current
ROCOV	-Rate of Change of Voltage
SLD	-Single Line Diagram
VAR	-Volt-Ampere Reactive
VSC	-Voltage Source Converter
WG	-Working Group

1 Introduction

This introductory chapter outlines the background, motivation and objectives of this research, followed by a brief overview of the organization of this thesis.

1.1 Background and Motivation

High Voltage Direct Current (HVDC) transmission has been used in power systems around the world, mostly as a point-to-point power delivery system. HVDC technology enables economic power delivery across long distances, is controllable and does not suffer from the excessive charging that AC cables experience when used for underground or submarine transmission systems [1]. HVDC grids are now being considered as a way to interconnect offshore wind resources, avoid overhead lines and add redundancy, flexibility and efficiency to a widespread power delivery system [1] [2] [3] [4].

While the line commutated converter (LCC) technology dominates the point-to-point HVDC schemes, voltage source converters (VSCs) are the preferred technology for HVDC grids. The main advantage of VSC technology is the ability to transport power in either direction without reversing polarity, which is essential in HVDC grids. The ability to operate in a weak AC system, reactive power flexibility and a small physical footprint are the other advantages. Newer multilevel VSCs (MMCs) offer additional advantages over two-level VSCs in terms of lower harmonics and switching transients [5].

However, VSCs have some inherent weaknesses in the way they respond to DC line faults. In order to ensure proper operation, each IGBT in a VSC needs to be provided with an antiparallel freewheeling diode. During a DC side short circuit, these diodes provide a path for fault currents as illustrated in Figure 1-1 for a basic two-level VSC. A fault on the DC side of the converter appears as a three-phase fault on the AC side. A bipolar converter based on typical half-bridge IGBT valves is unable to block this fault current [5].

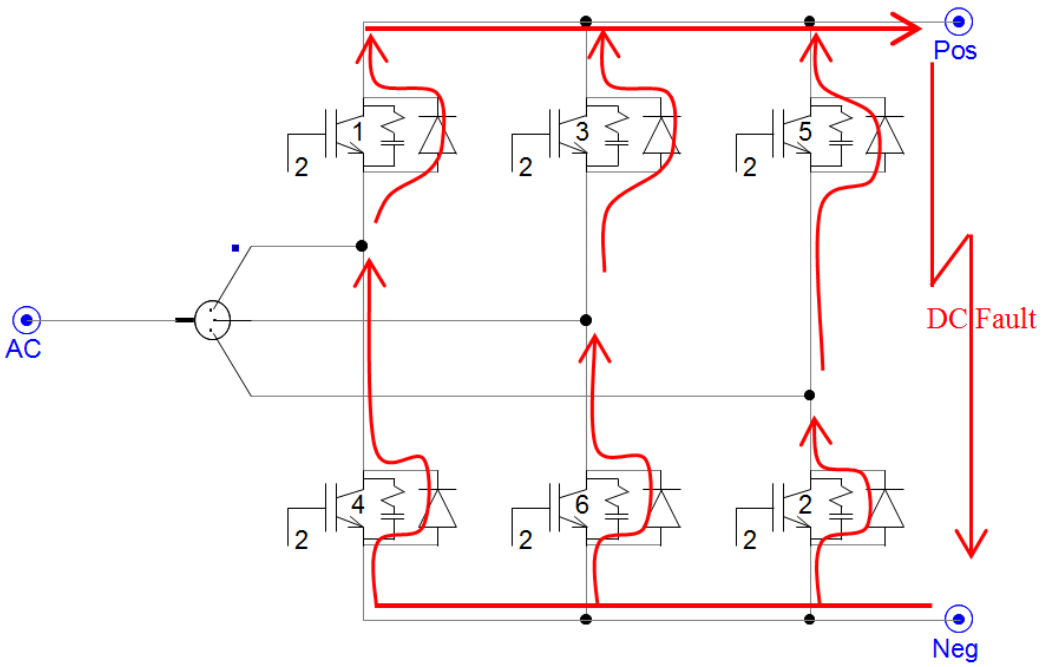

Figure 1-1 - IGBT Based Two-Level VSC Showing Freewheeling Diodes Which Allow a Fault Current Path from the AC System to Faults on the DC System

In order to harness the benefits of networking, DC line faults need to be detected, located and cleared with a minimum interruption to the healthy part of the HVDC grid. This requires appropriately positioned circuit interruption devices. The cost and limitations of current interruption capability of DC circuit breakers are major barriers for the development of HVDC grids and need to be considered in designing grids and the corresponding protection methodologies [6].

DC circuit breaker technology is still under development and the current interruption capability of the first generation devices are well below the steady state short circuit currents expected in DC grids [7] [8]. This necessitates interruption of fault currents before the rise beyond the capacity of DC circuit breakers, which in turn requires extremely fast fault detection and faulted element identification methods.

Protection against DC line faults is a prerequisite for implementation of DC grids. Although there are a few studies that discuss the protection of HVDC grids [9] [10] [11] [12], adequate protection solutions are yet to be developed. The main motivation for this project was to address this important need. In order to develop proper protection solutions, it is necessary to gain an understanding of how a DC grid would work during DC line faults and identify the critical

design factors for such a protection system. This invariably involves simulation-based investigations as resources required for experimentation with physical systems are prohibitive. The recently enhanced capability of modeling and simulation of VSC-based HVDC systems [13] [14] in electromagnetic transient simulation programs such as PSCAD [15], was an added motivation to undertake this research.

1.2 Objectives and Contributions

The overall objective of this research was to understand the behaviour of an HVDC grid during DC side faults and develop a method of detecting and discriminating faults within an adequate time frame. In order to achieve this objective, the state of the art of DC circuit breakers was reviewed and the protection system goals were identified. The thesis then proposed

(i) A method to locate the faulted line elements using local measurement within a very short time,

(ii) A strategy to select protection settings, and

(iii) A method to size the di/dt limiting series inductors to enable protection discrimination while meeting the limitations of the DC circuit breakers.

The proposed protection methods were implemented and evaluated on two different DC grids, a smaller grid with three converters and a larger grid with nine converters, modeled in PSCAD. The results are presented and discussed.

1.3 Organization

Chapter 2 discusses fault current behavior in a DC grid, analyzes the pros and cons of different options for responding to DC line faults, discusses DC circuit breaker capabilities, and details the proposed protection system goals.

Chapter 3 describes two of the PSCAD test grid models that were constructed and some of the initial simulation results that led to the proposed protection methods presented in Chapter 4.

Chapter 4 discusses the proposed method for a breaker to quickly determine if there is a fault

on the transmission segment that it is protecting and if it needs to trip. The studies that were performed to test the proposed concepts are detailed. The process for setting protection thresholds is discussed and the results of the process applied to the two test grids is documented.

Chapter 5 presents the results of studies performed to analyze the impact of di/dt limiting inductors on fault current and the process of sizing these inductors. The implementation of the hybrid DC breaker in PSCAD and the results of some studies including protective breaker action are discussed.

Chapter 6 presents conclusions that can be drawn from the simulation studies performed during this thesis and suggests some areas for further study.

2 Fault Response Options and Protection Goals

This chapter discusses fault current behavior in a DC grid, analyzes the pros and cons of different options for responding to DC line faults, discusses DC circuit breaker capabilities, and details the proposed protection system goals.

2.1 MMC Converters and Fault Currents

Modular Multilevel Converters (MMCs) are a type of Voltage Source Converter (VSC) which consists of multiple modules instead of the individual IGBTs seen in traditional two-level VSCs (as shown in Figure 1-1). A typical MMC layout utilizing half-bridge converter modules can be seen in Figure 2-1. While a two-level VSC relies on pulse width modulation (PWM) between two voltage levels to produce a sinusoidal AC voltage, an MMC can produce multiple different voltage levels resulting in a closer approximation of a sinusoidal wave with lower switching losses and less harmonics. Some MMC technologies utilize multiple voltage levels as well as some PWM while some use enough levels such that PWM is not required [14] [16].

MMC converters using half-bridge modules face the same downsides as two-level VSCs. It is necessary to have a diode to protect the IGBTs against reverse voltage. This can result in an unblockable fault current path in the event of a DC line or cable fault. Such a fault current path can be seen in Figure 2-2 [5].

An alternative to half-bridge based converters is full-bridge based converters. An example of a full-bridge module can be seen in Figure 2-3. Full-bridge converters can block fault current but have more losses during normal operations.

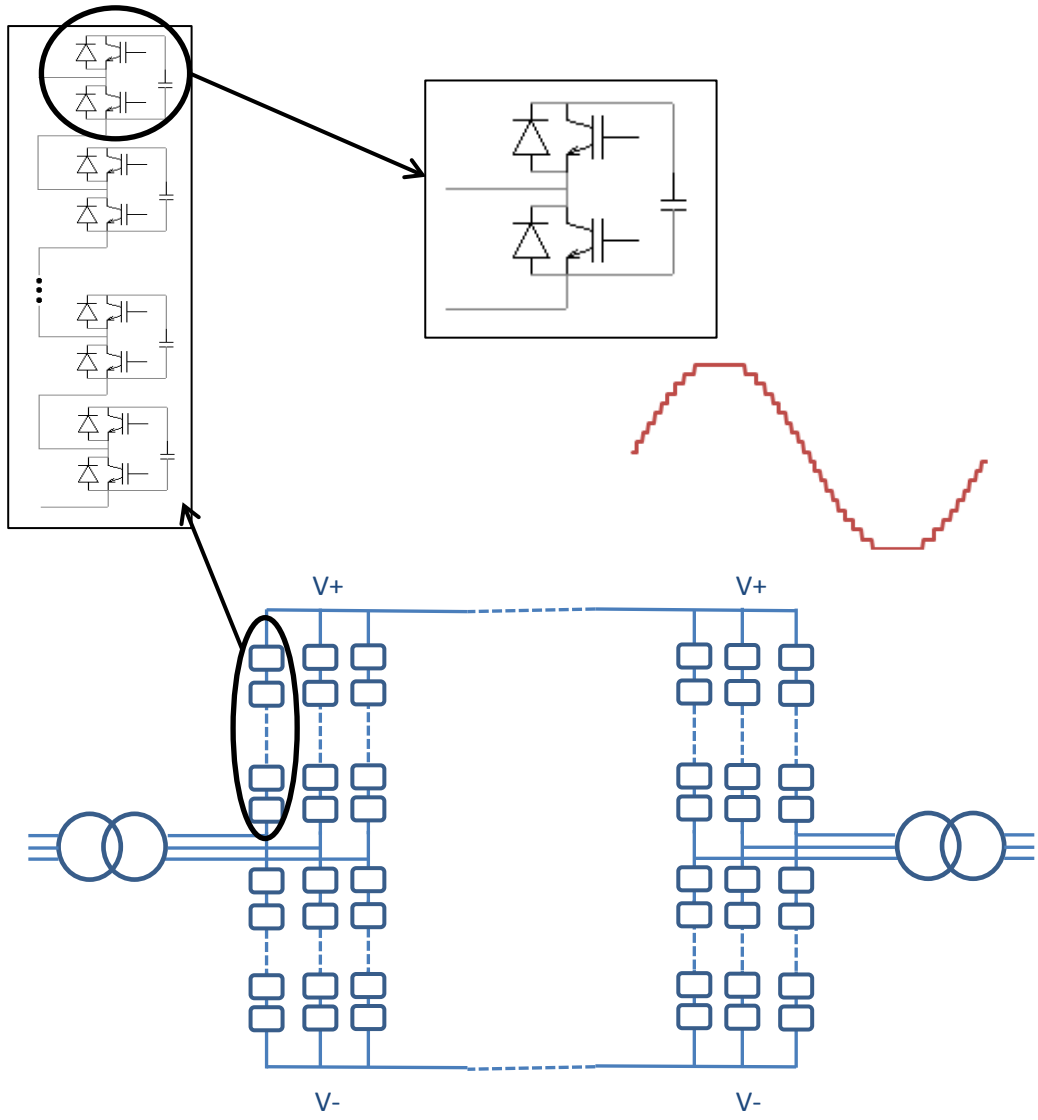

Figure 2-1 – Half-Bridge MMC Converter [14] [16]

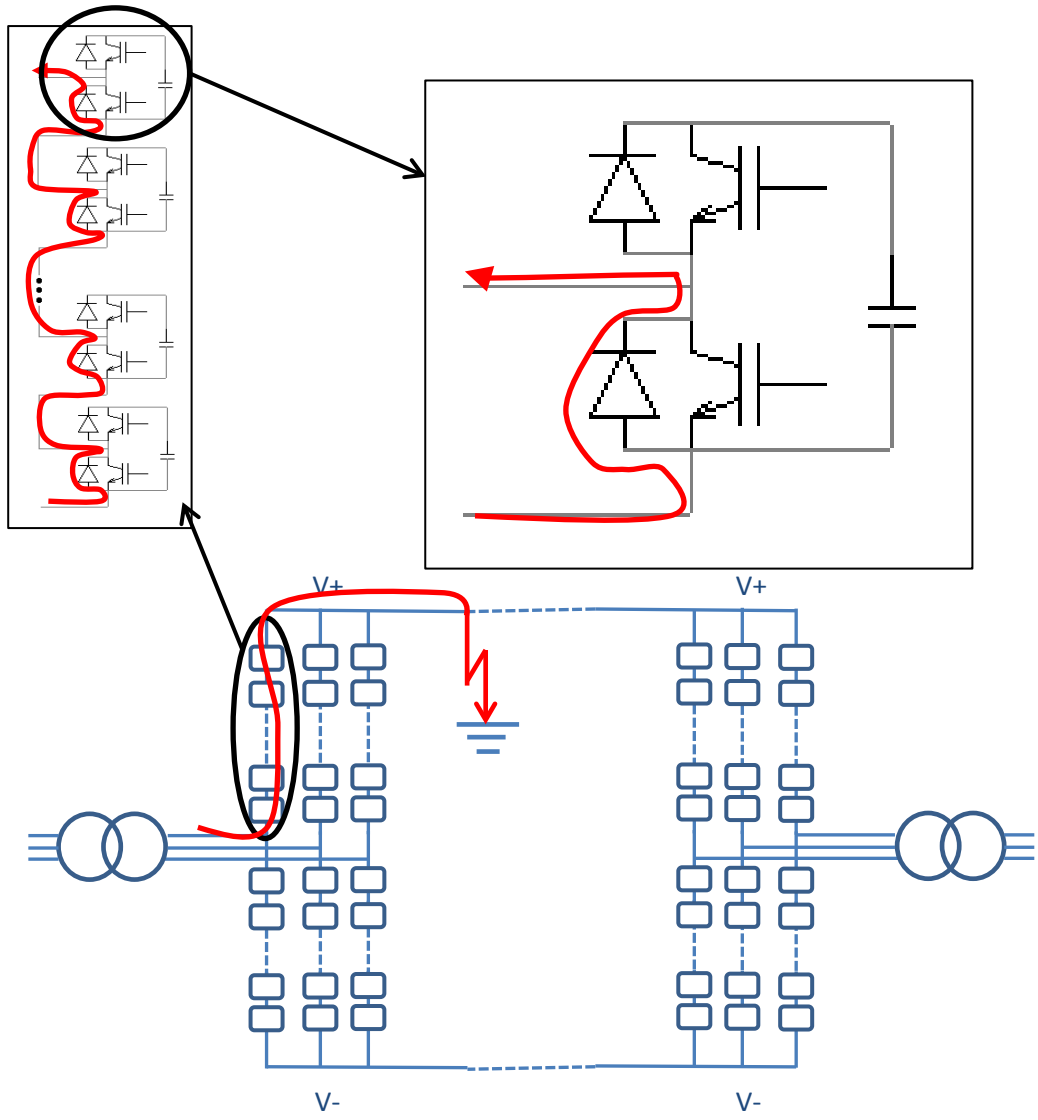

Figure 2-2 – Fault Current Path in MMC Converter

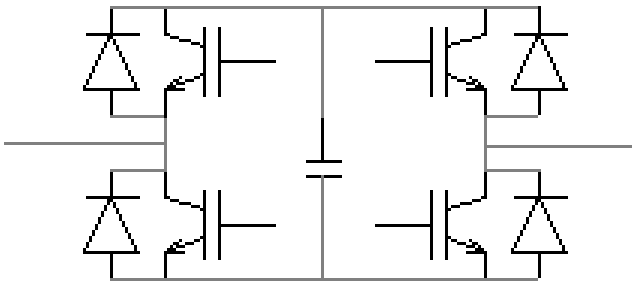

Figure 2-3 – Full-Bridge Module

2.2 Fault Current Behaviour in a VSC-based Grid

The path of steady state currents for a single pole-to-ground (P-G) fault in a DC grid depends on the configuration of the grid. An HVDC grid can have either monopole or bi-pole structure and could be operated with an earth return or a metallic return. Various possible configurations and earthing options are analyzed in [2]. The bi-polar structure with metallic return is most likely to be the HVDC grid configuration that meets operational, reliability, flexibility, extensibility, and environmental criteria. The type of earthing, location and number of earthing points affect the single pole-to-ground fault current paths and the protection scheme [2]. Unearthed HVDC grids have the distinct advantage of having no steady state fault current for single pole-to-ground faults [17], however cost of equipment would rise due to higher insulation requirements. Pole-to-pole (P-P) faults still result in a fault current path similar to that of earthed grids. Multiple earthing of an HVDC grid could result in steady state stray currents that lead to ground potentials and DC currents in nearby pipe lines and AC lines [2], and therefore may not be acceptable. Thus, in this study, a bipolar HVDC grid with a metallic return and a single earthing point, which is the most likely configuration in a practical HVDC grid, is considered. The fault current paths for a single pole-to-ground fault in such a grid are shown in Figure 2-4.

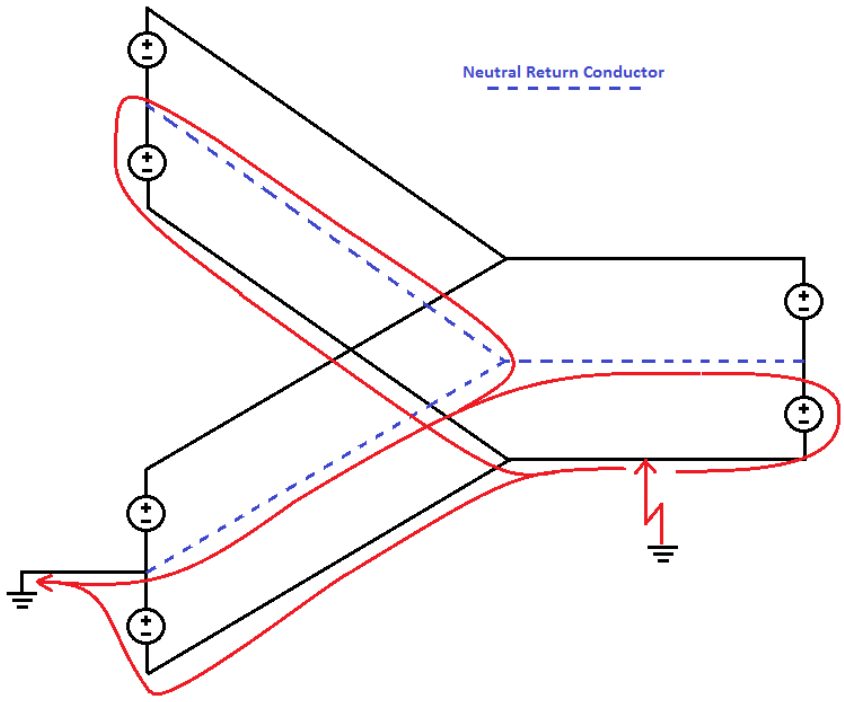

Figure 2-4 - Steady State Fault Current Path in Grounded Bi-Pole Grid

2.3 Fault Response Options for Earthed HVDC Grids

There are four basic options for how to respond to a DC fault in a VSC-based earthed grid:

1. Trip the AC circuit breakers at each converter on the grid. The grid would be disconnected and the fault current would be interrupted. The faulted segment could be located based on fault current direction. While this could be done with a central controller and communications, methods based on local measurements with no need for communications exist [18]. Mechanical switches could open the faulted segment and the grid could be restarted [16]. This would be adequate for small DC grids but would not be acceptable for very large systems.
2. Use full-bridge MMC VSC converters. Full-bridge MMC converters can block fault currents [19]. Upon detection of a fault, all the converters could block the current. The fault current would be interrupted, mechanical switches could isolate the fault and grid operation could be restarted. This new technology would be faster than the AC breakers but would still interrupt power flow across the entire grid for a period of time.
3. DC breakers could be placed in series with each converter [20]. During a line fault the DC breakers would block fault currents from all the converters. The lines and cables would discharge into the fault, mechanical switches would be opened to clear the faulted segment and then the DC breakers would close and restore the grid.
4. Use DC circuit breakers in a manner similar to how AC circuit breakers are used. Breakers would be placed at the ends of all line or cable segments. Fault currents would be interrupted and the faulted segment isolated without interrupting the operation of any of the converters or discharging the remote sections of the grid.

It is the fourth approach that was studied in this thesis and will be further discussed in this thesis.

2.4 DC Breakers

It is possible to interrupt DC current with a passive commutation circuit. Such a circuit would include a resonant LC circuit in parallel with a mechanical switch in parallel with a surge arrester as shown in Figure 2-5. Upon opening the switch, an arc would occur in parallel with the LC circuit and a current resonance would be induced [21]. As this resonating current crosses zero, the arc would be extinguished. The arrester would absorb the energy stored in the LC circuit and

the nearby lines. The operating time would be in the range of 10s of milliseconds. This type of breaker is not fast enough for a large scale HVDC grid [22]. If the clearing time is too long, the entire grid will discharge into the fault [23]. A prolonged DC fault will draw fault currents from the AC system at each converter.

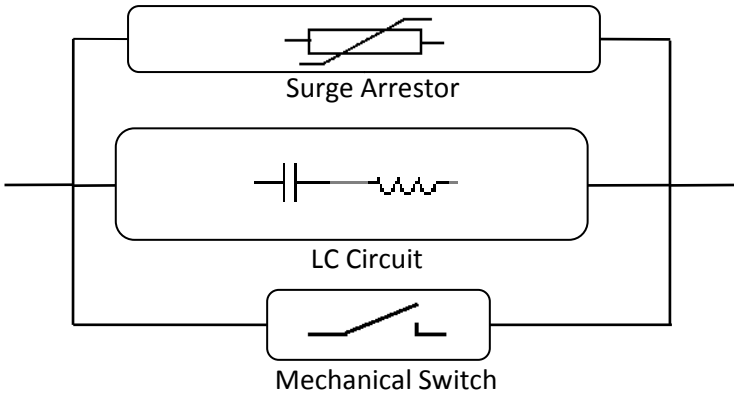

Figure 2-5 – Mechanical Resonant DC Breaker [7]

Another option is to use a solid state device such as an IGBT as a DC breaker. The advantage of this is that it is very fast. The operating time could be in the microseconds range. The disadvantage of this approach is that solid state devices are expensive and lossy. With many of these breakers in the system, significant power losses would occur. Large cooling systems would be necessary. These losses would be a major factor in designing the protection scheme and the layout of the grid itself [6].

The DC breaker approach that was considered in this thesis is the hybrid DC breaker. A hybrid DC breaker consists of a small solid state breaker in series with a very fast mechanical switch in parallel with a large solid state breaker in parallel with a surge arrester, as shown in Figure 2-6.

ABB has tested devices with an operating time of 2 ms, a maximum breaking current of 9 kA and a transient voltage capability of over 1.5 pu during current breaking. They have proposed a device with a maximum breaking current of 16 kA [7]. Alstom grid is developing and testing a similar device [8].

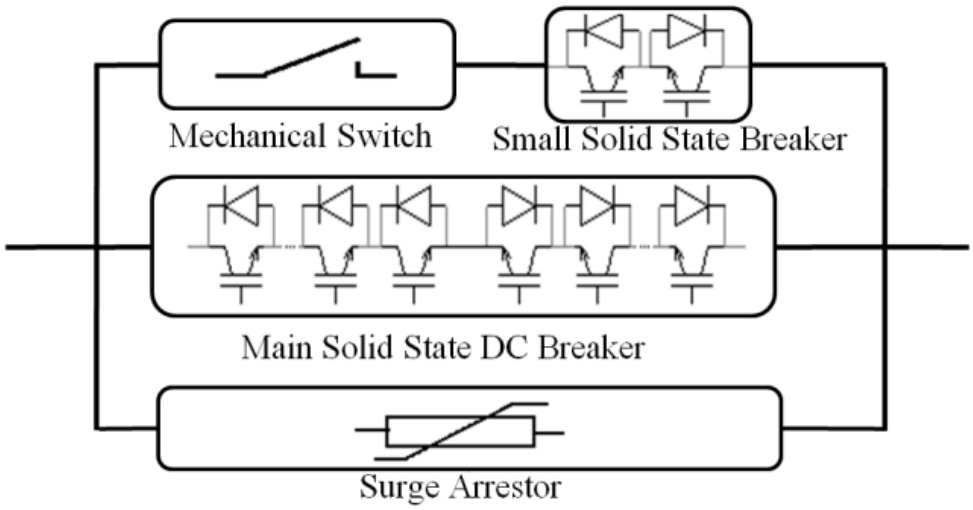

Figure 2-6 - Hybrid DC Breaker [7]

During normal operation, the current is going through the small solid state breaker, hence the losses are low. When a fault is detected, the small solid state device blocks and commutates the fault current into the main solid state device. At this time the fast mechanical switch is triggered. Opening this switch may take approximately 2 ms. Once this switch is opened, the large solid state device blocks and the current is commutated into the surge arrester which limits the voltage across the large solid state device to a tolerable limit.

2.5 **Requirements of an Earthed HVDC Grid Protection System**

The goal of the earthed bi-pole DC grid protection system proposed and studied in this thesis is similar to that of an AC protection system: to detect line faults and remove the faulted sections from the grid. Any individual line or cable fault should be detected and isolated without the loss of any other element in the system (other than radially connected converters).

The fault detection and location addressed in this thesis consists only of determining if the fault is on the immediate line or cable segment for the purpose of initiating a breaker action. There are established methods of determining exact fault locations on point-to-point DC lines for repair purposes [24]. A lot of good work has been done in adapting these methods to more complicated grid configurations [25]. This simulation effort only considered the challenge of determining which segment the fault is on.

While it is important to clear the faulted section before the rest of the DC and AC networks are adversely affected, in this case the main requirement for fast fault detection is the hybrid DC breaker operating time and the maximum breaking current. The peak fault currents of practical HVDC grids are likely to be much higher than the breaking capacity of proposed DC breakers. If the fault current may exceed the maximum breaking current, then it is necessary to break the fault current before it exceeds this level while it is still in the rising phase. This concept is illustrated in Figure 2-7.

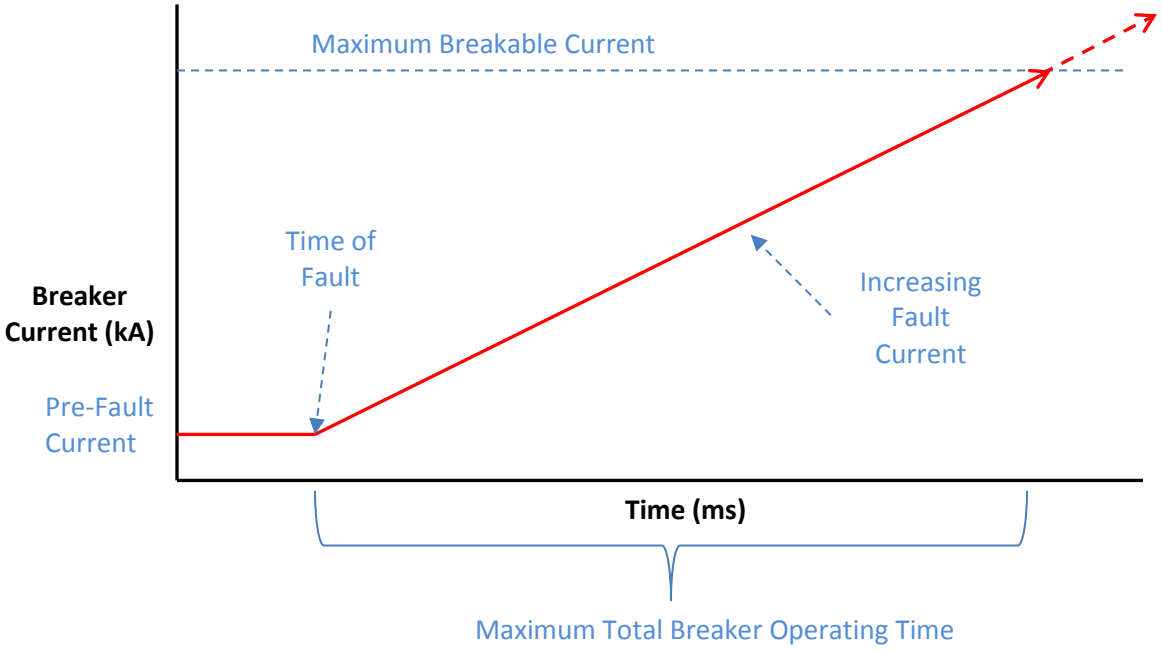

Figure 2-7 – Fault Current Rise through Breaker Concept

The breaker needs to detect the fault and operate within the time it takes for the current to exceed the maximum breaking current.

Figure 2-8 shows a fault detection scenario. Assuming that we have fast DC breakers at both ends of each line segment, a fault at location F1 should result in breakers B41 and B14 opening to isolate the faulted element. A fault F2 or F3 on the adjacent segments should not result in tripping of B41 or B14. The breakers at B41 and B14 need to be able to quickly identify the faulted line segment. For bus fault F4, B14 should trip but B41 needs to determine that the fault is beyond the breaker B14 and therefore not trip.

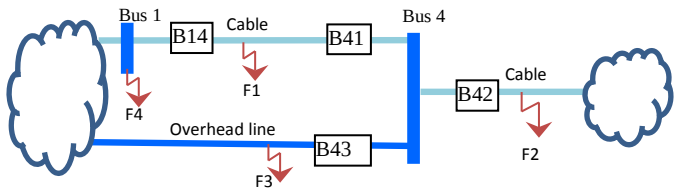

Figure 2-8 - Fault Detection Scenario

Two challenges with this type of protection system are quickly detecting/locating the faulted segment and limiting the fault current rise to interruptible levels for the breaker operating time [26]. The situation shown in Figure 2-7 demonstrates the both of these concerns. If the rate of rise of fault current through the breaker can be reduced, the maximum breaker operating time can be increased. As this maximum breaker operating time includes the detection and location of the fault as well as the operation of the breaker, it is ideal to not depend on long distance communications to locate the fault. If a fault is detected by B14 in Figure 2-8 and it has to wait for a communication to be sent to B41 and be returned confirming that the fault is indeed on the cable from bus 1 to bus 4, a significant time delay is added to the detection phase. For this reason and for reasons of communications reliability issues, a solution involving fault detection and location using only local measurements is preferred.

2.6 **Concluding Remarks**

This chapter discussed fault current behavior in a DC grid, analyzed the pros and cons of different options for responding to DC line faults, discussed DC circuit breaker capabilities, and detailed the proposed protection system goals. Chapter 3 will describe the PSCAD models which were used to evaluate these concepts and which led to the proposed protection system evaluated in Chapters 4 and 5.

3 DC Grid Modeling and Simulation

This research began as a desire for a fundamental understanding about how DC grids could work and how they could be protected. The method chosen for acquiring this knowledge consisted largely of simulation experiments carried out using PSCAD software. This chapter will describe two of the test HVDC grid models that were simulated in PSCAD and some of the initial simulation results that led to the proposed protection methods presented in Chapter 4.

3.1 Test HVDC Grids

Two of the constructed DC grid test cases are presented in this section. Section 3.1.1 presents the three converter small HVDC grid used to explain the proposed new protection concept, and Section 3.1.4 presents the nine converter large HVDC grid used to demonstrate the application of the protection system. Sections 3.1.2 and 3.1.3 give details of the converter controllers, and cable and line models respectively.

3.1.1 Three Converter Test Grid

A three converter test grid was modeled in PSCAD to study the proposed protection concept. A grid of this small size could be shut down in the event of a fault. However, it is useful for testing and demonstrating the protection principals that could be applied to a larger DC grid. The larger the grid, in terms of total power transfer and numbers of converters, the less feasible it is to shut down all converters in the event of a fault.

The Single Line Diagram (SLD) in Figure 3-1 shows the layout of the test grid. Three converter busses are connected to a central bus in a radial Y configuration. All converters are connected to equivalent sources on the AC side. The bipolar DC grid is rated at ±320 kV, and consists of one overhead line (1500 km) and two cables (500 km and 100 km).

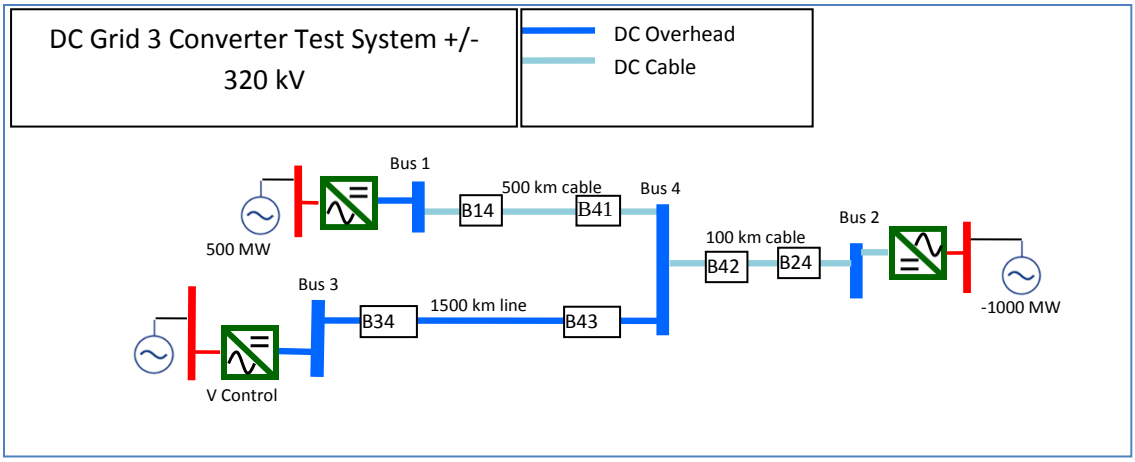

Figure 3-1 - Three Converter Test System

The representation of the three converter test grid in PSCAD is shown in Figure 3-2. Converters and controls are modeled in detail in the page modules.

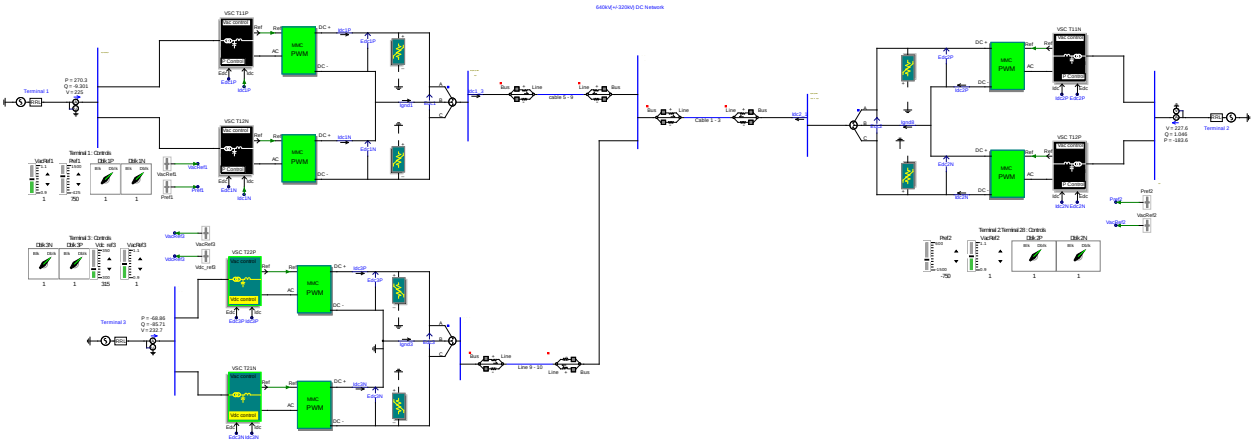

Figure 3-2 - Three Converter PSCAD Model

3.1.2 **Converter and Controller Models**

The AC to DC converter valve and controller models used in this study were provided by the Manitoba HVDC Research Center [14] [13]. They are generic multilevel VSC models. Two of the converters are in power control mode and one is in voltage control mode. This is simpler than a realistic grid steady state power and voltage control scheme, but is adequate for simulating the operation of protection functions.

Each AC/DC converter was modeled using control blocks and valve group blocks provided by WG B4-57 and the HVDC Research Center. For example, Figure 3-3 is the PSCAD representation of a converter on a bi-pole grid with a metallic return. It uses control blocks that adjust the valve group firing angles to control power and AC voltage. The valve group is a generic representation of a MMC module that uses 38 voltage levels as well as some pulse width modulation (PWM).

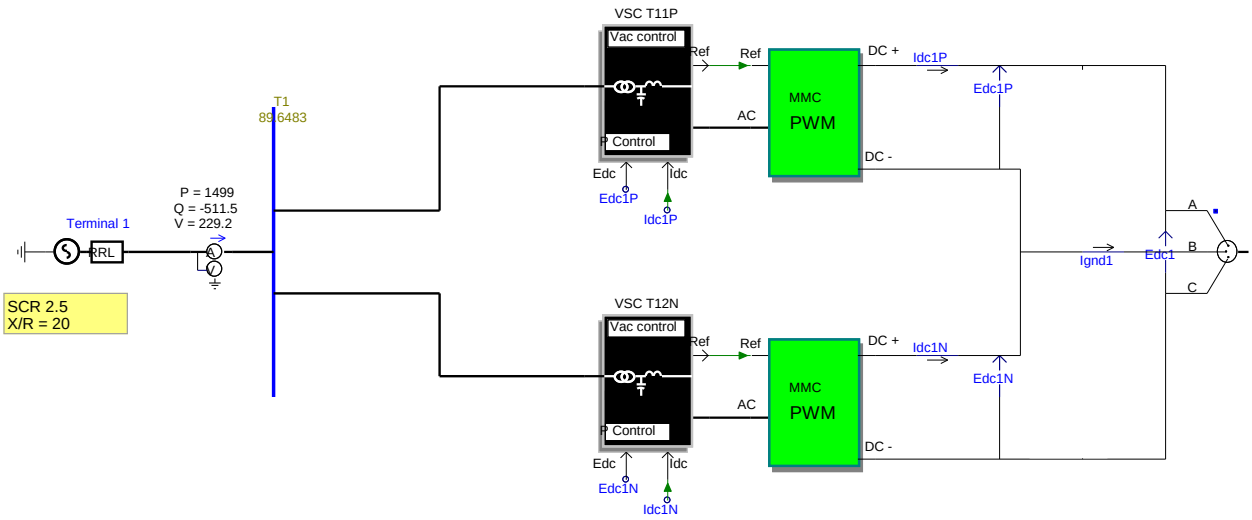

Figure 3-3 - MMC Module with Power Control and 38 Levels with PWM

The converter shown in Figure 3-4 is on a bi-pole grid with an electrode based earthing scheme. It has a control block that adjusts the valve group firing angles to control both the DC voltage and the AC voltage. The valve group is a generic representation of a MMC module that uses 98 voltage levels and no PWM.

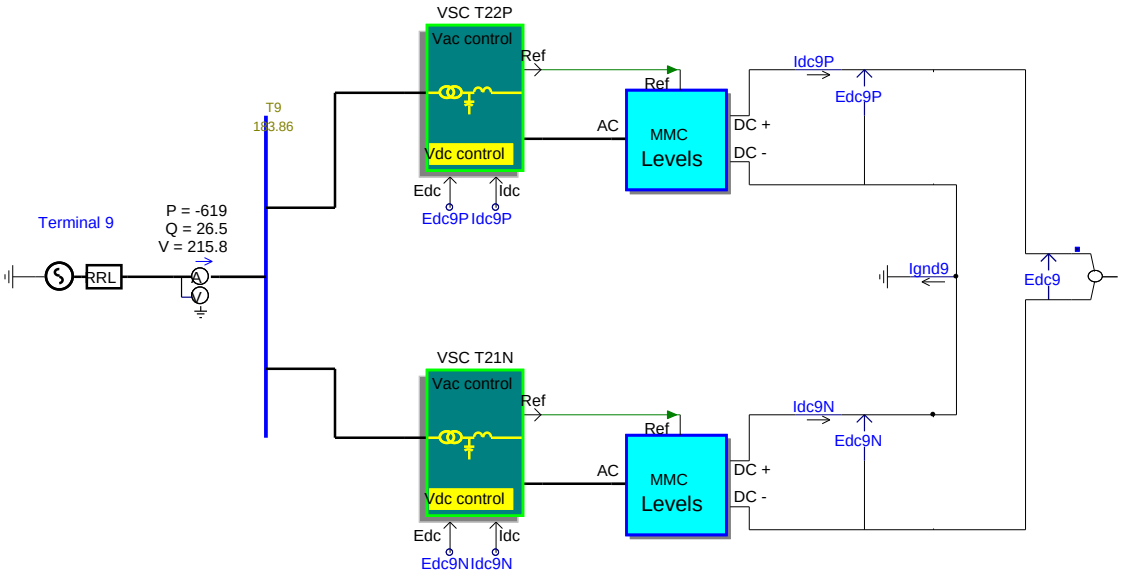

Figure 3-4 - MMC Module with Voltage Control and 98 Levels

3.1.3 **Cable and Line Models**

DC cable and line models were chosen somewhat arbitrarily and scaled to set the resistances such that the voltage drop across the respective test grid was approximately 10%. Scalability of DC grids is a challenge. A grid can be designed and conductors can be sized for a certain voltage drop under certain conditions. If the grid is later expanded the chosen maximum voltage drop may be exceeded. In the AC system reactive power can be added to raise voltages. The solution to this problem for a DC grid is a DC/DC converter to control voltage. Functionally this might be operated similarly to a phase shifting transformer in an AC system. DC/DC converters were not modeled in this thesis. The configurations of the cables and overhead lines used in the simulation are shown in Figure 3-5 and Figure 3-6 respectively.

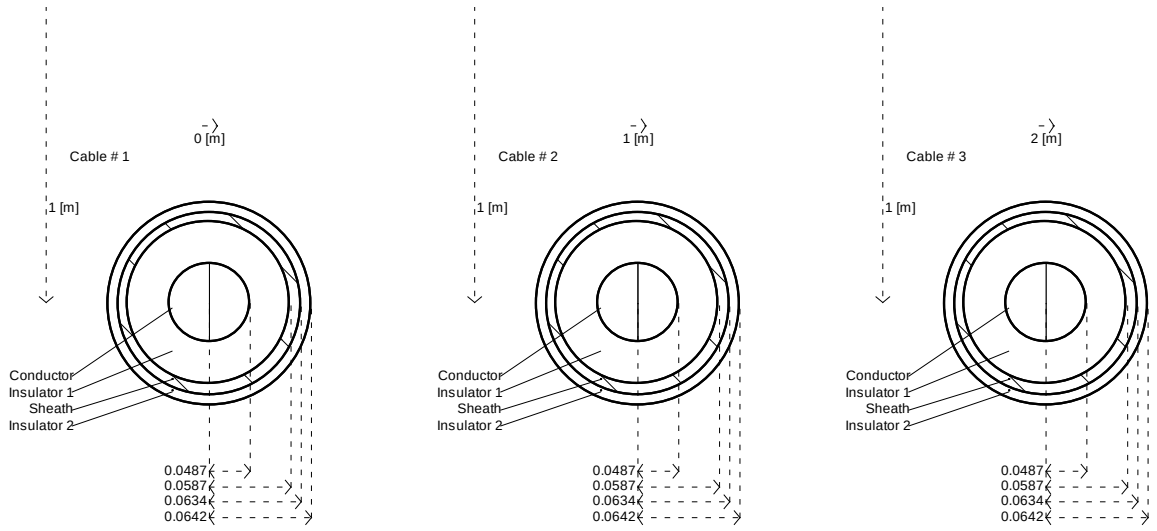

Figure 3-5 - DC Cable Models

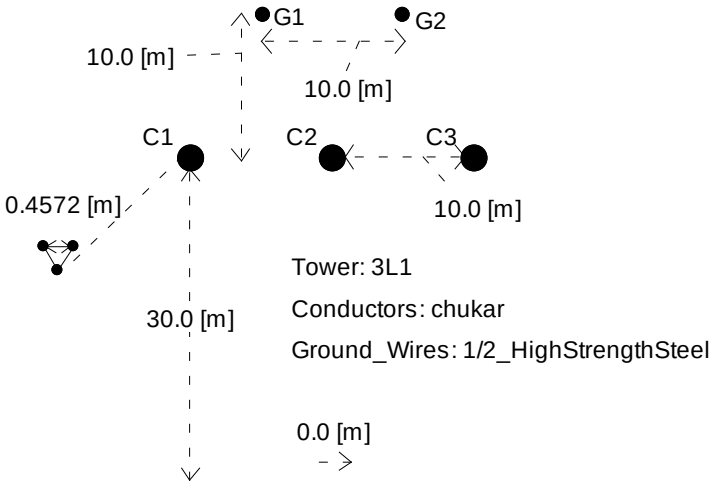

Figure 3-6 - DC Line Models

3.1.4 **Nine Converter Test Grid**

The nine converter test grid was obtained by slightly modifying a benchmark grid template draft proposed by WG B4-58 [27]. Its structure is shown in Figure 3-7. The network contains both overhead lines and cables, and has a meshed structure.

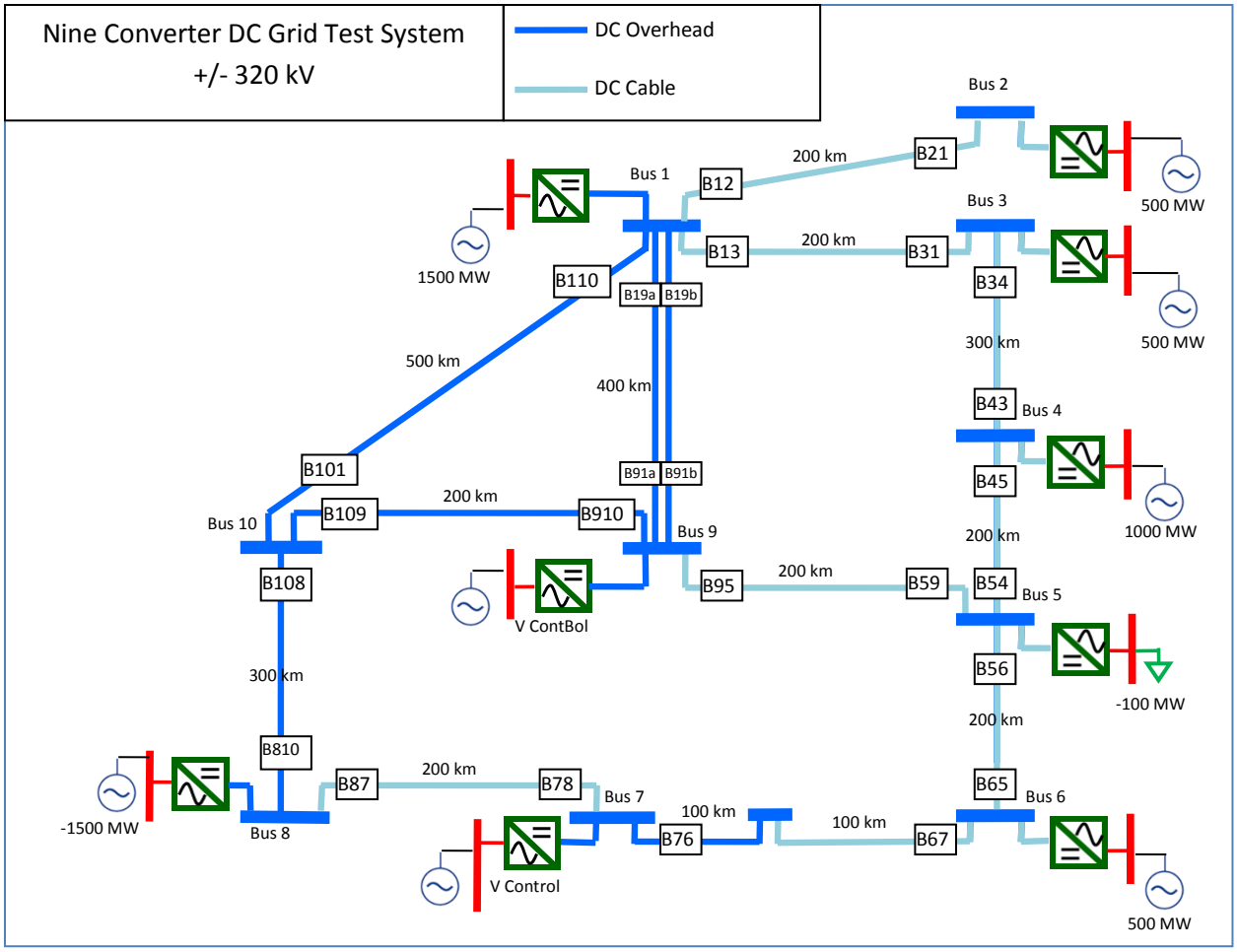

Figure 3-7 - Nine Converter Test Grid

The AC system present in the initial draft template proposal was largely removed. This thesis did not include AC faults or impacts on the AC system so only the ±320 kV DC network is represented. It is assumed that each line segment will have a relay and breaker on each end. These are represented in Figure 3-7 by the white boxes with 'B' and the number of the breaker.

The PSCAD case of the nine converter bi-pole DC grid with the metallic return based earthing is shown in Figure 3-8. The overhead lines and the cables in the model use the configurations described in Section 3.1.3.

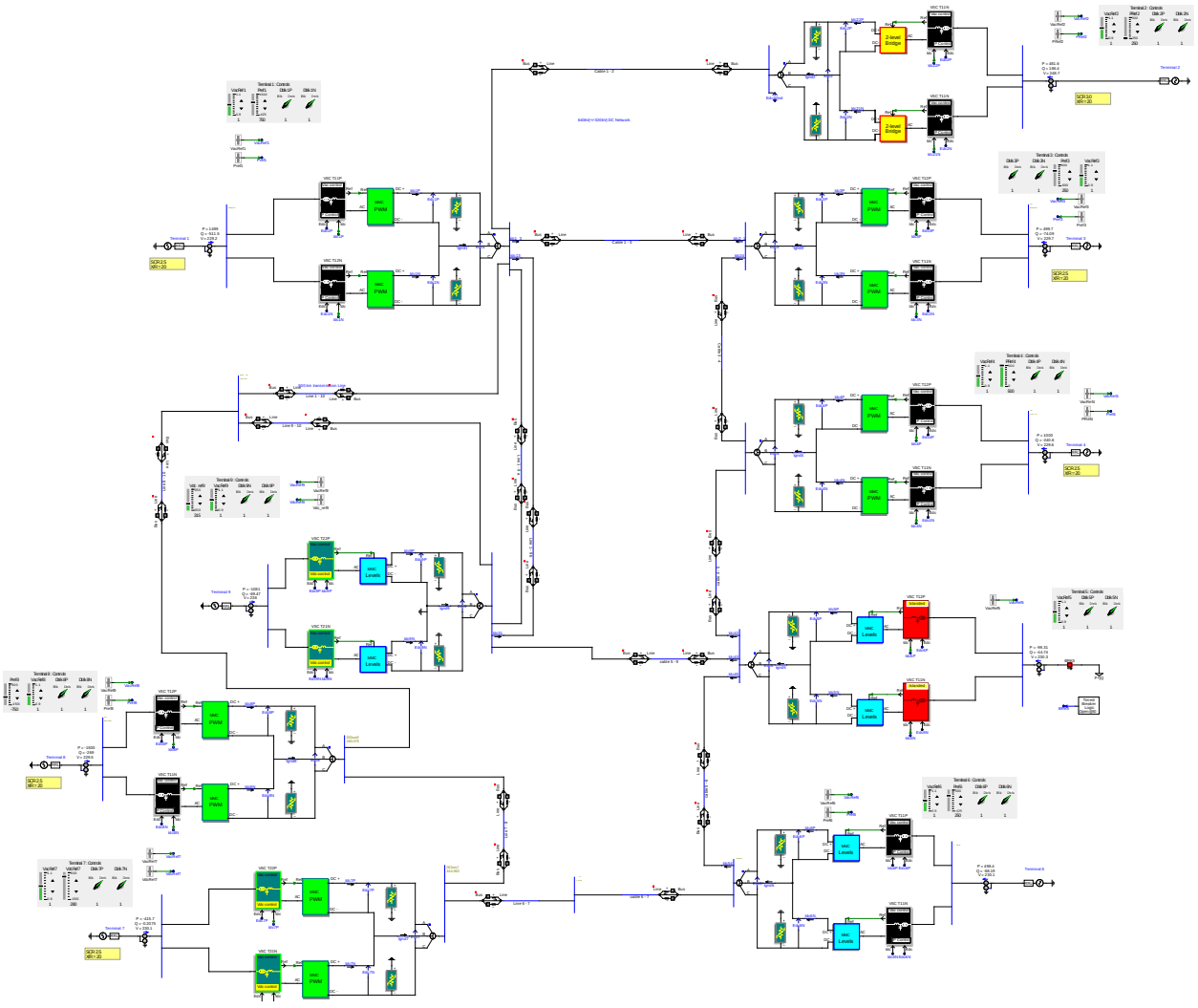

Figure 3-8 - Nine Converter Test Grid in PSCAD

In this nine converter test case, two converters were tasked with controlling DC voltage. Six converters were set to control power. These eight converters were all connected to an AC source with a fixed impedance. One additional converter was modeled with an islanded control mode. It was set to control AC voltage and AC frequency. A fixed impedance load was attached to the AC bus such that it draws 99 MW and 45 MVAR at rated voltage and frequency. This is represented as shown in Figure 3-9 with electrode based earthing.

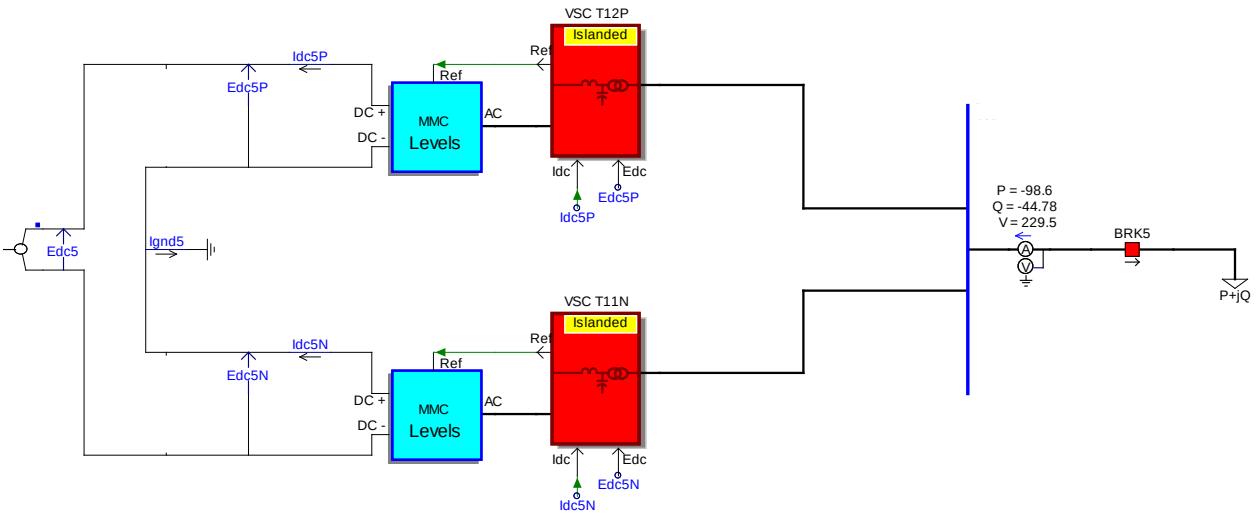

Figure 3-9 - MMC Module with Islanded AC Frequency Control

A DC grid may be operated with only one converter doing primary voltage control but all converters will help to control voltage when the voltage is above or below certain limits. The control blocks available for this study modulate their real power to control DC voltage, AC frequency or real power. For the purposes of this study two converters were assigned to voltage control mode to help with start-up stability.

3.2 Preliminary Study Results and Protection Challenges

Preliminary fault studies were run with the three converter test grid. No protections or current limiting devices were in place for these simulations. Initial fault simulations are shown in Section 3.2.1. Simulations of faults shown from the perspective of all breaker locations are discussed in Section 3.2.2. Section 3.2.3 gives an example steady state fault current flow for the nine converter test grid. In these simulations, it was assumed that there are no series inductors to limit the initial rate of rise of fault currents.

3.2.1 Fault Simulations – Three Converter DC Grid

For the given three converter test system, with the neutral grounding point at bus 3, a single pole-to-ground (P-G) fault at bus 1 terminal of the cable was simulated at time = 2.5 s. The fault location can be seen in Figure 3-10. The measurements taken at each breaker location can be

seen in Figure 3-11. For these simulations the inductor shown in Figure 3-11 was set to 0 mH.

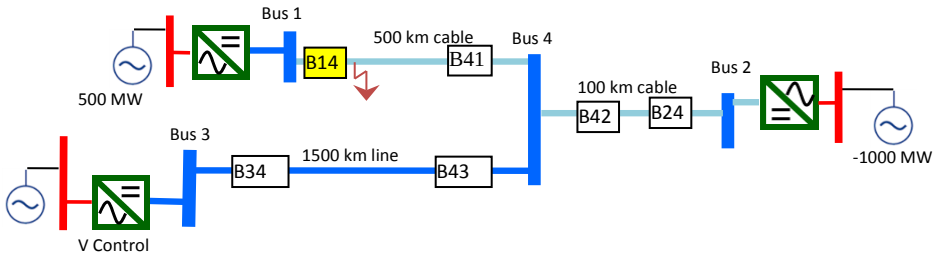

Figure 3-10 – Fault at Cable Terminal at Bus 1

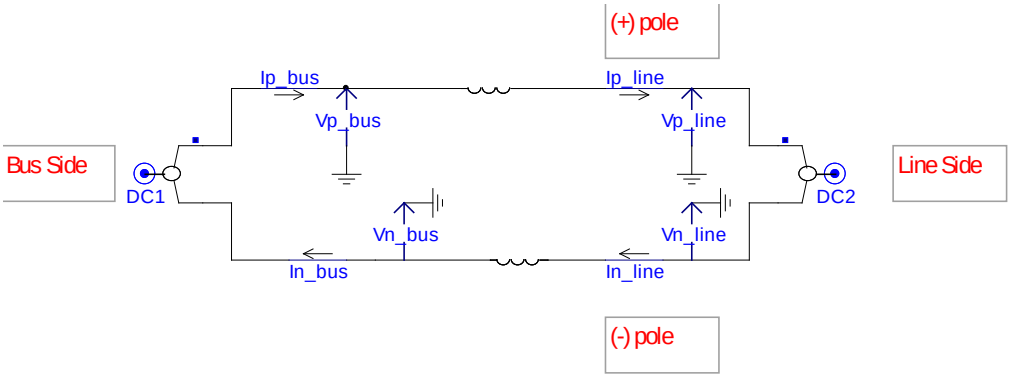

Figure 3-11 – Measurements at Each Breaker Location

The voltages at bus 1 and the currents measured at breaker B14 during the fault are shown on Figure 3-12 and Figure 3-13 respectively.

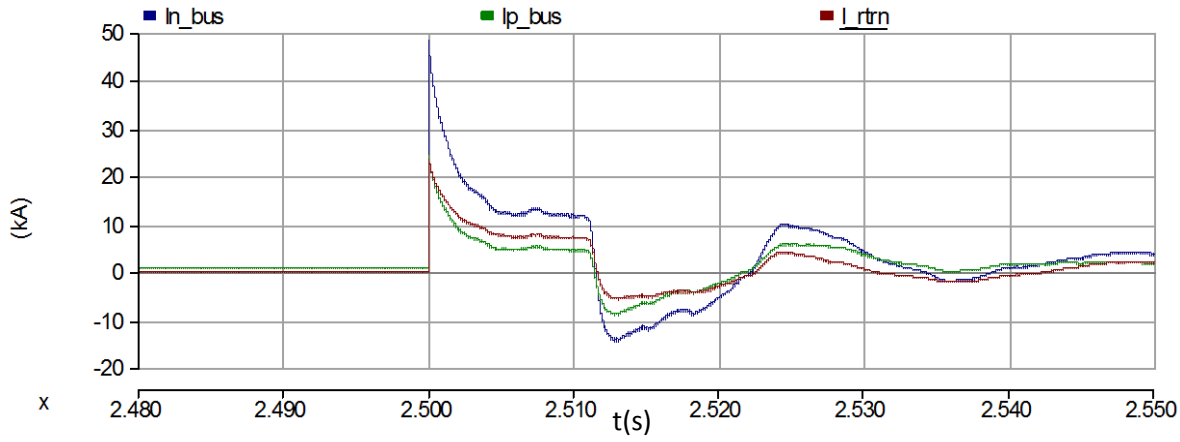

Figure 3-12 - Currents at B14 during a Pole-to-Ground Fault at Bus 1 end of the Cable (In_bus - current on negative pole, Ip_bus – current on negative pole, and I_rtn – current on return conductor)

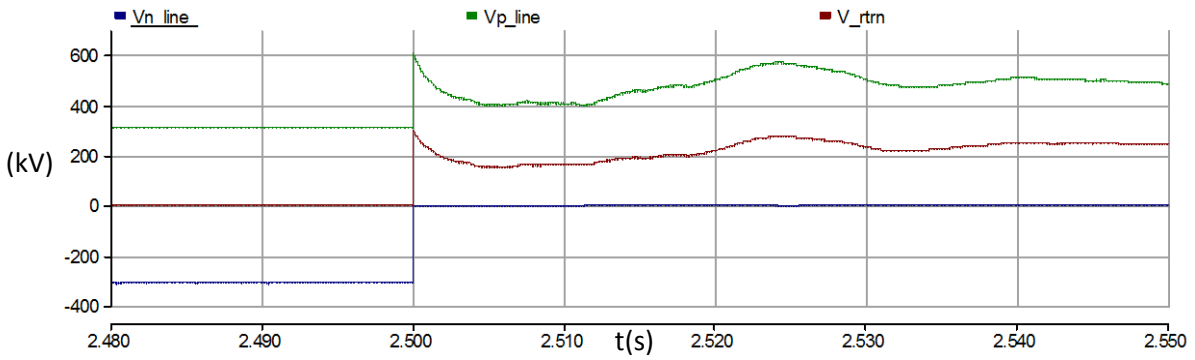

Figure 3-13 - Bus 1 Voltages during a Pole-to-Ground Fault at Bus 1 end of the Cable (Vn_line – voltage of negative pole, Vp_line – voltage of positive pole, and V_rtn – voltage on return conductor)

It can be seen in Figure 3-13 that the non-faulted pole experiences a temporary 2 pu overvoltage while the neutral return line experiences a temporary overvoltage up to approximately 1 pu of the rated pole voltages. Voltage doubling like this is a typical characteristic of an ungrounded DC grid but occurs in this grounded grid simulation due to two factors: (i) the long distance between the fault location and the single point on the grid at which the neutral metallic return ground path is grounded, and (ii) the short distance between the fault and a nearby AC/DC converter. In Figure 3-14 and Figure 3-15, the fault currents and voltages from Figure 3-12 and Figure 3-13 are plotted on a longer time scale and it can be seen that the voltage doubling is a transient phenomenon instead of a steady state phenomenon as with ungrounded grids.

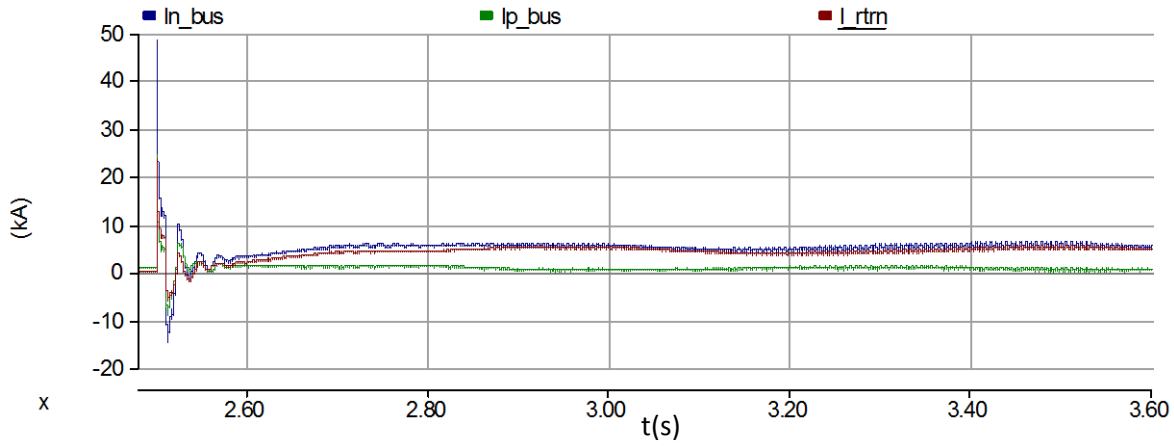

Figure 3-14 - Currents at B14 during a Pole-to-Ground fault at Bus 1 end of the Cable (In_bus - current on negative pole, Ip_bus – current on negative pole, and I_rtn – current on return conductor)

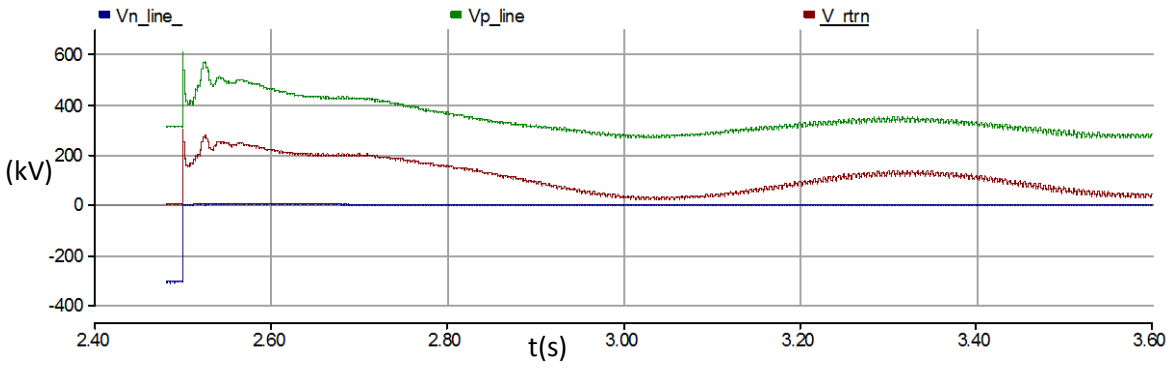

Figure 3-15 - Bus 1 Voltages during a Pole-to-Ground Fault at Bus 1 end of the Cable (Vn_line – voltage of negative pole, Vp_line – voltage of positive pole, and V_rtn – voltage on return conductor)

In the short term, a fault far away from the point on the grid where the metallic return is grounded acts like a fault on an ungrounded grid. The short term impact to the voltages is a shifting of the neutral line voltage up to 1 pu of the operating voltage and an approximate doubling of the non-faulted pole voltage.

The steady state result consists of fault current on the faulted line and the neutral line. During the initial transient period, there is a large fault current on the non-faulted pole as well, but this quickly drops to zero. It can be observed in Figure 3-12 and Figure 3-14 that the fault currents initially rise and then temporarily switch directions due to oscillations and traveling waves before settling into their respective steady-state values.

When the fault is located at the line terminal at bus 3 (as shown in Figure 3-16) close to the neutral line grounding point, the short term variations of the currents through B34 and the voltages at bus 3 are as shown in Figure 3-17 and Figure 3-18 respectively.

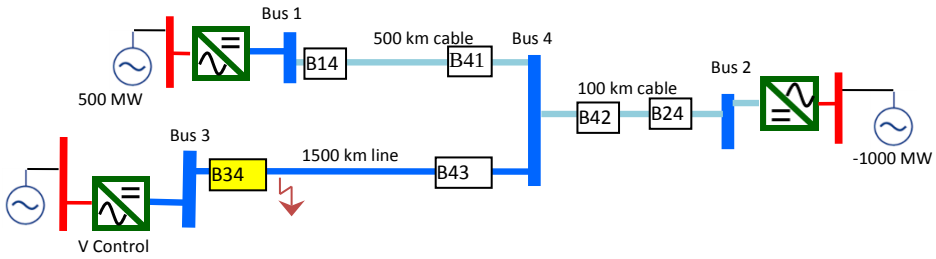

Figure 3-16 – Fault at Line Terminal at Bus 3

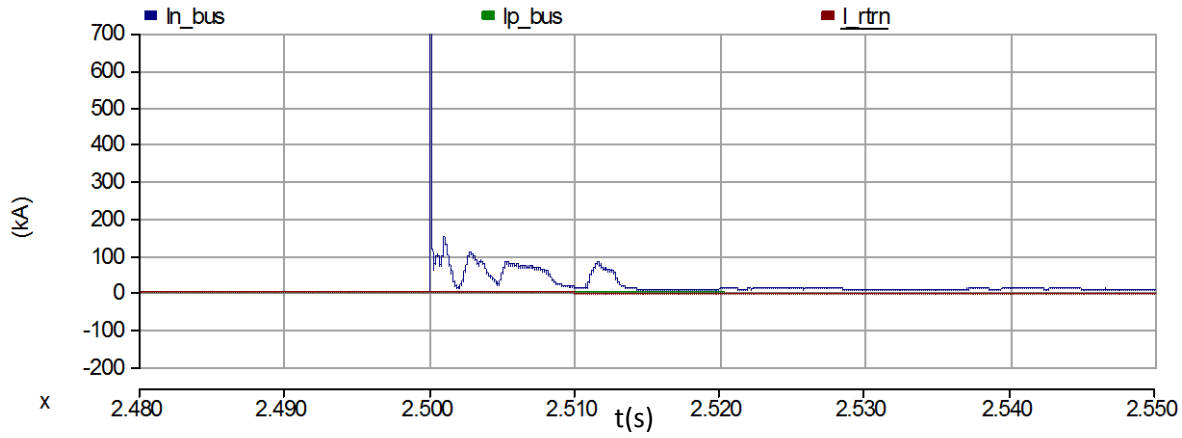

Figure 3-17 - Currents at B34 during a Pole-to-Ground Fault at Bus 3 end of the Line (In_bus - current on negative pole, Ip_bus – current on negative pole, and I_rtn – current on return conductor)

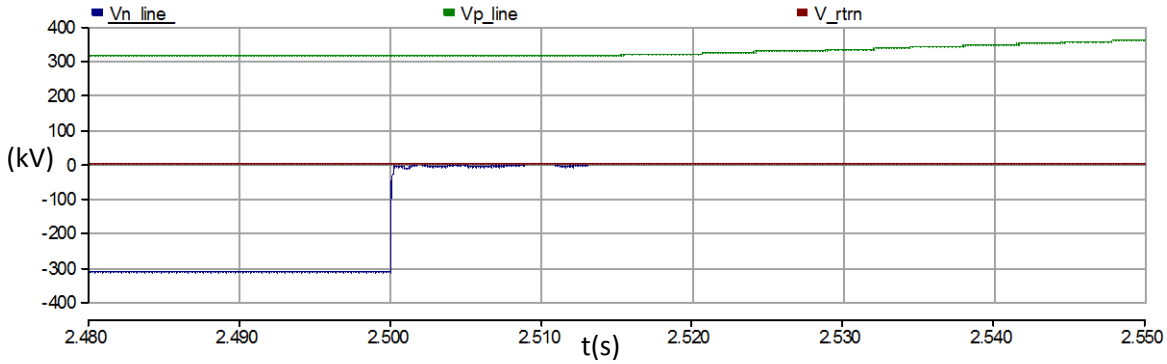

Figure 3-18 - Bus 3 Voltages during a Pole-to-Ground Fault at Bus 3 end of the Line (Vn_line – voltage of negative pole, Vp_line – voltage of positive pole, and V_rtn – voltage on return conductor)

For this fault, the initial current is higher due to a rapid discharge of capacitance in the half-bridge converter, and in the lines and cables. On the other hand, the metallic return wire voltage stays at zero, and the non-faulted pole voltage does not change significantly even during the first 10 ms following the fault. The voltage of the faulted pole drops to zero and remains at zero.

The same currents and voltages are plotted on a longer time frame in Figure 3-19 and Figure 3-20.

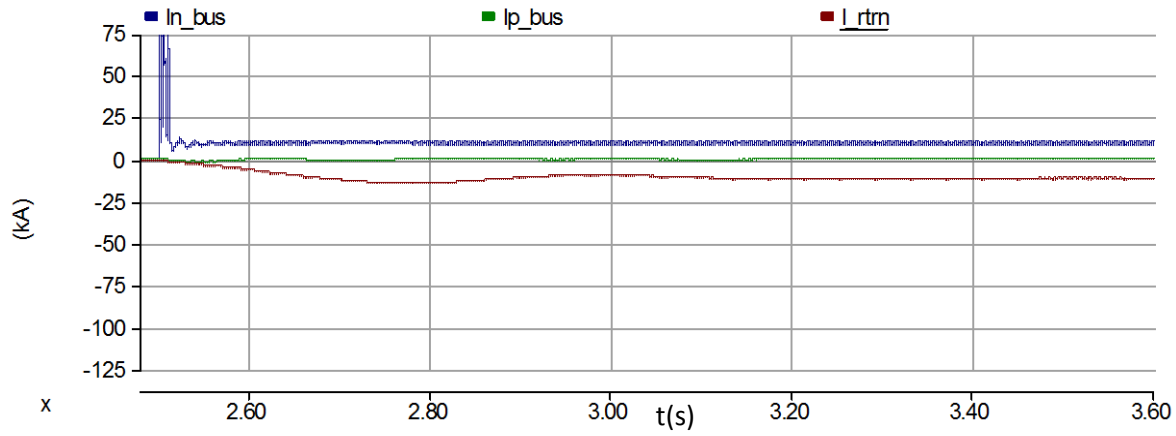

Figure 3-19 - Currents at B34 during a Pole-to-Ground Fault at Bus 3 end of the Line (In_bus - current on negative pole, Ip_bus – current on negative pole, and I_rtn – current on return conductor)

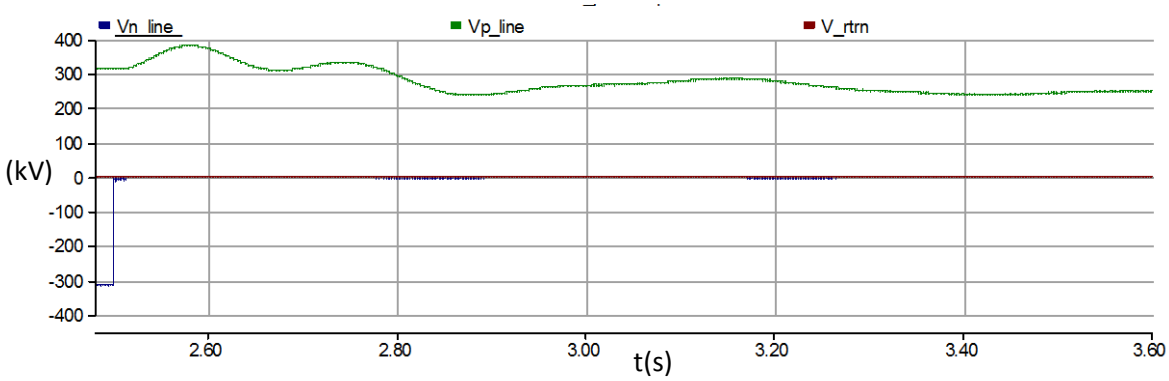

Figure 3-20 - Bus 3 Voltages during a Pole-to-Ground Fault at Bus 3 end of the Line (Vn_line – voltage of negative pole, Vp_line – voltage of positive pole, and V_rtn – voltage on return conductor)

As expected, a high steady state fault current flows on the faulted pole and on the metallic return line. The steady-state current on the non-faulted pole is similar to the pre-fault current. The positive pole voltage is somewhat impacted by the negative pole short to ground affecting the AC system.

The metallic return line current is supplying a fault current path from the ground at bus 3, through the grid to the other negative pole converters and from there to the fault through the negative lines in the grid.

In the third simulation, a pole-to-pole (P-P) fault was created at the terminals of the converter connected to bus 3 (same location shown in Figure 3-16), the currents and voltages at breaker B34 are shown in Figure 3-21 and Figure 3-22 respectively.

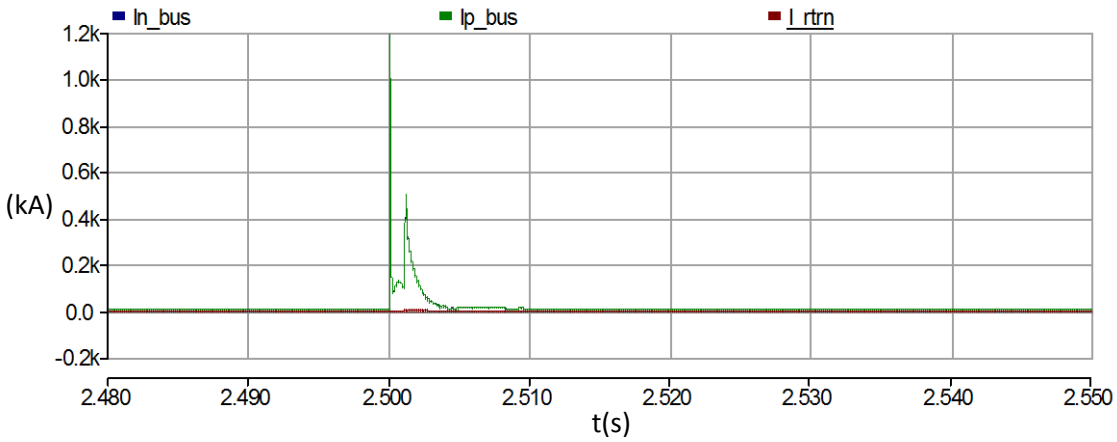

Figure 3-21 - Currents at B34 during a Pole-to-Pole Fault at Bus 3 end of the Line (In_bus - current on negative pole, Ip_bus – current on negative pole, and I_rtn – current on return conductor)

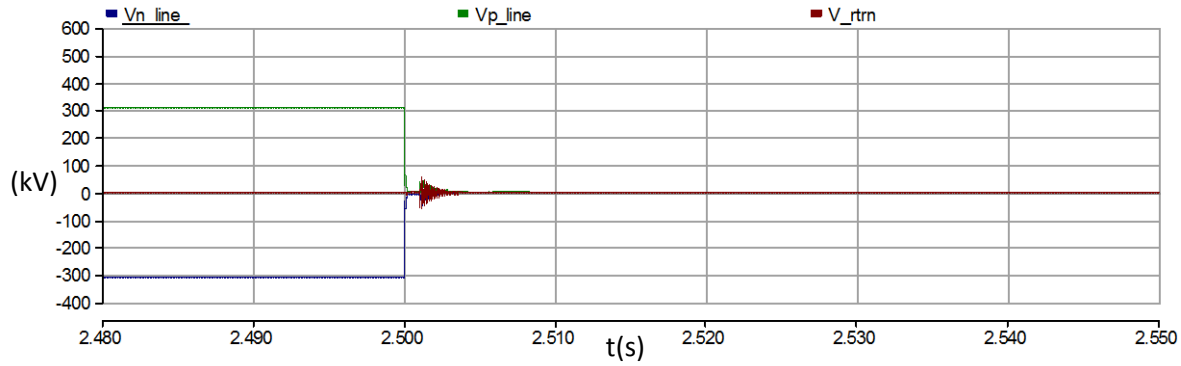

Figure 3-22 - Bus 3 Voltages during a Pole-to-Pole Fault at Bus 3 end of the Line (Vn_line – voltage of negative pole, Vp_line – voltage of positive pole, and V_rtn – voltage on return conductor)

In this case the steady state fault current path is from the AC system, through the converter and into the fault. The initial instantaneous surge in fault current is due to the discharge of the converter capacitance. The steady state fault current is difficult to see on the plot as it is dwarfed by the instantaneous fault current. The steady state current is current from the AC system feeding through the converter into the DC fault.

3.2.2 **Fault Currents and Voltages as Seen at Different Breakers**

Single pole-to-ground faults were simulated in several locations on the three converter test grid. The results for two of these fault locations (F1-50 and F3-50 are indicated on Figure 3-23) are shown in Figure 3-24 through Figure 3-27 and Table 3-1 through Table 3-4 .

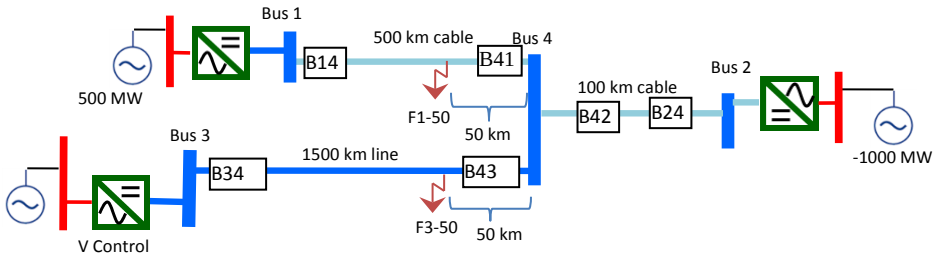

Figure 3-23 – Fault Locations for Plotted Currents

In these simulations, it was assumed that there are no series inductors to limit the initial rate of rise of fault currents.

Figure 3-24 and Figure 3-25 show the variations of the currents and voltages at all the breaker locations on the three converter test grid for a fault 50 km away from bus 4 on the cable connecting to bus 1. Propagation delays of the voltage and current surges and the effects of reflected traveling waves are visible on both current and voltage waveforms.

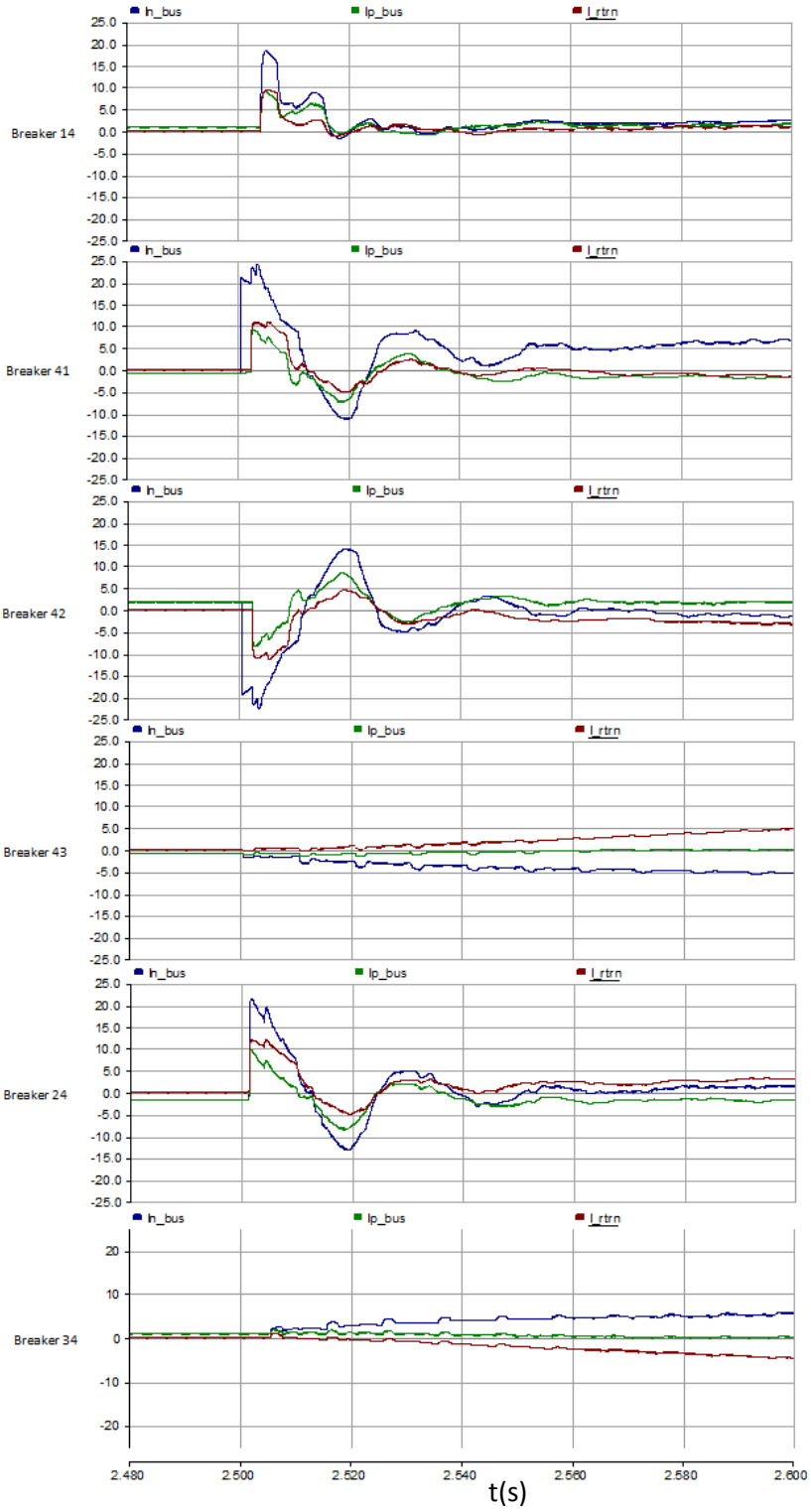

Figure 3-24 – Currents (kA) for Fault 50 km from Bus 4 on C1-4 with no Inductors

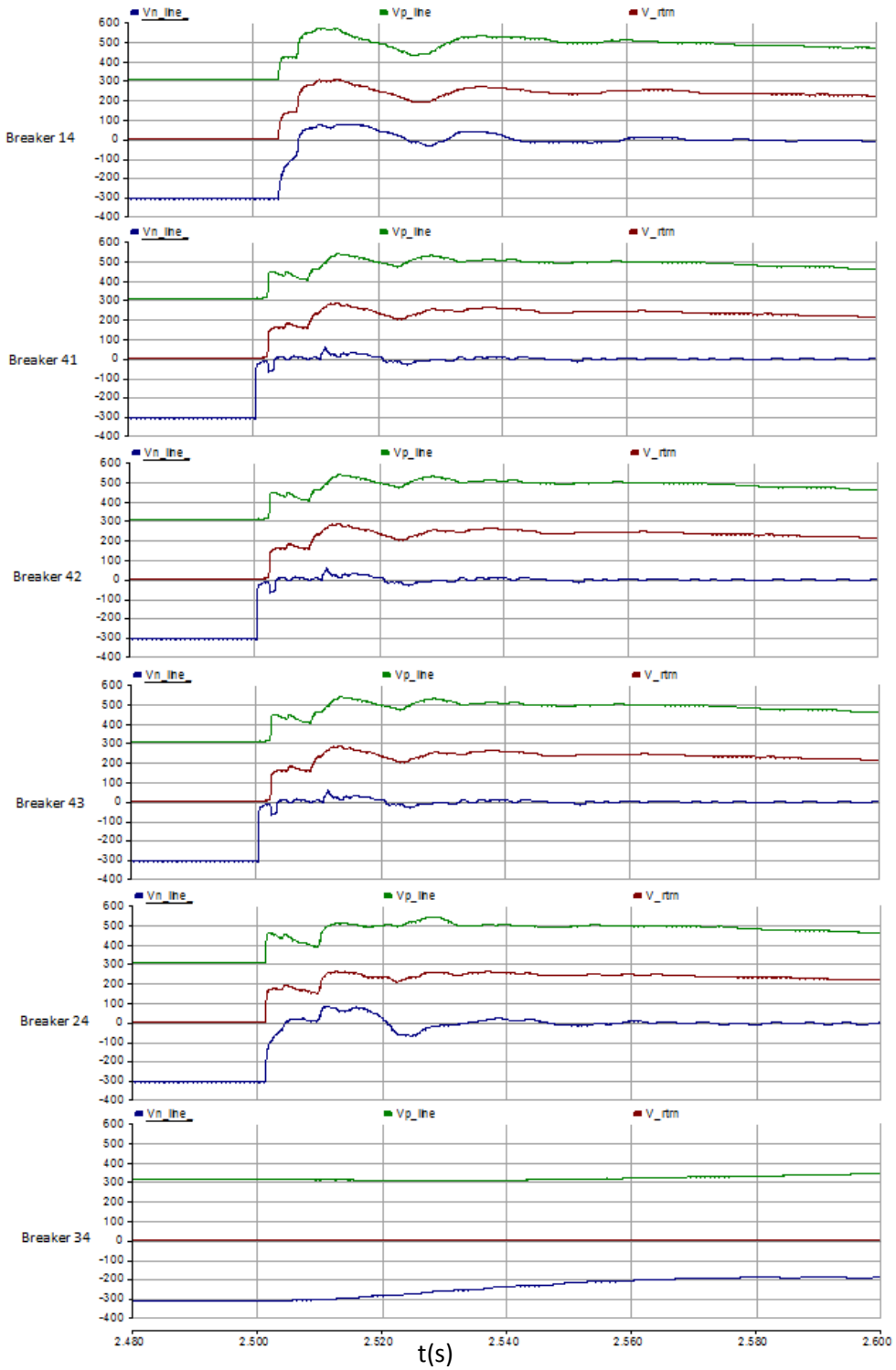

Figure 3-25 – Voltages (kV) for Fault 50 km from Bus 4 on C1-4 with no Inductors

The results from Figure 3-24 and Figure 3-25 are summarized in Table 3-1 and Table 3-2. Table 3-1 shows the maximum rate of change of voltage (ROCOV) observed at each of the six DC breaker locations on the three converter test grid.

Table 3-1 - ROCOV at Breaker Locations for a P-G *Fault on C1-4, 50 km from Bus 4*

Detection Location	Max ROCOV (kV/ms)
B14	522
B41	11700
B42	11689
B43	11694
B24	2589
B34	37

Table 3-2 presents the amount of time between the occurrence of the fault and the time when the fault current through the breaker exceeds 10 kA.

Table 3-2 - Time before Breaker Currents Exceed 10 kA for P-G Fault on C1-4, 50 km from Bus 4

Detection Location	Time from Fault to 10 kA (ms)
B14	4.26
B41	0.46
B42	0.46
B43	n/a
B24	1.39
B34	n/a

Figure 3-26 and Figure 3-27 show the currents and voltages respectively at the breaker locations on the three converter test grid for a fault 50 km away from bus 4 on the overhead line connecting to bus 3.

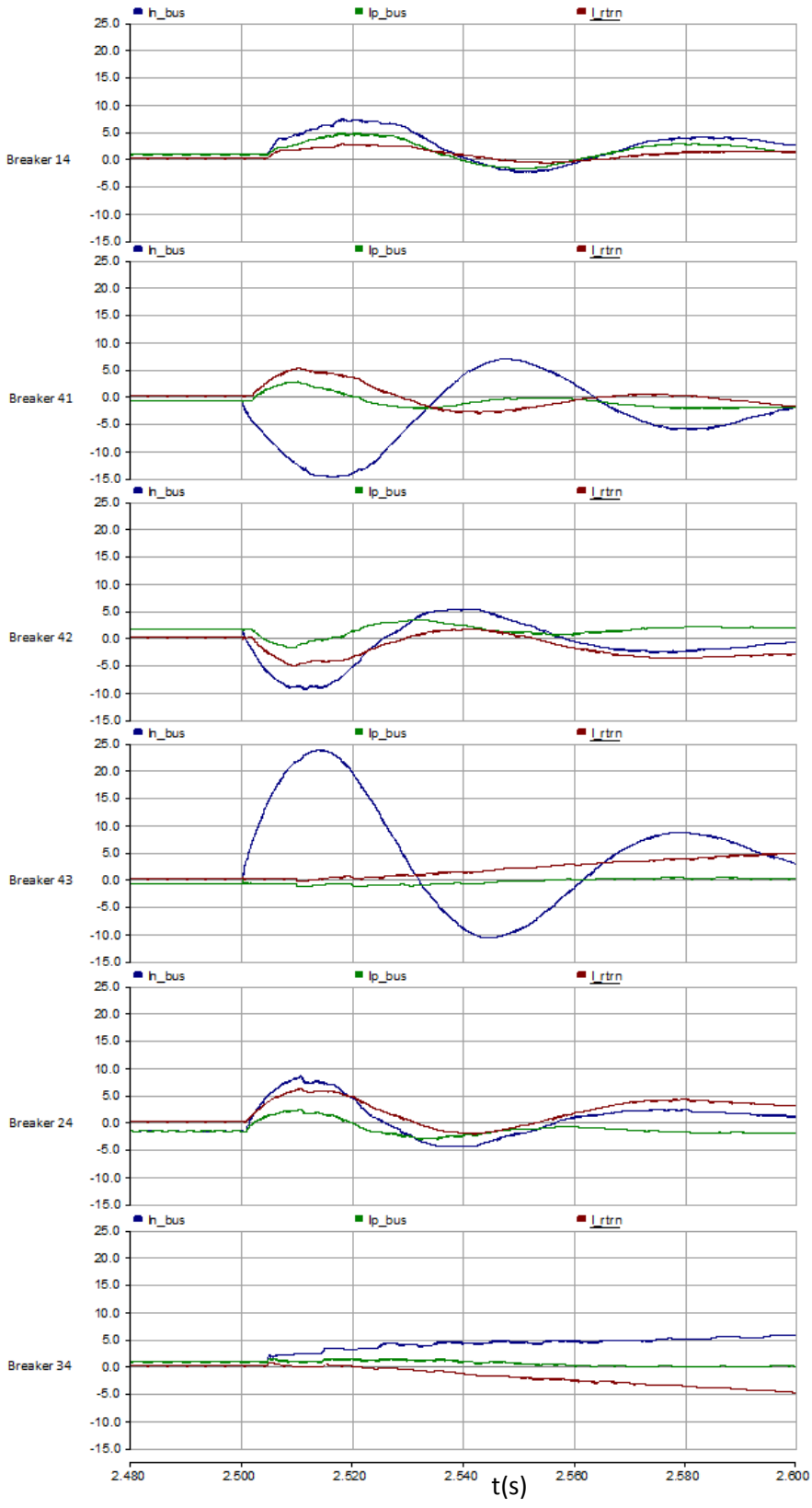

Figure 3-26 – Currents (kA) for Fault 50 km from Bus 4 on L3-4 with no Inductors

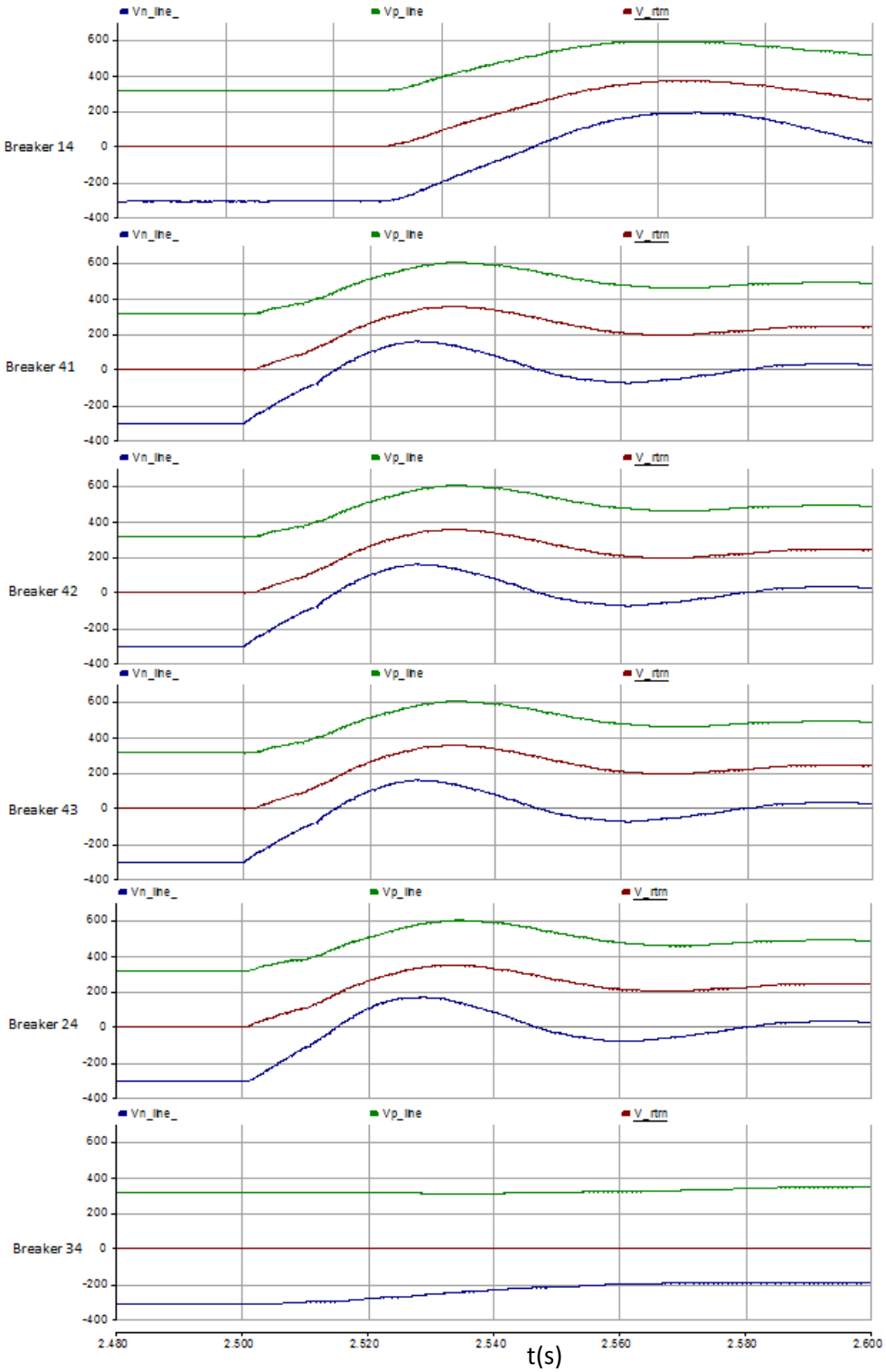

Figure 3-27 – Voltages (kV) for Fault 50 km from Bus 4 on L3-4 with no Inductors

The results from Figure 3-26 and Figure 3-27 are summarized in Table 3-3 and Table 3-4. Table 3-3 shows the maximum ROCOV observed at each of the six DC breaker locations on the three converter test grid. Table 3-4 gives the amount of time between the occurrence of the fault and the time when the fault current through the breaker exceeds 10 kA.

Table 3-3 - ROCOV at Breaker Locations for a P-G Fault on L3-4 50 km from Bus 4

Detection Location	Max ROCOV (kV/ms)
B14	74.45
B41	528
B42	528
B43	528.9
B24	140
B34	46

Table 3-4 - Time before Breaker Currents Exceed 10 kA for P-G Fault on L3-4 50 km from Bus 4

Detection Location	Time from Fault to 10 kA (ms)
B14	n/a
B41	6.98
B42	n/a
B43	3.08
B24	n/a
B34	n/a

Two protection challenges can be observed from the study results depicted in Figure 3-24 through Figure 3-27 and Table 3-1 through Table 3-4:

1. It is difficult to determine the segment that is faulted based on ROCOV alone.
2. The fault current can rise very quickly in the breakers at either end of the faulted segment.

The solutions for both of these protection challenges will be addressed in Section 4.1.

3.2.3 **Steady State Fault Currents**

An example of steady state fault currents can be seen in Figure 3-28. For a positive pole-to-ground fault at the midpoint of the cable from bus 1 to bus 3 on the nine converter test grid, the steady state currents on the faulted pole and the return conductors are shown on the SLD. The neutral metallic return conductors are grounded only at bus 9.

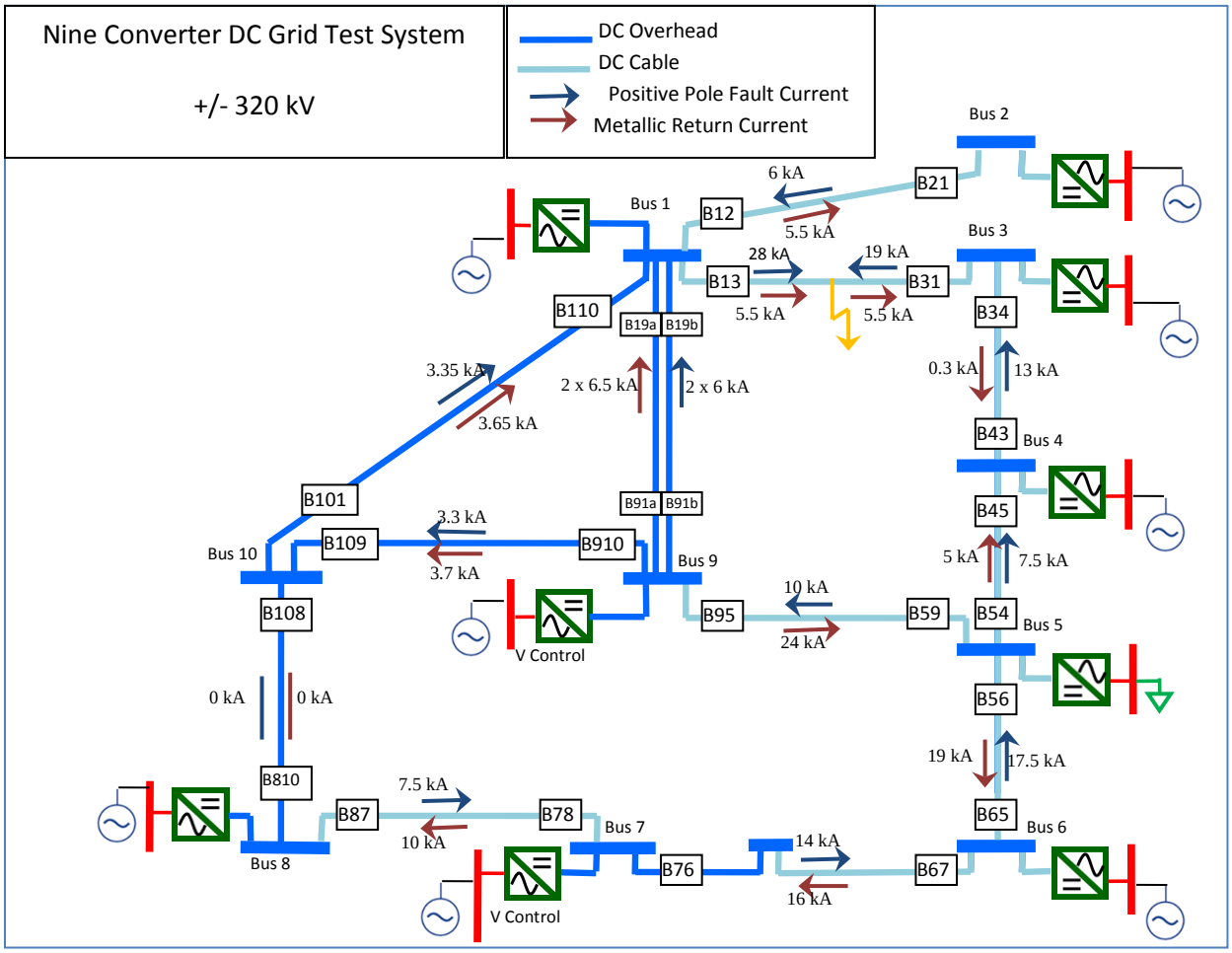

Figure 3-28 - Steady State Fault Current on Nine Converter Test Grid for a Positive Pole-to-Ground Fault on Cable 1-3

These results show that the steady state fault currents on the nine converter test grid are higher than the currents that can be interrupted with any of the proposed hybrid breaker solutions.

3.3 **Concluding Remarks**

This chapter described two of the test grid models that were modelled in PSCAD. Several fault scenarios were simulated and the results were used to gain an understanding of how faults affect voltages and currents in DC grids. Simulations showed that without series inductors to limit the rate of rise, fault current can potentially rise above the capability of currently proposed hybrid DC circuit breakers in a sub-millisecond time interval. In addition, the simulations showed that steady state fault currents are also beyond the capability of hybrid DC circuit breakers. These observations led to the proposed protection methods presented in Chapter 4.

4 Fault Detection

This chapter proposes a method for a breaker to quickly determine if there is a fault on the transmission segment that it is protecting and if it needs to trip. Next, the proposed concepts are tested through detailed simulation studies. Finally, a process for determining protection settings is discussed and the results of the process applied to the two test grids is documented.

4.1 Proposed Fault Detection System

Two main protection challenges were identified in Section 3.2, namely (i) fault detection and discrimination, and (ii) limiting the rise of fault currents to a level that DC breakers can interrupt. Both of these challenges can be addressed with properly sized di/dt limiting inductors in series with DC circuit breakers at the ends of each line segment.

Although line differential protection appears as a straightforward solution in terms of fault detection and discrimination, it is not possible to rely on protection schemes that would require communication from one end of the line to the other. Waiting for a fault transient propagating at a speed of 110 km/ms to reach the far end of the line and for a message to return (at a slightly faster speed) in order to determine if a fault is on the immediate line section, would add too much delay. The fault currents can rise to a level beyond the capacity of breakers within this time. Therefore, it is necessary for each breaker to be able to determine very quickly, using locally available measurements, whether the fault is on the segment of the line that it is protecting.

On the other hand, the fault current rise through any breakers that will operate also needs to be limited such that it is within the interruptible limits for the time needed to locate the fault and open the breaker. This can be achieved by connecting a properly sized di/dt limiting inductor in series with each DC circuit breaker. With the inductors in place, the steady state fault current would not be changed but the rate at which the fault current rises would be decreased. The inductors would need to be sized to limit the current to within interruptible levels within the time necessary for a breaker to operate.

Although overcurrent is a good indicator of a fault, waiting for the current to exceed a threshold

before signaling a trip, especially when it is necessary discriminate against the faults in the next line segment, adds a significant delay. The DC breakers may not be able to tolerate such a delay. Another option is to use the rate of change of current (ROCOC) seen by the breaker. Because each breaker is likely to have an inductor in series with it to limit the rate of rise of fault current, ROCOC is given by

$$\frac{di(t)}{dt} = \frac{v_{bus}(t) - v_{line}(t)}{L} \qquad (1)$$

where L is the inductance of the di/dt limiting inductor and v_{bus} and v_{line} are the voltages on the bus and line side of the inductor. The voltage on the bus side of a di/dt limiting inductor, v_{bus}, remains relatively constant for the first millisecond after the fault transient arrives at the breaker. As a result, the ROCOC seen by the breaker is in fact approximately proportional to the voltage change on the line side of the inductor and would be of no more use in determining fault location than the line side voltage measurement itself.

Figure 4-1 shows an example fault detection scenario. Assuming that we have fast breakers at either end of the line from bus 1 to bus 2, a fault F1 on that line segment should result in breakers B1 and B2 opening to isolate the faulted element. A fault F2 on the next segment should result in neither B1 nor B2 tripping. The breakers B1 and B2 need to be able to quickly identify the location of the fault. For breaker B2 the direction of the fault current could be used to determine if the fault is at F1 or F2 but for breaker B1 the fault current would be in the same direction for either fault.

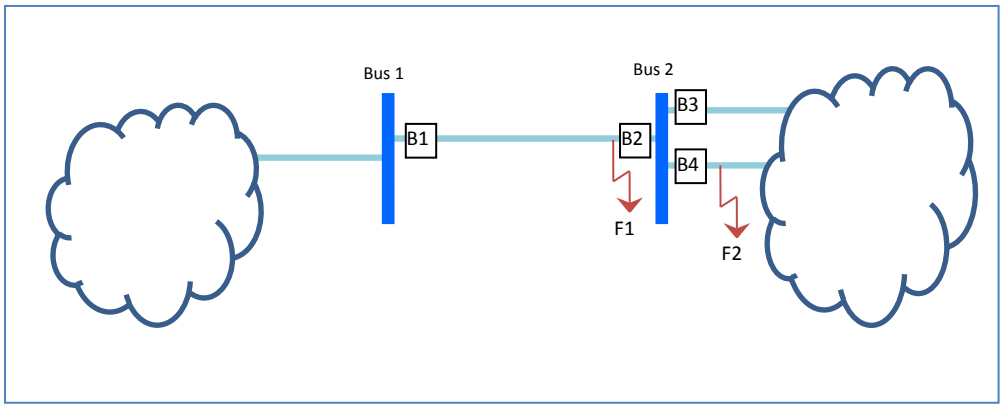

Figure 4-1 - Fault Detection Scenario

The new DC line protection scheme proposed in this thesis is based on the rate of change of voltage (ROCOV), and relies on the existence of di/dt limiting inductor. Consider Figure 4-2, which shows an HVDC grid with di/dt limiting inductors at either end of the each line segment. In this case, the ROCOV on the line side of the inductor can be measured and used to detect a fault and determine the location of the fault.

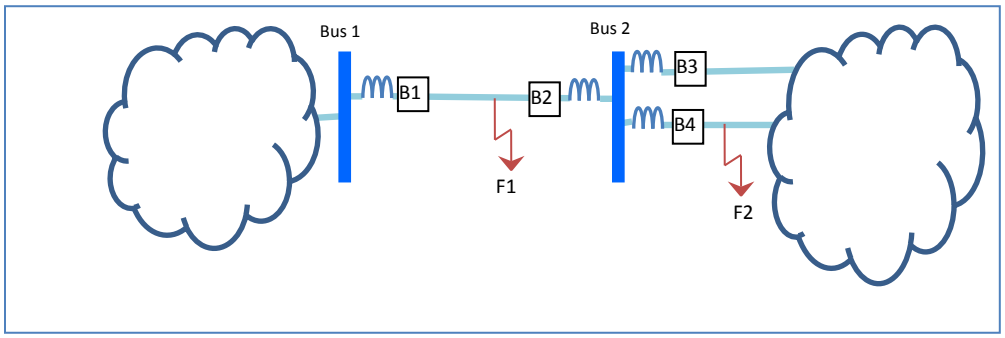

Figure 4-2 – DC Grid with di/dt Limiting Inductors

Consider fault F2 in Figure 4-2. The fault-generated voltage traveling wave arriving at breaker B4 is mostly reflected by the inductor in series with B4, essentially blocking its propagation beyond the inductor. Therefore, while the voltage at B4 is subjected to a rapid change due to the voltage wave, the voltages at bus 2, and breakers B2, B3, and B1, would be more or less isolated from this steep voltage change during the initial transient period. Thus for fault F2, the ROCOV measured at B1 will be much smaller than that measured at B4. This property can be used to discriminate the faults. For example, fault F1 in Figure 4-2 will result in a much larger ROCOV at B1, as the voltage traveling wave arising from the fault travels unimpeded to B1. Using this principle with properly selected thresholds, a breaker can determine, using local ROCOV measurements, whether a fault is within its protected zone or not. For example, a fault on the line segment from bus 1 to bus 2 would be identified and cleared by breakers B1 and B2 as shown in Figure 4-3 with no need for communications.

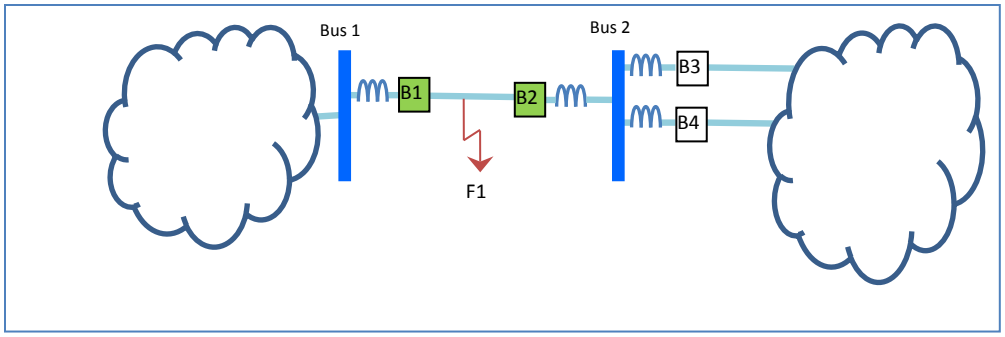

Figure 4-3 - Fault F1 Clearing Scenario

The fault current paths for a single pole-to-ground fault in a bi-pole grid with a neutral metallic return grounded at only one point and di/dt limiting inductors are shown in Figure 4-4. As mentioned earlier, the series inductors do not significantly alter the steady state fault currents but reduce their initial rates of rise. Additionally, the inductors facilitate ROCOV based fault discrimination.

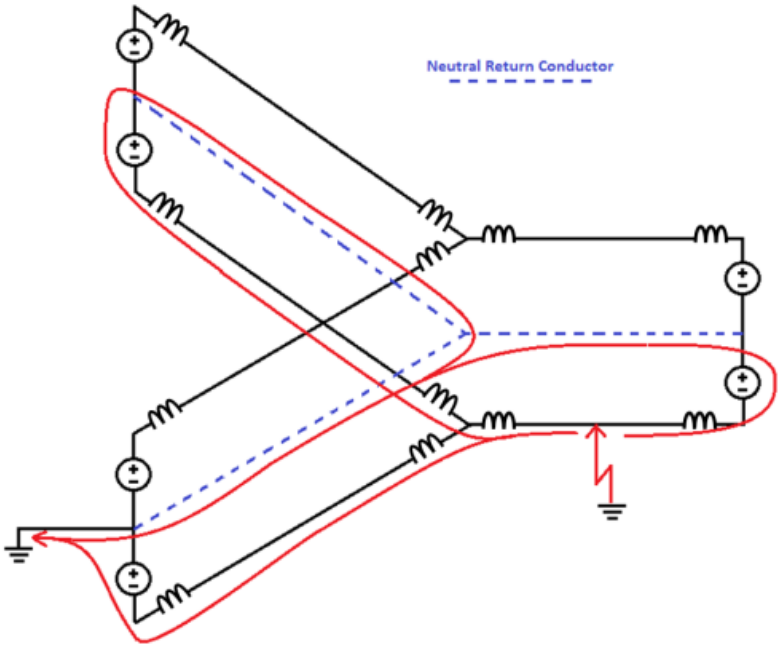

Figure 4-4 - Steady State Fault Current Path in Grounded Bi-Pole Grid with di/dt Limiting Inductors

The relationship between inductor size and ROCOV based fault discrimination will be explored further in Section 4.2. Protection threshold setting studies are discussed in Section 4.3. In Chapter 5 the di/dt limiting effect of the inductors is discussed.

4.1.1 **Zonal Protection**

It is not necessary to put breakers and inductors on each end of every line segment. A grid can be divided into zones of protection with inductors and breakers on the connection points between those zones. Figure 4-5 shows an example of a meshed grid that could be divided into four zones. A fault in any one of the zones would result in a high ROCOV within that zone and would be detected by the breakers on the boundaries. These would then open and effectively isolate the faulted zone from the rest of the grid.

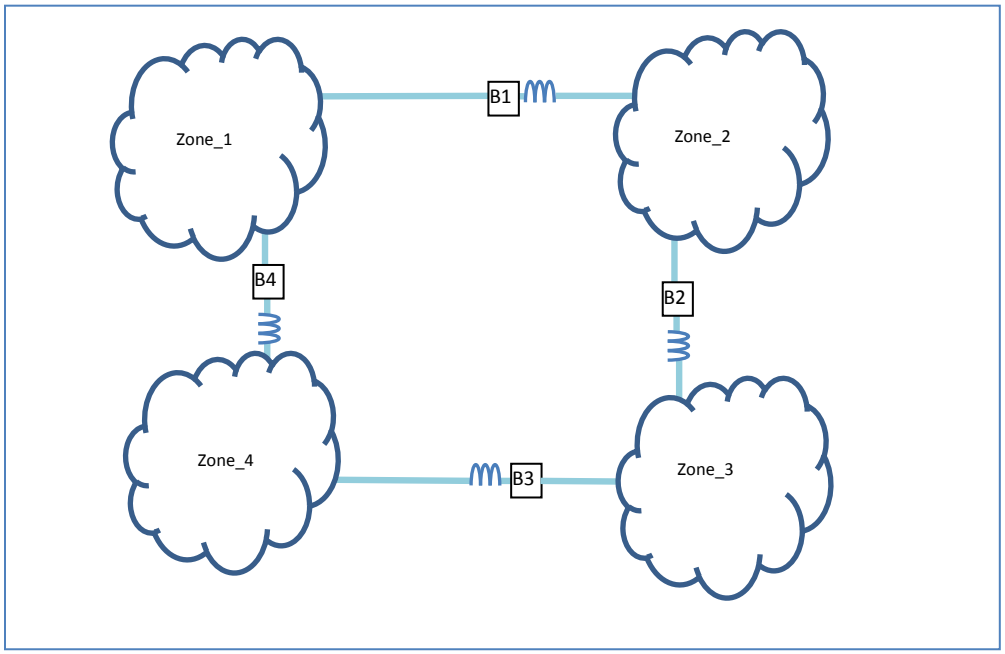

Figure 4-5 - Zonal Protection Scheme

If a protection zone includes an AC/DC converter which is not separated from the rest of the zone with a di/dt limiting inductor, it may be possible to experience 2 pu voltages on the non-faulted pole if the grounding point for the entire grid is far away from the faulted zone. This should be considered when implementing a zonal protection scheme.

Zonal protection was not simulated in the course of this thesis but is a good topic for further study.

4.1.2 Protection Backups

This section describes several protection failure scenarios and proposed backup solutions for these scenarios.

4.1.2.1 Breaker Fail Scenarios

In the event of a failed breaker (as shown in Figure 4-6) from a fault on the line segment from bus 1 to bus 2, the breaker B2 would detect that it had failed and signal the other breakers at the bus to trip. This would result in the loss of two additional line segments.

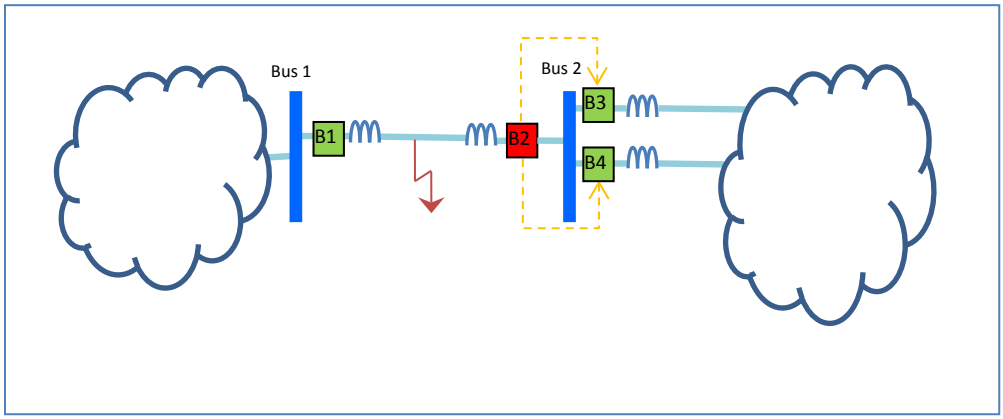

Figure 4-6 - Breaker Fail Scenario

The critical factor in this scenario is having enough time for the backup breakers to operate before the fault current exceeds the interruptible limits. One way to ensure that breakers B3 and B4 are ready to operate quickly would be to, upon detection of a fault for which B2 should operate, trigger all of the breakers at that bus to open their small solid state components and their mechanical switches. This way if B2 detects that it has failed, all B3 and B4 need to do is trigger their large solid state components which can be done very quickly. If B2 operated correctly and no B3 or B4 trip was required, the mechanical switches and small solid state breakers of B3 and B4 could simply be reclosed.

Similarly for a failed breaker during a bus fault, as shown in Figure 4-7, a signal could be sent from B2 to B1 upon detection of the fault initiating the first two steps in opening the hybrid DC breaker. Upon detection of a failed breaker opening at B2, another signal could be sent to B1 instructing it to operate.

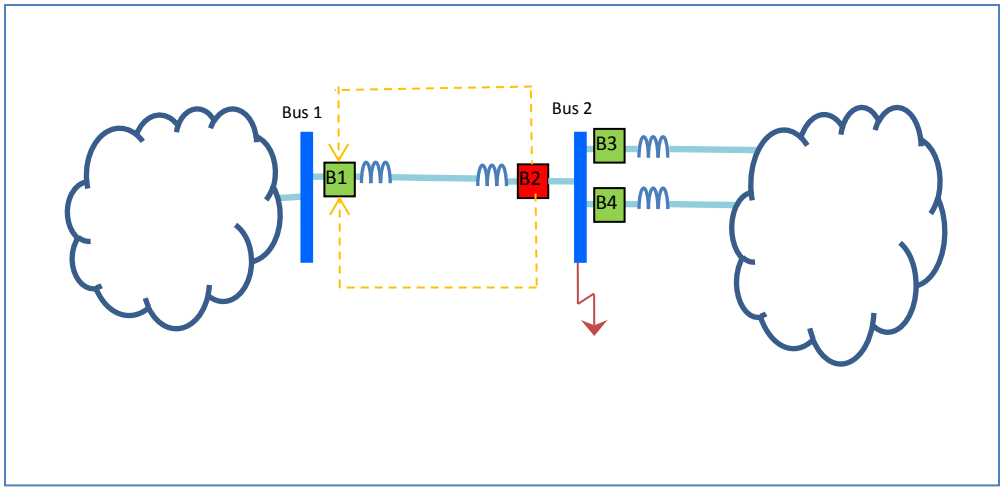

Figure 4-7 - Bus Fault Breaker Fail Scenario

The largest downside with this breaker fail backup is that it relies on communications. Communications add delays which must be managed as well as additional points of potential failure which impact reliability.

In the event of a breaker failure, if the backup communication based protection systems fail then the AC side breakers can be opened. This will block the fault current at the cost of some or all of the AC/DC converters in the grid.

4.1.2.2 Fault Detection Backup

As a backup for fast fault detection, when B1 or B2 detects a fault on the line segment from bus 1 to bus 2 using ROCOV, a message could immediately be transmitted to the breaker at the other end of the line segment with a command to trip, as depicted in Figure 4-8. This may be useful for really long lines where a fault at one end may be difficult to detect at the other end. However, it would not be adequate for missed close-in faults for the same reason that differential protection for long lines is not feasible. The time necessary for the fault current wave to travel all the way to the opposite end and for the communicated message to travel all the way back, would be too long.

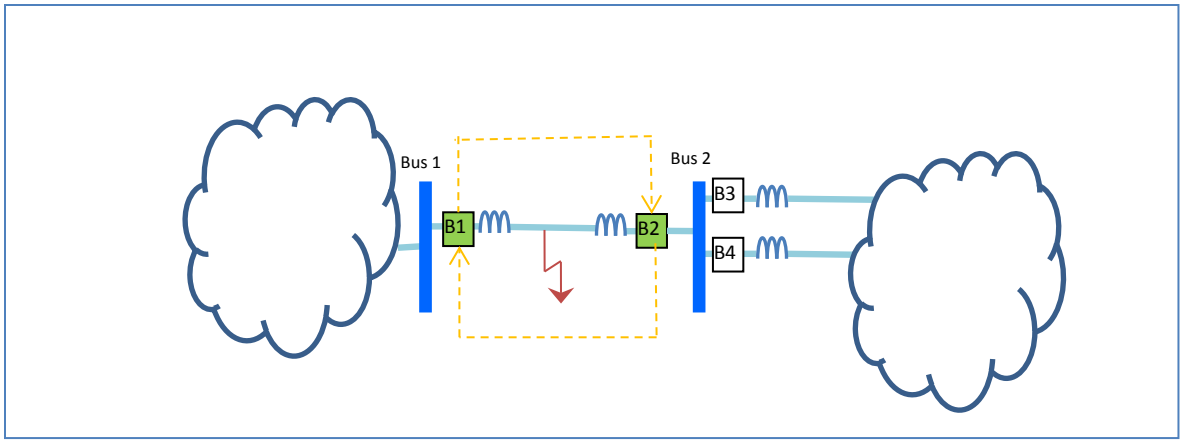

Figure 4-8 - Fault Detection Backup

As an additional prevention of unnecessary nuisance trips during faults, once a breaker has determined that there is a fault on the segment that it is protecting and that it should trip, it could send a communication to the other breakers on the same bus and the breakers one line segment away informing them of the trip and warning them not to trip during the expected transient from the fault and the subsequent tripping of the breaker. In Figure 4-9, once B4 signals a trip it instructs B1, B2 and B3 that there will be a transient and that they should not trip.

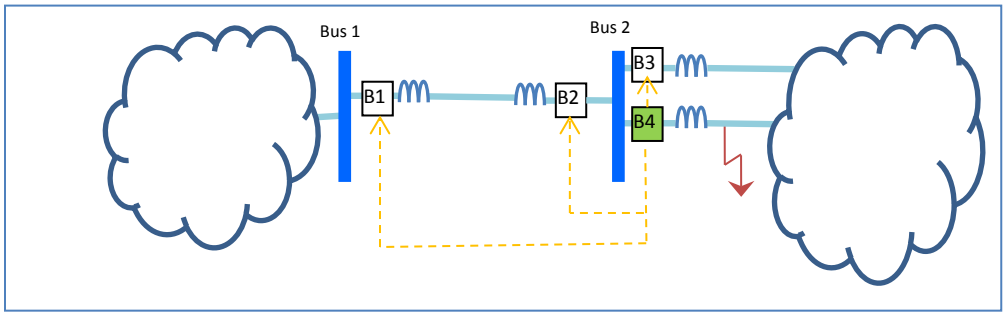

Figure 4-9 - Blocking Signals

The transient should not, of course, be enough to cause a trip if the primary protection settings are properly set. This is a precaution.

4.1.2.3 High Impedance Faults

High impedance faults (as shown in Figure 4-10) may result in a lower ROCOV on the faulted line segment and be difficult to identify. Differential protection schemes can be used to identify

these faults with both ends of the line communicating the observed currents to the other. Less speed may be required as the high impedance of the fault will result in a slower rise in fault current. Further study could be done to confirm that faults with impedances high enough such that the normal ROCOV method doesn't detect them can be tolerated for the time necessary for a differential current based method to detect them.

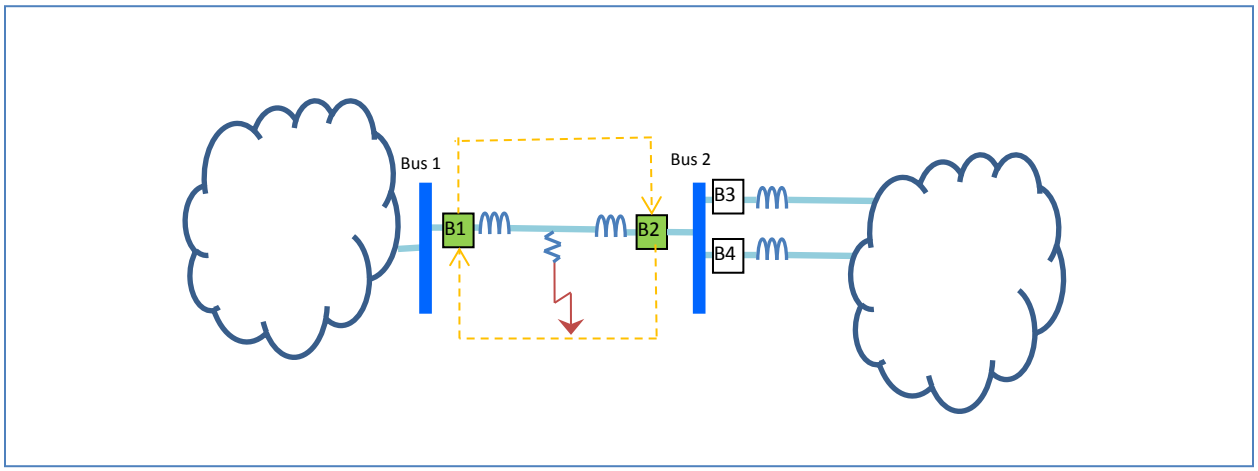

Figure 4-10 - High Impedance Faults

4.1.3 Detection of Faults on Neutral Metallic Return

Ground faults on the metallic return may be detected by perturbing the neutral point voltage at a converter, such that a voltage is induced on the metallic return line at that point, then measuring the current on the metallic return throughout the grid. If the metallic return is connected to ground at more than the one designated point, this will be detected when the current measurements are analyzed by the central controller. This was not simulated as part of this thesis.

4.2 Fault Detection Studies

The three converter test grid with di/dt limiting inductors and some studied fault locations added is depicted in Figure 4-11.

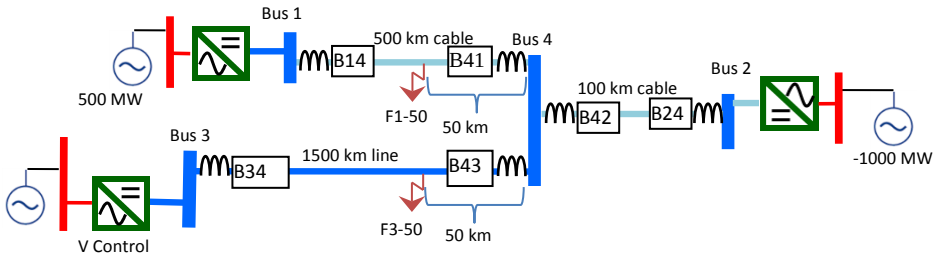

Figure 4-11 - Three Converter Test System with di/dt Limiting Inductors

4.2.1 Line Fault Detection using ROCOV

Figure 4-12 depicts a fault 50 km away from bus 4 on the cable to bus 1 (fault F1-50 in Figure 4-11) of the three converter test grid as seen at breaker B14. All inductors were sized at 100 mH.

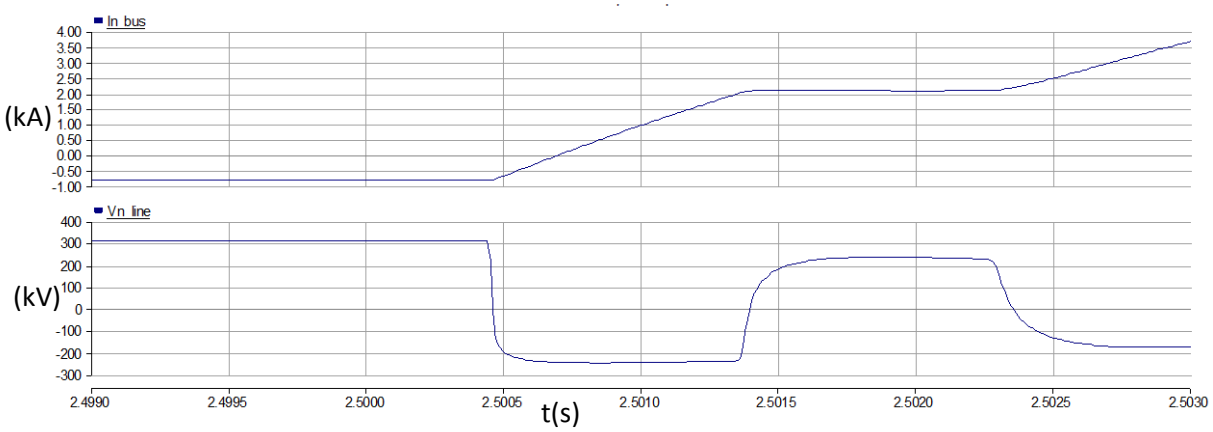

Figure 4-12 – Current and Voltage at B14 for a Fault 50 km from Bus 4 on Cable C1-4

In Figure 4-12, it can be seen that the voltage is subjected to sharp drop compared to the current that rises after the fault. Thus the measured ROCOV would detect this fault much faster than the current or rate of change of current. Approximately a millisecond after the fault, the voltage drops significantly, but the current has only risen to 1 kA, which is still within the acceptable current limits. Although the ROCOC could be used to detect the fault, it would be slower than the use of ROCOV. The current through the protection inductor is the integral of the voltage across the inductor. The derivative of the current (ROCOC) is proportional to the voltage across the inductor. But ROCOV is proportional to the derivative of this voltage. When

the line segment is bounded by protection inductors, ROCOV can not only detect the faults faster than other indicators but also discriminate against the faults in remote lines.

This section will document select cases from three sets of studies that were performed. Section 4.2.1.1 documents studies in which two different faults were simulated with two different inductor values. The measured voltages at each of the breakers on the three converter test grid are plotted and tabulated. Section 4.2.1.2 shows results for individual breakers where the voltages for faults at different locations are plotted. Section 4.2.1.3 plots the measured voltages when the size of the di/dt limiting inductor is varied.

4.2.1.1 Preliminary Studies with di/dt Limiting Inductors

Figure 4-13 through Figure 4-16 and Table 4-1 and Table 4-2 show some of the results of fault studies using the three converter test grid with the inductors added in series with all of the breakers. The post-fault voltages at the line side of each breaker location are plotted and the maximum ROCOV at each point is tabulated.

Figure 4-13 and Figure 4-14 show plots of the voltages at each breaker for a pole-to-ground fault 50 km away from bus 4 on the cable connecting to bus 1 (fault F1-50 in Figure 4-11) with 50 mH and 100 mH inductors respectively.

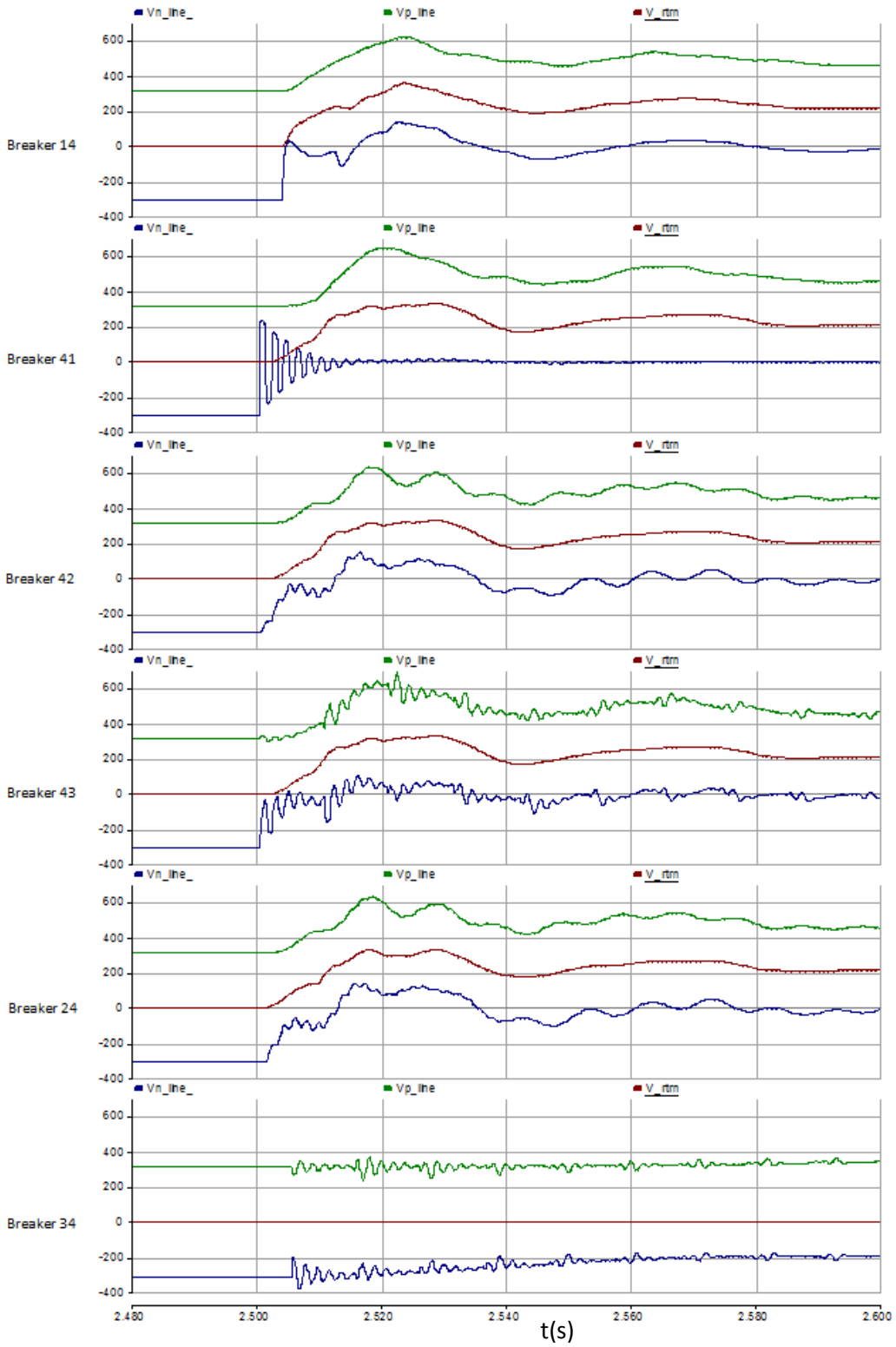

Figure 4-13 – Voltages (kV) for a Fault 50 km from Bus 4 on the Cable to Bus 1 with 50 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

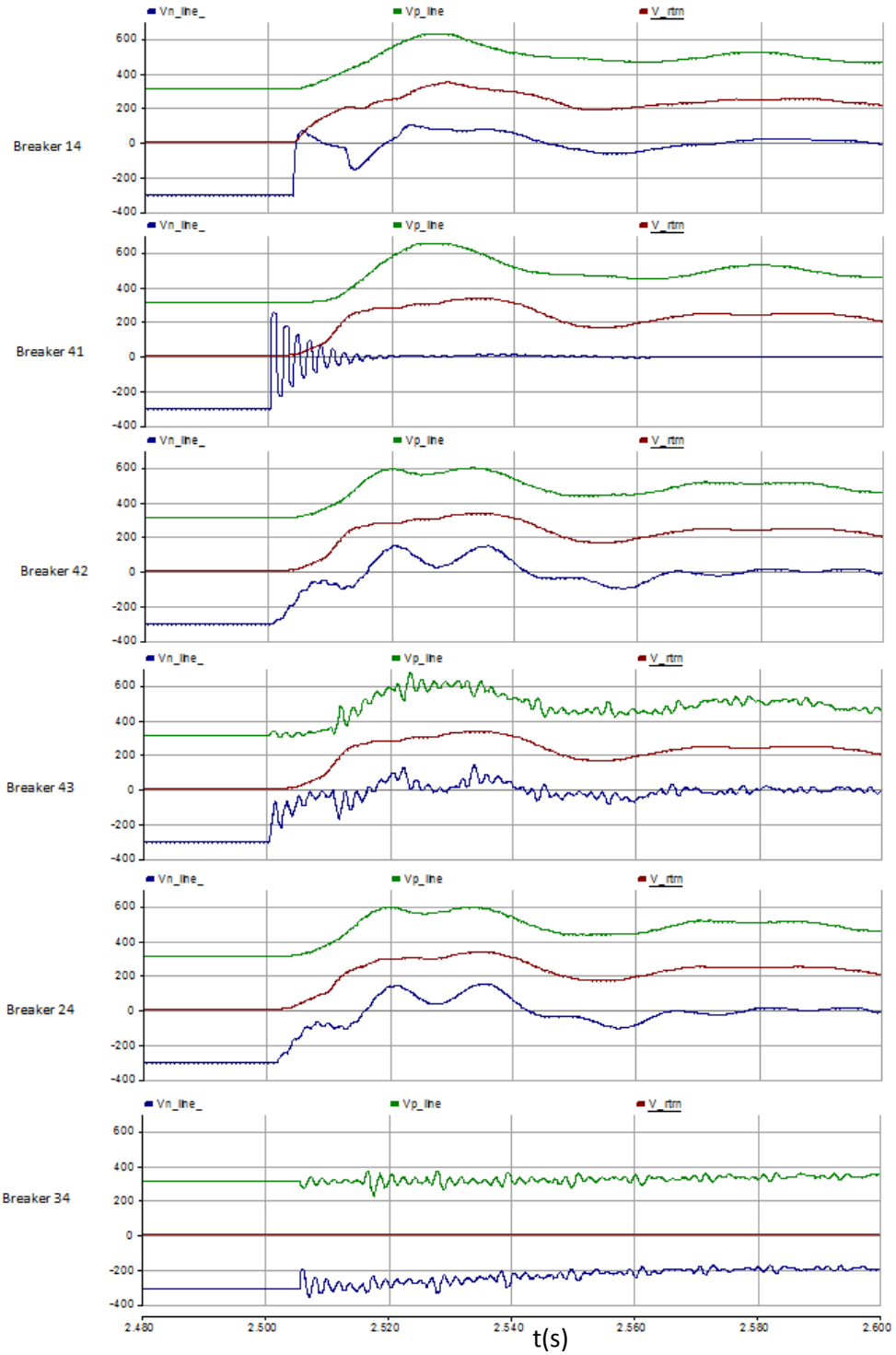

Figure 4-14 – Voltages (kV) for Fault 50 km from Bus 4 on the Cable to Bus 1 with 100 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

The results plotted in Figure 4-13 and Figure 4-14 are summarized in Table 4-1. The maximum rate of change of voltage (ROCOV) seen at each breaker on the line side of the inductor are plotted for cases with 50 mH inductors, 100 mH inductors and no inductors. The column with no inductors corresponds to the results in Figure 3-25 and Table 3-1 in Section 3.2.2.

Table 4-1 - ROCOV for Fault 50 km from Bus 4 on the Cable to Bus 1

Detection Location	No Protection Inductors	50 mH Protection Inductors at all Breakers	100 mH Protection Inductors at all Breakers
	Max ROCOV (kV/ms)		
B14	522	1504	1511
B41	11700	23872	23872
B42	11689	132	81
B43	11694	850	459
B24	2589	130	79.8
B34	37	701.95	458

It can be seen from this data that, when di/dt limiting inductors are modeled, the breakers at the ends of the faulted segment see a significantly higher ROCOV than breakers that are separated from the fault by one or more inductors.

Figure 4-15 and Figure 4-16 show plots of the voltages at each breaker for a fault 50 km from bus 4 on the line to bus 3 (fault F3-50 in Figure 4-11) with 50 mH and 100 mH inductors respectively.

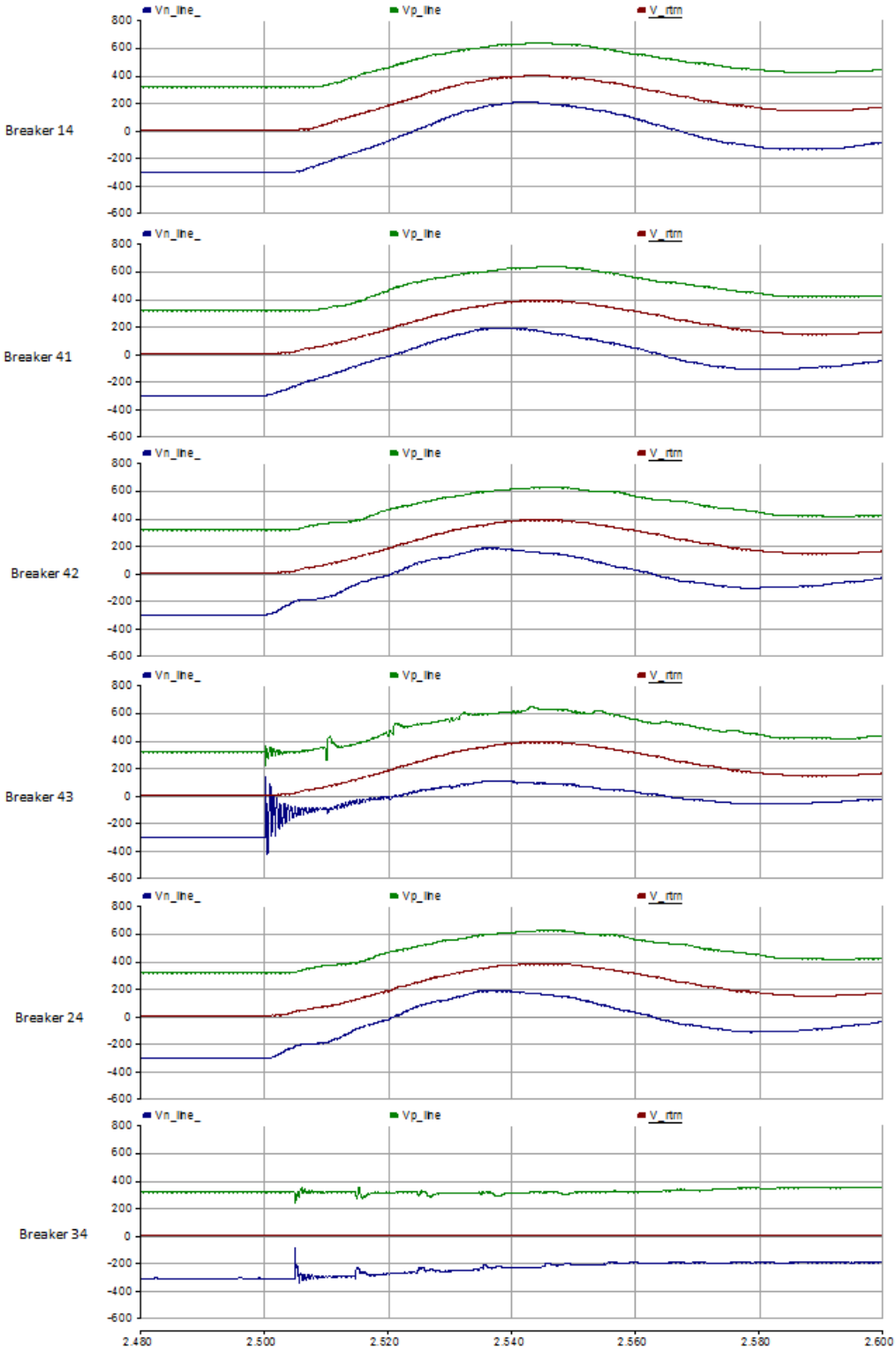

Figure 4-15 – Voltages (kV) for Fault 50 km from Bus 4 on the Line to Bus 3 with 50 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

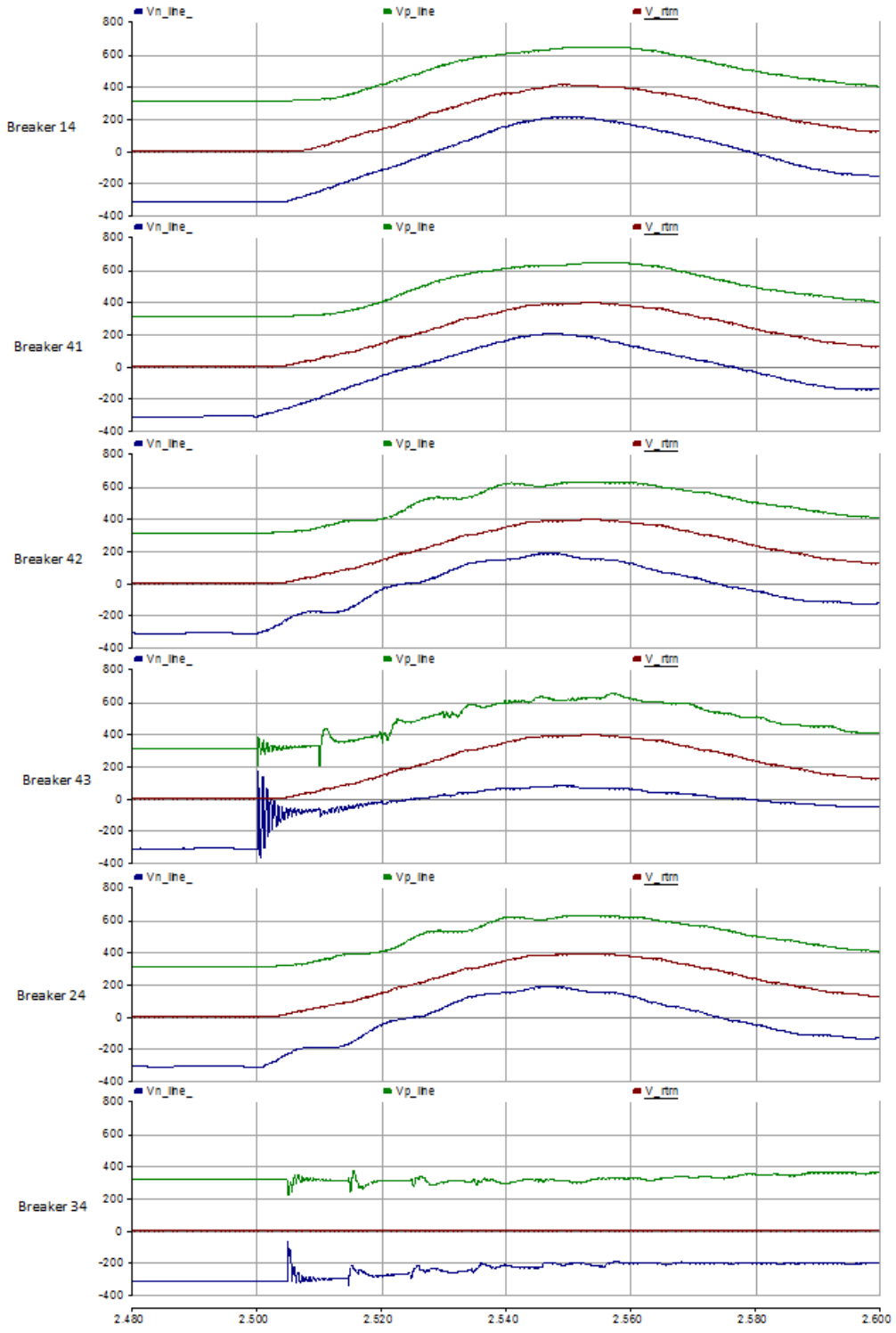

Figure 4-16 – Voltages (kV) for Fault 50 km from Bus 4 on the Line to Bus 3 with 100 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

The results plotted in Figure 4-15 and Figure 4-16 are summarized in Table 4-2. The maximum

rate of change of voltage (ROCOV) seen at each breaker on the line side of the inductor is listed for cases with 50 mH inductors, 100 mH inductors and no inductors. The column with no inductors corresponds to the results in Figure 3-27 and Table 3-3 in Section 3.2.2.

Table 4-2 - ROCOV for Fault 50 km from Bus 4 on the Line to Bus 3

Detection Location	No Protection Inductors	50 mH Protection Inductors at all Breakers	100 mH Protection Inductors at all Breakers
	Max ROCOV (kV/ms)		
B14	74.45	22	15.38
B41	528	37	20.25
B42	528	59.55	39.9
B43	528.9	22225	22611
B24	140	56.55	39.83
B34	46	3061	3374

It can be seen again that, when di/dt limiting inductors are modeled, the breakers at the ends of the faulted segment see a significantly higher ROCOV than breakers that are separated from the fault by one or more inductors.

4.2.1.2 ROCOV for Different Fault Locations

The solution proposed and studied in this thesis is to use the measured rate of change of voltage (ROCOV) at the line side of the di/dt limiting inductor to both detect and locate the faults. The rationale of the protection scheme can be explained considering the four DC grid faults F1, F2, F3 and F4 on the three converter test grid shown in Figure 4-17. All line/cable sections are provided with DC breakers (and associated di/dt limiting inductors of 100 mH) at both ends so that each segment can be isolated if a fault happens in the segment.

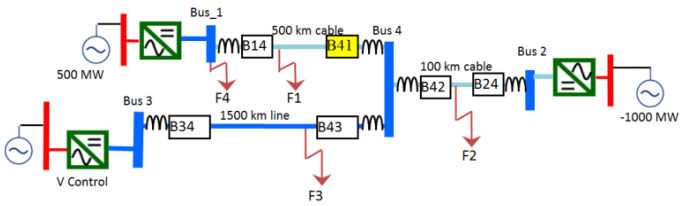

Figure 4-17 - Fault Detection Scenarios

Consider the voltage measurement taken at line side of breaker B41 for different pole-to-ground faults, shown in Figure 4-18. All faults are initiated at t = 2.5 s. The first seven plots are for fault F1, with each plot corresponding to a different fault location on cable C1-4 (0 km, 100 km, 200 km, 300 km, 400 km and 500 km from Bus 4). It can be observed for these faults that the slope (ROCOV) of the voltage wave front is quite steep even up to 500 km down cable C1-4.

The eighth plot in Figure 4-18 is the line side voltage measured at B41 for fault F4, a pole-to-ground fault at Bus 1. This is a remote bus fault. This fault is separated from the fault at 500 km down the line by one di/dt limiting inductor. The last two plots are voltages measured at B41 (line side) for fault F2 on cable C1-2 and fault F3 on line L3-4, at locations very close to Bus 4. However, faults F2 and F3 are each separated from breaker B41 by two di/dt limiting inductors. These series inductors act as a low pass filter and smooth out the voltage transient that is seen by B41 for faults F2, F3 and F4. Thus the faults across the inductor from B41, on L3-4 and C2-4, and faults at the far end of the line across an inductor, produce a much more gradual voltage change as seen on the line side of B41.

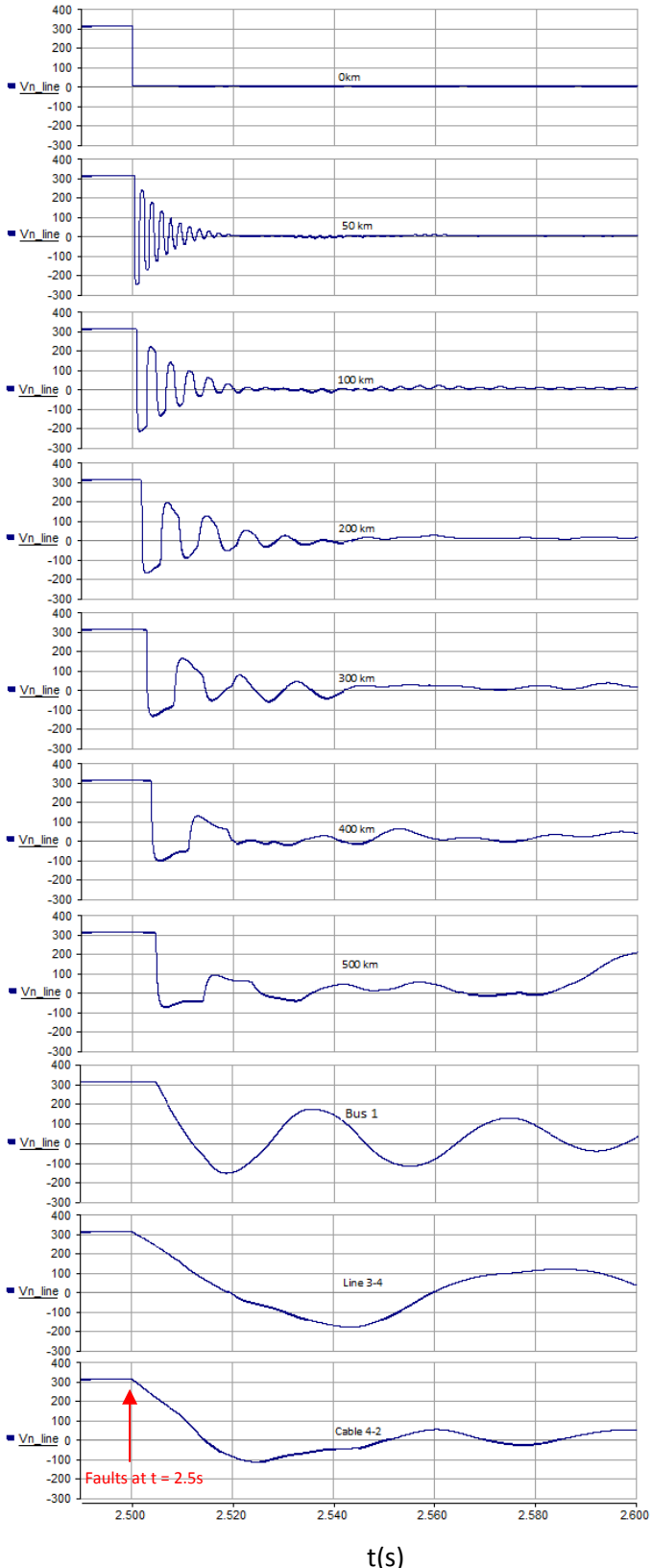

Figure 4-18 – Voltages (kV) at B41 for Different Fault Locations, Faults occur at Time = 2.5 seconds

Thus the change in ROCOV (from almost zero at steady state) can be used to detect the occurrence of a fault. The difference in ROCOV magnitudes can be used to differentiate the faults on the protected line from the faults on adjacent lines or bus faults. It can be seen that the ROCOV does decrease as the fault moves farther away from the measurement point. The maximum ROCOV observed for each fault scenario is tabulated in Table 4-3.

Table 4-3 - Maximum ROCOV at B41 for Different Fault Locations with 100 mH Inductors

Fault Location		ROCOV (kV/ms)
Cable 1-4	Distance from Bus 4 (km)	
	0	30651
	50	23874
	100	12603
	200	5490
	300	3017
	400	1872
	500	1264
Cable 2-4	0	31.85
Line 3-4	0	22.25

In PSCAD simulations, these ROCOV values were calculated by taking the differential of the measured voltage and scaling it to kV/ms.

When these values are plotted logarithmically (see Figure 4-19), it can be seen that there is still considerable margin between the ROCOV values observed for faults in the protected zone and those observed for faults on the adjacent zones.

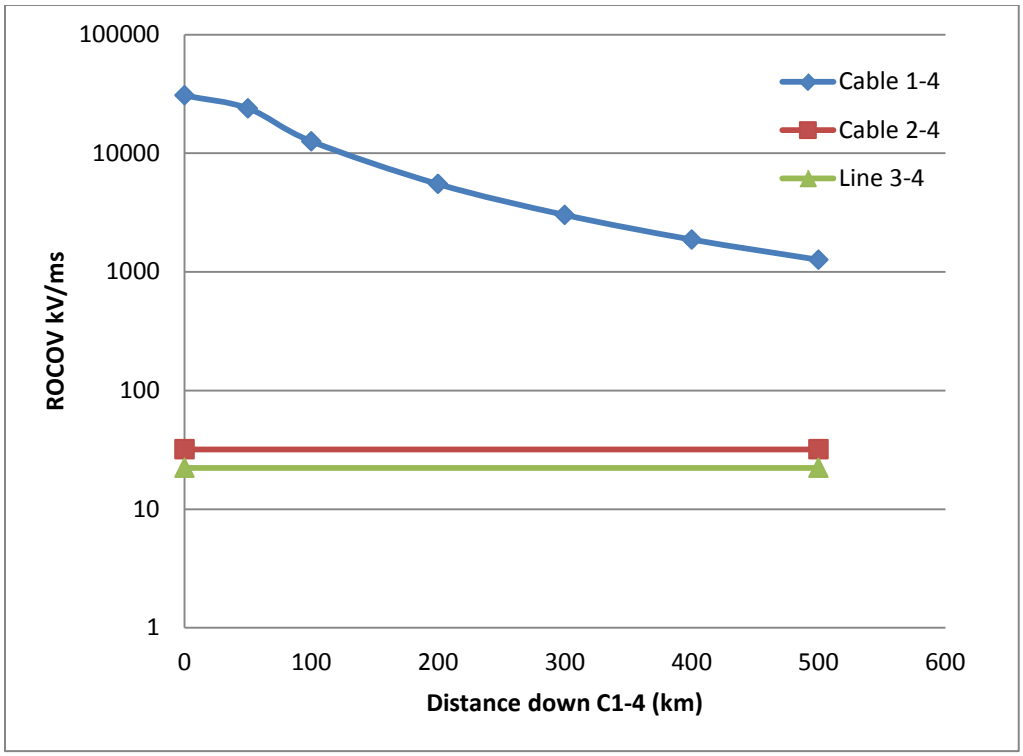

Figure 4-19 - ROCOV at B41 for Faults Down C1-4 towards Bus 1 and for Faults across the Inductors on C2-4 and on L3-4

Similarly, the line side voltages at B43 for faults at different distances along L3-4 and on adjacent line segments at bus 4 can be seen in Figure 4-20 (divided across two pages). ROCOV values observed at breaker B43 are shown in Figure 4-20, Table 4-4, and Figure 4-21. In this case the protected zone is an overhead line (L3-4) and therefore attenuation of ROCOV is smaller even for lengths of up to 1500 km. The ROCOV observed for faults not on the segment protected by B43 (F1 and F2) are higher compared to corresponding values observed at B41, due to the lower capacitance of the overhead line. However, for the distances studied, there is still enough margin between the ROCOV from the faults on the protected segment L3-4 and the faults on the other segments to differentiate between them. This demonstrates the concept that with di/dt limiting inductors in place effectively delineating each protection zone, it is relatively easy for a relay measuring ROCOV to determine if the fault is on the protected zone or in a remote zone.

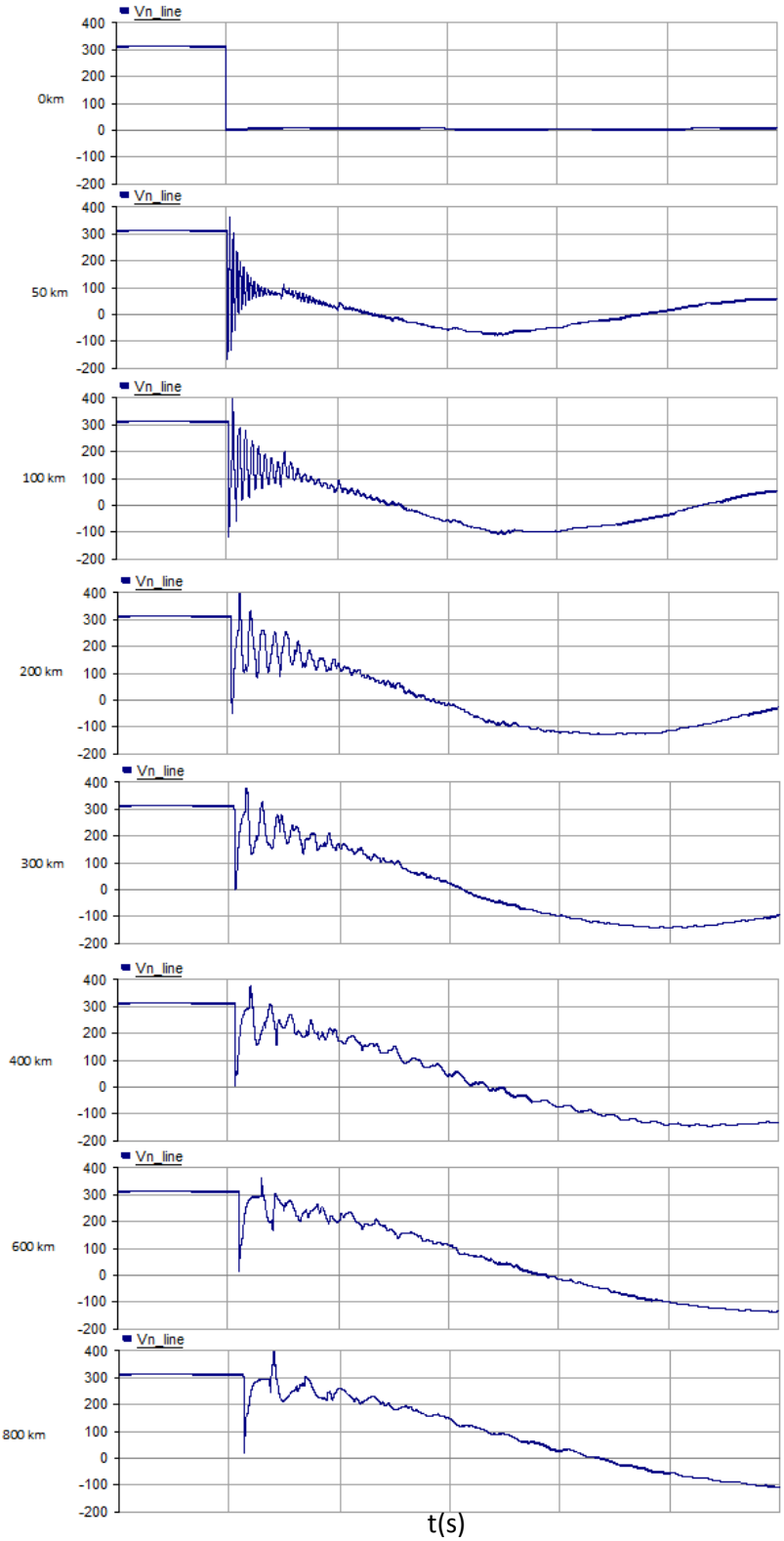

Figure 4-20 – Voltages (kV) at B43 for Different Fault Locations, Faults occur at Time = 2.5 seconds (Figure continues into the next page)

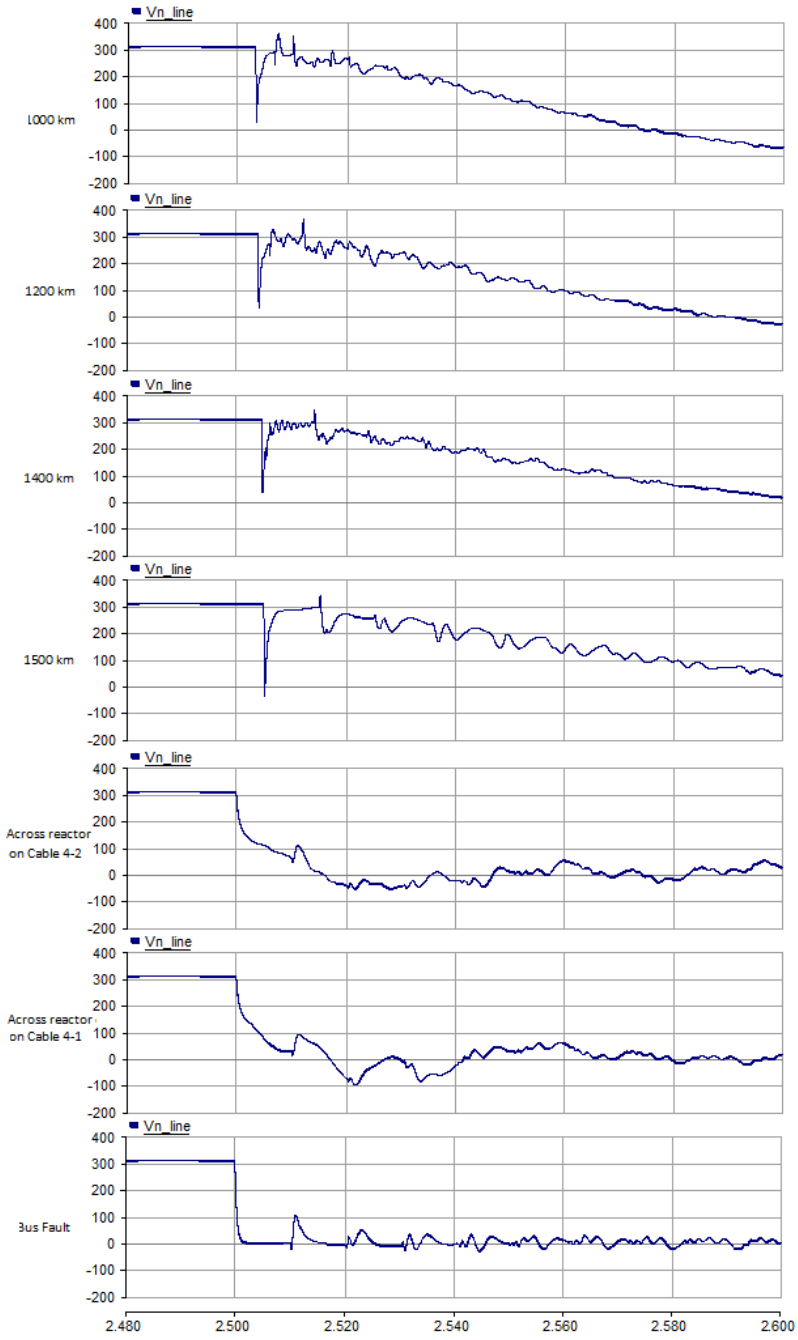

Figure 4-20 - Voltages (kV) at B43 for Different Fault Locations, Faults occur at Time = 2.5 seconds (Continued from previous page)

Table 4-4 - Maximum ROCOV at B43 for Different Fault Locations with 100 mH Inductors

Fault Location		ROCOV (kV/ms)
Line 3-4	Distance from Bus 4 (km)	
	0	30883
	50	22575
	100	15236
	200	10822
	300	8970
	400	7402
	600	6029
	800	5055
	1000	4389
	1200	3966
	1400	3583
	1500	4331
Cable 2-4	0	432
Cable 1-4	0	432
Bus Fault	0	1296

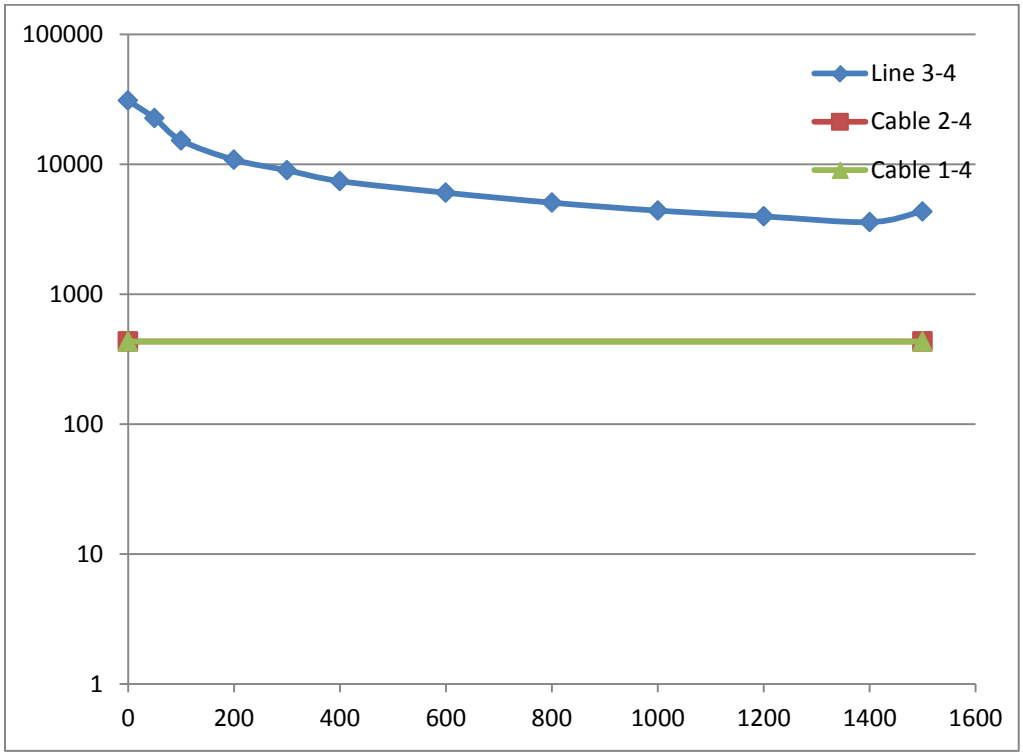

Figure 4-21 - ROCOV at B43 for Faults Down L3-4 towards Bus 3 and for Faults across the Inductors on C2-4 and on C1-4

4.2.1.3 ROCOV with Different Inductor Sizes (for a given breaker speed/rating)

Studies were performed to determine the impact of inductor size on ROCOV measurements as a fault detection method. For three different breakers, three different faults were simulated. Faults were simulated at the terminals of the breaker on the protected segment, 50 km down the protected segment and on an adjacent segment. The results can be seen in Table 4-5, Table 4-6 and Table 4-7.

Figure 4-22 shows three fault locations that were studied with different inductor sizes. Table 4-5 shows the ROCOV measurements at breaker B43.

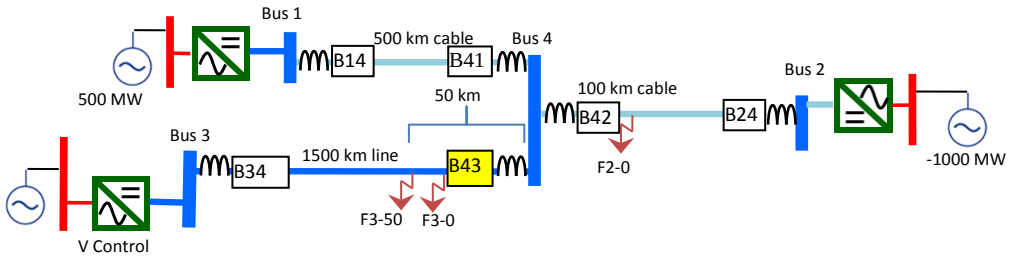

Figure 4-22 - Three Converter Test System Fault Locations for B43

Table 4-5 - ROCOV at B43 with Different Inductor Sizes

Inductor Size (mH)	Max ROCOV (kV/ms)		
	Fault across Inductor (F2-0 on Figure 4-22)	Fault 50 km Down Line to Bus 3 (F3-50 on Figure 4-22)	Fault at Breaker (F3-0 on Figure 4-22)
0	30203	572	30450
10	3685	19640	30897
100	432	22575	30883
200	218	22794	30928
500	88	22862	30873

Figure 4-23 shows three fault locations that were studied with different inductor sizes. Table 4-6 shows the ROCOV measurements at breaker B41.

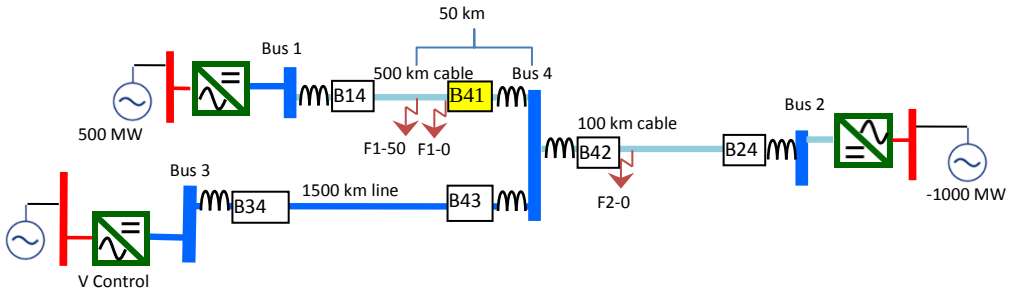

Figure 4-23 - Three Converter Test System Fault Locations for B41

Table 4-6 - ROCOV at B41 with Different Inductor Sizes

Inductor Size (mH)	Max ROCOV (kV/ms)		
	Fault Across Inductor (F2-0 on Figure 4-23)	Fault 50 km Down Cable to Bus 1 (F1-50 on Figure 4-23)	Fault at Breaker (F1-0 on Figure 4-23)
0	29984	12329	30437
10	204	23730	30653
100	31.8	23871	30648
200	21.6	23882	30653
500	13.8	23912	30691

Figure 4-24 shows three fault locations that were studied with different inductor sizes. Table 4-7 shows the ROCOV measurements at breaker B42.

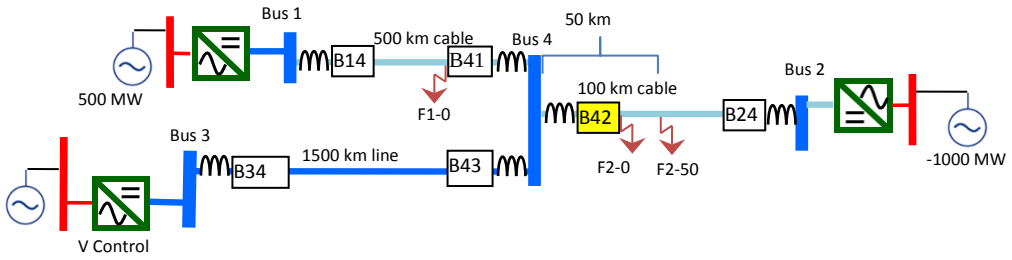

Figure 4-24 - Three Converter Test System Fault Locations for B42

Table 4-7 - ROCOV at B42 with Different Inductor Sizes

Inductor Size (mH)	Max ROCOV (kV/ms)		
	Fault Across Inductor (F1-0 on Figure 4-24)	Fault 50 km Down Cable to Bus 2 (F2-50 on Figure 4-24)	Fault at Breaker (F2-0 on Figure 4-24)
0	29984	12317	30437
10	224	23713	30671
100	51.8	23839	30643
200	34	23895	30703
500	20.3	23903	30700

It can be seen from Table 4-5, Table 4-6 and Table 4-7 that adding an inductor does not significantly change the ROCOV observed for terminal faults (the last column on tables) on the protected segment. Adding an inductor of any size does increase the ROCOV for faults a distance down the protected segment. This is due to the voltage doubling effect due to the reflection of the voltage wave at the inductor. Increasing the inductor value beyond 10 mH has very little impact for ROCOV measurements of faults on the protected segment. What increasing the inductor value does do, however, is decrease the observed ROCOV for faults on adjacent segments (column two of the tables) separated from the breaker by one or more inductors. The greater the inductance between the fault and the breaker, the lower the measured ROCOV. Based on this, it can be concluded that the inductance can be optimized to provide a significant enough margin between the lowest ROCOV measurement possible for a fault on the protected segment and the highest ROCOV measurement possible for a fault not on the protected segment.

4.2.2 **Pole-to-Ground vs Pole-to-Pole Faults**

Pole-to-pole (P-P) and pole-to-ground (P-G) faults were simulated on both test grids. For two fault locations (one on a line and one on a cable), the measured ROCOV at nearby breakers is listed.

Table 4-8 shows some results from simulations on the nine converter test grid. For two fault locations (one on a line and one on a cable), the measured ROCOV at nearby breakers is listed.

Table 4-8 – P-P vs P-G Faults for ROCOV

Fault Location	Breaker	P-P ROCOV (kV/ms)	P-G ROCOV (kV/ms)
B110 Terminals	B110	32354	32365
	B101	8712	5760
	B13	5.02	10.56
	B108	550	601
	B810	683	713
B31 Terminals	B31	31674	31596
	B13	4873	4861
	B34	3.32	11.23
	B43	3.47	10.77
	B12	10.83	18.19
	B21	10.09	21.39

Based on these two cases, it appears that the P-G faults provide

i. the lowest ROCOV on the protected line, and
ii. the highest ROCOV for faults on adjacent lines.

Therefore, for setting ROCOV protection thresholds to discriminate between the faults on the protected segment and faults on adjacent lines, P-G faults should be primarily considered. However, it is recommended to examine ROCOV values of P-P faults as well.

At steady state, on the other hand, a single pole-to-ground may provide the highest continuous current. The AC grid at the AC side of each AC/DC converter has a maximum amount of short circuit current that it can supply to a fault. For a pole-to-pole fault this short circuit current is divided between the two poles but for a pole-to-ground fault this short circuit capability is applied to only one pole.

4.3 Implementation of ROCOV Based Detection

This section documents the process and results of studies performed to set the ROCOV based protection thresholds for the breakers on the three converter test grid (Section 4.3.1) and the nine converter test grid (Section 4.3.2).

4.3.1 Three Converter Test System

Setting ROCOV threshold values requires determining the minimum possible ROCOV measured for a fault within the primary protection zone, for which the breaker should trip, and the maximum possible ROCOV for any fault for which the breaker should not trip. The threshold can then be set at an in-between ROCOV value with sufficient margins on both sides.

Table 4-9 shows the results of such an effort for the three converter test grid, with 100 mH di/dt limiting inductors. This inductance value was chosen somewhat arbitrarily at this point in the study. The lowest ROCOV on the protected segment can be compared to the highest possible ROCOV for a fault on a remote line or cable segment or bus or the subsequent clearing thereof. In some situations, clearing of a remote line or bus fault can create a ROCOV larger than that observed during the occurrence of the fault. Assuming that there is sufficient margin, a ROCOV threshold setting can be selected within said margin. If there is not sufficient margin, inductor values can be revisited to further reduce the ROCOV from remote faults.

Table 4-9 - ROCOV Based Protection Thresholds for Three Converter Test Grid with 100 mH Inductors

Breaker	Lowest ROCOV on Protected Segment	Remote Bus Fault ROCOV	Remote Fault	Highest ROCOV due to Fault on Adjacent Segment	ROCOV due to Remote Fault Clearing	ROCOV Trip Setting Selected
B41	1264	47.38	Cable 2-4	19.11	20.35	800
			Line 3-4	19	19	
B42	12662	103.74	Line 3-4	19	19	5000
			Cable 1-4	19	19	
B43	4331	602.15	Cable 2-4	432	525.9	2000
			Cable 1-4	432	756	
B14	1256	45.46	Cable 2-4	23.48	23.48	800
			Line 3-4	16.83	16.83	
B24	12672	94.8	Line 3-4	38.76	38.76	5000
			Cable 1-4	32	32	
B34	4110	786	Cable 2-4	274	274	2000
			Cable 1-4	276	360	

Setting these threshold values is an iterative process because the ROCOV due to clearing of faults can depend on the clearing time. The ROCOV from faults can be determined initially, and based on them, a set of preliminary threshold values can be chosen. The protection scheme can then be modeled, and the fault clearing can be simulated to determine the maximum ROCOV after the fault clearing. The preliminary ROCOV thresholds can then be updated if necessary. The breakers on an overhead line and a cable feeding into the same fault will see different effects when the fault is cleared. The presence of the cable feed-in will decrease the ROCOV seen by the breaker during the fault, but increase it during the clearing of the fault. For a fault on C1-4 (F1 in Figure 4-26), breaker B43 will see a higher maximum ROCOV when breaker B41 clears the fault than during the fault. For the same fault, breaker B42 will see a higher ROCOV during the initial fault than it will during the breaker clearing.

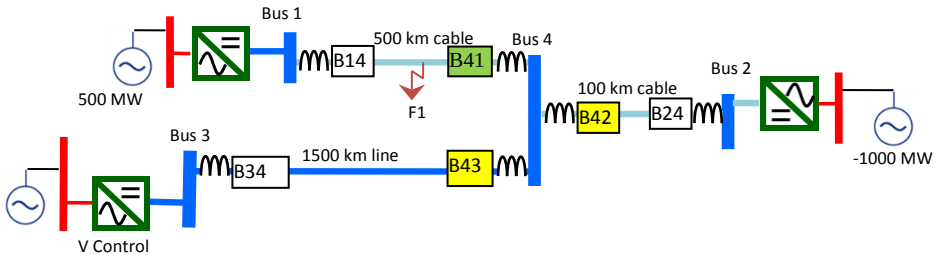

Figure 4-25 – Three Converter Grid

Bus faults should result in all breakers at that bus tripping. A local bus fault can be identified by comparing the voltages on both sides of all di/dt limiting inductors at the bus. When the condition defined in Equation (2) is met for all branches at the bus, a bus fault has occurred and all local breakers should trip.

$$\frac{dv_{bus}}{dt} > \frac{dv_{line}}{dt} \qquad \textbf{(2)}$$

Where v_{bus} is the voltage at bus side of the inductor and v_{line} is the voltage at line side of the inductor.

In Figure 4-26, the fault at Bus 2 could be located by comparing the observed ROCOV on either side of the inductors at B2, B3 and B4. All would see a higher ROCOV on the bus side.

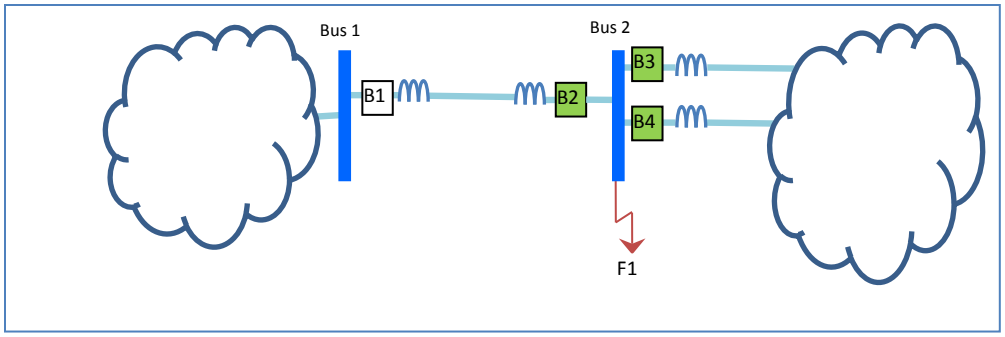

Figure 4-26 - Bus Fault Example

ROCOV for a fault on the bus at the far end of a line or cable ideally should not trip a breaker. This is not critical, however, as a remote bus fault will result in tripping the breaker at the other end of the line segment so the line segment is out of service. The results in Table 4-9 and Figure 4-18 show that there is still significant margin between the ROCOV for faults on remote busses and faults on protected line segments.

4.3.2 **Nine Converter Test System**

The same ROCOV threshold setting exercise that was performed for the three converter test grid was also undertaken for the nine converter test grid. Table 4-10 shows the results of study performed to set ROCOV based protection thresholds.

Table 4-10 - ROCOV Based Protection Thresholds for Nine Terminal Grid with 100 mH di/dt Limiting Inductors

Breaker	Lowest ROCOV on Protected Segment (Remote End of Segment)	Remote Fault	Highest ROCOV Due to Fault or Subsequent Clearing on Remote Segment (20 km From End)	ROCOV Trip Setting Selected
B21	4874	C13	14.51	1000
		L110	9.95	
		L19	11.91	
B12	4940	C13	17.25	1000
		L110	9.5	
		L19	13.35	
B13	4865	C12	18.19	1000
		C34	16	
		L19	9.1	
B31	4859	C34	17	1000
		C12	21.7	
		C19	10.48	
B34	4785	C31	31.5	1000
		C45	17.6	
B43	4800	C45	17	1000
		C31	30.1	
B45	4950	C43	10	1000
		C65	24.4	
B54	4940	C56	19	1000
		C43	10.88	

B56	4818	C54	14.65	1000
		C67	35	
B65	4885	C54	14.8	1000
		C67	34.8	
B67	433	C65	18	200
		C78	55	
B76	9835	C78	1268	4000
		C65	54	
B78	7183	L76	1043	3500
		L810	1453	
B87	7807	L810	1338	3500
		L76	1226	
B810	6720	C87	1108	3000
		L109	503	
B108	6370	C87	928	3000
		L109	1163	
B59	10169	C65	48	1000
		L910	20	
B95	10213	C65	49	1000
		L910	21	
B109	8761	L91	58	3000
		C95	58	
		L101	773	
B910	8457	L91	55	3500
		C95	55	
		L101	1221	
B101	5754	C13	41.3	2500
		L109	1172	
B110	5359	C13	36	2000
		L109	422	
B19	6257	C13	54.7	2000
		C95	45	
B91	6383	C13	46	2000
		C95	48	

It can be seen in the results from Table 4-9 and Table 4-10 that there is enough margin between minimum ROCOV for faults on the protected segment and maximum ROCOV for faults on adjacent segments to distinguish between them. If the inductor values need to change in order to limit the rate of rise of fault current, then this threshold setting exercise should be re-visited.

4.4 **Concluding Remarks**

This chapter presented the proposed method for a breaker to quickly determine if there is a fault on the transmission segment that it is protecting and if it needs to trip. Studies were performed to test the proposed concepts and the results showed that the proposed protection concept can successfully detect and discriminate the faults on a DC grid, provided that di/dt limiting inductors are connected in series with each breaker. A process for setting protection thresholds was discussed and the results of the process applied to the two different test grids were documented.

5 Series Inductor and Breaker Rating

This chapter presents the results of studies performed to analyze the impact of di/dt limiting inductors on fault current and the process of sizing these inductors. Simulation studies were carried out in PSCAD to examine the operation of the hybrid DC breaker combined with the proposed protection approach.

5.1 Fault di/dt Limiting Inductors

A fault on a DC grid can result in a rapid discharge of the energy in the DC capacitors of VSCs and DC cable capacitances into the fault. Thus the current can ramp up very quickly. Any given DC circuit breaker technology will have a maximum current that it can interrupt and a maximum operating time. In the case of the hybrid DC breaker discussed in Section 2.4, this operating time is mainly determined by the time necessary to open the fast mechanical disconnecter. In order to limit the current rise during the breaker operating time to a value below the maximum interruptible current of the breaker, it is necessary to place di/dt limiting inductors in series with the DC circuit breakers [28] as indicated in Figure 5-1.

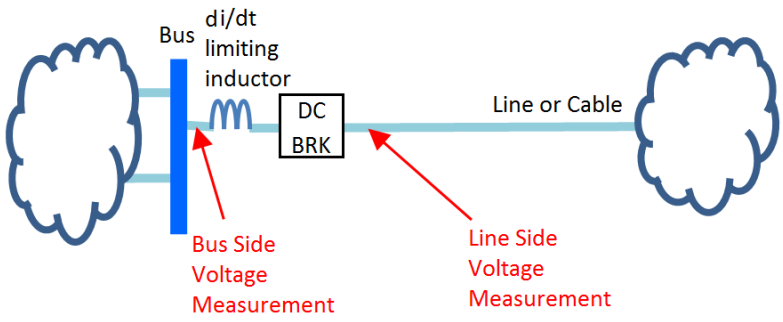

Figure 5-1 - Bus, Inductor, Breaker, and Measurements

Section 5.1.1 documents study results where faults are simulated in the three converter test grid with di/dt limiting inductors. The currents through each of the breakers are plotted. Section 5.1.2 documents the results of study where for a given breaker and a given fault location, the current through that breaker is plotted for different di/dt limiting inductor values. Section 5.1.3 summarizes the results from the preceding two sections and discusses some conclusions. Section 5.1.4 addresses the impact of inductor size on steady state fault currents.

5.1.1 **Initial di/dt Limiting Studies**

Simulations were run to determine the fault currents in the three converter test grid for several faults with different di/dt limiting inductor values. Using a systematic approach, different fault locations were simulated and the currents at the six breaker locations were plotted. The time between the fault and when the current exceeded 10 kA was calculated for each breaker and then tabulated. Two different inductor values, 50 mH and 100 mH, were considered. Example simulation results for two different fault locations are presented in Figure 5-2.

The grid currents for a pole-to-ground fault on cable C1-4, 50 km away from bus 4 with 50 mH and 100 mH inductors, can be seen plotted in Figure 5-2 and Figure 5-3 respectively.

These results shown in Figure 5-2 and Figure 5-3 can be compared to Figure 3-22 which is a plot of the same currents but with no inductors present. The results of calculating the time between the fault and when the current exceeded 10 kA is summarized in Table 5-1. For this cable fault close to bus 4, without the di/dt limiting inductor, the fault current quickly exceeds the arbitrarily chosen 10 kA at the nearby breaker locations. With either the 50 mH or 100 mH inductor added, there is more time before the current exceeds this limit. The critical breakers in this case are B14 and B41 as these are the breakers that should trip for this fault. The entry not applicable (n/a) is used when the fault current at the particular breaker locations does not exceed 10 kA.

Table 5-1 - Current Rise at Different Breakers for Fault on Cable 1-4 50 km from Bus 4

Detection Location	Time from Fault to 10 kA (ms)		
	No Protection Inductors	50 mH Protection Inductors at all Breakers	100 mH Protection Inductors at all Breakers
B14	4.26	5.97	7.47
B41	0.46	8.46	161
B42	0.46	10.5	n/a
B43	0.46	n/a	n/a
B24	1.39	121	n/a
B34	n/a	n/a	n/a

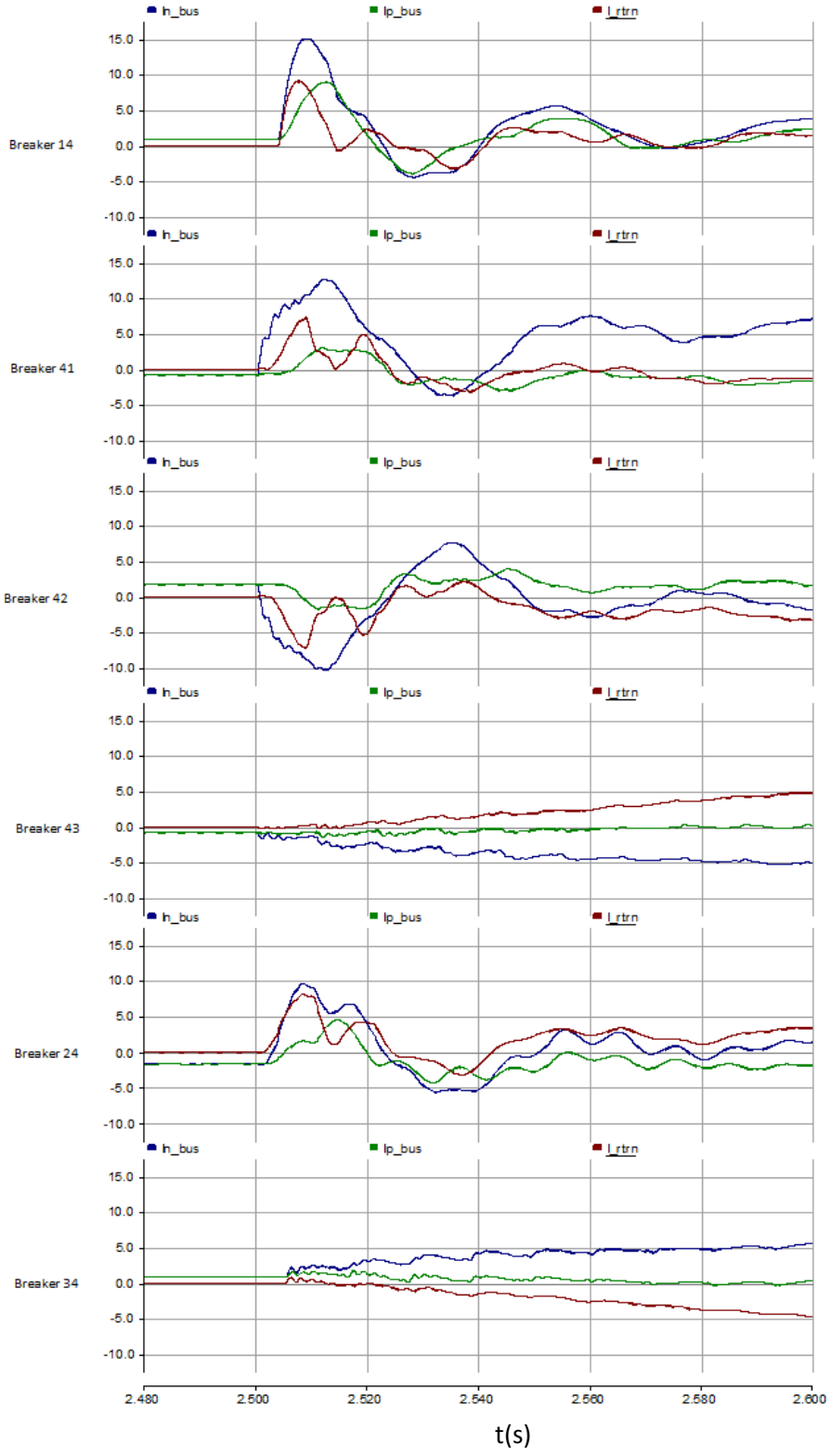

Figure 5-2 - Currents (kA) for a Pole-to-Ground Fault 50 km from Bus 4 on C1-4 with 50 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

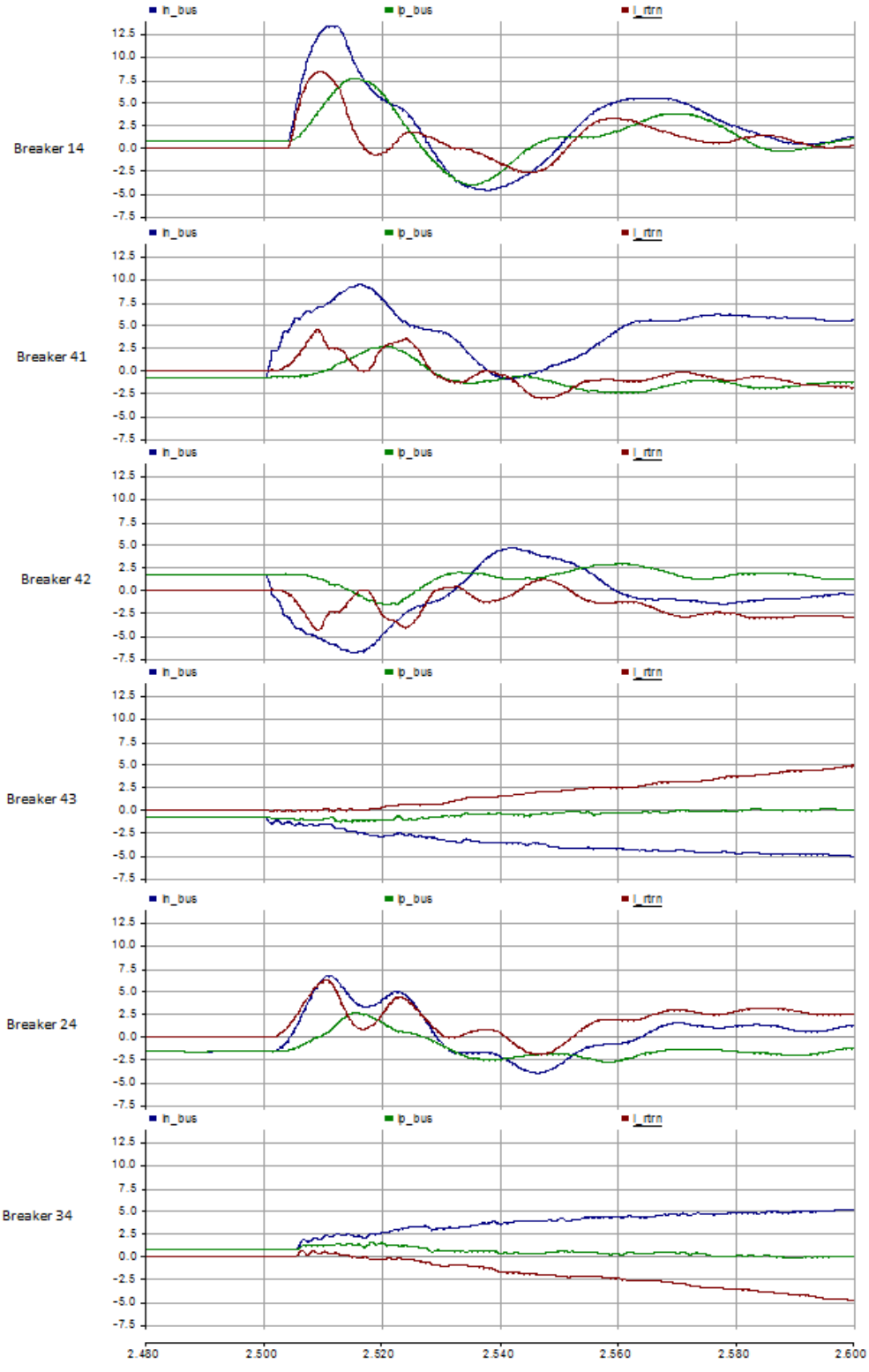

Figure 5-3 – Currents (kA) for a Pole-to-Ground Fault 50 km from Bus 4 on C1-4 with 100 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

Figure 5-4 and Figure 5-5 show the same plots for a pole-to-ground fault on L3-4 with 50 mH and 100 mH inductors respectively.

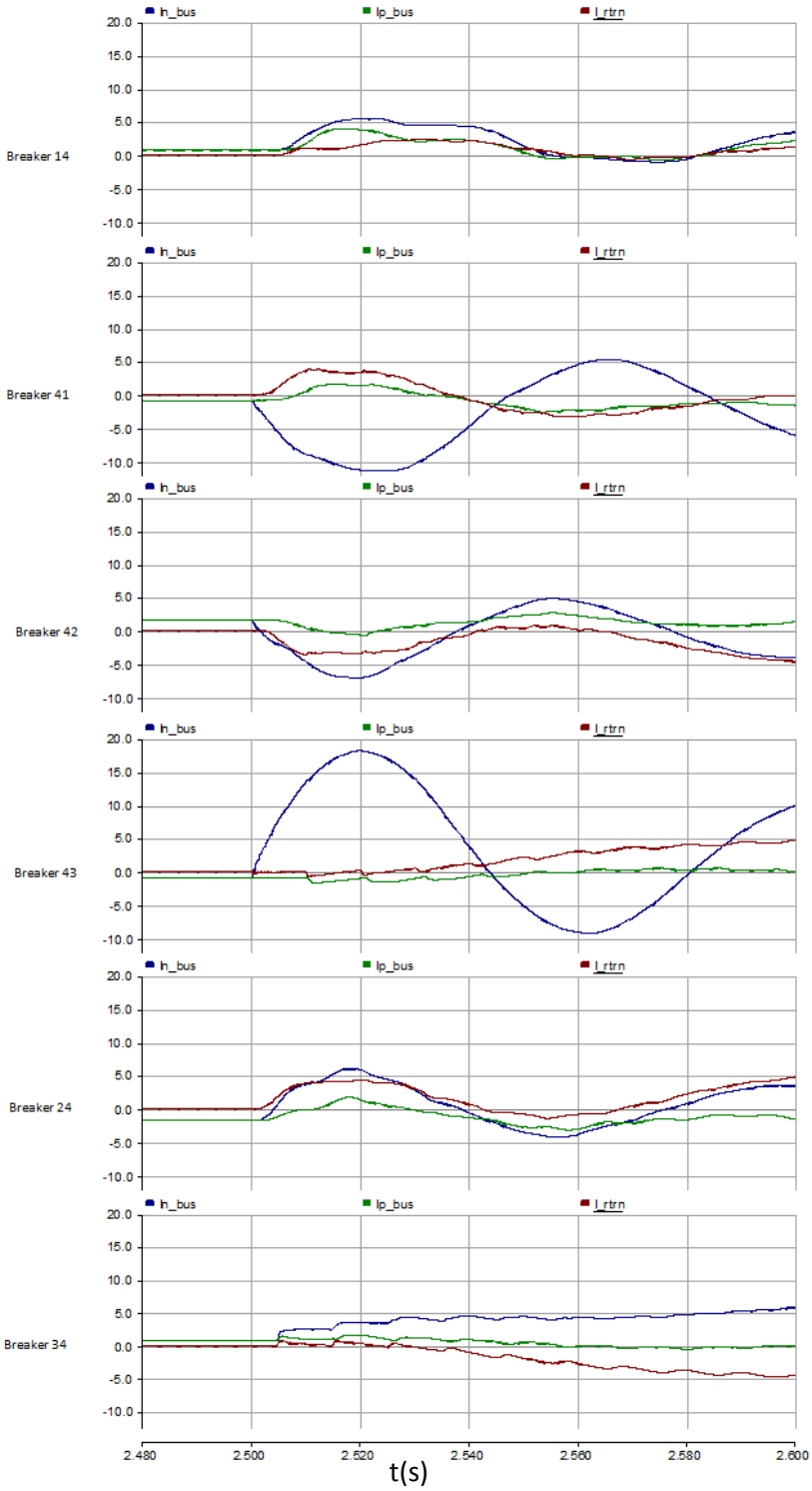

Figure 5-4 – Currents (kA) for a Pole-to-Ground Fault 50 km from Bus 4 on L3-4 with 50 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

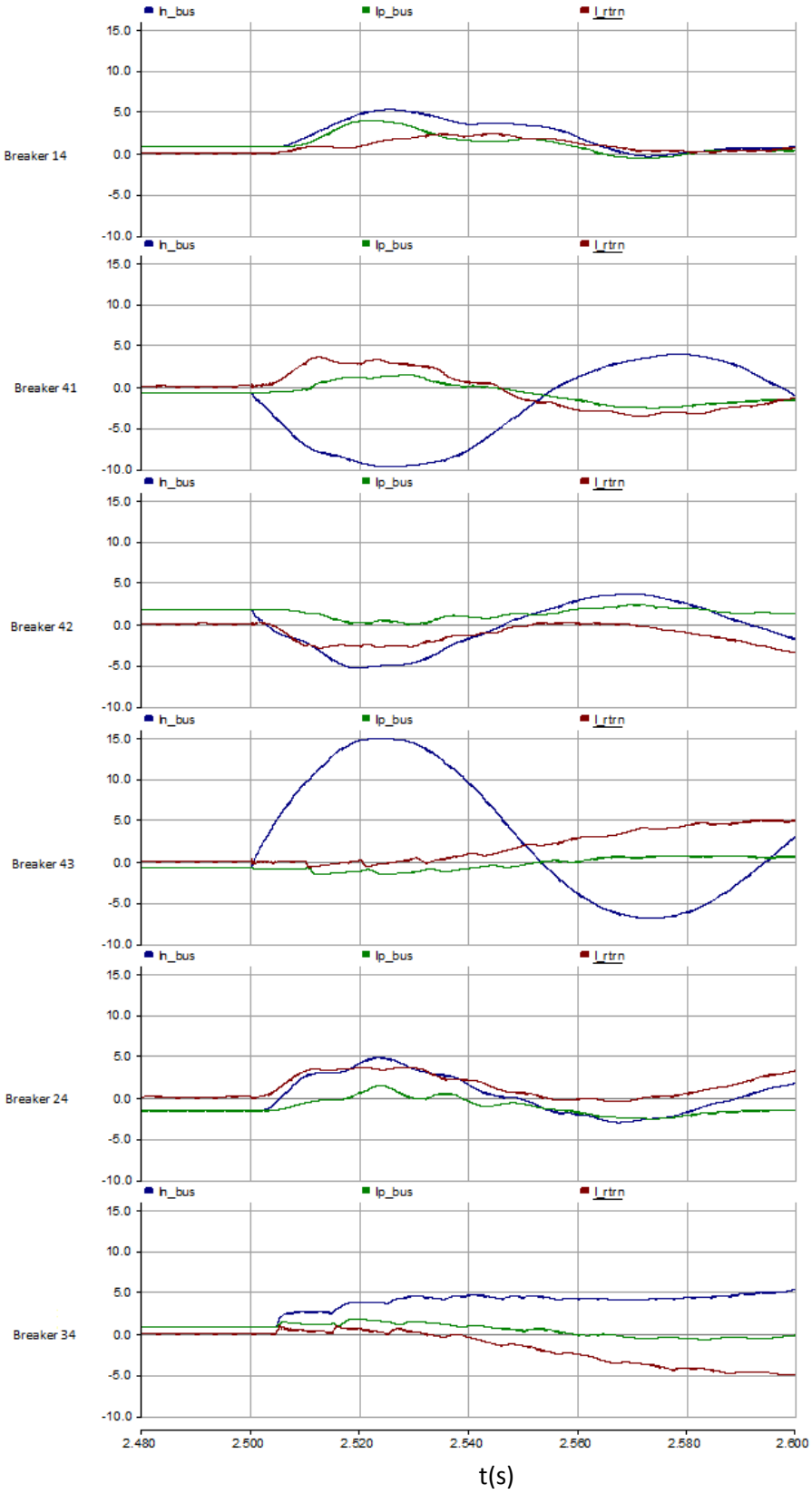

Figure 5-5 – Currents (kA) for a Pole-to-Ground Fault 50 km from Bus 4 on L3-4 with 100 mH Inductors (blue – negative pole, green – positive pole, brown – metallic return)

The times taken for fault currents to reach the 10 kA limit for faults on L3-4 are summarized in Table 5-2. It can be seen that most of the results in this table are not applicable (n/a) as the fault current at most of breaker locations on the three converter grid does not exceed 10 kA. The critical breaker, of course, is B43. The current at this breaker does exceed 10 kA and increasing the inductor size increases the time before that happens, giving the breaker more time to operate before its maximum interruptible current is exceeded.

Table 5-2 - Current Rise Times for Fault 50 km down L3-4 from Bus 4

Detection Location	Time from Fault to 10 kA (ms)		
	No Protection Inductors	50 mH Protection Inductors at all Breakers	100 mH Protection Inductors at all Breakers
B14	n/a	n/a	n/a
B41	6.98	n/a	n/a
B42	n/a	n/a	n/a
B43	3.08	6.81	10.8
B24	n/a	n/a	n/a
B34	n/a	n/a	n/a

It can be concluded that increased inductor values decreases the rise in fault currents throughout the grid.

5.1.2 **Inductor Sizing Studies**

Simulations were performed to determine the impact of different inductor sizes on fault current ramp-up times. The results are presented in Figure 5-6 to Figure 5-11 and Table 5-3 to Table 5-5.

Figure 5-6 and Figure 5-7 show fault currents measured at breaker B43 for a fault at the terminals of B43 and a fault 50 km from B43 down the line L3-4.

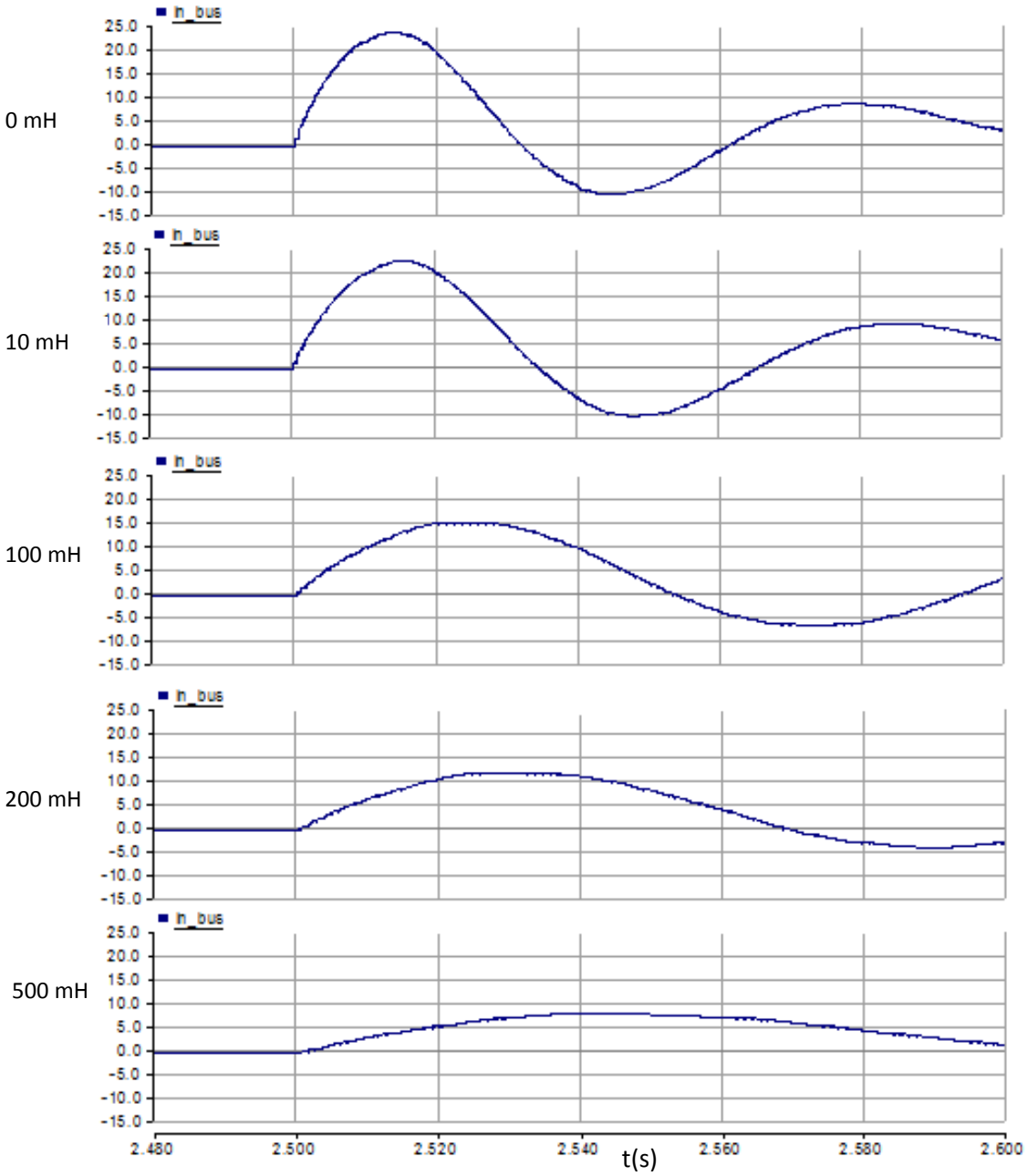

Figure 5-6 – Current (kA) for Fault 50 km from Bus 4 on L3-4, Measured at B43

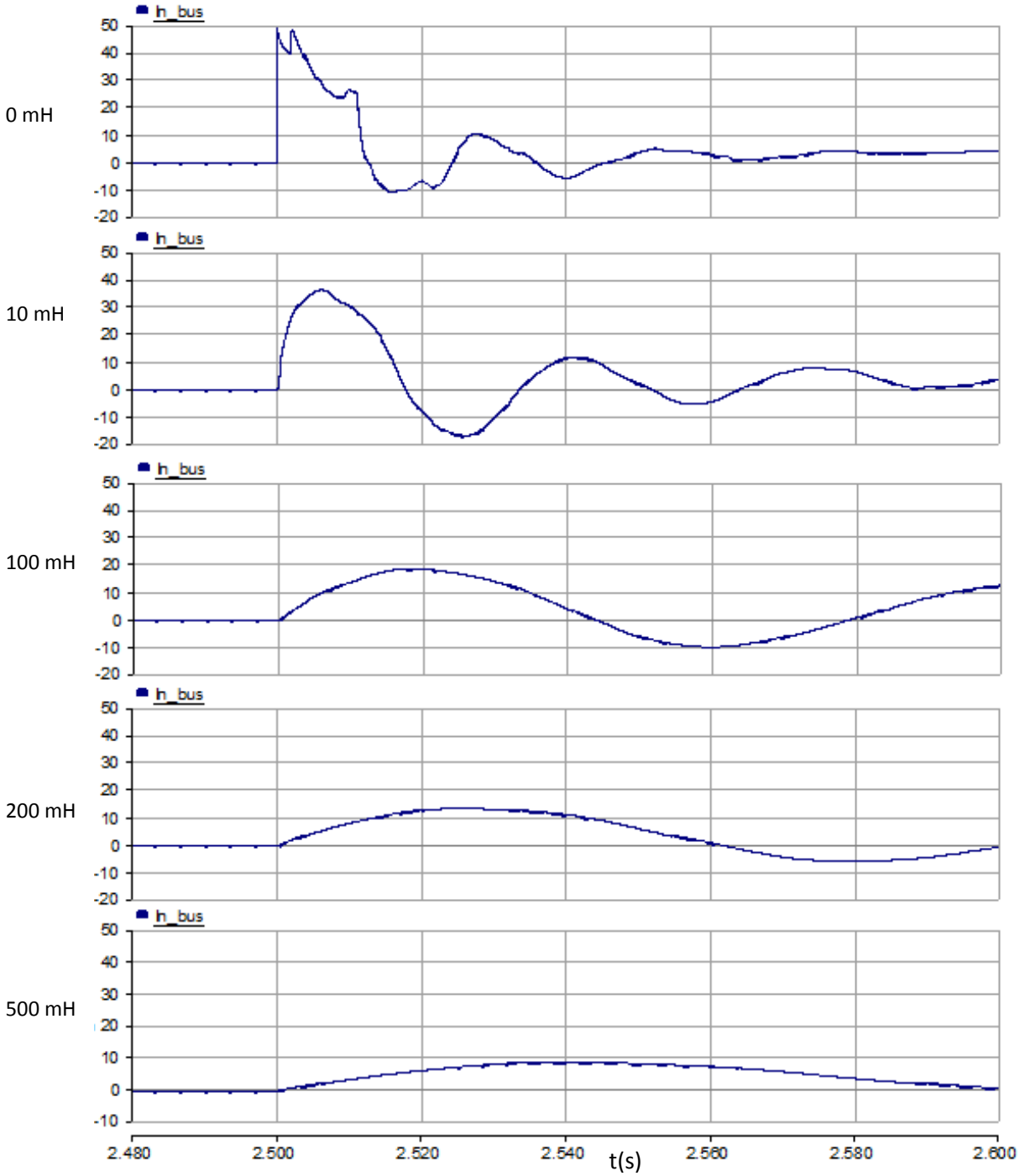

Figure 5-7 – Current (kA) for Fault 0 km from Bus 4 on L3-4, Measured at B43

It can be seen from these plots that the higher the inductor size, the slower the initial rise in fault current through the breaker. This is reflected in Table 5-3 which shows the time between the fault occurrence and the time when the fault current exceeds 10 kA.

Table 5-3 - Fault Current Rise at B43 with Different Inductor Sizes

Fault Current Rise at B43 with Different Inductor Sizes		
Inductor Size (mH)	Time Between Fault and 10 kA Fault Current (ms)	
	Fault 50 km Down Line	Fault at Breaker
0	3.1	0
10	3.8	0.6
100	10.8	6.6
200	19.3	14.6
500	201	193

Figure 5-8 and Figure 5-9 show fault currents at breaker B41 for a fault at the terminals of B41 and a fault 50 km down the cable from B41.

The results of the times to exceed the 10 kA limit corresponding to Figure 5-8 and Figure 5-9 are summarized in Table 5-4.

Table 5-4 - Fault Current Rise at B41 with Different Inductor Sizes

Inductor Size (mH)	Time Between Fault and 10 kA Fault Current (ms)	
	Fault 50 km Down Line	Fault at Breaker
0	0.5	0
10	1	0.9
100	161	16.3
200	178	163
500	211	208

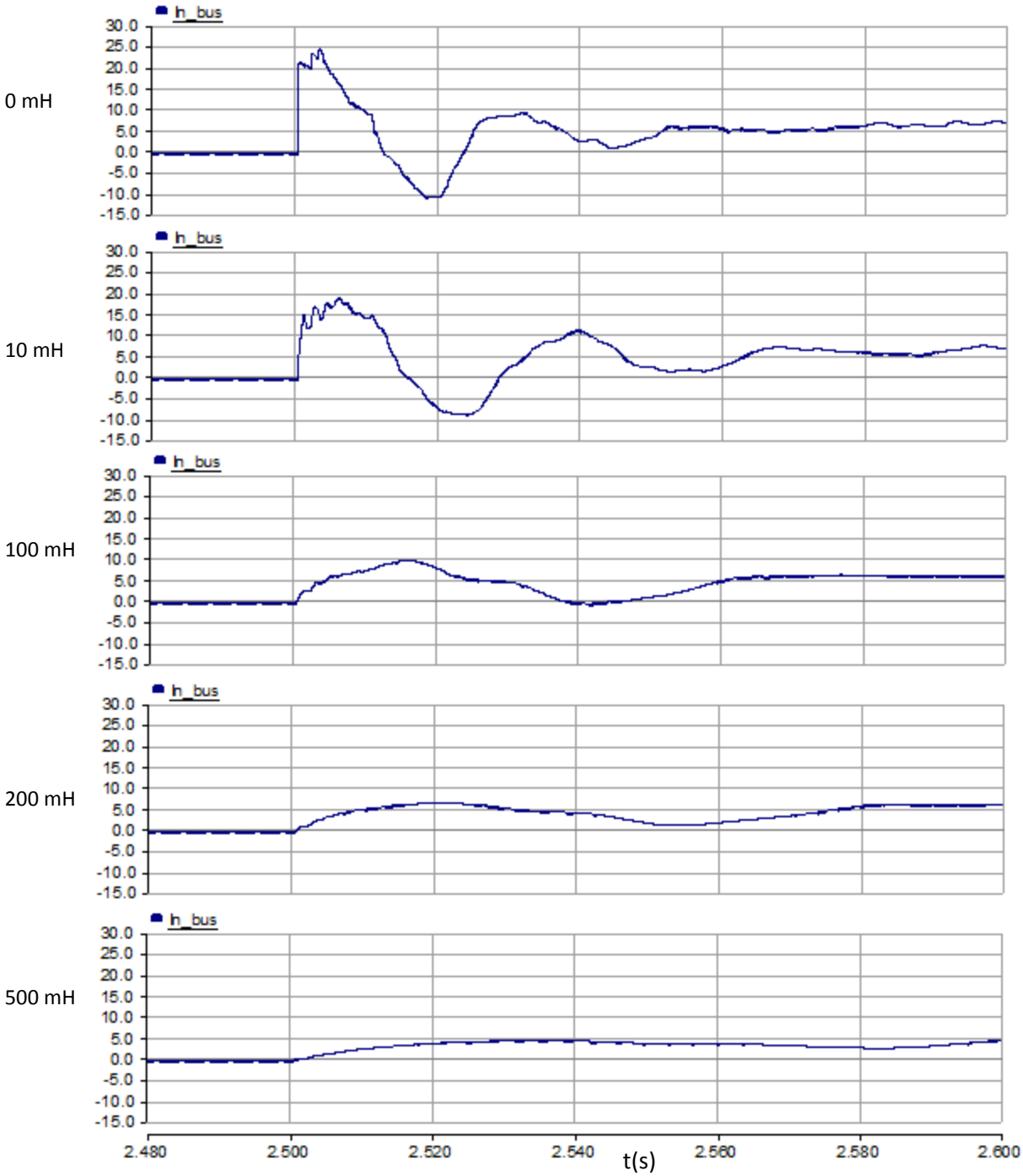

Figure 5-8 – Current (kA) for Fault 50 km from Bus 4 on C1-4, Measured at B41

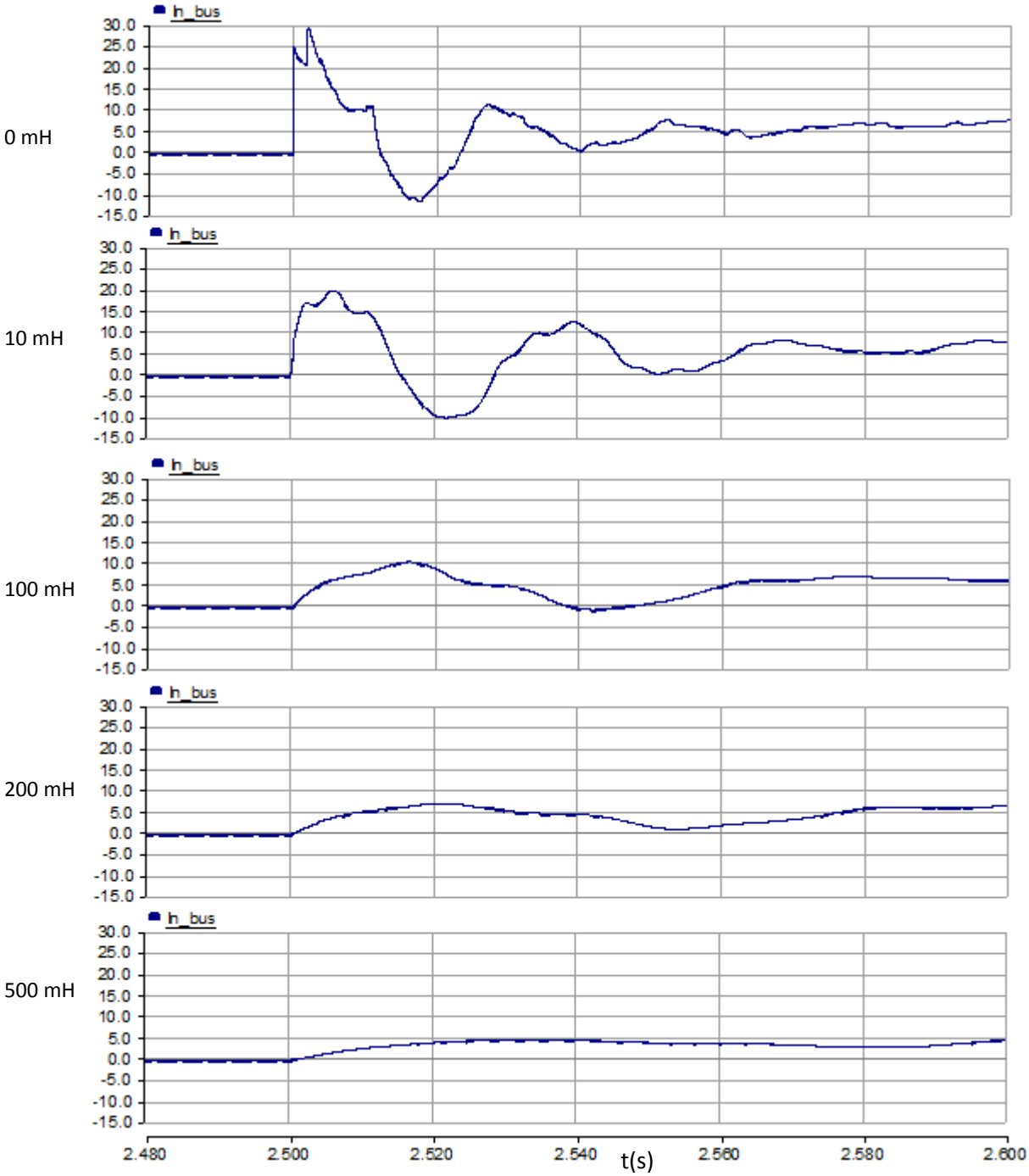

Figure 5-9 – Current (kA) for Fault 0 km from Bus 4 on C1-4, Measured at B41

Figure 5-10 and Figure 5-11 show the currents through B42 for faults at the B42 terminals and 50 km down the cable to bus 2 with different inductor values.

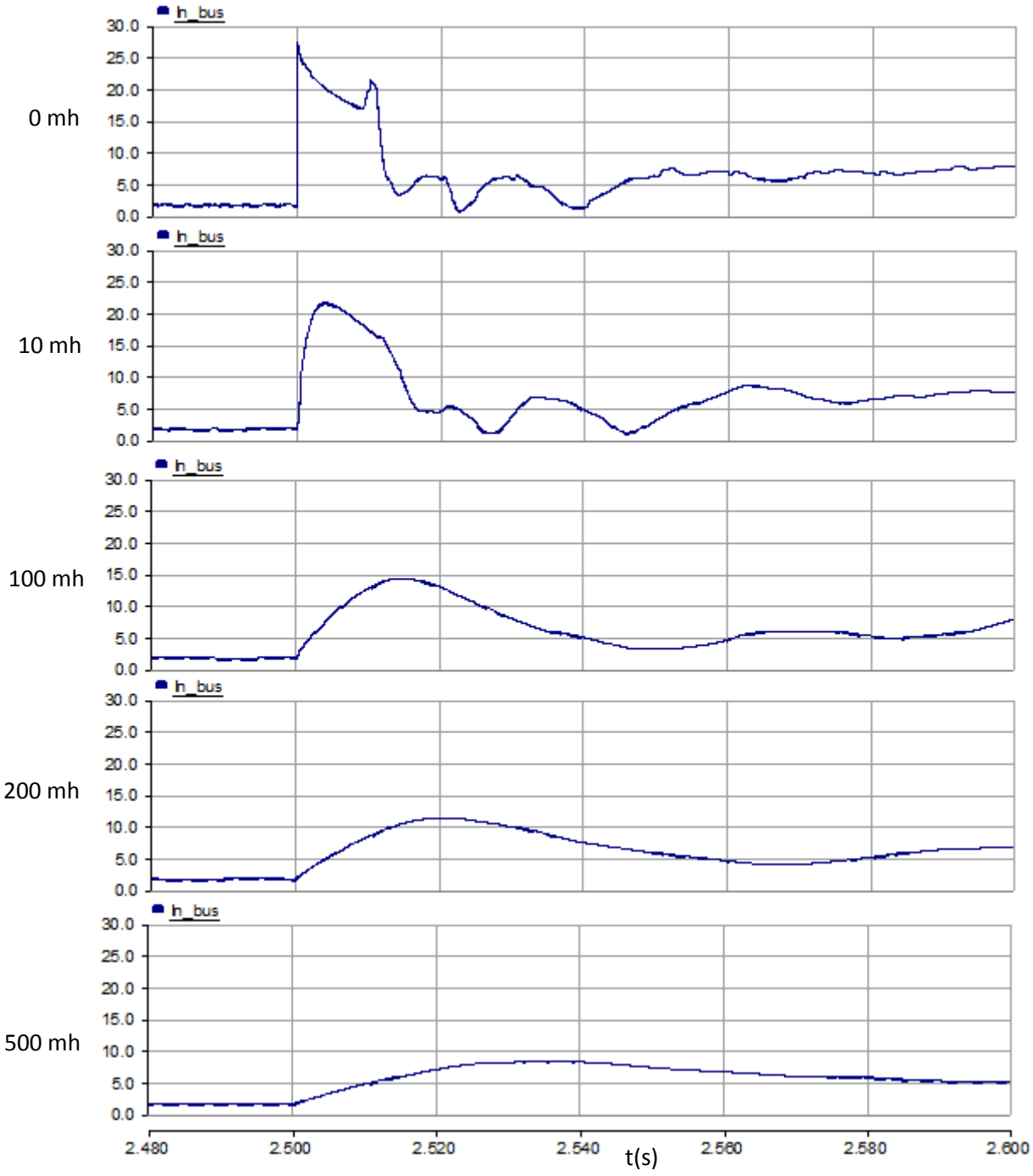

Figure 5-10 – Current (kA) for Fault 0 km from Bus 4 on C2-4, Measured at B42

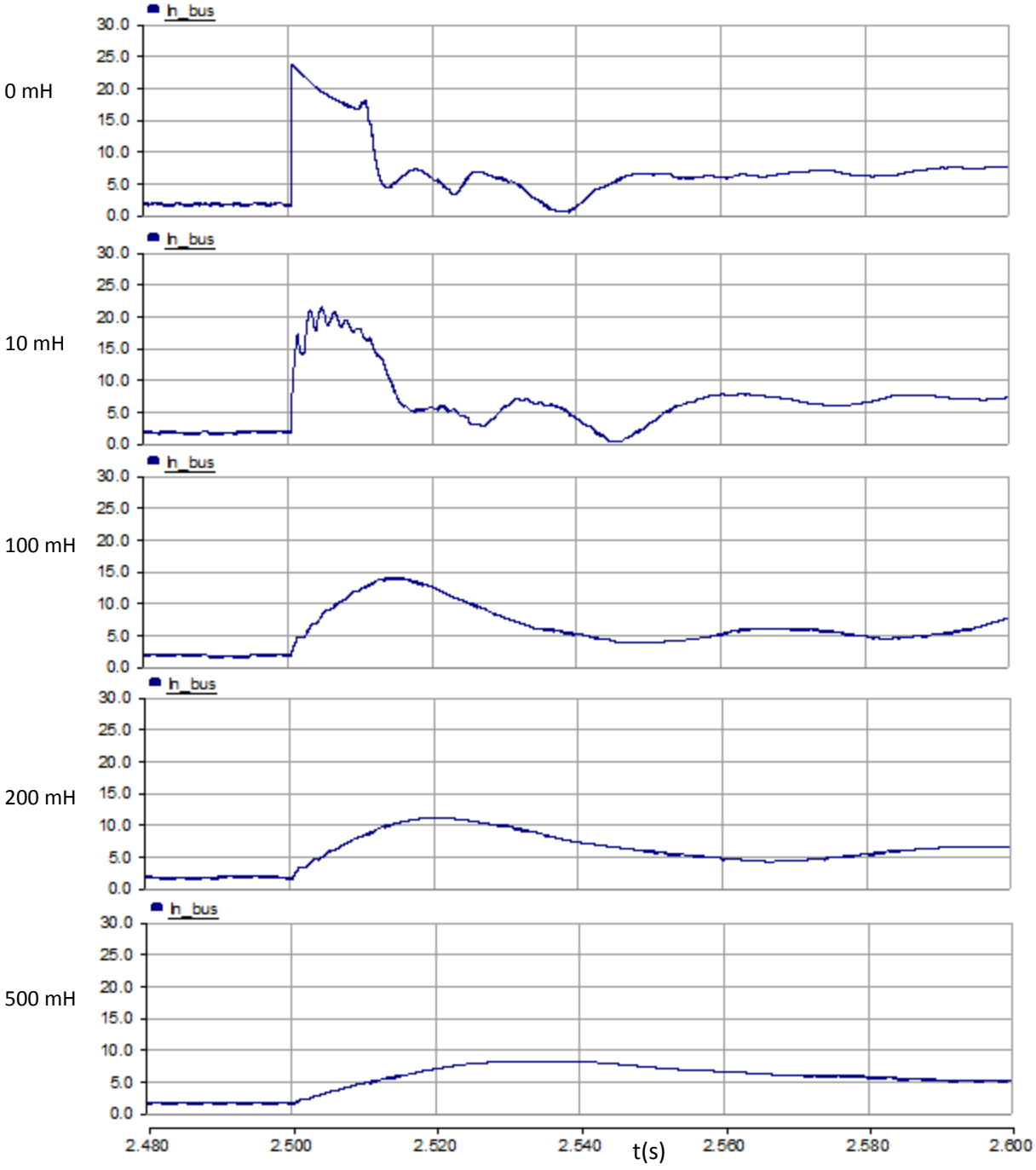

Figure 5-11 – Current (kA) for Fault 50 km from Bus 4 on C2-4, Measured at B42

The results of estimating the time to exceed 10 kA limit are summarized in Table 5-5.

Table 5-5 - Fault Current Rise at B42 with Different Inductor Sizes

Inductor Size (mH)	Time Between Fault and 10 kA Fault Current (ms)	
	Fault 50 km Down Line	Fault at Breaker
0	0.43	0
10	0.8	0.6
100	6.8	6.6
200	14.2	13.6
500	190	686

The fastest current ramp-up rates were observed for terminal faults on the line side of breaker B43. This is because of the fault current contributions from charge stored in the highly capacitive cables C1-4 and C2-4.

In Figure 5-6 through Figure 5-11 it can clearly be seen that the higher inductor values slow down the rise in fault current. For a breaker with a given operating time and a maximum interruptible current, it would be necessary to size the inductors such that for all fault types and all fault locations, the current rises slowly enough for the breaker to detect the fault and operate before the current rises beyond the breaker's interrupting capability.

5.1.3 **Important Factors to be Considered in Inductor Sizing**

Figure 5-12 shows simulated negative pole current and the voltages on both line and bus sides of the di/dt limiting inductor at B14 for a negative pole-to-ground fault on the line side of the inductor. The fault was initiated at t = 2.5 s. For this simulation, small 1 mH inductors were placed in series with all of the circuit breakers in the three converter HVDC grid.

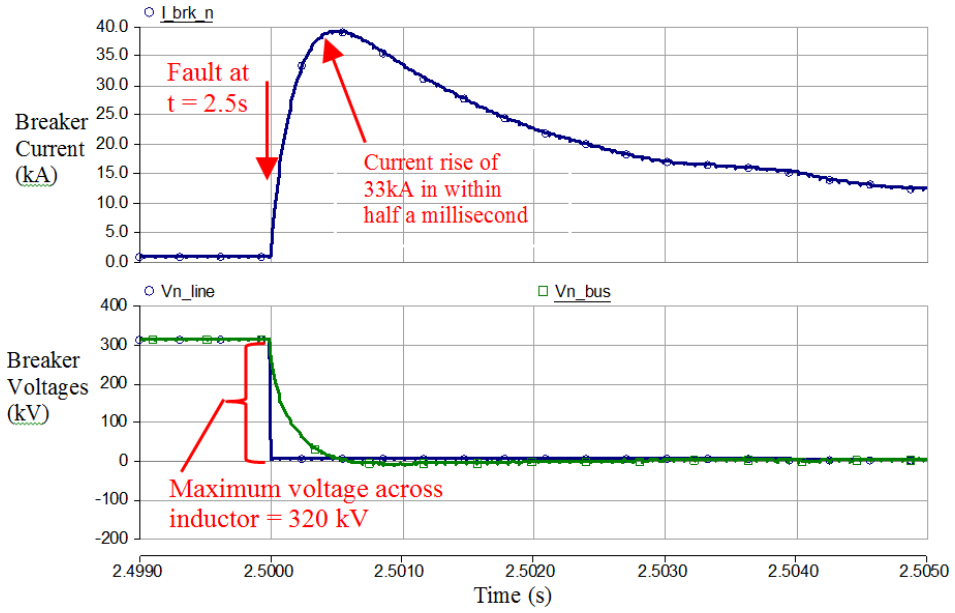

Figure 5-12 - Current and Voltage on both Line and Bus Side of the 1 mH di/dt Limiting Inductor at B14 for a Terminal Fault at Time = 2.5 seconds

With only 1 mH di/dt limiting inductors, the current quickly rises beyond the interrupting capability of the DC breaker. When the size of inductors is increased to 100 mH, the current rises much more slowly, as seen in Figure 5-13. It can be observed that the voltage on the faulted side of the breaker immediately drops to zero. The voltage on the bus side of the breaker decreases as the fault current ramps up.

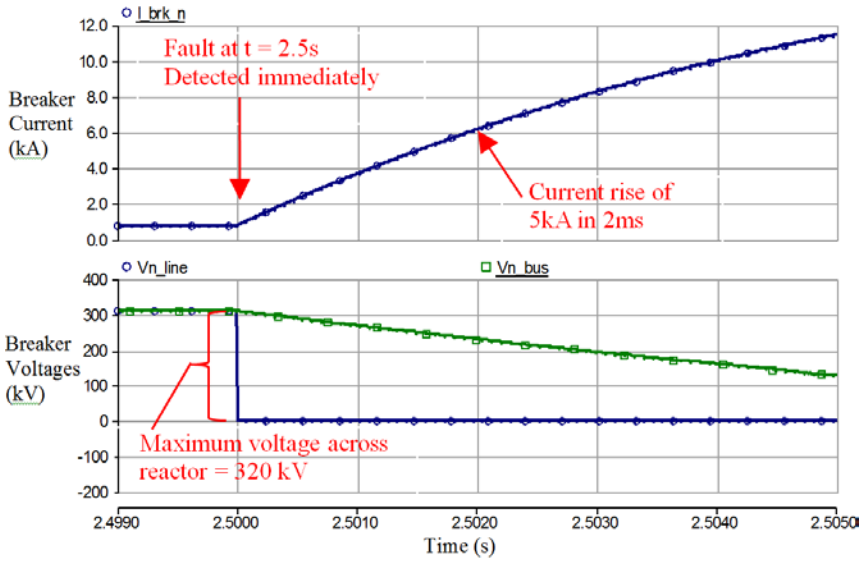

Figure 5-13 - Current and Voltage on both Line and Bus Side of the 100 mH di/dt Limiting Inductor at B14 for a Terminal Fault at Time = 2.5 seconds

The fault current increase given by Equation (1) is directly proportional to the voltage difference across the inductor. If the di/dt limiting inductor is 100 mH, for a ±320 kV grid operating at 1.1 pu voltage, the maximum theoretical rate of rise of current due to a fault at the line terminals is

$$\frac{di}{dt} = \frac{\Delta V}{L} = \frac{350kV}{0.1H} = 3.5\frac{kA}{ms} \quad (3)$$

In a case with more capacitance on the bus side of the breaker, possibly due to a larger converter or due to more cables feeding into the bus, the bus side voltage would remain high and the current rate of rise would not taper down as quickly. Thus the current rises almost linearly as shown in Figure 5-13. In Figure 5-14, the rise in current through breaker B14 for a fault on the line terminal close to the breaker is shown for different inductor values.

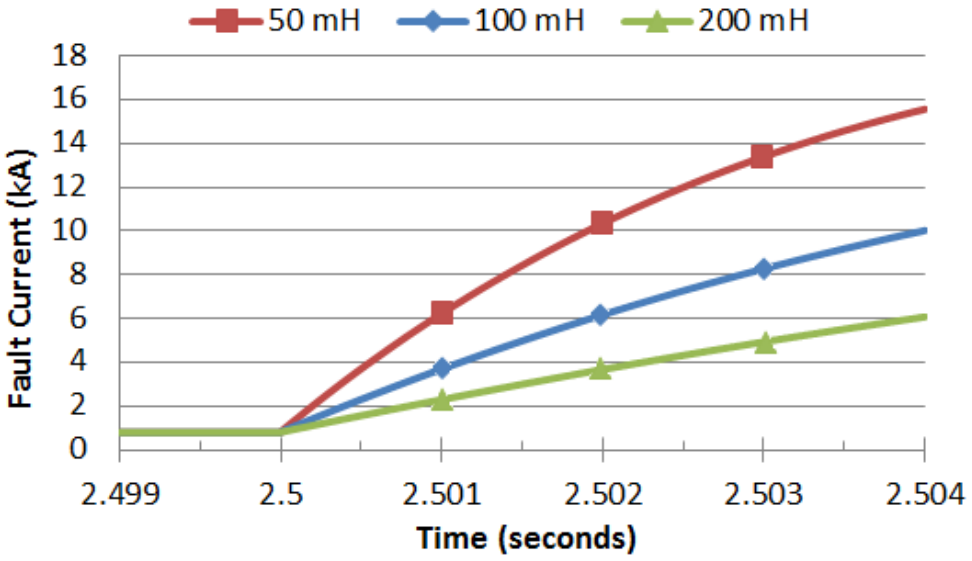

Figure 5-14 - Current Rise at B14 with Different Inductor Values for Terminal Fault at Time = 2.5 seconds

When choosing di/dt limiting inductor values, the breaker operating time and maximum interuptible current should be taken into account and the inductor should be sized accordingly. It should also be noted that the terminal fault shown here does not provide the highest possible rate of rise of current. Figure 5-15 shows the same quantities shown in Figure 5-13 (100 mH inductor), when the fault (at t = 2.5 s) is moved 150 km down the cable C1-4.

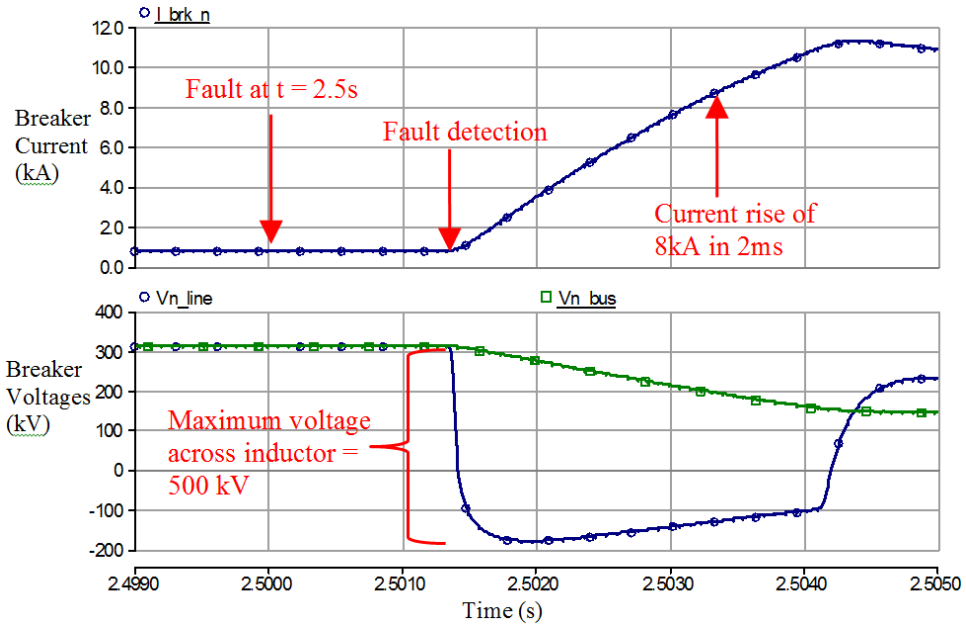

Figure 5-15 - Current and Voltage on both Line and Bus Side of the 100 mH di/dt Limiting Inductor at B14 for Fault 150 km Down the Cable at Time = 2.5 seconds

It can be observed in Figure 5-15 that in this case the fault transient takes approximately 1.4 ms to reach breaker B14 and that when it arrives, the voltage on the line side of the breaker drops below zero. The reflection of the incoming wave by the inductor results in a 'voltage doubling' at the line side of the inductor terminal. Due to increased voltage difference across the inductor (almost double), the rate of rise of current is much faster in this case. This phenomenon is most significant in cables.

The fastest rate of rise in current through a DC breaker occurs when the fault is located at a distance equal to the distance that the fault transient travels in half the operating time of the breaker. In the cable modeled in the test system, the fault transient travels at approximately 110 km/ms. For a breaker having an operating time, T_{op} = 2 ms, this critical fault location, *Dcrit*, that provides the highest current that the breaker needs to be able to interrupt, can be obtained as:

$$\boldsymbol{Dcrit = \frac{Velocity * Top}{2} = 110\frac{km}{ms} * \frac{2ms}{2} = 110km} \qquad (4)$$

If the fault current exceeds the capability of the breaker at its maximum operating time for a fault at *Dcrit*, the size of the inductor should be adjusted to limit the rise in current. Figure 5-16 shows the current rise for the fault 150 km down the cable when different inductor values are considered.

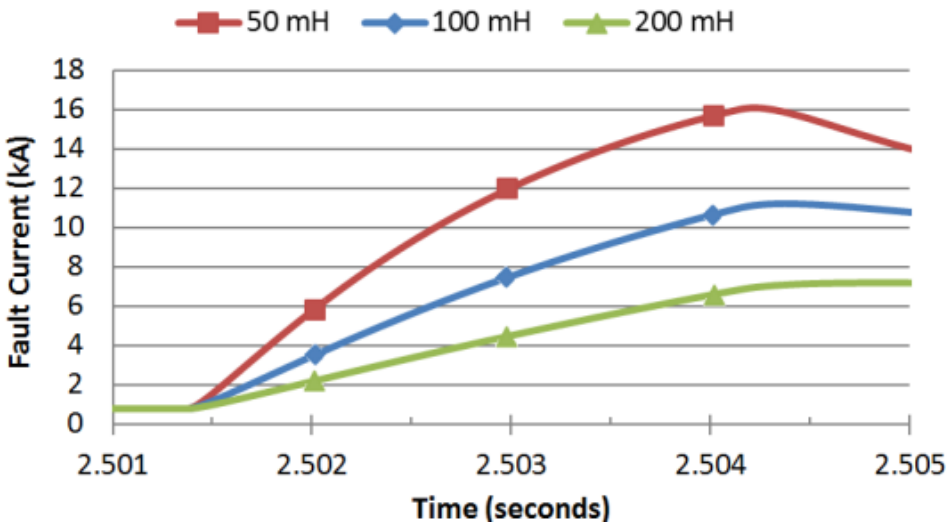

Figure 5-16 - Current Rise at B14 with Different Inductor Values for Fault 150 km Down the Cable at Time = 2.5 seconds

Detailed simulation studies (not all results are presented) showed that the worst case current should be determined for a given breaker by simulating

i. pole-to-pole faults
ii. at the highest possible operating voltage
iii. with the highest possible pre-fault operating current
iv. with the maximum breaker operating time, and
v. at the worst case location.

The worst case location for cables is as described above. The worst case fault location for the overhead lines modeled in this study is at the terminals of the breaker. The overhead lines have much less capacitance compared to the cables. The transient travel speed is significantly higher and the traveling wave has much lower current due to the lower capacitance to inductance ratio. There should be some margin between the worst case current and the interrupting limit of the breaker.

5.1.4 Inductor Size Impact on Steady State Fault Current

Figure 5-17 and Figure 5-18 respectively show the current measured through B42 for a terminal fault with 500 mH inductors and 10 mH inductors. The value of the di/dt limiting inductor has no significant impact on the final steady state fault current, which is as expected. Only the initial transient current is affected by the inductor size.

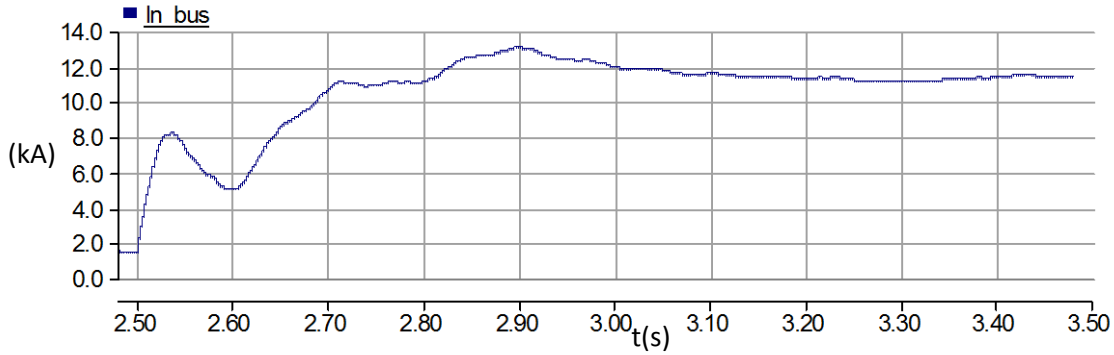

Figure 5-17 - B42 Current, Fault 0 km Down Line to Bus 2, 500 mH Inductors

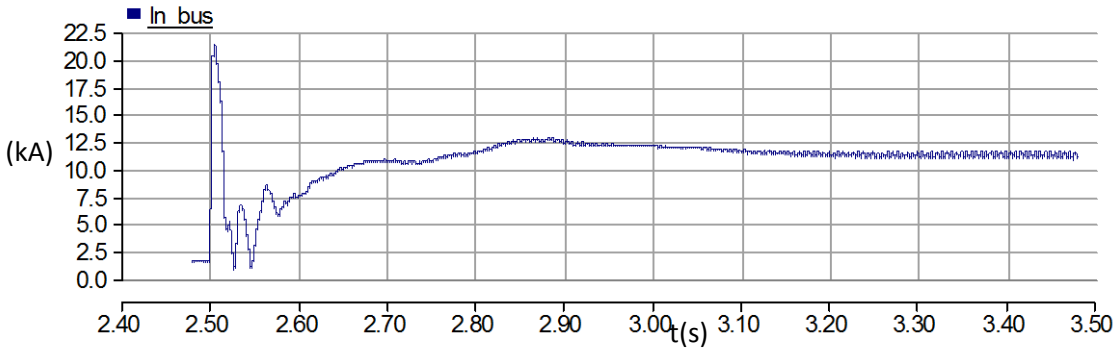

Figure 5-18 - B42 Current, Fault 0 km Down Line to Bus 2, 10 mH Inductors

Figure 5-17 and Figure 5-18 show that the fault current for a given fault with differently sized di/dt limiting inductors will resolve to the same steady state fault current. The inductors serve to limit the initial fault current rise due to the discharge of line/cable and converter capacitance.

5.2 Breaker Operation Simulations

A model of the hybrid DC breaker was implemented in PSCAD and studies were performed to

determine the impact of the arrester rating and the fault location on energy absorbed by the surge arrester component of the breaker. The impact of grid configuration on post-fault-clearing grid response is also discussed in Section 5.2.5.

5.2.1 **Implementation of Protection on the Simulated DC Grid**

In order to investigate the grid response to fault clearing after detection of a fault by the proposed protection system, the hybrid DC breaker was modeled and simulations were performed. The breaker was modeled as an ideal breaker with a time delay of 2 ms in parallel with a surge arrester. Upon detection of a fault on the segment protected by the breaker, the delay timer is started. When the breaker operates, the surge arrester conducts according to its voltage and current characteristics. Figure 5-19 shows the representation of a hybrid type breaker used for simulations. The di/dt limiting inductor was set to 100 mH.

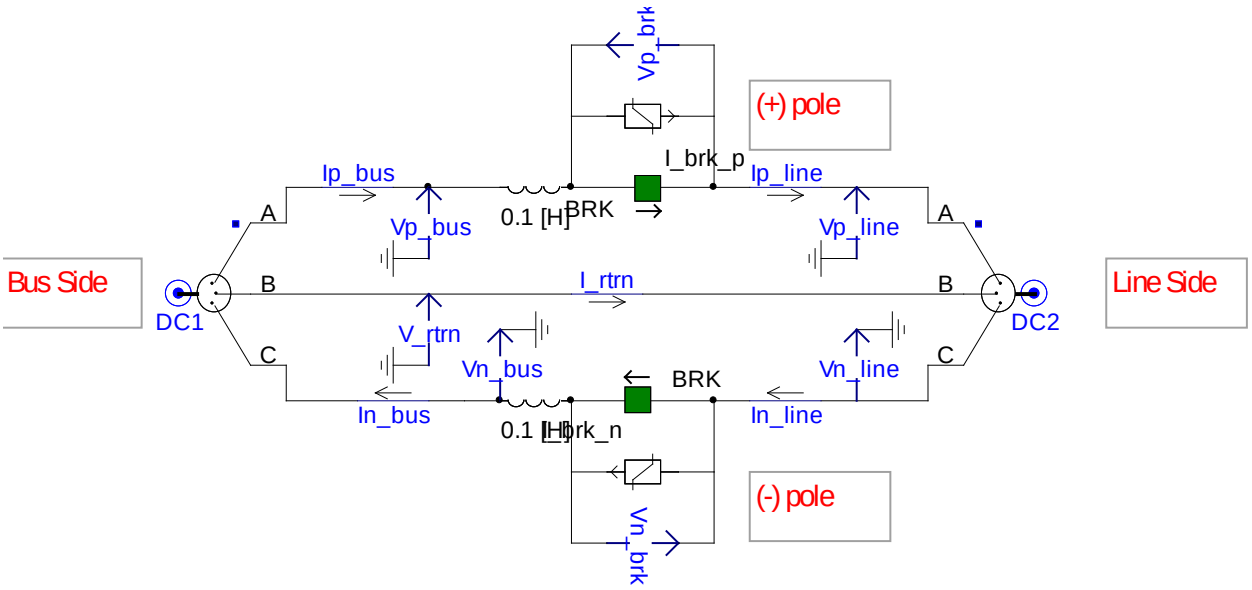

Figure 5-19 - Hybrid DC Breaker Implementation in PSCAD

Figure 5-20 shows the logic used to determine the maximum ROCOV on the line side of the breaker.

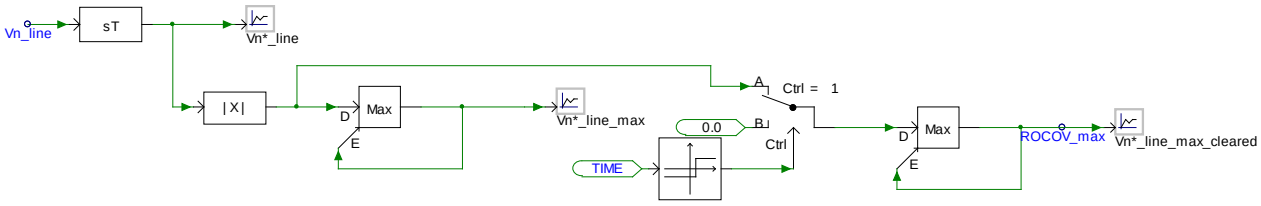

Figure 5-20 – Calculation of Maximum ROCOV in PSCAD

Figure 5-21 shows the logic used to compare the maximum ROCOV measured to the threshold 'trip point'. Any ROCOV higher than the threshold results in a trip being signalled. A delay of 2 ms represents the hybrid DC breaker operating time. Following this delay a trip signal is sent to the ideal breaker model.

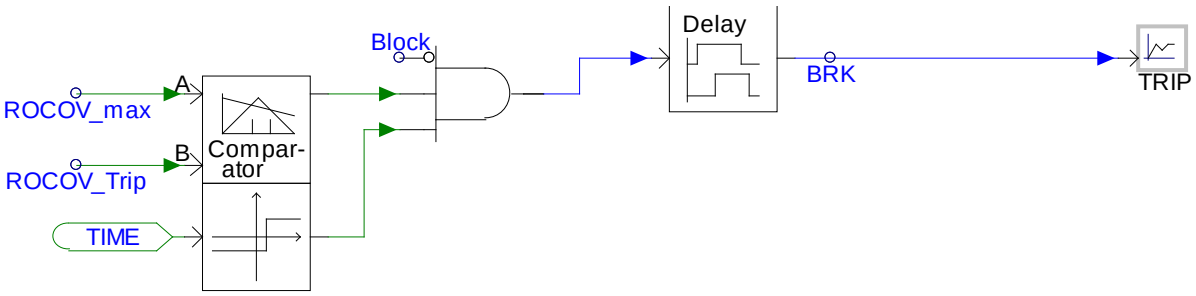

Figure 5-21 - Breaker Tripping Logic Implementation in PSCAD

When the ROCOV criterion is exceeded, a 2 ms timer is started. This delay represents the time to open the fast mechanical switch in the hybrid breaker. The auxiliary IGBT switch turns off very quickly to commutate current into the larger main IGBT. Once the mechanical switch is opened, the main IGBT switches turn off to commutate the current into the surge arrester. These IGBT turn-off times are in the range of few microseconds and are therefore ignored in the simulation. For these simulations, the breakers on both poles of the faulted segment were tripped.

5.2.2 **Arrester Rating and Arrester Energy**

Simulations were performed to study the impact of different arrester ratings on hybrid breaker fault current interruption. The three converter test grid was used. Some of these simulation results are presented in this section.

Figure 5-22 shows the operation of breaker B14 for a fault 150 km down the cable C1-4 towards bus 4. The di/dt limiting inductor value is 100 mH. The surge arrester was modeled using the AC surge arrester model available in PSCAD with default V-I characteristic and with a voltage rating of 243 kV.

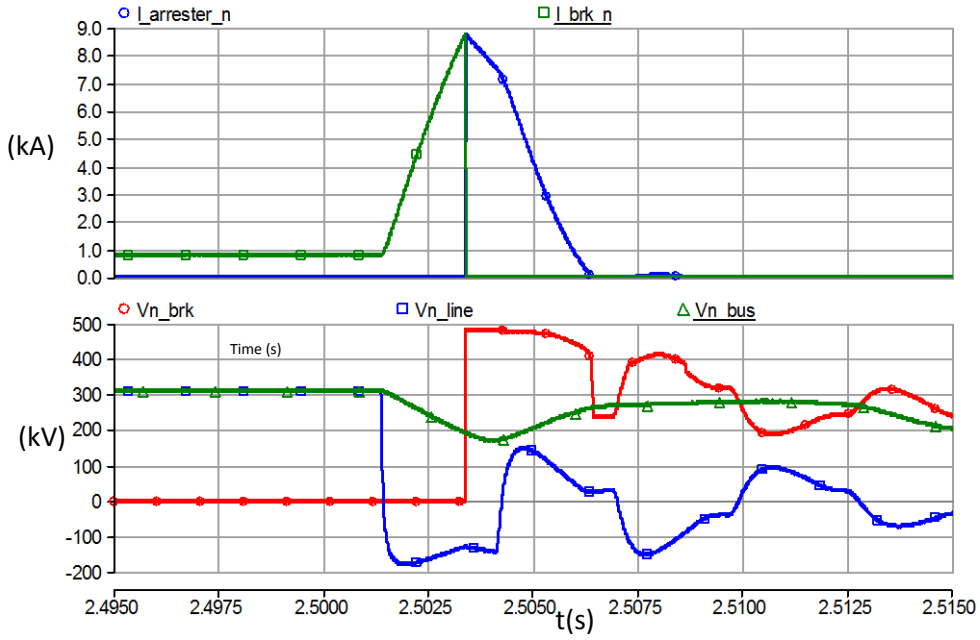

Figure 5-22 - Fault Clearing with 100 mH Inductors, Fault 150 km from B14 at Time = 2.5 seconds, Arrester set to 243 kV

The current through the breaker (green with square markers) can be seen ramping up after the fault transient reaches the breaker. After 2 ms, the breaker opens and the arrester conducts to clamp the voltage to approximately 1.5 pu of the line rating. Arrester current is shown by the blue curve with circle markers. The lower plot in Figure 5-22 shows the voltages at the bus side of the breaker (green with triangles) and the line side of the breaker (blue with squares) and the voltage across the breaker (red with circles).

The arrester needs to be selected such that it will keep the voltage across the breaker below the maximum voltage that the main breaker IGBT string can handle. A lower arrester voltage rating will result in more energy absorbed by the arrester during breaker operation.

The impact of different arrester voltage ratings can be seen in Figure 5-23 and Figure 5-24. A higher voltage rating will require a higher voltage withstand capability on the solid state component of the hybrid breaker but will result in a quicker current extinguishment.

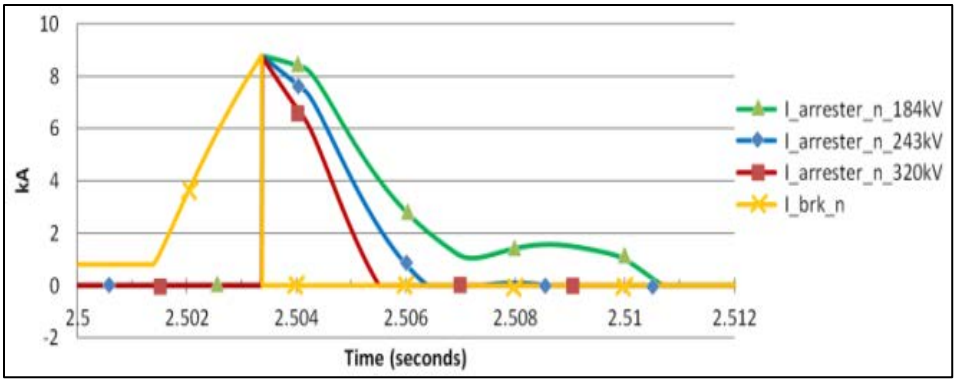

Figure 5-23 - Breaker Currents with Different Arrester Ratings (Fault at t = 2.5 s, 150 km Down Cable)

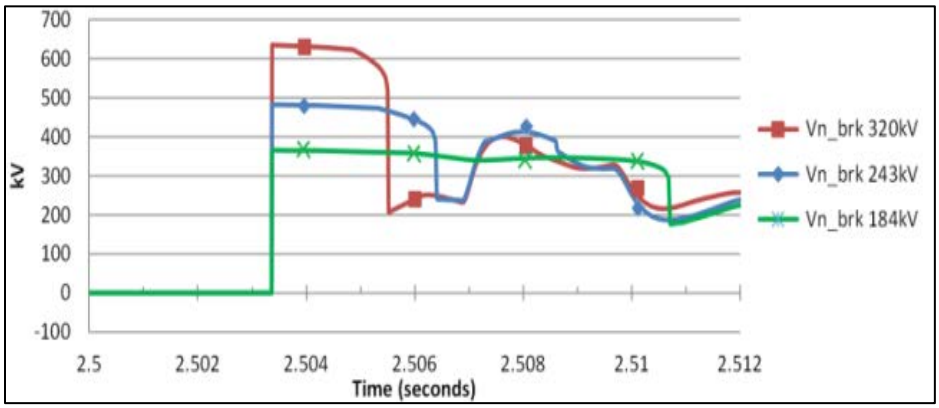

Figure 5-24 - Breaker Voltages with Different Arrester Ratings (Fault at t = 2.5 s, 150 km Down Cable)

The arrester energy results of the cases shown in Figure 5-23 and Figure 5-24 are summarized in Table 5-6.

Table 5-6 - Arrester Energy with Different Arrester Ratings

Energy Absorbed by Arrester at B14 for a given Arrester Rating (P-G Fault 150 km Down Cable, 100 mH Inductors)	
Arrester Rating	Arrester Energy (kJ)
320 kV	6386
243 kV	6659
184 kV	8309

The arrester rating impacts the energy that must be absorbed by the arrester. Typically the arrester should be sized to keep the voltage across the breaker below the maximum voltage that the large solid state component of the hybrid DC breaker can withstand.

5.2.3 Impact of Inductor Size on Arrester Ratings

The impact of inductor size on fault current and arrester energy can be seen in Figure 5-25 and Figure 5-26.

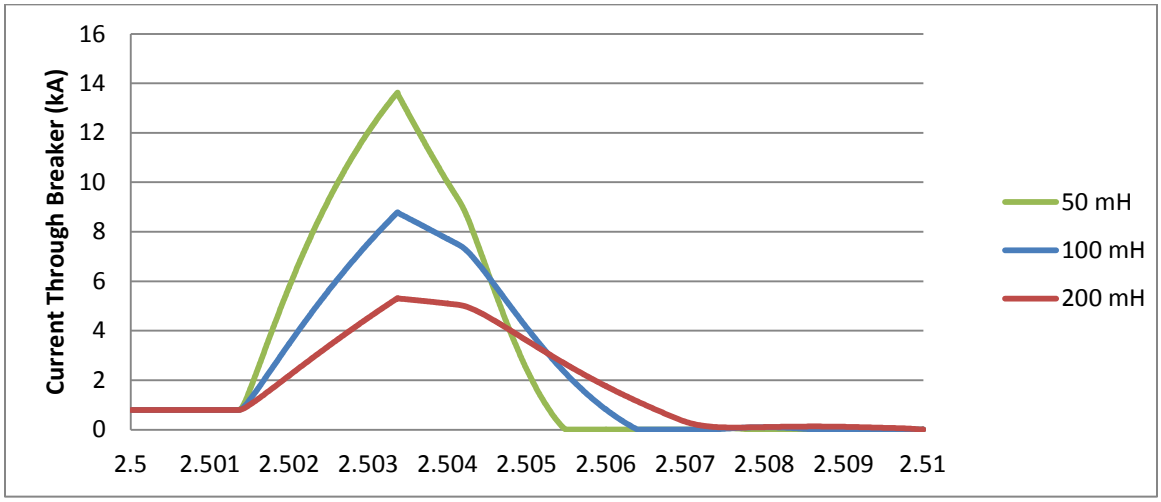

Figure 5-25 - Breaker Currents with Different Inductor Sizes (Fault at t = 2.5 s, 150 km Down Cable)

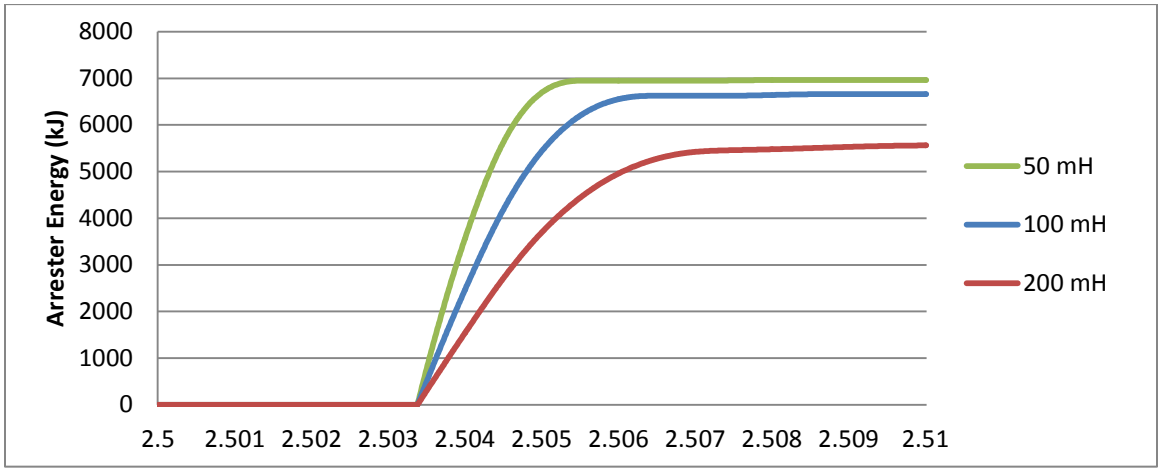

Figure 5-26 - Breaker Arrestor Energies with Different Inductor Sizes (Fault at t = 2.5 s, 150 km Down Cable)

A smaller inductor results in higher current through the breaker as well as higher arrester energy as the energy stored in the inductor is proportional to the square of the current through the inductor. A smaller inductor also results in quicker current extinction because the higher current results in the energy being absorbed faster

5.2.4 **Impact of Fault Location on Breaker Arrester Energy**

Simulations were run with ROCOV based fault detection and the hybrid breaker added to the nine converter test grid. The nine converter test grid and some of the test fault locations are shown in Figure 5-27. The results of these fault simulations are presented in this section.

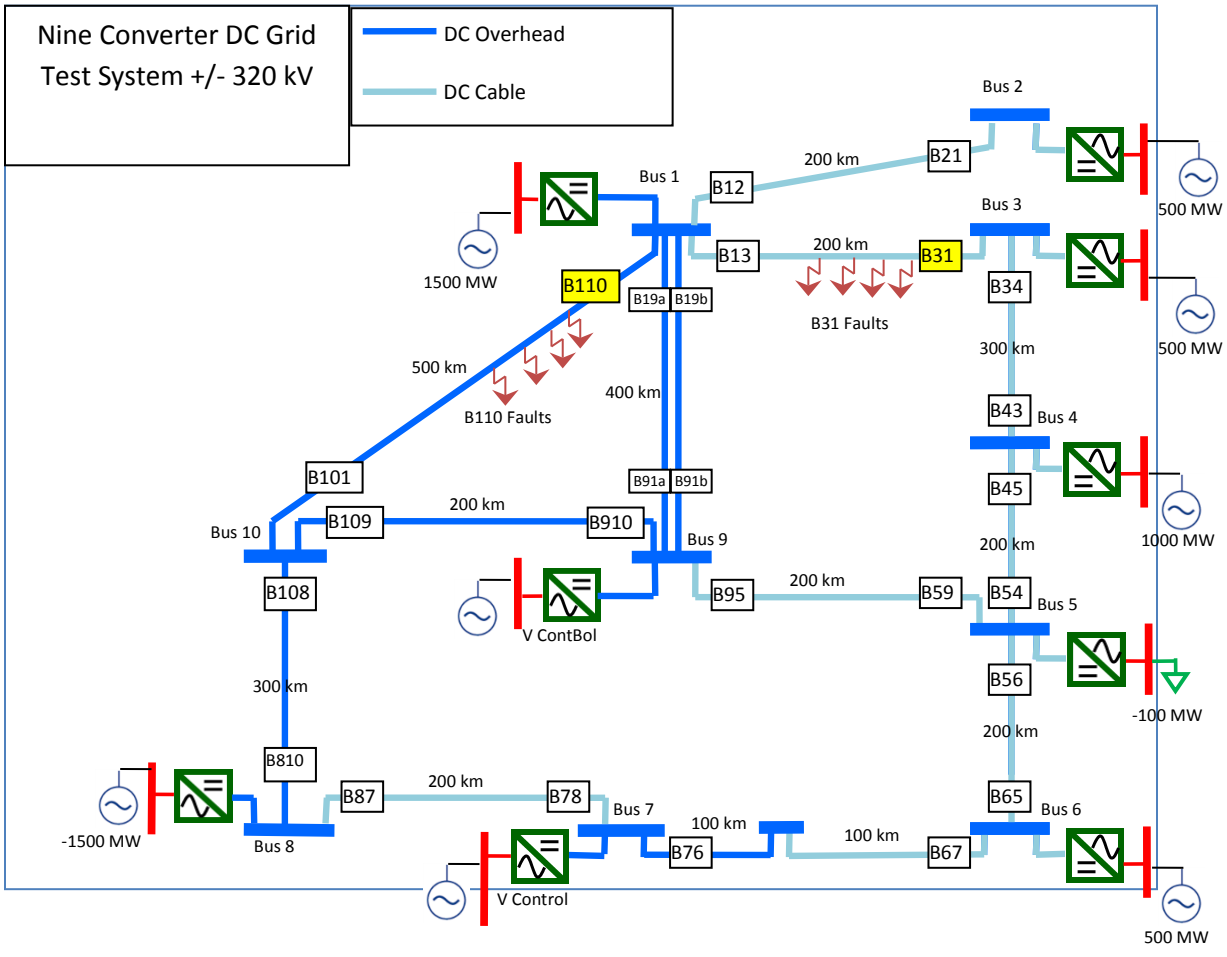

Figure 5-27 – B31 and B110 Faults on Grid

Figure 5-28 to Figure 5-31 and Table 5-7 show the values measured at B31 for faults at different locations on the cable from bus 3 to bus 1.

Figure 5-28 shows a single pole-to-ground fault on the cable from bus 3 to bus 1. The fault occurs at the 5 second mark. From 5.00 seconds until 5.002 seconds (2 milliseconds later) the current through the breaker rises. The faulted side of the breaker goes to 0 V immediately while the bus side of the breaker, separated from the fault by the di/dt limiting inductor, slowly drops from approximately 320 kV to 280 kV and then rises back up after the fault is cleared.

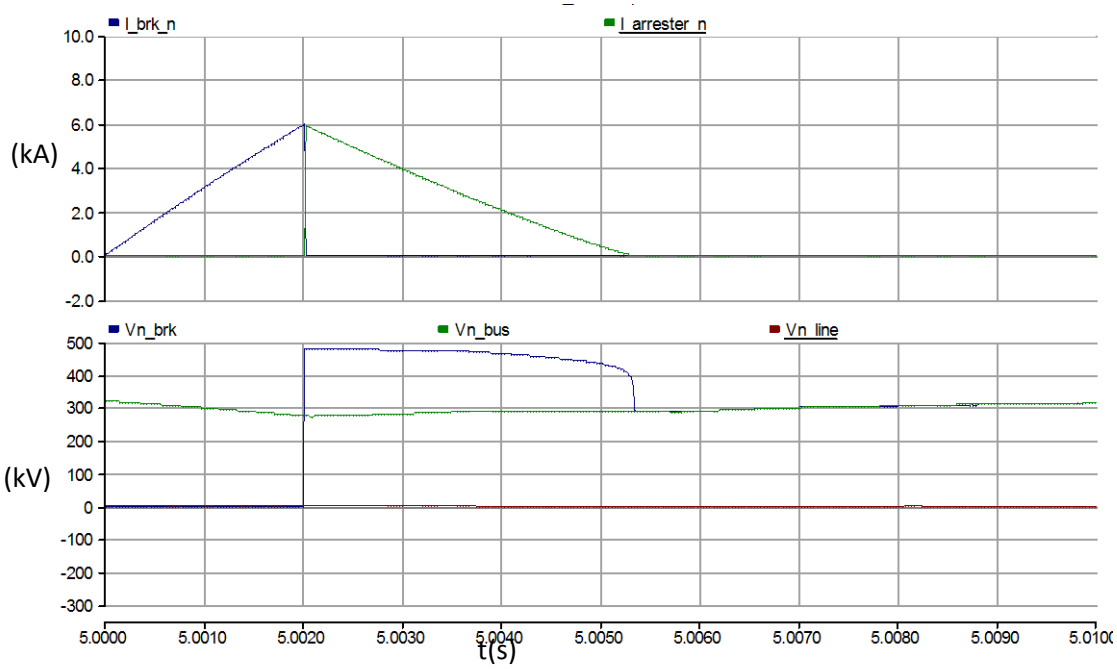

Figure 5-28 – P-G Terminal Fault Cleared by B31 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

At time = 5.002 seconds in Figure 5-28, the opening of the fast mechanical switch is complete and the large solid state component of the hybrid breaker opens. At this point the voltage across the breaker jumps to approximately 490 kV and the fault current is commutated into the surge arrester. The voltage across the breaker and the current through the surge arrester are proportional and depend on the voltage rating of the arrester. Once the energy stored in the inductor has been dissipated, the current is extinguished and the voltage across the breaker is reduced to the pole-to-ground voltage of the formerly faulted pole.

Figure 5-29 shows the same values with the fault moved 60 km down the cable. In this case it can be seen that it takes approximately 0.6 ms for the fault transient wave to travel the 60 km to B31. When the fault transient arrives at the breaker there is a voltage doubling effect when the wave reflects off of the inductor. The current rises proportionally to the voltage difference between the bus side and the line side of the breaker. When the reflected fault current wave returns to the fault and reflects back again to the breaker, the voltage on the line side of the breaker returns to close to the pre-fault voltage and the current rise slows considerably.

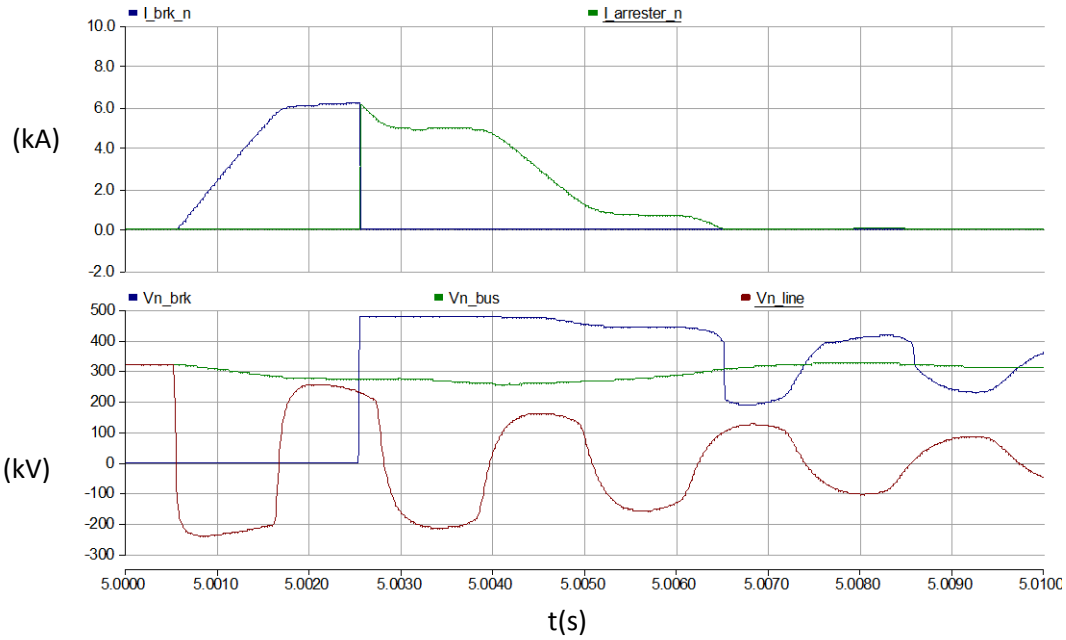

Figure 5-29 - Fault 60 km Down Cable Cleared by B31 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

In Figure 5-30 the fault is moved to 120 km down the cable from the breaker. In this case, the voltage doubling effect lasts for the entire 2 ms that it takes for the breaker to operate. As was discussed in Section 5.1.3, this should be close to the highest possible fault current that the breaker needs to interrupt.

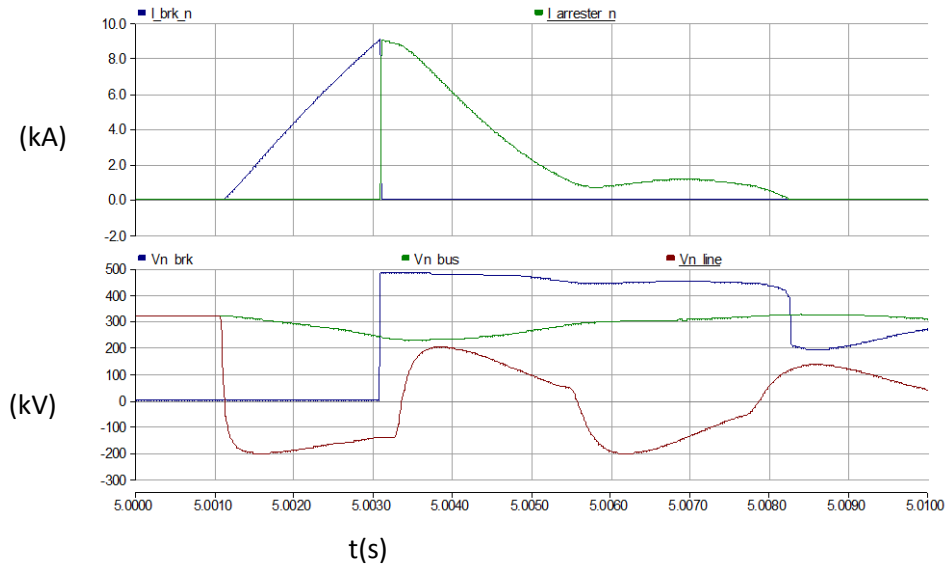

Figure 5-30 - Fault 120 km Down Cable Cleared by B31 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

In Figure 5-31 the fault is moved out to 200 km from breaker B31.

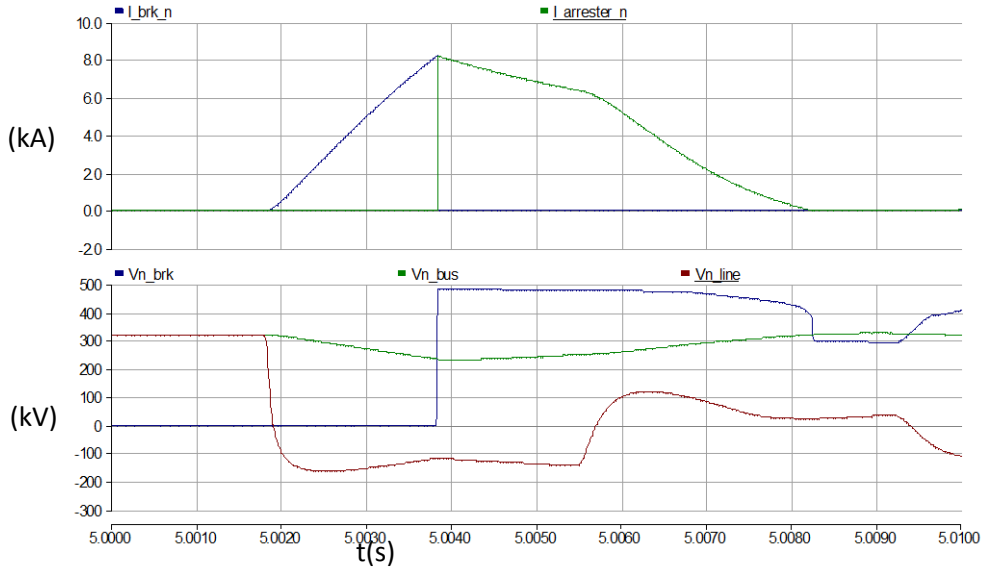

Figure 5-31 - Fault 200 km Down Cable Cleared by B31 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

Comparing these results with those from Figure 5-28, Figure 5-29 and Figure 5-30, it can be seen that at the moment when the large solid state component of the breaker operates (2 ms after the fault transient wave arrives at the breaker), the current is highest when the fault is 120 km away from the breaker. This is close to the distance that the fault generated traveling wave

travels within half of the operating time of the breaker.

Table 5-7 lists some details from the faults simulated in Figure 5-28 to Figure 5-31. The detection time is the time from fault occurrence to when the ROCOV fault detection logic detects the fault and mostly represents the travel time from the fault location to the breaker. The interruption time is the detection time plus the 2 ms delay for the mechanical switch to operate. The current zero time is the time from the fault occurrence to the point when all current through the arrester is extinguished. This is highest for pole-to-pole faults 120 km away from the breaker as is the maximum current through the breaker. The maximum voltage across the breaker corresponds to the current being interrupted. The energy absorbed by the arrester is highest for the faults 200 km away from the breaker. This is not the case with the highest current but the inductance of the additional length of cable draws additional current through the arrester.

Table 5-7 - Results for Cable Faults Interrupted by B31

Fault Type	Distance to Fault (km)	Detection Time	Interruption Time	Current Zero Time	Max Current (kA)	Max Voltage Across Breaker (kV)	Energy Absorbed by Arrester (kJ)
P-G	0 km	0 ms	2 ms	5.29 ms	5.93 kA	478 kV	4342 kJ
P-P	0 km	0 ms	2 ms	5.73 ms	6.23 kA	478.6 kV	5280 kJ
P-G	60 km	.55 ms	2.55 ms	6.47 ms	6.21 kA	478.4 kV	5382 kJ
P-P	60 km	0.54 ms	2.54 ms	6.78 ms	6.486 kA	478.78 kV	6759 kJ
P-G	120 km	1.08 ms	3.08 ms	8.22 ms	8.72 kA	482.9 kV	6837 kJ
P-P	120 km	1.075 ms	3.075 ms	8.38 ms	9.37 kA	483.5 kV	8811 kJ
P-G	200 km	1.81 ms	3.81 ms	8.17 ms	8.18 kA	481.6 kV	9543 kJ
P-P	200 km	1.814 ms	3.814 ms	8.35 ms	8.595 kA	482.4 kV	11498 kJ

Fault studies were repeated on the overhead line from bus 1 to bus 10 of the nine converter grid. Figure 5-32 shows the measurements at breaker B110 for a P-G fault at the breaker terminals.

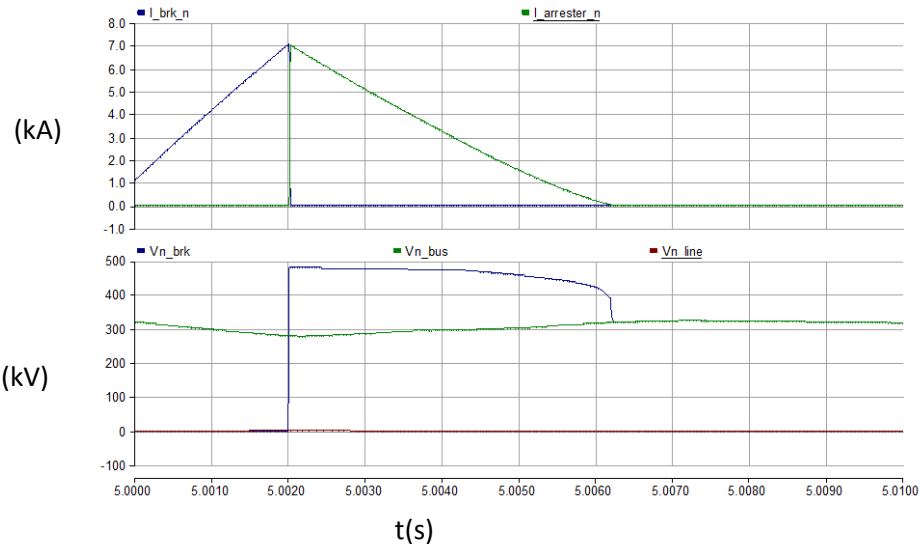

Figure 5-32 - Terminal Fault Cleared by B110 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

In Figure 5-33 the fault is moved 20 km down the line. The reflections of the traveling fault transient wave can be seen clearly in the line side voltage plot. It can be seen that moving 20 km down the line reduces the maximum current but increases the time to zero current. This is caused by the increased inductance of the line between the breaker and the fault.

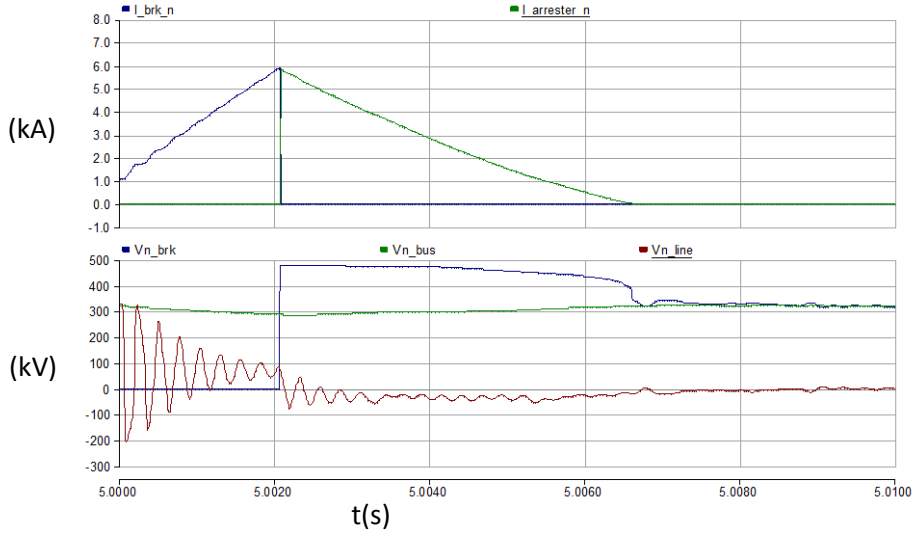

Figure 5-33 - Fault 20 km down Overhead Line Cleared by B110 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

In Figure 5-34 the fault is moved to 100 km down the line from the breaker. Moving the fault 100 km down the line further decreases maximum fault current and arrester energy and increases the time to zero current.

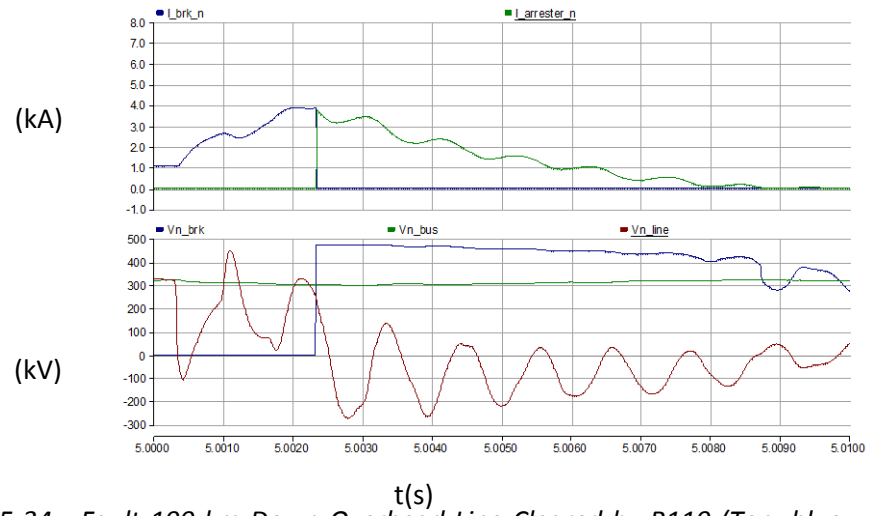

Figure 5-34 - Fault 100 km Down Overhead Line Cleared by B110 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

It was shown earlier that, for cables, the current, breaker voltage and current zero times were highest when the distance to the fault was such that the reflection of the fault from the breaker back to the fault and back to the breaker coincided with the opening time of 2 ms. The travel time of the fault wave on the overhead line from bus 1 to bus 10 is approximately 0.32 ms per 100 km so a fault location of 320 km away from the breaker was chosen to determine if the same effect occurs on the overhead line section. The simulation results shown in Figure 5-35 indicate that the phenomenon does not affect the current due to faults in overhead line segments as in the case of cables.

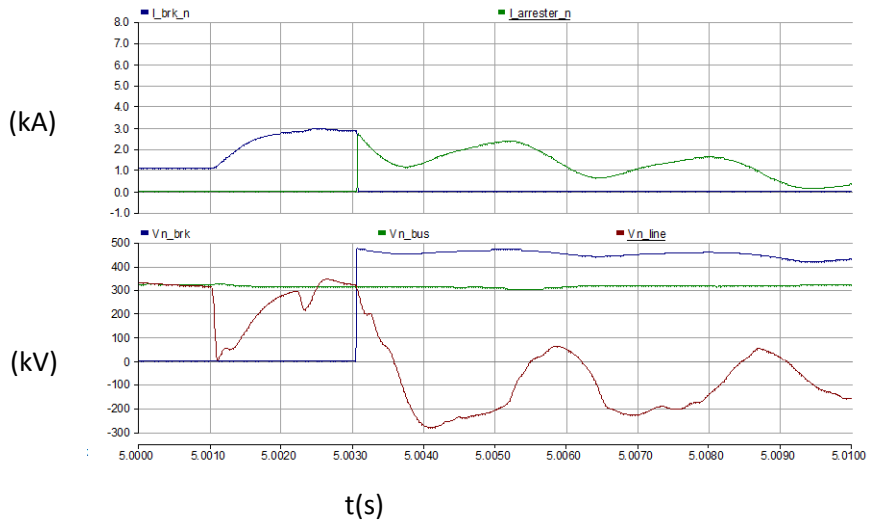

Figure 5-35 - Fault 320 km Down Overhead Line Cleared by B110 (Top: blue – current through IGBT, green – current through arrester; Bottom: blue – negative pole, green – positive pole, brown – metallic return)

Comparing the plots for the fault on the overhead line 320 km away from B110 (Figure 5-35) with the corresponding plots for the fault on the cable 120 km away from B31 (Figure 5-30), it can be seen that the voltage wave doubling effect does not have as much impact in the overhead line segments as it did in the cable segments. This is due to the higher impedance to capacitance ratio in the overhead line compared to the cable. The lower capacitance makes the surge very short. The current through the inductor raises the line side voltage quicker the less capacitance there is, leading to a decrease in the voltage across the inductor and a decrease in the current rate of rise. Another significant effect is attenuation of the traveling wave caused by line resistance when traveling a longer distance.

For faults on overhead line segments, the simulation results indicate that the highest fault currents and recovery voltages occur for faults closer to the breaker. The arrester energies do not scale with distance as consistently. These results are all tabulated in Table 5-8.

Table 5-8 - Results for Overhead Line Faults Interrupted by B110

Fault Type	Distance to Fault (km)	Detection Time	Interruption Time	Current Zero Time	Max Current (kA)	Max Voltage Across Breaker (kV)	Energy Absorbed by Arrester (kJ)
P-G	0 km	0 ms	2 ms	6.2 ms	7.03 kA	479.8 kV	6339 kJ
P-P	0 km	0 ms	2 ms	6.51 ms	7.408 kA	480.5 kV	7608 kJ
P-G	20 km	0.06 ms	2.06 ms	6.57 ms	5.83 kA	478 kV	5446 kJ
P-P	20 km	0.057 ms	2.057 ms	6.93 ms	6.68 kA	479.19 kV	7296 kJ
P-G	100 km	0.32 ms	2.32 ms	8.73 ms	3.87 kA	474.78 kV	4268 kJ
P-P	100 km	0.32 ms	2.32 ms	9.8 ms	4.995 kA	476.4 kV	6997 kJ
P-G	320 km	1.05 ms	3.05 ms	11.9 ms	2.93 kA	472 kV	4670 kJ
P-P	320 km	1.048 ms	3.048 ms	14.8 ms	3.786 kA	474.4 kV	7869 kJ

5.2.5 **Post-Fault Service Interruption**

Fault clearing simulations performed with the nine converter test grid resulted in the system clearing the fault and riding through with no significant interruptions to the AC interconnections. The impact of faults on the three converter test system was more significant.

With a star configuration as seen in Figure 5-36, the loss of any transmission segment will result

in the loss of an AC/DC converter. The largest interruption in power flow to and/or from the AC system in this case will be the time necessary for the appropriate converters to readjust their power levels to keep the power flow balanced and the voltage within tolerances.

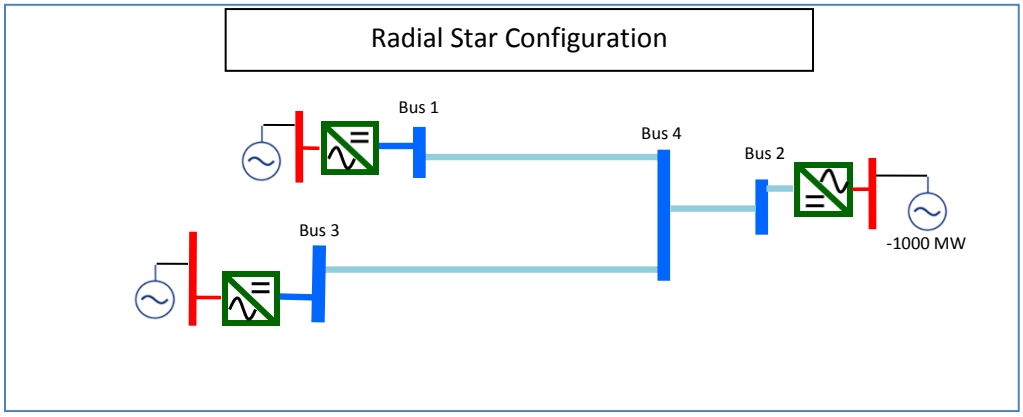

Figure 5-36 - Star Configuration

With the ring configuration shown in Figure 5-37, any single line or cable segment can be lost without the immediate loss of a converter. Transmission element thermal loading may require some re-dispatch of power in the medium to long term. In the immediate to short term, however, the loss of any individual transmission element should not result in any interruption in power transmission.

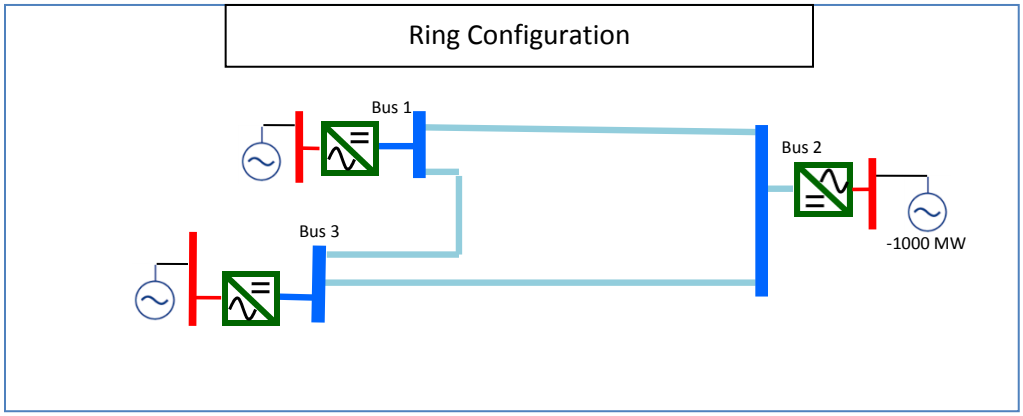

Figure 5-37 - Ring Configuration

All converters in the grid should at any given time have set points assigned to them by a centralized controller dictating their power flow set-point across a range of voltages. No central controller/operator involvement should be necessary for the grid to adjust to maintain voltages

following the loss of any one element. These adjustments may still take time and result in voltage and service interruptions as the speed of these adjustments may be limited by controller stability concerns. Models used for simulation included a MW/s limitation on the speed of these controls.

Studies would need to be run to determine the flexibility of all the connections to the AC system with regard to accommodating quick voltage control actions and longer steady state power flow needs. The DC grid should be able to lose one converter (n-1) without other non-radial tripping.

5.3 Concluding Remarks

This chapter presented the results of studies performed to analyze the impact of di/dt limiting inductors on fault current and the process of sizing these inductors. The simulation results demonstrated that the rate of rise of fault current can be limited by increasing the size of the di/dt limiting inductors placed in series with each DC breaker. These inductors should be sized such that the fault current through a breaker does not exceed the maximum breakable current within the breaker operating time. The inductors should be sized based on the fault type and location which would provide the fastest current rise within the breaker operating time. For the cables modelled, the worst case fault location was the distance down the line that the fault transient wave can travel in half of the breaker operating time. For the lines modelled, the worst case fault location was at the terminals.

The hybrid DC breaker was implemented in PSCAD and the results of some studies including protective breaker action were reported. A higher surge arrester MCOV voltage rating results in lower arrester energy absorbed and less time for the current to extinguish but a higher voltage. Arresters should be sized for the highest voltage that adequately protects all equipment, including the large solid state component of the hybrid HVDC breaker.

The impact of fault location on breaker performance was investigated. For cables, the highest fault current, fault clearing time and voltage across the arrester occurred with the pole-to-pole fault 120 km down the cable. The highest arrester energy, on the other hand, occurred for the fault farther down the cable (200 km in this case). This is not the case with the highest current but the inductance of the additional length of cable draws additional current through the arrester. Further study should be performed to determine the highest possible arrester energy

for all possible faults on the protected segment before arresters are sized.

For the overhead lines studied, the simulation results indicate that the highest fault currents and recovery voltages occur for faults close to the breaker. The arrester energies did not scale consistently with distance but were generally higher with pole-to-pole faults than with pole-to-ground faults.

6 Conclusions and Further Research Plans

This thesis report reviewed the state of the art of DC circuit breakers and identified critical HVDC grid protection system goals. The following have been proposed: (i) a method to locate the faulted line elements using local measurement within a very short time, (ii) a strategy to select protection settings, and (iii) a method to size the di/dt limiting series inductors to enable protection discrimination while meeting the limitations of the DC circuit breakers. Two DC grids were modeled in PSCAD. Fault simulations were run and the proposed protection methods were implemented and evaluated. The results have been presented and discussed. Based on these results, the conclusions in Section 6.1 are presented. DC grids are a relatively new concept. Whatever shape future DC grid projects take, there will be much work to do to determine what the protection systems will look like. A few ideas for further research are listed in Section 6.2.

6.1 Conclusions

The overall objective of this research was to understand the behaviour of an HVDC grid during DC side faults and develop a method of detecting, discriminating and interrupting faults within an adequate time frame. This objective was achieved and the following conclusions were arrived at through the studies reported in this thesis.

6.1.1 Fault Response Options and Protection Goals

Chapter 2 discussed fault current behavior in a DC grid, analyzed the pros and cons of different options for responding to DC line faults, and presented the state-of-the-art of DC circuit breakers. Based on this discussion, a set of protection system goals was outlined. It was proposed to use DC circuit breakers in a manner similar to how AC circuit breakers are used. Breakers would be placed at the ends of all line or cable segments. Fault currents would be interrupted and the faulted segment isolated without interrupting the operation of any of the converters or discharging the remote sections of the grid.

6.1.2 **Fault Currents in a DC Grid**

In Chapter 3, two DC grid models were implemented in PSCAD and several fault scenarios were simulated. The simulation results were used to gain an understanding of how faults affect voltages and currents in DC grids. Simulations showed that without series inductors to limit the rate of rise, fault currents can potentially rise above the capability of currently proposed hybrid DC circuit breakers in a sub-millisecond time interval. In addition, the simulations showed that steady state fault currents are also beyond the capability of hybrid DC circuit breakers.

6.1.3 **Fault Detection and Discrimination**

In Chapter 4, a method for a breaker to quickly determine if there is a fault on the transmission segment that it is protecting using local ROCOV measurements was proposed. Simulation studies were performed to test the proposed concepts and the results showed that the proposed protection concept can successfully detect and discriminate the faults on a DC grid, provided that di/dt limiting inductors are connected in series with each breaker. A process for setting protection thresholds was discussed and the results of the process applied to the two different test grids were documented. Because the grid is effectively segmented for the high frequency fault transients by the di/dt limiting inductors, the ROCOV measured at the line side of the inductor can be used to quickly determine whether there is a fault on the immediate line segment. There is no time delay involved as the measurements are local. Thus the proposed protection scheme is a simple yet very practical method for protecting HVDC grids from line and bus faults, without interrupting the whole grid. When setting ROCOV thresholds for discriminating against bus faults and faults on the adjacent lines, it is necessary to determine the minimum ROCOV that the breaker will see for a fault on the protected segment and the maximum ROCOV that the breaker will see for a fault that is not on the protected segment.

6.1.4 **Inductor and Breaker Rating**

Chapter 5 presented the results of studies performed to analyze the impact of di/dt limiting inductors on fault current and the process of sizing these inductors. It is feasible to use a hybrid HVDC breaker to protect a DC grid from pole-to-ground and pole-to-pole line and cable faults.

Use of series di/dt limiting inductors is necessary to limit the fault currents to a level below the rated breaker current within the time required for the breaker to operate.

The simulation results demonstrated that the rate of rise of fault current can be limited by increasing the size of the di/dt limiting inductors placed in series with each DC breaker. These inductors should be sized such that the fault current through a breaker does not exceed the maximum breakable current within the breaker operating time. The inductors should be sized based on the fault type and location which would provide the fastest current rise within the breaker operating time. The highest rate of rise of fault current for a cable fault will occur for a pole-to-pole fault at a critical distance away from the cable terminal. This critical distance is equal to half of the distance travelled by the fault transient during the breaker operating time. For the overhead lines, the worst case fault location was at the terminals.

The hybrid DC breaker was implemented in PSCAD and the results of some studies, including protective breaker action, were reported. A higher surge arrester MCOV rating results in higher voltage but lower arrester energy and less time for the current to extinguish. Arresters should be sized for the highest voltage that adequately protects all equipment, including the large solid state component of the hybrid HVDC breaker.

The impact of different inductor sizes on breaker current and arrester energy was investigated. A smaller inductor results in higher current through the breaker for a given operating time as well as higher arrester energy, as the energy stored in the inductor is proportional to the square of the current through the inductor. A smaller inductor also results in a quicker current extinction as the higher current results in faster arrester energy absorption.

The impact of fault location on breaker performance was investigated. For cables, the highest fault current, fault clearing time and voltage across the arrester occurred with the pole-to-pole fault at the critical distance from the breaker. The highest arrester energy, on the other hand, occurred for the fault farther down the cable.

For the overhead lines studied, the simulation results indicate that the highest fault currents and recovery voltages occur for faults close to the breaker. The arrester energies did not scale consistently with distance but were generally higher with pole-to-pole faults than with pole-to-ground faults.

6.2 **Ideas for Further Research**

The areas for further study with regard to DC grid protection are just about unlimited. This technology is in its infancy. Several specific topics that are important to extend the concepts developed in this thesis are:

-The protection backups discussed in Section 4.1.2 were not studied in depth. There is room for research into and study of any of these ideas.

-A method of detecting faults on the neutral metallic return conductors introduced in Section 4.1.3 could be analyzed for feasibility.

-It would be interesting to implement a zonal protection system as mentioned in Section 4.1.1. It may be that the margins between maximum ROCOV on remote faults and the minimum ROCOV on faults in the protected system are a lot smaller. The zones would need to be sized appropriately.

-The mid-term to long-term response of the grid to the fault and the fault clearing was not studied. Only the fault clearing was evaluated. The grid should be able to survive any single fault and the subsequent clearing for a period of time (mid-term) before central control action is necessary to control power flow to prevent thermal overloads (long-term). It would be good to do a more in-depth study to determine if the local controls are sufficient to maintain mid-term stability. The impact on stability of tripping both poles for a P-G fault vs tripping only the faulted pole and operating in an unbalanced configuration should be investigated.

Finally, ungrounded monopole DC grids could be protected in a number of different ways. This would be an interesting topic for further simulation studies.

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