Comparison of Firing Control Systems for HVDC Stations Connected to Weak AC Systems

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in Electrical Engineering

by
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COMPARISON OF FIRING CONTROL SYSTEMS
FOR HVDC STATIONS CONNECTED TO
WEAK AC SYSTEMS

BY

KETKI SHAH

A Thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Abstract

The dynamic performance of the High Voltage Direct Current (HVDC) transmission systems connected to weak ac systems depends strongly upon the control systems of the dc link. Some of the complications that arise are the high risk of commutation failure, possible voltage instability and long recovery times to disturbances.

In this thesis three suitable control systems are studied and compared by subjecting them to various operating conditions and system faults. The testing is done on a weak ac transmission system. All the work is carried out using EMTDC simulation.

Acknowledgements

I wish to thank Dr. A.M. Gole for his guidance, encouragement and patience throughout the course of this thesis.

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Chapter 1

INTRODUCTION

1 .1 BACKGROUND

A phase locked loop (PLL) can be used to recover a signal deeply imbedded in noise and harmonic distortions. The PLL generates a "clean" waveform that is in phase with the fundamental component of the input waveform.

One of the earliest utilizations of PLL techniques was for the synchronization of radio signals in the early 1930's. It became more widely used with the advent of television – for the horizontal and vertical synchronization of signals. Nowadays PLLs are also used for tracking very weak satellite signals.

In power systems applications the signal is crucial to the operation of the the controls to a converter station. It is important to fire the valves of a dc converter in exact synchronism with the ac system voltages which can often be distorted. A phase locked loop can be used to accurately lock on to the fundamental of the ac waveform and can thus be used as the reference for deriving the firing pulses. The accuracy of the PLL in doing its job facilitates the minimization of reactive power required and also helps overcome the susceptibility to harmonic instability by weak ac systems and recovery from faults.

1 .2 SCOPE OF THESIS

The intent of this thesis is to briefly discuss PLL theory and then consider its application to the control of converter stations.

At the converter station the conversion of ac to dc, or vice versa, is achieved through a pattern of thyristor firing. This systematic on/off scheme for the thyristors is regulated by a firing angle, which is generated as part of the controls of the station. Not only is the determination of this angle partially dependent on the actual incoming signal, but its firing also depends on the accuracy of the measurement of this signal. The less corrupted the waveform, the greater the control scheme's reliability and effectiveness. This is the job of the PLL – to deliver this accurate and ideal signal.

There are many ways to implement a PLL, in both analog and digital realizations [1,2]. One common application of PLLs in converter stations is to use it to deliver a train of pulses to fire the thyristors at a frequency exactly equal to the input signal frequency. So, regardless of any noise, harmonics or disturbances, the speed and accuracy of the PLL determines the dynamic and steady–state operation of the converter station. The PLL is a feedback loop and the derivation of this feedback differentiates various PLLs. Three different simulated control loops are studied and compared in this thesis. The first one is referred to as a pulse frequency controller [3,4]. In this loop any change is translated into a change in the actual frequency of the pulses. The second one is similar, but the change has a primary effect on the the phase of the pulses, hence it is referred to as a pulse phase controller [1]. These two are the more traditional control loops, while the third and last one considered in this thesis is a new application of the dqz transformation on a pulse frequency controller [5,6]. This transformation involves converting the three–phase input, which means three values are needed to represent the waveform at each instant, to a two–phase quantity which still retains the relevant information needed. The dqz transformation has already been used in machine control and can only be considered a novel approach with regards to converter control. This transformation has superior immunity to disturbances and harmonic distortion on the input, so it is ideal for incorporation in a PLL.

These three control loops are imbedded into the controls of a simulated weak hvdc system to evaluate their performance. One drawback of weak systems is the fact that it is more susceptible to voltage instability at the ac bus, therefore making the job of the PLL more demanding. Complications that might arise are the loss of synchronizing voltages, the high risk of commutation failure and long recovery times of the system to any faults on the line. We subject the system to various operating disturbances to test their responses, and we compare the results of the three control loops under consideration.

The simulation package used for this thesis is EMTDC, an electromagnetic simulation transient analysis program designed in Manitoba [7].

Chapter 2

CONTROL OF CONVERTERS

2 .1 INTRODUCTION

Converters are used to transform the ac quantities to dc quantities (this mode referred to as rectification), or vice versa (referred to as inversion). They consist of an arrangement of switches which are periodically fired on and off. The dc voltage, for example, is obtained by switching the proper ac phase at the appropriate time. The firing or turn on instant is important and incorrect firing can result in misfiring and the generation of uncharacteristic harmonics into the system. Since the firing is dependent on the incoming waveforms, this task is further complicated when they are distorted or fluctuating. This is where a PLL, which is capable of synthesizing the idealized version of its input, can play a major role in the converter controls.

2 .2 CONTROLS OF A DC SYSTEM

Figure 2 .1 shows a simplified dc system with two converters, one located at each end. At the sending end there is a rectifier which converts the ac to dc. The opposite is done by the inverter, situated at the receiving end.

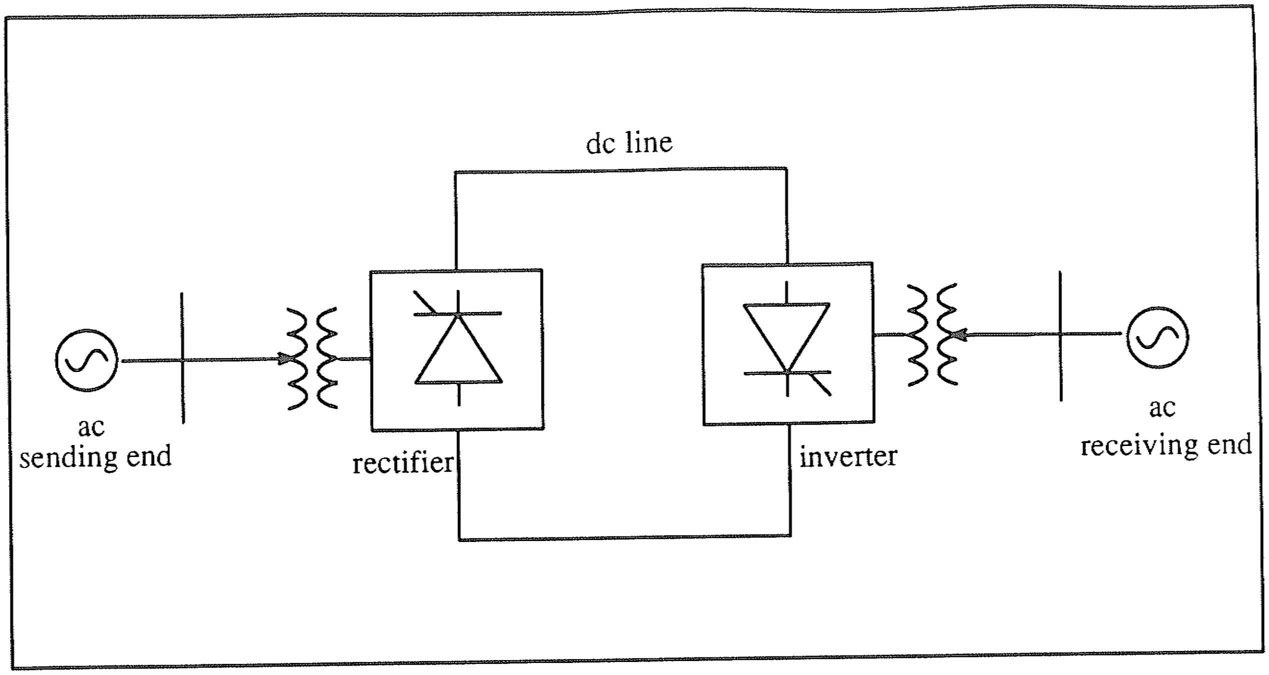

Figure 2 .1 : Line Representation of a DC System

The dc line is normally operated at its rated voltage for minimum power loss, and therefore to keep it constant the dc current is the quantity used to deliver the rated voltage. The load at the receiving end determines the required current in the dc line to meet the required demand. Though the controls of a converter regulate this current, it is only feasible for one of the converters, either the rectifier or inverter, to be in charge of this current control. To make best utilization of the line and have the least total reactive power compensation, this task is usually assumed by the rectifier. The other form of control, designated to the inverter, is constant extinction angle control and is necessary to keep the inverter firing angle at an optimum value. The characteristics of the rectifier and inverter can be seen in Figure 2 .2 , the operating point being the intersection of the two curves [8]. Note that these are the idealized basic characteristics. Various other control modes are superposed on this, such as current error control or voltage dependent current limits, which are not presented here. Similarly, completely different philosophies are sometimes used – such as voltage control on the inverter, etc.

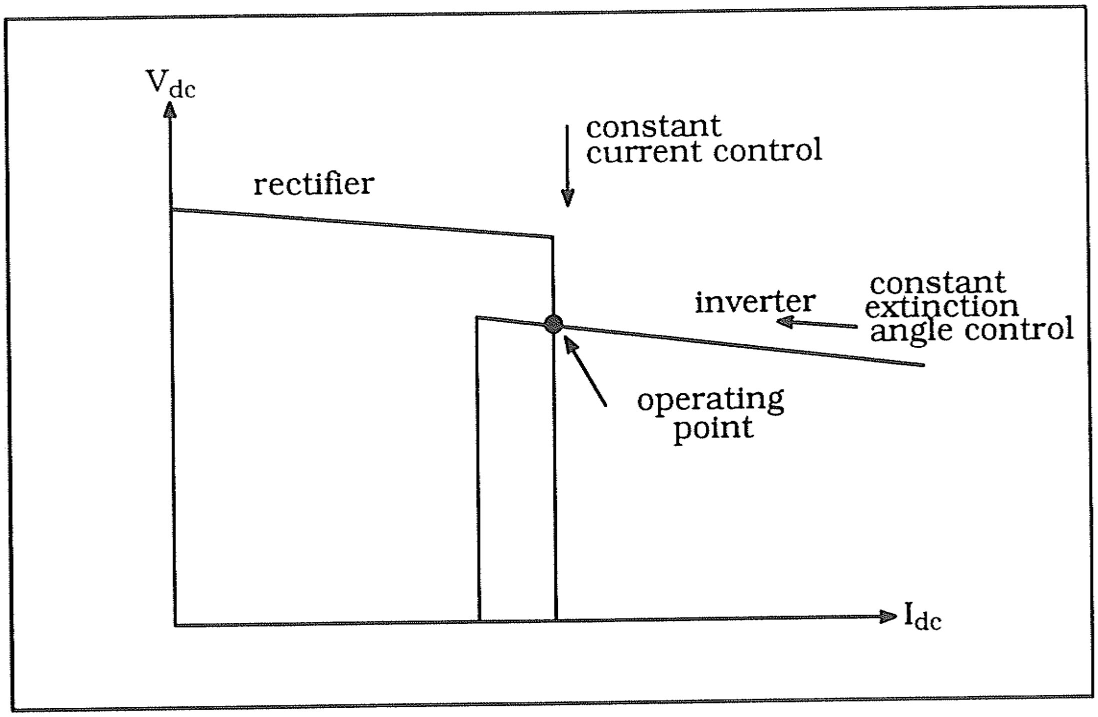

Figure 2 .2 : Characteristics of a Rectifier and Inverter

2 .3 FIRING CONTROL

The objective of the firing angle controls of a converter station is to regulate the firing angle. This angle is what makes possible the two modes of control described in section 2 .2 . The dc current in the line is actually determined by the firing angle, so current control is basically a matter of controlling this angle. The firing of a thyristor has a certain permissible time period and firing after this point causes a misfire, and commutation failure. Inversion requires a larger firing angle and is therefore susceptible to this problem.

After firing a thyristor there is an overlap angle, the time required for commutation to actually occur, and the period after this is defined as the extinction angle. It is important to note that the overlap angle is a function of the dc current, and is not a set definite value. This is why the extinction angle is a better and more important quantity to measure in an inverter as opposed to the firing angle. By keeping this angle large enough there is safety margin to avoid possible commutation failures. But it is also desirable to have as low an extinction angle as possible in terms of minimizing the total reactive power consumption. The need for a compromise between these two issues suggests the suitability of the converter for extinction angle control.

Along with delivering the load requirement and reducing the consumed reactive power, another important goal of the firing controls is to minimize the voltage drops at the ac terminals of the converter as its loading changes. This last item becomes more important when talking about weak ac systems, which exhibit a greater tendency towards this behavior.

2 .4 CHARACTERIZING A WEAK AC SYSTEM

The short circuit ratio (SCR) is often used as an indication of the strength of the ac/dc system. It looks at the system impedance and is defined as the ratio of the short circuit MVA at the ac busbar with the dc blocked, to the dc rated power taken from the same busbar.

$$SCR = \frac{\text{Short Circuit MVA}}{\text{HVDC Power}}$$

The SCR can also be defined as the ac system Thevenin admittance expressed in per unit of dc power. If filters are taken into account the effective short circuit ratio, ESCR, is obtained instead.

$$\text{ESCR} = \frac{\text{Short Circuit MVA} - \text{Filter MVA}}{\text{HVDC Power}}$$

The SCR is a reflection of the strength of the system. If the SCR is low the system is said to be weak, and conversely, if the SCR is high then the system is considered strong. A weak ac system has a larger voltage fluctuation of the ac bus for variation in the converter load. There is also more susceptibility to harmonic distortion. Generally a system with SCR below three is considered weak, while anything above three is considered to be a strong system. The ESCR tells more about a system's steady state operation and its susceptibility to overvoltages.

The controls of any converter station use the incoming signal as a reference for firing the thyristors. Once the controls of a converter have determined the desired firing angle, the firing pulse must be issued at the appropriate phase angle after the the reference signal, in this case the thyristor valve's voltage zero crossing. If there are variations in it, or it is easily disturbed, then any measurements or controls depending on this waveform are also affected. This is a greater problem in the case of an inverter because, in the course of even a relatively small variation, the angle will be too small and result in commutation failure. Depending on the controls and other existing conditions, this could lead to repeated or sustained commutation failures.

2 .5 TYPICAL FIRING CONTROLS IN CONVERTERS

The first hvdc converters used individual phase control to fire the thyristors. This involved determining the firing angle desired for each valve and then either firing at the voltage level corresponding to this angle or after the appropriate interval following the current zero crossing. In Figure 2 .3 we can see how harmonic distortion can result in incorrect firing using the first level detection method. From the second graph in Figure 2 .3 we can see how a frequency shift in the incoming waveform will result in inaccurate firing using the voltage crossing as a reference – the angle is no longer represented by the same time interval.

In rectification the firing angle is, by conventional theory, determined by the required dc current. For inversion the angle for safe and efficient commutation is often predicted based on the information derived from the signal waveform. It is apparent that both this predictive control of the inverter and the actual instant of firing are very much dependent on the incoming signal. A corrupted or distorted waveform will cause incorrect firing which can lead to the generation of non–characteristic harmonics for which there are no filters provided. This can lead to severe harmonic distortion and eventually even lead to blocking of the converter.

The need to be more independent of the voltage waveform, especially in light of the trend towards weaker systems, saw the emergence of "phase locked oscillators." This became what is now referred to as a phase locked loop in power systems applications. The basis of this control system is a voltage controlled oscillator (VCO) which delivers a train of pulses at a frequency directly proportional to its control voltage. The output of the VCO is a ramp signal at its frequency which triggers the pulses. The various PLLs differ only on the feedback method used to determine this voltage.

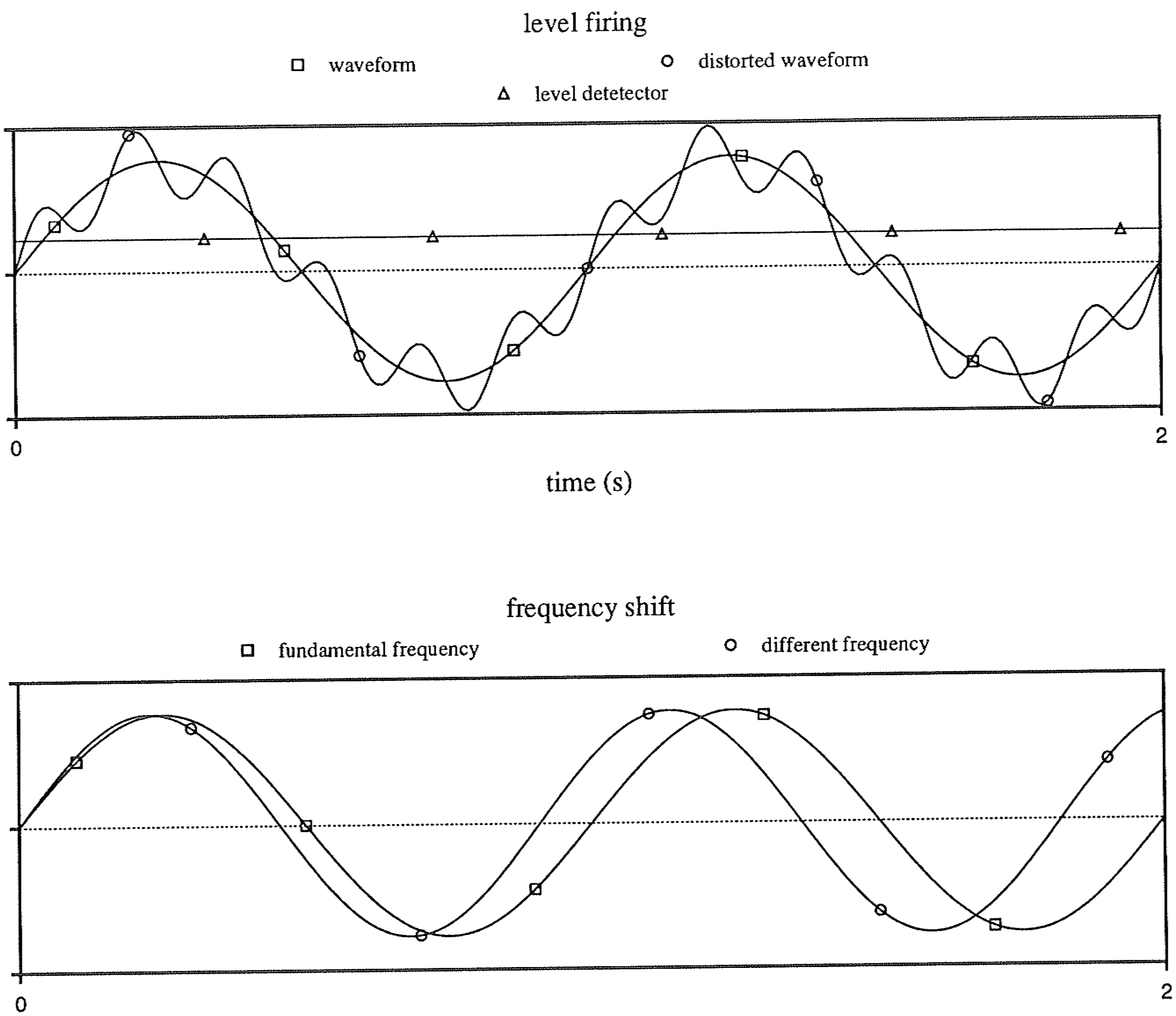

Figure 2 .3 : Firing Waveforms

2 .5 .1 Basic PLL Theory

The purpose of a PLL is to derive the fundamental waveform from the incoming signal [9,10]. The PLL is a feedback loop, as shown in Figure 2 .4 , consisting of three basic components :

(i) Phase Comparator (PC)

(ii) Loop Filter

(iii) Voltage–Controlled Oscillator (VCO)

The incoming signal is the original signal, while the VCO outputs the synthesized signal for comparison. It is important to note that the PLL output does not have to be of the same form as the input. The PC does a phase comparison on these two signals, which is possible independent of the type of the inputs. For example, in converters, though the voltage waveform is a sinusoid, the VCO outputs a ramp signal at the desired frequency. This will be explained in greater detail later on.

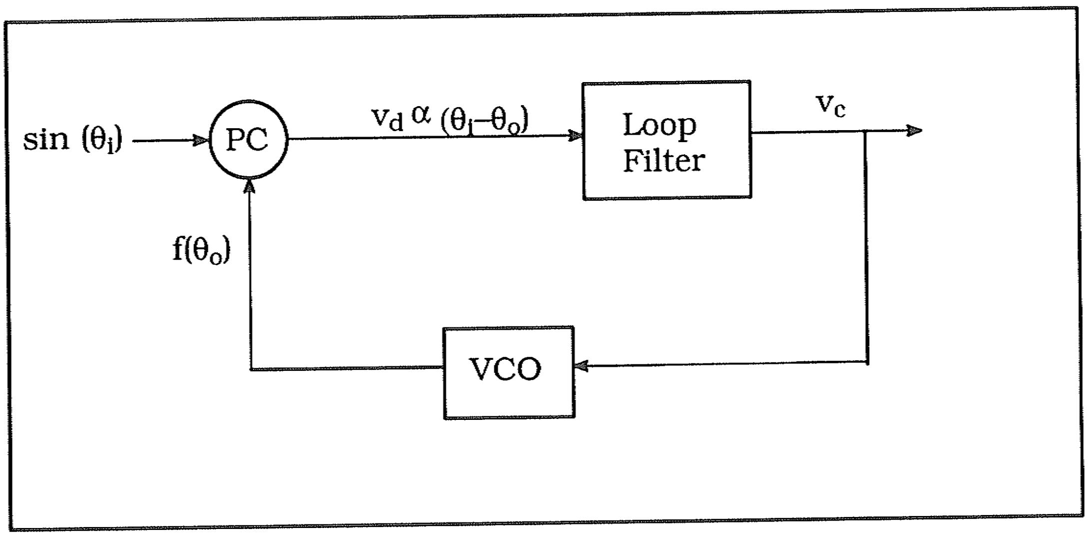

Figure 2 .4 : Simple Phase Locked Loop

Before examining it in detail, let us try first to qualitatively see how a PLL works. The VCO operates at a set frequency to begin with. The incoming signal and this signal are compared to generate an error which is related to the phase and frequency difference between these two. This error is then filtered, amplified and sent to the VCO. In this manner the VCO frequency is forced to vary in a direction that reduces the frequency difference between the VCO and the input signal. The feedback nature of the PLL causes it to synchronize or lock with the incoming signal. At this point the VCO frequency is identical to the input signal except for a finite phase difference. This is necessary to shift the set VCO frequency to that of the input.

Another way to describe a PLL is to realize that the phase comparator is really a multiplier circuit that mixes the input and VCO signal. This produces the sum and difference frequencies. When locked the difference frequency is zero, and the sum frequency is removed by the loop filter – therefore, only the dc component is sent to the VCO.

2 .5 .2 Loop Equations

When locked, i.e. the input signal and the VCO output are synchronized, the PLL can be approximated as a linear control system. The input signal has a phase $\theta_i(t)$ and the VCO output has a phase $\theta_o(t)$, and assuming a linear phase comparator its output will be proportional to the difference between these two. So, allowing for the phase comparator gain factor of K_d, we have

$$v_d = K_d \; (\; \theta_i - \theta_o \;)$$

or, in the Laplace domain,

$$V_d(s) = K_d \; [\; \theta_i(s) - \theta_o(s) \;] \; .$$

This is filtered by the loop filter – noise and high frequency components are suppressed. Representing the filter by the transfer function F(s), we can say

$$V_c(s) = F(s) \; V_d(s) \; .$$

The VCO has a centre frequency which is altered by a factor

$$\Delta\omega = K_o \; v_c \; ,$$

where K_o is the VCO gain factor. Since the frequency is the derivative of the phase, we could also say

$$\frac{d\theta_o(t)}{dt} = K_o \; v_c \; .$$

Now, by taking Laplace transforms, we have

$$s \; \theta_o(s) = K_o \; V_c(s) \; .$$

Therefore, the output of the VCO is

$$\theta_o(s) = \frac{K_o \; V_c(s)}{s} \; ,$$

or, in other words, the VCO functions as an integrator in the feedback loop. From this equation, we can see that the most determining factors on the performance of the loop are the loop gain and the filter transfer function, F(s). The above equations are used in the actual modeling of our PLLs, discussed in Chapter 3.

2 .5 .3 Loop Terminology

In the above loop equations, we have analyzed the PLL for a locked state. In this state if a frequency change occurs a phase error builds up and the control mechanism of the PLL works to eliminate or reduce the error to a minimum. There are three possible outcomes in this situation. The ideal one is that the locked state is regained without the VCO skipping any cycles. This means that the frequency deviation is within the "lock–in" range of the PLL. On the other hand, if one or more cycles are skipped before re–locking, the frequency is considered to be in the "pull–in" range. In the pull–in range the loop is considered to have lost lock for some duration, no matter how short, before reaching lock. Another common term in PLL literature used for either, or both, the lock–in and pull–in range is the capture range. If we go beyond this frequency range the loop cannot regain lock, and is unable to track the input signal.

So far we have only discussed a locked loop and the tracking of a PLL. One usually starts in the unlocked state and the actual process of bringing a loop into lock is termed acquisition. The ability of a PLL to obtain self–acquisition is often considered a slow and unreliable process. For better results PLLs usually rely on aided acquisition, which uses auxiliary circuits to initially bring the loop into lock.

Chapter 3

FIRING CONTROLS IN CONVERTERS

3 .1 INTRODUCTION

The firing controls of a converter can be achieved by various methods, and three are described in this thesis. The original PLL based implementation was introduced by Ainsworth, and was called a phase locked oscillator. This controller tries to reproduce and track the ac system frequency, and is referred to as a pulse frequency controller. An updated version of this, called a pulse phase controller, uses phase correction as a major component to achieve this same objective. Another name for this method is pulse position control. The last approach detailed for converter controls uses a phase transformation to help provide the necessary information for accurate firing.

3 .2 PULSE FREQUENCY CONTROL SYSTEM (PFC)

The first proposed PLL based control system for power systems applications is classed as a pulse frequency controller and was developed by Ainsworth. A block diagram of this is shown in Figure 3 .1 .

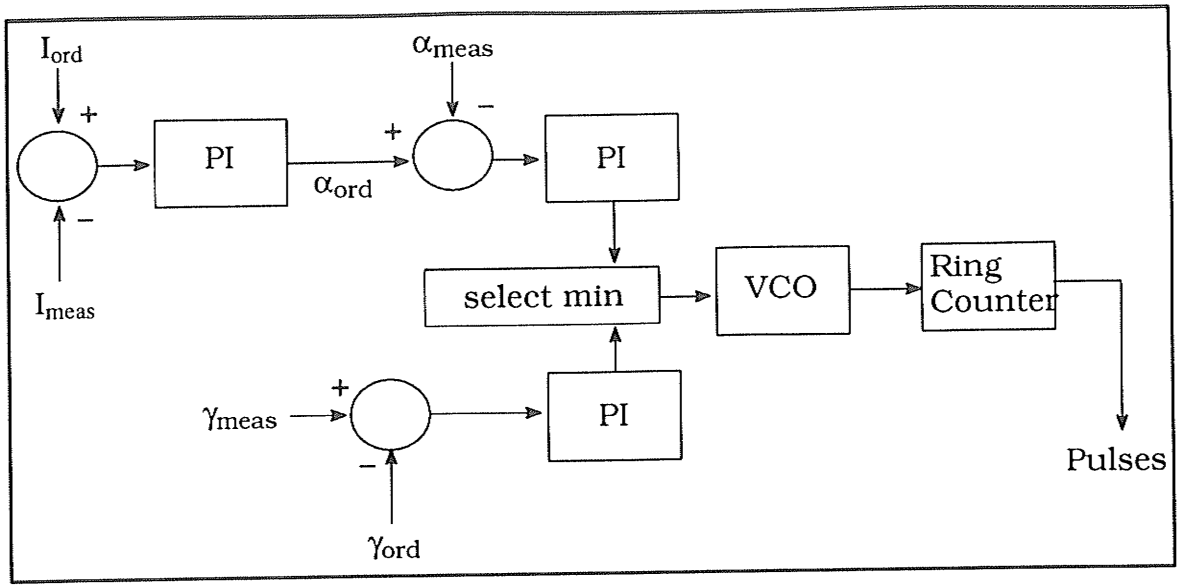

Figure 3 .1 : Block Diagram of Pulse Frequency Controller

The error signal for the rectifier is through dc current error, the difference between the desired current and the measured current. For the inverter the error is the difference between a set extinction angle and the one measured. The final outcome from the VCO is a continuous train of pulses, whose frequency is determined by the loop. The feedback error is used to modify the frequency of the train of the VCO pulses. By manipulating the frequency, not only is the desired frequency achieved, but speeding up and slowing down the pulses causes the input phase to also be reproduced. In Figure 3 .2 the output of the VCO and the triggered pulses are shown – here a phase change is shown to occur by a change in the pulse rate. This is rather a simplified diagram, but conceptually shows how the frequency of the PLL is modulated to create a change in the phase of the pulse rate.

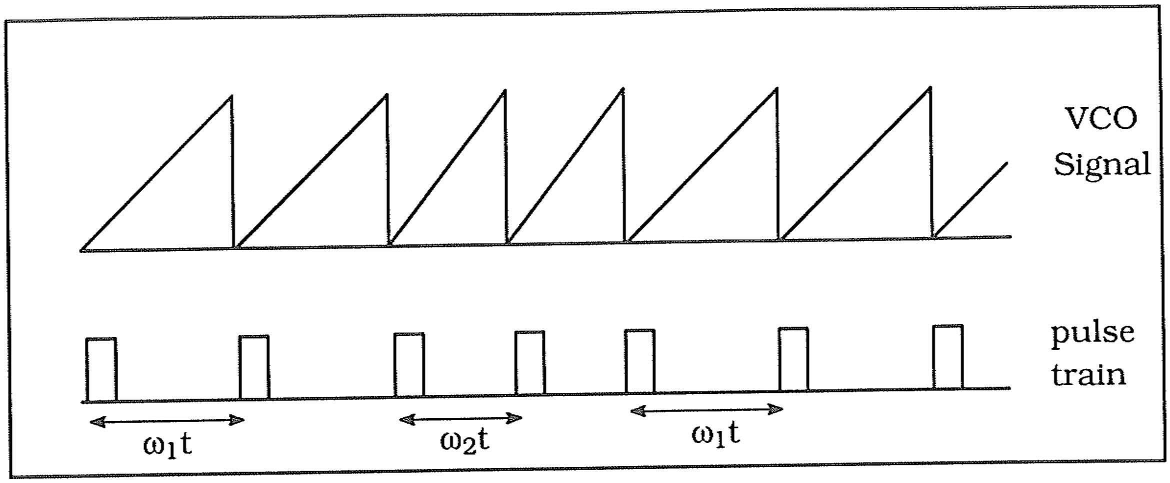

Figure 3 .2 : Pulse Frequency Controller

This train of pulses is further fed to a six-stage ring-counter which is stepped cyclically through by the oscillator pulses. As each stage is activated, a START pulse is sent to the next thyristor in the sequence. This will mean that each successive START pulse will normally occur in 60 degree intervals. Similarly, the STOP pulse for each thyristor is issued two stages later, meaning the duration a thyristor remains on is 120 degrees. In a twelve pulse scheme we have two six-stage ring-counters or pulses with 30 degree intervals, but the algorithm is the same.

Figure 3 .1 at first sight appears to be different from the PLL shown in Chapter 2 (Figure 2.4). However, it should be noted that α_{meas} is actually the phase difference between the ac voltage zero crossings and the issue of a firing pulse (i.e., the VCO output). Hence the α_{meas} signal can be treated as the phase error in the loop. Similarly if the γ path is selected, γ_{meas} is also an indication of the phase error.

For the constant current loop, the usual mode for a rectifier, the amplified difference between the current reference and the measured dc line current gives rise to a firing angle order. This order is compared to the actual firing angle and this difference provides the feedback control. So, unlike the conventional PLL, we are synchronized to the input signal with a phase shift corresponding to the firing angle order. This actually simplifies the electronics of the firing controls by using this offset as a reference point, instead of the zero crossings of the input ac voltage. Note that this difference is first fed through a proportional–integral (PI) controller to filter the input. In this manner, both the instantaneous and average error are taken into account. The PI controller is analogous to a loop filter,mentioned in the basic PLL theory.

To visualize the working of this control loop, let's first consider steady state operation. The amplified error gives the oscillator a frequency that issues pulses at a constant rate. These pulses will have a certain phase with respect to the ac system voltage, which corresponds to the firing angle. This angle will be the one necessary to result in the required dc current.

Now, to see how the loop is an effective control mechanism, let's say the current increases. In this case, the amplified difference in the feedback loop will cause the oscillator to slow down, thus delaying the pulses and thereby increasing the firing angle. Increasing the firing angle will eventually reduce the current to the required value. The system, by shifting frequency will actually, in the end, only change the phase in this case, the desired result. So, the system settles down to the same current, the same amplified difference and the same oscillator frequency as in steady state, but now has a different firing angle.

In extinction angle control, the reigning state for an inverter, the negative feedback is provided by the extinction angle error. This is the difference between the measured angle and the extinction angle setting. Again a PI controller is used to filter the "raw" error. The setting is determined as a compromise between allowing a margin of safety for the firing angle and that of minimizing the consumption of reactive power. The feedback is not of a constant nature, but actually has an impulse type behavior if the extinction angle falls below some specified value, a chosen minimum extinction angle. Therefore, if this condition is met a quick change to the phase is applied to avoid the extinction angle from falling into the danger zone of a possible commutation failure.

In this model of a pulse frequency controller the choice of feedback error is not predetermined, rather a minimum selection circuit makes this decision. In the case of a rectifier the firing angle error is smaller, so it is the controlling quantity, while the opposite is true of an inverter. Of course, usually the rectifier is designated in charge of current control and therefore the inverter has a lower current setting at which it is required to in current control. This will naturally force the firing angle error to be greater in an inverter than the extinction angle, making the choice of minimum error apparent. But we can see how transition from one mode to another control mode is accomplished by considering the case of an inverter where the dc line current drops below that of the current setting. At this point the minimum selection will change–over from extinction angle to firing angle error, and the inverter will now go into rectification.

There is a feedback signal from the minimum selection that is not shown in Figure 3 .1 . After choosing, a difference error is generated between the selected one and both the firing angle error and the extinction angle error. This is fed back to the original error signal, before selection. This keeps both signals at a similar level, making transition from one type to the other smoother.

3 .3 PULSE PHASE CONTROL SYSTEM (PPC)

The next controller is basically a revised or modified version of the PFC. The difference is that the greatest change is in the phase of the VCO pulses. In this case the loop has a component that causes an instantaneous position shift, proportional to a change in the firing angle order; with a slower mechanism for catching any phase or frequency variations. An example of a phase change is shown through the VCO output and the subsequent pulses in Figure 3 .3 . The proportional change is determined in such a way as to cause the catch–up in phase needed in one time step.

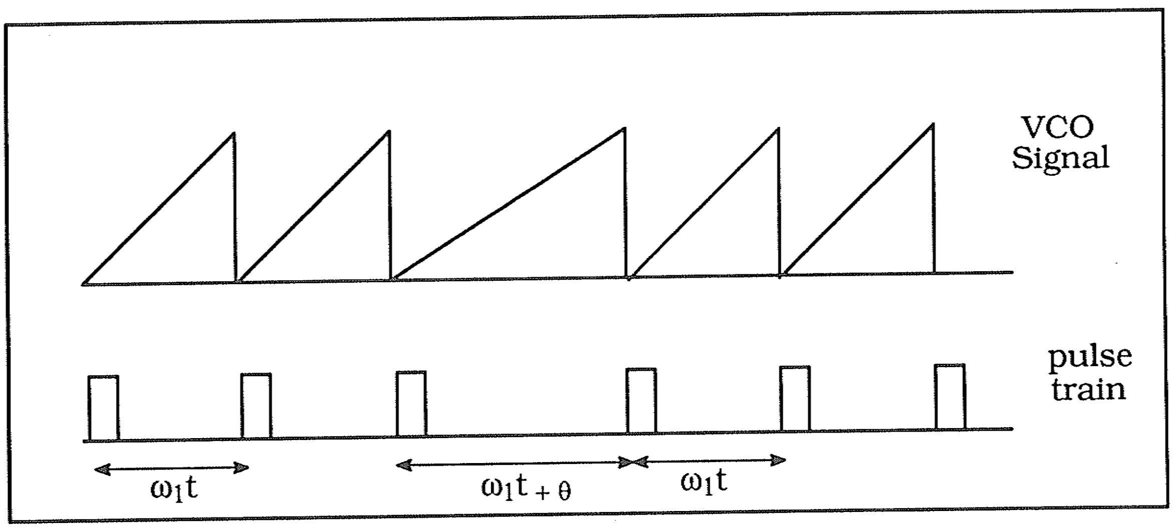

Figure 3 .3 : Pulse Phase Controller

As noted, the chief difference between a pulse phase controller and a pulse frequency controller is in the error management. Here the firing order differential is used to instantaneously change the VCO phase, rather than the frequency, for a step change in the actual firing angle to force immediate correction. In both types of controllers the error has both a proportional and an integral component – in this case the proportional gain plays a much larger role. There is a slower acting auxiliary circuit, which is similar in principle to the pulse frequency controller, that aids in following any phase and frequency variations. The PPC detailed in this thesis is based on the controller used on the Manitoba Hydro Nelson River Bipole II System, and is shown in Figure 3 .4 .

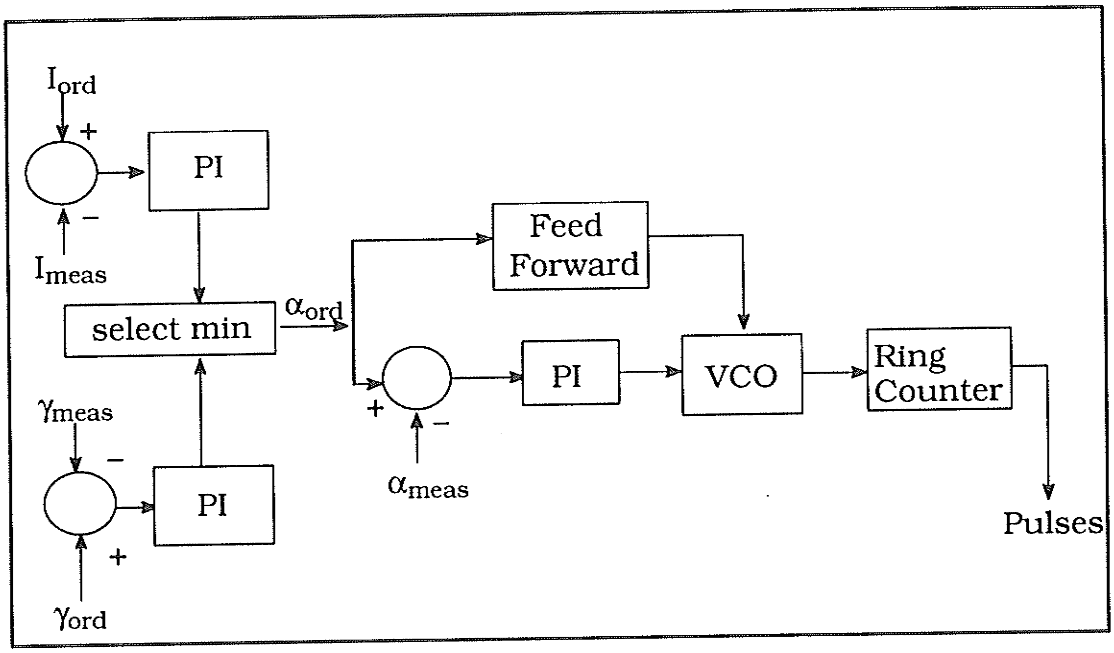

Figure 3 .4 : Block Diagram of Pulse Phase Controller

The error is generated with a slight variation to the earlier method. The minimum selection is done between the current error and the extinction angle error, both already fed through independent PI controllers, and this error produces a firing angle order. As explained before, the firing angle order is used two ways. First the change in the firing angle order is used in a feed forward type of control to initiate immediate correction in the phase of the VCO – an open loop correction. This is an immediate response to any change in the system's demands. And also in an auxiliary method to correct any residual error, by means of another PI controller, that will reflect any frequency change. For this error signal the order is compared to the measured firing angle to generate the desired response.

3 .4 dqz CONTROL SYSTEM (dqz Controller)

The last phase locked loop that was studied uses a d–q–z (or dqz) transformation to generate the error to control the firing pulses, as illustrated in Figure 3 .5 . The three phase voltages are transformed to two phases, the direct quadrature axes voltages, V_α and V_β, according to the following equations :

$$V_\alpha = \frac{2}{3}V_a - \frac{1}{3}V_b - \frac{1}{3}V_c$$

$$V_\beta = \frac{1}{\sqrt{3}}(V_b - V_c) \ .$$

The error signal is derived using

$$error = V_\alpha \ \sin\theta - V_\beta \ \cos\theta$$

where θ is the phase output by the VCO. The error signal is acted upon by a PI controller – then sent to the VCO to generate a signal to send to the sine–cosine oscillator, which outputs the $sin\theta$ and $cos\theta$ signals that make up the feedback to the phase voltages, V_α and V_β.

This method gives a continuous phase measurement based on the assumption of balanced ac voltages. Since the actual input signal generates the error signal it is an ongoing process. Of course this technique, as mentioned, relies on a balanced harmonic free three phase input, and will not be mathematically effective otherwise. Though, if unbalanced, it will still track the positive sequence. But we have to realize that a system with ac voltage imperfections will also affect the other methods of firing control – and though compromised, each system will still function. The error signal is simply the sine phase difference between V_a and θ. If the voltages are unbalanced the error is an oscillating quantity whose average represents the phase difference between the positive sequence fundamental voltage and the VCO output θ. In steady state the error is forced to zero thereby forcing θ in phase with the fundamental ac waveform. The VCO output θ can then be compared with the required firing angle and a firing pulse is issued when $\theta = \alpha_{ord}$.

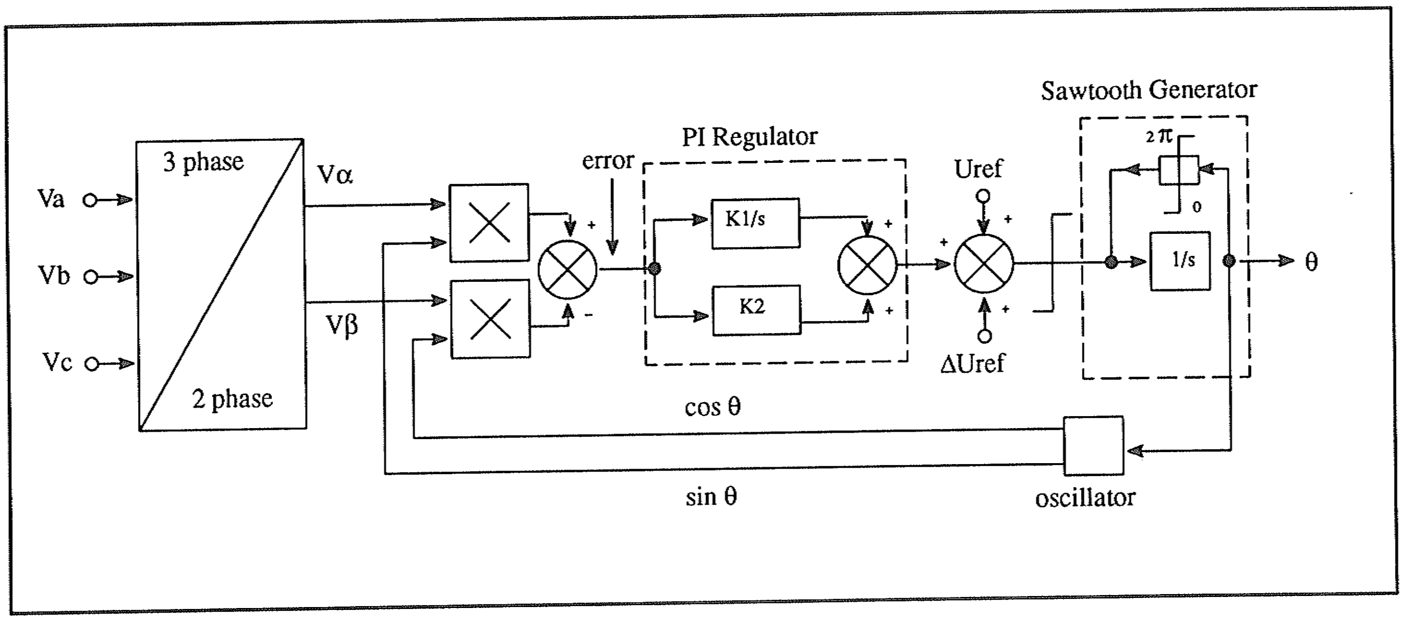

Figure 3 .5 : Block Diagram of dqz Controller

One difference to note between this control system and the previous two is the method of firing. Both the PFC and PPC use the output from the VCO to trigger the firing pulses at each periodic zero–crossing of the ramp signal. This method issues the pulses when the ramp reaches a specified level corresponding to the ordered firing angle.

Chapter 4

SIMULATION RESULTS

4 .1 INTRODUCTION

The PLL based firing control systems are tested and compared on a simulated system. The test system is based on the Nelson River Transmission System, and was modeled using EMTDC. We compare the controllers by monitoring their responses to various operating disturbances. Though the system has many parameters that can be compared for evaluation, in the thesis three are chosen as giving enough of an indication of the results: the dc current and firing angle at the rectifier end, and the extinction angle at the inverter end. They seem to reflect how each control loop behaved in each situation.

Each loop was tuned for optimal operation. Thus the comparison presented here is based on the assumption that each controller has been tuned to its best overall performance.

4 .2 NELSON RIVER TRANSMISSION SYSTEM

In the Figure 4 .1 is a schematic representation of the modeled system. By having a star–star and a star–delta valve group connected on each side we have a 12–pulse system. Only one 12 pulse valve group in one pole was modeled. Representation of the other pole was achieved through a dc current source of 1.8 kA, which is 1 per unit (p.u.) rated current, which is incident on the node between poles.

On the dc side the filters, smoothing reactor and simple by-pass switch model were included. The line itself is represented by all four conductors using distributed parameters. The conductors not incident at the pole being studied were terminated in their smoothing reactors and dc filters. Since dc currents involve no steady-state coupling effects, we can terminate the other conductors to ground. This assumes that no simultaneous voltage changes take place on the unmodeled converter during any of our tests.

The ac system models include the ac filters, the convertor transformers and a simple Thevenin equivalent circuit that is designed to provide the required short circuit capacity and the proper damping at two specified frequencies. The rectifier has a SCR of 3.0 at 85 degrees, while the inverter has a SCR of 2.5 at 80 degrees.

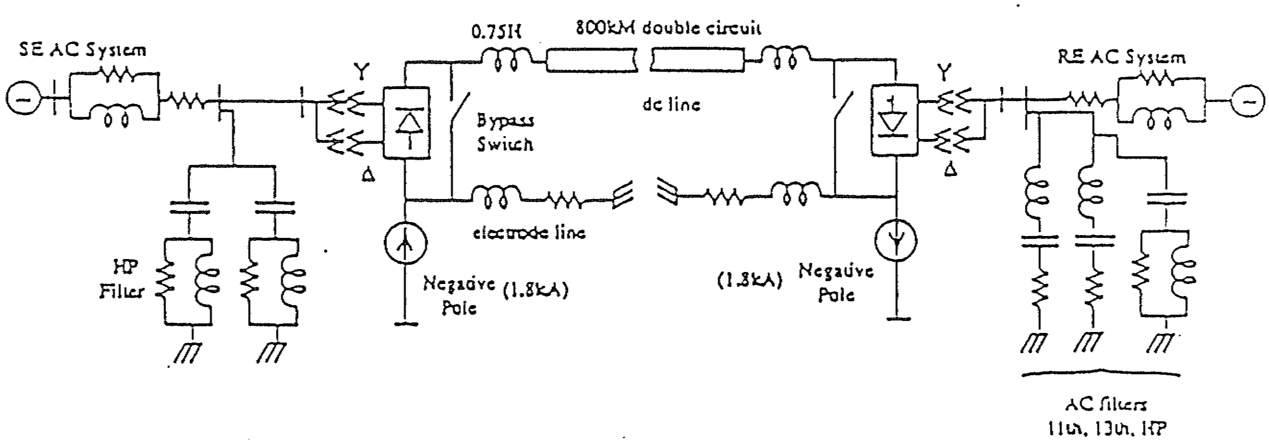

Figure 4 .1 : Nelson River Transmission System Model

4 .3 TEST SIMULATIONS

For the tests the three quantities are plotted to show the responses of the controllers. The dc current is measured in kiloamps. The firing angle, which can also be referred to as alpha as used in our results, is in degrees in the graphs. Similarly the extinction angle is referred to as gamma and is in degrees. The gains of each of the firing control systems were optimally adjusted to give the best overall response for the disturbances considered. The higher level controls, i.e. current and angle orders, were assumed to be the same for all cases.

4 .3 .1 Reference Current Drop

This test is very easily implemented in the program by just changing the current order at the rectifier, which is the converter station in current control. The current order was reduced by 50% from the original order for a 500 ms period and then returned to 100% status thereafter.

From Figures 4.2–4.4 we can see some of the results graphed from this test. The response of the PFC is the slowest and has the greatest overshoot from the desired values. The PPC and the dqz Controller are similar, but both the firing and extinction angle curves lock faster and tighter for the dqz Controller. The firing angle response to the order is almost instantaneous in these cases. For the dqz Controller we can see its superior ability to lock onto the order for both angles so accurately.

4 .3 .2 Extinction Angle Setting Change

Changing the setting of the desired extinction angle at the inverter is similar to the lowering of the reference current in ease of implementing in the program. The nominal extinction angle setting of 18 degrees was lowered to 15 degrees for 800 ms, and then returned to the original setting.

This is a delicate test in some ways since we are testing it on a weak system. Lowering the setting could raise the risk of commutation failure and make recovery difficult. By decreasing the extinction angle the need for reactive power consumption is reduced.

From Figures 4.5–4.7 we can see some of the effects of this test. It is not a major disturbance, so its overall effect is not of great magnitude, unless it leads to commutation failure. The dc current response shows the dqz Controller as the best, while the PPC and PFC follow, in that order. Again we can note the excellent tracking and accuracy of the dqz Controller in the angle graphs. Another point is clearly seen in the graphs for this case – the proportional nature of the control of the PPC. Though response is fast, settling down is not exact as slight oscillations continue to take place.

4 .3 .3 Single Phase Fault at Rectifier

To accomplish this type of fault the actual network simulated system was slightly altered. At the ac bus each line was connected to ground through a very large resistance, basically not changing the system in any discernable way at this point. When a fault is desired on any line this resistance can simply be reduced to a very low value that basically is a short between the line and ground. To remove the fault situation we just go back to the original value of the resistance. Note that when removing the fault, analogous to opening a switch, one would want to do it on a current zero. The faulted condition is induced for 50 ms in this test.

In this case the graphs, shown in Figures 4.8–4.10, show the dqz Controller to be the most effective. It has the fastest response and reaches steady state operation first. In the PFC the dc current reaches zero and has slowest recovery.

4 .3 .4 Single Phase Fault at Inverter

This is implemented in the same manner as the fault at the rectifier, but at the inverter end.

Similar to earlier, Figures 4.11–4.13 show the dqz Controller with the best response. In this case the PFC has a very poor recovery compared to the other two.

4 .3 .5 Three–Phase Fault at Rectifier

Almost exactly the same as the one–phase fault, except shorting out all three lines. This creates a balanced line–to–ground three–phase fault.

From Figures 4.14–4.16 we can see the response to this fault. All three controllers exhibit similar behavior. In this case the settling down time is very comparable. The dqz Controller does manage to bring the system to values close to equilibrium the fastest, as demonstrated in the dc current response curve.

4 .3 .6 Three–Phase Fault at Inverter

Again this is implemented in the same way as the rectifier fault, but at the inverter end.

These graphs, Figures 4.17–4.19, show a very similar result as that of the single phase fault at the inverter. They show the dqz Controller as having the best recovery, but the PPC being very close in response. The PFC has the worst results, with the slowest recovery and large overshoot.

4 .3 .7 DC Line Fault at Rectifier

Again we alter the system configuration to accommodate a dc line fault. At the dc bus we connect a large resistance to ground, which is switched to a negligible resistance to initiate a fault. The fault, in this case is sustained for 50 ms, after which point the resistance is increased so that the short again effectively disappears. In this situation a slightly different method was used during the fault – we specify the firing angle order after realizing the fault has occurred. This is done in the program, it was chosen to recognize the fault at 10 ms after its occurrence. At this point, the firing angle order was left as specified for 10 ms, which would be the maximum value. After this we ramped the order down to the minimum value, the fault being considered cleared.

For this case, Figures 4.20–4.22, the fastest recovery is seen to be by the dqz Controller. Though the PPC has a fast response, the recovery is quite a bit slower, and is more comparable, when taking into account the point where the system is considered settled down, to the PFC. But the PFC has a very large overshoot, and takes a long time to even come close to the normal operating conditions.

4 .4 AC VOLTAGE AT THE INVERTER BUS

Another system quantity of interest for comparison is the ac voltage at the bus. Table 4 .1 shows the overvoltages measured for the various tests just discussed. Control of this value is another criterion of a effective control system. The values seen here do not give any clear–cut best choice out of the three controllers, and they are relatively comparable based on overall response in this category.

Table 4 .1 : AC Overvoltages at the Inverter

Test #	PFC	PPC	dqz Controller
4.3.1	211.7 kV	211.8 kV	215.8 kV
4.3.2	194.3 kV	192.6 kV	192.3 kV
4.3.3	220.2 kV	228.3 kV	208.7 kV
4.3.4	224.3 kV	219.8 kV	221.1 kV
4.3.5	225.8 kV	232.7 kV	211.8 kV
4.3.6	204.3 kV	212.9 kV	214.5 kV
4.3.7	325.3 kV	318.2 kV	292.3 kV

4 .5 DISCUSSION

When analyzing the responses of the three PLLs to various operating conditions we have to consider different factors. The speed of recovery, settling down time, overshoots of different variables, etc. In our comparisons, the best performance was seen to be exhibited by the dqz Controller. The PFC was seen to be generally the slowest at recovery, and also had the greatest overshoots. Since operational disturbances are often more the case of locking onto the phase of the input signal than the actual tracking of frequency variations, the PPC shows how incorporating this into the original PFC improves the performance dramatically. When comparing the PPC and the dqz Controller, they are almost comparable in behavior.

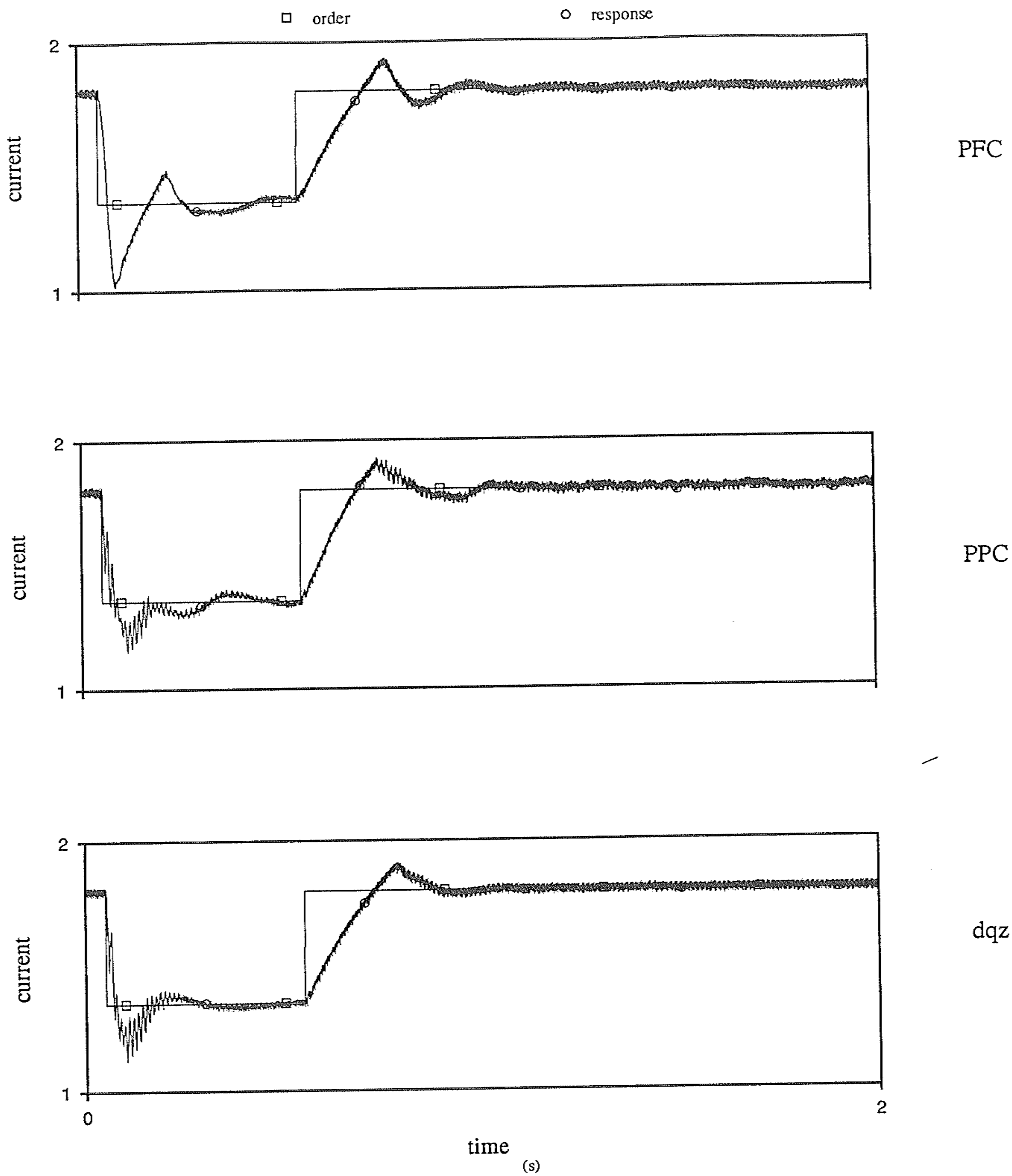

Figure 4.2 : DC Current for DC Reference Current Drop

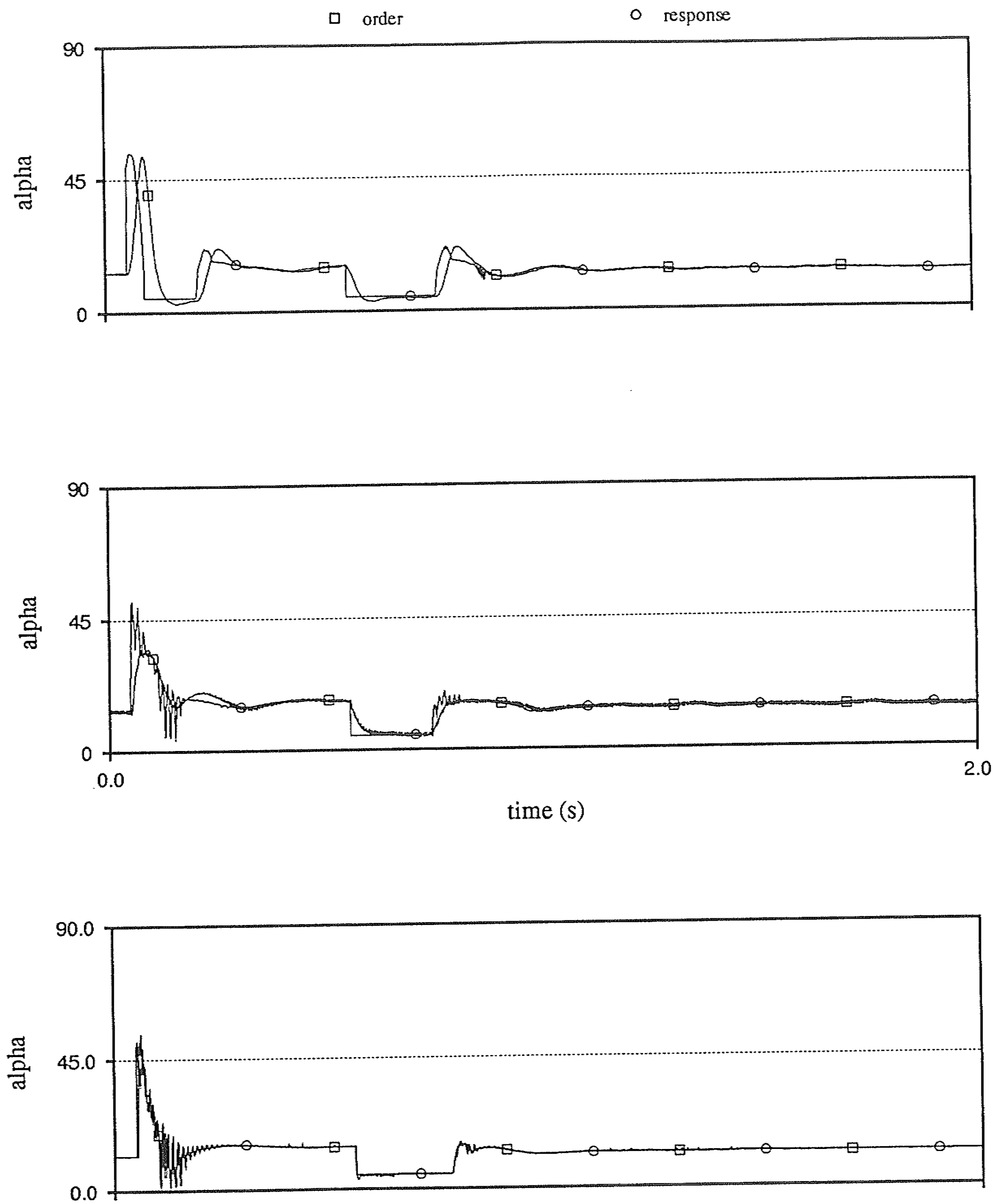

Figure 4.3 : Alpha for DC Reference Current Drop

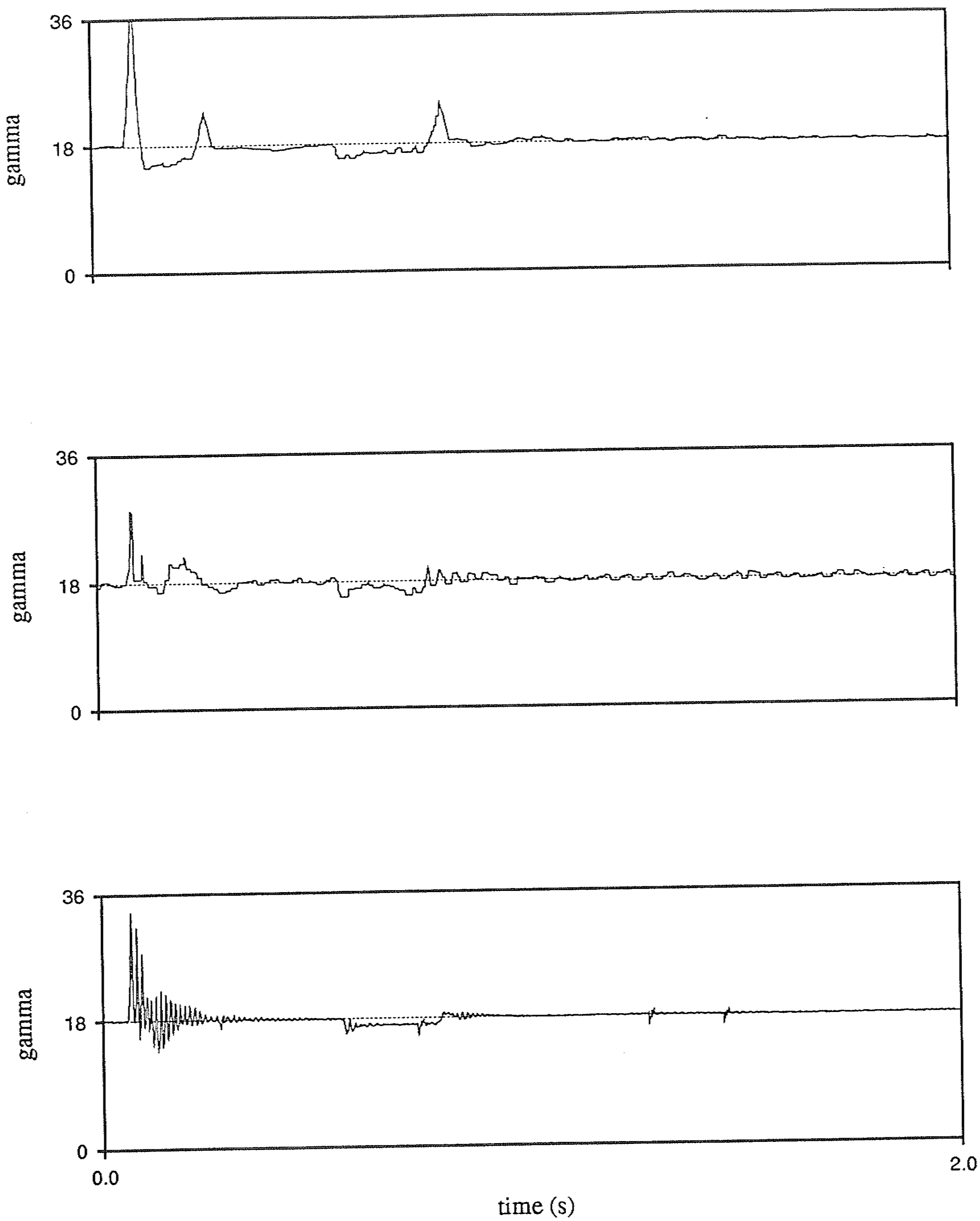

Figure 4.4 : Gamma for DC Reference Current Drop

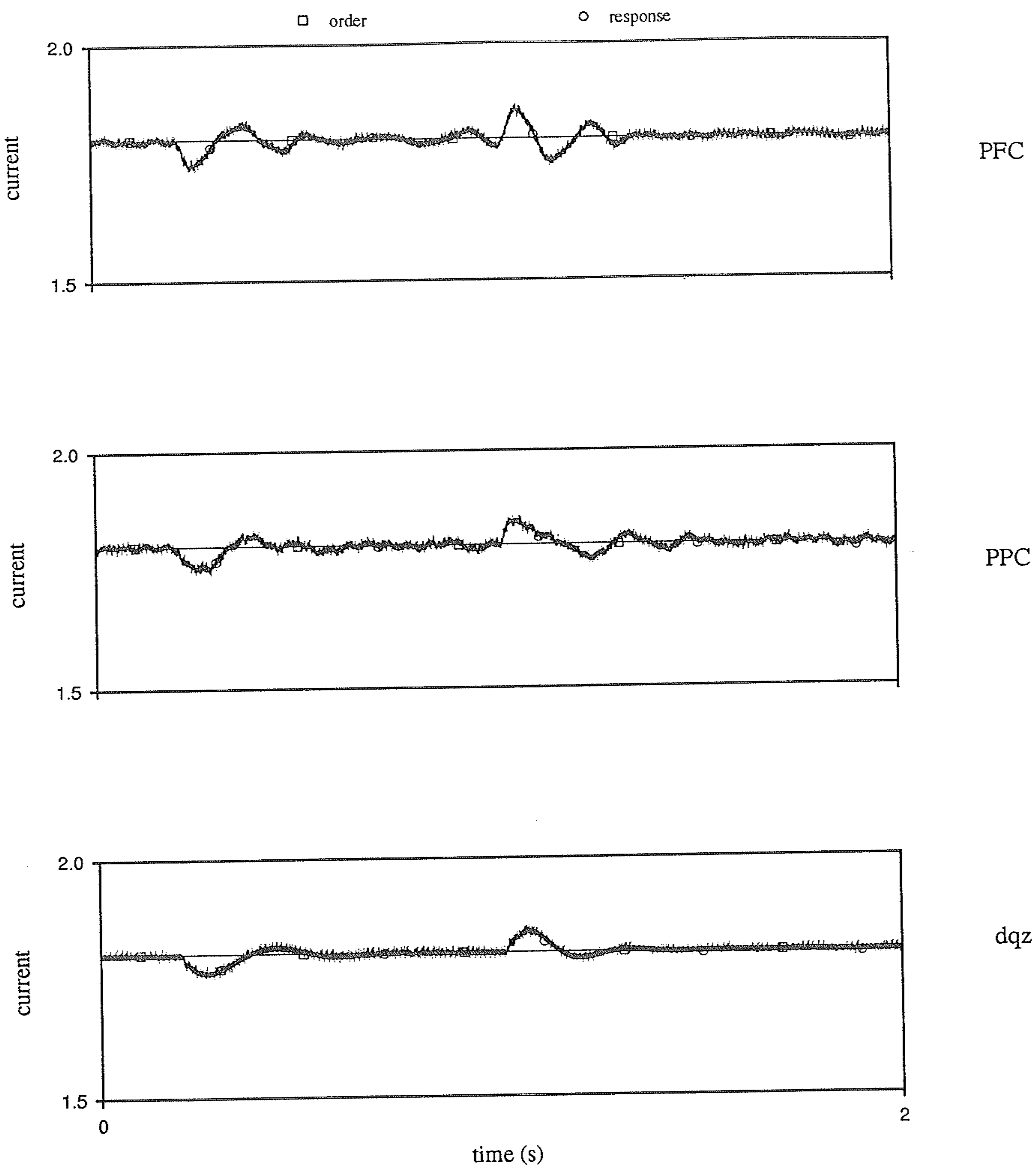

Figure 4.5 : DC Current for Reference Extinction Angle Drop

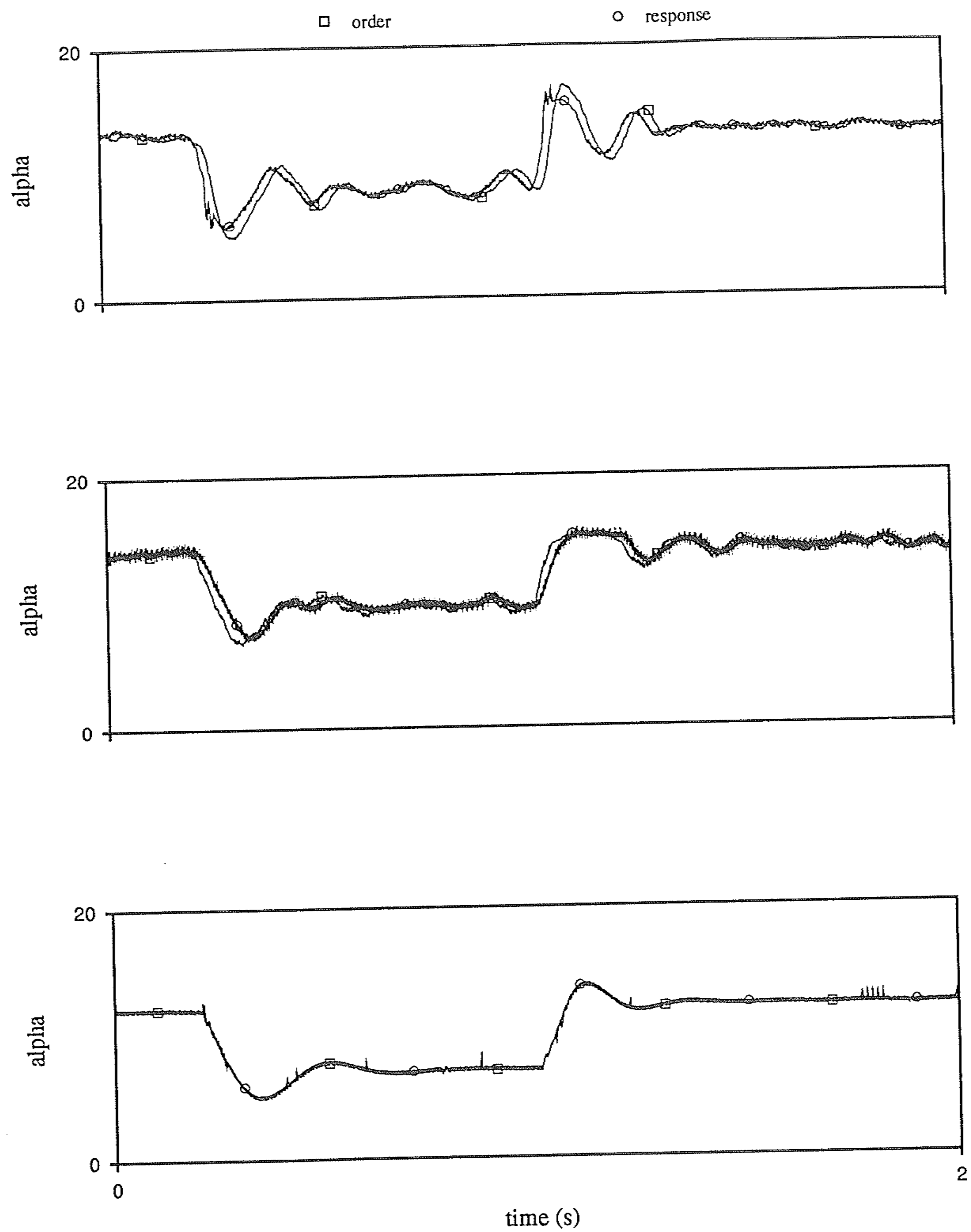

Figure 4.6 : Alpha for Reference Extinction Angle Drop

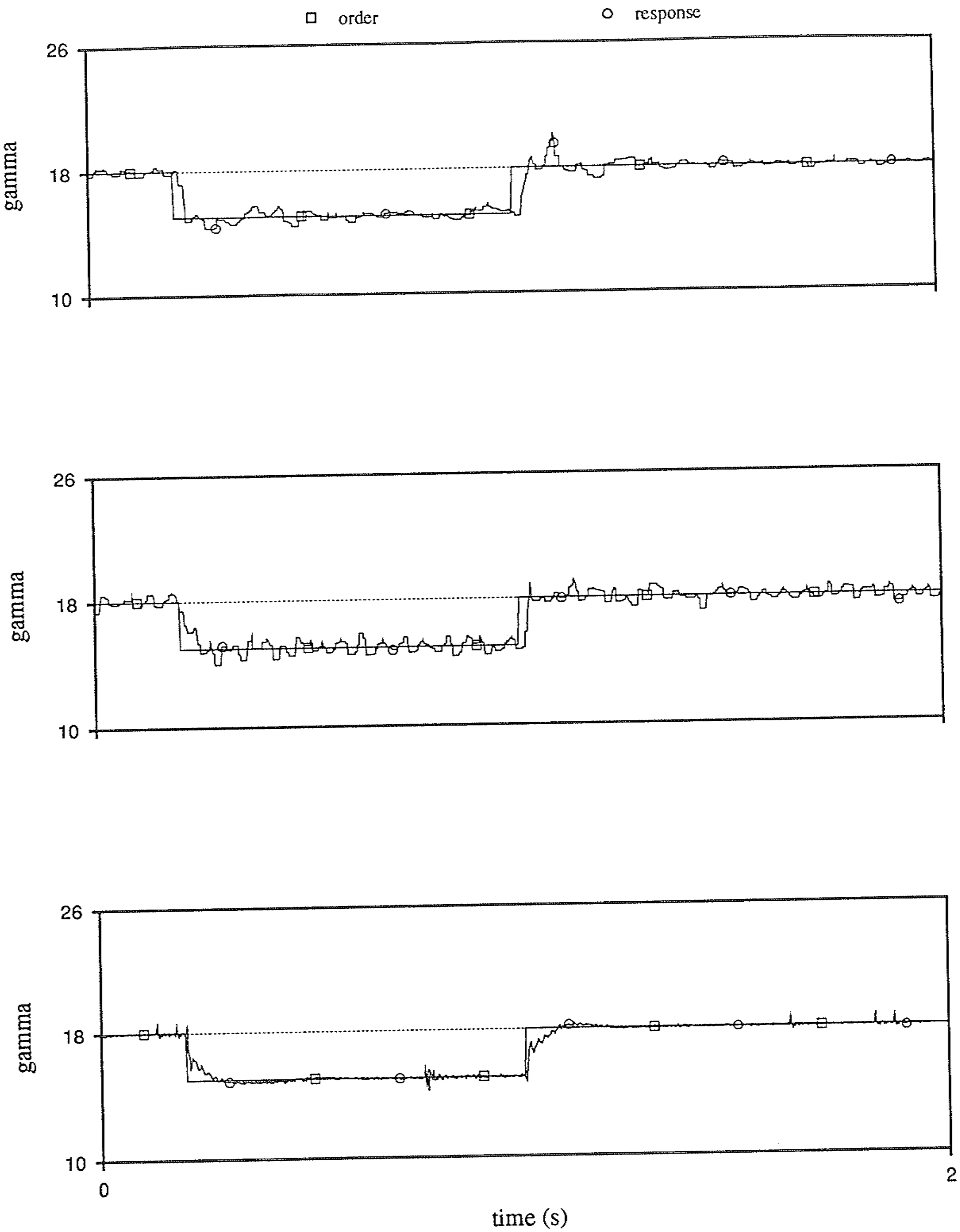

Figure 4.7 : Gamma for Reference Extinction Angle Drop

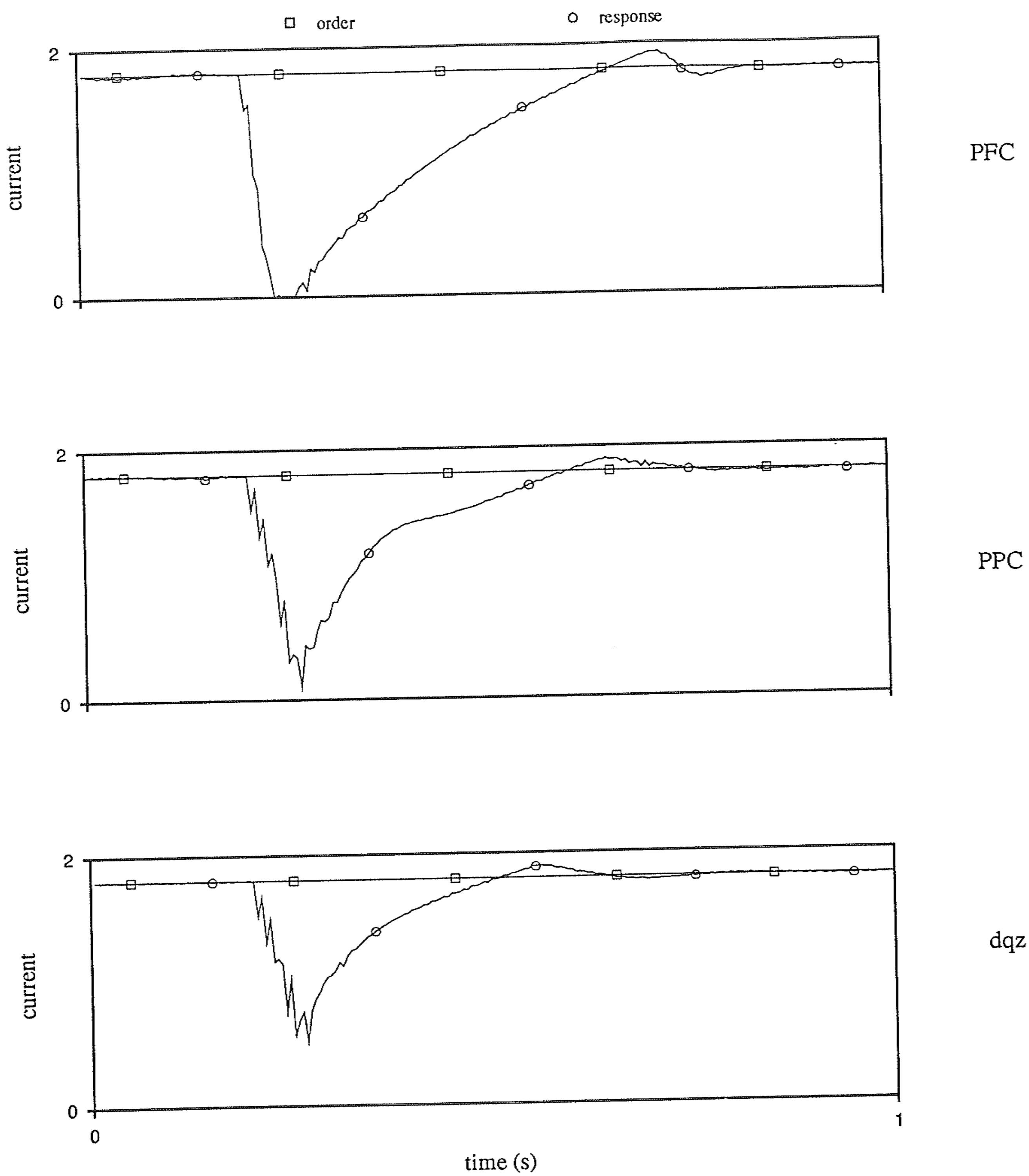

Figure 4.8 : DC Current for Single Phase Fault at Rectifier

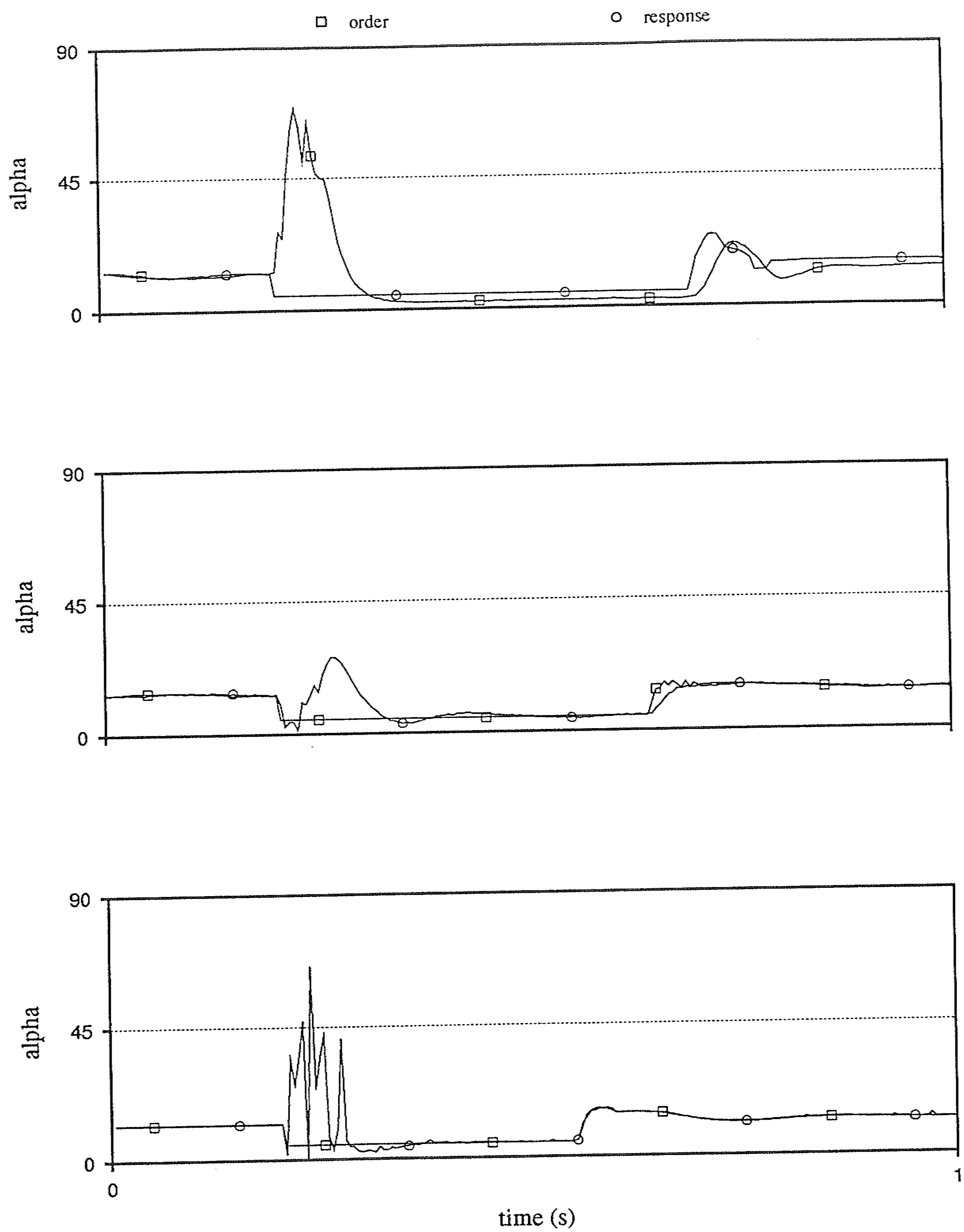

Figure 4.9 : Alpha for Single Phase Fault at Rectifier

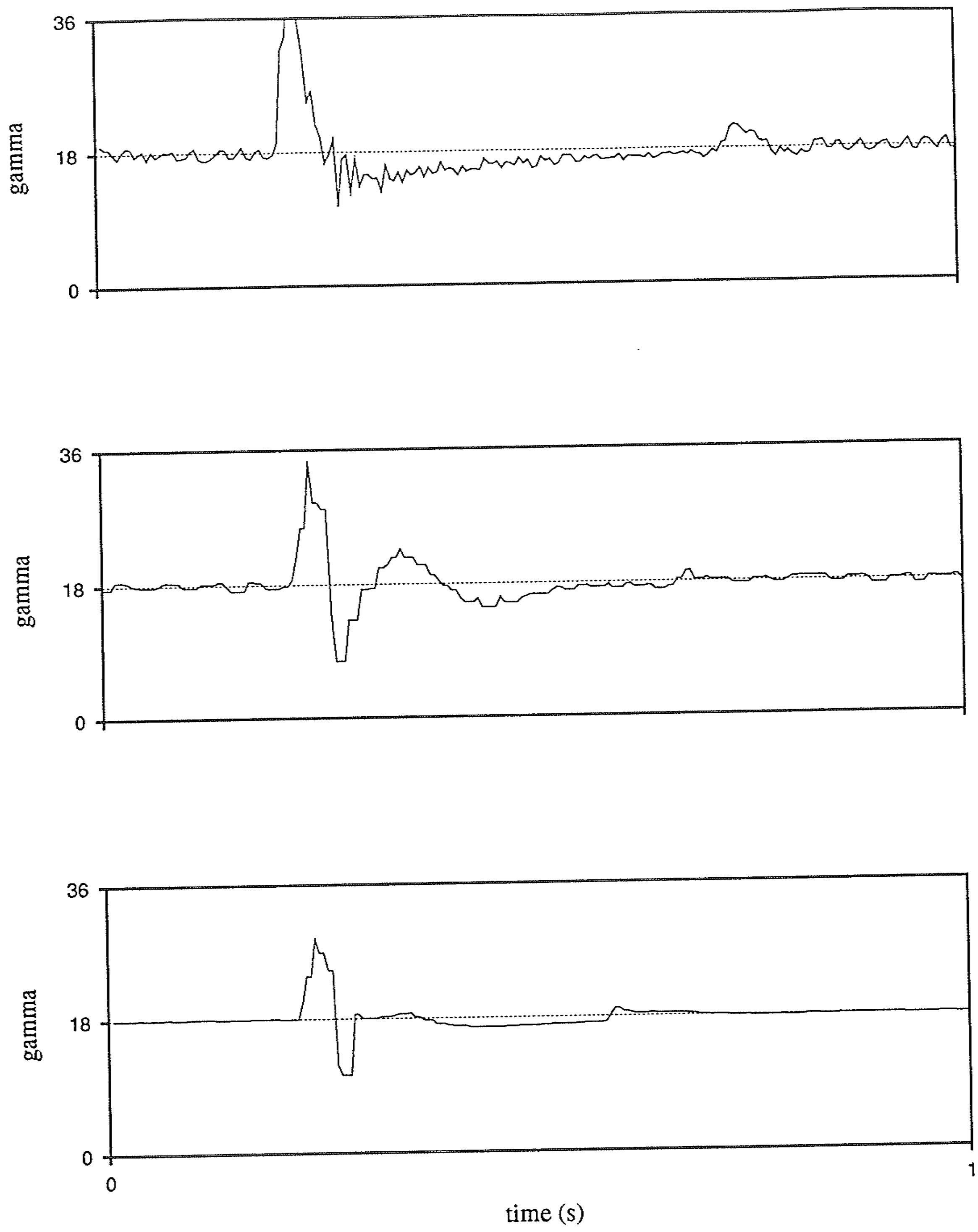

Figure 4.10 : Gamma for Single Phase Fault at Rectifier

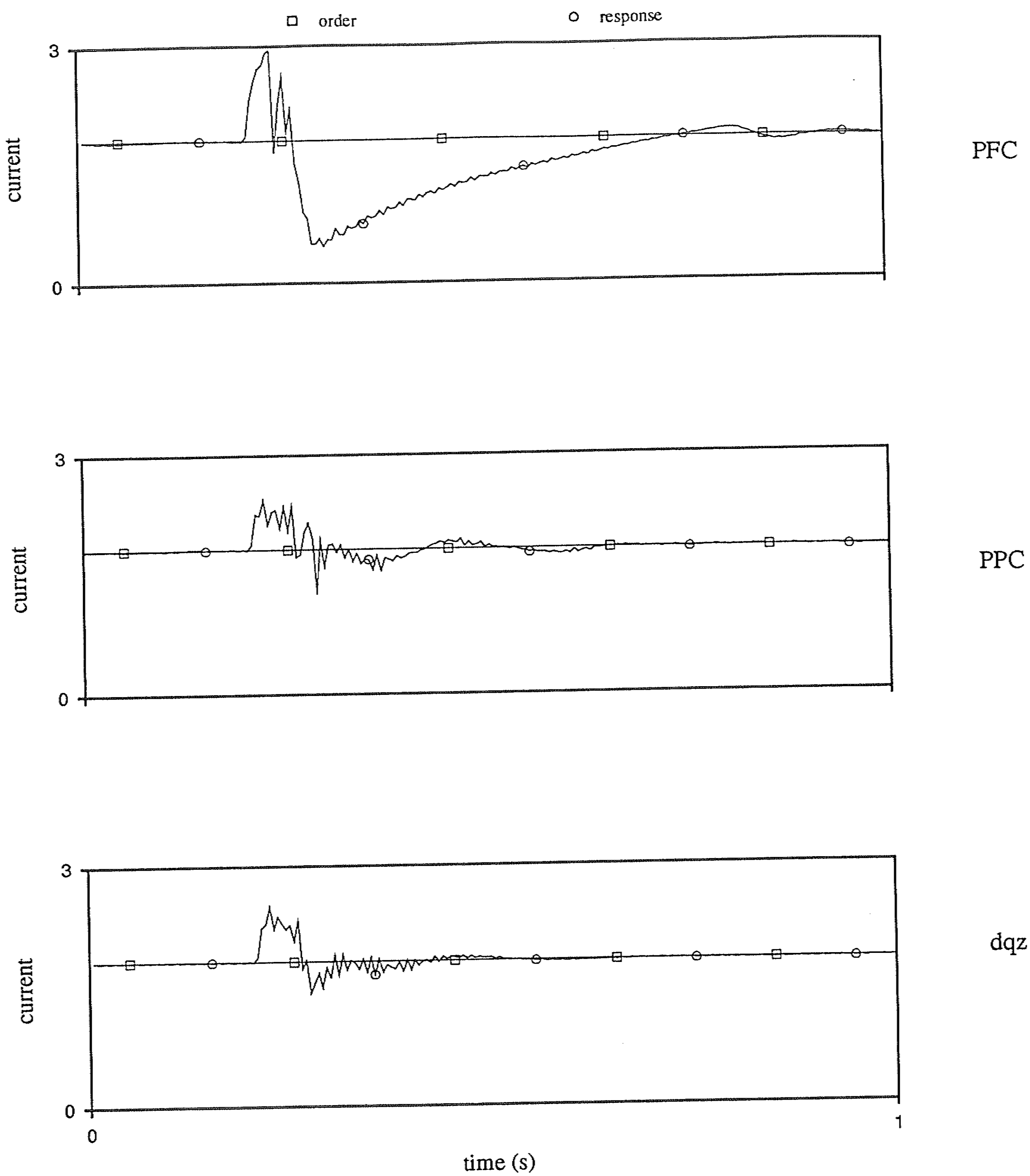

Figure 4.11 : DC Current for Single Phase Fault at Inverter

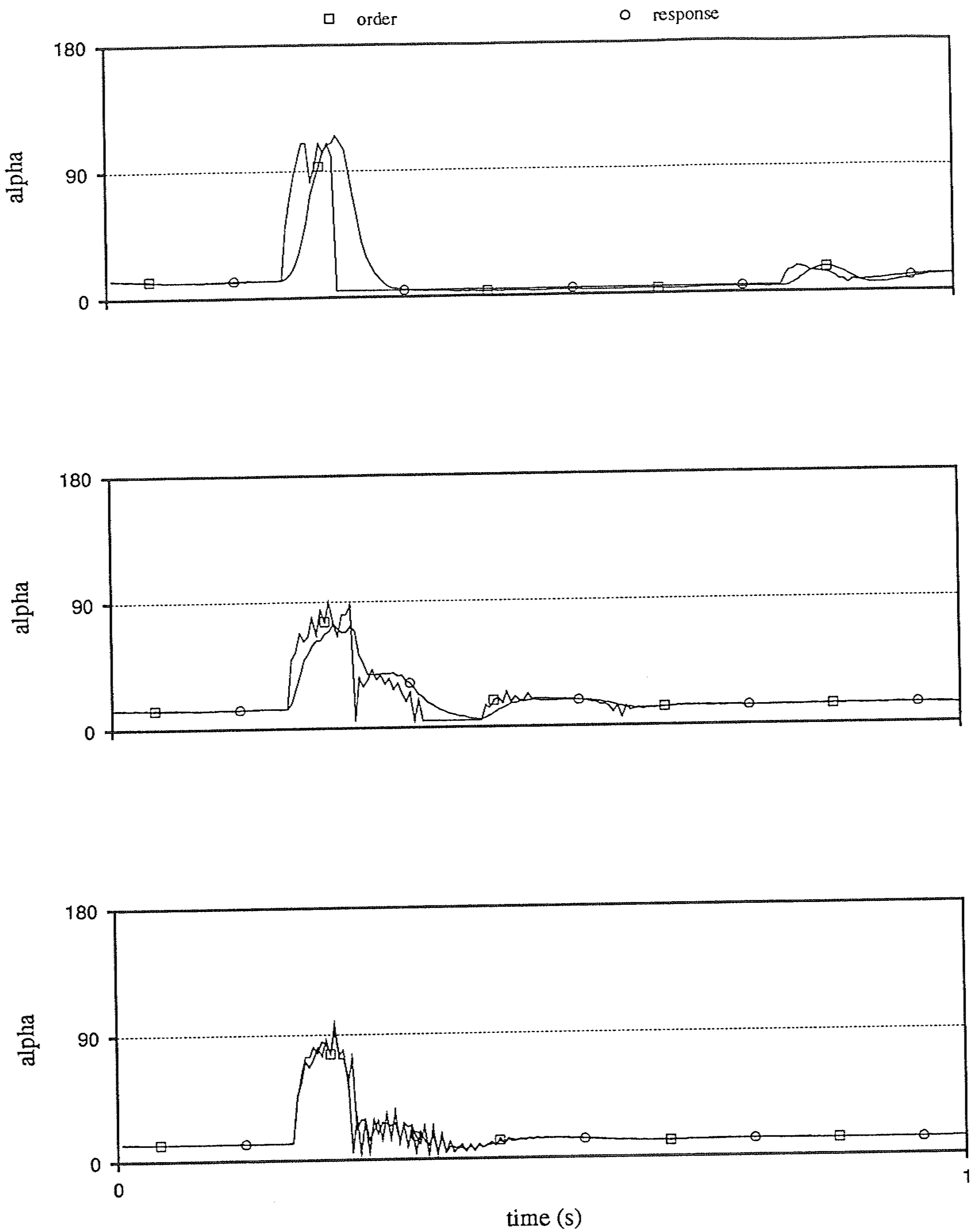

Figure 4.12 : Alpha for Single Phase Fault at Inverter

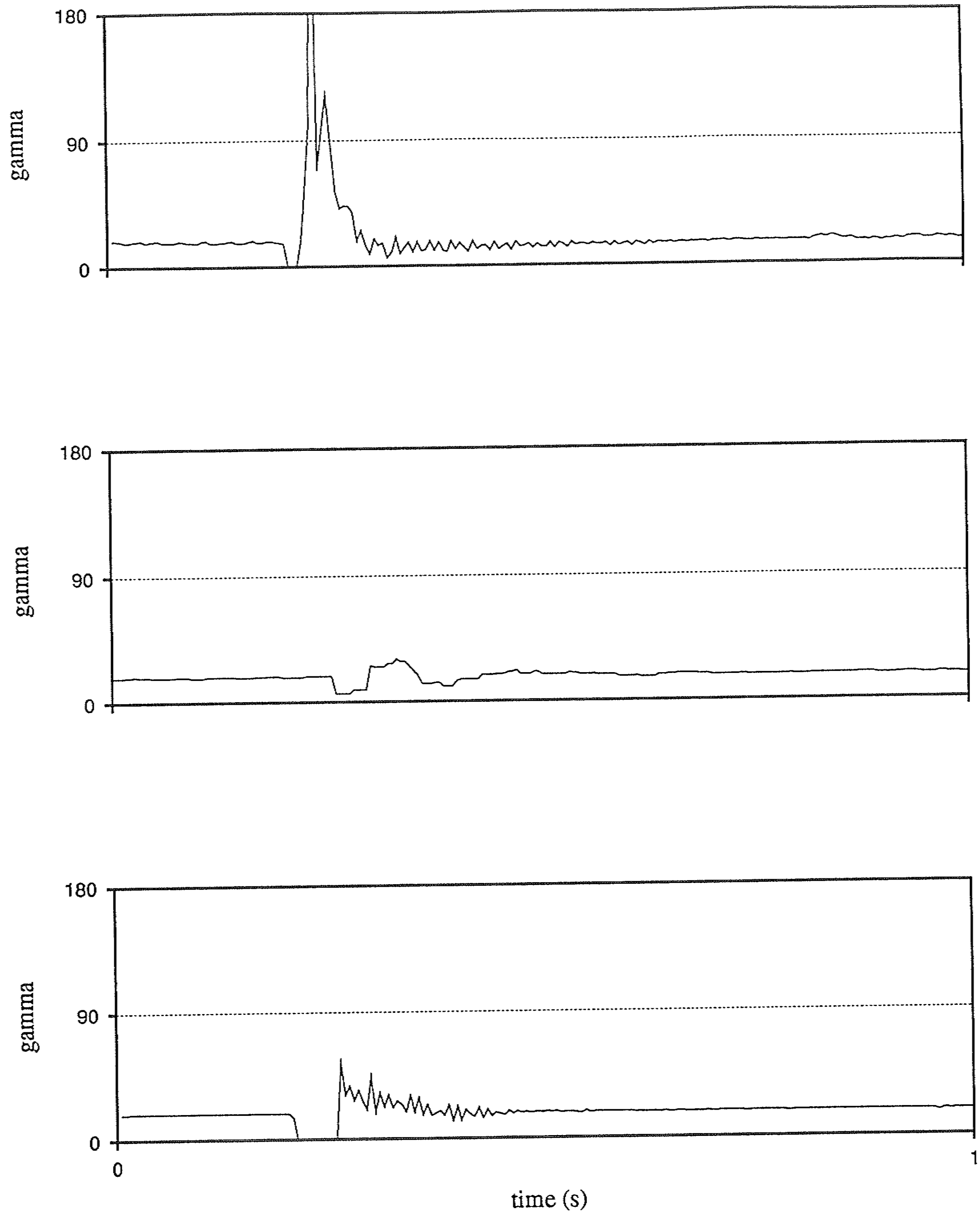

Figure 4.13 : Gamma for Single Phase Fault at Inverter

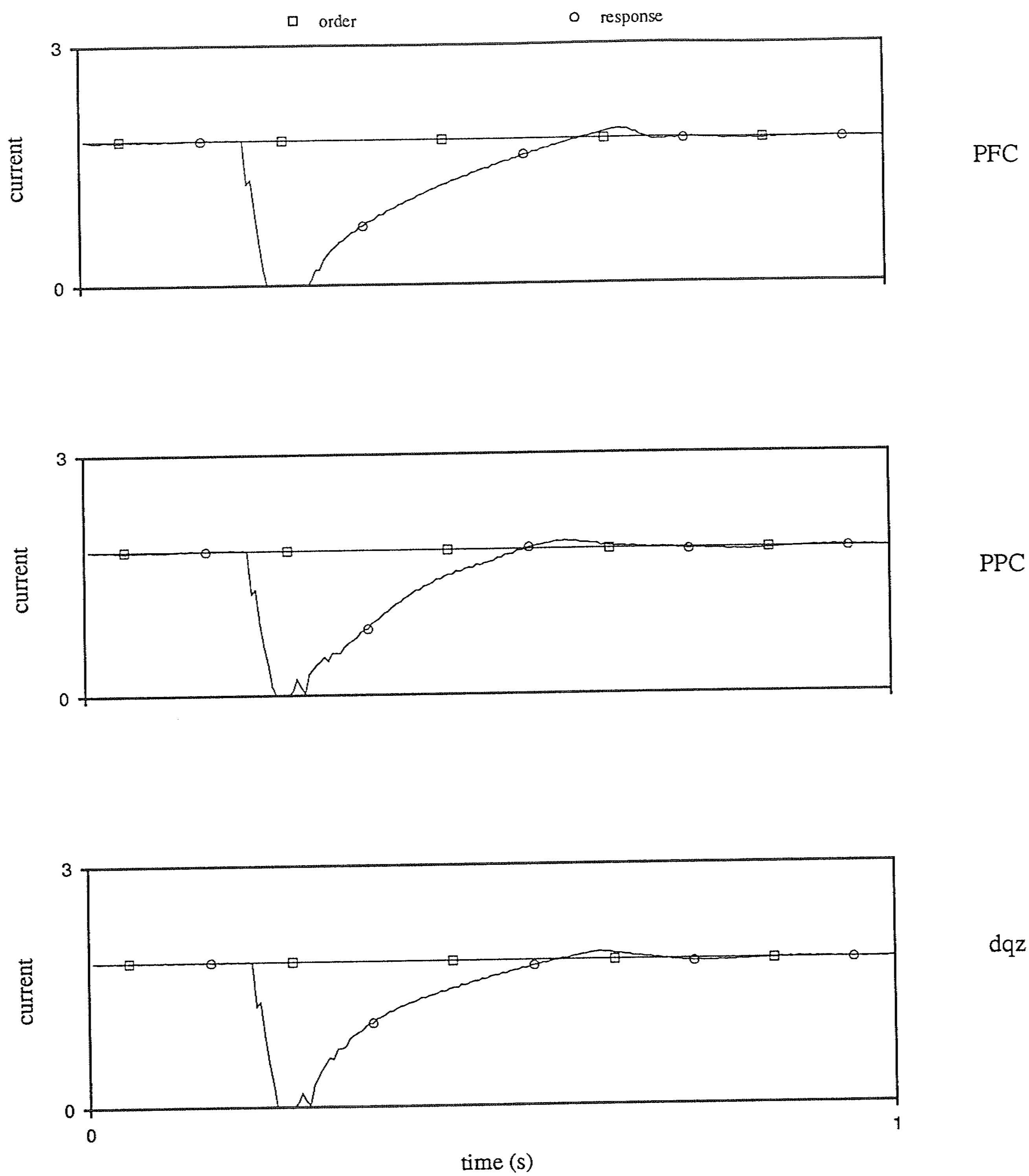

Figure 4.14 : DC Current for Three Phase Fault at Rectifier

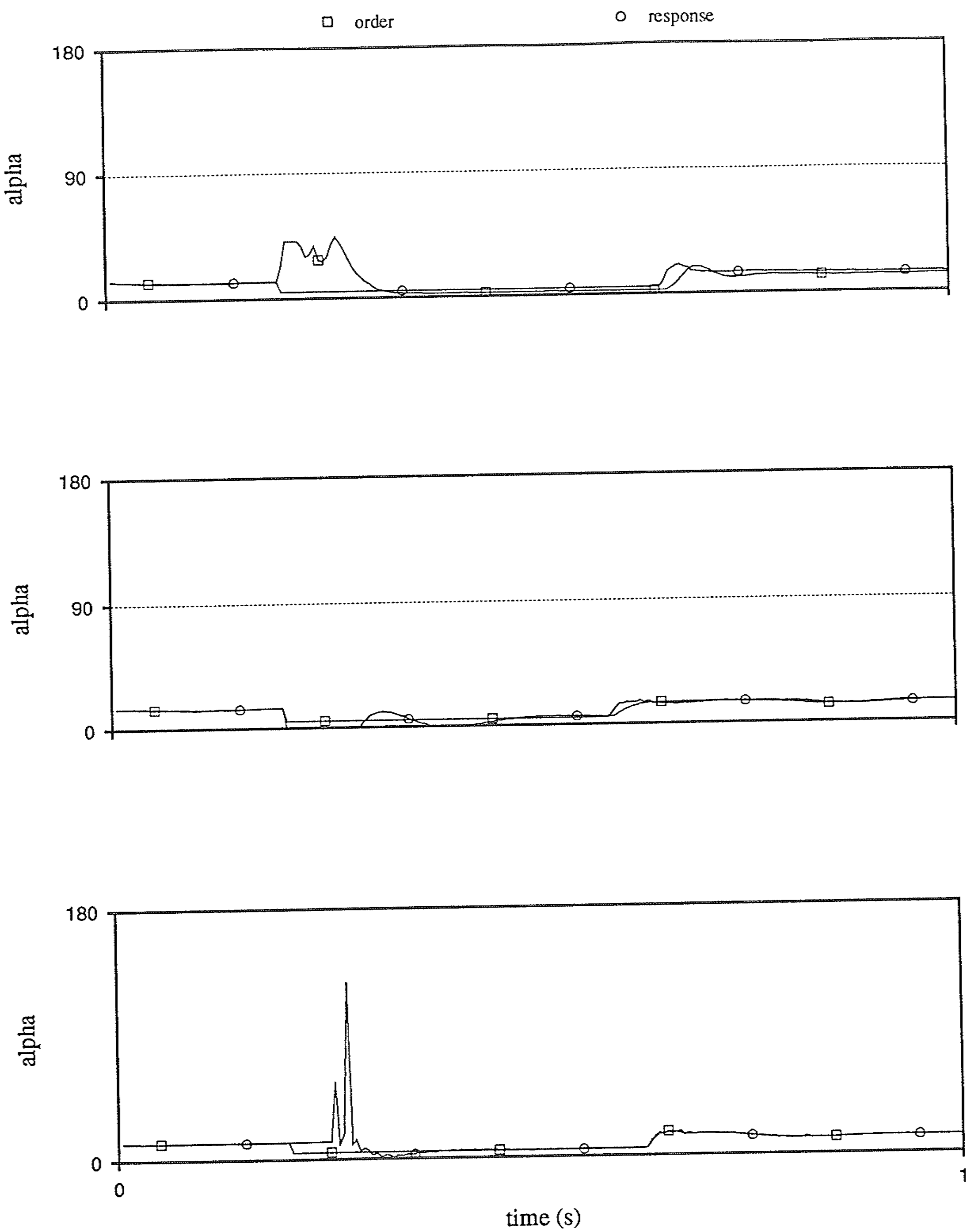

Figure 4.15 : Alpha for Three Phase Fault at Rectifier

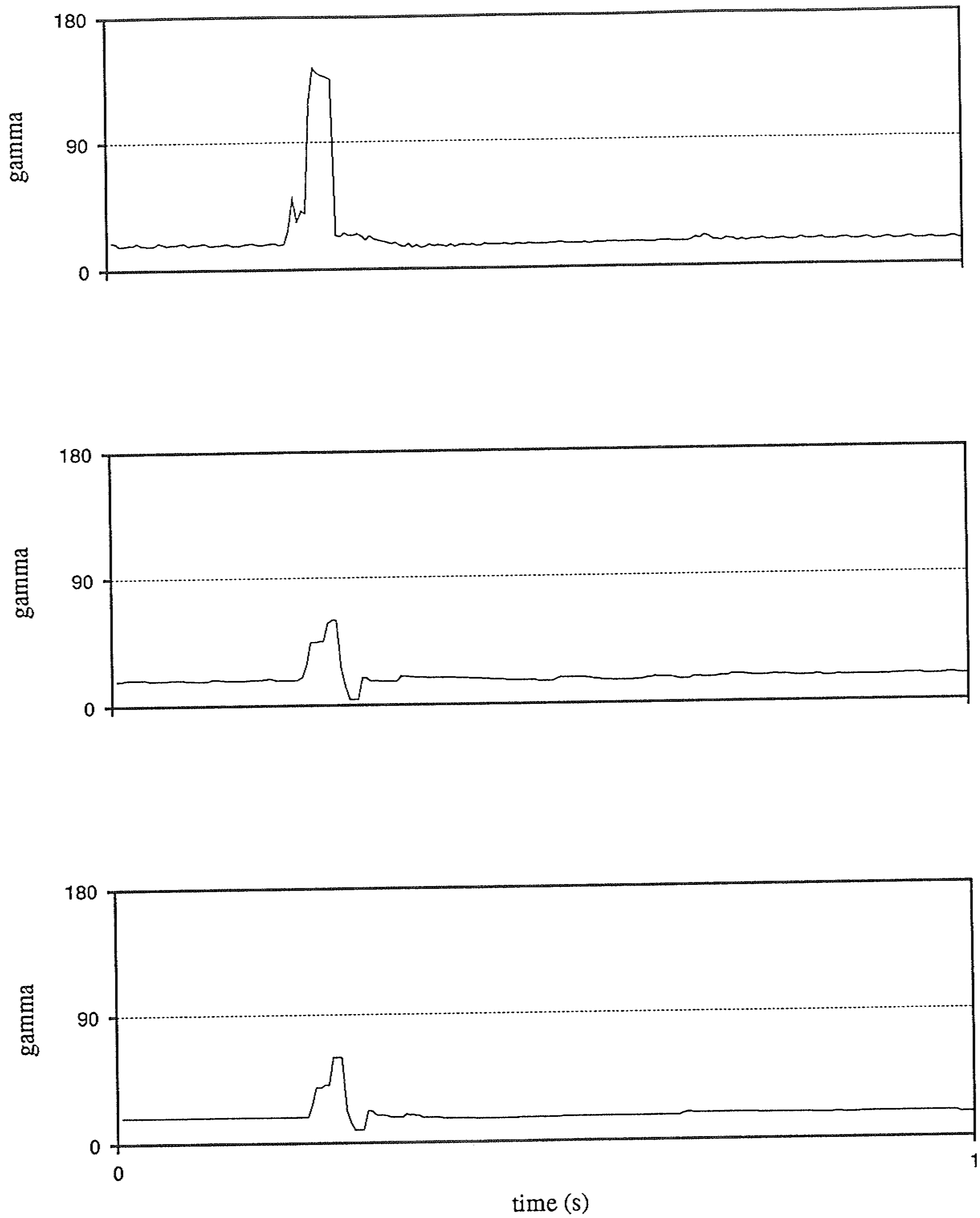

Figure 4.16 : Gamma for Three Phase Fault at Rectifier

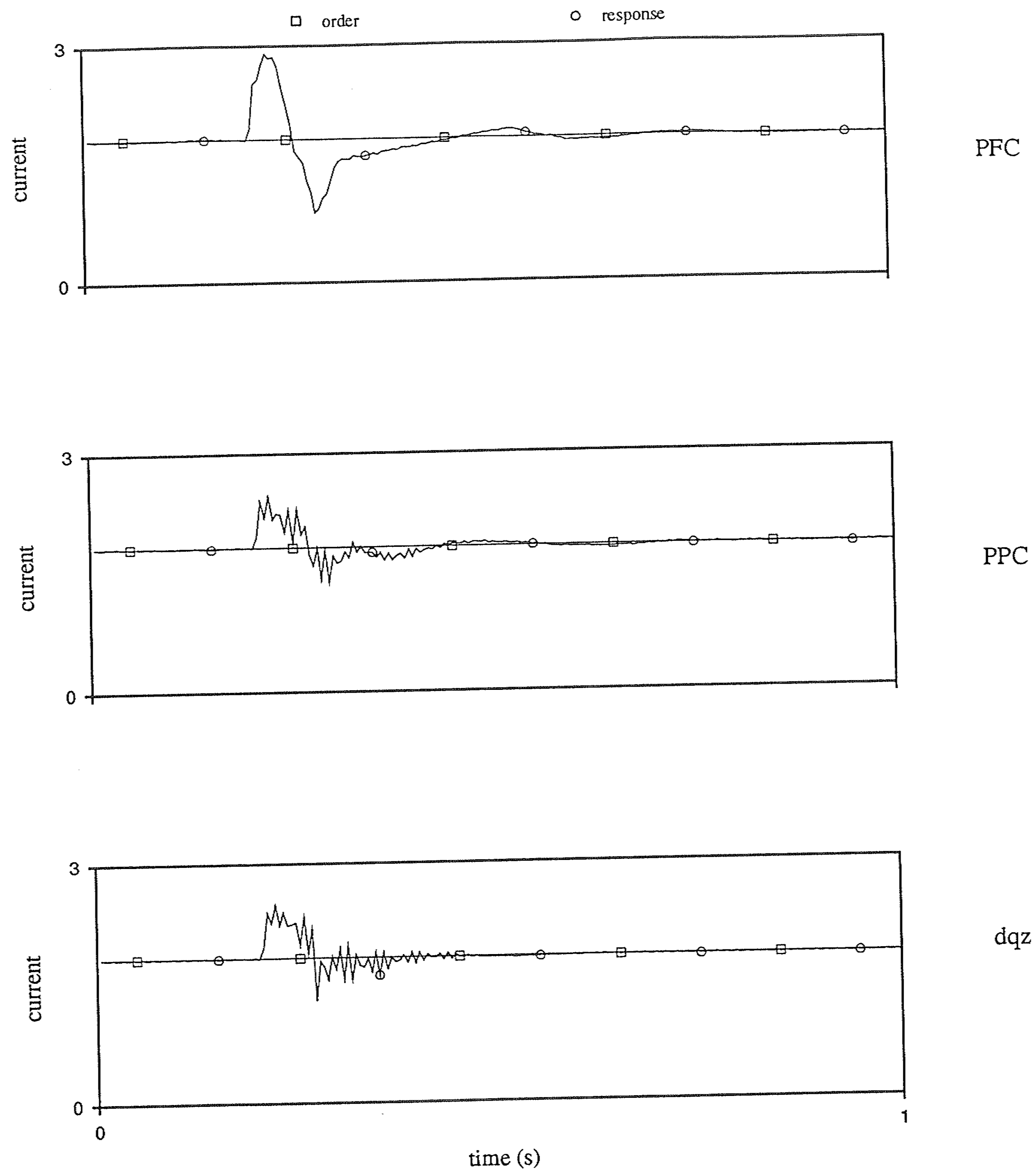

Figure 4.17 : DC Current for Three Phase Fault at Inverter

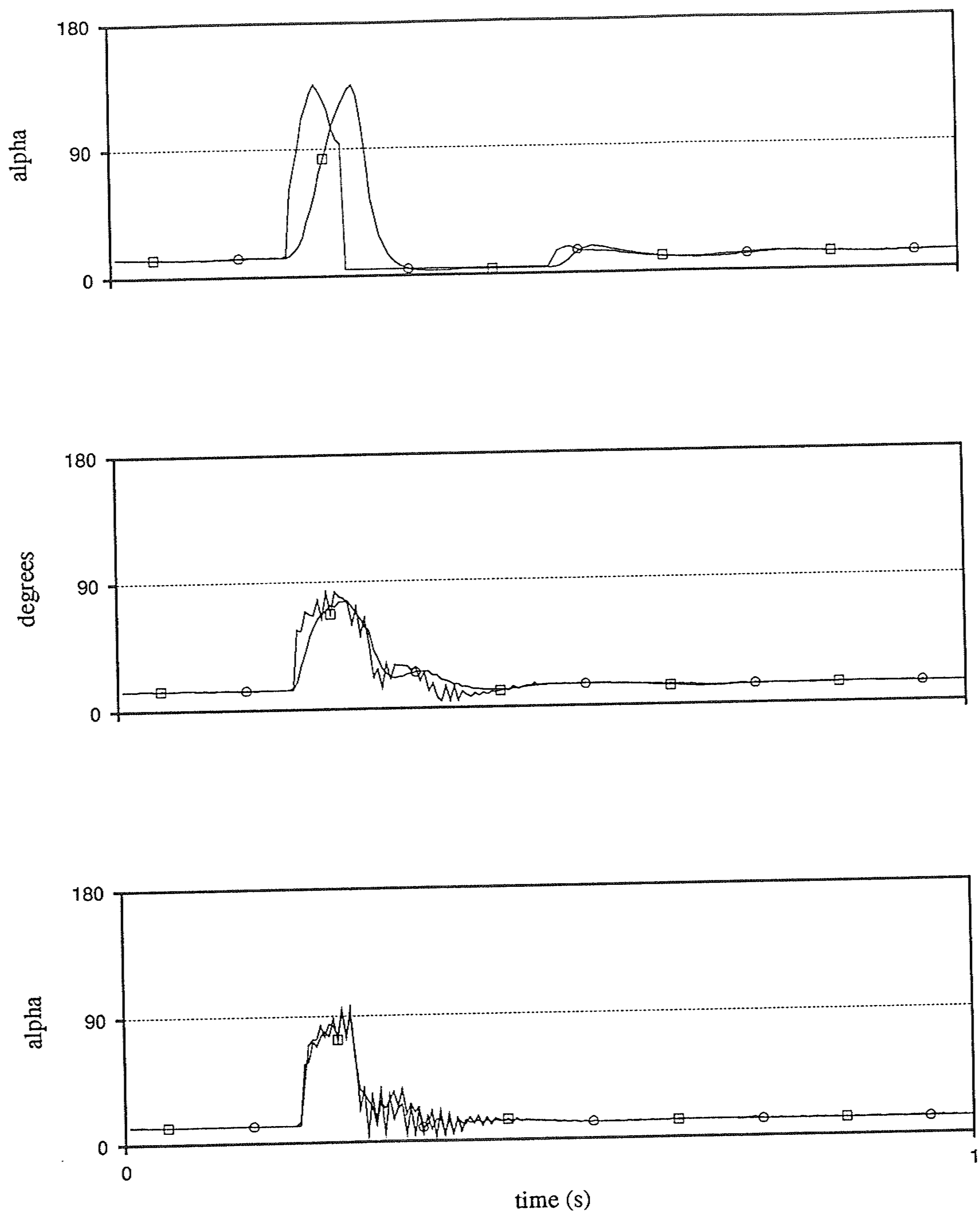

Figure 4.18 : Alpha for Three Phase Fault at Inverter

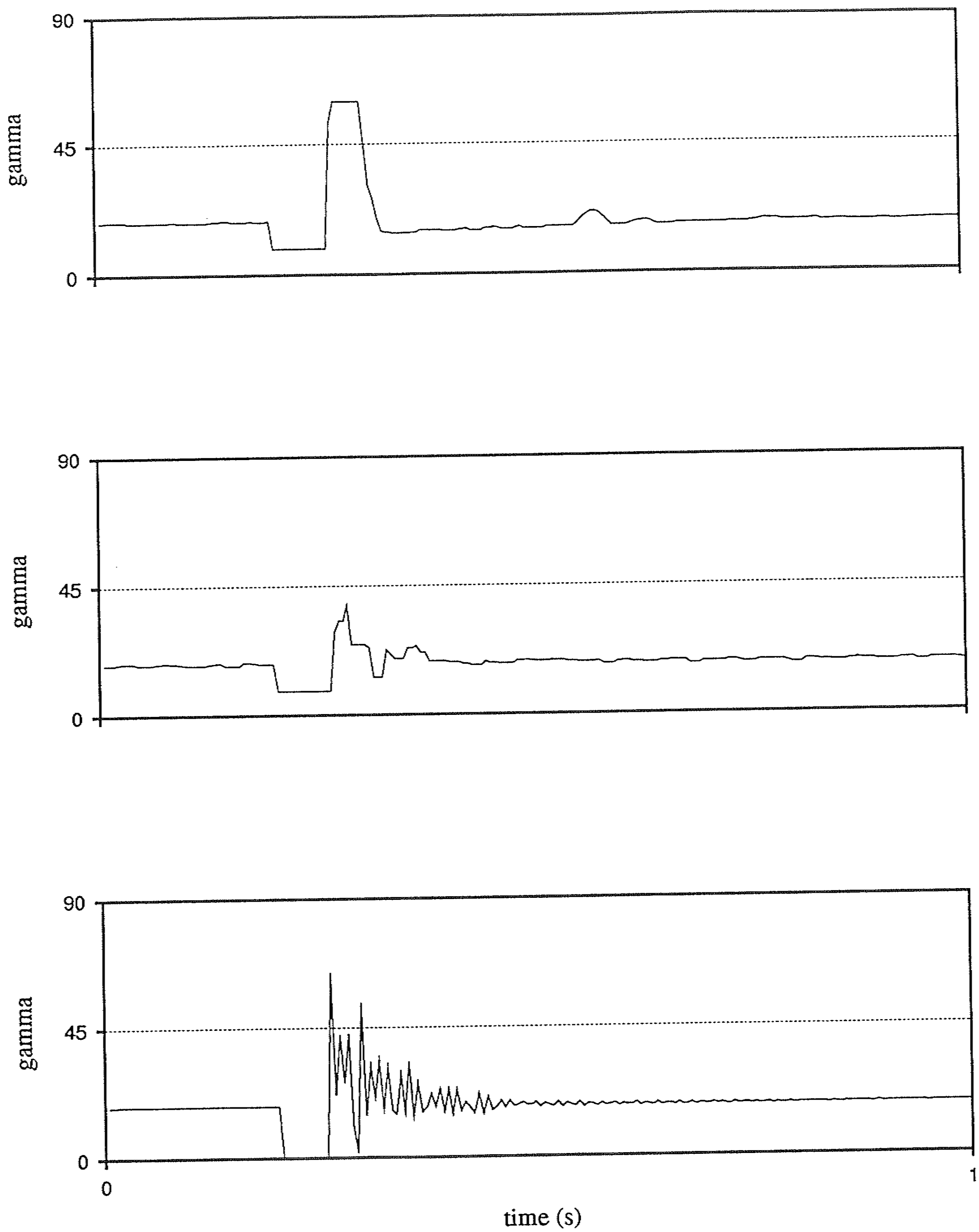

Figure 4.19 : Gamma for Three Phase Fault at Inverter

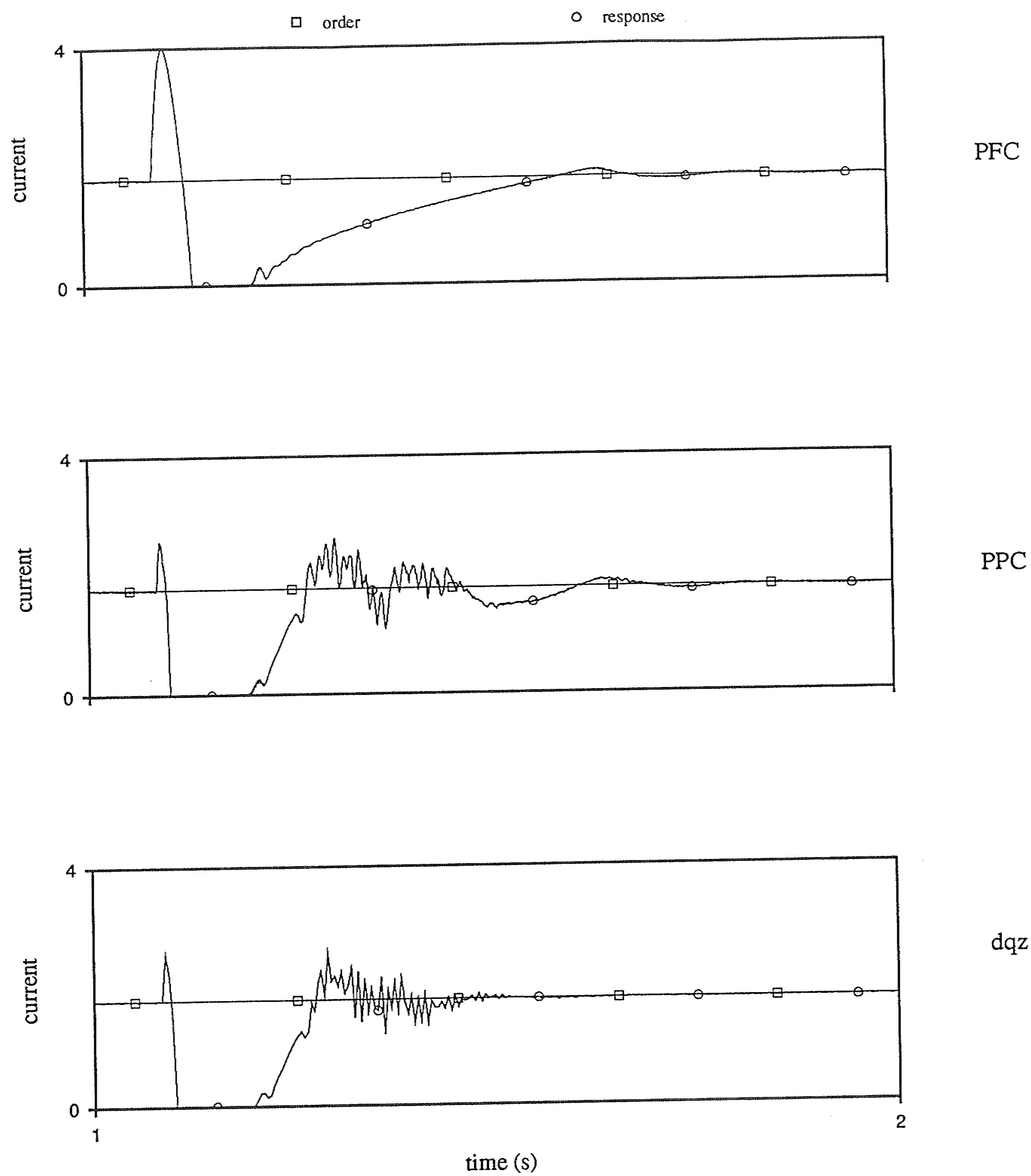

Figure 4.20 : DC Current for DC Line Fault

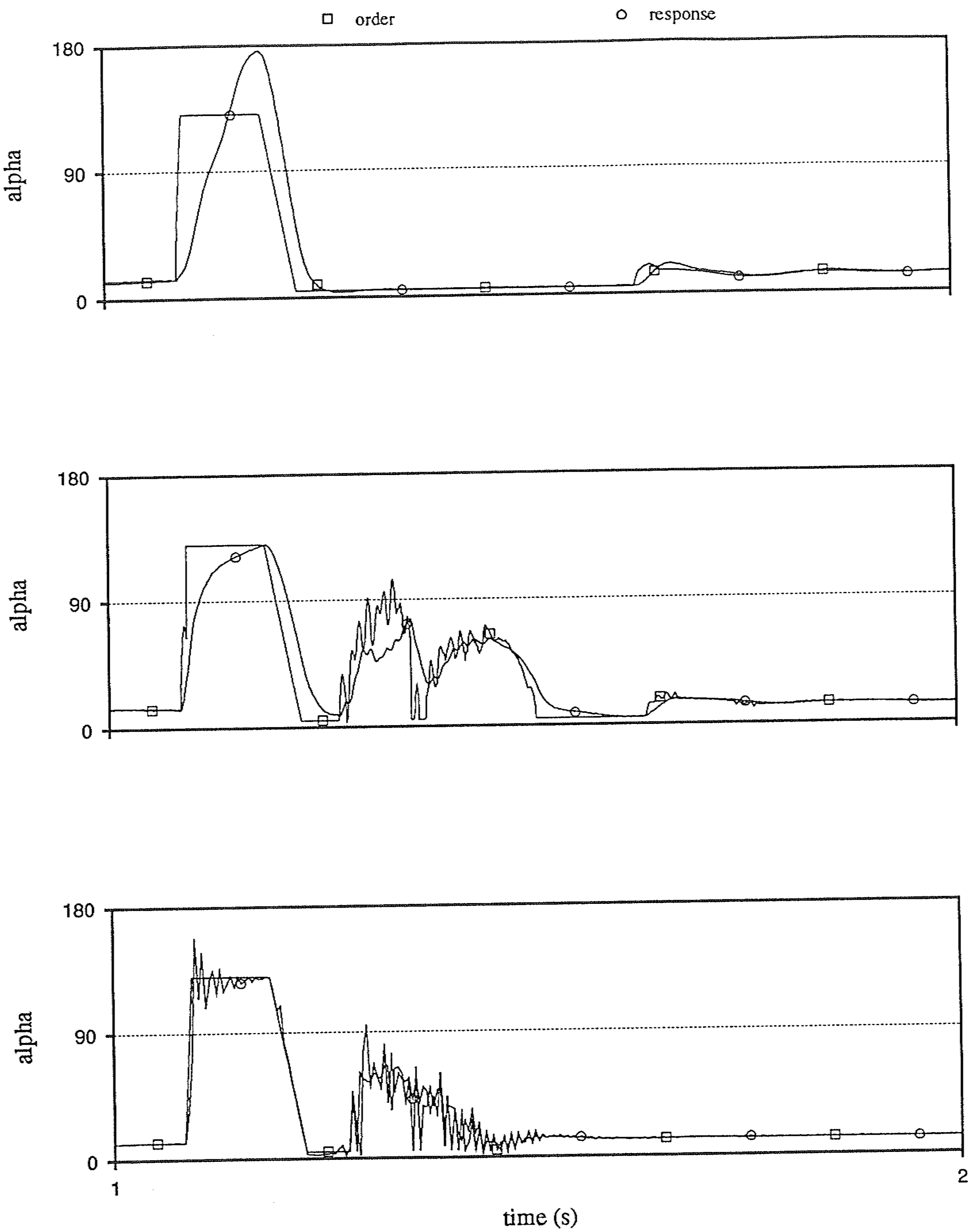

Figure 4.21 : Alpha for DC Line Fault

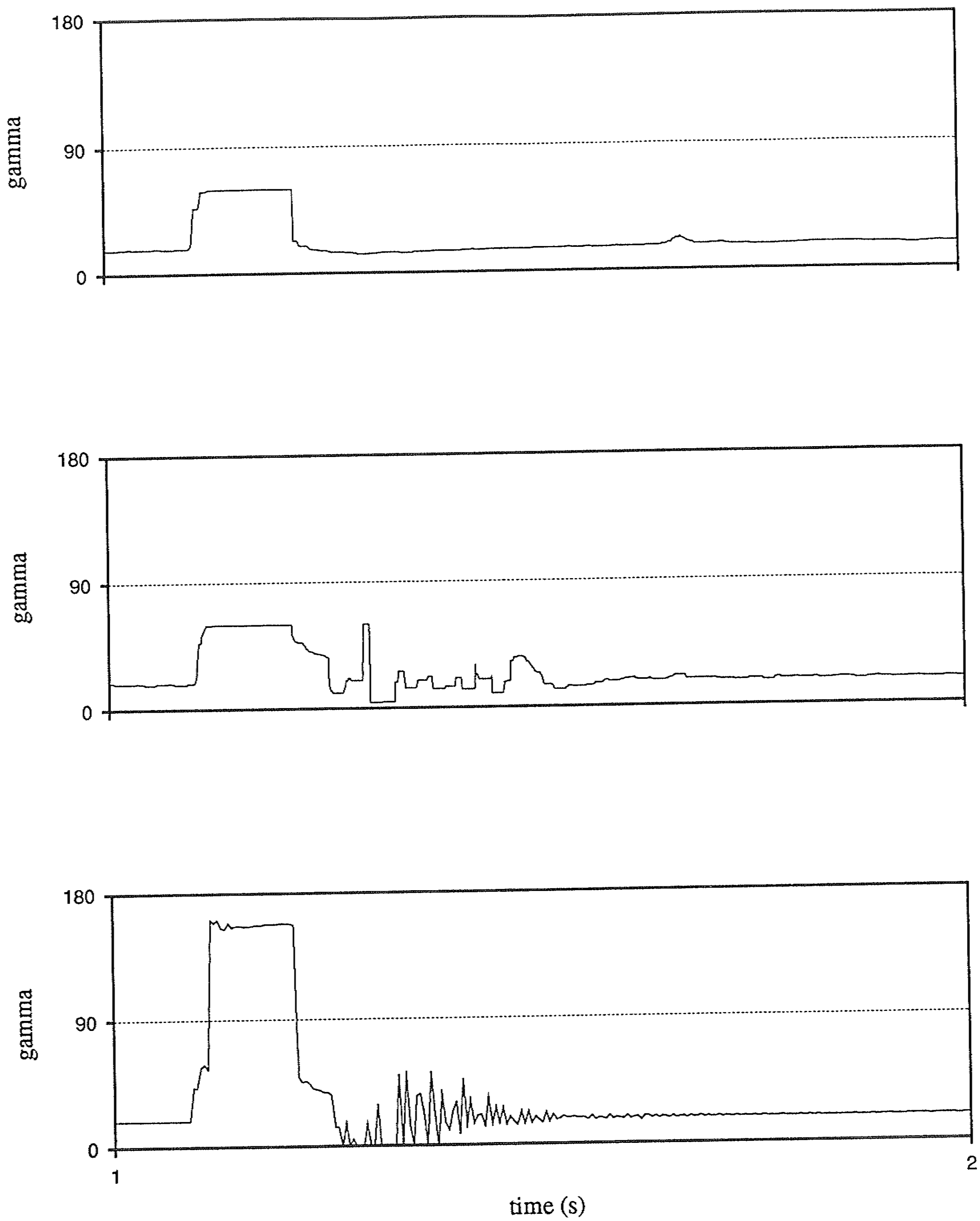

Figure 4.22 : Gamma for DC Line Fault

Chapter 5

CONCLUSION

The controls of a converter station are seen to use the incoming waveforms as a reference signal. Any distortions in the input can cause an incorrect or inefficient control system – particularly a problem in weak ac systems.

Phase locked loops are a method of "cleaning" up the input and tracking any changes in frequency or phase of this signal. Incorporating PLLs into converter control is one way of limiting the direct dependence of the firing controls on any references signal fluctuations. In this thesis three such systems are described and compared.

When trying to evaluate different controllers there are many parameters that can be discussed. The dc current response shows the dqz controller as the superior method. This value is a good indicator of the system's power recovery. One wants to regain steady state as soon as possible with a minimum of overshoot. Also, since the firing controls regulate the firing and extinction angles, these are also important to look at. The dqz Controller does the best job, with the PPC being quite comparable. The PFC is seen to be the poorest method in our tests.

Though our results have shown the dqz Controller to be the best, the PPC to be close and the PFC the least effective, it is important to note that all three controllers did manage a satisfactory recovery of the system to the various disturbances.

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