Construction of a Phasor Measurement Unit (PMU) for Power System Applications

By

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Abstract

The role played by phasor measurement units (PMU) in power grid monitoring systems today showcases the importance and usefulness of this device. There is a significant challenge regarding the design and implementation of PMUs today. This challenge stems from the closed source philosophy employed by commercial PMU vendors who strongly protect their hardware and software designs keeping it away from researchers. This philosophy has motivated a number of researchers to develop their own PMU devices.

This thesis presents the design and implementation of a PMU device utilizing off-the- shelf components to estimate power system parameters such as voltage magnitude, phase angle and frequency with key design information extracted from the OpenPMU group and the IEEE C37.118-2011 standard. The functionality of the PMU was tested by performing important power system experiments which compared measured result of voltage magnitude, phase angle and frequency of a balanced three phase signal from a rapid prototyping system with estimated results from PMU. The conducted experiments confirmed that the PMU could estimate voltage magnitude, phase angle and frequency approximately equivalent to the measured quantities of the input signal.

Acknowledgements

I would like to express my heart felt gratitude to Prof. Aniruddha Gole, for his immense contribution and guidance throughout this research. It has been a privilege to work under you as a master's student.

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Dedication

To my beloved family.

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List of Abbreviations:

TVE	Total Vector Error
LORAN-C	Long Range Navigation – Cyclan
GOES	Global Online Enrolment System
GPS	Global Positioning System
DAQ	Data Acquisition System
PCB	Printed Circuit Board
ROCOF	Rate of Change of Frequency
PMU	Phasor Measurement Unit
SE	State Estimation
PLL	Phase Locked Loop
CSV	Comma or Character-Separated Value
PDC	Phasor Data Concentrator
UTC	Universal Coordinated Time
UDP	User Datagram Protocol
IP	Internet Protocol
IEEE	Institute of Electrical and Electronics Engineers
THD	Total harmonic distortion
VILS	Voltage Instability Load Shedding
VSA	Voltage Stability Assessment
NTP	Network Time Protocol
SOC	Second-of-Century
IRIG-B	Inter-Range Instrumentation Group – Format B
OE-EMTS	Optimization Enabled EMT Simulation
USART	Universal Synchronous/ Asynchronous Receiver/ Transmitter
DMA	Direct Memory Access
OS	Operating System
FFT	Fast Fourier Transform
PC	Personal Computer
ADC	Analog to Digital Conversion
NMEA	National Marine Electronics Association
TTL	Transistor Transistor Logic

PPS	Pulse Per Second
DTE	Data Terminal Equipment
DCE	Data Communication Equipment
NI	National Instrument

Chapter 1: Introduction

1.1 Background

According to Saadat [1] the power system of today is a complex interconnected network which is split into four important parts: generation, transmission and sub-transmission, distribution and loads. The complex nature of the power system makes it necessary to regularly monitor the elements that make up the power system in order to protect these elements and in the long run avoid major contingencies in the power system. The concept of monitoring the power system network has become very important today as a result of different power system contingencies that have occurred in time past. Widespread power system outages in different parts of the world have made it necessary to monitor power system parameters such as amplitude, phase angle, and frequency to ensure that these parameters are constantly within statutory limits.

Monitoring the power system simply involves taking readings or measurements from power systems at specified time intervals while these systems are in service. Measurements of specific parameters on power systems are carried out by specific devices. One such device is

the phasor measurement unit (PMU) which is actually a key tool in providing situational awareness, operation and reliability of the power system network [2]. This thesis focuses on constructing a PMU with key design information extracted from the OpenPMU design rather than starting from scratch.

1.2 Phasor Measurement Unit (PMU)

The PMU is defined as a "*device that produces synchronized phasor, frequency, and rate of change of frequency (ROCOF) estimates from voltage and/ or current signals and a time synchronizing signal*" [3]. The history of the concept of PMU dates back to 1893 when the German-Austrian electrical engineer and mathematician Charles Proteus Steinmetz used phasor representation of waveforms to solve ac circuit problems [4].

A mathematical representation that illustrates the amplitude and phase angle of an electrical quantity or waveform is termed a phasor [5]. In the real context, PMU's are devices equipped with the functionality to estimate phasor values from electrical waveforms. One of the many applications of PMU is to capture phasor measurements from different locations and report these measurements on the same phasor diagram. The measurements collected from all locations are synchronized to a common time base with the aid of a GPS satellite navigation system. These synchronized phasor measurements are termed synchrophasors [6].

Power system engineers became interested in measuring the phase angles of voltage phasors of power network buses prior to 1980 [7]. This interest by power system engineers was as a result of the knowledge that real power flow in a power line is almost proportional to the sine of the angle difference between voltages at the two terminals of the line and again as a result of the fact that the planning and operational consideration in a power network are directly

linked with the flow of real power. The first modern application involving the direct measurement of phase angle difference was reported in early 1980 [7].

The systems concerned used LORAN-C, GOES satellite transmissions, and HBG radio transmissions to obtain synchronization of reference time at different locations in a power system.

The modern period of phasor measurement technology came into existence due to the research conducted on computer relaying of transmission lines. These transmission line relaying functions required computers to perform computation to solve six fault loop equations at each sample time which was done to ascertain if any one of the ten different types of faults possible on a three-phase transmission line are present. The computers available in the 70s were insufficient to manage these calculations to perform the transmission line relaying functions. To solve this problem, power system engineers searched for possible methods to eliminate the need to solve six equations and they came up with a new relaying technique which was based on symmetrical component analysis of line voltages and currents. Therefore positive sequence measurement which remains a crucial part of symmetrical component calculation became very important in phasor measurement. It was not until the early 1980s that these symmetrical components were put into service to build the first prototype of the modern PMU using GPS at Virginia Tech by Phadke [7, 8]. These PMU's were later distributed at a few substations in America and utilized to obtain measurements. This prototype brought about the birth of the first commercial implementation of the PMU by Macrodyne in 1991 with collaboration from Virginia Tech [8].

It should be known that the standard governing PMU devices is maintained by the IEEE C37.118 Working Group [3]. The latest standard comes in two parts; IEEE C37.118.1-2011

which describes methods and requirements for measurement verification of phasors while IEEE C37.118.2-2011 describes data exchange among measurement, data collection and application equipment.

The measurements done by PMU from different locations are transmitted to a Phasor Data Concentrator (PDC) which is defined as "*a device that combines data from several measurement devices*" [3]. It should be known that data is processed by the PDC and displayed on a user interface for users and can also be stored in a database for future use. Figure 1-1 shows the block diagram of a PMU.

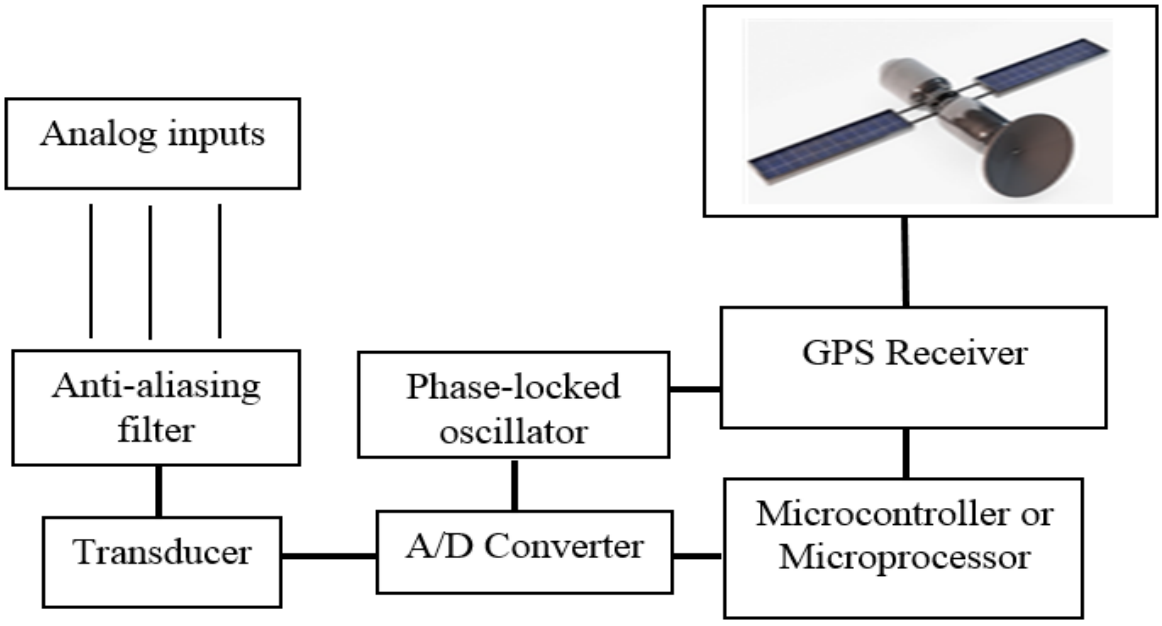

Figure 1-1 Block Diagram of PMU

1.3 Application of PMU in Power Systems

PMU has made it possible for a number of functions and roles to be possible today in the power system field. Explained below are some of the major applications of the PMU.

1.3.1 State Estimation

PMUs have become particularly useful and vital in power system state estimation (SE). Real power, reactive power injections and flows are utilized in conventional state estimation algorithms for estimation of system states (voltage amplitude and phase angle) [9]. State estimation is very important in real-time monitoring and control of the power system because it processes redundant measurements and provides steady-state operating state for advance Energy Management System (EMS) application programs [10]. It is known that traditional state estimation uses measured voltage, current, real power and reactive power to determine the operating condition of the electric network. Traditional state estimation has some limitations associated with it and these limitations are: (i) It is technically challenging and computationally more expensive to estimate the likely state of the power system based on measured parameters such as voltages, current, real power and reactive power. (ii) Traditional state estimation is usually solved in one minute interval, and this means that the result provided by the approach may be old. To overcome these technical and challenging difficulties, improved computational ability together with synchronized phasor measurement units (PMUs) are deployed to provide globally time synchronized phasor measurements with accuracy of one microseconds for bus voltages and line currents [10].

PMUs have the ability to improve SE accuracy by measuring voltage angles directly, which are the state variables to be estimated. The addition of voltage phase angle measurements to a traditional SE is capable of greatly increasing the accuracy of SE.

1.3.2 Oscillation Detection and Control

The increase in the amount of electric power that is transmitted through transmission lines is capable of causing transmission bottlenecks and oscillations of power transmission systems [10]. Basically, system oscillations originate from interconnected generators in power system. The deviation of one generator from the synchronous speed will prompt other generators in the system to provide power in order to reduce the speed deviation. However, the effect of inertia of the generators could creep in causing the entire system or part of the system to swing. In most cases, this disturbance might not be significant and would decay slowly. However, in other times, it might be very significant and does not decay which causes the system to lose synchronism and a final collapse of the system. PMUs could be used as the eye of the power system to detect oscillations early enough before they lead to critical consequences. One good example is the detection of a 0.8 Hz oscillatory mode in Eastern Denmark believed to have been of inter-area nature involving generators in Sweden and Eastern Denmark [11]. This discovery was accomplished by the DTU PMU produced at the Technical University of Denmark [12].

1.3.3 Voltage Stability Monitoring and Control

Severe changes in system conditions is enough to change the operating system of a power system dynamically [13]. Such changes affect the voltage phasor, current phasor and system frequency. Voltage stability has been known to be related to the loadability of a transmission network [10]. Different research has shown that voltage magnitude and phase angles are the best indicators of voltage stability margin.

The use of synchronized phasor measurements units (PMUs) to improve voltage stability monitoring and control has become very efficient. This is possible through the following applications:

- Voltage Instability Load Shedding (VILS)
- Wide Area Voltage Stability Monitoring and Control

Under the VILS approach, PMUs are used to monitor the electric network to track how close the transmission system is to its loadability limit. If the system is very close to that limit, and every other approach has been exhausted to avoid voltage collapse without significant improvement, the VILS scheme is then deployed as the last safety option to prevent voltage collapse in the system. The shedding of load is done in pre-defined blocks that are usually triggered in stages due to scheduled maintenance, and unexpected disturbances [10, 13] . PMUs provide measurement-based on-line voltage stability monitoring and control which has the ability to improve the power transfer limits and increase security of the system operation [10].

Under the Wide Area Voltage Stability Monitoring and Control scheme, computer simulation tools are used to help operators monitor and control system voltage stability. One good tool used is a Voltage Stability Assessment (VSA) program which relies on state estimators to provide steady-state solution [10].

1.3.4 Protection of Power Systems

A number of severe protection problems have been resolved by PMUs [6]. Examples of protection problems include: Protection of series compensated lines, protection of multi-terminal lines, and the inability to satisfactorily set out-of-step relays. The reliable

measurement of voltage or current is possible to offer substantial improvement in protection functions.

Furthermore, the communication of such measurements from one end of a protected line to another is necessary to improve protection functions. These measurements offered by PMUs are effective in improving protection functions which have relatively slow response time [9]. The latency of remote measurements for such protection functions, is not really a significant issue. The differential protection of buses, transformers and generators is a well-established protection principle that emphasizes the importance of synchronized phasor measurements. True differential protection was not possible before the introduction of synchronized phasor measurements. Differential protection is important for series compensated lines and tapped lines. Differential protection involves communication wires or communication band channels. The easy availability of synchronized measurements using GPS technology and the improvement in communication technology makes it possible to consider true differential protection of transmission lines and cables.

The chapters that make up this thesis are:

Chapter 1: Introduction

This chapter simply gives a brief introduction and background of PMUs as well as its importance and application in power system.

Chapter 2: The IEEE Synchrophasor Standard

This chapter gives a vivid description of the standard that guides the operation, design and implementation of a synchrophasor. It defines the methods for evaluating the measurements and requirements for compliance of synchrophasors with specific evaluation tests under

steady-state and dynamic conditions. This chapter also describes the modification made to these standards over the years as well as providing a literature review of different PMUs.

Chapter 3: Design and Implementation of the PMU

Chapter 3 of this thesis provides the method used in the design of the PMU device. It gives a description of the hardware circuit design as well as providing a description of how the software aspect of this design was implemented.

Chapter 4: Hardware Testing and Analysis of Result.

With the PMU designed and implemented, the next stage involved testing the PMU based on defined experiments to check its mode of operation and verify if the obtained outputs are within specified compliance limits. Therefore results obtained from the PMU device will be presented in chapter 4 and analyzed.

Chapter 5: Conclusion and Future Work

This chapter will highlight the major contributions achieved by this thesis. The challenges of the thesis is presented and finally future or further work will be stated as well.

Chapter 2: The IEEE Synchrophasor Standard

This chapter introduces the standards that guide the design, implementation and operation of a synchrophasor or phasor measurement unit. The standard simply defines a synchrophasor, frequency, and rate of change of frequency (ROCOF) measurements as well as defining the method of exchange of synchronized phasor measurement data between power system equipment. An investigative study has been performed on synchrophasor standards, starting with the first standard released by the IEEE Synchrophasor working group down to the latest standard used today. The literature of some PMU technology platforms is also covered in this chapter.

2.1 The IEEE 1344-1995 Synchrophasor Standard

This standard remains the first PMU standard. It was approved on 12 December 1995 by the IEEE Standards Board and re-affirmed on 17 March 2001. The synchronization of data sampling, data-to-phasor conversions, and formats for timing input and phasor data output from a PMU are all addressed in this standard [14]. Response time, accuracy, hardware, software, or the process for computing phasors are not addressed in this standard.

This standard was born out of the developments and need in power system to record time-tag, transmit, and analyze power system phasor quantities in real time. This standard specifies that phasor measurements shall be referenced and synchronized to Coordinated Universal Time (UTC) derived from a synchronizing source. This synchronizing source is distributed by direct method or by broadcast and can be local or global. The signal from the synchronizing source is needed to provide time information to determine second –of-century (SOC) which has to be in agreement with UTC. The basic repetition rate of this synchronizing signal shall be 1 pulse per second (1PPS) with a stability of at least 1E-07.

On time input, the standard specifies that UTC time and synchronization shall be provided to the PMU using IRIG-B and 1PPS or using any high-precision format time code. The standard with respect to data samples allows data to be tagged with UTC time during the second the sample is taken. This time tag is derived in accordance with the network time protocol (NTP) and it is a 4 B binary SOC number. The SOC number is defined by the standard as *"the UTC time in seconds calculated from midnight of January 1, 1900*" [14]. The addition or subtraction of Leap seconds from the scale is necessary to keep NTP synchronized with UTC. Time tag for phasors consist of two words. The first word is a 4 B word which provides the SOC time in the NTP time scale while the second word is a 2 B SMPCNT which provides the sample number of the last sample used in the calculating phasor. Sample number "0" is the sample taken on the 1 s mark. If the convention $v(t) = \sqrt{2}\,V\cos(\omega_0 t + \varphi)$ is applied, the phasor $Ve^{j\varphi}$, is obtained. It should be known that the phasor computed from a window starting at positive voltage maximum is real while the one computed from a window starting from positive going voltage zero is negative imaginary as shown in Figure 2.1.

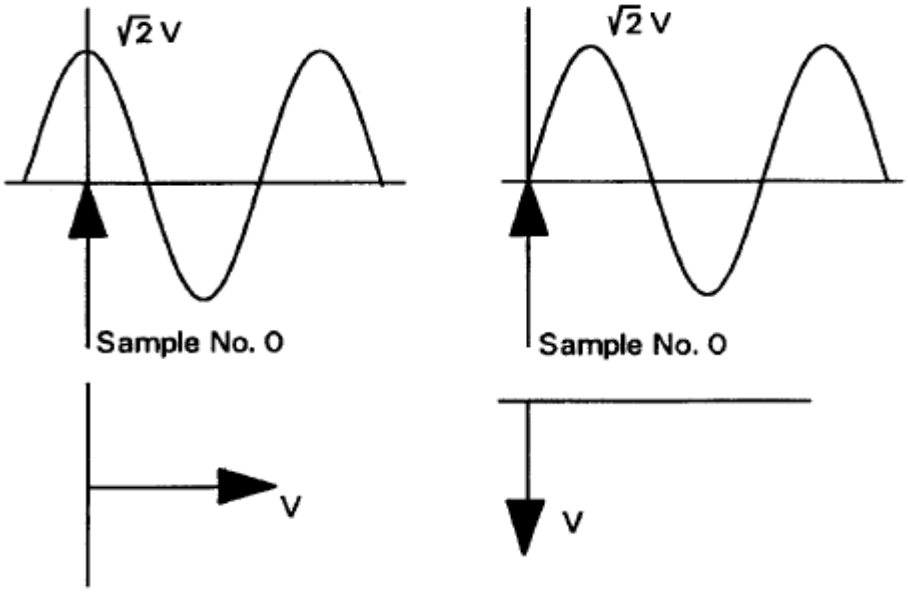

Figure 2- 1 Convention for phasor representation [14]

Similarly, the measured phasor corresponding to a sinusoidal signal $v(t) = \sqrt{2}\,V\cos(\omega_0 t + \varphi)$ with a frequency $\omega_0$is $Ve^{j}(\omega_0 t_0 + \varphi)$. This phasor will be obtained if the 1PPS signal occurs at a given time t_0. The measured phasor with time-tag that corresponds to the 1PPS instant is $Ve^{j}(\omega_1 t_0 + \varphi)$ for steady-state signals during off-nominal frequency ω_1

The message format of the PMU allows three types of information organized as frames to be transmitted. These frames are: Data frame, Header frame and Configuration frame. The definition of each frame is given in Table 2. 1.

Table 2. 1 Transmitted data frame [14]

Bits 15–14–13	Frame type	Definitions
000	data frame	Bits 0–12: sample count, 0–8191
001	header frame	Bit 12: first frame flag (0: first frame of header file, 1: continuing frame) Bit 11: last frame flag (0: not last frame, 1: last frame of file) Bits 0–10: frame count for file, 0–2047 (first frame is count 0)
010	configuration frame	Bit 12: first frame flag (0: first frame of configuration file, 1: continuing frame) Bit 11: last frame flag (0: not last frame, 1: last frame of file) Bits 0–10: frame count for file, 0–2047 (first frame is count 0)
011–100	reserved for expansion	Bits 0–12: to be assigned
101–111	user defined	Bits 0–12: user defined

The data frame contains measured data and it is identified by having the three most significant bits of the third word (5th byte) equivalent to zero. Figure 2-2 shows a transmitted data frame.

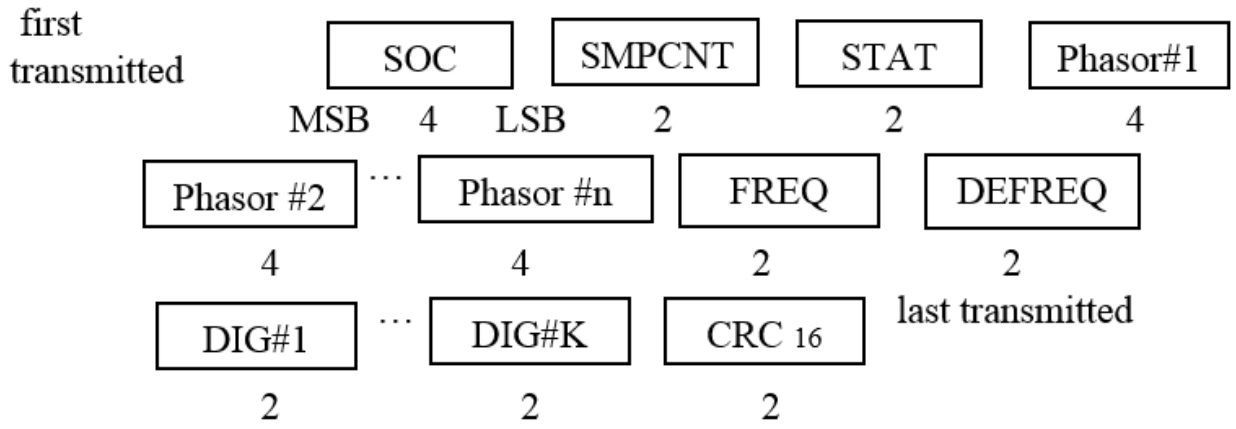

Figure 2-2 Data frame configuration [14]

The header frame is specified by the synchrophasor standard as an ASCII file. It contains information about the PMU which include: the data source, scaling, transducers, algorithms, analog filters used, etc. Figure 2-3 shows a transmitted header frame.

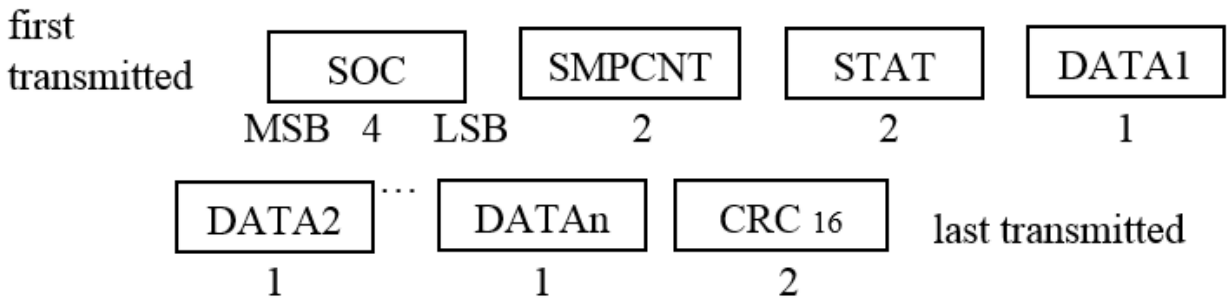

Figure 2-3 Header frame organization [14]

The configuration frame is specified to be a machine-readable binary file that contains information about processing parameters that are related to real-time data frame. Figure 2-4 shows a transmitted configuration frame.

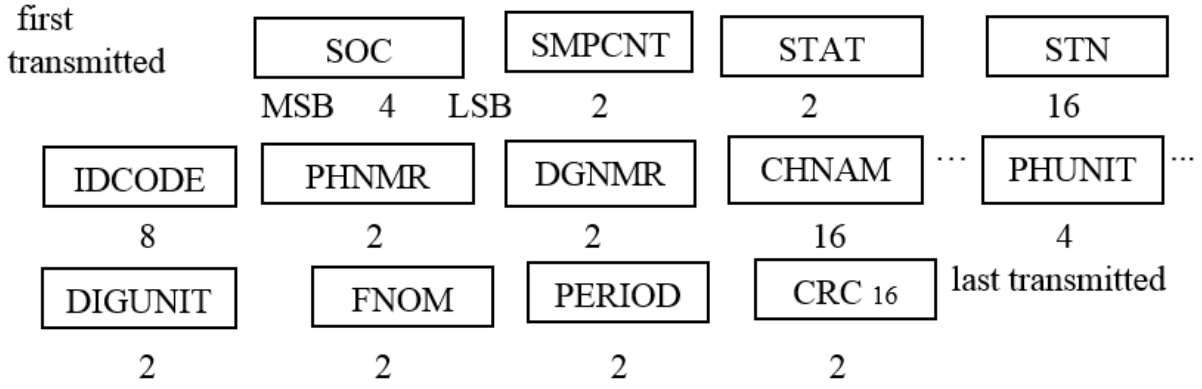

Figure 2-4 Configuration frame organization [14]

The standard also allows the PMU to receive commands from a control system and take appropriate actions. The received message frame is shown in Figure 2-5.

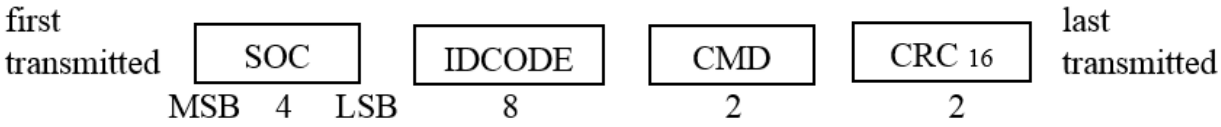

Figure 2-5 Received command frame organization [14]

Table 2. 2 shows the definition of the commands received by the PMU.

Table 2. 2 Synchrophasor command definition [14]

Command word bits	Definition
Bits 15-4	Reversed for future use
Bits 3-2-1-0:	
0001	Turn off real-time data
0010	Turn on real-time data
0011	Send HDR file
0100	Send CFG-1 file
0101	Send CFG-2 file
1000	Receive reference phasor in data frame format

2.2 The IEEE C37.118-2005 Synchrophasor Standard

This standard was approved on 21 October 2005 by the IEEE-SA Standards Board and approved on 1 February 2006 by the American National Standards Institute [15]. This standard contains definition for synchronized phasor measurement, methodology of quantifying these measurements, and specifications for quality test. Definition of data transmission formats for real-time data reporting is also contained in this standard. The IEEE C37.118-2005 standard gives a better description of synchrophasor measurement. This standard introduces the mathematical definition of a synchrophasor from a pure sinusoidal waveform $x(t) = X_m \cos(\omega t + \emptyset)$.

$$X = X_r + X_i \tag{2-1}$$

$$= (X_m/\sqrt{2})e^{j\emptyset}$$

$$= X_m/\sqrt{2}(cos\emptyset + jsin\emptyset)$$

"Where $X_m/\sqrt{2}$ is the rms value of the signal $x(t)$ and $\emptyset$ is the instantaneous phase angle relative to a cosine function at nominal system frequency synchronized to UTC" [15] . This angle is 0^0 when the maximum of $x(t)$ occurs at the UTC second rollover (1PPS time signal), and -90^0 when the positive zero crossing occurs at the UTC second rollover. This is shown in Figure 2-6.

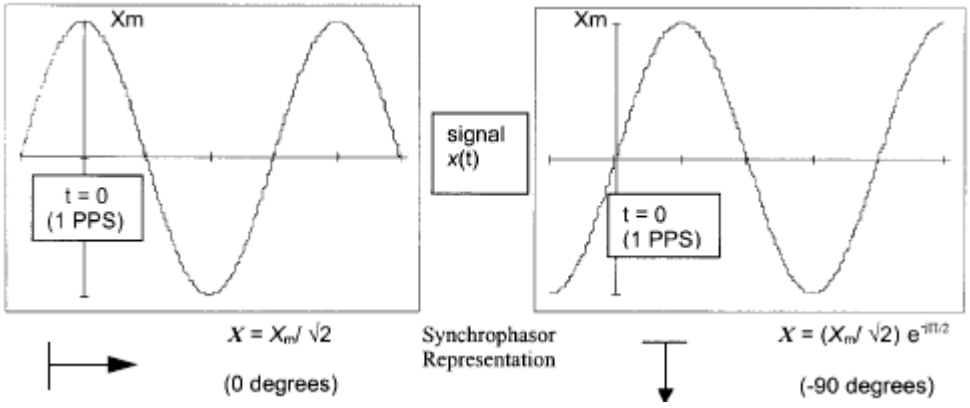

Figure 2- 6 Convention for synchrophasor representation [15]

For off-nominal frequency signals, the phasor representation of a sinusoid is independent of its frequency. Sinusoids can be observed at intervals {0, T_0, $2T_0$, $3T_0$…, nT_0, …} which corresponds to the following phasor representation {X_0, X_1, X_2, $X_{3,...}$}. A constant phasor is obtained at each observation if the interval T_0 becomes equal to an integer multiple of the period of the sinusoid $T = {}^{1}/_{f}$.

The observed phasor will have a constant magnitude if T_0 is not an integer multiple of the period. In this case, the angles of the sequence of phasors {X_0, X_1, X_2, $X_{3,...}$} will change uniformly at a rate $2\pi(f - f_0)T_0$, where $f_0 = {}^{1}/_{T_0}$. This is explained in Figure 2-7

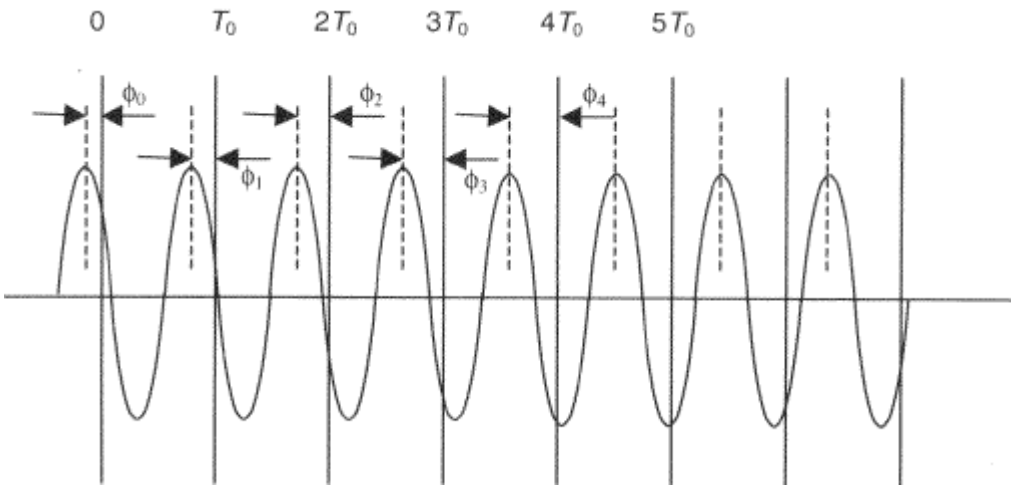

Figure 2-7 A sinusoid with period of T [15]

This standard made some modifications to the tagging of synchrophasor measurements from the former IEEE Std. 1344-1995 standard. Under this new standard, synchrophasor measurement became tagged with UTC time consisting of three numbers which are: a second-of-century (SOC), a fraction-of-second count, and a time status value. This is an improvement from the previous standard which had only the SOC number.

The IEEE Std. 1344-1995 standard, never specified accuracy for computing phasors which is necessary to obtain correct synchrophasor measurements. The new standard allows the synchrophasor measurements to be synchronized to UTC with accuracy sufficient to meet the accuracy requirements of this standard.

A concept known as the total vector error (TVE) was introduced under this standard. The TVE is defined as "*the magnitude of the vector difference between the theoretical phasor defined in equation 2-1 and the phasor estimate given by the measuring device, expressed as a fraction of the magnitude of theoretical phasor as shown in equations 2-2*" [15].

$$TVE = \sqrt{\frac{(X_r(n)-X_r)^2+(X_i(n)-X_i)^2}{X_r^2+X_i^2}} \tag{2-2}$$

The standard specified a time error of $1\mu s$ to correspond to a phase error of 0.022^0 for a 60Hz system and 0.018^0 for a 50 Hz system. A phase error of 0.57^0 will itself cause 1% TVE as defined in equation 2-1. Therefore a 60Hz system, and a 50Hz system will have a maximum time error of $\pm 26\mu s$ and $\pm 31\mu s$ respectively.

Furthermore, a new rate was introduced for transmitting synchrophasor estimates. The standard allows synchrophasor estimates to be obtained and transmitted as data frames at a rate F_s which is an integer number of times per second or integer number of seconds per frame as specified by the DATA_RATE variable contained in the configuration frame. This standard proposes that the PMU shall support data reporting (by recording or output) at submultiples of the nominal system frequency. Table 2.3 shows the required rates for 50Hz and 60Hz systems.

Table 2. 3 Required PMU reporting rates [15]

System frequency	50 Hz		60 Hz				
Reporting rates (F_s- frames per second)	10	25	10	12	15	20	30

If a reporting rate of N frames per second is to be reported, the reporting times is evenly spaced by each second with frame number 0 (numbered 0 through N-1) being coincident with the UTC second roller. The instantaneous values of the synchrophasor definition are determined using the reporting times.

Compliance verification is another new concept introduced in the IEEE C37.118-2005 standard. This concept allows compliance tests to be performed by comparing the phasor estimates obtained under the steady-state conditions to the corresponding theoretical values of $X_r$and X_i and calculating TVE. The steady-state condition is defined under this standard as "*conditions where $X_m, \omega, and\ \emptyset$ of the test signal, and all other quantities are fixed for the*

period of the measurement" [15]. The standard also requires a calibration device to verify performance. This is in accordance with compliance verification in the standard traceable to national standards and must have a "test accuracy ratio" of at least four compared with TVE measurement within 0.25% where TVE is 1%. A detailed analysis is required to be performed demonstrating compliance with these requirements in situations where no national standard exist to establish traceability. The standard specifies all compliance test to be carried out under steady state conditions. This must be performed with reference conditions and influence quantities as defined in Table 2. 4.

Table 2. 4 Influence quantities and allowable error limits for compliance levels 0-1 [15]

Influence quantity	Reference condition	Range of influence quantity change with respect to reference and maximum allowable TVE in percent (%) for each compliance level			
		Level 0		Level 1	
		Range	TVE (%)	Range	TVE (%)
Signal frequency	$F_{nominal}$	± 0.5 Hz	1	± 5 Hz	1
Signal magnitude	100% rated	80% to 120% rated	1	10% to 120% rated	1
Phase angle	0 radians	± π radians	1	± π radians	1
Harmonic distortion	<0.2% (THD)	1%, any harmonic up to 50th	1	10%, any harmonic up to 50th	1
Out-of-band interfering signal, at frequency f_i where $\|f_i - f_0\| > F_s/2$, F_s = phasor reporting rate, $f_0 = F_{nominal}$	<0.2% of input signal magnitude	1.0% of input signal magnitude	1	10% of input signal magnitude	1

In the IEEE C37.118-2005 standard, message format was updated from the original standard to improve information exchange with other systems, such as a master station. Specifically, the sync, frame size, and station identification fields have been added to the data frame, configuration frame, header frame, and command frame. It will also be recalled that the previous standard never had a command frame. The command frame is therefore a new frame added, being a machine-readable code sent to the PMU/data concentrator (DC) for control or configuration. Table 2. 5 shows the command frame organization.

Table 2. 5 Command frame organization [15]

No.	Field	Size	Comment
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2.
4	SOC	4	SOC time stamp, defined in 6.2.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2.
6	CMD	2	Command being sent to the PMU/DC.
7	EXTFRAME	0–65518	Extended frame data, 16-bit words, 0 to 65 518 bytes as indicated by frame size, data user defined.
8	CHK	2	CRC-CCITT check

The data frame is now identified by having bits 4 - 6 in the SYNC word set to zero. The frame starts with SYNC, FRAMESIZE, IDCODE, and SOC, and terminates with a CRC-CCITT. Table 2. 6 shows the data frame organization.

Table 2. 6 Data frame organization [15]

No.	Field	Size (bytes)	Comment
1	SYNC	2	Sync byte followed by frame type and version number.
2	FRAMESIZE	2	Number of bytes in frame, defined in 6.2.
3	IDCODE	2	PMU/DC ID number, 16-bit integer, defined in 6.2.
4	SOC	4	SOC time stamp, defined in 6.2, for all measurements in frame.
5	FRACSEC	4	Fraction of Second and Time Quality, defined in 6.2, for all measurements in frame.
6	STAT	2	Bitmapped flags.
7	PHASORS	4 × PHNMR or 8 × PHNMR	Phasor estimates as defined in Clause 5. May be single-phase or 3-phase positive, negative, or zero sequence. Values are 4 or 8 bytes each depending on the fixed 16-bit or floating-point format used, as indicated by the configuration frame.
8	FREQ	2 / 4	Frequency (fixed or floating point).
9	DFREQ	2 / 4	Rate of change of frequency (fixed or floating point).
10	ANALOG	2 × ANNMR or 4 × ANNMR	Analog data, 2 or 4 bytes per value depending on fixed- or floating-point format used, as indicated by the configuration frame.
11	DIGITAL	2 × DGNMR	Digital data, usually representing 16 digital status points (channels).
	Repeat 6–11		Fields 6–11 are repeated for as many PMUs as in NUM_PMU field in configuration frame.
12+	CHK	2	CRC-CCITT

The configuration frame is now identified by Bits 4 - 6 of the SYNC word as shown in Table 2. 7. It is also a machine-readable BINARY set that contains information and processing parameters for the PMU and the current real-time data set.

Table 2. 7 Configuration frame organization [15]

No.	Field	Size (bytes)	Short Description
1	SYNC	2	Sync byte followed by frame type and version number
2	FRAMESIZE	2	Number of bytes in frame
3	IDCODE	2	PMU/ DC ID number, 16-bit integer
4	SOC	4	SOC time stamp
5	FRACSEC	4	Fraction of Second and Time Quality
6	TIME_BASE	4	Resolution of fraction-of-second time stamp
7	NUM_PMU	2	The number of PMUs included in the data frame
8	STN	16	Station Name- 16bytes in ASCII format
9	IDCODE	2	PMU ID number as above, identifies source of each data block
10	FORMAT	2	Data format within the data frame
11	PHNMR	2	Number of phasors – 2 bytes integer (0 to 32 767)
12	ANNMR	2	Number of analog values – 2 byte integer
13	DGNMR	2	Number of digital status words – 2 byte integer
14	CHNAM	16 x (PHNMR + ANNMR + 16 x DGNMR)	Phasor and channel names- 16 bytes for each phasor, analog and each digital channel (16 channels in each digital word) in ASCII format in the same order as they are transmitted. For digital channels, the channel name order will be from the least significant to the most significant. (The first name is for Bit 0 of the first 16-bit status word, the second is for Bit 1, etc., up to Bit 15. If there is more than 1 digital status, the next name will apply to Bit 0 of the 2nd word and so on).
15	PHUNIT	4 x PHNMR	Conversion factor for phasor channels
16	ANUNIT	4 x ANNMR	Conversion factor for analog channels
17	DIGUNIT	4 x DGNMR	Mask words for digital status words
18	FNOM	2	Nominal line frequency code and flags
19	CFGNT	2	Configuration change count
	Repeat 8 -19		Fields 8-18, repeated for as many PMUs as in field 7 (NUM_PMU)
20+	DATA_RATE	2	Rate of data transmissions
21+	CHK	2	CRT-CCITT

The header frame simply contains human readable information about the PMU, data sources, scaling, algorithms, filtering, or other related information. This frame is identified by Bits 4 - 6 of the SYNC word as shown in Table 2. 8.

Table 2. 8 Header frame organization [15]

No.	Field	Size	Comment
1	SYNC	2	Sync byte followed by the frame type and version number
2	FRAMESIZE	2	Number of bytes in frame
3	IDCODE	2	PMU/ DC ID number, 16-bit integer
4	SOC	4	SOC time stamp
5	FRACSEC	4	Fraction of Second and Time Quality
6	DATA 1	1	ASCII character, 1st byte
K+6	DATA k	1	ASCII character, Kth byte, K>0 is an integer
K+7	CHK	2	CRC-CCITT check

2.3 The IEEE C37.118-2011 Synchrophasor Standard

This is the latest standard addressing synchrophasor measurements for power systems. It replaces the IEEE Std. C37.118-2005 and this new standard is now split into two standards: IEEE Std. 37.118.1-2011 which covers measurement provisions, and IEEE Std. 37.118.2-2011 which covers data communication [3]. Both parts contain the content found in previous standards with updates and additional provisions.

Additional clarification is provided in IEEE Std. 37.118.1-2011 for phasor and synchronized phasor definitions. The concept of TVE and compliance tests have been retained and expanded. The newly added concepts are: tests over temperature variation and dynamic performance tests. Furthermore, limits and characteristics of frequency measurement and ROCOF measurement have been developed.

The IEEE C37.118-2011 standard was born out of the need to have a better understanding of the conditions and circumstances surrounding power systems. It is known that these systems are stochastic in nature and this means that the frequency is not stable but changes as a result of disturbances making it possible to have off-nominal frequency.

The additional clarification for the synchrophasor definition is shown in equation (2-3)

$$x(t) = X_m \cos(\omega_0 t + \emptyset) = X_m \cos(2\pi f_0 t + \emptyset) \quad (2\text{-}3)$$

Where f_0 represents the nominal angular system frequency (50 Hz or 60 Hz) as shown in equation 2-1. This definition also specified that in general cases where the amplitude is a function of time $X_m(t)$ and the sinusoidal frequency is also a function of time $f(t)$, a function $g = f - f_0$ is defined. In this function, f_0 is the nominal frequency and g represents the difference between the actual and nominal frequencies. Equation 2-3 can be written as:

$$x(t) = X_m(t)\cos(2\pi \int f dt + \emptyset)$$

$$= X_m(t)\cos(2\pi \int (f_0 + g) dt + \emptyset)$$

$$= X_m(t)\cos(2\pi f_0 t + (2\pi \int g dt + \emptyset)) \quad (2\text{-}4)$$

The new synchrophasor representation of this sinusoidal waveform, is shown in Figure (2-5)

$$\boldsymbol{X}(t) = \left(X_m(t)/\sqrt{2}\right) e^{j(2\pi \int g dt + \emptyset)} \quad (2\text{-}5)$$

Finally, for cases where $X_m(t) = X_m$ is constant and $g = \Delta f$ is a constant offset from the nominal frequency, $\int g(t) = \int \Delta f dt = \Delta f t$ so that the new synchrophasor representation becomes:

$$\boldsymbol{X}(t) = (X_m/\sqrt{2}) e^{j(2\pi \Delta f t + \emptyset)} \quad (2\text{-}6)$$

Further clarifications were introduced to frequency and ROCOF estimation. Equation (2-7) shows a sinusoidal signal.

$$x(t) = X_m cos[\Psi(t)] \tag{2-7}$$

Frequency is now defined as shown in equation (2-8)

$$f(t) = \frac{1}{2}\frac{d\Psi(t)}{dt} \tag{2-8}$$

ROCOF is also defined as shown in equation (2-9)

$$ROCOF(t) = \frac{df(t)}{dt} \tag{2-9}$$

The computation of synchrophasors is performed in relation to the system nominal frequency f_0. Representing the cosine argument as $\Psi(t) = \omega_0 t + \varphi(t) = 2\pi[f_0 t + \varphi(t)/2\pi]$, introduces a new frequency formula as shown in equation (2-10)

$$f(t) = f_0 + d[\varphi(t)/2\pi]/dt = f_0 + \Delta f(t) \tag{2-10}$$

Where $\Delta f(t)$ represents the deviation of frequency from the nominal as shown in equation (2-11)

$$ROCOF(t) = d^2[\varphi(t)/2\pi]/dt^2 = d(\Delta f(t))/dt \tag{2-11}$$

TVE under the new standard was also clarified and redefined as "*an expression of the difference between a "perfect" sample of a theoretical synchrophasor and the estimate given by the unit under test at the same instant of time*" [3]. The TVE value is normalized and expressed as per unit of the theoretical phasor. TVE is mathematically defined in equation 2-12:

$$TVE(n) = \sqrt{\frac{(\hat{X}_r(n) - X_r(n))^2 + (\hat{X}_i(n) - X_i(n))^2}{(X_r(n))^2 + (X_i(n))^2}} \tag{2-12}$$

"Where $\hat{X}_r(n)$ and $\hat{X}_i(n)$ represent the estimates given by the unit under test, and $X_r(n)$ and $X_i(n)$ are theoretical values of the input signal at the instants of time (n) which are assigned by the unit to those values" [3].

The error associated with frequency and ROCOF is also a new concept introduced under the new standard. The absolute value of the difference between the theoretical values and the estimated values expressed in Hz and Hz/s is associated with frequency and ROCOF. Where frequency is expressed in Hz and ROCOF in Hz/s. The mathematical representation is shown in equation 2-13 and equation 2-14.

Frequency measurement error: $FE == |f_{true} - f_{measured}| = |\Delta f_{true} - \Delta f_{measured}|$ (2-13)

ROCOF measured error: $RFE == |(df/dt)_{true} - (df/dt)_{measured}|$ (2-14)

"*The measured and the true values are for the same instant of time, which is generally given by the time tag of the estimated values*" [3].

A slight modification was also added to the reporting rate of the PMU for the 50 Hz system. For a 50 Hz system, a 50 frames per second rate was added to the reporting rate when compared to the IEEE Std. C37.118-2005 standard. Table 2. 9 shows this reporting rate.

Table 2. 9 Required PMU reporting rates [3]

System frequency	**50 Hz**			**60 Hz**					
Reporting rates (F_S- frames per second)	10	25	50	10	12	15	20	30	60

Performance class is another concept introduced in IEEE Std. C37.118.1-2011. This concept defines classes of performance: P class and M class. Applications that require fast response and do not need explicit filtering are classified under the P performance class. This performance class is important in protection applications. Hence the letter "P" stands for

protection. Applications that could be severely affected by aliased signals and do not require the fast reporting speed are classified under the M performance class. This performance class is important in analytic measurements that need greater precision. Hence the letter M stands for measurement.

A more detailed steady-state synchrophasor measurement requirements table indicating additional parameters such as temperature and humidity has also been included under the latest standard. Table 2. 10 and Table 2. 11 shows this.

Table 2. 10 Steady-state synchrophasor measurement requirements [3]

Influence quantity	Reference condition	Minimum range of influence quantity over which PMU shall be within given TVE limit			
		P class		M class	
		Range	Max TVE (%)	Range	Max TVE (%)
Signal frequency range—f_{dev} (test applied nominal + deviation: $f_0 \pm f_{dev}$)	$F_{nominal}$ (f_0)	± 2.0 Hz	1	± 2.0 Hz for F_s<10 ± F_s/5 for 10 ≤ F_s < 25 ± 5.0 Hz for F_s ≥25	1
The signal frequency range tests above are to be performed over the given ranges and meet the given requirements at three temperatures: T = nominal (~23 °C), T = 0 °C, and T = 50 °C					
Signal magnitude—Voltage	100% rated	80% to 120% rated	1	10% to 120% rated	1
Signal magnitude—Current	100% rated	10% to 200% rated	1	10% to 200% rated	1
Phase angle with $\lvert f_{in} - f_0 \rvert$ <0.25 Hz (See NOTE 1)	Constant or slowly varying angle	±π radians	1	±π radians	1

Table 2. 11 Steady-state synchrophasor measurement requirements (continued) [3]

Influence quantity	Reference condition	Minimum range of influence quantity over which PMU shall be within given TVE limit			
		P class		M class	
		Range	Max TVE (%)	Range	Max TVE (%)
Harmonic distortion (single harmonic)	<0.2% (THD)	1%, each harmonic up to 50th	1	10%, each harmonic up to 50th	1
Out-of-band interference as described below (See NOTES 2 and 3)	<0.2% of input signal magnitude		None	10% of input signal magnitude for $F_s \geq 10$. No requirement for $F_s < 10$.	1.3
Out-of-band interference testing: The passband at each reporting rate is defined as $\|f - f_0\| < F_s/2$. An interfering signal outside the filter passband is a signal at frequency f where: $\|f - f_0\| \geq F_s/2$ For test the input test signal frequency f_{in} is varied between f_0 and ± (10%) of the Nyquist frequency of the reporting rate. That is: $f_0 - 0.1\ (F_s/2) \leq f_{in} \leq f_0 + 0.1\ (F_s/2)$ where F_s = phasor reporting rate f_0 = nominal system frequency f_{in} = fundamental frequency of the input test signal					
NOTE 1—The phase angle test can be performed with the input frequency f_{in} offset from f_0 where $\|f_{in} - f_0\| < 0.25$ Hz. This provides a slowly varying phase angle that simplifies compliance verification without causing significant other effects. NOTE 2—A signal whose frequency exceeds the Nyquist rate for the reporting rate F_s can alias into the passband. The test signal described for the out-of-band interference test verifies the effectiveness of the PMU anti-alias filtering. The test signal shall include those frequencies outside of the bandwidth specified above that cause the greatest TVE. NOTE 3—Compliance with out-of-band rejection can be confirmed by using a single frequency sinusoid added to the fundamental power signal at the required magnitude level. The signal frequency is varied over a range from below the passband (at least down to 10 Hz) and from above the passband up to the second harmonic ($2 \times f_0$). If the positive sequence measurement is being tested, the interfering signal is a positive sequence.					

Table 2. 12 shows the steady-state frequency and ROCOF measurement requirements. Frequency and ROCOF are required to comply with the measurement limits as presented in Table 2.12

Table 2. 12 Steady-state frequency and ROCOF measurement requirements [3]

Influence quantity	Reference condition	Error requirements for compliance			
		P class		M class	
Signal frequency	Frequency = f_0 ($f_{nominal}$) Phase angle constant	Range: $f_0 \pm 2.0$		Range: $f_0 \pm 2.0$ Hz for $F_s \leq 10$ $\pm F_s/5$ for $10 \leq F_s < 25$ ± 5.0 Hz for $F_s \geq 25$	
		Max FE	Max RFE	Max FE	Max RFE
		0.005 Hz	0.01 Hz/s	0.005 Hz	0.01 Hz/s
Harmonic distortion (same as Table 3) (single harmonic)	<0.2% THD	1% each harmonic up to 50th		10% each harmonic up to 50th	
		Max FE	Max RFE	Max FE	Max RFE
	$F_s > 20$	0.005 Hz	0.01 Hz/s	0.025 Hz	6 Hz/s
	$F_s \leq 20$	0.005 Hz	0.01 Hz/s	0.005 Hz	2 Hz/s
Out-of-band interference (same as Table 3)	<0.2% of input signal magnitude	No requirements		Interfering signal 10% of signal magnitude	
				Max FE	Max RFE
		None	None	0.01 Hz	0.1 Hz/s

Dynamic compliance is also another concept added to the IEEE Std. C37.118.1-2011. This test consist of the linear frequency ramp test, measurement bandwidth test and step response assessment test. To perform the linear frequency ramp test, the linear ramp of the system frequency is applied as balanced three-phase input signals during changes in system frequency. Table 2. 13 shows this performance requirement.

Table 2. 13 Synchrophasor performance requirements under frequency ramp tests [3]

Test signal	Reference condition	Minimum range of influence quantity over which PMU shall be within given TVE limit			
		Ramp rate (R_f) (positive and negative ramp)	Performance class	Ramp range	Max TVE
Linear frequency ramp	100% rated signal magnitude, & $f_{nominal}$ at start or some point during the test	± 1.0 Hz/s	P class	± 2 Hz	1%
			M class	Lesser of ± (F_s /5) or ± 5 Hz [a]	1%

Dynamic compliance performance test is also required during step changes in magnitude and phase. To perform the step response test, balanced three-phase step changes are applied to balanced three-phase input signals. Table 2. 14 and Table 2. 15 shows this concept.

Table 2. 14 Phasor performance requirements for input step change [3]

Step change specification	Reference condition	Maximum response time, delay time, and overshoot					
		P class			M class		
		Response time (s)	|Delay time| (s)	Max overshoot/ undershoot	Response time (s)	|Delay time| (s)	Max Overshoot/ undershoot
Magnitude = ± 10%, $k_x = \pm 0.1$, $k_a = 0$	All test conditions nominal at start or end of step	$1.7/f_0$	$1/(4 \times F_s)$	5% of step magnitude	See Table 11	$1/(4 \times Fs)$	10% of step magnitude
Angle ± 10°, $k_x = 0$, $k_a = \pm \pi/18$	All test conditions nominal at start or end of step	$1.7/f_0$	$1/(4 \times F_s)$	5% of step magnitude	See Table 11	$1/(4 \times Fs)$	10% of step magnitude

Table 2. 15 – Frequency and ROCOF performance requirements for input step change [3]

Signal specification	Reference condition	Maximum response time			
		P class		M class	
		Frequency response time (s)	ROCOF response time (s)	Frequency response time (s)	ROCOF response time (s)
Magnitude test as in Table 9	Same as in Table 9	$3.5/f_0$	$4/f_0$	See Table 11	See Table 11
Phase test as in Table 9	Same as in Table 9	$3.5/f_0$	$4/f_0$	See Table 11	See Table 11

Dynamic compliance performance test is required to test measurement bandwidth of the synchrophasor. To test the measurement bandwidth of the synchrophasor, balanced three phase input signals are modulated with sinusoidal signals which are applied to signal amplitudes and phase angles simultaneously as represented in Table 2-16 and Table 2-17.

Table 2. 16 – Synchrophasor measurement bandwidth using modulated signals [3]

Modulation level	Reference condition	Minimum range of influence quantity over which PMU shall be within given TVE limit			
		P class		M class	
		Range	Max TVE	Range	Max TVE
$k_x = 0.1$, $k_a = 0.1$ radian	100% rated signal magnitude, $f_{nominal}$	Modulation frequency 0.1 to lesser of $F_s/10$ or 2 Hz	3%	Modulation frequency 0.1 to lesser of $F_s/5$ or 5 Hz	3%
$k_x = 0$, $k_a = 0.1$ radian	100% rated signal magnitude, $f_{nominal}$		3%		3%

Table 2. 17 Frequency and ROCOF performance under modulation tests [3]

Modulation level, reference condition, range (use the same modulation levels and ranges under the reference conditions specified in Table 5)	Error requirements for compliance			
	P class		M class	
	Max FE	Max RFE[a]	Max FE	Max RFE[a]
$F_s > 20$	0.06 Hz	3 Hz/s	0.3 Hz	30 Hz/s
$F_s \leq 20$	0.01 Hz	0.2 Hz/s	0.06 Hz	2 Hz/s

The messaging format discussed under IEEE Std. C37.118.1-2005 is virtually the same as the one in IEEE Std. C37.118.2-2011 [3]. The only difference in the messaging format and data transfer is that a new configurations frame has been added.

2.4 GridTRAK PMU

The GridTrak PMU is an open source PMU developed at Baltimore University [16]. The GridTrak PMU is a PMU designed to digitally measure and transmit AC synchrophasor frequency, phase angle, and magnitude. Using an operational amplifier and a precision voltage reference, AC signal is converted to complimentary square waves. This design uses a precision timer to measure square wave cycle (frequency) and offset from PPS time reference (phase angle). In addition, it calculates the magnitude for the ideal sine wave of the signal. The design has the option to use GPS for precision PPS triggering and synchrophasor measurement values. Data is also transmitted based on the IEEE Std. C37.118-2005 specifications. The aim of the GridTrak device is to produce a PMU that is not costly and one that can be widely distributed among researches and amateur enthusiast. It is believed that this approach will allow widespread monitoring of the distribution network [17]. The design actually works using the zero crossings technique, making the unit simple and robust. One setback of the design is the loss of point-on-wave information which reduces GridTrak's applications [17].

2.5 DTU-PMU

The DTU-PMU was developed by the Centre of Electric Technology (CET), from the Technical University of Denmark (DTU) [12]. The DTU-PMU is made up of two PC units that work together to provide PMU function. One of the PC only runs on a disk operating system (DOS) and it is responsible for handling holds from administrative peripherals. Examples of holds include: timer, keyboard, USARTS (Universal Synchronous/ Asynchronous Receiver/ Transmitter), direct memory access (DMA), etc. Measurements are packeted and exported to this PC at intervals of 20ms [5].

The second PC runs on a windows 2000 operating system and it is used for performing tasks, such as data I/O, file creation and storage, etc. Figure 2-8 shows this illustration.

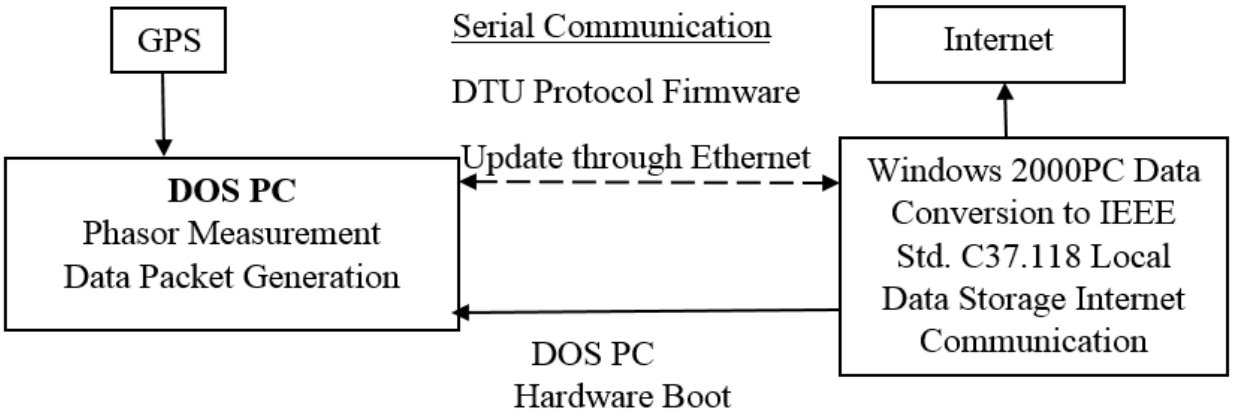

Figure 2-8 The DTU PC-based PMU [12]

This PMU is able to estimate the frequency of the AC power input signal and synchronize sampling with it. This is done to ensure that accurate phasors are obtained. Problems in phasor estimation are avoided by ensuring that sampling is synchronized to the actual power system signal. A 16-bit A/D (Analog to Digital) converter is used to take in 64 or 128 samples over the fundamental frequency period. Goertzel algorithm which is simply a FFT analysis that extracts only the fundamental frequency is used to estimate phasor. The phasor measurements are referenced to UTC. This PMU ensures that an internal clock is synchronized with the external UTC time derived from the GPS clock that is synchronized to the GPS receiver. The signal from the PMU has a time stamp latched to it from the GPS. This time stamping will ensure that the PC's internal time clock is synchronized within 1μs of the UTC time, which is based on the GPS accuracy of $\pm 100ns$. After the computation of each phasor, the PMU compares the phasor estimate time with the UTC time. This PMU is able to report a synchrophasor, by estimating the UTC referenced phase angle and magnitude of the phasors that equivalently covers the interval. Data is stored locally.

The second PC actually runs in the LabVIEW environment where estimation of waveform parameters can be performed with data archived locally and exported to another location.

2.6 The openPDC

The open source phasor data concentrator (openPDC) is a system equipped with the functionality to manage, process and respond to dynamic changes in fast moving streaming phasor data [18]. The openPDC was introduced on January 28, 2010 as the openPDC Management System. The basic components that make up the openPDC system have been in the development process by the Tennessee Valley Authority (TVA) after it released its source code for its data concentration software known as the Super Phasor Data Concentrator (SPDC) on October 7, 2009. Any data that can be described as "time-stamped measured values" can be processed by the openPDC. Measured values refers to numeric quantities that have been acquired at a source device and are typically called point, signals, events, time-series values. The measurement of a value, triggers a timestamp to be taken, using a GPS clock. The GPS clock is needed for accuracy and the value together with the timestamp, is streamed to the openPDC where it can be "time-aligned" with other incoming measurements so that an action can be taken on all data measured at the exact same time. Figure 2.9 shows the technical diagram which describes the adapter relationship and data flows in the openPDC. User defined input adapters are used to collect streaming data and incoming measurements are assigned an ID in this diagram.

Measurements are basically sorted with respect to time and distributed to customized adapters that can process the data. All measurements are finally distributed to output adapters that are used to queue up data for archival purposes.

Data flow in Figure 2-9 is split into: map, sort and queue. The *map* block refers to the stage for assigning an ID to a measurement, *sort* on the other hand is the stage for sorting the measurements by time so that appropriate action can be taken, finally the stage where measurements are queued so that they can be distributed to different outputs is called *queue*. The openPDC system allows users to load their own "assemblies", to provide better streaming of measured data.

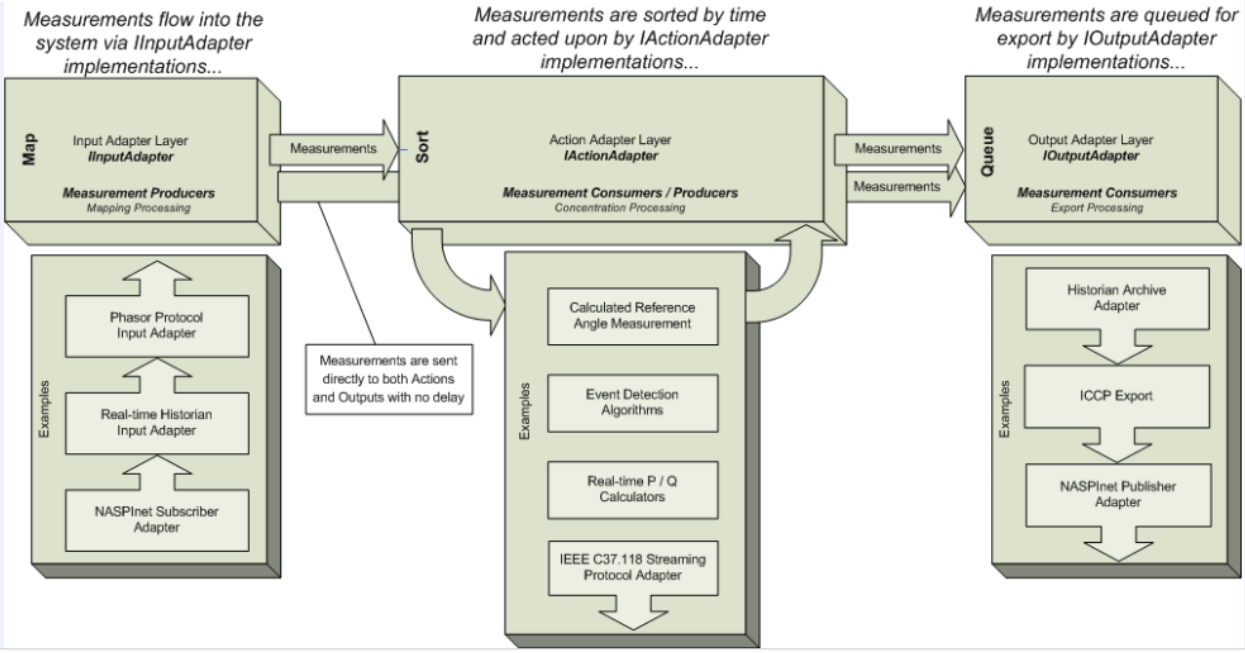

Figure 2-9 Technical diagram of openPDC [18]

2.7 The openPMU

The openPMU is a PMU device designed and developed at Queen's University Belfast (QUB), United Kingdom [5]. This design was implemented to meet the needs of targeted projects which revolved around investigating anti-islanding detection and phase control of islanded generators. The motivation behind this design was geared towards implementing an inexpensive PMU for real-time applications.

The openPMU design consist of hardware and software which have all been arranged to create the openPMU project. Figure 2.10 shows a schematic diagram for the OpenPMU device.

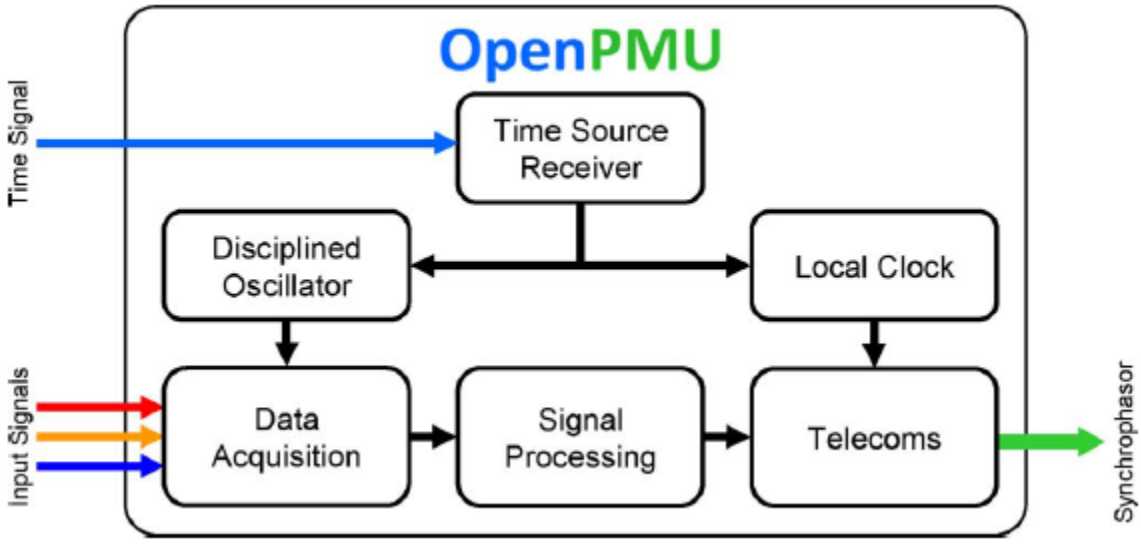

Figure 2-10 Schematic diagram of the OpenPMU [5]

The OpenPMU system is divided into two parts, the measurement system and the analysis system [19]. The measurement system is made up of analog data acquisition and time synchronization while the analysis comprises of an embedded PC and a communication structure.

The measurement system utilizes a data acquisition device (DAQ) from National Instruments (NI) and a GPS time source receiver from Garmin. The DAQ used in this design is the NI USB-6009-OEM device. The analog-to-digital converter (ADC) of this DAQ has a resolution of 14 bits and a sampling rate of 48 kHz. This ADC is capable of sampling eight channels through a multiplexer. The ADC was configured to sample 6 channels (three voltage and three current signals). For a nominal frequency of 50 Hz, the sampling rate would be 6.4 kHz for 128 samples per cycle while for a nominal frequency of 60 Hz, the sampling would be 7.68 kHz for 128 samples per cycle. The schematic of the measurement system is shown in Figure 2- 11. From Figure 2- 11, it can be seen that the GPS time receiver is directly connected to the DAQ through a PIC microcontroller. The GPS receiver is responsible for providing the time synchronization required for synchrophasor estimation. The GPS receiver has two outputs: a TTL level 1PPS signal and RS232 level NMEA sentences containing the UTC date and time.

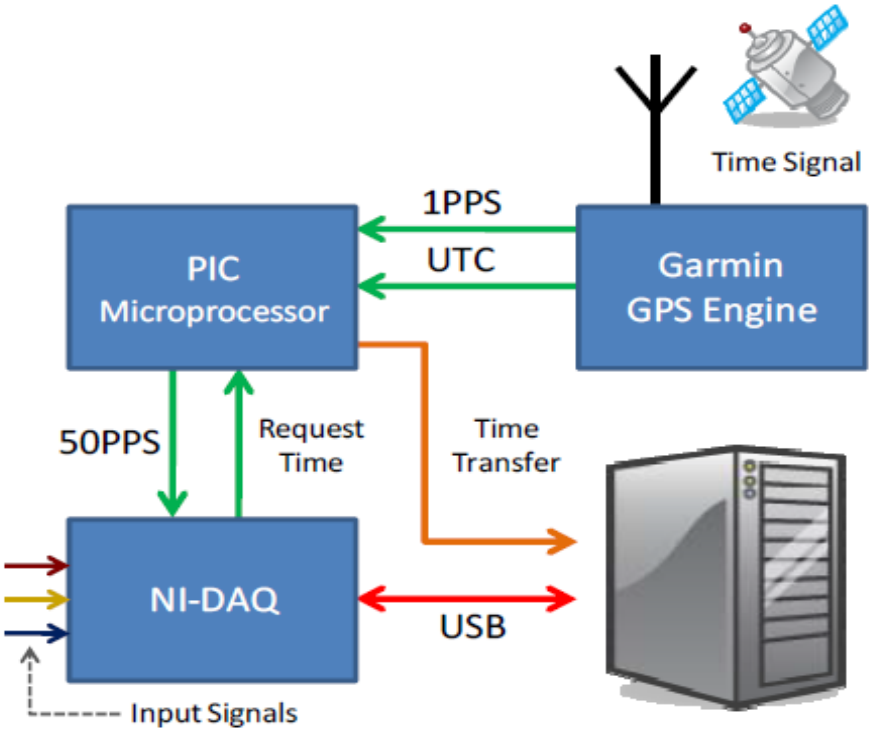

Figure 2- 11 Schematic of measurement system [19]

The 1PPS signal is a 1Hz square wave signal which is in phase with the UTC second transition, is directly transferred to a PIC microcontroller which runs a C program, functioning as phasor-lock-loop (PLL) with a 50 times multiplier which generates a 50Hz square wave (or 60 times multiplier which generates a 60Hz square wave).

The sample trigger of the DAQ is the 60 Hz signal which is used to kick start the acquisition process. Figure 2.11 shows that the input to the DAQ are three phase voltages and currents signals which are the signals under analysis and the sampling window trigger. Figure 2-12 shows a capture window in the LabVIEW environment which represents the type of data captured by the DAQ device. The (green) square wave signal represents the output of the GPS disciplined PLL, which is also the windowing function trigger used by the phasor estimation algorithm as a reference signal.

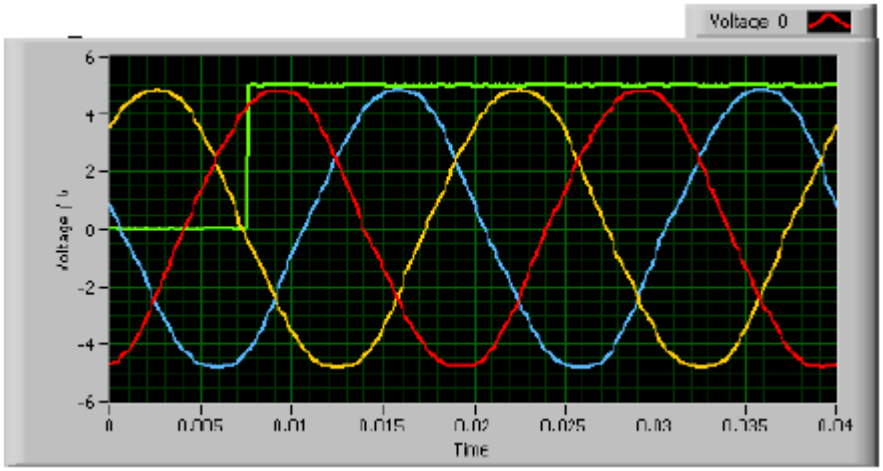

Figure 2-12 Waveform captured by NI-DAQ [19]

The OpenPMU phasor estimation algorithm runs on a standard x86/ x64 personal computer [19]. The PIC microcontroller in Figure 2-11 also provides a mechanism for time transfer from the GPS receiver to the PC that performs the analysis. The PC has the ability to actuate a TTL trigger called "Request Time" through the DAQ card. The PC is responsible for also recording the value of its internal clock at the same time that the TTL trigger signal is being actuated. The PIC communicates the UTC time to the PC and the PC recognizes this time transfer request. With this done, the PC corrects the time indicated by its internal clock to the UTC time and then the UTC time is extrapolated from the internal clock until the next time transfer event comes into play.

The data from the measurement device is represented with the extended markup language (XML) format before being converted from binary and coded in Base 64 representation before finally being pushed to the phasor estimation stage using the UDP/ IP as a protocol and standard Ethernet as physical media. The data payload is represented in XML format because it is human readable. Since XML is inefficient in transferring data due to too many individual tags, the data payload is converted to Base64 representation [20].

The analysis system of the OpenPMU design as mentioned earlier is the National Instruments LabVIEW software. Phasor estimation is performed using the NI LabVIEW software. The NI signal analysis libraries makes it possible to perform signal processing. Phasor estimation is performed in LabVIEW using the FFT/ spectral Leakage type algorithm which acts upon 40ms worth of samples windowed by a "Blackman-Harris" function [20]. The incoming signal from DAQ is first split into two 60Hz cycles (40ms) segments, and the "Blackman-Harris" windowing function is applied before processing is done by FFT. A spectral leakage function simply determines the nominal frequency, which is used to generate a reference from which the phase of the measured signal can be estimated [21]. The outputs of the phase estimation stage are pushed to the telecommunication stage using the UDP/ IP transport mechanism which carries these outputs as XML payloads. This payload holds the amplitude, frequency and phase angle for each waveform that is estimated, and this also includes the label which identifies the source of the data through the measurement system.

This payload is time coded with regards to the data from the measurement system and the data supplied to the communication stage must be sufficient so as to fulfill the IEEE C37.118 synchrophasor frame.

The communication stage is basically a module designed to be compliant with the IEEE C37.118.2 standard to transfer data to a data requester (PDC). It takes into consideration a set of critical parameters such as computation delay, functional checks on data, reception and transmission speeds etc. The communication module is shown in Figure 2-13. Figure 2-13 shows the flow of data from the input of this module to the output. The input block receives data in CSV (comma or character-separated values) format from the LabVIEW module, and

then the communication engine decides which data frame to send based on the request it receives from the data requester.

The communication engine also checks to see if the input module is receiving data from LabVIEW in the proper format, and if not it stops sending data until the stream to the input module is fixed. Finally the output module sends data and commands back and forth between communication engine and data requester. The entire communication module is programmed in Visual C++.

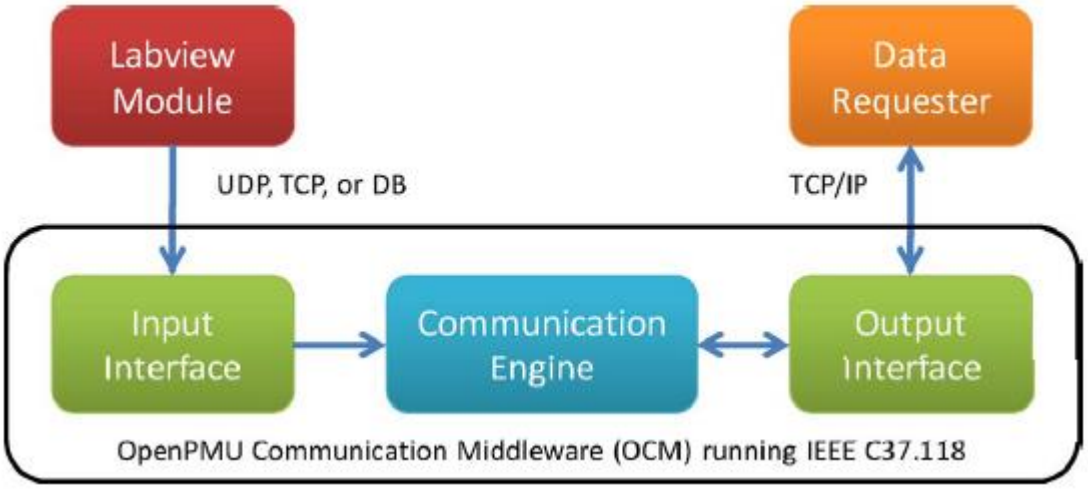

Figure 2-13 Schematic for communication module of OpenPMU [5]

Chapter 3: Design and Implementation of PMU

The design and implementation of the PMU for this thesis is basically broken down into hardware and software domain. This Chapter will start by introducing the platform used for designing the PMU with the block diagram of the PMU design presented. The design specification of the PMU which explains the hardware measurement architecture, communication architecture and time synchronization details is explained. The circuit schematic of the PMU will be introduced after which this schematic will be escalated to the PCB (printed circuit board) design phase where the different PCB foot prints are obtained for all the schematic components. With the PCB design done, the design is printed or etched on the circuit board where circuit components will be populated on the board by soldering. The next phase is to implement the phase estimation or software domain where data processing and analysis has been performed. This domain is implemented using the NI LabVIEW software. The challenge(s) encountered during design of PMU is elaborated as well.

3.1 PMU Design Philosophy

The PMU device in this thesis has been designed using key information extracted from the OpenPMU group. The OpenPMU group is an open source or platform which includes a PMU device developed to meet different needs at the University. It has design specifications and the PMU in thesis has been designed using some of these specifications. The specifications include PCB design, source code etc. The OpenPMU design has a PCB design which was studied and used in developing the schematic for the PMU design presented in this thesis. Similarly the source codes/ algorithms in OpenPMU design have been edited to meet the PMU design presented in this thesis. Figure 3-1 shows the block diagram of the PMU design for this thesis. Section 2.7 contains additional information on the OpenPMU design.

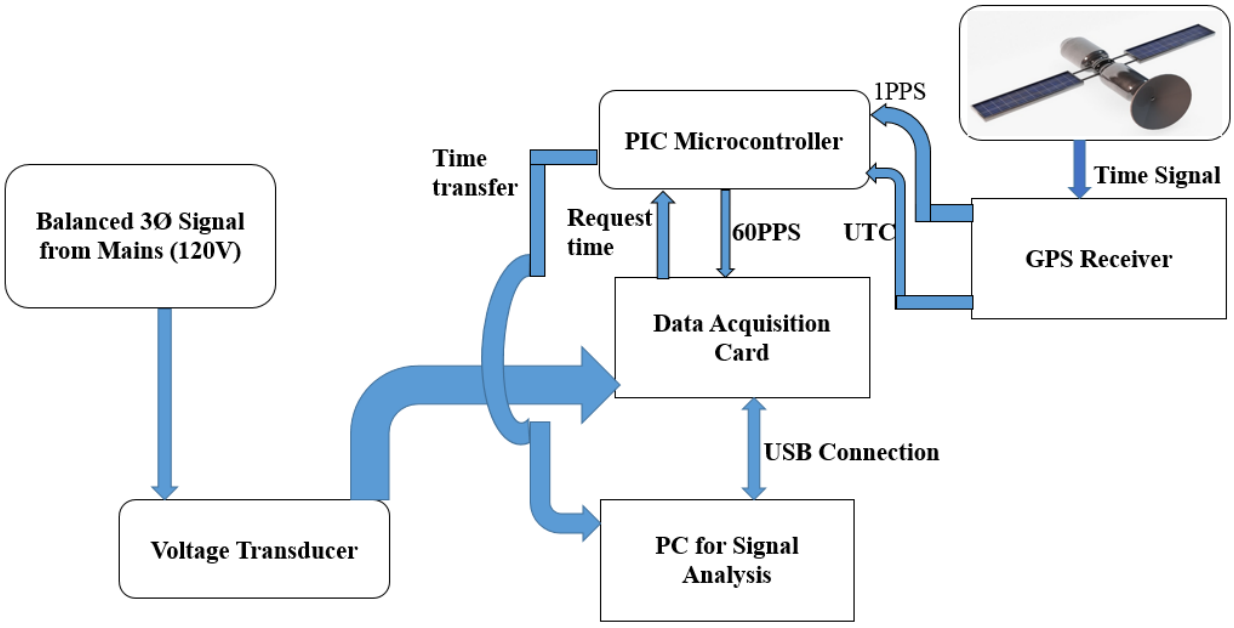

Figure 3-1 Block Diagram of PMU

All the blocks that make up the block diagram in Figure 3-1 have been arranged meticulously to produce the PMU design in thesis. It can be seen that balanced three-phase input signals from mains is sent to the voltage transducer.

The main function of the voltage transducer is to convert the high voltage balanced three-phase signals to a level that the data acquisition card will utilize for sampling. This is usually 5 Volts. The GPS receiver block generates two signals. One is a 1PPS signal and the other is a UTC signal. Both signals are important to the PMU design, because the 1PPS signal is required by the PIC to perform PLL multiplier function to generate the 60PPS signal which is the sampling trigger of the data acquisition card. The PIC in this design has been programmed in C language to perform the PLL task and generate time transfer needed by the PC. The PC is able to actuate a signal called "request time" through the DAQ to the PIC. The PC records the time of its internal clock the moment this signal is actuated. In the same vein, the moment the PIC receives the "request time" signal from the PC, it communicates a signal called "time transfer" to the PC. The request time is needed by the PC to correct its internal clock to the UTC time. The signals under analysis from the DAQ to the PC need to be time stamped for synchrophasor estimation. This is why the PC's internal clock needs to be accurate. The PC block contains the phasor estimation algorithm for estimating signal quantities like frequency, phase angle and voltage magnitude. This design only considers voltage signal and not current signal.

3.2 Design Challenge

One of the challenges encountered in the design of the PMU for this thesis was selecting an appropriate software that will be capable of handling schematic design and PCB design. The schematic design for the PMU in this thesis was firstly designed using the CadSoft Eagle PCB software. After implementing the schematic design and obtaining the PCB design from the schematic design, it became clear that a PCB design will be impossible to be printed on a circuit

board because of some restrictions tied to the use of the free version of the CadSoft Eagle PCB software. After realizing this, the entire design was abandoned and another software without PCB implementation restrictions was adopted. DesignSpark PCB software was eventually used to design the schematic from scratch and then the PCB design. Section 3.3 covers design specification for the designed PMU.

3.3 Design Specification

The design specification of this project has been broken down into a number of headings which are: (1) PMU (Hardware) Architecture (2) Data Acquisition System (3) Time Synchronization.

3.3.1 PMU (Hardware) Architecture

The PMU hardware architecture is simply the heart of the PMU design. It is simply the motherboard to which other devices connect to, to allow for communication between the device and the motherboard. The chief devices that make up the PMU hardware architecture are:

(i) Voltage Transducer

The voltage transducer in this design is needed to provide measurement of AC voltage level and conversion of high balanced three phase voltage signals to a lower level compatible for DAQ usage. The rating of this transducer is given thus:

(a) Primary current rating …….. starting at 10mA

(b) Secondary current rating …….. 25mA

(c) Nominal voltage measurement ……. 10 – 250VAC

(ii) DC Voltage Converter/ Power Supply

This is needed to power up the voltage transducer. Voltage transducers work mainly in conjunction with DC power sources.

Output Voltage Rating …… $\pm$9 to $\pm$15V

(iii) Microcontroller

A microcontroller that can easily implement phase lock loop (PLL) function acting as a frequency multiplier is needed for this design. Microcontroller must allow for serial communication.

(iv) Connectors and Terminal Blocks

(v) Voltage Regulator

This device is primarily needed for supplying specific DC voltage to specific devices such as LED, microcontroller. This is a 5V DC voltage regulator.

Input Voltage …….. 9 - 12V

Output Voltage …….. 5V

(vi) Passive Components

Resistors of different rating are needed throughout the circuit. Polarized and non-polarized capacitors are needed. These passive components are required as specified in datasheets of other components on the motherboard.

(vii) Miscellaneous

Crystal Oscillator …… 4MHz

(viii) Printed Circuit Board

Any simple double sided PCB with dimensions of 6” by 9” is perfect for design.

(ix) Line Driver and Receiver

The line driver and receiver is responsible for satisfying standard interface between the data terminal equipment (DTE) and data communication equipment (DCE). Here the DTE would be the PC and the DCE would be the GPS engine. Line driver and receiver must be TTL compatible.

3.3.1.1 Circuit Design/ Software Selection

Based on the design specification of the PMU, the various components that match the design specification have been selected and this has been used to make the circuit schematic as shown in Figure 3-1. These components are shown in Table 3.1.

The main circuit of the PMU device has been implemented using the DesignSpark PCB 7.0 software. The basic circuit schematic of the measurement system is shown in Figure 3-1.

DesignSpark PCB software was selected for the schematic design as well as for the PCB design not because it was better than other circuit schematic/ PCB software, but due to the following reasons: (1) It has the ability to convert schematic directly to PCB layout with ease (2) It has the ability to easily design foot prints for any component not in its library (3) It is user friendly and it is available free online without board size limitation as seen in other software.

PCBs are the far most common method of assembling modern electronic circuits [22]. PCBs comprise of a sandwich of one or more insulating layers and one or more copper layers which will normally bear the signal traces and the powers and grounds. The PCB designed for this PMU project is actually a two layer board.

Table 3.1 Components that make PMU

The Components:	Quantity
1. Traco Power Unit (THN 15 – 2423WI)	1
2. LEM LV25-P Voltage Transducer	1
3. 5V Voltage Regulator	1
4. 5V LED (Red)	1
5. PIC 18F252	1
6. Line Driver and Receiver (SN75155)	1
7. 100pF Capacitor	1
8. 1000pF 50V Electrolytic Capacitor	3
9. 100k Ohm Resistor	1
10. 240k Ohm Resistor	3
11. 47k Ohm 7W Resistor	3
12. 4MHz Crystal	1
13. 9 Pin D-Type Socket	1
14. 5-way screw terminal	1
15. 7-way screw terminal	1
16. 2-way screw terminal	1
17. 6-way screw terminal	1
18. USB-6009 IDC socket (2x17)	1
19. IDC socket (2x5)	1
20. IDC socket (2x7)	1
21. 5 Pin PCB Header	1

With the schematic designed in Figure 3-2, the next stage is the conversion of the schematic into its PCB equivalent. After conversion, the components are manually arranged and the circuit routed to complete the conversion process. Figure 3-3 shows the finally designed PCB layout of the PMU device.

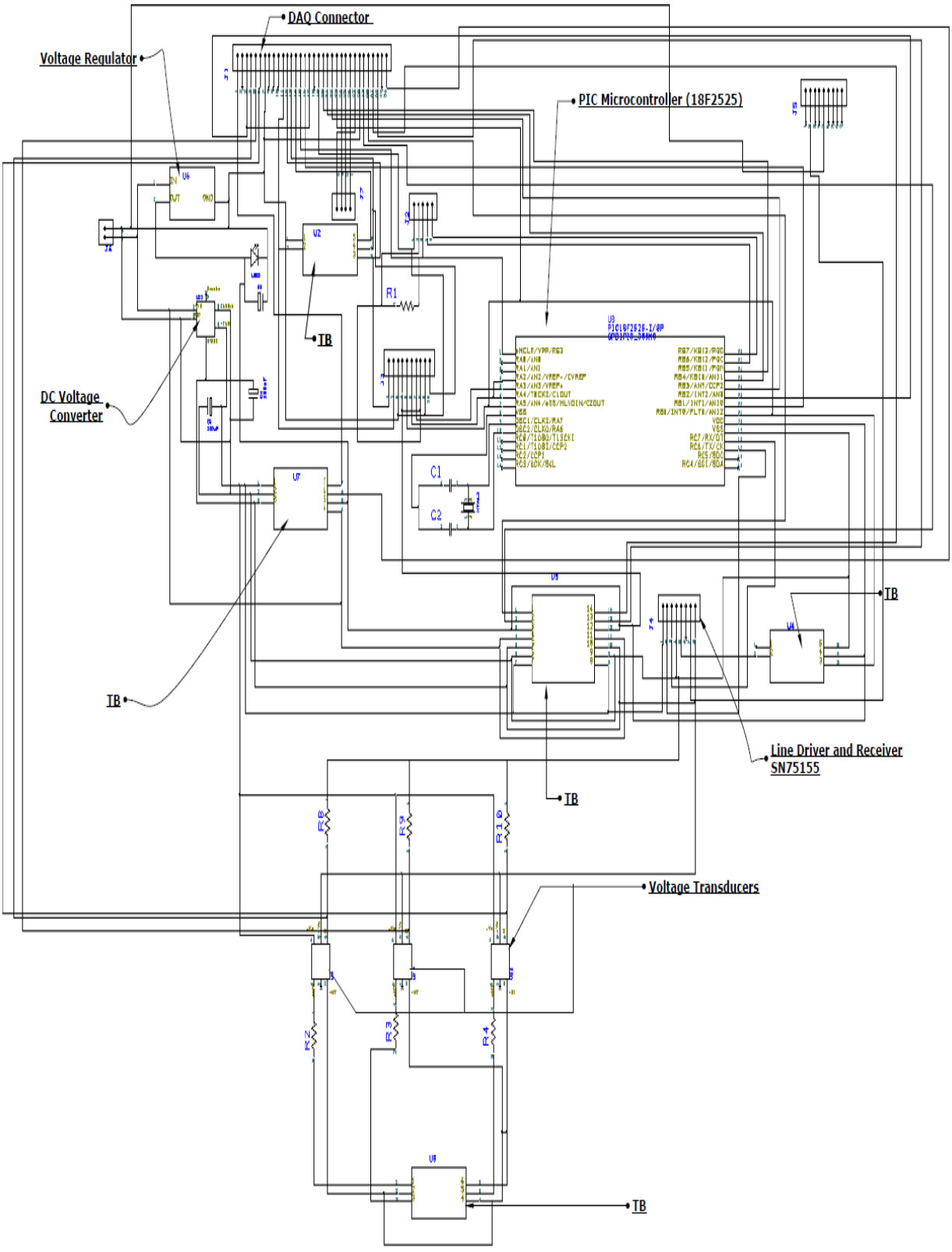

Figure 3-2 Circuit schematic of measurement system

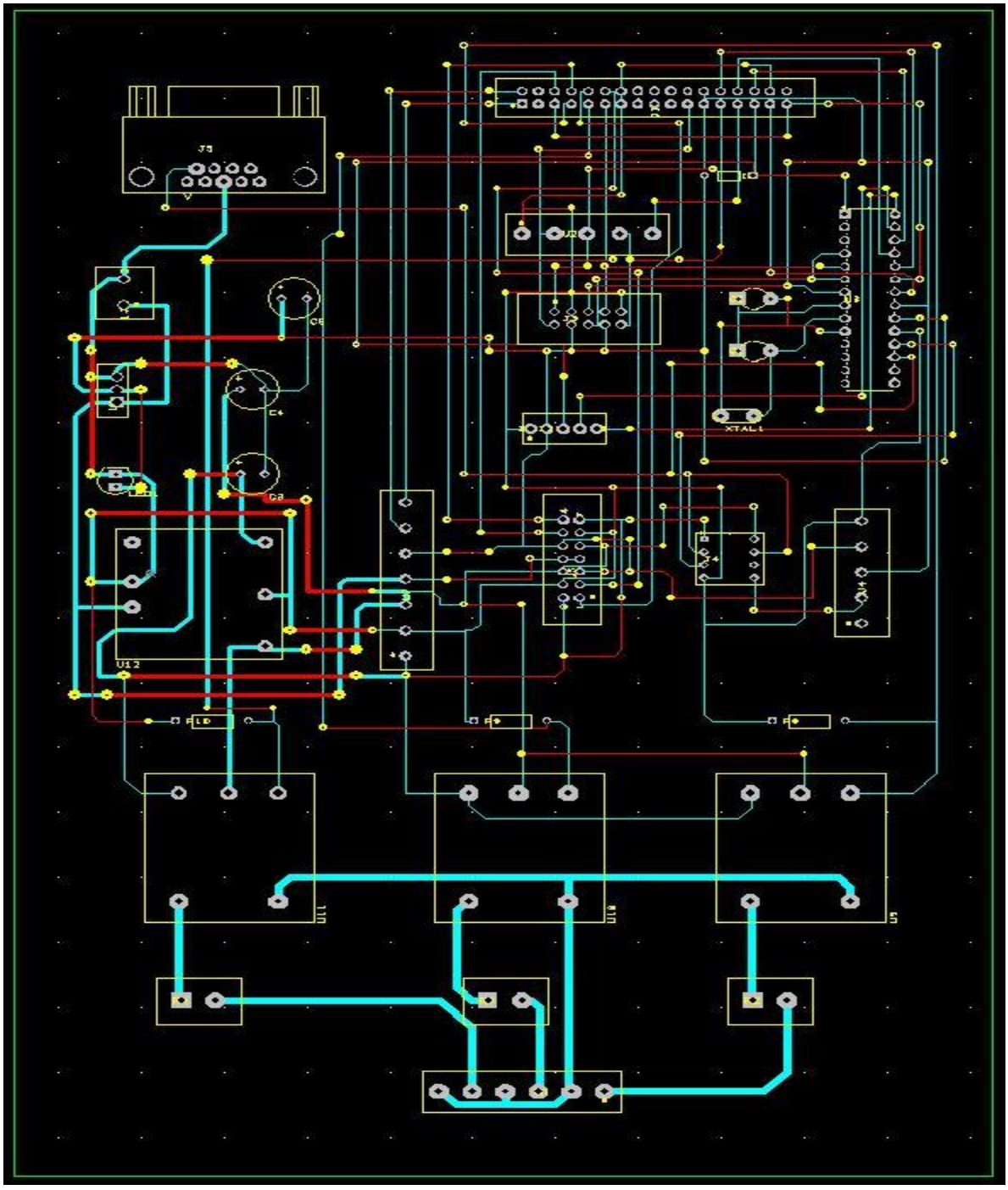

Figure 3-3 PCB layout of measurement system

The PCB design in Figure 3-3 is a double sided PCB, where the green color lines or traces represent the bottom layer and the red trace represents the top layer. After the circuit

schematic has undergone the routing process and converted to the PCB design as shown in Figure 3-3, it is checked for errors. After this check is done, and all errors corrected, the PCB files (Gerber files) were obtained and sent for the manufacturing process at the manufacturing laboratory, University of Manitoba. The Gerber file is the file standard format used by virtually all PCB industry software to describe the information contained in the PCB design. Such information include drill holes, copper layers, legend etc.

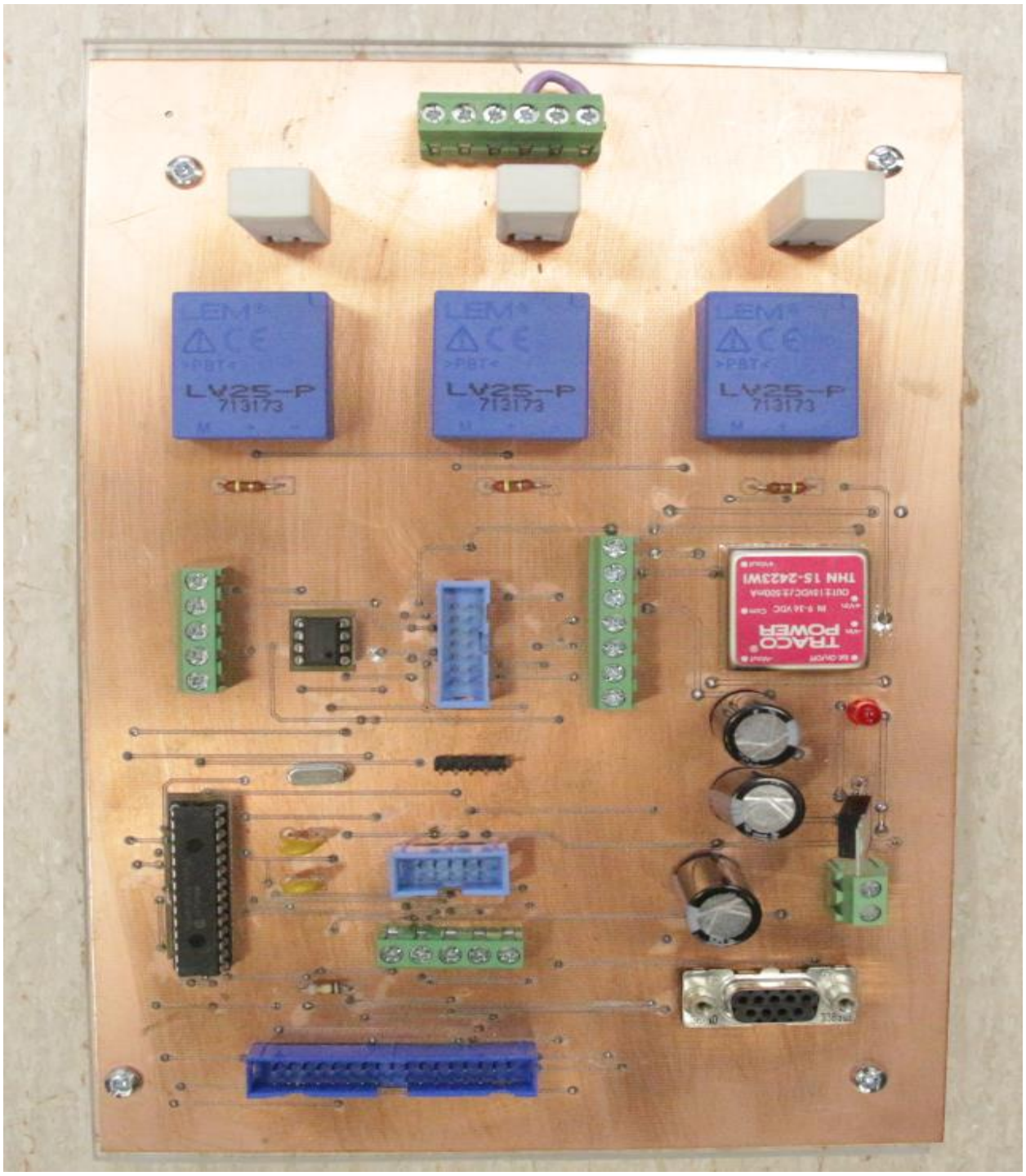

Figure 3-4 Top view of implemented measurement system

Figure 3-4 shows the implemented main circuit board of the PMU design. This capture does not show the NI data acquisition system (DAQ) and the GPS receiver. The DAQ comes as an independent device to be plugged directly to the bottom header of the PMU device as shown

in Figure 3-4. Similarly the GPS is an independent device to be attached to one of the input headers on the main circuit board.

3.3.1.2 Data Acquisition System

The DAQ selected for the PMU design is the National Instruments (NI) DAQ. The reason the NI DAQ was selected was because a lot of research work has been done on PMU using the NI software. Therefore standing on the research work of groups like the OpenPMU, it became necessary to use a DAQ by NI since the analysis algorithm has already been coded using NI LabVIEW. The PMU design will sample signals at 128 samples per cycle. Therefore, considering a 60 Hz system, this will yield a sampling rate of 7.68 kHz. The sampling resolution for PMU design is typically 16 bits or less. Three analog input channels are needed to send in three phase signal for phasor estimation. Therefore the NI DAQ that will be used for this PMU design has to be selected to match up with these requirements. The NI USB 6009-DAQ was selected for this design task. The ADC of this DAQ has a sampling rate of 48 kHz, a sampling resolution of 14 bits and 8 analog input channels. Figure 3-5 shows the NI USB 6009-DAQ.

Figure 3-5 NI USB 6009 DAQ

3.3.1.3 Time Synchronization

The PMU design requires a GPS receiver to provide time synchronization required for synchrophasor estimation. The specification of the required GPS receiver which is typical for most GPS is the ability to output two signal types. One of the signal is a 1PPS which is a TTL level signal and the other is RS232 level NMEA sentences containing the UTC data and time. The Garmin GPS engine has been selected for this task because of its extensive use in PMU research. In addition, it has been selected based on the fact that it is capable of outputting the 1PPS signal and the RS232 level signal. The specific type of Garmin receiver selected was the Garmin 18x LVC which comes with 5 meters of wire extension to allow the receiver to be placed at a distance far away from the PMU device as needed for proper GPS reception. Figure 3-6 shows a snapshot of the Garmin GPS receiver.

Figure 3- 6 Garmin GPS receiver

3.4 Analysis system

The analysis system consists of the NI LabVIEW environment of the PMU design. The LabVIEW environment as shown in Figure 3-7 is the environment that holds the phasor estimation algorithm for the PMU design. What is shown in Figure 3-7 is the front view of the LabVIEW platform which displays the voltage waveform, frequency waveform, phasor waveform and other details.

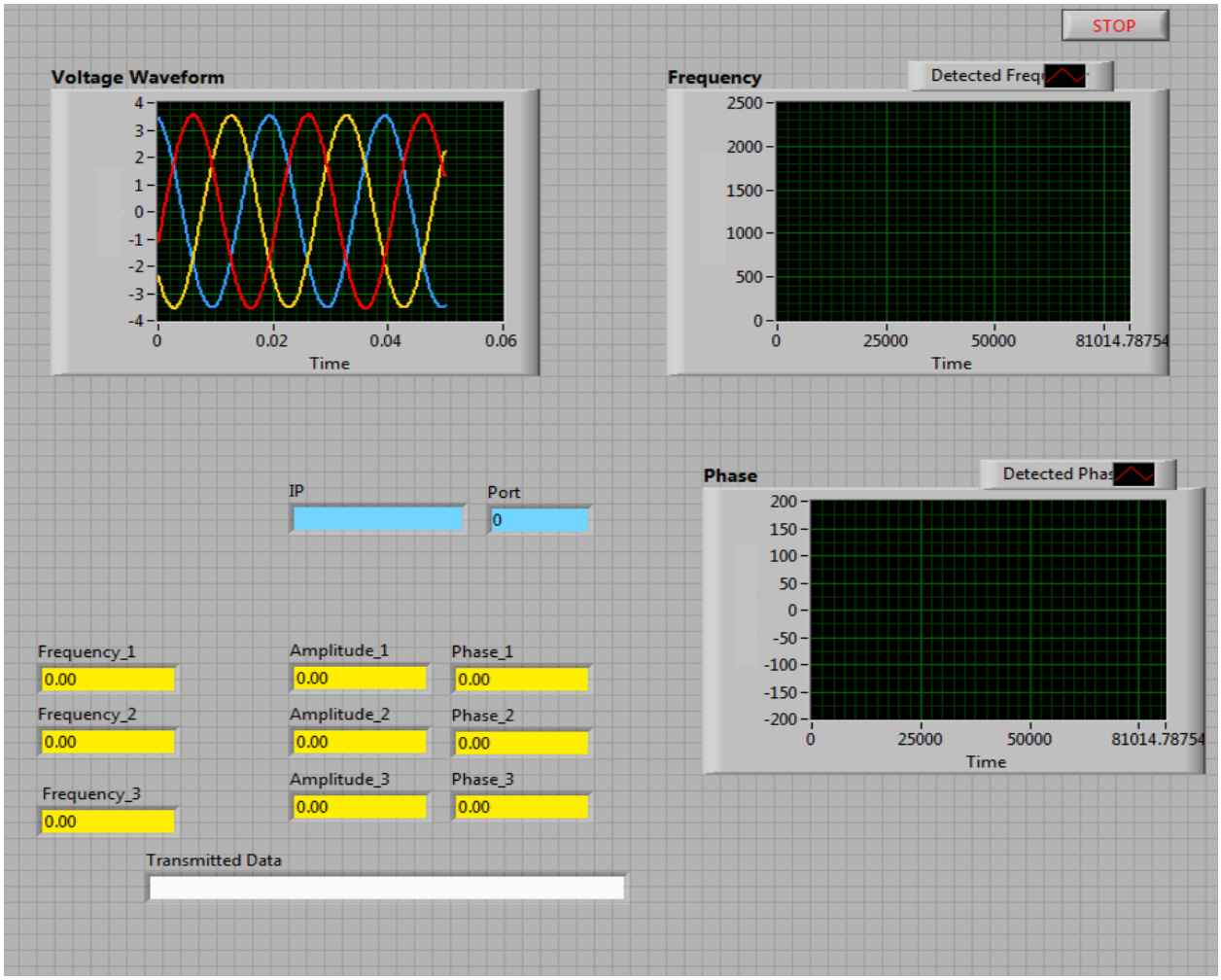

Figure 3-7 NI LabVIEW analysis

As discussed earlier on, the algorithm used in implementing phasor estimation remains the simple FFT/ Spectral Leakage type algorithm which simply acts upon 40ms worth of samples windowed by a “Blackman-Harris” function.

The LabVIEW software is mostly concerned with the configuration of the data acquisition card and accurately time coding the incoming waveform sample data. The incoming data is buffered in a queue and phase estimation performed [5]. The algorithm in the LabVIEW environment runs a regular but standard X64 personal computer with Windows being the operating system.

Chapter 4: Hardware Testing and Analysis of Results

Chapter 3 covered basically the design as well as the implementation of the PMU device with explanation of the software used in performing the phasor estimation. With the PMU device implemented and the algorithm setup in LabVIEW, the next stage was testing the PMU device which involved evaluating the performance of the PMU through some experiments as well as obtaining results and drawing conclusions based on the results. The Challenge(s) experienced during testing is elaborated first.

4.1 Test Challenges

Unavailability of important libraries in LabVIEW

The phasor estimation algorithm used in the PMU design of this thesis presented difficulties in terms of getting it to run successfully without errors. It took a month to finally debug the algorithm needed for phasor estimation. This issue stemmed from the absence of some libraries needed in the LabVIEW software to effectively run the algorithm without errors. Resolving this issue finally involved making important changes to the algorithm from OpenPMU and then

installing appropriate libraries to the LabVIEW software. On a similar development, there was difficulty getting proper GPS signal in the first laboratory where the experiment was setup. The inability for the GPS to receive satellite signal prevented the running of the algorithm because time synchronization is needed for phasor estimation. The entire experiment was eventually relocated to another laboratory to allow for effective GPS communication with satellite.

Play back device

The absence of a real-time play back device with precise GPS synchronization needed to communicate test signals to the PMU prevented the performance of the TVE test for both steady state and dynamic conditions required for compliance to the PMU standard.

4.2 Experiment 1: Accuracy of Voltage Monitoring

One of the many applications of PMU is to monitor the electric network to ensure that electrical quantities are within statutory limits. The designed PMU in this thesis was tested to see if it could measure or estimate the voltage phasor of a particular power system device which can be considered as a small station. The first experimental setup is shown in Figure 4-1. The Lab-Volt 8010-20 system is the system that the PMU device is interested in monitoring. This system is an experimental platform available at the University of Manitoba Power Laboratory. It is a rapid prototyping platform that permits the construction of a miniature power system. Balanced three phase voltage signal from this system is measured by the PMU for monitoring purposes. The PMU sends all measurements to the PC for phasor estimation. The inputs to the data acquisition system in the PMU device comes from the signal under analysis which is the balanced three phase voltage signal supplied by the Lab-Volt 8010-20 system.

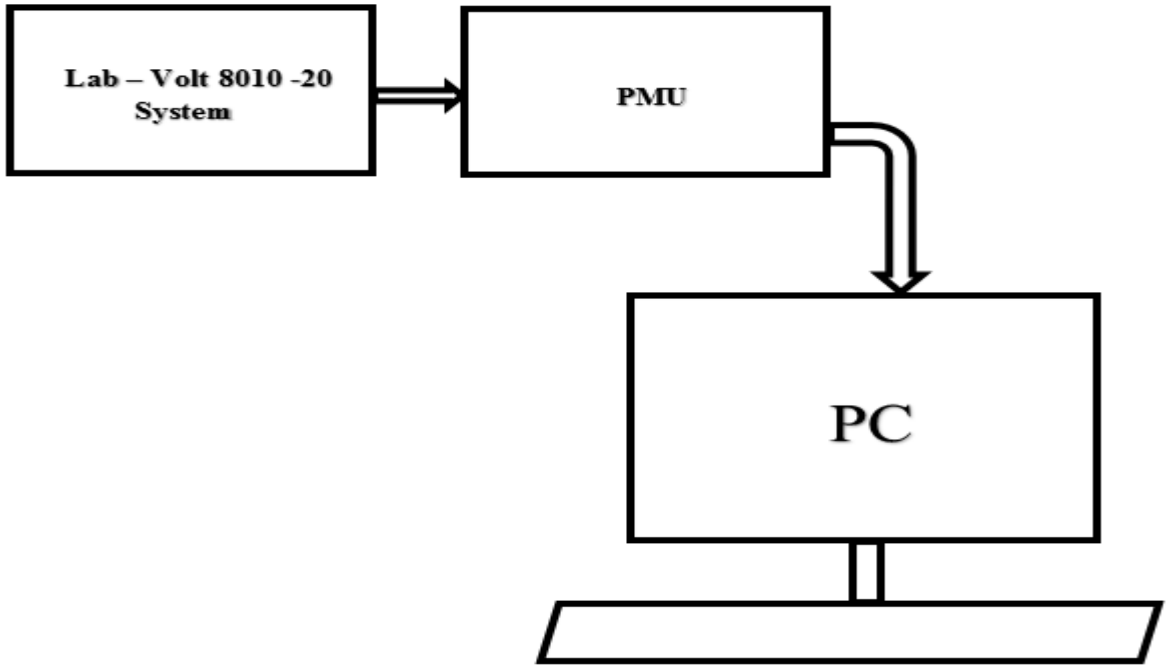

Figure 4-1 PMU device diagram setup

The Lab-Volt system is supplying a balanced three phase 120 Vrms voltage signal to the three voltage transducers as shown in Figure 4-3. Figure 4-2 shows the entire system set-up for experiment 1. The 12V DC voltage that is needed to power up the DC components that make up the PMU device comes from a different power supply unit as shown in Figure 4-2.

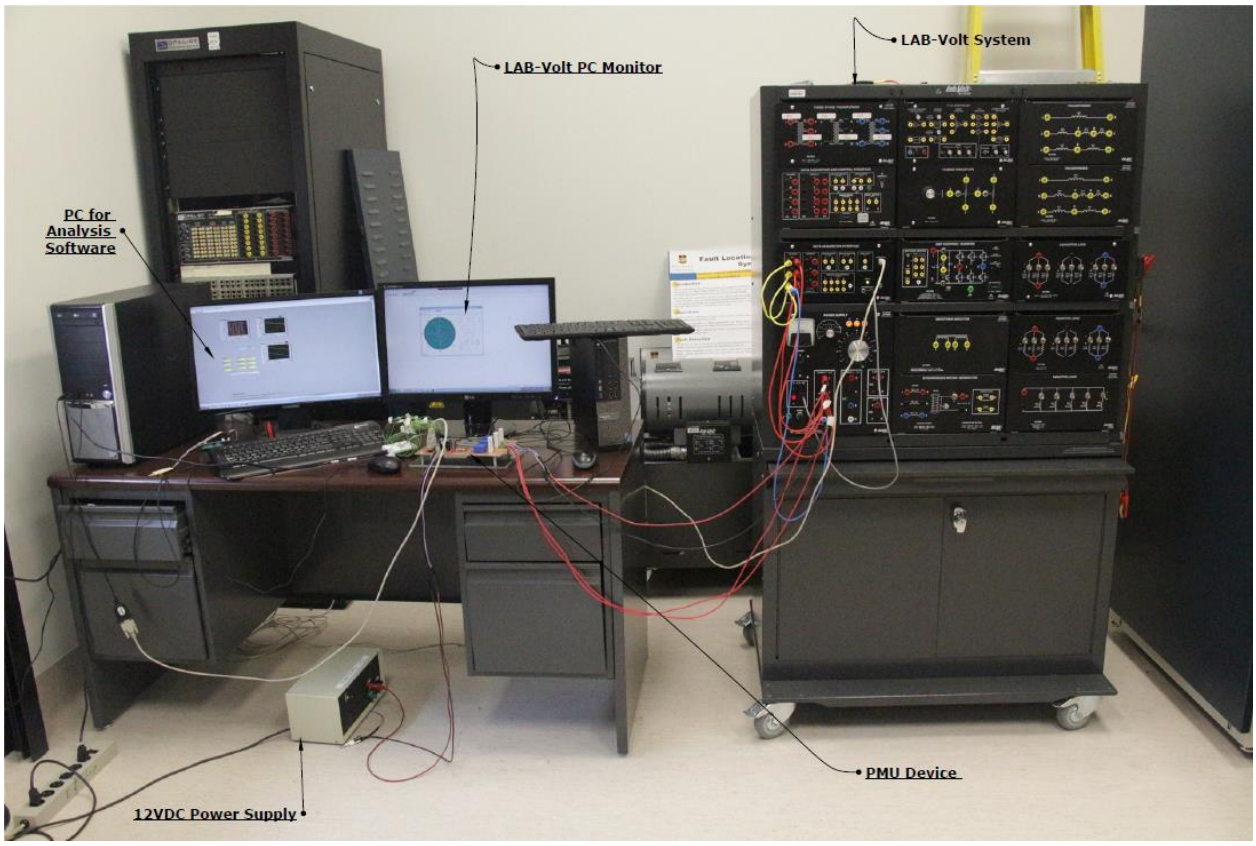

Figure 4-2 PMU device setup

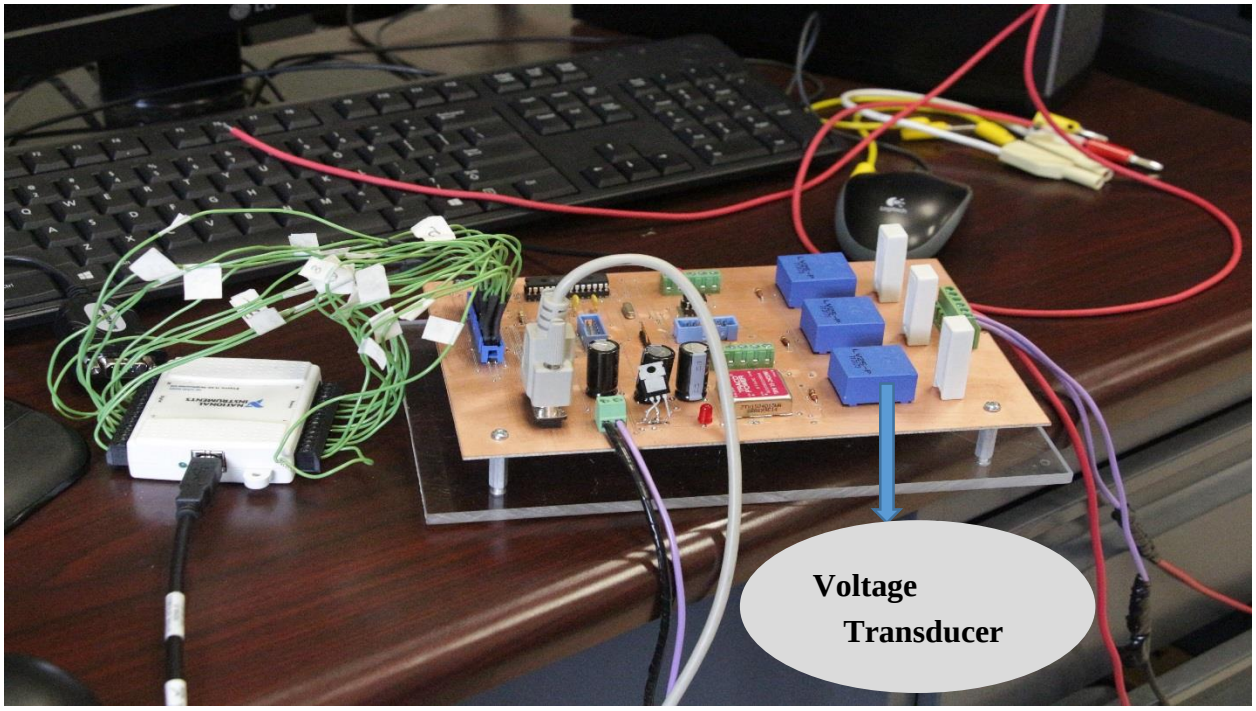

Figure 4-3 PMU device

4.3 Experiment 2: Accuracy of Phase Measurement

The second experiment involved designing an AC RC circuit and measuring specific electrical quantities in this circuit. It is known that PMUs are typically used to provide phase angle difference measurement from voltages and currents measured at different locations in a network. To evaluate this feature, a simple RC circuit as shown in Figure 4-4 was setup. The voltage V_1 represents the source voltage to the circuit and V_2 is the voltage across the C_1 capacitor. The aim of this experiment is to determine the phase angle difference between these two AC voltages. The estimated phase angle difference by the PMU is evaluated against the theoretical phase angle difference. The estimated and calculated results are presented in section 4.5.2.

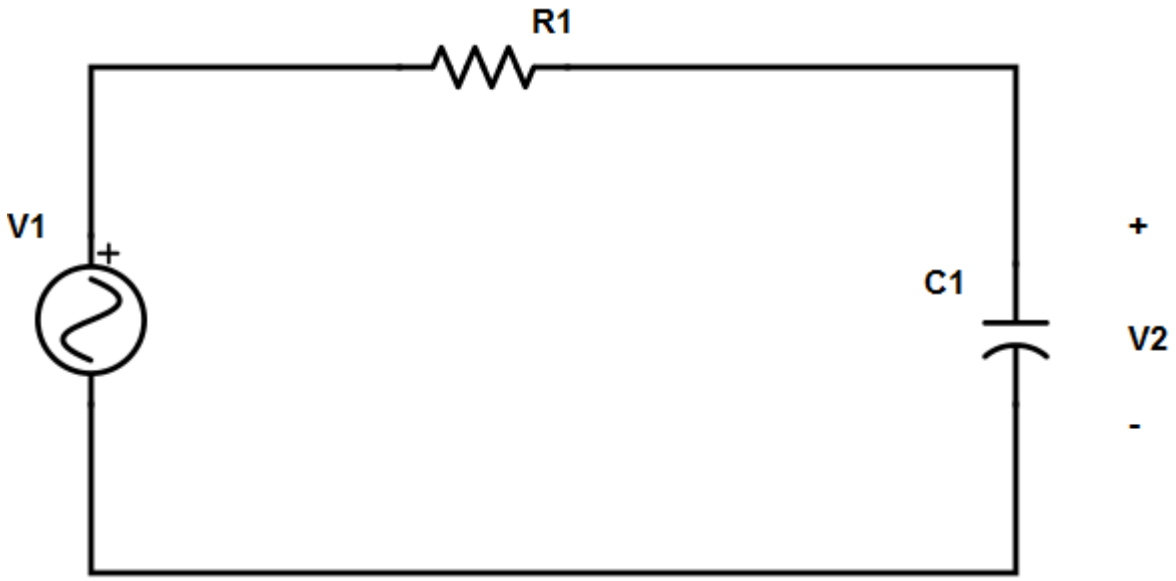

Figure 4-4 RC Circuit

Figure 4-4 shows an RC circuit where the major source of power comes from an AC power source (which is still the Lab-Volt system). In this experiment theoretically, $V_1 = 120 < 0^0 V$, $R_1 = 300\ ohms$, $C_1 = 4.4\mu F, 2.2\mu F$.

4.4 Measurement evaluation and compliance

It is a known fact that the theoretical values of a synchrophasor representation of a sinusoid and the values obtained from a PMU differ in both amplitude and phase [3]. A quantity exists that showcases the differences between a perfect sample of a theoretical synchrophasor and the estimates given by the unit test at the same instant of time. This quantity as discussed in Chapter 2 is the TVE and its value is normalized and expressed as per unit of the theoretical phasor. Under TVE, the amplitude and phase angle of a signal are considered for evaluation. Therefore the accuracy of PMUs are determined based on test signals. In [24] test signals were be generated by:

1) Defining mathematical functions
2) Software simulations or
3) Recorded oscillograms of real-world transients.

The compliance test for synchrophasor falls under the steady state compliance and the dynamic compliance tests as discussed in chapter 2. It is known that the fundamental parameters of a sinusoidal waveform are amplitude, phase angle, and frequency. The motive of the steady state test is to increment one of these parameters while keeping the other two parameters constant. Steady-state conditions are where amplitude, frequency and phase angle of the test signal, and all other influence quantities are fixed for the period of the measurement [3]. On the other hand the dynamic compliance is concerned with measurement bandwidth, linear system frequency ramp and the step input response [25]. This PMU design has only assessed the transducer performance as seen in experiment 1. The amplitude voltage is varied between 100 to 120 Vac (rms). When the voltage magnitude of the input phasor from the Lab-Volt system is varied, the obtained phasor from the PMU design is recorded as shown in section 4.5.

This thesis will not evaluate the current PMU design against the dynamic compliance test and other steady state test. Only the vector magnitude test under the steady-state condition has been performed to investigate the performance of the voltage transducer in reference to voltage amplitude measurement. The motivation behind this PMU design, is to design an educational PMU model that will showcase the basic operation and functionality of a synchrophasor.

4.5 Results and analysis

4.5.1 Experiment 1: Accuracy of Voltage Monitoring

To assess the performance of the voltage transducers of the PMU design, a simple experiment has been designed. As mentioned earlier, this experiment has varied the amplitude of the PMU design between 100 to 120 Vac (rms). This experiment has been carried out to evaluate the transducer performance. The results are presented in Table 4.1 to Table 4.6. In this experiment, voltage 1 has been used as the reference phase voltage for the other two voltages in terms of phase angle measurement. This is for both estimated and actual input measurement.

Table 4. 1 Input and Estimated Result of PMU system (120Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	119.44	60.03	-95.96
Voltage Transducer 2	119.14	60.02	23.97
Voltage Transducer 3	119.07	60.03	143.46
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	119.25	59.84	0.0
Voltage Transducer 2	120.08	59.88	119.6
Voltage Transducer 3	119.63	59.84	-119.3

Table 4. 2 Input and Estimated Result of PMU system (115Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	114.42	60.00	130.41
Voltage Transducer 2	115.41	59.99	-109.52
Voltage Transducer 3	115.37	59.99	9.86
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	115.00	59.91	0.0
Voltage Transducer 2	116.00	60.14	119.8
Voltage Transducer 3	115.59	59.88	-119.2

Table 4. 3 Input and Estimated Result of PMU system (110Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	109.42	60.01	-156.33
Voltage Transducer 2	110.14	60.01	-36.40
Voltage Transducer 3	110.02	60.00	83.14
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	109.58	59.84	0.0
Voltage Transducer 2	110.33	59.88	119.8
Voltage Transducer 3	110.01	59.88	-119.2

Table 4. 4 Input and Estimated Result of PMU system (105Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	105.01	59.98	-171.65
Voltage Transducer 2	105.51	59.97	-51.57
Voltage Transducer 3	105.48	59.99	67.72
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	105.33	60.01	0.0
Voltage Transducer 2	105.57	59.82	119.9
Voltage Transducer 3	105.44	59.85	-119.2

Table 4. 5 Input and Estimated Result of PMU system (100Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	100.55	59.99	1.34
Voltage Transducer 2	101.64	59.99	121.9
Voltage Transducer 3	101.50	59.99	-119.25
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	99.73	59.87	0.0
Voltage Transducer 2	101.02	59.95	119.8
Voltage Transducer 3	100.63	59.83	-119.3

Table 4. 6 –Input and Estimated Result of PMU system (95Vrms)

Sensor	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage Transducer 1	96.10	60.00	-13.88
Voltage Transducer 2	96.89	60.00	106.01
Voltage Transducer 3	96.96	59.99	-134.37
Sensor	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (Voltage 1 reference)**
Voltage Transducer 1	94.93	59.82	0.0
Voltage Transducer 2	95.62	59.82	120.3
Voltage Transducer 3	95.35	59.84	-191.1

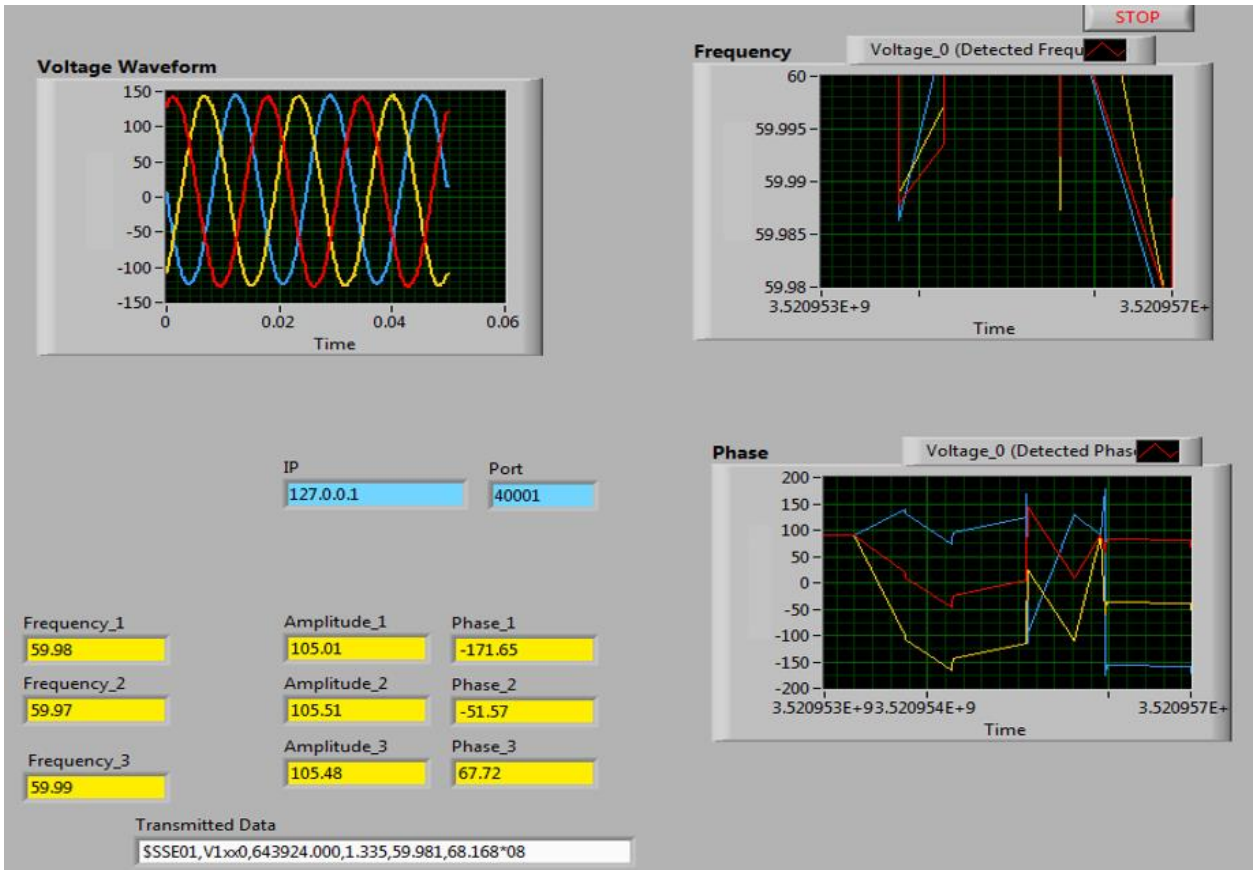

Figure 4-5 Snapshot of estimated phasor in Labview (110Vrms)

From Table 4.1 to Table 4.6, the results for phasor estimation is presented. Each table shows the voltage magnitude and phase angle of the input and the estimated phasor with reference to the voltage transducer concerned. The vector magnitude plot for voltage transducer 2 is shown in Figure 4-6. Figure 4-5, shows a snapshot of the LabVIEW environment for phasor estimation. A look at the "Voltage Waveform" in Figure 4-5 shows an amplitude of around 149V which is the peak voltage for an rms voltage of 105Vrms. When the estimation software is run, the frequency and phase angle plots are able to estimate the respective phasors as shown on the software working environment. The frequency and phasor plots of Figure 4-5 show transients for some seconds of both waveforms (oscillating) before generating a constant value for frequency and phasor.

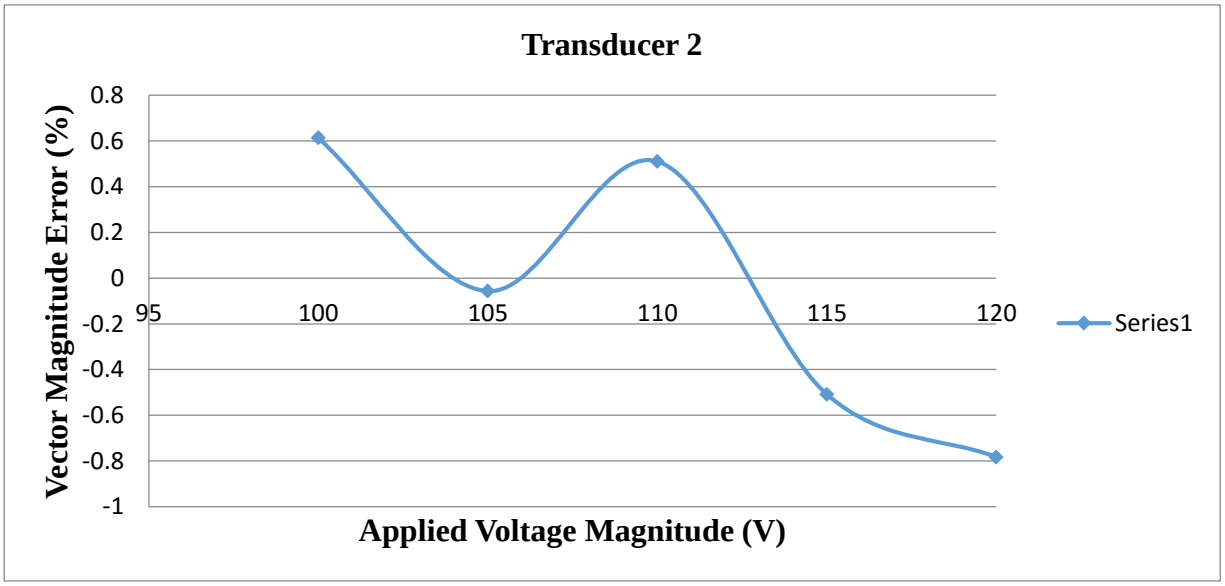

Figure 4-6 Vector magnitude error for a voltage transducer

It can be seen in Figure 4- 6 that the magnitude error is within $\pm 0.8\%$ for one of the voltage transducers across the range of 100 to 120 Vac (rms).

The other two voltage transducers produce errors that were lower than the 1% voltage magnitude error which is needed to showcase the accuracy of the transducers used.

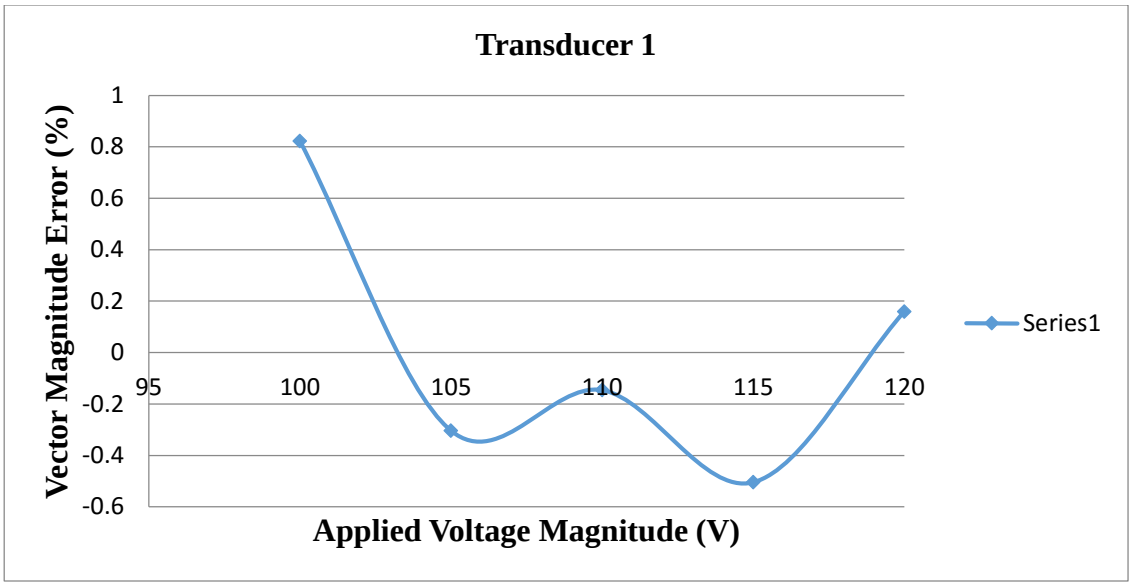

Figure 4-7 Vector magnitude error for voltage transducer 1

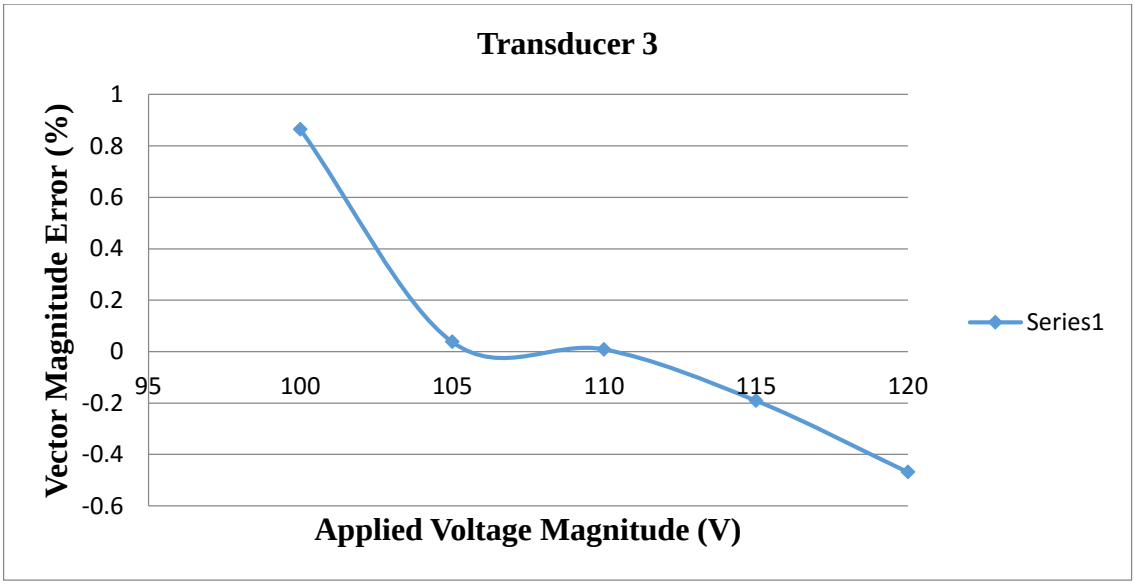

Figure 4-8 Vector magnitude error for voltage transducer 3

The phase angle of all the input voltage signals sent to the voltage transducer was also recorded in this experiment. It should be made clear that the Lab-Volt system used for supplying the balanced three phase voltage signal to the PMU device has been configured to

have voltage 1 (E_1) as the reference for phase angle measurement while the 1PPS signal from the GPS is the reference for the PMU design. Hence the absolute phase readings between phase readings do not match for both cases. However, the electrical angle between phases remains essentially 120^0 in the PMU.

4.5.2 Experiment 2: Accuracy of Phase Measurement

Table 4.7 and 4.8 show the estimated phasors results of the RC circuit for phasor V_1 and phasor V_2. From Table 4.7, the phase angle (φ) between $V_1$and V_2 with $C_1 = 4.4\mu F$ for both the input measurement and the PMU estimation are -27.5^0 and -27.52^0respectively. For Table 4.8, with $C_1 = 2.2\mu F$ the phase angle difference is -14.3^0 and -14.32^0 respectively.

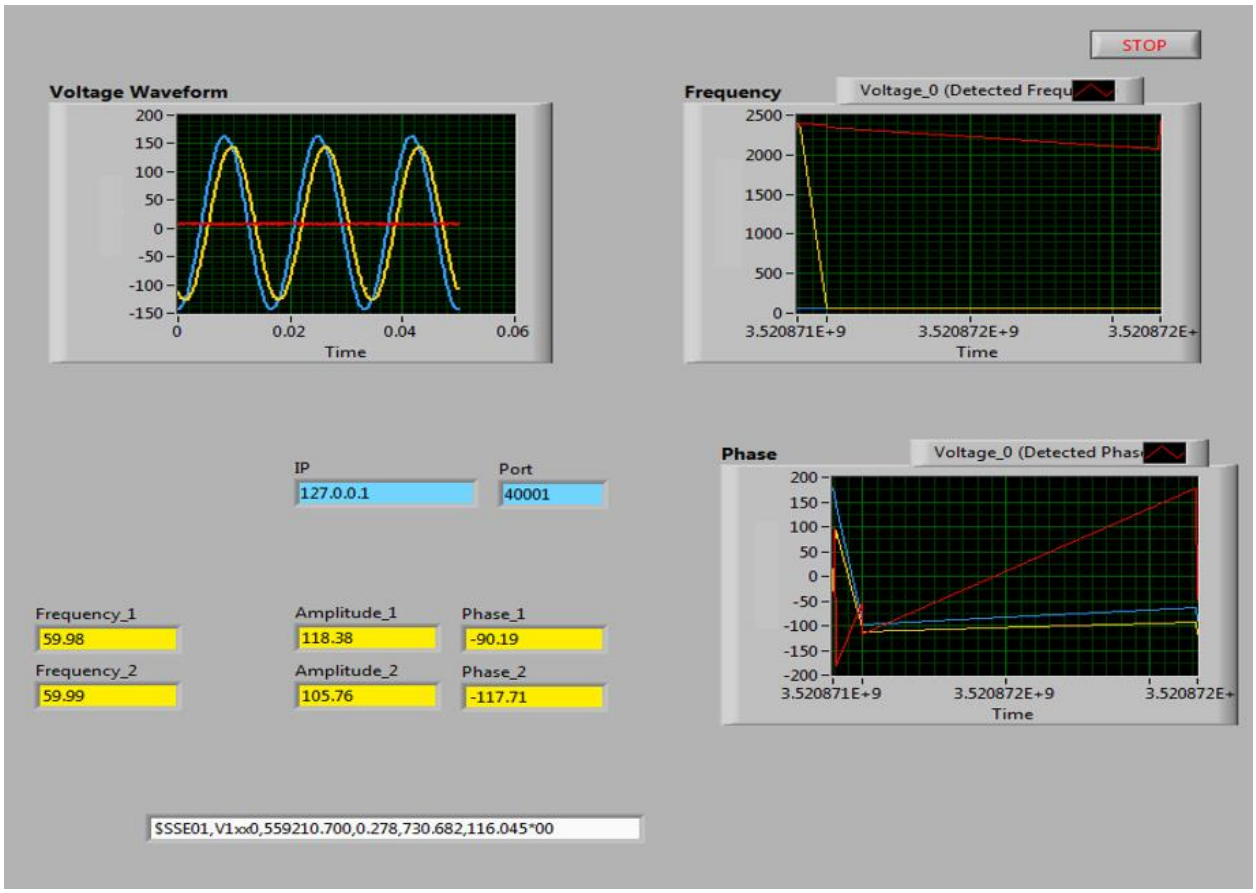

Figure 4-9 Estimated phasor

Figure 4-9 shows the estimated phasor after computation in the LabVIEW environment. The blue color signal in all three waveform represents Amplitude_1 under the voltage waveform, Frequency_1 under the frequency waveform and Phase_1 under the phasor waveform. Amplitude_2, Frequency_2 and Phase_2 signify the yellow color signal. It should be known that the red color signal in all three plots should be disregarded because only two phases are being considered.

Table 4. 7 - Input and Estimated Result of PMU system ($C_1 = 4.4\mu F$)

Voltage	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage 1	118.38	59.98	-90.19
Voltage 2	105.76	59.99	-117.71
Voltage	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	φ = -117.71- (-90.19)= **-27.52**
			Phase Angle (deg.) (Voltage 1 reference)
Voltage 1	118.97	59.84	0.0
Voltage 2	105.32	60.03	-27.5
			φ = -27.5 – (0.0) = **-27.5**

Table 4. 8 - Input and Estimated Result of PMU system ($C_1 = 2.2\mu F$)

Voltage	**Estimated RMS Voltage (V)**	**Obtained Frequency (Hz)**	**Phase Angle (deg.) (1PPS reference)**
Voltage 1	118.15	60.00	-98.47
Voltage 2	114.05	59.99	-112.79
Voltage	**Input RMS Voltage (V)**	**Obtained Frequency (Hz)**	φ = -112.79 – (-98.47) = **-14.32**
			Phase Angle (deg.) (Voltage 1 reference)
Voltage 1	119.22	59.92	0.0
Voltage 2	115.00	60.05	-14.3
			φ = -14.3 – (0.0) = **-14.3**

Considering Figure 4-4 and applying the voltage divider's rule, the voltage across C_1 is calculated thus:

$$V_2 = \left(\frac{{}^{1}/_{j\omega C}}{R + {}^{1}/_{j\omega C}} \right) V_1$$

$$V_2 = \left(\frac{1}{1 + j\omega RC} \right) V_1$$

The theoretical value for $V_1 = 120 < 0^0\ Vrms, R = 300\ ohms, C = \ 4.4\mu F$

$$therefore\ V_2 = \mathbf{107.42\ Vrms}$$

$$phase\ angle\ (\varphi) = -90^0 - \left(-tan^{-1} {}^{\left(\frac{1}{\omega C}\right)}/_{R} \right) = -26.46^0$$

With $C = \ 2.2\mu F$,

$$V_2 = \mathbf{116.45\ Vrms}$$

$$phase\ angle\ (\varphi) = -90^0 - \left(-tan^{-1} {}^{\left(\frac{1}{\omega C}\right)}/_{R} \right) = -13.97^0$$

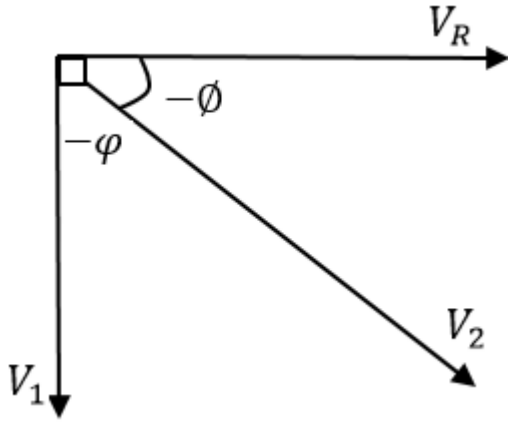

Figure 4-10 Phasor Diagram

It should be known that φ is the angle between V_1 and V_2. The calculated results show that with $C = 4.4\mu F$ the phase angle difference between V_1 and V_2 is -26.46^0. For $C = 2.2\mu F$ the phase angle difference between V_1 and V_2 is -13.97^0. Comparing the measured and the estimated phase angle with the calculated phase angle, it can be seen that the PMU can actually serve as a very important tool to monitor phase angle difference and report deviations from the statutory limits of these phase angles when they occur.

It should be known that phase angle estimation by the PMU has been done using the 1PPS signal from the GPS as reference while the phase angle of the calculated phasor would take its point of reference from voltage V_1. Synchrophasors are commonly reported in angles -180^0 to $+180^0$ rather than 0^0 to 360^0 as shown in Figure 4-11. This is why all the phase angles of the phasor estimates look different from the phase angle measurement from the input signal.

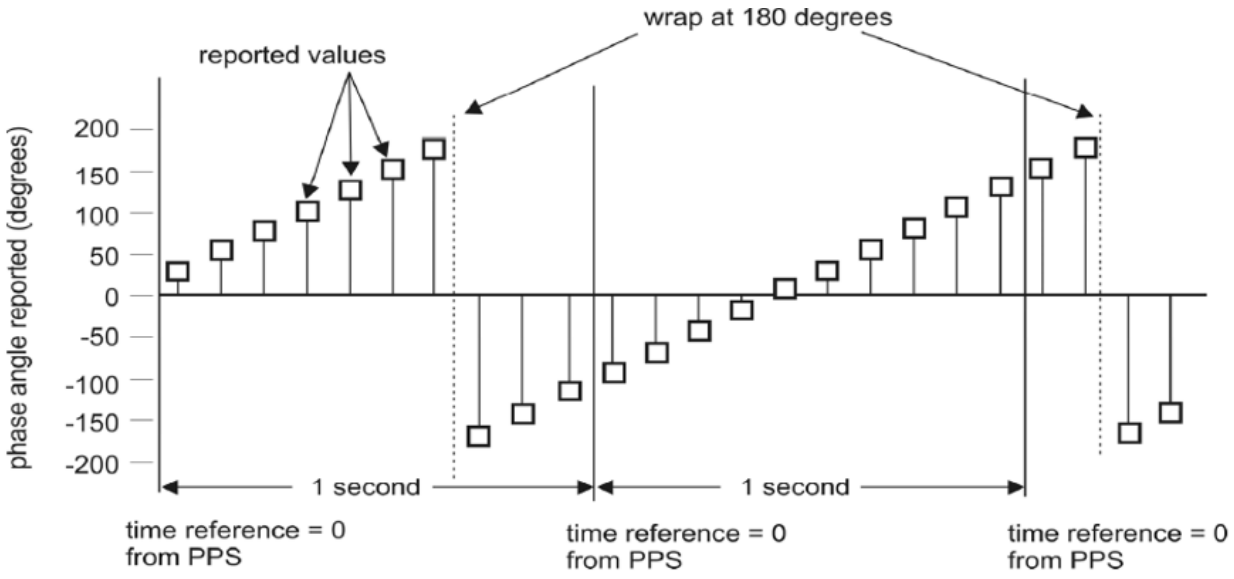

Figure 4-11 Sampling a power frequency sinusoid [3]

Chapter 5: Conclusion and Future Work

5.1 Contributions

The major contributions of this thesis are:

Schematic & PCB design of a PMU

A schematic as well as a PCB design was successfully implemented for the PMU in this thesis. This schematic design was implemented using the DesignSpark PCB 7.0 software which also provided a platform for the direct conversion of the schematic into PCB format. The beauty of this software is its user friendliness to create foot prints for components not available in its library.

Investigation of PMU standards and literature

This thesis has investigated the various synchrophasor standards starting with the first standard introduced in 1995 to the latest standard which was approved in 2011. The changes and improvement made from the first standard to the latest standard has been deeply investigated and explained in the thesis. Furthermore, this thesis has also highlighted important PMU innovation and technology introduced by different PMU groups using open platforms.

Construction and assembly of PMU

A PMU was successfully constructed by the assembly of different components that make up the PMU and soldering them. The mounting of the components on the PCB was achieved using through-hole technology. A single but double sided PCB board was used for the PMU design to allow for much higher component density by preventing component overload or too much board space on board.

Power system network monitoring

Through this work, PMUs have shown important usage in the area of monitoring the power system network by taking measurement of power system quantities such as phase angle, voltage magnitude, and frequency. These measurements are useful because they could be used as a yardstick or benchmark to detect faults or contingencies in the power system network before they escalate and lead to major issues in the network.

Knowledge contribution

The constructed PMU in this thesis will go a long way to contribute knowledge to the technology behind PMU design. The ability to utilize off-the-shelf electronic components to construct a PMU device that can readily meet specific needs in power systems is a major boost that will motivate students to delve into PMU research and make meaningful impacts. The designed PMU will provide a platform to educate and enlighten undergraduate students on the basic function of PMUs.

5.2 Conclusion

The constructed PMU has been able to achieve its fundamental purpose of estimating phasors based on balanced three phase voltage signals delivered to the device. The three voltage transducers in PMU show a voltage magnitude within $\pm 1\%$ across the range of 100 to 120 volts rms. Based on the achieved results it can be seen that a PMU device is possible to be constructed to meet specific educational needs tailored at contributing idea and knowledge to PMU design. The primary aim of this thesis remains to construct a PMU for educational purposes. This thesis has shown that it is possible to design a PMU device by simply using open source tools and off-the-shelf electronic components or products. The PMU designed for this thesis was constructed with$\sim C$ $700 in parts. The PMU system designed could be said to be more compliant with the M class of synchrophasors and not the P class [3]. This is because of its measurement and monitoring roles as "M" stands for measurement in the synchrophasor standard.

5.3 Recommended Future work

The future work for this thesis will simply involve ensuring that the designed PMU is compliant with the IEEE C37.118 standards for synchrophasors for both synchrophasor measurements and data transfer. This will involve performing all the evaluation and compliance tests which will go a long way to verify and assess the performance of the PMU device. These tests will require generating test signals to allow comparing of theoretical phasors with estimated phasors. For steady state and dynamic tests, TVE will be the major criteria to make this comparison possible. A number of researchers have deployed several

methods for generating tests signals essential for theoretical phasor estimation. In [25], test signals were generated for dynamic performance evaluation and testing of PMU.

The test signals were generated from mathematical models built in power system PSCAD/ EMTDC software played back to the PMU through a Doble F6150 real-time playback device with precise GPS synchronization. In [25] the PMU outputs have been evaluated against the actual test signals generated from the mathematical models. Furthermore, one of the setbacks of using the FFT or DFT algorithm for synchrophasor estimation is that it is unable to properly follow phasor changes that occur inside the observation window, thereby leading to wrong phasor estimation. To obtain better phasor estimation, a number of studies have been carried out. As a future work, use of the Taylor Fourier Transform (TFT) based on a Weighted Least Square (WLS) approximation of an observation window with respect to a second order Taylor model has been proposed in [26]. With this algorithm implemented in LabVIEW or any related software platform, dynamic phasor measurements can easily be observed.

Finally, it is necessary to ensure that estimated results can be sent through communication channels via the internet to PDCs that are located far away from PMUs. It will be noted that this thesis did not test the communication structure/ ability of the constructed PMU. This has also been included as a major area to be assessed for further work in the future.

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Appendix

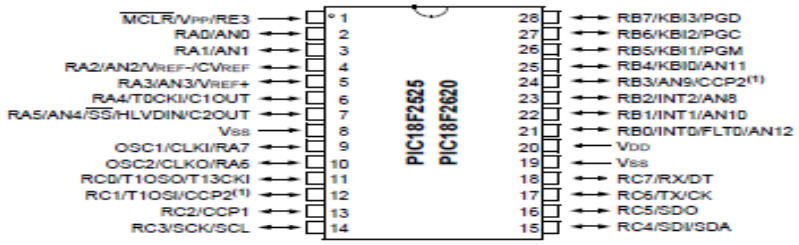
1. PIC 18F2525 Datasheet

PIC18F2525/2620/4525/4620
Data Sheet

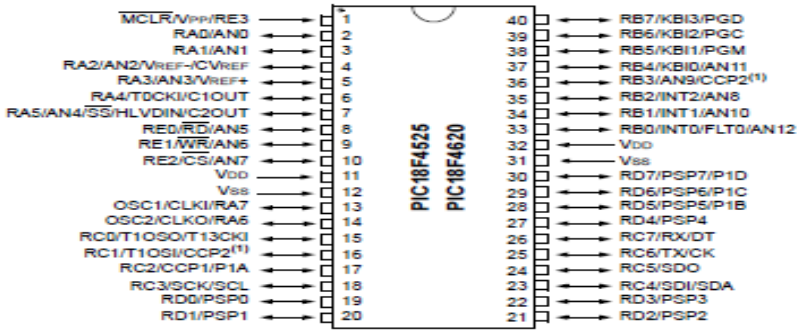
28/40/44-Pin
Enhanced Flash Microcontrollers
with 10-Bit A/D and nanoWatt Technology

Pin Diagrams

28-Pin SPDIP, SOIC



40-Pin PDIP



Note 1: RB3 is the alternate pin for CCP2 multiplexing.

Figure A- 1 Pin diagram of PIC 182525 (28 – Pin SPDIP)

2. Voltage transducer datasheet

LEM

Voltage Transducer LV 25-P

I_{PN} = 10 mA
V_{PN} = 10..500 V

For the electronic measurement of voltages : DC, AC, pulsed..., with a galvanic isolation between the primary circuit (high voltage) and the secondary circuit (electronic circuit).

5 YEARS GMT TRANSDUCERS WARRANTY

CE

RoHS COMPLIANT 2002/95/EC

16084

Electrical data

I_{PN}	Primary nominal current rms		10		mA
I_{PM}	Primary current, measuring range		0 .. ± 14		mA
R_M	Measuring resistance		$R_{M\ mini}$	$R_{M\ maxi}$	
	with ± 12 V	@ ± 10 mA $_{maxi}$	30	190	Ω
		@ ± 14 mA $_{maxi}$	30	100	Ω
	with ± 15 V	@ ± 10 mA $_{maxi}$	100	350	Ω
		@ ± 14 mA $_{maxi}$	100	190	Ω
I_{SN}	Secondary nominal current rms		25		mA
K_N	Conversion ratio		2500 : 1000		
V_C	Supply voltage (± 5 %)		± 12 .. 15		V
I_C	Current consumption		10 (@ ±15 V) + I_S		mA

Accuracy - Dynamic performance data

X_G	Overall Accuracy @ I_{PN}, T_A = 25°C	@ ± 12 .. 15 V	± 0.9		%
		@ ± 15 V (± 5 %)	± 0.8		%
ε_L	Linearity error		< 0.2		%
			Typ	Maxi	
I_O	Offset current @ I_P = 0, T_A = 25°C			± 0.15	mA
I_{OT}	Temperature variation of I_O	0°C .. + 25°C	± 0.06	± 0.25	mA
		+ 25°C .. + 70°C	± 0.10	± 0.35	mA
t_r	Response time [1] to 90 % of I_{PN} step		40		µs

General data

T_A	Ambient operating temperature		0 .. + 70	°C
T_S	Ambient storage temperature		- 25 .. + 85	°C
R_P	Primary coil resistance @ T_A = 70°C		250	Ω
R_S	Secondary coil resistance @ T_A = 70°C		110	Ω
m	Mass		22	g
	Standards		EN 50178: 1997	

Note: [1] R_1 = 25 kΩ (L/R constant, produced by the resistance and inductance of the primary circuit).

Features

- Closed loop (compensated) voltage transducer using the Hall effect
- Insulated plastic case recognized according to UL 94-V0.

Principle of use

- For voltage measurements, a current proportional to the measured voltage must be passed through an external resistor R_1 which is selected by the user and installed in series with the primary circuit of the transducer.

Advantages

- Excellent accuracy
- Very good linearity
- Low thermal drift
- Low response time
- High bandwidth
- High immunity to external interference
- Low disturbance in common mode.

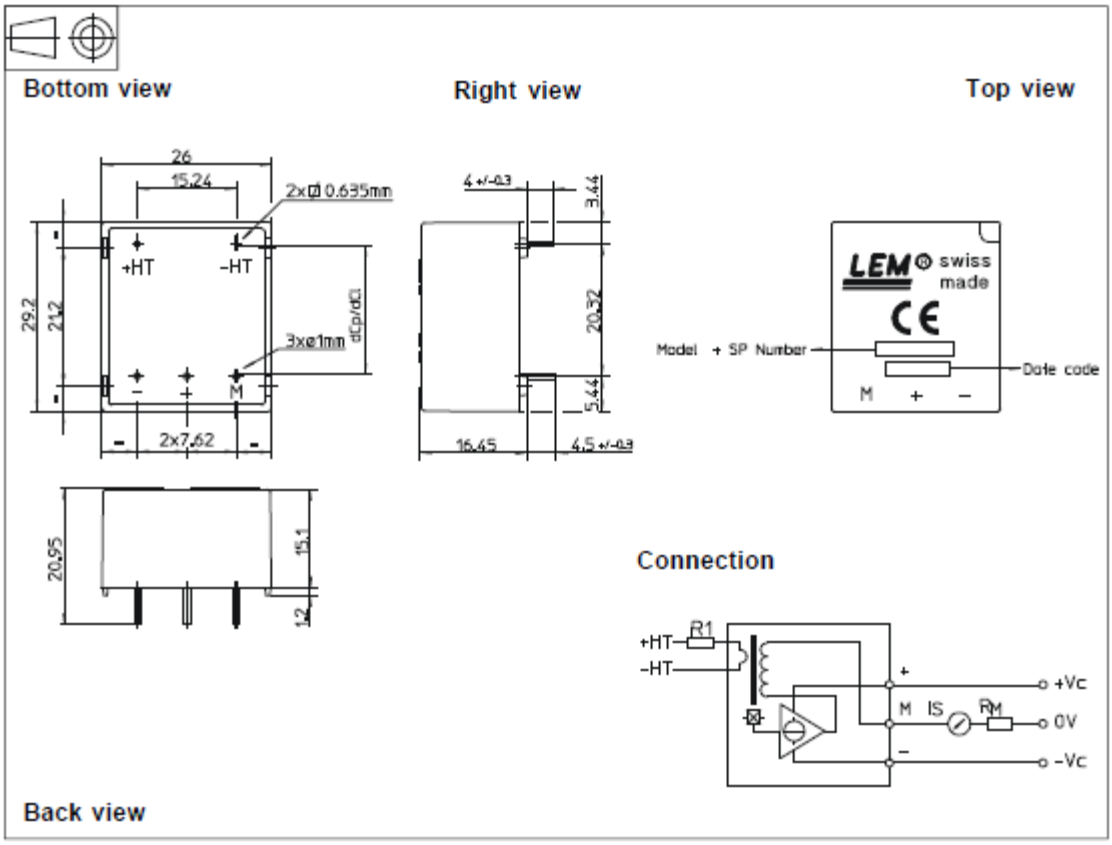
Applications

- AC variable speed drives and servo motor drives
- Static converters for DC motor drives
- Battery supplied applications
- Uninterruptible Power Supplies (UPS)
- Power supplies for welding applications.

Application domain

- Industrial.

Dimensions LV 25-P (in mm. 1 mm = 0.0394 inch)



Mechanical characteristics

• General tolerance	± 0.2 mm
• Fastening & connection of primary	2 pins 0.635 x 0.635 mm
• Fastening & connection of secondary	3 pins ∅ 1 mm
• Recommended PCB hole	1.2 mm

Remarks

- I_S is positive when V_P is applied on terminal +HT.
- This is a standard model. For different versions (supply voltages, turns ratios, unidirectional measurements...), please contact us.

Instructions for use of the voltage transducer model LV 25-P

Primary resistor R_1 : the transducer's optimum accuracy is obtained at the nominal primary current. As far as possible, R_1 should be calculated so that the nominal voltage to be measured corresponds to a primary current of 10 mA.

Example: Voltage to be measured V_{PN} = 250 V

a) R_1 = 25 kΩ / 2.5 W, I_P = 10 mA Accuracy = ± 0.8 % of V_{PN} (@ T_A = +25°C)
b) R_1 = 50 kΩ / 1.25 W, I_P = 5 mA Accuracy = ± 1.6 % of V_{PN} (@ T_A = +25°C)

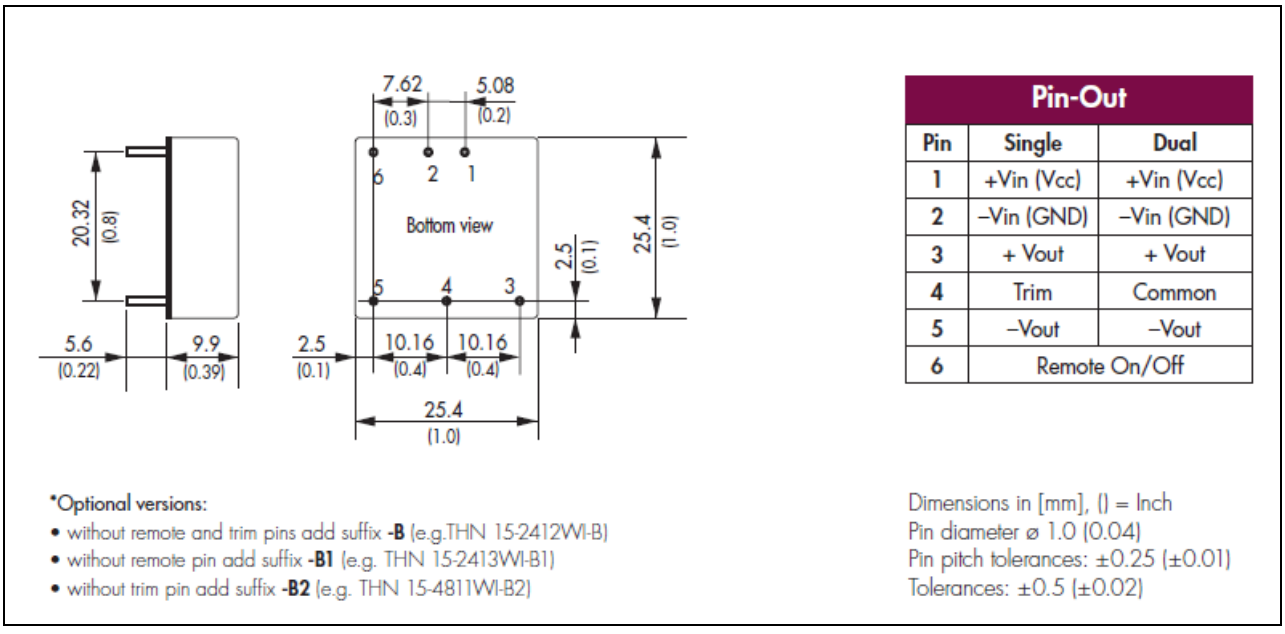
Operating range (recommended) : taking into account the resistance of the primary windings (which must remain low compared to R_1 in order to keep thermal deviation as low as possible) and the isolation, this transducer is suitable for measuring nominal voltages from 10 to 500 V.

3. Traco power (THN 15-2423WI) datasheet

Table A-1 Specification for traco power unit

Models

Order code	Input voltage range	Output voltage	Output current max.	Efficiency typ.
THN 15-2410WI	9 – 36 VDC (24 VDC nominal)	3.3 VDC	4'000 mA	86 %
THN 15-2411WI		5.0 VDC	3'000 mA	86 %
THN 15-2412WI		12 VDC	1'300 mA	87 %
THN 15-2413WI		15 VDC	1'000 mA	87 %
THN 15-2415WI		24 VDC	625 mA	90 %
THN 15-2421WI		±5 VDC	±1'500 mA	85 %
THN 15-2422WI		±12 VDC	±625 mA	87 %
THN 15-2423WI		±15 VDC	±500 mA	88 %
THN 15-2425WI		±24 VDC (48 VDC)*	±315 mA	91 %
THN 15-4810WI	18 – 75 VDC (48 VDC nominal)	3.3 VDC	4'000 mA	86 %
THN 15-4811WI		5.0 VDC	3'000 mA	87 %
THN 15-4812WI		12 VDC	1'300 mA	87 %
THN 15-4813WI		15 VDC	1'000 mA	87 %
THN 15-4815WI		24 VDC	625 mA	91 %
THN 15-4821WI		±5 VDC	±1'500 mA	85 %
THN 15-4822WI		±12 VDC	±625 mA	86 %
THN 15-4823WI		±15 VDC	±500 mA	87 %
THN 15-4825WI		±24 VDC (48 VDC)*	±315 mA	90 %



Pin-Out

Pin	Single	Dual
1	+Vin (Vcc)	+Vin (Vcc)
2	–Vin (GND)	–Vin (GND)
3	+ Vout	+ Vout
4	Trim	Common
5	–Vout	–Vout
6	Remote On/Off	

*Optional versions:
- without remote and trim pins add suffix **-B** (e.g.THN 15-2412WI-B)
- without remote pin add suffix **-B1** (e.g. THN 15-2413WI-B1)
- without trim pin add suffix **-B2** (e.g. THN 15-4811WI-B2)

Dimensions in [mm], () = Inch
Pin diameter ø 1.0 (0.04)
Pin pitch tolerances: ±0.25 (±0.01)
Tolerances: ±0.5 (±0.02)

Figure A- 2 Pin configuration for traco power

4. NI 6009 DAQ

Table A-2 Analog Terminal Assignments

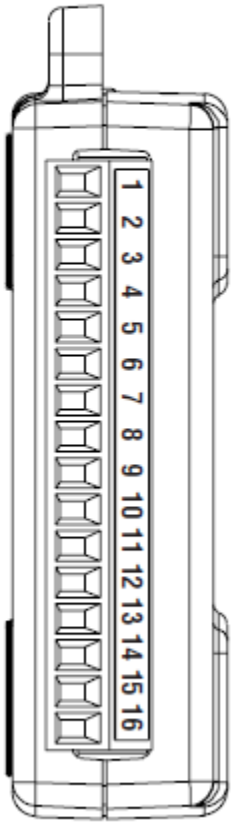
Module	Terminal	Signal, Single-Ended Mode	Signal, Differential Mode
	1	GND	GND
	2	AI 0	AI 0+
	3	AI 4	AI 0–
	4	GND	GND
	5	AI 1	AI 1+
	6	AI 5	AI 1–
	7	GND	GND
	8	AI 2	AI 2+
	9	AI 6	AI 2–
	10	GND	GND
	11	AI 3	AI 3+
	12	AI 7	AI 3–
	13	GND	GND
	14	AO 0	AO 0
	15	AO 1	AO 1
	16	GND	GND

Table A -3 Digital Terminal Assignments

Module	Terminal	Signal
	17	P0.0
	18	P0.1
	19	P0.2
	20	P0.3
	21	P0.4
	22	P0.5
	23	P0 6
	24	P0.7
	25	P1.0
	26	P1.1
	27	P1.2
	28	P1.3
	29	PFI 0
	30	+2.5 V
	31	+5 V
	32	GND

Table A-4 Signal descriptions

Signal Name	Reference	Direction	Description
GND	—	—	**Ground**—The reference point for the single-ended AI measurements, bias current return point for differential mode measurements, AO voltages, digital signals at the I/O connector, +5 VDC supply, and the +2.5 VDC reference.
AI <0..7>	Varies	Input	**Analog Input Channels 0 to 7**—For single-ended measurements, each signal is an analog input voltage channel. For differential measurements, AI 0 and AI 4 are the positive and negative inputs of differential analog input channel 0. The following signal pairs also form differential input channels: <AI 1, AI 5>, <AI 2, AI 6>, and <AI 3, AI 7>.
AO 0	GND	Output	**Analog Channel 0 Output**—Supplies the voltage output of AO channel 0.
AO 1	GND	Output	**Analog Channel 1 Output**—Supplies the voltage output of AO channel 1.
P1.<0..3> P0.<0..7>	GND	Input or Output	**Digital I/O Signals**—You can individually configure each signal as an input or output.
+2.5 V	GND	Output	**+2.5 V External Reference**—Provides a reference for wrap-back testing.
+5 V	GND	Output	**+5 V Power Source**—Provides +5 V power up to 200 mA.
PFI 0	GND	Input	**PFI 0**—This pin is configurable as either a digital trigger or an event counter input.