

A MULTI CHANNEL, TRANSISTORIZED,
COINCIDENCE--ANTICOINCIDENCE UNIT

by

Harvey L. Pollock



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Harvey L. Pollock

Winnipeg, Manitoba

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CHAPTER 1

ANALYSIS OF COINCIDENCE COUNTING

1.1 Introduction

Coincidence counting may be defined as the registration of events detected by separate detectors and occurring within a certain time interval, all other events being rejected. Anticoincidence counting may be defined as the non registration of events occurring within a certain time interval, all other events in a certain channel or channels being registered.

Coincidence methods have been used as early as 1930 in studies of cosmic rays which involve the detection of a single particle in two or more detecting units. More recently the coincidence technique has been used for studies of the simultaneous emission by nuclei of two or more separate particles each of which operates a detecting unit. Some of the more important uses of coincidence techniques in modern experiments are angular correlation studies, reduction of background level in which a detector is placed near the shield of a second detector used to measure the radiation from the source, and the shield detector operates in anticoincidence with the source detector. Coincidence techniques may also be applied to eliminate registration of noise pulses from detectors.

1.2 Theory of Coincidence Counting

A theory of coincidence counting has been developed by Dunworth¹ and others, a summary of which is given below.

Consider N disintegrations per minute of a nucleus A emitting two different particles p_1 , p_2 and yielding a nucleus B .

The net efficiency of detection of a particle, e_p , may be defined by $e_p = 1/4\pi \int_0^\pi E_p da$, where E_p is the efficiency of a detector for particles of type p proceeding outwards from the source in a solid angle da in some direction and the integration is carried out over all such elements of solid angle.

Let counter #1 detect Ne_1 particles of type p_1 and none of p_2 . Let Q_1 be the counting rate in counter #1 due to other causes, (cosmic particles, particles arising from other transitions in the disintegration of nucleus A , etc.). Let Ne_2 and Q_2 be the corresponding quantities for counter #2. Then the following will apply.

Total counting rate in counter #1 is $Ne_1 + Q_1 = D_1$

Total counting rate in counter #2 is $Ne_2 + Q_2 = D_2$

Genuine coincidence rate due to p_1 and p_2 is $Ne_1e_2 = G$

Cosmic coincidence rate is C , say.

The chance coincidence rate is given by $2D_1D_2P = F$, where P is the effective length of the electrical pulse at the mixer stage of the coincidence counter.. P is defined

as the resolving time of the coincidence circuits and in the above is assumed to be a constant of the circuit.

Suppose the coincidence count in the above is carried out for a time T minutes. Since the time of experiment is finite, the observed total coincidence counting rate will be subject to a standard deviation given by

$$\left(\frac{(C + G + F) T}{T} \right)^{\frac{1}{2}}$$

The fractional error f in the genuine coincidence rate G , determined by the above coincidence circuit is

$$f = \left(\frac{(C + G + F)}{T} \right)^{\frac{1}{2}} \cdot \frac{1}{G} \quad (1.2.1)$$

It has been assumed in the above that C and F have been previously determined with sufficiently small error.

Now $e_1 = G/(D_2 - Q_2)$ and since $(D_2 - Q_2)$ is much larger than G , the fractional error in the determination of $(D_2 - Q_2)$ in a time T is much less than f . Hence the error in e_1 may be attributed entirely to the error in G .

Substituting for G , F , and D_2 in equation (1.2.1) and simplifying yields

$$f = \frac{1}{T^{\frac{1}{2}}} \left\{ \frac{1}{N e_1 e_2} + \frac{C}{(N e_1 e_2)^2} + \frac{2P}{e_1 e_2} \left(1 + \frac{Q_1}{N e_1} \right) \left(1 + \frac{Q_2}{N e_2} \right) \right\}^{\frac{1}{2}} \quad (1.2.2)$$

Clearly in the above as N increases, f falls to a limiting value of

$$\frac{1}{T^{\frac{1}{2}}} \left[\frac{2P}{e_1 e_2} \right]^{\frac{1}{2}} = f_L$$

In practice, C is much smaller than $N e_1 e_2$, Q_1 is much smaller than $N e_1$, and Q_2 is much smaller than $N e_2$. Now if N_0 is the value of N for which the chance coincidence rate is equal to the genuine coincidence rate, then

$$2(N_0 e_1 / Q_1) \cdot (N_0 e_2 / Q_2) \cdot P = N_0 e_1 e_2$$

and taking note of the conditions imposed above, we get

$$N_0 = 1/2P \quad (1.2.3)$$

If the value of N_0 is substituted into equation (1.2.2) under the imposed conditions, the result yields $f = \sqrt{2} f_L$. It is clear from the above that there is no great advantage obtained by increasing N to a value greater than N_0 and that for a given accuracy f , the required counting time approaches the limiting value $2P/(e_1 e_2 f^2)$. From equation (1.2.3) it is clear that the maximum source strength is governed solely by the resolving time of the electrical circuits. It should also be noted that for a given detection efficiency and counting time, the fractional error varies directly as the square root of the resolving time. Hence it is desirable to obtain the lowest possible resolving time for the circuits.

1.3 Specifications for the Coincidence Circuit

From the preceding theory of coincidence counting the specifications for the coincidence circuit have been compiled and are listed below.

- (1) In order for the resolving time to be constant for a given set of circuits it is necessary that it be independent of the

single counting rates in the counters, the size of the pulses from the counters, and the shape of the pulses from the counters.

(2) The satisfactory use of a small resolving time will be possible only if it is greater than the rise time of operation of the detectors and the time interval between the successive emission of the particles to be detected. Since the time interval between associated events is generally of the order of 10^{-12} seconds, and since the rise time of operation of the detector varies between 10^{-6} and 10^{-9} seconds depending on the type of detector used, the minimum allowable resolving time for coincidence measurements will depend on the particular detector selected. It should be noted that for the values of resolving time mentioned above, the maximum source strength required for coincidence experiments will be of the order of 10^{-1} to 10^{-4} curies[#].

[#] 1 curie $\equiv 3.7 \times 10^{10}$ disintegrations per second.

CHAPTER 2

TRANSISTOR SWITCHING CIRCUITS

2.1 Analysis of the Grounded Base Transistor Circuit

It has been shown² that the equivalent T-network for a transistor may be represented as in Fig. (1) for the common base configuration. Referring to Fig. (1), it is seen that r_{mie} is a fictitious voltage generator that transforms a passive T-network into an active transistor equivalent network. The internal parameters of the transistor are represented by r_e , r_b , and r_c . The equations of the circuit may be written in the form

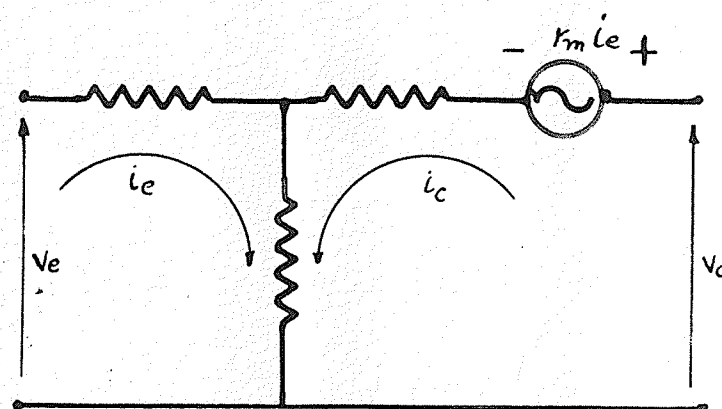
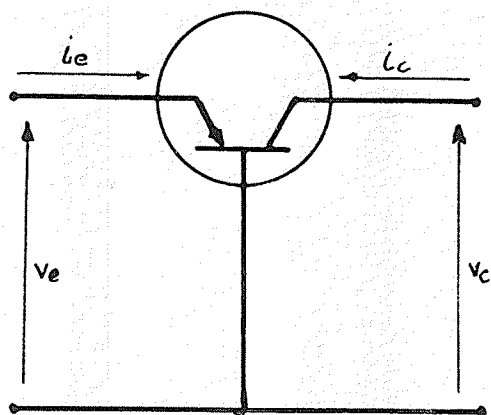
$$\begin{bmatrix} v_e \\ v_c \end{bmatrix} = \begin{bmatrix} r_{11} & r_{12} \\ r_{21} & r_{22} \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix}$$

and upon substitution of the circuit constants the equations become

$$\begin{bmatrix} v_e \\ v_c \end{bmatrix} = \begin{bmatrix} (r_e/r_b) & r_b \\ (r_m/r_b) & (r_b/r_c) \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix}$$

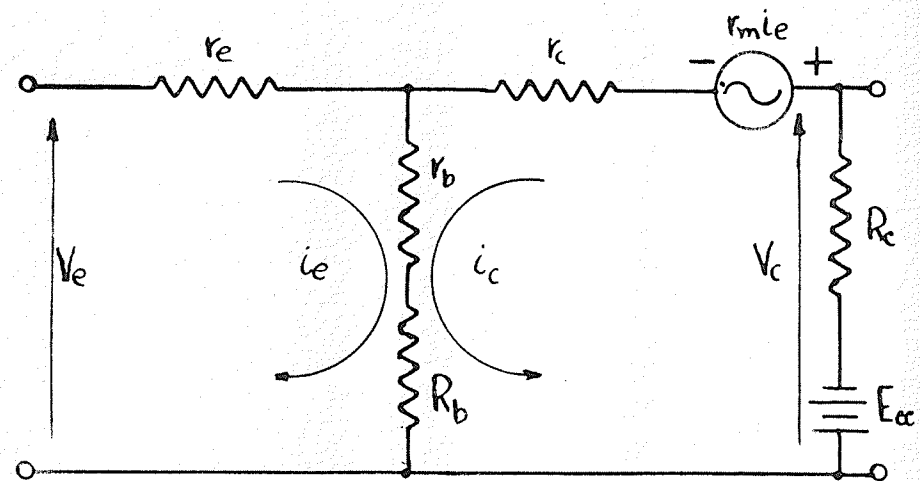
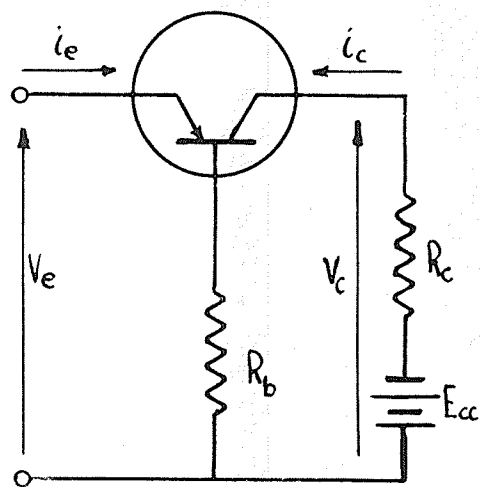
It is desirable to obtain an expression for the input voltage v_e as a function of the input current i_e , termed the emitter input characteristic.

Consider the circuit of Fig. (2) in which R_b and R_c represent external loads.



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FIG.1 EQUIVALENT T NETWORK FOR GROUNDED BASE TRANSISTOR



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FIG. 2 TRANSISTOR NETWORK WITH LOADS

The circuit equations are given by

$$\begin{bmatrix} (r_e/r_b/R_b) & (r_b/R_b) \\ (r_b/R_b/r_m) & (r_c/r_b/R_b) \end{bmatrix} \cdot \begin{bmatrix} i_e \\ i_c \end{bmatrix} = \begin{bmatrix} v_e \\ v_c \end{bmatrix} \quad \begin{matrix} (a) \\ (b) \end{matrix} \quad (2.1.1)$$

A further equation may be written in the form

$$-E_{cc} = v_c / i_c R_c \quad (2.1.2)$$

If the expression for v_c from equation (2.1.1 b) is substituted into equation (2.1.2), the result is given by

$$-E_{cc} = i_e(r_b / r_m / R_b) / i_c(r_b / r_c / R_b / R_c) \quad (2.1.3)$$

Now, if the expression for i_c from equation (2.1.3) is substituted into equation (2.1.1 a), the result may be simplified to yield an expression for v_e as a function of i_e given by

$$v_e = i_e \left\{ r_e/r_b/R_b - (r_b/R_b) \frac{(r_m/r_b/R_b)}{r_b/r_c/R_b/R_c} \right\} - \frac{E_{cc} (r_b/R_b)}{r_b/r_c/R_b/R_c} \quad (2.1.4)$$

It is also desirable as will be seen shortly to obtain an expression for collector current i_c in terms of emitter current i_e , termed the transfer characteristic of the circuit. This may be obtained by rewriting equation (2.1.3) in the form

$$i_c = -i_e \frac{r_b / r_m / R_b}{r_b / r_c / R_b / R_c} - \frac{E_{cc}}{r_b/r_c/R_b/R_c} \quad (2.1.5)$$

For the purposes of simplification the following assumptions will be made.

- (1) R_b will be so chosen that β is much larger than r_b
- (2) In practice r_m is much larger than r_b and r_c is much larger than r_b and hence $\alpha \equiv \frac{r_m / r_b}{r_c / r_b} \approx \frac{r_m}{r_c}$, where α is the

short circuit current amplification factor.

If the above simplifications are taken into account, equations (2.1.4) and (2.1.5) become

$$v_e = i_e(r_e / R_b - R_b \cdot \frac{r_m/R_b}{r_c/R_b/R_c}) - E_{cc} \cdot \frac{R_b}{r_c/R_b/R_c} \quad (2.1.6)$$

$$i_c = -i_e \cdot \frac{r_m / R_b}{r_c/R_b/R_c} - \frac{E_{cc}}{r_c/R_b/R_c} \quad (2.1.7)$$

The emitter input and transfer characteristics may be separated into three distinct regions which are described below.

(a) Cutoff Region

In this region, both the emitter-base and collector-base diodes are open. The following conditions are then applicable.

r_e is much larger than R_b . $\alpha = 0$.

Imposition of the above conditions yields the following.

$$v_e = i_e r_e - E_{cc} \cdot \frac{R_b}{R_c/R_b/r_c} \quad (2.1.8)$$

$$i_c = -i_e \cdot \frac{R_b}{R_b/R_c/r_c} - E_{cc} \cdot \frac{1}{R_b/R_c/r_c} \quad (2.1.9)$$

(b) Transition Region

The characteristics of the Transition Region are that the emitter-base diode is conducting, the collector-base diode is open, and the circuit is subject to current amplification. The following assumptions are then valid.

r_e is much smaller than R_b .

Imposition of the above assumption leads to the following equations.

$$v_e = i_e R_b \cdot \frac{R_c}{R_b + r_c + R_c} - E_{cc} \cdot \frac{R_b}{R_b + r_c + R_c} \quad (2.1.10)$$

$$i_c = -i_e \cdot \frac{R_b + \alpha r_c}{R_b + r_c + R_c} - \frac{E_{cc}}{R_b + r_c + R_c} \quad (2.1.11)$$

It is of special interest to note from equation (2.1.10) that if R_c is less than $r_c(\alpha - 1)$, a negative emitter input resistance will be encountered in the transition region. It will be shown later that this condition is necessary to permit operation of the circuit as a trigger or switching circuit.

(c) Saturation Region

In this region, both the emitter-base and collector-base diodes are conducting. The transistor behaves approximately like a conductor. The following conditions are then applicable.

$\alpha \doteq 0$; r_e is much less than R_b ; r_c is much less than R_b .

Imposition of the above conditions yields the following.

$$v_e = i_e \cdot \frac{R_b R_c}{R_b + R_c} - E_{cc} \cdot \frac{R_b}{R_b + R_c} \quad (2.1.12)$$

$$i_c = -i_e \cdot \frac{R_b}{R_b + R_c} - \frac{E_{cc}}{R_b + R_c} \quad (2.1.13)$$

The preceding equations may be solved for the points of intersection of the transition and saturation regions yielding

$$i_e = \frac{E_{cc}}{\alpha(R_b + R_c) - R_b} \quad (2.1.14)$$

$$v_e = \frac{R_b(1-\alpha)E_{cc}}{\alpha(R_b/R_c)-R_b} \quad (2.1.15)$$

$$i_c = \frac{-\alpha E_{cc}}{\alpha(R_b/R_c)-R_b} \quad (2.1.16)$$

The results of tests made on two type 2N22, Northern Electric point contact transistors to determine the emitter input and transfer characteristics are given by the graphs of Fig. (3) and (4). The circuit parameters used in the determination of the theoretical curves were those specified by the manufacturer as typical values.

It is clear from the results obtained that the theoretical calculations for the emitter input and transfer characteristics will at best only serve to indicate the general behaviour of the circuit. It should also be noted that the characteristics obtained from each of the two transistors tested differed considerably, particularly at peak and valley points. It was felt that the main reason for the preceding ^{deviations} was the inability of the manufacturer to maintain a controlled production process. However, it should also be noted that part of the deviation may be attributed to the fact that r_c and α do not remain constant with varying emitter current as was assumed in the circuit analysis.

In view of the difficulty in obtaining transistors having nearly identical characteristics, it was felt that the experimental

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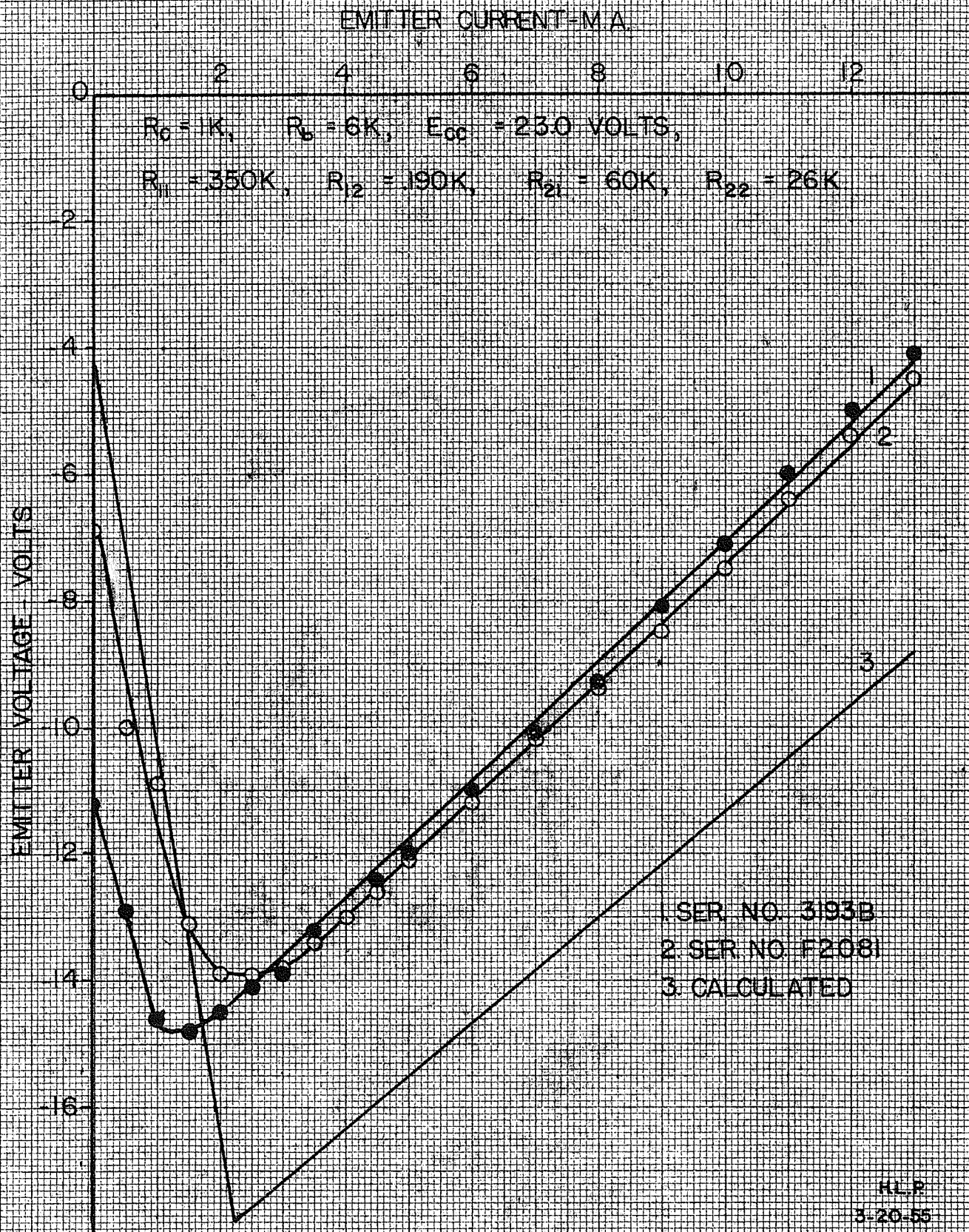


FIG. 3. EMITTER INPUT CHARACTERISTIC-2N22 TRANSISTORS

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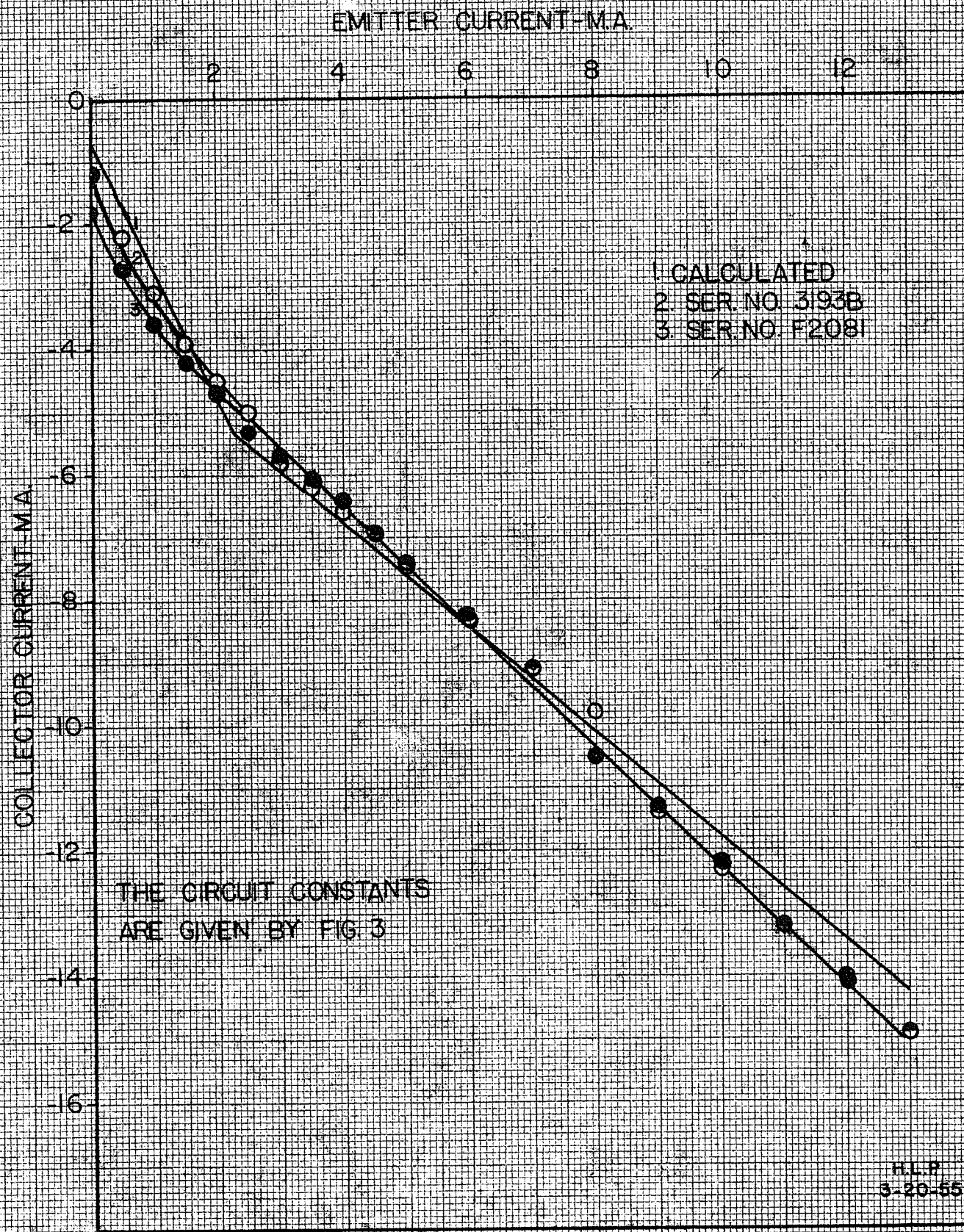


FIG. 4 TRANSFER CHARACTERISTIC 2N22 TRANSISTORS

approach would be most suited for the design of trigger circuits. This would necessitate the experimental choice of circuit components for each individual transistor as is shown elsewhere in this report.

2.2 The Grounded Base Transistor as a Trigger Circuit

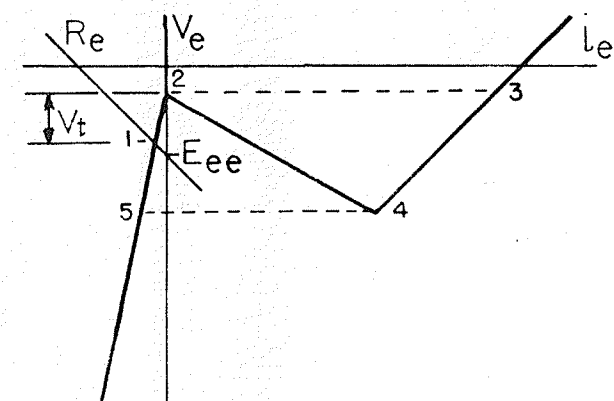
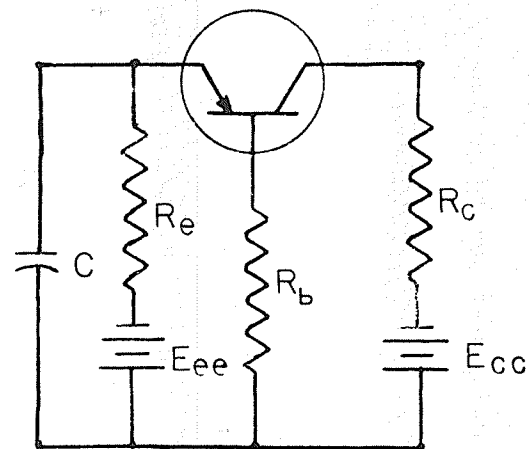
It has been previously shown that by proper choice of the external loads, the grounded base transistor may be made to exhibit a negative resistance characteristic. The various trigger circuits which may arise out of the negative resistance characteristic are the monostable, astable and bistable circuits. The monostable circuit is considered in detail below.

The basic monostable circuit and emitter input characteristic are given in Fig. (5). The basic equation governing the emitter input to the circuit in the quiescent condition is given by

$$v_e = -i_e R_e - E_{ee} \quad (2.2.1)$$

It is clear from the above that the d.c. load line for the circuit of Fig. (5) has a slope $-R_e$ and intercepts the v_e axis at $v_e = -E_{ee}$. Let the value of E_{ee} and R_e be so chosen that the load line intersects the emitter input characteristic only in the cutoff region.

In the quiescent state, C is fully charged and is

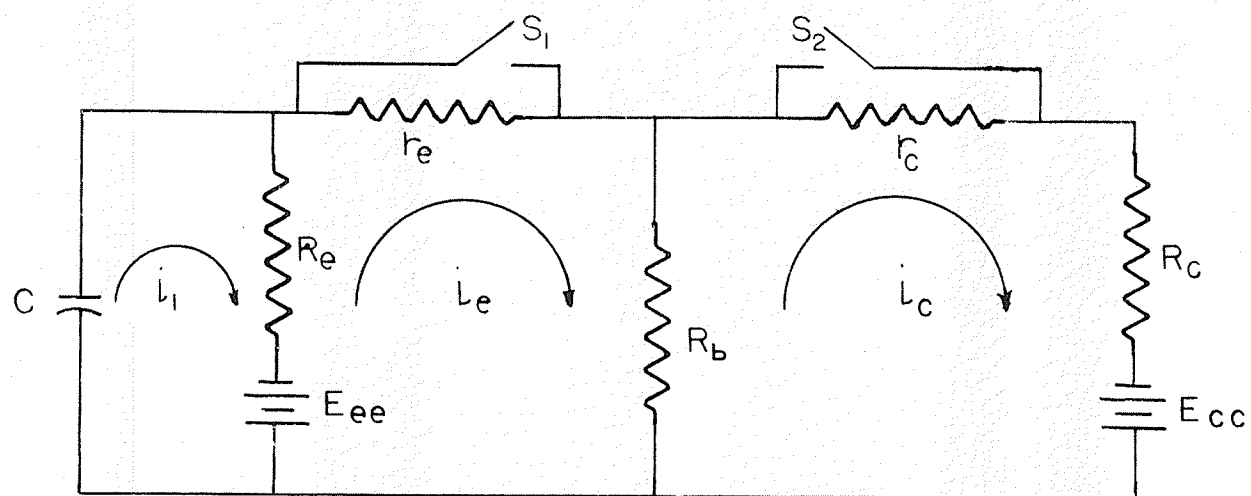


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FIG. 5 BASIC MONOSTABLE CIRCUIT

effectively an open circuit. Hence the operating point for the circuit must be at (1) on the emitter input characteristic. Let a triggering voltage V_t be applied to the emitter causing a triggering current to send a positive current into the emitter. The circuit will then pass into the unstable negative resistance region (2). By virtue of the current amplification within the transistor and the positive feedback action afforded by the base resistance, the collector and emitter currents increase rapidly and since the voltage across the condenser cannot change rapidly, the operating point will shift to the saturation region (3) at constant voltage. The condenser is now being charged in opposite polarity to that of the quiescent state. As the condenser continues charging, the operating point shifts along the saturation curve moving towards the valley point (4). When the unstable negative resistance region is again entered, the effect of diminishing emitter current and storing action of the capacitor is to shift the operating point at constant voltage to the cutoff region (5). The capacitor is then charged to its original polarity returning the operating point to its original position (1). The circuit is now able to repeat its cycle upon application of another trigger pulse.

The equivalent circuit for the monostable circuit is given by Fig. (6). The conditions imposed upon this circuit are given below.



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FIG. 6 EQUIVALENT CIRCUIT FOR MONOSTABLE OPERATION

- (1) At $t=0$, S_1 and S_2 are closed
 (2) $i_1 = 0$ for t less than 0. That is the condenser is fully charged in the quiescent state.

The circuit may be solved by the Laplace Transformation Method or any of the standard methods to yield the following equations.

$$i_e = I_0 \exp. \left[\frac{-R_b/R_c \cdot t}{R_b R_c C} \right], \quad 0 \leq t \leq T \quad (2.2.2)$$

where T is the period.

$$I_0 = \frac{E_{cc} \cdot r_e (R_b/R_c/r_c) / R_c}{(R_e/r_e)(R_b/R_c/r_c) / R_b(R_c/r_c)} - \frac{E_{ee} \cdot R_b/R_c \cdot r_e (R_b/R_c/r_c) / R_b R_c}{(R_e/r_e)(R_b/R_c/r_c) / R_b(R_c/r_c)}$$

$$i_e = \frac{E_{cc} R_b - E_{ee} (R_b/R_c/r_c)}{(R_e/r_e)(R_b/R_c/r_c) / R_b(R_c/r_c)}, \quad t \leq 0 \quad (2.2.3)$$

$$i_c = \frac{R_b}{R_b/R_c} \cdot I_0 \exp. \left[\frac{-R_b/R_c \cdot t}{R_b R_c C} \right] / \frac{E_{cc}}{R_b/R_c}, \quad 0 \leq t \leq T \quad (2.2.4)$$

$$i_c = \frac{E_{cc}}{R_b/R_c/r_c} / \frac{R_b}{R_b/R_c/r_c} \cdot \frac{E_{cc} R_b - E_{ee} (R_b/R_c/r_c)}{(R_e/r_e)(R_b/R_c/r_c) / R_b(R_c/r_c)}, \quad t \leq 0 \quad (2.2.5)$$

The emitter current at the valley point may be obtained by equating the emitter input equations for the transition and saturation region, equations (2.1.10) and (2.1.12) respectively. The resultant expression, which yields the current at the cutoff point of the monostable circuit, is given below.

$$i_e = \frac{E_{cc}}{\alpha (R_b/R_c) - R_b} \quad (2.2.6)$$

If equations (2.2.6) and (2.2.2) are equated and the resultant is solved for t , an expression for T , the period is obtained as given below.

$$T = \frac{R_b R_c C}{R_b / R_c} \cdot \ln \left\{ \frac{I_o}{E_{cc}} \cdot [\alpha (R_b / R_c) - R_b] \right\} \quad (2.2.7)$$

The value of i_e given by equation (2.2.3) would be of the order of a few microamperes since the value of r_e in the cutoff region is of the order of one or two megohms. Hence the second term in equation (2.2.5) could be neglected since it is much smaller than the first term. This would yield the result

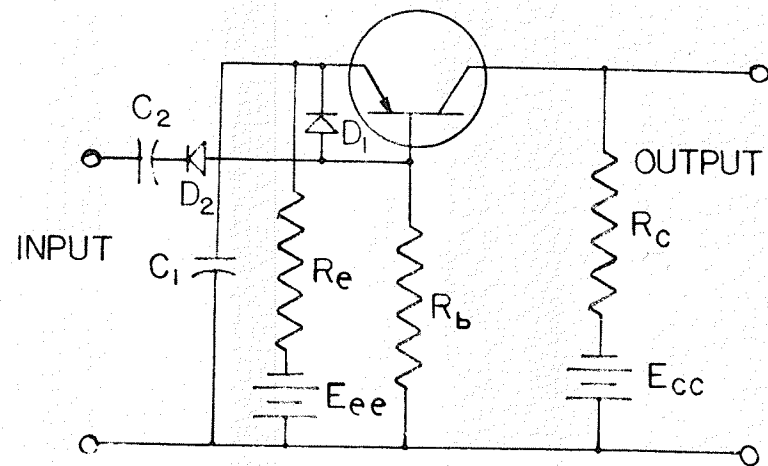
$$i_c = \frac{E_{cc}}{R_b / R_c / r_c} = I_{co}, \quad (2.2.8)$$

where I_{co} is defined as that value of collector current flowing in the circuit when the emitter current is zero.

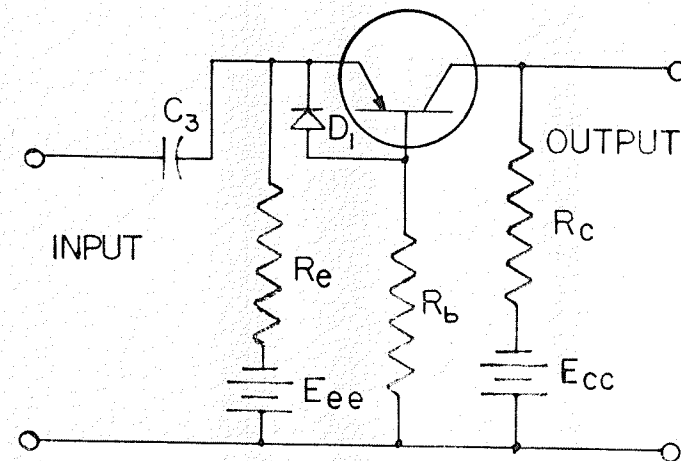
The expressions previously determined may be considerably simplified if the emitter load is removed. Since experimental evidence³ indicates that the peak point of the emitter input characteristic is located slightly to the right of the voltage axis, the circuit would still be monostable.

If the emitter load is removed, the equations of the monostable circuit take the following form.

$$i_e = \frac{E_{cc} r_c}{(R_b / R_c / r_c) R_c} \exp. \left(- \frac{R_b / R_c}{R_b R_c C} \cdot t \right), 0 \leq t \leq T \quad (2.2.9)$$



A. NEGATIVE INPUT



B. POSITIVE INPUT

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FIG. 8 A PRACTICAL MONOSTABLE CIRCUIT

sufficiently low impedance to allow the circuit to operate. Generator impedances⁴ of the order of ten thousand ohms and lower have been reported as acceptable for this type of circuit.

It is clear from the theory previously developed, that when the circuits of Fig. (8) have triggered from the saturation to the cutoff state, the condensers C_1 and C_3 must discharge through the internal emitter resistance r_e , in parallel with the load line resistance R_e , before the circuits are again ready to operate. Since r_e is of the order of a few megohms and since R_e could be of the order of ten thousand ohms or higher, the resultant high discharge time limits the maximum pulse repetition rate to which the circuits would respond. The recovery diodes D_1 in both circuits of Fig. (8) shunt the emitter-base and provide a low impedance discharge path for the capacitors, thereby allowing the circuits to respond to a considerably higher pulse repetition rate. Circuits employing recovery diodes have been found to have recovery times as low as a few microseconds in this investigation.

The output pulse amplitude and width of either circuit are independent of the input pulse amplitude and width subject to the following restrictions.

(1) If the input pulse width is greater than the output pulse width, the amplitude of the input pulse must not be so large

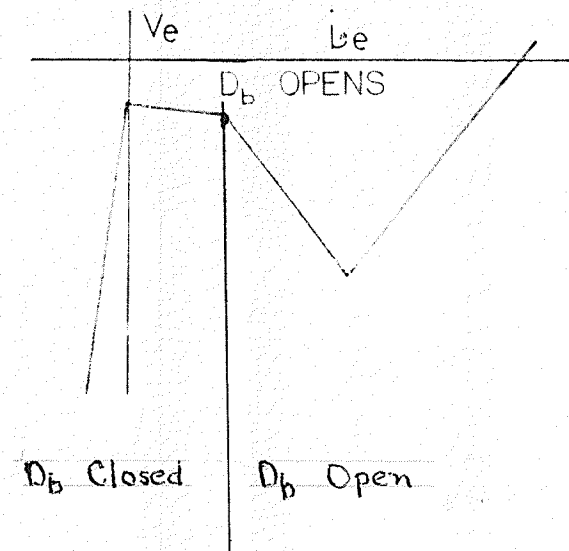
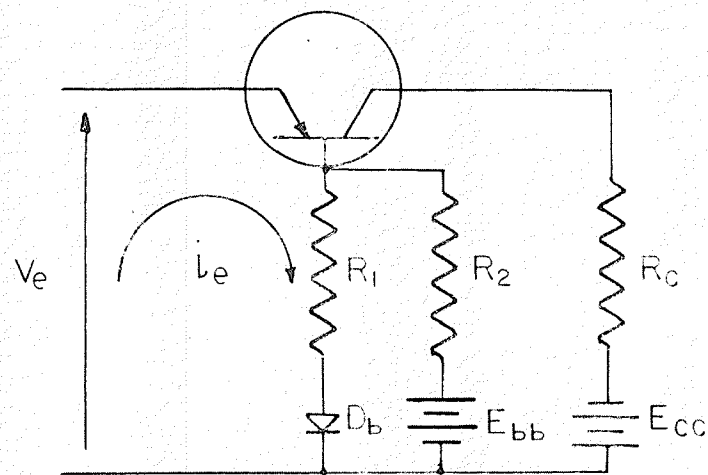
that it will exceed the voltage required to trigger the circuit immediately after it has switched from the saturation to the cutoff region. If the input pulse is not restricted in this manner, an increase in the output pulse width would result.

(2) If the amplitude of the input pulse is just sufficient to trigger the circuit, the width of the input pulse must be slightly less than the recovery time of the circuit. If the input pulse width is equal to or greater than the recovery time of the circuit, multiple output pulses will result from the initiation of a single input trigger pulse.

2.4 Stabilization of the Trigger Point

It has been found that transistor parameters tend to vary over a considerable range for a given type of transistor and that the parameters for a given transistor may vary widely because of ambient temperature changes, aging, etc. In particular, changes of the peak point of the emitter input characteristic would cause the circuit either to fail to trigger or to run freely. This effect would be more pronounced in a circuit designed to operate from a small input trigger source. On the other hand, variations in the valley point of the emitter input characteristic could cause variations in the output pulse width, however, it will be shown later that this will not affect the operation of the coincidence unit.

A basic circuit for stabilization of the trigger point^{5,6,7} employing a biased diode in the base is given in Fig. (9). In this circuit typical values of R_1 and R_2 are one and ten kilohms respectively. When the emitter current is small and positive, the base diode D_b is closed and the effective base resistance is the value of R_1 and R_2 in parallel. As the value of emitter current increases, the base current reverses by virtue of the current amplification properties of the transistor, the base diode opens and the effective base resistance is R_2 . This circuit is advantageous in that it offers a small value of base resistance at triggering, thereby minimizing the effect on triggering of variations in the collector resistance r_c , and a large value of base resistance after triggering, thereby yielding a pronounced negative resistance characteristic.



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FIG. 9 STABILIZED TRIGGER CIRCUIT

CHAPTER 3COINCIDENCE--ANTICOINCIDENCE CIRCUITS3.1 Basic Trigger Circuit

The basic trigger circuit given by Fig. (10) is the fundamental unit of the coincidence circuits and may be triggered by either positive or negative input sources. It has been previously shown that a low value of base resistance is desirable for purposes of stabilizing the trigger point of the circuit, and that a higher value of base resistance is desirable in order to attain a pronounced negative resistance characteristic. In the circuit of Fig. (10) the base resistance has been chosen to favor trigger stability since this factor is of major importance for good operation of coincidence circuits. The value of collector resistance R_c has been so chosen as to favor a pronounced negative resistance characteristic thereby compensating for the use of a low base resistance.

Since transistor characteristics may vary considerably from one unit to the next, the value of R_c must be specially selected by experiment for any given transistor. It has been found that most transistors (type 2N22) operate satisfactorily with a collector load of four thousand ohms[#]. However, in some cases it has been found that collector loads of eight thousand

[#] The above is a direct result of this investigation.

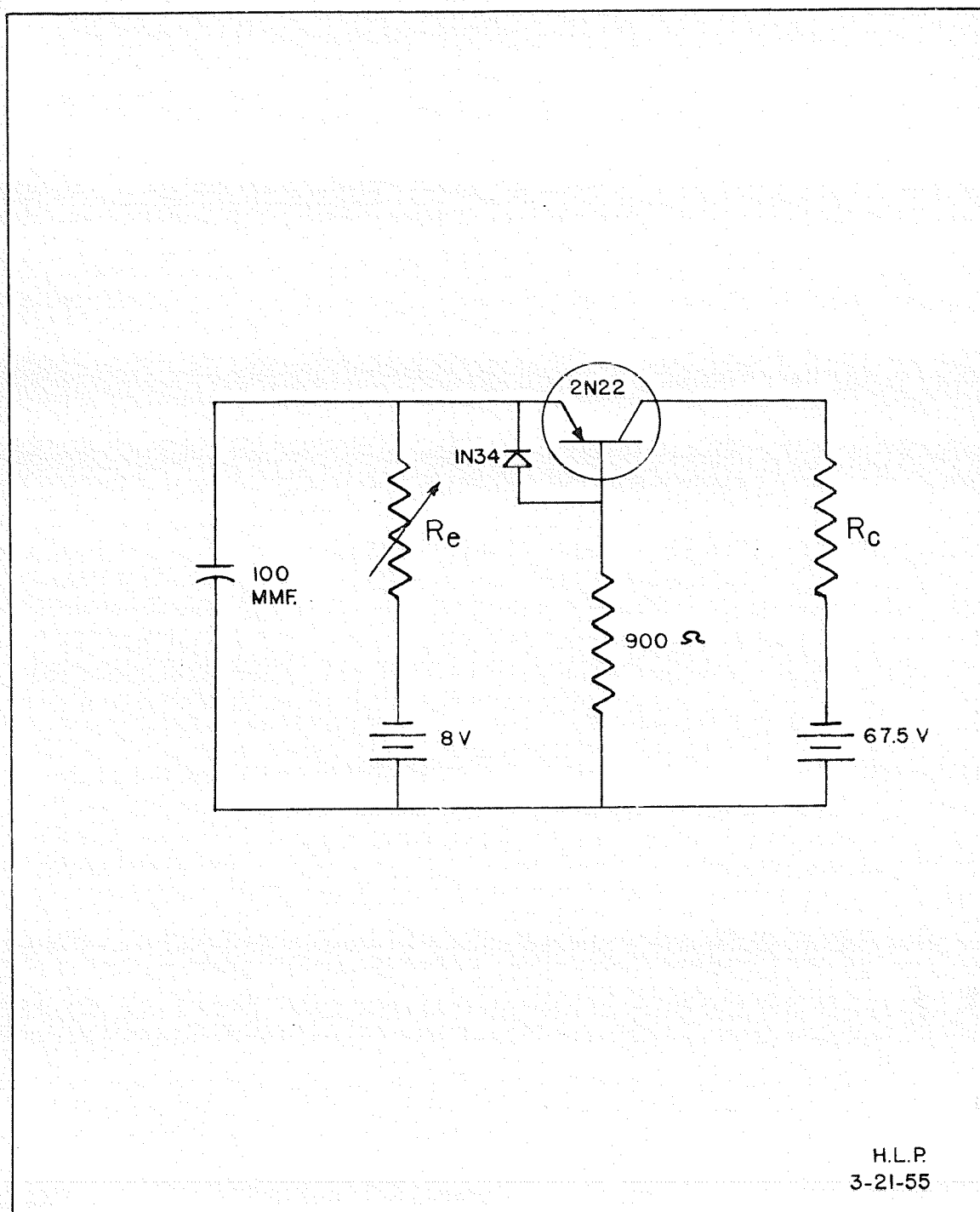


FIG. 10 FUNDAMENTAL COINCIDENCE CIRCUIT

ohms were necessary to operate the circuit satisfactorily.

In general, the above values may be considered as the upper and lower limits of collector resistance for satisfactory operation.

It was found necessary to set the trigger points experimentally on each transistor and for convenience this was achieved by varying the emitter loads while maintaining a fixed emitter bias of eight volts. The value of R_e required for a two volt input pulse to trigger the circuit is of the order of two thousand ohms.

As an illustration of the degree to which a properly selected collector load compensates for a low value of base resistance, typical values of components for the circuit of Fig. (10) have been assumed, calculations have been made for the required emitter loads and output current constants I_o , and the results are tabulated below.

TABLE I VARIATION OF I_o WITH BASE RESISTANCE

R_b	R_e	E_{ee}	I_o
900 ohms	2.1 Kohms	8.0 Volts	10.9 M.A.
10 Kohms	13.7 Kohms	25.0 Volts	9.3 M.A.
$r_e = 250$ ohms, $r_c = 20$ Kohms, $\alpha = 2.5$, $E_{cc} = 67.5$ Volts, $R_c = 4$ Kohms.			

The conclusions which may be drawn from the above results and from the equations previously developed[#] are:

- (1) For the circuit with the large base resistance, a pronounced negative resistance characteristic is obtained, and it is necessary to use an emitter bias of the order of twenty-five volts in order to cause the circuit to be monostable.
- (2) The circuit having a low base resistance has a less pronounced negative resistance characteristic and hence lower emitter bias may be satisfactorily used.
- (3) If the collector load R_C is properly chosen, the effect of a low base resistance on the negative resistance characteristic may be minimized. It is clear from Table I that if the circuit loads are properly chosen, the effect of a low base resistance on the output current is not appreciable.
- (4) The effect of lowering the base resistance in the trigger circuit is to produce an output pulse of slightly larger amplitude, having a sharper exponential drop with time and a smaller period.

3.2 Single Channel Circuit

A block and schematic diagram for one channel of the coincidence--anticoincidence unit is given in Fig. (11). The basic trigger circuit has been previously described and will be mentioned only briefly in this section.

[#] See Sections 2.1 and 2.2

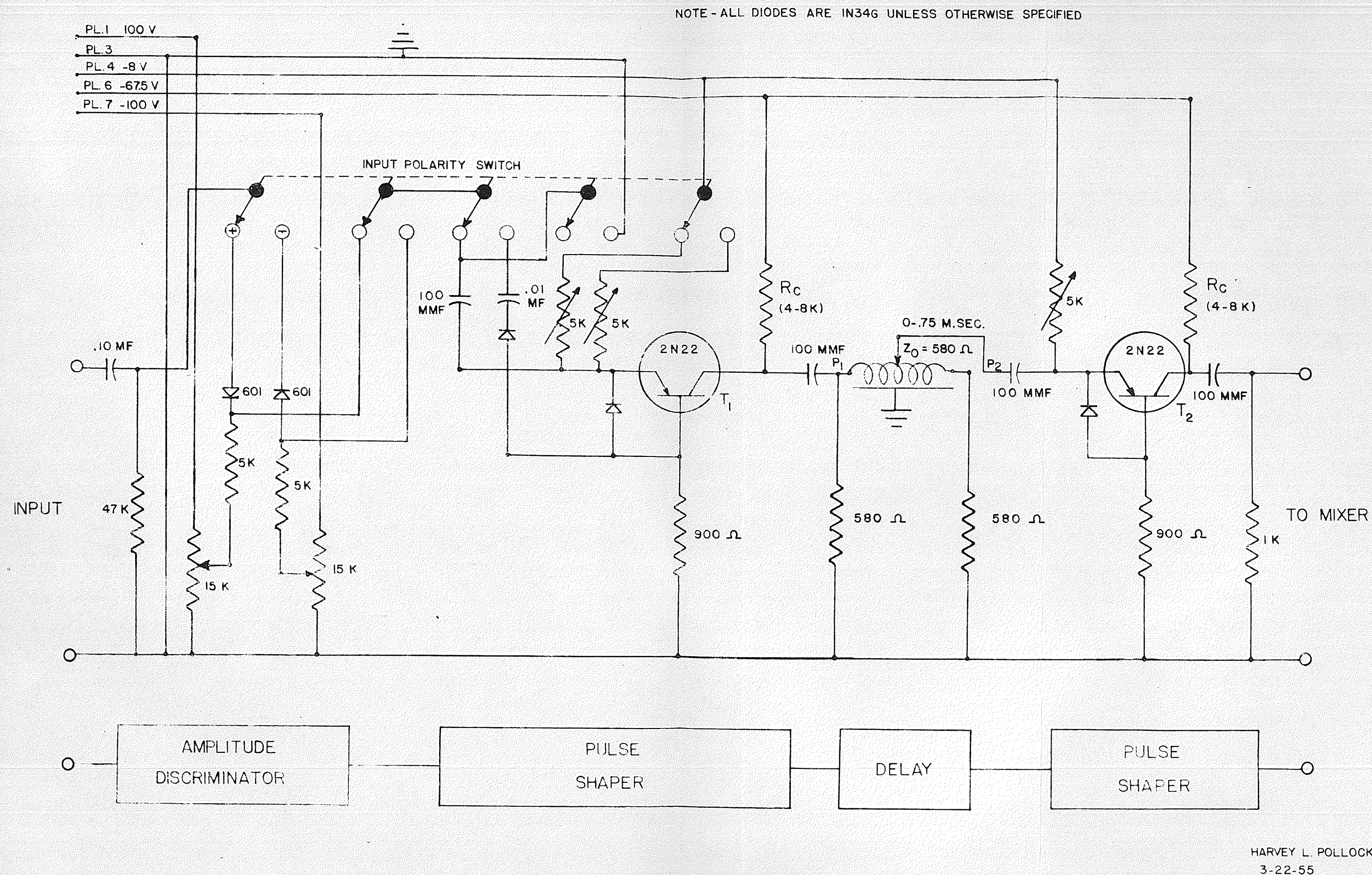


FIG. II INPUT CHANNEL FOR COINCIDENCE-ANTICOINCIDENCE COUNTER

The voltages are supplied from a specially constructed regulated supply described later in this report. The channel is provided with an input switch for positive and negative sources and it is desirable that the input sources be of low impedances (of the order of one thousand ohms or less) for best operation of the amplitude discriminator. Independent emitter loads are provided for the positive and negative inputs and are adjusted so that for either input, the circuit will trigger on two volts.

The amplitude discriminators consist of simple diode clipping circuits employing silicon crystal diodes. Variable clipping levels are obtained from the fifteen kilohm potentiometers. In order to ensure accurate direct readings of the discriminators, the potentiometers in the clipping circuits are ten-turn Helipot with vernier dials. Two of the three channels (Channels #1 and #3) are provided with continuously variable delay lines,[#] 0-0.75 microseconds, characteristic impedance 580 ohms. In the third channel (Channel #2) the delay line is replaced by a 1000 ohm resistor, the points P_1 and P_2 are connected to one end of the resistor and the other end of the resistor is connected to ground.

Upon inspection of the block diagram it might at first appear that the use of two pulse shaping circuits in one channel is unnecessary. The transistor T_1 is adjusted to

[#] Advance Electronics, Type 507 Delay Line

trigger on sources of two volts or higher and it is necessary that there be no distortion of the input pulse feeding the first trigger circuit in order to maintain a high degree of accuracy on the direct reading amplitude discriminator. The delay line must therefore be inserted after the first trigger circuit T_1 . The small distortion produced in the delay line is removed by the second pulse shaper T_2 before being passed into the mixing circuit. It should also be noted that if the input pulse is of sufficiently high amplitude and width, small distortions of the output pulse from the trigger circuit T_1 would result. It is necessary to remove these distortions by means of a second trigger circuit, T_2 , in order to ensure the lowest possible resolving time in the mixer. It is clear that the two-transistor channel design will meet the specifications[#] for the coincidence unit as outlined early in this report whereas there is some doubt about a single transistor channel meeting the first of these specifications.

3.3 Coincidence Mixing Circuit

The block^{diagram} and schematic circuit for the coincidence mixer are given by Fig. (12). Pulses from the channels in coincidence are fed to an adding circuit formed by paralleling the one thousand ohm resistors terminating each channel, and thence to a trigger circuit. The pulse shaper is adjusted so that

[#] See Section 1.3

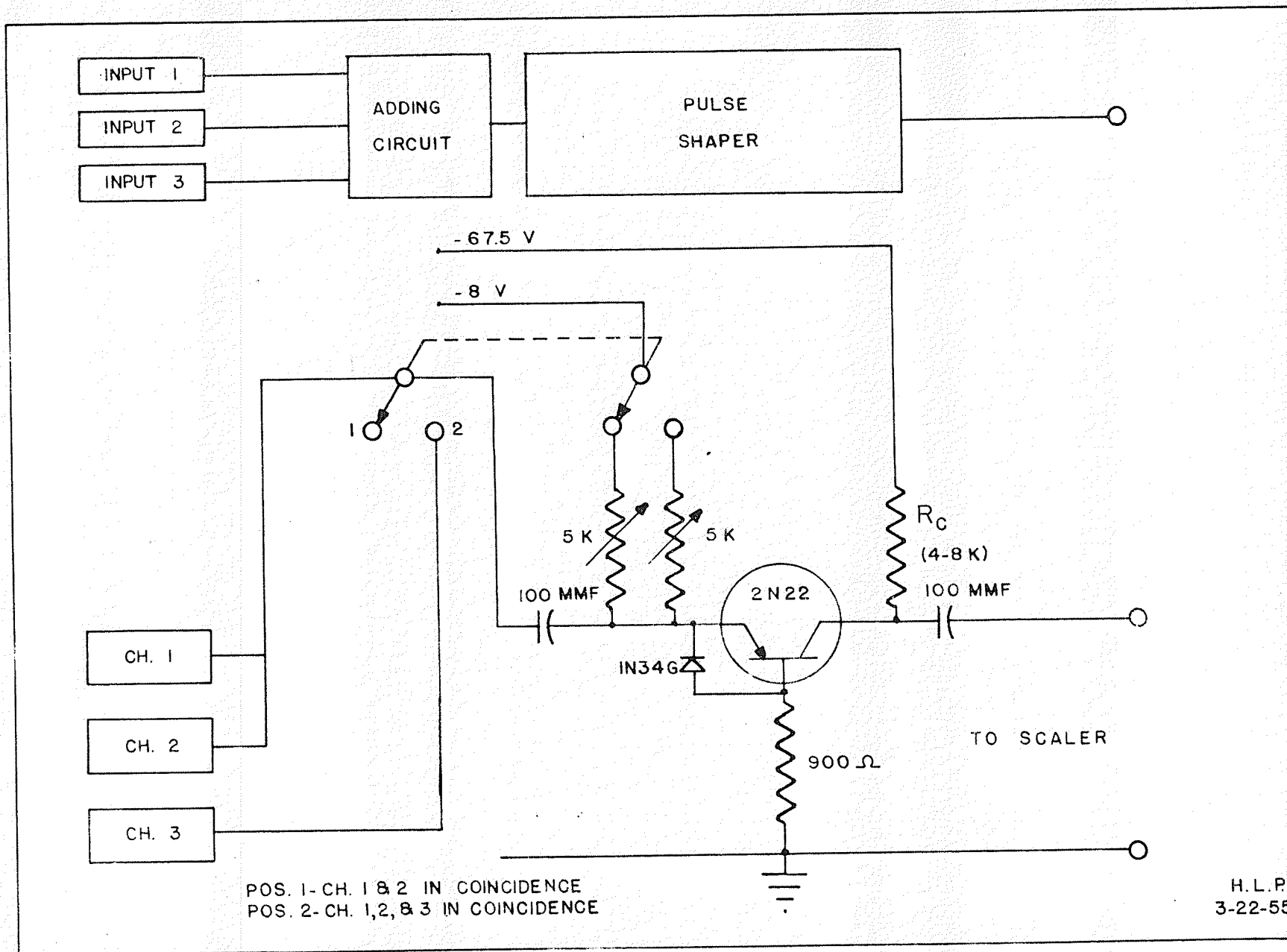


FIG. 12 COINCIDENCE MIXING CIRCUIT

it will trigger only when the output voltage of the adding circuit is close to the maximum value obtained when the pulses from the particular channels concerned are in perfect coincidence. Although the voltage required to trigger the pulse shaper may be adjusted to a value very close to the maximum output of the adding circuit, a small amount of tolerance has been allowed in setting this trigger level to compensate for possible shifting of the trigger point due to aging, variations in temperature, etc. It should be noted that the resolving time of the circuit depends on the voltage required to trigger the pulse shaper and hence may easily be varied.

The principle of operation of the adding circuit, given by Fig. (13), is as follows. If S_1 is closed, the voltage across R will be,

$$E_{R1} = \frac{E}{R_s + R} \cdot R \quad (3.3.1)$$

If S_1 and S_2 are closed, the voltage across R becomes,

$$E_{R2} = \frac{E}{R_s/2 + R} \cdot R \quad (3.3.2)$$

If S_1 , S_2 , and S_3 are closed, the voltage across R becomes,

$$E_{R3} = \frac{E}{R_s/3 + R} \cdot R \quad (3.3.3)$$

If the value of R is so chosen that R_s is much larger than $3R$, the preceding equations may be written as,

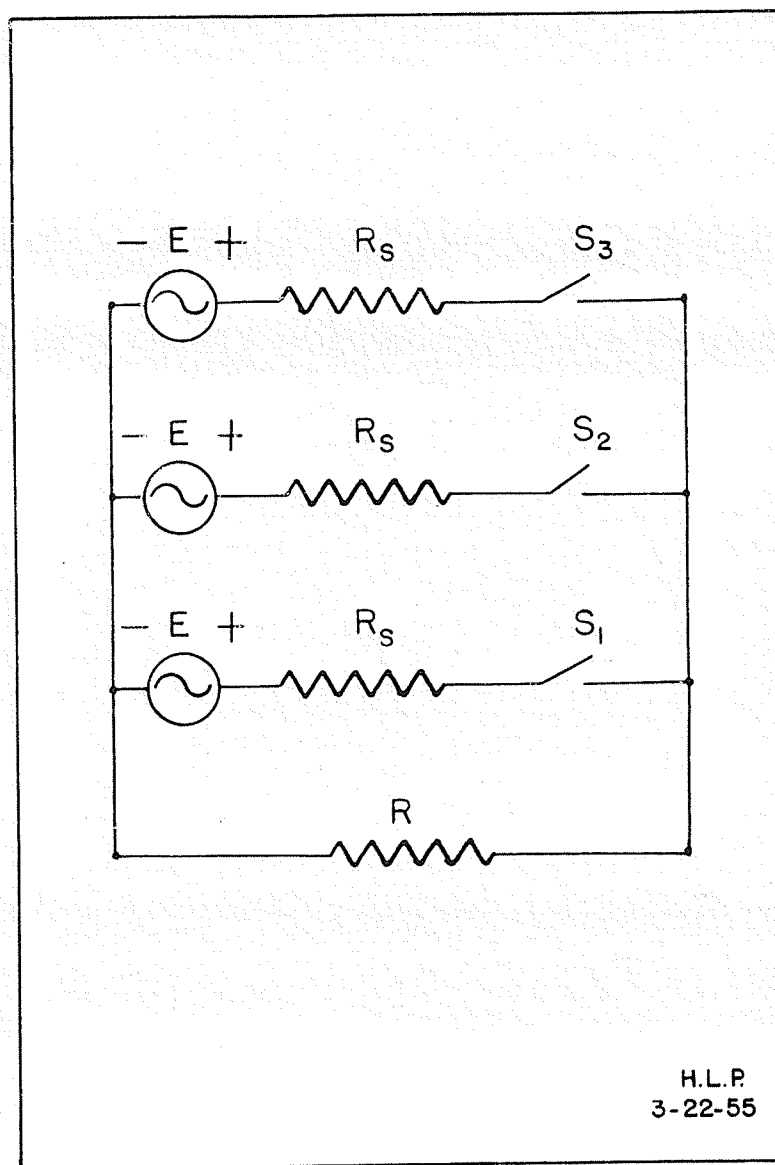


FIG. 13 ADDING CIRCUIT

$$E_{R1} = \frac{E}{R_s} \cdot R \quad (3.3.4)$$

$$E_{R2} = \frac{2E}{R_s} \cdot R \quad (3.3.5)$$

$$E_{R3} = \frac{3E}{R_s} \cdot R \quad (3.3.6)$$

It is clear from the above that if R_s is much larger than $3R$, the circuit of Fig. (13) will operate as an adding circuit. The adding circuit of Fig. (12) is essentially the same as the circuit considered above except that the load resistor R is effectively 500 ohms for two channel coincidence and 333 ohms for three channel coincidence. The principle of coincidence mixing can be extended by appropriate adjustment of the trigger point of the pulse shaper to register simultaneous inputs from any number of channels, in theory.

3.4 Anticoincidence Mixing Circuit

The block and schematic diagrams for the anticoincidence mixing circuit are given by Fig. (14). The input and anti-coincidence pulses from the channels are both positive. If both pulses are applied to the mixer simultaneously the positive anticoincidence pulse applied to the base of the trigger circuit will prevent triggering. The load line R_o may be adjusted to obtain the desired degree of resolving time in the mixer, the lower the input voltage required to

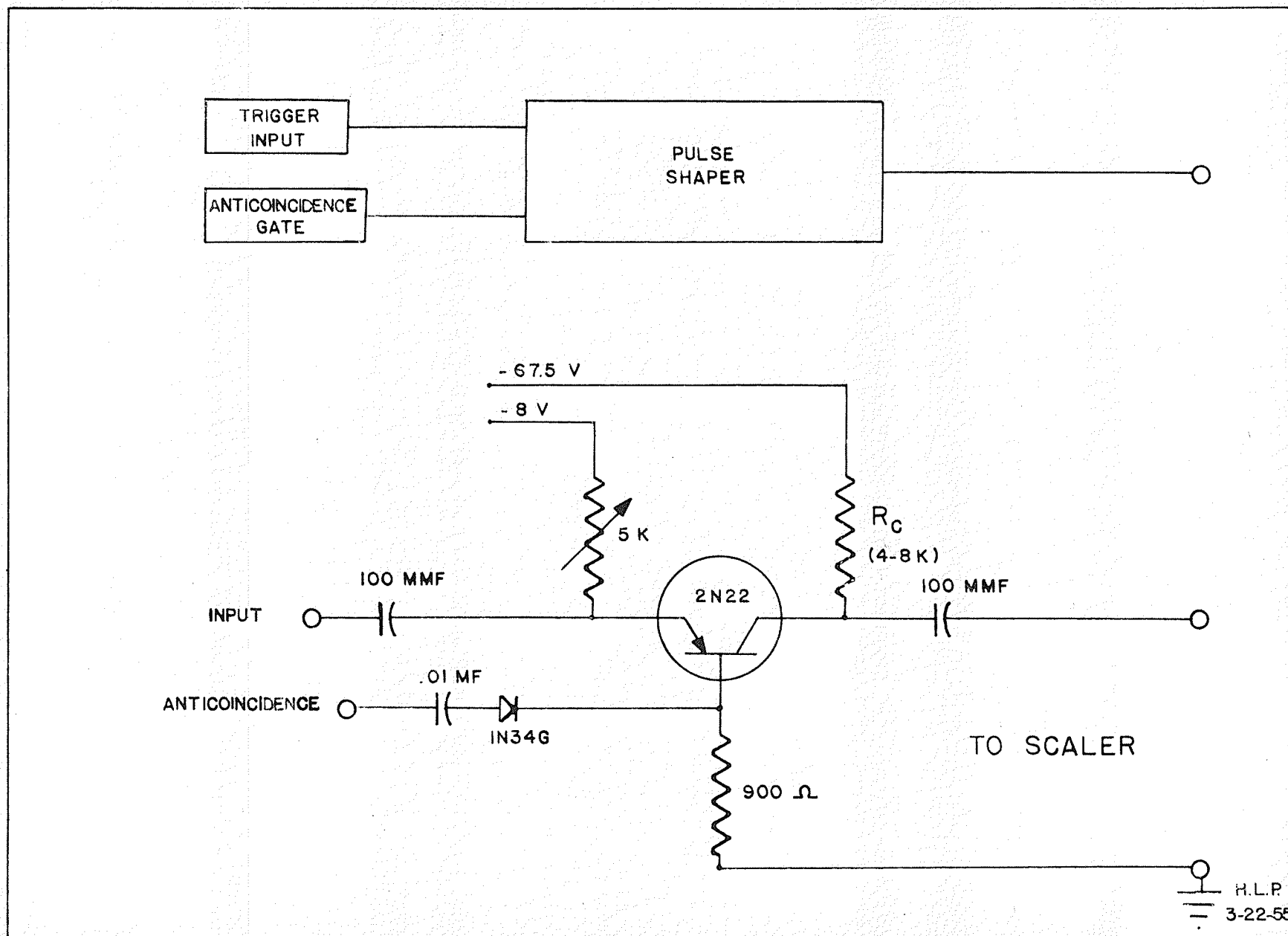


FIG. 14 ANTICOINCIDENCE MIXING CIRCUIT

trigger the circuit, the lower will be the resolving time. It should be noted that it is necessary to remove the recovery diode shunting the emitter-base in order that positive pulses applied to the base of the mixer do not trigger the circuit. It would appear that an increase in the recovery~~time~~ of the mixing circuit would result from the removal of the emitter-base diode, However, by suitable choice of the emitter bias, (8 volts for the 2N22 transistors used in this investigation) the required emitter load may be made sufficiently small to provide a low discharge path for the feedback capacitor, thereby allowing the circuit to maintain a short recovery time. The anticoincidence mixing circuit is very versatile in that it can be made to respond to different combinations of coincidence-anticoincidence pulses with a low resolving time by appropriate adjustment of the emitter load.

3.5 Three Channel Coincidence-Anticoincidence Unit

The results of this investigation have led to the design of a three channel coincidence-anticoincidence unit. It is of interest to note, however, that a unit employing many channels may be easily designed on the basis of results obtained in this investigation in which only minor modifications of the basic circuitry would be required.

This value was selected by experiment.

A regulated, low impedance, four-section voltage supply has been designed for the unit. For portable use, the required voltages could be supplied by dry batteries. A circuit diagram of the supply is given in Fig. (15). It is the well known series regulator type, design of which may be obtained from any of the standard reference sources⁹. It will be sufficient here to note that the supply has been designed to operate only on the loads supplied by the coincidence-anticoincidence unit viz, 5 kilohms for the plus and minus 100 volt sections, 2-4 kilohms for the minus 67.5 volt section, 300-1000 ohms for the minus 8 volt section. The reference for all voltages and loads mentioned above is ground potential.

It might also be noted that the influence of the external loads upon the coupling between sections of the supply must be given due consideration in the design. The regulation of the supply was found to be approximately 0.13%--i.e. a change of 100 volts in the plate supply causes a change in the output voltage of 0.13 volts. The minimum filament voltage which would permit regulation was found to be 5.4 volts.

The internal impedance of the series regulator type voltage supply varies slightly with the applied load, thereby causing a small variation of the output voltage. For anticoincidence operation, the diode shunting the emitter-base in the mixing unit is removed thereby causing

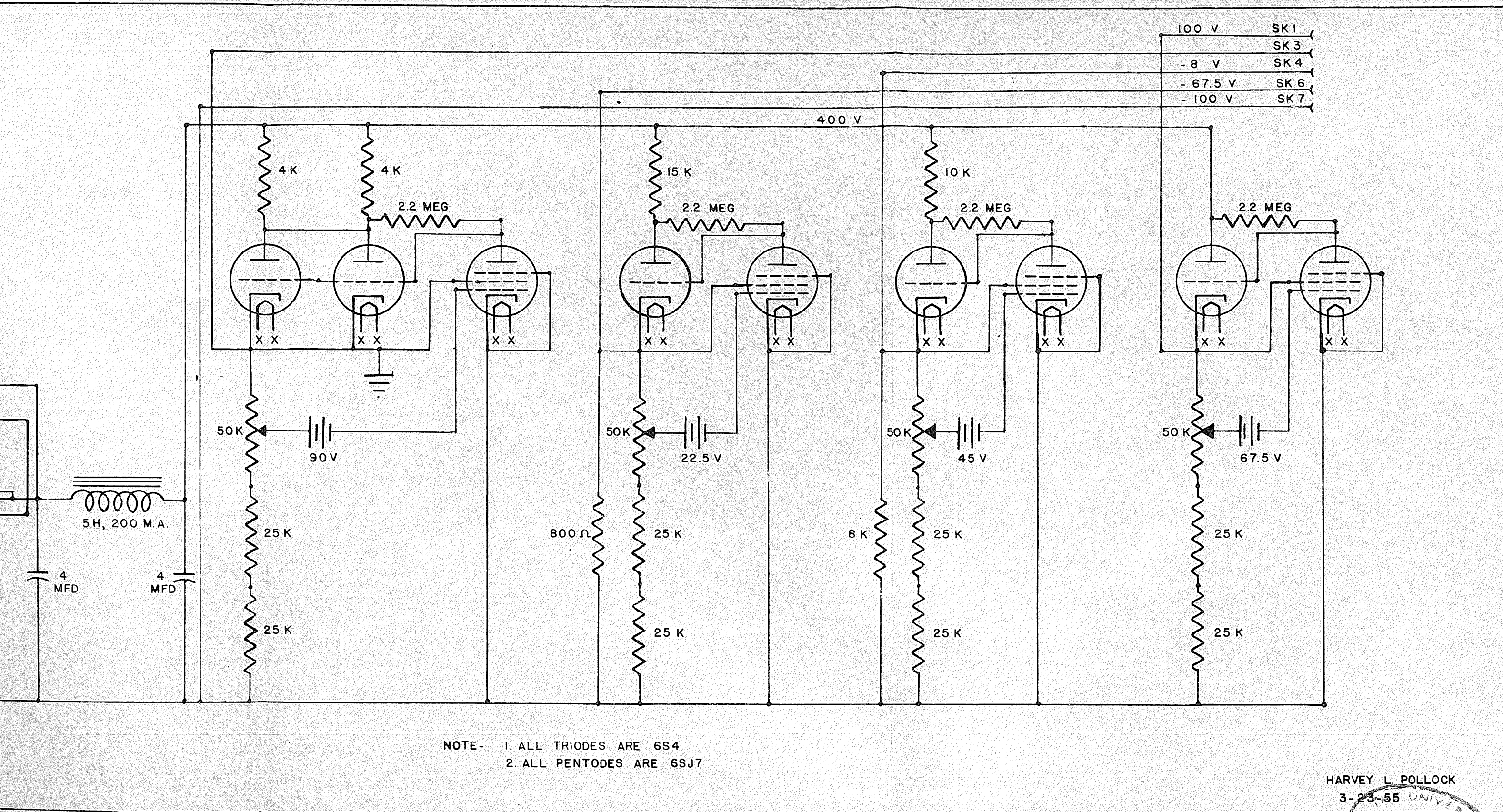
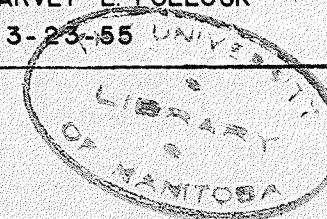
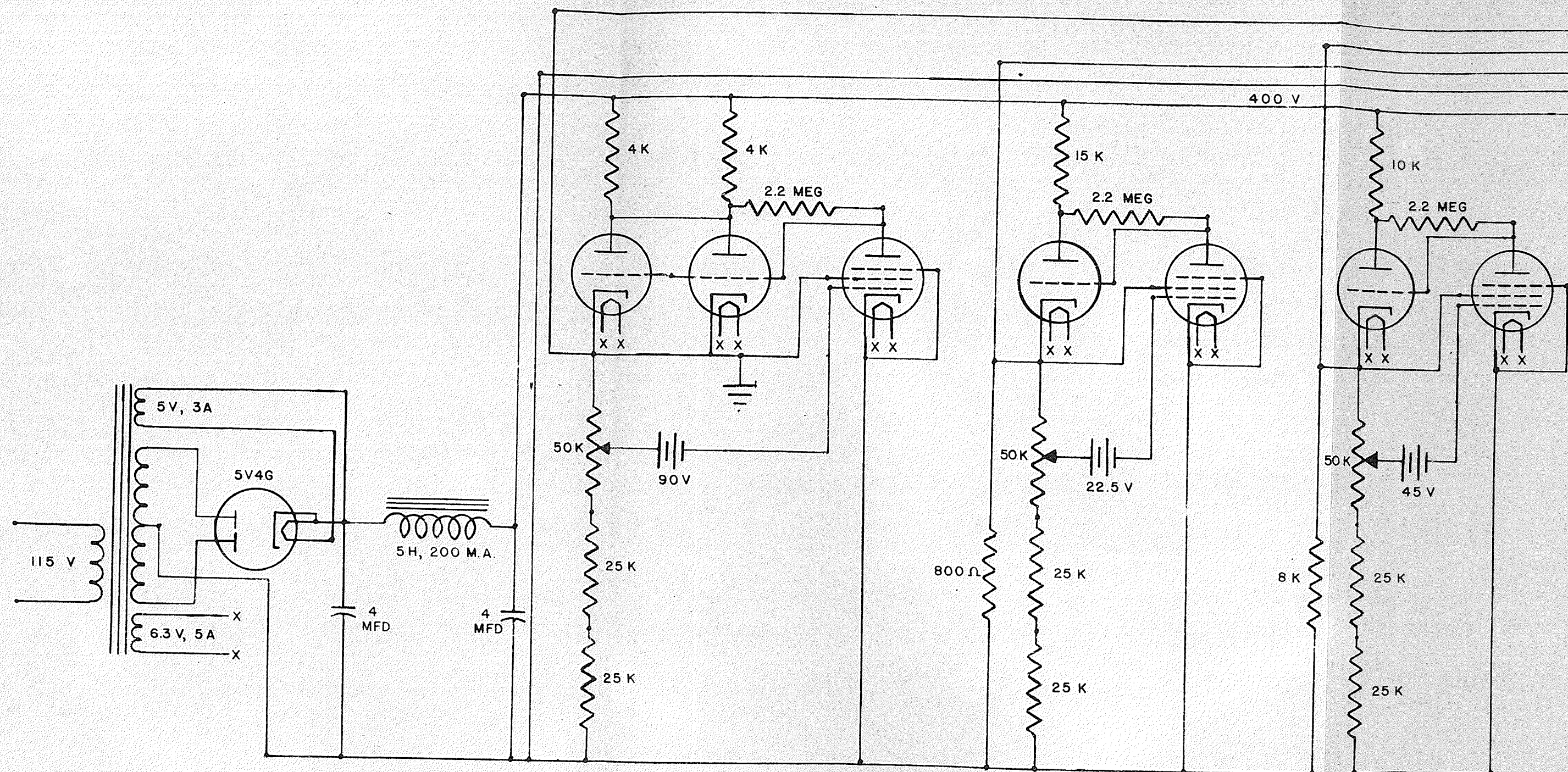


FIG. 15 REGULATED VOLTAGE SUPPLY

HARVEY L. POLLOCK
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NOTE- 1. ALL TRIODES ARE 6S4
2. ALL PENTODES ARE 6SJ7

FIG. 15 REGULATED VOLTAGE SUPPLY

the minus 8 volt line to work into a larger external load resistance. This would ordinarily require that a small adjustment (approximately 0.2 volts) be made on the minus 8 volt line when the unit is switched from coincidence to anti-coincidence operation and vice versa. The necessity for adjustment has been eliminated by switching in an appropriate resistance in parallel with the minus 8 volt output when the unit is placed in anticoincidence operation.

The complete three channel coincidence-anticoincidence circuit is given by Fig. (17). Channels (1) and (3) are provided with continuously variable delay lines (0-0.75 microseconds) and the unit may be operated in any one of the following arrangements.

- (1) Channels (1) and (3) in coincidence.
- (2) Channels (1), (2), and (3) in coincidence.
- (3) Channels (1) and (3) in coincidence and channel (2) in anticoincidence with this output.
- (4) Channel (3) in anticoincidence with channel (1).
- (5) Channel (2) or (3) in anticoincidence with channel (1).

The numbering of the above corresponds to the switch positions on the mixing unit, Switch M.

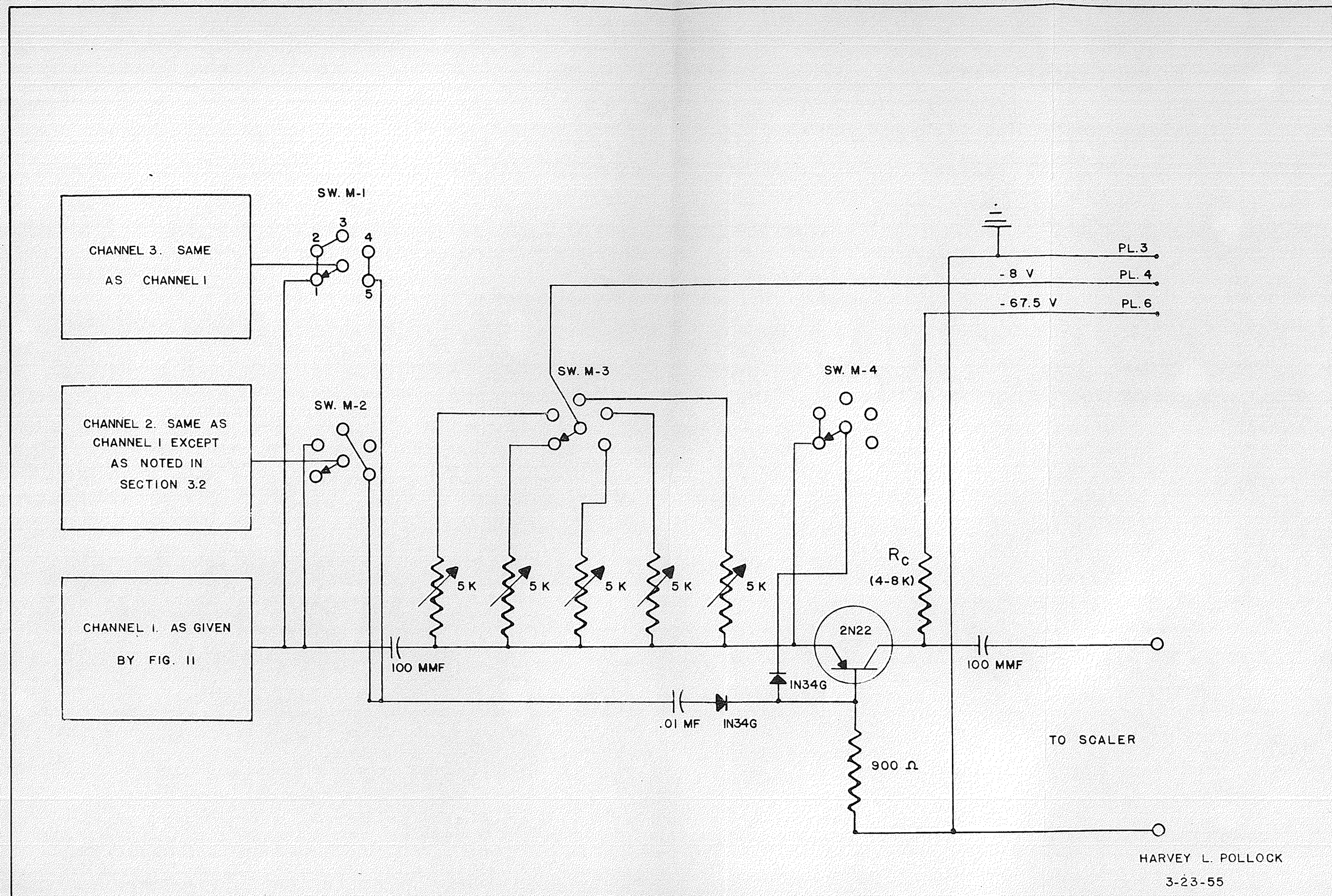


FIG. 16 COINCIDENCE-ANTICOINCIDENCE COUNTER

CHAPTER 4

PROPERTIES OF THE COINCIDENCE--ANTICOINCIDENCE UNIT

4.1 Single Channel Properties

The amplitude discriminator was tested using a Tektronix Oscilloscope Type 511 AD, to measure the input and output pulse amplitudes and a high impedance voltmeter to measure the biases applied to the diode. The discrepancy between the actual output pulse amplitude and that predicted on the basis of the applied bias was found to be less than 5%. The discriminator circuit employs as the clipping element a Texas Instruments Type 601 silicon diode having a back resistance of greater than 10 megohms and a forward resistance of approximately 150 ohms. The leakage across the diode due to shunt capacitance was found to be 0.75 volts for an applied pulse of 90 volts peak amplitude and one microsecond width. Calculations of this leakage based on the manufacturer's specification of a shunt capacitance of 2.5 micromicrofarads are in close agreement with the above. The manufacturer also specifies the recovery time of the diode as 2 microseconds which satisfactorily meets the circuit requirements.

The bias applied to the discriminator is controlled by a ten-turn Helipot, guaranteed linear to within 0.5% by the manufacturer, employing a vernier dial and operated in conjunction with the regulated voltage supply, thus

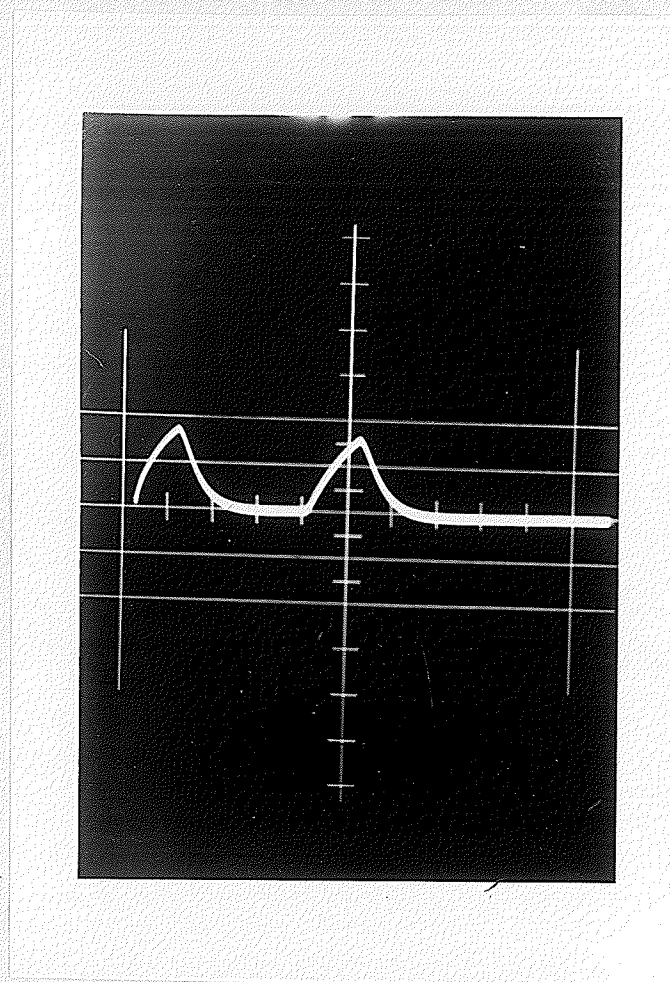
enabling the operator to measure accurately the amount of amplitude discrimination.

Calculations based on the previously developed theory of trigger circuits indicate that a variation in collector resistance r_c of 100% will cause a variation in the voltage required to trigger the circuit of 1 volt. This would indicate that the unit should be highly stable if due cognizance of the above is taken in setting the trigger levels of all transistors in the circuit.

The characteristics of the pulses in a single channel are illustrated by the photographs in Figs. (17), (18), (19), and (20). The conclusions which may be drawn from these photographs are as follows.

- (1) The shape and size of the output pulse are independent of the shape and size of the input pulse. #
- (2) The recovery time of the channel is no greater than four microseconds.
- (3) Typical rise times for the output of the trigger circuits are approximately 0.03 microseconds.
- (4) The amplitude and width of the output pulse from a single channel are approximately 35 volts and 1.5 microseconds.
- (5) A small amount of distortion is produced by the delay line; however, this has no effect on the output pulse.

This conclusion is based on the results of experimental evidence.



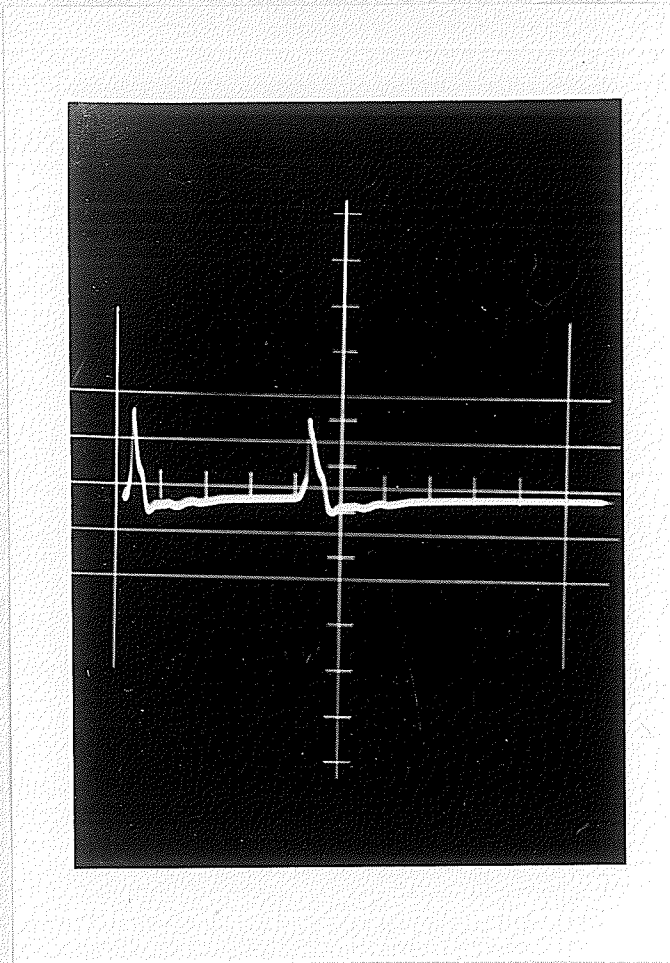
Scale: 1 Volt/div.

1 microsecond/div.

FIG. 17 DETECTOR INPUT TO CHANNEL

Note: 1 horizontal division = 1 cm.

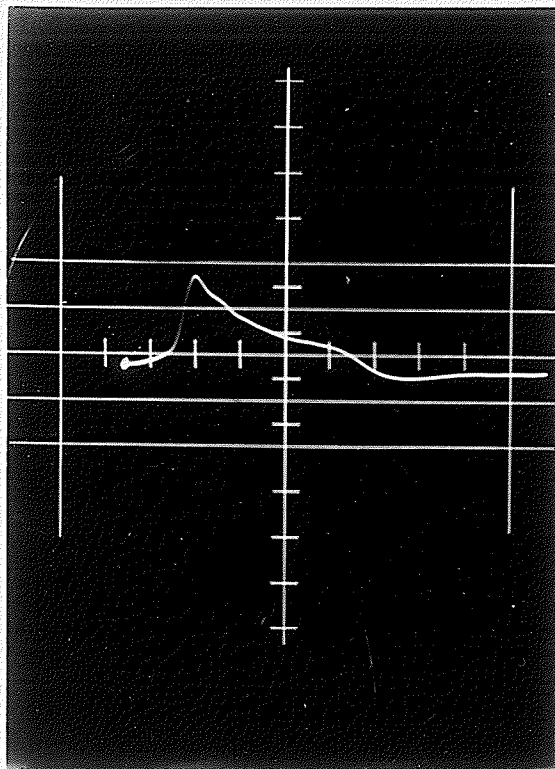
1 vertical division = 0.5 cms.



Scale: 2 Volts/div.

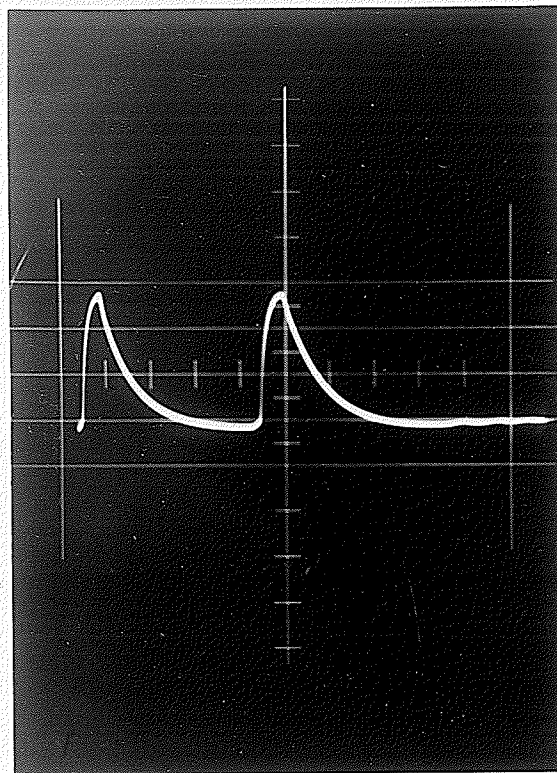
1 microsecond/div.

FIG. 18 OUTPUT FROM FIRST PULSE SHAPER OF CHANNEL



Scale: 0.1 microsecond/div

FIG. 19 RISE TIME OF TYPICAL PULSE SHAPER OUTPUT



Scale: 5.5 Volts/div.

1 microsecond/div.

FIG. 20 OUTPUT FROM SECOND PULSE SHAPER OF CHANNEL

4.2 Properties of the Mixing Stages

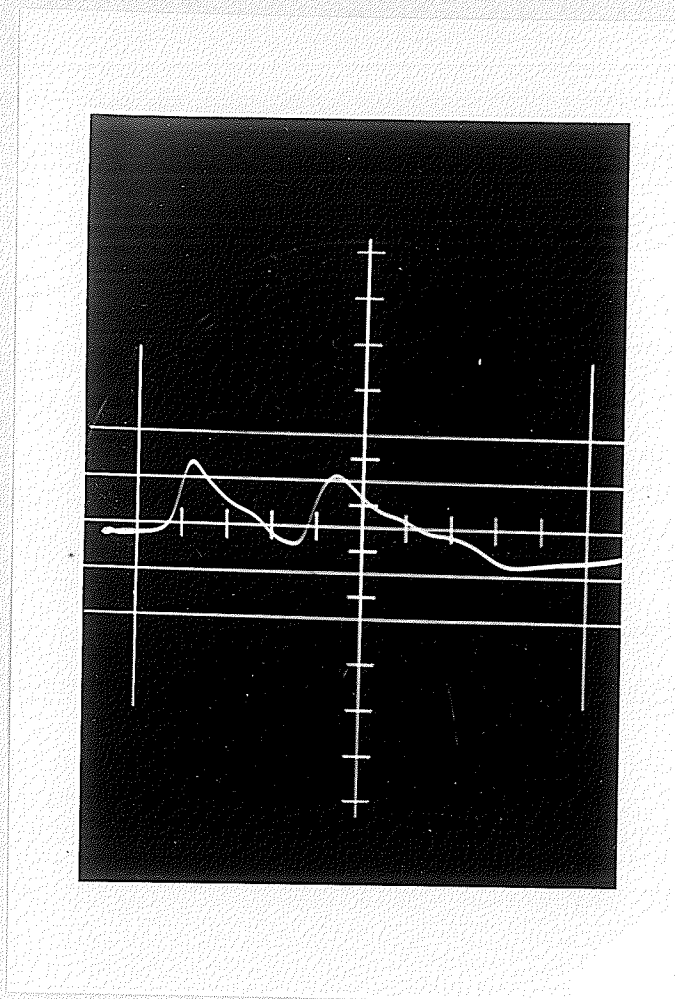
The properties of both coincidence and anticoincidence mixing have been evaluated on the basis of results obtained for two channel operation. It is clear, however, that the same results may be expected for a multi channel mixer (and especially for a three channel mixer) since these employ exactly the same circuitry for both coincidence and anticoincidence mixing with the one exception that the triggering levels of the mixing units would be different.

The method used in determining the resolving time of the mixer is as follows. Identical input pulses are fed into two channels and a fixed amount of delay is introduced in one of the channels by means of the variable delay line. The delay on the other channel is then varied and the variation in delay which yields, or does not yield, an output pulse from the mixer is noted, depending on whether resolving times for coincidence or anticoincidence are required. The resolving time of the mixer is then one half the observed variation in delay.

The resolving times obtained using the above method were 0.023 microseconds for the coincidence mixer and 0.025 microseconds for the anticoincidence mixer. The error in these measurements was estimated as ± 0.003 microseconds.

The properties of the coincidence mixer are illustrated by the photographs in Figs. (21) and (22) which show the input to the mixer. It is clear that the adding circuit is operating fairly linearly, thereby allowing the trigger level to be critically adjusted to operate the circuit only when there is almost perfect coincidence between the two input pulses. This fact largely accounts for the extremely low resolving time of the mixer.

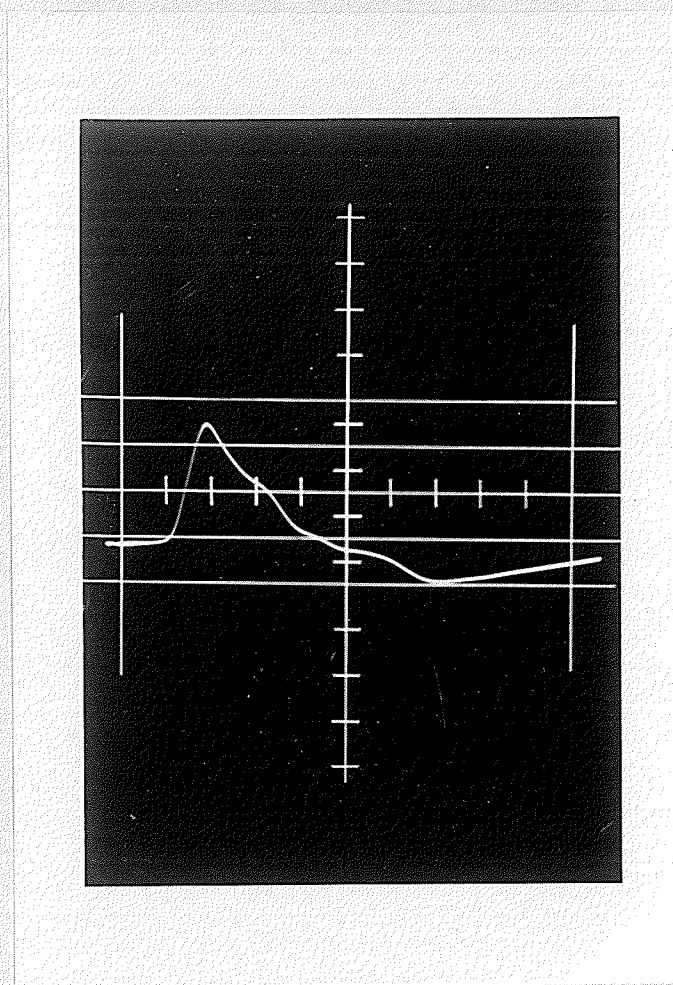
The properties of the anticoincidence mixer are illustrated by the photographs in Figs. (23) and (24) of the base of the mixer. The positive anticoincidence pulse is much greater than the positive pulse produced at the base by the emitter input just before the circuit triggers. The true magnitude of the anticoincidence pulse is not indicated on the photograph because of blocking in the oscilloscope amplifiers. The sudden negative drop in voltage of the smaller of the two pulses in Fig. (23) indicates that the circuit has triggered causing a sudden reversal in base current. It is of interest to note that the fall time of this pulse is a measure of the rise time of the output pulse. In Fig. (24), it is clear that the anticoincidence pulse applied at the base in phase with the trigger pulse applied at the emitter prevents the circuit from triggering by back-biasing the emitter-base diode. Since the anticoincidence pulse applied to the base is much



Scale: 2.5 Volts/div.

0.1 microsecond/div.

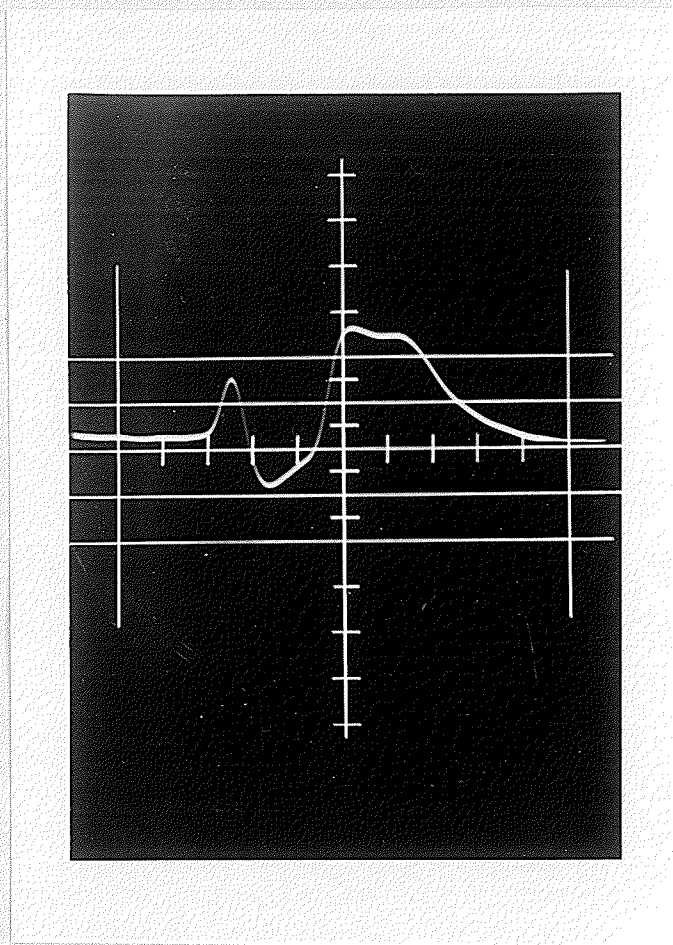
FIG. 21 DELAYED INPUT TO TWO CHANNEL COINCIDENCE MIXER



Scale: 2.5 Volts/div.

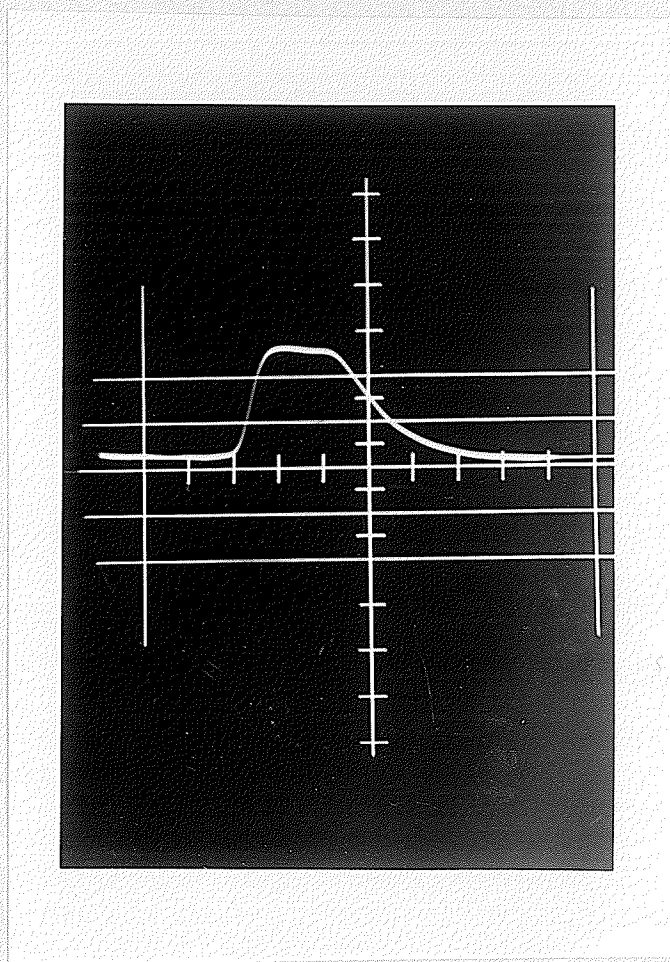
0.1 microsecond/div.

FIG. 22 COINCIDENCE INPUT TO TWO CHANNEL COINCIDENCE MIXER



Scale: 0.1 microsecond/div.

FIG. 23 DELAYED INPUT TO TWO CHANNEL ANTICOINCIDENCE MIXER



Scale: 0.1 microsecond/div.

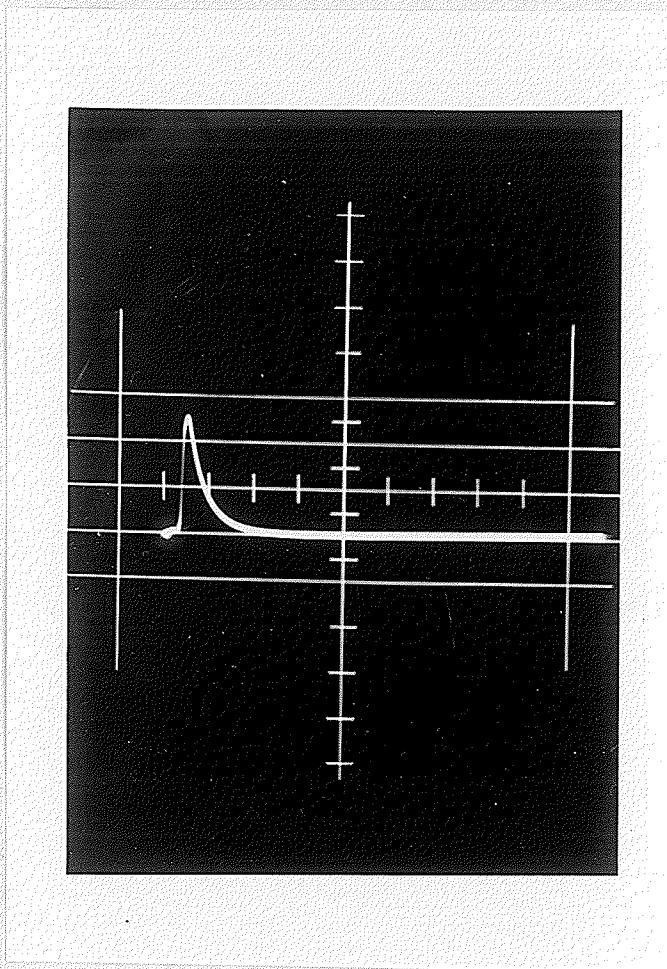
FIG. 24 COINCIDENCE INPUT TO TWO CHANNEL ANTICOINCIDENCE MIXER

greater than the pulse appearing at the base due to the input pulse applied to the emitter, the anticoincidence circuit is inherently capable of producing much lower resolving times than the coincidence mixer. The smaller the input voltage required to trigger the circuit, the greater will be the resolving time of the mixer.

The output pulse produced by the mixer for either coincidence or anticoincidence operation is shown in the photograph in Fig. (25). The amplitude and width of the output pulse to the scaler are 27 volts and 1 microsecond respectively.

4.3 Evaluation of the Coincidence-Anticoincidence Unit

The coincidence-anticoincidence unit can best be evaluated by comparison to the Coincidence Unit, type 1036A, designed by the Atomic Energy Research Establishment, Harwell. The latter is considered as a useful instrument for detectors having rise times in the region of 10^{-6} to 10^{-7} seconds. A table of comparison is given below. It should be noted in this table that the minus 100 volt supply required for the transistor unit provides the variable amplitude discrimination for negative input pulses, a feature which is not available on the 1036A Coincidence Unit.



Scale: 5 Volts/div.

1 microsecond/div.

FIG. 25 OUTPUT FROM COINCIDENCE-ANTICOINCIDENCE MIXER

TABLE II PERFORMANCE OF THE COINCIDENCE--ANTICOINCIDENCE UNIT

Specification	Transistorized Unit	Type 1036A Unit ⁸
Amplitude Disc.	Cont. variable 2-102 volts for pos. or neg. input	Cont. variable 2-50 volts for pos. input. 2 volts fixed for neg. input
Typical Rise Time	0.03 microseconds	-----
Recovery Time	4 microseconds, max.	5 microseconds, min.
Coincidence Resolving Time	0.023 microseconds	0.1 microseconds
Anticoincidence Resolving Time	0.025 microseconds	0.1 microseconds
No. of Channels	3	3
No. of different operations performed	5	5
No. of tubes or transistors/channel	2 transistors	6 tubes
No. of Mixers	1	2
No. of tubes or transistors for mixing	1 transistor	11 tubes
Voltage Supplies Required	+100V, -100V, -8V, -67.5V.	+285 V, +95V.

Abbreviations: cont.--continuously; disc.--discriminator;
pos.--positive; neg.--negative.

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CONCLUSION

A three channel, transistorized, coincidence-anticoincidence unit has been designed having resolving times of approximately 0.02 microseconds and a rise time of operation of approximately 0.03 microseconds. The circuitry has been considerably simplified in comparison with vacuum tube circuits performing similar functions. The relatively fast rise times and the overall reduction in size, cost, and complexity of the transistorized unit suggest that further study of the applications of transistor circuitry to Nuclear Physics Instrumentation be made.

It is suggested that the problem of transistorizing such instruments as the differential discriminator and the scintillation counter be investigated. On the basis of the results of this investigation, it would appear that an overall improvement in the above instruments might be anticipated.