AN AUTOMATIC ANALOG TO DIGITAL CONVERTER FOR GRAPHICAL RECORDS

THESIS

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by

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ERRATA

PAGE	LINE	
8	16	This factor necessitated the design and construction...
39	22	programming
63	10	The pin holes in the scanning heads are ...

ABSTRACT

This paper describes the logical and electronic design of an eight channel graph-reader or analog to digital converter. The purpose of the apparatus is to automatically convert a graphical record of an eight-channel Electroencephalograph into a binary coded punched paper tape suitable for analysis by a digital computer.

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AN AUTOMATIC ANALOG TO DIGITAL CONVERTER FOR GRAPHICAL RECORDS

CHAPTER I

INTRODUCTION

Since 1925 when Berger[1] discovered that the electrical activity of the brain - the Electroencephalograph (EEG) could be recorded at the surface of the scalp, it has been used for a test of brain function. The "reading" or interpreting of these noise-like waveforms (Figure 1) is done by a trained analyst who views each record and measures the amplitude and frequency of the predominant waveforms. His interpretation is based on his individual experience. This method is slow, cumbersome, and of limited usefulness, especially in borderline cases. In an effort to put the "reading" of EEG records on a more scientific basis, many investigators are attempting to determine some characteristics of the EEG waveforms and empirically correlate these characteristics with present clinical knowledge. One method used to obtain these characteristics is to perform various mathematical operations upon the waveforms. Examples of such operations are, inter alia, finding the Fourier components of the waveforms, determining power spectral densities, simple averaging, auto and cross-correlations.

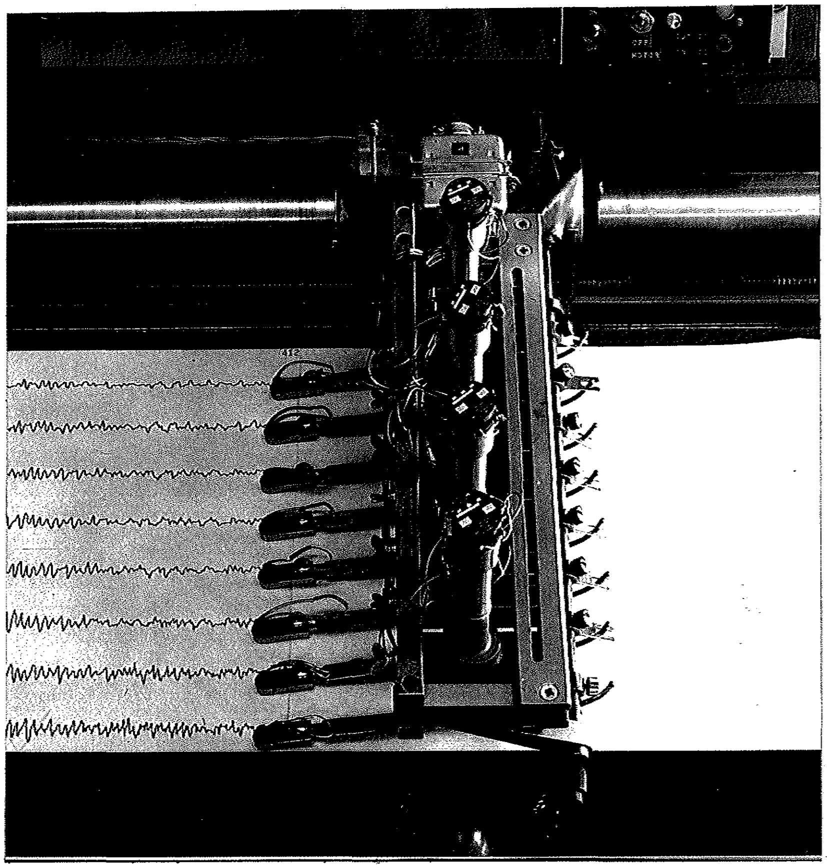


FIGURE 1:

Typical EEG record being Digitized

Because of the complexity of the waveforms (Figure 1) and the large volume of data to be processed (each EEG record is about thirty feet long) some automatic form of computation is necessary. While analog or digital equipment can be used to process the data, digital computers possess an advantage when many different types of analysis are to be used. Since the research is only in a preliminary phase, many different forms of analysis are required, and a digital computer is used for computations.

Data for use in a digital computer should be in the form of an appropriately coded binary representation. The input medium is commonly punched paper tape. To translate the continuous EEG waveforms to a coded punched paper tape, some form of sampler and analog-to-digital converter (ADC) is required.

The standard EEG data is available in the form of graphical records. While apparatus is commercially available to handle analog voltages in real time, no standard equipment will automatically handle graphical records.

The standard method of digitizing graphical records is to manually measure and note the amplitude of the recorded waveform at intervals along the time axis. The method is laborious, time consuming, boring and often inaccurate. The most annoying thing about this simple method is that it can be done by anyone and always works. Various types of scales, graticules and semi-automatic cursors have been devised to make the measuring and translating of the data somewhat easier[2]. All of these methods suffer from long conversion times and errors due to operator fatigue.

Where the record is a single channel to a large scale, with a low frequency content, line followers [2], [3], [4], have been designed to automate the foregoing procedure. For multichannel records, this procedure is not economical. The most practical method for multichannel work is some form of scanner and multiplexer arrangement with a single readout and output device.

Previous work at the EEG Department of the Winnipeg General Hospital had led to the development of a crude graph-reader[5]. This apparatus consisted of an opto-mechanical scanner and relay circuitry plus a commercial digital voltmeter - printer, - paper punch combination. This equipment was inaccurate and slow. The time required for each conversion was of the order of two to five seconds.

Since no commercial equipment was available, an apparatus was designed to automatically convert these graphical records into digital punched tape. The logical and electronic design of this apparatus is the subject of this thesis.

The final apparatus (Figure 2) is a large complex instrument using the scanning method of the previously described prototype and the same punch output. This paper will describe the design of the machine logic and the electronic implementation of the design. Particular attention will be given to the design of the logic and the digitizer. The design of other portions of the instrument will be described only in relationship to the central design. This somewhat arbitrary division is necessary for the sake of brevity.

CHAPTER II

SYSTEM DESIGN

The initial design was begun on two fronts; the "Operational Requirements" and the actual "Design". As the design evolved, the requirements were, of necessity, modified until the design was said to be final. At this stage, the system logic was fixed. The electronic details were still unknown but functions were generally blocked out.

Due to the complicated relationships between the electronic and logical design and requirements the actual design procedure cannot be discussed. This chapter describes the final design and indicates the important factors which governed the design procedure.

Initial Specifications and Design:

Early in the design, it was decided that the apparatus should be in the form of a movable console. The unit was to be self-contained and only need connecting to the appropriate services to be put in operation. A console was designed and constructed (Figure 2).

The paper record was to be fixed in position on the table and the scanning mechanism was to advance by preset increments of 1/4, 1/2 or 1 mm. Thus samples would be taken along the record corresponding to equal increments of time. Each channel was to have its own scanning head - patterned after the prototype[5].

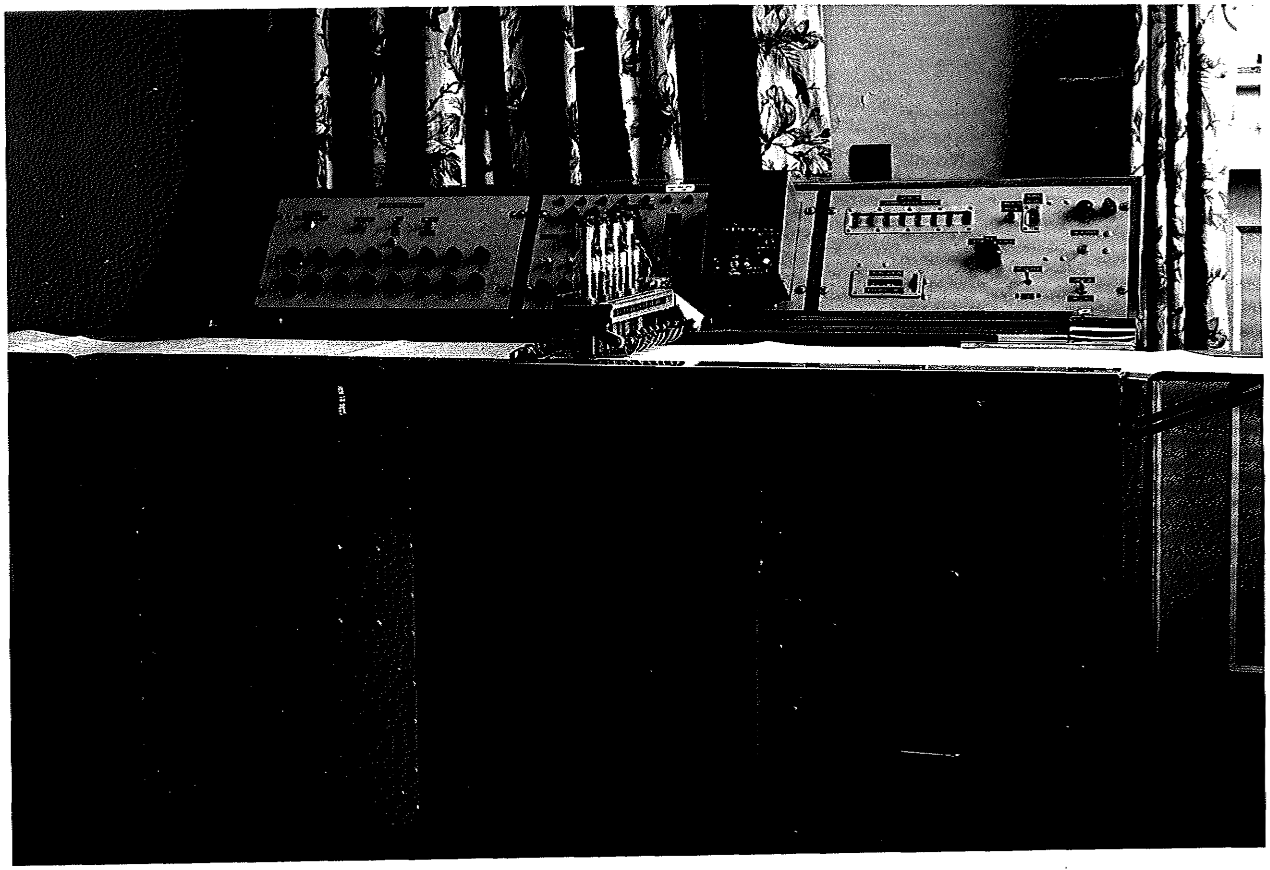


FIGURE 2:

The Analog to Digital Converter

In the interests of economy and reliability, the electronics was to be a mixture of semiconductor and relay type circuitry. The output device was to be a "Clary 703" paper tape punch. The punch code was to match the "Royal McBee LGP-30" computer.

The actual design was governed by three main factors:

1. Conversion Speed
2. Conversion Precision
3. Parts Cost

1. Conversion Speed

The prime requirement was for the greatest possible speed of operation. This was important because of the large number of data points to be digitized. The EEG bandwidth was from 0 to 50 hz. The minimum number of samples was then 100/sec. and 200 samples per second were desirable [6, 7]. As the routine EEG recording paper speed was 30 mm./sec., and the minimum reliable step of the mechanical scanner was 1/4 mm., the maximum sampling rate was 120 samples per second. Since it was desired to digitize samples of 30 seconds duration, this meant 30 x 120 = 3,600 samples per channel or, for eight channels, 28,800 sample points - approximately 300,000 binary bits.

For the fastest rate of prototype (2.5 seconds per conversion) the conversion time was:

$$\begin{aligned} 28{,}800 \times 2.5 &= 72{,}000 \text{ seconds} \\ &= 20 \text{ hours} \end{aligned}$$

which was prohibitive.

It was desired to design for a rate of approximately five conversions per second. This meant that the sample could be digitized in one or two hours.

Associated with the speed of conversion was the need for rapid data loading of the computer. This factor was governed by the punch coding and will be described in Chapter 3.

2. Conversion Precision

The data required only moderate precision. The figure of ± 1/2% was set as an acceptable error[5]. That is, by setting the amplitude scale to ± 100 units (or 200 units peak to peak) an error of ± 1 unit could be tolerated. This permitted the use of simple, high-speed, digital conversion techniques.

Since the data was treated by statistical methods, larger, isolated errors could be tolerated as long as they were few and randomly distributed. This meant that the digital data handling could be very simple, without the need for self-checking codes.

3. Parts Cost

The last and most binding of all requirements was that of keeping parts cost to a minimum. This factor necessitated the design construction of many circuits which would otherwise have been bought.

A. D. C. Logical Design

Basic Analog to Digital Conversion:

Analog to Digital Converters (ADC's) are basically of the form shown in Figure 3. This diagram will be used to explain the logic and operation of the ADC.

The analog signal is first sensed and sampled by the sampler. The sampler selects and stores a DC voltage proportional to the signal at the time of sampling.

The sampler is controlled by the logic. The logic section ensures that a correct sample is taken, and that it is taken at the proper time in the operating sequence of the equipment.

The sampled signal voltage is then applied to the ADC proper or digitizer. The digitizer performs the digital measurement of the analog signal voltage stored in the sampler. It operates by generating a voltage of known digital value equal to the signal voltage. The digital signal representation may be in ordinary binary notation or coded according to some error-reducing scheme. The digitizer is also controlled by the logic to ensure that the correct signal sample is digitized, and that the operation is synchronized with the other machine operations.

The signal, now in digital form is then routed to the output, which, at the command of the logic, stores the coded data in the desired format. The output unit also signals the logic when it has finished storing the data.

After receiving a "stored" signal from the output the logic resets the digitizer and sampler units and allows the cycle to repeat.

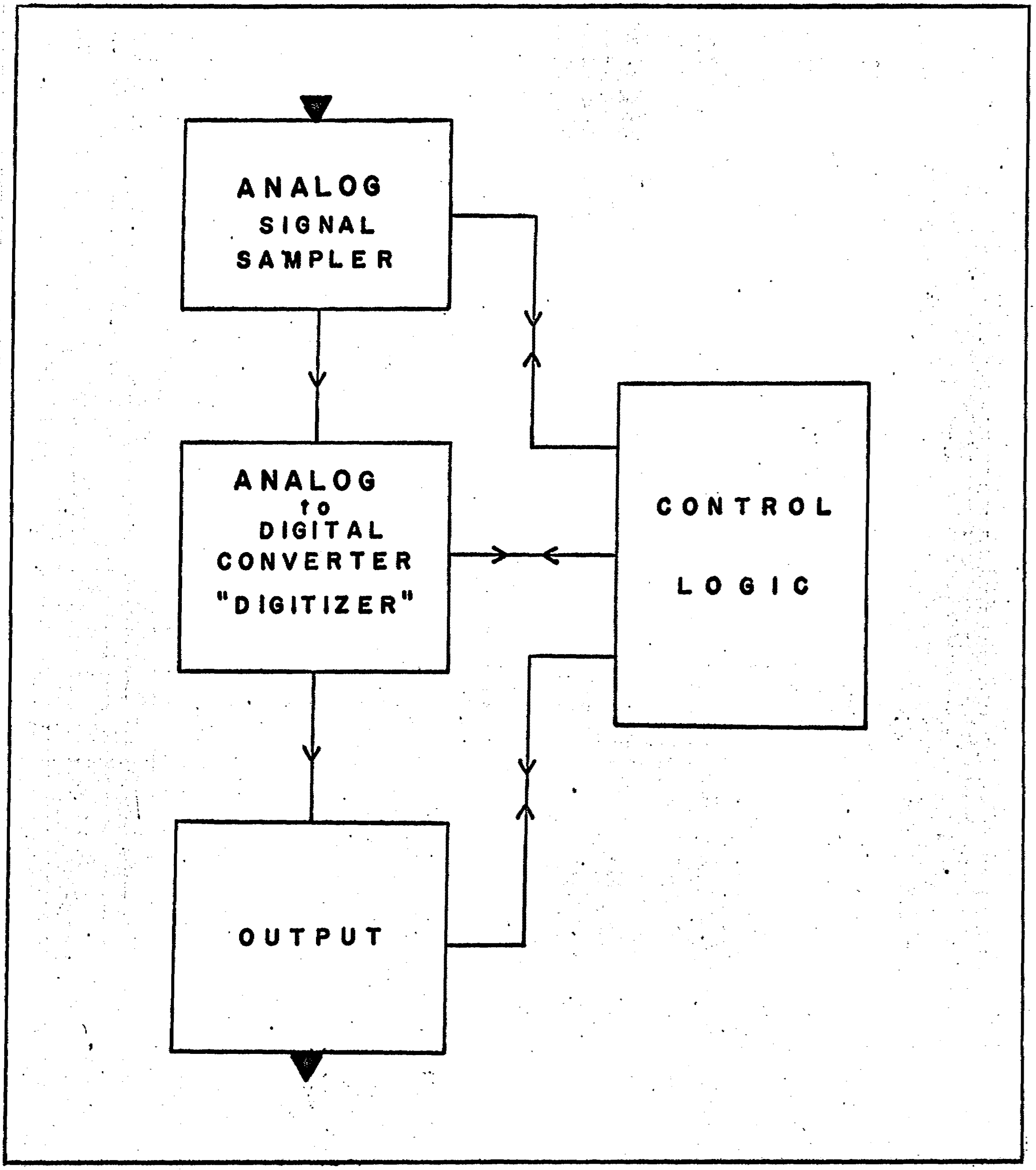


Fig. 3
BASIC A. D. C.
BLOCK DIAGRAM

Actual Machine Logic:

The A. D. C. logic outlined in the preceeding section is quite simple. However, when expanded to cover the actual equipment, additional steps must be introduced. As the original signal is in the form of a graphic tracing, the record must be sampled and a proportional sample voltage must be generated. Also, multichannel operation requires more internal logic for each operation. Figure 4 illustrates the Flow Diagram for the operation of the machine.

The three main blocks, Logic, Scanner and Readout are closely interrelated. The division is made in this manner to better illustrate the different operating phases.

The operation of the actual converter is best understood by considering the general machine logic. Each of the main blocks shown in Figure 4 performs a specific function under the control of its own sub-program. Each sub-program controls the main program for its own portion of the cycle, with control being switched by the overall program for each phase of the cycle. Thus each block is either in an active state corresponding to control of the program for that particular phase, or in a dormant or inhibited state when some other block is active. The inhibition of all except the one active block is performed by the logic block. The description of the different functional states follows. Figures 5 and 6 show the flow diagrams for the two operating modes.

a) Scanner Control

The scanner function is to sample the graphical record.

The scanner (Figure 5) consists of an opto-mechanical scanning head (Figure 1) mechanically coupled to a potentiometer to produce a voltage proportional to the angular deflection of the optical sensing head. This voltage is connected through the scanning relays to memory capacitors.

The photo sensing heads are swept across the back-lighted paper, and when the photocell crosses the inkline a pulse is produced, thus detecting the position of the line.

The pulse will set the scanning flip-flop for that channel thus opening the scanning relays and storing a voltage proportional to the position of the inkline on the memory capacitors.

The scanning flip-flops "remember" the scanned state and signal "scanned" to the Logic. Each flip-flop also turns on a light to give visual indication of having scanned.

Thus all channels are scanned simultaneously and the information (ink line position) is temporarily stored as proportional voltage amplitudes on the memory capacitors. The signals are then in analog form.

When all channels are in the "scanned" state, the Logic shifts control to the readout phase.

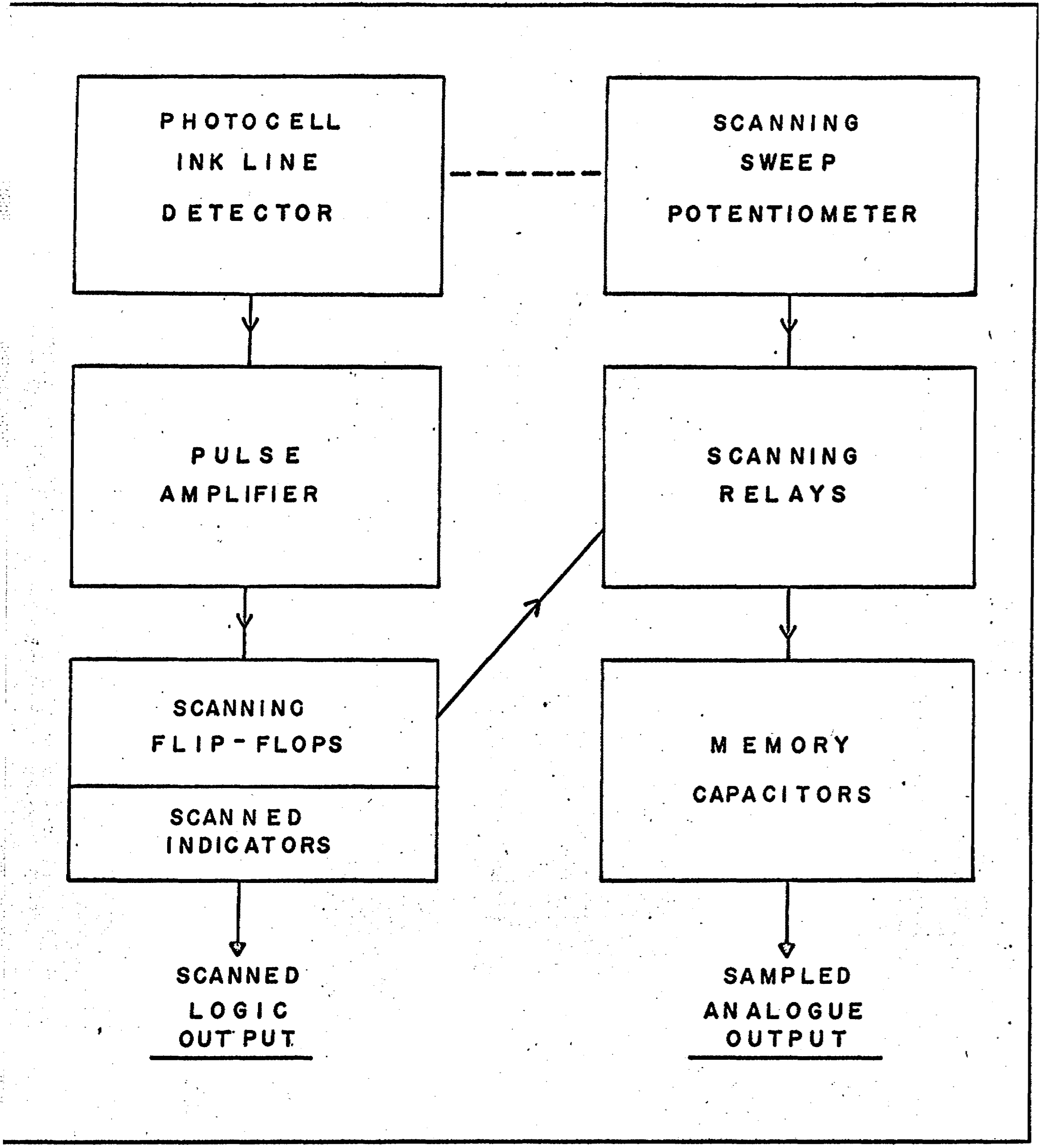


Fig. 5
SCANNING FLOW DIAGRAM

b) Readout Control

When the scanning phase is finished, the readout cycle (Figure 6) starts. The memory capacitors are interrogated serially in the sequence set on the Logic. Each capacitor is connected in turn to the electrometer and digital voltmeter for measurement of the sampled signal voltage. This "digitizer" produces a binary coded relay type output to the paper tape punch and a visual decimal representation for the operator. The punch reproduces the coded data on paper tape to be fed to the computer. At the end of a punch cycle, the readout is switched to the next capacitor and the cycle repeats until all are read. Then the Logic again switches over to the Scanner and the overall machine cycle is repeated.

The readout circuitry encompasses those circuits which translate the stored voltage signals into punched paper tape.

The channelselection portion of the Logic serially activates the readout relays to connect the memory capacitors to the digitizer. A decimal projection type display is also activated to indicate the channel number being read out. Both circuits are activated through a single contact by means of a diode gate.

The channel number signal to the punch is derived from an isolated reed relay located in the coil of the readout relay. Thus, the existence of the channel code on the tape is then evidence that the readout relay did operate, and that it was the correct relay.

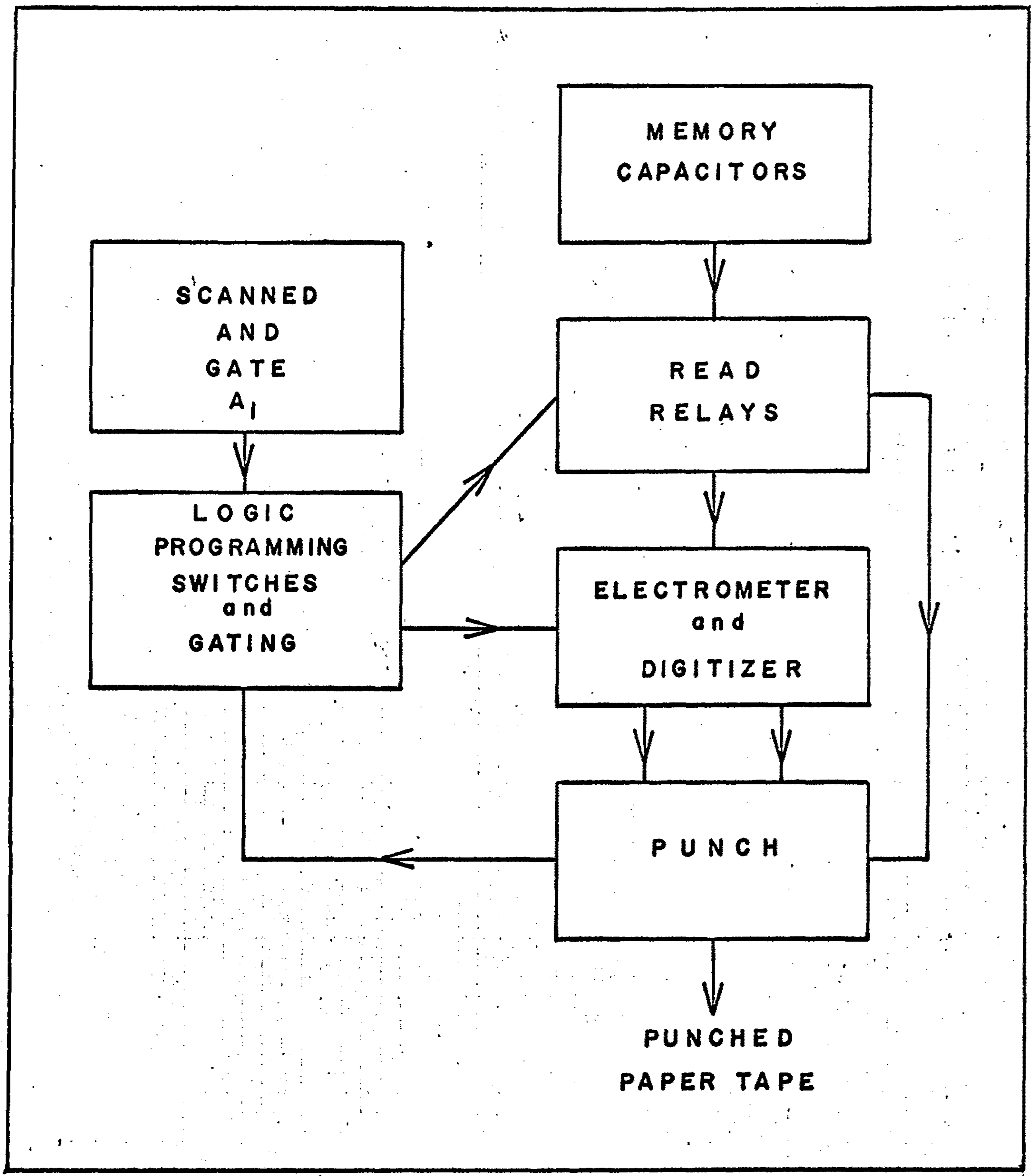


Fig. 6
READOUT FLOW DIAGRAM

After several milliseconds delay to ensure that transients in the electrometer circuit are damped out, the digitizer is enabled and the capacitor voltage is digitized. Upon completion of the digitization, the digitizer signals the Logic which generates a start punch signal to the paper tape punch. The start punch signal is a simple contact closure from a relay activating a clutch solenoid in the punch. Once started, the punching cycle continues under the control of the built in stepping switch which serially selects the four words for that channel.

In order to signal the Logic that the data has been punched, the last contact on bank two of the punch stepping switch is used to actuate a relay at the end of the punching cycle. When the Logic receives this punched signal, it advances the channel selector readout switch one step, resets the digitizer, and the readout cycle repeats for the next channel.

c) Logic Control

While a great deal of the machine logic is built in to the scanner and readout as a fixed program, there are other, variable, logical tasks. The operator can set up any sequence of channel readout that is desired. Also, the Logic synchronizes the different functions to permit proper continuous operation. The Logic section is used by the operator to program the machine for Manual Operation for setting up, Automatic Operation for data digitizing or Single Operation for checking purposes.

The flow diagrams Figures 5 and 6 show the important signal paths during the two main operational phases. The details of each functional block will be discussed in following chapters.

The initial design was based on a synchronous or clocked mode of operation. That is, all functions would be carried out in order sequenced by a central clock. Half way through construction this design had to be adapted to a non-synchronous mode when the mechanical scanning mechanism was delivered and was found to be a continuous-running device. In order to synchronize the different operations, gating circuits were added which greatly increased the complexity of the logical circuitry.

CHAPTER III

DATA OUTPUT FORMAT AND CODING

Tape Output - Data Coding

The tape characteristics of the paper punch determined the design of the readout. The punch (Clary 703) is basically a set of solenoids controlling a hole punching mechanism. Associated with the solenoids is a Diode Encoding Board for generating different codes, a multicontact stepping switch, and 120 pin connector used as a program cartridge. These facilities permit one to program the tape perforator in four ways and to select whichever method of operation is desired by means of external contact closures. The tape perforator punches data in the form of rows of holes across the width of the paper tape. The column position of the hole determines its coded value.

The first step in choosing the tape format was to determine which code would permit the fastest operation. After investigating several coding schemes the following code was decided on as best for this application.

All numbers are digitized and coded in pure binary form. Thus the channel numbers 0-8 decimal require four binary bits and the sampled data in the range of 0-200 decimal counts require eight binary bits. As this data tape feeds an LGP-30 computer, the tape should be in LGP-30 code and also requires some additional coding for data handling by the computer.

The data for each channel point then requires only four rows of words on the tape (Figure 7). Binary coded decimal coding would require five rows, and also require computer time to internally decode the data.

Using this method of coding, the data can literally be "dumped" into the computer memory by the use of a simple input program; instead of the normal method of translating the coded data with an input subroutine. Since the translation of input data in the LGP-30 computer is quite a slow process, this coding speeds up the data loading by about twenty times over the normal method. In view of the large amount of data to be handled, speed is of great importance.

This type of coding does not allow the use of a self-checking type of code. As discussed in the introduction, this was not considered serious since errors should be few and random and therefore have small effect on the computed results. This assumption has since been verified in practise.

The tape format is:

Word 1: channel number and data code
Word 2: data high order 4-bits and data code
Word 3: data low order 4-bits and data code
Word 4: conditional stop code

The channel number is shown by punching the appropriate holes in the tape columns one through four and a hole in column five which is the computers code for data input.

The high and low order bits of the binary data is similarly represented.

This is followed by a single bit in the sixth position which indicates the end of that data word and signals the computer to dump the input register into memory. This code is generated in the punch by the internal stepping switch.

In order to conserve time, the punched data for each cycle follows one upon the heels of the other without a zero code between the cycles.

This tape format (Figure 7) allows the computer to directly accept the serial data and assemble it in its input register in the following binary form:

Channel Number	Data		
4 bits	high order 4 bits	low order 4 bits	zeros
0 1 0 0	0 0 1 1	0 1 0 1	0 0 0 0

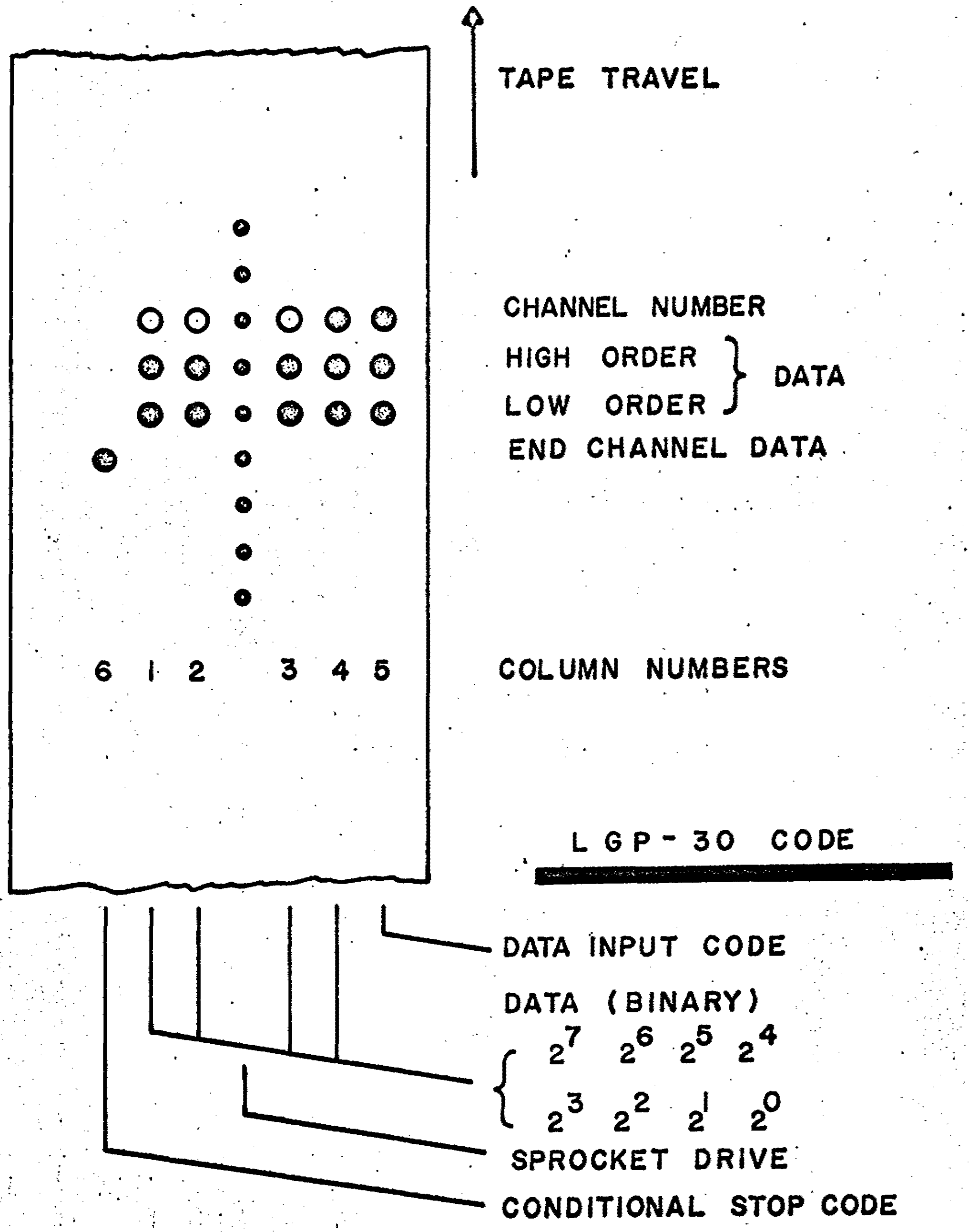


Fig. 7
PUNCHED TAPE CODING

Tape Punch Coding:

Once the data format was decided upon the problem arose of programing the punch unit to produce this format and also still be useable with a Clary Printer drive since the normal Clary procedure is to drive the punch from a printer. As this process was too slow it was necessary to drive the punch directly. The punch logic was modified slightly to permit a direct drive. Figure 8 shows the diode gating used to generate the data coding. The punch selector switch presents the data sequentially in the four blocks previously described. Note that the clutch is energized whenever a punch solenoid is energized.

Channel Number:

The channel number being read out is signalled by means of a single relay closure (decimal data). This isolated set of relay contacts is part of the readout relay of each channel. This decimal number is decoded to binary by the decimal to binary diode matrix on the encoding board in the punch (Figure 8).

Binary Data:

The digitized data (already in binary form), the conditional stop code and the data input code are fed directly to the solenoids through "or" gates formed by diodes added to the encoding board.

The binary signals to the punch are generated by reed relays in the digitizer circuit. These relays are not rated to make or break the heavy currents used in the punch. In this use, however, the contacts close and then current is later supplied from the punch. The reed relays should have very long life under these conditions. The other reason for using reed relays is their high operating speed - a necessity since they must follow the transistor counter.

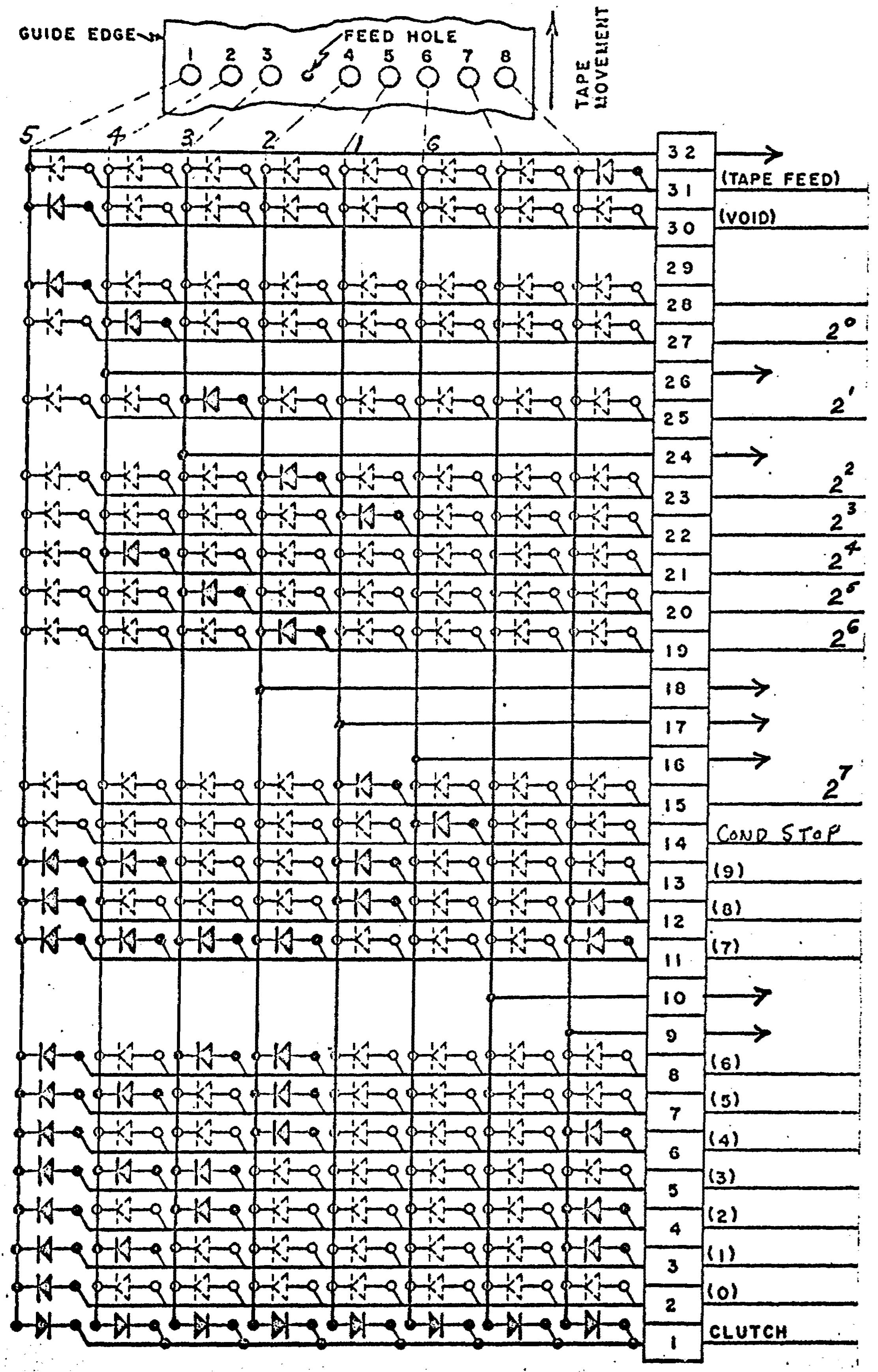


Fig. 8

DIODE ENCODING BOARD -- CLARY TAPE PUNCH

CHAPTER IV

DIGITIZER

The digitizer is composed of the electrometer circuit (Appendix 2) feeding an Electrologic Digital Voltmeter which has been modified to provide an electrical output. The output is a series of pulses which are counted by an eight stage binary counter controlled by a gating system of original design.

Digital Voltmeter

The Electrologic Voltmeter is a simple Digital Voltmeter (DVM) of the stroboscopic ramp type [8]. That is, an internally generated ramp voltage (Figure 9) is compared with the unknown voltage by a comparator circuit which indicates when the ramp is equal to the unknown voltage. In this voltmeter the ramp voltage is generated by a continuously turning carbon film potentiometer. Mechanically coupled to the potentiometer wiper is a drum bearing a photographic film having a bar-space design and numbers on it. When the comparator senses equality of the ramp and the unknown voltage, it triggers a strobe lamp at the next occuring clear stripe on the film track. The light shines through the film and projects the corresponding number on the film against a frosted glass to produce the decimal readout. The device is simple and relatively inexpensive. It was decided to use this DVM as the basis of the digitizer rather than make a full digitizer. A commercial digitizer would have cost over $5,000 and the electrologic DVM cost was $300. Additional parts cost was estimated at less than $300.

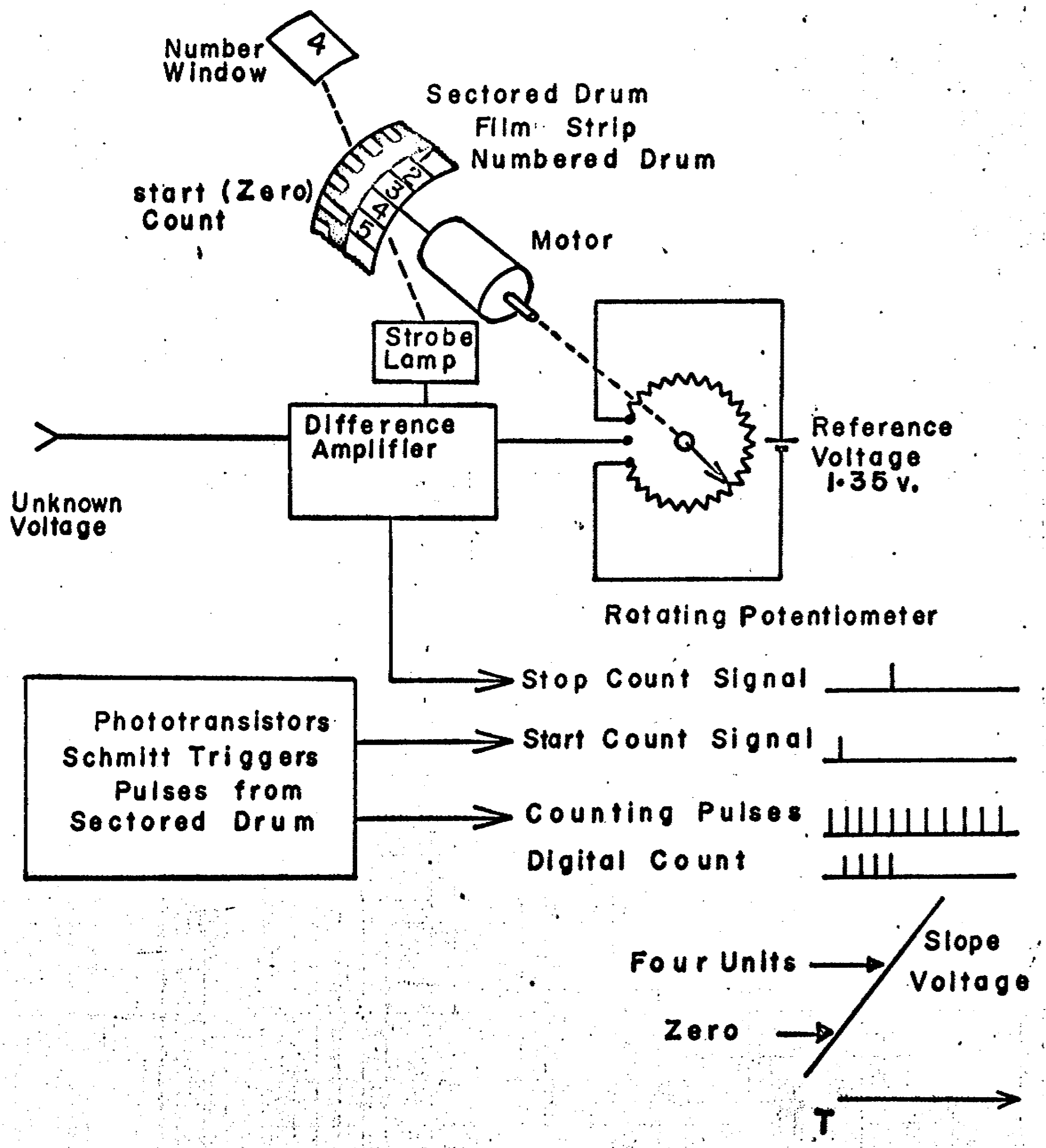


Fig. 9
ELECTROLOGIC VOLTMETER

The method was to use the optically striped drum (Figure 9) of the DVM as a source of pulses to be counted by a binary counter. The counter would be controlled by a gating system so that it would start counting at the foot of the ramp voltage and stop counting when the comparator indicated equality of the ramp with the unknown voltage. While straightforward enough in principle there were practical difficulties which very shortly made themselves apparent.

The main difficulty was that the instrument had not been designed for this sort of use. The ramp voltage and the corresponding numbers on the film drum were somewhat arbitrarily arranged in relation to the sensing phototransistor. It was found necessary to make an adjustable mount for the phototransistor to allow setting of the time relationship between the start pulse, the ramp voltage, and the counting pulse.

When the blank film space that corresponded to zero volts was located, it was lengthened and another phototransistor was put in to act as a zero indicator (start-count-pulse generator). The phototransistor signal was squared up by a schmidt trigger circuit similar to the electrologic design.

The phototransistors were mechanically phased so that the start pulse was one-half pulse width ahead of the first counting pulse; thus the start and stop pulses could both appear (in the case of zero volts unknown) before a pulse was counted. An electrical output was taken from the comparator circuit to act as a stop counting pulse.

Thus the modified DVM provided a start count pulse, a series of 250 counting pulses synchronized both to the start pulse and the ramp voltage, and a stop count pulse whenever the ramp equalled the unknown voltage.

The functions of the gating circuitry proved to be somewhat more complicated than appeared on the surface. The interconnected gating circuit shown in Figures 10 and 11 evolved as the design answer. The complications arise from the fact that the DVM runs continuously while a triggered mode of operation is required. The circuit shown is used to synchronize the DVM to the readout cycle from the Logic. This circuit makes the continuously running DVM operate as a triggered digitizer insofar as the electrical output is concerned.

CONTROL GATING

The control gating of the counter has to do the following:

a) reset the counter and counter logic after punching data. This function is signalled from the Logic - only during the readout mode.

b) wait for a start pulse before allowing pulses through to the counter, and not be affected by a stop pulse if one appears before a start pulse: i.e. set the operating program.

c) upon receipt of a start pulse it simultaneously allows counting pulses to pass through the counting gate and also immediately becomes sensitive to the next stop pulse.

d) upon receipt of the stop pulse (following a start pulse) the circuit stops the counting pulses and latches itself so that it is totally unaffected by succeeding start or stop pulses until it is again reset by the Logic.

These functions allow the counter to retain the count until the data is read out to the punch. Thus the gating involves memory states and sequence detection in addition to the gating functions. The triggering of the control gate circuit into its "counted" state also signals the Logic to start the punch and so punch out the digitized data stored in the counter.

The method adopted is a combination of two binary stages for memory combined with cross linked "and" gates. i.e. A_4, A_5, and FF_a, FF_b of Figure 11. The circuit is shown in Figure 11 and the Block diagram in Figure 10.

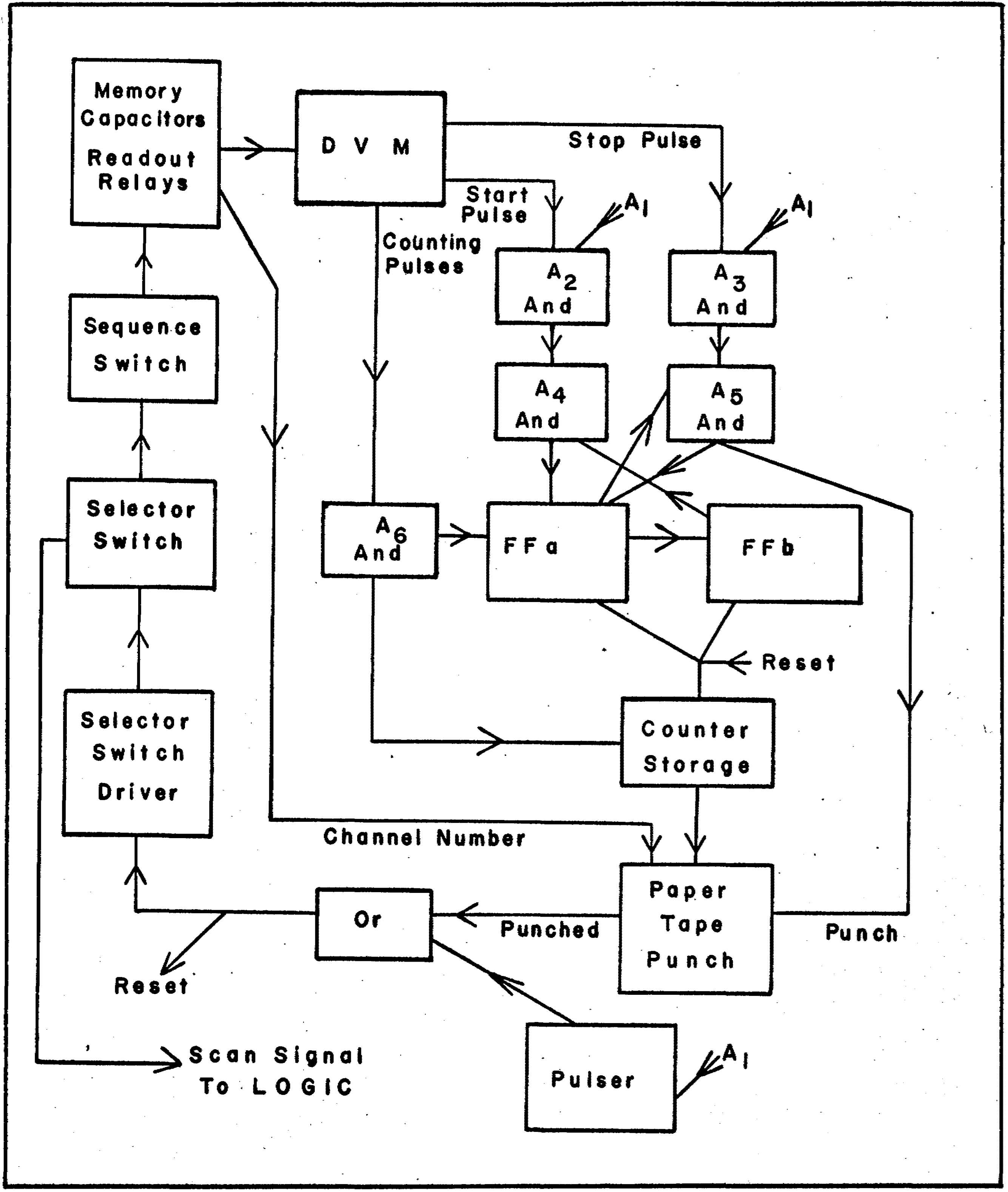


Fig. 10

DIGITIZER LOGIC

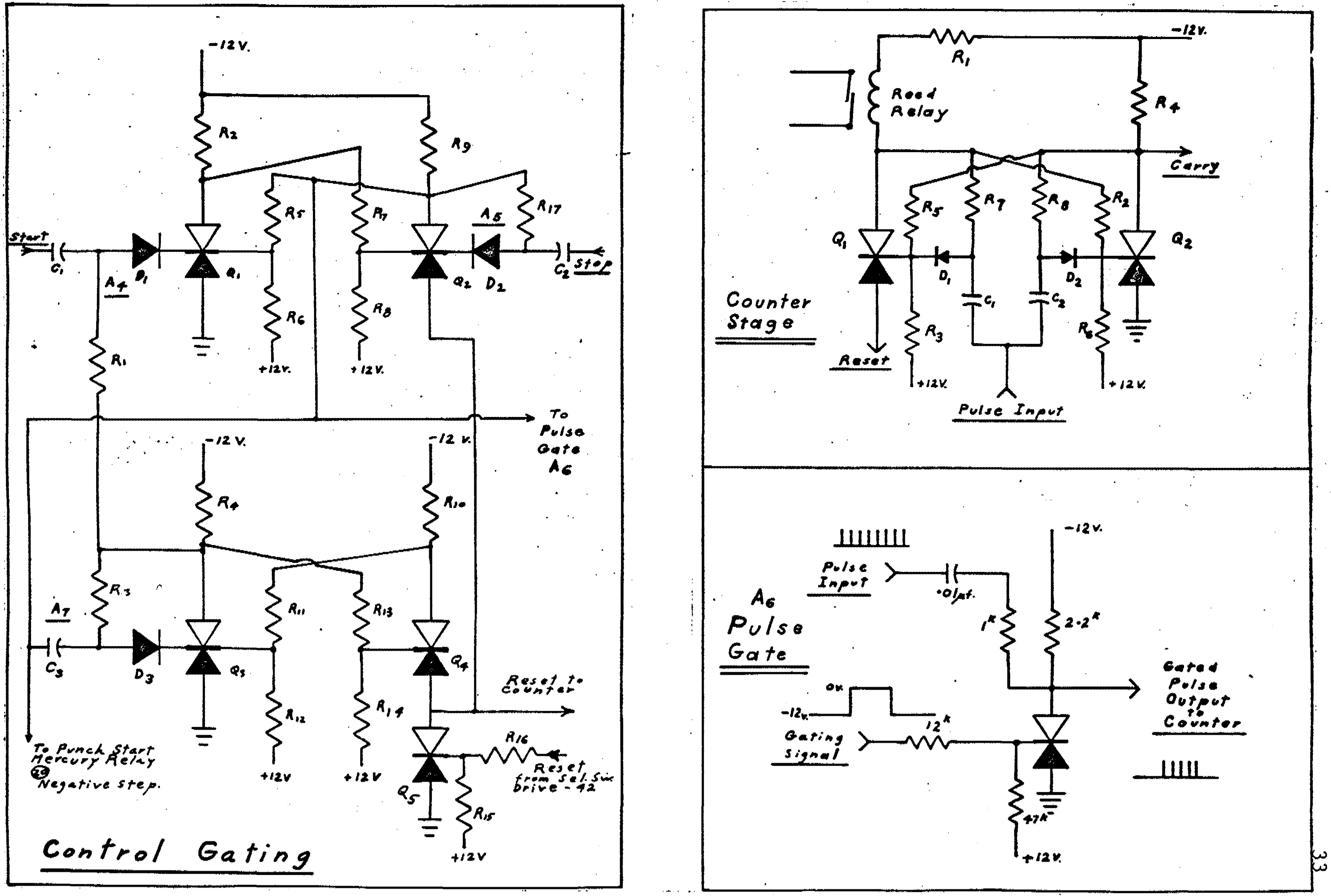


Fig. 11
DIGITIZER CIRCUITRY

The operating sequence is as follows:

Start, stop and data pulses are continuously generated by the DVM. In order to ensure that the gated counter is active only during the readout phase, "and" gates A_2, A_3 are controlled by the scanned "and" gate A_1. So long as the Logic is in the scanning mode, no signals pass through A_2 and A_3. After all channels have scanned, A_1 enables gates A_2 and A_3 and then FF_a, FF_b and the binary counter are reset after the readout has been switched to the first channel.

Then the circuit states are:

<u>Condition 1:</u>

A_2, A_3, A_4, A_7	Enabled - passing pulses
A_5, A_6	Inhibited - no pulses pass
FF_a	$\bar{a}$
FF_b	$\bar{b}$

Therefore, stop pulses cannot pass through to FF_a but start pulses can. The circuit thus waits for a start pulse. After triggering by a start pulse, the conditions:

<u>Condition 2:</u>

A_2, A_3, A_5, A_6	Enabled - passing pulses
A_4, A_7	Inhibited - no more start pulses pass
FF_a	a
FF_b	b

Pulses pass through A_6 and are counted by the counter. When a stop pulse appears, it turns FF_a off and thereby inhibits gates A_5 and A_6 stopping the counting pulses from being counted.

Then the circuit states are:

Condition 3:

A_2, A_3 .... Enabled - passing pulses

A_4, A_5, A_6, A_7 .... Inhibited - not passing pulses

FF_a .... a

FF_b .... b

In terms of Boolean Algebra, the logical equations are:

$$\begin{array}{lcl} A_2 & = & \text{start} \cdot A_1 \\ A_3 & = & \text{stop} \cdot A_1 \end{array}$$

State 1:

$$\left.\begin{array}{lcl} A_4 & = & A_2 \cdot \bar{b} = \text{start} \cdot A_1 \cdot \bar{b} \\ A_7 & = & a \cdot \bar{b} \end{array}\right|_{\bar{b}}$$

$$\left.\begin{array}{lcl} A_5 & = & A_3 \cdot a = \text{stop} \cdot A_1 \cdot a \\ A_6 & = & \text{pulses} \cdot a \end{array}\right|_{\bar{a}}$$

State 2:

$$\left.\begin{array}{lcl} A_4 & = & \text{start} \cdot A_1 \cdot \bar{b} \\ A_7 & = & a \cdot \bar{b} \end{array}\right|_{b}$$

$$\left.\begin{array}{lcl} A_5 & = & \text{stop} \cdot A_1 \cdot a \\ A_6 & = & \text{pulses} \cdot a \end{array}\right|_{a}$$

State 3:

$$\left.\begin{array}{lcl} A_4 & = & \text{start} \cdot A_1 \cdot \bar{b} \\ A_7 & = & a \cdot \bar{b} \end{array}\right|_{b}$$

$$\left.\begin{array}{lcl} A_5 & = & \text{stop} \cdot A_1 \cdot a \\ A_6 & = & \text{pulses} \cdot a \end{array}\right|_{\bar{a}}$$

The circuitry then is in a latched state, incapable of counting more data pulses. The associated binary counter stores the counted pulses. The circuit stays in this latched state until it is reset from the Logic. Upon reset it returns to the initial ready state. The program of start-count-stop, is inherent to the circuit design.

The circuit to do this complicated bit of gating is shown in Figure 11. This design takes maximum advantage of the many possible inputs and outputs of the standard binary flip-flop. This circuit contains a minimum of components because the logical gates (A_4 & A_5 of Figure 10) are incorporated as part of the pulse-steering circuits of the flip-flops. They are a mixture of level and pulse type gates. The circuit is simple and operates well. This circuit is an original design.

COUNTER/STORAGE

The counter stages are shown in Figure 11_b. The circuit is a standard cascaded binary chain or ripple counter. Each transistor Q_1 controls a reed relay for readout of the state of the flip-flop to the Clary punch - a one is indicated by a contact closure. The flip-flops function as a counter and then serve as memory when isolated by the control gating circuit.

Reset of the synchronizing gate and counter binaries is done by opening the emitter circuits of the selected transistors. The circuit is reset after the storage capacitor is connected to the readout circuitry so that the voltmeter reading may settle to a steady value. It should be noted that reset does not alter the state of FF_a and so does not produce a punch start signal.

CHAPTER V

LOGIC

All other functions not previously discussed are encompassed by the Logic.

The original design conceived the logic as an internal clock controlling gates governing the operation of the other functional blocks. Then the scanning mechanism was changed to a continuously running system as was the DVM with the adoption of the Electrologic DVM. This changed the function of the logic from clocking to synchronizing and sequencing. This multiplicity of functions enormously complicated the logic circuitry. While the logical outline did not change very much, the circuitry became very complicated due to there being so very many possible operating sequences.

Some of the logical functions which had been simple triggers under the clocked method were now required to produce long pulses so that overlapping of states could take place. These logical delays increased the conversion time of the apparatus but were necessary.

At this stage the design procedure degenerated to thinking of possible combinations, designing them into the logic circuitry, then building the circuit, and trying it, in order to find the combinations that had not been foreseen. The reason for this was that these changes were forced on the design after it was almost completed; and there was not sufficient time to redesign the apparatus. Also, the expected usefulness of the equipment did not justify a complete redesign.

This method did succeed, however in producing a workable design. One might almost say that the design evolved in answer to the difficulties that arose during this period of making and testing.

Since the functioning of the Logic is mainly one of sychronizing and sequencing, each section of the logic must be discussed by itself and also in relationship to the rest of the machine. In the interest of brevity, the following discussions will deal with only some of the individual sections of the logic and introduce the interrelationships as required.

The first and foremost function of the Logic is to sequence the different machine functions so that the machine can start and then continue to operate. While this sounds self evident, it is a fact often forgotten by designers of logical systems. In this apparatus, the machine is started by a master control switch which resets the circuitry as if the readout cycle had just ended - ready for scanning.

This is done in the "Manual" position. To set the machine in operation, the switch is thrown to operate and the scanning cycle starts. Alternatively, if testing is required, the switch is turned to the "Single Operate" position and one scanning and readout cycle is performed on the manually selected channel. The circuitry of this switch will be discussed later.

At the heart of the Logic are the programing switches - the sequence switch and selector switch. These circuits are tied into almost every other logic circuit.

SEQUENCE SWITCH:

The purpose of the sequence switch is to permit variable programming of the scanned channels. The paper record has eight channels of information numbered from one through eight respectively. The sequence switch permits digitizing any number of the channels in any desired sequence. The desired channel order is simple set-up in order on the eight sequence switches. The eight sequence switches are selected sequentially by the driven selector switch to digitize whichever channel is set on the chosen switch. This approach permits very flexible programming.

The switching is done by a nine by eight crosspoint matrix of switch contacts. Thus any of the eight switches can select any channel line or else zero.

The data routed by each switch for a selected channel is:

Bank 1:

The "scanned" signal from the scanning flip-flops to the logic "and" (A_1) gate. Thus only the desired channels need to be set to scan. All other channels are neglected and do not control the logic.

Bank 2:

The readout channel command from the selector switch to the chosen channel.

Bank 3:

The "reset selector switch to position 11" command if that sequence switch is set at zero.

By the use of this switching arrangement, the sequence program is unlimited. Any sequence is set on the switch in the desired order. Some examples are:

a) only channel 1 once; sequence: 1 0 0 0 0 0 0 0

b) only channel 1-3 times; sequence: 1 1 1 0 0 0 0 0

(This would be used for checking for errors)

c) channels 1 through 5; sequence: 1 2 3 4 5 0 0 0

d) or other sequences; 2 1 3 6 7 8 5 4

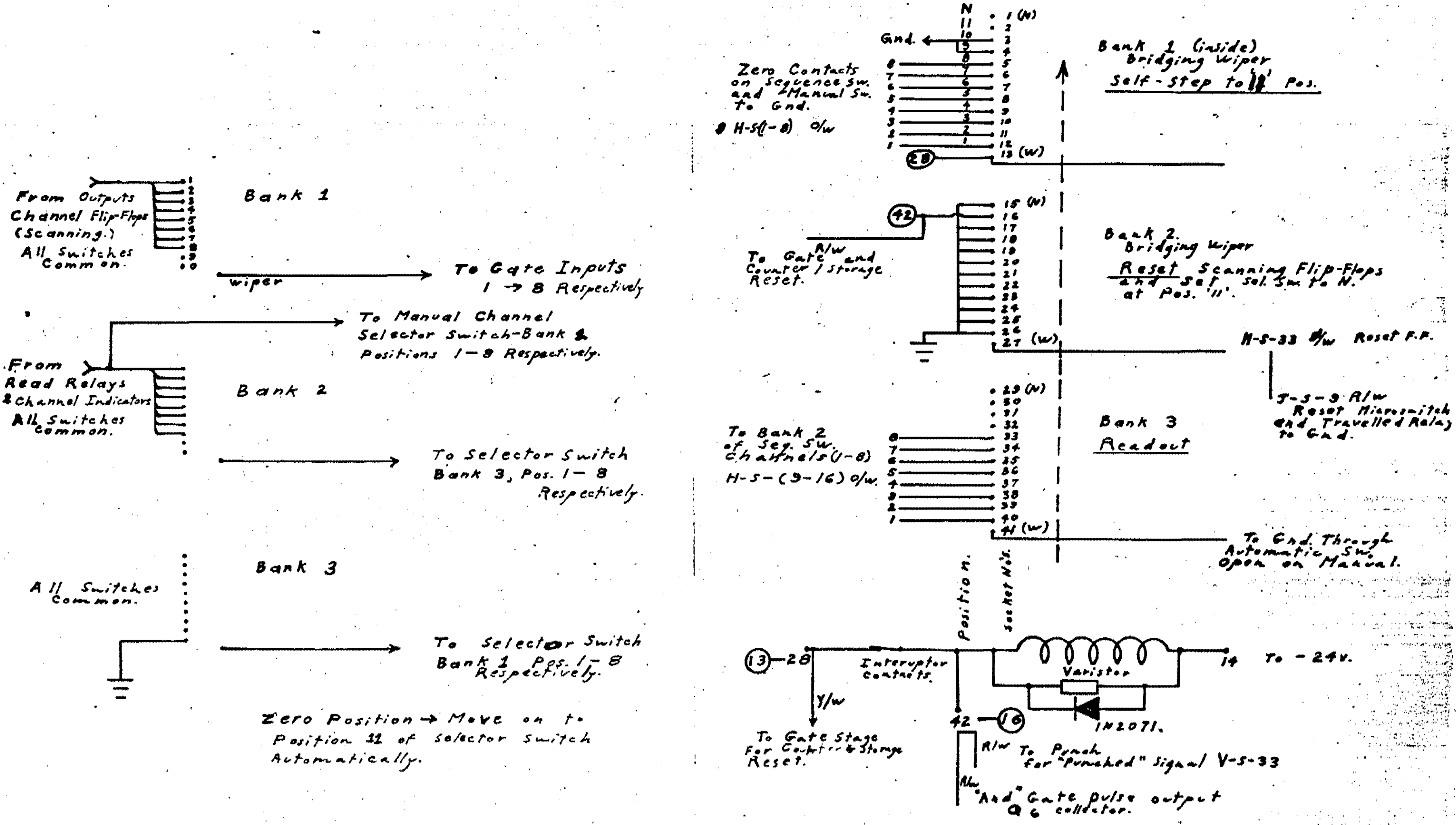
1 2 3 8 0 0 0 0

etc.

As the slowest part of the actual digitization is the punch-out, it is arranged that zero channels do not punch-out. This switching logic makes the machine faster and much easier to program than the prototype which required that nine channels be set-up and all read out even if a zero code were programmed for every second channel.

Each of the eight switches forming the sequence switch then had three independent banks (i.e. a 3P 10 pos. switch).

Typical wiring for one switch (all are similar) is shown in Figure 12. In order to have an in-line readout, printed circuit thumbwheel switches (Chicago Dynamics Corp.) were selected. This type of switch was selected on the basis of its long life, good electrical characteristics, and of presenting a lot of information in a small space, as well as being pleasing to view. The switch is shown in the upper right panel in Figure 2.



Sequence Switch

Selector Switch

Fig. 12
LOGIC PROGRAMING SWITCHES

CHANNEL SELECTOR SWITCH:

The selector switch is a three pole twelve position stepping switch of the type used for telephone service (Siemens Miniature Uniselector). It was chosen because of its use in the prototype and the fact that it was inexpensive and locally available. Also, its use at this point in the logic made for considerable cost savings over solid state switching matrices. As the speed of operation was not high, the stepping switch gave adequate performance. If only a single channel is being scanned however, it does waste time.

This switch is the type that is cocked by a driving pulse, then advances at the release of the pulse. Advantage was taken of this mode of operation to allow gating and logic functions to be performed quite simply.

The selector switch is active only during the readout phase. During the scanning phase, it sits on normal or home (position 12) and thereby inhibits the readout functions.

The wiring of the channel selector switch is shown in Figure 12. The three banks of contacts are shown:

Bank 1 - step to position 11

This set of contacts is connected to the wipers of Bank 3 of the sequence switch. Whenever the wiper (at contact 13) is grounded, it closes a gate and allows the logic to automatically step the selector switch onward. Thus whenever a selected channel is set to zero on the sequence switch (or always at positions 9 & 10 of the channel selector) the logic self-steps the stepping switch, so that it moved on to position 11. The switch will stop on position 11 due to the previously mentioned drive system. That is, at the end of the drive pulse received at position 10, the switch is advanced to position 11 and the gate is opened preventing further self-stepping

Bank 2 - reset scanning flip-flops

Bank 2 is used to signal the end of the readout cycle. This is done by inhibiting the resetting of the Scanning Flip-Flops until the end of the readout cycle. Once scanned, the Scanning Flip-Flops, through logic gate A_1, keep the Logic in the readout mode. By resetting the Flip-Flops at the end of the readout cycle the Logic is transferred back to the scanning mode. This function is performed by making this set of contacts part of a contact type "and" gate controlling the reed relay scanning flip-flop reset. As long as the wiper (contact 27) is grounded through one of its contacts, the reed relay is held closed and the Flip-Flops cannot reset. Since this is a bridging type (make before break) wiper, the wiper is grounded except when at position 11. Then, at the end of the readout cycle, the scanning Flip-Flops are reset and the stepping switch pulsed on to "home" where it waits for the beginning of the next readout cycle. The other inputs to the reset control circuit are from the sweeping microswitch and the travelled relay. Thus the scanning Flip-Flops cannot be reset until the stepping switch has reached position 11 (readout finished), the scanning carriage has travelled its full distance, and the sweep is about to begin.

Bank 3 - readout

The third bank has a non-bridging wiper so that only one contact is selected at a time. This bank is used to activate the selected channel readout relay through Bank 2 of the sequence switch. The reed relay circuits use telephone type practice. One end of the coil is attached to the power line and the circuit is completed by switching in the ground side. This has the advantage that switch breakdowns do not result in shorting of the power supply. The same configuration is also suitable for a transistor relay driver.

Bank 3 then, as it sequentially selects the programed sequence of readout relays, actually performs the interrogation of each channel.

SELECTOR SWITCH DRIVE:

The selector switch is pulsed by the selector switch driver.

The driver accepts single pulses from either:

"and" gate A_1 signalling the beginning of the readout cycle and stepping the selector switch to position "1",

or;

from the punched circuit of the punch signalling the end of that channel readout, thus moving the switch to select the next programed channel,

or;

from the resetting of the scanning flip-flops. The selector switch is moved to "home" by the leading edge of this signal pulse while the scanning flip-flops are not reset until the end of the pulse. This is to ensure that the selector switch is always on "home" and ready to move to position 1, when the next scan occurs. Since the reset pulse is a synchronizing pulse, it may have almost any time duration,

or;

from the gated oscillator producing a series of pulses to drive the selector switch to position 11.

The selector switch drive then is an "or" gate followed by a monostable multivibrator and power drive transistor. Outputs are also taken from the driver circuit to perform different resetting and gating functions.

SCANNED "and" GATE - A_1:

This "and" gate is used to switch the logic from a scanning mode to a readout mode upon completion of scanning. In conjunction with the scanning flip-flops which provide the memory function, the A_1 gate does the following:

a) detects when all chosen channels have scanned (from the scanning flip-flops).

b) advances the channel selector switch to the first position to initiate the readout cycle.

c) enables the gates so that pulses from the DVM can go to the counter-storage logic and so digitize the measured voltage.

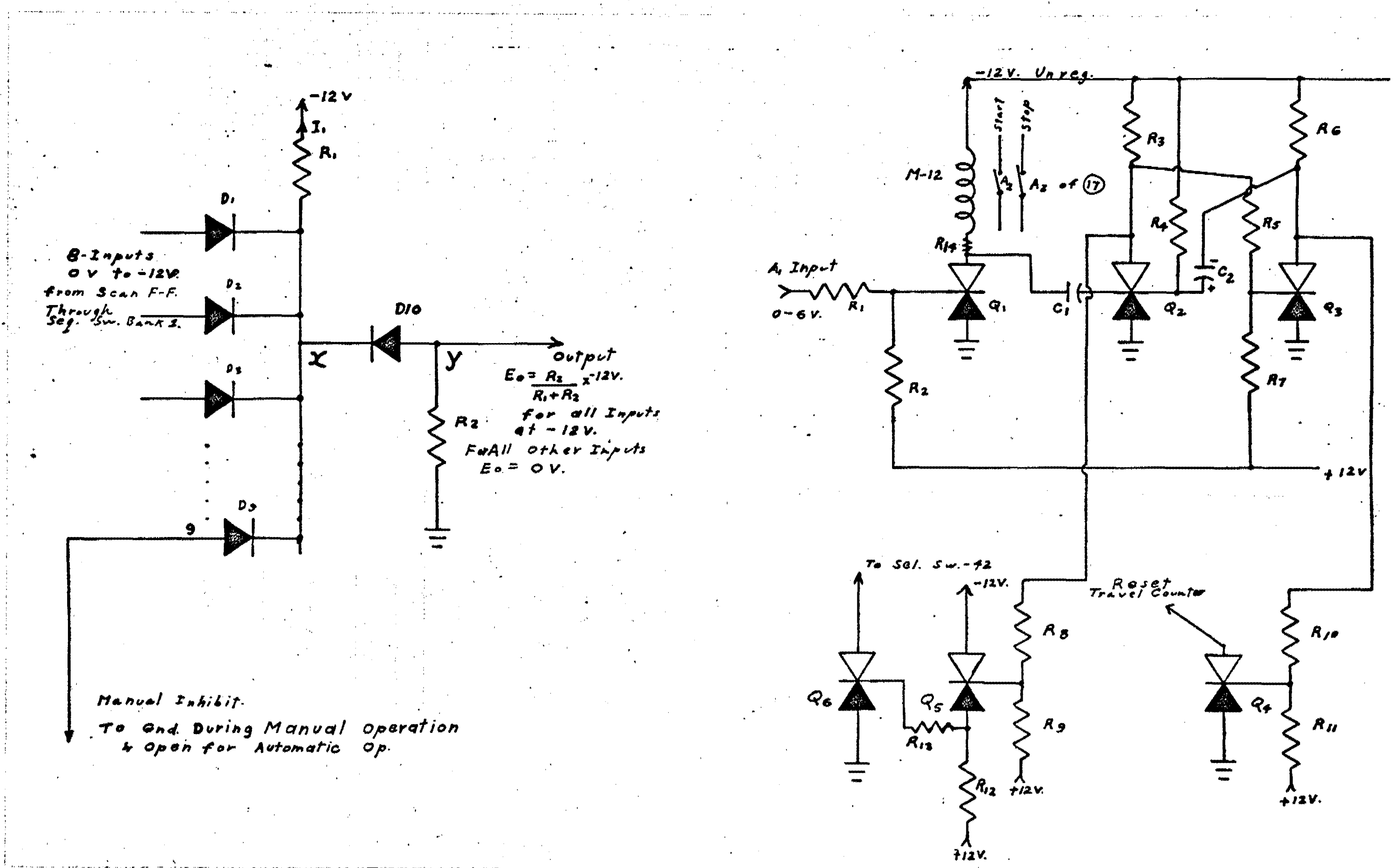
d) reset the travel counter so that it can advance the carriage to the next sample point.

The diode gate shown in Figure 13 is a standard circuit. So long as one of the inputs is at ground potential, the associated diode (D 1-8) will conduct due to the current drawn up through R_1 to the negative supply, and point "x" will be clamped close to ground.

Diode D_{10} is included to balance out the effect of the voltage drop across the input diodes. Diode D_{10} also conducts and has approximately the same voltage drop as the input diodes, therefore the voltage at point "y" - the output, will be less negative than at point "x" and will be virtually the same as the input voltage.

When all of the inputs are either open circuited or else negative (- 12v.) the input diodes no longer conduct, and the total current drawn by resistor R_1 is supplied through R_2 and D_{10}. If the diode voltage drop is neglected, the output voltage is half of the negative supply voltage. Thus when all inputs are either open or negative (scanned condition) the gate output falls from zero to -6 v. This voltage step is the gate output.

The gate output feeds a common emitter inverter (Q_1 of Figure 13) to isolate the A_1 gate from succeeding circuitry. The output of Q_1 drives a monostable multivibrator which, through buffers, drives the selector switch to position 1 and resets the travel drive circuitry. Also, the output controls gates A_2, A_3 of the digitizer logic.



Diode Gate

Pulse and Level Output

Fig. 13

SCANNED AND GATE --A_1

TRAVEL DRIVE:

The travel drive steps once, twice or four times corresponding to 1/4, 1/2, or 1 mm. of carriage travel. The travel drive logic is shown in Figure 14. It consists of a three stage binary counter which inhibits a gating circuit to stop further pulses getting to the counter and pulsing the travel driver. The drive pulses are generated by the continuously turning scanning cam-shaft via a synchronizing microswitch.

The relay gating circuit also inhibits the resetting of the scanning flip-flops while the carriage is travelling. This ensures that the curve is sampled only at the correct sampling points.

The circuit is self-latching once it has counted. It is started by resetting the counters and control circuit. The reset is done either by the reset pulse from "and" gate A_1 or by means of a manual travel push switch.

The driving waveform is a negative going square wave. During the negative pulse the solenoid relay is activated, but the counter is driven by the positive-going trailing edge of the pulse. This has the effect that the counter stages count the just performed mechanical step. After the preset number of steps have occurred, the relay gate is inhibited during the grounded portion of the input waveform. Thus no more pulses pass to the travel driver and it is quiescent until again reset.

To conserve time, the carriage travels during the readout phase.

The carriage drive is made up of a half nut on the carriage riding on a precision lathe screw running the length of the machine. The drive pulses control an air solenoid driving a sprocket attached to one end of the screw. The screw is rotated a small angle by each drive pulse, advancing the carriage in 1/4 mm. steps.

MANUAL/AUTOMATIC SWITCH:

This master switch is used when starting the machine. It forces the gating circuits in the logic into the finished readout condition when at "Manual". Then the machine can be put into the scanning mode by turning the switch to "Operate" or "Single Operate". The circuitry is shown in Figure 15.

In the manual and single operate state, the channel is chosen by the manual channel selector switch.

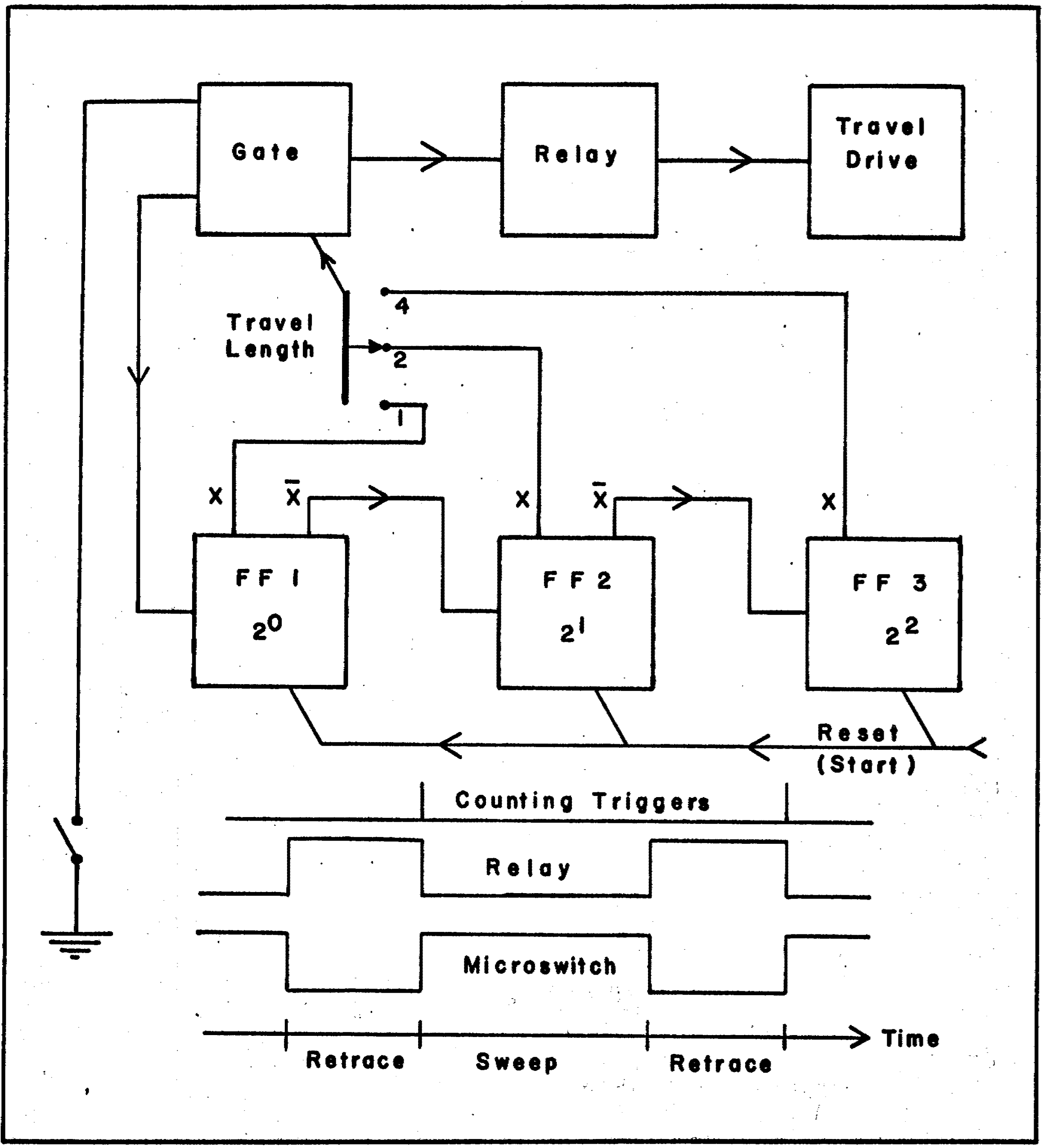


Fig. 14

TRAVEL DRIVE LOGIC

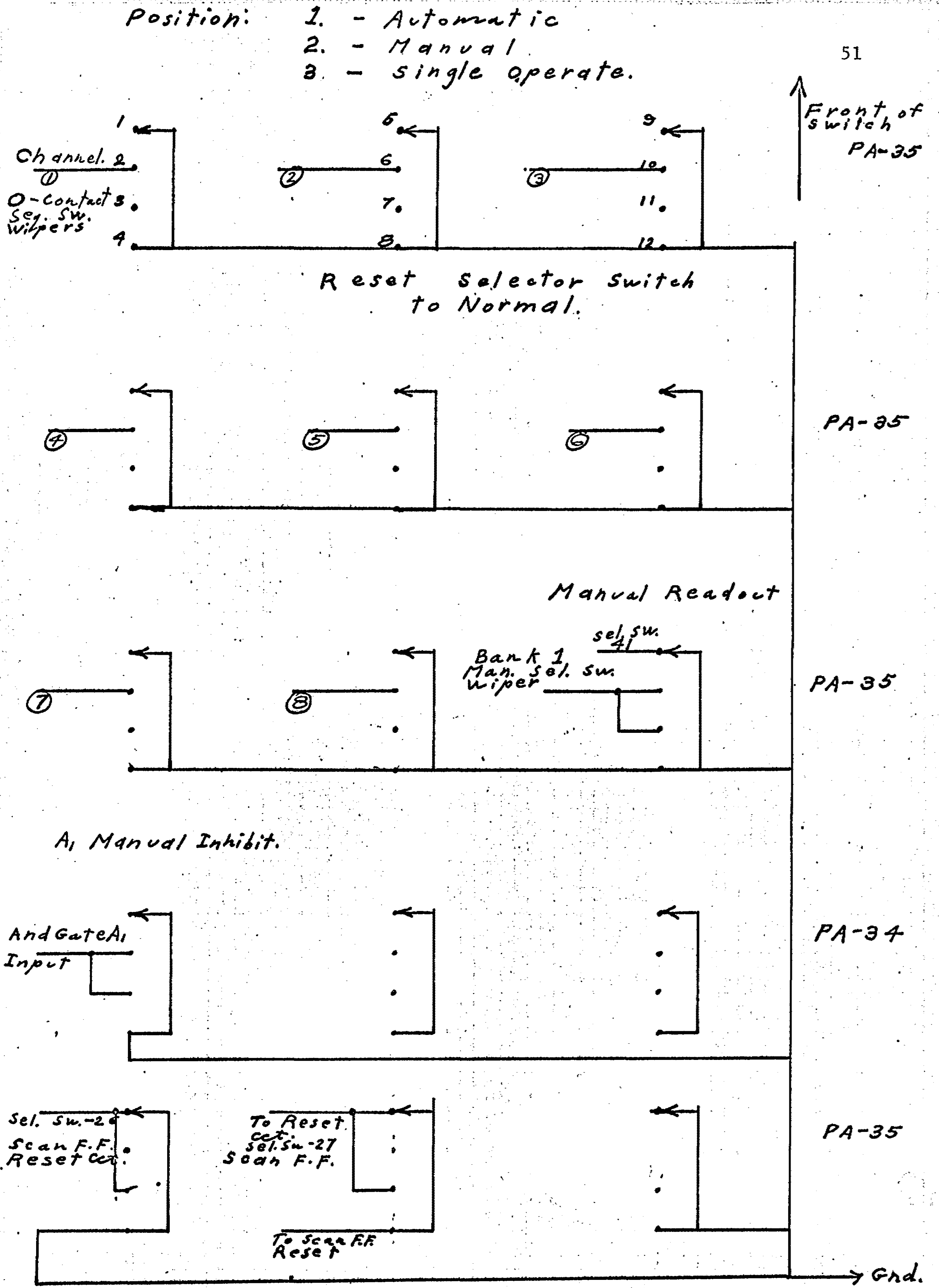


Fig. 15
MANUAL / AUTOMATIC SWITCH

CHAPTER VI

RESULTS AND CONCLUSIONS

Accuracy and Reproducibility:

The apparatus operates within the desired range of accuracy of ± 1 count in 200.

A test for reproducibility was performed by disconnecting the air supply to the travel drive mechanism. Thus the machine operated normally except that the carriage did not travel. The punched out numbers were all within one count of the mean for each channel. Thus for a single position, the reproducibility is within the inherent errors of the digitizing process.

Additional performance tests were: scanning straight lines parallel to the baseline and at an angle of fo~~u~~rty-five degrees. The lines were reproduced with an error of the thickness of the line (approx. 1/4 mm). Reproductions of recorded sine waves were also within the line width when the mechanical scanner was set correctly. For most scans, however the sine wave exhibited less than 5% even order distortion. The reasons for this are discussed in Appendix A-1. An additional source of uncertainty was the recorder used to record the sine waves.

Considering only the straight line tests (thus having a near-perfect graphical signal) the errors are only about one quarter mm. In a total scan width of fifty mm. this represents an error of one part in two hundred. The apparatus then meets the specifications for accuracy.

Conversion Time:

As stated in the discussion on the logic section, delay circuits were inserted as required to insure synchronization of the different circuit functions. This reduced the operating speed of the apparatus from that of the original design.

The average conversion time for all eight channels to be scanned, digitized, and punched out is 7.1 seconds. This time is mainly due to the delays necessary for synchronization and could be reduced by optimizing the delay times. The punching time for each data channel is approximately 250 milliseconds, the digitization time is about 50 milliseconds. If these were the only times involved, the conversion time would be about 300-400 milliseconds. Since the actual conversion time is 887 milliseconds per channel the effect of the synchronizing delays is evident. The effect of the delays is even greater when only a single channel is being converted - the average conversion time then is 1.66 seconds.

The actual conversion time then is twice the minimum time required by the punch and digitizer combination. Proper selection of certain logical delays would reduce this time from 887 milliseconds to about 650 milliseconds. Incorporation of parallel binary memory stages to permit simultaneous digitization and punch out would reduce the conversion time to about 200 milliseconds per channel.

While the conversion speed was reduced by the adoption of the non-synchronous mode of operation, the tape data format was used as designed. Thus even though the apparatus did not operate as rapidly as desired, the data handling was speeded up due to the direct data loading to the computer.

The non-synchronous mode of operation also produced a great deal of trouble in setting-up and trouble-shooting the apparatus. Due to the large number of different possible time-combinations, days were spent finding the troublesome combinations. Circuit delays were then inserted to ensure proper gating of the different machine functions.

At the conclusion of the project, the initial specifications were re-examined and found to be quite insufficient - in particular the condition of lowest component cost. This condition led to circuits composed of both relay and semiconductor type logic. Also the polarity convention for gating signals (positive gate or negative gate) was inverted as necessary for lowest component count. This mixing of types of logic, while it produced a low component cost, made trouble-shooting and design difficult. The difficulty arose because of the necessity of trying to remember whether a voltage level represented an enabling or an inhibiting signal. Afterwards, it was decided that a common type of logic circuitry, even though it would require additinal inverters, etc., would be worthwhile in terms of the time saved.

An indirect result was that the saving of components was made up for in the extra time required. The net cost of the apparatus would have been the same if more conventional circuit design had been used with a consequently larger component cost.

Conclusions:

The apparatus performs at the rate of 1.1 conversions per second within a usual error of 1/2 percent. As expected, a few random errors of larger amplitude do occur mainly due to the malfunction of the electrologic DVM used in the digitizer. The machine logic and electronic circuitry perform as designed. The speed of operation can be improved by minor circuit changes.

Improvements to the machine could be effected by:

a) returning to a clocked mode of operation.

b) changing the scanning method so that the photocells do not move.

c) performing the digitization directly during the scan rather than going through the multi-step procedure.

APPENDIX

APPENDIX A - 1

Opto-Mechano-Electronic Scanner

Operating Description:

The scanning mechanism is basically the same as that described in Reference 5. The mechanism is illustrated in Figure 1.

Consider the operation of one channel: The scanning potentiometer and the photocell are mechanically coupled. As the photocell sweeps across the record, the potentiometer wiper generates a voltage proportional to the swept angle. This voltage is led to the storage capacitor (Figure 16) through the scanning relays which are held closed by the scanning flip-flops.

When the photocell crosses the inkline, a pulse is generated which triggers the scanning flip-flops and opens the scanning relays. The capacitor then retains the voltage of the potentiometer wiper at the instant of the pulse from the inkline. The stored voltage on the capacitor is proportional to the position of the inkline for that sample instant.

All channels operate in the same manner. The capacitors serve as a'memory' - holding the voltage until they are individually and sequentially attached to the common readout line by the readout relays. Thus sampling is done in parallel and readout in serial fashion.

The difficulty with this scanning method lies with the mechanical arrangement. It is extremely difficult to set the mechanical scanner to reproduce the curvilinear writing path of the recording pen. Any misalignment causes distortion of the signal. This is equivalent to a mapping of the record into another plane through a curved line, but plotting the data on a linear grid.

A further difficulty is the trouble involved in sensing the middle of the line. With the inks and recording pens presently in use, a signal to noise ratio of two to three is all that can be expected. The paper density is quite non-homogeneous and the inks are translucent. The present sensing system functions by transillumination. A system based on reflection was tried but gave even lower signal to noise ratios. The ink apparently dries with a shiny surface which reflects almost as well as the paper. Use of a proper ink increases S/N ratio to 10:0 or even 50:1.

This scanning method then, requires setting of the pulse amplifier sensitivity for each channel. The setting depends on the density of the inkline, the paper roughness etc. If these conditions vary, the sensitivity must be changed accordingly.

Design Considerations:

The electrical requirements of the scanner are accuracy within 1/4 to 1/2%. The design considerations were:

a) time delay of the relays. This should be as low as possible.

b) leakage of charge from the storage capacitors during the memory period and also dielectric storage effects in the capacitors.

c) loading effect of the voltmeter.

d) time distortion of the sweep voltage due to the RC time constant of the sweep bridge circuit.

e) loading error of the capacitor charging current on the potentiometer.

This effect is non-linear due to the changing resistance of the bridge circuit.

The value of capacitor chosen is a compromise between factors b, c, d and e. A larger value minimizes error due to b and c while a smaller value of capacitance minimizes errors due to factors d and e. Cost is also a factor since larger value capacitors cost more. While the charging time constant can be made small by choosing the bridge resistors small, this means a larger current drain on the power supply and heating of the scanning potentiometers.

The different factors were resolved as follows:

Capacitors with a polystyrene dielectric were chosen to reduce the effect of dielectric storage to a negligible value. These capacitors were of a hermetrically sealed construction to reduce changes in characteristics. The capacitor and associated reed relays were encapsulated in epoxy resin to do away with the effects of ambient humidity. Without this provision, leakage is a real problem under humid conditions.

Reed relays were chosen because of; their glass to metal seal which made them convenient for potting, their ease of use, and very fast break time without appreciable bounce. The break time of the relays used was of the order of 0.2 ms. Including the time constant of the coil, the total delay could be kept much less than .3 ms. In a useful sweep time of 100 ms. this constant delay is small and is compensated for in the initial setting-up. The only effect of the delay is to act as a shift in the base line. This is compensated for by setting zero under dynamic (scanning) conditions. The leakage resistance of this type of construction should be of the order of the reed relay leakage (5×10^{14} - ohms). This effectively does away with all errors due to leakage.

The resistances of the bridge circuit were chosen as shown in Figure 16. They are a compromise between power drain and heating, capacitor effects, life expectancy etc. To some extent the final choice was somewhat arbitrary (design based upon "engineering judgment"!). The bridge circuit is designed so that the sweep potentiometer is the largest resistance. With a final choice of a 0.1 mfd. capacitor, the maximum charging time constant was approximately:

$$5 \times 10^3 \times .1 \times 10^{-6} = .5 \text{ ms.}$$

which is much less than the sweep time of 100 ms. Thus there is not appreciable phase distortion of the sweep voltage.

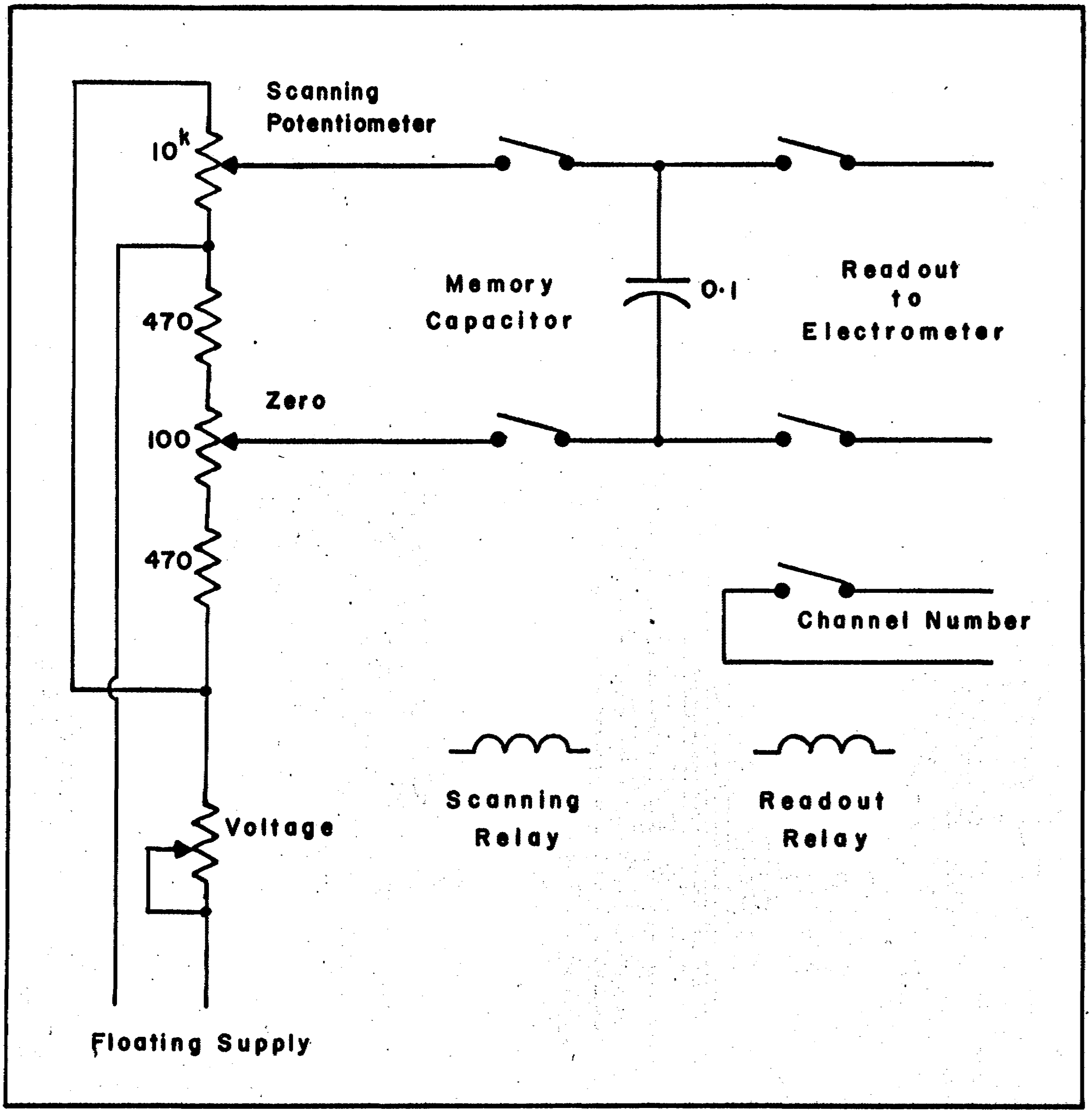


Fig. 16

Scanner-Sweep Circuitry

The limiting factors in the choice of capacitor value were the loading effect of the electrometer(A2,)and the charging current loading on the sweep potentiometer. The 0.1 mf. chosen allows a comfortable margin for both factors.

i.e. for a steady potentiometer drain of 1/2 ma. the charging current should be less than .050 ma.

charging current:

$$I \cong \frac{V}{t} \times C$$

$$\text{for } \frac{V}{t} = \frac{5V.}{100 \text{ ms.}}$$

$$I \cong \frac{5 \times .1}{100 \times 10^{-3}} \times 10^{-6}$$

$$= .5 \times 10^{-6+1}$$

$$= 5 \mu a \text{ which is less than .05 ma.}$$

An electrometer amplifier (Appendix 3) is used as a buffer between the memory capacitor and the digitizer. The droop during even five seconds of readout would be only about 0.2% (see Figure 19).

Since the normal readout will take place in less than a second, negligible error is introduced.

The bridge power supply was zener diode regulated and derived from a winding on a 1% regulating transformer. This gave a simple, floating supply voltage with adequate stability.

The supply must be floating in order to allow the electrometer and digitizer to have one side grounded. During set-up, one corner of the scanning bridge is connected to ground through the electrometer and DVM and the supply must therefore float.

Optical Scanner:

The optical scanner heads are shown in Figure 1. The sensing cell is a cadmium selenide photoconductive cell (Clairex CL 604L). This type of cell is very sensitive and has fast enough response under the high light levels used.

The pin holes are in the scanning heads empirically selected to give adequate sensitivity.

The scanning heads are driven from a cam and follower arrangement to convert rotary to linear motion and then angular motion of the scanning head.

Scanning Potentiometers:

The scanning potentiometers are subjected to a very great number of cycles of revolution. If the scan is set for only a small arc, this leads to a great deal of localized wear.

Initially, wire wound servo type potentiometers were used but these rapidly wore out. Their life of a million cycles only lasted about nine months. This is a direct result of the continuous sweeping method adopted. Most of the sweep cycles are not used for scanning. If sweeping was done only for scanning as had originally been envisaged, the potentiometer life would have been adequate.

Carbon film type potentiometers were then chosen and have been in use for the past year. These potentiometers should have a useful life of ten million cycles.

The angle scanned by the photo-head is multiplied by a gear system to drive the potentiometer over a wider angle. This provides better resolution of the sweep voltage.

Pulse Amplifier and Photoconductive Cell:

The amplifier Figure 17, is a conservative design embodying a large amount of negative feed-back to stabilize gain and DC bias conditions. It consists of a common-emitter stage followed by a common-collector stage for low output resistance. Shunt feed-back is applied around the pair to provide low input and output resistance. The series input resistor is variable and serves as the gain control. In operation, the gain is turned up until the flip-flop triggers reliably.

The photoconductive cell is of cadmium selenide (Clairex CL 604L). This type of cell is extremely sensitive-being a hundred times more sensitive than the silicon photovoltaic types previously used.

The bias conditions for the cell were determined empirically under the actual conditions of use. The signal pulse from the photocell is of the order of 50-100 mv.

The only difficulty experienced with this type of cell is that the scanning mechanism seems to provide enough vibration to damage the cell. Several have failed during operation due to this cause.

The output from the amplifier is a positive-going pulse of maximum amplitude 12 v.

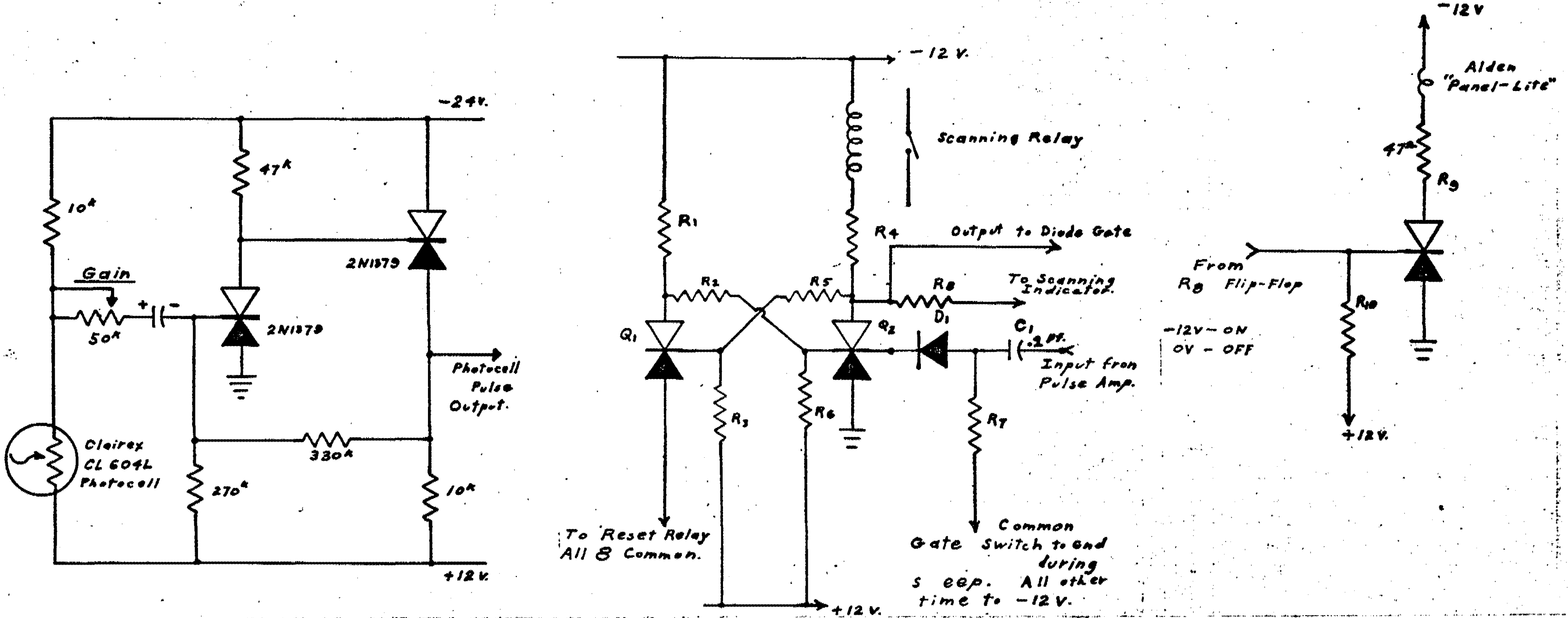
Scanning Flip-Flops:

Transistor bistable circuits or flip-flops, are used to control the scanning relays. They are used to control and also to "remember" the scanning state.

The scanning flip-flops(Figure 21)use a basic bistable circuit. This basic circuit is used throughout the converter in several forms (see Appendix 4).

The flip-flops are reset by the logic just before the scan phase. This is done by momentarily opening the emitter circuit of transistors Q_1. This forces transistors Q_2 to conduct and puts the flip-flop in the zero state.

The input to the scanning F.F. is fed through the biased gate consisting of C_1, D_1 & R_7. This gate serves several purposes.



Photocell and Pulse Amplifier Scanning Flip-Flop Scanned Indicator

Fig. 17
SCANNER ELECTRONIC CIRCUITRY

a) The signals from the pulse amplifier are gated by the logic circuitry so that pulses can reach the flip-flops only during the scan period and not during the retrace. This is necessary in order to do away with the effects of sloppiness in the mechanical scanner and possible movement of the paper record. This is done by connecting the end of R_7 Figure 17 to -12 v. except during the scan period when it is at zero volts.

b) The 0. 1mfd. capacitor (C_1) differentiates the pulse from the pulse amplifier. This provides a truer approximation to sensing the middle of the line. The size is a compromise between the differentiation effect and triggering sensitivity.

c) During the scan, R_7 can be returned to a preset bias to act as a threshold control. This would get rid of the effect of a great deal of the small-amplitude or lower frequency "noise" in the photocell signal if necessary.

Scanning Relays:

The reed relay coils are directly in the collector circuits of transistors Q_2. This is done to cut down on parts. The scheme has the disadvantage that the flip-flop is badly unbalanced and greater care had to be taken in its design. An easier design would be a balanced flip-flop feeding a driver transistor.

The relay coil current is chosen for a minimum value that will allow reliable operation. This technique gives the fastest relay response and lightest duty for the driver transistor. The driver transistor is chosen for high collector-emitter cut-off voltage (VCE). When collector current is switched off rapidly, the relay coil self-induced voltage adds to the supply voltage and can actually cause a momentary collector to emitter breakdown. This is allowable as long as the transistor power dissipation is quite limited.

Scanned Indicator:

Small indicator lamps (Alden-Panel-Lites) are driven by a single transistor and serve to indicate that the corresponding channel has scanned; i.e. its flip-flop has been triggered to the "OFF" state. The transistor is used as a simple switch-current driven in the "ON" state and voltage biased in the "OFF" state.

Scanned Output:

The scanning flip-flop drives an inverter which provides isolation between the flip-flop and the scanned "and" gate (A_1). When all scanning flip-flops are "OFF", the "and" gate changes state and signals the end of the scanning cycle to the logic.

Scanning Errors

Mechanical Sweep:

The previous calculations have assumed a linear sweep velocity. The sweep is obtained from a cam which is cut so as to provide the following velocity pattern: sweep - pause - retrace - pause.

The middle portion of the sweep period is used for scanning.

Any non-linearity in the sweep velocity is introduced into the scan. This occurs mainly due to the fixed time lag of the scanning relays. While this time lag can be cancelled out if the sweep is linear, non-linearity of the sweep causes the effect of the lag to vary with the position of the inkline.

This source of error was recognized, but, since it was not part of the design has not been taken into account. Also, the mechanical design of the sweeping mechanism does not lend itself to analysis - the mechanical coupling method is variable and the sweep pattern can be altered at the whim of the operator.

The sweep method also has an inherent error due to the translation from linear to angular motion. Even though the reciprocating arm moves with a steady linear velocity, the angular motion varies as the inverse tangent of the displacement divided by the radius arm. This error could be corrected by curving the coupling so that the radius changes with the deflection.

The effect of this error is to produce a sigmoid shaped transfer characteristic (of position) for the scanner, thus introducing even-order distortion to the signal.

APPENDIX A - 2

Electrometer

The electrometer is a DC amplifier of very high gain stability and exceedingly low drift originally described by Scroggie[9]. The amplifier is basically a balanced differential input stage (V_1, V_2) feeding a pair of cathode followers (V_3, V_4) as output stage. The circuit is shown in Figure 18. Also shown is a measurement of input resistance. (Figure 19).

Negative feedback is applied from the output to the reference side of the differential amplifier, and the signal is applied from the common side of the output to the grid of the input tube. The signal is thus also inside the feedback loop, and sees a very high impedance. The static input resistance is made high by proper selection of tube type and operating point.

The input tube is selected to have high gain under low plate current operation. It should also preferably be a double tube to keep DC balance conditions. While pentodes give higher gain, and therefore slightly better performance, it was determined that triodes would give adequate performance and need a much simpler power supply. The type CK 5755 tube was chosen - this tube is made for DC amplifier service. This choice of tube proved satisfactory and has been in use for over two years. The output tube (a type 12 AU 7) was chosen on the basis of a high mutual conductance under the design conditions. This provides a low output impedance which is lowered still further by the 100% negative feedback.

With the operating point 9, 11, of the input tubes chosen for lowest grid current, the input impedance is of the order of $3 \times 10^{10}\Omega$. This was measured by rate of capacitor discharge (Figure 19). The tube operating point was empirically varied to obtain the highest, most stable input resistance. The filament voltage was reduced from normal to aid in attaining low grid current. When properly zeroed, the input resistance is stably greater than $10^{10}\Omega$. The output resistance is approximately $50\,\Omega$ or less.

The gain is slightly less than unity but since it is very stable this does not affect the system.

The power supply is floating to enable the common point between input and output to be grounded. This is necessary because the digitizer has a single ended input.

The power supply is a simple VR tube type run from a sola regulating transformer. The transformer provides 1% regulation for plate and filament voltages and allows sufficient isolation to float the supply. Another winding on the regulating transformer supplies power for a simple transistor regulator as a floating supply for the scanning bridge circuit.

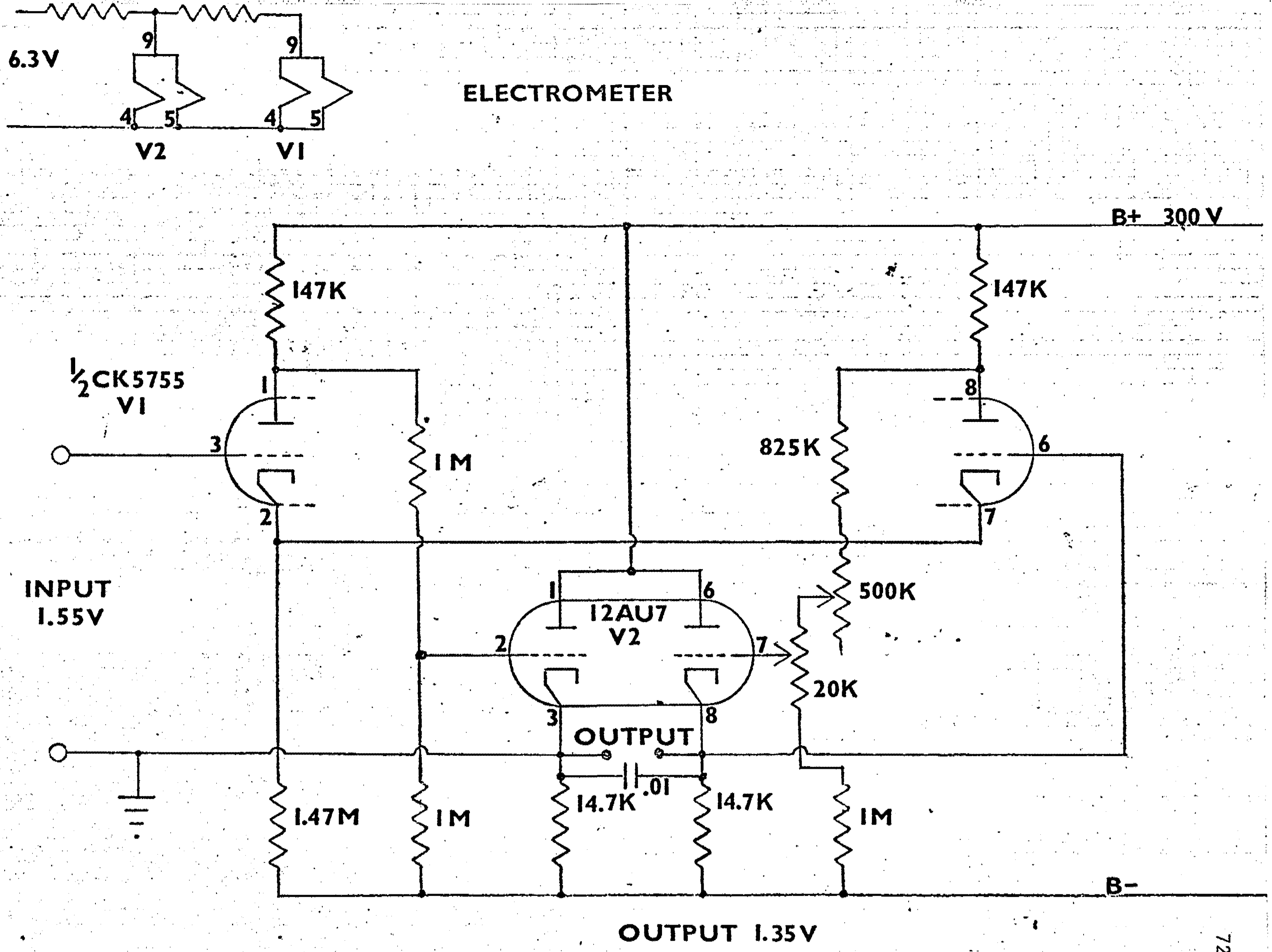
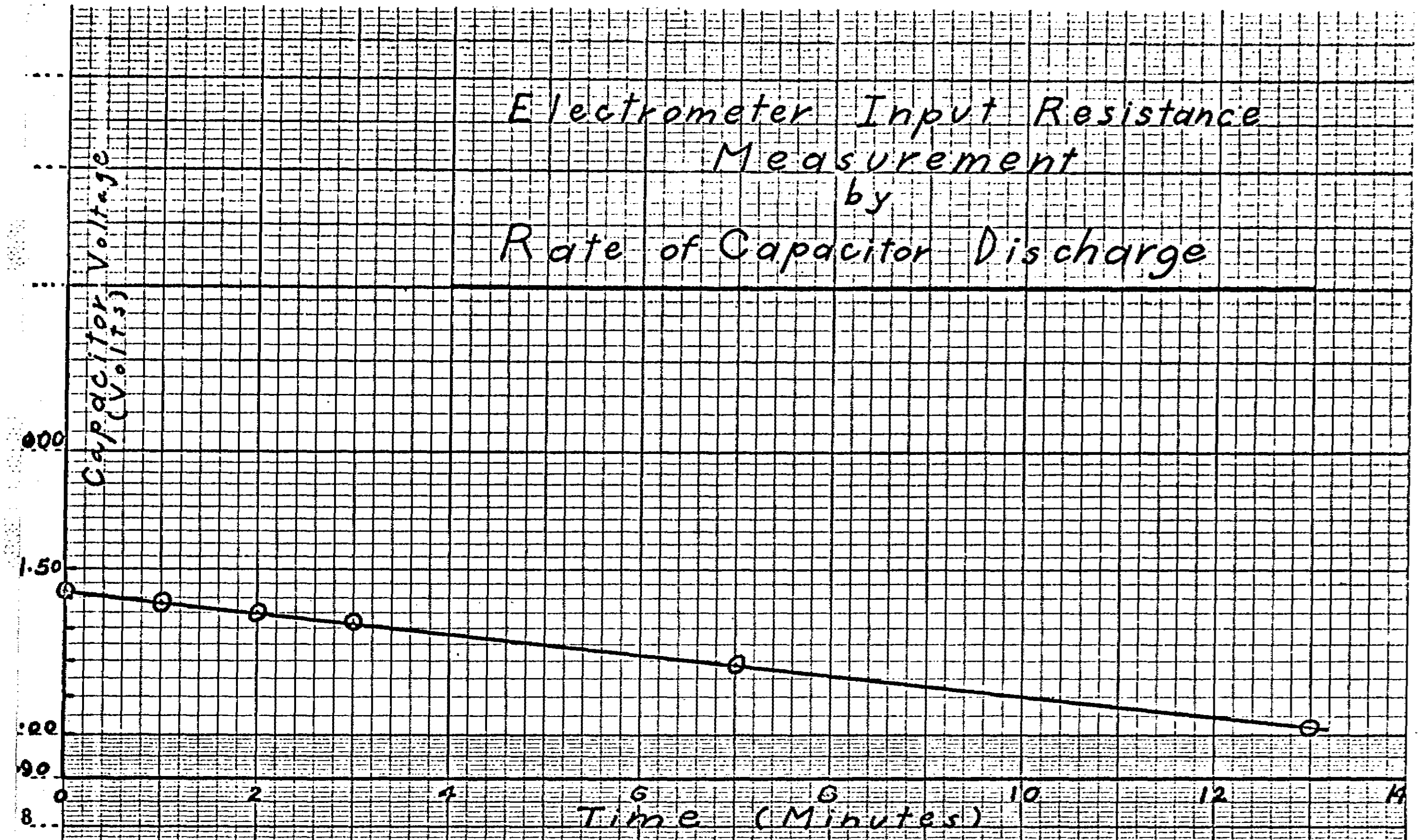


Fig. 18
ELECTROMETER CIRCUIT



Resistance:

$$\Delta V = \frac{It}{C} \cong \frac{E_0}{R} \times \frac{t}{C}$$

Then $R \cong \frac{t}{C} \times \frac{E_0}{\Delta V}$

for $t = 5$ Minutes $= 300$ Seconds $\cong \frac{300}{0.1} \times \frac{1.42}{0.17} \times 10^6$

$E_0 = 1.42$ V.

$\Delta V = 0.17$ V.

$C = 0.1\ \mu f.$

$$\underline{\cong 2.5 \times 10^{10}\ \Omega}$$

Fig. 19
ELECTROMETER INPUT RESISTANCE

APPENDIX A - 3

Transistor Circuit Design

The multivibrator circuits used throughout the apparatus are versions of the simple, saturated, two-transistor collector to base coupled circuit[10].

The general circuit is shown in Figures 20 and 21. The design is governed by the choice of collector loads. Once the collector loads are fixed, the coupling circuits are also determined. That is, for the "ON" condition, with I_c fixed:

$$I_b \text{ min.} \geq \frac{I_c}{\beta \text{ Min.}}$$

and the coupling resistor is chosen to drive at least I_b min. into the base.

For the "OFF" condition, the base must be back-biased by the voltage divider action. For stability, the bleed current in the voltage divider should be greater than the maximum expected I_{co}.

Inverter design follows the same philosophy. The design procedure is simple, and since only moderate speeds are required, proves quite adequate.

Coupling and triggering circuits are also designed for worst case conditions where pulse specifications are known.

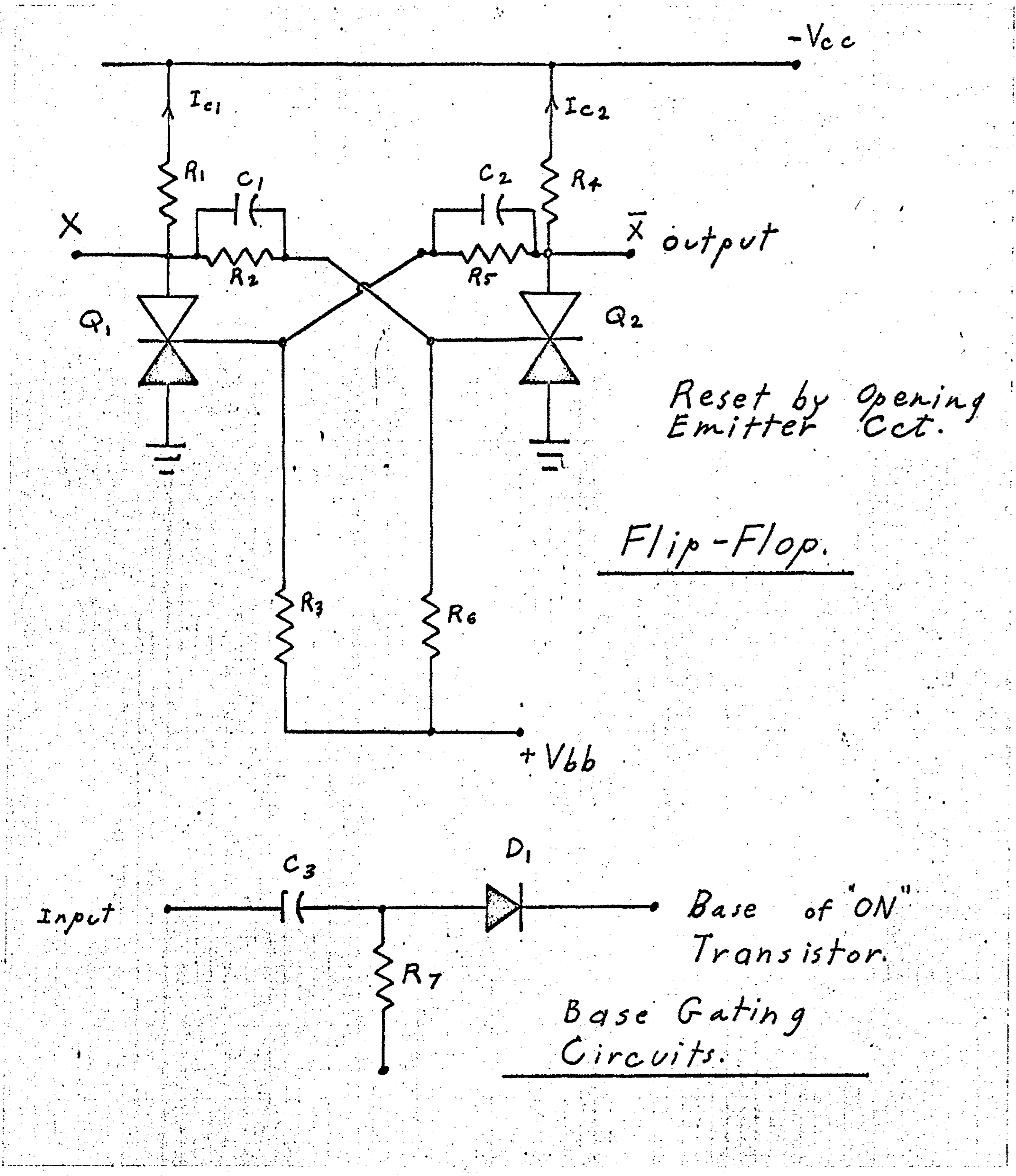


Fig. 20
GENERAL FLIP- FLOP CIRCUIT

A sample design of the scanning flip-flops shows the design method.

The scanning relay has a resistance of 175 ohms and requires at least 25 ma. of current. The added series resistance is 120 ohms making a total collector load of 395 ohms.

Thus the actual collector current is $\frac{12}{395} = 30$ ma.

The inductive kick of the coil is of the order of 20 volts requiring the transistor to have a V_{CER} rating of -35 v. The Motorola 2N1193 transistor is chosen for Q_2.

Then for saturation:

$$I_b \geq \frac{I_c}{\beta \text{ min.}}$$

$$\text{for } \beta \text{ min.} = 50$$

$$I_b \geq \frac{30 \text{ ma.}}{50}$$

$$\geq 0.6 \text{ ma.}$$

Now the collector load for the opposite transistor (Q_1) is chosen as 2.7 K to give a collector current of about 5 ma. The transistor chosen for this position is the 2N1374.

Then for Q_2 saturated:

$$I_b \geq 0.6 \text{ ma.} \geqq \frac{12 \text{ v.}}{2.7+10\text{K}}$$

$$= \frac{12}{12.7} = 1 \text{ ma.}$$

and a choice of coupling resistor of 10K is satisfactory. If 10K is satisfactory for the "ON" state of Q_2 it will also satisfy the "ON" requirements of Q_1.

For the "OFF" state we require a reverse bias of approximately two and a half volts. This level of reverse bias ensures stability against false triggering in the "OFF" state, and is less than the safe rating for the transistors.

For the condition of 2.5 v. reverse bias:

$$\frac{2.5 \text{ v.}}{10\text{K}} = \frac{10 \text{ v.}}{\text{R}}$$

$$\text{R} = \frac{10 \text{ v.}}{2.5 \text{ v.}} \times 10\text{k}$$

$$= 40\text{k}$$

$$\text{or} \quad 43\text{k chosen value.}$$

The bleeder current is then $\frac{12 \text{ v.}}{53\text{k}} = 250\ \mu\text{a.}$

Since the maximum I_{cbo} will only be of the order of $50\ \mu$a., this bleeder current assures reverse bias up to the maximum temperature limits.

The value of the 43k resistor must also be checked to insure that current drawn from the coupling resistor in the "ON" state is not excessive.

i.e. drive current through $R_2 = -1$ ma.

drain through $R_6 = +.3$ ma.

therefore, $I_b = -0.6$ ma.

For the assumed collector currents, output loads up to several milliamperes may also be drawn through coupling resistors.

Triggering:

To trigger Q_2 to the "OFF" state, we will assume that 1/2 ma. of current is required. This is a slightly pessimistic approach. If the trigger pulse is to be of 6 v. amplitude and have a rise time of about 1 ms. or less, then to a first approximation:

$$C_1 \geqq i \quad x \quad \frac{t}{\Delta v.}$$

$$\geqq \frac{0.5 \quad x \quad .1 \quad x10^{-6}}{6}$$

$$\geqq 0.08 \text{ mfd.}$$

i.e. 0.1 mfd. chosen

This simplified design procedure embodies the characteristics of more formal methods which require calculation of loop gains, and stability factors. By making the appropriate assumptions at the beginnings of the worst case design (min. β , max. I_{co}, etc.) safety factors, component tolerances, and temperature effects are included. The method does not necessarily realize an optimum design, but does assure an operable circuit.

A great deal of design information was taken from Reference 10, concerning the triggering and operation of flip-flops.

Base Gating Circuits:

The capacitor-resistor-diode gates used with the flip-flops (Figure 20) are used for pulse steering and logical control of pulse or step inputs applied to the capacitors. The resistor is used to set the D.C. level of the junction point. Then the signal pulse will pass through the diode if it is more positive than the voltage bias set by the resistor. Thus the gate is inhibited by connecting the resistor to a negative voltage or enabled by grounding the resistor.

The time constant of the capacitor resistor combination must be short enough to permit full charging of the capacitor between input pulses. Otherwise the time constant can be chosen to pass the input pulse or differentiate it remembering that the transistor base input resistance is very low initially and then increases as the transistor turns off.

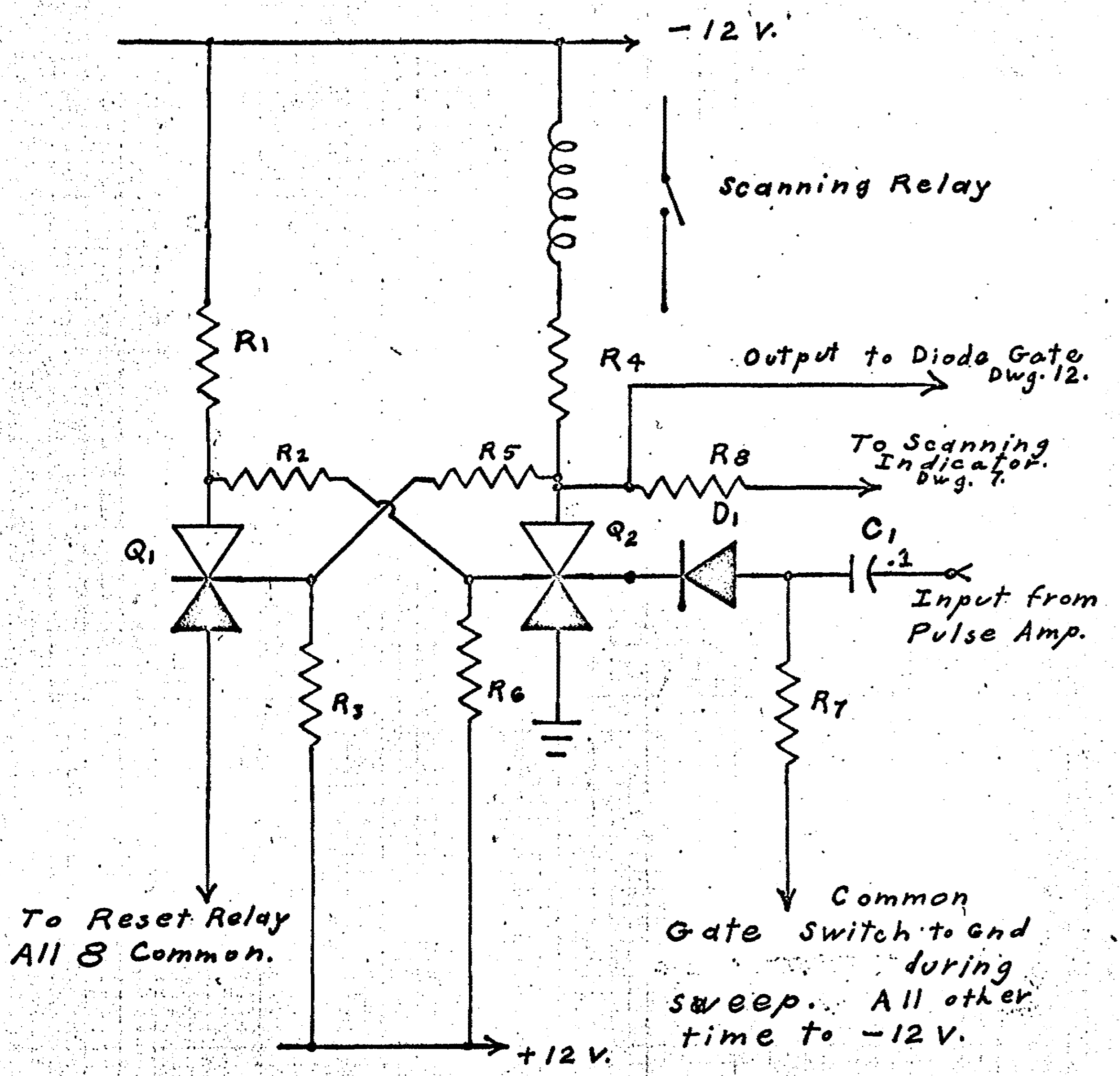
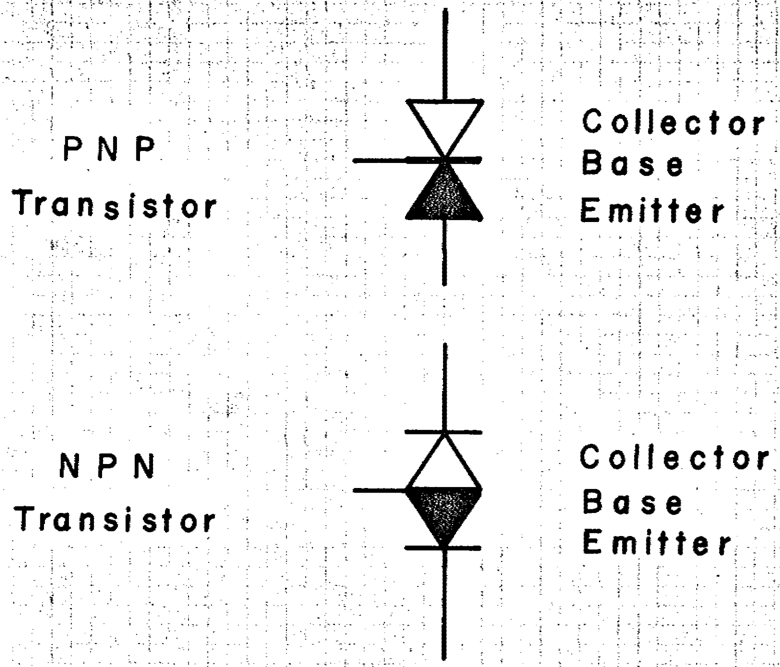


Fig. 21
SCANNING FLIP-FLOP

SYMBOLOGY



NRC Transistor Symbols

FIG. 22

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