Modular Multilevel Converters with Partially Integrated Battery Energy Storage

by

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Abstract

This thesis investigates Modular Multilevel Converters (MMCs) with partially integrated Battery Energy Storage Systems (BESS), where only a subset of sub-modules (SMs) are equipped with battery energy storage via bidirectional boost converters. The primary goal of incorporating BESS is to provide inertial and frequency support to the grid. These converters are typically studied using Electromagnetic Transient (EMT) simulations. A continuous-time model of the MMC-BESS is developed based on the state-space equations of the converter. The proposed model enhances computational efficiency in two key ways: (i) it significantly reduces the number of nodes in the conventional switching model, thereby shrinking the size of its admittance matrix, and (ii) it avoids computationally expensive re-triangularization of the admittance matrix during normal operation, restricting it to rare instances of converter blocking. This method results in substantial reductions in the simulation time of MMC circuits, making it particularly useful for studies requiring repetitive simulations. The computational efficiency and accuracy of the proposed model are validated by comparing its implementation in the PSCAD/EMTDC simulator against conventional detailed switching models and experimental measurements from a single-phase scaled-down laboratory setup. The Peak Current Mode (PCM) control strategy is used to manage the DC-DC converters integrating the batteries with the MMC. PCM provides a protective layer that limits the current through the battery and DC-DC converters' switches. An Averaged Value Model (AVM)

of the MMC-BESS, along with its per-unit representation, is also derived. The AVM is beneficial for low-frequency studies, such as upstream control design and SM capacitor sizing. Finally, the proposed topology and its model are used to explore replacing Manitoba's outdated Bipole I HVDC system with a VSC-HVDC system featuring MMC and MMC-BESS at the rectifier and inverter terminals, respectively. The study aims to stabilize and maintain system frequency while eliminating synchronous condensers and AC line filters.

Copyright Notes

- Parts of the contents of Chapter 2 and 3 are published in the following papers.
  - R. Parvari; S. Filizadeh; I. Fernando, ”Detailed Equivalent Modeling and Simulation of Modular Multilevel Converters with Partially-Integrated Battery Energy Storage,” *Journal of Modern Power Systems and Clean Energy*, 2024.
  - R. Parvari; S. Filizadeh; D. Muthumuni, ”An Accelerated Detailed Equivalent Model for Modular Multilevel Converters,” *Electric Power Systems Research*, 2023.
- Chapter 5 is reprinted from the following paper that is submitted to *2024 CIGRE Canada Conference & Exhibition*. This paper has been accepted and was presented at the conference.
  - R. Parvari; S. Filizadeh; I. Fernando, ”Exploring the Potential of Grid-Assisting MMCs with BESS in Manitoba’s Power Infrastructure,” submitted to *2024 CIGRE Canada Conference & Exhibition.*

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To Mina

Table of Contents

List of Tables

List of Figures

List of Acronyms

HVDC	High Voltage Direct Current
VSC	Voltage Source Converter
MMC	Modular Multilevel Converter
BESS	Battery Energy Storage System
SM	Sub-Module
HBSM	Half-Bridge SM
FBSM	Full-Bridge SM
CONV	Conventional
EMT	Electromagnetic Transient
DEM	Detailed Equivalent Model
DSM	Detailed Switching Model
AVM	Average Value Model
PTP	Pole-to-Pole

PCM	Peak Current Mode
NLC	Nearest Level Control
RoCoF	Rate of Change of Frequency
pu	Per Unit

Symbols

x	a scaler quantity
$\vec{\mathbf{x}}$	a vector quantity
$\mathbf{X}$	a matrix quantity
$\odot$	Hadamard or element-wise product
$\oslash$	Hadamard or element-wise division
$\cdot$	dot (inner) product
j	imaginary unit
$\langle x(t) \rangle_{T_\mathrm{s}}$	average of the signal $x(t)$ over the period of T_s
$\mathbf{T}\{\}$	abc to dq0 transformation
$\mathbf{T}^{-1}\{\}$	dq0 to abc transformation

Chapter 1

Introduction

1.1 Literature Review

1.1.1 Low Inertia and Solutions

Inertia, i.e., the tendency of an object to remain in its present state of motion, has been adopted to power system analysis wherein it refers to the kinetic energy stored in the large rotating masses of synchronously-interconnected machines. This stored energy plays a vital role in maintaining grid frequency following contingency events in which a power plant is lost or a transmission line fails. Subsequently, the grid frequency, the manifestation of the synchronous speed, starts to deviate from its nominal value as a result of the imbalance between supply and demand. Historically, the major source of inertia has been constituted by the kinetic energy stored in rotating masses within the generators that are powered by fossil fuel, nuclear, or hydro power. With increasing penetration levels of Inverter-Based Resources (IBRs), however, questions have emerged about the frequency stability and, thus, the reliability of power systems. Photovoltaic (PV) and wind resources, as the most promising IBRs for electricity generation [1–3], do not provide inertia because they do not in-

herently possess a rotating mass and/or they are decoupled from the grid through power electronic converters [4]. Therefore, the effective inertia is diminished when conventional generation is replaced with IBRs [5–8]. There have been various solutions proposed to combat the consequences of low inertia in power systems, and they are explored as follows.

Synchronous Condensers (SCs): One of the most convenient and readily-available solutions is to augment additional inertia without exchanging the real power by deploying SCs. [9–12]. SCs are unloaded synchronous motors rotating freely and synchronously with the grid. The stored kinetic energy in the rotor of SCs can be used as source of inertia in frequency events. Considerable operating and capital costs, however, have hindered extensive use of SCs for inertia improvement [13].

Virtual Synchronous Machines (VSMs): With the replacement of Synchronous Generators (SGs) with IBR renewables, the intermediate power electronic converters have been investigated to be controlled in such a manner to mimic SGs. VSMs, proposed in [14, 15], are essentially inverters imitating electromechanical dynamics of SGs. So far, several models of VSMs with different control strategies have been introduced in the literature [16–22]. The core idea which is common in various studies is to realize VSMs by constructing both electrical and mechanical governing equations of the SG so that the well-known analyses in conventional power systems remain still valid.

DC-link Capacitors: DC-link capacitors are requisite components in almost all types of grid-connected converters. They have been reported to alleviate the Rate of Change of Frequency (RoCoF) and frequency nadir through inertia emulation [13, 23–26]. Even in Modular Multilevel Converters (MMCs) where the DC bus capacitor is eliminated, the aggregate stored energy in the

sub-module capacitors is a considerable potential for inertia emulation, as proposed by [27]. The central principle of this method is that the capacitor bears a close resemblance to the rotating mass in terms of stored energy. Specifically, the capacitance and voltage in capacitors are playing the same role as the momentum of inertia and angular frequency do in a rotating object, respectively.

Supercapacitors: Supercapacitors gain distinct advantages over conventional capacitors. They are efficient and have long lifetime, and more importantly, their power density is high [28]. When there is not enough inertial support coming from the DC-link capacitors, supercapacitors can be utilized to resolve the low-inertia issues by proportionally linking the grid frequency to the voltage of the supercapacitor, as discussed in [29, 30]. Supercapacitors were found to be capable of mitigating the impact of wind and solar generation on the dynamic performance of the French island of Guadeloupe grid in the case of a major generation outage [31]. Usually, they are connected to the DC-link capacitor through a bidirectional DC-DC converter to boost the voltage level to the required value. They have also been integrated with sub-module capacitors of MMC to enhance grid stability, as demonstrated in [**?**, Errigo2022] Supercapacitors have demerits of high cost and low specific energy [32].

Battery Energy Storage Systems (BESS): BESS are prevailing the market thanks to their low cost, high energy density and fast response [13, 28]. With regard to modern power systems, BESS have been at the focus of attention for the provision of services pertaining to inertial response and frequency support as discussed in [32–37]. For instance, in 2009, a 12 MW/4 MWh BESS was installed in northern Chile in order for offloading the primary frequency control obligation of a 277 MW thermal generation station [34, 38]. In [35] the application of BESS for frequency support in the isolated power system of Baja California Sur in Mexico is presented. In 2015, a 40 MW/20 MWh BESS was installed at the Sendai-Nishi substation in Japan to regulate frequency against

fluctuating generation output by wind power generation [39, 40]. Focusing on the frequency nadir and using a simple low order system frequency response, [36] examines the effect of BESS with droop control, used for primary frequency control on the power system of South Korea. Paper [37] reports various engineering experiences from several BESS projects including grid frequency regulation services. In [32], the system inertia is improved by properly controlling the power of BESS using the derivative of frequency deviation as a control signal. In contrast to capacitors and supercapacitors, batteries present nearly constant voltage which makes the voltage control, analogous to frequency control, impractical for frequency regulation. Instead, BESS's output power, which can be fully controlled, is used for inertia emulation. One possible solution is to relate the power reference to the Rate of Change of Frequency [13].

Following the prevailing trend in the use of energy storage systems for frequency support, this thesis is particularly aimed at studying the inclusion of BESS in MCCs. More often than not, a 2- or 3-level Voltage Source Converter (VSC) including 3-level T-type converter, Neutral Point Clamped (NPC) converter, Active Neutral Point Clamped (ANPC) converter, and flying capacitor converter are used to interface the BESS with the AC grid [41, 42]. In these typologies DC-DC converters may be placed between the battery and the grid-connected DC-AC converter to regulate the DC bus voltage [43–47]. It is worth mentioning that a bulky line-frequency transformer is required in all above-mentioned converter types for BESS integration to the grid. Thus, directly connected converters have been proposed to eliminate the need for line-frequency transformers [41, 42]. One solution is to use a conventional MMC whose DC terminal is tied to a series connection of batteries cells. Batteries are placed in series to gain high voltage thereby reducing the current stress in the semiconductors. However, connecting a large number of battery cells in series can reduce system reliability [48]. To address this problem, the whole series connection of batteries is distributed among sub-modules of the MMC which is discussed in detail in the following subsection.

1.1.2 Modular Multilevel Converters with BESS

MMCs are becoming the converter of choice for High Voltage Direct Current (HVDC) applications. In comparison to two- or three-level VSCs [49], MMCs have much better harmonic performance, show much less stress on the switches, and are inherently scalable [50, 51] – a property that makes adoption of the converter in high-voltage, high-power applications much more attainable. The output voltage waveform of an MMC is produced by adding up the voltages across each building block known as Sub-Module (SM). According to a sinusoidal reference, SMs are inserted and/or bypassed in order to achieve a low harmonic voltage waveform at the AC terminal. With increasing number of SMs, the quality of the output voltage improves while the frequency of switching each SM is reduced. Despite various types of SMs , Half-Bridge and Full-Bridge SMs (HBSM and FBSM) are presently the most common types owing to their cost-effectiveness and DC-fault-blocking capability, respectively [52].

Recently, MMCs with embedded energy storage systems have been explored to provide additional services, such as frequency response and black start capability, to existing MMC designs. For example, [53] proposes integrating energy storage systems into MMCs using parallel branches connected to the arm inductors. Experimental results from a low-voltage prototype of this topology are presented in [54]. Another approach to energy storage integration involves incorporating battery energy storage systems (BESS) into all sub-modules (SMs) via bi-directional DC-DC converters, as described in [55–58]. In these converters, each SM is augmented with a battery and a DC-DC converter that connects the battery to the SM capacitor. With this arrangement, the converter will be equipped with a large energy storage reservoir (the collection of batteries) that may be tapped into for large-scale energy transactions. This, however, might not be economical in HVDC applications where a considerable number of SMs are required while only a small fraction of the converter's capacity is required for frequency support [59, 60]. Hence, it is expected that the frequency support

will be at a fraction of converter's nominal power and, thereby, MMCs with partially embedded energy storages, in which only some SMs are integrated with BESS, are considered in this study. Even though [61] addresses the partial inclusion of BESS in MMCs for frequency support and ancillary service provision, it lacks detailed analysis of the BESS system, i.e., the interfacing DC-DC converter as well as the State of Charge (SoC) for batteries and their balancing.

1.1.3 Modeling and Simulation

Computer simulation models play vital rules in studies of MMCs. The model must accurately and efficiently exhibit the dynamics of the MMC under various conditions such as normal operation and faults. The most obvious model is the Detailed Switching Model (DSM) in which all elements of an MMC, e.g. IGBTs, diodes, and SM capacitors, are considered as separate electrical components. Due to the large number of SMs, this leads to a large admittance matrix that is changing with time according to the switching functions of IGBTs. In such a case, a large admittance matrix must be inverted every time a switching event occurs, which places a significant computational burden for electromagnetic transient-type (EMT-type) simulators. Thus DSMs are usually used for very specific applications or MMCs with a low number of SMs, e.g., as in [62]. To overcome the computational burden of the time-varying large admittance matrix, several equivalent models have been introduced.

The Averaged-Value Model (AVM) proposed in [63,64] is a popular model, which is preferable for low-frequency steady state analysis of MMCs in normal mode of operation. This model is suitable for system-level and controller design studies, e.g., for suppression of circulating currents as carried out in [65, 66]. It is also useful for the analysis of the voltage ripple in capacitors and thereby sizing them [67]. Even though AVMs are generally intended to study the terminal behavior of the MMCs in normal mode of operation, several works [68–72] have introduced improved AVMs

to model the converter in the blocking mode such as in DC fault conditions. The main drawback of AVMs is that a single equivalent capacitor is used to characterize the stack of SMs in the arm, which prevents the study of individual capacitor voltages.

Detailed Equivalent Models (DEMs), on the contrary, accurately and efficiently simulate MMCs in full detail without any loss of information compared with a DSM. The core idea in a DEM is to replace the stack of SMs with a Thevenin or Norton equivalent circuit, which reduces hundreds of nodes to two or three, thus in turn, diminishing the size of the network admittance matrix by many orders of magnitude. The parameters of such Thevenin or Norton equivalent circuits, i.e., the values of the voltage or current source and the resistor are affected by the numerical integration method employed for developing a discretized relationship between the voltage and current of the SM capacitors. Using trapezoidal integration method, references [55, 57, 73–76] and [77, 78] have developed DEMs with Thevenin and Norton equivalent circuits.

Although DEMs introduced in the literature have remarkably increased the computational efficiency of EMT simulations compared with a conventional DSM, the network admittance matrix is still modified frequently according to the switching functions of the SMs, which makes re-triangularization of the admittance matrix, albeit a smaller one, unavoidable at every switching instant. In a large power system, this would be problematic as the admittance matrix of the whole system needs to be inverted frequently only because of the presence of even one MMC. This is further aggravated in systems wherein several MMCs may be present, e.g., in modern renewable-intensive systems.

To overcome this significant drawback, this thesis proposes an alternative approach to achieve a constant network admittance matrix that is re-inverted only when the converter blocking mode is invoked, e.g., in DC fault conditions. Since converter blocking is a rare event, the resulting models yield significant computational gains over existing DEMs, while retaining the ability to represent

the converter during both normal and blocked conditions. This is an important contribution to the enhancement of the EMT modeling of modern power systems in which MMCs are embedded and whose simulation requires significant time and resources.

1.2 Motivation

Based upon the above literature review, the topic of including large-scale battery energy storage in the grid is a relatively new concept. Since BESS can supply large amounts of power to the grid within a short period of time, it can provide virtual inertia to the system. Many utilities have added or are on the verge of adding large-scale BESS to their systems. These undertakings are to address the consequences of massive integration of renewables and to combat its effects on the load-generation profiles and diminishing inertia. BESS have extensively captured the market among other alternatives for inertial support due to their low cost, high energy density and fast response.

MMCs, compared to 2- or 3-level VSCs, have several advantages such as modularity, scalability, low harmonic output voltage, and reduced switching frequency. MMCs are also already the converter of choice for HVDC applications and a great deal of practical experience with them already exists.

Inclusion of the BESS in MMCs brings substantial benefits that provides motivation to inspect the operation of such converters in inertia-deficient power systems. Although, MMCs with fully-integrated BESS have been investigated in the literature, partial integration of BESS would be beneficial to study in that only a small fraction of the converter's capacity is required for frequency support. Analysis of these types of converters requires EMT simulations with appropriate and efficient models. Therefore, this thesis aims at developing AVM and DEM models suitable for

different case studies.

1.3 Outline of the Thesis

The reminder of the thesis is organized as follows.

Chapter 2: The continuous-time model of the MMC-BESS is developed. Based on the state-space equations of the converter, a compact model of an arm is derived, reducing hundreds of nodes to just two or three.

Chapter 3: The continuous-time model is discretized using numerical integration methods to achieve a DEM model for EMT simulations. A suitable control system for BESS converters is introduced. Various case studies and experimental tests validate the accuracy of the DEM model. The computational efficiency of each DEM is also investigated, along with a discussion on the numerical stability of the model.

Chapter 4: An AVM model of the converter is derived, essential for low-frequency system-level studies and controller design. The per-unit system of the converter and its corresponding block diagram are also examined.

Chapter 5: The application of the MMC-BESS in power systems is explored, specifically its feasibility in Manitoba Hydro's system as a replacement for Bipole I. This study aims to improve frequency response while eliminating synchronous condensers and AC line filters.

Chapter 6: The thesis concludes with a summary of findings and contributions, along with recommendations for future research.

Chapter 2

Continuous-Time Modeling of the Arm in MMC-BESS

Parts of this chapter have been published in [79].

2.1 Introduction

Figure 2.1(a) shows a three-phase MMC-BESS displaying the stack of SMs and arm inductors in the upper and lower arms. The stack of SMs consists of two SM types: those with a battery and a dc-dc converter (BESS-SMs) and conventional SMs (CONV-SMs) as shown in Figures 2.1(b) and (c), respectively. The aim of the proposed model is to represent the stack of SMs with a computationally efficient model; once obtained, each arm stack is then connected to the arm inductors and the rest of the system using conventional EMT models.

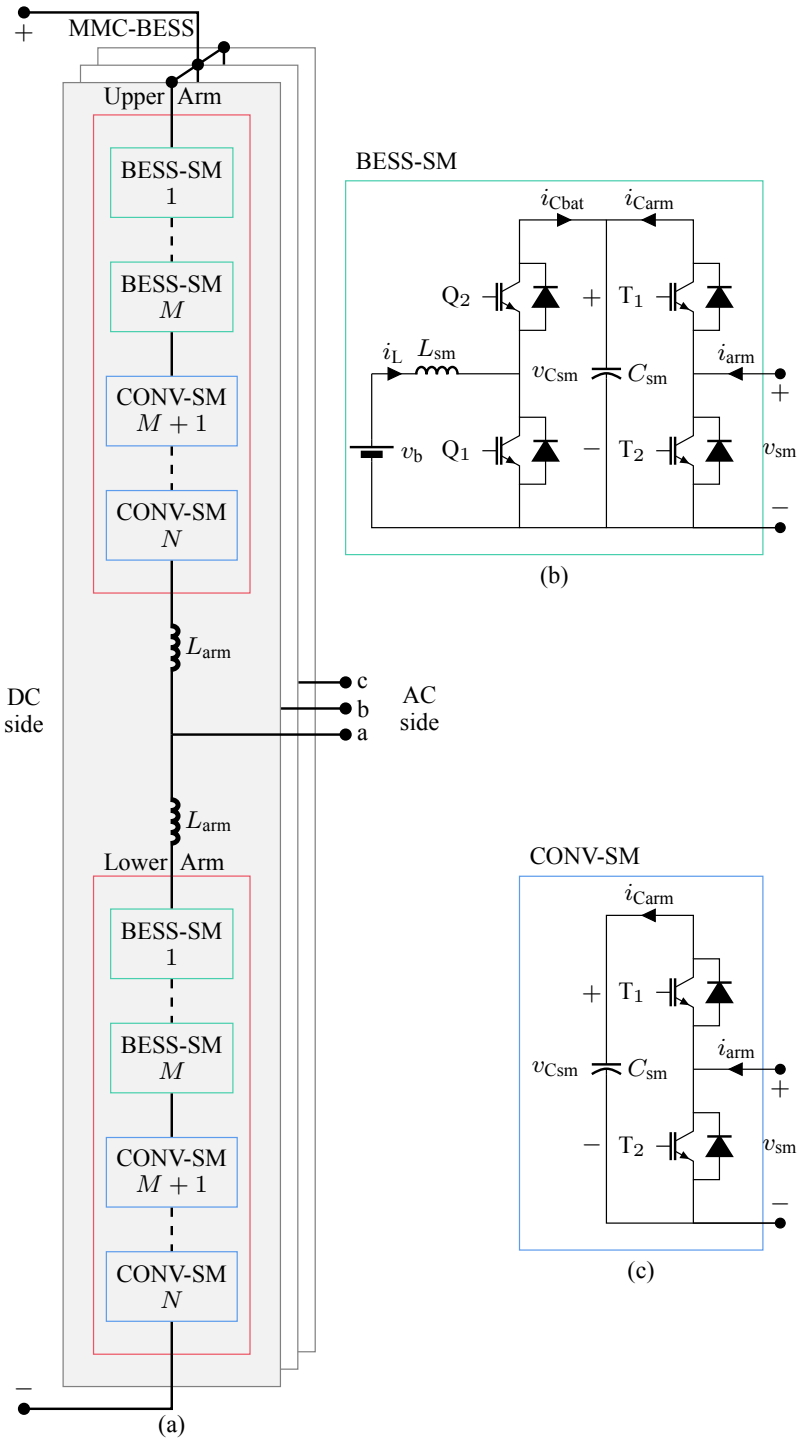


Figure 2.1: (a) Three phase MMC partially integrated with BESS, (b): BESS-SM HBSM, and (c): CONV-SM.

The total number of SMs in each arm is N out of which there are M BESS-SMs. In both SM types, the main switch cell is a half-bridge (HB) arrangement consisting of two switches denoted as T_1 and T_2 in Figures 2.1(b) and (c). Each SM has a capacitor with a capacitance of C_{sm} that retains an instantaneous voltage $v_{\text{Csm}}(t)$. The current of the CONV-SM capacitor has only one component, i.e. i_{Carm} (coming from right side as shown), while the BESS-SM capacitor current is composed of two components, i.e., i_{Carm} and i_{Cbat} (coming from left side as shown). Current i_{Carm} is in fact the arm current, i_{arm}, being switched by the main switch cell and i_{Cbat} is the current provided by BESS.

To increase the battery voltage to what is required for the SM capacitor, a boost converter is used. The converter must facilitate bidirectional energy transactions between the battery and the terminal power system. For this purpose, a bidirectional boost converter is considered. The boost converter is composed of a sub-module inductor L_{sm} and a switch cell containing Q_1 and Q_2 with respective anti-parallel diodes.

2.2 Modeling for Normal Operation

In this section the arm stack is modeled in the normal mode for which the main SM switch cells are operated according to modulation waveforms and switching strategy of choice. A circuit analysis approach is adopted to derive the equivalent circuit of the arm stack. For this purpose, the switch cells, i.e., the main SM switch cell or the boost converter's switch cell, are modeled using a combination of dependent voltage and current sources and then they are replaced with their equivalents.

2.2.1 Main SM Switch Cell

The main SM switch cell is shown in Figure 2.2 (a) wherein switches T_1 and T_2 are operated in a complementary manner.

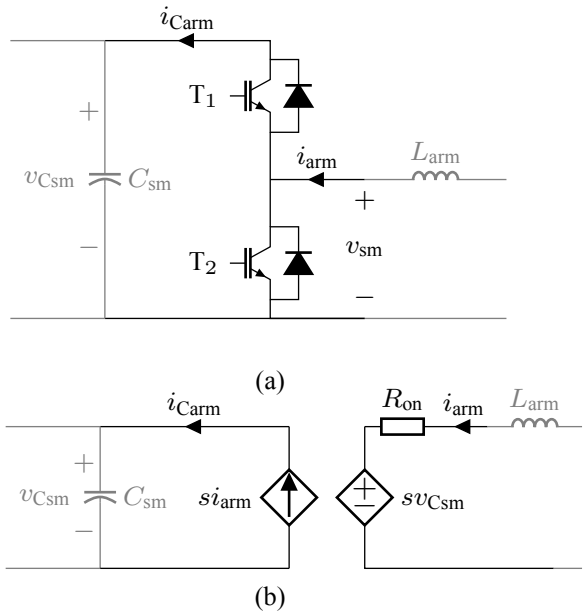


Figure 2.2: (a): main switch cell, (b): equivalent model.

If the switching function of the main switch cell is defined as

$$s(t) = \begin{cases} 1 & \text{T}_1\text{: on, } \text{T}_2\text{: off} \\ 0 & \text{T}_1\text{: off, } \text{T}_2\text{: on} \end{cases} \tag{2.1}$$

the sub-module voltage, v_{sm}, and the current i_{Carm} can be written as follows.

$$v_{\text{sm}}(t) = R_{\text{on}} i_{\text{arm}}(t) + s(t) v_{\text{Csm}}(t) \quad , \quad i_{\text{Carm}}(t) = s(t) i_{\text{arm}}(t) \tag{2.2}$$

where R_{on} is the ON-state resistance of a switch, and is considered to be the same for IGBTs and anti-parallel diodes, as is commonly done in EMT-type models [80]. Equation (2.2) offers a dependent-source representation of the cell as indicated in Figure 2.2(b).

2.2.2 DC-DC Converter Switch Cell

The switch cell in the DC-DC boost converter is shown in Figure 2.3(a). With a switching function for Q_1 and Q_2 defined as

$$q(t) = \begin{cases} 1 & Q_1\text{: on, } Q_2\text{: off} \\ 0 & Q_1\text{: off, } Q_2\text{: on} \end{cases} \tag{2.3}$$

the voltage and current relationships at the ports of the switch cell can be written as follows.

$$v_{\text{Q1}}(t) = R'_{\text{on}} i_{\text{L}}(t) + (1 - q(t)) v_{\text{Csm}}(t) \qquad , \qquad i_{\text{Cbat}}(t) = (1 - q(t)) i_{\text{L}}(t) \tag{2.4}$$

where R'_{on} is the ON-state resistance of a DC-DC converter switches. This leads to the representation of the switch cell with dependent sources as shown in Figure 2.3(b).

By replacing the two switch cells with their dependent-source equivalent models, a BESS-SM and a CONV-SM can be represented as shown in Figures 2.4(a) and (b), respectively. The parameters shown in these Figures are summarized in Table 2.1.

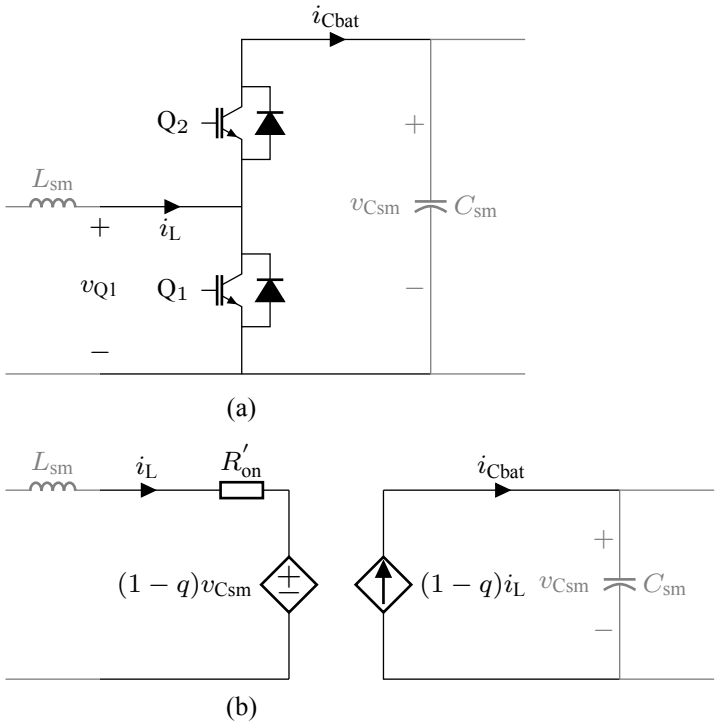


Figure 2.3: (a): DC-DC converter switch cell, (b): equivalent model.

Table 2.1: Parameters of the sub-modules

C_{sm}	SM capacitance
L_{sm}	SM inductance for SM-BESS
R_{on}	On-state resistance of the main switch (IGBT and diode)
R'_{on}	On-state resistance of the DC-DC converter switch (IGBT and diode)
R_{L}	Inductor series resistance
G_{Csm}	SM capacitor parallel conductance

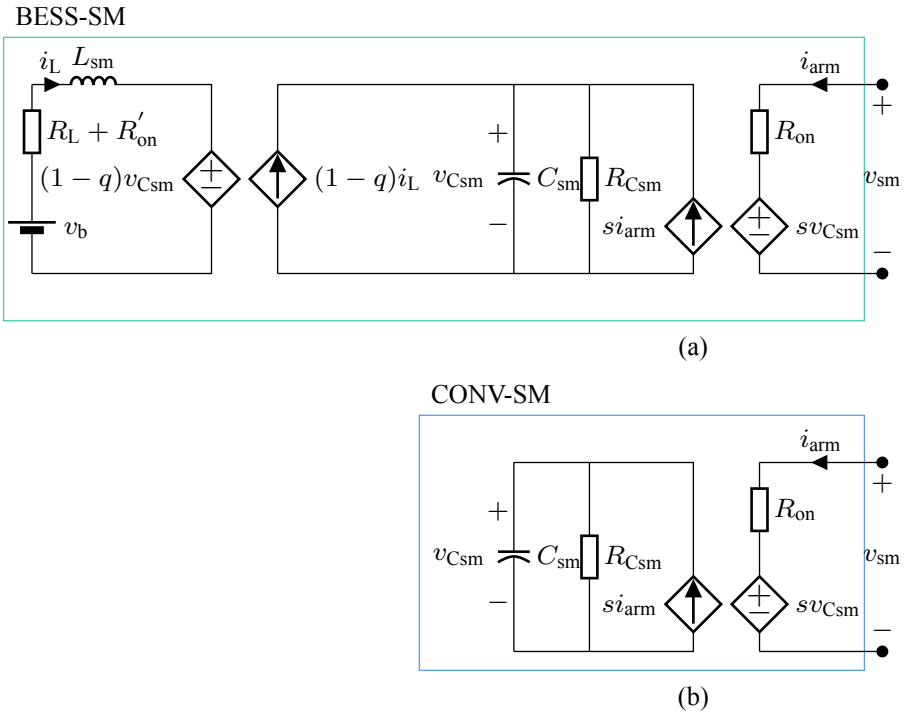


Figure 2.4: Normal mode model of a SM with dependent sources. (a): BESS-SM, (b): CONV-SM.

To obtain a computationally-efficient, admittance matrix-based EMT simulation model, the sub-module's equivalent circuits in Figure 2.4 are further reduced to only one voltage source in series with a resistor by replacing other circuit elements using algebraic and differential equations that govern those elements. These equations are interfaced with the nodal-analysis solution of the network. Figure 2.5 depicts the equivalent model that shows two SM types each involving only three nodes (two terminal nodes and one internal node between the dependent voltage source and the equivalent resistance).

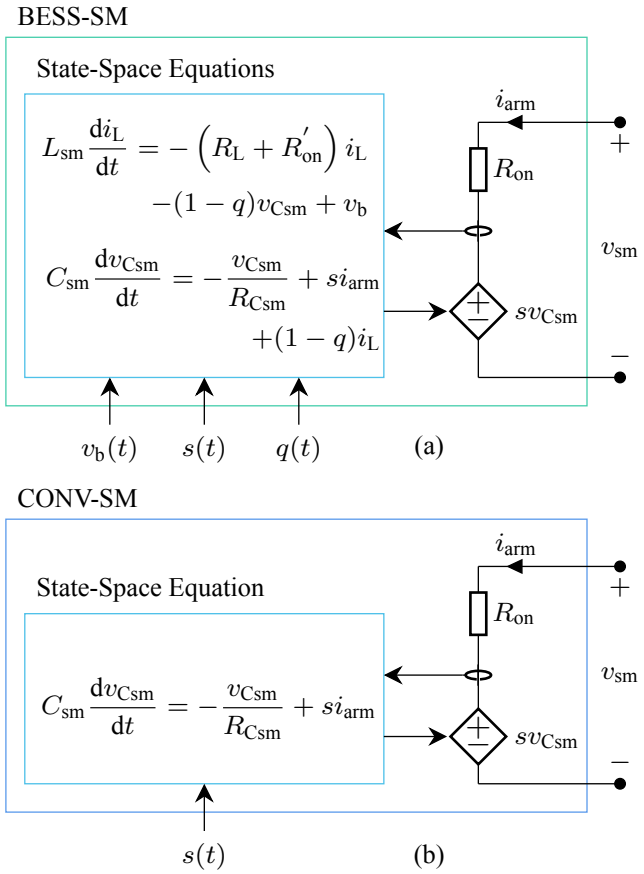


Figure 2.5: Normal mode model of a SM with state-space representation. (a): BESS-SM, (b): CONV-SM.

By connecting sub-module models together, the equivalent arm model of a partially-integrated BESS-MMC is achieved as illustrated in Figure 2.6. This model is valid only for the normal mode of operation in which the main switches in each SM, i.e., T_1 and T_2, are switched in a complementary manner. Note that vector algebra is used in the derivation of arm model in Figure 2.6. It must be noted that two types of vector multiplication are used in this model. The first one is the dot product, denoted by "$\cdot$", which returns a scalar value equal to the sum of the products of the corresponding entries of two vectors. The second one is the Hadamard product (or element-wise), denoted by "$\odot$",

that gives a vector whose elements are achieved by multiplication of the corresponding entries of two (or more) vectors. The definitions of the vectors in Figure 2.6 are tabulated in Table 2.2.

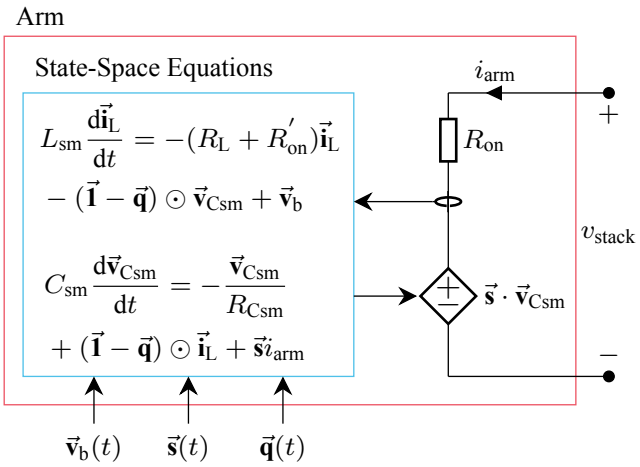


Figure 2.6: Normal model of the BESS-MMC arm with state-space representation.

Table 2.2: Vector Definitions

$\vec{1}$	Ones vector. $[\underbrace{1, 1, \cdots, 1}_{N}]^t$
$\vec{s}(t)$	Main switching vector. $[\underbrace{s_1(t), s_2(t), \cdots, s_N(t)}_{N}]^t$
$\vec{q}(t)$	DC-DC switching vector. $[\underbrace{q_1(t), q_2(t), \cdots, q_M(t)}_{M}, \underbrace{1, \cdots, 1}_{N-M}]^t$
$\vec{v_{Csm}}$	Capacitor voltages. $[\underbrace{v_{Csm1}, v_{Csm2}, \cdots, v_{CsmN}}_{N}]^t$
$\vec{i_L}$	Inductor currents. $[\underbrace{i_{L1}, i_{L2}, \cdots, i_{LM}}_{M}, \underbrace{0, 0, \cdots, 0}_{N-M}]^t$
$\vec{v}_b(t)$	Battery voltages. $[\underbrace{v_{b1}(t), v_{b2}(t), \cdots, v_{bM}(t)}_{M}, \underbrace{0, 0, \cdots, 0}_{N-M}]^t$

2.2.3 Modeling of the Blocked Mode

When the converter is blocked, e.g., during a dc fault, all IGBTs are turned off and only the free-wheeling diodes conduct the current. By adopting a similar circuit-based approach, the blocked-mode models of the BESS-SM and CONV-SM are obtained as shown in Figures 2.7(a) and (b), respectively. It is worth noting that these circuits resemble those in Figure 2.4 except that $s(t)i_{\text{arm}}$ is replaced with i_{Carm}.

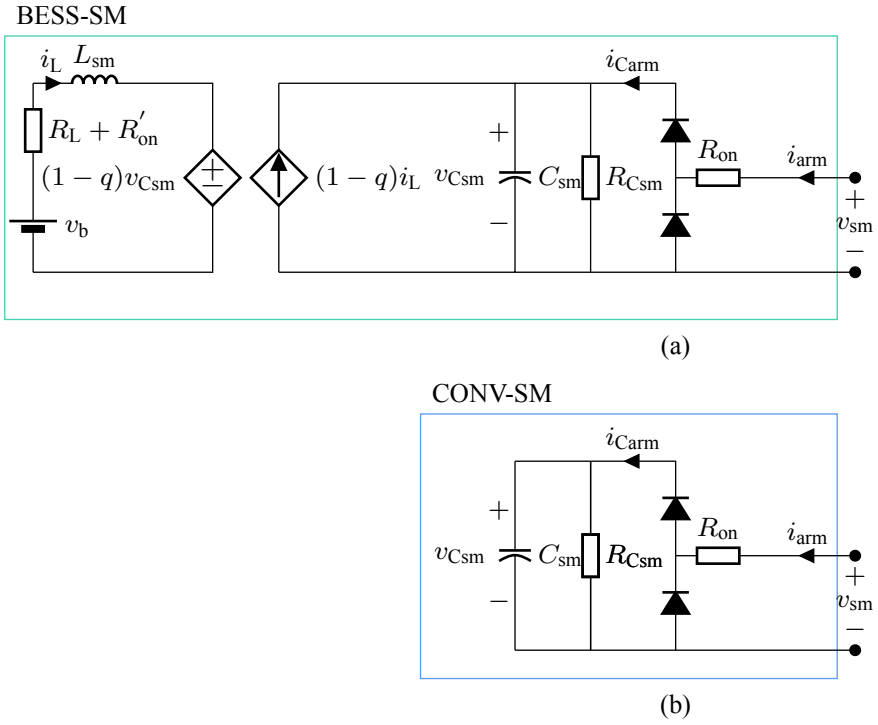


Figure 2.7: Blocked mode model of a SM with dependent sources. (a): BESS-SM, (b): CONV-SM.

The same procedure is followed to transform the derived circuits to differential equations, which are shown in Figure 2.8.

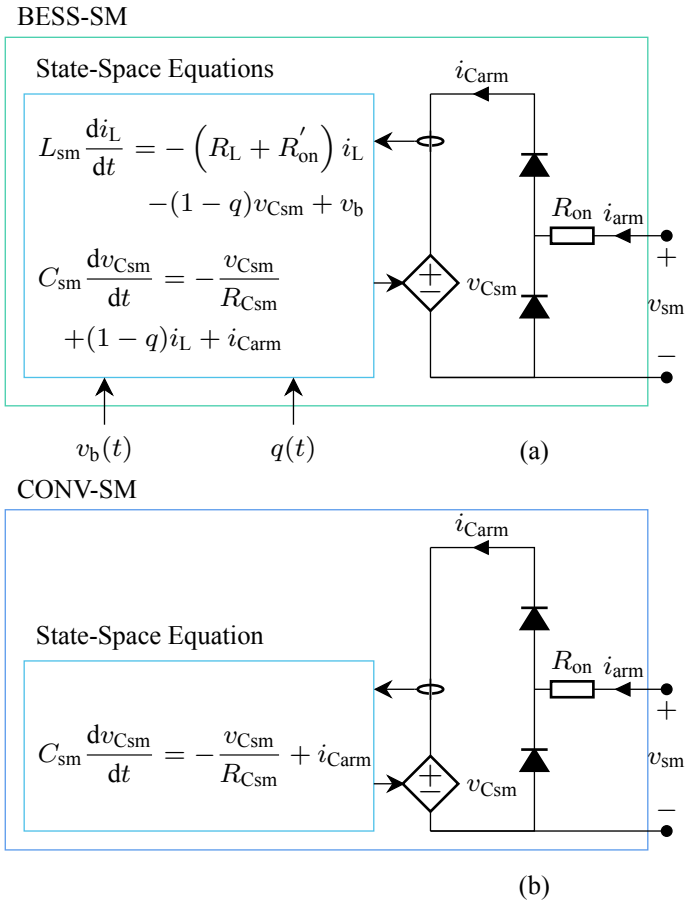


Figure 2.8: Blocked mode model of a SM with state-space representation. (a): BESS-SM, (b): CONV-SM.

In the blocked mode, each SM is a half-wave diode rectifier and hence series connected SMs may be considered as one equivalent half-wave rectifier. The arm stack circuit's model is readily realized by series connection of all SMs and using vector notation as indicated in Figure 2.9.

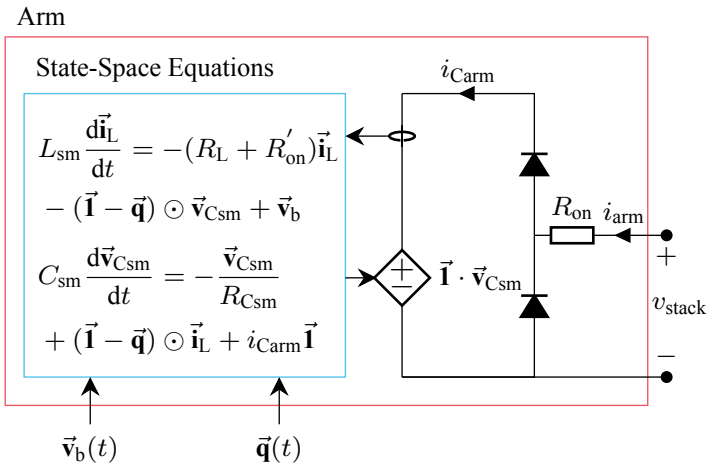


Figure 2.9: Blocked mode model of the arm with state-space representation.

2.2.4 Generalized Arm Stack Model

The equivalent circuits of the converter arm of a partially-integrated BESS-MMC for normal and blocked modes of operation can be amalgamated into a single circuit by adding an extra controlled switch with an ON-state resistance of R_{on} and two diodes. This is illustrated in Figure 2.10 where the controlled switch is turned on/off using the blocking signal. As long as the arm operates in normal mode, the switch is turned on and, along with the anti-parallel diode, it inserts the equivalent voltage source into the path of the current. In the blocked mode of operation, the controlled switch is turned off and the circuit becomes a half-bridge diode rectifier. The modes of the operation are determined according to the blocking signal defined as follows.

$$b(t) = \begin{cases} 0 & \text{Normal Mode} \\ 1 & \text{Blocking Mode} \end{cases}$$

$$\bar{b}(t) = 1 - b(t) \tag{2.5}$$

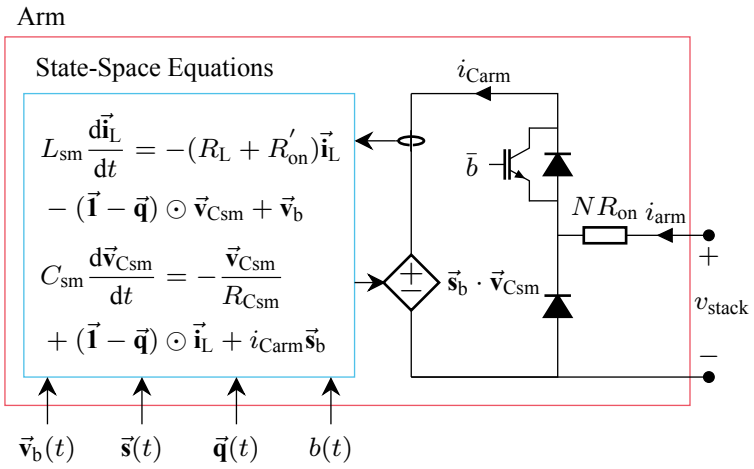


Figure 2.10: Generalized model of the arm stack.

Some parameters and variables of the circuit in Figure 2.10 must be modified through a selector function whose purpose is to switch between the normal and blocked modes. This is done via a vector function with the same length as the ones introduced in Table 2.2 and defined as follows.

$$\vec{s_b}(t) = \bar{b}(t)\vec{s}(t) + b(t)\vec{1} \tag{2.6}$$

2.3 DC-DC Converter Control

DC-DC converters are usually used to obtain a stable output voltage from a given input DC voltage. The regulated DC output voltage is achieved by modulating the duty cycle of the pulses by which the switches turn on and off. This method is called PWM wherein the duty cycle, as a control signal, is compared with a high-frequency saw-tooth carrier to generate the gate pulses. In a converter with robust control, the output voltage is regulated regardless of the loading and variations in the input voltage. However, in the proposed topology, the output voltage of the DC-DC converter, i.e., the

voltage of the SM capacitor, is already tightly regulated and depends on the HVDC link's voltage and the number of SMs. If the total DC voltage across the HVDC link is V_{dc}, the average voltage of each capacitor will be $\frac{V_{\text{dc}}}{N}$ regardless of the presence of BESS in some sub-modules. On the other hand, the input port of each DC-DC boost converter is connected to a battery, which is a voltage source in essence. Hence, in the DC-DC converter under consideration, both the input and output ports of each boost converter are DC voltage sources, implying the fact that the duty cycle must be constant if the converter is considered ideal. Even with non-idealities such as the series resistance of the inductor and the ON-state resistance of the switches, the interval where the duty cycle can change is negligibly small, thereby disallowing any meaningful control action via duty cycle variations. In such a case, current-control methods can be adopted to control the DC-DC converter. Here, the inductor current, as an independent variable, will be the control signal by means of which the amount of power being sent from or received by each battery is regulated.

It is worth noting that batteries are recommended to operate within a specific state-of-charge (SoC) range to enhance their lifespan [81]. In [82], an SoC reference interval of 0.45–0.55 was utilized to meet the requirements of battery energy storage systems (BESS) for primary frequency regulation. SoC values exceeding 0.9 are generally avoided, eliminating the necessity for charging batteries in constant voltage mode. Consequently, the current control of batteries does not need to be adjusted to accommodate charging in this mode.

The method used in this study is the Peak Current Mode (PCM) control [83] wherein the peak of the inductor current, which is the same as the peak of the switch current, is bounded. The circuit diagram of PCM control method is illustrated in Figure 2.11. In this circuit, the rising edge of the clock pulse sets the SR-latch and turns on Q_1. Consequently, the inductor current starts to rise until it reaches the given peak value, i_{ctrl}, when the comparator resets the SR-latch; this turns Q_2 on causing the inductor current to fall until the next rising edge of the clock pulse is issued starting

the next period of switching.

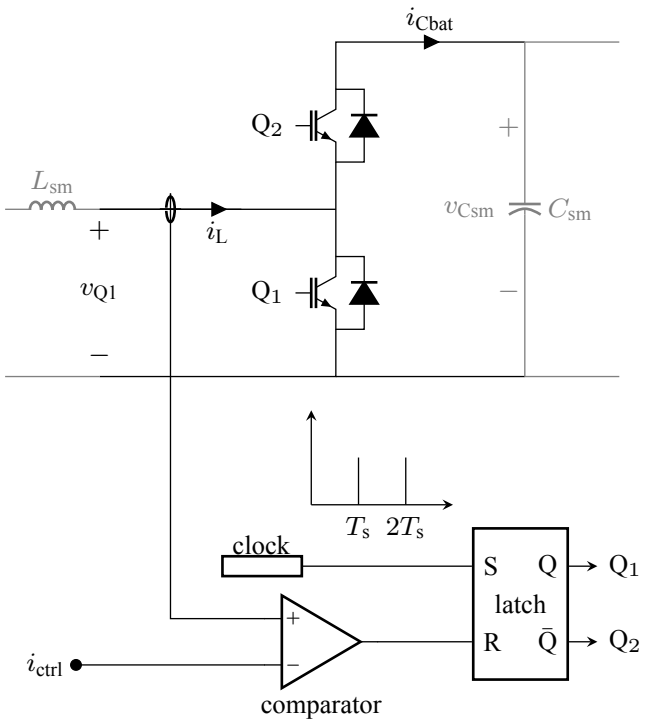


Figure 2.11: PCM control of the DC-DC converter.

2.4 Chapter Contributions

In this chapter, a continuous-time model of the converter was developed, which is capable of representing the converter in both normal and blocked modes. Various integration methods may be applied to discretize the related state-space equations, resulting in different EMT models. This universal model can be interfaced with virtually any EMT-type simulation platform, as it provides a continuous-time physical representation of the converter's arm. However, the discretization methods may vary depending on the specific implementation of the platform.

Chapter 3

Detailed Equivalent Model

Parts of this chapter have been published in [84] and [79].

In this chapter the governing equations of the arm stack derived in chapter 2 are discretized for the purpose of time-domain simulation with a fixed time-step. Depending on the method of integration used in the discretization process, there will be different EMT models of the converter's arm with varying accuracy and numerical stability properties. The trapezoidal rule of integration is widely used in EMT modeling applications; in the context of an MMC with partial BESS integration, however, using the trapezoidal rule yields a time-varying Thevenin resistor in the discretized model of the dependent voltage source in Figure 2.10. This is due to the fact that the value of the dependent voltage source is related to its current at the present time-step, i.e. $i_{\text{Carm}}(t)$. The value of the Thevenin resistance, on the other hand, varies with the switching functions $\mathbf{s}(t)$, which, in turn, necessitates re-triangularization of the admittance matrix every time a switching event occurs. Utilizing the trapezoidal integration method during the discretization process, the equivalent Thevenin resistance of the arm in normal mode, as expressed in the following equation, comprises the ON-state resistance of all switches, along with the summation of companion resistances asso-

ciated inserted capacitors.

$$R_{\text{th}} = NR_{\text{on}} + \left(\frac{\Delta t}{2C_{\text{sm}}}||R_{\text{sm}}\right) \times \vec{\mathbf{1}}.\vec{\mathbf{s}}(t) \tag{3.1}$$

In order to overcome this major computational drawback, the terms with $i_{\text{Carm}}(t)$ are discretized with Euler's method of integration, which expresses the integral as a function of the integrand at the previous time-step, i.e., $i_{\text{Carm}}(t - \Delta t)$. Note that other terms such as $\vec{\mathbf{i}}_{\text{L}}(t)$ and $\vec{\mathbf{v}}_{\text{b}}(t)$, which do not contribute to creation of the time-varying Thevenin resistance are discretized with the trapezoidal integration method. The resulting discrete-time model of the converter's arm is shown in Figure 3.1 and respective mathematical symbols are explicitly summarized in Table 3.1. Note that the element-wise multiplication and division are denoted by $\odot$ and $\oslash$, respectively. Evidently, there is no term including $i_{\text{Carm}}(t)$ in the expansion of the product $\vec{\mathbf{s}}_{\text{b}}(t) \cdot \vec{\mathbf{v}_{\text{Csm}}}$ that could have otherwise been manifested as an external Thevenin resistor.

It is also worth mentioning that the value of the voltage source in Figure 3.1 is known at the present time and can be found from the previous values of the states; hence the symbol of an independent voltage source is used in the Figure 3.1. Note that in addition to terminal voltage and current of stack of SMs, all other state variables, such as SMs' capacitor voltages and BESS' inductor currents, are fully accessible during simulation.

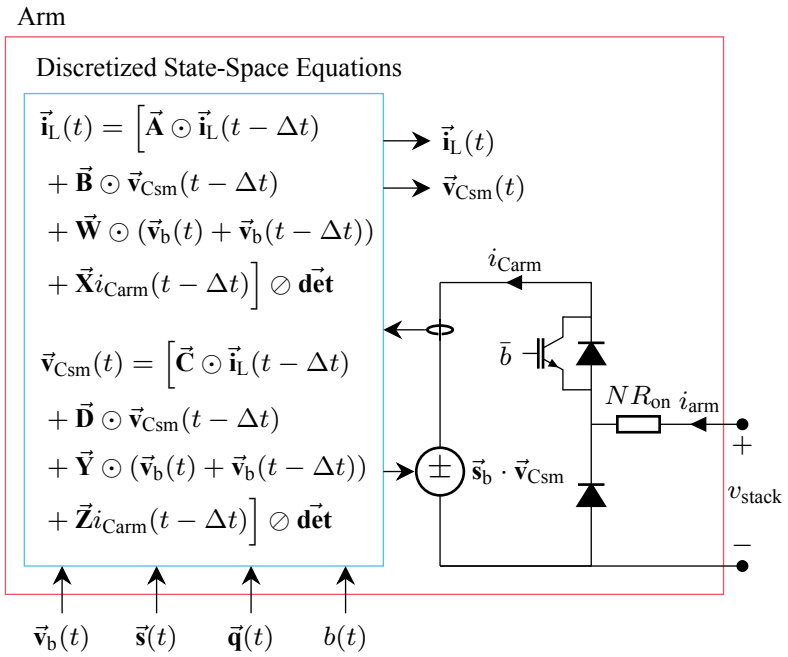


Figure 3.1: Discretized model of the converter's arm.

Table 3.1: Formulas of Figure 3.1

$\vec{\mathbf{det}}$	$(1+k_{\mathrm{L}})(1+k_{\mathrm{C}})\vec{\mathbf{1}} + g_{\mathrm{L}} r_{\mathrm{c}}(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t))$
$\mathbf{A}$	$(1-k_{\mathrm{L}})(1+k_{\mathrm{C}})\vec{\mathbf{1}} - g_{\mathrm{L}} r_{\mathrm{c}}\Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t)\Big) \odot \Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t-\Delta t)\Big)$
$\mathbf{B}$	$-g_{\mathrm{L}}\Big((1+k_{\mathrm{C}})(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t-\Delta t)) + (1-k_{\mathrm{C}})(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t))\Big)$
$\mathbf{C}$	$r_{\mathrm{c}}\Big((1+k_{\mathrm{L}})(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t-\Delta t)) + (1-k_{\mathrm{L}})(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t))\Big)$
$\mathbf{D}$	$(1+k_{\mathrm{L}})(1-k_{\mathrm{C}})\vec{\mathbf{1}} - g_{\mathrm{L}} r_{\mathrm{c}}\Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t)\Big) \odot \Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t-\Delta t)\Big)$
$\mathbf{W}$	$g_{\mathrm{L}}(1+k_{\mathrm{C}})$
$\mathbf{X}$	$-2g_{\mathrm{L}} r_{\mathrm{c}}\Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t)\Big) \odot \vec{\mathbf{s}_{\mathrm{b}}}(t-\Delta t)$
$\mathbf{Y}$	$g_{\mathrm{L}} r_{\mathrm{c}}\Big(\vec{\mathbf{1}} - \vec{\mathbf{q}}(t)\Big)$
$\mathbf{Z}$	$2r_{\mathrm{c}}(1+k_{\mathrm{L}})\vec{\mathbf{s}_{\mathrm{b}}}(t-\Delta t)$

$g_{\mathrm{L}} = \frac{\Delta t}{2L_{\mathrm{sm}}}$ $\quad r_{\mathrm{C}} = \frac{\Delta t}{2C_{\mathrm{sm}}}$ $\quad k_{\mathrm{L}} = g_{\mathrm{L}}(R_{\mathrm{L}} + R'_{\mathrm{on}} + R_{\mathrm{b}})$ $\quad k_{\mathrm{C}} = \frac{r_{\mathrm{C}}}{R_{\mathrm{Csm}}}$

3.1 Model Validation with conventional MMCs

The arm equivalent circuits derived in section 3.1 are implemented in the PSCAD/EMTDC simulator [85, 86] for both HBSM and FBSM sub-modules.

Several case studies are carried out to evaluate the performance of the proposed models, particularly to (i) establish their accuracy, and (ii) assess their computational advantage over existing DEMs. A simple test system comprising a single MMC connected to an infinite bus via a reactance is considered first. This example serves to validate the steady state operation of the converter and its response to a pole-to-pole (PTP) dc fault. Simulation results from this case are compared against those from the existing DEM in PSCAD/EMTDC to verify the accuracy of the proposed models. Next three CIGRE B4-57 MMC-HVDC grids [87, 88] are considered, in which several MMCs are embedded in increasingly more complex dc grids.

It must be noted that existing commercially available DEMs have been heavily used over the past decade by manufacturers, utilities, and consulting engineers, and are known to be accurate in representing the behavior of an actual MMC. They have also been verified against analytical and experimental results [89]. This is why they are used as the benchmark to validate the models proposed in this paper.

3.1.1 Case Study 1: Single-MMC Circuit

The circuit diagram of the simple test system used for accuracy verification of the proposed models is shown in Figure 3.2.

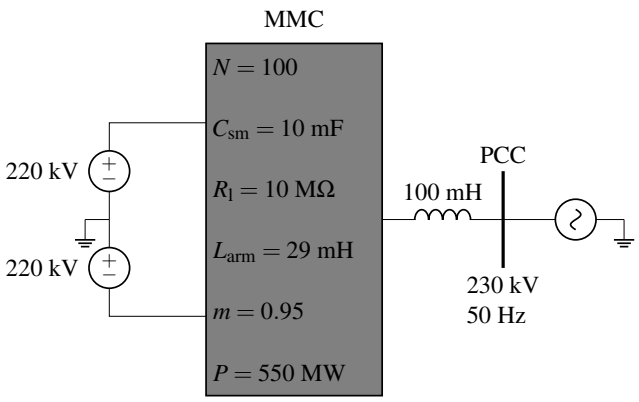


Figure 3.2: Circuit diagram of the system in case study 1.

The MMC is operated with the DC side voltage of 440 kV and 95% modulation index, producing a line-to-line voltage of 256 kV at its AC terminal. The produced voltage leads the PCC voltage by 17.2° to deliver 550 MW of real power to the power system. A PTP fault is applied at $t = 0.4$ s and the converter is blocked 1 ms thereafter. The circuit is simulated with both HBSM and FBSM topologies, with a simulation time-step of 50 μs. Figure 3.3 shows the waveform of the dc fault current, ac terminal voltage and current, and voltage and current of a randomly selected SM capacitor (64^{th}) from the top and bottom arm for both HBSM and FBSM circuits. After the fault is cleared, the system settles at a new operating condition for which the arm currents, summation of capacitors voltages in each arm, and voltage and current of a random SM (31^{th}) are shown in Figure 3.4. Except for slight discrepancies in the SM-level waveforms, the results produced by the proposed models (dashed lines) match those by the existing DEM (solid lines), thus they verify the accuracy of the proposed models during both steady state and faulted conditions. Slight differences in the SM-level quantities are due to the small differences in the sorted SM capacitor lists submitted to the firing pulse controller.

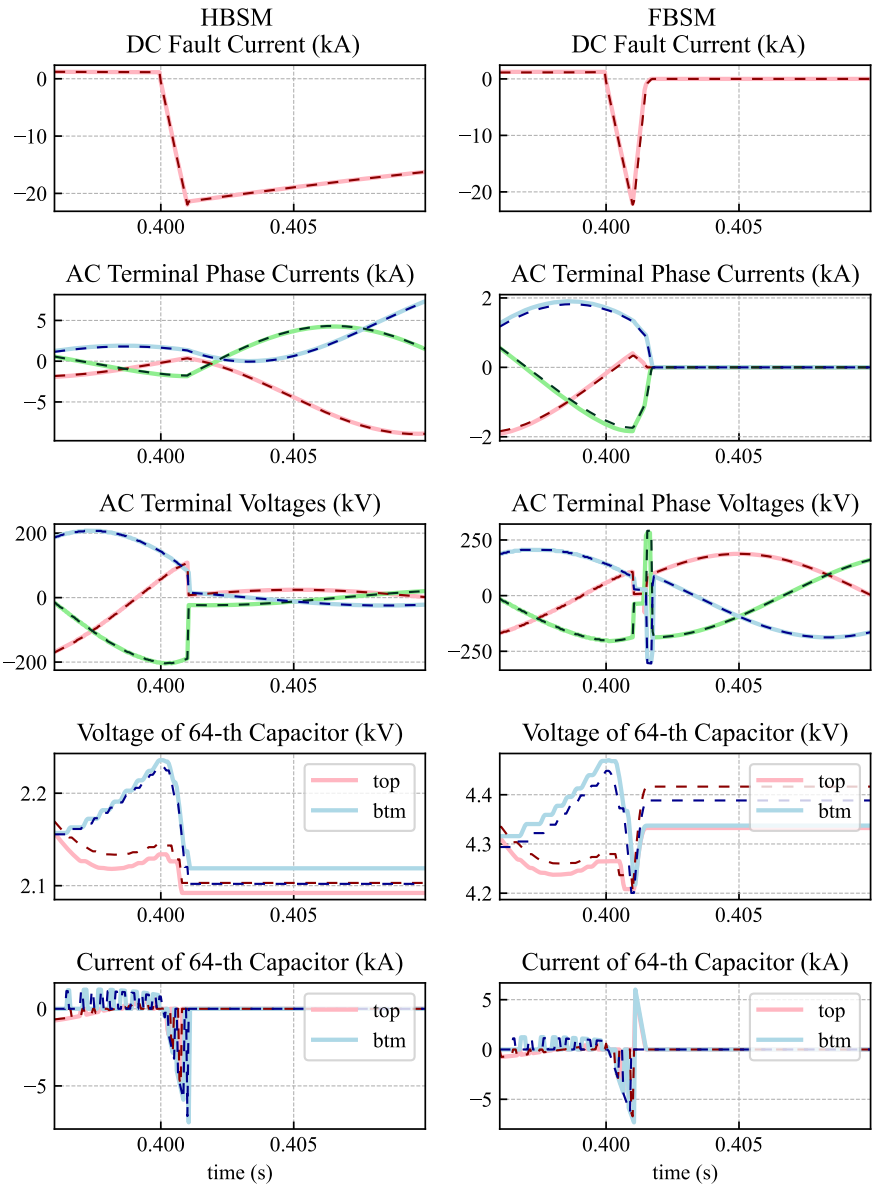


Figure 3.3: Case study 1: Waveform for a PTP fault for HBSM and FBSM topologies. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

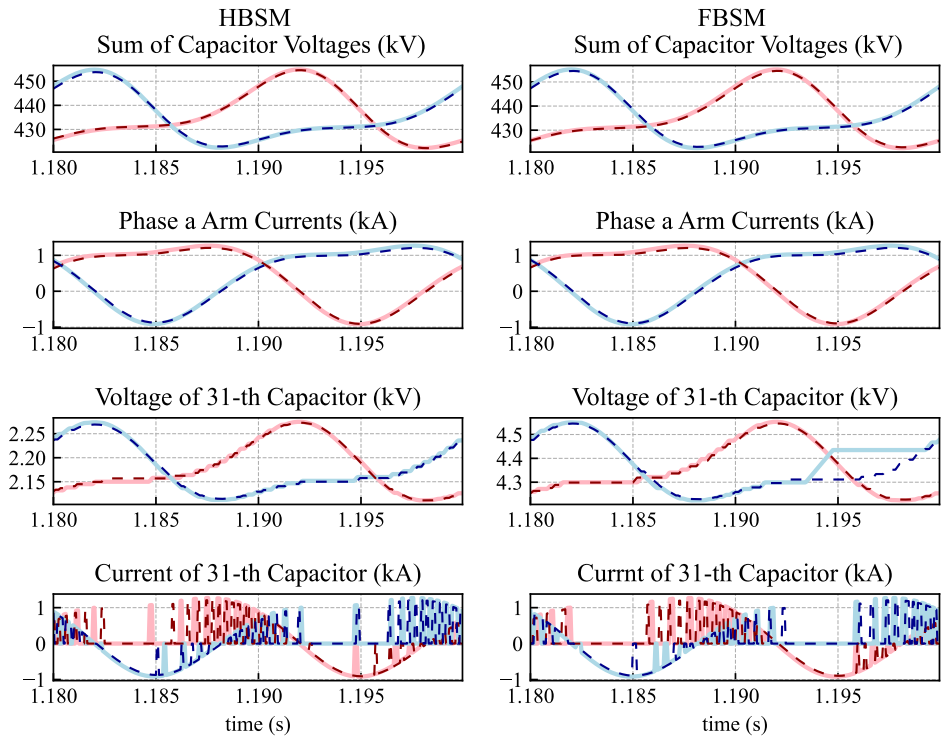


Figure 3.4: Case study 1: Waveforms of MMC during normal mode. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

3.1.2 Case Study 2: CIGRE MMC-HVDC Benchmarks

Three simulation models of the CIGRE B4-57 MMC-HVDC grids [87,88] with 2, 4, and 16 MMCs are considered. Specifications of the systems and their parameter values may be found in [88]; they are not repeated here for brevity. In all simulations in this section, the MMCs are considered to have the same number of sub-modules. Two tests, as elaborated upon below, are conducted to evaluate the performance of the proposed models.

Test I

The MMC-HVDC network with 4 MMC units is considered for this test. The single-line diagram of this network is shown in Figure 3.5.

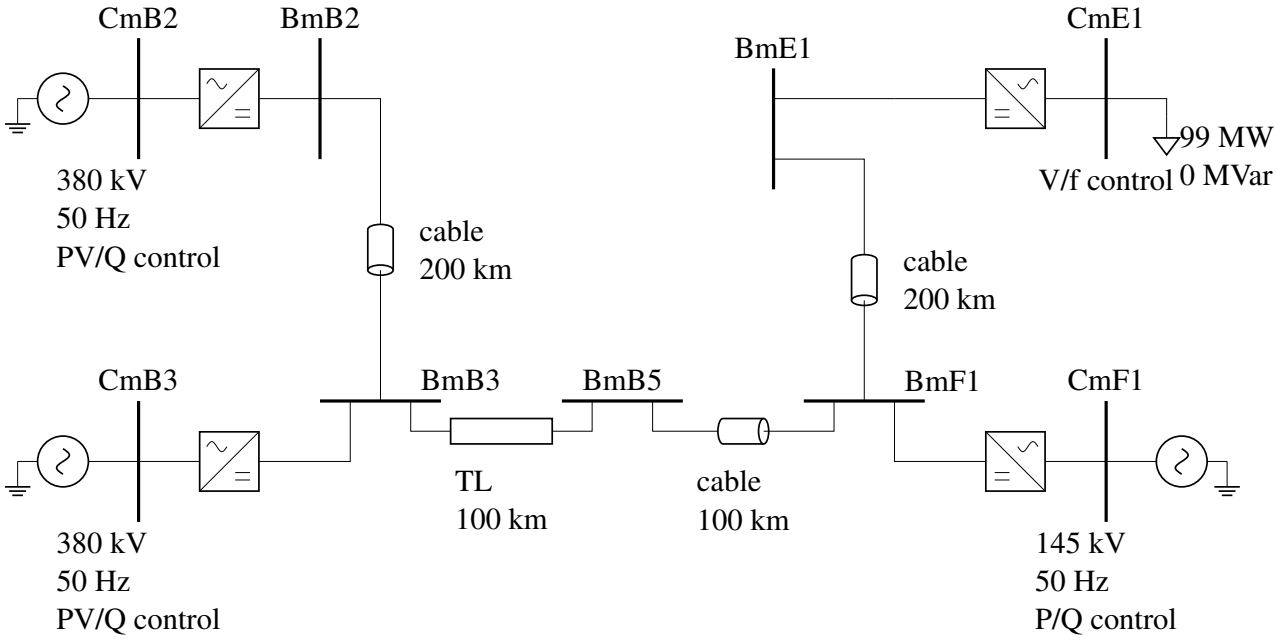


Figure 3.5: CIGRE B4-57 MMC-HVDC grid with 4 MMC stations.

Each arm of the MMCs in the network consists of 200 HBSM with a $10000\,\mu$F SM capacitor. The network is simulated twice, once with the existing DEM in PSCAD/EMTDC as the benchmark and once with the proposed DEM. Figure 3.6 shows the arm currents and summation of the capacitor voltages for phase-a of each converter station in steady state. A negative step change of 200 MW is applied at $t = 1.5$ s to the converter at bus CmF1, followed by a positive 300 MW step change at $t = 2.0$ s. The variations of the measured power at the dc terminals of the converter stations are shown in Figure 3.7. A permanent PTP fault is applied at the converter station CmF1 at $t = 2.5$ s. The voltage and current waveforms of the dc terminals of each converter station are shown in Figure

3.8. As clearly seen, the waveforms from the existing PSCAD/EMTDC's DEM match perfectly with those produced by the proposed model, thus further validating its accuracy.

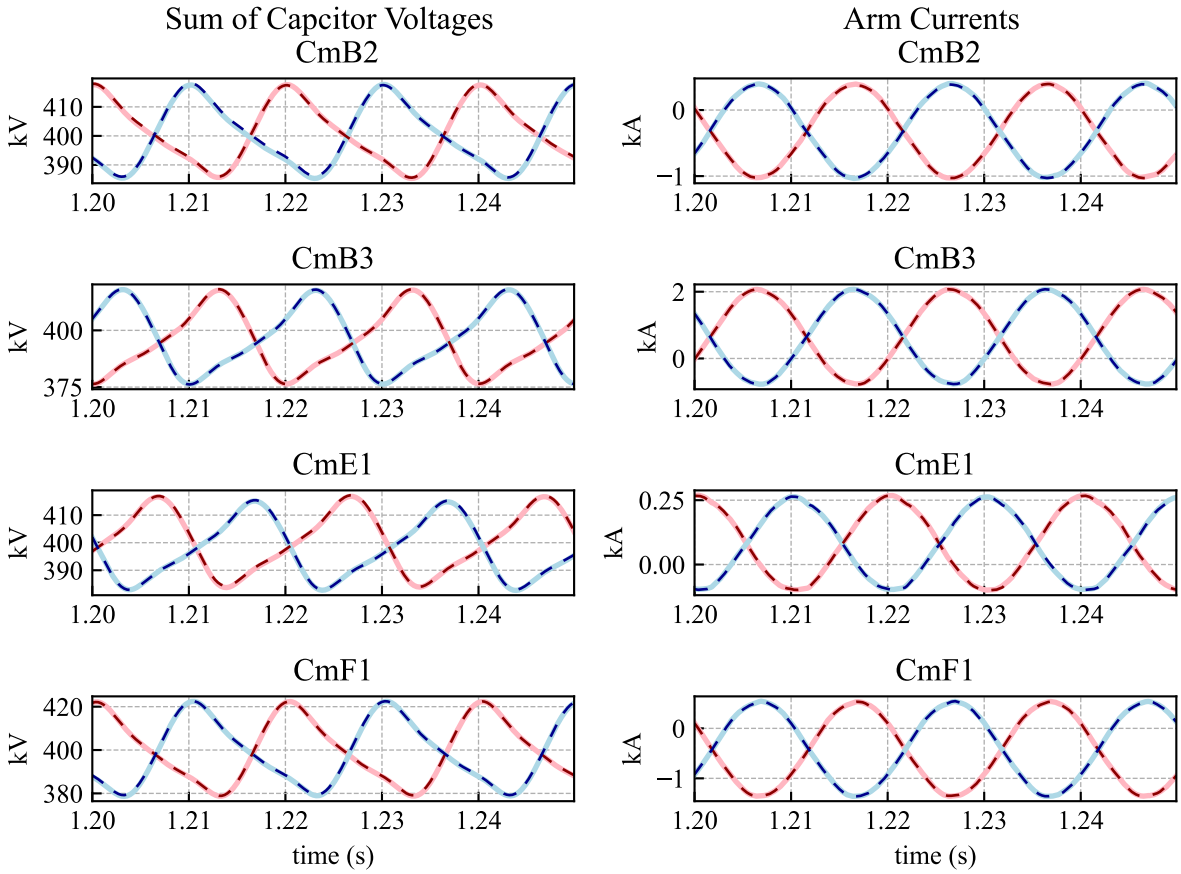


Figure 3.6: Case study 2 (Test I): Arm currents and summation of capacitor voltages. solid: PSCAD/EMTDC's existing DEM, line: proposed model.

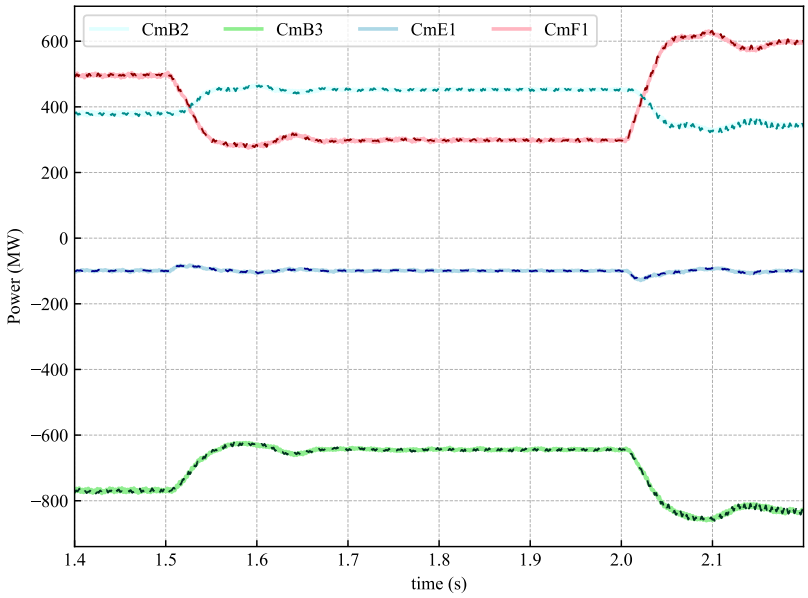


Figure 3.7: Case study 2 (Test I): Measured power in converter stations. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

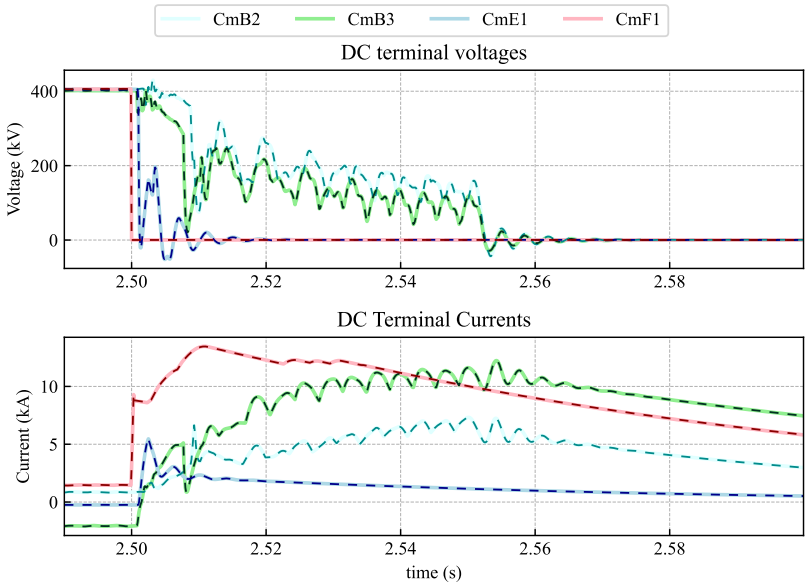


Figure 3.8: Case study 2 (Test I): Measured DC voltages and currents in converter stations. solid: PSCAD/EMTDC's existing DEM, dashed: proposed model.

Test II

Each of the MMC-HVDC grid models, i.e. with 2, 4, and 16 MCCs, is simulated with different number of SMs using both the proposed and PSCAD/EMTDC's existing DEM. In order to achieve the same dynamic responses as the number of SMs is varied, the SM capacitance is updated so that the equivalent arm capacitance, $C_{\text{arm}} = C_{\text{sm}}/N$, remains constant at $50\,\mu$F. The simulation time-step and run duration are $50\,\mu$s and 2 s, respectively. Simulations are conducted on a computer with 3.40 GHz Intel Core i7-6700 CPU with 16 GB of memory. To eliminate the effect of run-time plotting of waveforms on the recorded CPU time, all figures (graphs) are removed after first having confirmed that the resulting waveforms are accurate. Table 3.2 shows the measured CPU run-time in seconds for systems with different number of MMCs and sub-modules for HBSM topology. The tests are also repeated for the same systems with FBSMs with proper control circuitry, and the results are tabulated in Table 3.3. To compare the effectiveness of the proposed model, the ratio of its CPU run-times to those of the PSCAD/EMTDC's DEM is plotted against the number of sub-modules in Figure 3.9.

The graph shows the run-time ratio for different number of MMCs in the network for both HBSM and FBSM configurations. The graphs show significant reductions in CPU time by the proposed models. For 200 HBSMs per arm, for example, the proposed model is around 30% more computationally efficient than the existing DEM. For 200 FBSMs, however, it is more than 60% accelerated. The CPU run-time is chiefly affected by two factors. One is the time needed for re-triangularization of the admittance matrix. The other is the time consumed for calculations of control signals for IGBTs' firing signals. In each run, the dimensional order of the admittance matrices remain constant and nearly the same for both the proposed model and the PSCAD/EMTDC's DEM. However, the number of control signals is approximately proportional to the number of sub-modules in each run. Therefore, for larger numbers of SMs, the CPU run-time is predominately

determined by the number of sub-modules. Because control signal calculations are held the same for the cases with the proposed and existing DEMs, the ratio is expected to increase and approach unity when the number of the SMs increases, as is also seen in Figure 3.9. The proposed models, however, show significant savings even for SM counts as high as 400, for which the proposed FBSM models are more than twice as fast as the existing DEM.

Table 3.2: CPU Run-Time of MMC-HVDC Systems with HBSM

N_{MCC}	2		4		16	
N_{sm}	Proposed	Existing	Proposed	Existing	Proposed	Existing
50	3.7	8.8	7.3	16.5	38.9	96.4
100	6.4	12.9	12.7	23.5	52.6	116
150	10.6	17.8	21.7	33.1	81.3	152
200	16.2	24.1	31.9	44	117	185
250	23.7	32.4	45.7	58.9	165	239
300	32.5	41.9	62.3	76.6	210	289
350	43.1	52.3	85.8	99.4	298	375
400	50	65.2	104	117	383	431

Table 3.3: CPU Run-Time of MMC-HVDC Systems with FBSM

N_{MCC}	2		4		16	
N_{sm}	Proposed	Existing	Proposed	Existing	Proposed	Existing
50	4.3	15.2	8.7	29.1	62.1	139
100	6.7	24.6	13.1	43.4	77.3	200
150	10.9	35.3	22.3	62.2	104	279
200	16.7	47.5	31	84.7	145	354
250	23.7	62.8	42.5	110	181	455
300	32.4	75.7	59.4	137	254	567
350	40.1	90.9	78.4	162	307	646
400	52.3	107.6	93	197	371	753

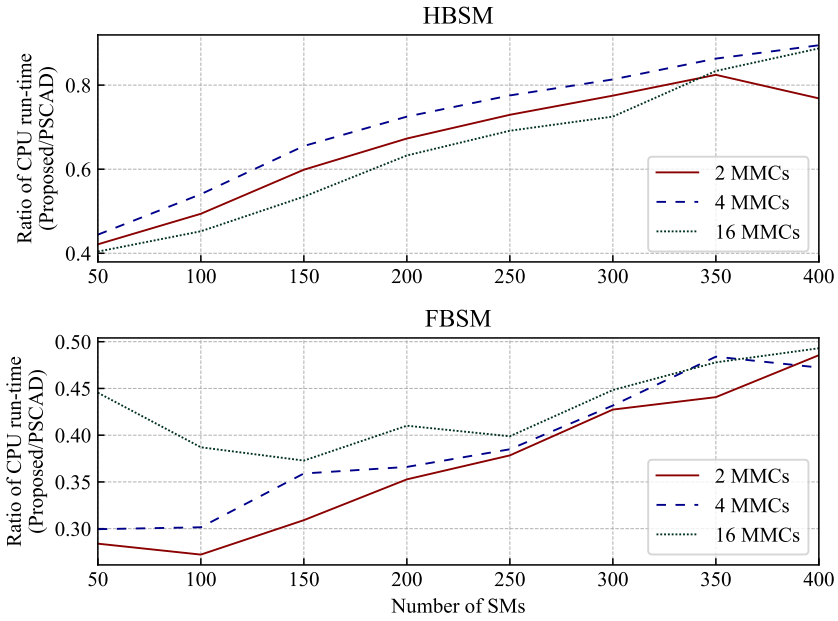


Figure 3.9: Ratio of CPU run-time of the proposed models to the existing DEMs.

3.1.3 Case Study 3: Inclusion of MMC-BESS in CIGRE Benchmarks

In this section the developed DEM is used in EMT simulation of a large HVDC system to demonstrate the functionalities of the MMC-BESS. The case study focuses mainly on the converter-level responses and waveforms, and as such ancillary services such as inertial support are not demonstrated. The CIGRE B4-57 MMC-HVDC grid [87,88] with four converter stations, shown in Figure 3.10, is considered. Each station consists of a MMC (with half-bridge sub-modules) with a rated AC voltage of 220 kV connected to an external AC system via a transformer with the respective turns ratio. All the converters share a common DC voltage rated at 400 kV through HVDC transmission lines and cables. Nearest Level Control (NLC) [90] is used to generate firing pulses for the IGBTs in all converter stations. Furthermore, Circulating Current Suppression Control (CCSC) [65] is

added to the control circuit of each station for elimination of the second order harmonics in arm current. Table 3.4 highlights specifications of the converters in each station.

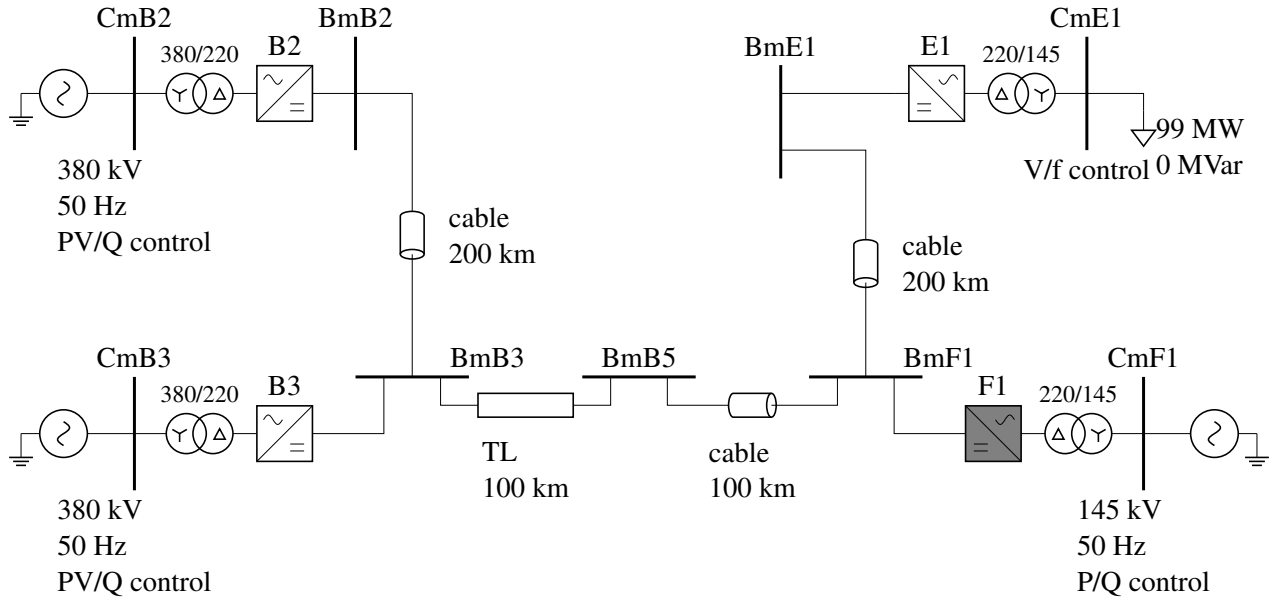


Figure 3.10: CIGRE B4-57 MMC-HVDC grid with four MMC stations. Gray-colored station is equipped with BESS.

The *dq* reference frame theory [91] is employed as the main control scheme in each station which is shown in Figure 3.11. However, generation of the reference *dq* currents and/or voltages varies from station to station. At bus 'CmE1', the voltage magnitude and frequency are regulated since it operates in the islanded mode with a fixed load on its AC side. The bus 'CmF1' is a P/Q-controlled bus whose reference *dq* currents are produced by outer loops regulating the real and reactive power with respective reference values. Both 'CmB2' and 'CmB3' buses are PV/Q-controlled with the same strategy used in 'CmF1' except that the reference real power is augmented by the DC voltage deviation from its rated value multiplied by a droop coefficient so that the DC voltage drops as DC power delivered towards the DC hub is increased. The controllers' default

parameters, as specified in [88], are applied to all simulations.

Table 3.4: Specifications of Converters

Parameter	B2	B3	E1	F1	Unit
Rated Power	800	1200	200	800	MV A
BESS Included	No	No	No	Yes	-
Number of CONV-SMs	200	200	200	200	-
Number of BESS-SMs	0	0	0	100	-
SM Capacitance	10	15	2.5	10	mF
Cap. Leakage Resistance	10	10	10	10	MΩ
Switch ON Resistance	1	1	1	1	mΩ
Arm Inductance	29	19	116	29	mH
Trans. Voltage Ratio	380/ 220	380/ 220	145/ 220	145/ 220	-
Trans. leakage reactance	0.18	0.18	0.18	0.18	pu
Trans. Copper Loss	0.006	0.006	0.006	0.006	pu

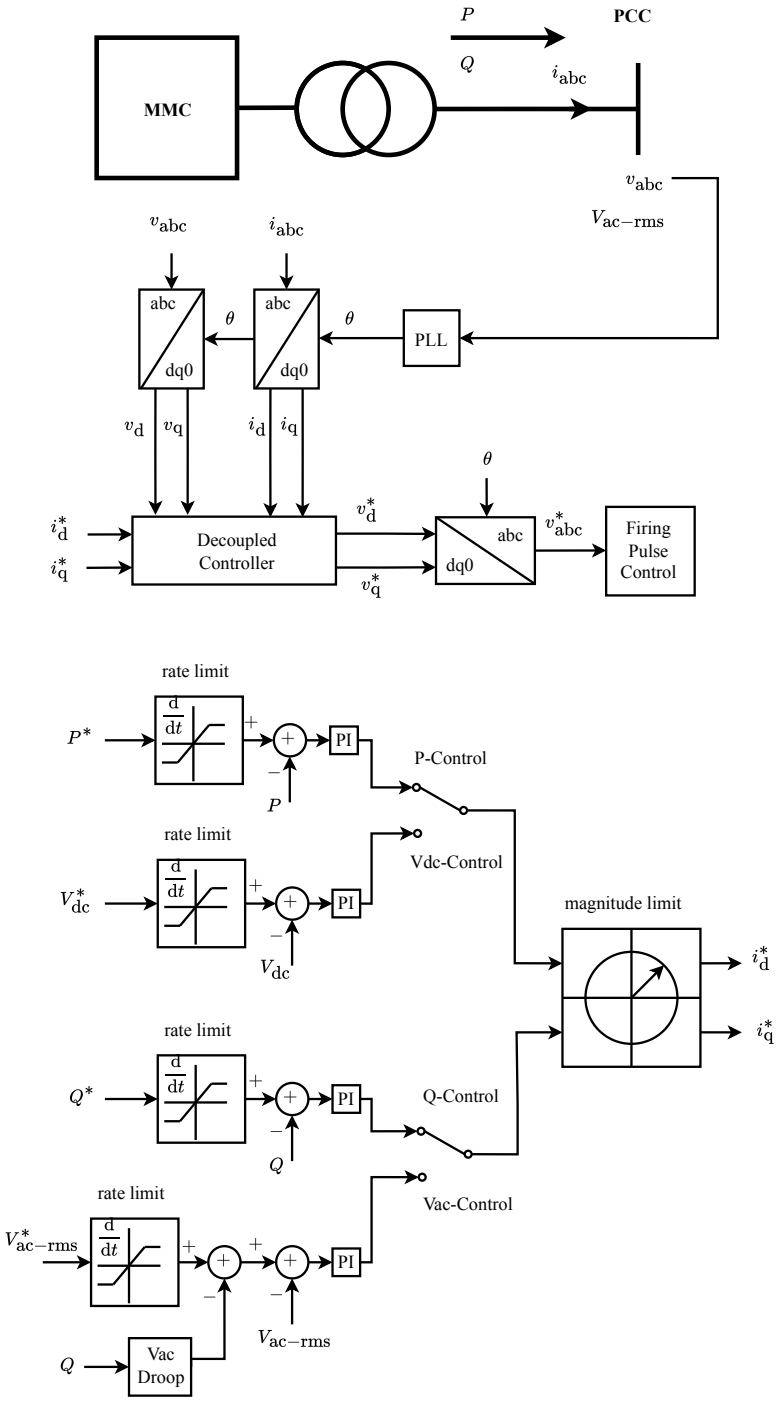


Figure 3.11: Control block diagram of MMC.

The control of BESS is largely independent from the control modes of the MMC due to two main reasons. Firstly, the DC voltage regulation is managed by the MMC, which incorporates sorting and balancing algorithms. BESS does not engage in this control mode as it does not attempt to regulate sub-module voltage via feedback control loops. Secondly, reactive power and/or AC voltage are regulated either by modulation index or the imaginary component of the current in the decoupled *dq* reference frame, with BESS integration exerting minimal influence on this control mode. Active power is the sole variable modulated by the injection or absorption of battery power. The adjustment of battery power commands (or battery current) is then dictated by the chosen control function, which may originate from frequency control or inertial support mechanisms.

The converter 'F1' is equipped with BESS. It consists of 200 half-bridge sub-modules, half of which are upgraded to include batteries and DC-DC converters. For simplicity, the battery is modeled with a DC voltage behind an internal resistor with values of 1.2 kV and 1.0 $\mathrm{m\Omega}$, respectively. DC-DC converters are operated under the PCM control wherein the peak current is determined based on the power command, to be either injected or absorbed, and battery's specifications. Note that the peak current is approximately the same as the battery's average current thanks to the relatively high-inductance reactor of the DC-DC converter. The DC-DC converter's inductor is 0.1 H with series resistance of 1.0 $\mathrm{m\Omega}$, which is switched with the frequency of 2 kHz. All simulations are executed with the time-step of 10 $\mu\mathrm{s}$.

Injection and absorption of power by batteries

Initially, the converter 'F1' delivers 500 MW to the DC side without drawing real power from the batteries. Once steady state is achieved, a demand for 72 MW of power from the batteries is initiated at $t = 2$ s, while maintaining the power command of the AC system at bus 'CmF1' at 500 MW, along with other AC buses. Subsequently, at $t = 3$ s, the batteries are instructed to charge with

the same power. Figures 3.12, 3.13, and 3.14 depict the DC voltage, power at the DC terminals of the four converter stations, and the total battery power at the converter 'F1', respectively. Despite operating in both charging and discharging modes, the DC voltage at each bus remains within a 0.025 pu range, where 1 pu corresponds to 400 kV. However, the DC power varies based on the bus type and control mode of each station. While the DC power aligns with the power command from the batteries at 'BmF1', the power at 'BmE1' remains constant due to its fixed AC-side load. Consequently, the surplus power from the batteries, either +72 MW starting at $t = 2$ s or -72 MW starting at $t = 3$ s, is distributed among stations 'CmB2' and 'CmB3' according to their respective power/voltage droop characteristics.

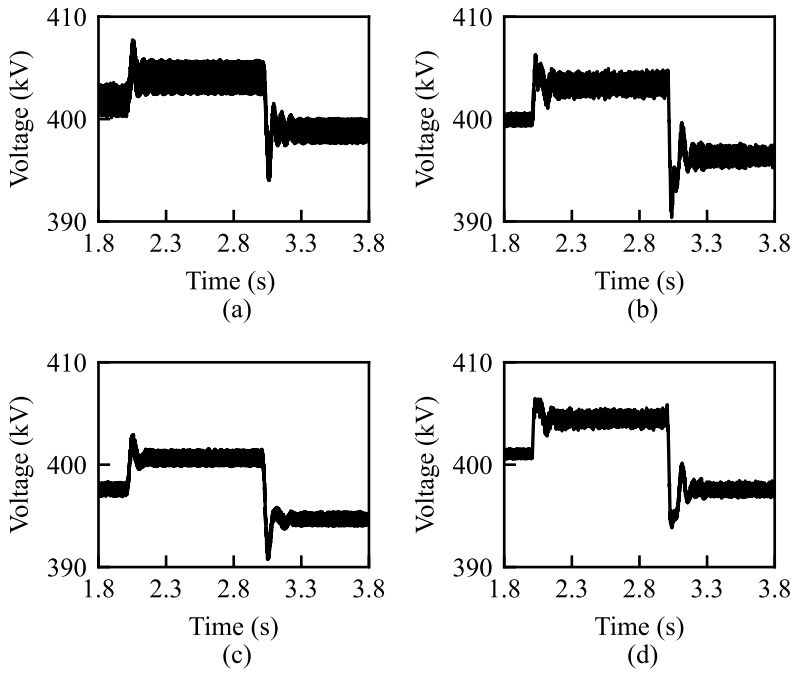


Figure 3.12: DC voltage at DC terminals of the converter stations (a): BmB2, (b): BmE1, (c): BmB3, (d): BmF1.

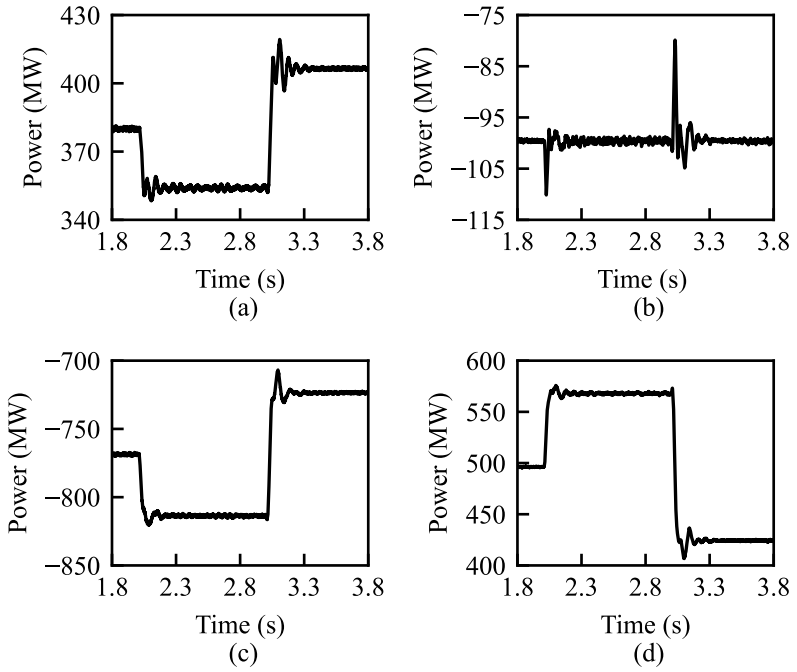


Figure 3.13: DC power at DC terminals of the converter stations (a): BmB2, (b): BmE1, (c): BmB3, (d): BmF1.

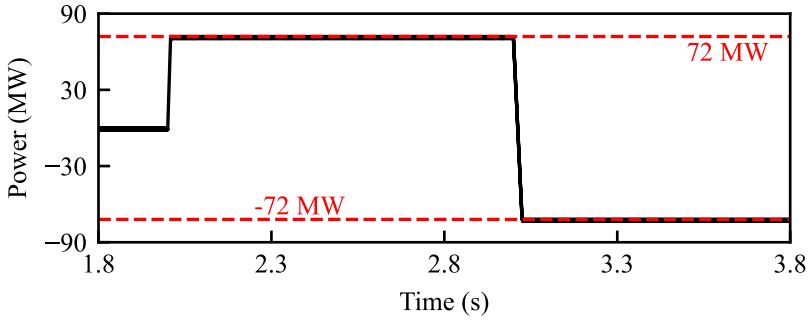


Figure 3.14: Total battery power.

Arm-level waveforms

Figure 3.15 shows the arm current and the average of the SM capacitor voltages in the top and bottom arms of the BESS-MMC.

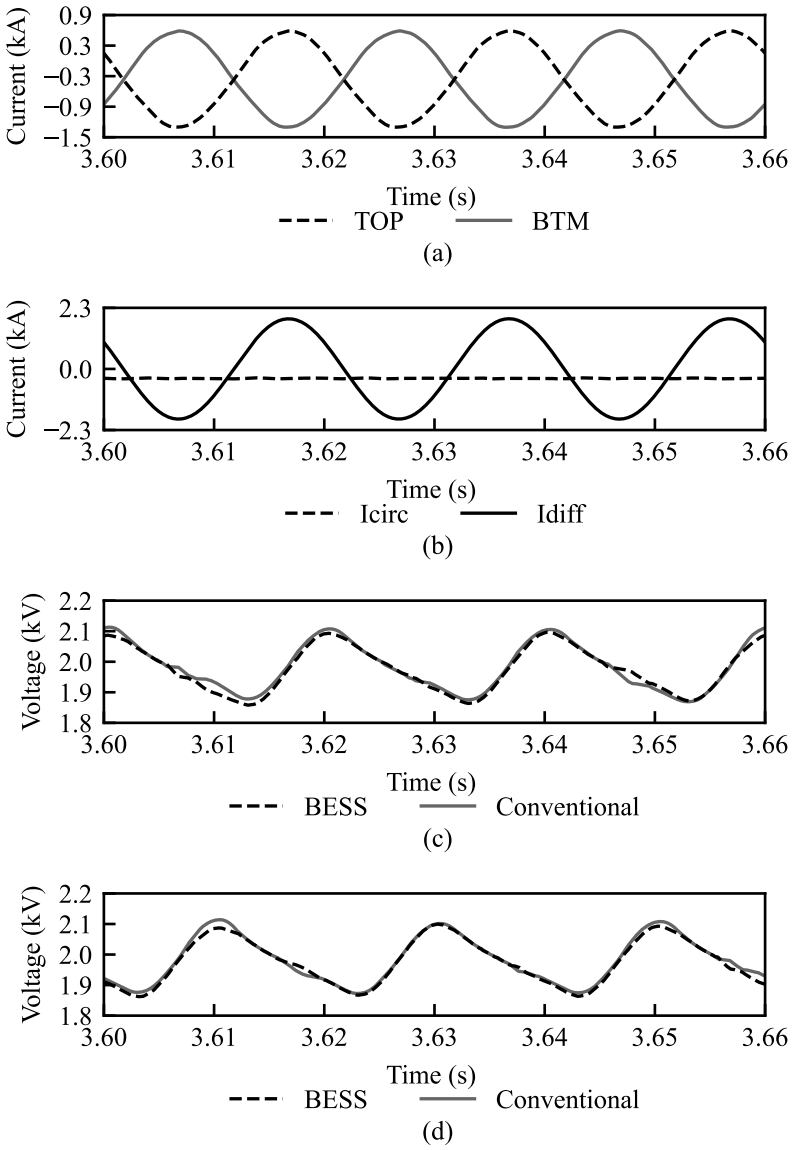


Figure 3.15: Arm level waveforms, (a): arm currents, (b): circulating and differential currents, (c): average of voltages across CONV-SM and BESS-SM capacitors for top arm, (d): average of voltages across CONV-SM and BESS-SM capacitors for bottom arm.

These waveforms are taken while the batteries are charged with the peak current order of 100 A. Note that the differential current, which is the same as AC terminal current, exhibits sinu-

soidal behavior. Conversely, the circulating current is constant. Thus the arm currents are nearly completely sinusoidal with a DC offset because of the operation of the circulating current suppression controller. It is also noted that the average of voltages across capacitors of CONV-SMs and BESS-SMs are slightly different due to the inherent topological asymmetry. The SM capacitance is selected to maintain a 10% peak-to-peak voltage ripple, a criterion recommended by CIGRE Working Group B4.57 in [92].

Response of battery currents

The steady-state current waveform of sample batteries from the top and bottom arms are depicted along with the commanded peak current in Figure 3.16.

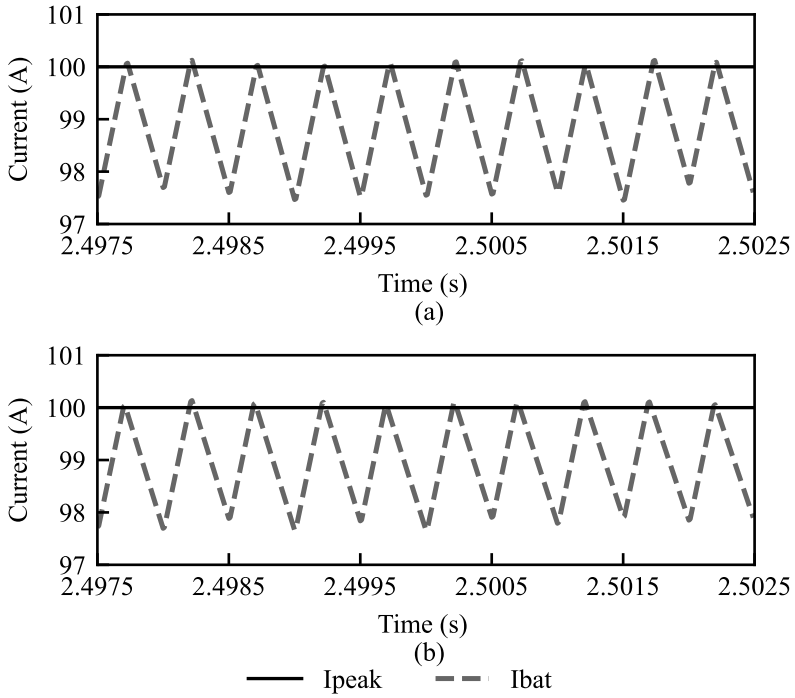


Figure 3.16: Steady-state waveforms of battery currents, (a): current of 11-th battery from the top arm, (b): current of 37-th battery from the top arm.

As shown, the battery current (which is the same as the DC-DC converter's inductor current) rises up starting at the beginning of a switching period until it reaches the commanded peak current (in this case 100 A). Reaching the peak value, the inductor current starts to fall until the next switching period starts. It is evident that the inductor's average current (99 A in this case) is close to the peak current and the difference is often neglected.

The transient responses of the battery (inductor) currents to a step change in the commanded peak current from 100 A to -100 A are shown in Figure 3.17 for two representative batteries. They both quickly settle into the requested steady state, with a settling time that is influenced by the DC-DC converter's inductance.

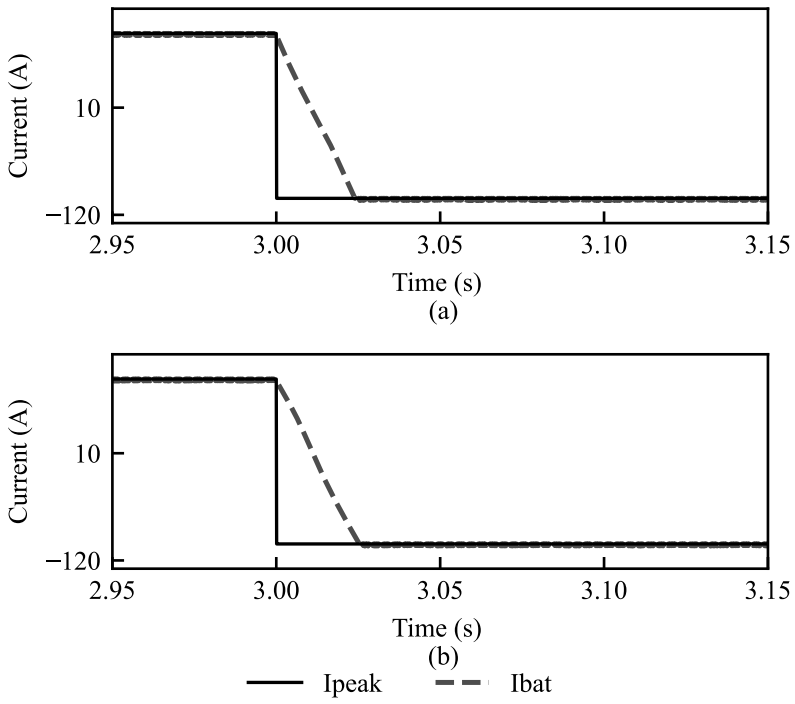


Figure 3.17: Transient response of battery currents to a step change in commanded peak current, (a): current of 11-th battery from the top arm, (b): current of 37-th battery from the top arm.

Pole-to-pole DC fault

At $t = 2$ s, a Pole-to-Pole (PTP) DC fault is applied at BmF1. The fault is detected when the magnitude of DC current exceeds 6 kA, and a blocking signal is issued after 30 μs. Subsequently, after 2 cycles (40 ms), the AC side breakers open. This blocking and tripping scheme is implemented for all stations. Fig. 3.18 illustrates the DC current of each converter.

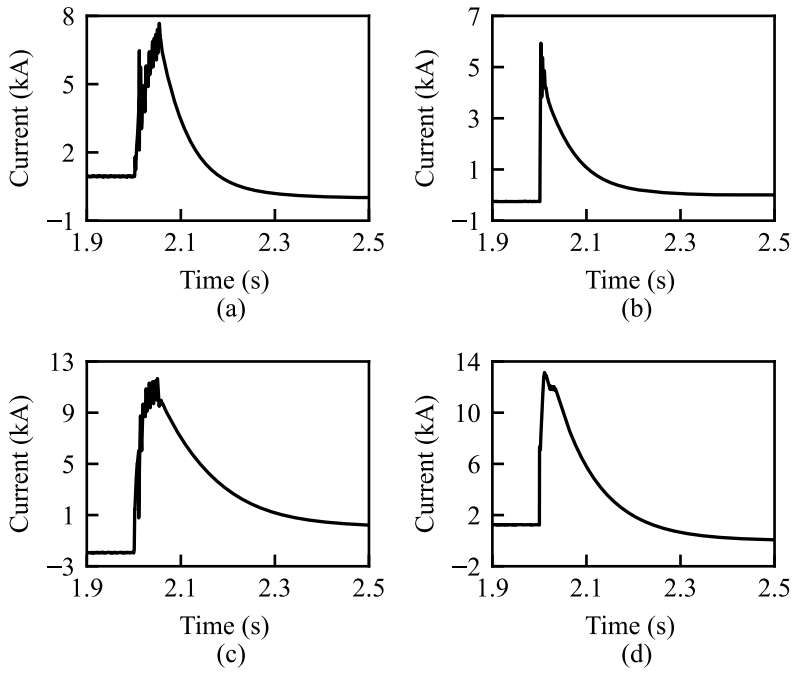


Figure 3.18: DC currents under PTP DC fault at BmF1 for DC buses (a): BmB2, (b): BmE1, (c): BmB3, (d): BmF1.

It is important to note that the measured current direction is toward the DC hub. It is evident that the current increases immediately after the fault occurrence. Subsequently, all converters are blocked, while the AC breakers have not yet disconnected the stations from their AC sides. Consequently, the AC sides contribute to the DC fault current, as depicted in Fig 3.19. However, it is worth mentioning that the AC side of converter CmE1 does not contribute to the fault current since

it operates in islanded mode, with a passive load on its AC side.

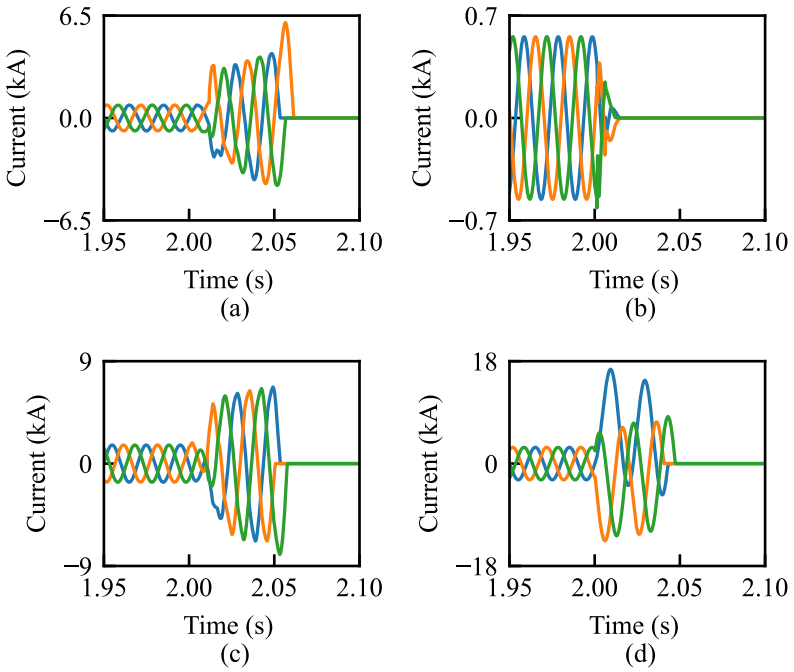


Figure 3.19: AC currents under PTP DC fault at BmF1 for AC buses (a): CmB2, (b): CmE1, (c): CmB3, (d): CmF1.

3.2 Experimental Validation

Presently there are no commercially available DEM model for the MMC-BESS that could be used for accuracy cross-validation. Thus, this section validates the accuracy of the proposed DEM by comparing its results against those obtained from a down-scaled single-phase prototype of an MMC with partially-integrated BESS. Figure 3.20 depicts the block diagram of the developed test-bed shown in Figure 3.21. Table 3.5 shows the specifications and parameters of the experimental setup.

The nearest level control (NLC) method for pulse generation is used for firing the switches in

each arm. For the sorting and balancing of capacitor voltages as well as measurement and monitoring, waveforms including arm currents, SM capacitor voltages, battery voltages, and battery currents are measured and interfaced with the signal measurement unit through analog-to-digital conversion. The gate pulses for all switches are then generated and sent back to the MMC-BESS hardware via PWM generation platform. A 1 kHz anti-aliasing filter is used for each low-frequency analog signal in order to eliminate the noises associated with analog-to-digital conversion.

Table 3.5: Parameters of the Experimental Setup

Parameter	Value	Unit
Total number of SMs per arm	8	-
Number of BESS-SMs per arm	3	-
DC link Voltage	200	V
Sub-module capacitance	4700	μF
Modulation index	0.95	-
AC voltage frequency	60	Hz
DC-DC converter switching frequency	10	kHz
Arm inductance	8	mH
DC-DC converter inductance	900	μH
Load inductance	10	mH
Load resistance	10.24	Ω
Battery nominal voltage	12	V
Battery capacity	7	A h

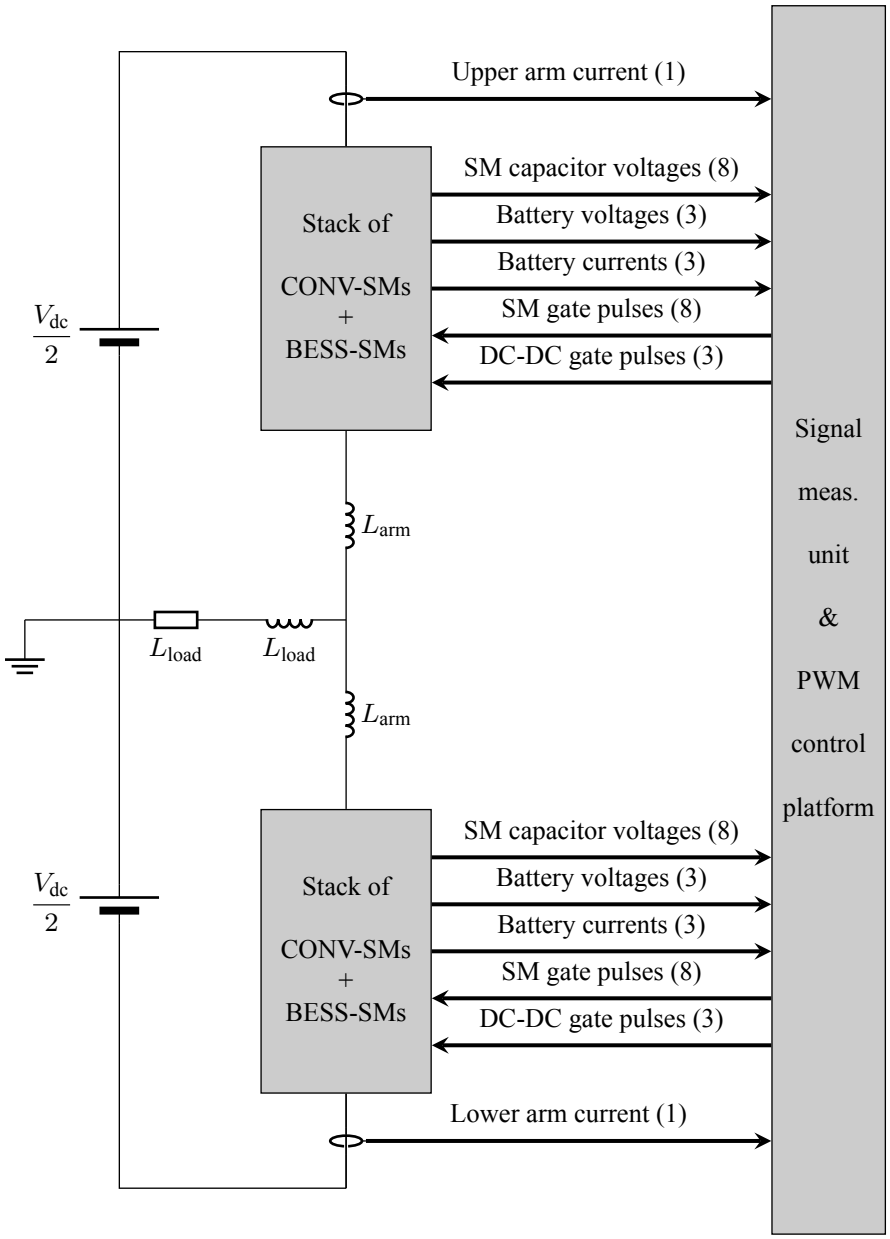


Figure 3.20: Schematic diagram of the experimental setup.

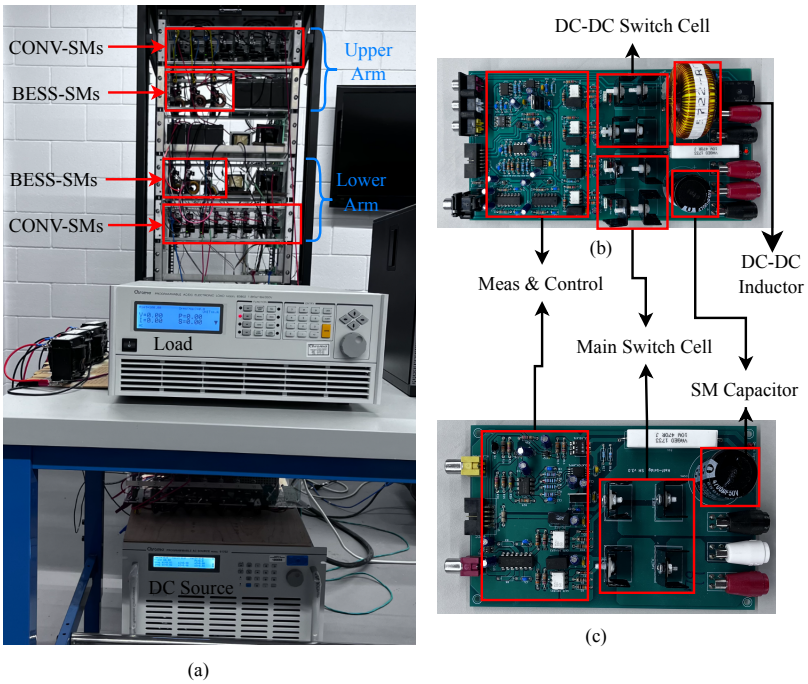


Figure 3.21: (a): Experimental setup, (b): BESS-SM, (c): CONV-SM.

A model of the experimental test setup is built in the PSCAD/EMTDC simulator using the DEM developed in this section. The simulation time-step is set to 10 µs. Figures 3.22 and 3.23 compare low-frequency steady-state waveforms from the experimental setup against those produced by the DEM for two battery current commands $I_{\text{ctrl}} = 1$ A (discharging) and $I_{\text{ctrl}} = -0.8$ A (charging), respectively. The comparison clearly shows that both simulation and experimental waveforms follow each other closely. Note that root mean square errors calculated for voltage and current waveforms of Figures 3.22 and 3.23 are less than 0.5% and 10%, respectively. The higher error in current measurement stems from two reasons. Firstly, it is impractical to precisely adjust the power supply for the hall effect sensor to obtain an exact value. Secondly, the arm and load inductors are not accurately measured and modeled. These components exhibit nonlinearity, and their inductance varies with current. However, in the simulation, they are treated as fixed linear inductors.

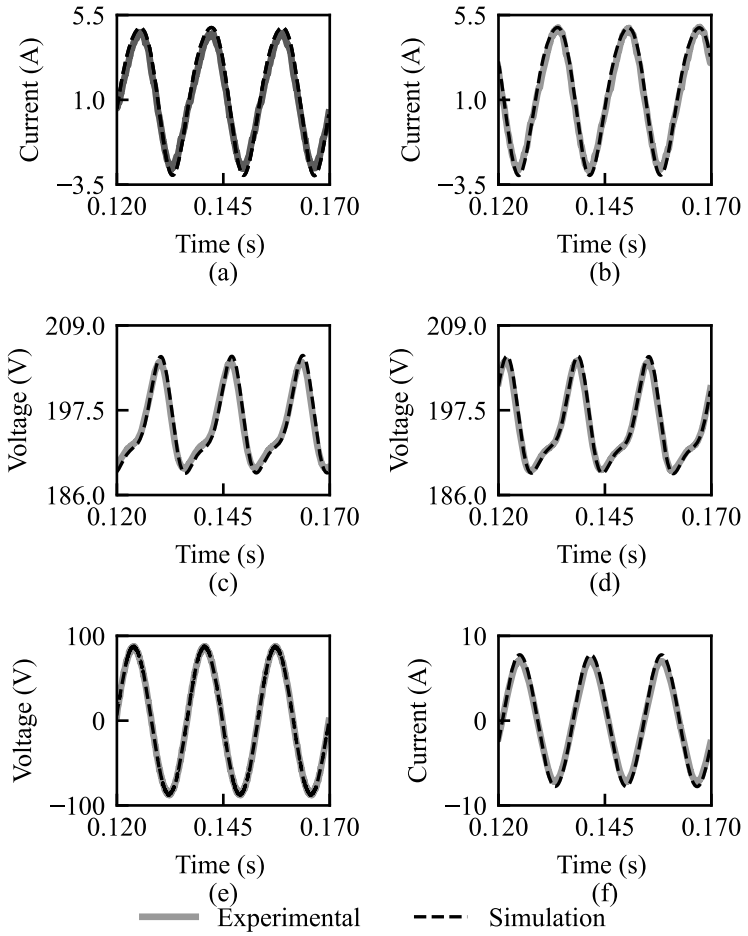


Figure 3.22: Low frequency waveforms with $I_{\text{ctrl}} = 1$ A (discharging). (a): top arm current, (b): bottom arm current, (c): sum of top capacitor voltages, (d): sum of bottom capcitor voltages, (e): terminal voltage, (f): load current.

The transient responses of the DC current to step changes in the reference peak current are also shown in Figure 3.24. In this experiment, the DC current is achieved by passing the circulating current into a first-order filter with a time-constant of 0.1 s to eliminate the second- and higher-order harmonics. As shown in Figure 3.24, the DC current decreases when the reference peak current of the battery (or inductor) is increased and vice versa. Furthermore, the results of simulations and experiments show excellent conformity.

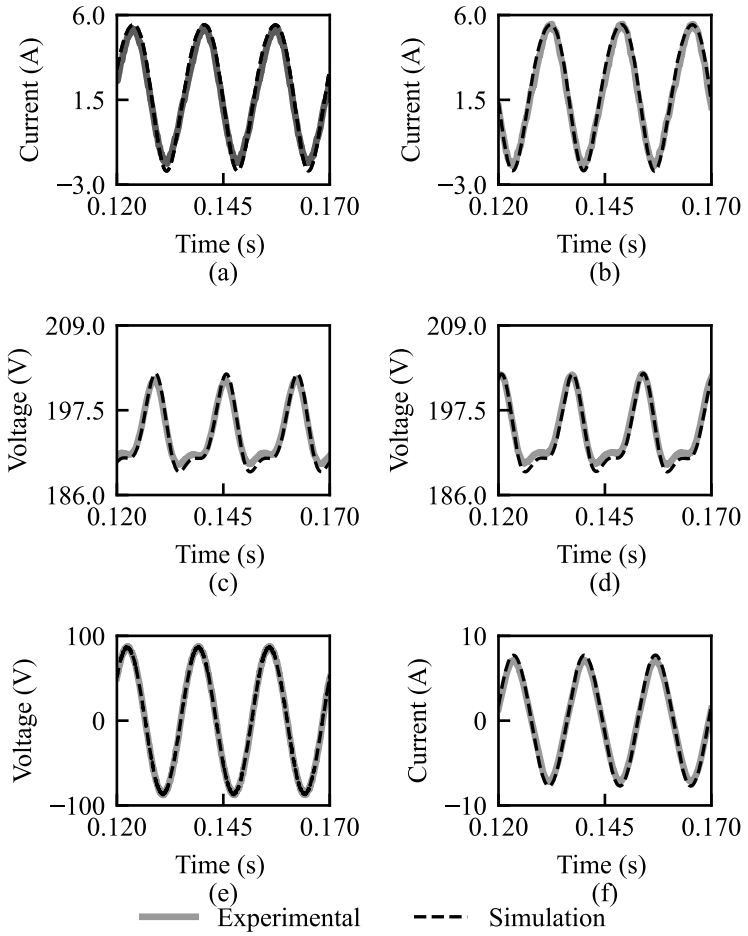


Figure 3.23: Low frequency waveforms with $I_{\text{ctrl}} = -0.8$ A (charging). (a): top arm current, (b): bottom arm current, (c): sum of top capacitor voltages, (d): sum of bottom capcitor voltages, (e): terminal voltage, (f): load current.

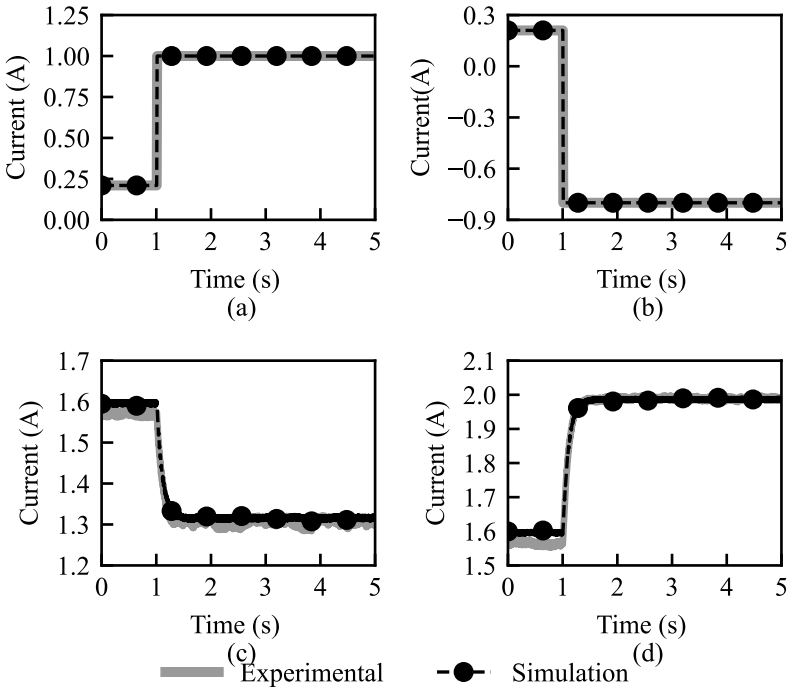


Figure 3.24: Dynamic response of the DC current to peak current command variations. (a),(b): peak current, (c),(d): DC current.

3.3 Computational Efficiency of the Developed DEM

This section studies computational efficiency of the proposed model. The performance of the proposed DEM is compared against that of DSM wherein the MMC-BESS is built with individual switching elements, i.e., IGBTs, diodes, and passive elements. A three-phase MMC with fully-integrated BESS supplying a three-phase RL load is considered as shown in Figure 3.25. The simulation is carried out by changing the number of SMs in each run. Note that the peak current is set to zero and the SM capacitance is updated so that the equivalent arm capacitance, $C_{\text{arm}} = C_{\text{sm}}/N$, remains constant at $600\,\mu$F. The battery voltage is also modified for each case so that the ratio of the battery voltage to that of the SM capacitor is kept constant at 0.6. The inductance and switching

frequency of the DC-DC converter are set to 9 mH and 1 kHz, respectively. Each case is simulated for 1 second with the time-step of 50 $\mu\mathrm{s}$ in the PSCAD/EMTDC simulator on a computer with 12th Gen Intel(R) Core(TM) i7-12700 2.10 GHz CPU and 32.0 GB installed RAM. To remove the impact of plotting on the CPU run time, all graphs are removed after having validated the accuracy of waveforms. Figure 3.26 shows the CPU run time versus the number of SMs for the DSM and the proposed DEM. It is evident that the run time grows exceedingly large with the number of SMs for DSMs while it stays essentially constant for the DEMs. It must be noted that practical BESS-MMC circuits will have considerably larger SM counts that the numbers used in this illustrative example, and as such the computational efficiency the of developed DEM is anticipated to be orders of magnitude better than a DSM for practical BESS-MMCs.

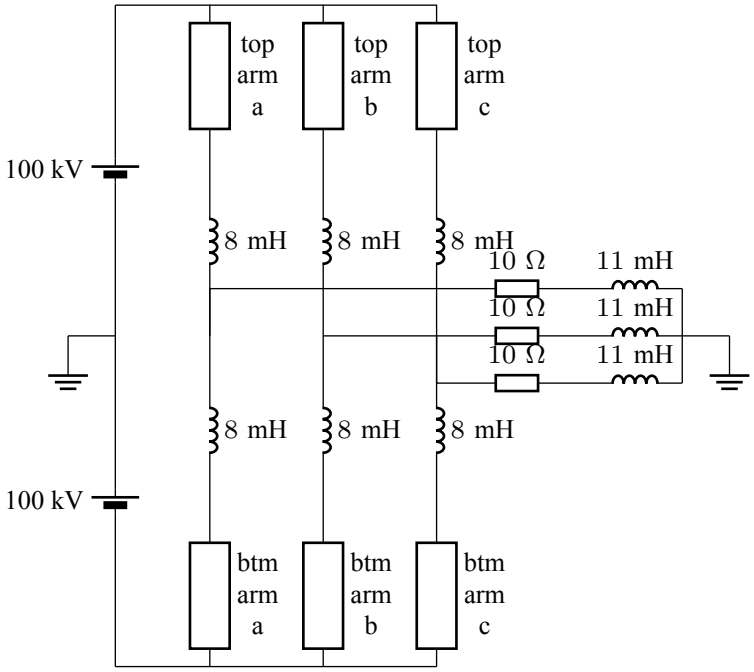


Figure 3.25: Case study for computational efficiency.

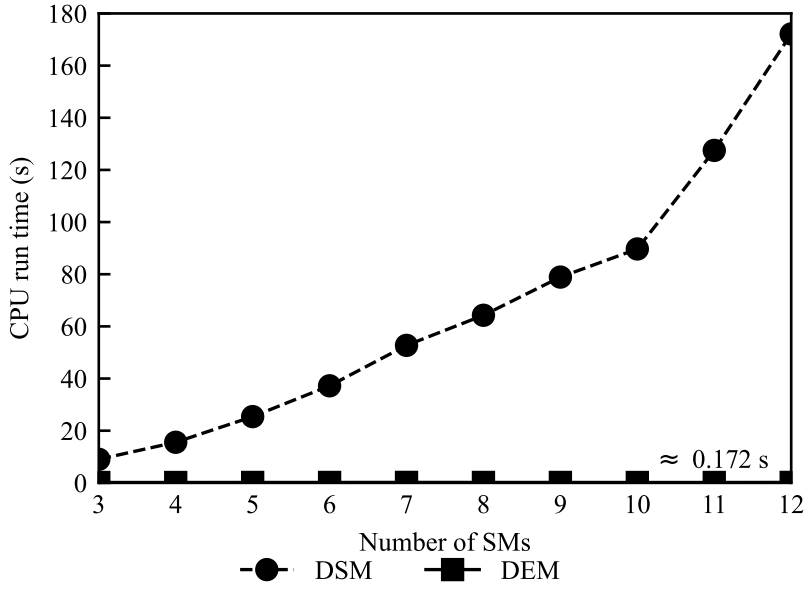


Figure 3.26: CPU run time vs. number of SMs.

3.4 Numerical Stability and Accuracy

Euler's method of integration is not A-stable and will become numerically unstable if the time-step exceeds certain limits. This limit is determined by the maximum value of the eigenvalues of the discretized state-space matrix of the circuit provided that all state variables are discretized with the Euler's method. In this thesis, however, only the stack of SMs are discretized with Euler's method and the rest of the circuit including the arm inductors, transmission lines, transformers, etc, are modeled with the trapezoidal method as shown in Figure 3.27(a). This mixture of integration methods is also not A-stable but its margin of stability is greater than that of the case where all components are constructed with the Euler's method.

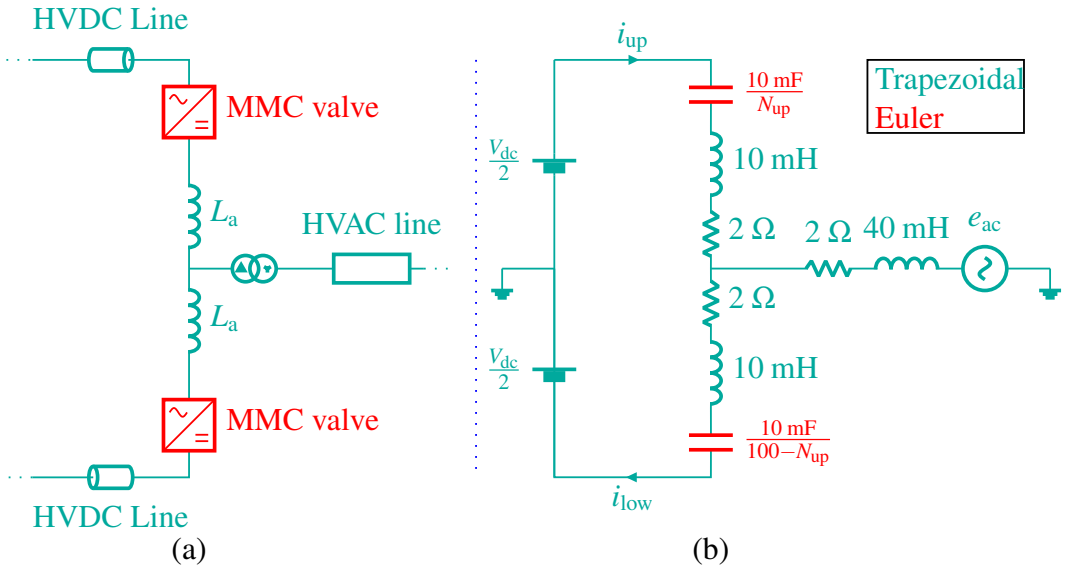


Figure 3.27: A network modeled with mixed integration method.

Figure 3.27(b) shows an example of an MMC with 100 SMs in normal mode in which, at every moment, N_{up} and $100 - N_{up}$ capacitors are inserted in the upper and lower arms, respectively. By performing circuit analysis, the state-space equation in the discrete domain may be written as follows:

$$\mathbf{X}(t) = \mathbf{G}(\Delta t)\mathbf{X}(t - \Delta t) + \text{effects of the inputs} \tag{3.2}$$

where $\mathbf{X}$ is the states and $\mathbf{G}$ is the discretized state-space matrix, which is a function of Δt. For all possible number of SMs inserted, the maximum time-step beyond which the simulations are numerically unstable are calculated and plotted in Figure 3.28. As shown, the worst-case maximum time-step is around 670 µs, which is 13 times larger than 50 µs, the typical time-step in power system applications.

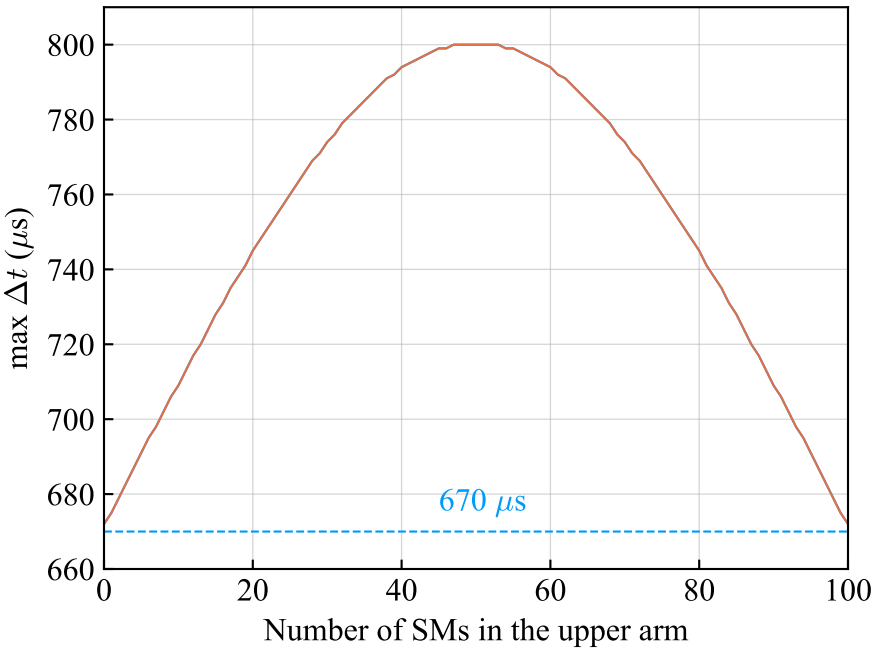


Figure 3.28: Maximum time-step vs. number of SMs inserted from upper (lower) arm.

For a network with switching elements the eigenvalues are not the only determinant of the maximum time-step. In fact, switching frequencies and time durations by which the circuit undergoes different states are of significant importance for if the time-step is not small enough, switching events will be missed. Heuristically, one tenth of the minimum switching period is considered for selecting the time-step.

In MMCs, the voltage generated by the stack of SMs is a staircase quantized sinusoidal waveform. Assuming that time intervals in the staircase waveform are equal, the length of each interval is $\frac{1}{Nf}$ where N and f are the number of SMs and frequency of the AC network, respectively. For instance, if the MMC has 100 SMs per arm and the AC network frequency is 60 Hz, the length of each interval would be $\frac{1}{100\times60} = 166.66$ µs meaning that the maximum time-step is 166.66 µs.

Such a rough calculation is specifically useful for MMCs controlled by the Nearest Level Control method. In PWM-controlled MMCs the recommended time-step is one tenth of the switching period of the PWM signal. For example, if the PWM signal has a frequency of 1 kHz, the recommended time-step would be $\frac{1}{10\times1000} = 100$ µs. Hence, a typical time-step in MMC simulations does not usually exceed 150 µs and for a common time-step of 50 µs, it is highly unlikely that the proposed mixed integration method becomes numerically unstable or inaccurate for (i) all elements except the stack of SMs are modeled with the trapezoidal integration method and (ii) the time-step must be inherently small enough to avoid missing switching events. The results of simulation case studies presented in this chapter validate the stability and accuracy of the proposed method.

3.5 Chapter Contributions

A novel detailed equivalent model was introduced for EMT simulation of MMCs with partially-integrated BESS. The developed DEM offers significant reductions in computational load by diminishing the number of nodes that are interconnected to other nodes in the structure of the MMC. Except when blocking is invoked, the proposed DEM eliminates time-varying electrical conductances, thereby avoiding re-factorization of the admittance matrix; this further helps its computational efficiency. State variables such as SM capacitor voltages and DC-DC inductor currents are also computed and are accessible for control purposes such as NLC modulation method and battery current control. To study the performance of the MMC-BESS, the PCM control strategy was introduced by which the battery current, and hence its power, is controlled with a simple circuitry. Different modes of operation such as charging, discharging, and idle mode can be prompted by adjusting the peak current to a positive value, negative value, and zero, respectively. Moreover, PCM adds a protection layer limiting current of the battery and DC-DC converters' switches. The model's

computational advantage was demonstrated against a conventional DSM, and it was observed that orders of magnitude improvement in computational efficiency are achieved. The accuracy of the DEM was validated using experimental results from a single-phase down-scaled version of the MMC-BESS. Furthermore, it was shown that using Euler's method does not adversely affect the stability of the models.

Chapter 4

Average Value Modeling of MMC-BESS

4.1 Average Value Modeling of DC-DC Converters

To obtain the average value model, the moving average operator, as described in (4.1), is utilized.

$$\langle x(t)\rangle_{T_\mathrm{s}} = \frac{1}{T_\mathrm{s}} \int_{t-\frac{T_\mathrm{s}}{2}}^{t+\frac{T_\mathrm{s}}{2}} x(\tau)\ \mathrm{d}\tau \tag{4.1}$$

This operator calculates the average of the input signal, $x(t)$ over a switching period, T_s, centered around a specified time, t. It is important to note that the output of this operator can vary with time. This operator is a linear operator for which the frequency response may be derived using Fourier transform. Recall that the Fourier transform of a signal $x(t)$ is defined as

$$\mathcal{F}\{x(t)\}(f) = \int_{-\infty}^{+\infty} x(t) e^{-\mathrm{j}2\pi f t}\, \mathrm{d}t \tag{4.2}$$

where f denotes the frequency in Hz. Taking the derivative of (4.1) and applying the Fourier transform yield the following equations

$$\frac{\mathrm{d}}{\mathrm{dt}}\langle x(t)\rangle_{T_\mathrm{s}} = \frac{x(t+\frac{T_\mathrm{s}}{2}) - x(t-\frac{T_\mathrm{s}}{2})}{T_\mathrm{s}} \tag{4.3}$$

$$\mathrm{j}2\pi f\mathcal{F}\{\langle x(t)\rangle_{T_\mathrm{s}}\}(f) = \frac{e^{\mathrm{j}\pi T_\mathrm{s} f} - e^{-\mathrm{j}\pi T_\mathrm{s} f}}{T_\mathrm{s}}\mathcal{F}\{x(t)\}(f) \tag{4.4}$$

from which the frequency response of the moving average operator may be expressed as

$$\frac{\mathcal{F}\{\langle x(t)\rangle_{T_\mathrm{s}}\}(f)}{\mathcal{F}\{x(t)\}(f)} = \mathrm{sinc}(\frac{f}{f_\mathrm{s}}) \tag{4.5}$$

where f_s is the switching frequency. Recall that the sinc function is defined as

$$\mathrm{sinc}(z) = \frac{\sin(\pi z)}{\pi z} \tag{4.6}$$

A typical switching-type signal and its average are plotted in Figure 4.1. As shown, the switching content of the actual waveform is removed when the moving average operator is applied. This is additionally explained in the frequency response plot of the operator, illustrated in Figure 4.2, where the switching frequency and its integer multiples are fully filtered out, while the DC-like nature of the waveform is passed with minimal attenuation.

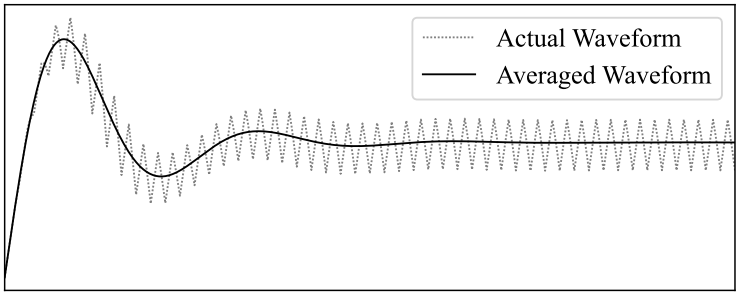


Figure 4.1: A typical time domain response of the moving average operator.

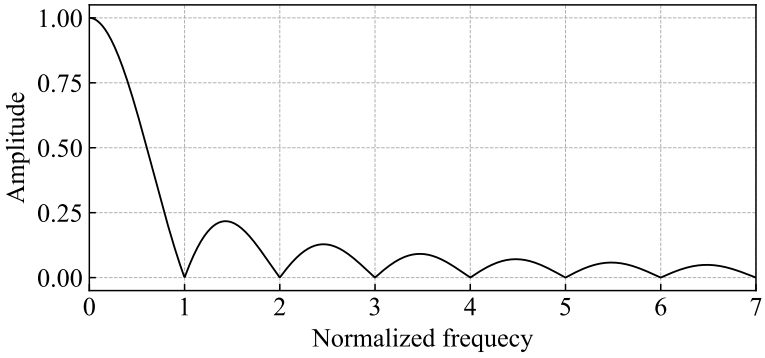


Figure 4.2: Frequency response of the moving average operator.

In applying the moving average operator for modeling power electronic converters, continuous waveforms such as *capacitor voltage* and *inductor current* are assumed to be constant over one switching period resulting in the following formula that is useful in the derivation of the averaged circuit model.

$$\begin{aligned}\langle \text{switched waveform} \rangle_{T_\text{s}} &= \frac{1}{T_\text{s}} \int_{t-\frac{T_\text{s}}{2}}^{t+\frac{T_\text{s}}{2}} (\text{continuous waveform}) \times (\text{switching function})\ \text{d}\tau \\ &\approx (\text{continuous waveform}) \times \frac{1}{T_\text{s}} \int_{t-\frac{T_\text{s}}{2}}^{t+\frac{T_\text{s}}{2}} (\text{switching function})\ \text{d}\tau \\ &= (\text{continuous waveform}) \times (\text{duty cycle}) \end{aligned} \tag{4.7}$$

The circuit model of the DC-DC converter derived in chapter 2 is shown in Figure 4.3. By using the formula in (4.7), the dependent voltage and current sources in Figure 4.3, which are expressed with switching function $q(t)$, are replaced with their respective averaged model as shown in Figure 4.4. Note that new dependent sources are now expressed in terms of the duty cycle, $d(t)$. The obtained model can be further reduced to an alternative equivalent model, depicted in Figure 4.5, realizing that the combination of the two dependent sources represents an ideal transformer with

the turns ratio of $(1 - d(t)) : 1$.

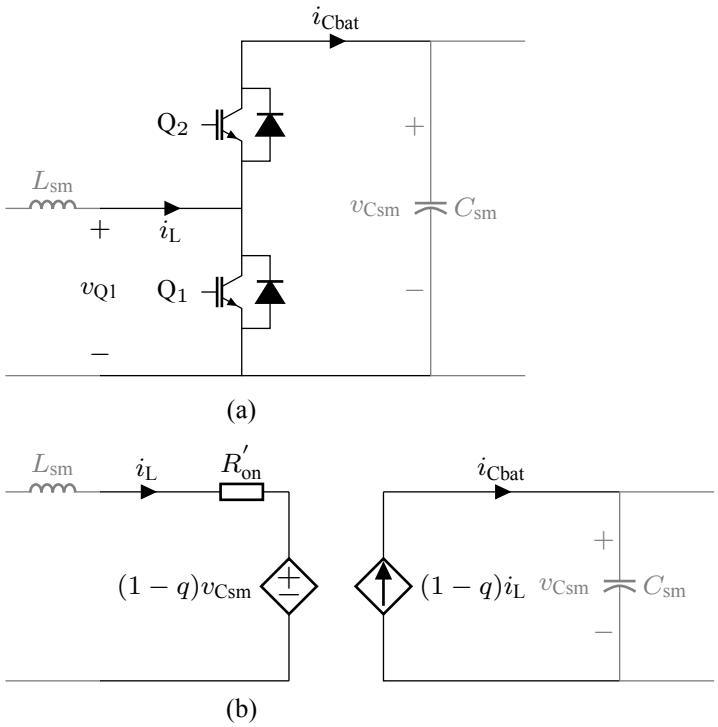


Figure 4.3: DC-DC converter switch cell and its equivalent model.

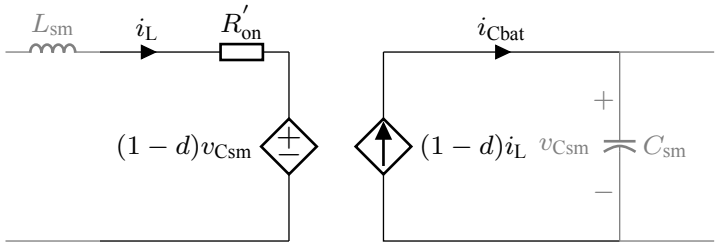


Figure 4.4: AVM of the DC-DC converter switch cell represented by dependent sources.

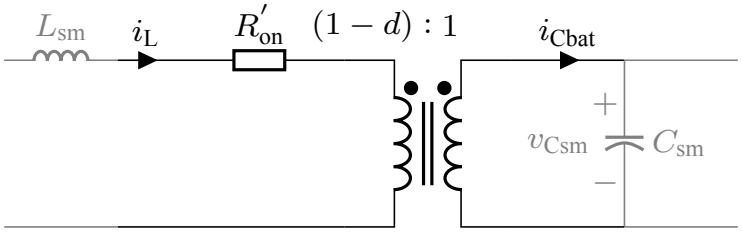


Figure 4.5: AVM of the DC-DC converter switch cell represented by ideal transformer.

The obtained averaged model of the DC-DC converter is primarily used for regulating the output voltage. This regulation is achieved by continuously adjusting the turns ratio of the ideal transformer and/or the duty cycle, $d(t)$, via a feedback loop. However, this type of control is not suitable for BESS integration in MCCs because both the input and output voltages of the DC-DC converter are nearly constant. The input terminal of the converter is connected to the battery, which provides an almost constant voltage regardless of the load. The output terminal of the converter is connected to the SM capacitor, which maintains the voltage within a limited range thanks to the HVDC voltage control loop and the NLC scheme of switching that balances all SM capacitor voltages.

Assuming that the circuit components are ideal, the duty cycle may be expressed by

$$d = 1 - \frac{v_{\text{bat}}}{v_{\text{Csm}}} = 1 - N\frac{v_{\text{bat}}}{v_{\text{dc}}} \tag{4.8}$$

where N, v_{bat}, v_{Csm}, and v_{dc} are the total number of SMs in one arm, battery voltage, SM capacitor voltage, and DC line voltage, respectively. This relationship indicates that the duty cycle must remain constant provided that the battery and DC line voltage are constant. More importantly, the duty cycle is not related to the current, suggesting that the battery power, whether in charging or discharging mode, cannot be regulated with the duty cycle. However, if parasitic elements such as

inductor series resistance and *switch ON resistance* are taken into account, the duty cycle becomes dependent on the current. Thus, it appears possible to have the duty cycle as a function of current to control the converter. However, this is not practical since the values of parasitic elements are not fixed and vary with temperature and operating conditions. Even with known non-ideal components, there is limited scope to adjust the duty cycle.

Average value of the indutor current is almost equal to the peak current in the PCM control mode assuming that the ripple component of inductor current is negligible.

$$\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}} \approx i_{\mathrm{ctrl}} \tag{4.9}$$

Thus, the primary (left) side of the transformer in Figure 4.5 is derived with an independent current source whose value is determined by the upstream control of MMC-BESS. The current in the secondary (right) side of the transformer is then calculated as follows.

$$\begin{aligned}\langle i_{\mathrm{Cbat}}(t)\rangle_{T_{\mathrm{s}}} &= (1-d)\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}} &(4.10)\\ &= \frac{\langle v_{\mathrm{Q1}}(t)\rangle_{T_{\mathrm{s}}} - R'_{\mathrm{on}}\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}}}{\langle v_{\mathrm{Csm}}(t)\rangle_{T_{\mathrm{s}}}}\langle i_{\mathrm{L}}(t)\rangle_{T_{\mathrm{s}}} \\ &= \frac{\langle v_{\mathrm{Q1}}(t)\rangle_{T_{\mathrm{s}}} - R'_{\mathrm{on}} i_{\mathrm{ctrl}}}{\langle v_{\mathrm{Csm}}(t)\rangle_{T_{\mathrm{s}}}} i_{\mathrm{ctrl}} &(4.11)\end{aligned}$$

Note that the intermediate variable d is eliminated from the expression. Equation (4.11) suggests an equivalent circuit, depicted in Figure 4.6, that will be used hereafter in the derivation of the AVM for entire MMC-BESS.

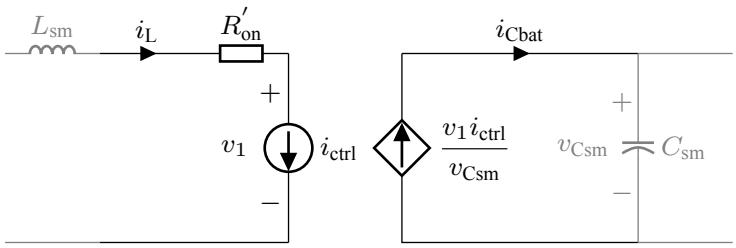


Figure 4.6: Averaged equivalent circuit of the DC-DC converter operated with PCM control.

4.2 Average Value Modeling of the Stack of SMs

A single BESS-SM consists of the DC-DC converter followed by the main SM switch cell. The SM switch cell is modeled by a combination of dependent current and voltage sources that are determined by the switching function and terminal values. By connecting the AVM of the DC-DC converter, as in Figure 4.6, to the main switch cell, the SM-BESS may be represented by Figure 4.7.

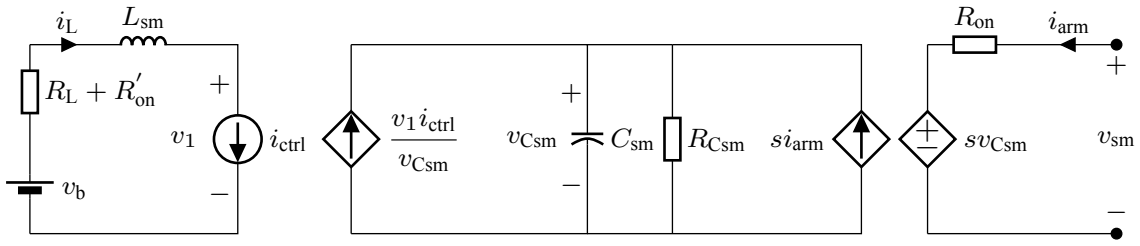


Figure 4.7: Averaged model of SM-BESS with PCM control.

To achieve the averaged model of the arm, the following assumptions are made.

1. All batteries are balanced and hold identical instantaneous voltage, i.e.,

$$v_{\text{b}1}(t) = v_{\text{b}2}(t) = \cdots = v_{\text{b}M}(t) \triangleq v_{\text{b}}(t) \tag{4.12}$$

2. All SM capacitors hold identical instantaneous voltage, i.e.,

$$\langle v_{\text{Csm1}}\rangle_{T_\text{s}}(t) = \langle v_{\text{Csm2}}\rangle_{T_\text{s}}(t) = \cdots = \langle v_{\text{Csm}M}\rangle_{T_\text{s}}(t) = v_{\text{Csm}M+1}(t) = \cdots = v_{\text{Csm}N}(t) \triangleq v_{\text{Csm}}(t) \tag{4.13}$$

3. All the inductors in BESS-SMs carry identical instantaneous moving-average current, i.e.,

$$\langle i_{\text{L1}}\rangle_{T_\text{s}}(t) = \langle i_{\text{L2}}\rangle_{T_\text{s}}(t) = \cdots = \langle i_{\text{L}M}\rangle_{T_\text{s}}(t) \triangleq i_{\text{L}}(t) \tag{4.14}$$

4. All the inductors are commanded the same reference peak current, i.e.,

$$i_{\text{ctrl1}}(t) = i_{\text{ctrl2}}(t) = \cdots = i_{\text{ctrl}M}(t) \triangleq i_{\text{ctrl}}(t) \tag{4.15}$$

From the circuit point of view, equations (4.13) and (4.14) are fictitious KVL and KCL equations. These imply that all SM and BESS-SM capacitors, along with the surrounding circuitry, are effectively in parallel, while all BESS-SM inductors and the surrounding circuitry are effectively in series. The total voltage produced by stack of SMs are sum of the voltages across individual SMs and BESS-SMs. Thus, the first representation of the averaged model for the stack of SMs may be achieved as shown in Figure 4.8. By defining *modulation waveform* as

$$m(t) \triangleq \frac{s_1(t) + s_2(t) + \cdots + s_N(t)}{N} = \frac{\sum s(t)}{N} \tag{4.16}$$

the second representation of the model is obtained at Figure 4.9. A capacitor with the capacitance of C being injected with the current i produces the same voltage as a capacitor with the capacitance of $\frac{C}{k}$ with the current of $\frac{i}{k}$. Similar statement can be made for the resistive element that results in the upgraded version of equivalent circuit as shown in Figure 4.10 where the voltage of the capacitor is

still indicating the voltage of individual SM capacitor. Note also that the number of SM, N, appears in the expression of the total voltage produced by stack of SMs. In order to eliminate the parameter N, an equivalent capacitor and resistor, $C_{\text{eq}} = \frac{C_{\text{sm}}}{N}$ and $R_{\text{Ceq}} = NR_{\text{Csm}}$ are defined such that the total voltage of $v_{\text{Ceq}} = Nv_{\text{Csm}}$ appears on them. By doing so, the equivalent circuit is evolved into version 4 and 5 as shown in Figures 4.11 and 4.12, respectively. Hereafter, the version 5 will be used for the rest of the thesis.

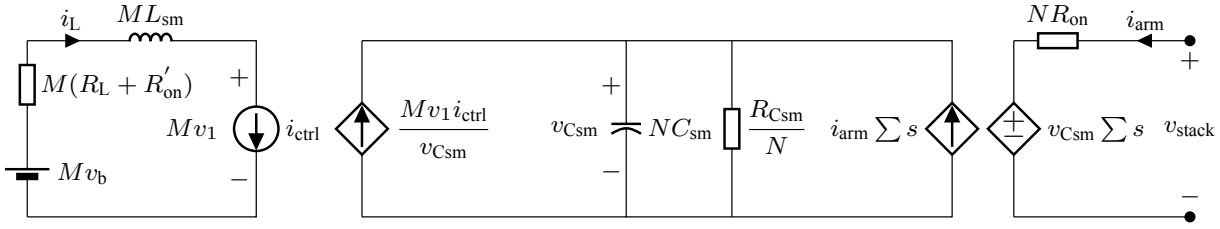


Figure 4.8: Averaged model of stack of SMs, version 1.

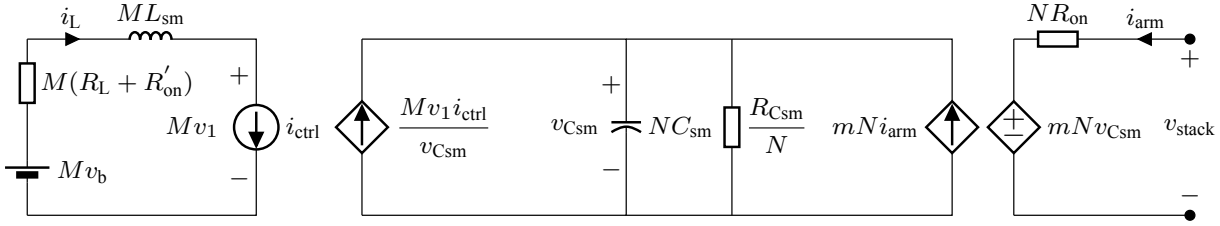


Figure 4.9: Averaged model of stack of SMs, version 2.

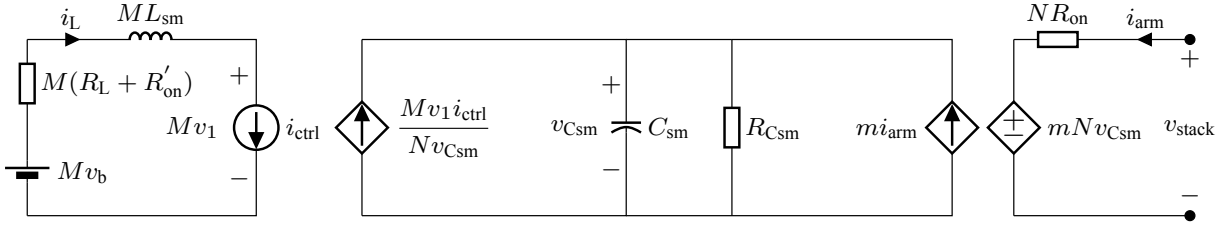


Figure 4.10: Averaged model of stack of SMs, version 3.

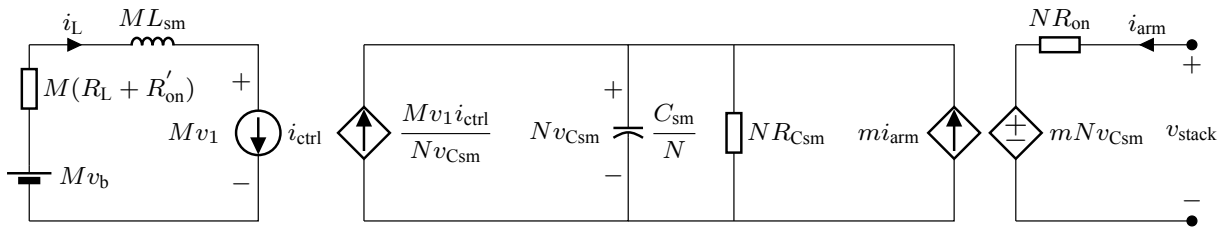


Figure 4.11: Averaged model of stack of SMs, version 4.

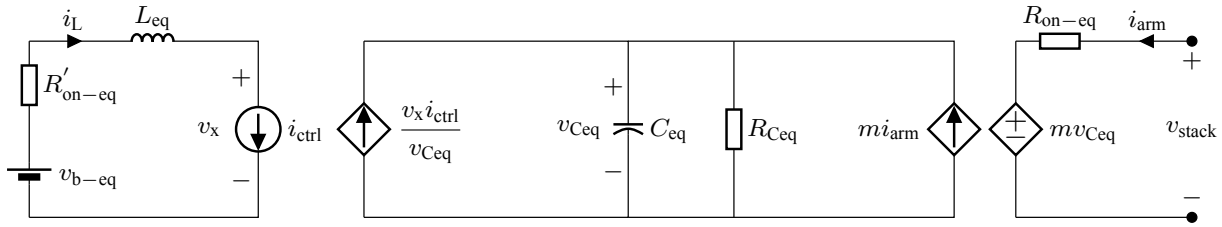


Figure 4.12: Averaged model of stack of SMs, version 5.

4.3 Average Value Modeling of the Entire Converter

Figure 4.13 shows a single phase of the MMC-BESS with averaged value model that is created by connecting the upper and lower arms including respective arm inductors L_{a}. The total resistance of the stack of SMs augmented with the equivalent series resistance of the arm inductor are lumped into the arm resistor denoted as R_{a}. Note that, the combination of the dependent sources representing the behavior of the sack of SMs, shown in Figure 4.12, is modified into the ideal transformer representation as depicted in Figure 4.13. To achieve a more simplified model that is able to represent the converter's behavior viewed from its DC and AC terminal, KVL and KCL equations are analysed as follows.

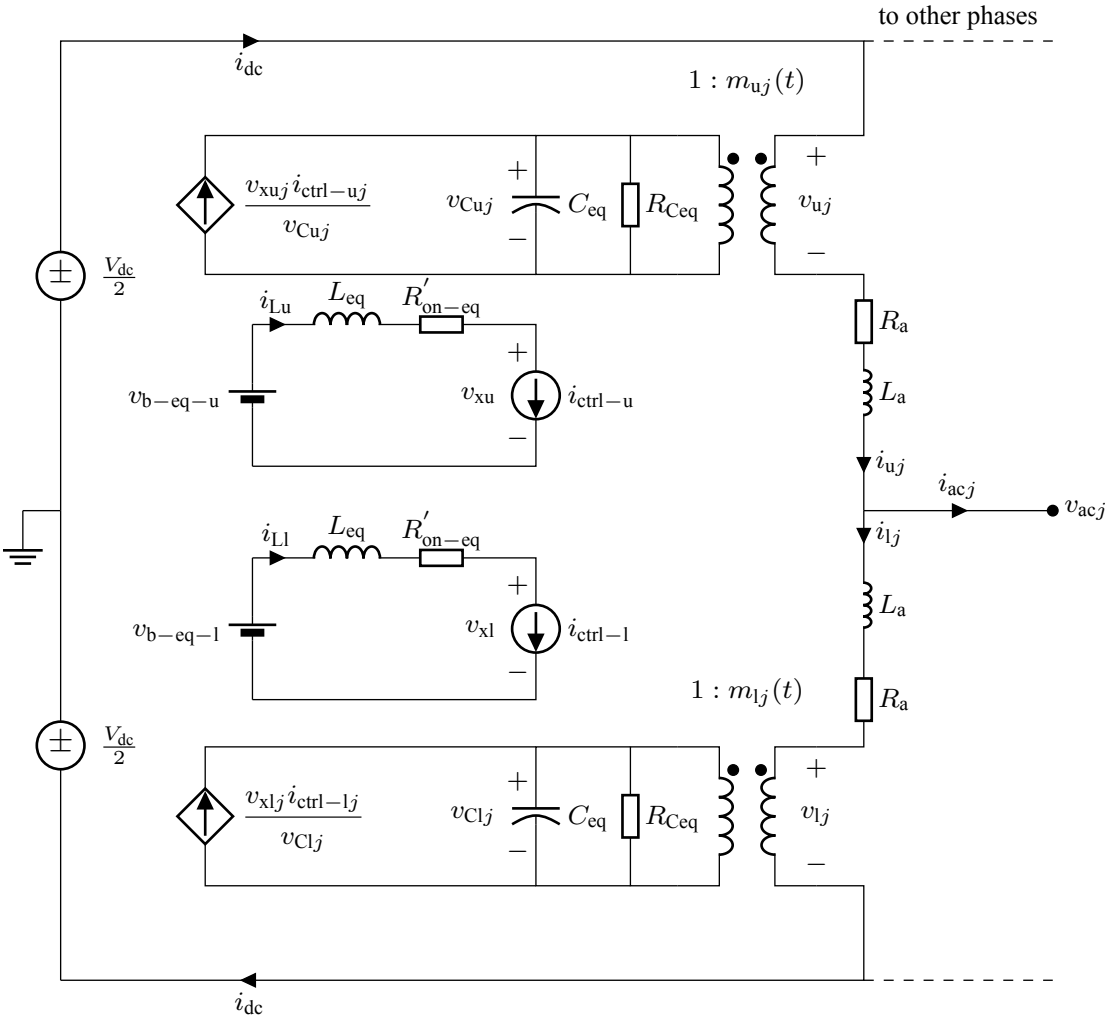


Figure 4.13: Single phase representation of the MMC-BESS with AVM.

4.3.1 KVL analysis

Two KVL equations from the positive and negative DC rail to the AC terminal of the converter may be written for phase j as follows.

$$\frac{V_{\text{dc}}}{2} - v_{\text{ac}j}(t) = m_{\text{u}j} v_{\text{Cu}j} + L_{\text{a}} \frac{\text{d}i_{\text{u}j}}{\text{d}t} + R_{\text{a}} i_{\text{u}j} \tag{4.17}$$

$$\frac{V_{\text{dc}}}{2} + v_{\text{ac}}(t) = m_{\text{l}j} v_{\text{Cl}j} + L_{\text{a}} \frac{\text{d}i_{\text{l}j}}{\text{d}t} + R_{\text{a}} i_{\text{l}j} \tag{4.18}$$

Summation and subtraction of these equations results in

$$\begin{aligned} V_{\text{dc}} &= m_{\text{u}j} v_{\text{Cu}j} + m_{\text{l}j} v_{\text{Cl}j} + 2L_{\text{a}} \frac{\text{d}i_{\text{circ}j}}{\text{d}t} + 2R_{\text{a}} i_{\text{circ}j} \\ &= \frac{v_{\text{Cu}j} + v_{\text{Cl}j}}{2} + \frac{v_{\text{Cl}j} - v_{\text{Cu}j}}{2} m_j + 2L_{\text{a}} \frac{\text{d}i_{\text{circ}j}}{\text{d}t} + 2R_{\text{a}} i_{\text{circ}j} \end{aligned} \tag{4.19}$$

$$\begin{aligned} v_{\text{ac}j} &= \frac{m_{\text{l}j} v_{\text{Cl}j} - m_{\text{u}j} v_{\text{Cu}j}}{4} - \frac{L_{\text{a}}}{2} \frac{\text{d}i_{\text{diff}j}}{\text{d}t} - \frac{R_{\text{a}}}{2} i_{\text{diff}j} \\ &= \frac{v_{\text{Cl}j} - v_{\text{Cu}j}}{4} + \frac{v_{\text{Cu}j} + v_{\text{Cl}j}}{4} m_j - \frac{L_{\text{a}}}{2} \frac{\text{d}i_{\text{diff}j}}{\text{d}t} - \frac{R_{\text{a}}}{2} i_{\text{diff}j} \end{aligned} \tag{4.20}$$

where the circulating and differential current is defined as

$$i_{\text{diff}j} \triangleq i_{\text{u}j} - i_{\text{l}j} = i_{\text{ac}j} \tag{4.21}$$

$$i_{\text{circ}j} \triangleq \frac{i_{\text{u}j} + i_{\text{l}j}}{2} \tag{4.22}$$

The number of SMs inserted from upper and lower arm are added up to the total number of SMs in the single arm. Thus, the summation of the respective modulation waveforms, i.e. $m_{\text{u}j}$ and $m_{\text{l}j}$ are added to unity and , in turn, they can be express as

$$m_{\text{u}j} = \frac{1}{2}(1 - m_j) \tag{4.23}$$

$$m_{\text{l}j} = \frac{1}{2}(1 + m_j) \tag{4.24}$$

where m_j is the modulation/reference waveform of the phase j. Neglecting the ripple component of the capacitor voltage, both in upper and lower arm, (4.19) and (4.20) may be simplified into

$$V_{\text{dc}} = v_{\text{C}j} + 2L_{\text{a}}\frac{\text{d}i_{\text{circ}j}}{\text{d}t} + 2R_{\text{a}}i_{\text{circ}j} \tag{4.25}$$

$$v_{\text{ac}j} = \frac{m_j}{2}v_{\text{C}j} - \frac{L_{\text{a}}}{2}\frac{\text{d}i_{\text{diff}j}}{\text{d}t} - \frac{R_{\text{a}}}{2}i_{\text{diff}j} \tag{4.26}$$

where $v_{\text{C}j}$ is considered as the average of the voltage of capacitors in upper and lower arms. Summing up (4.25) over phases *a, b*, and *c*, and results in

$$V_{\text{dc}} = v_{\text{C}} + \frac{2}{3}L_{\text{a}}\frac{\text{d}i_{\text{dc}}}{\text{d}t} + \frac{2}{3}R_{\text{a}}i_{\text{dc}} \tag{4.27}$$

where v_{C} is the voltage of the total representative capacitor that is average of the all SM capacitors in a three phase MMC-BESS, defined in the following equation.

$$v_{\text{C}} \triangleq \frac{1}{3}\sum_{j\in\{\text{a,b,c}\}} v_{\text{C}j} \tag{4.28}$$

4.3.2 KCL analysis

KCL equation at the capacitor nodes both in upper and lower arms can be written as follows.

$$C_{\text{eq}}\frac{\text{d}v_{\text{Cu}j}}{\text{d}t} + \frac{v_{\text{Cu}j}}{R_{\text{Ceq}}} = m_{\text{u}j}i_{\text{u}j} + \frac{v_{\text{xu}j}i_{\text{ctrl-u}j}}{v_{\text{Cu}j}} \tag{4.29}$$

$$C_{\text{eq}}\frac{\text{d}v_{\text{Cl}j}}{\text{d}t} + \frac{v_{\text{Cl}j}}{R_{\text{Ceq}}} = m_{\text{l}j}i_{\text{l}j} + \frac{v_{\text{xl}j}i_{\text{ctrl-l}j}}{v_{\text{Cl}j}} \tag{4.30}$$

Considering that the voltage of batteries and reference current are identical in both upper and lower arms, summation of the above equations is simplified into the one expressed as follows.

$$2C_{\text{eq}}\frac{\mathrm{d}v_{\text{C}j}}{\mathrm{d}t}+2\frac{v_{\text{C}j}}{R_{\text{Ceq}}}=i_{\text{circ}j}-\frac{m_j}{2}i_{\text{ac}j}+2\frac{v_{\text{x}j}i_{\text{ctrl}j}}{v_{\text{C}j}} \tag{4.31}$$

Th obtained equation can be further summed up over phases *a, b,*, and *c*, that leads to

$$6C_{\text{eq}}\frac{\mathrm{d}v_{\text{C}}}{\mathrm{d}t}+6\frac{v_{\text{C}}}{R_{\text{Ceq}}}=i_{\text{dc}}-\frac{1}{2}\sum_{j\in\{\text{a,b,c}\}}m_j i_{\text{ac}j}+6\frac{v_{\text{x}}i_{\text{ctrl}}}{v_{\text{C}}} \tag{4.32}$$

The combination of equations (4.26), (4.27), and (4.32) reveals a compact equivalent circuit of the MMC-BESS from the perspective of its terminal points as shown in Figure 4.14.

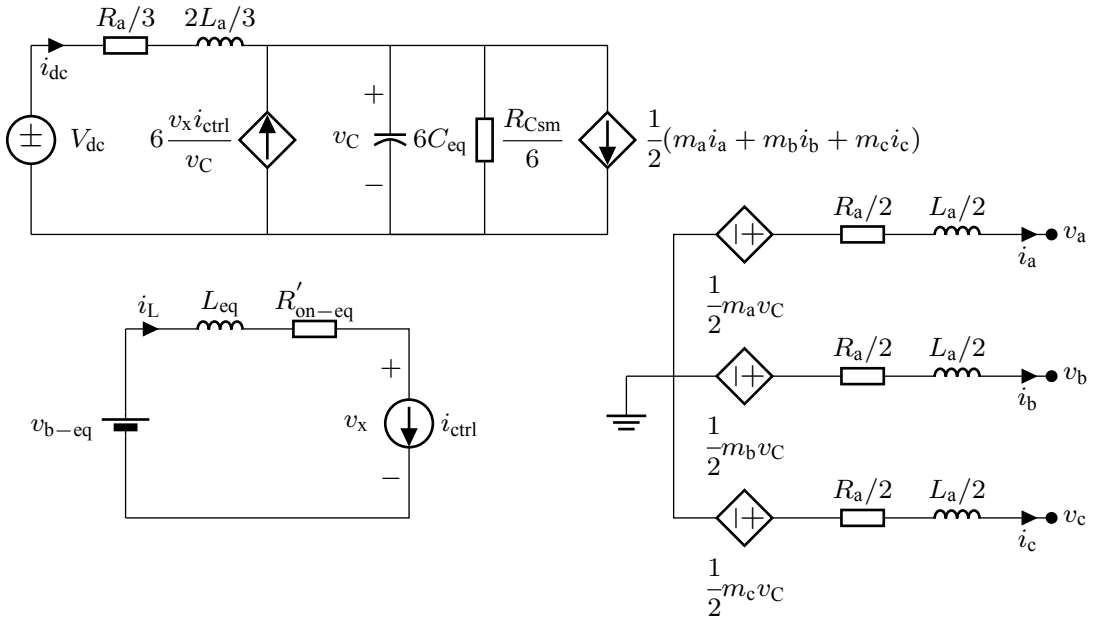


Figure 4.14: Single phase representation of the MMC-BESS with AVM.

4.4 Per-unitization of the MMC-BESS System

Expressing a power-electronic converter system in per-unit terms is often more convenient than in original units. This technique involves normalizing values to a common base, thereby facilitating more straightforward analysis, comparison, and system modeling, as outlined in the following per-unitization system.

As shown in Figure 4.14, there exist three circuits each of which represents different terminals of the converter. A common power or MVA base S_{B} is chosen for all circuits. The base power is usually selected as identical to the MVA rating the converter. The base voltage of the HVDC link, V_{Bdc}, is chosen as the rated HVDC voltage at which the converter is operated. The base DC voltage for the battery side is chosen to be the nominal voltage of the individul battery unit multiplied by the number of BESS-SMs inserted in each arm. The base currents for DC, AC and battery side are then calculated according to the following rules.

$$S_{\mathrm{B}} = V_{\mathrm{Bdc}} I_{\mathrm{Bdc}} = \frac{3}{2} V_{\mathrm{Bac}} I_{\mathrm{Bac}} = 6 V_{\mathrm{Bbat}} I_{\mathrm{Bbat}} \tag{4.33}$$

Note that the base voltage and current for the AC side are chosen as the peak value of the line-to-neutral voltage and peak value of the line current, respectively; this is in contrast to the conventional per-unit system by which the rms line-to-neutral voltage and rms line current are used as bases in AC power systems. The base voltage of the AC side circuit is chosen to be $2V_{\mathrm{Bdc}}$ so that the 1.0 pu DC voltage yields 1.0 pu open-circuit peak voltage at unity modulation index [93]. Hence, the relationship between the base DC and AC currents can be derived using (4.33) as follows.

$$V_{\mathrm{Bac}} = 2 V_{\mathrm{Bdc}} \tag{4.34}$$

$$I_{\mathrm{Bdc}} = \frac{3}{4} I_{\mathrm{Bac}} \tag{4.35}$$

The base impedances of various sides are calculated as follows.

$$Z_{\text{Bdc}} = \frac{V_{\text{Bdc}}}{I_{\text{Bdc}}} \tag{4.36}$$

$$Z_{\text{Bac}} = \frac{V_{\text{Bac}}}{I_{\text{Bac}}} \tag{4.37}$$

$$Z_{\text{Bbat}} = \frac{V_{\text{Bbat}}}{I_{\text{Bbat}}} \tag{4.38}$$

The base inductance at the AC side may be computed from the division of the corresponding base impedance by base angular frequency ω_{B} as in (4.39). It is important to highlight that, such definition for the DC and battery side is unintelligible since there is no frequency associated with these sides. Instead, the concept of *inertia* will be utilized to convert the energy storage components, i.e. capacitors and inductors, into per-unit-like values.

$$L_{\text{B}} = \frac{Z_{\text{Bac}}}{\omega_{\text{B}}} \tag{4.39}$$

The KVL equation in (4.27) may be rewritten in the following form where the actual quantities is represented by the product of their respective base and per-unit values.

$$V_{\text{Bdc}} V_{\text{dc}}^{\text{pu}} = V_{\text{Bdc}} v_{\text{C}}^{\text{pu}} + I_{\text{Bdc}} \left(\frac{2}{3} L_{\text{a}}\right) \frac{\text{d}i_{\text{dc}}^{\text{pu}}}{\text{d}t} + I_{\text{Bdc}} \left(\frac{2}{3} R_{\text{a}}\right) i_{\text{dc}}^{\text{pu}} \tag{4.40}$$

Defining *arm damping factor*, D_{a}, and *arm inertia constant*, H_{a}, as

$$D_{\text{a}} \triangleq \frac{\text{Resistance in the DC side}}{\text{Base impedance}} = \frac{2}{3} \frac{R_{\text{a}}}{Z_{\text{Bdc}}} = \frac{2}{3} R_{\text{a}} \frac{I_{\text{Bdc}}}{V_{\text{Bdc}}} \tag{4.41}$$

and

$$H_{\mathrm{a}} \triangleq \frac{\text{Stored energy in equivalent inductor at base dc current}}{\text{Base power}} = \frac{\frac{1}{3}L_{\mathrm{a}}I_{\mathrm{Bdc}}^{2}}{S_{\mathrm{B}}} \tag{4.42}$$

results in (4.43) expressed in per-unit. It is worthwhile to mention that the derivative is still taken with respect to the actual time; hence, the inertia constant, expressed in seconds or MJ/MVA, appears behind the derivative term.

$$V_{\mathrm{dc}}^{\mathrm{pu}} = v_{\mathrm{C}}^{\mathrm{pu}} + 2H_{\mathrm{a}}\frac{\mathrm{d}i_{\mathrm{dc}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{a}}i_{\mathrm{dc}}^{\mathrm{pu}} \tag{4.43}$$

The same per-unitization procedure can be applied to various equations corresponding to different parts of the circuit. Table 4.1 summarizes the per-unitized equations required for modeling the converter from it terminal point of view. The damping factor and inertia constants that are defined only for DC and battery side systems are listed in Table 4.2

Table 4.1: Terminal equations of MMC-BESS in per-unit

DC side KVL	$2H_{\mathrm{a}}\frac{\mathrm{d}i_{\mathrm{dc}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{a}}i_{\mathrm{dc}}^{\mathrm{pu}} = V_{\mathrm{dc}}^{\mathrm{pu}} - v_{\mathrm{C}}^{\mathrm{pu}}$
DC side KCL	$2H_{\mathrm{C}}\frac{\mathrm{d}v_{\mathrm{C}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{C}}v_{\mathrm{C}}^{\mathrm{pu}} = i_{\mathrm{dc}}^{\mathrm{pu}} - \frac{2}{3}(m_{\mathrm{a}}i_{\mathrm{a}}^{\mathrm{pu}} + m_{\mathrm{b}}i_{\mathrm{b}}^{\mathrm{pu}} + m_{\mathrm{c}}i_{\mathrm{c}}^{\mathrm{pu}}) + \frac{v_{\mathrm{x}}^{\mathrm{pu}}i_{\mathrm{ctrl}}^{\mathrm{pu}}}{v_{\mathrm{C}}^{\mathrm{pu}}}$
AC side KVL	$\frac{1}{2}\frac{L_{\mathrm{a}}^{\mathrm{pu}}}{\omega_{\mathrm{B}}}\frac{\mathrm{d}i_{\mathrm{ac}j}^{\mathrm{pu}}}{\mathrm{d}t} + \frac{R_{\mathrm{a}}^{\mathrm{pu}}}{2}i_{\mathrm{ac}j}^{\mathrm{pu}} = m_j v_{\mathrm{C}}^{\mathrm{pu}} - v_{\mathrm{ac}j}^{\mathrm{pu}} \quad ; \quad j \in \{\mathrm{a,b,c}\}$
Battery side KVL	$2H_{\mathrm{b}}\frac{\mathrm{d}i_{\mathrm{ctrl}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{b}}i_{\mathrm{ctrl}}^{\mathrm{pu}} = v_{\text{b-eq}}^{\mathrm{pu}} - v_{\mathrm{x}}^{\mathrm{pu}}$

Table 4.2: Definitions of damping factors and inertia constants

Damping factors	Inertia constants
$D_{\mathrm{a}} \triangleq \frac{2}{3}\frac{R_{\mathrm{a}}}{Z_{\mathrm{Bdc}}}$	$H_{\mathrm{a}} \triangleq \frac{1}{3}\frac{L_{\mathrm{a}} I_{\mathrm{Bdc}}^2}{S_{\mathrm{B}}}$
$D_{\mathrm{C}} \triangleq \frac{6 Z_{\mathrm{Bdc}}}{R_{\mathrm{Ceq}}}$	$H_{\mathrm{C}} \triangleq \frac{3 C_{\mathrm{eq}} V_{\mathrm{Bdc}}^2}{S_{\mathrm{B}}}$
$D_{\mathrm{b}} \triangleq \frac{R'_{\text{on-eq}}}{Z_{\mathrm{Bbat}}}$	$H_{\mathrm{b}} \triangleq \frac{1}{2}\frac{L_{\mathrm{eq}} I_{\mathrm{Bbat}}^2}{S_{\mathrm{B}}}$

4.5 DQ reference frame transformation

Definition

Considering three phase real-valued signals, $(x_{\mathrm{a}}(t), x_{\mathrm{b}}(t), x_{\mathrm{c}}(t))$, with no zero sequence component, i.e. $x_{\mathrm{a}}(t) + x_{\mathrm{b}}(t) + x_{\mathrm{c}}(t) = 0$, the dq transformation is defined as

$$\mathbf{X}(t) = x_{\mathrm{d}} + \mathrm{j}x_{\mathrm{q}} = \mathbf{T}\Big\{(x_{\mathrm{a}}(t), x_{\mathrm{b}}(t), x_{\mathrm{c}}(t))\Big\}(\theta) = \frac{2}{3}\left(e^{\mathrm{j}0} x_{\mathrm{a}}(t) + e^{-\mathrm{j}\frac{2\pi}{3}} x_{\mathrm{b}}(t) + e^{\mathrm{j}\frac{2\pi}{3}} x_{\mathrm{c}}(t)\right) e^{\mathrm{j}\theta} \tag{4.44}$$

The real-valued abc signals can be retrieved from the inverse transformation as follows.

$$(x_{\mathrm{a}}(t), x_{\mathrm{b}}(t), x_{\mathrm{c}}(t)) = \mathbf{T^{-1}}\Big\{\mathbf{X}(t)\Big\}(\theta) = \mathfrak{Re}\Big\{\mathbf{X}(t) e^{-\mathrm{j}\theta}(e^{\mathrm{j}0}, e^{\mathrm{j}\frac{2\pi}{3}}, e^{-\mathrm{j}\frac{2\pi}{3}})\Big\} \tag{4.45}$$

Transformation of balanced three phase signal

When the transformation angle is locked to the phase angle (a) of a balanced three-phase signal represented by sine waves, the d component becomes zero, and the q component equals to the amplitude of the signal in the abc domain. Mathematically this can be expressed as follows.

$$\sin.\left(\omega t,\, \omega t - \frac{2\pi}{3},\, \omega t + \frac{2\pi}{3}\right) \quad \xrightarrow{\mathbf{T}@\theta=\omega t} \quad 0 + \mathrm{j}1 \tag{4.46}$$

Now, another three phase signal that has a phase shift of α with respect to the reference waveform will be transformed as follows.

$$\sin.\left(\omega t + \alpha,\, \omega t + \alpha - \frac{2\pi}{3},\, \omega t + \alpha + \frac{2\pi}{3}\right) \quad \xrightarrow{\mathbf{T}@\theta=\omega t} \quad \sin(\alpha) + \mathrm{j}\cos(\alpha) \tag{4.47}$$

Instantaneous active and reactive power

According to [94] the instantaneous active and reactive power are computed as

$$\begin{aligned} P &= \frac{3}{2}\left(v_{\mathrm{d}} i_{\mathrm{d}} + v_{\mathrm{q}} i_{\mathrm{q}}\right) \\ Q &= \frac{3}{2}\left(v_{\mathrm{d}} i_{\mathrm{q}} - v_{\mathrm{q}} i_{\mathrm{d}}\right) \end{aligned} \tag{4.48}$$

Note that these definitions are made with arbitrary transformation angle and derived such that they coincide with the conventional steady-state definitions in power system analysis. It is important to highlight that the coefficient $3/2$ is not present in per-unit representation with the proper choice of base values.

With the transformation angle locked to the phase angle (a) of the Point of Common Cou-

pling (PCC), channels of active and reactive power are decoupled, as shown in (4.49), since the d component of the voltage is zero. Thus, the active and reactive power transaction at PCC are independently controlled by i_{q} and i_{d}, respectively.

$$P^{\mathrm{pu}} = v_{\mathrm{q}}^{\mathrm{pu}} i_{\mathrm{q}}^{\mathrm{pu}} \qquad , \qquad Q^{\mathrm{pu}} = -v_{\mathrm{q}}^{\mathrm{pu}} i_{\mathrm{d}}^{\mathrm{pu}} \tag{4.49}$$

Derivative property

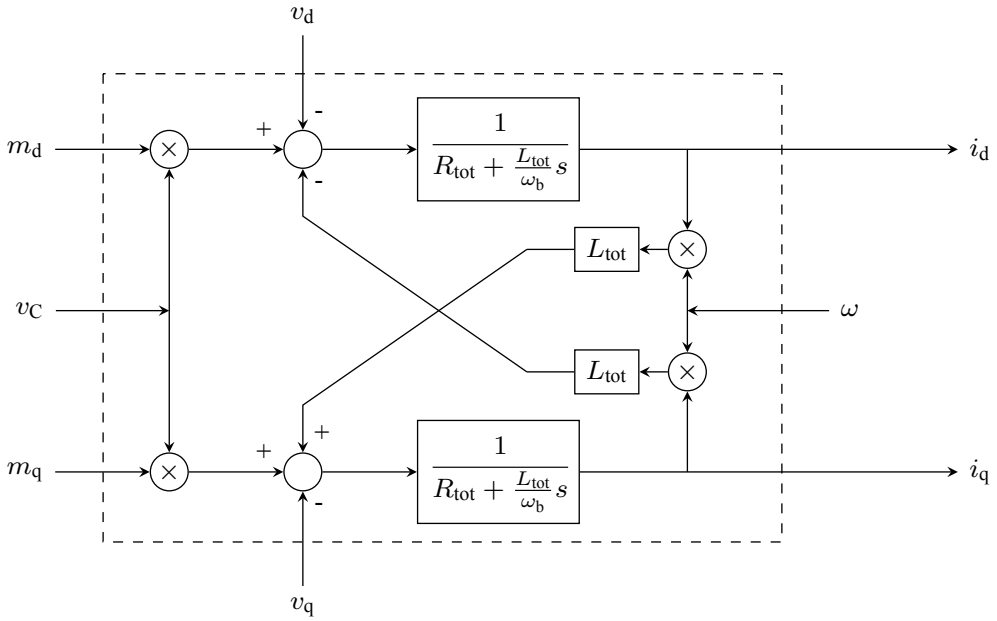
The derivative of a three phase signal can be transformed into dq component with the use of following property

$$\frac{\mathrm{d}}{\mathrm{dt}}(x_{\mathrm{a}}, x_{\mathrm{b}}, x_{\mathrm{c}}) \quad \xrightarrow{\mathbf{T}} \quad \frac{\mathrm{d}\mathbf{X}}{\mathrm{dt}} - \mathrm{j}\omega\mathbf{X} \tag{4.50}$$

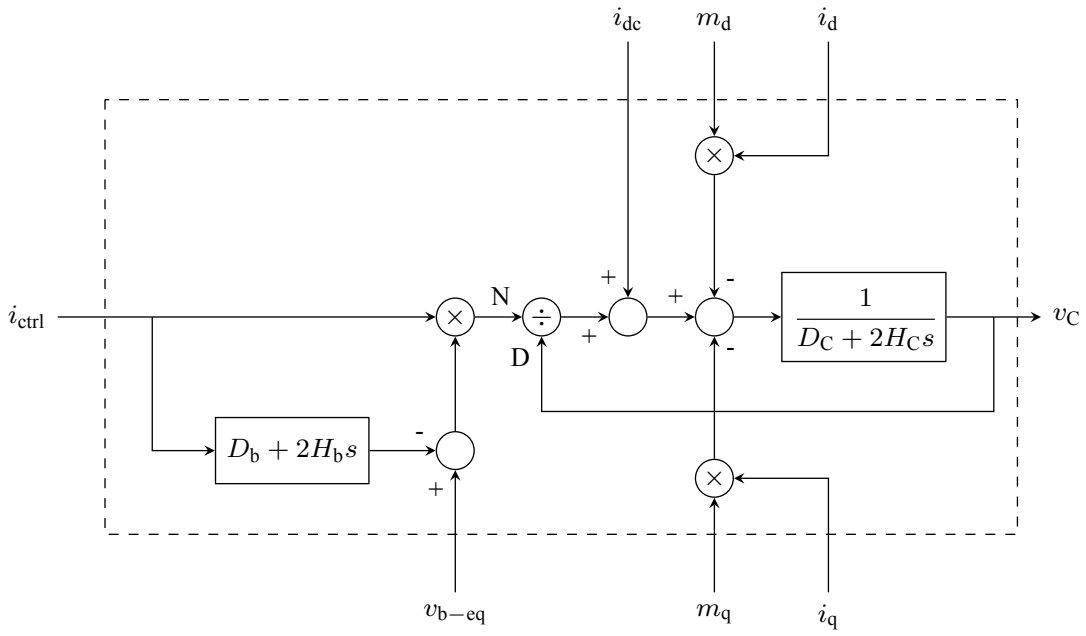
where ω is the time derivative of the transformation angle θ. Applying this property to the AC side KVL equation in the Table 4.1 results in the set of equations expressed in dq domain that are summarized in Table 4.3. These equations are converted into a block diagram representation which is shown in 4.15.

Table 4.3: Terminal equations of MMC-BESS in dq reference frame

DC side KVL	$2H_{\mathrm{a}}\dfrac{\mathrm{d}i_{\mathrm{dc}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{a}} i_{\mathrm{dc}}^{\mathrm{pu}} = V_{\mathrm{dc}}^{\mathrm{pu}} - v_{\mathrm{C}}^{\mathrm{pu}}$
DC side KCL	$2H_{\mathrm{C}}\dfrac{\mathrm{d}v_{\mathrm{C}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{C}} v_{\mathrm{C}}^{\mathrm{pu}} = i_{\mathrm{dc}}^{\mathrm{pu}} - \left(m_{\mathrm{d}} i_{\mathrm{d}}^{\mathrm{pu}} + m_{\mathrm{q}} i_{\mathrm{q}}^{\mathrm{pu}}\right) + \dfrac{v_{\mathrm{x}}^{\mathrm{pu}} i_{\mathrm{ctrl}}^{\mathrm{pu}}}{v_{\mathrm{C}}^{\mathrm{pu}}}$
AC side KVL (d)	$\dfrac{L_{\mathrm{a}}^{\mathrm{pu}}}{2\omega_{\mathrm{B}}}\dfrac{\mathrm{d}i_{\mathrm{d}}^{\mathrm{pu}}}{\mathrm{d}t} + \dfrac{R_{\mathrm{a}}^{\mathrm{pu}}}{2} i_{\mathrm{d}}^{\mathrm{pu}} + \dfrac{L_{\mathrm{a}}^{\mathrm{pu}}\omega^{\mathrm{pu}}}{2} i_{\mathrm{q}}^{\mathrm{pu}} = m_{\mathrm{d}} v_{\mathrm{C}}^{\mathrm{pu}} - v_{\mathrm{d}}^{\mathrm{pu}}$
AC side KVL (q)	$\dfrac{L_{\mathrm{a}}^{\mathrm{pu}}}{2\omega_{\mathrm{B}}}\dfrac{\mathrm{d}i_{\mathrm{q}}^{\mathrm{pu}}}{\mathrm{d}t} + \dfrac{R_{\mathrm{a}}^{\mathrm{pu}}}{2} i_{\mathrm{q}}^{\mathrm{pu}} - \dfrac{L_{\mathrm{a}}^{\mathrm{pu}}\omega^{\mathrm{pu}}}{2} i_{\mathrm{d}}^{\mathrm{pu}} = m_{\mathrm{q}} v_{\mathrm{C}}^{\mathrm{pu}} - v_{\mathrm{q}}^{\mathrm{pu}}$
Battery side KVL	$2H_{\mathrm{b}}\dfrac{\mathrm{d}i_{\mathrm{ctrl}}^{\mathrm{pu}}}{\mathrm{d}t} + D_{\mathrm{b}} i_{\mathrm{ctrl}}^{\mathrm{pu}} = v_{\mathrm{b\text{-}eq}}^{\mathrm{pu}} - v_{\mathrm{x}}^{\mathrm{pu}}$



(a) AC-side model in dq reference frame.



(b) DC- and battery-side model.

Figure 4.15: Block diagram model of MMC-BESS.

4.6 AVM Model Validation

To validate accuracy of the derived AVM model, a single converter connected to an infinite bus via an inductive link is considered as shown in Figure 4.16. Parameters of the system under study is listed in Table 4.4.

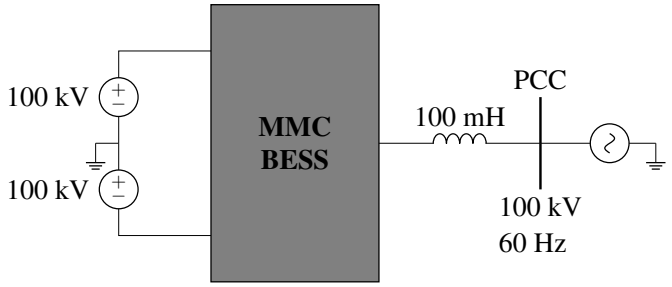


Figure 4.16: MMC-BESS connected to an infinite bus.

Table 4.4: Parameters of the MMC-BESS system under study

Parameter	Value	Unit
Total number of SMs	100	-
Number of SMs with BESS	20	-
SM capacitance	20000	μF
SM capacitor leakage conductance	1	μS
SM-BESS inductance	10	mH
SM-BESS inductor series resistance	0.001	Ω
Arm inductance	30	mH
IGBT's/Diode's On-state resistance	0.01	Ω
Battery nominal voltage	1.2	kV
Battery internal resistance	0.01	Ω
DC-DC converter switching frequency	2	kHz

Figure 4.17 illustrates the real power transacted across various terminals of the converter in

response to step changes in the current command.

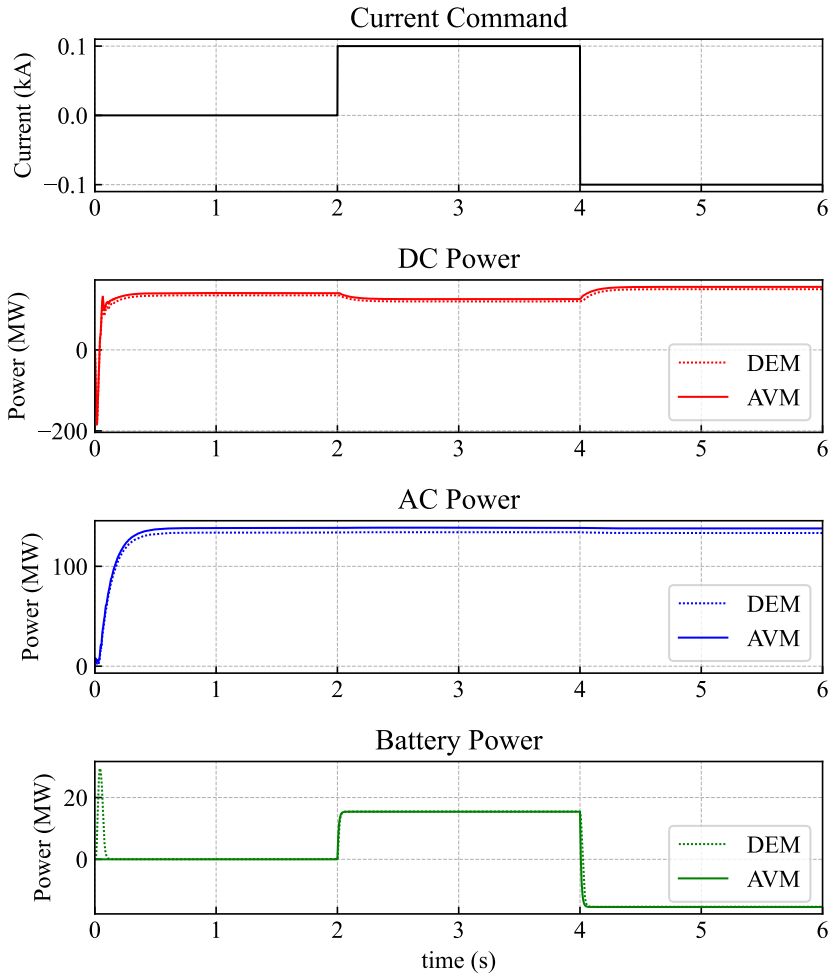


Figure 4.17: Active power waveforms.

The results from the DEM model align closely with those from the AVM. The only significant discrepancy appears in the battery power waveform at the start of the simulation when the SM capacitor voltages are nearly zero. This condition causes the PCM control to draw a high current from the battery. This can be further explained with battery current and voltage waveforms as shown in Figure 4.18. To prevent this issue, all DC-DC converters can be disabled until the SM

capacitors reach their rated voltage. Summation of capacitor voltages and arm currents with both DEM and AVM models are also depicted in Figure 4.19 to confirm that result match closely.

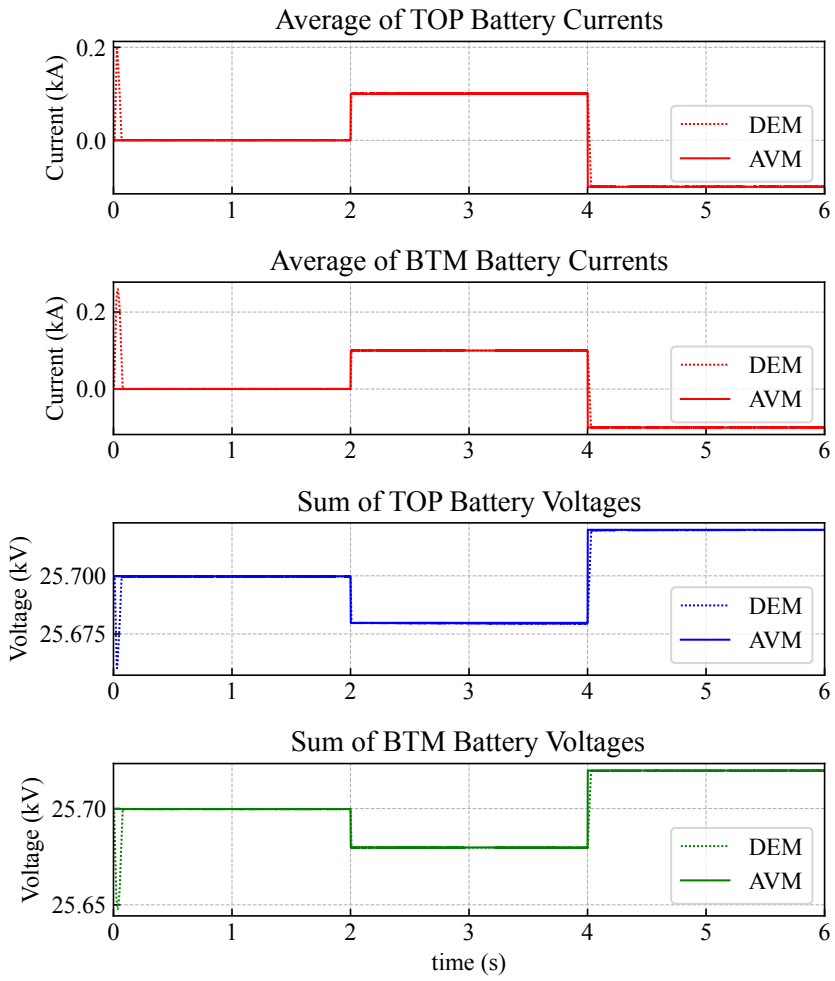


Figure 4.18: Battery current and voltage waveforms.

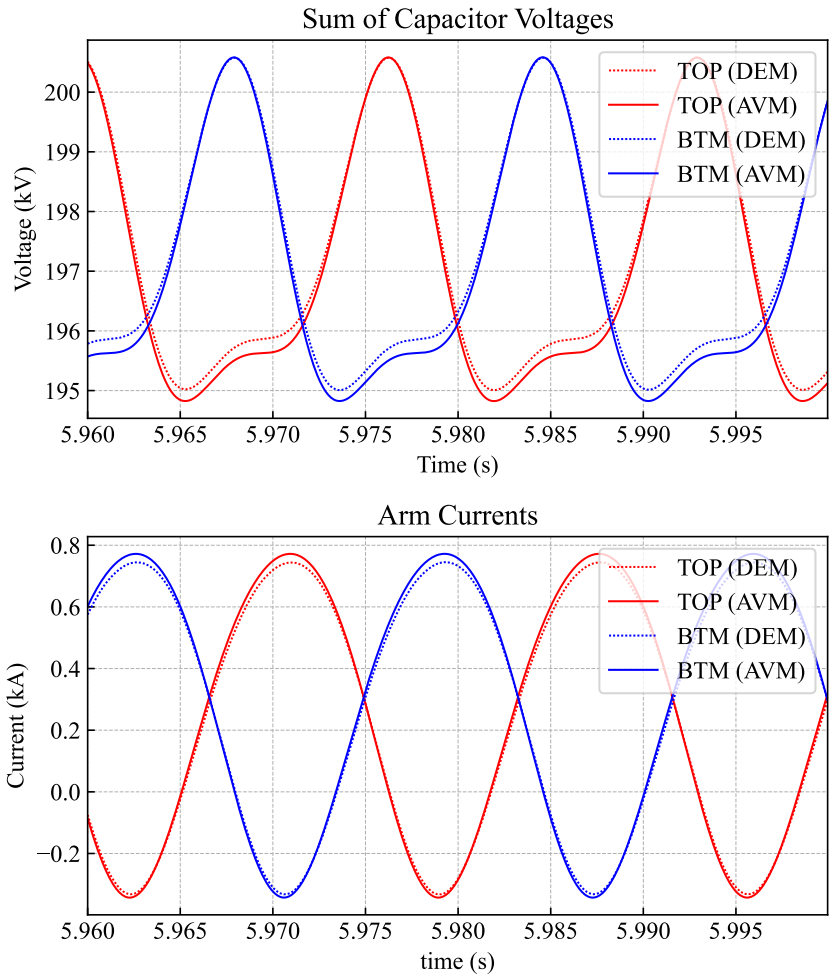


Figure 4.19: Sum of capacitor voltages and arm currents.

4.7 Chapter Contributions

In this chapter, the AVM of the MMC arm with partial BESS integration was derived. This included the AVM of the DC-DC converters operating under PCM control and the AVM of the stack of submodules in each arm. The AVM of the entire three-phase MMC-BESS converter was also

developed by reducing the order of the corresponding circuit using several approximations. The reduced model is particularly useful for analyzing the converter from a terminal perspective. However, it does not account for the voltage ripple in the SM capacitors, which is critical for their sizing. Finally, all circuits and equations were per-unitized, leading to a block diagram representation of the MMC-BESS that is analogous to that of a synchronous machine.

Chapter 5

Application of MMC-BESS in an Exemplar HVDC System

The contents of this chapter are reprinted from the paper [95], which has been accepted for the 2024 CIGRE Canada Conference & Exhibition.

Preliminary investigations are underway to plan for the retirement of Bipole I in Manitoba Hydro's system, given its impending end of life. The leading technology that is being considered as a replacement for Bipole I is the VSC-HVDC system using MMCs. This technology is favored for its modularity, scalability, low harmonic contents, and significantly reduced switching losses. It would also eliminate the need for synchronous condensers that are critical for supporting voltage and reactive power in the existing line commutated converters of Bipole I. Nevertheless, elimination of synchronous condensers at the inverter end of the transmission system could lead to a decrease in the system inertia, which is crucial for maintaining system stability and frequency control. To counteract this potential drawback, this chapter aims to investigate deployment of MMC-BESS in such application. This integration strategy aims to enhance system performance by mitigating

the need for synchronous condensers, thereby simplifying the transmission system and potentially reducing maintenance costs associated with synchronous condensers [96].

Unlike 2-level VSCs or neutral point clamped converters, which require an expensive and bulky line-frequency transformer to integrate the BESS into the system [42], the proposed converter topology eliminates the need for such a transformer. This design choice reduces not only the overall cost but also the physical footprint of the system.

A simplified grid-assisting control scheme is utilized to stabilize the frequency by injection or absorption of real power by batteries. The amount of transacted power is determined based on the frequency deviation passed through a droop or rate-of-change-of-frequency (RoCoF) controller.

5.1 Case Study

The point-to-point VSC-HVDC transmission system that is used as replacement of the existing LCC-HVDC Bipole I is shown in Figure 5.1. Both the rectifier and inverter ends of the transmission line are based on the MMC technology with bipole configuration. The MCC at the inverter end is partially augmented with BESS at the sub-module level. Note that the rectifier converter has no BESS integration. Table 5.1 shows parameters of the converter that is used in this study.

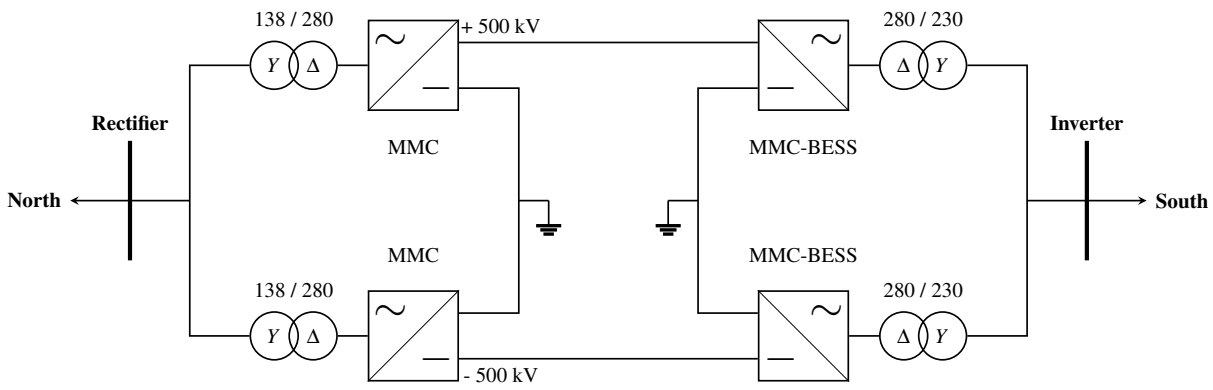


Figure 5.1: MMC-based HVDC system with BESS integration for replacement of Bipole I.

Table 5.1: Parameters of the converters

Parameter	**Rectifier end**	**Inverter end**
Converter's rating/pole	1000 MVA	1000 MVA
Total number of SMs	100	100
Number of SMs with BESS	N/A	20
SM capacitance	10 mF	10 mF
Arm inductance	30 mH	30 mH
Transformer's MVA/pole	1000 MVA	1000 MVA
Transformer ratio (sys/conv)	138/280 [kV]	230 /280 [kV]
Transformer leakage reactance	0.18 pu	0.18 pu
DC-DC inductor	N/A	20 mH
Battery internal voltage	N/A	2 kV
Battery internal resistance	N/A	10 $\mathrm{m}\Omega$
DC-DC switching frequency	N/A	2 kHz

Both rectifier and inverter ends are operated under grid-following mode using decoupled control. The rectifier and inverter ends operate in $V_{dc} - V_{ac}$ and $P - V_{ac}$ control modes, respectively. The DC voltage at the rectifier terminal is regulated at ± 500 kV. The AC voltage at the rectifier and inverter terminals are regulated at 1.0 and 1.05 pu, respectively. The Bipole I is loaded with 67% and 90 % of rated capacity corresponding with two case studies that will be elaborated upon in the next section. These reference values are set while the BESS is in idle mode and not contributing to power exchange. All these settings are placed to attain nearly identical power flows to the existing LCC-HVDC.

The control block diagram of the BESS is illustrated in Figure 5.2. This control is designed to improve the frequency response in the southern Manitoba system. The frequency of the southern AC system at the inverter end is measured using a Phase-Locked Loop (PLL). To eliminate noise and high-frequency oscillations caused by numerical errors in the PLL frequency estimation, the measured frequency is run through a first-order filter with a time constant of 10 ms. Additionally, to further reduce the sensitivity of the BESS control to small, high-frequency perturbations, a deadband block is added after measuring the frequency deviation. The deadband block prevents frequent charge/discharge operations, thereby extending the lifetime of the BESS [97].

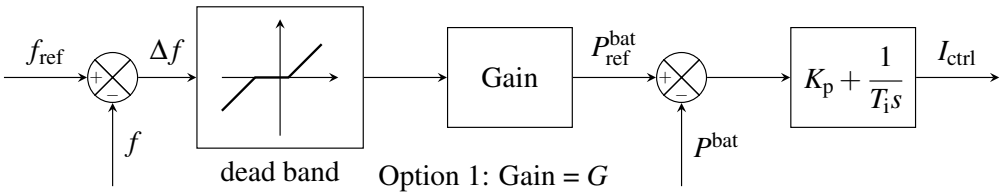


Figure 5.2: BESS control system.

The frequency deviation is fed into the gain block, which outputs a reference signal for the required battery power to compensate for the frequency deviation following a contingency in the power system. This study considers two options for the gain block. The first option is a droop controller, represented by a pure DC gain (G). The second option is the RoCoF controller, which is a derivative term that responds to the rate of change of frequency. In this study, the time constant of the derivative term, T_{d}, is set to 1.0 second. The reference battery power produced is then subtracted from the measured battery power, and the result is fed to a proportional-integral (PI) controller. This generates the peak current signal, which is used to operate the PCM control of the BESS.

It is important to note that the total measured battery power is added to the inverter's reference power, which is the converter's reference power in the decoupled controller. If this addition is not made, the inverter will continuously attempt to regulate the real power to its set value under steady-state conditions, thereby preventing the BESS from contributing to the inertial response.

5.2 Simulation Results

All simulations are performed using PSCAD/EMTDC, employing detailed equivalent models of the MMC and MMC-BESS for Bipole I, of a three-Bipole multi-infeed HVDC system. After reaching steady state with all machines initialized, a three-phase solid fault is applied to the northern interconnection at the Bipole I rectifier bus. The fault is cleared after 5 cycles, causing a temporary dip in frequency in the southern system at the inverter end of Bipole I. In all simulation cases with VSC-HVDC, the harmonic filters at both the rectifier and inverter ends, as well as the synchronous condensers at the inverter end, were out of service. However, the harmonic filters and synchronous condensers of other LLC Bipoles, i.e., Bipole II and III, remained intact in all scenarios. The results of simulations for two cases, each with identical total generation in Northern Manitoba Hydro's

system, but with 67% and 90% loading on Bipole I, are discussed in the following subsections.

5.2.1 Bipole I Loaded to 67% of Capacity

Figures 5.3 and 5.4 display the simulation results with the droop and RoCoF controllers, respectively. Each figure has three columns corresponding to various time constants of the PI controller, denoted by T_{i}. Notably, the proportional constant of the PI controller, K_{p}, is set to zero in all scenarios.

As shown in these figures, the LCC-HVDC system exhibits the lowest (most problematic) frequency nadir. Replacing the LCC with the MMC alternative improves the frequency nadir and rate of change of frequency, even without BESS integration. Further enhancement is achieved by the BESS injecting a portion of the converter's MVA in both droop and RoCoF controller modes. During the fault, the total AC power delivered by the inverter also increases when the BESS injects power. With a small time-constant, the output power is plateaued as the BESS reaches its maximum deliverable power for a short duration. The frequency response is dependent on the PI controller's time constant. Reducing the time constant increases the rate at which the peak current (i_{ctrl}) and, consequently, the battery power (as shown in the second row of figures) rise, thereby improving the frequency response.

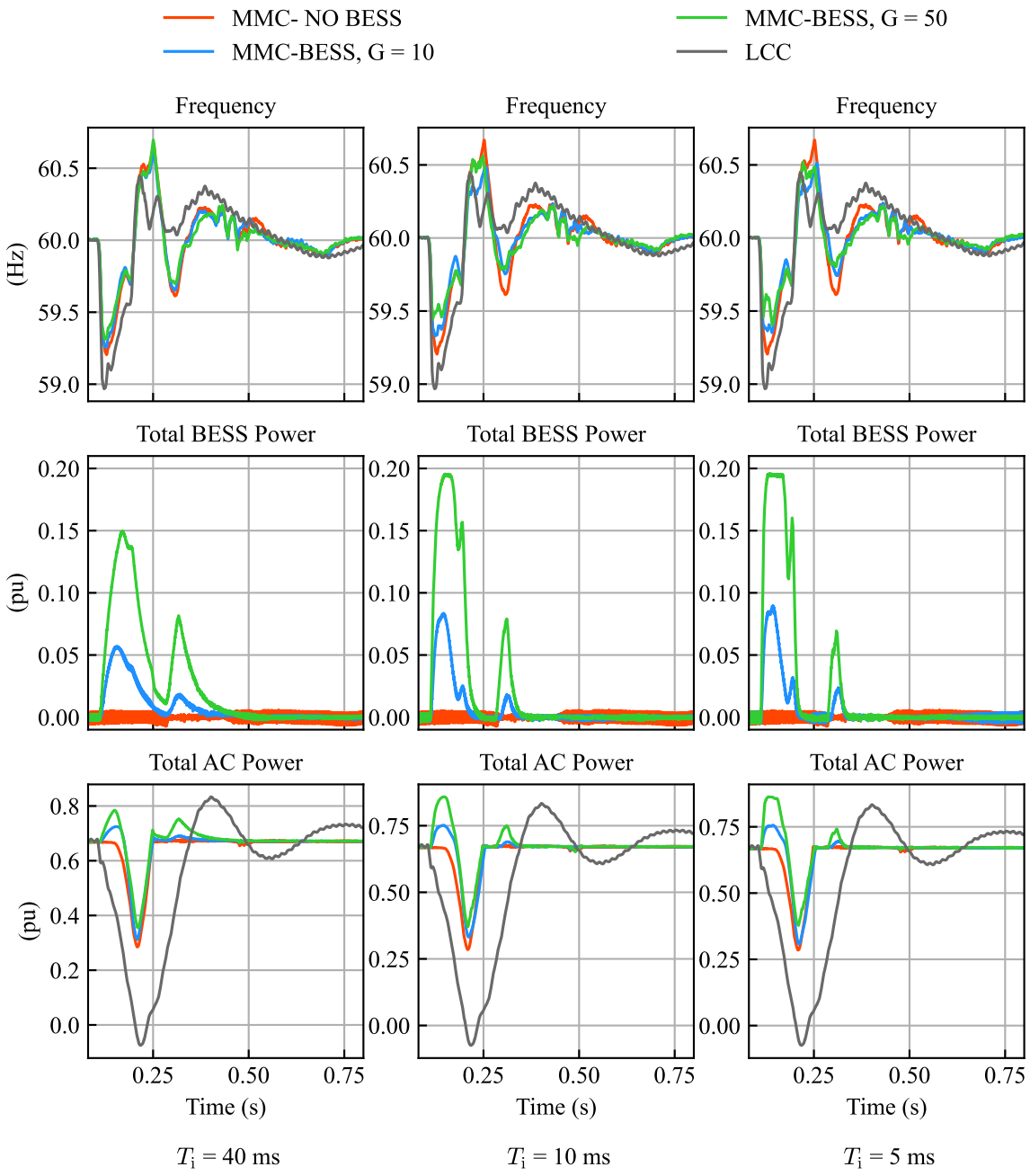


Figure 5.3: Results with droop controller for 67% loading.

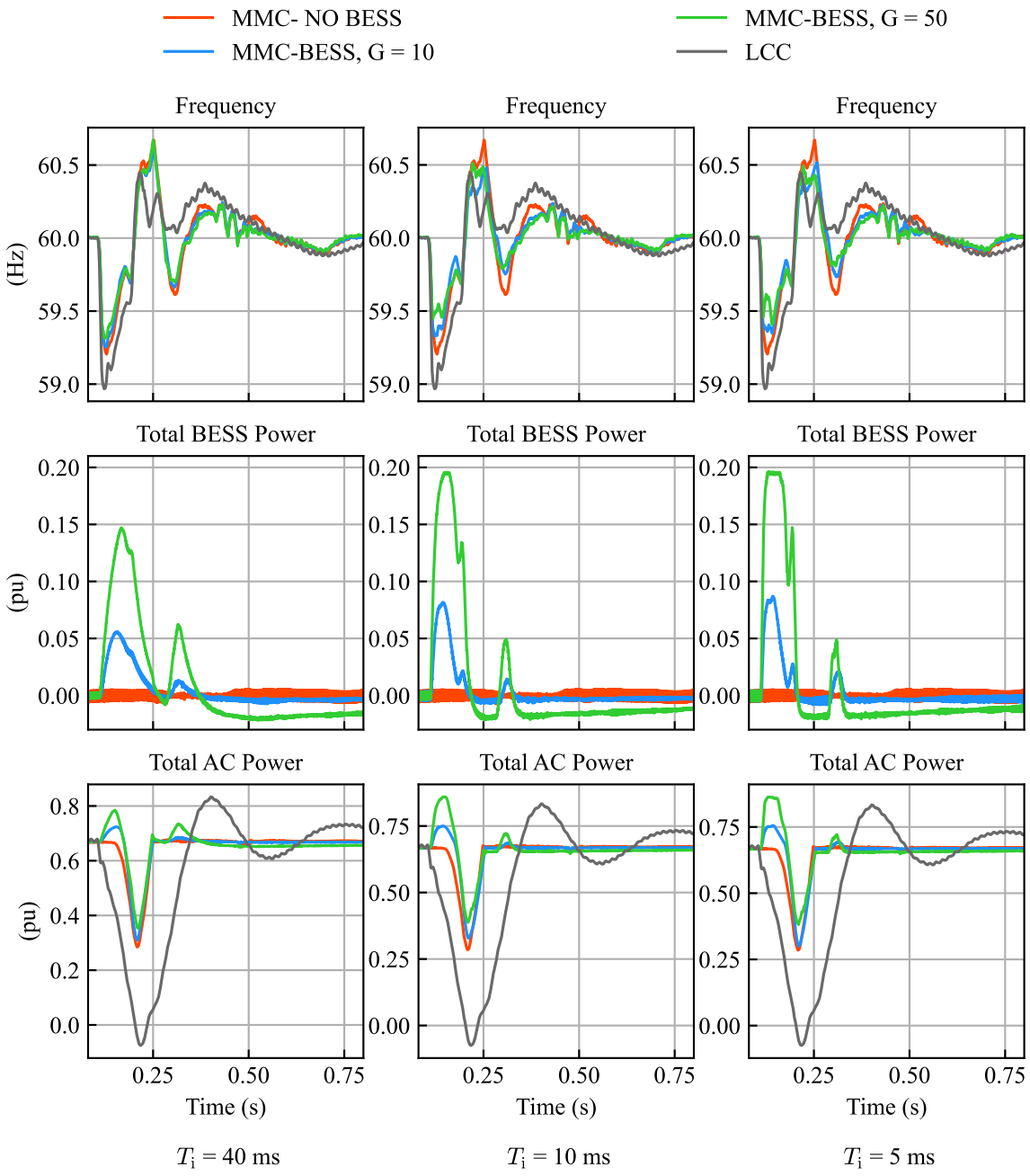


Figure 5.4: Results with RoCoF controller for 67% loading.

5.2.2 Bipole I Loaded to 90% of Capacity

Using the same procedure and identical controller parameters as explained in the previous subsection, simulation results were obtained with Bipole I loaded to 0.9 pu. Figures 5.5 and 5.6 show the results with droop and RoCoF controllers, respectively. It was observed that the distance between the frequency nadir associated with the LCC option and the MMC-BESS alternatives is greater than that with 67% loading of Bipole I. This indicates that MMC-BESS shows even better performance for inertial response when the HVDC system is heavily loaded. Note that the total power delivered by the inverter exceeds 100%, implying that the converter must have enough headroom to handle the power exchange facilitated by the installed batteries. It is also important to highlight that the rectifier end must be capable of delivering extra power to charge the BESS at the inverter end when needed.

No significant improvement in frequency response is observed when switching from the droop controller to the RoCoF controller during the fault. This is because the gains of both controllers are identical when exposed to abrupt changes, despite differences in their steady-state responses.

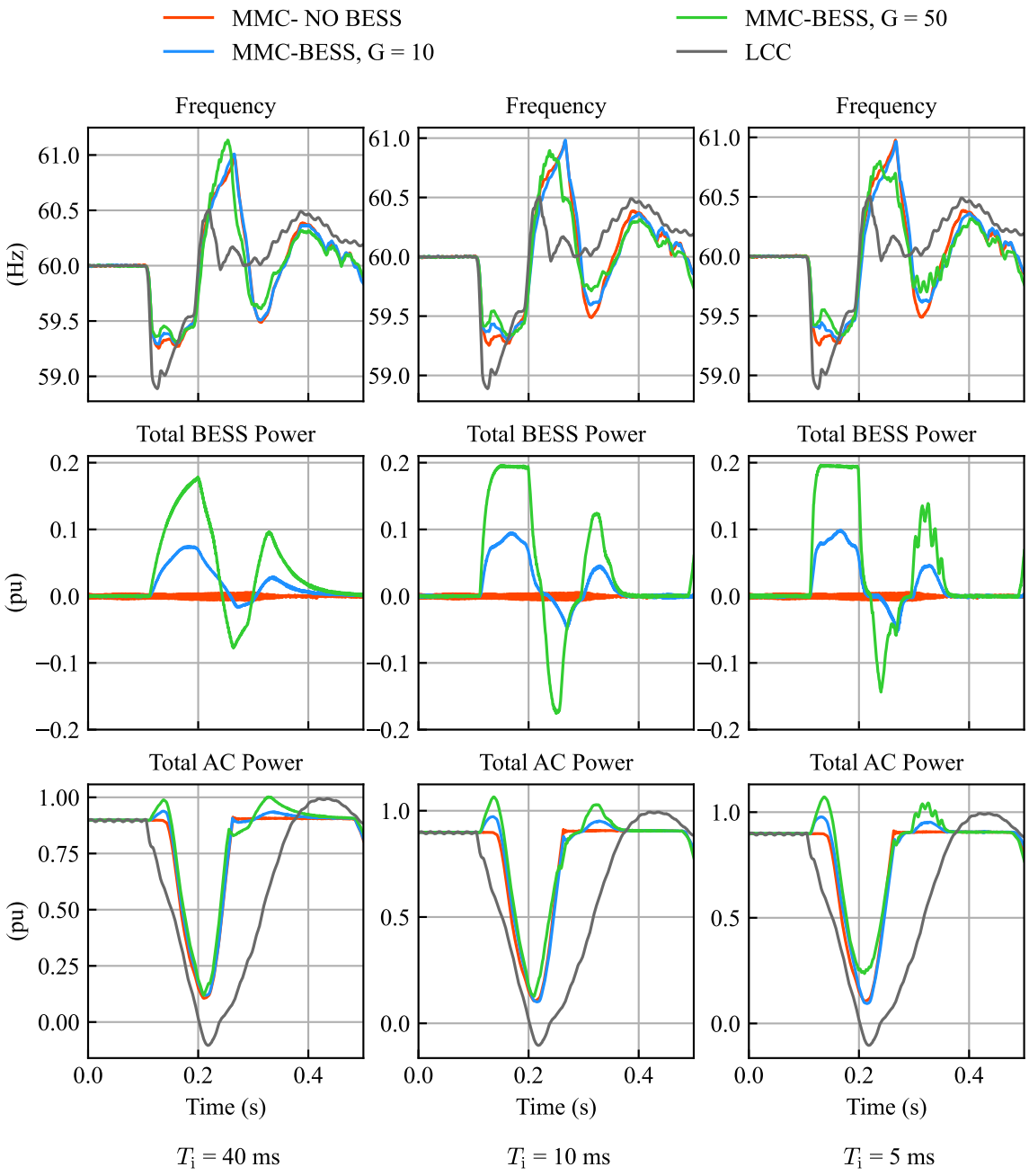


Figure 5.5: Results with droop controller for 90% loading.

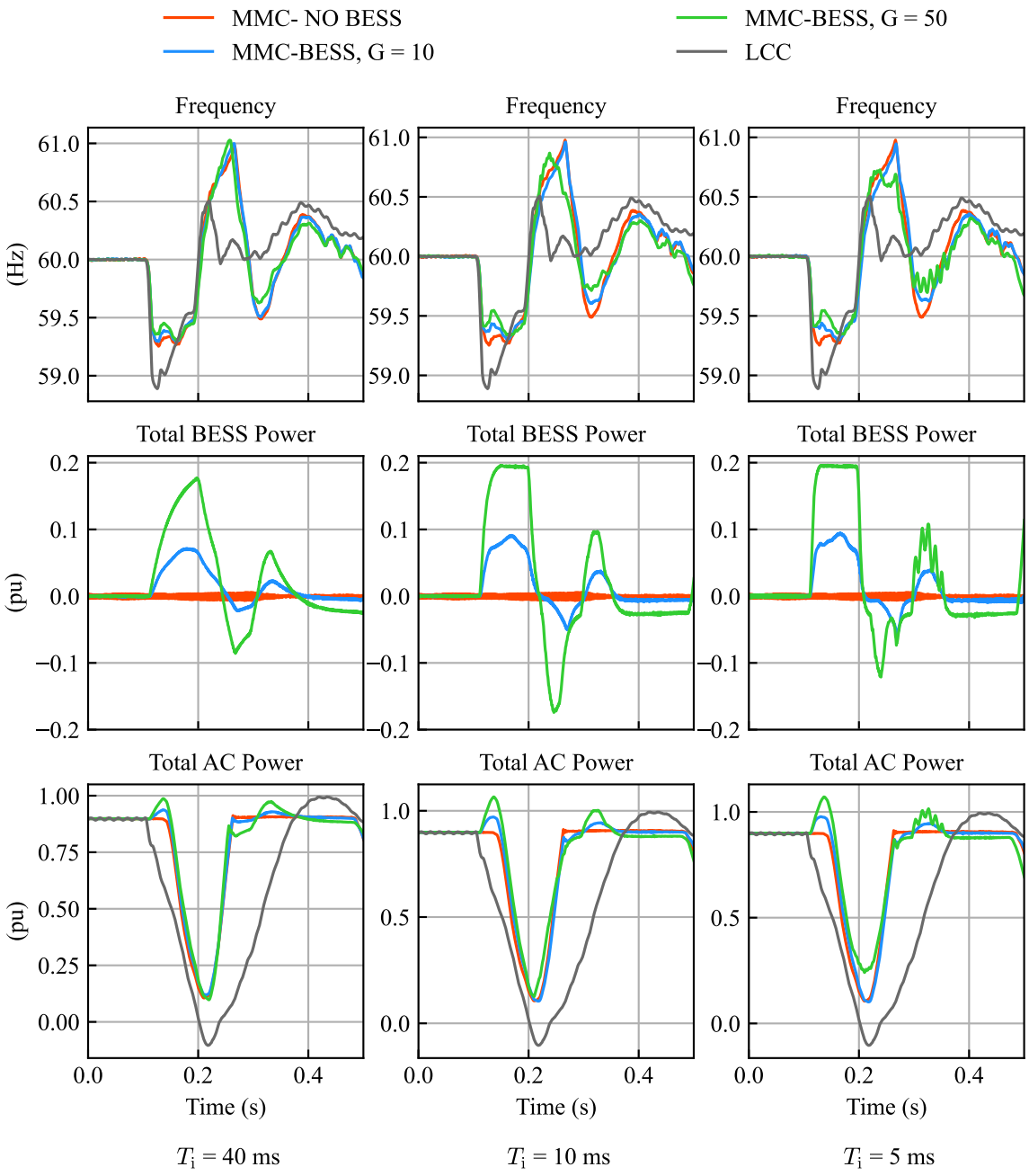


Figure 5.6: Results with RoCoF controller for 90% loading.

5.3 Chapter Contributions

This chapter demonstrated that integrating BESS within an MMC-based VSC-HVDC system can effectively replace the aging Bipole I in Manitoba Hydro's system, offering improvements in frequency response and system stability. By eliminating the need for bulky and expensive transformers and synchronous condensers, the proposed topology reduces maintenance costs. The simulations confirm that the MMC-BESS configuration enhances the system's ability to manage frequency deviations by providing rapid and effective real power support. The study concludes that the MMC-BESS technology is a viable and advantageous solution for modernizing HVDC transmission systems, ensuring reliable and efficient power delivery.

Chapter 6

Conclusions, Contributions, Limitations, and Future Work

6.1 Conclusions and Contributions

This thesis presented the modeling, simulation, and application of MMCs partially integrated with BESS. The work focused on enhancing computational efficiency, developing versatile modeling techniques, and exploring the practical benefits of this technology for HVDC transmission systems. The key findings and contributions of each chapter are summarized below:

1. **Development of a continuous-time model for simulation of MMC-BESS (Chapter 2):**

    - A comprehensive continuous-time model for converters was developed, representing both normal and blocking modes. This model can be applied to various EMT platforms (e.g., PSCAD/EMTDC, EMTP, MATLAB/Simulink) by discretizing state-space equations using different integration methods, making it versatile and platform-independent.

2. **Introduction of a DEM for MMC-BESS EMT simulation (Chapter 3):**

    - A novel DEM was introduced for simulating MMCs with partially-integrated BESS, offering significant computational efficiency by reducing the number of interconnected nodes.
    - The DEM minimizes time-varying electrical conductances, avoiding the need for frequent re-factorization of the admittance matrix, further enhancing computational performance.
    - State variables critical for control purposes, such as SM capacitor voltages and DC-DC inductor currents, are computed and accessible, facilitating control strategies such as NLC modulation and battery current control.
    - A PCM control strategy was introduced, enabling seamless transitions between charging, discharging, and idle modes, while providing additional protection by limiting currents in the battery and DC-DC converters.
    - The DEM's computational efficiency was validated, showing significant improvements compared to traditional DSM, with accuracy confirmed through experimental results from a scaled MMC-BESS prototype.

3. **Development of an AVM for MMC-BESS (Chapter 4):**

    - AVMs for the MMC arm with partial BESS integration were derived, including AVMs for the DC-DC converters operating in PCM mode and for the SM stacks in each arm.
    - A reduced-order model for the three-phase MMC-BESS was developed, providing an effective tool for terminal behavior analysis, despite not capturing voltage ripple in SM capacitors, which is essential for sizing considerations.

- The per-unitization of circuits and equations led to a block diagram representation that parallels the structure of a synchronous machine, facilitating easier analysis and integration into larger power systems.

4. **Study of the aplication of MMC-BESS for modernizing Bipole I in Manitoba Hydro's grid (Chapter 5):**

    - The study demonstrated that integrating BESS within an MMC-based VSC-HVDC system offers a viable replacement option for the aging Bipole I in Manitoba Hydro's network.
    - The proposed MMC-BESS solution enhances frequency response and system stability, reducing the need for bulky transformers and synchronous condensers.
    - Simulation results confirmed that the MMC-BESS configuration effectively manages frequency deviations by providing rapid real power support, making it a viable and advantageous solution for modernizing HVDC transmission systems and ensuring reliable, efficient power delivery.

The work presented in this thesis has led to the following publications.

1. R. Parvari; S. Filizadeh; I. Fernando, "Exploring the Potential of Grid-Assisting MMCs with BESS in Manitoba's Power Infrastructure," *2024 CIGRE Canada Conference & Exhibition*
2. R. Parvari; S. Filizadeh; I. Fernando, "Detailed Equivalent Modeling and Simulation of Modular Multilevel Converters with Partially-Integrated Battery Energy Storage," *Journal of Modern Power Systems and Clean Energy*
3. R. Parvari; S. Filizadeh; D. Muthumuni, "An Accelerated Detailed Equivalent Model for Modular Multilevel Converters," *Electric Power Systems Research*, 2023 [84]

4. J.Rupasinghe; S. Filizadeh; D. Muthumuni; R. Parvari, ”A Multi-Solver Framework for Co-simulation of Transients in Modern Power Systems,” *Electric Power Systems Research*, 2023 [98]

5. R. Parvari; S. Filizadeh ”Exact Solution of Modulation Waveforms for MMCs Operating with Circulating Current Suppression Control (CCSC) Strategy,” *IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*, 2021 [66]

6. R. Parvari; S. Filizadeh ”Analysis of Pole-to-Pole Faults in Half-Bridge and Full-Bridge MMCs,” *IEEE Electrical Power and Energy Conference (EPEC)*, 2021 [66]

6.2 Limitation of the Thesis

This thesis has the following limitations.

1. All batteries are modeled using a fixed internal DC voltage source and an internal resistor. While this model is suitable for short run-time simulations, it is not accurate for longer simulations, as variations in the battery’s state of charge affect its internal voltage. Consequently, real-time simulation of MMC-BESS, which typically requires longer run times, would also lack accuracy.

2. All switching devices, such as diodes and IGBTs, are represented by a two-state ideal switch model with respective ON-state and OFF-state resistances. These approximations result in inaccurate loss calculations, as they often neglect the switching transitions between ON-state and OFF-state. Additionally, the conduction loss is inaccurately modeled; IGBTs, which exhibit a voltage source behavior during conduction, are instead represented in this thesis as constant resistors while conducting.

3. The proposed model does not provide access to the internal nodes within the stack of SMs, making the study of internal faults infeasible.

6.3 Recommendations for Future Work

The following recommendations are suggested for future work on the subject of MMC-BESS:

Loss Analysis in High-Frequency DC-DC Converters: MMC-BESS incorporates DC-DC converters operating at high frequencies, presenting a challenge in EMT modeling due to associated switching losses. Given their high-frequency operation, these converters could significantly contribute to the total power loss in MMC-BESS. Therefore, a detailed analysis of loss calculations at various operating points is necessary.

Energy Storage Enhanced STATCOMs: A potential application of MMC-BESS is in energy storage-enhanced STATCOMs. Beyond reactive power compensation and voltage regulation, these STATCOMs can inject or absorb real power, which can be used for inertia emulation and frequency response improvement.

Grid-Forming Control Studies: With grid-forming control becoming increasingly popular in power systems, it is important to study HVDC links and energy-enhanced STATCOMs with MMC-BESS configurations under this control strategy. Such studies should explore the behavior of the converter and the system's response to faults and contingencies.

Internal and Asymmetrical Faults: Analyzing converter behavior under internal faults, where a node within the stack of SMs is short-circuited to ground, is crucial for the inner-layer protection of the converter. Additionally, analyzing asymmetrical AC faults is recommended to evaluate system stability and to aid in the design of protective relays and circuit breakers.

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