PSCAD/EMTDC™ Modelling of Active Filters for HVdc Applications

by

Mohd. Halimi Abdullah

A Thesis

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Abstract

In recent years, major power engineering equipment manufacturers such as Siemens and ABB have proposed the use of active filters in place of traditional passive filters in their newer HVdc schemes. The compact design and many other advantages offered by active filters over their passive counterpart have increased the appeal for this new technology.

The aims of this thesis are to develop detailed PSCAD/EMTDC™ models of active filters for both the ac- and dc-side of an HVdc scheme. The models are then integrated into the CIGRE HVdc Benchmark Model through suitably designed de-coupling elements, to evaluate their effectiveness in reducing harmonic currents in the system. Transient simulations have been carried out to examine the active filter controller responses to transient conditions typical to such an HVdc scheme.

This thesis also includes an investigation into the feasibility and performance of an ac-side active filter installation within the Capacitor Commutated Converter (CCC) HVdc scheme.

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CHAPTER 1

Introduction

High Voltage Direct Current (HVdc) converters have long been identified as the source of harmonic *voltages* on the dc transmission lines and harmonic *currents* on the ac systems connected to them and these are mostly due to the switching actions of the thyristor valves. To prevent these harmonics from leaving the converter station, "passive" filters have traditionally been employed. These filters work on the principle of supplying a low-impedance path at the chosen harmonic frequencies and thus appearing as a short-circuit to ground for the respective harmonic currents.

In the past couple of years, there have been some interesting developments in the area of filter design with the introduction of the so-called "active" filters by major power engineering equipment manufacturers such as Siemens and ABB in their newer HVdc schemes. Instead of

using passive components tuned to give the required harmonic filtering, these active filters employ power electronic switching devices to produce *compensating current signals* to cancel out the harmonics. Several papers have been published pertaining to this concept of active harmonic filtering [1,2,3,4,5].

1.1 What are Harmonics?

Harmonics are defined as "the sinusoidal components of a repetitive waveform which consist exclusively of frequencies that are exact multiples (or harmonic orders) of the fundamental frequency" [6, p.35]. A complete set of harmonics then makes up a Fourier series which altogether represents the original waveform. Literature discussing the nature of HVdc converter harmonics usually classify them as either of the *characteristic* or the *non-characteristic* type. Both will be discussed in more detail in the following sections.

1.2 Characteristic Harmonics

Characteristic harmonics have *orders* that are related to the pulse number of the HVdc converter. A converter of pulse number p produces (under ideal system conditions) only characteristic harmonic voltages of orders

$$h = pk \tag{1.1}$$

on the dc side, and harmonic currents of orders

$$h = pk \pm 1 \tag{1.2}$$

on the ac side of the system; k being any integer.

Most HVdc converters are either of the 6- or 12-pulse configuration, thus generating harmonics of the orders given in Table 1.1 below.

Pulse no.	dc side	ac side
p	pk	$pk \pm 1$
6	0,6,12,18,...	1,5,7,11,13,17,19,...
12	0,12,24,...	1,11,13,17,19,...

Table 1.1 Orders of characteristic harmonics

The derivations of these characteristic harmonics can be found in literature [6,7,8]. Figures 1.1 and 1.2 on the next page present the variation of the 11th and the 13th harmonic currents, respectively, as a percentage of the fundamental current and in relation to the HVdc converter angle of delay, α and the overlap, μ [6, pp. 45-46].

In general, the higher the order of harmonics, the lower the harmonic current magnitudes are. The results presented in Figures 1.1 and 1.2 will be used in the next chapter to calculate the steady state harmonic voltage magnitudes across the ac-side active filter terminals and then on, the active filter transformer rating.

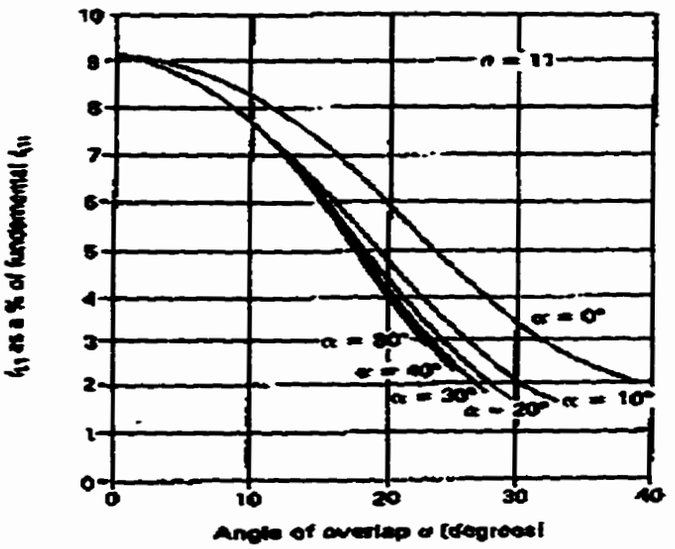


Figure 1.1 Variation of the 11th harmonic current with respect to the angle of delay and the overlap [6, pg. 45]

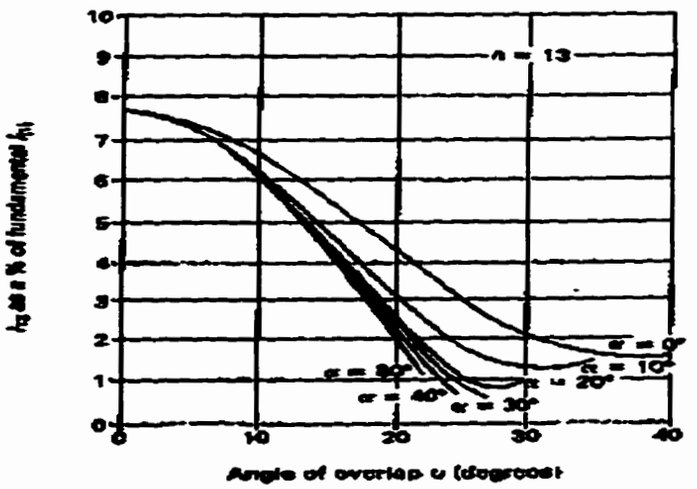


Figure 1.2 Variation of the 13th harmonic current with respect to the angle of delay and the overlap [6, pg. 46]

1.3 Non-characteristic Harmonics

The characteristic harmonics presented earlier arise from ideal system conditions. However, ideal conditions are rarely observed in practice and as a result, small amounts of *non-characteristic* harmonics will be present in the system. The term non-characteristic harmonics is used to indicate harmonic currents or voltages which frequencies are other than those given by equations (1.1) and (1.2) previously.

In HVdc systems, these non-ideal conditions are most often the result of such events as:-

(1) Unbalanced 3-phase ac voltages due to a single-phase (i.e. a non-symmetrical) fault.

(2) Imbalance in the converter components (e.g. due to component failure).

(3) Misfiring of the converter valves.

(4) Changes in the direct current magnitude initiated by the remote HVdc station.

Under either one of these conditions, the converter will start to produce large amounts of non-characteristic harmonics. For example, converter transformer saturation (due to a non-symmetrical fault on the ac-side of the HVdc converter) will produce a 2nd order harmonic current on the ac-side, which will then give rise to a fundamental frequency current on the dc-side of the system. This phenomenon called 'complementary resonance' is, in most cases, very unstable and lightly damped due to the fact that the dc transmission lines are often resonant at the fundamental frequency [6, p.113].

1.4 Harmonic Elimination

Excessive harmonics must be prevented from entering either the dc transmission line or the ac system due to their tendency to cause voltage distortion, extra losses on the transmission lines, overheating in capacitors and generators, instability in the converter controls and more seriously, interference with external services such as telephone and railway signals [6, p.51]. Harmonic containment measures must be given top priority because if left unchecked, harmonic currents or voltages will no longer be confined to the vicinity of the converter

station, but may well be propagated over long distances (through transmission lines) and affecting equipment and facilities far away from the source of the problem. The principle means of harmonic elimination are:-

(1) Increasing the pulse number of the HVdc converter, and

(2) Installing harmonic filters.

Increasing the converter pulse number, as indicated by equations (1.1) and (1.2) given previously, will increase the frequency at which the lowest order of harmonics is produced and hence, the magnitude of the harmonics. Although this method has been used in some converter schemes, it is of general opinion that especially for HVdc applications, beyond the pulse number 12 the use of harmonic filters are more economical [7, p.296]. This is because the design of higher pulse-number converters presents the following disadvantages:

(1) Increased levels of lower order harmonics if and when the converter transformers are taken out of service.

(2) Increased number of converter transformers used, both in service and as spares.

(3) Complexity in transformer connections and insulation coordination.

HVdc schemes in particular, have to utilise as simple transformer connections as possible in order to minimise the problem of insulating the converter transformers to withstand the combination of alternating and high direct voltages. Moreover, HVdc passive harmonic filters have the ability to serve a dual purpose of eliminating harmonics and providing reactive power supply to the converter.

The recent years have seen the development of a new type of harmonic filters generically referred to as 'active filters'. In contrast to traditional 'passive' filters, so called because of their design which is solely based on passive components, active filters utilise cutting edge technology in power electronics and signal processing to pro-actively inject a carefully modulated current or voltage signal into the system to counteract the problematic harmonics. It is this interesting development in power engineering which will be pursued in greater detail in this thesis.

1.4.1 Passive Filters

Passive filters work on the principle of supplying a low impedance path at the designated harmonic frequencies, thus appearing as a short-circuit path for the corresponding harmonic currents to flow to ground. In their favour, the filters are electrically simple and very effective especially if the harmonics are located within a narrow frequency range while the impedance of the harmonic source (in this case, the HVdc converter) is high [1]. Nevertheless, they possess a few limitations:-

(1) Passive filters are ineffective in covering a wide range of frequencies, thus prompting the need to install several different filters to cater for different harmonic frequencies or range of frequencies.

(2) Changes in the passive component characteristics e.g. due to capacitor ageing, will cause detuning of the filter and the subsequent degradation of filter performance.

(3) Passive filters operation depend on the ac network impedance and the fundamental frequency.

(4) Problem of resonance of the filters with the ac network [6, p.186].

These technical limitations may lead to increasing design constraints and complexity which ultimately bring about an increase in the cost of such filter installations.

1.4.2 Active Filters

Active filters, on the other hand, measure the harmonic voltages or currents on the ac or dc line and through the use of a *controllable voltage source*, introduce the appropriate 'compensating' voltages or currents into the network. The active filter voltage or current waveforms are modulated in such a way that they are in phase opposition to the harmonic voltage or current, thus cancelling out these harmonic quantities. Some of the advantages of using active filters are as follows:-

(1) Flexibility of the filters to adapt to changes in the ac network frequency or topology.

(2) In a 'hybrid' configuration where an active filter is used in conjunction with a passive one, the former will be able to compensate for the de-tuning of the latter.

(3) The harmonic attenuation achievable by the filter is very high on the whole frequency range.

(4) In addition to harmonic elimination, the active filter can also be used to dampen resonance in the ac network [9].

(5) The comparatively small size of the filter installation makes it easy for the filter to be transported and/or relocated.

(6) Modifications to filter characteristics only require changes to be made to the control software. As no hardware changes are necessary, updates can be made quickly and with minimal additional costs incurred.

(7) In the 'hybrid' configuration, the number and size of the passive filter banks can be reduced significantly. As well as saving costs, this also reduces the energy associated with voltage transients at the filter location.

However, with reference to the last point, it needs to be said here that for the ac-side active filter installation, the total amount of available reactive power compensation from the passive filter and shunt capacitor banks obviously needs to be maintained. Therefore, if the number of passive filters are reduced, the reduction in the reactive power supply has to be compensated by the shunt capacitors and remaining passive filters.

1.5 Previous Work on Active Filters

As mentioned in the beginning of this chapter, there are a few papers published on the subject of active filtering, albeit with different emphasis on the areas covered and the amount of details presented. With PWM-based FACTS (Flexible AC Transmission Systems) applications becoming more important in the pursuit of increased power transmission efficiency and cost reduction, we should expect to see more publications dealing with the application of active filtering in power engineering in the very near future.

During the time in which this thesis is written, the majority of published papers on the aforementioned topic have covered such areas as:-

(1) Steady state analysis of the filter; mostly emphasizing the effectiveness of the filter in removing harmonics [2, 4].

(2) Simple transient analysis covering the filter response to system start-up and voltage increment/reduction [4].

(3) Costing exercises to gauge the feasibility and cost advantage to be gained from such implementation of active filters on new or existing HVdc schemes [4].

(4) Appropriate controls strategies for application on different ac network topology [1].

(5) Operational aspects of active filter installations [3].

There are also a few papers that deal specifically with the application of PWM-based power electronic circuits to dampen resonance in a power system network [1, 9]. Although this is somewhat loosely related to harmonic filtering, the main concept of using PWM-based power electronic circuits to inject carefully modulated current or voltage signals into a network and the control strategies employed are very similar to those used in active filtering applications and thus can be inferred to in various areas covered in this thesis.

1.6 Aims of This Thesis

Foremost, this thesis focuses on developing detailed PSCAD/EMTDC models of 'hybrid' active filters for use on both the ac- and dc-side of an HVdc scheme. This completed, the models are then integrated within the CIGRE HVdc Benchmark Model [11] to evaluate their effectiveness in reducing the harmonic levels in the system and also to test their responses to simulated transient conditions typical to such a system.

On the ac-side of the system in particular, it will be shown that the double-tuned 11/13th passive harmonic filter banks normally installed on the lines can be removed altogether; their functions taken over completely by the active filters. In this case, not only has the harmonic attenuation on the lines been improved, the active filters have also provided some form of immunity against changes in the ac system characteristics. Nevertheless, the loss in available reactive power supply has to be made up by increasing the size of the shunt capacitor banks and this has been duly taken into consideration.

1.7 Structure of The Thesis

The following chapter will begin with the equivalent circuit representation of the active filter model which will then be used to formulate the steady state equations for the system. These equations will later be applied in calculating the kVA rating of the active filter transformer. The transformer represents a major cost in the active filter scheme and therefore requires some degree of optimisation.

Next, Chapter 3 will describe the hybrid active filter models developed using the PSCAD/EMTDC™ transient simulation software. Here, only the dc-side active filter model will be explained as both the ac- and the dc-side installations are almost identical. This will be followed by descriptions of the control blocks used to measure the harmonic currents in the system and to produce the appropriate PWM signals for the active filter voltage source.

The different simulation runs performed on the filter models and the analysis of results obtained from EMTDC will then be explained in Chapter 4. These analysis will hopefully help to verify the credibility of the models and to indicate the degree of effectiveness of the filter installations. The tests also include transient simulations which are performed to determine the filter controller

stability under various fault conditions. In addition, some study cases will be presented to illustrate the impacts of ac system topology changes on the performance of the active filters.

Next in Chapter 5, an investigation into the feasibility of an active filter installation in a Capacitor Commutated Converter (CCC) scheme will be conducted. For this exercise, the CCC scheme as proposed by ABB and for which an equivalent circuit model has been developed by one of the author's colleagues will be used to test the active filter performance. Results from steady state simulations will be presented before the readers for analysis.

Finally, Chapter 6 will conclude the thesis by summarising the work done thus far and the main conclusions that may be derived from the whole exercise. On the final note, some recommendations for further work in this area will be presented.

CHAPTER 2

Active Filter Equivalent Circuit and Steady State Analysis

In Chapter 1, the principle behind active harmonic filtering has already been explained in brief. This involves (1) detecting the phase and amplitude of the line harmonic current and (2) injecting the appropriate 'compensating' current (which is equal in amplitude but completely out of phase to the harmonic current) into the line at the measuring point and therefore cancelling out the harmonics.

Depending on how the active filters are connected to the network, they can be classified as either series or shunt filters. Figure 2.1 on the next page illustrates the series active filter configuration [1]. Here, the series filter prevents harmonics generated by Network #1 from entering the other network by introducing a complementary voltage signal V_{af}, which is

equal in magnitude but opposite in phase to the harmonic voltage V_h from Network #1. The net result is zero harmonic voltage at the filter terminals.

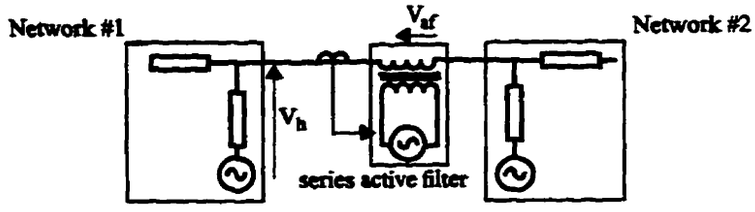


Figure 2.1 Series active filter

For HVdc applications, this configuration is obviously not feasible due to the fact that the fundamental current (which is usually quite large) flows through the active filter. This means that the rating of the active filter isolating transformer has to be very large to accommodate the current. Secondly, due to the large switching and lightning surge levels typical to HVdc schemes, the basic insulation level (BIL) of this transformer has to be designed to match these surge levels. Both factors above will undoubtedly increase the cost of the filter. A more feasible solution will be to use the shunt active filter configuration, as depicted in Figure 2.2 on the next page.

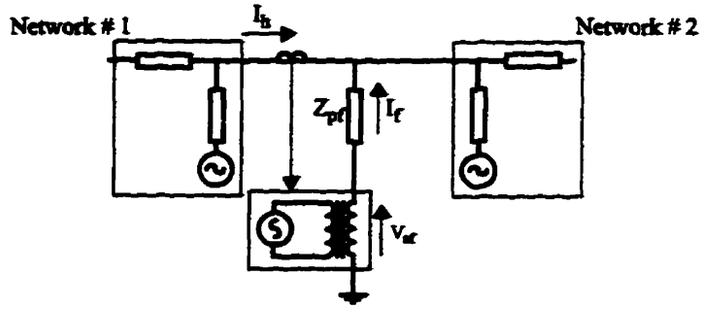


Figure 2.2 Shunt active filter

Here, the filter unit measures the harmonic current I_h, flowing in the line and produces a 'complementary' current signal I_f to cancel out the harmonics. A *de-coupling element* is placed in between the active filter unit and the line to prevent the network fundamental frequency voltage from appearing across the filter terminals. In the case presented above, a *passive filter* network with impedance Z_{pf} is used for such a purpose. This combination of active and passive filters, otherwise known as the 'hybrid active' filter, offers a lot of advantages such as:-

(1) The active filter is able to compensate for the de-tuning of the passive filter, and

(2) The passive filter can be designed to provide a low impedance path for the active filter current injection into the system and for higher order harmonics from the system to flow to ground. This arrangement reduces the workload of the active filter as the filter can now be used to cancel out the more dominant harmonics (e.g. the 11th and 13th) while the passive filter takes care of the higher order harmonics. The active filter transformer rating can then be reduced accordingly.

2.1 The 'Hybrid Active' Filter on the Ac-Side of an HVdc System

A single-line diagram of the proposed 'hybrid active' filter designed for the ac-side of an HVdc scheme is illustrated in Figure 2.3. The active filter is connected to the ac busbar through a passive filter network which, in this case, is a high-pass filter. The complementary harmonic current injection of the active filter unit is provided through a *controllable voltage source* which uses a pulse-width modulation (PWM) technique to produce the required current profile.

Next, an isolation transformer is used to provide potential isolation, voltage matching between the PWM voltage source and the voltage across the filter unit, V_{af} and some filtering of the high PWM switching frequencies [1].

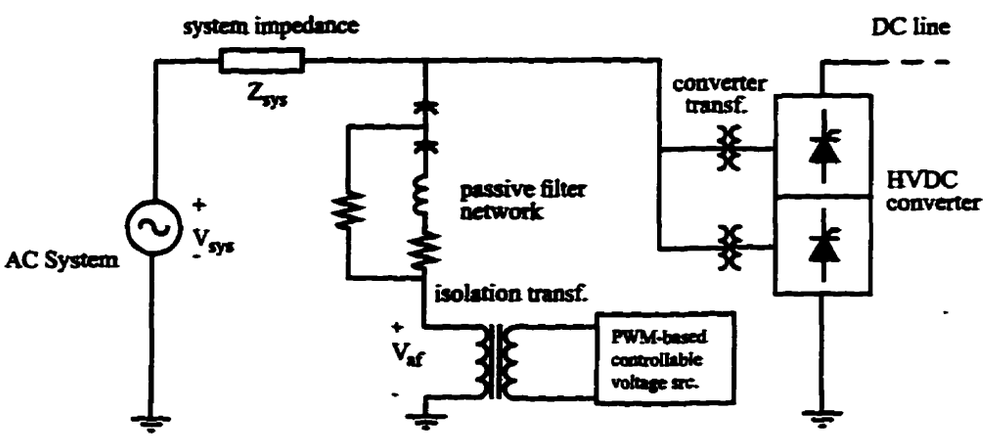


Figure 2.3 Single line diagram of the ac-side hybrid active filter

2.1.1 Equivalent Circuit

In order to develop the equivalent circuit for the hybrid active filter, the single-line diagram in Figure 2.3 on the previous page is re-drawn with the passive filter network represented by a single impedance Z_{pf} and the active filter unit replaced by a voltage source. The simplified diagram is shown in Figure 2.4 below. In this diagram, I_{load} denotes the HVdc *converter current*, I_f is the current injection from the active filter unit, V_{af} is the voltage across the active filter source and I_{sys} is the ac *system current*.

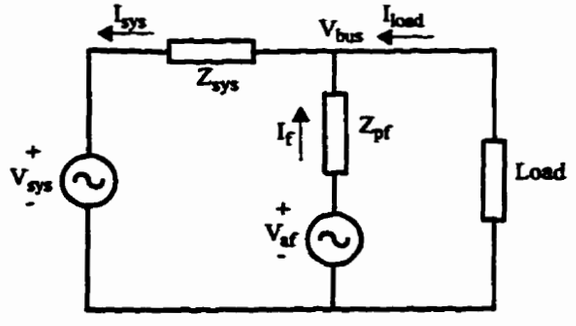


Figure 2.4 Simplified diagram of the active filter

At the fundamental frequency, the fundamental bus voltage V_{bus} will be dropped predominantly across the passive filter network; the passive filter effectively blocking out the fundamental components from the active filter unit. The active filter is no longer subjected to the full rated ac busbar voltage and current and hence can be designed with smaller transformer kVA rating and lower basic insulation level (BIL).

At the harmonic frequency f_h ($f_h = h*f_l$, where f_l is the fundamental frequency and h is the harmonic number), the equivalent circuit of the hybrid active filter will be reduced to the one depicted in Figure 2.5 below.

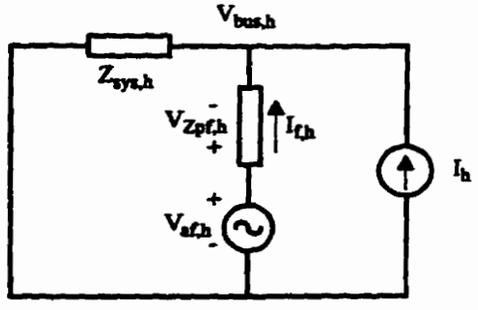


Figure 2.5 Equivalent circuit of the active filter at harmonic frequency.

In Figure 2.5, I_h represents the current generated by the harmonic source (i.e. the HVdc converter). As mentioned earlier, the active filter must produce the appropriate current signal $I_{f,h}$ to cancel out the harmonic current and thus prevents it from entering the ac system.

Therefore,

$$I_{f,h} = -I_h \tag{2.1}$$

Under the condition above, it is obvious that $V_{bus,h}$ will be zero. This can only be true if

$$V_{af,h} = V_{Z_{pf},h} \tag{2.2}$$

Where $V_{Z_{pf},h}$ is the voltage at harmonic frequency h, across the passive filter network. From equation (2.2) above, we can therefore deduce that

$$V_{af,h} = -\left(Z_{pf,h} \cdot I_h\right) \tag{2.3}$$

Equation (2.3) re-affirms the benefits of using a passive filter network as the de-coupling element. As the passive filter offers a low impedance path to ground at the tuned frequencies, only the tuned harmonic voltages will appear across the active filter terminals. Henceforth, the total voltage across the active filter terminals will be small compared to the fundamental ac voltage and this reduces the kVA requirement of the active filter isolation transformer (see Figure 2.3).

2.1.2 Steady State Calculations

Equation (2.3) developed earlier will now be used in this section to determine the kVA rating of the isolation transformer for the hybrid active filter. The transformer represents the bulk of the cost associated with the active filter installation as well as the losses [2,4] so a smaller transformer rating is desirable. To begin with, the impedance of the passive (de-coupling) filter, Z_{pf} will be calculated and its magnitude plotted against the harmonic number to verify that the filter tuning is correct.

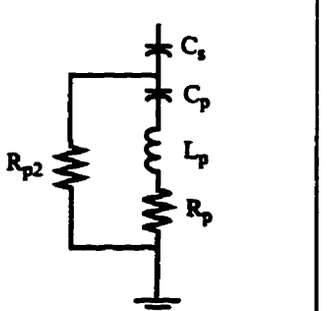


Figure 2.6 De-coupling filter

Filter parameters:

C_s = 6.685 uF

C_p = 74.27 uF

L_p = 136.4 mH

R_p = 29.76 ohms

R_{p2} = 261.87 ohms

Given,

$$Z_{arm1}(h) = Z_{C_p}(h) + Z_{L_p}(h) + Z_{R_p}(h) \qquad \text{and}$$

$$Z_{arm2}(h) = \dot{R}_{p2}$$

Thence, the passive filter impedance Z_{pf} is given by,

$$Z_{pf}(h) = Z_{C_s}(h) + \left(\frac{Z_{arm1}(h) \cdot Z_{arm2}(h)}{Z_{arm1}(h) + Z_{arm2}(h)} \right) \qquad (2.4)$$

Figure 2.7 on the next page shows the magnitude of Z_{pf} plotted against the harmonic number. In this thesis, the CIGRE HVdc Benchmark Model [11] has been used to test the active filter scheme. The filter unit is connected to the ac-side of the HVdc rectifier being fed from an ac voltage source of 345kV (rms) (see Appendix I). Now, based on the fundamental ac line current of 1.673kA (rms) and using the curves in Figures 1.1 and 1.2 shown previously in Chapter 1, the peak magnitudes of the 11th and 13th harmonic currents can be calculated. Note that the HVdc model operates at a delay angle, $\alpha = 15°$ and overlap angle, $\mu = 25°$.

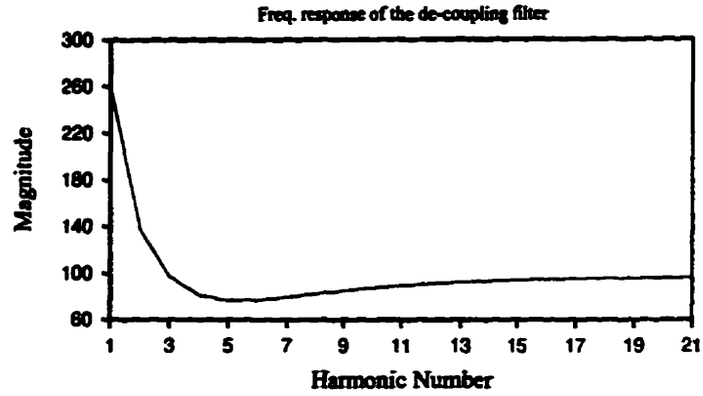


Figure 2.7 Frequency response curve for the de-coupling filter

Here, only the magnitudes of the 11th and 13th harmonic currents have been considered; the two being the dominant harmonics on the ac-side. Using equation (2.3) developed earlier and the calculated value of Z_{pf} at the chosen harmonics, the voltage across the active filter terminals can then be determined. The results are given in Table 2.1.

h	$\lvert\hat{I}_{f,h}\rvert$ Amps, rms	$\lvert\hat{V}_{af,h}\rvert$ kV, rms
11	50.19	4.47
13	25.10	2.28

Table 2.1 Magnitude of ac harmonic currents and voltages at the filter location

The kVA rating of the active filter transformer is calculated conservatively by first determining the rms values of the harmonic currents and voltages and then taking the product of both quantities.

$$I_f(rms) = \sqrt{I_{11}^2 + I_{13}^2} = \sqrt{50.19^2 + 25.10^2} = 56.12\ \text{A (rms)}$$

$$V_f(rms) = \sqrt{V_{11}^2 + V_{13}^2} = \sqrt{4.47kV^2 + 2.28kV^2} = 5.02\text{kV (rms)}$$

Thus,

$$\text{kVA}_{af} = 56.12\text{A} \times 5.02\text{kV} = \underline{0.28\ \text{MVA}}\ \text{(rms)}$$

Hence, an isolating transformer rated to at least 280 kVA will be required for the active filter on the ac-side of the HVdc system. The turns ratio of this transformer, on the other hand, will have to take into account the fact that a voltage of at least 5.02kV (rms) needs to be available on the winding side connected to the ac line. In the final design, as will be seen later, a turns ratio of 25:1 has been chosen to satisfy the above requirement.

2.2 The Dc-side Hybrid Active Filter

In this section, the hybrid active filter for the dc side of the HVdc system will be described. Most of the steps involved in the development of the equivalent circuit for the filter and the steady state equations used are similar to those already developed in the previous section and hence will only be inferred to at this stage. Figure 2.8 below shows the single-line diagram of the active filter unit connected to the dc line via a double-tuned 12/24th passive harmonic filter. The passive filter network is used primarily to provide a low impedance path for the harmonic current injection into the dc line. Nevertheless, as will be seen later in Chapter 4, the chosen passive filter is also able to provide a reasonable amount of harmonic filtering by itself.

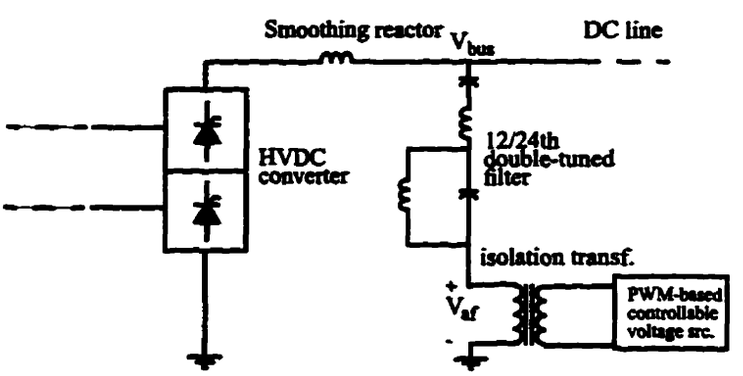


Figure 2.8 Single line diagram of the dc-side hybrid active filter

2.2.1 Equivalent Circuit

Figure 2.9 below shows the equivalent circuit of the dc-side hybrid active filter at the harmonic frequency, f_h. This circuit is derived from the single line diagram in the same way as has been done in section *2.1.1* earlier. $Z_{d,h}$ represents the impedance of the dc smoothing reactor at the harmonic frequency, f_h.

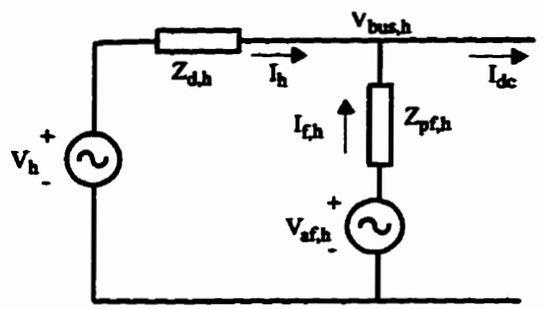


Figure 2.9 Equivalent circuit of active filter at harmonic frequency.

In the circuit above it is easy to see that at the harmonic frequency, $V_{bus,h} = 0$ for an ideal condition where we have perfect cancellation of the harmonic current emanating from the HVdc converter, I_h. Therefore, as given in the previous section, the current injection from the active filter unit, $I_{f,h}$ will be,

$$I_{f,h} = -I_h \tag{2.5}$$

Hence, $V_{af,h} = -\left(Z_{pf,h} \cdot I_h\right)$ which in actual fact is equation (2.3) from section *2.1.1* earlier.

2.2.2 Steady State Calculations

Again here, equation (2.3) is used to calculate the kVA rating of the active filter isolation transformer. In this case, only the 12th and 24th harmonic quantities are taken into consideration; both being the dominant harmonics on the dc-side of the HVdc scheme. The 12th and 24th harmonic currents are measured directly near the input terminals to the active filter unit rather than obtaining them by calculation as this seems to be more convenient. The harmonic voltages across the active filter terminals are then calculated and the results are as tabulated on the next page.

h	$\lvert\hat{I}_{f,h}\rvert$ Amps, rms	$\lvert\hat{V}_{af,h}\rvert$ kV, rms
12	9.61	0.91
24	1.22	0.11

Table 2.2 Magnitude of dc harmonic currents and voltages at the filter location

From the results above, the kVA rating of the active filter transformer is calculated conservatively by determining the rms values of the harmonic currents and voltages and taking the product of both.

$$I_f = \sqrt{I_{12}^2 + I_{24}^2} = \sqrt{9.61^2 + 1.22^2} = 9.69 \text{ A (rms)}$$

$$V_f = \sqrt{V_{12}^2 + V_{24}^2} = \sqrt{0.91kV^2 + 0.11kV^2} = 0.92 \text{ kV (rms)}$$

Thus, kVA_{af} = 9.69A x 0.92 kV = 8.91 kVA (rms). Hence, an isolating transformer rated to only 8.91 kVA will be required for the active filter on the dc-side of the HVdc system. This is quite small compared to the 280 kVA transformer required for the ac-side active filter. In the final design, a transformer rating of 9 kVA has been used. Also, a turns ratio of 10:1 has been chosen as only 0.92 kV is needed on the transformer winding connected to the de-coupling filter.

CHAPTER 3

Active Filter Modelling in PSCAD/EMTDC™

In the previous chapter, the equivalent circuit for the hybrid active filter has been developed and from the steady state equations that followed, a rough guide to the ratings and turns ratios of the active filter isolation transformers have been specified. Now in this chapter, the other component of the filter, namely the *PWM controllable voltage source* (or more commonly referred to as the *voltage source inverter* - VSI), will be developed and explained. Following this, the control blocks for the active filter as well as the control strategy employed will be studied in detail.

Before proceeding further, it should be noted here that the active filter components developed in this thesis apply equally well to both the ac- and the dc-side harmonic elimination, therefore only the dc-side filters will be examined in this chapter

In this thesis, the hybrid active filter models and their associated controls have been developed using the standard library components available in the PSCAD/EMTDC simulation software. This simulation tool provides a very flexible platform to create and simulate the transient responses of power engineering circuits such as the ones used in the active filter design.

3.1 PWM Voltage Source Inverter (VSI)

At the heart of the active filter unit is the VSI which utilizes pulse-width modulation (PWM) techniques to produce appropriate current signals to cancel out the harmonic currents from the HVdc converter. The PWM-based VSI is illustrated in Figure 3.1. Although the dc input to the VSI bridge is usually obtained by rectifying the utility ac voltage, the inverter circuit model in this thesis is provided with its own dc source to simplify the circuit. IGBTs have been proposed as the switching devices for the VSI in a number of papers describing active filters and FACTS devices [1,2,4,17,18]. However, in EMTDC, the modelling of IGBTs and GTOs are almost identical since both types of devices are simply represented by a switch with gate turn-on and turn-off controls [15]. Taking

this into consideration, GTO models (which are readily available from the PSCAD library) have been used for the switching devices in this thesis. Nevertheless, the switching characteristics of these devices have been designed to closely simulate those of IGBTs [15].

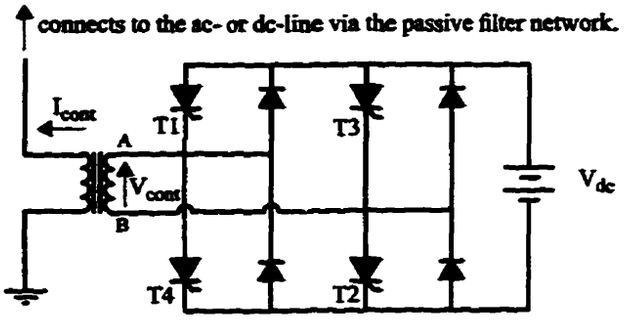


Figure 3.1 PWM voltage source inverter (VSI)

In the VSI design, a *tolerance-band* switching control strategy has been employed to turn the appropriate VSI GTO pairs on or off in order to connect the bridge outputs (A-B) to either the positive or negative pole of the direct voltage source, V_{dc} [10, 19].This effectively modulates the magnitude of the PWM inverter current output, I_{cont} to follow a *current order* from the filter controls. This concept of tolerance-band switching control is best illustrated by Figure 3.2 on the next page.

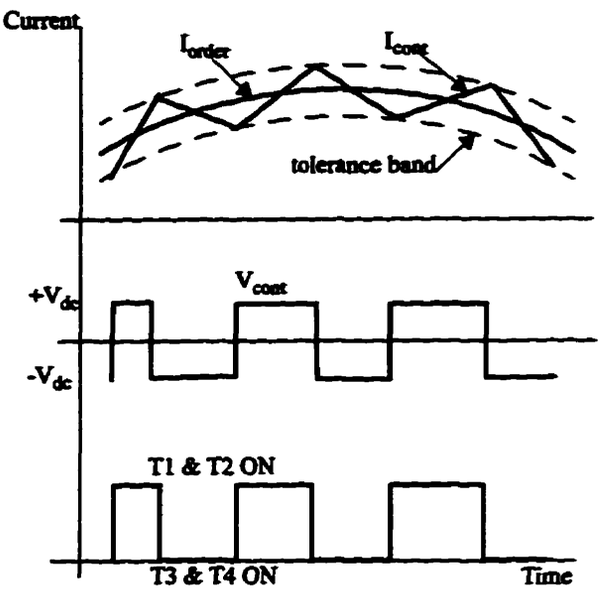


Figure 3.2 PWM inverter tolerance-band switching

As can be seen above, depending on the present level of I_{cont} in relation to I_{order} (i.e. the current order from the filter controls), GTO thyristor pairs T1,T2 or T3,T4 are switched on to modulate the VSI bridge output voltage V_{cont} to be between $+V_{dc}$ and $-V_{dc}$. The polarity changes in V_{cont} thus increases or decreases I_{cont} to within the pre-specified tolerance band limits.

3.2 Active Filter Controls

The strategy employed in the active filter controls can roughly be categorised into two distinct approaches:-

(1) Where the filter control is designed to cancel out all measurable harmonics on the line, and

(2) Where the active filter is only used to cancel out selective harmonics (usually the more troublesome ones).

In references [2,17], the PWM controller has been designed in such a way that it measures the *full complement of harmonics* on the line (by subtracting the fundamental from the measured line current) and then forces the VSI to track the measured harmonic currents by issuing the appropriate current orders. This approach eliminates all existing harmonics on the line; the down-side is that harmonic attenuation is only mediocre as the PWM has to work across a broad spectrum of frequencies.

In this thesis, a *selective harmonics elimination* approach has been taken whereby the active filter is designed to remove only the more dominant (i.e. more troublesome) harmonics from the line. All higher order harmonics are left

for the passive filters to take care of. This control strategy has been found to give a much better harmonic attenuation at the chosen frequencies with only a small voltage source required.

The dc filter controls have been divided into two groups of control blocks: (1) Harmonic current signal processing blocks and (2) PWM modulator and pulse logic control blocks. Both will be explained in greater detail in the following sections.

3.2.1 Harmonic Current Signal Processing Blocks

The harmonic current signal processing blocks are given in Figure 3.3. In order to eliminate the harmonics, the magnitudes and phases of the harmonic currents need to be determined. Here, the dc line current is measured and imported into an FFT block (available from the PSCAD components library). The FFT block then performs a Fourier analysis on the current signal and obtains its harmonic components in terms of their peak magnitudes (I_h) and phases (P_h). From this information, cosine functions are used to re-construct the 12th and 24th harmonic current waveforms. The two harmonic currents are summed up and the resultant signal inverted to form the *preliminary* reference current order.

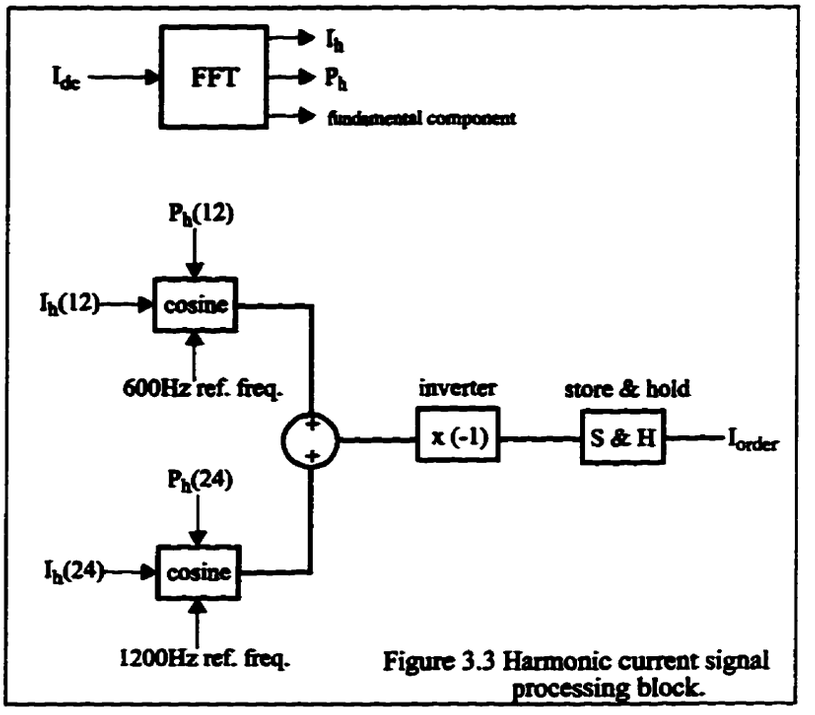


Figure 3.3 Harmonic current signal processing block.

Next, the reference current signal is passed through a 'store and hold' function block. The 'S&H' block is the PSCAD equivalent of a 'ring buffer' and introduces a 1.67ms delay into the control loop (which corresponds to one complete cycle of the 12th harmonic current). This delay is purposely put into place to approximate the response of a real-time controller whereby the processing of an input signal will inherently incur some time delay as the signal traverses through the various control blocks in the system [15]. The resultant reference current

order, referred to here as I_{order} is then sent to the next control group for further processing.

3.2.2 PWM Modulator and Pulse Logic Control Blocks

Figure 3.4 on page 44 shows the PWM modulator and pulse control logic blocks. As the name suggested, this second control group consists of two different control functions, (1) the PWM modulator, the function of which is performed by a small component called the *hysteresis buffer* (or also called a *hysterectic comparator* [17]), and (2) the pulse logic controller.

3.2.2.1 The Hysteresis Buffer

In Figure 3.4, the PWM inverter current I_{cont} is initially compared to the reference current order I_{order} to determine the deviation of the former from the latter. The *error* signal is then fed into the hysteresis buffer component which controls the width of the switching tolerance band (refer to Figure 3.2). The buffer measures the level of error signal fed into it and if the signal exceeds a user-specified *threshold limit*, the component then toggles its present logic level between 1 and 0 (depending on whether the error signal breached the upper or the lower

threshold limit). In other words, the buffer converts a real signal into a logic signal. While the error signal is within the hysteresis zone (i.e. within the threshold limit), the present logic level is maintained until the next state transition takes place.

The hysteresis function of the buffer also provides some form of noise immunity to the controls in the sense that a state transition between logic levels cannot occur until the input signal to the block (i.e. the current error signal) has moved *decidedly* across the input threshold limit set by the user [16]. By changing the input threshold limit within this control block, the user can define the width of the tolerance band used in the switching scheme and subsequently the PWM inverter switching frequency.

Figure 3.5 (a) on page 47 shows the actual waveform of I_{cont} in relation to I_{order} and also the width of the tolerance band specified in the hysteresis buffer. The output from the hysteresis buffer is a pulse-width modulated (PWM) signal which is used later to control the firing sequence of the GTO thyristor pairs in the active filter VSI (Figure 3.5 (b), page 47).

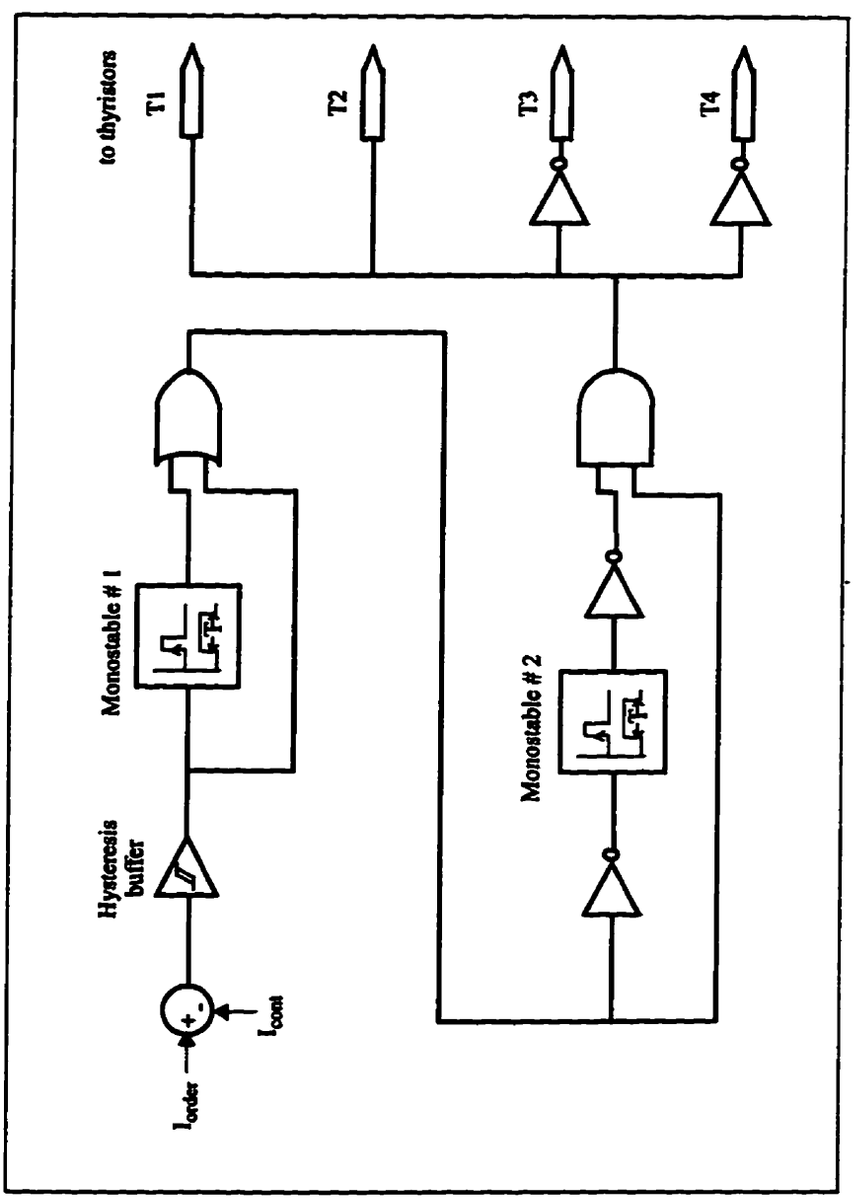


Figure 3.4 PWM modulator and pulse logic control

3.2.2.2 The Pulse Logic Controls

The pulse logic controls are not involved in controlling the firing sequence of the thyristors but rather play an important role in preventing erratic switching of the GTO devices. The controls, made up of two "monostable" buffers and their associated logic gates, are used to detect the leading and trailing edges of the PWM signal output from the hysteresis buffer and then, if necessary, to condition the signal before it is sent to trigger the GTOs.

In Figure 3.4, the first monostable unit receives a PWM signal from the hysteresis buffer and upon sensing a *leading edge* in the signal, changes its state from 0 to 1. The 'high' state is then maintained for a pre-defined time length of $30\mu s$ (a time step of $10\mu s$ has been used consistently throughout the simulation exercises in this thesis). This $30\mu s$ time delay is used to ensure that the maximum switching frequency in each of the GTOs is no more than $1/30\mu s$ or 33kHz. This limit has been intentionally designed into the controls to approximate the switching frequency characteristic of an IGBT [15]. Please refer to the switching waveforms in Figure 3.5 (c) on page 48. The first monostable output is then compared to the original PWM signal using an OR-gate.

In the second stage, the output signal from the previous stage is firstly inverted before being fed into the second monostable block. Thus, the leading edge detected by this monostable block is actually the *trailing edge* of the original PWM signal. As soon as the 'leading edge' is detected, the monostable output goes 'high' and as before, this logic state is maintained for at least 3 time steps long. The second monostable output is then inverted so that the indicated 'leading edge' will now become, once again, the trailing edge of the signal. This signal is finally re-combined with the output from the first monostable stage in an AND-gate to give a resultant output PWM signal which will produce a GTO firing sequence with a maximum switching frequency limited to 33kHz.

The actual PSCAD waveform showing the second monostable state transitions is given in Figure 3.5 (d) on page 48. An important thing to note here is that during the simulations done to produce the waveforms given in Figure 3.5 (a)-(d), none of the outputs from the hysteresis buffer component have state transitions that are less than three time steps in length so the PWM signal output from the second monostable stage is in every way identical to the original PWM signal from the hysteresis buffer. As no state transitions have violated the user-defined length of three time steps, no signal conditioning is necessary in this case.

Finally, the delayed and conditioned PWM signal is sent to initiate the proper firing sequence of the GTO thyristors in the VSI.

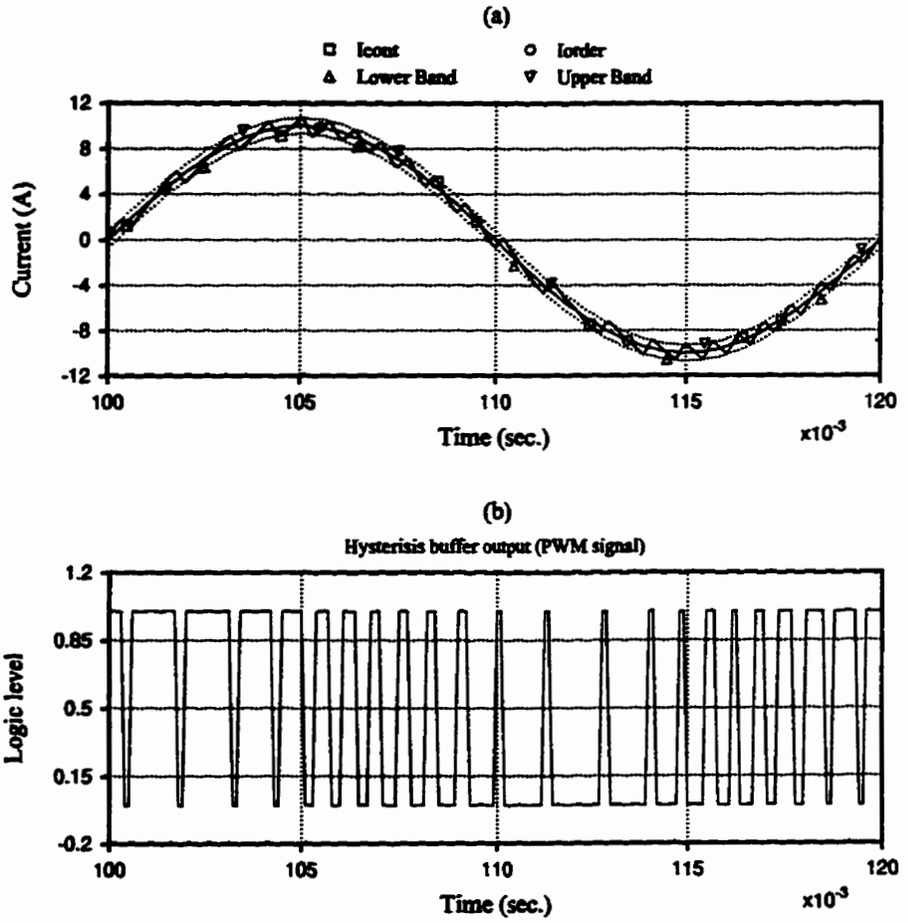


Figure 3.5 (a-b) Control blocks signal waveforms (part I)

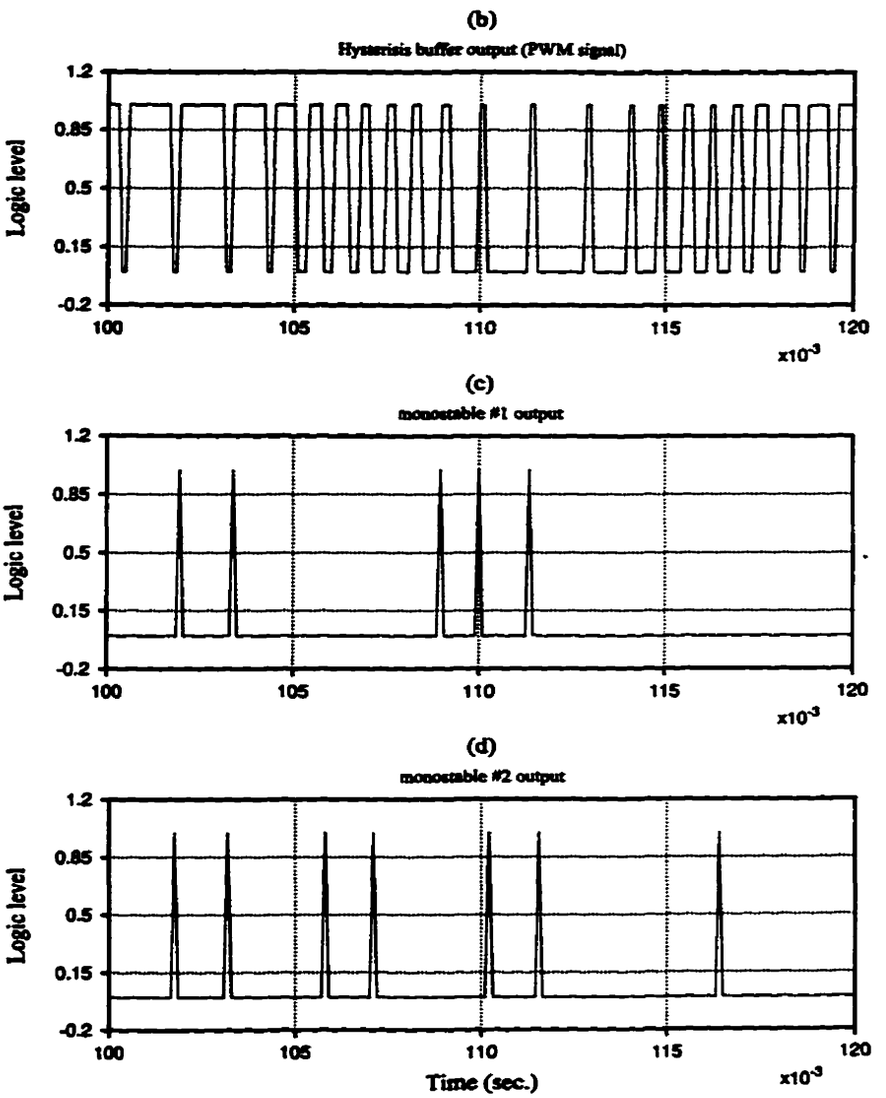


Figure 3.5 (b - d) Control blocks signal waveforms (part II)

CHAPTER 4

Steady State and Transient Simulations

lThe active filter models developed in Chapter 3 have been tested in EMTDC by connecting them to the *CIGRE HVdc Benchmark Model* [11]. Two types of simulations have been performed and the results are presented in this chapter: (1) steady state simulations, and (2) transient state simulations.

Steady state simulations are conducted to verify the feasibility of active filtering when applied to the ac- and dc-side of an HVdc scheme. From these exercises, it is hoped to be able to predict the performance of the filter in terms of the magnitudes of harmonic currents or voltages that have been prevented from entering the ac system (for ac-side active filter) or the dc line (dc-side filter). On the other hand, transient simulations are performed to test the active filter controller stability when subjected to

transient conditions such as a single- or a 3-phase fault on the ac line. Simulation of these conditions will help in identifying potential problems (if any) which may affect the performance of the active filter controller and harmonics filtering in general.

In addition, some study cases have been done to show the readers what happens when the system topology changes e.g. due to a shunt capacitor bank failure on the ac system or when a change is made in the dc smoothing reactor size. Furthermore, on the ac-side a new circuit model using a 3-phase PWM VSI feeding into a 3-phase transformer has been developed and tested to determine its feasibility and transient responses.

All these simulation runs and test cases will, hopefully, help us to better understand the workings of the active filter on both the ac- and dc-side of an HVdc system and to gauge the effectiveness of the filter installation in preventing harmonics generated from the convertor station from entering either the ac system or the dc transmission line.

4.1 Ac-side Active Filter Simulations

The ac-side active filter configuration has been detailed in Chapter 3. In that configuration, each of the three phases on the ac line is connected to a shunt filter unit through a high-pass filter network which acts as the de-coupling element. PSCAD drafts of the HVdc system with the active filter units and the filter control blocks are given in Appendix I and II.

With respect to the original CIGRE benchmark model, the 11/13th double-tuned passive filter banks which are normally provided on such a system have been removed; the slack in the reactive power availability from these filter banks is compensated by increasing the shunt capacitor sizes accordingly. With such arrangements, the active filter units are now tasked with the elimination of the 11th and 13th harmonic currents on the line; all higher order harmonics are taken care of by the high-pass filters.

4.1.1 Steady State Simulations

In the steady state simulations, the HVdc is started in the PSCAD Runtime™ module and allowed to reach a steady state condition before the active filter circuits are switched in at time t=0.6s.

Plots of the (peak) magnitudes of the 11th and 13th harmonic currents plus other important quantities are acquired within the Runtime module and imported into the PSCAD Multiplot™ module for processing and obtaining hard-copy printouts. Most of the figures provided in this chapter are obtained from the Multiplot module.

Figures 4.1 (a) and (b) on the next page show the level of reduction in the magnitudes of the 11th and 13th harmonic currents respectively, on phase 'a' of the ac line before and after the active filter units are switched in at t=0.6s; similar results are obtained from the other phases. As can be seen, the 11th and 13th harmonic currents *before* active filtering are already quite low; the 11th harmonic current, for example, is measured at only 4.0A despite the fact that the 11/13th harmonic filters have been removed from the system. This is, however, not surprising since the large shunt capacitor (10.027μF) on the ac line has provided

much of the filtering for the 11th and higher order harmonics. In addition, the de-coupling filter has also provided some harmonic filtering in the system. In Figure 4.1 (a), the active filter has reduced the 11th harmonic current magnitude on phase 'a' down to around 0.45A.

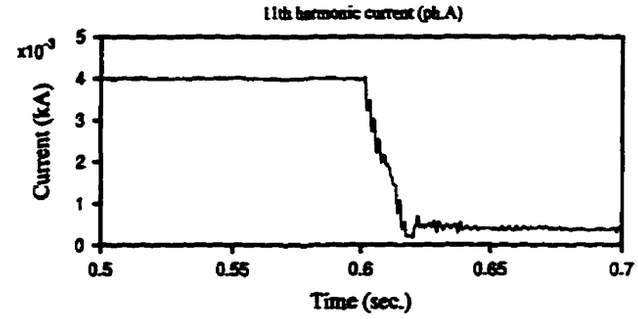


Figure 4.1 (a) Magnitude of 11th harmonic current

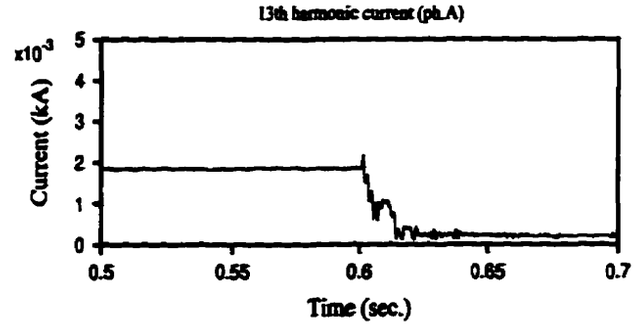


Figure 4.1 (b) Magnitude of 13th harmonic current

The influence of the shunt capacitors on the harmonic level in the ac system is reflected in total harmonic distortion (THD) measured on the current waveform (see Table 4.1 below). The active filter is able to slightly better the THD value by 0.05%.

Active filter = off	Active filter = on
THD = 1.070%	THD = 1.020%

Table 4.1 Measured total harmonic distortion (THD)

in the current waveform from Figure 4.1 (f)

However, as the HVdc converter reactive power requirement increases or decreases, the shunt capacitor banks have to be switched in and out to cater for these changes and thus we expect the harmonic levels to change accordingly. The application active filtering in this case will then ensure that whatever changes take place in the system topology, the amount of harmonics entering the ac system remains the same. This shall be illustrated in Case Study # 1 later in this chapter. In addition, the active filter also provides some immunity against changes in the ac network frequency. Figures 4.1 (c) and (d) show the active filter current output I_{cont} in relation to the current reference order I_{order} sent to the filter control circuit.

As shown, the measured switching frequency of the PWM inverter is close to 17 kHz and the specified tolerance band (Figure 4.1 (d)) is around 30A near the peak of the controller current waveform. These results are consistent with those reported by Rastogi, Mohan et.al [2].

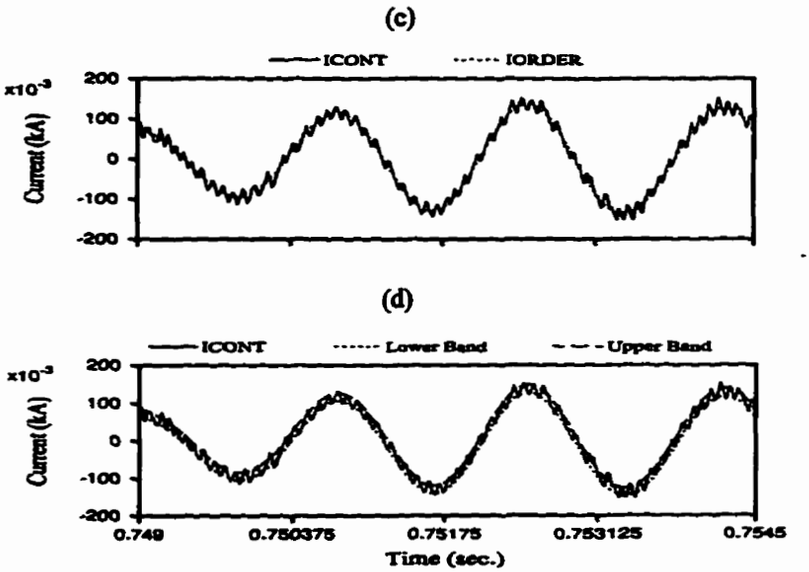


Figure 4.1 (c), (d) PWM controller current in relation to the reference current order

Next in Figures 4.1 (e) and (f), the phase 'a' current waveforms are shown to illustrate two important points: (1) the combination of the high-pass filter and the active filter is proven to be effective in removing most of the harmonics on the ac line, as indicated by the smooth current waveform measured

just beyond the harmonic filtering point (Figure 4.1 (f)), and (2) the switching-in of the active filter at time t=0.6s has negligible impact on the system as no current transients are noticeable in both waveforms.

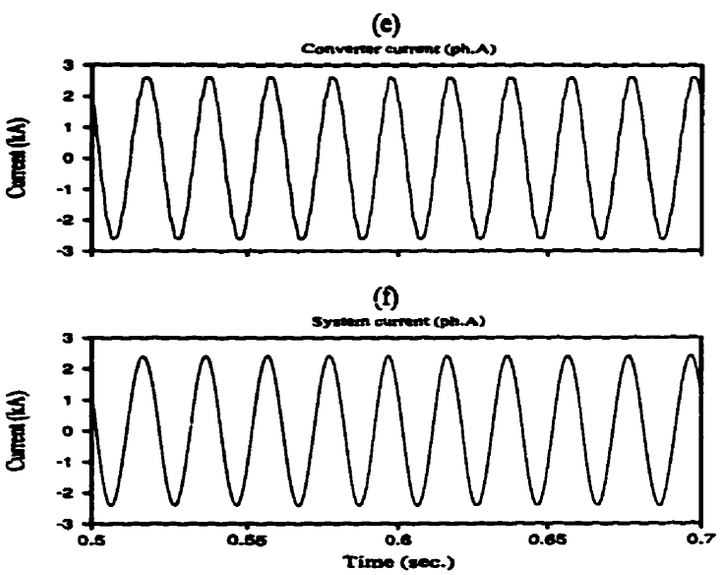


Figure 4.1 (e), (f) AC current waveforms on phase 'a'

Figures 4.1 (g) and (h) on the next page show the results of a Fourier analysis performed on the ac current waveforms from Figures 4.1 (e) and (f), respectively. In the topmost plot, the system is shown to have a predominant 11th and 13th harmonics and also a significant amount of 23rd and 25th harmonic cur-

rents. The combination of high-pass and active filters is then shown (in the bottom plot) to have successfully remove most of the harmonics from the line.

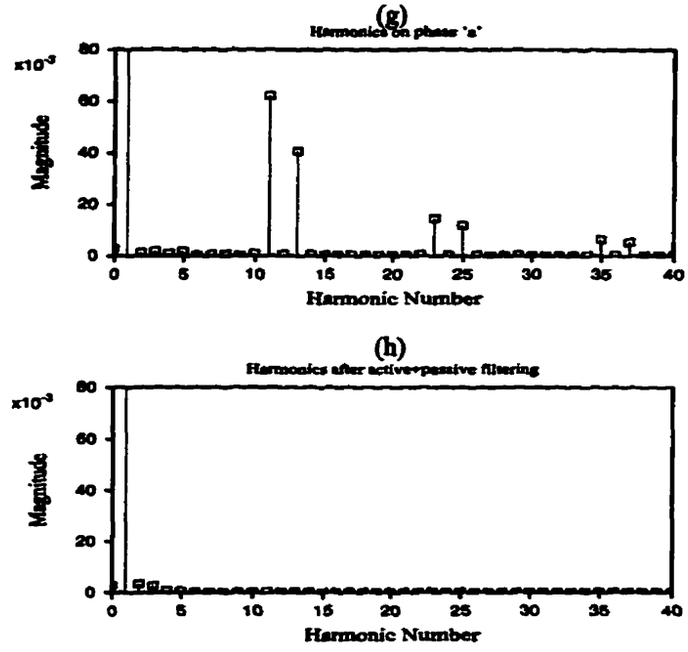


Figure 4.1 (g), (h) Current harmonics on phase 'a' before and after application of passive and active filtering

4.1.2 Case Study # 1: Shunt Capacitor Bank Failure

In the previous section, the shunt capacitor banks have been shown to impart a significant influence on the level of harmonic currents on the ac line. This case study will show the effect of a reduction in the shunt capacitor size due to a capacitor failure and how the active filter can then lend support in preventing the increased current harmonics from entering the system. In this case study, the shunt capacitor values have been reduced by 25% to 7.52μF and the steady state simulation repeated in the same manner as described in section 4.1.1.

Figure 4.2 on the next page shows the reduction in the 11th harmonic current magnitude upon switching-in of the active filter. The current magnitude prior to the application of active filtering is nearly 9.2A and the filter is able to reduce this current to 0.73A. As have been done previously, the THD is measured on the ac current waveforms and the results are presented in Table 4.2 below.

Active filter = off	Active filter = on
THD = 1.301%	THD = 1.025%

Table 4.2 Measured total harmonic distortion (THD)

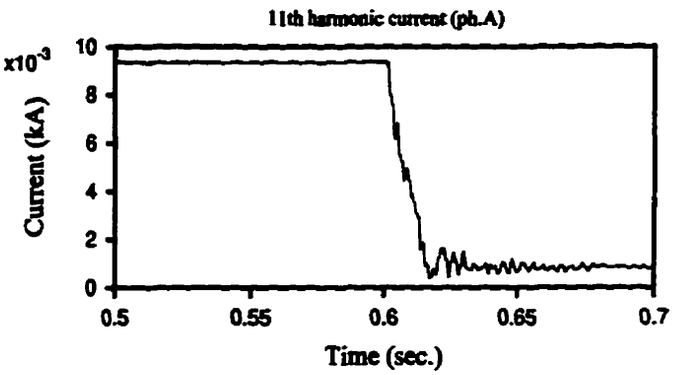


Figure 4.2 Magnitude of 11th harmonic current

With a 25% reduction in the shunt capacitor value, the THD as measured on the ac current waveform has increased by approximately 21.5% compared to the 1.070% THD obtained in the previous section (see Table 4.1). The use of an active filter in this case has the effect of reducing the THD to around 1.025%; almost back to the same level as it has been with the full shunt capacitor banks in place. This simple exercise thus shows the flexibility of the active filter to adapt to changes in the ac network - as quoted earlier in the introduction to this thesis.

4.1.3 Transient Simulations

Transient simulations are conducted to evaluate the active filter controller action in response to system disturbances at start-up and also due to single- and 3-phase faults. This will give some indication as to how stable the controller is and whether such disturbances have any effect on the filter performance.

4.1.3.1 System Start-up

In this part of the simulation, the HVdc system is started with and without the active filter switched in. This exercise is done in order to ascertain whether any unnecessary disturbances is caused by the active filter operation which will then necessitate the use of a viable start-up procedure as suggested by Rastogi, Mohan, et. al. [2].

Figures 4.3 (a) and (b) on the next page show a comparison between the phase 'a' system current waveforms at system start-up under both conditions described above. The current waveforms indicate that there are no obvious problems associated with system start-up with the active filter on and therefore it can be concluded that, at least in this particular system, no special start-up procedure needs to be employed.

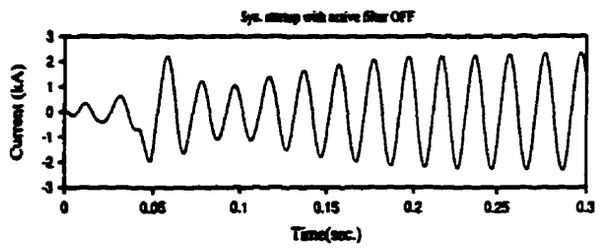


Figure 4.3 (a) System start-up with active filter off

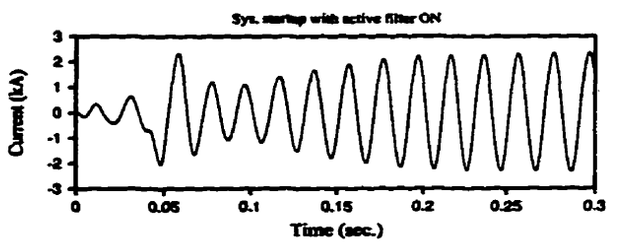


Figure 4.3 (b) System start-up with active filter on

4.1.3.2 System Response to a Single-phase Fault

Throughout all the single- and 3-phase tests which will be detailed in the following sections, the active filter is switched on at the starting point in the simulation run and remains connected to the system until the end of the test. In this section of the thesis, a single line-to-ground (L-G) fault is applied to the phase 'a' of the system at time t=0.6s and for a duration of 50ms.

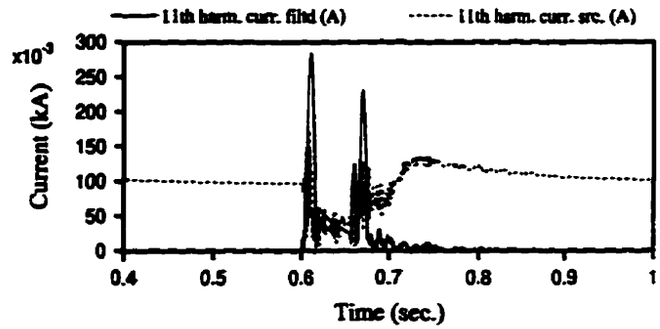


Figure 4.4 (a) 11th harmonic current magnitude following a single L-G fault on phase 'a'

Figure 4.4 (a) above shows the transients in the 11th harmonic current magnitude following the applied L-G fault on phase 'a' and also the recovery period thereafter. As illustrated above, the active filter controller is able to recover from the transient condition and continue with its task after about 0.2s with no observable degradation in the harmonic filtering performance. (Note: harm. curr. filtd = *system harmonic current*, harm. curr. src. = *converter harmonic current*)

Next, in Figure 4.4 (b), the filtered ac current waveforms (i.e. the *system currents*) indicate that during the first half-cycle following the fault, a huge overcurrent nearly 10.5kA in magnitude has occurred on phase 'a'. The overcurrent condition persisted during the next two cycles before the phase current returned to normal as the fault is cleared at time t=0.65s.

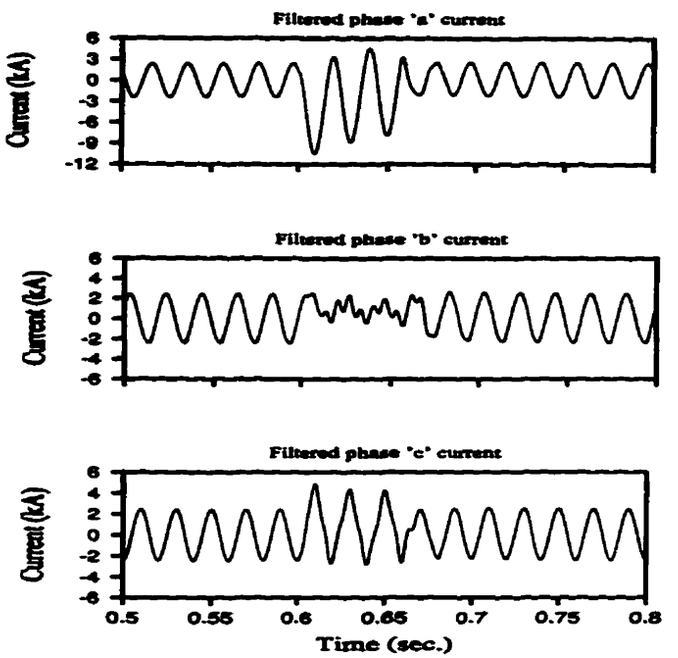


Figure 4.4 (b) Phase currents during L-G fault

4.1.3.3 System Response to a 3-phase Fault

This section details the 3-phase L-G fault simulations on the HVdc system described in the previous section. Here, a L-G fault is applied on all three phases on the ac line at time t=0.6s for a duration of 50ms while the active filter is connected to the system. As mentioned earlier, each of the ac line is connected to a single-phase PWM inverter through a high-pass filter network acting as the

de-coupling element. Figure 4.5 (a) below shows the transients in the 11th harmonic current magnitudes due to the applied 3-phase fault.

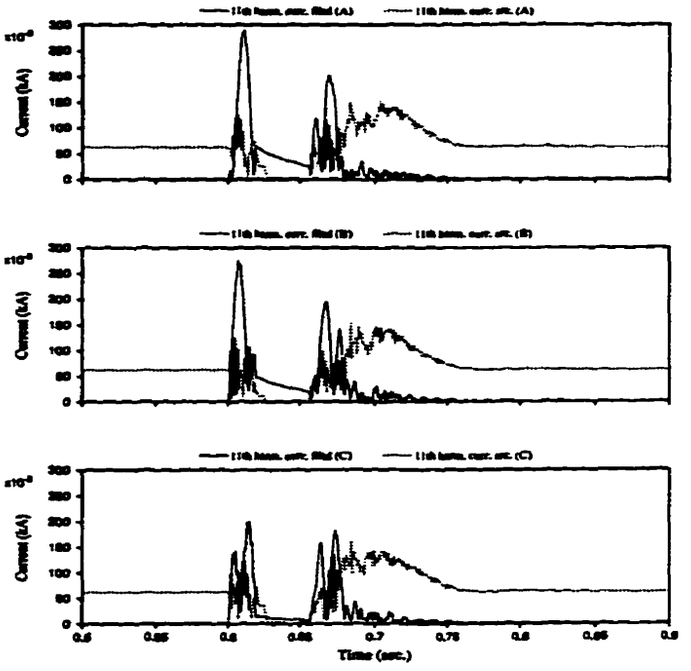


Figure 4.5 (a) 11th harmonic current magnitudes following a 3-phase fault

Again here, the active filter controllers are able to recover from the severe 3-phase fault approximately 0.15s after the faults are cleared. No controller instability is detected even after application of such a severe fault thus indicating the robust nature of the designed controls for the filter.

4.1.3.4 Case Study # 2: 3-Phase PWM Inverter

For this section, a 3-phase PWM voltage source inverter (VSI) feeding into the ac line through a 3-phase 25:1 isolation transformer rated at (3 x 280) kVA has been developed (Note: in the single-phase design, a 280 kVA transformer has been used). As usual, a high-pass filter network has been used as the de-coupling element while the 11/13th filters have been removed from the ac line. The PSCAD draft illustrating this new VSI configuration is shown in Appendix III. A simplified diagram of the circuit is shown in Figure 4.6 on the next page.

Comparing this circuit to the original ac-side active filter (Appendix I), we can see that the new circuit uses half the number of GTOs and diodes and a single 3-phase transformer instead of 3 separate single-phase ones. This new configuration obviously makes for a more compact filter design than the original single-phase circuit.

The VSI works on the assumption that the three phase harmonic current inputs to the active filter controller add up to zero. In other words, it is assumed here that there is no zero-sequence harmonic current flowing on the ac line - a valid deduction for a system with a balanced 3-phase supply from the ac

source. As such, it is interesting to find out how such a filter configuration performs under imbalance condition on the system; a condition which may occur, for example, due to an asymmetrical fault on the line (i.e. a single-phase L-G fault).

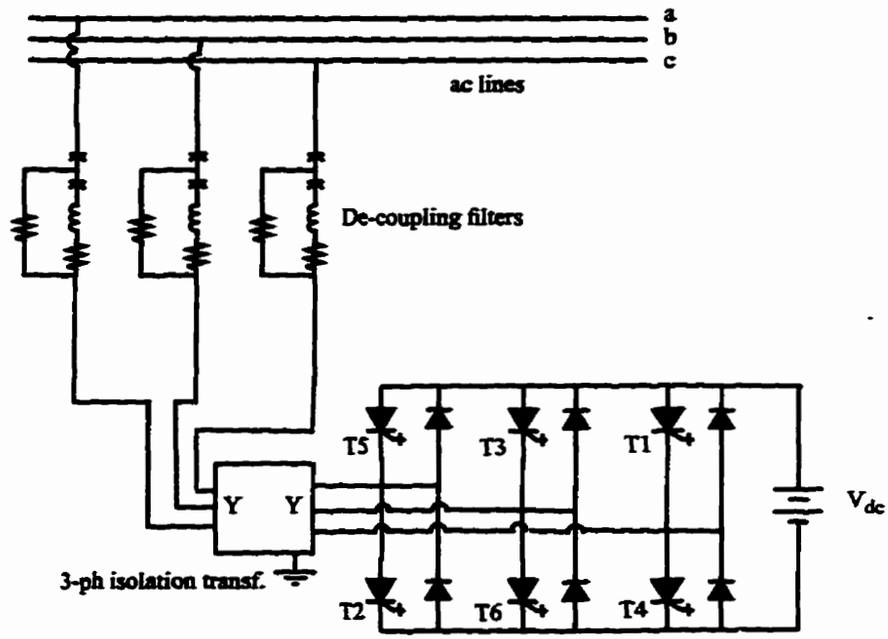


Figure 4.6 3-phase PWM voltage source inverter

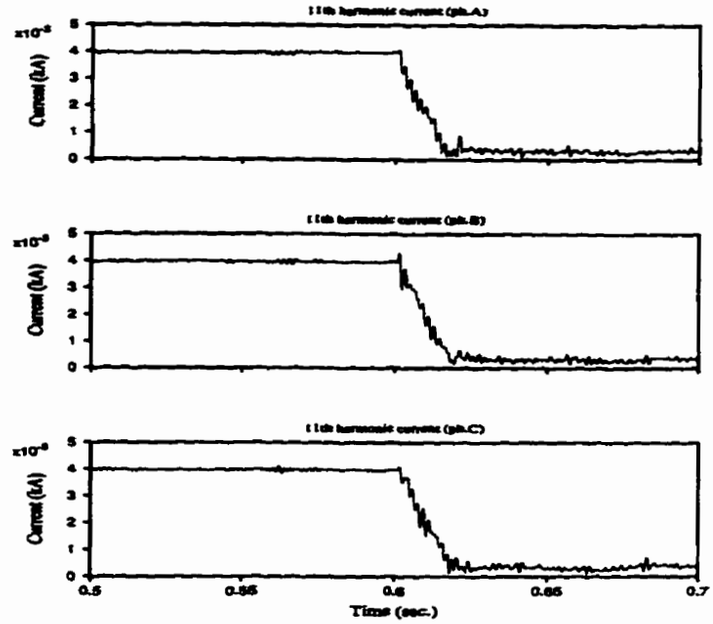


Figure 4.6 (a) 11th harmonic current magnitudes

Figure 4.6 (a) above illustrates the magnitudes of the 11th harmonic currents being reduced to around 0.35A after the active filters are switched in at time t=0.6s. The achieved reduction in the 11th harmonic current magnitude confirms that under balanced system condition, the 3-phase PWM VSI performance is at least on par with those obtained earlier using the single-phase PWM circuit.

Now, the same circuit is subjected to a single-phase L-G fault similar to the one discussed earlier in section *4.1.3.2*. Figure 4.6 (b) then shows the

magnitude of the 11th harmonic current on the line before the applied fault and during the recovery period.

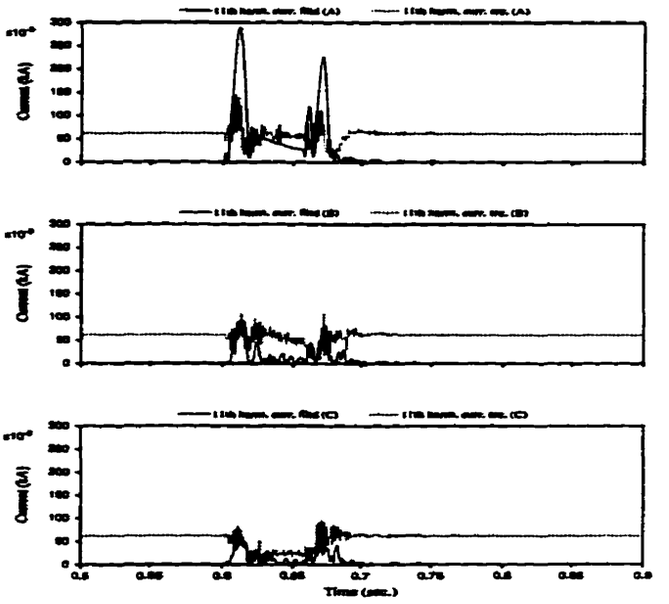


Figure 4.6 (b) 11th harmonic current magnitudes during single-phase fault

The plots above prove that the transient harmonic currents on the two unfaulted phases are not as bad as expected under such imbalance condition. Although the single-phase fault has caused some degradation in the filtering performance on the other two phases, the active filter is still capable of correcting itself as soon as the fault is cleared from the line. In addition, no adverse transient overcurrents are present on the two unfaulted lines.

4.2 Dc-side Active Filter Simulations

The dc-side active filter configuration has also been explained in detail in the previous chapter. In the configuration dictated in Chapter 3, the active filter unit is connected to the dc line through a double-tuned 12/24 passive filter network which acts as the de-coupling element. However, as shown through the steady state calculations performed in Chapter 2, the dc-side active filtering only requires an isolation transformer rated to 8.9kVA. A turns ratio of 10:1 has been chosen for this transformer to provide enough current output from the PWM inverter to match the dc harmonic currents to be eliminated.

With reference to the original CIGRE HVdc benchmark model used as the test system in this thesis, a few parametric adjustments have to be made to this model to facilitate the dc-side simulations. The CIGRE model design is actually based on a real HVdc scheme which connections are via long dc cables and as such, the huge cable capacitance have made redundant the need for filters to be installed on the dc side. Therefore, the dc line parameters have been modified to approximate a long overhead dc transmission line while two 400mH smoothing reactor have been installed at both ends of the line. The PSCAD drafts showing the dc-side active filter installations and the filter controls can be found in

Appendix IV and V. Please note that active filtering is only provided on the rectifier side of the system; no harmonic filtering is applied on the inverter side of the dc line.

In this part of the thesis, only steady state simulation runs have been conducted. Faults on the ac side of the system is normally dealt with by the HVdc converter controls which limits the converter operation and prevents much of the transient energy associated with such occurrences from propagating into the dc side of the system. For dc line faults, the converter controls will normally revert to a special mode of operation called "force-retarding" [6, pg.174] which is designed to dissipate the energy from the fault transients. Thus, it is assumed that any occurrences of fault on either the ac- or the dc-side will not badly affect the active filter controls.

The dc-side active filter controls have been designed to eliminate only the 12th and 24th harmonic currents - the two being the more prominent harmonics on the dc side. In the case study for this section of the thesis, the rectifier-side dc smoothing reactor size is reduced by as much as 50%, thus increasing the dc harmonic currents and consequently the work load imposed on the active filter circuit. The active filter performance under such condition is then investigated.

4.2.1 Steady State Simulations

Figures 4.7 (a) and (b) show the reduction in the magnitudes of the 12th and 24th harmonic currents due to active filtering applied at time t=0.6s. (Note: harm. curr. filtd = *dc line harmonic current*, harm. current (REC) = *rectifier harmonic current*)

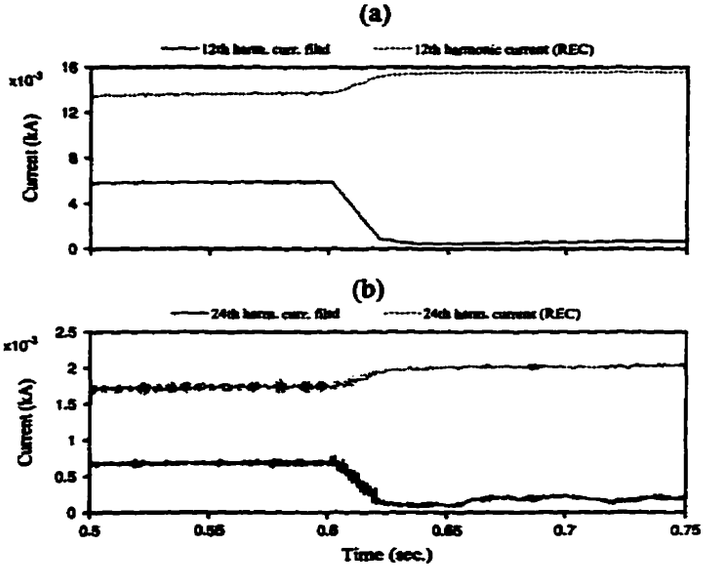


Figure 4.7 (a) and (b) Magnitudes of the 12th and 24th harmonic currents.

The magnitudes of the 12th and 24th harmonic currents on the dc line before the application of active filtering are 13.6A and 1.75A, respectively. The

use of a 12/24 double-tuned passive filter as a de-coupling element has given an added benefit of partially removing some of the 12th and 24th harmonic currents from the line. The switching in of the active filter then reduces the harmonics to around 0.6A (12th) and 0.16A (24th). Table 4.3 below gives the 12th and 24th harmonic current magnitudes as a percentage of the rated dc line current of 2kA.

Harmonic order	Harmonic currents as a percentage of the rated dc line current	
	Active filter = off	Active filter = on
12	0.68%	0.03%
24	0.09%	0.008%

Table 4.3 12th and 24th harmonic current magnitudes as a percentage of the rated dc current

The findings above can be confirmed through a Fourier analysis on the dc current waveform, the result of which is shown in Figure 4.7 (c) on the next page. Note that the dc current contains a small amount of first and second order harmonics. These harmonics are, however, not significant enough to be of any problem on the dc line and are thus left untreated in the present case.

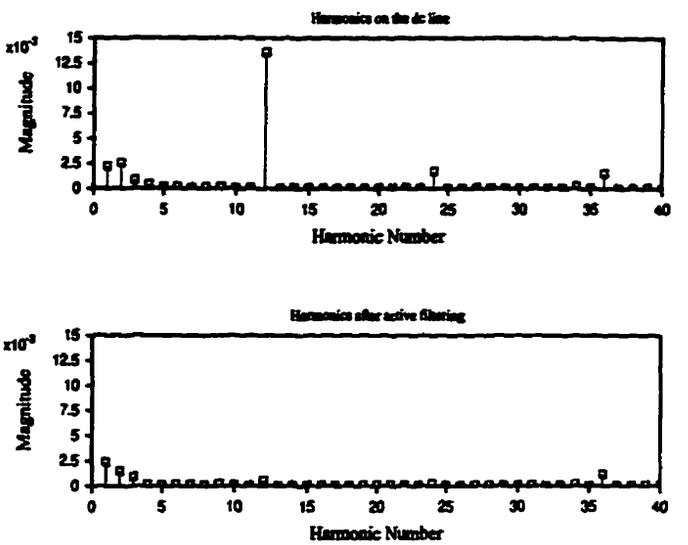


Figure 4.7 (c) Fourier analysis on the dc line current

4.2.2 Case Study # 3: Reduction in the DC Smoothing Reactor

Smoothing reactors are installed on the dc line to remove some of the dc ripples produced by the HVdc converter thyristor firing. The same function can be performed by an active filter and thus, in HVdc schemes where a dc-side active filter has been proposed, the size of the smoothing reactor is usually reduced by 50% for economic reasons.

The aim of this case study is therefore to investigate the active filter performance under such a proposal. As the starting point, the smoothing reactor on the rectifier side of the HVdc converter has been reduced to 200mH. Figures 4.8 (a) and (b) below show the increased magnitudes of the 12th and 24th harmonic currents on the dc line and the reductions achieved by active filtering.

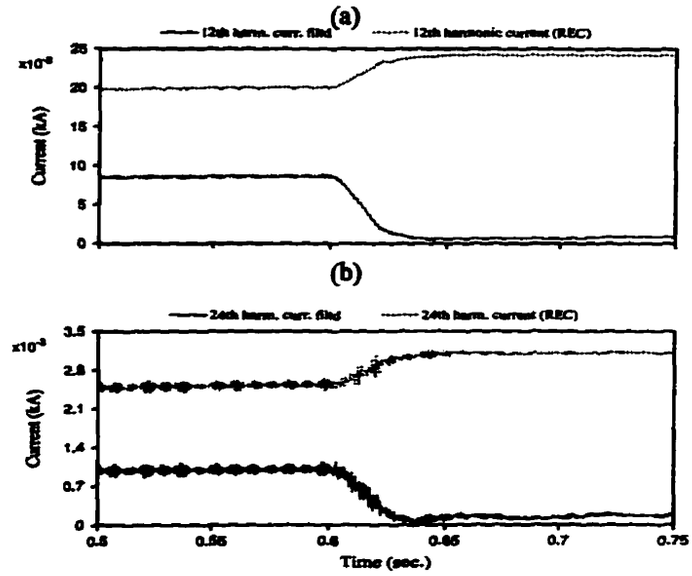


Figure 4.8 (a) and (b) Magnitudes of the 12th and 24th harmonic currents

The plots above show that the application of active filtering has been successful in reducing the 12th and 24th harmonic currents to 0.62A and 0.147A

respectively. The harmonics have effectively been reduced to the same level as achieved previously in section *4.2.1* with the original smoothing reactor size of 400mH, despite the fact that the unfiltered level of harmonics on the dc line have increased by almost 40%. Therefore, the installation of an active filter unit on the dc line has enabled us to reduce the dc smoothing reactor size considerably without increasing the level of harmonic currents entering the dc transmission line.

4.3 Summary

In view of the amount of information presented in this chapter, it is only prudent that the chapter be concluded with a brief summary of the results obtained thus far:

- On the ac-side, the active filter has been proven to be effective even when the system is subjected to a 25% reduction in the shunt capacitor values which effectively increases the ac harmonic currents by more than 20%.
- Operation of the filter controls remains stable under single and 3-phase L-G faults on the ac line. The filter controls have been able to resume normal filtering operation in under 0.2s following the clearing of the fault.

- The 3-phase PWM circuit developed in section *4.1.3.4* has been shown to perform well under an asymmetrical fault on the ac line. Although the filtering performance on the unfaulted lines is affected by the single-phase fault, this has not lead to unstable filter operation on the whole. The 3-phase configuration has the advantages of being more compact in design and also requiring less number of components compared to single-phase active filters.
- On the dc-side, the use of an active filter has made it possible to reduce the size of the dc smoothing reactor by as much as 50% without compromising on the harmonic filtering performance on the dc line. The active filter has performed well despite the fact that the dc harmonics in the system has increased by almost 40%.

CHAPTER 5

Active Filter Installation in a Capacitor Commutated Converter (CCC) Scheme

In the previous chapter, it has been shown in the ac-side active filter application that the passive filter banks which are normally installed on the line can be removed altogether; their functions are then taken over by active filters. Nevertheless, the amount of reactive power that these filter banks provide obviously has to be compensated and this entails the need to increase the size of the shunt capacitors. Hence, the economic savings gained from the reduction in the passive filter banks are then lost to the increased size of the shunt capacitors.

In recent years, a new type of HVdc converter scheme called the Capacitor Commutated Converter (CCC) has been introduced by ABB and this new concept in ac-dc conversion seems poised to take advantage of the benefits provided by the active filter technology [5]. The principles

behind the CCC will not be discussed here as they are beyond the scope of the thesis. Nevertheless, readers will find excellent background and theoretical analysis of the CCC concept provided in published papers by Reeves, et. al. [12] and Gole, et. al. [13]. Suffice to say here that, unlike the conventional HVdc converter which reactive power consumption amounts to about 0.5 pu (per unit) of the active power, the CCC concept (as proposed by ABB) makes use of the *commutation capacitors* (Figure 5.1) to provide reactive power compensation proportional to the load of the HVdc converter. As such, minimal reactive power is required from the ac system and therefore the shunt capacitor banks can be eliminated. The small reactive power consumption by the converter can be compensated merely through the reactive power generation of the passive ac filter banks.

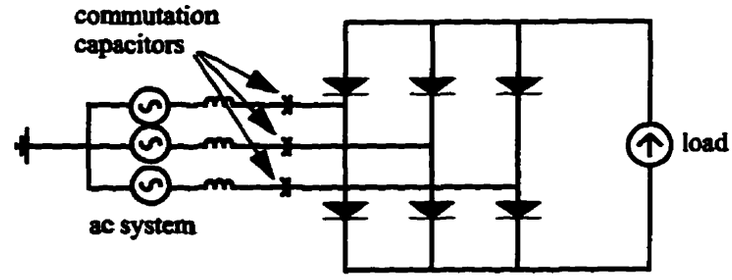


Figure 5.1 Capacitor Commutated Converter (CCC)

Under such circumstances, the use of an active filter on the ac-side of the system has its economic advantages in the sense that the passive filter network used as the de-coupling element for the active filter unit can then be designed to produce the required reactive power compensation for the system while the active filter unit bears the burden of eliminating the ac-side harmonic currents. Cost savings are then realised in the form of reduced converter station area requirement and the equally reduced complexity of the filter installation. The smaller shunt filters will also decrease significantly the load rejection overvoltage on the ac-side of the HVdc converter in the event of a thyristor commutation failure [5, 6, p.186].

In this chapter, a simplified circuit of the CCC developed by my colleague, Mr. A.H. Hashim for the preliminary work on his Masters thesis has been used to gauge the feasibility and performance of an ac-side active filter installation within the CCC scheme [14]. The PSCAD draft of this circuit is presented in Appendix VI. Note that detailed active filter configuration has been shown only on phase 'c'; the filters on the other phases are simply represented using block diagrams. The active filter unit in this particular exercise is connected to the ac system via a high-pass filter network which acts as the de-coupling element and also provides the small amount of reactive power compensation required by the HVdc converter. It should be noted here that the CCC equivalent circuit has been mod-

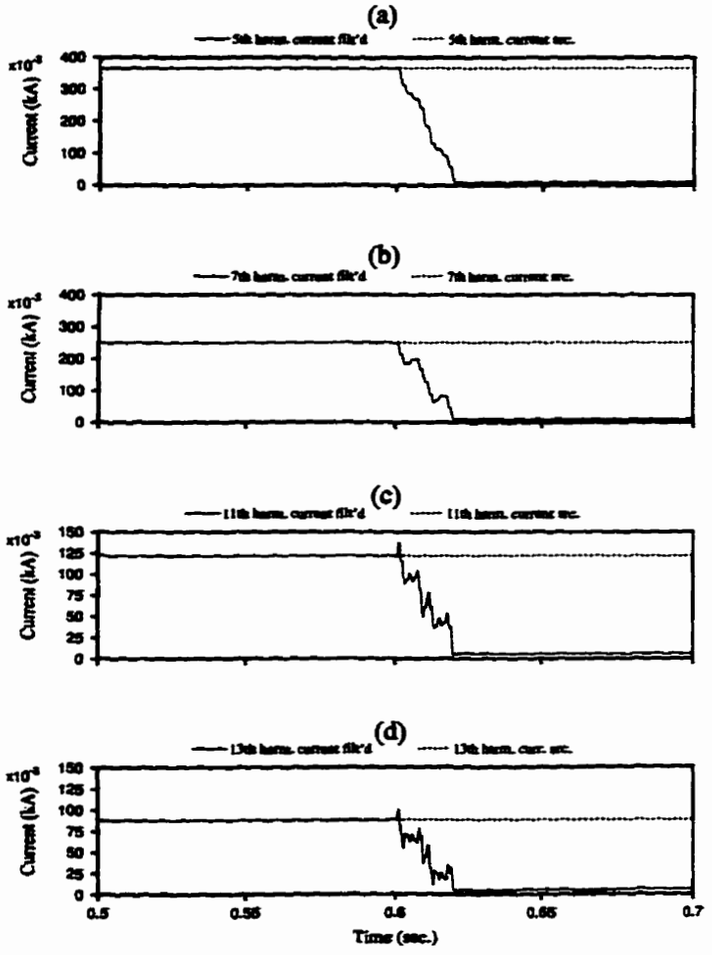
elled only as a 6-pulse converter and therefore, the dominant ac-side harmonics, according to equation (1.2) in Chapter 1, are the 5th and 7th.

Taking this into consideration, the filter controls have been modified to eliminate the 5th and 7th harmonic currents as well as the 11th and 13th, as have been done previously. Persson et. al. [5] have mentioned in their paper that the CCC produces up to 20% more harmonics compared to the conventional HVdc converter and therefore, the rating of the active filter isolation transformer has been increased proportionally to match the increased harmonics and workload imposed by the 5th and 7th harmonic currents elimination.

5.1 Steady State Simulation

Steady state simulations not too dissimilar to the ones detailed in the previous chapter have been repeated in this section to determine the active filter performance in eliminating the 5th, 7th, 11th and 13th harmonic currents on the ac line. Figures 5.1 (a) - (d) on the next page illustrate the harmonic current reductions on the line when the active filter circuit is switched in at time t=0.6s. The steady state harmonic currents have been measured to be between 360A (5th) and

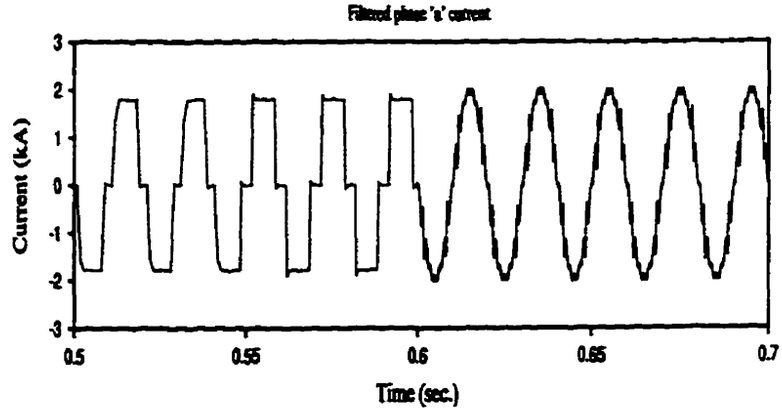
88A (13th) and the active filter has then been able to reduce them to between 8.5A and 5.18A, respectively.



Figures 5.1 (a) - (d) Magnitudes of the 5th, 7th, 11th and 13th harmonic currents.

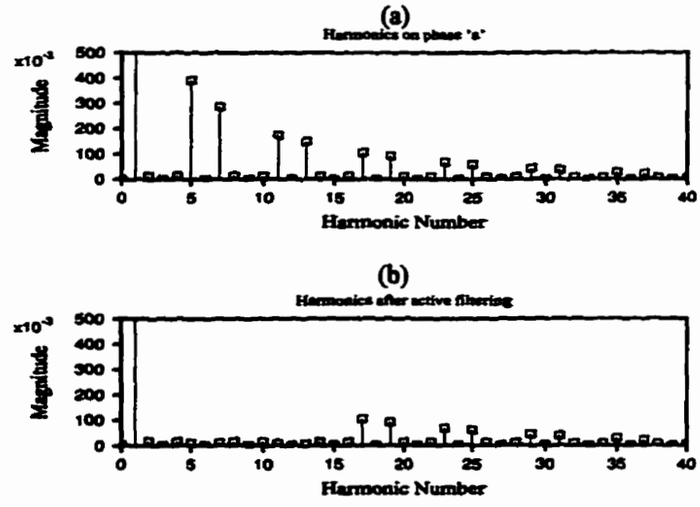
The huge reduction in the harmonic current contents on the ac line is clearly reflected in the phase 'a' current waveform shown in Figure 5.2 below. The waveform after the active filter has been switched on appears to be more sinusoidal, albeit having slight transients due to the PWM switching.

The current transients are more apparent now as the PWM inverter current injection has been increased to compensate for the increased harmonic currents on the ac line.



Figures 5.2 Phase 'a' current waveform

Figures 5.3 (a) and (b) below show the results of a Fourier analysis on the current waveform from the previous page. At a glance, it is evident that the four dominant harmonics on the ac line have been successfully removed by the active filter. The other higher order harmonics, for example the 17th and the 19th which are somewhat significant in the present system, can easily be included in the active filter controls, if such actions are deemed necessary. As mentioned earlier in the introductory chapter to this thesis, such modifications to the filter controls are mostly software-based and therefore will not incur significant financial constraints on the part of the power utility.



Figures 5.3 (a) and (b) Current harmonics on phase 'a' before and after active filtering

CHAPTER 6

Conclusions

First and foremost, detailed PSCAD/EMTDC™ models of the 'hybrid-active' filters for both the ac- and dc-side of an HVdc scheme have been developed. Although the PWM-based VSI has been modelled using GTO thyristors, IGBT switching characteristics have been designed into the filter controls to give a more practical feel to the models. Signal processing delays have also been incorporated into the filter controller design to simulate the delays in real time controllers. The active filter isolation transformer has also been given special attention since it is felt that the cost of the transformer unit itself will, in the end, dictate the overall cost of such filter installations. The transformer has been designed to be as small as possible yet capable of providing the VSI with enough current injection to satisfactorily cancel out harmonic currents on the ac or dc line.

The models have then been integrated within the CIGRE HVdc Benchmark Model using properly designed de-coupling elements, to evaluate their effectiveness in reducing harmonic currents in the system and also to test the active filter controller responses to transient conditions typical to such an HVdc scheme.

Next, steady state and transient simulations have been performed on the CIGRE HVdc Benchmark Model with active filters installed on the ac- and then the dc-side of the system. The simulation results can be summarised as follows:

- The ac-side active filter has been proven to perform satisfactorily even when the ac shunt capacitors are reduced by as much as 25%. Although under such circumstances the ac harmonics have been found to have increased by as much as 20%, no degradation in active filtering performance has been noticed.
- Operations of the active filter controls have been observed to be stable under severe single- and 3-phase faults on the ac line. Under those conditions, the filter controls have been able to resume normal filtering operation after 0.2s following the clearing of the fault.

- Installation of the dc-side active filter has made it possible to reduce the size of the dc smoothing reactor by as much as 50% without increasing the level of harmonic current entering the dc line. The active filter has been shown to perform quite well despite the fact that the dc harmonics have then increased by almost 40%.

In Chapter 5, an investigation into the feasibility and performance of an ac-side active filter installation within the Capacitor Commutated Converter (CCC) HVdc scheme has been carried out. For this exercise, a simple equivalent circuit of the CCC based on the design proposed by ABB has been used. Again, the active filters has been shown to be effective in eliminating a significant amount of ac harmonic current from the line. This has been achieved despite the fact that the CCC design is widely known to generate as much as 20% more harmonics compared to a conventional HVdc converter. In addition, the de-coupling filter used in the active filter configuration can be re-designed to also provide the minimum required reactive power compensation for the CCC, therefore eliminating the need to install additional passive filters on the system. Using this approach, cost savings can be realised in the form of reduced converter station area requirement and the equally reduced complexity of the filter installation.

6.1 Recommendations for Further Work on Active Filters

Firstly, the active filter controls can be improved further to include, for example, supervisory and protective functions such as those proposed by Sadek, et. al. [1]. This will, for example, monitor the state of the PWM switching devices and initiate an automatic filter shutdown should an IGBT device failure be detected which, invariably, will lead to incorrect switching sequences in the VSI.

Another control strategy which has not been looked at in this thesis but is nevertheless very practical, involves the measurement of the line voltage and processing it in such a way as to make the active filter appears like a substantially resistive impedance at the chosen frequencies, thus providing positive damping to the system [1,10].

With regards to the 3-phase PWM inverter developed in Chapter 4, Raju, Venkata et. al. [18] have proposed the use of a capacitor to replace the dc source used in the VSI. This may be possible provided the VSI is properly designed to allow a small active power flow into the circuit to maintain enough voltage across the inverter capacitor. This constant voltage is necessary for the capacitor to produce and sustain the required current injection into the ac line.

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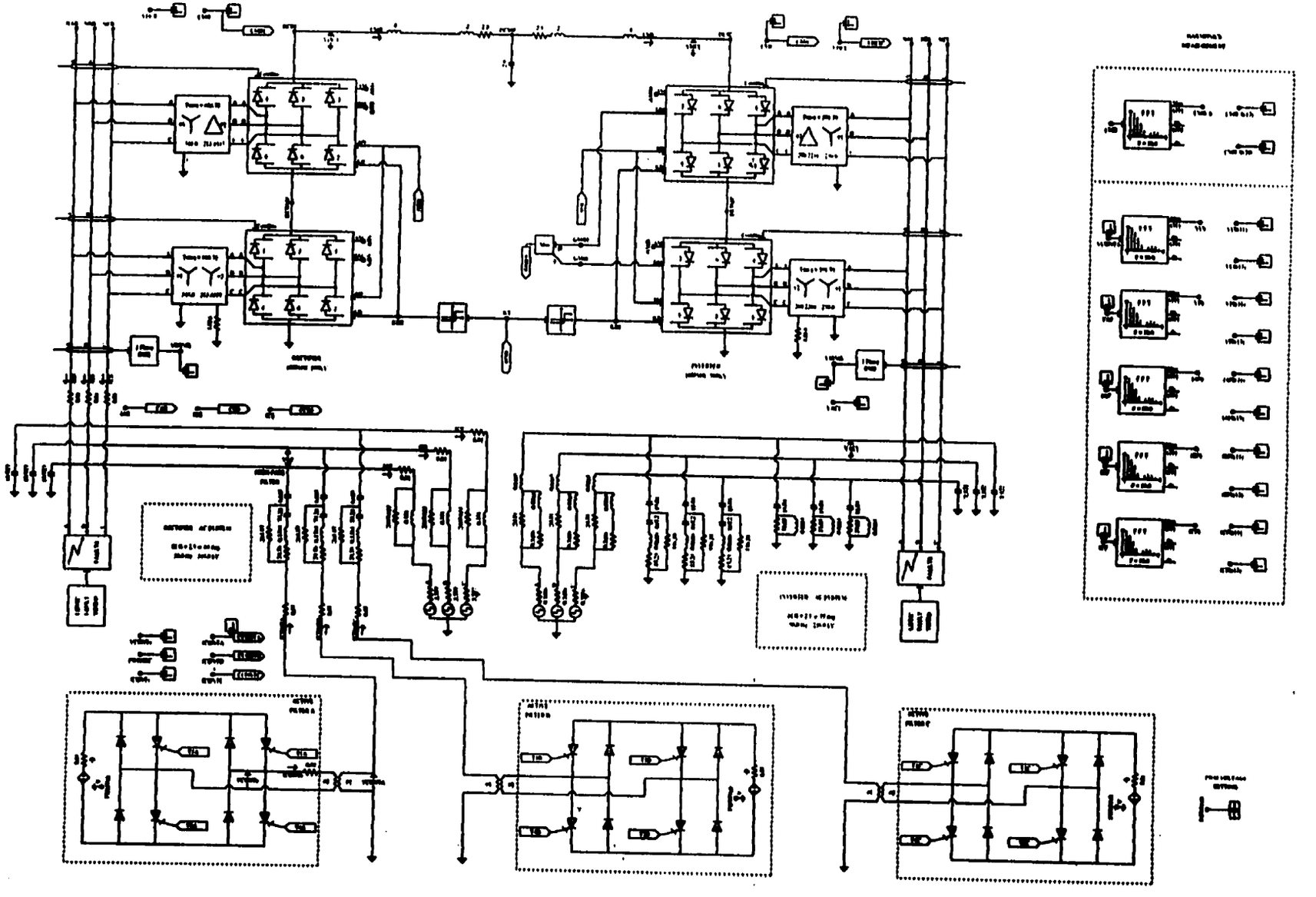

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CIGRE MODEL, 1000MW, 500kV + HYBRID-ACTIVE FILTER

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FILTER CONTROLS

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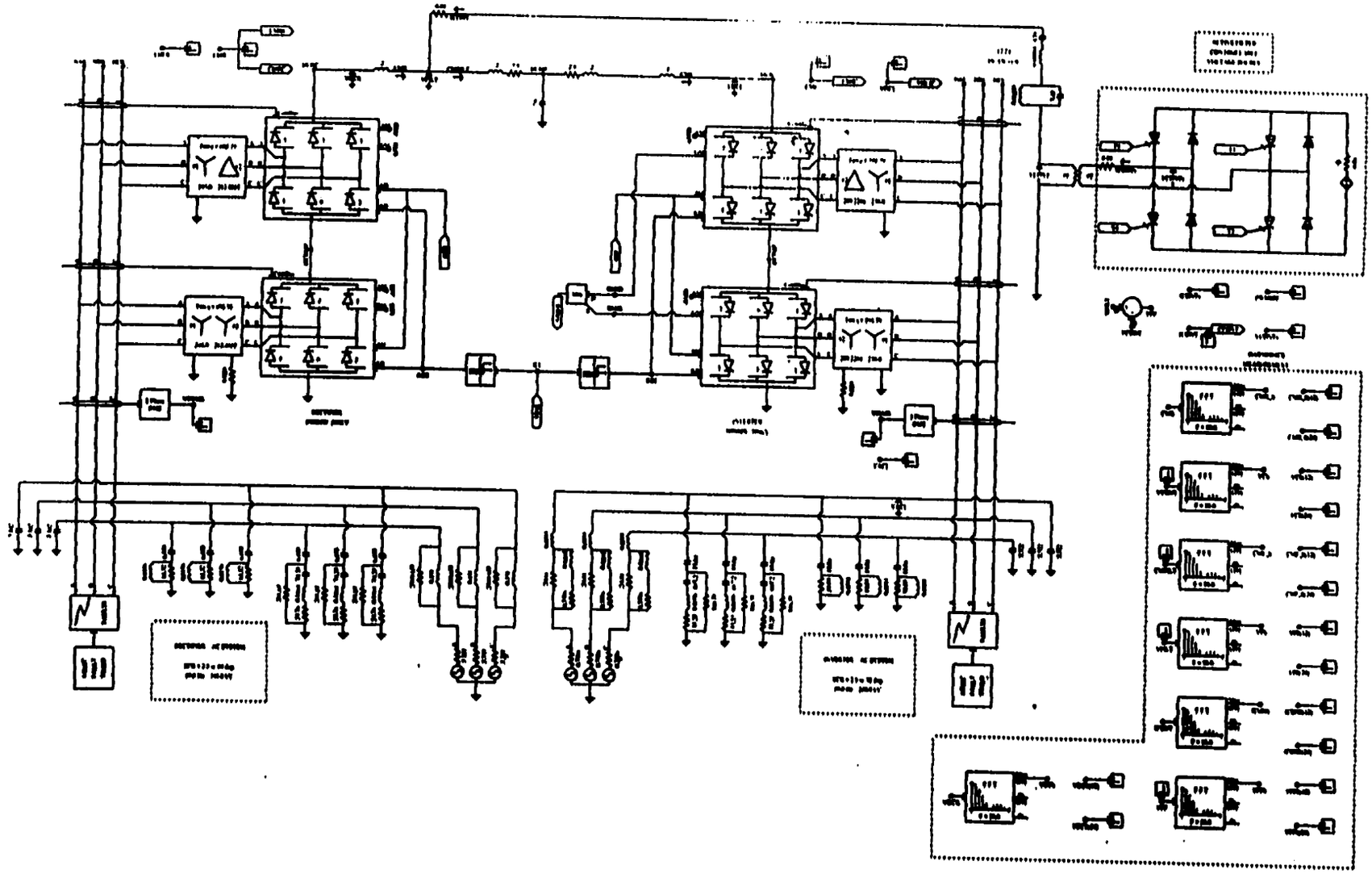

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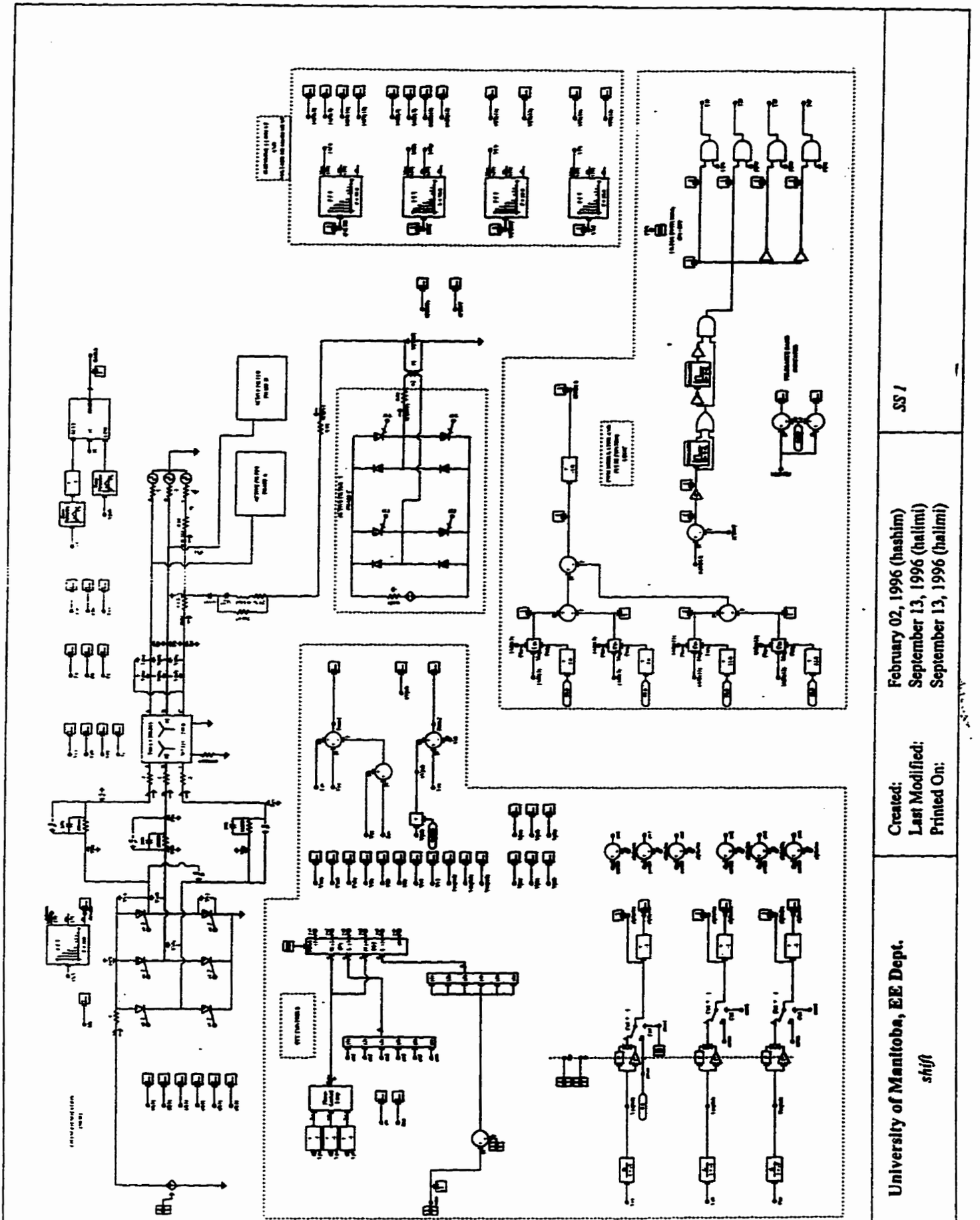

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