DESIGN OF A DIGITAL IMPEDANCE RELAY FOR TRANSMISSION LINE PROTECTION

A Thesis

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Master of Science in Electrical Engineering

by

Jasbir Singh Sandhar

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ABSTRACT

In this thesis it is attempted to design a digital impedance relay for the protection of transmission lines. The design is based on a compact and inexpensive, 8-bit M6800 microprocessor. Major emphasis is laid on a software design for the system. The software design increases the flexibility and reliability of the system. However, this requires a trade-off between hardware and software implementation.

Problems of d.c. offset currents and harmonics due to faults on transmission lines, have been carefully studied. These problems are reduced by an analog band-pass filter tuned to 60 Hz.

Finally, this device has been tested in the laboratory. For the protection of transmission lines, the results obtained are close to the expected ones.

ACKNOWLEDGEMENT

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Finally, the author expresses sincere appreciation to his brother Avtar for his encouragement.

To my Mother

With Deep Gratitude and Affection

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CHAPTER 1

INTRODUCTION

1.1 Relaying

A protective relay is a device which responds to abnormal conditions on an electrical power system to control a circuit breaker so as to isolate the faulty section of the system with the minimum interruption to service [9]. To isolate the faulty section of the system, a relay must decide which circuit breaker should trip. Relays are made responsive to changes that occur in some of the electrical quantities, such as voltage, current, phase angle, frequency, etc., during transition from healthy to faulty conditions.

1.1.1 Distance relays

Based on the nature of measured electrical quantities, relays can be classified into several kinds such as distance relays, over current relays, pilot wire relays, differential relays, etc. Among these, distance relays are the most versatile family of relays and are used primarily for the protection of transmission lines. As their name implies, they measure distance between the fault point on the transmission line and the relay point and respond in accordance with the setting of the relay. Since impedance of the line is almost linearly proportional to its length, distance to the fault can be measured by estimating the impedance of the line (which in turn is calculated from the voltage and current signals at the relay point). Distance relays are classified according to their polar characteristics and the method of comparison made, as impedance relays, admittance relays and reactance relays. Among them,

the impedance relay, which is concerned only with amplitude, has the simplest circular characteristic with center at the origin on an R-X diagram.

It is a mathematical dual of the directional relay which is the simplest of the relays, having a straight line characteristic. No doubt an impedance relay has limitations over longer lines where it is more vulnerable to tripping on power swings [9]. Still, it is stable and gives very good results for medium lines.

1.1.2 Digital relay development

The conventional distance relays are of either electro-mechanical or solid-state electronic construction. Before about 1945, the major emphasis was on mechanical distance relays, but in the late 1940's and early 1950's many scientists and engineers tried to develop electronic relays by using a pentode tube as a comparator triggering a thyratron for tripping purposes [9]. Unfortunately, thermionic relays, because of unreliability, could not be accepted for commerical use. In the 1960's the rapid development of semiconductor technology turned a new page in microcomputer history. Toward the end of that decade many experts in the field of power system relaying began to contemplate the use of digital computers for protection of transmission lines and other apparatus. At that time the benefits of such a computer-based approach were not clear, and few specified ways in which such a system could actually be built and programmed had been considered.

The subsequent introduction and proliferation of minicomputers began an era of plummeting costs of processors suitable for relaying. The computer implementation of protection promised to be less expensive than more conventional approaches [3]. As a result, a number of

investigators published results of work on specific hardware and software techniques for relaying by minicomputer and microcomputers. At present, processor hardware costs have reached still lower levels. Manufacturers and users are looking closely at practical system designs which are likely to appear in commerical service during the next few years.

1.2 Algorithm Classification

A number of algorithms for design and development of computer-based impedance relays have been proposed in numerous papers [1-6]. They can be categorized into three groups:

i) Frequency domain algorithm.

ii) Time domain algorithm.

iii) Phasor domain algorithm.

1.2.1 Frequency domain algorithm

The frequency domain algorithm uses the discrete Fourier transform to form the voltage and current phasors. A data window (defined as the time span covered by the sample set needed to execute the computation procedure) of 1 cycle is used [4]. Algorithms based on a one cycle data window are described to be accurate and provide good harmonic rejection but require a line model to remove the decaying d.c. transient present in fault current. The frequency domain algorithm is well explained and derived in [4].

1.2.2 Time domain algorithm

In the time domain algorithm the transmission line is simulated by a set of first order linear differential equations of the form

$$L \frac{di}{dt} + RI = V$$

This equation is solved for R and L by different approaches such as formation of the integral equation and solving it for R and L over two independent time intervals. Ranjbar and Cory [6] conclude that the accuracy of the digital method under transient fault conditions can be improved if undesirable high frequency components are attenuated by carefully selecting the integration intervals. The same technique was used later by [1] to develop an algorithm to measure impedance.

In earlier work, Mann and Morrison developed an impedance algorithm from instantaneous and differential equations of voltage and current, as follows.

If v, i, v', i' are instantaneous values of voltage and current and their time derivatives respectively, then at any time t,

$$v = V_{PK} \sin \omega t$$

$$i = I_{PK} \sin (\omega t + \phi)$$

$$v' = \omega V_{PK} \cos \omega t$$

$$i' = \omega I_{PK} \cos (\omega t + \phi)$$

$$\therefore \quad |Z| = \frac{V_{PK}}{I_{PK}} = \frac{\sqrt{v^2 + (\frac{v'}{\omega})^2}}{\sqrt{i^2 + (\frac{i'}{\omega})^2}}$$

and phase angle $\phi = \arctan (\frac{\omega i}{i'}) - \arctan (\frac{\omega V}{v'})$.

These equations enable complete impedance determination, as:

$$Z = R + jx = Z (\cos\phi + j \sin\phi).$$

Derivatives of voltage and current can easily be obtained by passing the voltage and current signals through an operational amplifier differentiator.

1.2.3 Phasor domain algorithm

The third category for impedance estimation is the phasor domain algorithm. This algorithm seems to be the simplest and easiest to derive and reasonably accurate. The author has written an algorithm for impedance estimation of transmission lines in the phasor domain. The impedance is calculated by estimating the voltage and current peaks using a peak detector software program on a Motorola 6800 microprocessor. The phase difference between voltage and current waveforms is also determined. Impedance is then calculated by simply dividing the voltage peak by the current peak:

$$Z = |\dot{Z}| = \frac{V_{PK}}{I_{PK}} = \frac{|\dot{V}|}{|\dot{I}|}$$

where $\dot{V}$ and $\dot{I}$ represents the phasors for voltage and current and $\dot{Z}$ is the complex impedance.

The possible existence of an exponentially decaying dc transient and high frequency noise present in the voltage and current signals of a high-voltage system causes some difficulties in real peak detection programs. It is shown in equations (B.1) and (B.2) that after the occurrence of a fault both current and voltage waves contains transient d.c. components. Mann and Morrison explored the possibility of removing d.c. offset in the current signal by using mimic impedance in the current transformer secondary [10]. It was assumed that if an ideal CT is connected to a secondary burden having the same X/R ratio as the primary circuit then the voltage across the burden will be purely sinusoidal as he explained in [10]. However, the author believes that elimination of d.c. offsets in currents can be achieved more accurately if a linear coupler (in place of a current transformer) is used. Warrington explored the possibility of reducing d.c. offsets up to 90% and even more by using

linear couplers.

Since linear couplers act as purely differentiating devices the instantaneous output quantity becomes a voltage given by

$$v_o = M \frac{di_p}{dt} \tag{1.1}$$

where

v_o = secondary output voltage

i_p = primary current

M = coefficient of primary to secondary mutual inductance.

if

$$i_p = I_{PK}[\sin(\omega t + \alpha - \phi) + \sin(\alpha - \phi)\, e^{-t/\tau}] \tag{1.2}$$

where τ = L/R, the time constant of the resulting power system

α = fault inception angle

ϕ = phase angle (power factor angle)

I_{PK} = peak value of current

L and R are, respectively, inductance and resistance of the transmission line. Then

$$v_o = M\, I_{PK}[\omega \cos(\omega t + \alpha - \phi) - \frac{1}{\tau} \sin(\alpha - \phi)\, e^{-t/\tau}] \tag{1.3}$$

Equations (1.2) and (1.3) represent, respectively, the current into the linear coupler and voltage out of the linear coupler. When equations (1.2) and (1.3) are compared, it has been seen that

	into linear coupler	out of linear coupler
coefficient of sinusoidal part	I_{PK}	$M\, I_{PK}\, \omega$
coefficient of exponent part	I_{PK}	$M\, I_{PK}\, \frac{1}{\tau}$

i.e., the ratio of unwanted (exponential) part to the wanted (sinusoidal) part is 1 as the signal enters the linear coupler and $\frac{1}{\tau\omega}$ as the signal leaves the linear coupler. Since $\frac{1}{\tau\omega}$ is typically 0.2

(X/R for the transmission line equals five), the "signal-to-noise ratio" is improved.

One of the disadvantages of using a linear coupler is that besides attenuating d.c. offsets it increases noise (due to harmonic currents) as is evident from equation (1.3). In order to suppress both d.c. current offsets and unnecessary high frequency noise, the author has developed a second order band-pass active filter which is described fully in Chapter 4. This filter is very economical and reliable as it allows only the fundamental frequency component to reach the microcomputer, thus simplifying the problem of possible false peak detection. Another advantage of this filter is that it introduces zero phase delay at the resonant frequency.

CHAPTER 2

MICROPROCESSOR SYSTEM DESCRIPTION

A complete microprocessor system or microcomputer, has principal components similar to those of other computer systems: a central processing unit (CPU), a memory-module, an input-output module and a clock. A block diagram of a basic microprocessor system is drawn in Fig. (2.1).

The main hardware requirements for the implementation of the impedance relay design are:

1. Central Processing Unit
2. Memory
3. Peripheral Interface Adapter (PIA)
4. Analog to Digital Converter
5. Active filters.

Each of the first four of these is described in detail in this chapter but the active filter is given in Chapter 4.

2.1 Central Processing Unit: (CPU)

The major part of a microcomputer is the CPU which itself is composed of an Arithmetic-Logic-Unit (ALU) and Control Unit (CU). The Arithmetic-Logic-Unit performs both arithmetic and logic operations on data and the Control Unit sequences the operation of the entire system. In fact, it operates and manages all control signals necessary to synchronize operations and data flow. One of the essential roles of the Control Unit is to fetch, decode and execute successive instructions stored in memory.

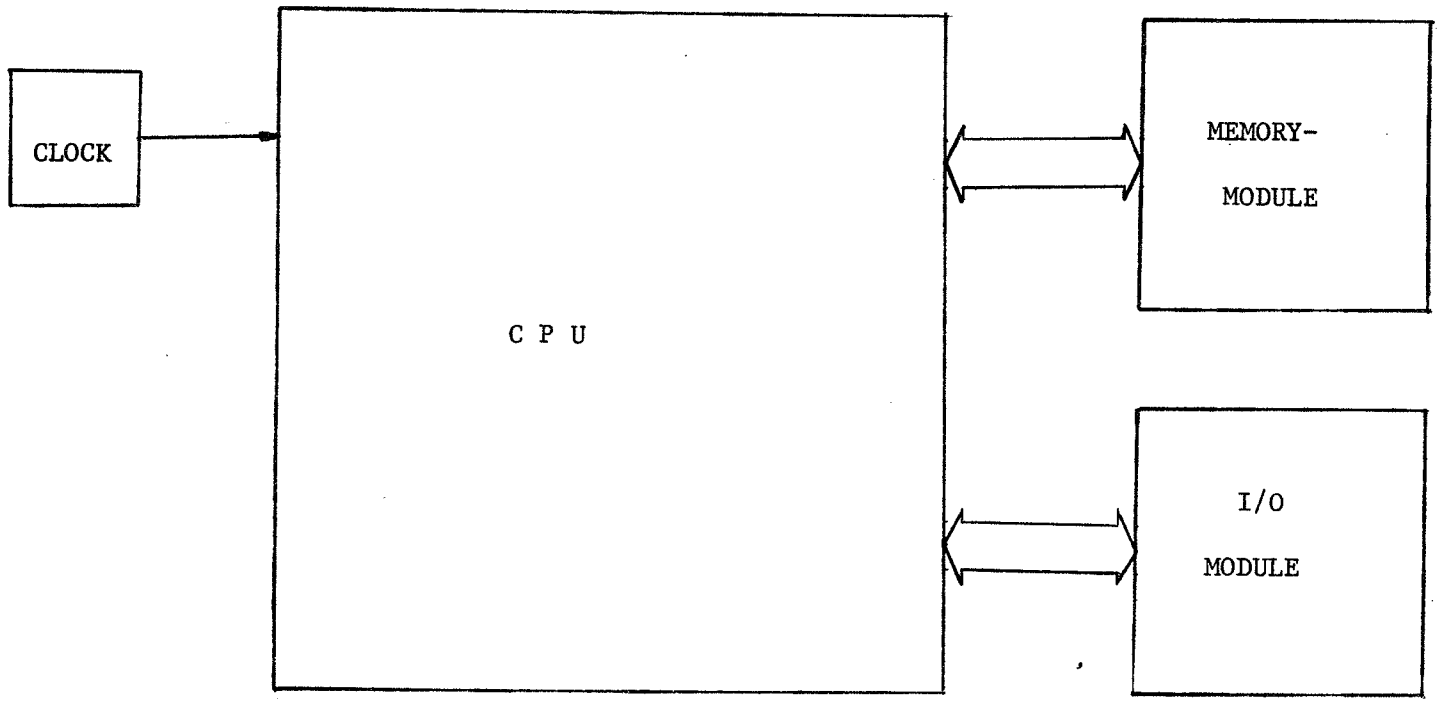


Fig. 2.1 Basic structure of microcomputer system.

The processor unit used in this particular design, a Motorola M 6800, is a bidirectional, bus oriented, 8-bit parallel machine capable of addressing up to 65 K bytes of memory with 16 bits of address. The various registers it contain are:

a) Two 8-bit Accumulators

b) 16-bit Index register

c) 16-bit Stack (Random Access Read-Write Memory)

d) 6-bit Condition Code Register and,

e) Program Counter.

The M 6800 microprocessor requires only a single +5 V power supply. The minimum instruction execution time is 2 microseconds but the one used here takes 2 x 2.4 microseconds.

Processor Control lines include RESET which automatically re-starts the processor, as well as INTERRUPT REQUEST and NON-MASKABLE INTERRUPT to monitor peripheral status. The other control lines are THREE STATE CONTROL DATA BUS ENABLE and HALT which can be used for multi-processing.

2.2 Memory

Computers, as with any other organization, must have some means of retaining information for later reference. Among the many kinds and storage techniques used, semiconductor memories are universally used in microcomputers.

Semiconductor memories can be classified into several kinds depending on whether they are accessible to write information in and then read it out, or only capable of being read from. These two kinds of memory are known as Random Access Memory (RAM) (or Read/Write memory), and Read Only Memory (ROM), respectively. ROMs are non-volatile while RAMs are volatile.

This particular system uses both kinds of memory. Apart from the CPU itself, there is a 1 K ROM for the Monitor and 512 bytes of RAM for the control program and data. The control program resides in the first two pages of the memory map.

2.3 Peripheral Interface Adapter (PIA) [M 6820/21]

Information about the outside world must be gathered and processed. Once processed, the information can be utilized to control various devices and/or display the information. In order to communicate with the peripheral devices interfacing is required.

The Motorola 6800 microprocessor has no input/output instructions but the system uses a memory-mapped input-output scheme. In this scheme the CPU treats input and output ports as simple memory locations. The Motorola 6820/21 Peripheral Interface Adapter (PIA) provides a universal means of interfacing devices to the Motorola 6800 CPU through two 8-bit bi-directional data buses, three chip select lines, two register select lines, two interrupt request lines, a Read/Write line, an Enable line and a Reset line. These signals, in conjunction with the M 6800 VMA output, permit the CPU to have complete control over the PIA. No external logic is used for interfacing too many peripheral devices.

The functional configuration of the PIA is programmed by the microprocessor during system initialization (discussed below). Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface. The structure of the Motorola 6820/21 PIA chip is shown in the block diagram of Fig. 2.3.

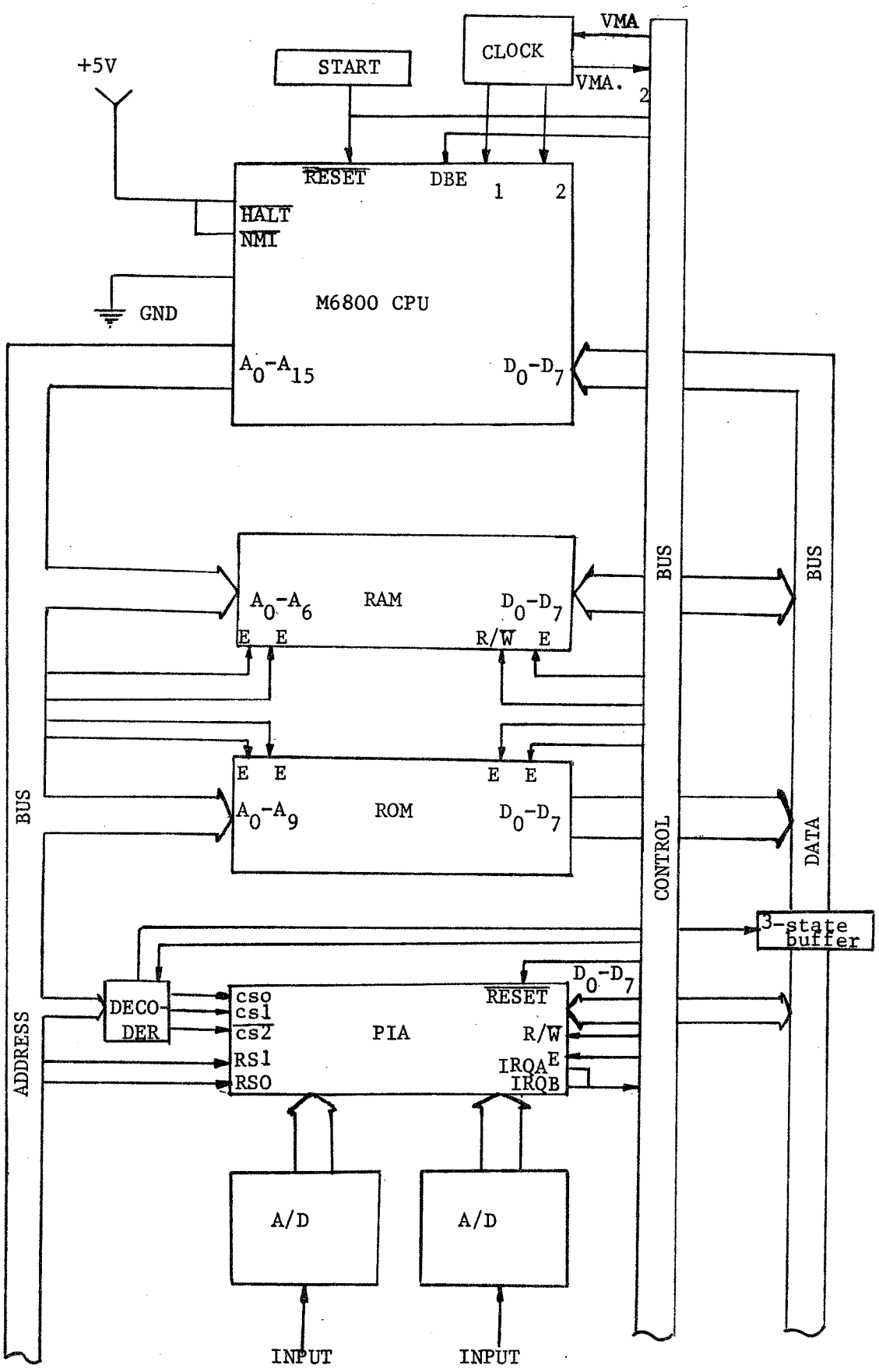


Fig. 2.2 Structure of the microprocessor system.

In order to minimize noise interference, control lines are connected to high state inputs through 1 KΩ resistors. The control lines are mainly for hand-shaking purposes and are not used in this particular project. Reset and Read/Write lines are connected to the CPU to help transfer of data from CPU to PIA and vice-versa, depending upon the state of the R/$\bar{W}$ line. The Enable ($\bar{E}$) signal is driven by the phase-two clock of the system directly. The two interrupt request lines are tied together and connected to $\overline{IRQ}$ of the CPU.

Since the available 65 K memory locations of our microprocessor system are not fully utilized, a partial address decoding scheme for the PIA is used as shown in the block diagram of Fig. 2.4.

2.3.1. PIA initialization

There are six registers within the PIA accessible to the CPU data bus: two peripheral (output) registers, two data direction registers and two control registers; but they occupy only four memory locations. Three different registers are assigned to each of the two channels (I/O Ports) of the PIA. The output register is a temporary data storage location and can be used as an input or an output register. The Data Direction Register controls the buffer between the output register and the Peripheral Data Bus (PDB). Each of the bits in the Data Direction Register can be set to zero or 1 enabling the PDB line to act as input or output, respectively. Since the Data Direction Register and the Output Register share the same address (Fig. 2.5), bit 3 of the corresponding Control Register acts as a pointer bit and selects Output Register or the Data Direction Register, depending on the state of bit 3.

The particular partial decoding scheme used in this project assigns addresses 8000 and 8001 to Port A while 8002 and 8003 are assigned

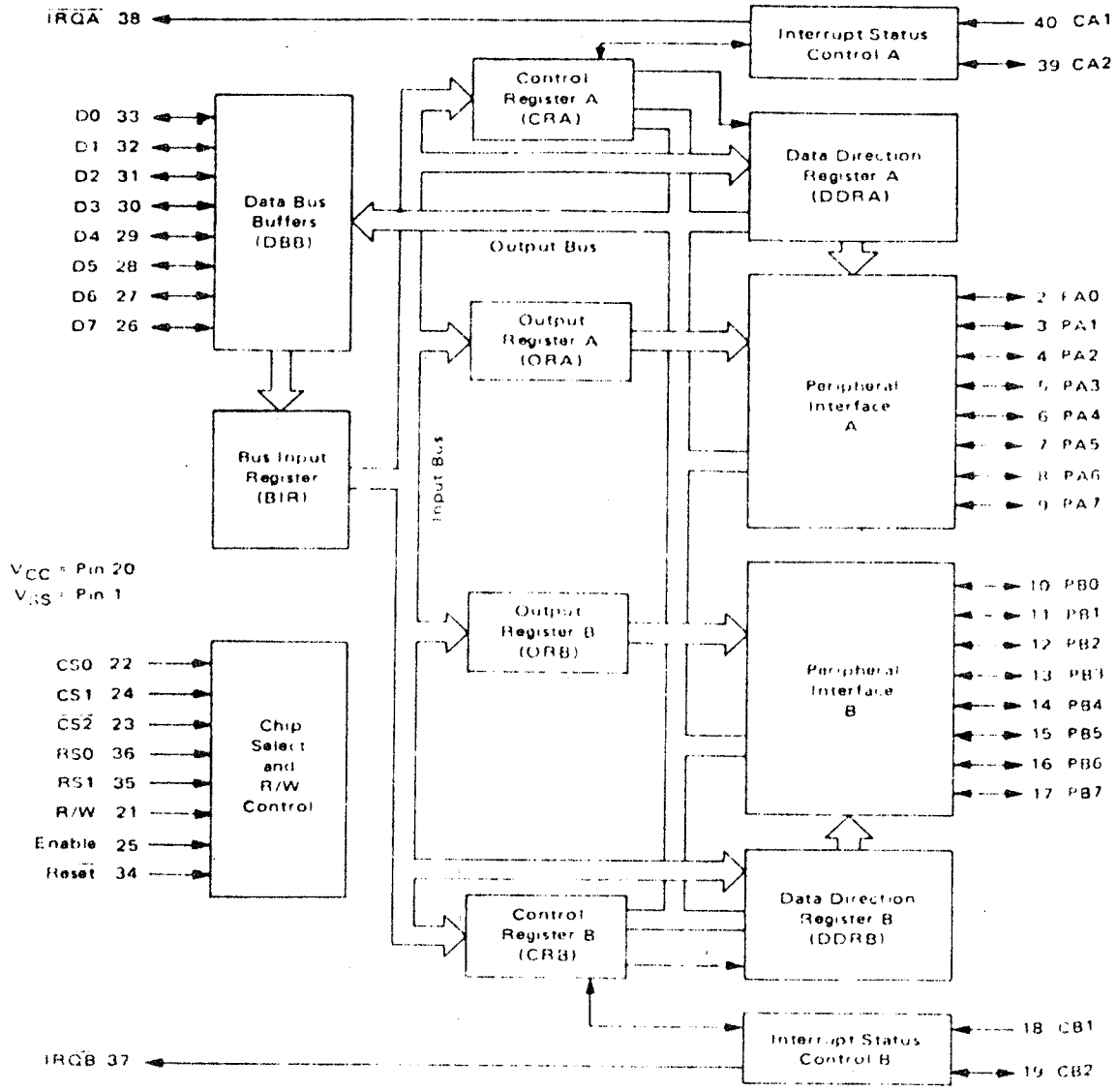


Fig. 2.4 Motorola 6820/21 PIA block diagram.

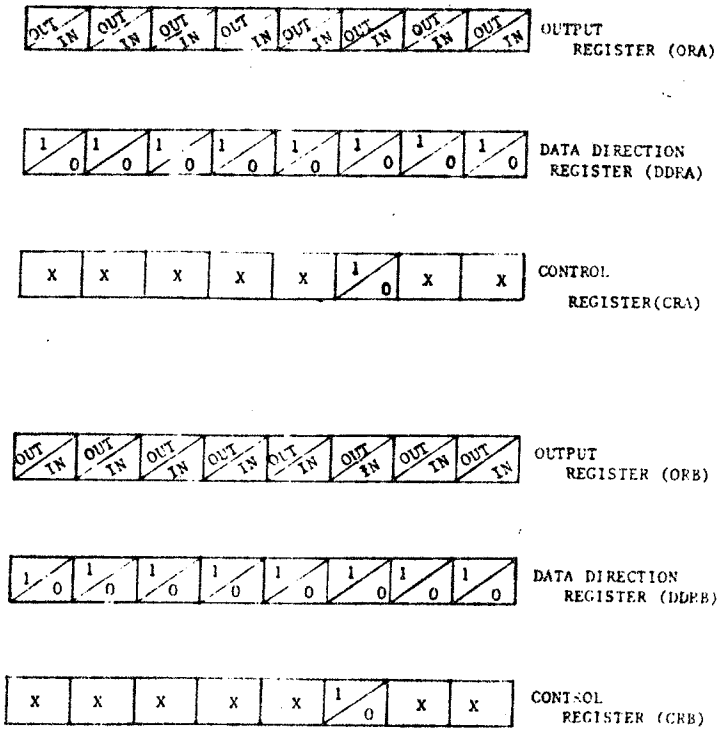


Fig. 2.5: PIA dual Registers

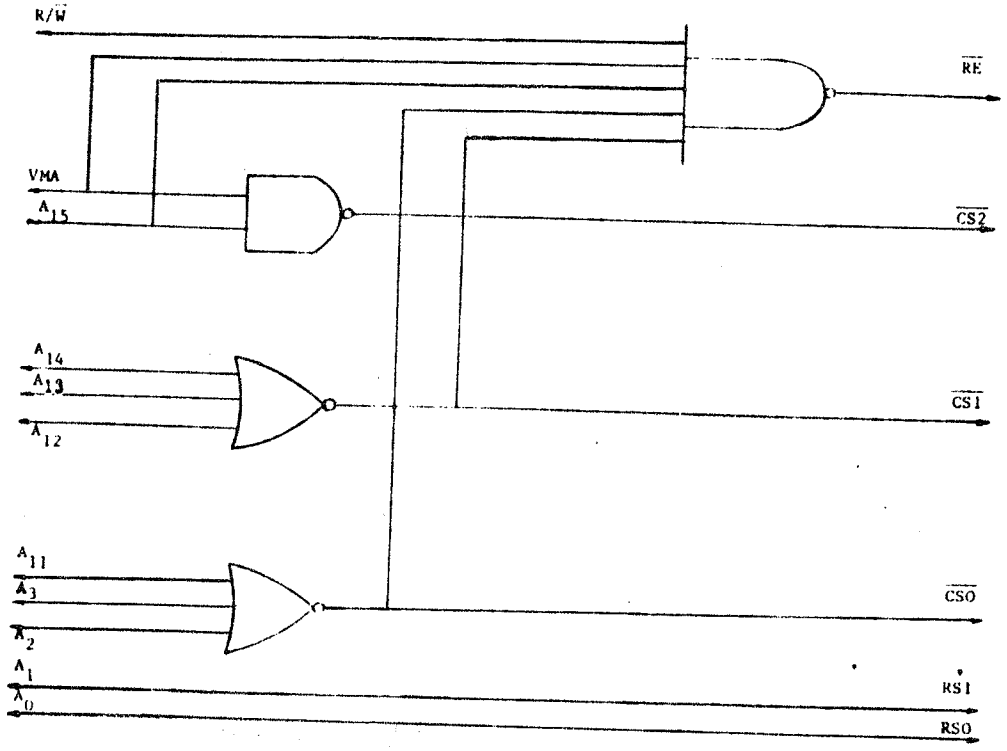


Fig. 2.4: Address decoder for M6821 PIA

to Port B. Once the system is reset, all the registers of the PIA get cleared thus simplifying the initialization procedure of the PIA.

The following program demonstrates the simplicity of the PIA initialization.

```
***   PIA Initialization
      LDX   #$0004
      STX   $ 8000
      STX   $ 8002
```

(a)

X	X	X	X	X	X	X	X
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0

X	X	X	X	X	X	X	X
0	0	0	0	0	0	0	0
0	0	0	0	0	1	0	0

(b)

Fig. 2.6 (a) PIA initialization Program
(b) Input-Input port configuration

x - any data

Once the PIA is initialized, it starts receiving data from, or sending data to, the microprocessor system as well as the outside world. The above program enables both ports of the PIA to receive data from the converter, *i.e.*, to act as input ports.

2.4 Analog to Digital Converter (A/D)

Communicating between the analog and digital worlds requires devices that can translate the language of the two worlds. The analog to digital (A/D) converter translates the language of the analog world into the language of the digital world. The analog signal is presented to the input of the A/D converter and after a finite amount of conversion time the digital output is available for use by the digital computer.

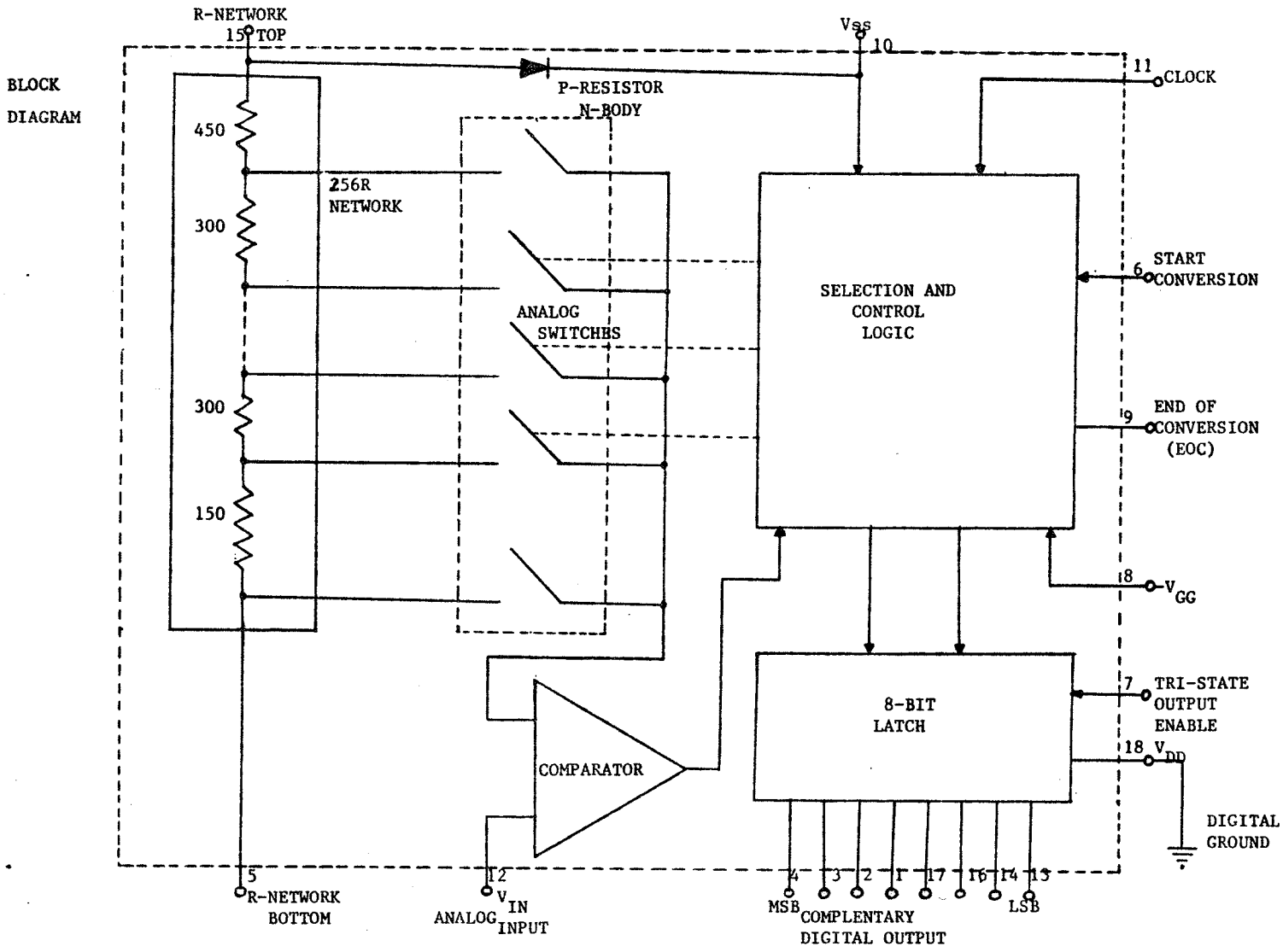


Fig. 2.7 Internal structure of A/D Converter.

Key characteristics of A/D converter include absolute and relative accuracy, linearity, resolution, conversion speed, stability and price.

In this project, the ADC 0800 (MM 5357B), an 8-bit A/D converter, is used. The internal construction of this converter is shown in Fig. 2.7. It contains a high input impedance comparator, 256 series resistors and analog switches, control logic and output latches. Conversion is performed using a successive approximation technique where the unknown voltage is compared to the resistor tie points using analog switches. When the appropriate tie point voltage matches the unknown voltage, conversion is complete and the digital output contains an 8-bit complementary binary word corresponding to the unknown. Conversion requires 40 clock periods and the data transfer occurs in about 200 ns so that valid data is present, virtually all of the time. The device is operated in the free-running mode by connecting the Start Conversion line to the End of Conversion line.

The reference applied across the 256 resistor network determines the analog input range. For maximum accuracy it is desirable to operate with at least 10 V range. With the top of the R-network connected to 5 V and the bottom connected to -5 V a ±5 V range is used. The A/D converters use a specific data representation called "complementary offset binary code" to represent the digital quantities. This code can be represented as having a linear relationship with the analog voltage levels as is shown graphically in Fig. 2.8.

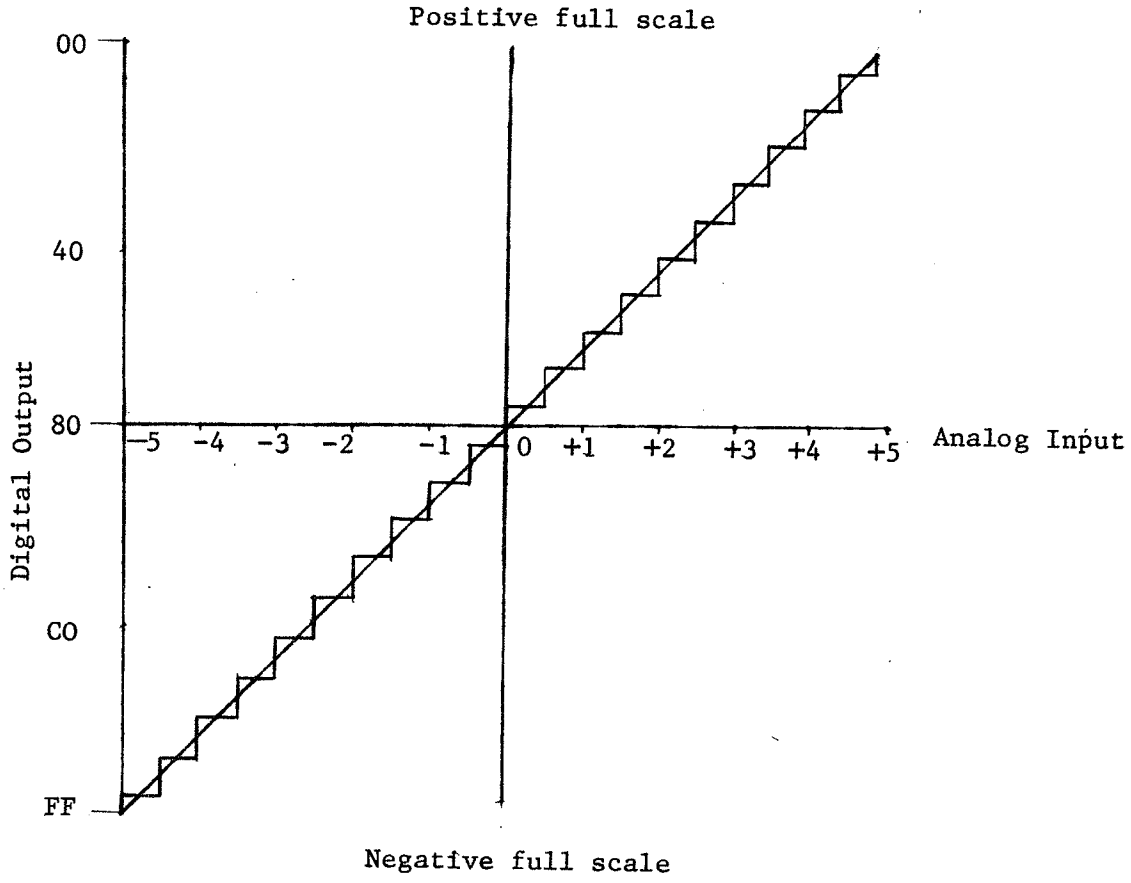


Fig. 2.8 Ideal Conversion relationship in an 8-bit A/D converter.

CHAPTER 3

RELAY SYSTEM DESIGN

3.1 Fundamental Operating Principle

Transmission line fault detection is achieved by detecting the change in system impedance by constantly observing voltage and current magnitudes along with their phase angle. Voltage and current magnitude changes can easily be detected by observing their peak values which, for particular conditions, remain constant, and the phase angle from the time difference between the occurrence of voltage and current peaks.

If V_{PK} represents the peak value of voltage

I_{PK} represents the peak value of current

then $|\dot{Z}|$ the complex impedance magnitude is given by

$$Z = |\dot{Z}| = \frac{V_{PK}}{I_{PK}} \tag{3.1}$$

if α represents the fault inception angle,

ϕ the phase difference between voltage and current waveforms,

$\dot{V}$ the phasor voltage at fault occurrence

and $\dot{I}$ the phasor current at the same instant

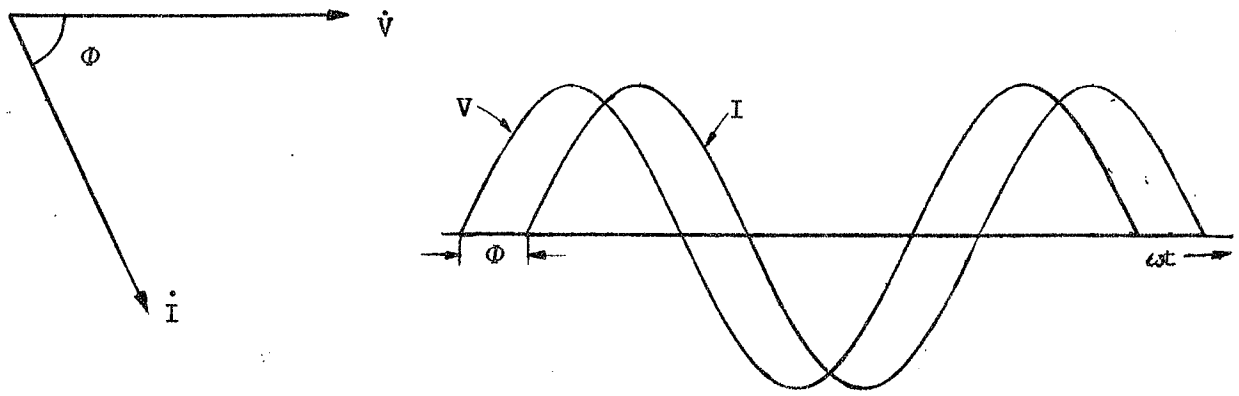
then $$\dot{V} = V_{PK} \angle \theta_V \tag{3.2}$$

$$\dot{I} = I_{PK} \angle \theta_i \tag{3.3}$$

where $$\theta_V = 90 - \alpha \tag{3.2a}$$

$$\theta_i = 90 - \alpha \pm \phi \tag{3.3a}$$

The phasor and instantaneous values of voltage and current, at the instant of fault occurrence, are shown in Fig. 3.1(a) and (b), respectively.



(a) (b)

Fig. 3.1

In equation (3.3a) a positive sign indicates the current leading the voltage, while a negative sign indicates current lagging the voltage. The complex impedance is given by

$$\dot{Z} = \frac{\dot{V}}{\dot{I}} = \frac{V_{PK} \angle 90 - \alpha}{I_{PK} \angle (90 - \alpha \pm \phi)}$$

or $$\dot{Z} = |\dot{Z}| \angle \mp \phi \qquad (3.4)$$

if expressed in R and X components the complex impedance

$$\dot{Z} = |\dot{Z}| (\cos\phi \mp j \sin\phi)$$

or $$\dot{Z} = R \mp jX \qquad (3.5)$$

where $$R = |\dot{Z}| \cos\phi \qquad (3.6a)$$

$$X = |\dot{Z}| \sin\phi \qquad (3.6b)$$

magnitude $$Z = |\dot{Z}| = \sqrt{R^2 + X^2} = \frac{V_{PK}}{I_{PK}} \qquad (3.7a)$$

and $$\phi = \tan^{-1}\left(\frac{X}{R}\right) \qquad (3.7b)$$

Equation 3.7(a) gives circular characteristics of the complex impedance with radius Z on R-X plane which is shown in Fig. 3.2.

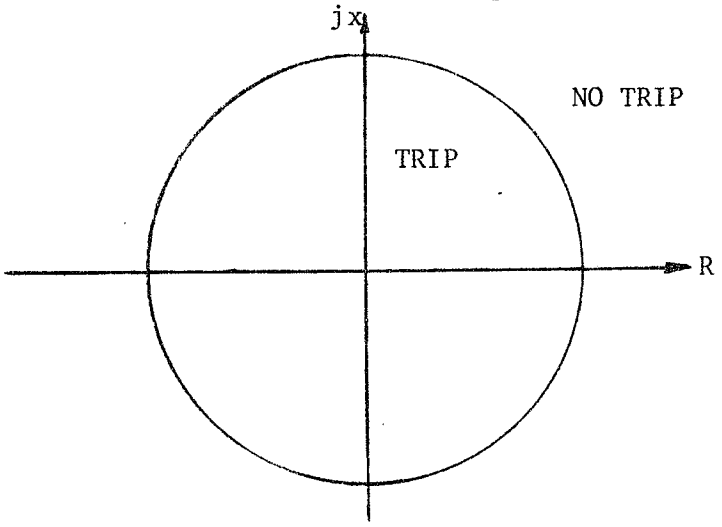


Fig. 3.2 Characteristics of Impedance Relay

3.2 Signal Conditioning

Signals of voltage and current from the transmission line are derived from a step down potential transformer and a current transformer, respectively. Because of the complexity of the converter operation the current signal is changed into current proportional voltage by passing it through an appropriate valued resistor: Fig. 3.3.

It has been shown that the fault on the line results in addition to the fundamental components of voltage and current, a d.c. offset and other high harmonics which cause distortion in the original sinusoid. The algorithm developed on the basis of equation (3.7) simply detects the maximum value of the sinusoidal waveforms which, in the presence of harmonics, could easily be feigned before the real maxima occur. To avoid this abnormality, it becomes necessary to, somehow, remove the unwanted d.c. offset and noise and let only the 60 Hz component reach the microcomputer. Many methods have been suggested in a number of papers [1-6], *e.g.*, using a combination of lowpass and digital filters, using digital

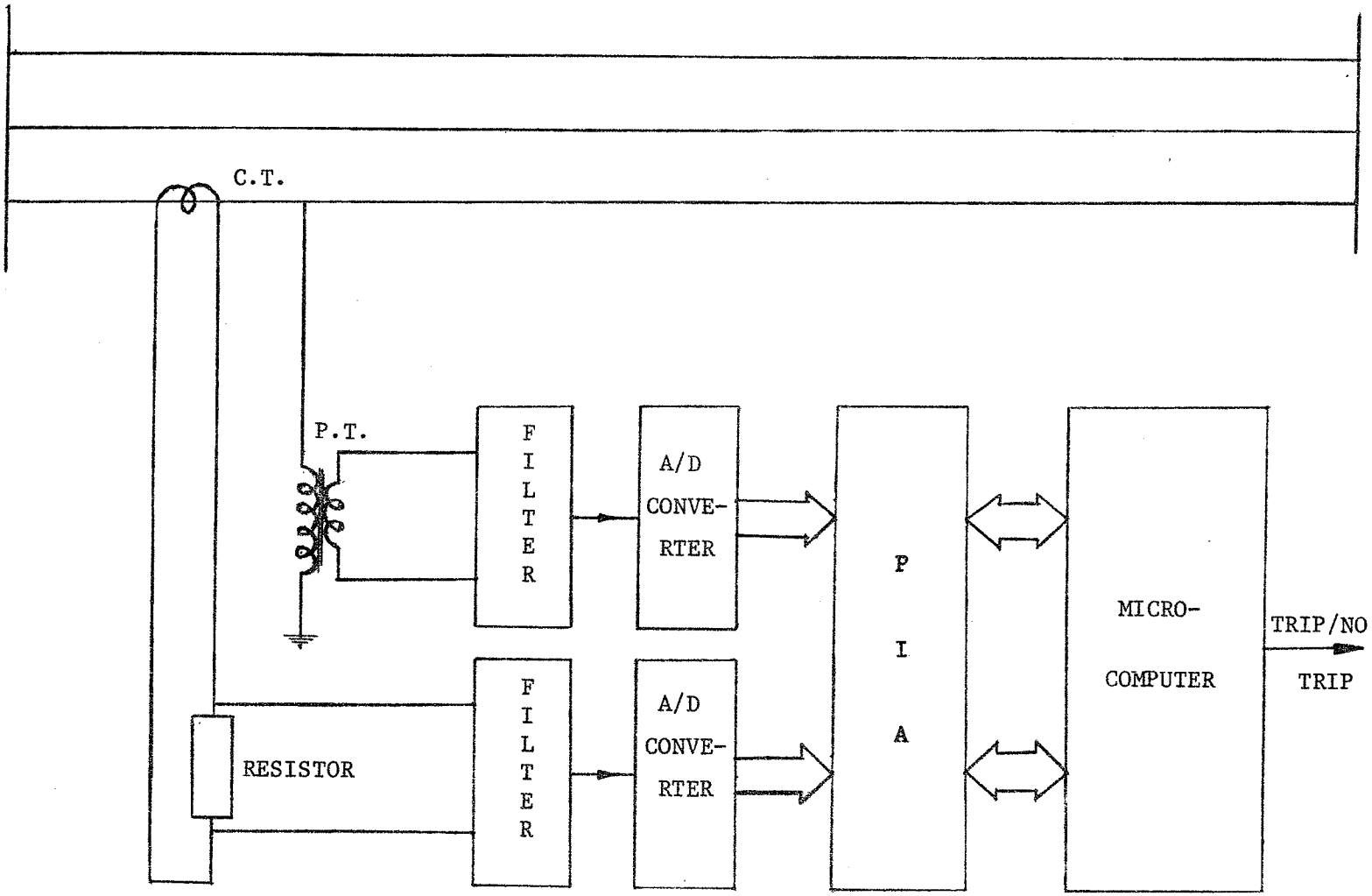


Fig.3.3 Block diagram of the Digital Impedance Relaying System

filters only, etc. The author suggests using an analog band-pass (2nd. order) active filter tuned at 60 Hz frequency. This filter described in a later chapter, successfully removes or attenuates d.c. and noise to an extent that is acceptable to the algorithm used.

The analog conditioned signal is then fed to the analog to digital converter which converts it into an 8-bit (255_{10}) discrete resolution. The microcomputer, thus detects peak values of voltage, and current proportional to voltage, and finally computes impedance of the faulted line. If the fault is detected within the protected zone the computer sends a trip signal to the appropriate circuit breaker. Otherwise it continues to compute the line impedance until some abnormal condition appears on the line. The system that detects the fault, and then generates a trip signal is shown in Fig. 3.3.

3.3 Flow Chart

The flow chart of the algorithm based on equation (3.6) is given in Fig. 3.5. The various steps taken in developing this program are discussed briefly.

3.3.1 PIA initialization

The PIA is initialized by a simple program given in Fig. 2.6, repeated here:

```
LDX    0004
STX    PORT A
STX    PORT B
```

This simple program initializes both ports as input ports, *i.e.*, it accepts digitized signals from both converters. To the microcomputer, the PIA Ports are simple memory locations from where data can be read at

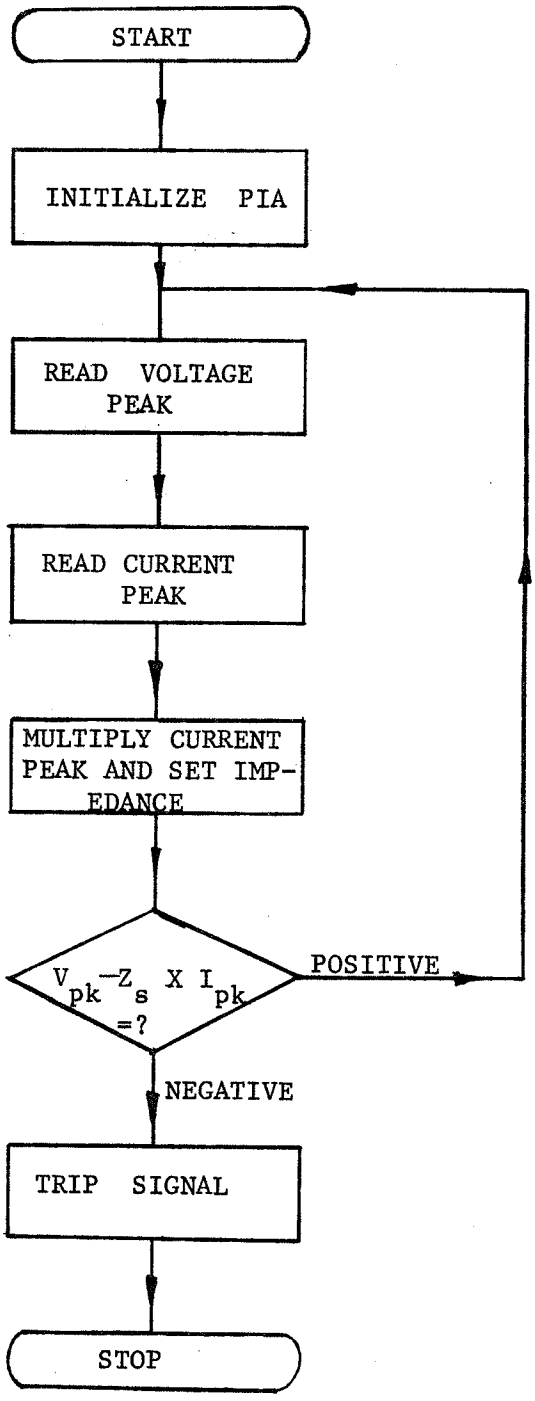


Fig.3.5 Fault Detection Flow Chart.

any time. Once the PIA is initialized it accepts data from the converter continuously.

3.3.2 Peak detection

According to the Sampling Theorem, in order to represent the input signal correctly and also to avoid aliasing problem, the sampling rate must be at least twice as fast as the fastest occuring signal (or maximum harmonic frequency) in the system. Since we are blocking all higher frequency noise and low frequency and d.c. offsets with band-pass filter and there may exist harmonics not for above the 60 Hz signal, a sampling frequency of at least 180 Hz should be used. However, to get results as accurate as possible, a sampling frequency of 4320 Hz was used thus giving a resolution of 5° (electrical). The data is then processed in the microcomputer. This process, after PIA initialization, remains operative until the maximum value sample has been detected. This value is saved for impedance calculations. The flow chart to detect peak value is shown in Fig. 3.7. This program has one advantage in that it detects a positive or negative peak, whichever occurs first, and then starts computation. The waveform resolution period is controlled by a 'Delay' program flow chart given in Fig. 3.6.

3.3.3 Multiplication and division modifications

The Motorola 6800 microprocessor instruction set has no provision for ordering multiplication and division operation. A program of simple multiplication by repeated addition of two numbers up to a maximum value of $FF_{16} = 256_{10}$, because of physical limitations of the 8-bit processor, would give results to a maximum value of FF_{16} and if carry bit is included the product result would reach the maximum value $1\,FF_{16}$ or

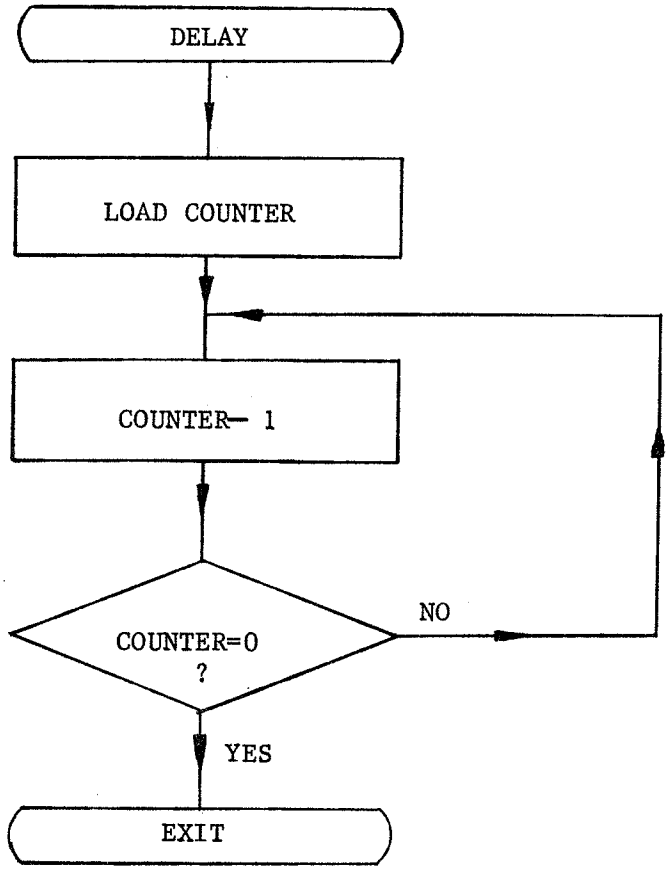
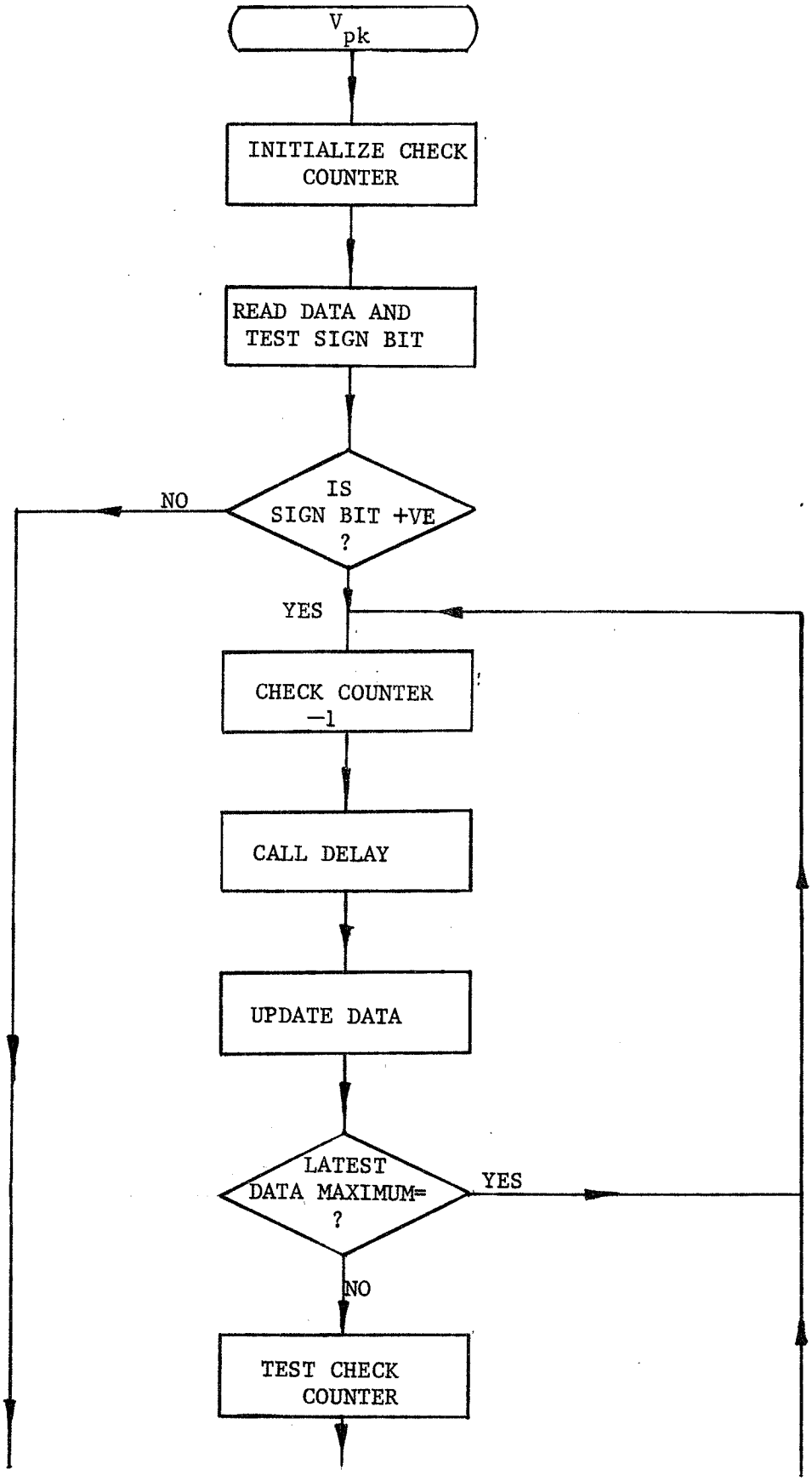


Fig. 3.6 Delay Sub-routine Flow Chart.


V_{pk}
INITIALIZE CHECK COUNTER
READ DATA AND TEST SIGN BIT
IS SIGN BIT +VE ?
NO
YES
CHECK COUNTER −1
CALL DELAY
UPDATE DATA
LATEST DATA MAXIMUM= ?
YES
NO
TEST CHECK COUNTER

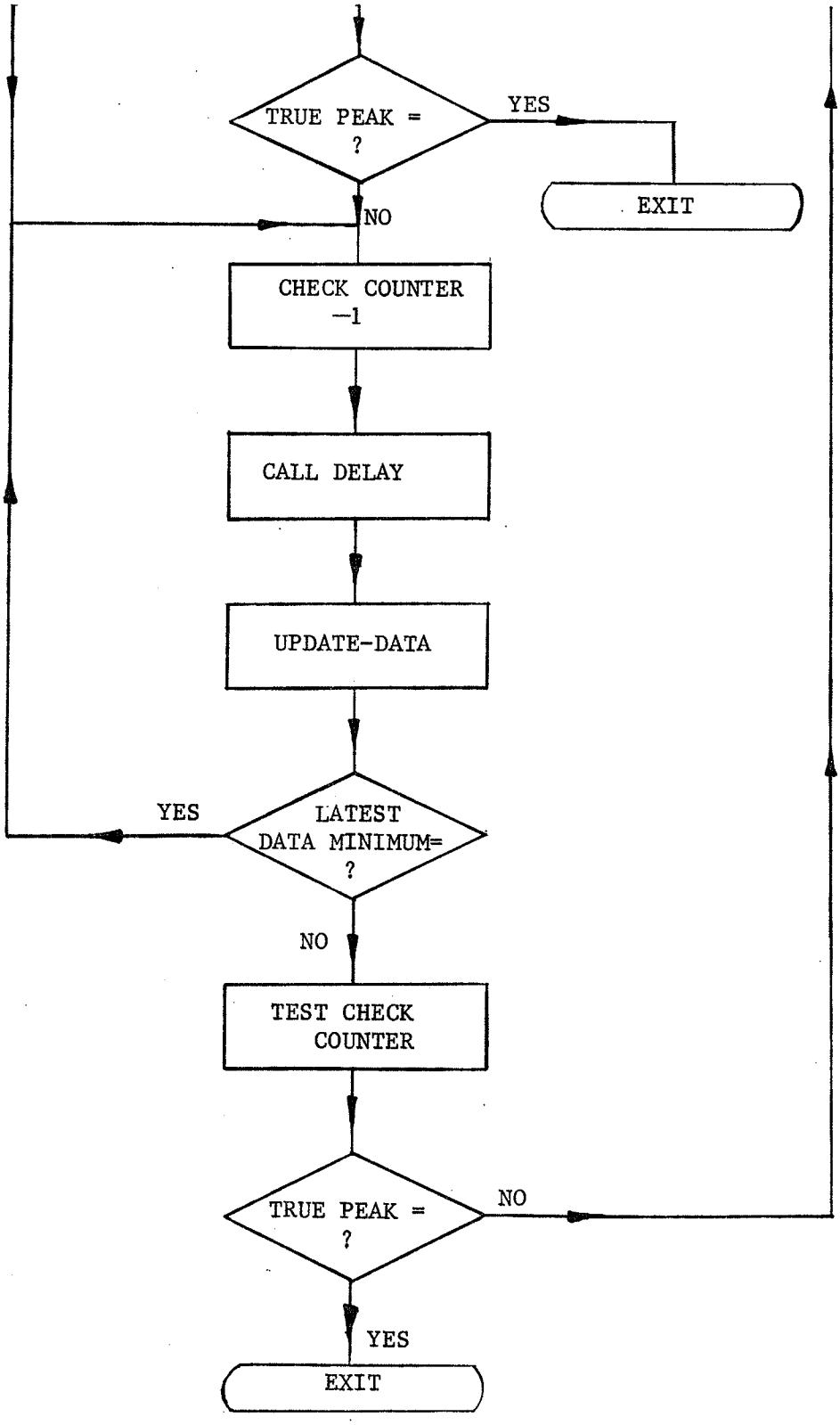


Fig.3.7 Voltage/Current Peak detection program Flow Chart.

512_{10}. In order to get a larger product, multiple precision is used. This can produce results of any desired magnitude. For example, double precision can produce a number 130591_{10} when a carry bit is included and 65295_{10} when a carry bit is excluded. A flow chart for a double precision multiplication program is given in Fig. 3.8.

Similarly single precision division by repeated subtraction of two numbers produces a whole number quotient which when modified to multiple precision yields a quotient of any fractional part of a number. This helps in evaluating the line impedance to be protected against the selected impedance of any fractional number.

This program is written in machine language for the Motorola 6800 microprocessor and finally converted into machine codes. Both are given in Appendix A.

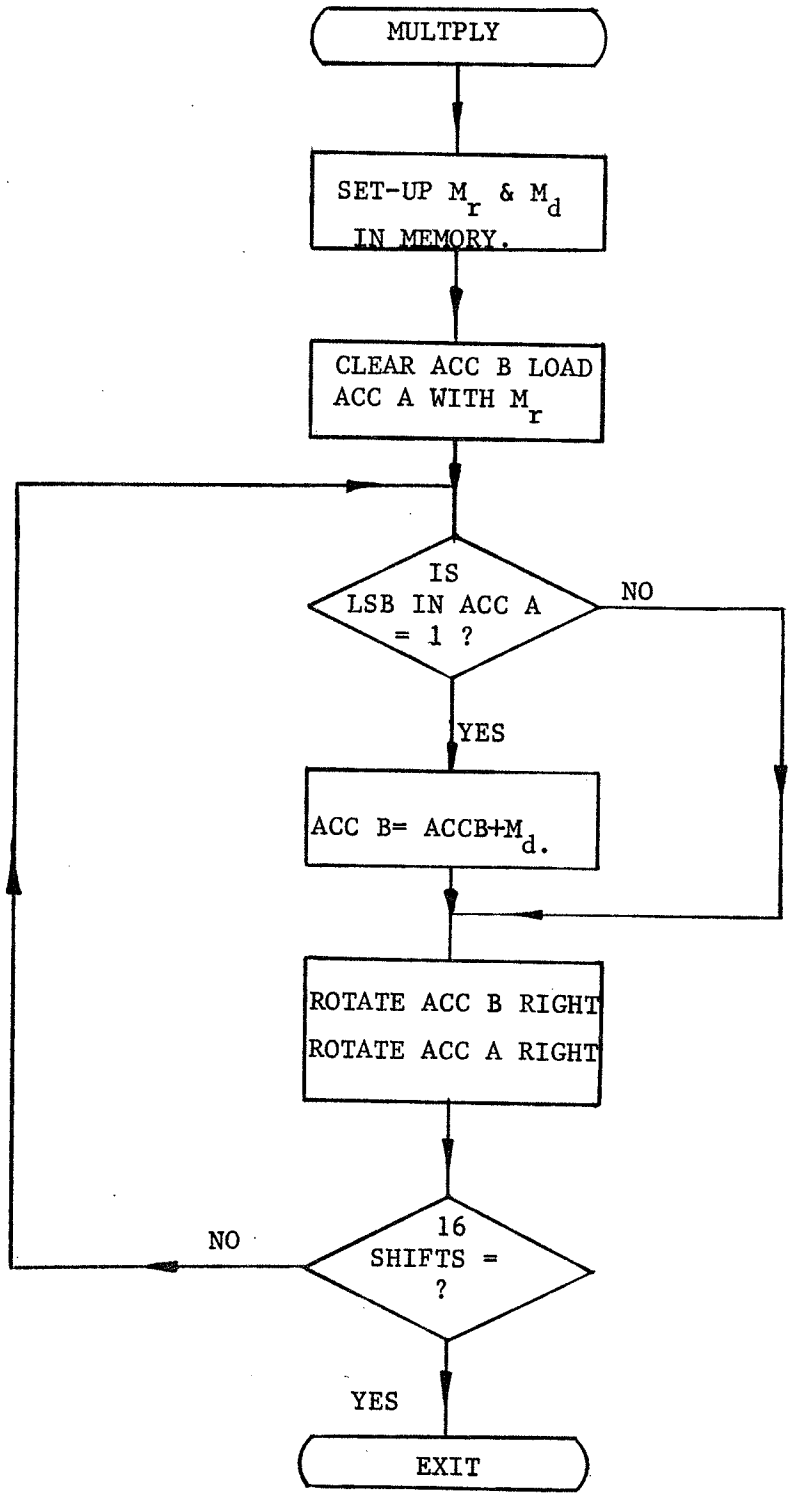


Fig.3.8 Multiplication of Two Numbers (Double-precision) Flow Chart.

CHAPTER 4

FILTERING

4.1 Reason for Filtering

A fault on a transmission line distorts current and voltage waveshapes because of resonances and travelling waves [11]. Distorted waves on analysis would yield in addition to fundamental, several other frequency components best known by the term "noise" (or "harmonics"). Digital relays are found to be very sensitive to noise because of the absence of magnetic and mechanical time constants. Typical distortion of waveshapes due to noise and d.c. offsets is shown in Fig. 4.1. Also in Appendix B, it has been proven mathematically that a fault introduce a d.c. offset, if the fault occurs at other than voltage peak.

Since the peak finding algorithm used to estimate impedance of the transmission line always compares two consecutive samples of current (or voltage) waveshapes, the presence of d.c. offset and noise, could easily cause a false peak determination. In these circumstances, it is necessary to remove these unwanted higher harmonics and d.c. components. The best way of attenuating them is by analog or digital filtering.

4.2 Choice of a Filter

Of the two types of filtering, analog filtering is selected in this design. The reasons for choosing an analog filter is that

(a) it does not increase the computational burden on the microcomputer,

(b) it uses operational amplifiers which are inexpensive and are easy to use, and

(c) it does not introduce quantization errors as would a digital filter.

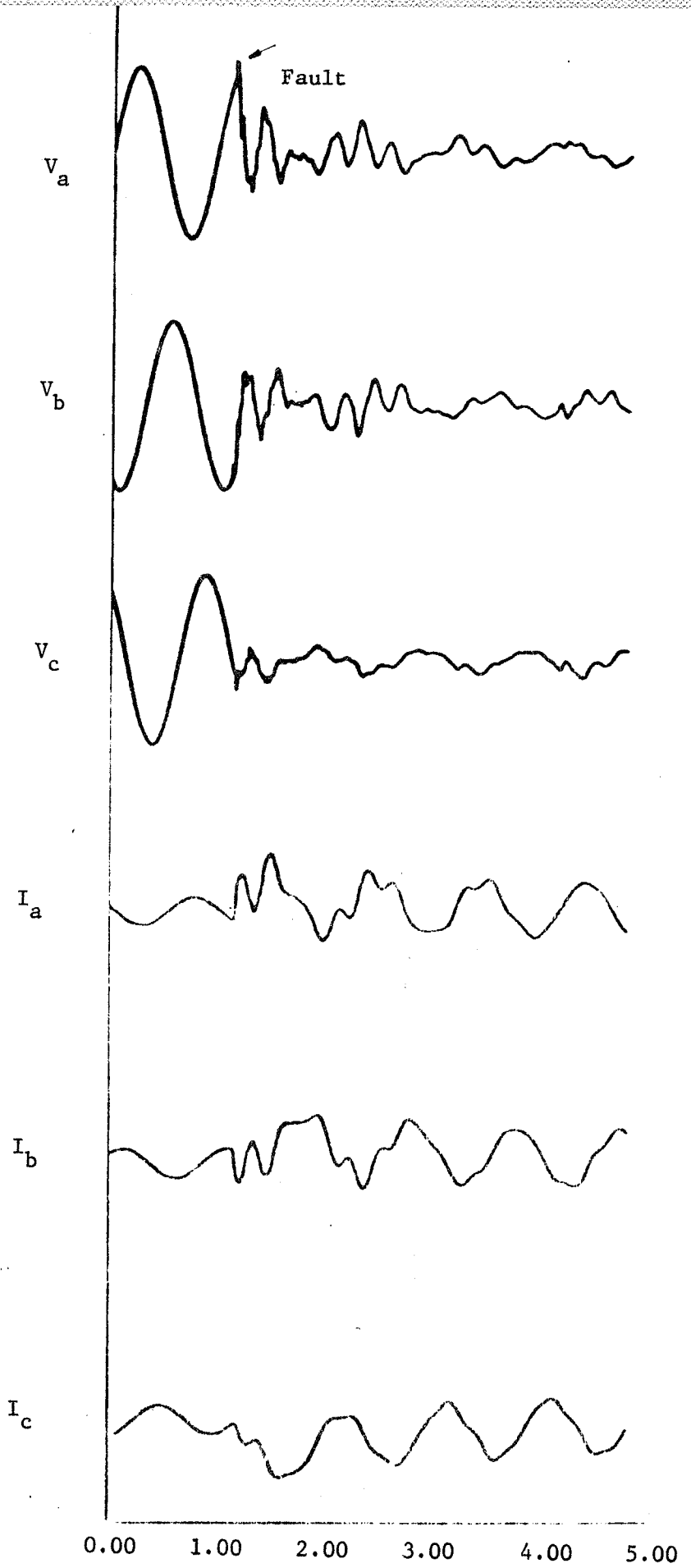


Fig. 4.1 Sample Fault simulation (three phase).

Active filters have some characteristics of their own that make them different from passive filters. For example, active filters usually have single ended inputs and outputs and thus do not float with respect to the system power supply or common as a passive RLC network can. Active filters can provide excellent isolation capabilities, that is, high input impedance and low output impedance. The integrated circuit op-amp proves to be an extremely useful active device in the realization of active RC network.

4.3 Filter Design

The filter network functions of interest are magnitude, phase and time delay. The network parameters are the characteristic frequency, storage or quality factor Q and passband gain. These functions and parameters for a complex-pole-pair bandpass network are as described below.

The complex-conjugate-pole-pair bandpass transfer function is:

$$H(s) = \frac{G\,\alpha\omega_0\, s}{s^2 + \alpha\omega_0 s + \omega_0^2} \tag{4.8}$$

where $\alpha = \frac{1}{Q}$

and $$Q = \frac{\omega_0}{\omega_U - \omega_L} = \frac{f_0}{f_U - f_L} \tag{4.9}$$

The parameters f_U and f_L are the upper and lower cut-off frequencies and f_0 is the center frequency where the band-pass gain is G. The sinusoidal steady-state transfer function may be written in the form

$$H(j\omega) = \frac{G}{1 + jQ(\omega/\omega_0 - \omega_0/\omega)} \tag{4.10}$$

and the magnitude, phase and delay functions are

$$G(\omega) = \left[\frac{G^2}{1 + Q^2(\omega/\omega_0 - \omega_0/\omega)^2}\right]^{1/2} \tag{4.11a}$$

$$= \left[\frac{G^2\alpha^2\omega_0^2\omega^2}{\omega^4 + \omega^2\,\omega_0^2(\alpha^2 - 2) + \omega_0^4}\right]^{1/2} \tag{4.11b}$$

$$\phi(\omega) = \frac{\pi}{2} - \arctan\left(\frac{2Q\omega}{\omega_0} + \sqrt{4Q^2 - 1}\right) - \arctan\left(2Q\,\frac{\omega}{\omega_0} - \sqrt{4Q^2 - 1}\right) \tag{4.12}$$

$$\tau(\omega) = \frac{2\,Q\cos^2\phi}{\omega_0} + \frac{\sin 2\phi}{2} \tag{4.13}$$

In order to realize the second-order filter functions and parameters, consider a general circuit of one operational amplifier, resistors and capacitors. Figure 4.2(a) illustrates the multiple-feedback connection for a pair of complex-conjugate S-plane poles with zeros restricted to the origin or infinity. Each element Y_i represents a single resistor or capacitor.

To derive the transfer function, let us write the node equations at the intermediate point 'a' and the inverting input node:

$$(Y_1 + Y_2 + Y_3 + Y_4)\,V_a - Y_1\,V_1 - Y_4\,V_2 = 0 \tag{4.14}$$

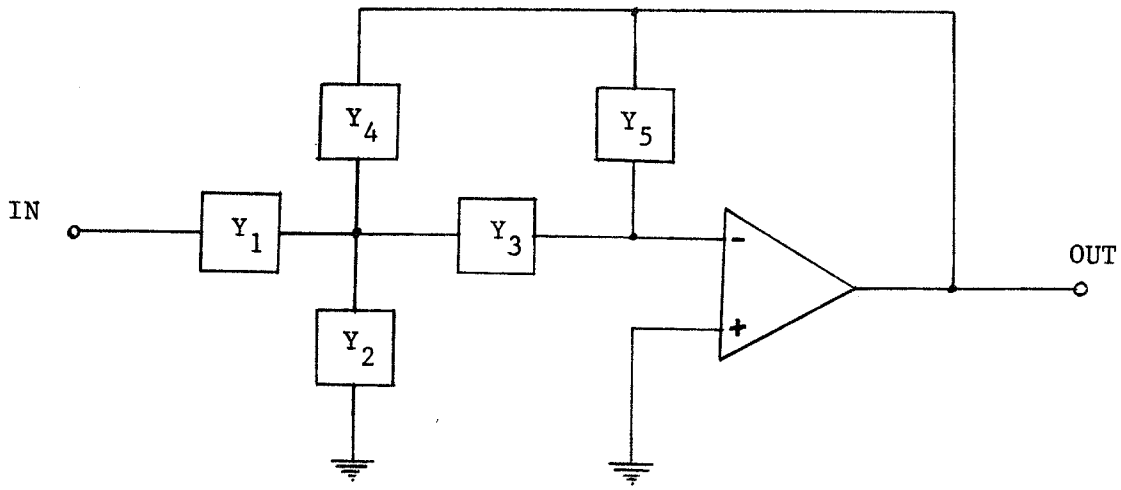
$$-Y_3\,V_a - V_2\,Y_5 = 0 \tag{4.15}$$

Eliminating V_a we get

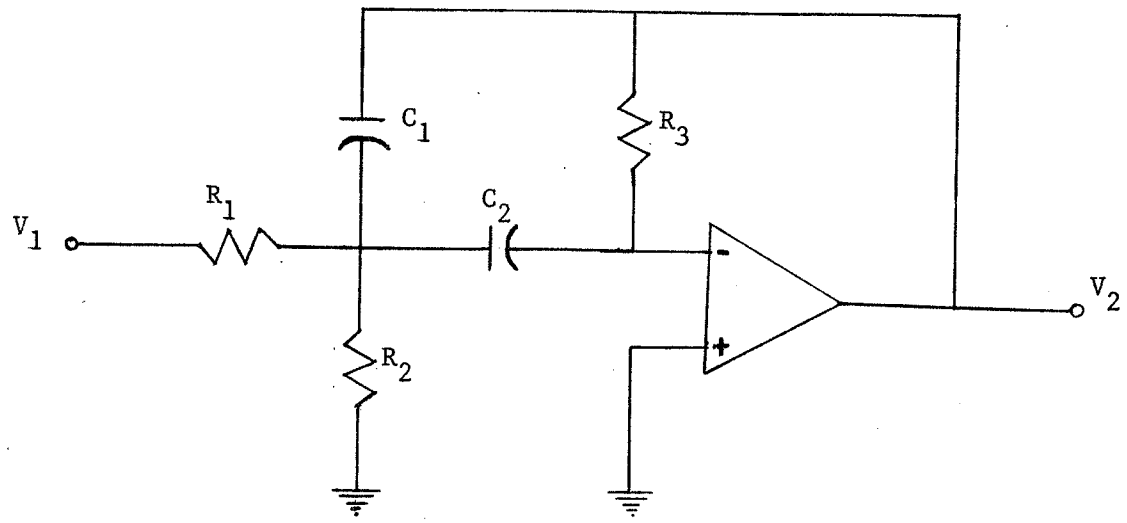
$$\frac{V_2}{V_1} = -\frac{Y_1\,Y_3}{Y_5(Y_1 + Y_2 + Y_3 + Y_4) + Y_3\,Y_4} \tag{4.16}$$

Since the amplifier is used in its inverting configuration, with the positive input grounded, the circuit produces an inverting gain.

We require a second-order band pass filter with inverting gain G, center frequency ω_0, and bandwidth B. From Fig. 4.2b the filter transfer function is:



(a). A general second-order infinite-gain multiple-feedback circuit.



(b). Multiple-feedback band pass filter.

FIG. 4.2 Band-pass filter

$$\frac{V_2}{V_1}(s) = \frac{-s(1/R_1C_1)}{s^2 + S(1/R_3)(1/C_1 + 1/C_2) + (1/R_3\,C_1C_2)(1/R_1 + 1/R_2)}$$

and the bandpass network function is

$$G = \frac{1}{(R_1/R_3)(1 + C_1/C_2)} \tag{4.17}$$

where

$$\omega_0^2 = \frac{1}{R_3\,C_1\,C_2}\left(\frac{1}{R_1} + \frac{1}{R_2}\right) \tag{4.18}$$

$$\frac{1}{Q} = \alpha = \sqrt{\frac{1}{R_3[1/R_1 + 1/R_2]}}\left(\sqrt{\frac{C_1}{C_2}} + \sqrt{\frac{C_2}{C_1}}\right) \tag{4.19}$$

$$\phi = \pi + \phi_{BP} \tag{4.20}$$

$$\tau = \tau_{BP}$$

In practice $R_1 \geq R_2$ and thus R_2 is used to trim the Q. Then, to adjust the center frequency, R_2 and R_3 can be simultaneously adjusted by the same percentage with negligible effect on the Q.

R_1, R_2, R_3, C_1 and C_2 are appropriately selected so that the circuit yields the desired response. This is illustrated by the example given below. The detailed calculations are given in Appendix C.

4.3.1 Numerical values

Let $C_1 = 0.1\ \mu F$; $C_2 = 0.22\ \mu F$; $f_0 = 60$ Hz

and Gain $G = 1$

a) for $Q = 2$:

$R_1 = 53.05\ k\Omega$

$R_2 = 4.1449\ k\Omega$

$R_3 = 77.164\ k\Omega$

b) Similarly, for $Q = 5$

$R_1 = 132.626\ k\Omega$

$R_2 = 1.6788\ k\Omega$

$R_3 = 192.91\ k\Omega$

At different frequencies, the response magnitude is calculated from equation 4.11(a), tabulated in Table 4.1 and plotted in fig. 4.4.

4.3.2 Choice of Q

To analyse the output waveform let the step input to the filter be a steady-state sinusoidal waveform with amplitude A, and frequency f_0.

Then $E_{in} = A \sin \omega_0 t$ (4.22)

Converting to Laplace transforms,

$$E_i(s) = A \frac{\omega_0}{s^2 + \omega_0^2}$$

Then from the tranfer function

$$H(s) = \frac{E_0(s)}{E_i(s)} = \frac{\alpha\omega_0 s}{s^2 + \alpha\omega_0 s + \omega_0^2} \qquad \text{(4.8) (repeated)}$$

$$E_0(s) = \frac{G\alpha\omega_0 s}{(s^2 + \alpha\omega_0 s + \omega_0^2)} E_i(s)$$

$$= \frac{G\omega_0/Q\ s \cdot A\omega_0}{(s^2 + \omega_0/Q\ s + \omega_0^2)(s^2 + \omega_0^2)} \quad \text{where } \alpha = 1/Q,$$

$$= A\,\omega_0\,G \left[\frac{1}{s^2 + \omega_0^2} - \frac{1}{s^2 + \omega_0/Q\ s + \omega_0^2} \right]$$

$$\mathcal{L}^{-1}E(s) = \mathcal{L}^{-1} \frac{GA\omega_0}{s^2 + \omega_0^2} - \mathcal{L}^{-1} \frac{GA\omega_0}{s^2 + \omega_0/Q\ s + \omega_0^2}$$

$$E_0(t) = AG \sin \omega_0 t - GA\omega_0\, \mathcal{L}^{-1} \frac{1}{(s + \omega_0/2Q)^2 + (\omega_0^2 - 1/4\ \omega_0^2/Q^2)}$$

$$= AG \sin \omega_0 t - GA\omega_0 \frac{e^{-\omega_0/2Q\ t}}{\omega_0^2(1 - 1/4Q^2)} \cdot \frac{d}{dt} \cos(\omega_0\sqrt{1 - 1/4Q^2})t$$

TABLE 4.1

FILTER AMPLITUDE RESPONSE

f/f_o	20 log $\|H(j\omega)\|$ (dB) Q = 2	Q = 5
0.1	-59.7	-78.0
0.2	-45.34	-63.6
0.3	-36.3	-54.4
0.4	-29.2	-47.1
0.5	-23.0	-40.5
0.6	-17.1	-33.8
0.8	- 5.9	-18.0
1.0	0	0
2	-23.0	-40.5
3	-33.8	-51.9
4	-40.5	-58.7
5	-45.3	-63.6
6	-49.6	-67.47
7	-52.4	-70.7
8	-55.18	-73.5
10	-59.7	-78.0

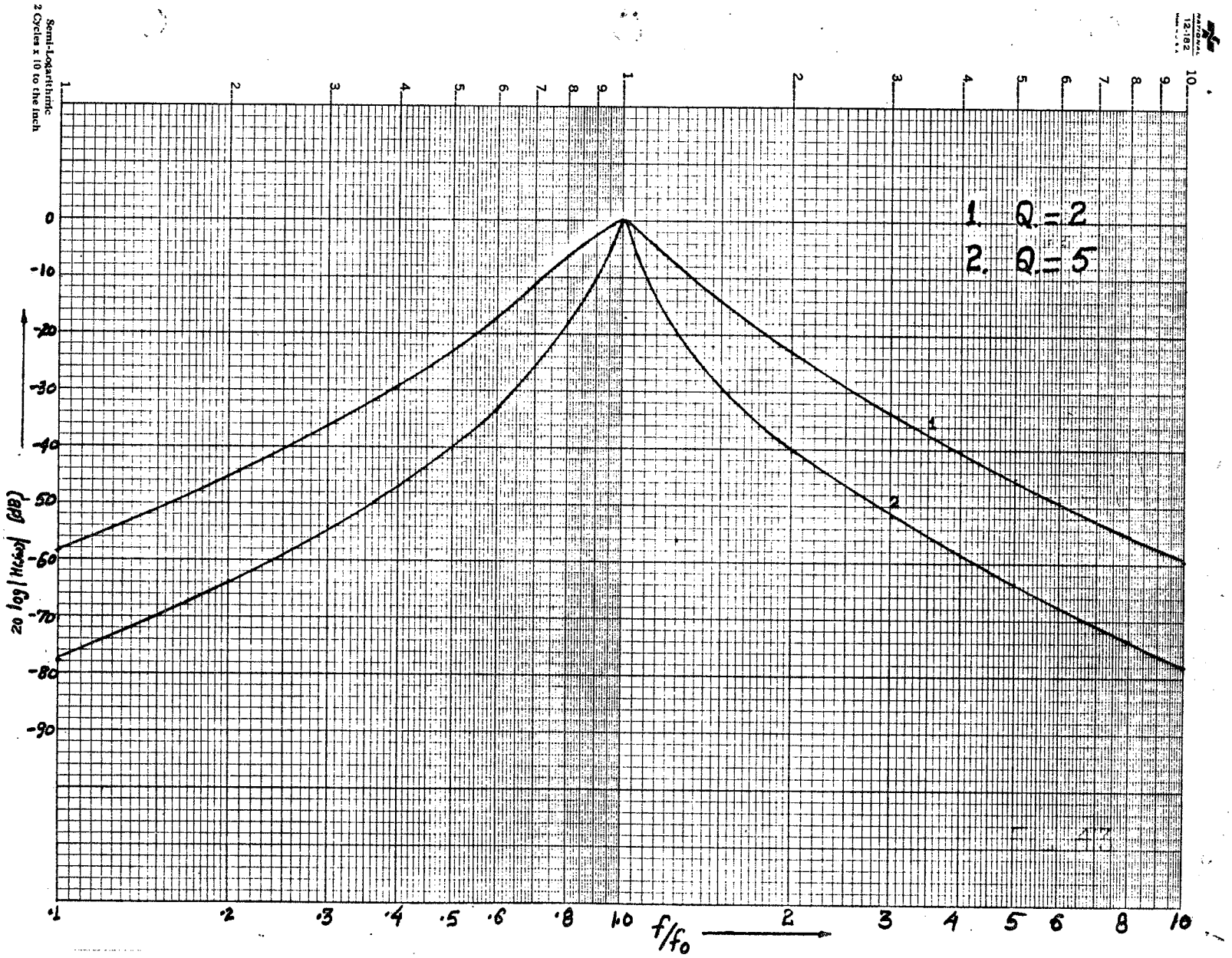


Fig. 4.3 Filter magnitude response.

$$= AG \sin \omega_0 t - \frac{GA\,\omega_0^2\, e^{-\omega_0/2Q\, t}}{\omega_0^2(1 - 1/4Q^2)} \sqrt{1 - 1/4Q^2} \cdot \sin(\omega_0\sqrt{1 - 1/4Q^2})t$$

$$E_0(t) = GA \sin \omega t - \frac{GA}{\sqrt{1 - 1/4Q^2}} e^{-t/\tau} \sin \omega_0\sqrt{1 - 1/4Q^2}\, t \qquad (4.24)$$

where $\tau = \frac{2Q}{\omega_0}$

transient build up or decaying time constant of the filter (time delay).

Thus $\tau \propto Q$ or $\tau = KQ$ (4.25)

where $K = \frac{2}{\omega_0}$ sec. (a constant)

It is evident from (4.24) that the output from the filter is a transient sinusoid with a time constant directly proportional to the Q of the filter circuit. The larger the value of Q, the larger is the transient build-up time constant as shown in Fig. 4.4(a,b) and 4.5(a,b). The dependency of time constant upon Q can also be confirmed from equation (4.13). From (4.12), zero phase delay produced by the filter at center frequency f_0 is obvious thus reducing (4.13) to

$$\tau(\omega_0) = \frac{2Q}{\omega_0}$$

demonstrating the validity of (4.25).

In order to suppress the low and high frequency components effectively, and retain a low time constant, an appropraite value of Q must be selected. As seen in fig. 4.3, for Q equal to 2, the attenuation provided by this particular filter for 3rd harmonic is 33.8 dB. At Q = 5 this value is 51.9 dB. For the fifth harmonic the attenuation by the two filters respectively, is 45.3 dB, and 63.6 dB, compared to the gain at the fundamental frequency. The amount of attenuation provided by the two filters at 30 Hz is 23 dB and 40.5 dB, respectively.

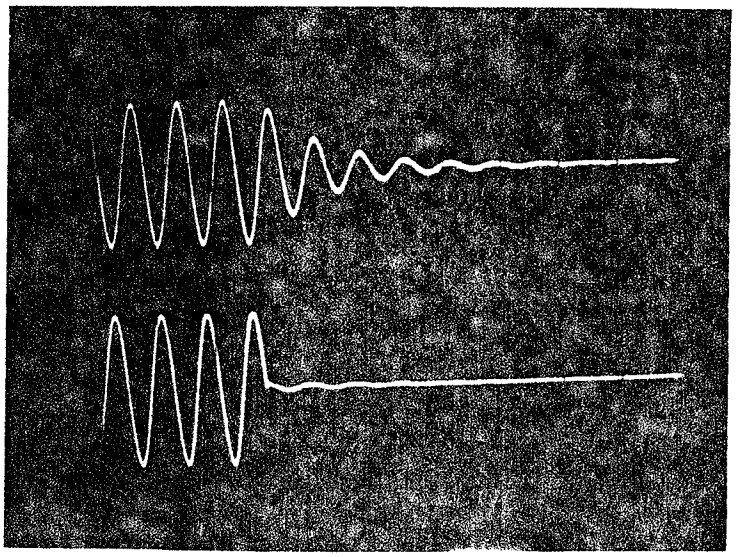
For the two filters the time constant, respectively, is 11 ms and 27 ms *i.e.*, the filter at Q = 2 takes 0.6 cycle to reach within 63% of the final value (by definition of time constant), while the filter at Q = 5 takes almost 1.6 cycles to reach within 63% of the final value.

The delay introduced by the filter of Q = 5 is considered unacceptably large. Therefore, Q = 2 was selected. It attenuates high and low frequency component noise effectively and introduces a reasonable time delay for transient build-up: about half of a cycle.

4.4 Filter Testing and Results

In Fig. 4.3 $|H(j\omega)|$ in dB is plotted against f/f_0, the normalized frequency, for Q = 2 and Q = 5. It can be inferred from the figure that as Q increases, the filter more effectively attenuates high and low frequency components. However, the sharper peak is attained at the expense of a larger time lag. Figures 4.4a, 4.4b and 4.5a, 4.5b demonstrate step input responses, with the filters designed for Q = 2 and Q = 5. Evidently, at higher values of Q, the filter response takes a longer time to reach the final value.

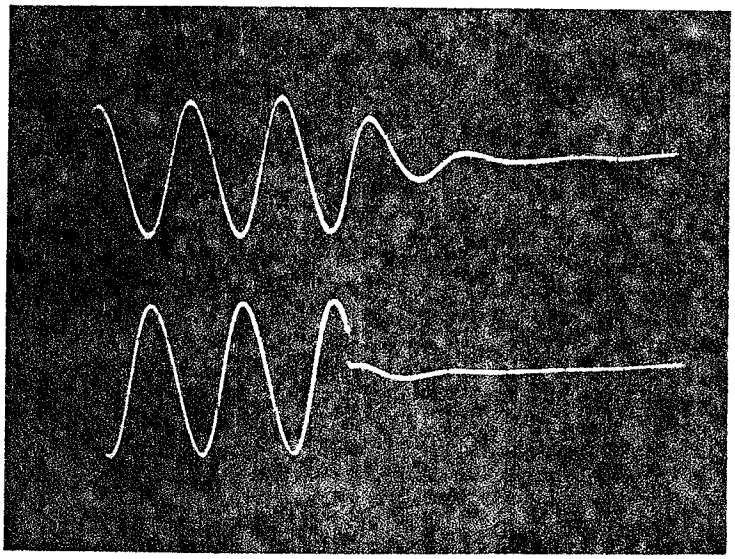
Time delays introduced by the two kinds of filters [Q = 2 and 5], actually measured from the envelope formed by the transient build-up were estimated to be 12 ms and 30 ms. While theoretical delay predictions, for both filters, were 11 ms and 27 ms, respectively. Thus the theoretical and actual delays are in close agreement.



Q = 5, f = 60Hz

(a). ONE: OUTPUT

TWO: INPUT

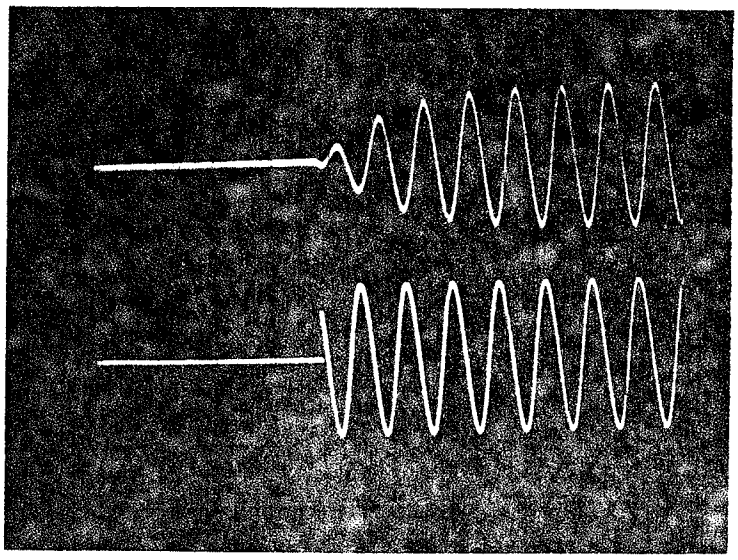


Q = 2, f = 60Hz

(b). ONE: OUTPUT

TWO: INPUT

Fig. 4.4 Filter response.

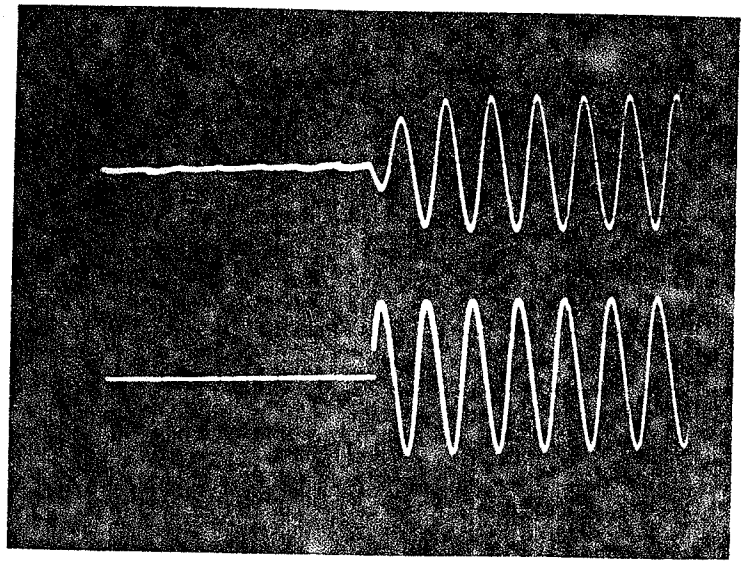


Q = 5 , f = 60Hz

ONE: OUTPUT

TWO: INPUT

(a)



Q = 2, f = 60Hz

ONE: OUTPUT

TWO: INPUT

(b)

Fig. 4.5 Filter response.

CHAPTER 5

TESTING AND RESULTS

5.1 Testing the Algorithm

The method described in the last chapter is used to calculate the fundamental frequency phasors of voltage and current. This information was then used to calculate the complex impedance of the line which further is separated into apparent resistive and reactive components. Table 5.1 details the complex impedance estimation at various phase angles. This test data was then used to draw relay characteristics on an R-X plane as shown in Fig. 5.1. Reasons for deviation from the ideal (a circle) are discussed later.

The relay worked perfectly at all phase angles except in the fourth quadrant where the algorithm is slightly unstable. Since in case of transmission line protection, we are concerned mainly with the first quadrant of the R-X plane, this algorithm is satisfactory. Later the algorithm was tested for different protected impedance zones and for different fault current levels. Data for these tests is tabulated in Tables 5.2 and 5.3, respectively.

5.2 Fault Detection Time

The function of the relay is to detect the fault and decide whether it is inside the protected zone or outside and generate a trip or no trip signal accordingly. For these three functions it should take the least time to avoid any further damage to the line or other equipment. In this particular relay the time between the fault occurrence on the line and the trip signal generation by the microcomputer takes a minimum

TABLE 5.1

RELAY ACCURACY AS A FUNCTION OF PHASE ANGLE

CURRENT	PHASE ANGLE w.r.t. current	SETTING	TRIP CURRENT	TRIP IMP.	ERROR
4.5703 V	+12.3°	1Ω	4.6094 V	0.9915	-0.85%
4.6094 V	+45°	1Ω	4.6484 V	0.9916	-0.84%
4.6484 V	+90°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	+135°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	+172°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	+179°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	-135°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	-90°	1Ω	4.6875 V	0.9917	-0.83%
4.6484 V	-45°	1Ω	unstable		
4.6484 V	-20°	1Ω	4.6875 V	0.9917	-0.83%

TABLE 5.2

RELAY ACCURACY AS A FUNCTION OF VOLTAGE

VOLTAGE	PHASE ANGLE	SETTING	TRIP CURRENT	TRIP IMP.	ERROR
4.6094 V	90°	1Ω	4.6484	0.996	-0.84%
3.9453 V	90°	1Ω	3.9844	0.99	-0.98%
2.98875V	90°	1Ω	3.0078	0.987	-1.3%
2.0313 V	90°	1Ω	2.07	0.981	-1.89%
1.0156 V	90°	1Ω	1.0557	0.963	-3.7%

TABLE 5.3

RELAY ACCURACY AS A FUNCTION OF IMPEDANCE

VOLTAGE	PHASE ANGLE	IMPEDANCE SETTING	TRIP CURRENT	TRIP IMPEDANCE	ERROR
2.46094 V	90°	2Ω	1.25	1.9688	-3.13%
2.46094 V	90°	1.5Ω	1.6797	1.465	-3.49%
2.46094 V	90°	1.25Ω	1.992	1.234	-1.47%
2.46094 V	90°	1.0Ω	2.5	0.984	-1.45%
2.46094 V	90°	0.75Ω	3.32	0.741	-0.88%
2.46094 V	90°	0.5Ω	4.96094	0.496	-0.394%

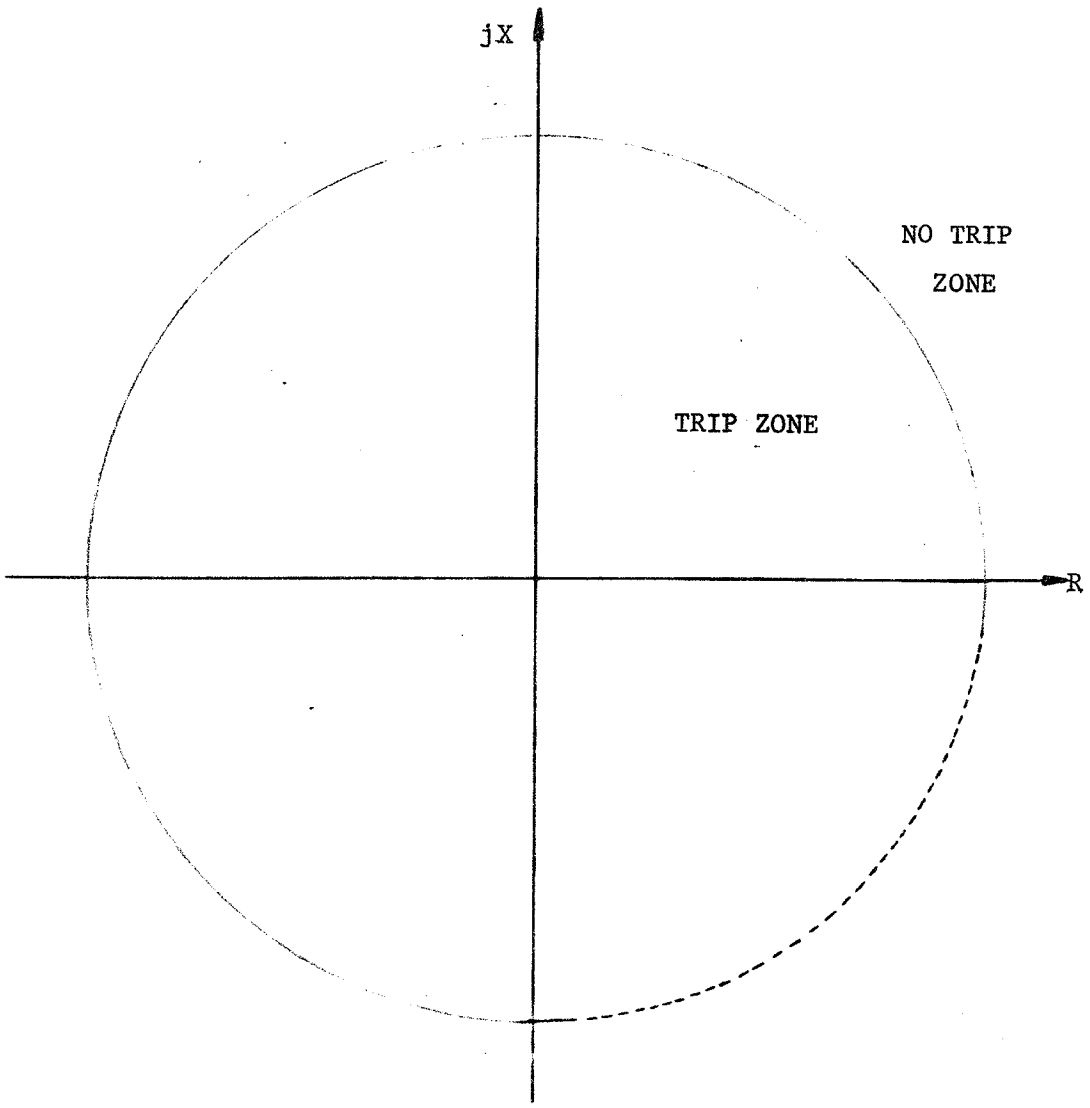


Fig. 5.1 Characteristics of the Digital Impedance Relay.

of 3/4th of a cycle and a maximum of 3/2 of a cycle. In detail it is calculated as described below.

a) Delay produced by analog filter T_f = 10.106 ms

b) Conversion time; analog to digital T_c = 0.05 ms

c) Voltage and current peak detection T_{PK}:

Let α = fault inception angle in degrees

ϕ = phase angle (lagging)

then minimum T_{PK} = $(90 + \phi - \alpha)$ degrees electrical

Provided $\phi > 5°$ (the sampling interval)

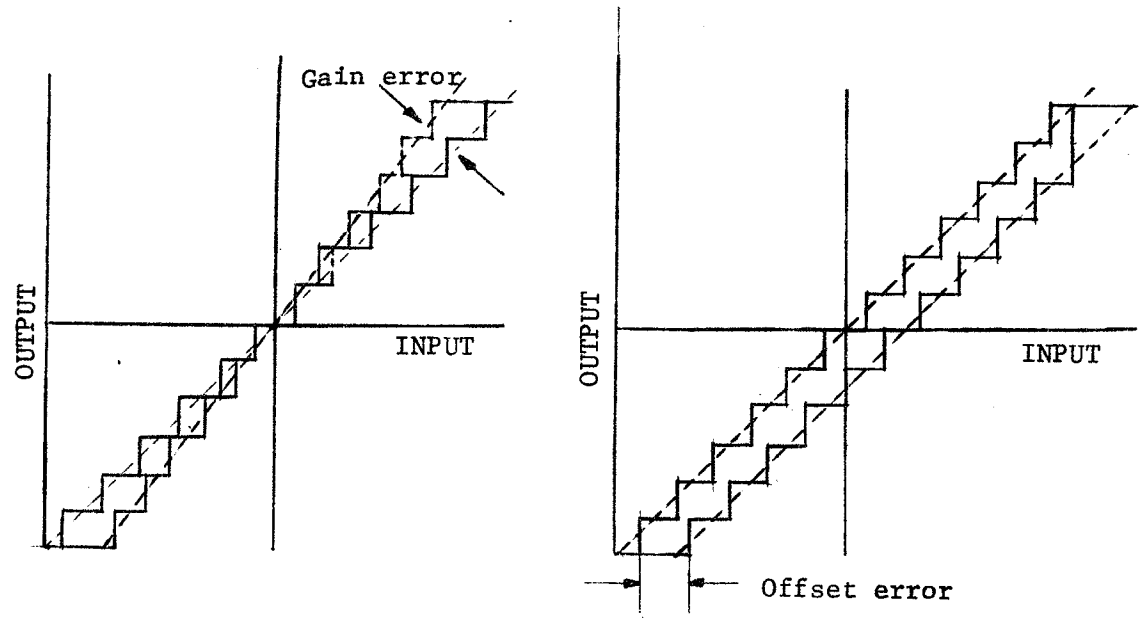
d) Impedance computation T_i = 1.17 ms
(25.25°)

The reason of providing the condition $\phi > 5°$ is: To detect the true peak of the waveforms, the microcomputer should know at least one sample before the true peak occurs.

T_{PK} calculated above is the minimum time taken by the peak detection algorithm. Summing all four together it works out to be 11.3 ms + $(90 + \phi - \alpha)°$ or in time unit [15.5 + $(\phi - \alpha)$ x 0.046] ms. Evidently, this relay generates trip signal in time varying from 3/4th of a cycle to 3/2 of a cycle which, presumably, fast enough to clear the fault or to isolate the faulty line from rest of the system.

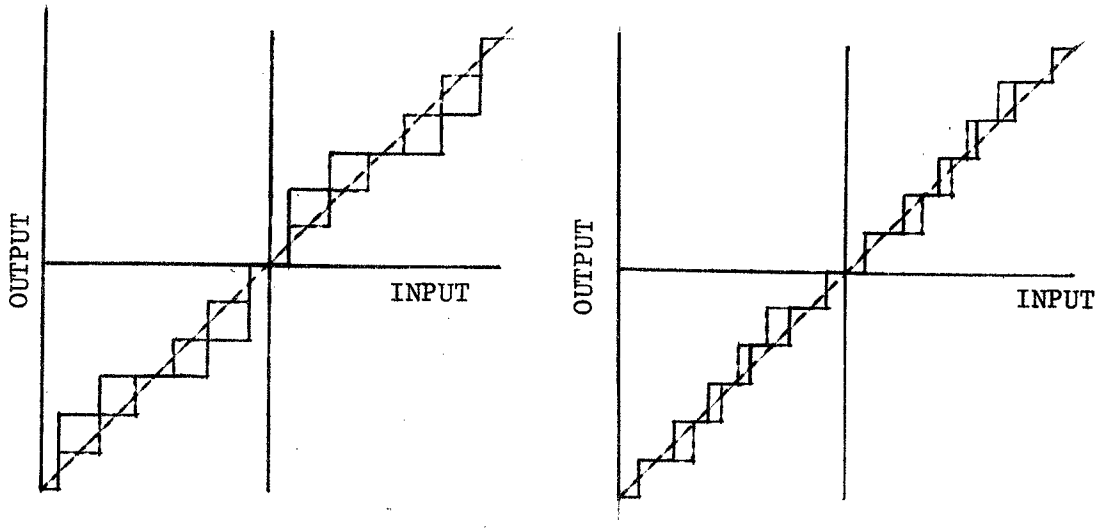
5.3 Sources of Errors

In A/D conversion, there is an inherent quantization uncertainty of ±1/2 LSB. This can be reduced by increasing the number of bits. Besides this, other errors are offset error; the first transition from one code to the next may not occur at exactly ±1/2 LSB; scale factor (or gain) error; the difference between the values at which first transition



a. Gain error

b. Offset error



C. Linearity error

d. Excessive differential nonlinearity error

Fig. 5.2 Typical sources of errors for the analog to digital converter

and last transition occur is not equal to (F.S. - 2 LSB); and linearity error; the difference between transition values are not all equal or uniformly changing. If the differential linearity error is large enough, it is possible for one or more codes to be missed. Figure 5.2 shows all the sources of error graphically for an 8-bit A/D converter.

Besides A/D errors, errors were also observed in impedance measurements as compared with known impedance values. For three cases of testing, the maximum error occured, when impedance settings were changed, from -0.39% to -3.5%. The reason for such a wide variation of errors is the relative weightage of bits near zero level and maximum levels in the multiplication and division processes. Taking a specific example:

In 8-bit resolution with reference voltage -5 V to +5 V the voltage difference between two consecutive bit levels is equal to 39 mV. The measured impedance is less than the actual impedance. Thus, the difference between the real and apparent impedance would obviously be more at lower levels (resulting in large errors) and least at upper levels (resulting in small errors) of the current. These errors exist because of the instruction used in the program that generates a trip signal only when the measured current is slightly (one bit) more than it should have been.

Similarly, the reasons for deviation of this relay characteristics from the ideal circle characteristics can be explained.

CHAPTER 6

CONCLUSIONS

In this work, the author has discussed the application aspects of the 8-bit Motorola 6800 microprocessor system in power system protection. From this design it can be concluded that:

1) The Motorola 6800 microprocessor system is suitable for realization of a digital distance relay and is feasible to use for transmission line protection.

2) A sampling frequency of 4320 Hz (5° electrical) is satisfactory to get results free from aliasing problems.

3) The analog band-pass filter used works accurately to eliminate noise and d.c, currents satisfactorily.

4) A different suitable algorithm would make it possible to use the Motorola microprocessor for the realization of any kind of digital relay.

This microcomputer uses 8-bit analog to digital converters. However, to get more accurate results a 16-bit converter is needed. Accuracy could further be enhanced if in place of 8-bit, a 16-bit processor is used.

This relay's fault detection time should be reduced. Since the major portion of delay is taken by filtering, a better approach to filtering is needed. For example, a combination of analog and digital filtering (to be more economical and reliable).

It is possible to change the performance of a digital impedance relay into that of a digital directional relay simply by noting the phase

angle along with waveform peaks and generating trip signals for some particular phase angle range. Use of multiplexers can further increase the functions that a single microprocessor can process.

APPENDIX A

IMPEDANCE CALCULATION ALGORITHM

```
        LDX     #$0004          Initialization of PIA, both parts as
                                input ports.
        STX     PORT A
        STX     PORT B

TO      BSR     V_PK            Read V_PK
        JSR     V_iPk           Read V_iPk
        BSR     MULTP.          Calibrate V_PK by N
        STAB    Loc 9  Hi       Gave high and low bytes of calibrated
        STAA    Loc 10 Lo       V_PK (Double precision)
        BSR     MULT +9         Calculate V_iPK x Zs
        SUB A   Loc 10          Calculate N x V_PK - V_iPK x Zs
        SBC B   Loc 10          Caclulate N x V_PK - V_iPK x Zs
        BCC     JUMP
        JSR     CLRDIS          if > 0; NO TRIP and continue
                                otherwise generate a TRIP signal
        BSR     TRIP
        STOP

JUMP    JSR     DISPLAY
        BRA     TOP
```

* V_{PK} sub-routine to estimate Voltage Peak.

```
        LDA B   #$02            Initialize check counter
        LDA A    PORT A         Read Port A of PIA and
        BMI      GO             Test the sign bit if negative then
DO      STA A    Loc 1          Skip otherwise save the value.
        DEC B                   Decrease check counter
        BSR      Delay          Apply some delay before reading
        LDA A    PORT A         the signal again
        CMP A    Loc 1          Then compare with previously read
        BCS      DO             value and if greater start again
        TST B                   otherwise test check counter
        BMI      JUMP 1         for valid max. read value.
        BZ       JUMP 1         If not valid peak then
GO      STA A    Loc 1          save and start reading again
        Dec B
```

```
          BSR       DELAY
          LDA A     PORT A
          CMPA      Loc 1
          BCC       GO
          TST B
          BMI       JUMP 2
          BZ        JUMP 2
JUMP 1    LDA A     Loc 1
          NEG A
          JUMP
JUMP 2    LDA A     Loc 1          Calculate the peak value in ascending
          SUB A  #$80              order starting from  00  and save.
          STA A     Loc 2
          RTS.
```

Sub-routine to calculate current peak and phase angle with respect to voltage zero.

$*V_{iPK}$

```
          CLR       Loc 5          Prepare two locations for
          CLR       Loc 6          phase angle measurement
          LDA B  #$ 02             initialize check counter
          LDA A     PORT B         read from Port B of PIA
          BMI       BRANCH         test for sign bit and
START     STA A     Loc 3          save
          inc.      Loc 6
          Dec 8                    Decrease check counter
          JSR       DELAY          Apply some delay before reading
          LDA A     PORT B         the signal again
          CMP A     Loc 3          Then compare with previously
          BCS       START          read value and if greater
          inc       Loc 5          start again otherwise test
          TST B                    check counter for valid
          BZ        JUMP 1         peak.  If not valid then
          BMI       JUMP 1         start reading resolutions
BRANCH    STA A     Loc 3          again
          INC       Loc 6
          Dec B
          JSR       DELAY
          LDA A     PORT B
          CMP A     Loc 3
          BCC       BRANCH
          INC       Loc 5
          TST B
          BZ        JUMP 2
          BMI       JUMP 2
          BRA       START
JUMP 1    LDA A     Loc 3          Adjust reading in proper
          NEG A                    ascending order starting
          JUMP      SKIP           from zero upwards and
JUMP 2    LDA A     Loc B          save and return to
          SUB    #$ 80             master program.
          STA A     Loc 4
          RTS
```

```
*  Sub-routine calculating multiplication of two numbers (Double-Precision)

*  MULTP   LDA A     Loc 4          Make data ready for
           STA A     Loc 11         computation
           LDA A     Loc 8          Load accumulator with multi-
           JUMP      FOUR           plier
 MULT + 9  LDA A     Loc 2          Make data ready for
           STA A     Loc 11         computation
           LDA A     Loc 7          Load accumulator with Mr.
 FOUR      LDX     #$ 0008          Load shift counter
           CLR B                    Prepare for result
 HIGH      BIT A   #$ 01            Test accumulator for 1 and
           BZ        CONTIN         skip.  If one then
           ADC B     Loc 11         add Md to accumulator B.
 CONTIN    ROR B                    shift B and A accumulator
           ROR A
           CLC
           DEX                      decrease shift counter
           BNE       HIGH           If 8 shifts completed then
           RTS                      stop.  Otherwise start again.

           Sub-routine for producing delay.

DELAY      LDX       #$ 000A
    Loops  DEC X
           BNE          Loop 1
           RTS.

           Sub-routine to clear display units.

* CLRDIS
           JSR       OUTSTJ
           00
           00
           00        BLANKS
           00
           00
          $80        The period is necessary
           RTS.

           * Sub-routine to display  V_PK  and  V_iPK

 DISPL
           LDX       # Loc 1
           LDA B     # 02
           JSR.      DISPLAY
           JSR       REDIS
           LDX       #$ --
     Loop  DEX.
           BNE       loop
           RTS.
```

```
                * Sub-routine to display 'TRIP'

TRIP    JSR     OUTSTJ      Call subroutine to
        T                   display TRIP
        R
        I
        P.
        RTS.
```

A.1 Impedance Calculation Algorithm in Machine Language

```
0001    CE      0004
0004    FF      8000
0007    FF      8002

000A    8D      20
000C    BD      0100
000F    8D      59
0011    D7      99
0013    97      9A
0015    8D      5C
0017    90      9A
0019    D2      99
001B    24      07
001D    BD      015A
0020    8D      79
0022    3E
0023    BD      01A1
0026    20      E2

002C    C6      02
002E    B6      8000
0031    2B      11
0033    97      93
0035    5A
0036    8D      52
0038    B6      8000
003B    91      93
003D    25      F4
003F    5D
0040    27      15
0042    2B      B
0044    97      93
0046    5A
0047    8D      41
0048    B6      8000
004B    91      93
004D    24      F4
004F    5D
0050    27      0A
0052    2B      08
0054    20      DC
0056    96      93
```

```
0058    40
0059    7E      005F
005C    96      93
005E    80      80
0060    97      91
0061    39.

0100    C6      02
0102    B6      8002
0105    2B      14
0107    B7      0094
010A    5A
010B    BD      008A
010E    B6      8002
0111    B1      0094
0114    25      F1
0116    50
0117    27      18
0119    2B      16
011B    B7      0094
011E    5A
011F    BD      008A
0122    B6      8002
0125    B1      0094
0128    24      F1
012A    5D
012B    27      0B
012D    2B      09
012F    20      C8
0131    B6      0094
0134    40
0135    7E      013B
0138    B6      0094
013B    80      80
013D    B7      0092
0140    39.

006A    96      92
006C    97      69
006E    96      98
0070    7E      0079
0073    96      91
0075    27      69
0077    96      97
0079    CE      0008
007C    5F
007D    85      01
007F    27      02
0081    D9      69
0083    56
0084    46
0085    0C
0086    09
0087    26      F4
0089    39
```

```
008A    CE    000A
  8D    09
  8E    26    FD
  90    39

015A    BD    FD8C
015D    00
015E    00
015F    00
0160    00
0161    00
0162    80
0163    39

01A1    CE    0091
01A4    C6    03
01A6    BD    FD7B
01A9    BD    FCBC
01AC    CE    2FFF
01AF    09
01B0    26    FD
01B2    39

009B    BD    FD8C
009E    46    05
00A0    04    67
00A2    80
00A3    39.
```

APPENDIX B

SHORT CIRCUIT CURRENT CALCULATION

In order to approach the problem of calculating the initial short circuited current, consider the transmission line has constant inductance and resistance and leakage current is zero. Let the amplitude of voltage at any time t be $V_{PK}\sin(\omega t + \alpha)$. The angle α is the voltage angle when the fault occurs. If the instantaneous voltage is zero and increasing in a positive direction, $\alpha = 0$. If the voltage is at its positive maximum instantaneous value, α is $\pi/2$. At a negative peak α is $3\pi/2$. The differential equation at the instant of fault occurrence is

$$V_{PK}\sin(\omega t + \alpha) = R\, i_f + L\frac{di_f}{dt} \qquad (B.1)$$

if we solve this equation we get the following result

$$i_f = I_{PK}[\sin(\omega t + \alpha - \phi) - e^{-R/L\ t}\sin(\alpha - \phi) \qquad (B.2)$$

where $\phi = \tan^{-1}\frac{\omega L}{R}$

Equation (B.2) demonstrates the presence of a decaying d.c. component with a time constant $\tau = \frac{L}{R}$. Similarly a fault voltage equation can be written as

$$v_f = V_{PK}[(\sin\omega t + \alpha - \theta] - \frac{\sin\theta\sin(\alpha - \phi_1)}{\sin\phi_1}\ e^{-R/L\ t}] \qquad (B.3)$$

In these equations, α represents phase of fault incidence. In equations (B.2) and (B.3) the first term is a pure sinusoid while the second term represents a decaying d.c. offset with time constant which depends upon the L/R ratio of the transmission line.

APPENDIX C

CALCULATION OF Q FOR FILTER

Calculations of circuit parameters

Let $C_1 = 0.1\ \mu F$; $C_2 = 0.22\ \mu F$

Center frequency $\omega_0 = 377$ rad/s

or $f_o = 60$ Hz and $G = 1$

(a) for: $Q = 2$

from relation 4.17

$$1 = \frac{1}{\frac{R_1}{R_3}\left[1 + \frac{0.1}{0.22}\right]}$$

or $$\frac{R_1}{R_3} = \frac{2.2}{3.2}$$

from relation 4.18

$$(377)^2 = \frac{10^{12}}{R_3 \times 0.1 \times 0.22}\left[\frac{1}{R_1} + \frac{1}{R_2}\right]$$

And from 4.19

$$\frac{1}{2} = \sqrt{\frac{1}{R_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right]}}\left(\sqrt{\frac{0.1}{0.22}} + \sqrt{\frac{0.22}{0.1}}\right)$$

squaring both sides and putting the values of $\left(\frac{1}{R_1} + \frac{1}{R_2}\right)$

$$\frac{1}{4} = \frac{10^{12}}{R_3(377)^2 \times R_3 \times 0.1 \times 0.22}\left[\sqrt{\frac{1}{2.2}} + \sqrt{2.2}\right]^2$$

Gives $R_3 = 77.164\ K\Omega$

Also $$R_1 = \frac{2.2 \times R_3}{3.2} = \frac{77.164}{3.2} \times 2.2 = 53.05\ K\Omega$$

$$\frac{1}{R_1} + \frac{1}{R_2} = (377)^2 \times R_3 \times 0,1 \times 0,22 \times 10^{-12}$$

$$= (377)^2 \times 77,164 \times 0,1 \times 0,22 \times 10^{-12} \times 10^{+3}$$

$$= .0002412793$$

$$R_2 = 4.14489 \text{ K}\Omega$$

(b) for: $Q = 5$

$$1 = \frac{1}{\frac{R_1}{R_2}\left[1 + \frac{0,1}{0,22}\right]}$$

$$\frac{R}{R_3} = \frac{2,2}{3,2} = 0,6875$$

Also

$$(377)^2 = \frac{10^{+12}}{R_3 \times 0,1 \times 0,22}\left[\frac{1}{R_1} + \frac{1}{R_2}\right)$$

$$\frac{1}{R_1} + \frac{1}{R_2} = R_3 \times (377)^2 \times 0.022 \times 10^{-12}$$

And

$$\frac{1}{25} = \frac{1}{R_3\left[\frac{1}{R_1} + \frac{1}{R_2}\right]}\left(\sqrt{\frac{0,1}{0,22}} + \sqrt{\frac{0,22}{0,1}}\right)^2$$

gives

$R_3 = 192.91 \text{ K}\Omega$

$R_1 = .6875 \times R_3 = 132,6256 \text{ K}\Omega$

$R_2 = 1,6788 \text{ K}\Omega$

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