EFFICIENT INVERTER DRIVE FOR PUMPS AND FANS

by

FAKHRY AHMED MOUSTAFA EISSA

A Thesis

Submitted to the Faculty of Graduate Studies

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In Partial Fulfillment of the Requirements for the Degree

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IN ELECTRICAL ENGINEERING

Department of Electrical Engineering

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ABSTRACT

The main objective of this investigation is to achieve maximum drive efficiency while controlling the flow of a pump or a fan by a pulse width modulation inverter motor drive.

Different techniques for flow control of pumps and fans, as well as a comparison of these techniques have been reviewed.

The use of a modified McMurray inverter using a microprocessor based Pulse Width Modulation (PWM) for pump and fan drives, was investigated.

The commutation circuit of the inverter was analysed and a strategy of PWM was developed.

Preliminary no-load tests on a prototype single-phase inverter were performed and test results were analysed. A better power supply and better types of filtering and commutating capacitors were recommended for future prototypes.

ACKNOWLEDGEMENT

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LIST OF PRINCIPAL SYMBOLS

C_{F1}	Filtering capacitor
C_{F2}	Filtering capacitor
C1	Commutating capacitor
C2	Commutating capacitor
C_b	Snubber capacitor
D	Toroid average diameter (m)
e_{C1}	Voltage across C1 (V)
e_{C2}	Voltage across C2 (V)
f_1	Fundamental frequency (Hz)
$\hat{f}$	Maximum operating frequency (Hz)
f_{sp}	Specified fundamental frequency (Hz)
i_1	Current through inductor L1 (A)
i_2	Current through inductor L2 (A)
i_3	Current through inductor L3 (A)
I	Total rms harmonic current (A)
I^*	Normalized total rms harmonic current (A)
I_L	Load current (A)
$\hat{I}_L$	Maximum load current (A)
$\hat{I}_n$	nth. harmonic peak current (A)
I_p	Commutation current peak (A)
k	Ratio of toroid average diameter to turn radius
L1	Commutating inductor
L2	Commutating inductor
L3	Commutating inductor
M	Number of commutations per quarter cycle

n	Order of harmonic
N	Toroid number of turns
N_{sp}	Specified motor speed (rpm)
p	Number of pole pairs
Q	Quality factor
r	Toroid turn's radius (m)
r_1	Limiting resistance (Ω)
r_2	Limiting resistance (Ω)
R	Resistance of inductor toroid (Ω)
R_1	Stator resistance (Ω)
R_2	Rotor resistance (Ω)
R_b	Snubber resistance (Ω)
s	Slip (pu)
t_{off}	Thyristor turn-off time (s)
T	Torque (N.m)
T_c	Commutation time (s)
U_g	Half the dc bus voltage (V)
V1	Main thyristor
V2	Main thyristor
V3	Diode
V4	Diode
V5	Auxilliary thyristor
V6	Auxilliary thyristor
V_n	nth. harmonic peak voltage (V)

V_n^*	nth. harmonic normalized peak voltage
v_{1sp}	Specified normalized fundamental peak voltage (V)
v_{AN}	Phase voltage of phase A (V)
v_{AB}	Line A-to-Line B voltage (V)
X	Commutation circuit equivalent reactance (Ω)
X_1	Stator leakage reactance (Ω)
X_2	Rotor leakage reactance (Ω)
X_m	Magnetizing reactance (Ω)
ρ	Resistance per 1000 ft (Ω)
ω	Angular frequency (rad/s)
ω_o	Resonance angular frequency (rad/s)
ϕ_{AG}	Air gap flux (wb)
τ	Duration at the end of which V2 is fired (s)

CHAPTER I

INTRODUCTION

1.1 Pump and Fan General Characteristics

An important factor in the control of flow of a pump or fan is the pump or fan charactertistic . Figure 1.1 shows the design curves of head and efficiency versus flow for a type of pump where head decreases as flow increases [1]. Other pumps may have flatter or steeper head/flow characteristics. The drooping type of characteristic of Figure 1.1 is desirable for systems where flow control is required.

Figure 1.1 shows the pump characteristics at 100% of the rated speed. As flow increases, the static head that the pump can operate against, goes down. Also, the figure shows the variation of the pump efficiency with flow at 100% of the rated speed. The system resistance is shown in Figure 1.2. Higher flow means higher static head (pressure) for the pump to operate against. The intersection of the system head curve with the pump head curve determines the operating point. Fans have similar operating characteristics.

1.2 Flow Control of Pumps and Fans

Flow control of pumps and fans can be accomplished by two methods. The first controls the flow at a constant pump speed by creating an artificial system head. The second controls the flow by driving the pump with an adjustable speed drive.

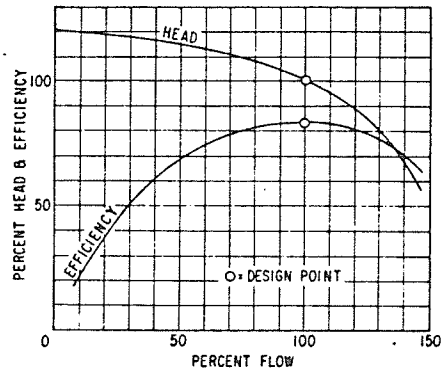


Figure 1,1 Pump Characteristics.

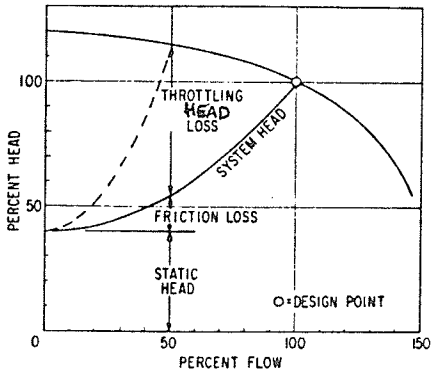


Figure 1,2 System Characteristics.

1.2.1 Flow control at constant speed

In this method, the flow control is accomplished by using throttling valves or dampers. Hence a new system head is created. As shown in Figure 1.2 [1], if the flow is to be reduced from 100% to 50%, the overall head must be increased by partially closing the valve until the artificial system head intersects the pump head curve at 50% as shown by the dotted line. The objective of reduced flow is accomplished, but the head exerted by the pump is more than that required by the system resulting in what is called throttling energy loss which is relatively large as shown in Figure 1.2. The friction losses in a pumping system are a function of pipe size and length, number and type of fittings, liquid flow rate and the nature of the liquid. In general, they vary as the square of the flow rate. The total system head curve is the sum of the static head and friction losses.

1.2.2 Adjustable speed pumps and fans

To help realize the significance of adjustable speed pumps and fans, compared to constant speed ones, the following fundamentals are presented:

1) All else being constant, flow is proportional to pump (fan) speed (rpm).
2) All else being constant, head (pressure) exerted by a pump (fan) varies as the square of speed.

An approximate set of head/flow curves for various speeds can be constructed as shown in Figure 1.3 [1]. It can readily be seen that if

flow is to be reduced by varying the speed, then all that is needed is to reduce the speed of the pump until its head curve intersects the system head curve at the desired flow.

Figure 1.4 shows the effect of speed on pump (fan) efficiency [1]. While flow control at constant speed results in a decline in the efficiency with reduced flow (Figure 1.1), the speed control has the effect of maintaining the pump (fan) efficiency on a relatively high level over a wide range of flow.

1.3 A Comparison Between Flow Control at Constant Speed and Using a Variable Speed Drive

Figure 1.5 shows a comparison between controlling the flow of a pump at constant speed and using an adjustable speed drive. The pump has a constant static head H_s. In order to reduce the flow from 100% by an amount q_1 at constant speed (n_1), an artificial system curve (dashed curve) is created by partially closing a throttling valve and consequently increasing the head losses by an amount h_s (point B to point A). On the other hand, by reducing the pump speed from n_1 to n_2 to reduce the flow by the same amount q_1, the head losses will be reduced from H_1 to H_2 (point C to point B) and the power required by the pump at the reduced flow will be reduced from point A_1 to point B_1 on the power curves.

1.4 Variable Speed Induction Motor Drives for Pumps and Fans

For many years, variable speed drives have been a necessary prerequisite for many industrial processes. The variable speed dc motor drives are the most commonly used power source in this connection.

However, in certain cases, the dc motor does not satisfy the demands for reliability and low maintenance. This may apply in hazardous and corrosive environments and certain locations, where access to the

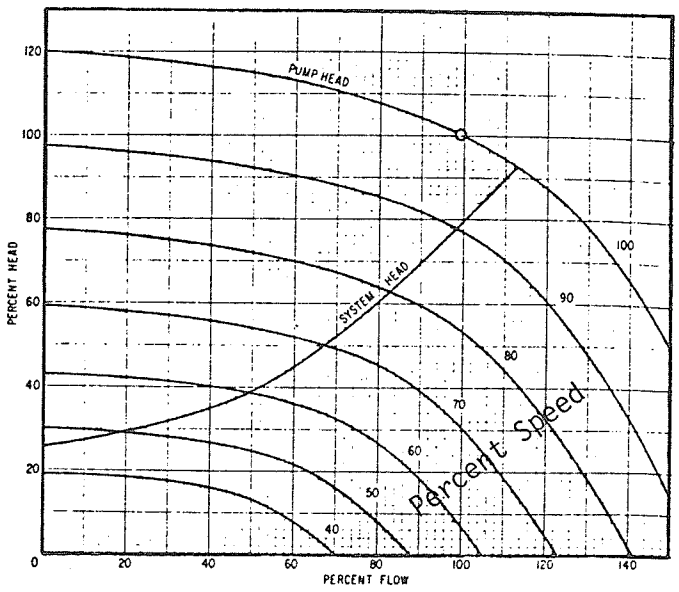


Figure 1.3 Typical Head/Flow/Speed Curves.

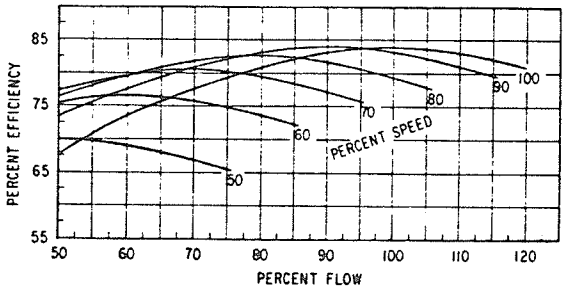


Figure 1.4 Pump efficiency/Flow/Speed Curves.

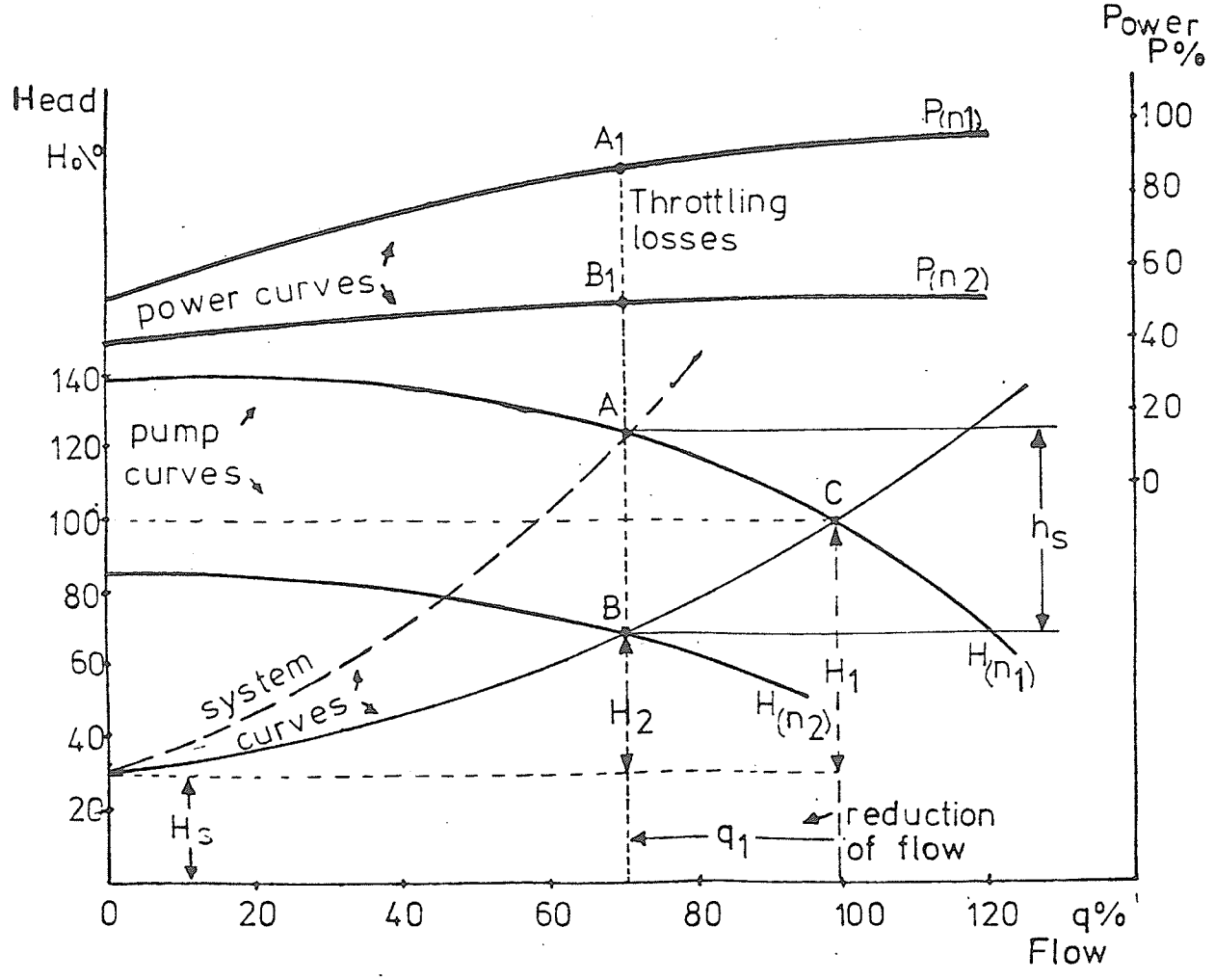


Figure 1.5 A comparison between flow control at constant speed and using a variable speed drive.

motor for servicing is restricted. Pump and fan drives are involved. There is consequently a general desire to use compact brushless motors for such applications. One alternative to the dc motor in such instances is the ac squirrel-cage induction motor (SCIM).

The SCIM offers some distinct electrical and mechanical advantages. Electrically, the motor has no slip rings or brushes requiring electrical maintenance, and needs no additional source of excitation. Both the rotating and stationary magnetic fields are provided by one set of three power leads. Mechanically, the motor offers a rugged cast rotor capable of mechanical integrity to a very high speed. Coupled with the absence of the mechanical commutator, present in dc machines, this allows the SCIM to achieve far greater maximum speeds than it is possible with dc machinery. The SCIM, when compared to dc machines, is far less expensive, smaller, weighs less and has a lower rotor inertia for better dynamic response.

The SCIM has always been considered to be an extremely robust and reliable machine, but it has the disadvantage of normally running at an essentially constant speed. Therefore, due to all the advantages, mentioned of a SCIM, great efforts have been made to develop a suitable speed control system for it.

As a result of the development of high power semiconductor devices during the last decade, it is now possible to build static frequency converters for feeding induction motors. The general principles of such frequency converters have been known for many years. However, such equipment has been expensive and has had difficulties in competing with

dc motor drives, despite the disadvantages of the dc motor in severe environments where pumps and fans are often involved.

Nevertheless, in recent years, there has been a significant increase in the demand for such systems. At the same time, the semiconductors have become cheaper and therefore frequency converters have become more competitive with dc motor drives. Further, the reliability and low maintenance costs of the induction motor are being more and more widely appreciated and customers are prepared to pay for these advantages.

It should be noted in particular that if the induction motor is already installed in the plant, then only a frequency converter is required, and that may be the cheapest solution.

Even if the frequency converter is very reliable, it will result in a still safer system since an induction motor, in the event of a fault in the frequency converter, can also be connected direct to the network. This gives an extra back-up. Until the frequency converter has been put back into service again, the process can therefore be provisionally controlled by means of ON/OFF control of the motor.

In the case of multi-motor drives with more than three or four motors connected to the same frequency converter, the purchase price alone may justify a frequency converter, since the induction motor is much cheaper than a dc motor.

There are mechanical methods available for varying the speed of pumps and fans. These methods will not be reviewed since they are out of the scope of this thesis.

1.5 Pulsewidth Modulated Inverters for Squirrel-Cage Induction Motor Drives

The variable speed squirrel-cage induction motor requires the dual functions of voltage and frequency control. Both the cycloconverter and the inverter can achieve these functions.

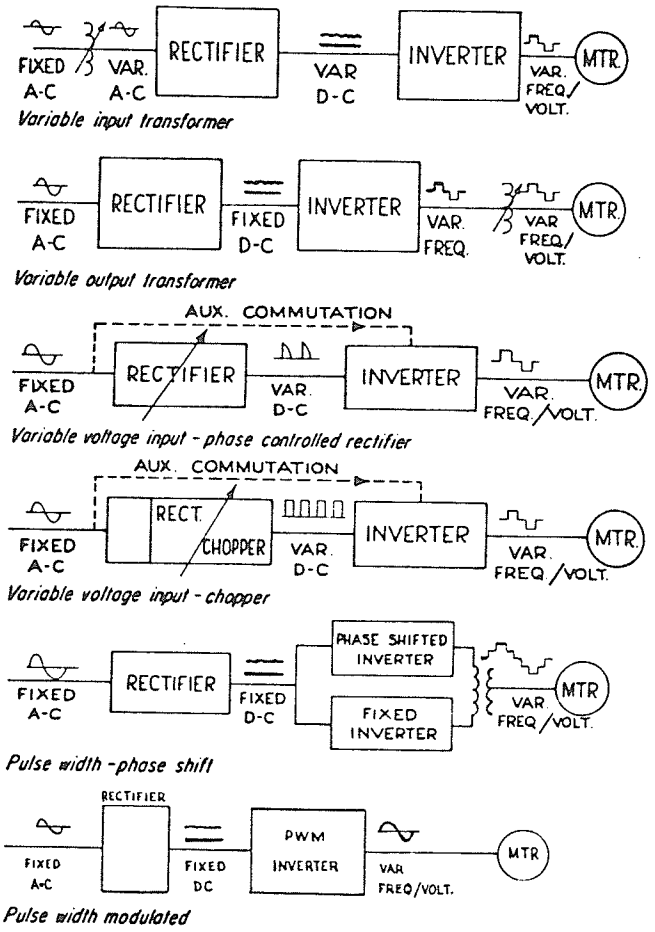
The inverter systems can be designated as:

1. Variable-input transformer.
2. Variable-output transformer.
3. Variable-voltage input (phase-controlled rectifier or chopper).
4. Pulse-width (phase shift).
5. Pulse-width modulation (PWM).

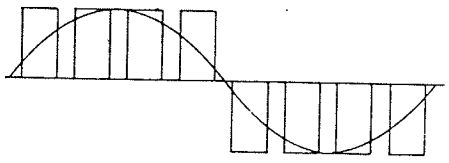
Comparative block diagrams of these inverter types are shown in Figure 1.6.

The most modern approach to static adjustable frequency power conversion, the PWM inverter, offers a list of features unobtainable with anyone of the shown inverter types [19]:

1. It is a completely solid-state device, offering a fast accurate response and efficient power conversion.
2. Only one controlled power stage is required, eliminating the need for phase controlled rectifiers, choppers or transformers and their associated regulators.
3. As opposed to the phase-controlled inverter, the PWM inverter with its fixed diode rectifier taking power smoothly from the plant supply, operates at a 96 percent power factor, regardless of frequency.



Inverter system classification by type of voltage control employed.



Typical single-phase PWM wave shape.

Figure 1,6 Inverter Types.
(Taken from Reference [19]).

4. The PWM inverter operates from a fixed-voltage dc supply, allowing multi-inverter operation from a common dc bus. Since the inverter bridge is itself inherently capable of regenerating power back to the dc bus, the bus acts as a common energy-source sink for multi-inverter systems. Motoring inverters will draw power from the bus, while inverters whose motors are holding back or braking an overhauling load will pump power to the bus. The net power difference, i.e., work load plus machine losses, is drawn from the plant power. (Without the ability to be operated from a common bus, any inverter with an overhauling load would require a special regenerative rectifier section to allow pumping power back to the plant line).

   The fixed-voltage dc bus also lends itself to support by means of energy storing capacitors or batteries to provide unaffected inverter operation during plant power outages.

5. The modulated wave shape greatly improves low-frequency motor operation. Using existing modulation techniques to generate low-frequency voltage waveshapes more closely resembling a sinewave, induction and synchronous reluctance motors may be operated at very low frequencies without the cogging and excessive heating inherent with conventional square-wave inverters.

1.6 Losses and Efficiency of Variable Speed Induction Motors Driving Pumps and Fans

One of the control methods in common use today is to maintain a constant voltage/frequency (V/f) ratio (constant flux) while controlling the speed of an induction motor.

A simplified analysis is presented in this section to show that while controlling the speed of an induction motor driving a pump or a fan over a wide speed range, more reduction in the total motor losses can be achieved by adjusting the supply voltage to a value lower than that required to maintain a constant V/f ratio while still producing the torque required by the load.

Some approximations and assumptions have been made to simplify the analysis. However, the approach could be a guide for future investigations.

1.6.1 Induction Motor Approximate Performance Calculations

The analysis of induction motors under conditions of variable frequency operation can be based on the conventional equivalent circuit shown in Figure 1.7.

The following assumptions and approximations are made:

(a) With a low slip speed over a wide speed range, the rotor reactance X_2 would be much smaller than R_2/s and therefore may be neglected.

(b) The air gap flux is a fixed percentage of the total stator flux [2]. In other words, the air gap voltage E_G is a fixed fraction

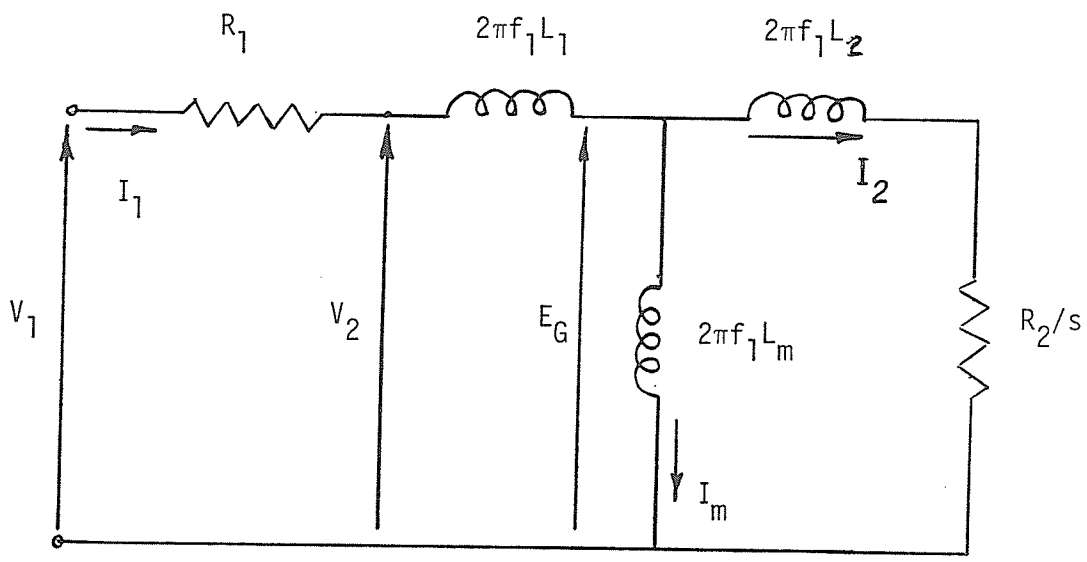


Figure 1.7 Induction motor conventional equivalent circuit.

of V_2 (Figure 1.7). A typical value for this fraction is 0.93 [2].

(c) The values of the equivalent circuit parameters (R_1, L_1, L_m, L_2 and R_2) remain constant when both the supply voltage and frequency are changed. (R_1 and R_2 are the stator and rotor resistances respectively. L_1 and L_2 are the stator and rotor inductances respectively. L_m is the magnetizing inductance).

The air gap voltage E_G induced by the air gap flux ϕ_{AG} is given by

$$E_G = k_G \, \phi_{AG} \, f_1 \quad \text{V/phase} \tag{1.1}$$

where, f_1 is the supply fundamental frequency (Hz)

k_G is a constant.

The rotor current I_2 can be found from

$$I_2 = \frac{E_G}{[R_2/s)^2 + (2\pi f_1 L_2)^2]^{\frac{1}{2}}}$$

$$\cong k_i \, \frac{V_2}{(R_2/s)}$$

where, k_i is a constant.

If V_1 is used as being nearly equal to V_2 [2], then

$$I_2 \cong k_i \, \frac{V_1}{(R_2/s)} \quad . \tag{1.2}$$

The developed torque per phase can be expressed as

$$T = \frac{7.04}{N_s} I_2^2 \, (R_2/s)$$

$$= \frac{7.04p}{60 \, f_1} \, I_2^2 \, (R_2/s) \qquad (1.3)$$

where, N_s is the synchronous speed (rpm)

p is the number of pole pairs.

Substituting for I_2 from 1.2 into 1.3 yields

$$T = k_t \left(\frac{V_1}{f_1}\right)^2 sf_1 \qquad (1.4)$$

where, k_t is a constant.

The net developed power per phase can be obtained as

$$P_o = I_2^2 \, R_2 \left(\frac{1-s}{s}\right) \quad . \qquad (1.5)$$

The magnetizing current can be expressed approximately by

$$I_m \cong \frac{V_1}{2\pi L_m f_1} \quad . \qquad (1.6)$$

Since I_2 and I_m are in quadrature, then the stator current can be found from

$$I_1^2 = I_2^2 + I_m^2 \quad . \qquad (1.7)$$

1.6.2 Simplified Analysis of Motor Losses and Efficiency

(a) Copper Losses:

Rotor copper losses = $I_2^2 R_2^2$

Stator copper losses = $I_1^2 R_1 = (I_2^2 + I_m^2) R_1$

Therefore,

$$\text{Total copper losses} = (1 + \frac{R_1}{R_2}) I_2^2 R_2 + I_m^2 R_1 \quad . \qquad (1.8)$$

By eliminating $(I_2^2 R_2)$ and I_m using (1.5) and (1.6) respectively, (1.8) becomes

$$\text{Total copper losses} = (1 + \frac{R_1}{R_2}) (\frac{s}{1 - s}) P_0 + \frac{R_1}{(2\pi L_m)^2} (\frac{V_1}{f_1})^2 \quad . \qquad (1.9)$$

Since the first term of expression (1.9) depends on the load and the second term depends upon the magnetizing current, then by defining the first term as load losses (W_L) and the second term as excitation losses (W_{ex}), we get

$$W_L = (1 + \frac{R_1}{R_2}) (\frac{s}{1 - s}) P_0 = k_L (\frac{s}{1 - s}) P_0 \qquad (1.10)$$

$$W_{ex} = k_{ex} (\frac{V_1}{f_1})^2 \qquad (1.11)$$

where k_L and k_{ex} are constants given by

$$\left.\begin{aligned} k_L &= 1 + \frac{R_1}{R_2} \\ k_{ex} &= \frac{R_1}{(2\pi L_m)^2} \end{aligned}\right\} \qquad (1.12)$$

(b) Iron Losses

The two components of iron losses are given by [3] as:

Eddy-Current Losses:

$$W_e \propto B_m^2 f_1^2$$

where, W_e is the eddy-current losses.

B_m is the magnetic flux density.

The constant of proportionality depends on the lamination thickness and steel resistivity.

Since the air gap flux is proportional to (V_1/f_1), then,

$$W_e = k_e V_1^2 \qquad (1.13)$$

where, k_e is a constant.

Hysteresis Losses:

$$W_h \propto f_1 B_m^x$$

where, W_h is the hysteresis losses.

x varies between 1.5 and 1.7

(for convenience of comparison, x will be taken equal to 2 in this analysis).

The constant of proportionality depends on the quality of iron and volume of core. Hence,

$$W_h = k_h \left(\frac{V_1}{f_1}\right)^2 f_1 \qquad (1.14)$$

where, k_h is a constant.

(c) Mechanical Losses

For motors driving pumps and fans, where power varies as the cube of the speed, the mechanical losses would also vary as the cube of the speed. Therefore,

$$W_m = k_m f_1^3 \qquad (1.15)$$

where, W_m is the mechanical losses.

k_m is a constant.

From (1.10), (1.13), (1.14) and (1.15), the total motor losses (W_T) can be obtained as a function of the net developed power (P_0), supply voltage (V_1), supply frequency (f_1) and pu slip (s) as:

$$W_T = k_L \left(\frac{s}{1 - s}\right) P_0 + k_{ex} \left(\frac{V_1}{f_1}\right)^2 + k_e V_1 + k_h f_1 \left(\frac{V_1}{f_1}\right)^2 + k_m f_1^3 \qquad (1.16)$$

where, k_L, k_{ex}, k_e, k_h and k_m are constants.

A pump or a fan requires a torque which varies as the square of speed and an input power which varies as the cube of speed. Therefore, for an induction motor driving a pump or a fan:

$$\left.\begin{aligned} T &\propto N^2 \\ P_0 &\propto N^3 \end{aligned}\right\} \quad (1.17)$$

where, N is the speed

T is the developed torque per phase

P_0 is the net developed power per phase.

In the following analysis, subscripts A and B will be used to denote all the variables at 100% speed and reduced speed respectively.

Assume that the pump speed was reduced from N_A to N_B by reducing the motor's power supply frequency from f_{1A} to f_{1B}. Then, by defining

$$x_n = N_B/N_A = f_{1B}/f_{1A} \quad , \quad x_n < 1 \quad , \qquad (1.18)$$

T_B and P_{OB} would be obtained by (1.17) as:

$$\left.\begin{aligned} T_B &= x_n^2 \, T_A \\ P_{OB} &= x_n^3 \, P_{OA} \end{aligned}\right\} \quad (1.19)$$

While reducing the supply frequency from f_{1A} to f_{1B}, assume the supply voltage was reduced from V_{1A} to V_{1B}. As a result, assume the slip has changed from s_A to s_B.

Let,

$$x_v = V_{1B}/V_{1A} \quad , x_v < 1 \tag{1.20}$$

$$x_s = s_B/s_A \quad , x_s \leq 1 \tag{1.21}$$

It can be shown, from equations (1.4), (1.18), (1.19), (1.20) and (1.21), that

$$x_s = x_n^3/x_v^2 \quad . \tag{1.22}$$

From expressions (1.10), (1.11), (1.13), (1.14) and (1.15) for the different motor losses, it can be shown that

$$\left.\begin{aligned} W_{LB}/W_{LA} &= x_n^3 \left(\frac{x_s\, s_A}{1 - x_s\, s_A}\right)/\left(\frac{s_A}{1 - s_A}\right) \\ W_{exB}/W_{exA} &= (x_v/x_n)^2 \\ W_{eB}/W_{eA} &= x_v^2 \\ W_{hB}/W_{hA} &= x_v^2/x_n \\ W_{mB}/W_{mA} &= x_n^3 \end{aligned}\right\} \tag{1.23}$$

where, x_n, x_v and x_s are given by (1.18), (1.20) and (1.21) respectively.

Table 1.1 shows the different motor losses at 50% speed ($x_n = 0.50$) as in percentage of the motor losses at 100% speed for three different supply voltage adjustments at the reduced speed ($x_v = 0.50$, 0.40 and $1/2\sqrt{2}$). The table is based on the equations given by (1.23) assuming 0.04 pu slip (s_A) at 100% speed.

It can readily be seen from the table that, at 50% speed, by adjusting the supply voltage at 50% of its value at 100% speed (constant V/f ratio), the slip was reduced by 50% ($s_B = 0.02$ pu) and the load losses were reduced appreciably but at the expense of the excitation losses where no reduction took place. On the other hand, by adjusting the voltage to $1/2\sqrt{2}$ ($\cong 0.35$) of its value at 100% speed, the slip did not change from its value at 100% speed ($s_B = s_A = 0.04$ pu) and although the excitation and iron losses were appreciably reduced, the load losses were almost doubled compared to the first adjustment ($x_v = 0.50$). In the third case, when the supply voltage was adjusted at 0.40 of its value at 100% speed, which is between the two values of the other two adjustments, a relatively reasonable reduction in all the motor losses was obtained.

The above comparison indicates that at any reduced speed, by adjusting the supply voltage at a proper value below the value required to maintain a constant flux, we should be able to achieve more reduction in the overall motor losses and hence improve the motor efficiency. This can also be shown from the expression for the total motor losses at any reduced speed which can be obtained

	$x_v = 0.50$	$x_v = 0.40$	$x_v = 1/2\sqrt{2}$
s_B (pu)	0.02	0.03	0.04
Rotor copper losses (%)	6.12	9.66	12.5
Stator copper losses (%)	6.12	9.66	12.5
Excitation losses (%)	100	64.0	50.0
Eddy current losses (%)	25	16.0	12.5
Hysteresis losses (%)	50	32.0	25.0
Mechanical losses (%)	12.5	12.5	12.5

Table 1.1

Motor losses at 50% speed as in percentage of losses at 100% speed for different supply voltage adjustments. (Assuming 0.04 pu slip at 100% speed).

from equation (1.16) as:

$$W_{TB} = k_L \left(\frac{s_B}{1 - s_B}\right) P_{OB} + k_{ex} \left(\frac{V_{1B}}{f_{1B}}\right)^2 + k_e V_{1B}^2 + k_h f_{1B} \left(\frac{V_{1B}}{f_{1B}}\right)^2 + k_m f_{1B}^3 \tag{1.24}$$

By eliminating s_B using equations (1.20), (1.21) and (1.22), equation (1.24) can be expressed as:

$$W_{TB} = \frac{a}{V_{1B}^2 - b} + c\, V_{1B}^2 + d \tag{1.25}$$

where,

$$\left.\begin{aligned} a &= k_L\, P_{OB}\, V_{1A}^2\, s_A \left(\frac{f_{1B}}{f_{1A}}\right)^3 \\ b &= s_A\, V_{1A}^2 \left(\frac{f_{1B}}{f_{1A}}\right)^3 \\ c &= \frac{k_{ex}}{f_{1B}} + \frac{k_h}{f_{1B}} + k_e \\ d &= k_m\, f_{1B}^3 \end{aligned}\right\} \tag{1.26}$$

The factors a, b, c and d, defined by (1.26), depend on the reduced frequency (speed), the load torque/speed characteristic (which determines P_{OB}), parameters of the motor's equivalent circuit (which determine k_L and k_{ex}) and the type of motor (which determines k_h, k_e and k_m). Therefore, for a particular reduced speed, a specific load characteristic , and a specific motor, the factors a, b, c and d could be considered constant.

Hence, it can readily be seen from equation (1.25) that at any reduced speed there is an optimum value for the supply voltage (V_{1B}^*) at which the total motor losses can be minimized while still producing the power required by the load at the reduced speed. Assuming the values of a, b, c and d are known at the particular reduced speed, V_{1B}^* can simply be obtained by differentiating both sides of (1.25) with respect to V_{1B} and setting the derivative equal to zero.

By defining the motor efficiency at the reduced speed as

$$\eta_B = \frac{P_{OB}}{P_{OB} + W_{TB}} \tag{1.27}$$

then, by adjusting the supply voltage at V_{1B}^*, the total motor losses (W_{TB}) could be minimized and consequently according to (1.27), the motor efficiency would be maximized while still producing the power (P_{OB}) required by the load at the reduced speed.

An experimental study [4] has been implemented on an induction motor (3 HP, 208V, 8.9A, 3-phase) driving a pump (with a specified torque/speed characteristic). Over a wide speed range, values for the optimum supply voltage were determined at which motor efficiency was maximized at any reduced speed. An emperical relation between the optimum supply voltage and frequency was determined as

$$E_1 = 0.1665\ f_1^{1.718} + 17.96 \qquad V \tag{1.28}$$

where, E_1 is the optimum line-line supply voltage (V).

f_1 is the supply frequency (Hz).

They found that, over a wide speed range, the optimum supply voltage (achieving maximum motor efficiency) was less than that required to maintain a constant V/f ratio, (see Figure 1.8 taken from [4]. which is consistent with the simplified analytic approach presented in this section.

The main subject of this thesis is to achieve maximum drive efficiency while controlling the flow of a pump or a fan by a Pulse Width Modulation (PWM) inverter motor drive.

An efficient PWM inverter circuit is analysed in Chapter II.

An optimum PWM strategy is developed, in Chapter III, to achieve the optimum voltage/frequency relation (1.28) [4] and hence maximize the motor efficiency over a wide speed range. While achieving the optimum V/f relation, the PWM switching patterns developed minimize the motor nontriplen harmonic currents up to the 43rd. harmonic.

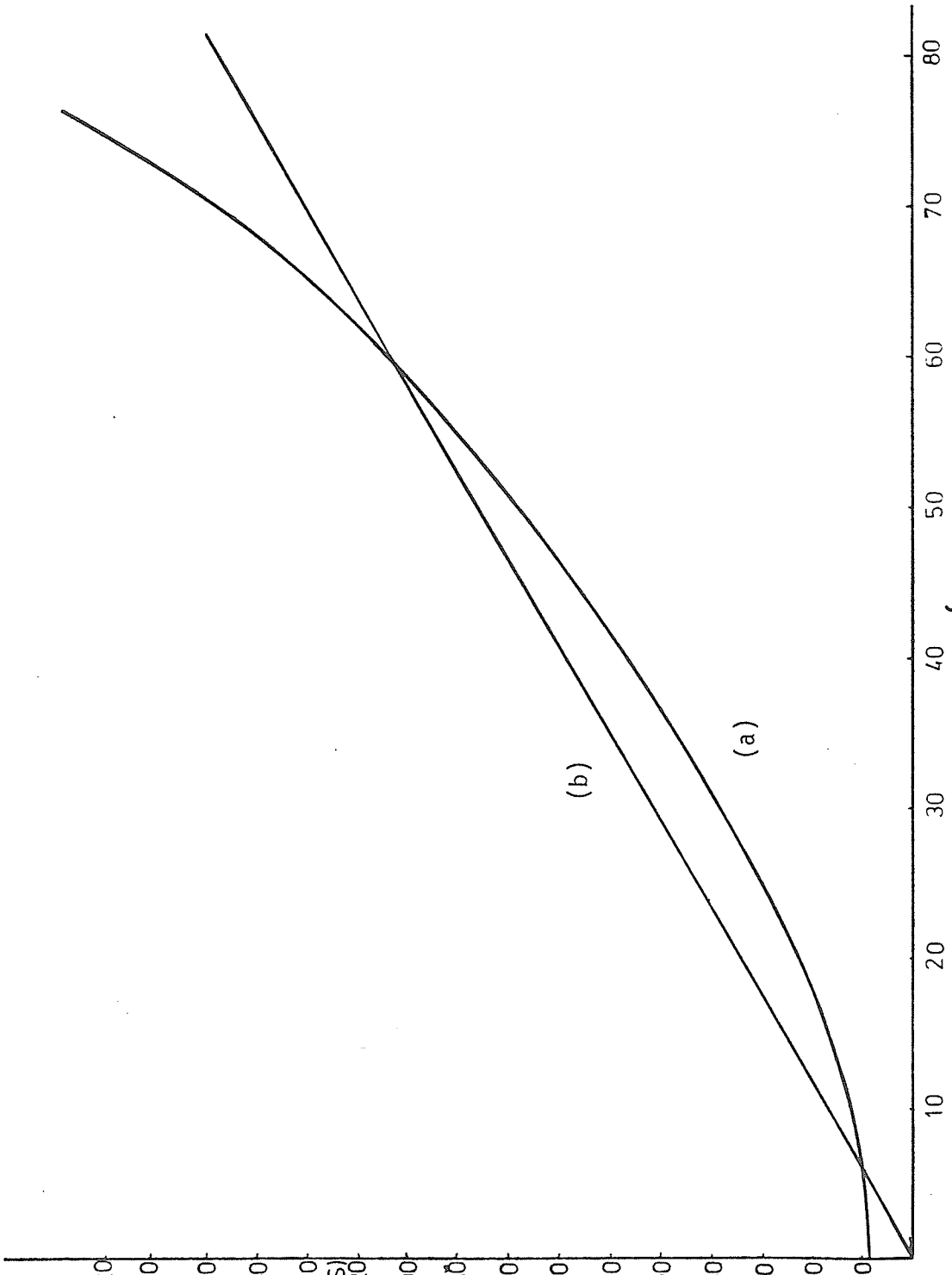


Figure 1.8 Supply line-line voltage versus frequency (taken from Ref. [4]).

(a) Optimum V/f relation. (b) Constant V/f ratio.

CHAPTER II

INVERTER DESIGN

2.1 General Principle

The inverter circuit [5], shown in Figure 2.1, is one phase of a three-phase inverter. The other two phases are duplicates of this circuit.

The circuit consists of two main thyristors V1 and V2, two diodes V3 and V4, two auxilliary or commutating thyristors V5 and V6, two equal capacitors C1 and C2 and three equal inductors L1, L2 and L3.

Commutation of the main thyristors V1 and V2 is accomplished by means of the auxilliary thyristors V5 and V6 in conjunction with the capacitors C1 and C2 and the inductors L1, L2 and L3. To commutate V1, V5 is fired, while to commutate V2, V6 is fired.

2.2 Theory of Operation

Suppose, initially, that capacitor C1 is charged negatively ($e_{C1} = - U_g$) and capacitor C2 is charged positively ($e_{C2} = + 3 U_g$) relative to the polarities of e_{C1} and e_{C2} shown in Figure 2.1. The charges on C1 and C2 have been acquired during the previous operation.

Also, assume initially that the main thyristor V1 is conducting current I_L to the load in the direction shown in Figure 2.1. The inverter load, being an induction motor, is highly inductive. Therefore

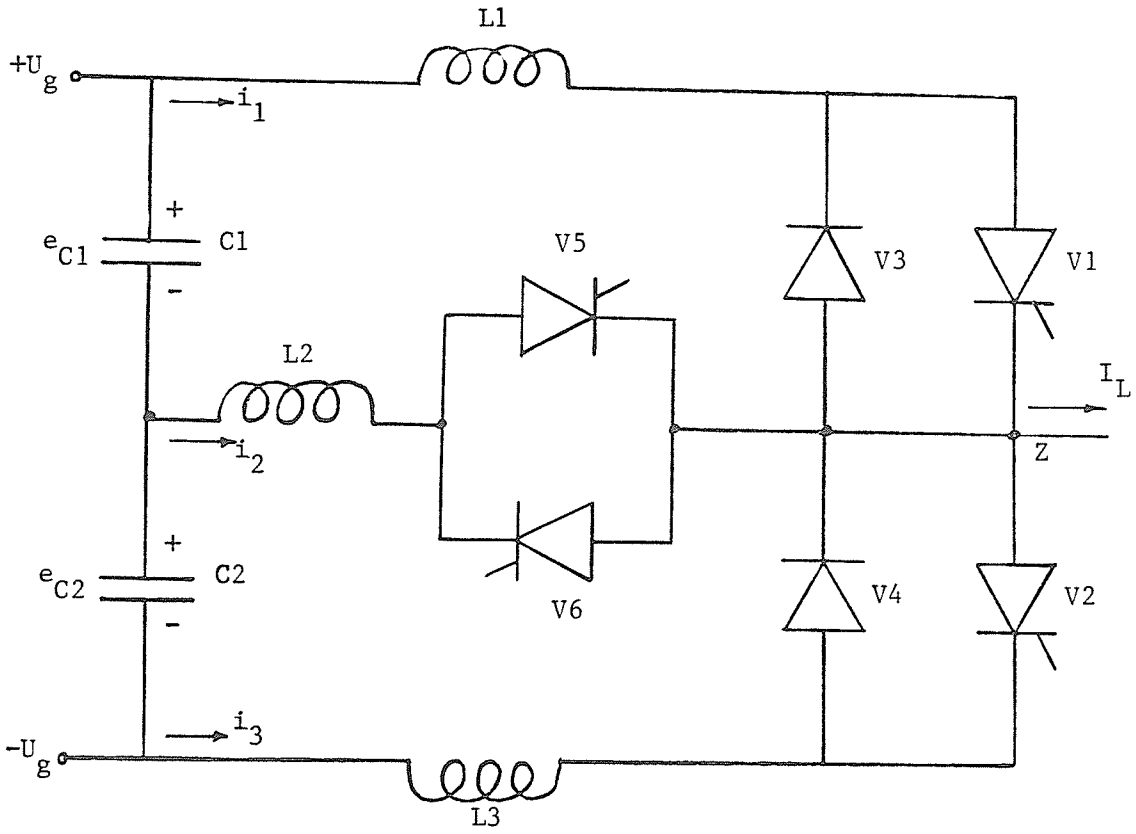


Figure 2,1 INVERTER CIRCUIT,
(L1=L2=L3=L & C1=C2=C)

the load current, I_L, during the commutation interval is assumed to be constant.

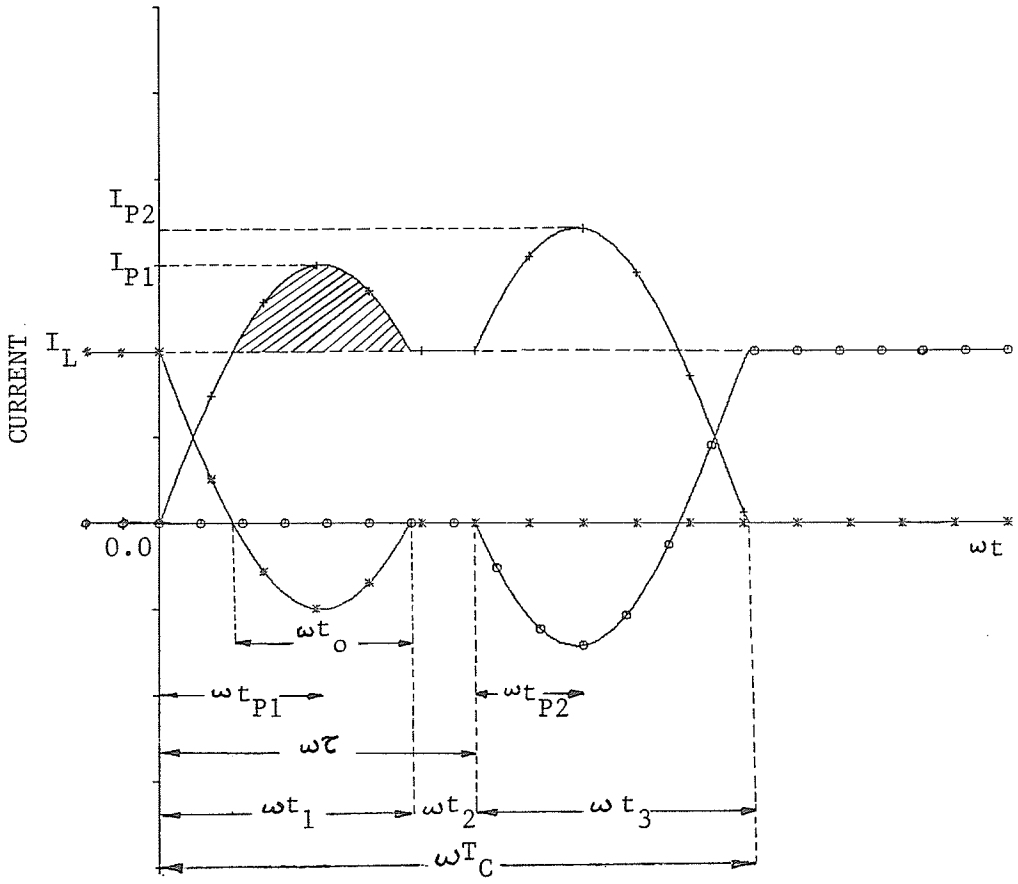
Figure 2.2 shows a detail of the commutation interval of the inverter circuit Figure 2.1.

Firing thyristor V5, allows a path for capacitors C1 and C2 to discharge through, producing the commutating current, i_2, which flows in the upper half of the inverter circuit. The current i_2 builds up taking part of the load current from V1 and hence reducing the current i_1 in inductor L1 (initially, $i_1 = I_L$). When i_2 equals I_L, the current in V1 is reduced to zero, and any further increase in i_2 flows through diode V3 (shaded area in Figure 2.2a).

When i_2 decreases to the point when i_2 equals I_L (after time t_1), the current in diode V3 is zero, and thyristor V1 must be capable of blocking voltage. The minimum time for which i_2 exceeds I_L, t_o, is the turn-off time of the thyristor. During this interval, the thyristor V1 has a reverse voltage equal to the forward voltage drop on diode V3.

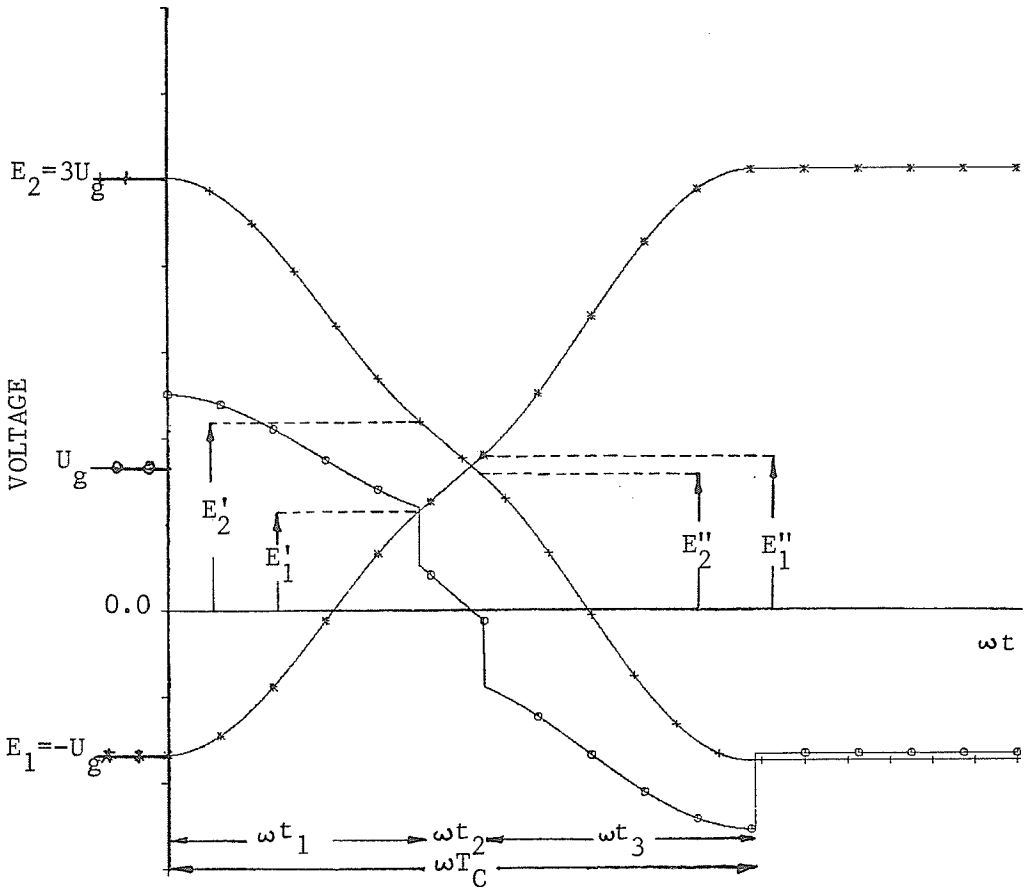
When i_2 equals I_L, the former, being a resonant current, tends to decrease below I_L. But, since I_L is assumed to be substantially constant during the commutation interval, the commutating current i_2 is held constant at the value of I_L and the capacitor voltages change linearly with time for a duration t_2 at the end of which the main thyristor V2 is fired.

Firing thyristor V2, allows a path for capacitors C1 and C2 to discharge through. The discharge current i_2 (having an initial value



*** I1
+++ I2
000 I3

FIGURE 2.2A INVERTER OPERATION, CURRENT WAVEFORMS.



××× VOLTAGE ACROSS C1
+++ VOLTAGE ACROSS C2
000 VOLTAGE OF POINT Z

FIGURE 2.2B INVERTER OPERATION, VOLTAGE WAVEFORMS.

of I_L) builds up exceeding I_L. The excess of i_2 over I_L flows through V2 to the lower half of the inverter circuit of Figure 2.1.

When i_2 equals I_L, the current in V2 is reduced to zero. As i_2 goes below I_L, the current i_3 (in inductor L3) builds up and flows through diode V4 so that the sum of i_2 and i_3 at any instant is equal to the load current I_L.

At the end of the commutation interval, i_2 is reduced to zero, while i_3 equals I_L and diode V4 carries the load current. Capacitor C1 is positively charged ($e_{C1} = + 3 U_g$) and capacitor C2 is negatively charged ($e_{C2} = - U_g$).

2.3 Analysis of the Commutation Circuit

The analysis of the commutation circuit of the inverter of Figure 2.1, is based on the analysis of the general circuit of Figure 2.3. This circuit consists of a capacitor C', inductance L' and resistance R' (representing losses), connected in series to a source of d.c. voltage E_o. The initial voltage on the capacitor is E_i, and the initial current is I_i, with polarities as indicated in Figure 2.3.

Assuming the oscillatory case, the current i_C and the voltage e_C can be obtained as:

$$i_C = \frac{E_o - E_i}{\omega L'} e^{-\alpha t} \sin\omega t - I_i \frac{\omega_o}{\omega} e^{-\alpha t} \sin(\omega t - \phi) \qquad (2.1)$$

$$e_C = E_o - (E_o - E_i) \frac{\omega_o}{\omega} e^{-\alpha t} \sin(\omega t + \phi) + \frac{I_i}{\omega C'} e^{-\alpha t} \sin\omega t \qquad (2.2)$$

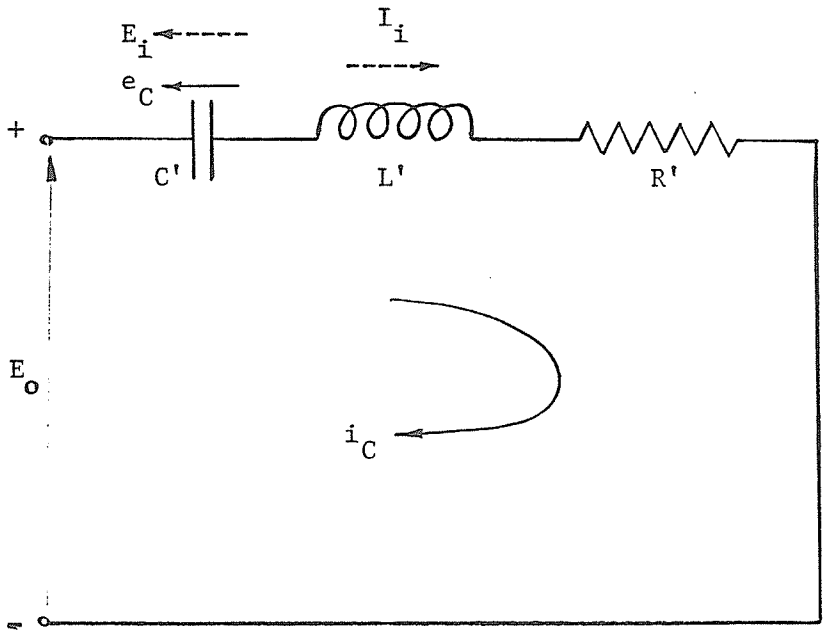


Figure 2,3 A general L-R-C circuit with a d,c. source,

where,

$$\left.\begin{aligned} \omega_o^2 &= \frac{1}{L'C'} \quad , \quad \alpha = \frac{R'}{2L'} \\ \omega^2 &= \omega_o^2 - \alpha^2 > 0 \quad , \quad \phi = \tan^{-1}\left(\frac{\omega}{\alpha}\right) \end{aligned}\right\} \quad . \tag{2.3}$$

If the losses in the circuit are relatively small, then $\omega_o >> \alpha$ and the following approximations are valid.

$$\left.\begin{aligned} \omega_o &\approx \omega \\ X = \sqrt{\frac{L'}{C'}} &\approx \omega L' \approx \frac{1}{\omega C'} \\ \frac{\alpha}{\omega} = \frac{R}{2\omega L'} &\approx \frac{1}{2Q} \quad ; \quad \left(Q = \frac{X}{R'}\right) \\ \phi &\approx \frac{\pi}{2} \quad , \sin(\omega t - \phi) \approx -\cos\omega t \end{aligned}\right\} \quad . \tag{2.4}$$

Equations (2.1) and (2.2) can now be written approximately as

$$i_C \approx \left[\frac{E_o - E_i}{X} \sin\omega t + I_i \cos\omega t\right] e^{-\omega t/2Q} \tag{2.5}$$

$$e_C \approx E_o + \left[X I_i \sin\omega t - (E_o - E_i) \cos\omega t\right] e^{-\omega t/2Q} \quad . \tag{2.6}$$

Before proceeding to the inverter circuit, the following assumptions are made and will be used in the analysis of the commutation circuit.

1) The load current remains constant during the commutation interval.
2) The thyristors are perfect switches.
3) Each of the commutating inductances is lumped, i.e., no stray circuit inductance.

The approximate general equations (2.5) and (2.6) for i_C and e_C, respectively, will now be applied to the specific conditions of the commutation circuit of the inverter of Figure 2.1.

During the first part, of duration t_1 (Figure 2.2), it can be shown that the inverter circuit is equivalent to the circuit shown in Figure 2.4. Comparing Figures 2.3 and 2.4, equations (2.3) - (2.6) apply with:

$$R' = 2R \quad , \quad L' = 2L \quad , \quad C' = 2C \tag{2.7}$$

$$E_o = o \quad , \quad I_i = o \quad , \quad E_i = - E_1 = U_g$$

giving,

$$i_2 = \frac{U_g}{X} \, e^{-\omega t/2Q} \sin\omega t \tag{2.8}$$

$$e_{C1} = - \, U_g \, e^{-\omega t/2Q} \cos\omega t \tag{2.9}$$

$$i_1 = I_L - i_2 \quad . \tag{2.10}$$

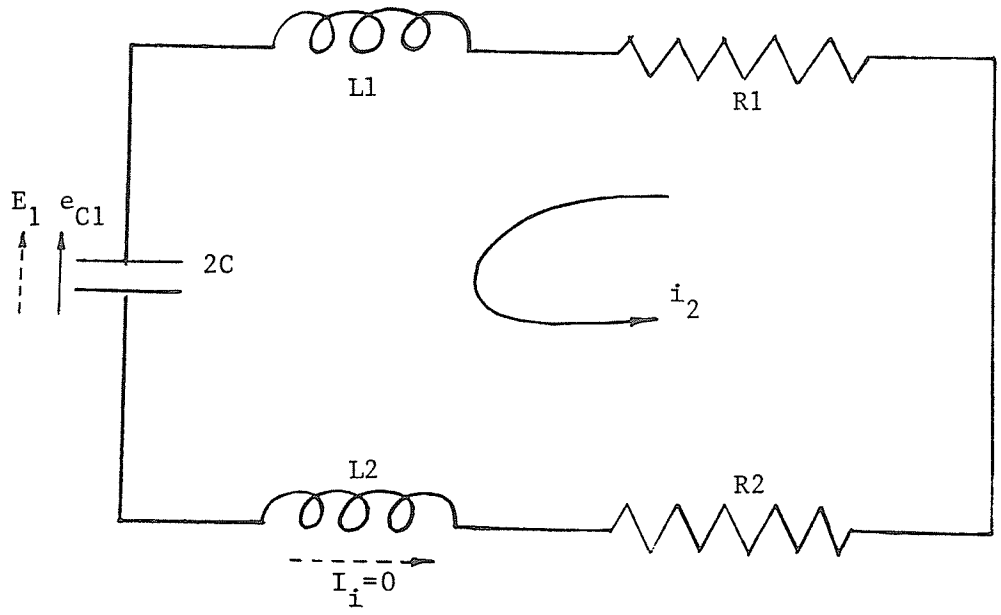


Figure 2.4 Equivalent circuit of Figure 2.1 during the first part of the commutation interval, (L1=L2=L3=L & R1=R2=R).

The voltage on capacitor C2 is simply given by

$$e_{C2} = 2\,U_g - e_{C1} = 2\,U_g + U_g\,e^{-\omega t/2Q}\cos\omega t \quad . \tag{2.11}$$

As shown in Figure 2.2a, the commutating current, i_2, builds up exceeding the load current I_L and reaches a peak I_{P1} after time t_{P1}. The peak I_{P1} can easily be found by differentiating i_2 [given by equation (2.8)] with respect to time and setting the derivative equal to zero, i.e.,

$$0 = \frac{U_g}{X}\; e^{-\omega t_{P1}/2Q}\,[\omega\cos\omega t_{P1} \;-(\omega/2Q)\sin\omega t_{P1}] \quad .$$

Therefore,

$$\omega t_{P1} = \tan^{-1}(2Q) \quad , \quad 0 < \omega t_{P1} \leq \frac{\pi}{2} \tag{2.12}$$

Substituting for the value of ωt_{P1} from equation (2.12) in equation (2.8), the peak I_{P1} is obtained.

At the end of the first transient, after time t_1, thyristor V1 must have been turned off, and the final conditions are found from equations (2.8) - (2.11) as:

$$I_L = \frac{U_g}{X}\; e^{-\omega t_1/2Q}\;\sin\omega t_1 \tag{2.13}$$

$$E_1' = -\,U_g\,e^{-\omega t_1/2Q}\cos\omega t_1 \tag{2.14}$$

$$i_1 = 0 \tag{2.15}$$

$$E_2' = 2\,U_g - E_1' = 2\,U_g + U_g\,e^{-\omega t_1/2Q}\cos\omega t_1 \qquad (2.16)$$

where, E_1' and E_2' are the voltages on capacitors C1 and C2, respectively, after time t_1, (with respect to the polarities on C1 and C2 shown in Figure 2.1).

The final conditions, at the end of the first transient, are the initial conditions of the second transient of duration t_2. During this duration, the capacitor voltages, as shown in Figure 2.2b, change linearly with time as

$$e_{C1} = E_1' + (X\,I_L)\,\omega t \qquad (2.17)$$

$$e_{C2} = 2\,U_g - e_{C1} = E_2' - (X\,I_L)\,\omega t \qquad (2.18)$$

while current i_2 is equal to the load current I_L.

For proper thyristor activation during the commutation interval, the firing instant of the main thyristor V2, should be independent of the load current commutated. In order to meet this requirement, a fixed duration (τ), to be elapsed after the instant V5 is fired, is specified (Figure 2.2). Accordingly, the duration of the second transient is determined as:

$$\left.\begin{aligned} t_2 &= \tau - t_1 \\ \text{or} \qquad \omega t_2 &= \omega\tau - \omega t_1 \end{aligned}\right\} \quad . \qquad (2.19)$$

It is readily seen from equation (2.13) that the angle (ωt_1) depends upon the load current (I_L). In order to maintain ($\omega\tau$) at the specified value, the duration t_2 is found to be dependent on the load current in the way given by equation (2.19).

Equation (2.13) has been solved to find (ωt_1) for different values of load current, with

$$\left.\begin{aligned} \hat{I}_L &= 40.0 \text{ A} \quad = \text{Maximum load current} \\ U_g &= 134 \text{ V} \quad , \quad Q = 18.55 \quad , \omega\tau = 3.0 \text{ rad.} \end{aligned}\right\} \qquad (2.20)$$

(X is related to Q, U_g and $\hat{I}_L$ as will be shown in section 2.4).

With ($\omega\tau$) specified to be equal to 3 rad., (ωt_2) was determined, for each value of the load current, by using equation (2.19).

The angles (ωt_1) and (ωt_2) were, then, plotted against the load current I_L as shown in Figure 2.5. It can readily be seen that the angle (ωt_1) ranges between a minimum value and a maximum value. The minimum value of (ωt_1) [when $I_L = \hat{I}_L$] represents the minimum time to be elapsed since V5 is fired so that the main thyristor V1 can be turned-off. In this case, (ωt_2) is at its maximum value. The maximum value of (ωt_1) is ($\omega\tau$) [$\omega t_2 = o$]. This value corresponds to a load current (I_{LO}) which can be determined from equation (2.13) as

$$I_{LO} = \frac{U_g}{X} \; e^{-\omega\tau/2Q} \sin\omega\tau \quad . \qquad (2.21)$$

($I_{LO} = 8.146$ A for the conditions given by (2.20)).

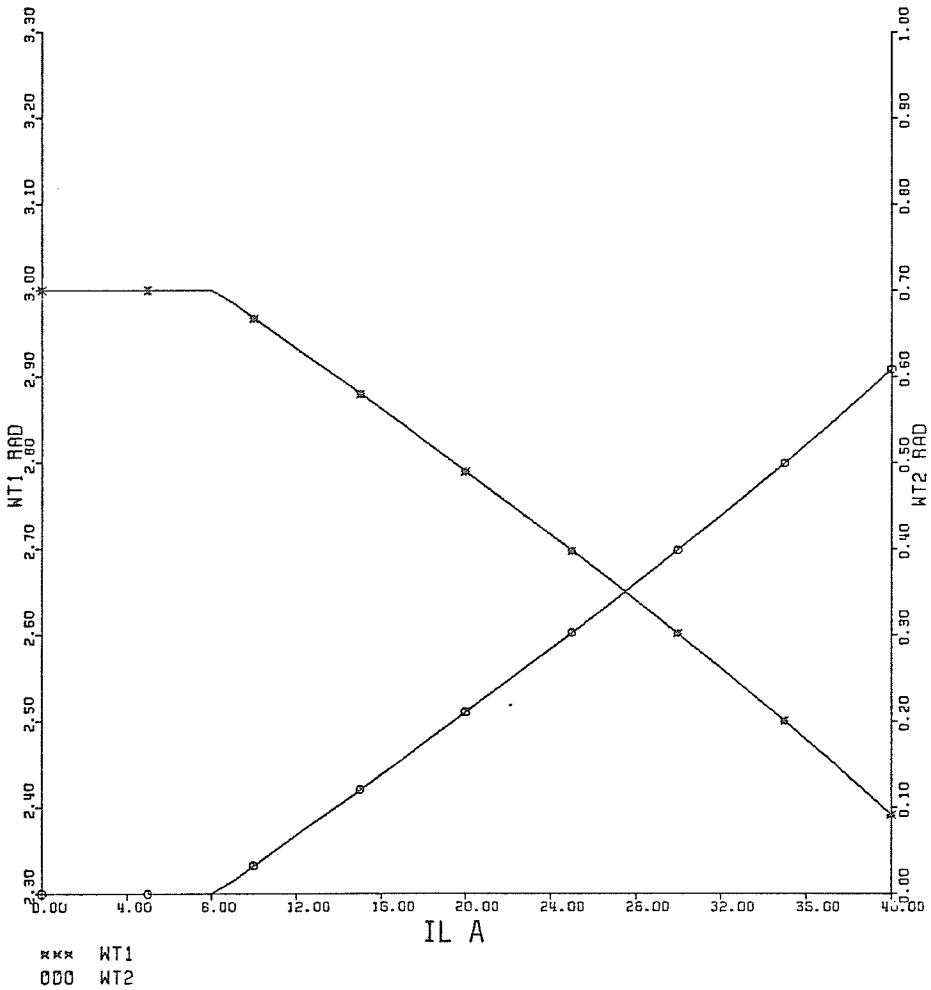


FIGURE 2.5 VARIATION OF WT1 & WT2 WITH LOAD CURRENT.

The importance of (ωt_1) and (ωt_2) lies in the fact that (ωt_1) affects the capacitor voltages at the beginning of the second transient, i.e., E_1' and E_2' given by equations (2.14) and (2.16) respectively. The angle (ωt_2) affects the final conditions of the second transient (initial conditions of the third transient). These conditions are obtained from equations (2.17) and (2.18) as

$$\left.\begin{aligned} E_1'' &= E_1' + (X\ I_L)\ \omega t_2 \\ E_2'' &= 2\ U_g - E_1'' = E_2' - (X\ I_L)\ \omega t_2 \end{aligned}\right\} \qquad (2.22)$$

as well as,

$$i_2 = I_L$$

The third transient, of duration t_3, of the commutation interval, is initiated by firing V2 at the end of duration $(\omega\tau)$.

The inverter circuit of Figure 2.1 is, then, equivalent to the circuit shown in Figure 2.6. Comparing Figures 2.3 and 2.6, equations (2.3) - (2.7) apply with,

$$E_o = 0 \quad , \quad I_i = I_L \quad , \quad E_i = - E_2'' \qquad (2.23)$$

giving,

$$i_2 = \left[\frac{E_2''}{X} \sin\omega t + I_L \cos\omega t\right] e^{-\omega t/2Q} \qquad (2.24)$$

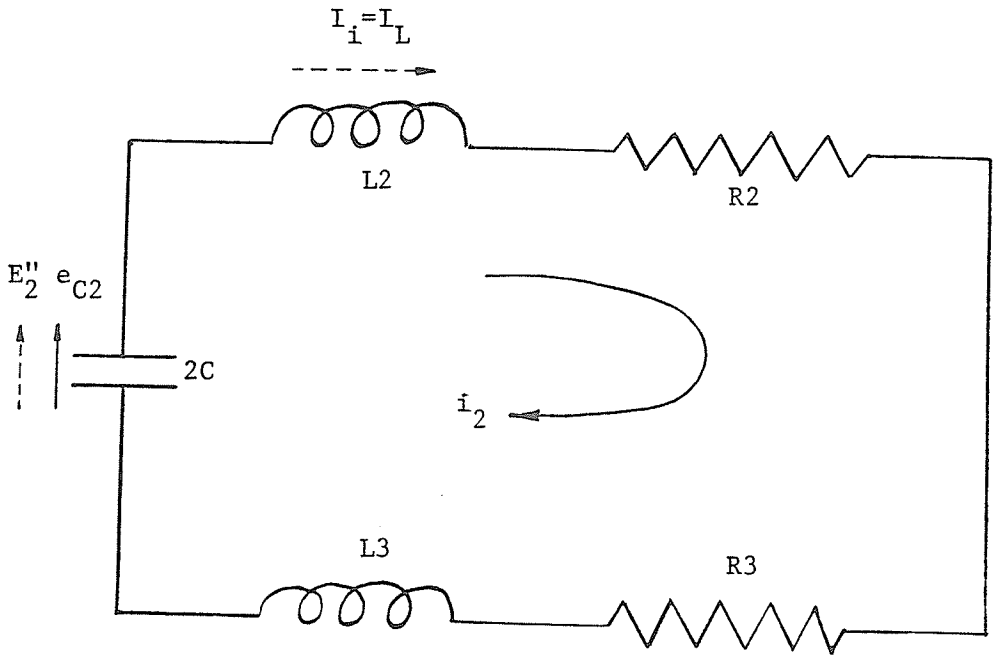


Figure 2.6 Equivalent circuit of Figure 2.1 during the third part of the commutation interval.
(L2=L3=L & R2=R3=R).

$$i_3 = I_L - i_2 \tag{2.25}$$

$$e_{C2} = [E''_2 \cos\omega t - X\ I_L \sin\omega t]\ e^{-\omega t/2Q} \tag{2.26}$$

$$e_{C1} = 2\ U_g - e_{C2} \quad . \tag{2.27}$$

The current i_2 builds up, as shown in Figure 2.2a, exceeding the load current and reaches a peak I_{P2} after time t_{P2}, then decreases to zero after time t_3 at the end of the commutation interval. The peak I_{P2} can be determined by setting the derivative of i_2 [equation (2.24)] with respect to time, equal to zero. Hence the time t_{P2} can be determined by:

$$\omega t_{P2} = \tan^{-1}\left[\frac{2QE''_2 - X\ I_L}{E''_2 + 2Q\ X\ I_L}\right] \quad , \ 0 < \omega t_{P2} \leq \frac{\Pi}{2} \quad . \tag{2.28}$$

Substituting for (ωt_{P2}) from equation (2.28) in equation (2.24), the peak I_{P2} can be determined.

The final conditions at the end of the commutation interval are determined by setting i_2 equal to zero in equation (2.24). Hence (ωt_3) is obtained as

$$\omega t_3 = -\tan^{-1}\left[\frac{X\ I_L}{E''_2}\right] \quad , \quad \frac{\Pi}{2} < \omega t_3 \leq \Pi \quad . \tag{2.29}$$

Substituting for the value of (ωt_3) from equation (2.29) in equations (2.26) and (2.27), the final voltages on the commutating capacitors C2 and C1, respectively, can be determined. Also, the

current i_3 is then equal to the load current which is carried by diode V4 Figure 2.1.

For a specified value of ($\omega\tau$) and by using euqation (2.29), the commutation time, T_C, can be found from:

$$\omega T_C = \omega\tau + \omega t_3 \quad . \tag{2.30}$$

Equations (2.24) - (2.30), describing the analysis of the commutation circuit during the last transient of the commutation interval, apply for values of load current in the range $I_{LO} < I_L \leq \hat{I}_L$, where $\hat{I}_L$ is the maximum load current that can be commutated and I_{LO} is given by equation (2.21).

The analysis of the commutation circuit with load current values in the range $-\hat{I}_L \leq I_L \leq I_{LO}$, can proceed as follows (Figures 2.7a and 2.7b).

The commutation interval, of duration T_C, consists of three parts or transients. The first transient, of duration $\omega\tau$, is identical to the first transient for the case of $I_{LO} < I_L \leq \hat{I}_L$. Therefore equations (2.8) - (2.11) apply. The final conditions of this transient are obtained as

$$\left.\begin{aligned} i_2(\omega\tau) &= I_{LO} = \frac{U_g}{X} e^{-\omega\tau/2Q} \sin\omega\tau \\ i_1(\omega\tau) &= I_L - i_2(\omega\tau) = I_L - I_{LO} \end{aligned}\right\} \tag{2.31}$$

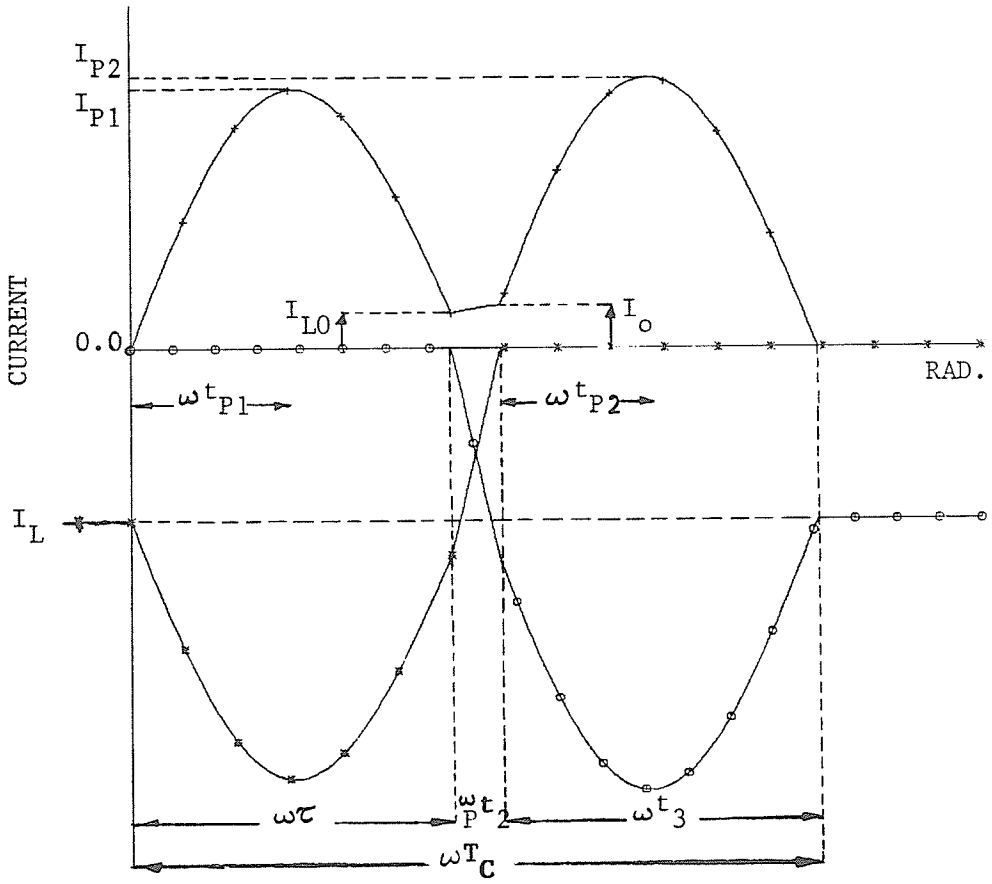
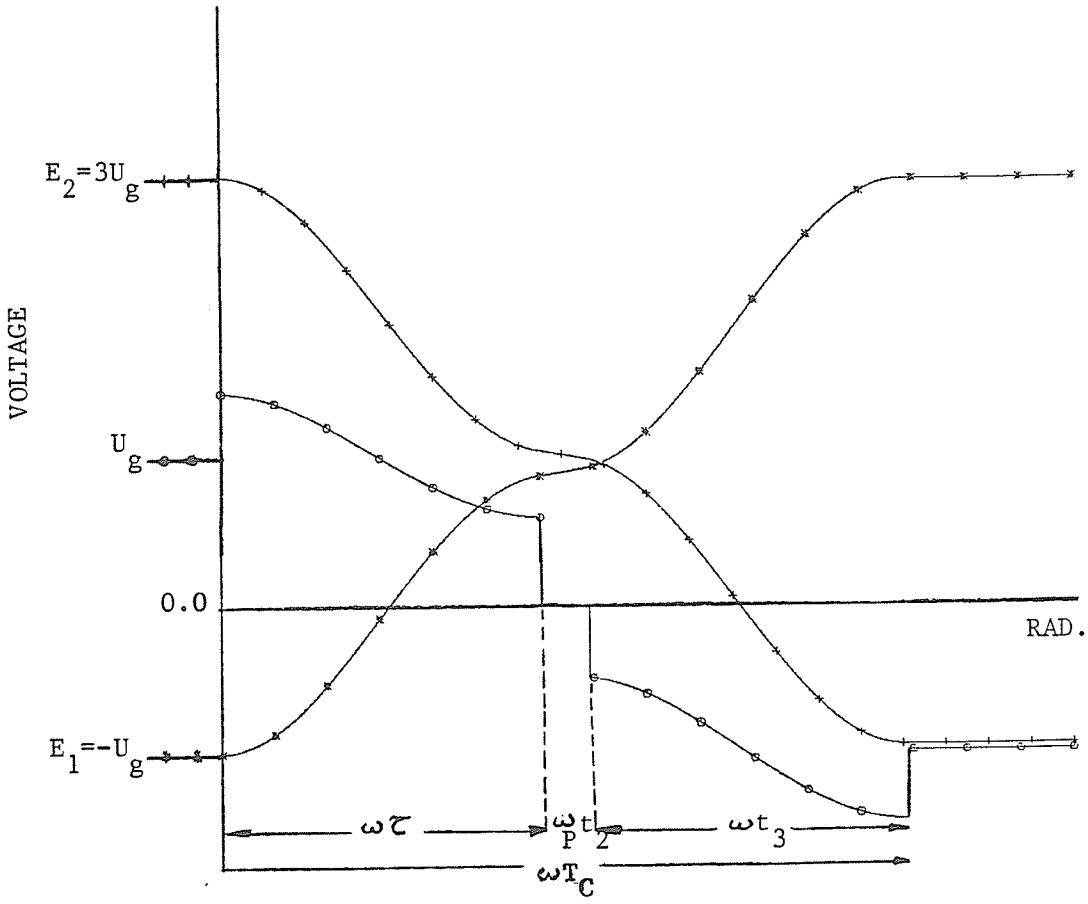


FIGURE 2.7A INVERTER OPERATION, WITH A NEGATIVE LOAD CURRENT (CURRENT WAVEFORMS).



xxx VOLTAGE ACROSS C1
+++ VOLTAGE ACROSS C2
ØØØ VOLTAGE OF POINT Z

FIGURE 2.7B INVERTER OPERATION, VOLTAGE WAVEFORMS.

$$\left.\begin{aligned} i_3(\omega\tau) &= 0 \\ e_{C1}(\omega\tau) &= -\,U_g\, e^{-\omega\tau/2Q}\cos\omega\tau \\ e_{C2}(\omega\tau) &= 2\,U_g - e_{C1}(\omega\tau) \quad . \end{aligned}\right\} \qquad (2.31)$$

At the end of the first transient, the main thyristor V2 is fired, and the second transient of duration t_2 is initiated. The equivalent circuit of the inverter during this transient is shown in Figure 2.8. The initial conditions of this stage are the final conditions of the first transient given by (2.31).

Three loop equations for the currents i_a, i_b and i_c, Figure 2.8, can be written taking into consideration that the initial values of these currents are:

$$i_{ao} = i_{bo} = I_{LO}/2$$

and

$$i_{co} = 0 \quad .$$

The three loop equations can be obtained as:

$$i_a\left(2SL + 2R + \frac{1}{SC}\right) + i_b\,(2SL + 2R) + i_c\,\left(SL + R + \frac{1}{SC}\right) = 2L\,I_{LO} - \frac{e_{C1}(\omega\tau)}{S}$$

$$i_a(2SL + 2R) + i_b\left(2SL + 2R + \frac{1}{SC}\right) + i_c\,(SL + R) = 2L\,I_{LO} - \frac{e_{C1}(\omega\tau)}{S}$$

$$i_a\left(SL + R + \frac{1}{SC}\right) + i_b\,(SL + R) + i_c\,\left(2SL + 2R + \frac{1}{SC}\right) = L\,I_{LO} + \frac{e_{C2}(\omega\tau)}{S}$$

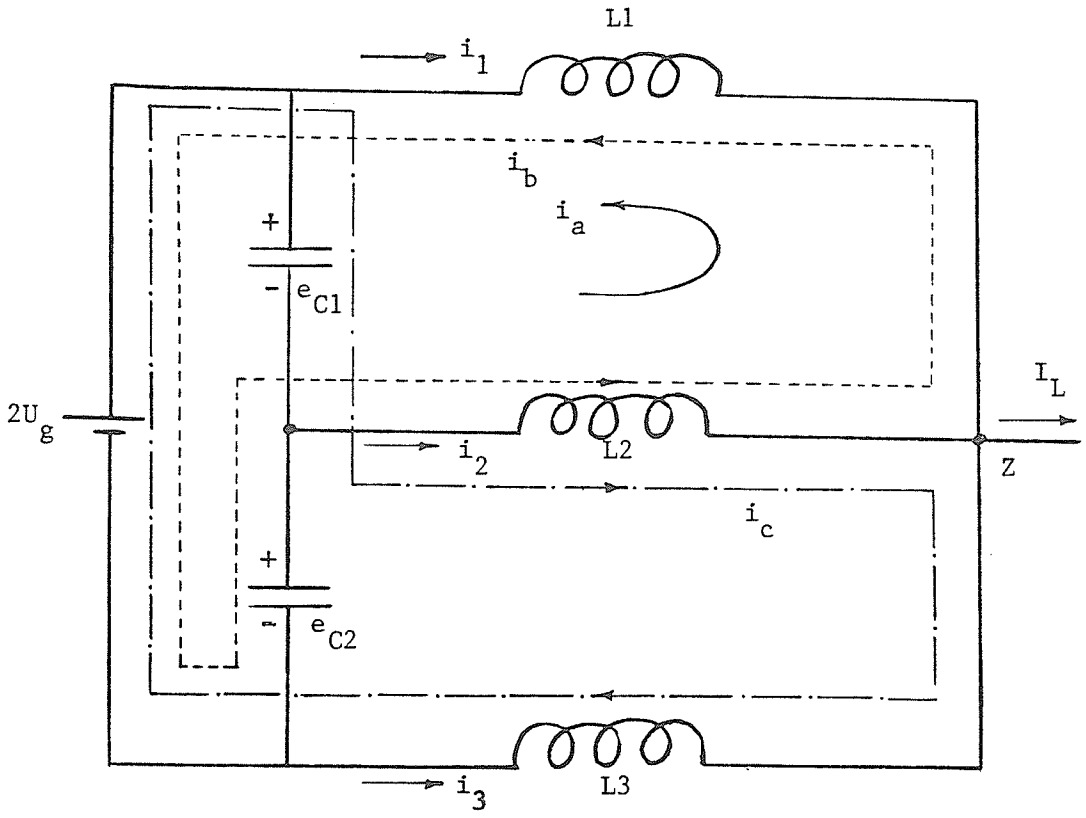


Figure 2.8 Equivalent circuit of Figure 2.1 during the second part of the commutation interval for $-\hat{I}_L \leq I_L \leq I_{LO}$. (L1=L2=L3=L & C1=C2=C).

Solving the above three loop equations in i_a, i_b and i_c and taking the inverse Laplace transforms yield,

$$\left.\begin{aligned} i_a &= -\frac{3Q_p}{X_p} U_g + \left(\frac{3Q_p}{X_p} U_g + \frac{I_{LO}}{2}\right) \exp\left(-\omega_p t/Q_p\right) \\ i_b &= A_1 \exp\left(-\omega_p t/2Q_p\right) \sin\left(\omega_p t+\theta_1\right) \\ i_c &= i_b = i_a \end{aligned}\right\} \qquad (2.32)$$

where,

$$\left.\begin{aligned} A_1 &= \sqrt{\left(\frac{U_g - e_{C1}(\omega\tau)}{3\omega_p L}\right)^2 + \left(\frac{I_{LO}}{2}\right)^2} \\ \theta_1 &= \sin^{-1}\left(\frac{I_{LO/2}}{A_1}\right) \\ \omega_p &= \frac{1}{\sqrt{3LC}} \\ X_p &= 3\omega_p L = \frac{1}{\omega_p C} = \sqrt{\frac{3L}{C}} \\ Q_p &= \frac{\omega_p L}{R} = \frac{X_p}{3R} \end{aligned}\right\} \qquad (2.33)$$

The branch currents i_1, i_2 and i_3, Figure 2.8, are then obtained from:

$$i_1 = I_L - (i_a + i_b)$$
$$= I_L + \frac{3Q_p}{X_p} U_g - (\frac{3Q_p}{X_p} U_g + \frac{I_{LO}}{2}) \exp(-\omega_p t/Q_p)$$
$$- A_1 \exp(-\omega_p t/2Q_p) \sin(\omega_p t + \theta_1) \quad (2.34)$$

$$i_2 = i_a + i_b + i_c$$
$$= 2A_1 \exp(-\omega_p t/2Q_p) \sin(\omega_p t + \theta_1) \quad (2.35)$$

$$i_3 = -i_c$$
$$= -\frac{3Q_p}{X_p} U_g + (\frac{3Q_p}{X_p} U_g + \frac{I_{LO}}{2}) \exp(-\omega_p t/Q_p)$$
$$- A_1 \exp(-\omega_p t/2Q_p) \sin(\omega_p t + \theta_1) \quad . \quad (2.36)$$

Consequently, the capacitor voltages can be found as

$$e_{C1} = U_g - X_p A_1 \exp(-\omega_p t/2Q_p) \cos(\omega_p t + \theta_1) \quad (2.37)$$

$$e_{C2} = 2U_g - e_{C1} = U_g + X_p A_1 (-\omega_p t/2Q_p) \cos(\omega_p t + \theta_1) \quad . \quad (2.38)$$

The second transient, of duration t_2, is terminated when i_1 is reduced to zero. The angle $\omega_p t_2$ can be found by solving equation (2.34) with the left-hand-side set to zero. Substituting for $\omega_p t_2$ in equations (2.34) - (2.38), the final conditions of the second transient can be obtained as:

$$
\left.
\begin{aligned}
& i_1\ (\omega_p t_2) = 0 \\
& i_2\ (\omega_p t_2) = I_o = 2\ A_1\ \exp\ (-\omega_p t_2/2Q_p)\ \sin\ (\omega_p t_2 + \theta_1) \\
& i_3\ (\omega_p t_2) = I_L - i_2\ (\omega_p t_2) \\
& e_{C1}\ (\omega_p t_2) = U_g - X_p\ A_1\ \exp\ (-\omega_p t_2/2Q_p)\ \cos\ (\omega_p t_2 + \theta_1) \\
& e_{C2}\ (\omega_p t_2) = U_g + X_p\ A_1\ \exp\ (-\omega_p t_2/2Q_p)\ \cos\ (\omega_p t_2 + \theta_1)
\end{aligned}
\right\} \qquad (2.39)
$$

Comparing the expressions for ω and ω_p given by equations (2.4) and (2.33) respectively, it can be seen that the resonant frequency of the commutation circuit during the second transient differs from that during the first transient.

Once i_1 is reduced to zero, the third (final) transient, of duration t_3, of the commutation interval, is initiated. The equivalent circuit of the inverter will be as shown in Figure 2.9. The initial conditions of this transient are the final conditions of the second transient given by (2.39). It can easily be shown from Figure 2.9 that,

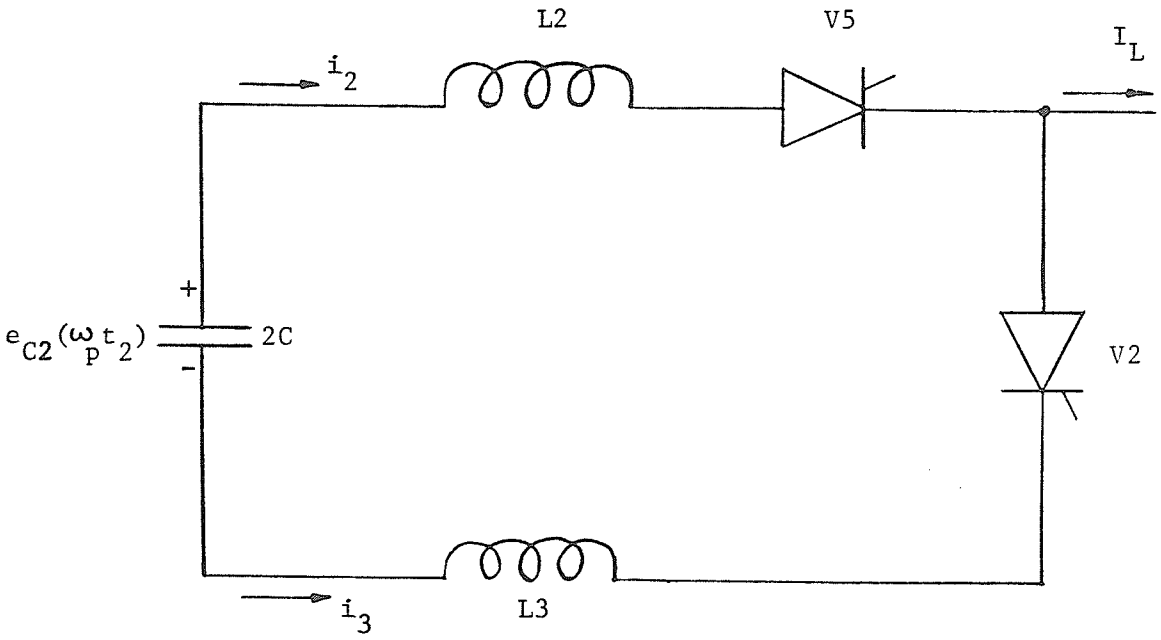


Figure 2.9 Equivalent circuit of Figure 2.1 during the third part of the commutation interval for $-\hat{I}_L \leq I_L \leq I_{LO}$. (L2=L3=L).

$$
\left.
\begin{aligned}
i_2 &= A_2 e^{-\omega t/2Q} \sin(\omega t + \theta_2) \\
i_3 &= I_L - i_2 = I_L - A_2 e^{-\omega t/2Q} \sin(\omega t + \theta_2) \\
e_{C2} &= X\, A_2 e^{-\omega t/2Q} \cos(\omega t + \theta_2) \\
e_{C1} &= 2\, U_g - e_{C2}
\end{aligned}
\right\} \qquad (2.40)
$$

where,

$$
\left.
\begin{aligned}
A_2 &= \sqrt{\left(\frac{e_{C2}\ (\omega_p t_2)}{X}\right)^2 + I_o^2} \\
\theta_2 &= \sin^{-1}\left(\frac{I_o}{A_2}\right)
\end{aligned}
\right\} \qquad . \qquad (2.41)
$$

The current i_2 builds up and reaches a peak I_{p2} after time t_{p2}. The angle ωt_{p2} can be found by setting the derivative of i_2, equation (2.40), equal to zero, giving

$$
\omega t_{p2} = \tan^{-1}(2Q) - \theta_2 \qquad . \qquad (2.42)
$$

The final conditions at the end of the commutation interval are determined by setting i_2 equal to zero in equation (2.40). Hence (ωt_3) is obtained as

$$\omega t_3 = \Pi - \theta_2 \quad . \tag{2.42}$$

Substituting for (ωt_3) from equation (2.42) in equation (2.40), the final voltages on the commutating capacitors C1 and C2 can be determined. Also the current i_3 is then equal to the load current I_L.

For a specified value of $\omega\tau$, the commutation time, T_C, is obtained as

$$T_C = \frac{\omega\tau}{\omega} + \frac{\omega_p t_2}{\omega_p} + \frac{\omega t_3}{\omega} \quad . \tag{2.43}$$

Figures 2.10 - 2.15 show details of the commutation interval for different values of load current I_L. The Figures are plotted for the parameters specified by (2.20).

2.4 Selection of the Optimum Commutating Capacitors and Inductors

To achieve adequate commutation under the conditions depicted in Figure 2.2, the commutating current, i_2, must exceed the load current, I_L, for an interval, t_o, which is longer than the turn-off time of the thyristor. Another constraint on selecting C and L, is that the energy provided by the commutating circuit, in order to turn-off the main thyristor V1, has to be minimum.

Using the optimum values of C and L given by [6], the optimum values of C and L of the inverter of Figure 2.1, which satisfy the above constraints, are given by

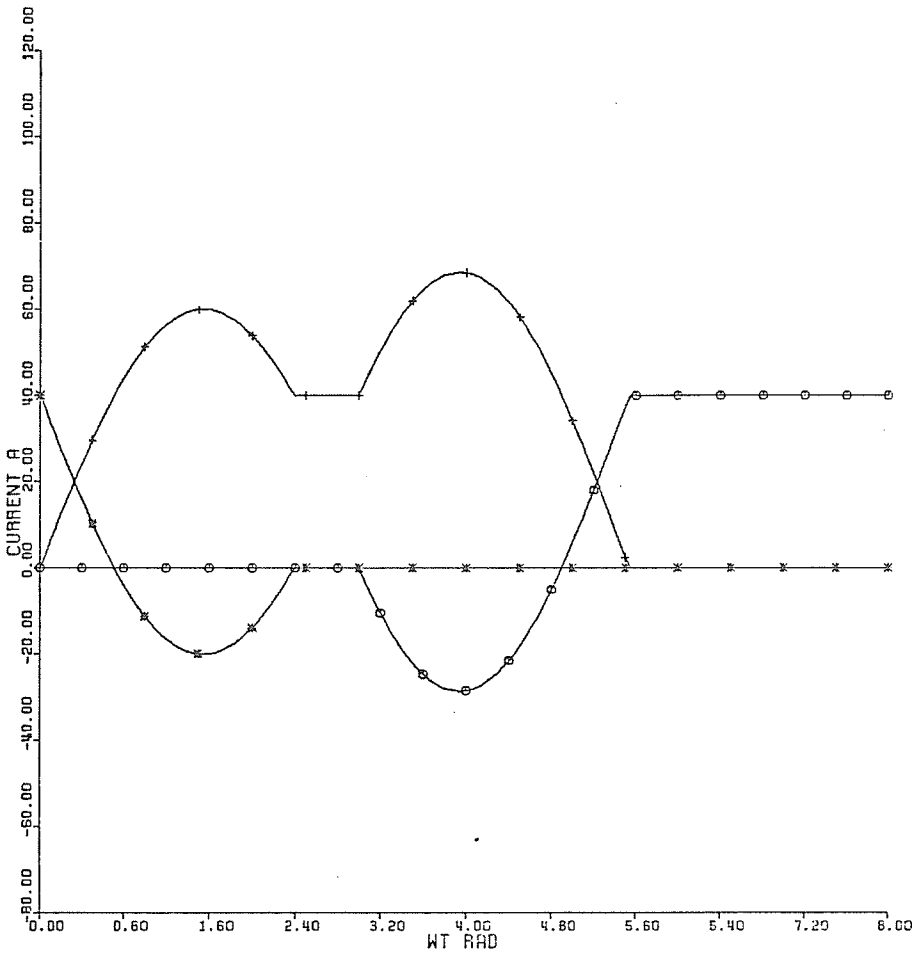


FIGURE 2.10A CURRENT WAVEFORMS WITH IL=+IL MAX.

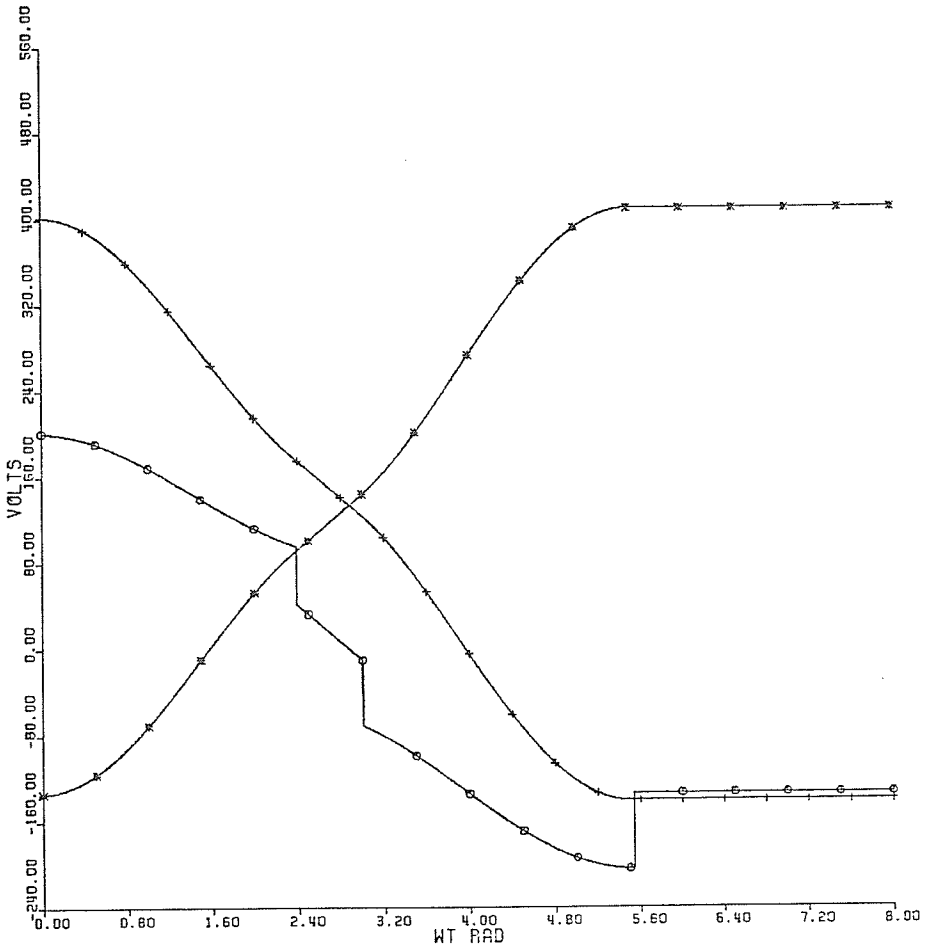


FIGURE 2.10B VOLTAGE WAVEFORMS WITH IL=IL MAX.

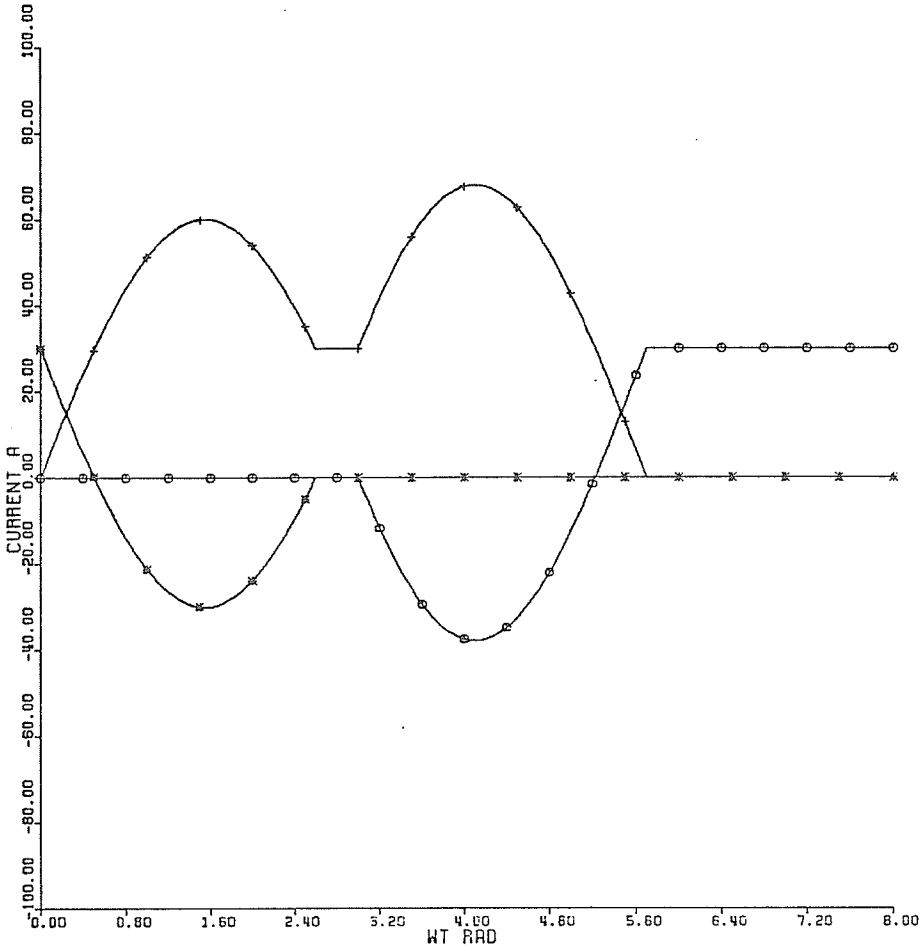


FIGURE 2.11A CURRENT WAVEFORMS WITH IL=30 A

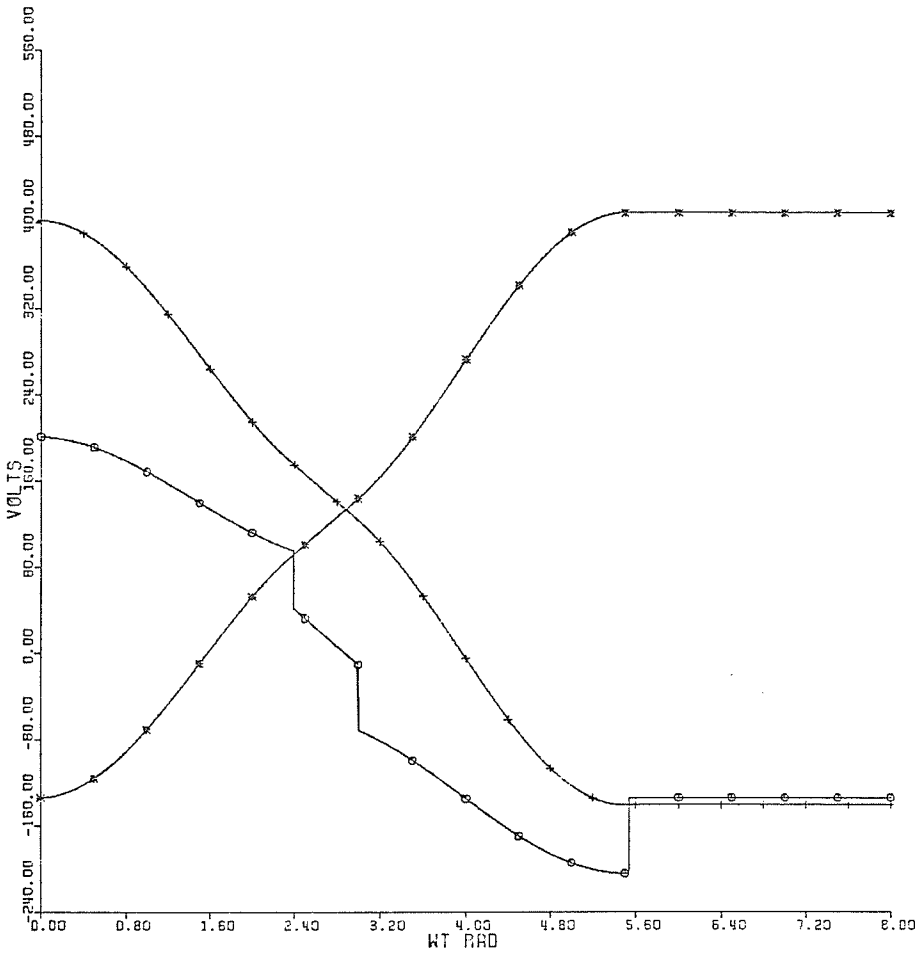


FIGURE 2.11B VOLTAGE WAVEFORMS WITH IL=30 A

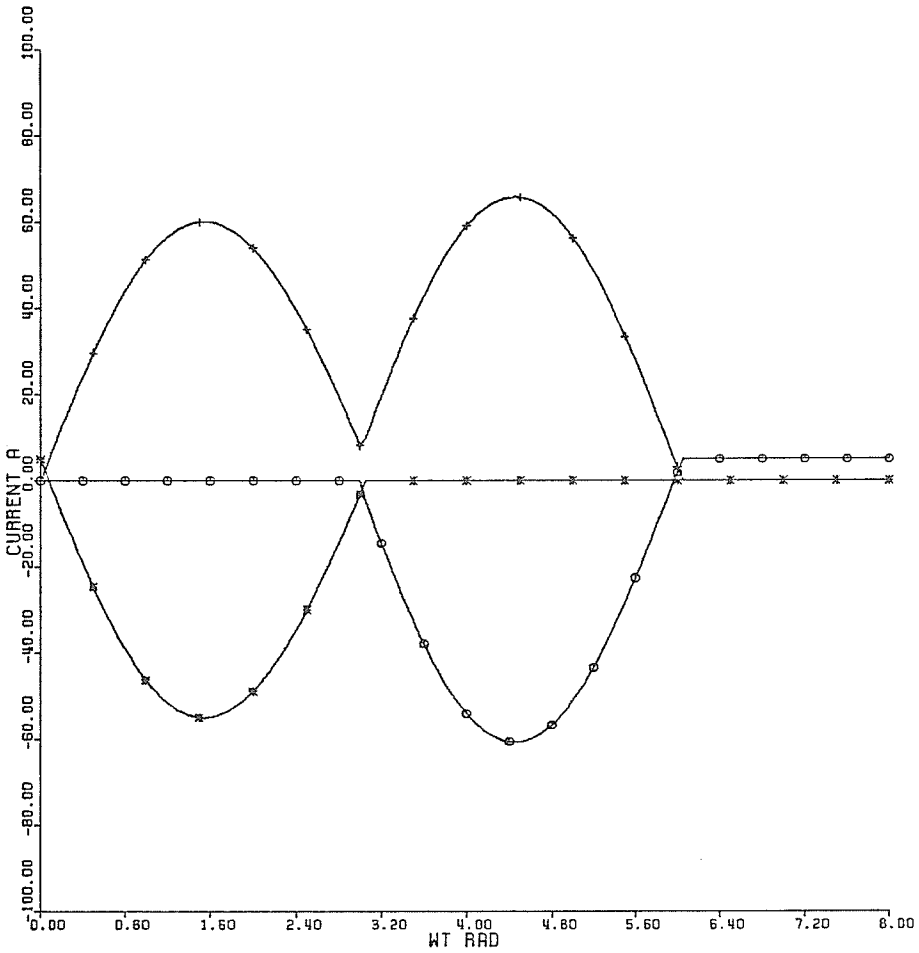


FIGURE 2.12A CURRENT WAVEFORMS WITH IL=5 A

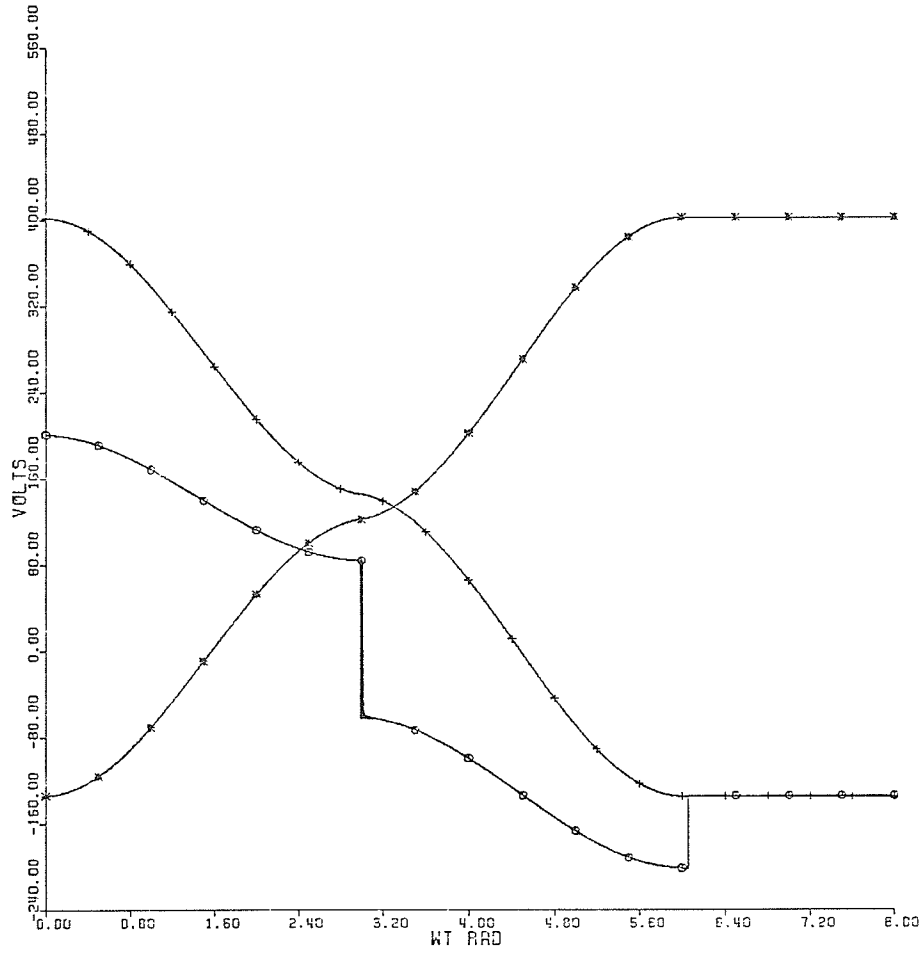


FIGURE 2.12B VOLTAGE WAVEFORMS WITH IL=5 A

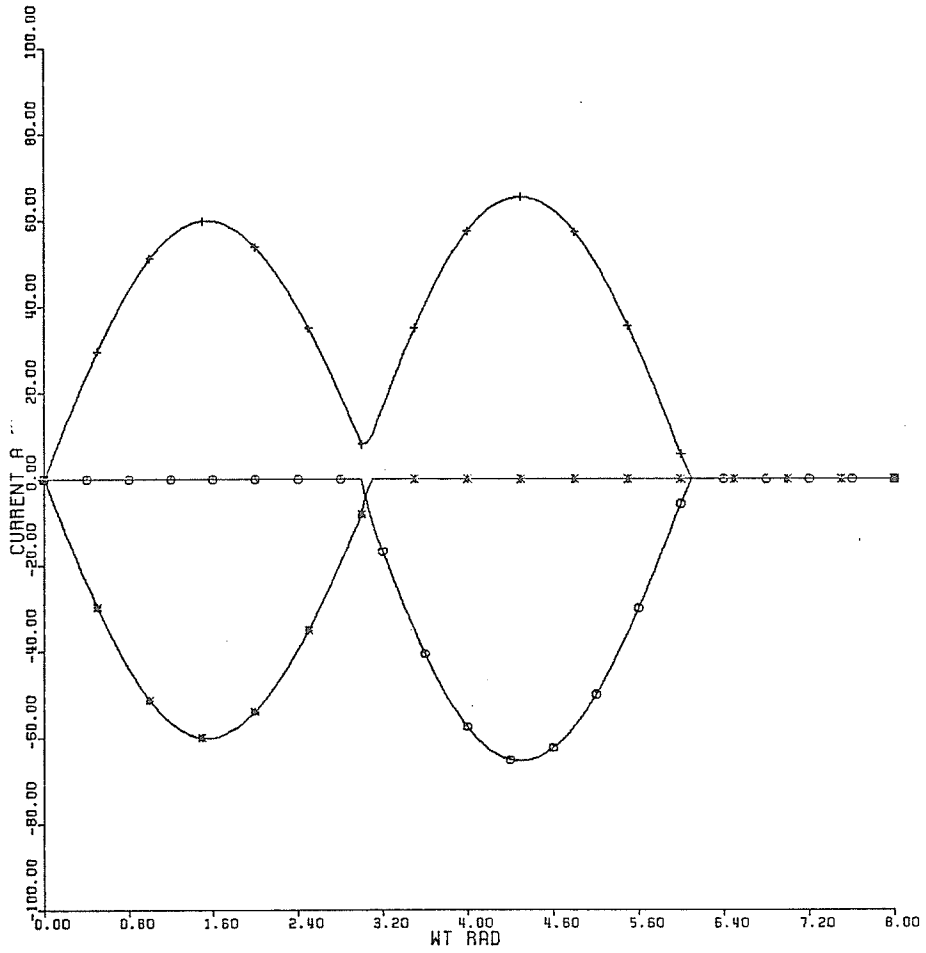


FIGURE 2.13A CURRENT WAVEFORMS WITH NO LOAD.

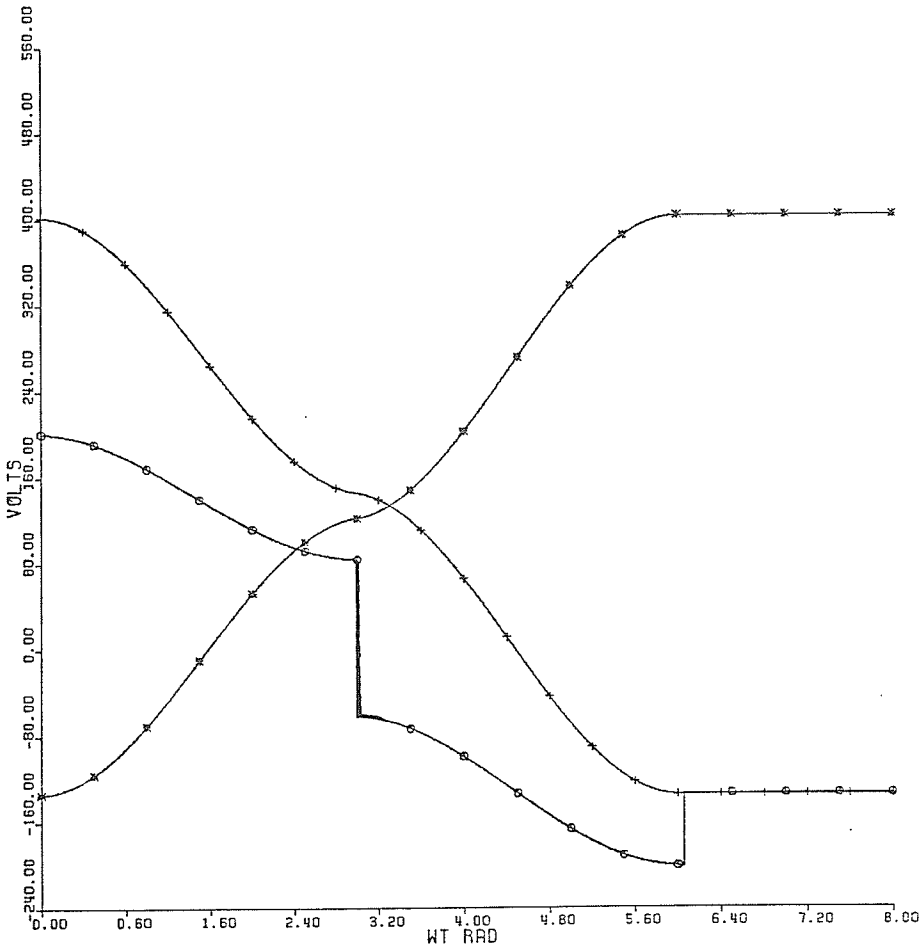


FIGURE 2.13B VOLTAGE WAVEFORMS WITH NO LOAD.

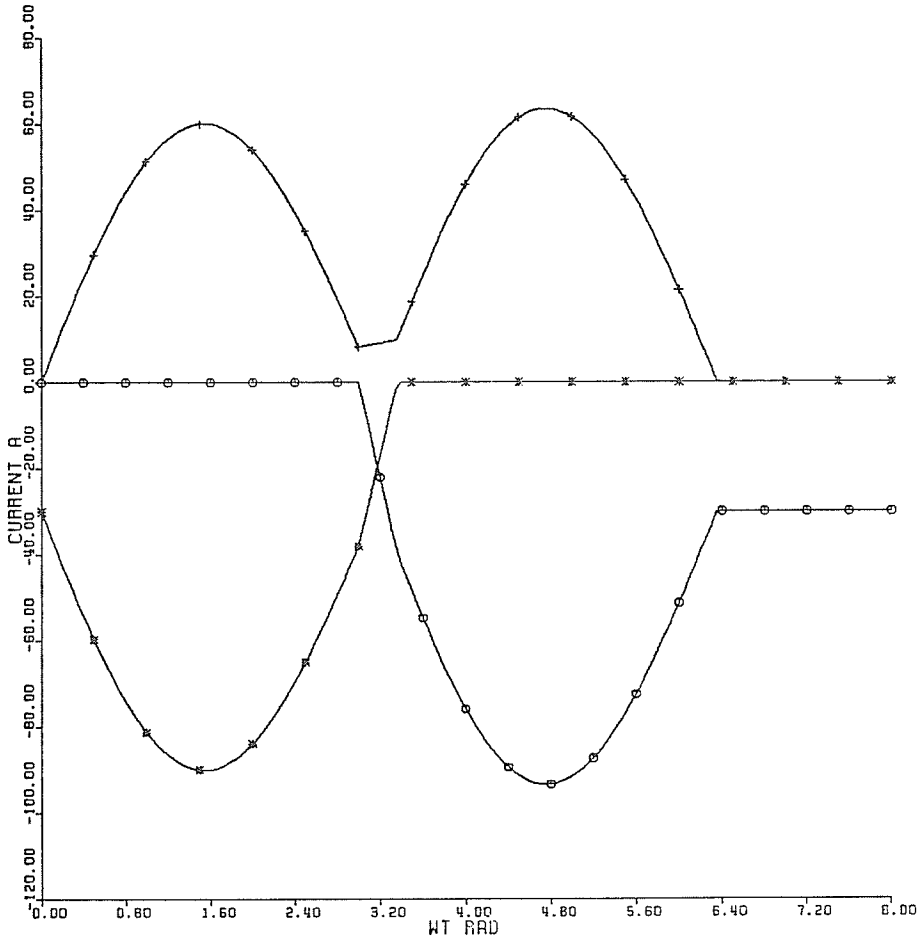


FIGURE 2.14A CURRENT WAVEFORMS WITH IL=-30 A

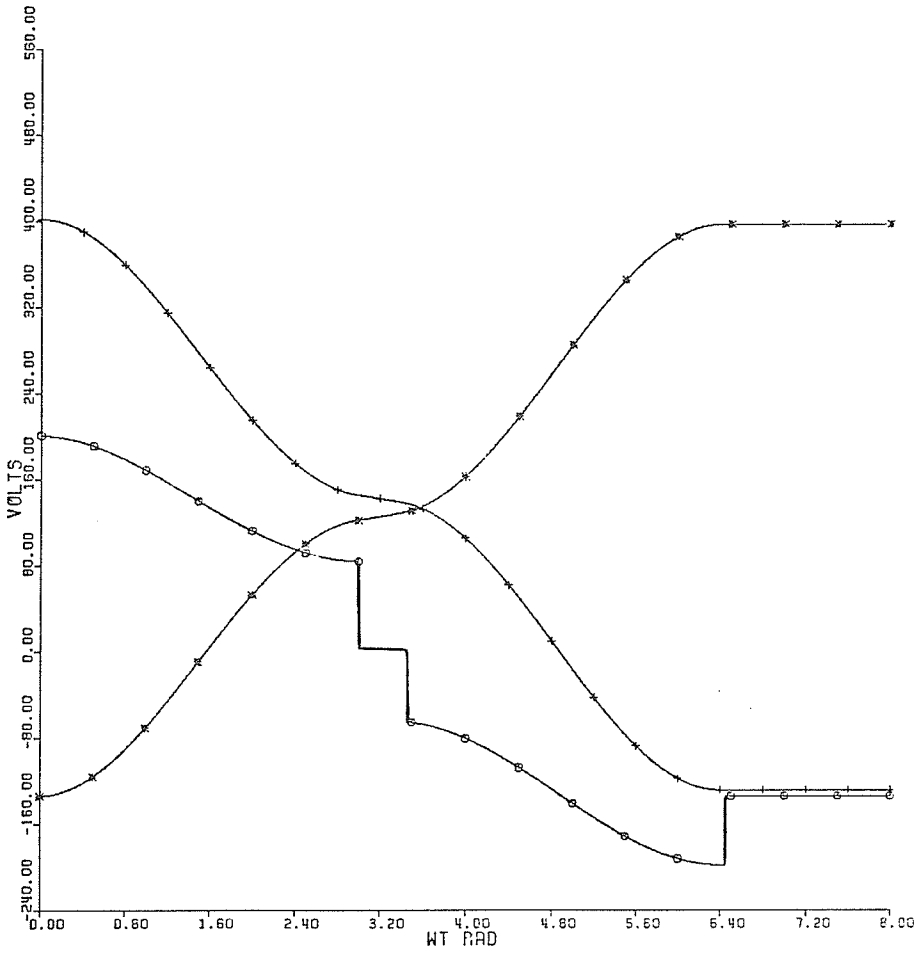


FIGURE 2.14B VOLTAGE WAVEFORMS WITH IL=-30 A

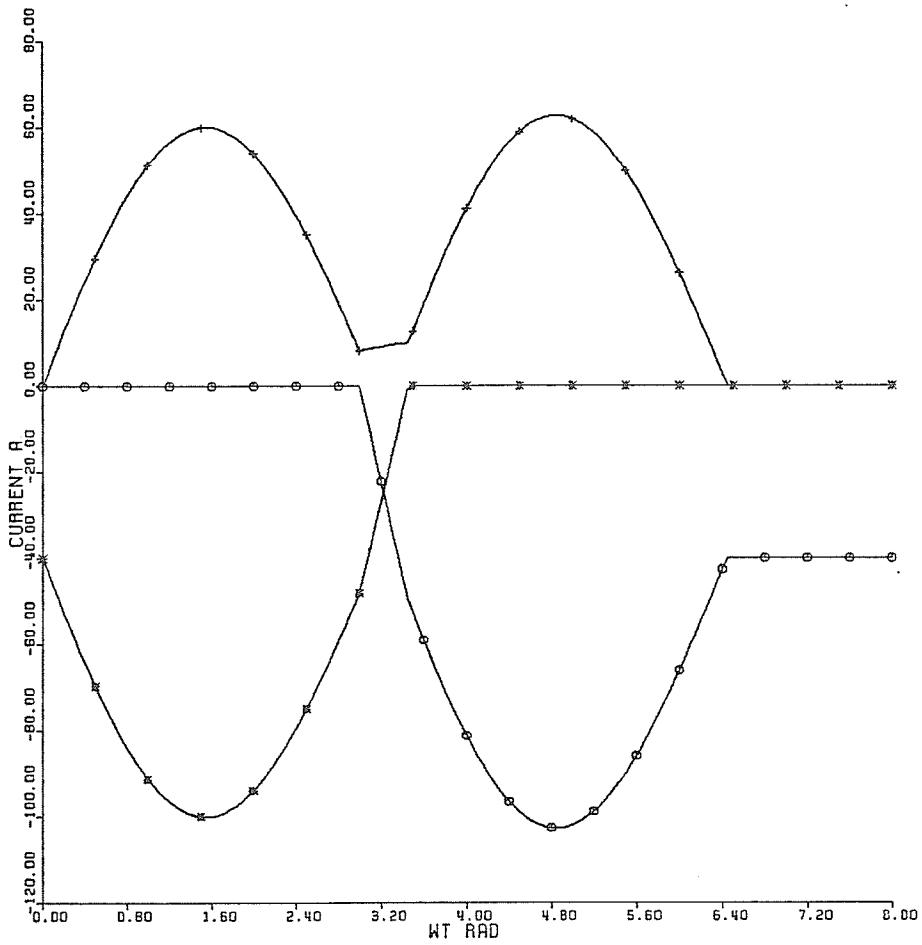


FIGURE 2.15A CURRENT WAVEFORMS WITH IL=-IL MAX.

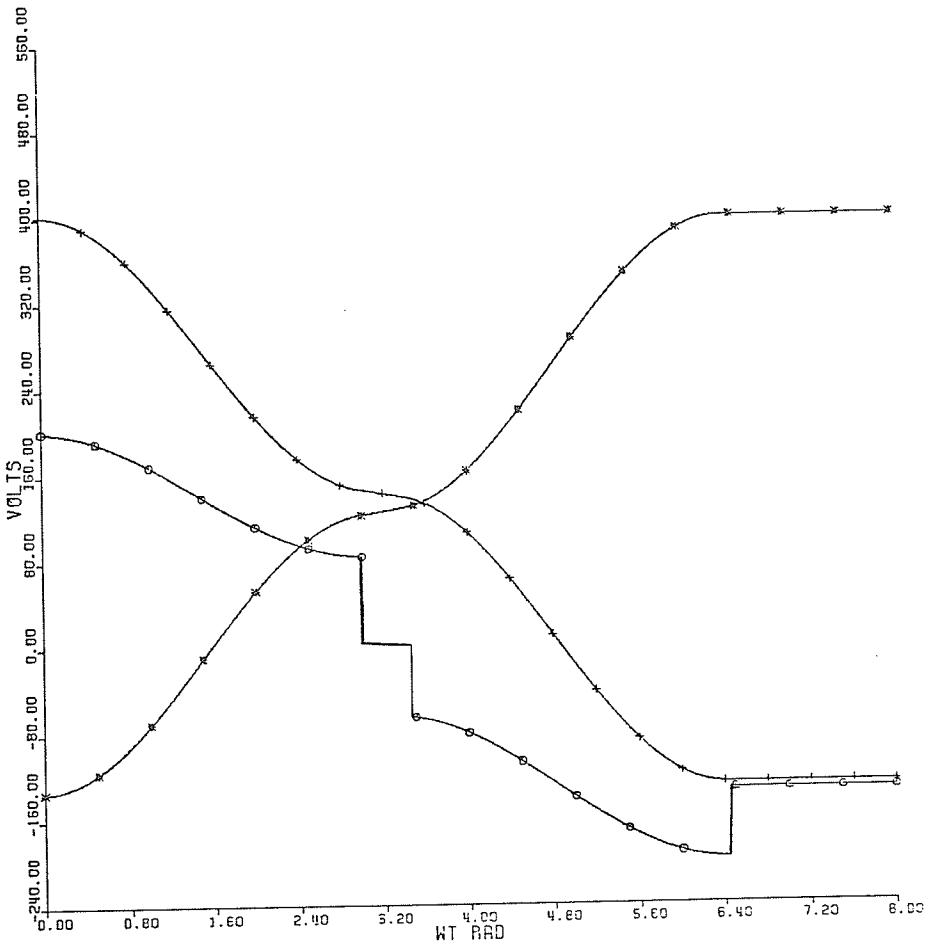


FIGURE 2.15B VOLTAGE WAVEFORMS WITH IL=-IL MAX.

$$C = \frac{0.893}{2} \cdot \frac{\hat{I}_L}{U_g\, e^{-\pi/4Q}} \cdot t_{off} \quad F. \tag{2.44}$$

$$L = \frac{0.397}{2} \cdot \frac{U_g\, e^{-\pi/4Q}}{\hat{I}_L} \cdot t_{off} \quad H. \tag{2.45}$$

where,

$\hat{I}_L$ is the maximum load current (A)

U_g is half the dc supply voltage (V)

t_{off} is the turn-off time of the Thyristor in seconds

Q is the quality factor

The factor $e^{-\pi/4Q}$ appears in equations (2.44) and (2.45) to allow for losses in the commutation circuit.

The values of C and L given by equations (2.44) and (2.45) respectively, result in a peak (I_{p1}) of the commutating current i_2 (Figure 2.2a), which is equal to 1.5 times the maximum load current ($\hat{I}_L$).

2.5 Inductor Design

The commutating inductors of the inverter Figure 2.1, were selected to be air cored and each having the configuration shown in Figure 2.16, where r is the turn radius, D is the average diameter of the toroid and N is the number of turns.

The inductance L of the toroid of Figure 2.16, is given by

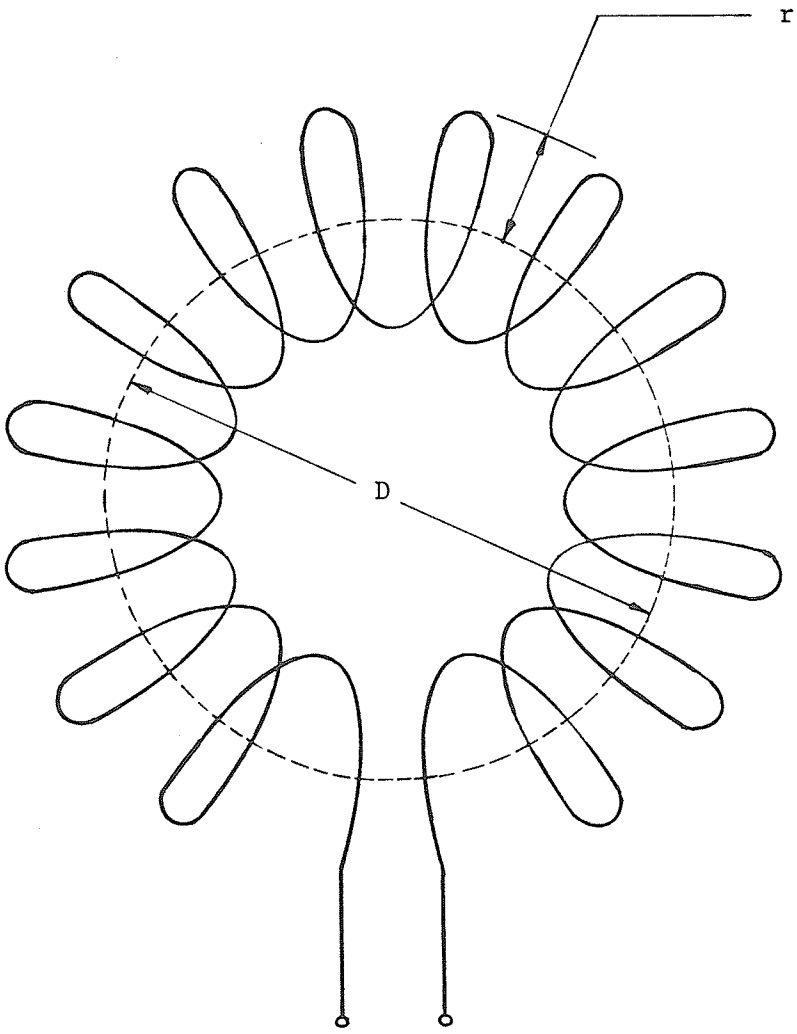


Figure 2.16 Toroid Configuration.

$$L = \mu_o \frac{N^2 r^2}{D} \quad \text{H.}$$

where, r and D in meters and μ_o is the free-space permeability and has the numerical vlaue of $4\pi \times 10^{-7}$ H/m.

Setting the ratio of D to r equal to k (k > 1), L is then obtained as

$$L = \mu_o \frac{N^2 r}{k} \quad .$$

Hence

$$r = \frac{kL}{\mu_o N^2} \quad \text{meters} \quad . \tag{2.46}$$

The resistance R of the inductor is given by

$$R = 2\pi r N \frac{\rho}{1000} \quad \text{ohms}$$

where, ρ is the wire resistance per 1000 ft and r in ft.

But, $R = \frac{X}{2Q}$ [equations (2.4) and (2.7)] .

Therefore,

$$\frac{X}{2Q} = 2\pi r N \frac{\rho}{1000} \quad .$$

Hence,

$$r = \frac{1000X}{4\pi N\rho Q} \quad \text{ft}$$

or

$$r = \frac{1000X}{4\pi(3.281)N\rho Q} \quad \text{meters}, \tag{2.47}$$

ρ in ohms/1000 ft.

The number of turns N can, then, be obtained from equations (2.46) and (2.47) as:

$$N = 0.033\,\frac{k\rho LQ}{X} \quad \text{turns} \tag{2.48}$$

where, L in (μH.), ρ in (ohms/1000 ft) and X in (ohms).

Once N is determined by equation (2.48), the turn radius r can be found from equation (2.46) as

$$r = 0.796\,\frac{kL}{N^2} \quad \text{meters} \tag{2.49}$$

where, L in μH.

CHAPTER III

OPTIMUM PWM STRATEGY FOR SPEED CONTROL OF PUMPS AND FANS

3.1 Basic Principle of Three-Phase PWM Inverter

The basic inverter circuit used to supply a three-phase induction motor is shown in Figure 3.1. The circuit consists of six switching elements which are located between the dc bus and the load.

An analysis can be made of this circuit by conceptually representing the output stage by the set of single-pole double-throw switches shown in Figure 3.2. Through the proper activation of the switches, the fixed dc link voltage is applied for short time intervals with either polarity across the motor terminals, in such a way as to result in a fundamental output voltage of adjustable magnitude and frequency. The set of rules determining the sequence and the timing of the switch activations is termed the modulation policy or the switching pattern. The indicated switches are sequenced to give a 120° phase displacement between the three phases.

A periodic waveform, as shown in Figure 3.3, is assumed for the output voltage of pole A of the inverter with respect to a theoretical dc neutral "o" (Figure 3.2). The waveform has quarter-wave symmetry with the angles α_i, with i = 1, 2, 3,....., M, given as:

$$0 \leq \alpha_1 \leq \alpha_2 \leq \alpha_3 \leq \ldots. \leq \alpha_M \leq \frac{\pi}{2} \quad . \tag{3.1}$$

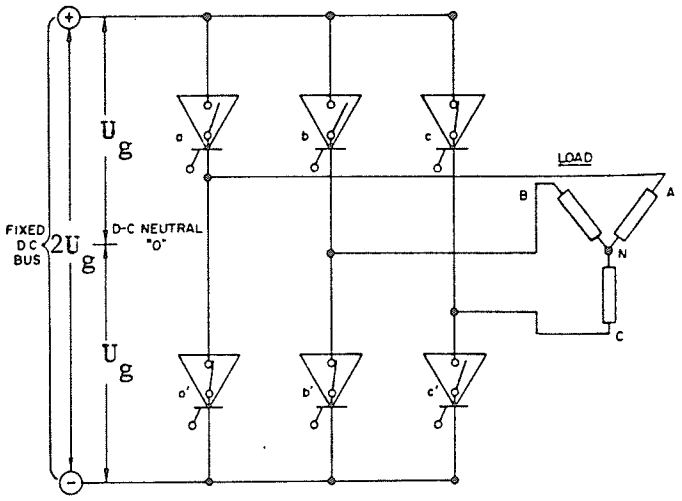


Figure 3.1 Basic Three-Phase Inverter With Motor Load.

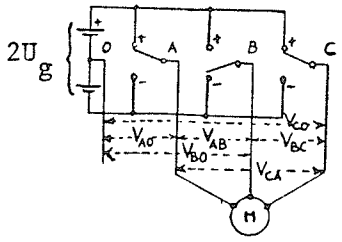


Figure 3.2 Conceptual Diagram Of A PWM Inverter Motor Drive.

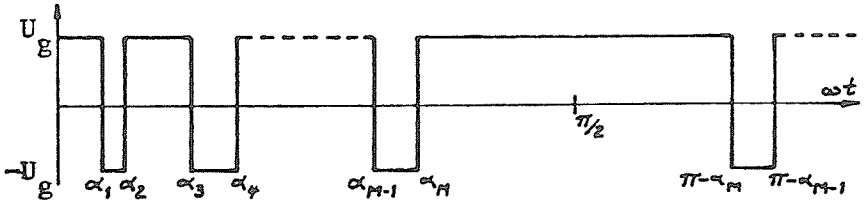


Figure 3.3 Single-Pole Output Voltage Waveform.

The waveform of Figure 3.3 has obviously only odd harmonics. Hence the instantaneous output voltage expressed as a Fourier series of odd harmonics, is given by:

$$v_{AO} = \sum_{n=1}^{\infty} V_n \sin(n\omega t) \tag{3.2}$$

where,

$$V_n = \frac{4\, U_{g/\pi}}{n} \left[1 - 2 \sum_{i=1}^{M} (-1)^{i+1} \cos(n\alpha_i)\right] \quad . \tag{3.3}$$

Since the voltages v_{AO}, v_{BO} and v_{CO}, of poles A, B and C respectively, are displaced 120° apart, it can be easily shown that the phase voltage v_{AN} is given by:

$$v_{AN} = \sum_{n=1,5,7,11...}^{\infty} V_n \sin(n\omega t) \tag{3.4}$$

where V_n is given by equation (3.3). Hence the triplen harmonics are missing in the phase voltage.

It can, also, be shown that the line to line voltages are given by:

$$\left.\begin{aligned} v_{AB} &= \sqrt{3} \sum_{n=1,5,7,11,...}^{\infty} V_n \sin n(\omega t + 30°) \\ v_{BC} &= \sqrt{3} \sum_{n=1,5,7,11,...}^{\infty} V_n \sin\ n(\omega t° - 90°) \\ v_{CA} &= \sqrt{3} \sum_{n=1,5,7,...}^{\infty} V_n \sin n(\omega t + 150°) \end{aligned}\right\} \tag{3.5}$$

3.2 Load Current

The inverter load is a three-phase squirrel cage induction motor, Y - connected with neutral not connected. In the following discussion, per phase analysis is considered taking into consideration that the three-phase voltages are displaced 120° apart.

The impressed line-to-neutral voltage is given by equation (3.4). Analysis of the performance of the motor can proceed as if there were a series of independent generators all connected in series supplying the motor as shown in Figure 3.4.

Equation (3.4) represents the voltage waveform most frequently encountered with three-phase induction motors. It does not contain any even harmonics or triplen harmonics. Neglecting saturation, the principle of superposition holds, and the current produced by each harmonic is independent of the others.

Clearly, if the fundamental system, n=1, is of positive phase sequence, the following systems exist for the harmonics:

(1) Positive sequence = n=7, 13, 19, 25, ...

(2) Negative sequence = n=5, 11, 17, 23, ...

The equivalent circuit for the harmonics can be derived directly from the well known equivalent circuit for the fundamental shown in Figure 3.5. If the slip for the fundamental is s, then the slip for the nth. harmonic, depending on phase sequence, is given by:

$$\text{Positive sequence} = \frac{n-1+s}{n}$$

$$\text{Negative sequence} = \frac{n+1+s}{n} \quad .$$

Since these expressions for the harmonic slip give a value approximately equal to 1, the resistive component of the equivalent circuit for the harmonics is small if skin effect is neglected. Also, the magnetizing reactance is shunted by the secondary leakage, and hence it is also negligible. Thus, for both positive and negative sequence harmonics, the equivalent circuit is shown in Figure 3.6 [7].

From the equivalent circuits, Figures 3.5 and 3.6, the following expressions for the currents are obtained [7]:

Fundamental peak current:

$$\hat{I}_1 = \frac{V_1}{|Z_o|} \tag{3.6}$$

where,

$$Z_o = R_1 + j\,X_1 + \frac{(R_2/s)\,X_m^2 + j\,X_m\,[(R_2/s)^2 + X_2(X_2 + X_m)]}{(R_2/s)^2 + (X_2 + X_m)^2}$$

$$\cos\phi_1 = \frac{\mathrm{Re}(Z_o)}{|Z_o|} \triangleq \text{Fundamental power factor} \; .$$

Positive and negative sequence peak harmonic currents:

$$\hat{I}_n = \frac{V_n}{n\omega L} \quad , \quad n=5,\ 7,\ 11,\ 13,\ \ldots \tag{3.7}$$

$\cos\phi = 0 \triangleq$ Harmonic power factor (lagging).

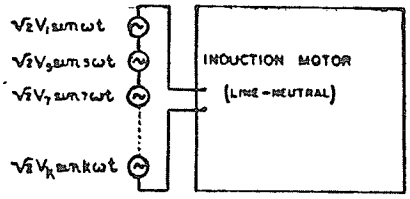


Figure 3.4 Nonsinusoidal Excitation Of Induction Motor (Per Phase.)

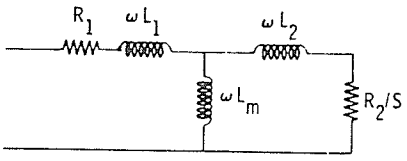


Figure 3.5 Fundamental Equivalent Circuit.

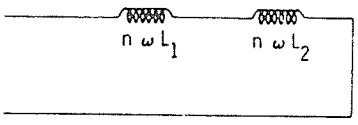


Figure 3.6 Equivalent Circuit Of Positive And Negative Sequences.

where, $L = L_1 + L_2 \triangleq$ leakage inductance,

$\omega \triangleq$ the fundamental angular frequency

$V_1, V_5, V_7, V_{11}, \ldots$ are given by equation (3.3).

The total rms harmonic current is given by:

$$I = \sqrt{\frac{1}{2} \sum_{n=5,7,11,13,\ldots}^{\infty} \hat{I}_n^2} \quad .$$

Then, from equation (3.7), I is obtained as:

$$I = \frac{1}{\sqrt{2}\,\omega L} \cdot \sqrt{\sum_{n=5,7,11,13,\ldots}^{\infty} \left(\frac{V_n}{n}\right)^2} \quad . \qquad (3.8)$$

3.3 Voltage Control and Harmonics in a PWM Inverter

3.3.1 Existing techniques

In recent years, a number of PWM techniques have been suggested to control the magnitude of the fundamental of the inverter output voltage as well as to reduce the harmonics generated.

In the elimination technique [8] and [9], a fixed number of harmonics can be eliminated and the higher harmonics that are in the output are attenuated by an output filter circuit. Control of the fundamental voltage amplitude is possible if a single degree of freedom is introduced in the problem; thus, in order to eliminate M harmonics

and at the same time control the fundamental component, (M+1) variables (switchings) are needed. With the degree of freedom introduced, it is possible to vary the output voltage fundamental amplitude from a maximum value to zero continuously while eliminating the M specified harmonics.

In the minimization technique [10], the switching pattern is chosen so that the fundamental voltage is controlled and the total rms harmonic current is minimized.

In the subharmonic technique [11], the switching instants are readily determined by conventional analog circuitry in which a high-frequency triangular carrier wave is compared with a sinusoidal reference signal at the desired fundamental output frequency. The intersections of the two waveforms determine the switching instants in the PWM wave. In this technique, the fundamental output voltage is limited. If the modulator is saturated, by increasing the modulation index (ratio of sine wave amplitude to carrier amplitude) above unity, a larger fundamental voltage is obtained, but appreciable low-order harmonics appear in the PWM waveform.

3.3.2 Constrained optimal pulse width modulation

In this section, optimal switching patterns are determined. Each pattern minimizes the nontriplen current harmonics (up to the 43rd. harmonic) subject to a specified value for the fundamental voltage (V_{1sp}), a specified number of switchings (commutations) per quarter cycle (M) and a fixed angular difference between the commutation angles

($\Delta\alpha$) which may be calculated by:

$\Delta\alpha$(degrees) = 360 x commutation time (seconds) x maximum operating frequency (HZ) . (3.9)

Problem Statement

The problem is to minimize the objective function defined by:

$$\overset{*}{I} = \left[\sum_{n=5,7,11,\ldots}^{43} \left(\frac{\overset{*}{V}_n}{n}\right)^2 \right]^{\frac{1}{2}} \qquad (3.10)$$

subject to:

$$\overset{*}{V}_1 = \overset{*}{V}_{1_{sp}} \quad \text{and,}$$

$$\alpha_1 \geq \Delta\alpha \;, \; \alpha_2 \geq \alpha_1 + \Delta\alpha \;, \ldots\ldots, \; \frac{\pi}{2} \geq \alpha_M + \frac{\Delta\alpha}{2}$$

where,

$\overset{*}{V}_n$ is the normalized peak harmonic voltage given from equation (3.3) by: $\overset{*}{V}_n = V_n/(4\ U_g/\pi)$, n=1, 5, 7, 11,...

$\overset{*}{I}$ is the normalized total rms harmonic current given from equation (3.8) by: $I^* = I/\dfrac{(4\ U_g/\pi)}{\sqrt{2}\ \omega L}$

$\overset{*}{V}_{1_{sp}}$ is the specified normalized fundamental voltage.

The optimization problem, stated, was solved using the Sequential Unconstrained Minimization Technique [12], for the following cases:

(a) M=2 , $\Delta\alpha$ = 5°

(b) M=2 , $\Delta\alpha$ = 10°

(c) M=4 , $\Delta\alpha$ = 5°

(d) M=4 , $\Delta\alpha$ = 10° .

In each case, different specified values for the normalized fundamental voltage ($\overset{*}{V}_{1_{sp}}$) were considered. Figures 3.7 to 3.10 show the optimal switching patterns as well as the minimum normalized harmonic current plotted versus $\overset{*}{V}_{1_{sp}}$.

3.4 Optimum Voltage and Frequency for Speed Control of Pump and Fan Drives

A number of control strategies have been implemented to meet the load requirements in an induction motor drive system. A constant horsepower variable speed operating range is desirable in many applications [13]. A controlled slip operation of an induction motor has been adopted with different control strategies [14 - 17], specially in traction applications where constant torque operation is required over a certain speed range and constant horsepower operation is required over another speed range.

An induction motor, driving a pump or a fan, is required to produce a torque which is proportional to the frequency squared.

An experimental study has been implemented on variable speed pump and fan drives [4]. The speed control strategy was to vary the induction motor speed by changing both the supply voltage and frequency in such a

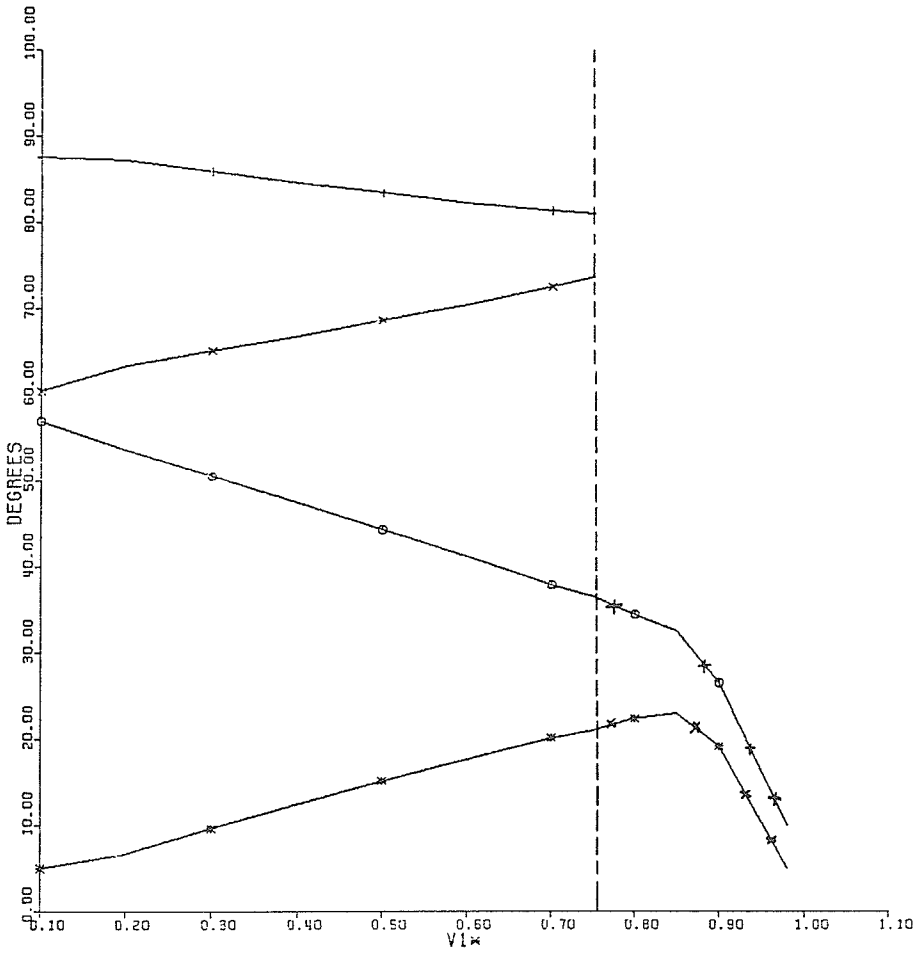


FIGURE 3.7A OPTIMAL SWITCHING PATTERNS FOR M=2 & DELTA=5 DEGREES.

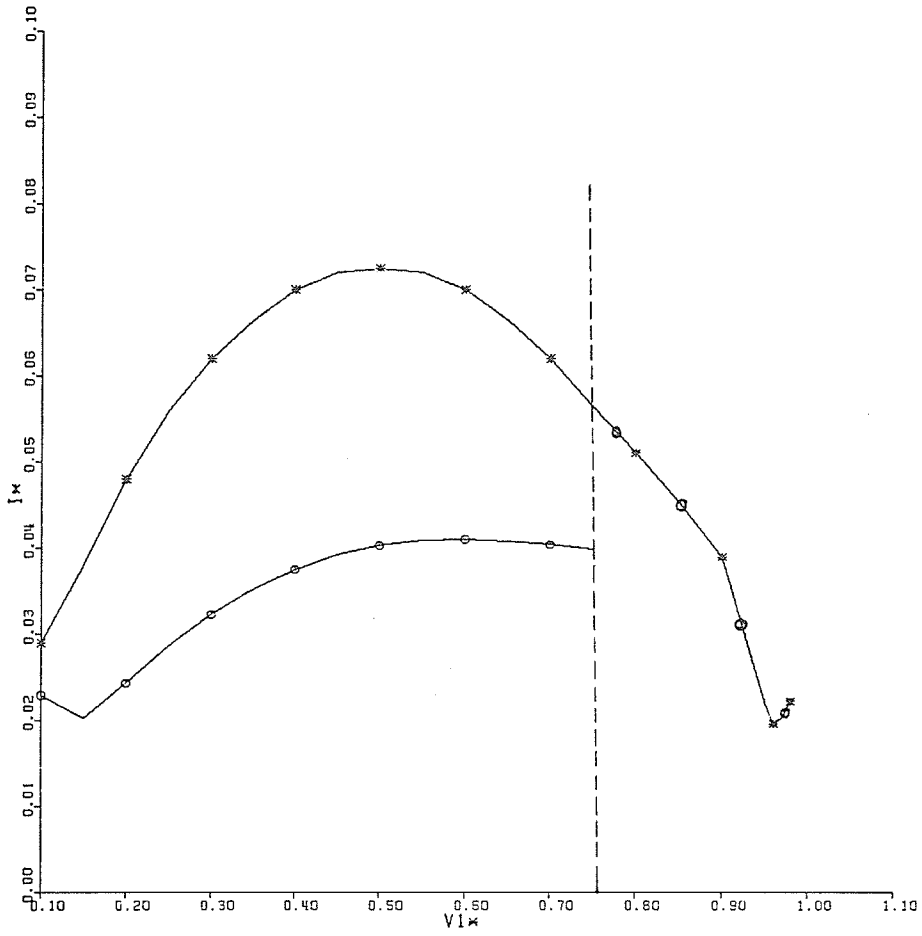


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FIGURE 3.7B MINIMUM NORMALIZED HARMONIC CURRENT VERSUS NORMALIZED FUNDAMENTAL VOLTAGE FOR M=2 & DELTA=5 DEGREES.

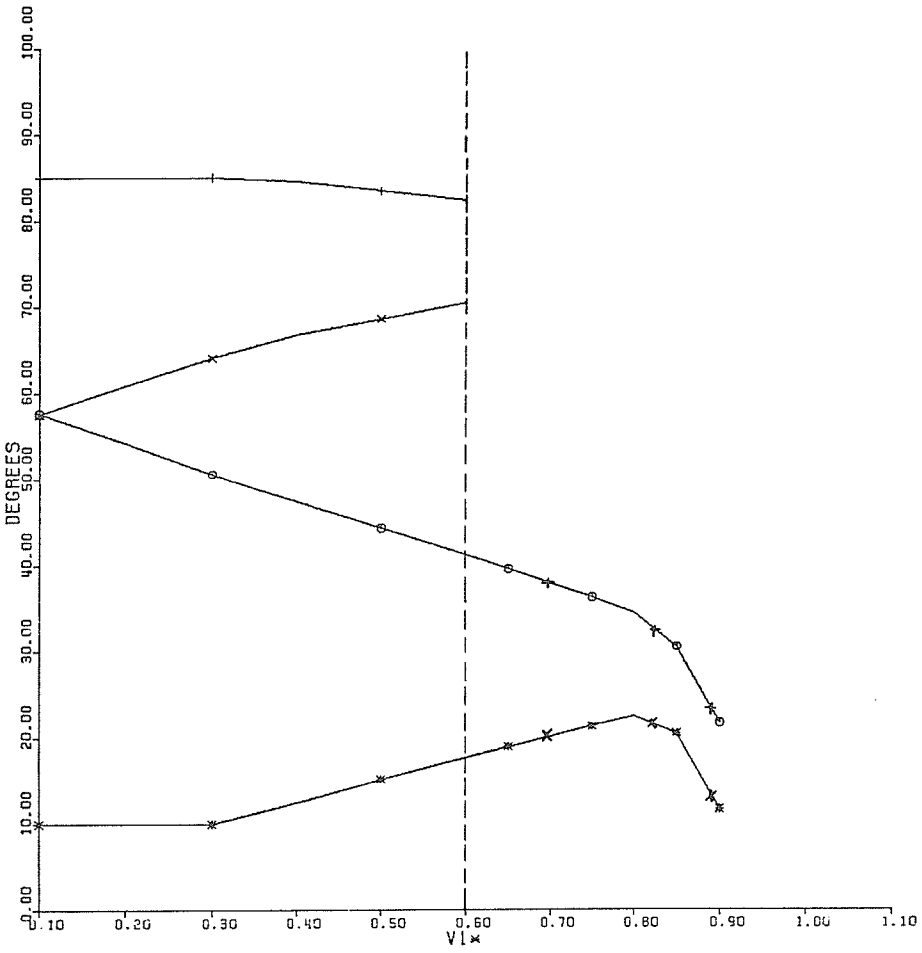

FIGURE 3.8A OPTIMAL SWITCHING PATTERNS FOR M=2 & DELTA=10 DEGREES.

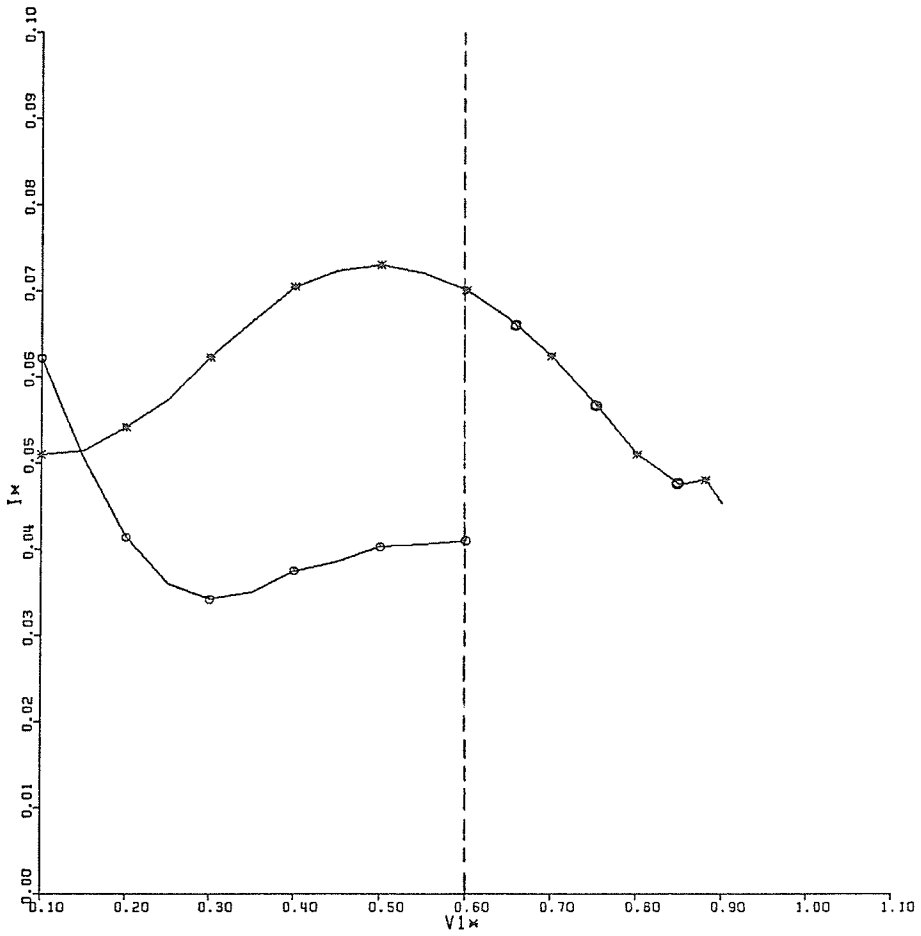

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FIGURE 3.8B MINIMUM NORMALIZED HARMONIC CURRENT VERSUS NORMALIZED FUNDAMENTAL VOLTAGE FOR M=2 & DELTA=10 DEGREES.

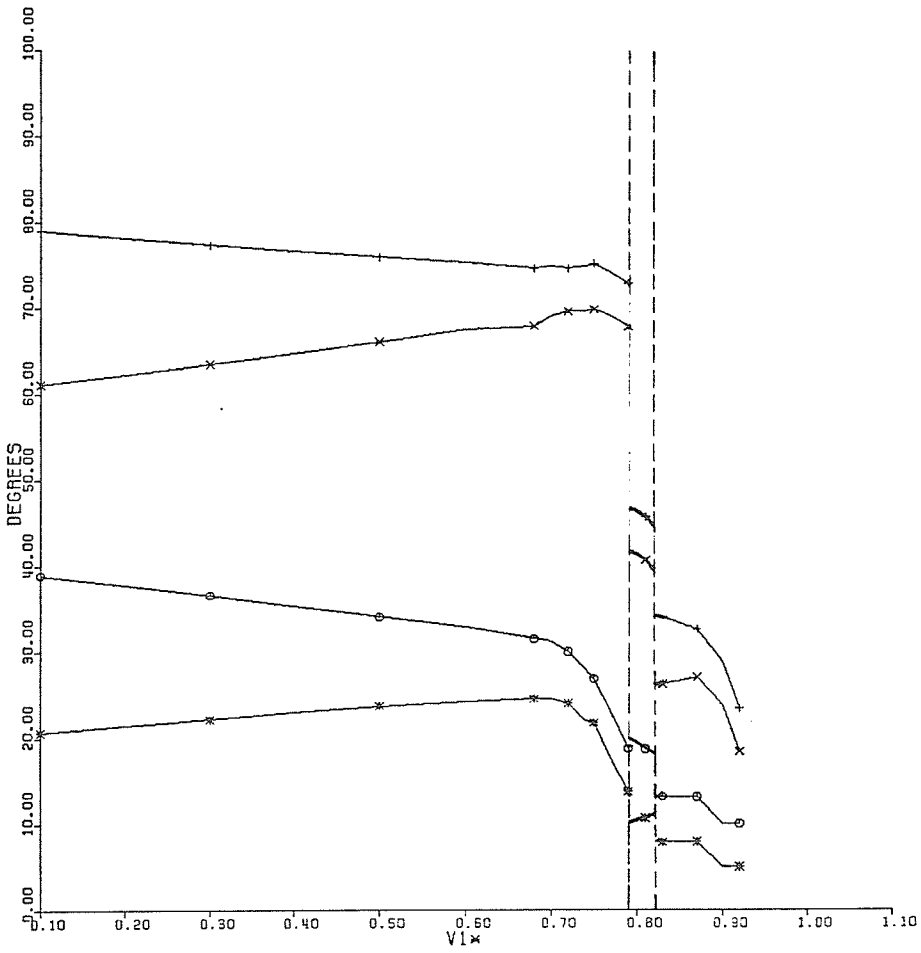


FIGURE 3.9A OPTIMAL SWITCHING PATTERNS FOR M=4 & DELTA=5 DEGREES.

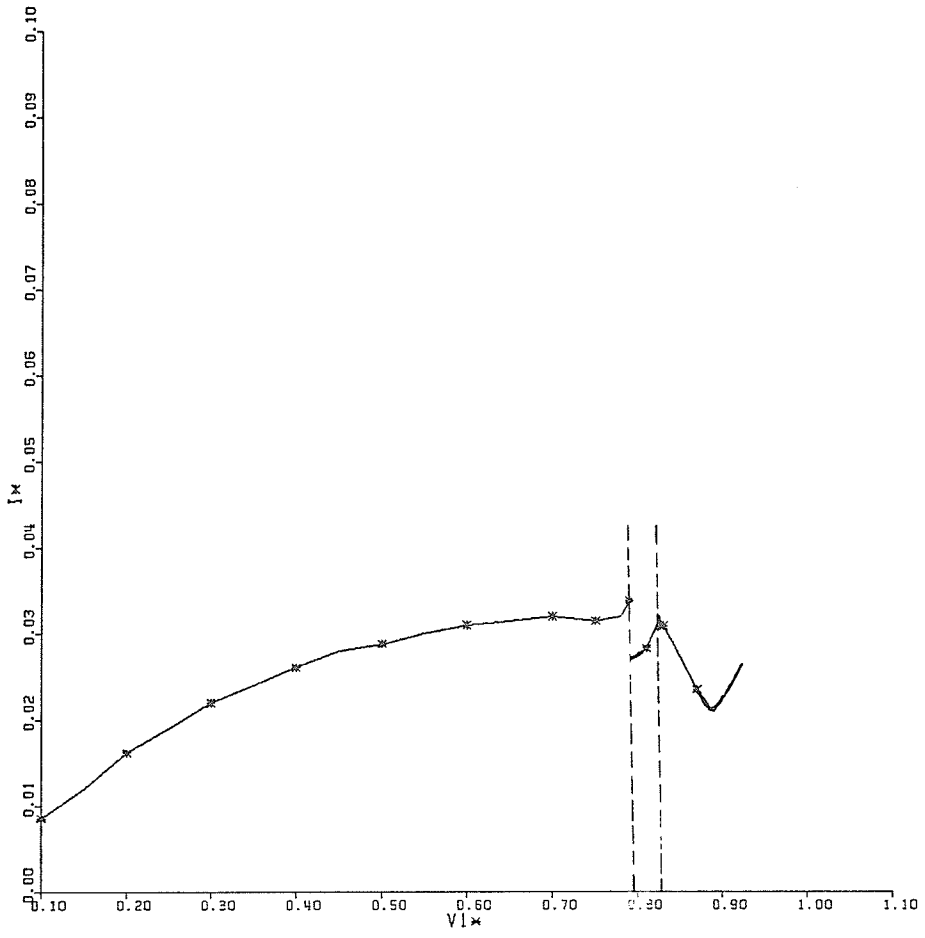


FIGURE 3.9B MINIMUM NORMALIZED HARMONIC CURRENT VERSUS NORMALIZED FUNDAMENTAL VOLTAGE FOR M=4 & DELTA=5 DEGREES.

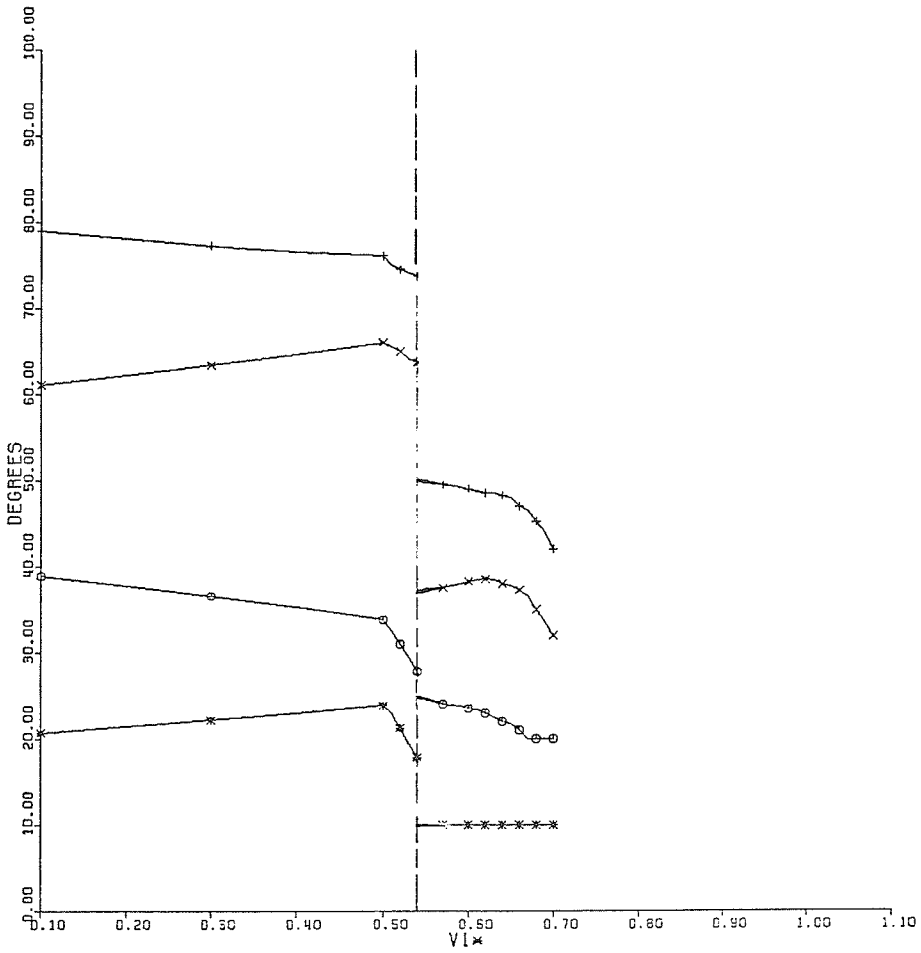


FIGURE 3.10A OPTIMAL SWITCHING PATTERNS FOR M=4 & DELTA=10 DEGREES.

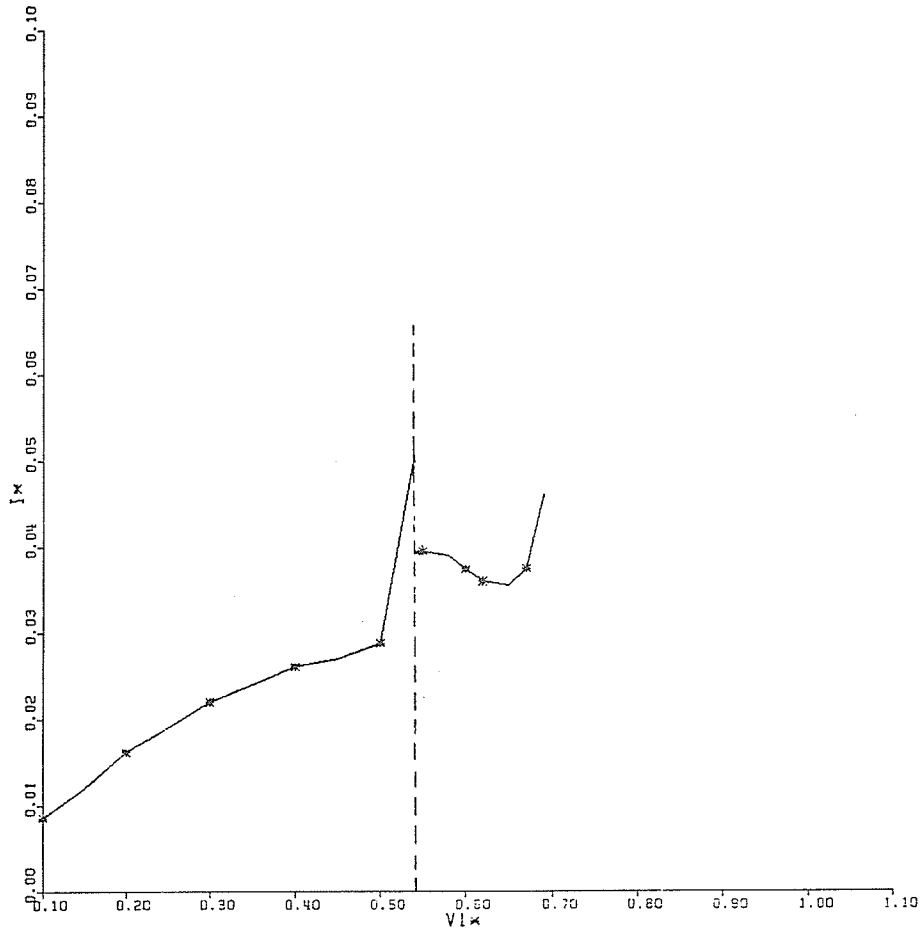


FIGURE 3.10B MINIMUM NORMALIZED HARMONIC CURRENT VERSUS NORMALIZED FUNDAMENTAL VOLTAGE FOR M=4 & DELTA=10 DEGREES.

relation that maximum motor efficiency is achieved. This relation was emperically derived and is given by:

$$E_1 = 0.1665\ f^{1.718} + 17.96 \qquad (3.11)$$

where,

E_1 is the rms line-line supply voltage, in volts.

f is the supply frequency, in Hz.

The above emperical relation was derived from results of an experimental work on an induction motor: 208 V line-line, 3 HP, 3 phase, star connected and a current rating of 8.9 A. Emperical formulae for the induction motor losses and equivalent circuit parameters were derived as functions of frequency, slip and applied voltage.

3.5 Microprocessor control scheme

Each thyristor of the three-phase PWM inverter of Chapter II, has to be fired at the right instant, so that the inverter circuit can operate properly and generate the required PWM voltage wave shapes. The firing sequence of the thyristors is microprocessor controlled.

The backbone of the control scheme is the construction of a look-up table which has to be stored in the microprocessor memory, and according to which the complete control is accomplished.

The look-up table is constructed as follows:

1. A set of discrete frequencies is selected in the required operating frequency range (20 - 60 Hz).

2. For a specified frequency (f_{sp}), in that range, the optimum fundamental peak phase voltage is determined from equation (3.11) as:

$$V_{1_{sp}} = \sqrt{\frac{2}{3}} \; (0.1665 \; f_{sp}^{1.718} + 17.96) \qquad \text{volts} \quad .$$

Then, the normalized fundamental peak voltage ($\overset{*}{V}_{1_{sp}}$) is obtained from:

$$\overset{*}{V}_{1_{sp}} = V_{1_{sp}} / (4 \; \bar{U}_g / \pi)$$

where,

U_g is half the dc supply voltage at the inverter input.

3. The minimum angular difference between commutations ($\Delta\alpha$) is determined from equation (3.9) as:

$$\Delta\alpha = 360 \; T_c \; \hat{f} \qquad \text{degrees}$$

where,

T_c is the commutation time (s)

$\hat{f}$ is the maximum operating frequency (Hz)

= 60 Hz in the range (20-60 Hz).

4. Subject to the values of $\overset{*}{V}_{1_{sp}}$ and $\Delta\alpha$, obtained in steps 2 and 3, the normalized total rms harmonic current, I^*, (given by equation (3.10)), is minimized for M=2 and for M=4 as explained

in Section 3.3.2. The lesser minimum of I^* will determine the switching pattern, i.e., where M=2 or M=4 as well as the associated optimal commutation angles at the specified frequency (f_{sp}).

5. The process is repeated for the rest of the discrete frequencies in the operating frequency range. The family of the operating frequencies and their corresponding switching patterns will constitute the look-up table required for storage in the microprocessor memory.

According to the look-up table, constructed as explained, a microprocessor control program was implemented to provide the proper firing scheme of the 12 thyristors (4 for each single phase inverter) of the three-phase inverter of Chapter II [18].

The order of events in a complete control cycle is as follows:

1. A specified motor speed, N_{sp} (rpm), is selected by a speed control switch. This, automatically, determines a certain frequency (f_{sp}) corresponding to N_{sp} from:

$$f_{sp} = \frac{N_{sp}\, p}{60} \quad \text{Hz} \quad \text{(for a 2p -pole machine).}$$

2. The switching pattern, corresponding to f_{sp}, is fetched from the look-up table stored in the microprocessor memory. According to this particular switching pattern, control signals to the firing circuits will determine the firing sequence of the inverter 12 thyristors.

3. The proper activation of the thyristors will generate the optimal PWM voltage wave shape at the inverter output in order to drive the motor at the specified selected speed at maximum efficiency and minimum current harmonics.

Although the operating frequencies, stored in the memory, are discrete, the program provides a means to allow gradual changes in motor speed.

CHAPTER IV

PROTOTYPE INVERTER TESTING

4.1 Prototype Design Specifications

A prototype of the single-phase inverter circuit, of Figure 2.1, was built in the laboratory according to the following specifications:

(a) Commutating capacitors and inductors:

$$\left.\begin{aligned} &C1 = C2 = C = 3.0 \ \mu F \\ &L1 = L2 = L3 = L = 15.0 \ \mu H \\ &\text{Hence,} \\ &X = \sqrt{L/C} = 2.24 \ \Omega \end{aligned}\right\} \qquad (4.1)$$

(b) Toroid winding:

A winding bar (1.0 inch diameter) and a former (15/8 inch diameter) were used to form the toroid configuration (Figure 2.16). The turn radius (r) and the mean path diameter (D) are, then, obtained from the geometry as:

$$\left.\begin{aligned} &r = 0.0135 \ m \\ &D = 0.0746 \ m \\ &\text{Hence,} \\ &k = D/r = 5.526 \\ &\text{An AWG \#14 enamel coated wire was used with} \\ &\rho = 3.08 \qquad \Omega/1000 \ ft. \end{aligned}\right\} \qquad (4.2)$$

Form (2.48), (2.49), (4.1) and (4.2), the toroid number of turns (N) and quality factor (Q) are given by:

$$\left.\begin{aligned} N &= 69.92 \cong 70.0 \text{ turns.} \\ Q &= 18.59 \end{aligned}\right\} \qquad (4.3)$$

(c) Thyristor specifications:

General Electric C140 (2N3653) SCR (see Appendix A).

(d) Thyristor protection:

A snubber circuit, consisting of a capacitor C_b (0.10 μF, 600 V) and a resistance R_b (20 Ω , 2W), was connected across each thyristor for protection against excessive (dV/dt) as well as limiting the peak reverse recovery voltage at the instant of blocking.

Two limiting resistors r_1 and r_2 (3.5 Ω, 5 KW each) were connected in series with the dc bus, as shown in Figure 4.1, to protect the main thyristors V1 and V2 against short circuit current in case of commutation failure.

(e) Power supply requirements:

Two separately excited dc machines were connected as shown in Figure 4.1 to deliver 100 V and -100 V. Each machine is rated at: 3 KW, 125 V, 24 A and 1200 r.p.m.

Two electrolytic-type filtering capacitors C_{F1} and C_{F2} (7650 μF each) were connected across the two dc machines.

Three power supplies were used to provide 5V, - 5V and 12V to the control circuits (see Appendix B).

(f) Maximum allowed load current ($\hat{I}_L$):

Using equations (2.8), (2.12), (4.1) and (4.3) with U_g = 100 V, the current peak I_{P1} (Figure 2.2a) of the commutation pulse is calculated to be 42.8 A.

For optimum commutation, the load current should not exceed (I_{P1}/1.50) [6].

Hence, $\hat{I}_L$ = 42.8/1.5 = 28.53 A.

(g) The value of τ (Figure 2.2)

Using the values of L and C given by section 4.1(a), the angular frequency ω of the commutation circuit is calculated to be 0.075 x 10^6 rad/s.

For $\omega\tau$ = 3.0 rad, τ = 40.0 μs.

4.2 Prototype and Control Circuits Description

The thyristors and diodes were mounted on heat sinks which perform the dual function of cooling and of being common connecting points. The thyristors are anode mounted while the diodes are cathode mounted. The heat sinks, the commutating capacitors and the snubber circuits were mounted on one fiber board (see Figure 4.2a). The snubber circuits

are not shown since they are mounted under the board). As shown, shielded pairs of wire were used to connect the thyristor gate and cathode terminals to the control circuits to avoid pick-up of any unwanted signals which may affect firing the thyristors.

The commutating inductor toroids were mounted on a separate fiber board, Figure 4.2b. Each toroid was glued between two fiber discs to ensure rigidity and to avoid deformation in its geometry which may affect the value of the commutating inductance. Pick-up coils were wound as shown for measuring the currents through the toroids.

Electrolytic-type capacitors were used for the commutating capacitors. AWG #12 (600 V) insulated wire was used in wiring the prototype.

The control circuits are shown in Figure 4.2C. To the bottom left of the photograph, the microprocessor unit is shown. A thumb-wheel speed selector is mounted on the microprocessor breadboard. Start and reset push buttons are shown. To the top right of the photograph is a delay circuit. The other two modules shown are the firing circuits. Each module provides firing pulses to one of the main thyristors and one of the auxilliary thyristors via shielded pairs of wire.

4.3 Basic Test Set-Up

Figure 4.1 shows a schematic diagram of the test set-up. Measuring and display equipment used are listed in Appendix B. Figure 4.3 shows a photograph of the prototype and control circuits.

4.4 Preliminary Test Results

4.4.1 Testing the control circuits

The control circuits were tested separately from the prototype inverter.

(i) First, the circuits were tested for square wave operation by setting the frequency at 60 Hz. The firing pulses (which are supposed to trigger thyristors V6, V1, V5 and V2) were observed. The test results, shown in Figure 4.4, indicated that the control circuits were operating properly for square wave operation.

(ii) Next, the control circuits were tested for pulse width modulation by reducing the frequency to 56 Hz. The firing pulses (to main thyristors V1 and V2) were observed. The test results, shown in Figure 4.5, indicated proper operation of the control circuits with pulse width modulation.

Testing the control circuits, as described, indicated that they were operating properly and in the correct sequence for both square wave and pulse width modulation operation.

4.4.2 Prototype inverter preliminary tests

With the control circuits connected to the prototype inverter, the commutation circuits were tested with the inverter on no-load.

(i) First, the prototype inverter was tested for square wave operation by setting the frequency at 60 Hz. The voltages across the

main thyristors V1 and V2 were observed as shown in Figure 4.6. With a zero voltage across V1, the voltage across V2 was 200 V. Also with a zero voltage across V2, a voltage of 200 V occurred across V1. This alternate operation of the main thyristors indicated that the commutation circuits were responding as expected to the control circuits. The overshoots observed in the waveforms of Figure 4.6 are due to switching transients. Figure 4.8 shows detail of the switching transient of the voltage across main thyristor V1 shown in Figure 4.7.

(ii) Next, the prototype inverter was tested for pulse width modulation operation. Different frequencies were selected below 60 Hz, and the corresponding waveforms of the voltage across main thyristor V2 were observed. The test results shown in Figures 4.9 - 4.13 indicated that the prototype inverter was operating, as expected, with pulse width modulation at different frequencies.

(iii) Following the no-load tests, trials were made to test the prototype inverter on load. It was not possible to complete the load tests because of commutation failure under different loading conditions (resistive, inductive or resistive-inductive loads). Trying to investigate the commutation failure, further no-load tests were performed (described in (iv) and (v)). The results of these tests indicated some peculiar behavior which was not expected in comparison to the theoretical waveforms.

(iv) The behavior of the voltages e_{C1} and e_{C2}, across the commutating capacitors C1 and C2 respectively, was observed at the initial starting transient (when V6 is fired then V1) as shown in Figure 4.14. This behavior was not expected. The test indicated that the time rate of change of e_{C1} was higher than that of e_{C2} and that after experiencing some damped oscillations, e_{C1} and e_{C2} stabilized at -50 V and 250 V respectively. On the other hand, e_{C1} and e_{C2} were expected to change from 100 V to 300 V (across C2) and -100 V (across C1) at the same rate with respect to time, Figure 4.15.

Under these conditions, the dc bus voltage was observed and the waveform, Figure 4.16, was obtained. The Figure indicates a peculiar behavior which was not expected. The voltage dips from 200 V to about 125 V, undergoes some damped oscillations and then stabilizes at approximately 200 V. The dc bus voltage was expected to be constant at 200 V under any conditions, Figure 4.15.

With the same conditions at starting, the current i_2 (through commutating inductor L2) was observed as shown in Figure 4.17 which was not expected. The test indicates a relatively highly damped sinusoidal waveform with a peak of 24 A, while the theoretical waveforms, Figure 4.18, approaches a pure sinusoidal waveform with a peak of 43 A.

(v) Since the starting waveforms of Figures 4.14, 4.16 and 4.17, observed during the test, did not agree with the theoretical waveforms

of Figures 4.15 and 4.18, further no-load tests were performed to help investigating the peculiar behavior of the waveforms obtained.

First, the dc bus voltage as well as the commutation current i_2 were observed during the first half cycle of commutation (initiated by firing V5 while V1 is already on). The current waveform, shown in Figure 4.19, was not in agreement with the theoretical waveform shown in Figure 4.20. The test waveform indicated lower peaks as well as a reverse current through the auxilliary thyristor V5.

The dc bus voltage showed another peculiar behavior (Figure 4.19) which was different from its behavior at starting (Figure 4.16). During the first transient of the commutation interval, the test indicated the voltage rising above 200 V. At the end of this transient, the voltage dropped to about 160 V. During the second transient (initiated by firing V2), the voltage dropped to about 40 V at a different rate from that at the end of the first transient. At the end of the first half cycle of commutation damped oscillations in the voltage waveform were observed.

Second, both dc voltage and commutation current i_2 were observed during the second half cycle of commutation as shown in Figure 4.21. The test indicated the same peculiar behavior of the dc bus as compared to its vehavior during the first half cycle. Another unexpected behavior was observed when comparing the values of the current peaks during the second half cycle (Figure 4.21) to those at the first half cycle

(Figure 4.19). The test indicated lower peaks in the second half cycle relative to the first half cycle. Theoretically, they should be approximately equal.

4.5 Analysis of Preliminary Test Results

4.5.1 Analysis of the peculiar behavior of the starting waveforms

This analysis is presented in conjunction with the equivalent circuit of the prototype inverter at starting shown in Figure 4.22.

(1) Before starting, the test indicated the voltages across C1 and C2 to be the same and equal to 100 V (Figure 4.14). Also the dc bus voltage was indicated to be equal to 200 V (Figure 4.16). Therefore a conclusion can be reached that the test results proved the commutating capacitors C1 and C2 to be equal.

(2) Upon starting, firing V6 then V1 Figure 4.22, the voltage rate of change across C1 was indicated to be higher than that across C2 (test result Figure 4.14). Applying these results to Figure 4.22, means that i_a flowing in loop a is higher than i_b flowing in loop b. This cannot happen except if the impedance of loop b is higher than that of loop a upon starting. Since C1 and C2 have been proven to be equal and since L1 and L2 are common in both loops, then there is no way for the impedance of loop b to be higher than that of loop a at starting except if the equivalent filtering capacitance C_F drops to a very low value at starting.

(3) The dip in the dc bus voltage indicated by the test result Figure 4.16 supports the above analysis. This is because, since the dc bus voltage is equal to the voltage across C_F, then any drop in the voltage across C_F would cause a similar dorp in the dc bus voltage. Flow of the current i_b in the indicated direction, Figure 4.22, tends to change the polarity across C_F. With a very low value of C_F, the flow of i_b causes the voltage across C_F to drop appreciably. This drop is reflected on the dc bus voltage causing the dip indicated by the test result Figure 4.16.

(4) The test indicated a highly damped waveform of the current i_2 (Figure 4.17). In virtue of the equivalent circuit Figure 4.22 and the test result, the circuit Q factor must be very low, i.e., highly lossy. The lower Q factor could be due to changes in the inductance of the commutating inductors L1 and L2, lossy commutating capacitors or lossy filtering capacitors. The way the commutating inductor toroids were mounted does not leave any doubt that the inductance of the commutating inductors was constant during the test. Therefore the only source of losses would be due to the use of lossy commutating and filtering capacitors.

Another indication of high circuit losses (low Q factor) can be realized through the values of the final voltages across the commutating capacitors C1 and C2 at the end of the starting transient which are -50 V and 250 V respectively as indicated by test results Figure 4.14. According to the theoretical waveforms Figure 4.15, these

voltages were supposed to be -100 V and 300 V based on a relatively very high Q factor.

(5) Although the current i_2 dropped to zero 50 μs after starting had been initiated (Figure 4.17), the test indicated existence of oscillations after 50 μs in the waveforms of the dc bus voltage. (Figure 4.16) and the voltages across C1 and C2 (Figure 4.14). The only explanation for the existence of these oscillations with $i_2 = 0$, is the existence of a resonance response between the commutating and filtering capacitors and a high inductance. The only source of this inductance is the dc machines. Therefore these oscillations would prove that the dc machines have too much source impedance

4.5.2 Analysis of the peculiar behavior during and between commutations

The test results obtained during the first half cycle of commutation can be analyzed in virtue of Figure 4.19 and the equivalent circuits of the prototype inverter during the first and second transients shown in Figures 4.23 and 4.24 respectively. The test result indicated an appreciable rise in the dc bus voltage upon initiating the first transient, and an appreciable drop upon initiating the second transient. Since the voltage across C_F is equal to the dc bus voltage, then it should follow the same behavior. From Figure 4.23, upon initiating the first transient by firing V5, the flow of i_b in the direction shown would not overcharge C_F unless C_F is small enough. Since the test result indicated a rise in voltage, then this should mean that

upon initiating the first transient, the filtering capacitance C_F has dropped to such a very low value that the current i_b was able to overcharge C_F. This would explain the dc bus voltage rise during the first transient.

The same analysis can explain the dc bus voltage drop upon initiating the second transient of commutation in virtue of Figure 4.24.

During the second half cycle of commutation, the test results Figure 4.21 indicated the behavior of the dc bus voltage to be similar to that during the first half cycle. This ensures the interpretation which relates this behavior to low equivalent value of C_F.

The lower current peaks, compared to those during the first half cycle, is another indication of low circuit Q factor.

The reverse current appearing between commutation, as indicated by the test results Figures 4.19 and 4.21, could be due to an effect imposed by the current measuring probe.

4.6 Conclusion

The preliminary tests performed on the prototype inverter indicated the following:

(i) The dc machines proved to have too much source impedance.

(ii) The filtering capacitors were not capable of operating at high frequencies.

(iii) The commutating capacitors proved to be lossy.

Until such a time as better capacitors could be ordered and a better power supply could be available, load tests could not be completed because of commutation failure.

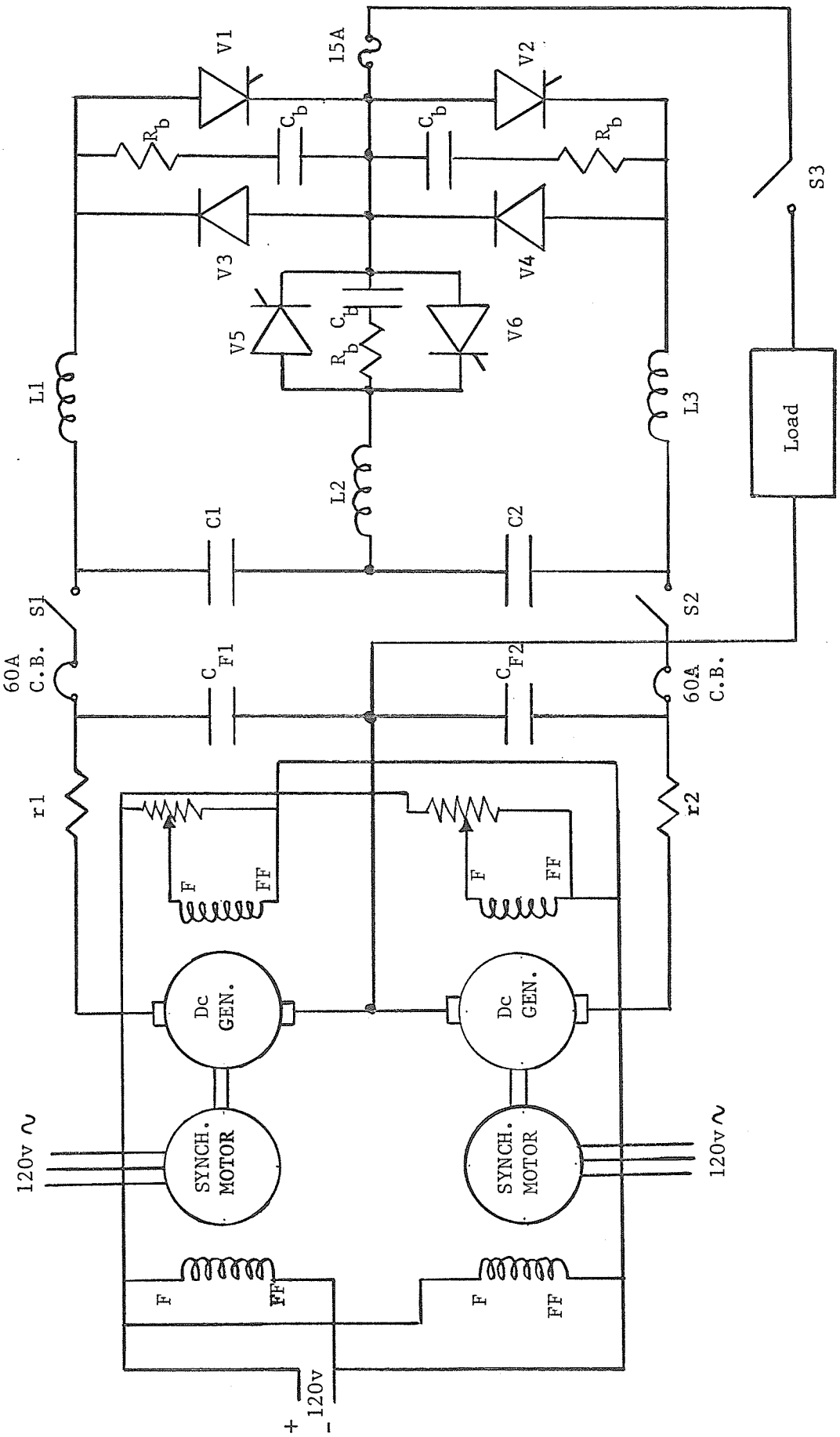


Figure 4.1 Basic test set-up circuit diagram

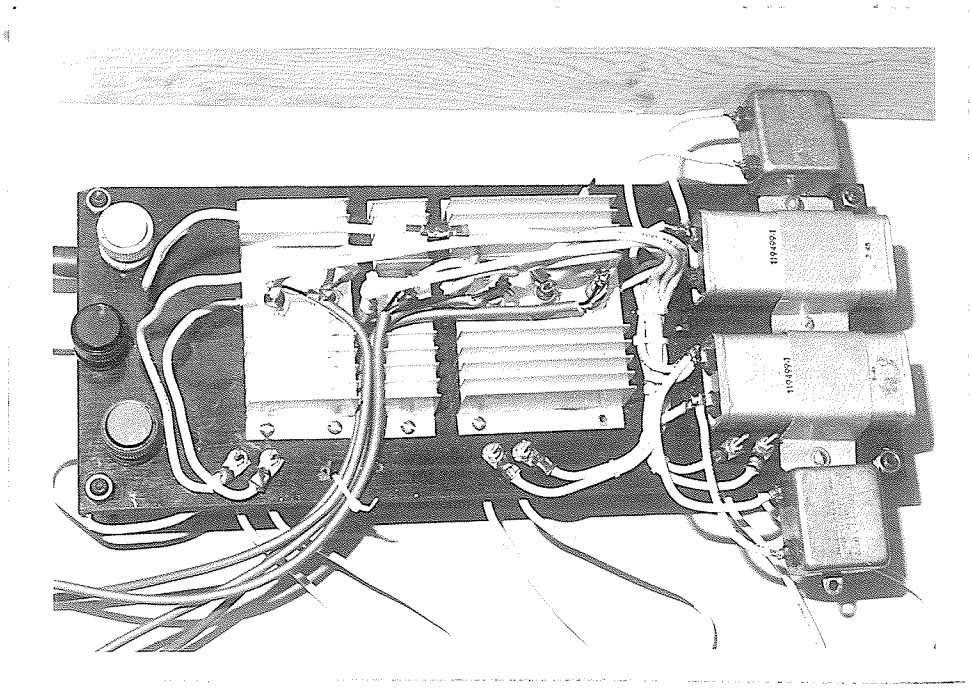


Figure 4.2a Prototype Inverter,Thyristor Board.

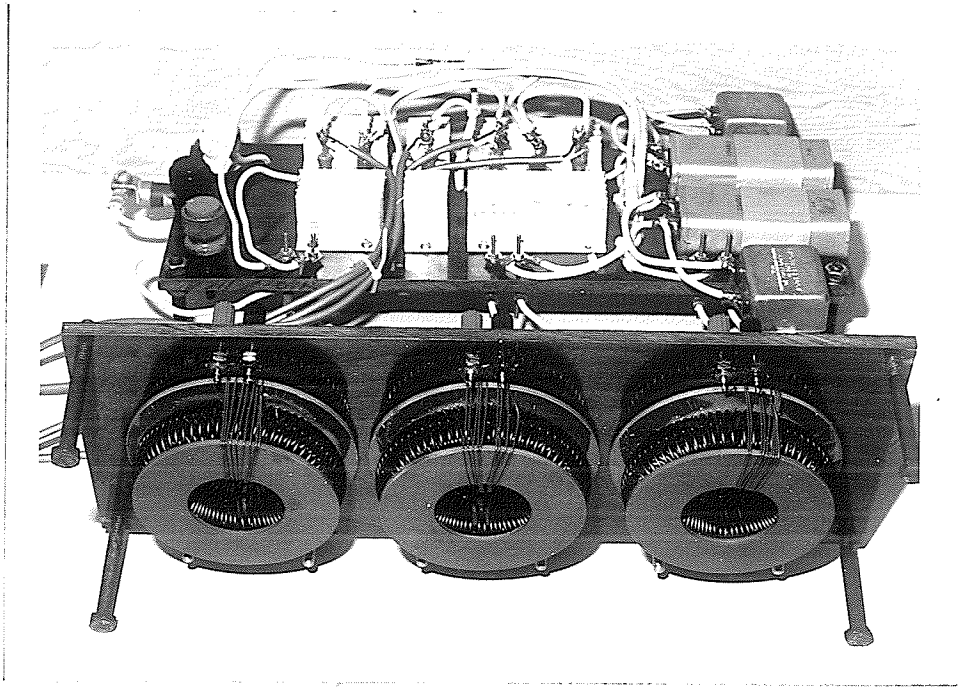


Figure 4.2b Prototype Inverter,Inductor Board.

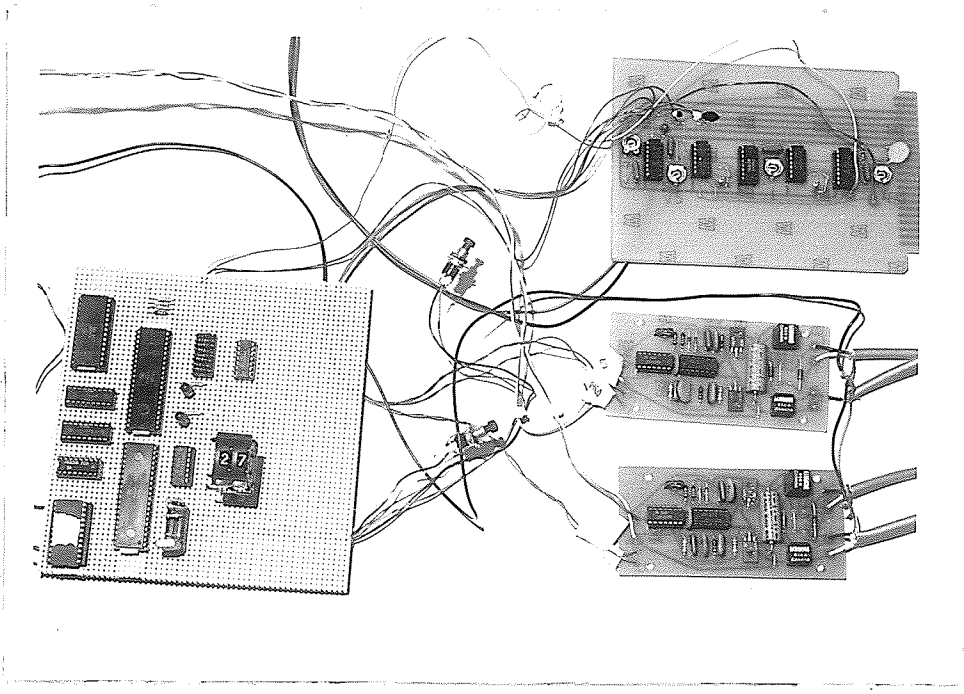


Figure 4.2c Control Circuits.

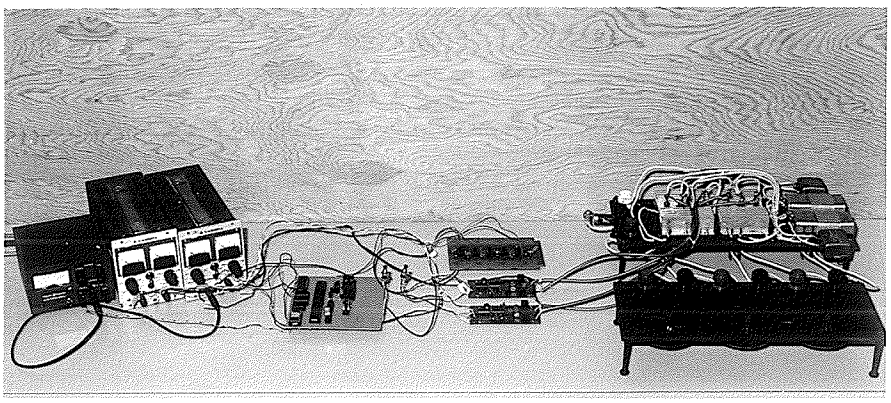


Figure 4.3 Prototype Inverter and Control Circuits.

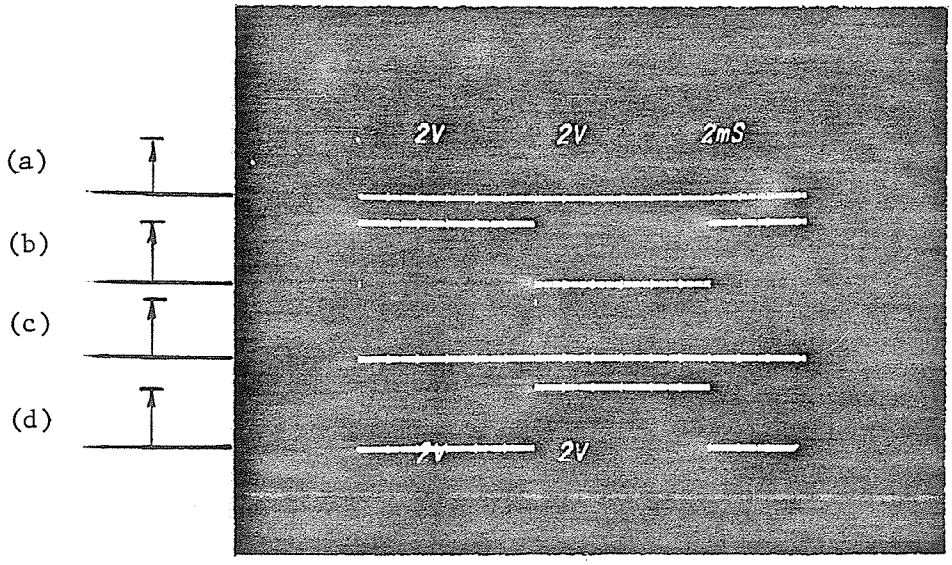


Figure 4.4 Firing pulses during testing the control circuits for square wave operation

(a) To auxilliary thyristor V6.
(b) To Main thyristor V1.
(c) To auxilliary thyristor V5.
(d) To main thyristor V2.

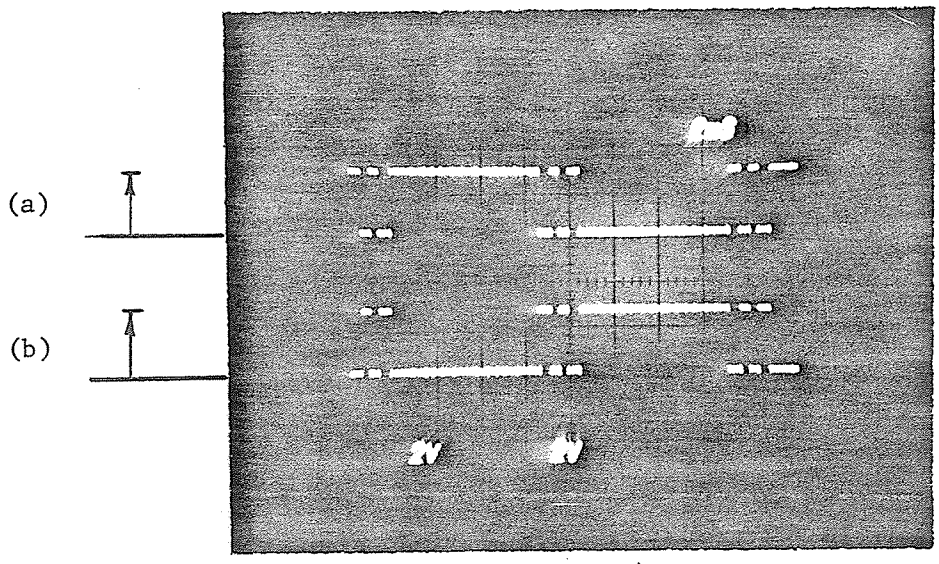


Figure 4.5 Firing pulses during testing the control circuits for PWM (at 56 Hz)

(a) To main thyristor V1.

(b) To main thyristor V2.

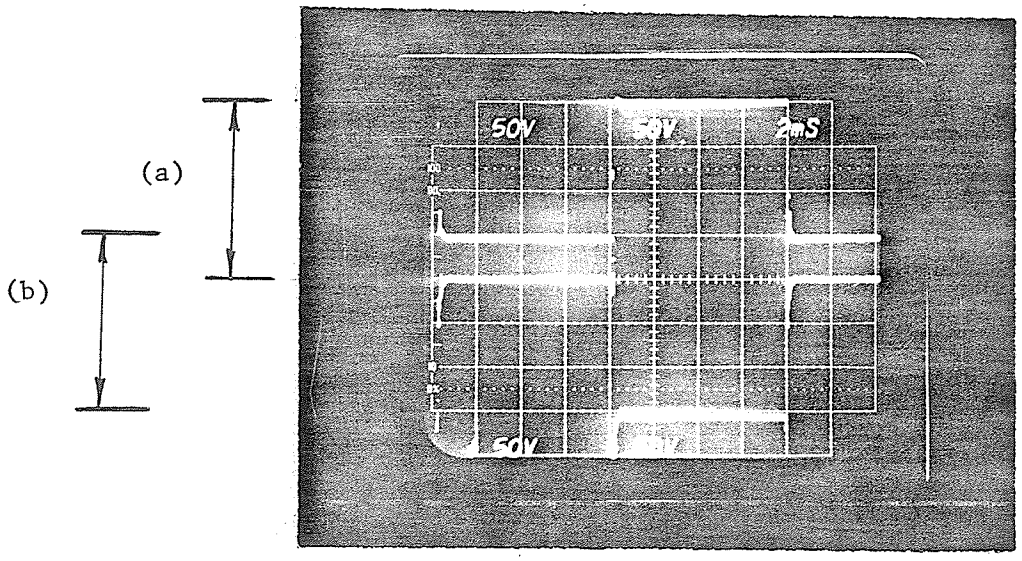


Figure 4.6 Voltages across main thyristors V1 and V2 during no-load test

(a) Voltage across V1.

(b) Voltage across V2.

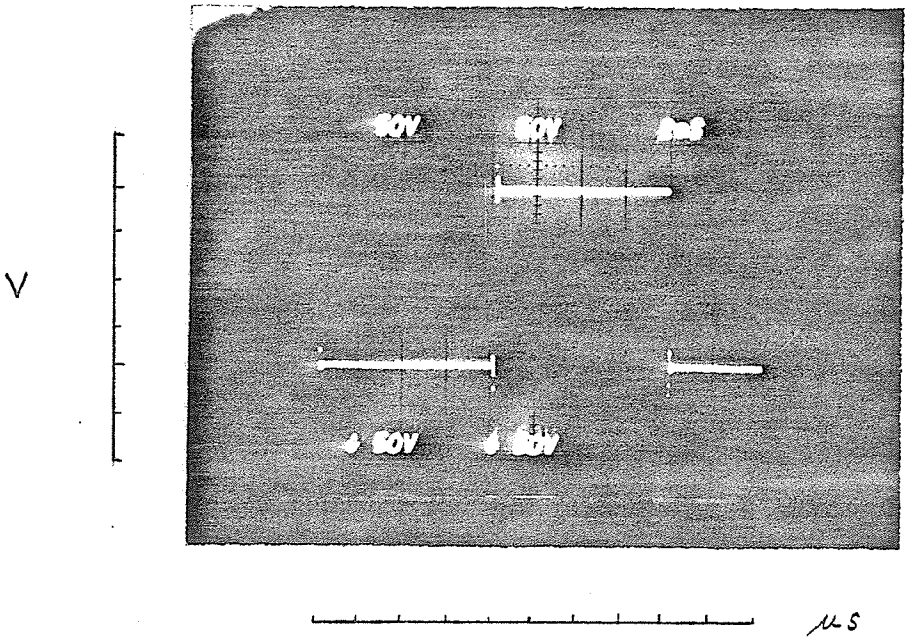


Figure 4.7 Voltage across main thyristor V1 during no-load test (at 60 Hz)

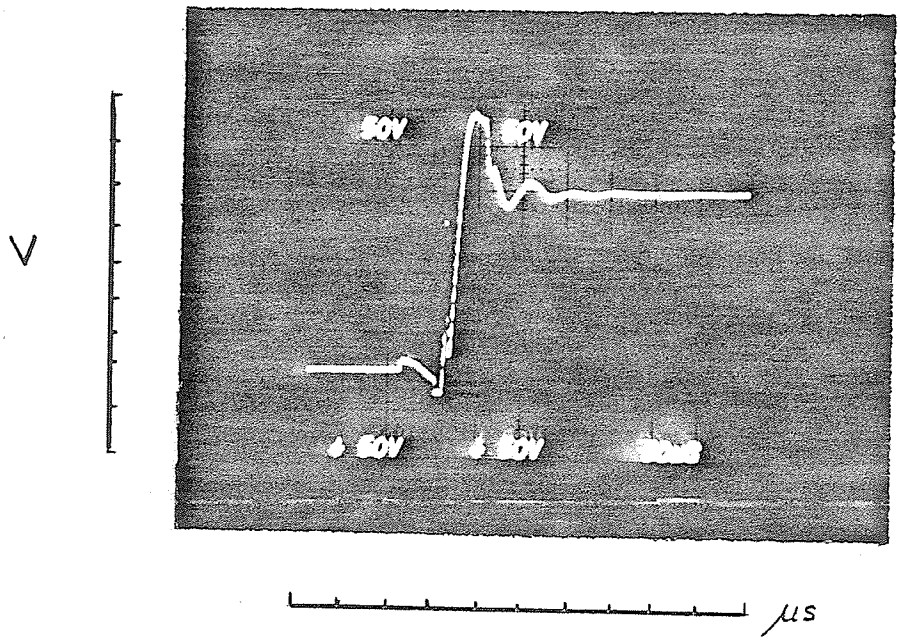


Figure 4.8 Voltage transient across main thyristor V1 during no-load test

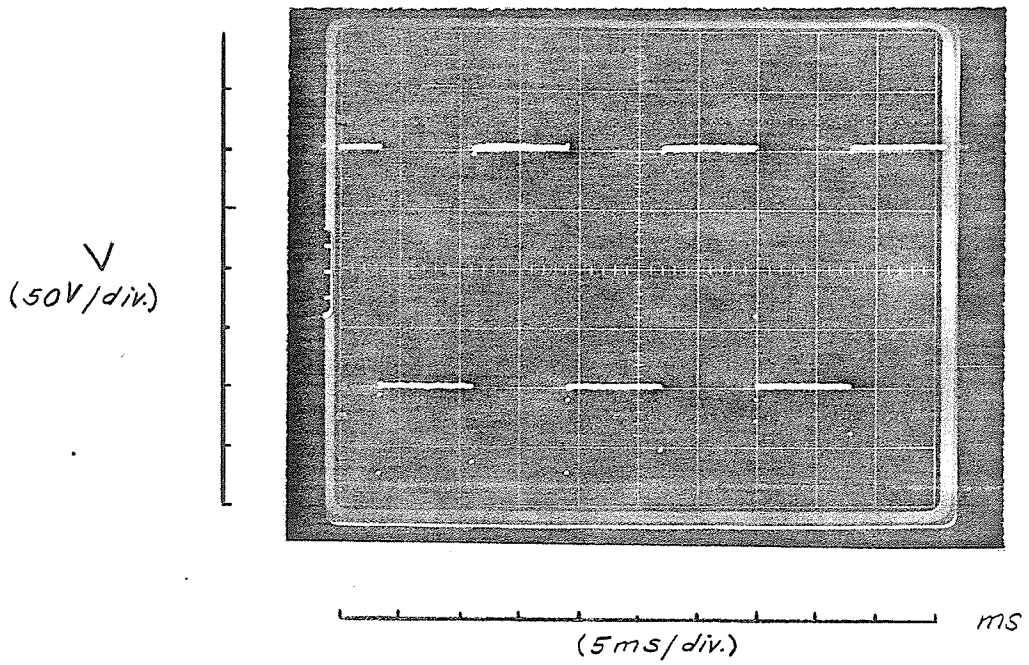


Figure 4.9 Voltage across main thyristor V2 at 60 Hz, no-load test

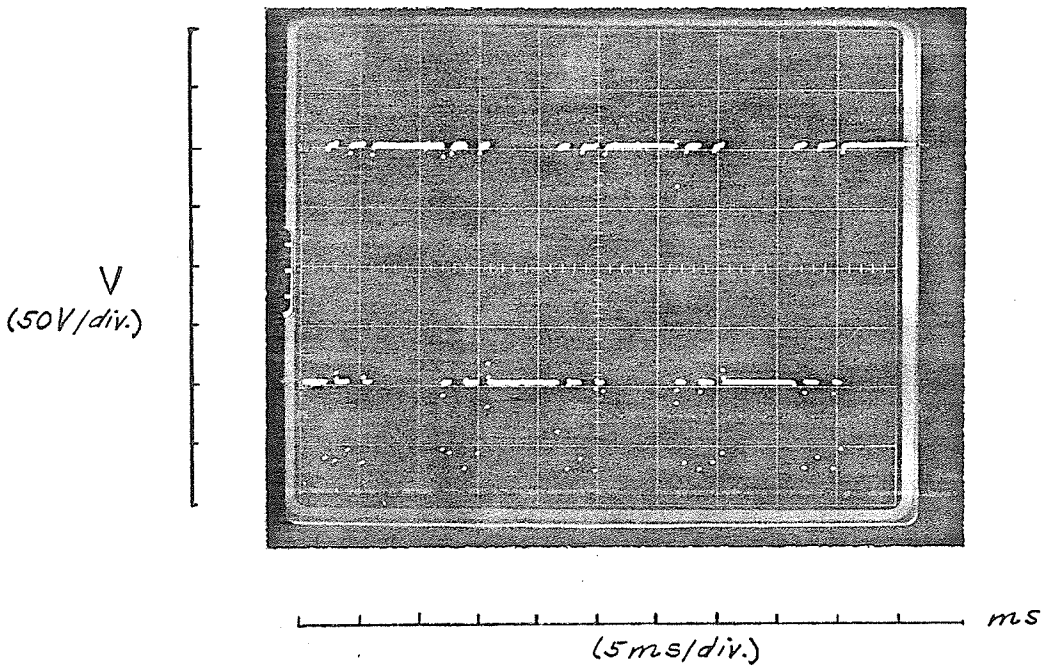


Figure 4.10 Voltage across main thyristor V2 at 50 Hz, no-load test

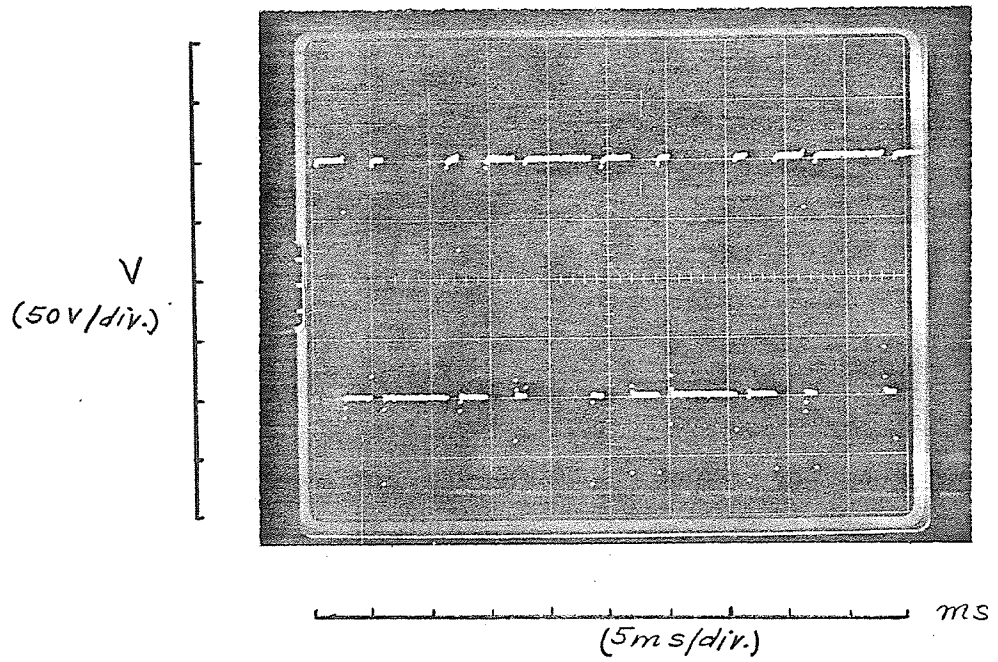


Figure 4.11 Voltage across main thyristor V2 at 40 Hz, no-load test

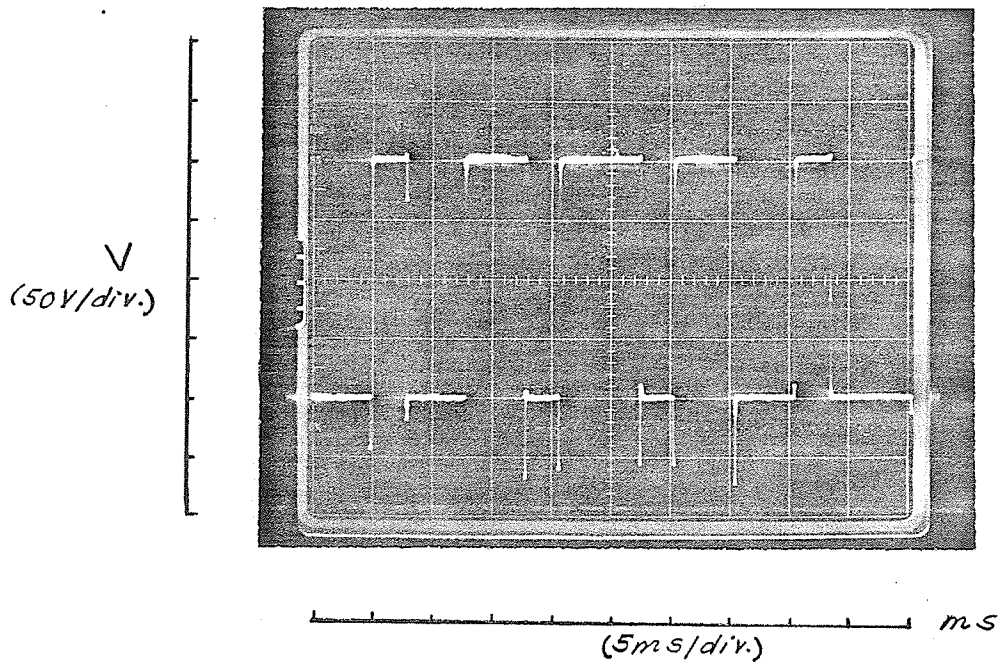


Figure 4.12 Voltage across main thyristor V2 at 30 Hz, no-load test

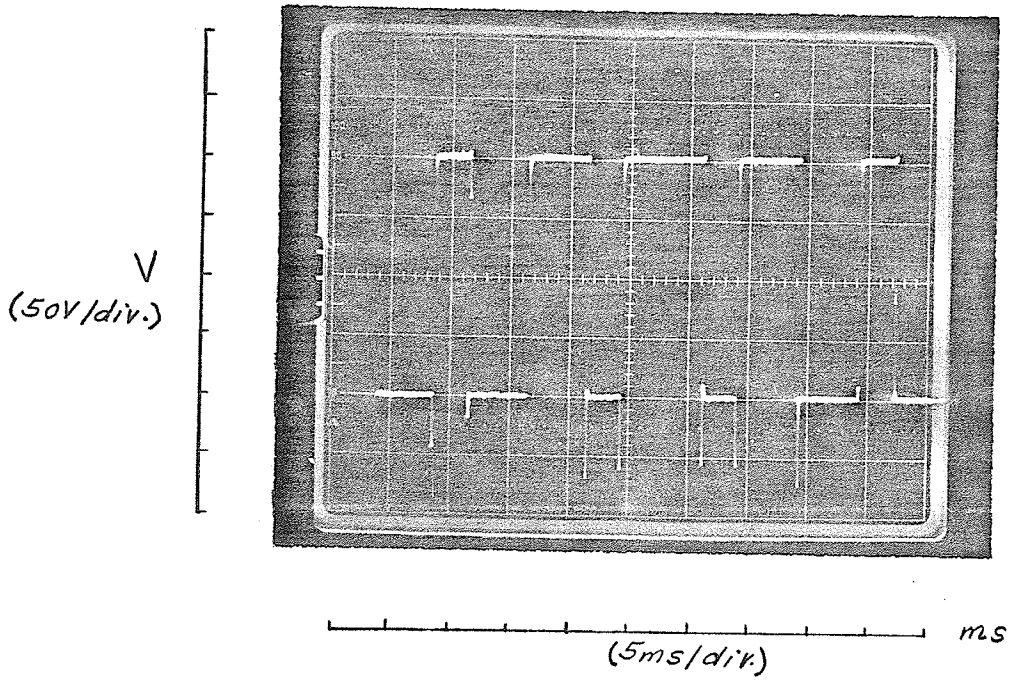


Figure 4.13 Voltage across main thyristor V2 at 20 Hz,no-load test

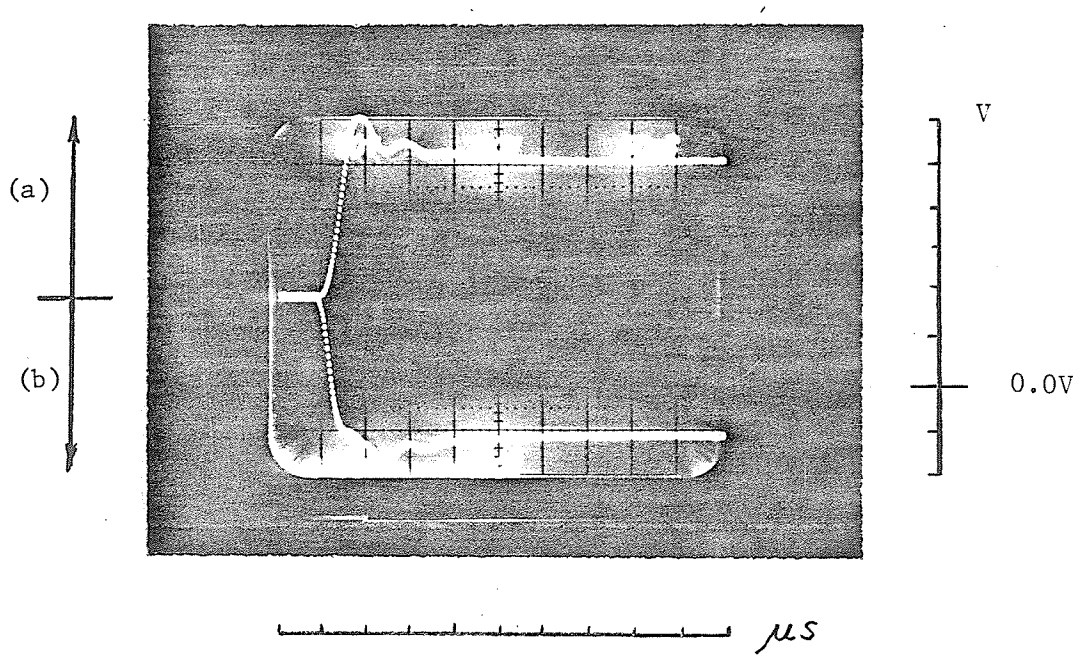


Figure 4.14 Starting waveforms of the voltages across C1 and C2, no-load test

(a) Voltage across C2.

(b) Voltage across C1.

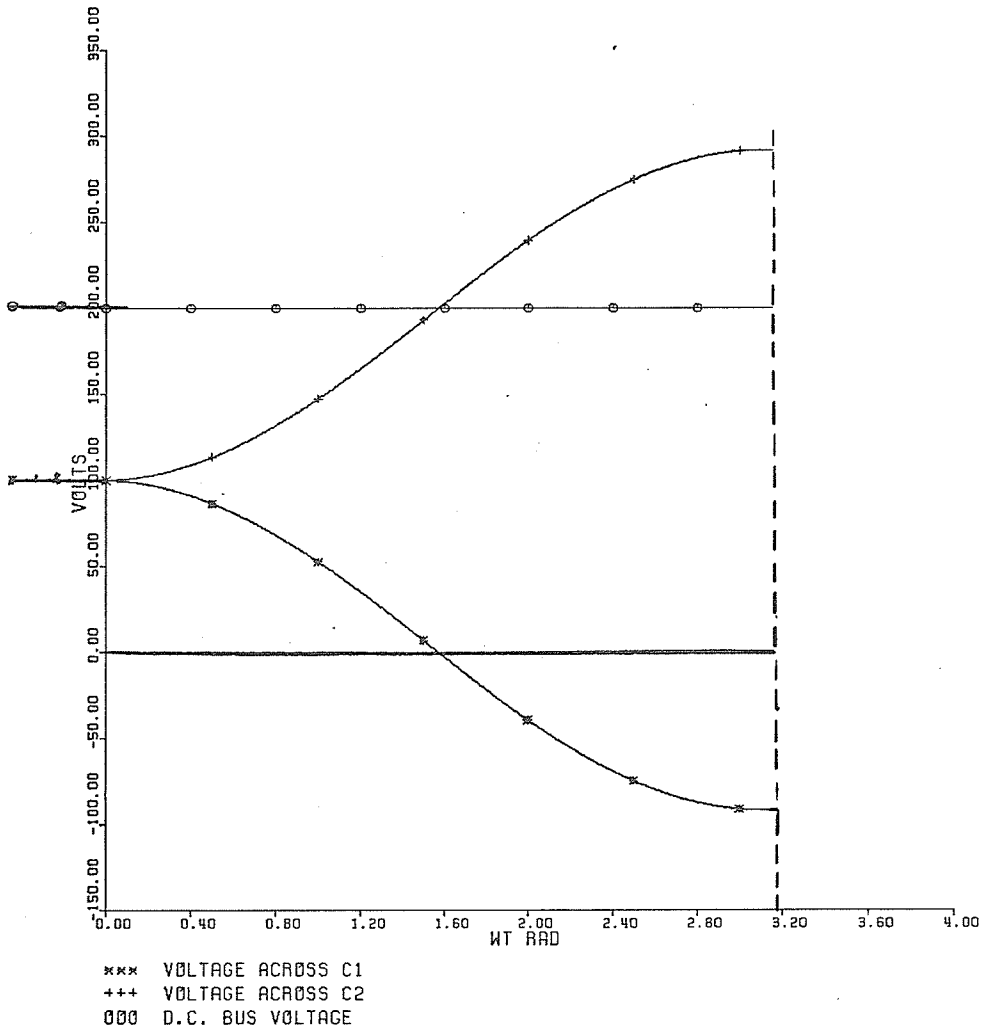


Figure 4.15 Theoretical starting waveforms of the voltages across C1 & C2 and the dc bus voltage ,at no-load

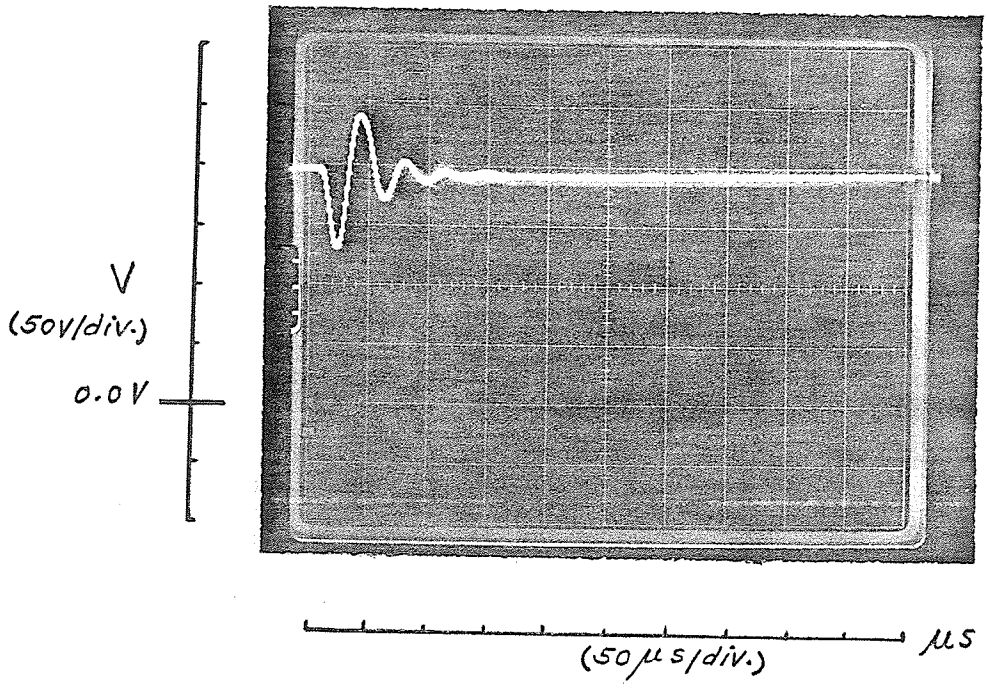


Figure 4.16 Starting waveform of the dc bus voltage , no-load test

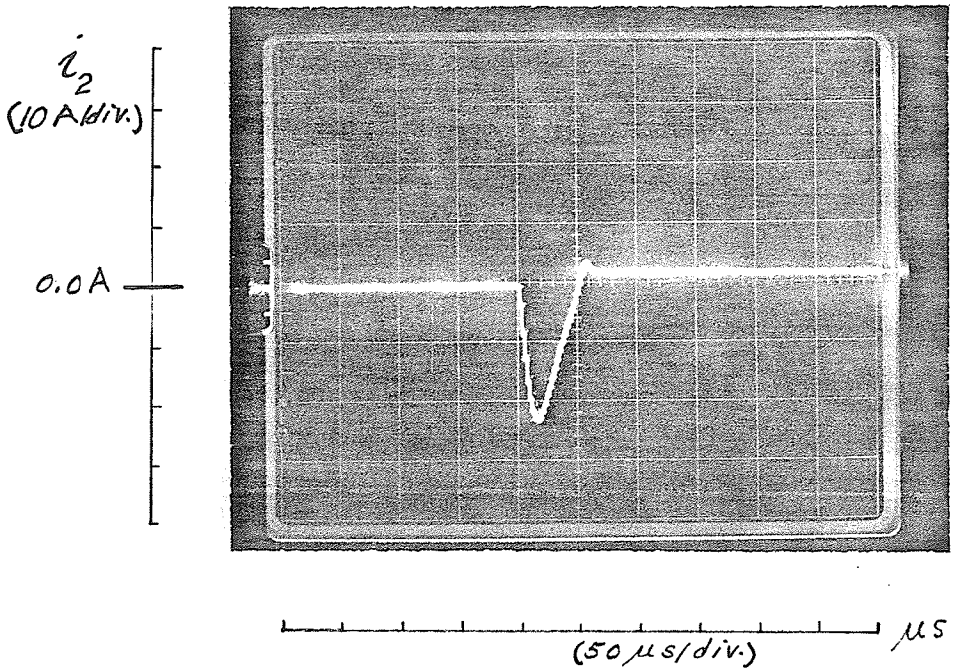


Figure 4.17 Starting waveform of i_2 ,no-load test

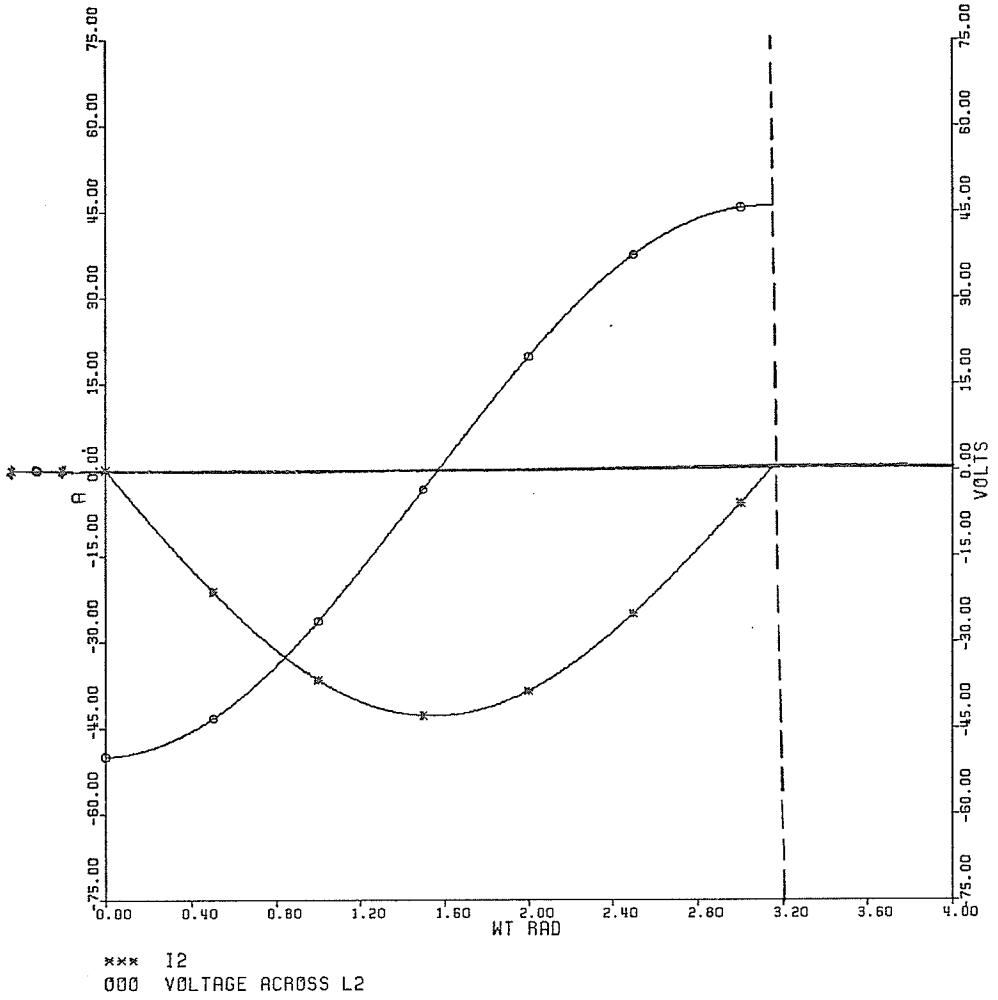


Figure 4.18 Theoretical starting waveforms of i_2 and the voltage across L2 ,at no-load

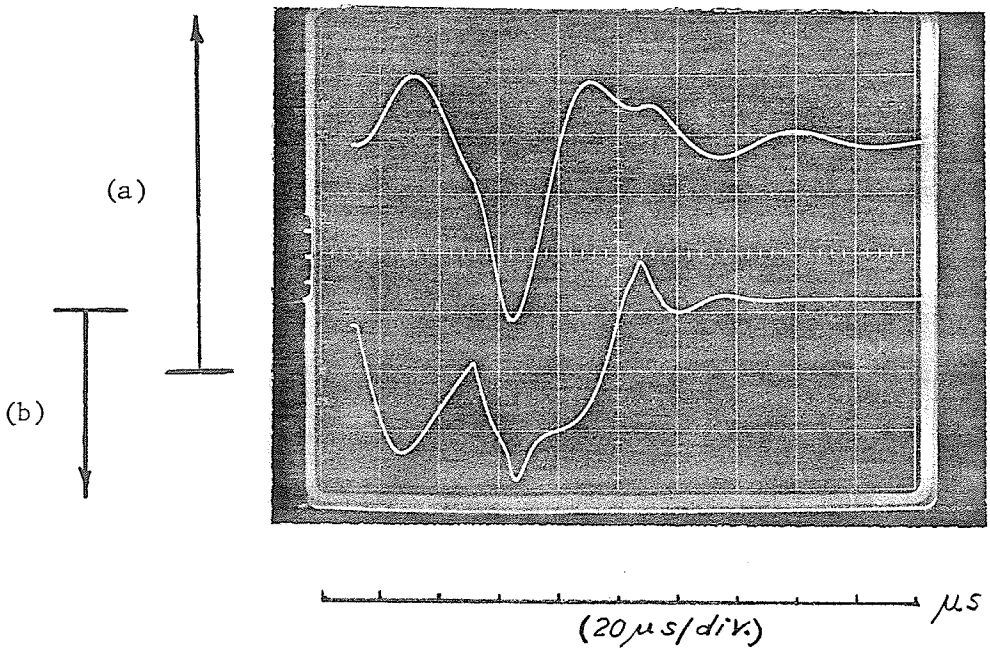


Figure 4.19 Waveforms of the dc bus voltage and i_2 during the first half cycle of commutation, no-load test

(a) Dc bus voltage (50V/div.)
(b) Current i_2 (10A/div.)

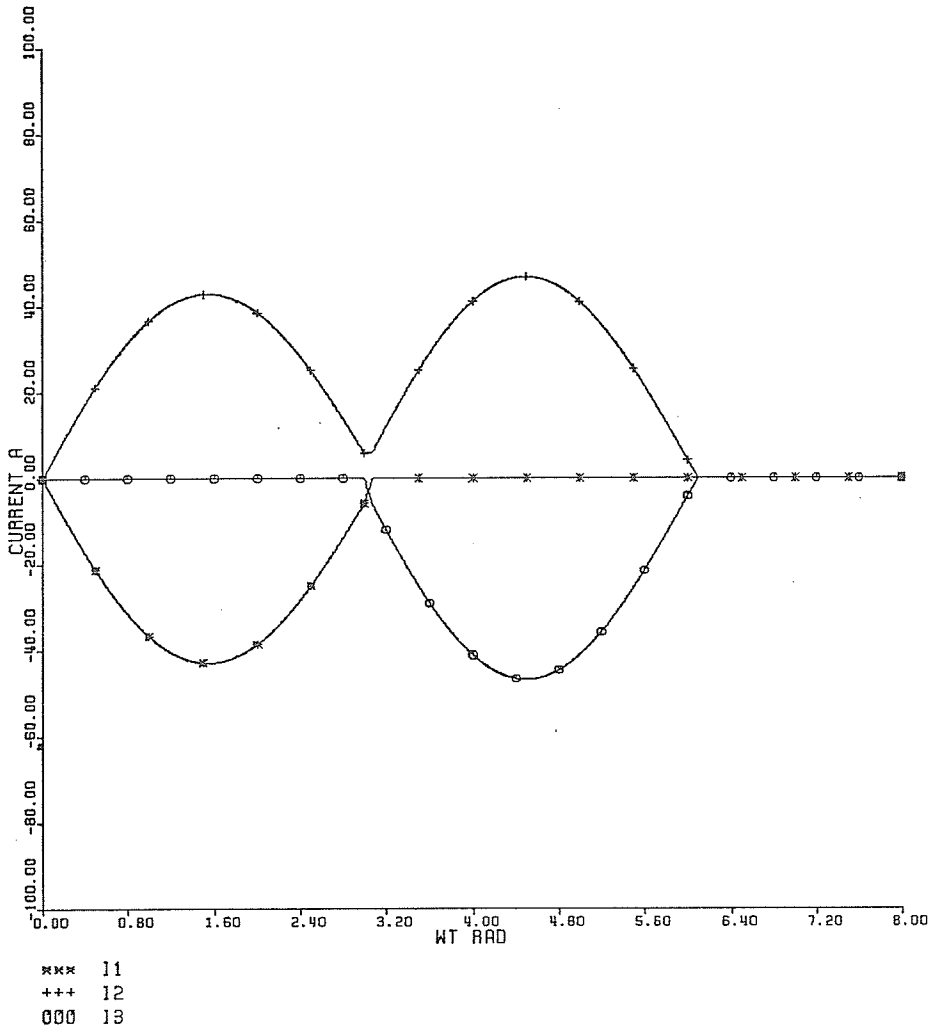


Figure 4.20 Theoretical waveforms of i_1, i_2 and i_3 during the first half cycle of commutation, at no-load

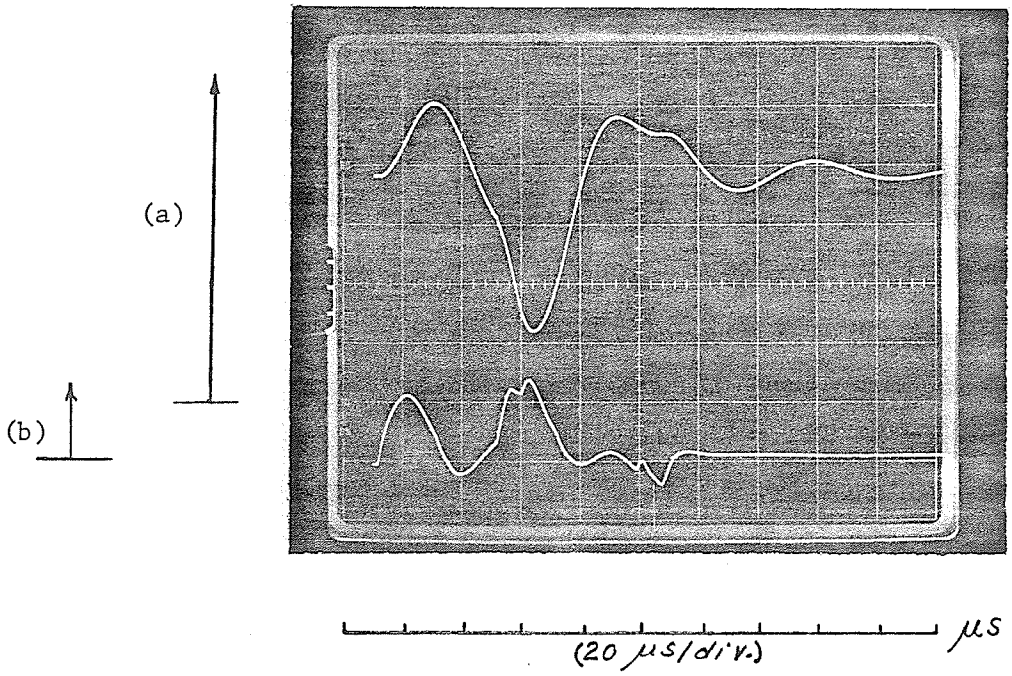


Figure 4.21 Waveforms of the dc bus voltage and i_2 during the second half cycle of commutation, no-load test

(a) Dc bus voltage (50V/div.)
(b) current i_2 (10A/div.)

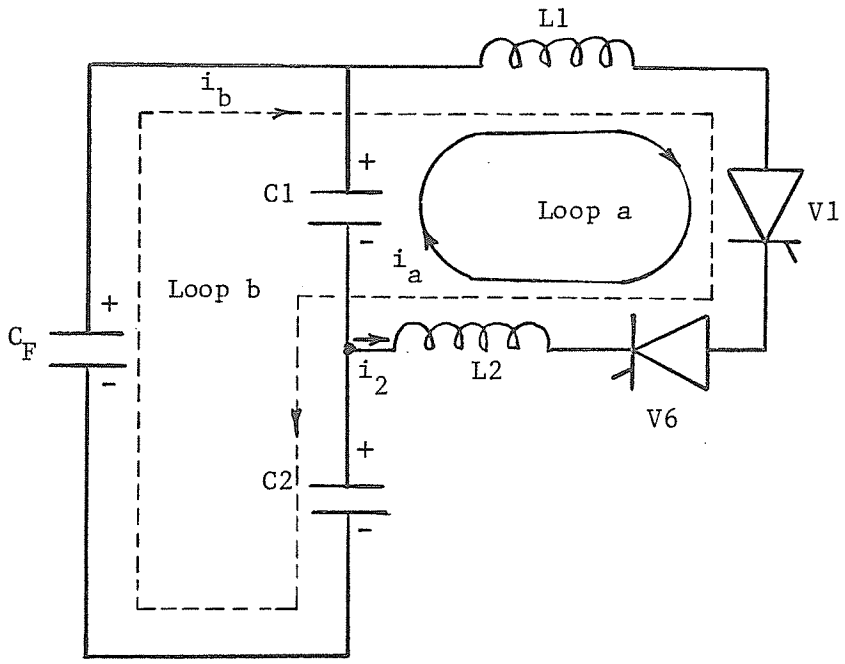


Figure 4.22 Initiating the starting transient by firing V6 then V1.

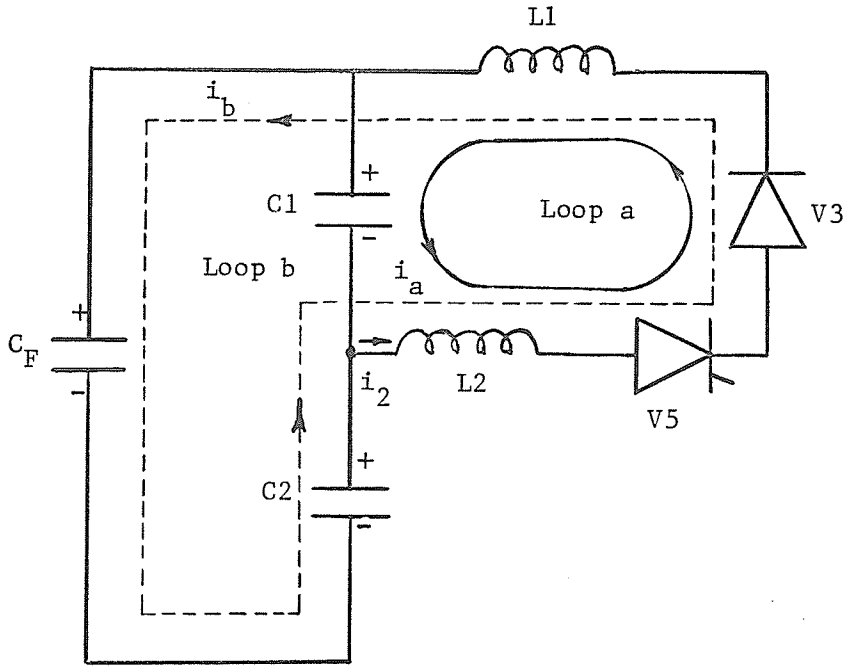


Figure 4.23 Initiating the first transient of the first half cycle of commutation by firing V5.

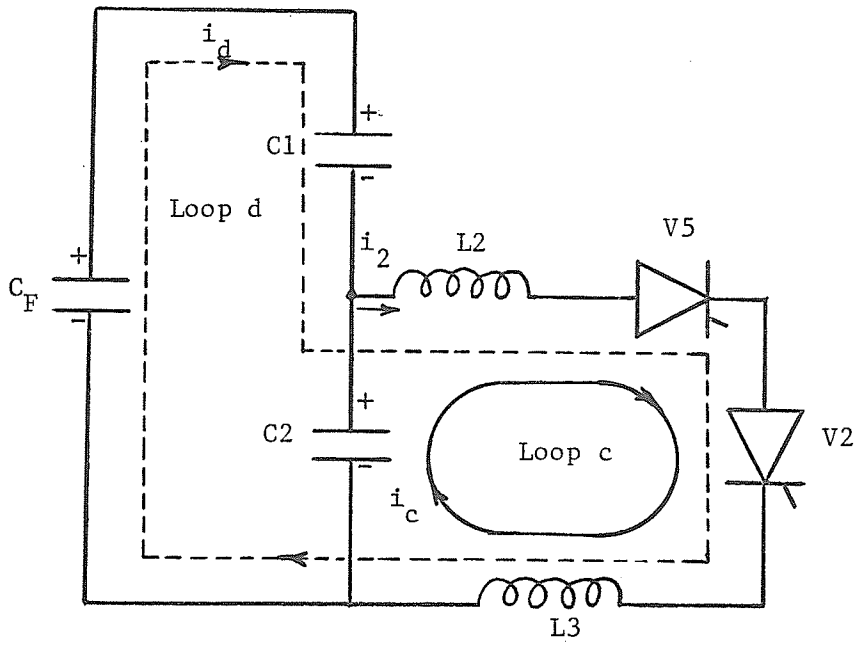


Figure 4.24 Initiating the second transient of the first half cycle of commutation by firing V2.

CHAPTER V

CONCLUSION AND RECOMMENDATIONS

5.1 Conclusion

(1) The inverter analyzed provides the following features:

(a) No iron elements are used, which are lossy, expensive and bulky and impose some operating limitations due to saturation problems.

(b) Relatively low commutation losses.

(c) Relatively less number of solid state components.

(d) Compact and relatively cheap.

(2) A constrained optimal Pulse Width Modulation (PWM) strategy has been developed in which nontriplen current harmonics (up to the 43 rd. harmonic) have been minimized while incorporating practical constraints such as minimum time between commutations.

(3) Maximum efficiency of induction motors driving pumps and fans may be achieved by the implementation of optimum PWM strategy applied to a modified McMurray inverter circuit. The PWM control strategy was implemented on a microprocessor in order to achieve optimum drive efficiency at each speed and hence flow rate.

(4) A prototype single-phase inverter was built, preliminary no-load tests were performed and test results were analyzed.

5.2 Recommendations

(1) The preliminary study done on voltage/frequency (V/f) characteristics for motors driving pumps and fans [4], should be generalized for various motors and various loads.

(2) In addition to the microprocessor control program, providing two additional commutations per quarter cycle [18], the program should be modified to provide four additional commutations per quarter cycle as well.

(3) It is already known that at lower frequencies, the harmonic currents become quite appreciable. Therefore, additional commutations are required to minimize these harmonic currents. On the other hand, at higher frequencies, the harmonic currents become insignificant.

A study is recommended to determine the frequency below which additional commutations are required.

(4) An overall efficiency may be estimated by considering inverter commutation losses as well as the recommendations above.

(5) A better power supply should be used in future prototype tests. The dc machines proved to have too much source impedance.

(6) Better types of commutating capacitors as well as filtering capacitors must be used. Special commutation capacitors have recently been introduced by European manufacturers.

REFERENCES

[1] Morton, W.R., "Economics of AC adjustable speed drives on pumps," IEEE Trans. Ind. Appl., Vol. IA-11, No. 3, pp. 282-286, May/June 1975.

[2] Tsivitse, P.J. and Klingshirn, E.A., "Optimum voltage and frequency for polyphase induction motors operating with variable frequency power supplies," IEEE Trans. Ind. Gen. Appl., Vol. IGA-7, No. 4, pp. 480-487, July/August 1971.

[3] Buschart, R.J., "Motor efficiency," IEEE Trans. Ind. Appl., Vol. IA-15, No. 5, pp. 507-510, Sept./Oct. 1979.

[4] Petursson, M. and Hewitt, N., "Efficiency maximization of an induction motor speed control system," A B.Sc. thesis presented to the Dept. of Elect. Eng., The University of Manitoba, April 1980.

[5] Brown Boveri Review, Vol. 66, No. 1, p. 9, Jan. 1979.

[6] B.D. Bedford and R.G. Hoft, Principles of Inverter Circuits, Chapter 7. John Wiley & Sons, New York, 1964.

[7] L.J. Jacovides,"Analysis of induction motor drives with a nonsinusoidal supply voltage using Fourier analysis," IEEE Trans. Ind. Appl., Vol. IA-9, No. 6, pp. 741-747, Nov./Dec. 1973.

[8] Patel, H.S. and Hoft, R.G., "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part I - Harmonic elimination," IEEE Trans. Ind. Appl., Vol. IA-9, No. 3, pp. 310-317, May/June 1973.

[9] Patel, H.S. and Hoft, R.G., "Generalized techniques of harmonic elimination and voltage control in thyristor inverters: Part II - Voltage control techniques," IEEE Trans. Ind. Appl., Vol. IA-10, No. 5, pp. 666-673, Sept./Oct. 1974.

[10] G.S. Buja and G.B. Indri, "Optimal pulsewidth modulation for feeding AC motors," IEEE Trans. Ind. Appl., Vol. IA-13, No. 1, pp. 38-44, Jan./Feb. 1977.

[11] Schonung, A. and Stemmler, H., "Static frequency changers with 'subharmonic' control in conjunction with reversible variable-speed AC drives," Brown Boveri Review, Vol. 51, pp. 555-576, Aug./Sept. 1964.

[12] Fiacco, A.V. and McCormick, G.P., Nonlinear programming: Sequential Unconstrained Minimization Technique. John Wiley and Sons, New York, 1968.

[13] Humphery, A.J., "Constant horsepower operation of induction motors," IEEE Trans. Ind. Gen. Appl., Vol. IGA-5, No. 5, pp. 552-557, Sept./Oct. 1969.

[14] Murphy, J.M.D., Hoft, R.G. and Howard, L.S., "Controlled-slip operation of an induction motor with optimum PWM waveforms," IEEE Conference on Electrical Variable Speed Drives, pp. 157-160, London, Sept. 25, 1979.

[15] Plunkett, A.B., "Direct flux and torque regulation in a PWM inverter-induction motor drive," IEEE Trans. Ind. Appl., Vol. IA-13, No. 2, pp. 139-146, March/April 1977.

[16] Plunkett, A.B. and Plette, D.L., "Inverter-induction motor drive for transit cars," IEEE Trans. Ind. Appl., Vol. IA-13, No. 1, pp. 26-37, Jan./Feb. 1977.

[17] Agarwal, P.D., "The GM high-performance induction motor drive system," IEEE Trans. Power Apparatus and System, Vol. PAS-88, No. 2, Feb. 1968.

[18] Au-Yeung, H., "Microporcessor control of inverter circuits using pulse width modulation scheme," A project presented to the Elect. Eng. Dept., The University of Manitoba, June 1980.

[19] Jerry J. Pollack, "Some Guidelines for the Application of Adjustable-Speed AC Drivers," IEEE Trans. On Industry Applications, Vol. IA-9, No. 6, pp. 704-710, November/December 1973.

APPENDIX A

SCR

C140(2N3649-53)

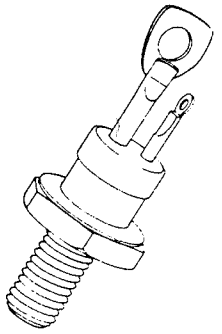
C141(2N3654-58)

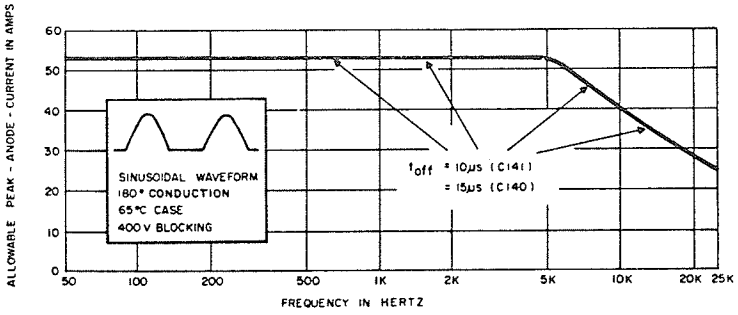
The General Electric C140 and C141 Series of Silicon Controlled Rectifiers are reverse blocking triode thyristor semiconductor devices designed primarily for high-frequency power switching applications which require blocking voltages up to 400 volts and load currents up to 35 amperes RMS, at frequencies up to 25 kHz.

For line commutated applications (phase control, AC switching) at power line frequencies, up to 35 amperes RMS, the following preferred SCR types are recommended: C35 (Pub. #160.20), and C137 (Pub. #160.45).

The C140 and C141 Series feature:

- Contoured junction surfaces for high-voltage stability
- Shorted emitters for high dv/dt (200V/μsec)
- Distributed gates for high di/dt (400A/μsec)





The improved dynamic characteristics and the interdynamic balance of these characteristics permit the operation of these General Electric SCR's up to 25 kHz with specified turn-off times and dv/dt maintained.

Equipment designers can use the C140 and C141 SCR's in demanding applications such as:

- Choppers
- Inverters
- Regulated power supplies
- Cycloconverters
- Ultrasonic generators
- High frequency lighting
- Sonar transmitters
- Induction heaters
- Radio transmitters

This specification sheet uses a simpligied and easy-to-use rating system which graphically presents:

- Case Temperature
- Peak Anode Current
- dv/dt and Turn-off Times

for rectangular and sinusoidal anode-current waveforms

MAXIMUM ALLOWABLE RATINGS

TYPE	DC FORWARD BLOCKING VOLTAGE V_{FO} (1) T_C = −65°C to +120°C	PEAK FORWARD VOLTAGE PFV (1) T_C = −65°C to +120°C	DC REVERSE VOLTAGE V_{RO} (1) T_C = −65°C to +120°C	NON-REPETITIVE PEAK REVERSE VOLTAGE (Half Sine Wave) V_{ROM} (non-rep) (1) T_C = −65°C to +120°C
C140F (2N3649) C141F (2N3654)	50 volts*	50 volts*	50 volts*	75 volts*
C140A (2N3650) C141A (2N3655)	100 volts*	100 volts*	100 volts*	150 volts*
C140B (2N3651) C141B (2N3656)	200 volts*	200 volts*	200 volts*	300 volts*
C140C (2N3652) C141C (2N3657)	300 volts*	300 volts*	300 volts*	400 volts*
C140D (2N3653) C141D (2N3658)	400 volts*	400 volts*	400 volts*	500 volts*

Turn-On Current Limit (See Chart 10) — 400 amperes per μsec*
RMS Forward Current, On-State — 35 amperes
DC Forward Current, On-State, T_C = 40°C — 25 amperes*
Peak Rectangular Surge Forward Current (5.0msec width, t_r = 50μsec) I_{FM} (surge) — 180 amperes*
I^2t (for fusing) — 165 ampere² seconds (for times ≧ 1.0 millisecond)
Peak Gate Power Dissipation, P_{GM} — 40 watts*
Average Gate Power Dissipation, $P_{G(AV)}$ — 1.0 watt*
Peak Reverse Gate Voltage, V_{GRM} — 10 volts*
Peak Forward Gate Current, I_{GFM} — 6.4 amperes*
Reverse Recovery Energy — 0.002 watt sec.
Storage Temperature, T_{stg} — −65°C to +150°C*
Operating Temperature, T_C — −65°C to +120°C*
Stud Torque — 30 Lb-in (35 Kg-Cm)

CHARACTERISTICS

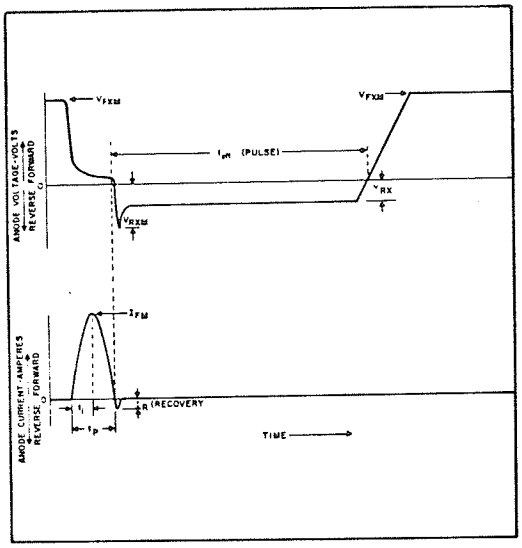
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
PULSE CIRCUIT COMMUTATED TURN-OFF TIME C140 (2N3649-53) C141 (2N3654-58)	t_{off} (pulse)	— —	— —	15* 10*	μsec μsec	See Charts 1 and 4. T_C = +115°C, I_{FM} = 100 amps, Approx. Sinusoidal current waveform (t_r = 1.0 μsec, t_p = 2.05 $^{+0.5}_{-0}$ μsec), No delay reactor, Pulse rep. rate = 400 Hz. V_{FXM} = Rated, V_{RXM} ≦ 200 volts, v_{RX} = 30 volts. Rate of rise of reapplied forward blocking voltage (dv/dt) = 200 volts/μsec (linear ramp). Gate supply: 20 volts open circuit, 20 ohms, 1.5 μsec square wave pulse, Rise time = 0.1 μsec max.
CONVENTIONAL CIRCUIT COMMUTATED TURN-OFF TIME C140 (2N3649-53) C141 (2N3654-58)	t_{off}	— —	— —	15* 10*	μsec μsec	T_C = +120°C, I_{FM} = 10 amps (50 μsec pulse), Rectangular current waveform, Test repetition rate = 60 Hz. V_{FXM} = Rated, V_{RXM} = Rated (see Chart 1), v_{RX} = 15 volts (see Chart 1). Rate of rise of current < 10 amps/μsec. Rate of fall of current ≦ 5 amps/μsec. Rate of rise of reapplied forward blocking voltage (dv/dt) = 200 volts/μsec (linear ramp). Gate bias = 0 volts, 100 ohms (during turn-off time internal).

CHARACTERISTICS (Cont.)

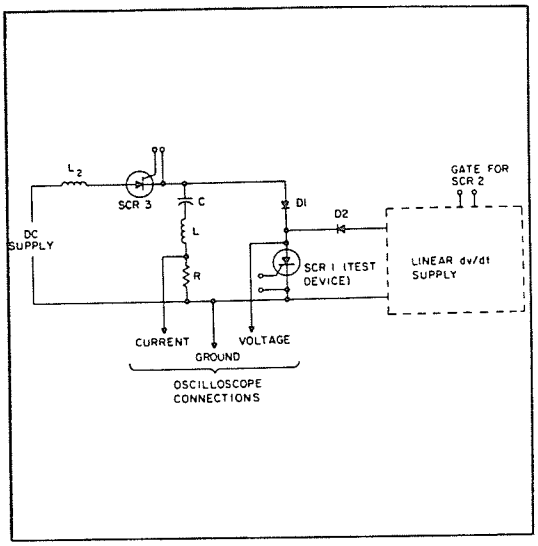
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
DC REVERSE OR FORWARD BLOCKING CURRENT (1)	I_{RO} or I_{FO}					$T_C = +25°C$
C140F (2N3649) C141F (2N3654)		—	1.0	6.0	mAdc	$V_{RO} = V_{FO} = 50V$ DC
C140A (2N3650) C141A (2N3655)		—	1.0	6.0	mAdc	$V_{RO} = V_{FO} = 100V$ DC
C140B (2N3651) C141B (2N3656)		—	1.0	6.0	mAdc	$V_{RO} = V_{FO} = 200V$ DC
C140C (2N3652) C141C (2N3657)		—	1.0	5.5	mAdc	$V_{RO} = V_{FO} = 300V$ DC
C140D (2N3653) C141D (2N3658)		—	1.0	4.0	mAdc	$V_{RO} = V_{FO} = 400V$ DC
DC REVERSE OR FORWARD BLOCKING CURRENT (1)	I_{RO} or I_{FO}					$T_C = +120°C$
C140F (2N3649) C141F (2N3654)		—	5.0	6.0*	mAdc	$V_{RO} = V_{FO} = 50V$ DC
C140A (2N3650) C141A (2N3655)		—	5.0	6.0*	mAdc	$V_{RO} = V_{FO} = 100V$ DC
C140B (2N3651) C141B (2N3656)		—	5.0	6.0*	mAdc	$V_{RO} = V_{FO} = 200V$ DC
C140C (2N3652) C141C (2N3657)		—	5.0	5.5*	mAdc	$V_{RO} = V_{FO} = 300V$ DC
C140D (2N3653) C141D (2N3658)		—	3.5	4.0*	mAdc	$V_{RO} = V_{FO} = 400V$ DC
GATE TRIGGER CURRENT	I_{GT}	—	80	180	mAdc	$T_C = +25°C$, $V_{FX} = 6$Vdc, $R_L = 4$ ohms
		—	150	500*	mAdc	$T_C = -65°C$, $V_{FX} = 6$Vdc, $R_L = 2$ ohms
GATE TRIGGER VOLTAGE	V_{GT}	—	1.5	3.0	Vdc	$T_C = +25°C$, $V_{FX} = 6$ Vdc, $R_L = 4$ ohms
		0.25*	—	—	Vdc	$T_C = +120°C$, V_{FX} = Rated, $R_L = 200$ ohms
		—	2.0	4.5*	Vdc	$T_C = -65°C$, $V_{FX} = 6$Vdc, $R_L = 2$ ohms
PEAK ON-VOLTAGE	V_F	—	1.8	2.05*	V	$T_C = +25°C$, $I_{FM} = 25A$ 1msec. pulse. Duty cycle = 1%
HOLDING CURRENT	I_{HO}					Anode supply = 24Vdc Initial forward current pulse, 0.1ms to 10ms wide, = 3.0A
		—	75	150	mAdc	$T_C = +25°C$. Gate supply: 10V open circuit, 20 ohms, 45 μsec min. pulse width.
		—	150	350*	mAdc	$T_C = -65°C$. Gate supply: 20V open circuit, 20 ohms, 45 μsec min. pulse width.
EFFECTIVE THERMAL RESISTANCE (DC)	θ_{J-C}	—	0.85	1.7*	°C/watt	
RATE OF RISE OF FORWARD BLOCKING VOLTAGE THAT WILL NOT TURN ON SCR	dv/dt	200*	—	—	volts/ μsec	$T_C = +120°C$. Gate open circuited. V_{FO} = Rated

(1) Maximum case to ambient thermal resistance for which maximum V_{FO}, V_{RO} ratings apply equals 5°C/watt.
* Indicates values included in Jedec Type Number Registration.

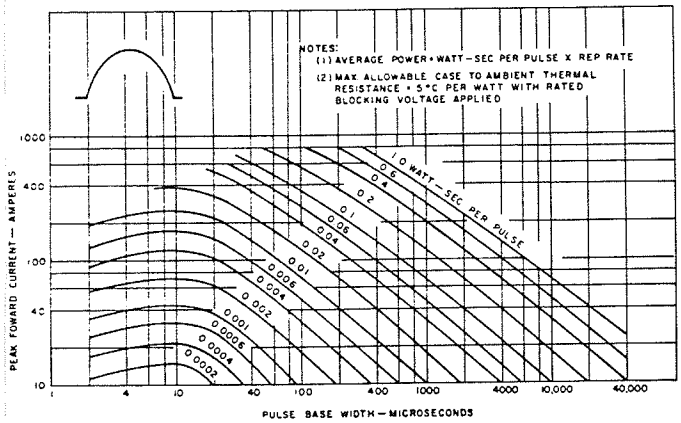
140, C141



1. WAVEFORMS FOR PULSE TURN-OFF TIME TEST

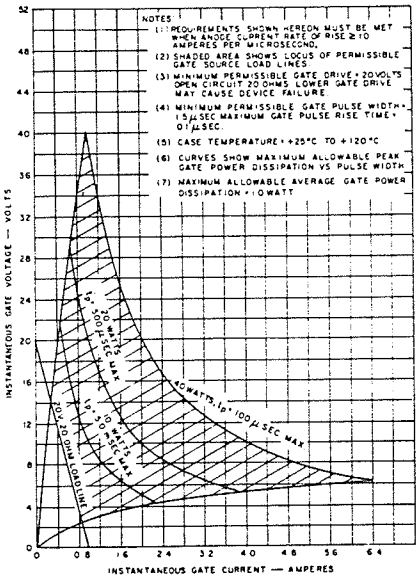


2. PULSE TURN-OFF TIME BASIC TEST CIRCUIT



3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

This chart provides a rapid means of determining anode dissipation with half-sine-wave pulses. Multiply the energy per pulse by the repetition rate to obtain average anode dissipation.



4. GATE TRIGGER REQUIREMENTS FOR HIGH FREQUENCY AND HIGH di/dt OPERATION

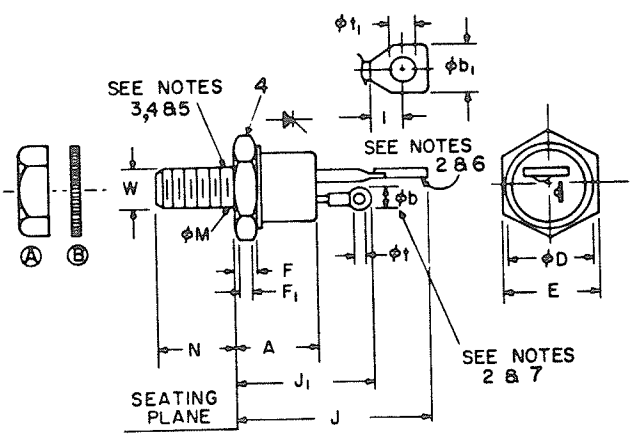
OUTLINE DRAWING
(COMPLIES WITH JEDEC TO-48)

NOTES:
1. Complete threads to extend to within 2½ threads of seating plane. Diameter of unthreaded portion .249" (6.32MM) Maximum, .220" (5.59MM) Minimum.
2. Angular orientation of these terminals is undefined.
3. ¼-28 UNF-2A. Maximum pitch diameter of plated threads shall be basic pitch diameter .2268" (5.76MM), minimum pitch diameter .2225" (5.66MM), reference: screw thread standards for Federal Service 1957, Handbook H28, 1957, P1.
4. A chamfer (or undercut) on one or both ends of hexagonal portions is optional.
5. Case is anode connection.
6. Large terminal is cathode connection.
7. Small terminal is gate connection.
8. Insulating kit available upon request.

A. ¼-28 steel nut, Ni. plated, .178 min. thk.

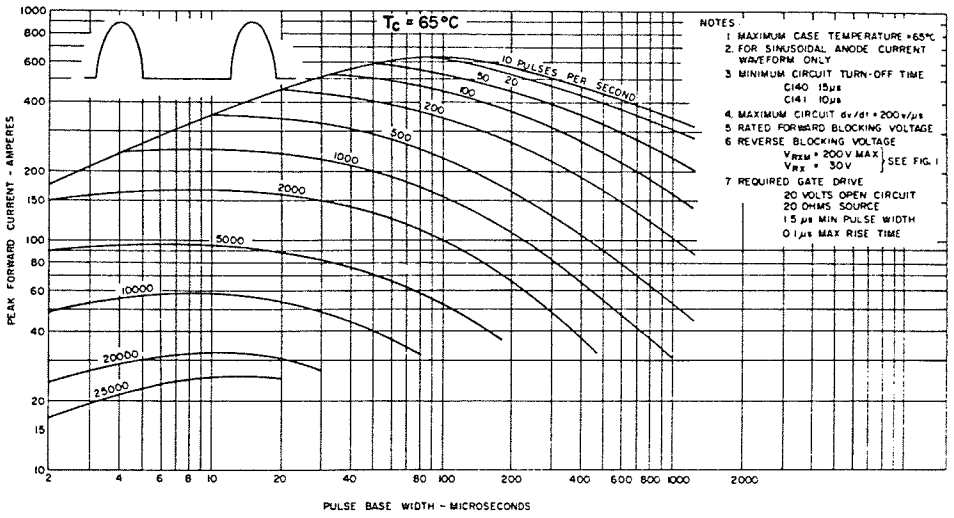
B. Ext. tooth lockwasher, steel, Ni. plated, .023 min. thk.

(COMPLIES WITH JEDEC TO-48)

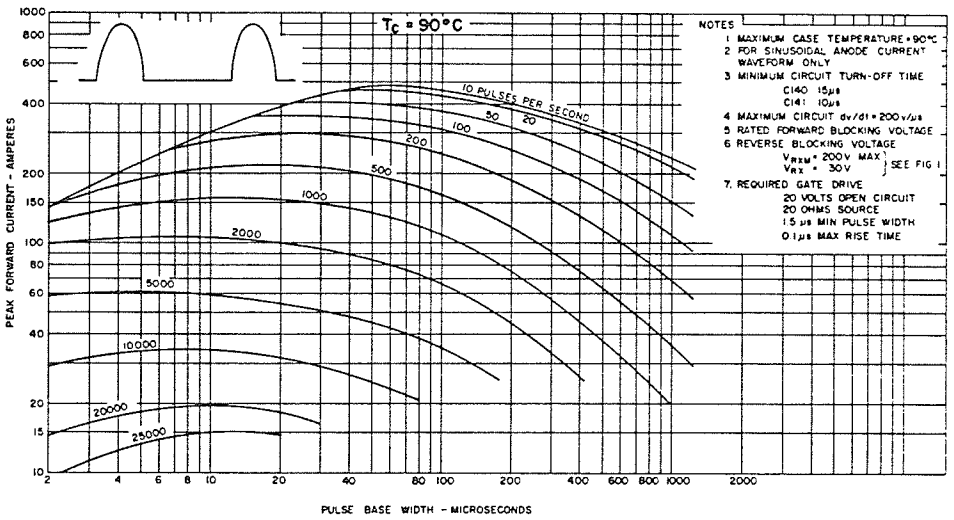


SYMBOL	INCHES MIN.	INCHES MAX.	MILLIMETERS MIN.	MILLIMETERS MAX.	NOTES
A	.330	.505	8.38	12.83	
øb	.115	.140	2.92	3.56	2
$øb_1$	.210	.300	5.33	7.62	2
øD		.544		13.82	
E	.544	.562	13.82	14.27	
F	.113	.200	2.87	5.08	4
F_1	.060		1.52		
J		1.193		30.30	
J_1		.875		22.23	
l	.120		3.05		
øM					1
N	.422	.453	10.72	11.51	
ot	.060	.075	1.52	1.91	
ot_1	.125	.165	3.18	4.19	
W					3

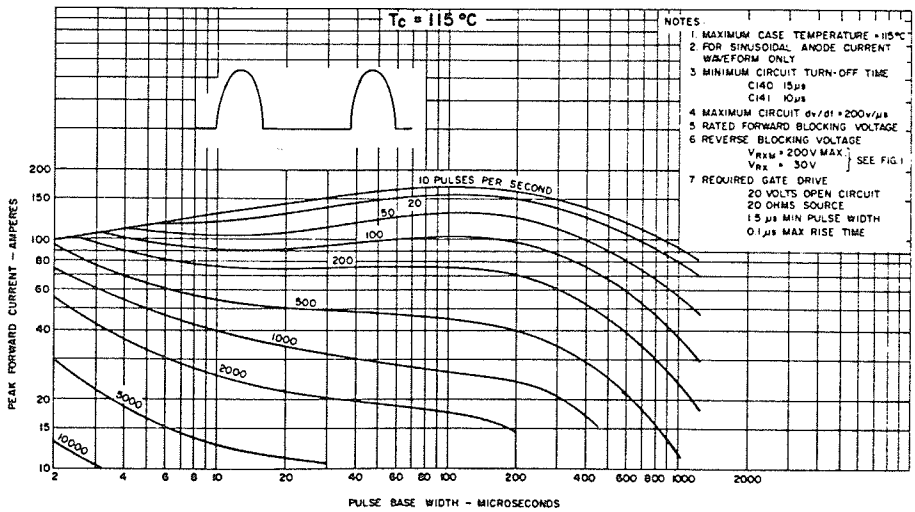
SINE WAVE DATA



5. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT vs PULSE WIDTH (T_C = 65°C)

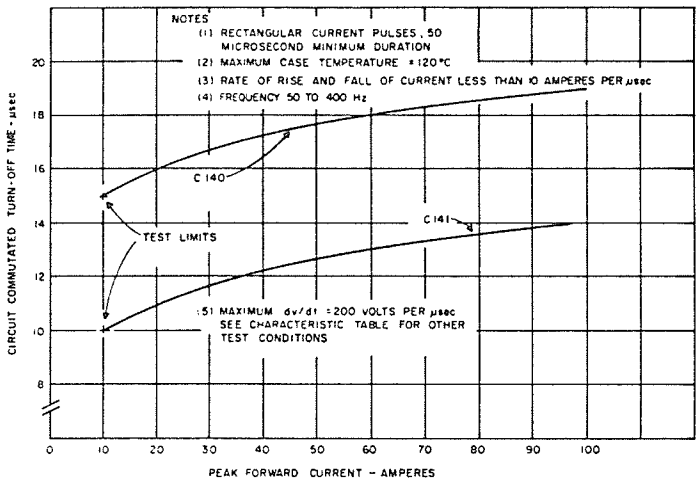


6. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT vs PULSE WIDTH (T_C = 90°C)

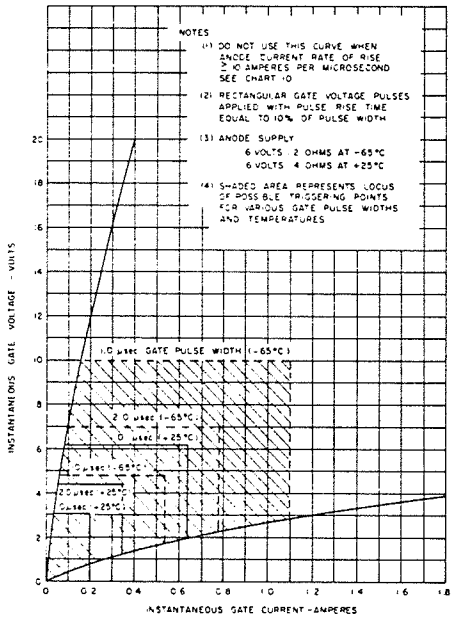


7. MAXIMUM ALLOWABLE PEAK FORWARD CURRENT vs PULSE WIDTH (T_C = 115°C)

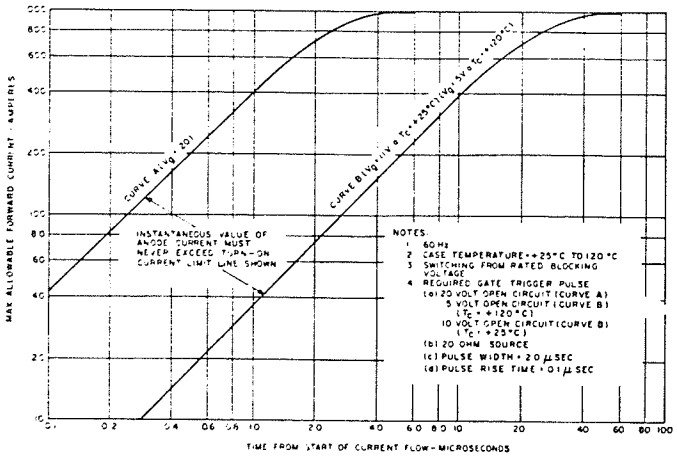
Charts 5, 6 and 7, for three case temperatures 65°C, 90°C, and 115°C, give the maximum value of peak forward current at which the specified turn-off time and dv/dt still apply. The specified gate drive requirements *must* be adhered to.



8. MAXIMUM CONVENTIONAL CIRCUIT-COMMUTATED TURN-OFF TIME vs PEAK FORWARD CURRENT, ON-STATE



9. PULSE GATE TRIGGER CHARACTERISTICS



10. TURN-ON CURRENT LIMIT

This chart gives the guaranteed maximum turn-off time of the C140 and C141 as a function of the forward current. The use of this chart is necessary for rectangular anode current pulses of the specified pulse width and frequency.

Specification Sheets

140.12	1N3879 Series (6 amp) Fast Recovery Diode
140.22	1N3889 Series (12 amp) Fast Recovery Diode
140.23	A28 Series (12 amp) Very Fast Recovery Diode
140.47	1N3899 Series (20 amp) Fast Recovery Diode
140.48	1N3909 Series (30 amp) Fast Recovery Diode
145.55	A96 Series (250 amp) Fast Recovery Diode
160.35	C140 Series (35A) 50-400V High Speed SCR
160.39	C144 Series (35A) 500-800V High Speed SCR
170.35	C154-7 Series (110 amp) High Speed SCR
170.36	C158, 9 Series (110 amp) High Speed SCR
170.37	C385 Series (250 amp) High Speed SCR
170.38	C358 Series (225A) High Speed SCR
170.42	C395 Series (550A) up to 600V, High Speed SCR
170.44	C388, C387 Series (550A) High Speed SCR
170.45	C398, C397 Series (700A) High Speed SCR
170.53	C185 Series (235 amp) High Speed SCR
170.57	C354, 5 Series (115 amp) High Speed SCR
170.76	C506 Series (625 amp) High Speed SCR
170.80	C510 Series (625 amp) High Speed SCR

Application Notes

200.38	"Application of Fast Recovery Rectifiers"
200.41	"Simple Circuits For Triggering SCR's Into Fast-Rising Load Currents"
200.42	"Commutation Behavior of Diffused High Current Rectifier Diodes"
200.49	"A Low Cost Ultrasonic Frequency Inverter Using A Single SCR"

Technical Paper Reprints

660.13	"The Rating and Application of SCR's Designed for Switching at High Frequencies"
660.14	"Basic Magnetic Functions in Converters and Inverters Including New Soft Commutations"
660.15	"SCR Inverter Commutated By An Auxiliary Impulse"
660.16	"An SCR Inverter With Good Regulation and Sine Wave Output"

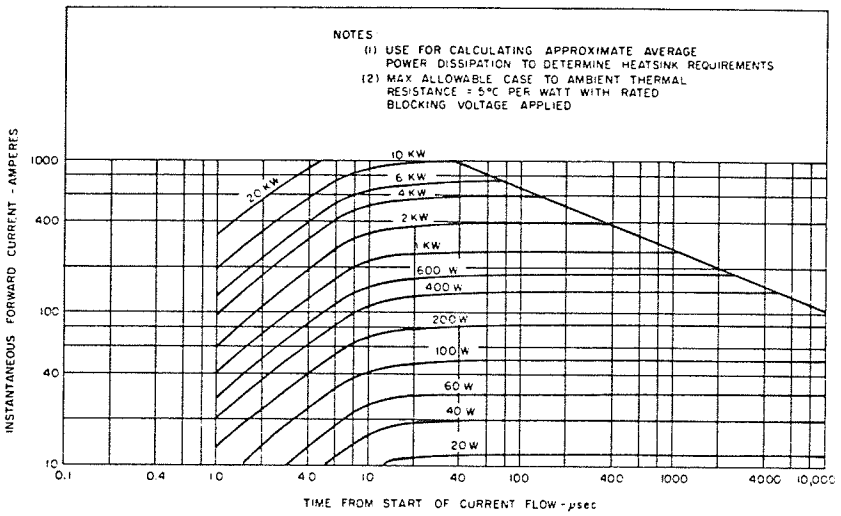
Seminar Notes

671.4	"The Widening World of The Fast Recovery Rectifier Diode"
671.15	"The Amplifying Gate SCR"

*For copies of any published information, please order by decimal publication number from: General Electric Company, Distribution Services, 1 River Road, Schenectady, N. Y. 12305.

In no circumstances may the SCR anode current waveform, when plotted in this curve, cross the turn-on current limit line. If it does, the SCR may be destroyed. Two lines are given; one for required gate drive in high di/dt applications and the other for gate drive that will just turn the SCR on. The user must take care that, in a circuit capable of producing high di/dt anode current, no gate pulses of insufficient magnitude (due to noise for example) triggers, and thus possibly damages, the SCR.

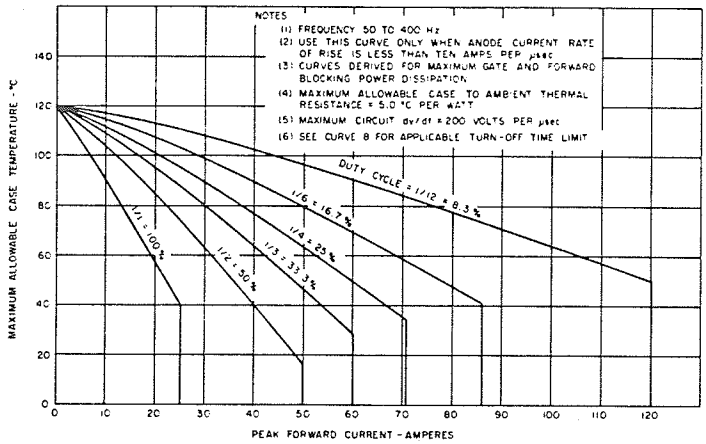
LOW REPETITION RATE DATA



11. INSTANTANEOUS FORWARD POWER DISSIPATION

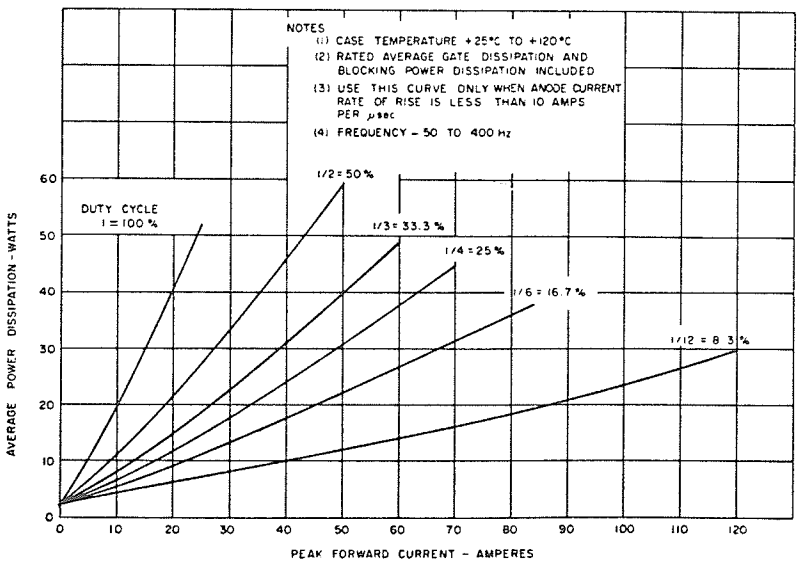
This chart gives the instantaneous power dissipated within the SCR as a function of time from start of current flow and the instantaneous value of forward anode current. Used as follows, this chart yields average dissipation information for any anode current waveshapes:

1. Plot the anode current waveform on this chart.
2. On linear paper, replot instantaneous forward power dissipation versus time. The area under the curve gives watt seconds of energy dissipated per anode current pulse.
3. Multiply the energy by the repetition rate to give average power dissipation.



12. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM

This chart is used when the SCR is carrying rectangular current with no significant turn-on switching duty at a repetition rate between 50 and 400 pulses per second.



13. AVERAGE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM

This chart provides a rapid means of determining SCR dissipation with low values of di/dt. It is applicable only between 50 Hz and 400 Hz.

HOW TO USE THIS SPECIFICATION SHEET

EXAMPLE I. (High Frequency Sinusoidal Pulse)

Problem:

Find the maximum allowable average anode current that can be carried by a C141 if the pulse is 50 μseconds wide and the repetition rate is 5000 Hz. The case is held at 80°C. What is the dissipation in the SCR? Find the maximum permitted thermal resistance between case and cooling air at 45°C. Assume the gate and blocking losses total 1 watt.

Answer:

From Chart 5 (65°C) the maximum permitted peak current at 5000 Hz, 50 μsec pulse width is 72 amperes; Chart 6 (90°C), 45 amperes; Chart 7 (115°C), 10 amperes. Interpolation gives the permitted peak current at 80°C as 55 amperes peak.

$$\text{The average current} = I_{pk} \times \frac{2}{\pi} \times \frac{\text{Pulse Width}}{\text{Pulse Period}}$$

$$= 55 \times \frac{2}{\pi} \times \frac{50}{200} = 8.8 \text{ amps average}$$

From Chart 3 at 50 μseconds pulse width and 55 amperes peak current the energy dissipated per pulse is 0.004 watt-seconds per pulse. The average anode dissipation is 0.004 × 5000 = 20 watts.

From this information the heatsink can be chosen using the equation:

$$\text{Maximum case to cooling fluid thermal resistance} = \frac{\text{Case Temperature} - \text{Cooling Fluid Temp.}}{\text{Anode Dissipation} + \text{Gate \& Blocking Losses}}$$

$$= \frac{80 - 45}{20 + 1} = 1.7°\text{C/watt.}$$

Note that a turn-off of 10 μseconds and a dv/dt of 200 volts/μsecond can be applied concurrently to the C141 at the above current and temperature conditions.

EXAMPLE II. (Low Frequency, Low di/dt Pulse)

Problem:

A C140 is carrying a 20 amp rectangular pulse, 833 μseconds wide at a repetition rate of 400 pulses per second. The initial di/dt is 5 amps per μsecond. What is the maximum allowable case temperature? What is the power dissipation? What turn-off time and dv/dt may be applied to the C140?

Answer:

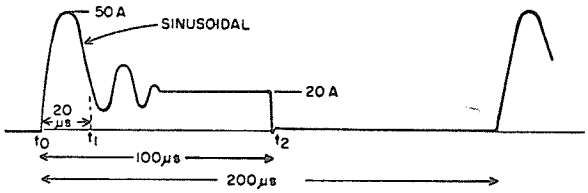
An 833 μsecond pulse in a 2.5 ms period gives a duty cycle of $\frac{833}{2500} \times 100 = 30\%$. Chart 12 shows that with this duty cycle a 20 amp rectangular pulse has a maximum allowable case temperature of 98°C. Chart 13 gives the total dissipation as 13.5 watts.

From Chart 8, 20 amps forward current permits a turn-off time of 16 μseconds and a dv/dt of 200 volts/μsecond to be applied concurrently.

EXAMPLE III. (High Frequency, Irregular Pulses)

Problem:

What is the maximum allowable case temperature for a C141 carrying the following anode current waveform: What turn-off time and dv/dt may be applied?



Answer:

No rigorous method has yet been developed for handling this case. The following method is approximate only but provides a conservative answer.

The di/dt of the initial pulse imposes the most severe strain on the SCR during the cycle. Use the initial half cycle to establish a case temperature and then lower the case temperature by an amount = effective thermal resistance (DC) of the SCR × wattage dissipated during the rest of the cycle (t_1 to t_2) to establish the maximum permitted case temperature.

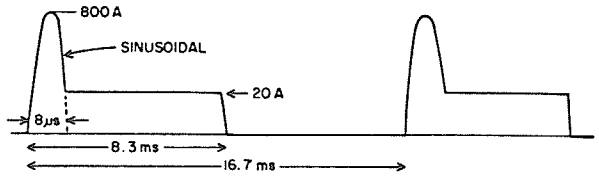
The average anode dissipation (time t_1 to t_2) can be found by means of Chart 11 (for method see Example IV). The energy dissipated per pulse is 0.0032 watt-seconds. The average anode dissipation = 0.0032 watt-seconds × 5000 pulses per second = 16 watts.

Chart 6 shows that a 5000 Hertz, 50 ampere, 20 μsecond pulse requires a case temperature of less than 90°C. Subtract from this case temperature a temperature of 1.7 °C/watt × 16 watts = 27°C to give the maximum permitted case temperature, with the given waveform, of 90°C − 27°C = 63°C. As the end of the current pulse is rectangular, Chart 8 will have to be used to find the required turn-off time which is 16μseconds. The concurrent dv/dt is 200 volts/μsecond.

EXAMPLE IV. (Low Frequency, Irregular Pulses With High Initial di/dt)

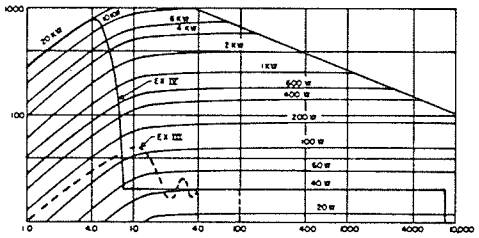
Problem:

What is the maximum allowable case temperature for a C141 carrying the following anode current waveform?

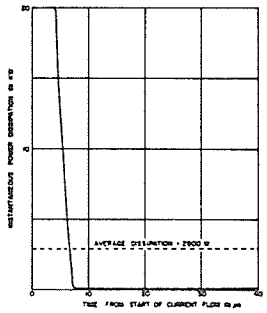


Answer:

Check the initial di/dt by plotting the first 10 μseconds of current flow on Chart 10. The waveform is found to be within safe limits provided that the high gate pulse shown on Chart 4 is used. Note that an inadequate gate pulse could destroy the SCR. To find the anode dissipation, plot the anode current waveform on Chart 11.



Replot the intersections of anode current with the instantaneous power lines. In this case it is convenient to replot the first 40 μseconds of current flow separately in order to use a convenient scale.



By graphical integration, the energy per pulse for the first 40 μseconds is seen to be 0.12 watt-second. To this must be added the energy dissipated during the rectangular portion of the pulse which is 40 watts × 8.3 ms = 0.33 watt-seconds. Thus the total energy dissipated per pulse is 0.12 + 0.33 = 0.45 watt-seconds. The average dissipation due to anode current flow is 0.45 watt-seconds × 60 pulses per second = 27 watts.

As the repetition rate is within the limits of 50 to 400 Hz a convenient way of ascertaining the maximum permitted case temperature is to convert the high di/dt irregular waveform to a low di/dt rectangular pulse with the same dissipation.

From Chart 13, a 27 watt, 50% duty cycle pulse gives an average anode current of 25 amperes peak.

From Chart 12, a 25 ampere, 50% duty cycle current gives a maximum allowable case temperature of 75°C.

Note: For repetition rates lower than 50 Hz, the temperature excursion within the SCR each cycle becomes too high for the use of Charts 12 and 13. The procedure for dealing with these very-low-frequency pulses is discussed in the General Electric SCR Manual, 3rd Edition, Chapter 3.

APPENDIX B

APPENDIX B

Power Supplies

(1) LAMBDA Power Supply, Model LP410FM:

- provides 5 V
- two of them were used to provide 5 V and -5 V

(2) HEWLETT PACKARD Power Supply, Model 6215A:

- provides 12 V.

Measuring and display equipment

(1) DIGITIZING OSCILLSCOPE : TEKTRONIX 5223.

(2) DUAL TRACE AMPLIFIER : TEKTRONIX 5A48.

(3) DIFFERENTIAL AMPLIFIER : TEKTRONIX 5A21N.

(4) STORAGE OSCILLSCOPE : TEKTRONIX 7613.

(5) DUAL TRACE AMPLIFIER : TEKTRONIX 7A18.

(6) CURRENT PROBE : P6021.

(7) DIFFERENTIAL VOLTAGE PROBE : P6105 (Times 10).