AN AUTOMATED TESTING TECHNIQUE FOR MHO RELAYS USING A MINICOMPUTER

A Thesis

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"AN AUTOMATED TESTING TECHNIQUE FOR MHO RELAYS USING A MINICOMPUTER"

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ABSTRACT

A distance relay as with other protective equipment is normally tested during its factory and initial commissioning period manually, using the conventional test bench method [1]. With the advent of low-power-requirement solid state relays and minicomputers, there arises a possibility of automating the relay testing technique.

Such a test program has been written to assess the static and dynamic characteristic of a distance relay. An experimental Mho distance relay was used in the development of the test technique.

The test method is highly automated with all data handling and processing automatically performed. The test results in the forms of the relay characteristic locus and operating time are finally displayed on the graphic display terminal of the minicomputer.

The proposed automated test technique can lead to valuable savings in time and expense and as well as increased flexibility over the conventional method.

ACKNOWLEDGMENTS

The author gratefully acknowledges the help and supervision he has received from Professor G.W. Swift during the course of this study without whose guidance and encouragement this work would not have been possible. The author also wishes to express his sincere appreciation to the Dean, Professor L.M. Wedepohl, for the numerous invaluable advice and suggestions. Last, but not least, the author wishes to acknowledge his gratitude to Professor Lehn, Mr. N.J. Morphy, and Mr. A.W. De Groot of the Electrical Engineering Department and Mr. Jim Roik from the Manitoba Hydro for many helpful discussions.

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LIST OF SYMBOLS

C(I)	The magnitude of current at the I^{th} sampling instants.
C.T	Current transformer.
C_{max}	Maximum number of cycles of simulated test waveform.
d/dt	First differentiation with respect to time.
E	Source voltage.
I	Integer number between 1 and 20 for number of sample.
I_C	Magnitude of the exponential component of fault current at time equal zero.
I_F	Fault current.
I_M	The amplitude of the steady state fault current.
I_T	Transient component of the fault current.
K	The constant of the polarizing voltage.
L_2	The inductance of the fault impedance.
m	Number of samples per cycle.
N	Number of cycles.
N_T	The number of cycle at which the relay trips.
P.T.	Potential transformer.
R_1	Resistance of source impedance.
R_2	Resistance of fault impedance.
R_3	Fault resistance.
S	Input to relay.

t	Time variable.
T_I	Sampling time.
T	Time constant of the system.
$V(I)$	Magnitude of voltage at the sampling instant.
$V(N)$	Amplitude of the voltage at the N^{th} cycle.
V_o	Initial value voltage at N = 0.
V	Input relay voltage.
V_P	Polarizing voltage.
W	Frequency in radians/sec.
X	Trip signal of relay.
X_1	Reactance of the source impedance.
X_2	Reactance of the fault impedance.
$Z(N_T)$	Impedance seen by the relay.
Z_F	Impedance from the relay position to fault not including the fault resistance.
Z_L	Line impedance.
Z_N	Replica impedance of the relay.
Z_S	Source impedance.
Z_T	Total system impedance.
α	System phase angle.
β	$\theta - \alpha$
γ	Multiplication factor for voltage in the static test.
θ	Phase angle of the source voltage.
ϕ	Phase angle between the inputs of the comparator.

CHAPTER 1

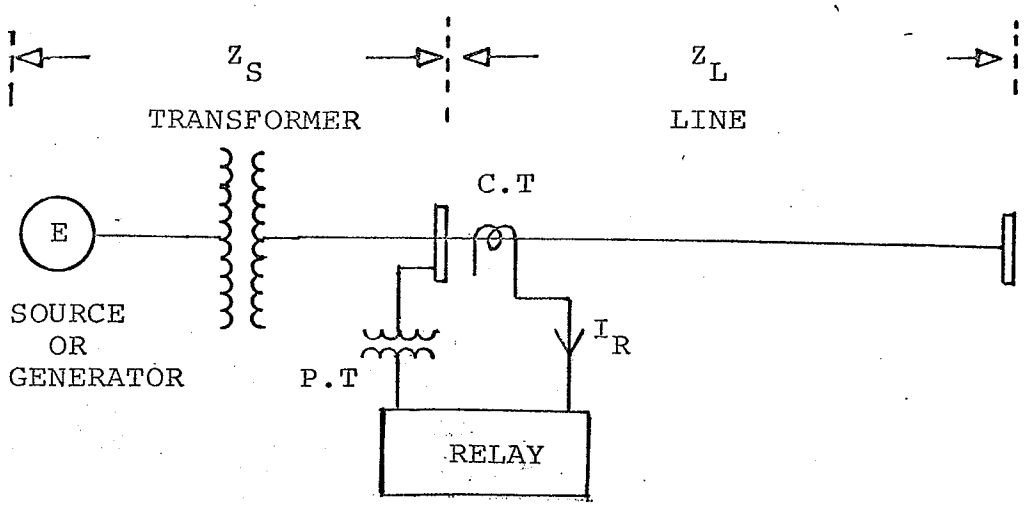
INTRODUCTION

Distance relays such as the Mho relays are used to protect a section of a power system transmission line. The Mho relay measures the distance of the inception of a fault from the terminal point by monitoring the impedance of the line and comparing it with a preset value in the relay. The preset value of the replica impedance of the relay corresponds to the impedance of the section of the line under protection. The relay recognises the occurrence of a fault on the line when the impedance it monitors falls to a value less than the preset value. Subsequently, the relay initiates a trip signal to the circuit breaker which opens the faulty line. In this way, the faulty line is prevented from possible destruction due to the high fault current. The removal of the faulty line may also prevent the system from swinging to instability. A typical protection scheme using a Mho relay is shown in Figure 1.1 (a) and (b).

1.1 Principle and Characteristic of a Static Mho Relay

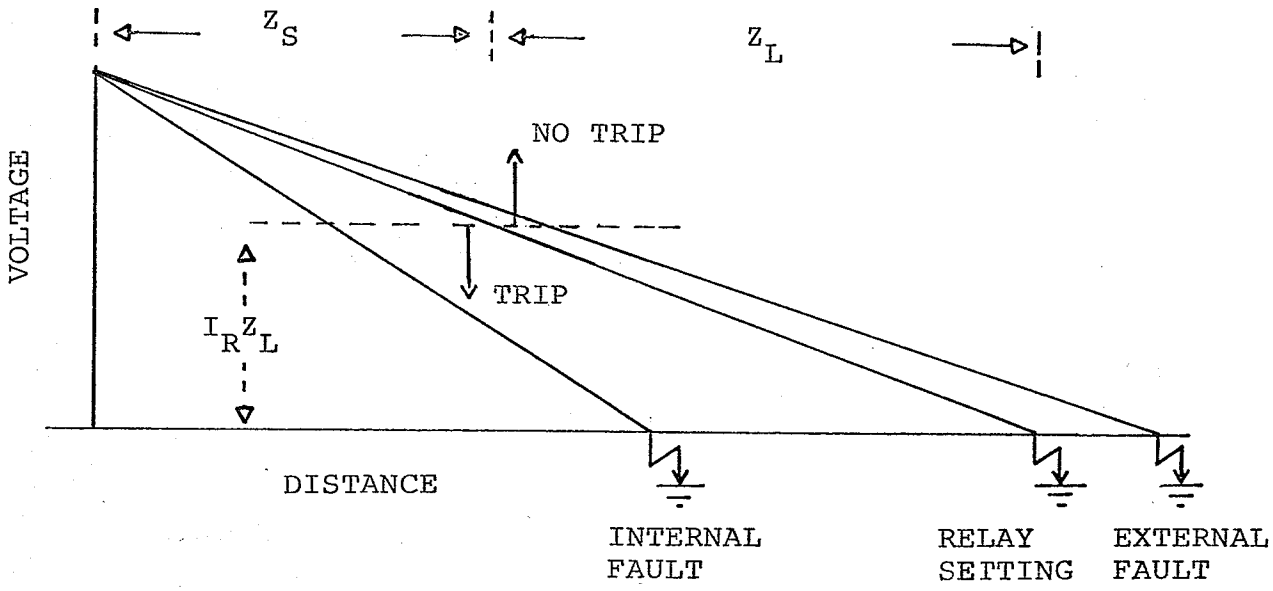
1.1.1 Unpolarised Mho Relay

The characteristic of a Mho relay was first introduced by A.R. Van C. Warrington [2]. On an impedance diagram, the Mho



An example of transmission line protection scheme using a Mho distance relay

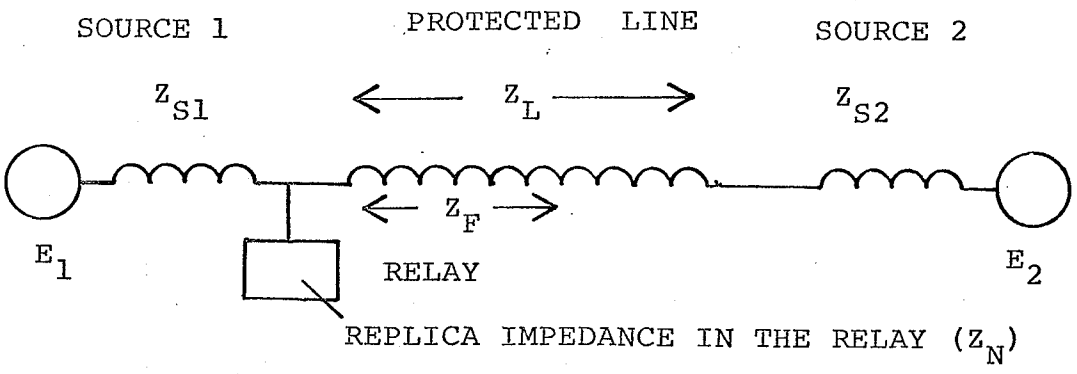
(a)

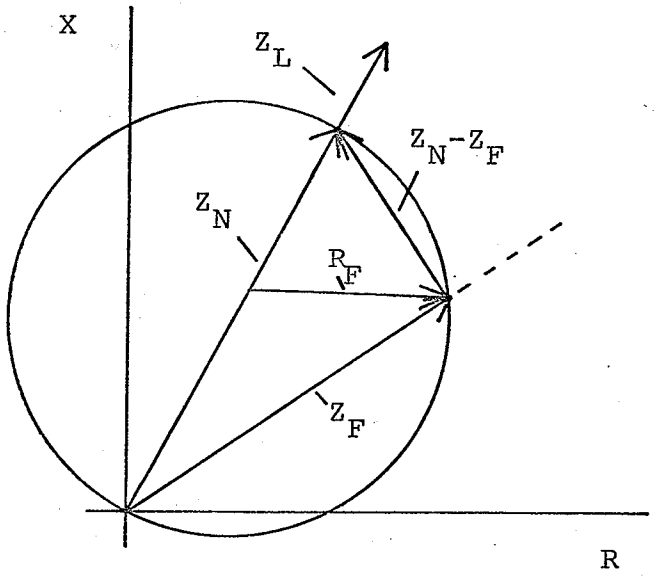


Principle of impedance distance measurement (voltage profile from source to fault)

(b)

Fig. 1.1





The theoretical characteristic of an unpolarized relay

Fig. 1.2

characteristic is a circle passing through the origin as shown in Fig. 1.2. The area which is inside the circle represents the trip zone and outside the no trip zone.

The Mho characteristic can be realised by either using a phase or an amplitude comparator. In a typical Mho relay using a phase comparator, the two inputs to the relay are

$$S_1 = V \tag{1.1}$$

$$S_2 = I_R Z_N - V \tag{1.2}$$

where

S_1 and S_2 are inputs to the comparator;

V is the voltage at the relay;

I_R is the input current to the relay;

Z_N is the replica impedance, a resistance-plus-inductance built into the relay and through which I_R is passed, (e.g., Z_N = 80% of Z_L); and

Z_F is the impedance from the relay to a fault location including the arc resistance.

The phase comparator measures the phase between the two inputs to the relay and initiates relay operation when the phase angle falls to less than ninety degrees (90^o). Thus, the criterion of operation of the relay is

where $$\overline{\Pi}/2 \leqslant \phi \leqslant \overline{\Pi}/2$$

ϕ is the phase angle between the inputs of the comparator. Such a criterion of operation as illustrated in Fig. 1.2 gives the familiar circular characteristic of a Mho relay.

1.1.2 Polarized Mho Relay

The principal aspect of a polarized Mho relay is that it has an extra memory element incorporated into the device.* The memory element holds the voltage phase information for a few cycles after an inception of a fault on the line.

Without a memory element, a relay may fail to operate properly for a close-in or terminal fault since the characteristic of an unpolarized Mho relay near the origin is a point of an uncertainty. The point of uncertainty is removed from the origin when the Mho relay is polarized. The inputs to the phase comparator of a polarized Mho relay are

$$S_1 = V + V_p \tag{1.3}$$

$$S_2 = I_R Z_N - V \tag{1.4}$$

where

V_p is the polarizing voltage from the memory element.

The polarizing voltage (V_p) ensures that the phase information of the relay voltage prior to the fault is maintained for several cycles after the inception. The voltage feeding the relay which is obtained through the voltage transformer, may be reduced to zero for close-in fault but the memory element provides the necessary phase information in a polarized Mho relay.

---

* "Sound phase polarizing" where the polarizing voltage is derived from the healthy phases of the line is another commonly used technique.

Suppose the polarizing voltage is given by the following equation [3]

$$V_p = KE$$

where

K may be complex and E is the source voltage.

The inputs to the phase comparator of the polarized Mho relay become

$$S_1 = V + KE$$

$$= I_R(Z_F + KZ_S + KZ_F) \qquad (1.5)$$

$$S_2 = I_R Z_N - V \qquad (1.6)$$

where

Z_F is the line impedance from relay to fault and

Z_S is the source impedance.

Dividing equations (1.5) and (1.6) by current (I_R) results in the following equations:

$$S_1' = KZ_S + (1 + K)Z_F \qquad (1.7)$$

$$S_2' = Z_N - Z_F \qquad (1.8)$$

Assuming (1 + K) is real, it is apparent that the characteristic of the polarized Mho relay [3] is a circle whose diameter is defined by points

$$Z_F = Z_N$$

and

$$Z_F = -(K/(1 + K)Z_S)$$

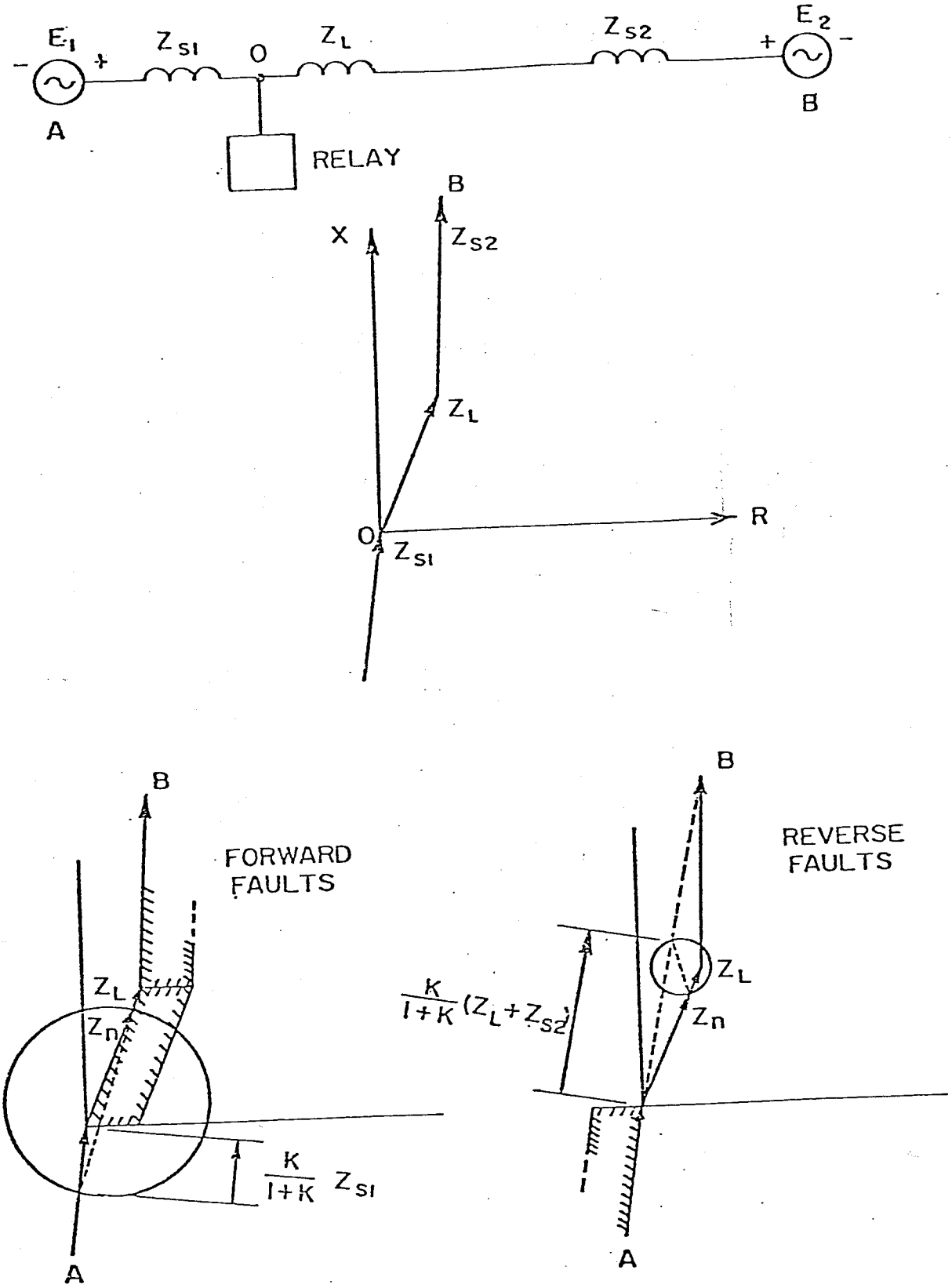


Illustration of the characteristics of a polarized Mho relay for the forward and reverse faults.

Fig. 1.3

In his work, Wedepohl [3] has also shown that for a reverse fault, the circle has diameter defined by points

$$Z_F = -Z_N$$

and

$$Z_F = -(K/(1 + K)Z_S$$

The circular characteristics of the polarized Mho relay for the forward and reverse faults are shown in Fig. 1.3.

1.2 Performance Criteria of a Static Mho Relay

In general, the performance of a static relay is expressed in terms of [3]

a) its immunity to surges

b) its static and dynamic characteristics .

The surge test attempts to establish the relay's immunity to power system surges such as those caused by switching and lightning.

The static performance test examines the characteristic of the relay for different values of current levels. This test would assess the tendency of the relay characteristic to be deformed at low current levels. The relay's accuracy and operating time under transient fault conditions are investigated too. This is normally pursued using the so-called dynamic test.

1.3 Conventional Testing Method

The conventional testing technique [1] which is used for a relay performance test was first introduced by Hamilton and Ellis [12]. The test procedure has to be done manually on a test bench. All test

parameters such as voltage, current, phase angles and trip conditions have to be recorded and processed manually. Such a task can indeed be laborious, time consuming and expensive too.

In the static test, the current is simply kept constant, but the voltage is decreased manually until the relay trips. The procedure is repeated for different phase angles so that the circular characteristic can be obtained.

In the dynamic test, the test waveforms representative of typical fault conditions have to be generated under a variety of conditions such as line length, line angle, fault resistance, source impedance and d.c. offset conditions. This could be an added cost factor to the test expenses. The measurement of test parameters is more complicated since the operating time of the relay needs also to be measured and recorded too.

Hence present testing techniques are tedious, time consuming and expensive and as well may not accurately assess the performance of a modern Mho relay.

1.4 Computer-aided Methods

Paul, Wright and Cavero [11] introduced a programmable testing technique to test a power system protective equipment. The technique stores simulated fault waveforms on an analogue system analyser and later the waveforms are reproduced to test distance relays or any other protective equipment.

The programmable testing equipment is not capable of automatic data handling and processing. All measurements and processing of parameters have to be done manually. It should be noted that the

whole sequence of the testing procedure is not integrated. Input test waveforms in the form of fault current and voltage have to be generated and stored in one locality and reproduced for testing somewhere else.

The proposed automated method in this thesis attempts to alleviate the shortcomings of the conventional method and that proposed by Paul, Wright and Cavero. The new automated testing technique originates from the realisation that the new modern electronic and solid state relay need only to be provided with information. The operating power requirement is provided separately and at much reduced level. The idea leads to the possible application of the minicomputer to relay testing techniques.

The fault condition is simulated in the computer. Through the computer interface system, the test waveforms are applied to the relay on line and the trip signal is fed back to the computer. All test data are handled and processed automatically. Hence the characteristic of the relay can be plotted automatically on the computer graphic terminal, permitting the performance of the device under test (D.U.T.) to be assessed.

CHAPTER 2

STATIC PERFORMANCE TEST

2.1 Brief Description

The test voltage and current waveforms of the static or the quasi-steady stage are assumed to be sinusoidal in nature. This assumption is consistent with the conventional test-bench method. The test waveforms are simulated in the computer and are applied to the relay via the 'Digital to Analogue Converter' (D/A) of the computer.

In order that the impedance change slowly from a no-trip value, the test current waveform is kept constant at a specified value while the voltage is decreased exponentially. The voltage has the following expression

$$V(N) = V_0(1 - \gamma)^N \qquad (2.1)$$

where

$V(N)$ is the amplitude of the voltage at N^{th} cycle,

γ is a small constant, e.g., 0.02, and

V_0 is the initial value of voltage at N = 0.

It can be easily shown that equation (2.1) has also the following recursive form

$$V_{(N+1)} = V_{(N)} * (1 - \gamma) \qquad (2.2)$$

where

$V_{(N+1)}$ is the voltage amplitude at the $(N+1)^{th}$ cycle, and

$V_{(N)}$ is the voltage amplitude at the $(N)^{th}$ cycle.

The expression in equation (2.2) is used in the test program to simulate the exponentially decreasing voltage waveforms.

The trip signal emanating from the relay is fed back to the computer through the 'Analogue to Digital Device' of the computer. If the relay trips, the computer is programmed to calculate the apparent impedance seen by the relay according to the following equation

$$Z(N_T) = \frac{\text{Magnitude of voltage at } N_T^{th} \text{ cycle}}{\text{Magnitude of current at } N_T^{th} \text{ cycle}}$$

$$= \frac{V_0(1-\epsilon\gamma)^{N_T}}{V_0(1C_0\quad)^{N_T}}$$

where

N_T is the cycle number at which the relay trips;

C_0 is the specified level of current; and

$Z(N_T)$ is the impedance seen by the relay at tripping.

The impedance seen by the relay is assumed to be negligible if the relay does not trip.

Subsequently, the computer transfers the impedance information on the graphic display terminal. The procedures is repeated automatically for different phase angles between current and voltage waveforms until the whole circular locus characteristic of the relay is displayed.

2.2 Description of System Architecture and Software

2.2.1 System Architecture

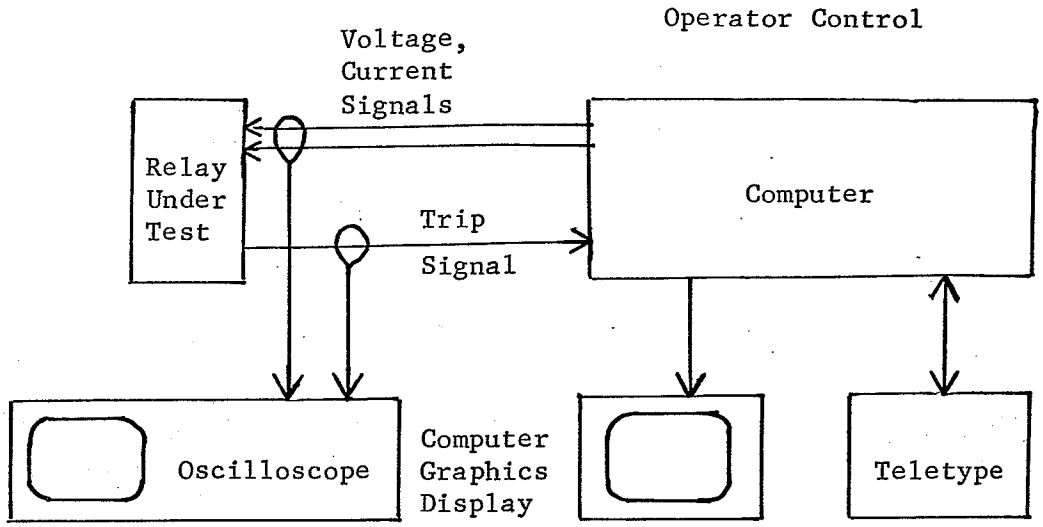
The computer is a Digital Equipment Corporation PDP-11/40 [4,5,6]. The simplified system block diagram is shown in Fig. 2.1. The PDP 11/40 minicomputer which is available at the University of Manitoba's Electrical Engineering Department, has a Central Processing Unit (CPU), Core Memory, a Unibus, a Disc storage, a LA 30 Decwriter, a CRT screen GT 40, and a Laboratory peripheral system. Further illustrations of test system are shown in Fig. 2.2.

The Unibus is the principal communication medium of the computer system peripherals. Communication between any two devices is in the form of a 'Master-Slave' relationship. All device peripherals can control the Unibus and hence can communicate with each other without the intervention of the CPU. When the Unibus is relieved of its control, the Central Processor performs other internal routines such as mathematical and logical operations.

The minicomputer has a 16K core memory. Of this, the operating system uses 6K of memory locations. The remaining 10K is available for the user.

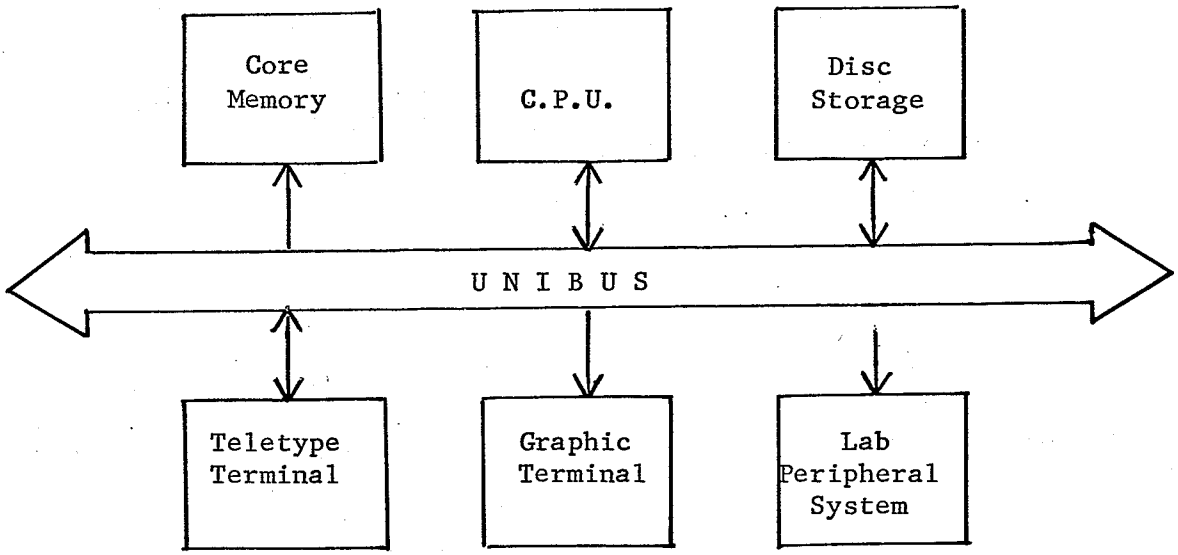
The logical and mathematical operations are performed in the Central Processor. It has eight 16 bit general purpose registers. The sixth and seventh registers are known as the stack pointer (SP) and the program counter (PC) respectively. The other six registers are available for normal programming usage. In addition, there are over four hundred hardwired instructions available.

Many devices in the computer can be programmed to control the Unibus. This procedure is done through the device-interrupt routine.



Testing system configuration

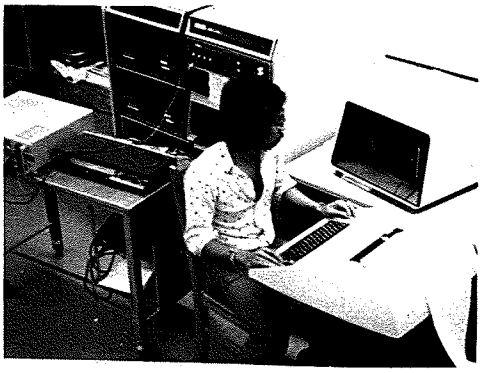
(a)



PDP 11/40 system simplified block diagram

(b)

Fig. 2.1



Photograph of test equip. ment.The relay under test is beside the oscilloscope.

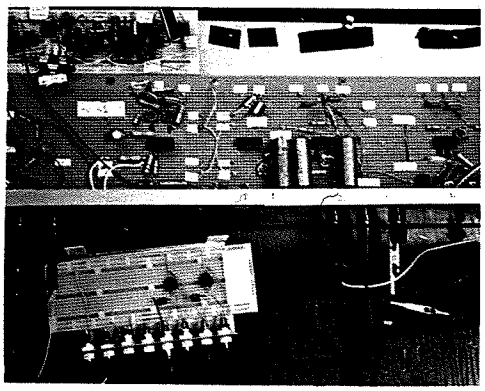
(a)

Graphic and teletype terminal.

(b)

Manual key input.

(c)



Experimental electronic relay under test.

(d)

Fig. 2.2

The clock-interrupt in particular, has been found to be very useful in this work. The former is used to realise the sampling time required to simulate the test waveforms.

The programs and instructions are normally input to the computer through the terminal called the LA 30 Decwriter. Another form of input/output peripheral is the CRT screen or what is also sometimes called the Graphics terminal. The latter is used in this work to plot the R-X diagram, and the operating-time characteristic.

One of the useful aspects of the minicomputer is that it has a Laboratory Peripheral system. The D/A channels of the LPS support are used to apply the simulated test waveforms to the device under test (D.U.T.). The Lab support also has a set of A/D channels, light emitting diodes display, a clock, and a set of relays. The A/D device is used to receive the trip response from the relay device under test.

2.2.2 System Software Support

The operating system on the Declab 11/40 is the RT 11 [7,8]. It performs all the standard users requests such as start and stop routines, and writes new programs onto a disc.

It has been mentioned that only 10K of memory locations are available in the core at a time. Such limited amount of memory may not be sufficient for large programs as in this work. Some kind of a storage economy may thus be desired. The large program which requires more than the available space is divided into several sections. Only the active sections of the program are allowed to reside in the core. The rest of the sections of the program are stored in the mass storage device, the so-called Disc Storage. Hence, a fairly large program such as the size of this test program can be conveniently run.

BASIC [6,7] is the only high level language that is available on the computer. BASIC has a syntax which is similar to the familiar FORTRAN Language. One of the differences between the two languages is that BASIC is an interactive language.

BASIC can be easily interfaced with an Assembly language routine. It can perform a routine of which BASIC is not capable and thus enhance the overall program capability. This may include the users' own written programs.

The operating system has an Assembler which enables the users to write their own routines in Assembly Language. The Assembler which is called the MACRO, produces object modules in Assembly language from the user input ASCII format. The Linkagee Editor (LINK) program takes a group of BASIC object modules and the users' own object modules, if available, and links them together to produce a main machine language program. Another program that is available in the operating system is the Text Editor (EDIT). It is used to write and input all assembly language programs into the computer and can also be used to write BASIC programs.

2.3 Device under Test (D.U.T.) - a Solid State Mho Relay

The experimental electronic mho relay which is used to test the technique developed was constructed by A.W. Degroot. The design of the relay was assisted and advised by Professor L.M. Wedepohl. The additional memory element was incorporated by Professor G.W. Swift and A.W. Degroot.

The block diagram of the static Mho relay is shown in Fig. 2.3 (a). The block average comparator was preferred over the block instan-

taneous comparator and the pulse comparison type in the design of the relay. The block average comparator [3,14] is well-known to have good immunity against transient offsets and surges. Also, the minimum operating time [14] of the comparator can be designed to be one-half of the power frequency period without incurring transient overreach and without requiring special filtering circuits in the input signals.

The mixing circuit used an operational amplifier as the analog signal processor. The circuit configuration is shown in Fig. 2.3 (b). The replica or the mimic impedance is realised by setting the impedances Z1, Z2, Z3, Z4 and Z5 to some specified values. The detailed derivation of the necessary conditions is given in the Appendix A. The outputs of the mixing circuit are the following Signals:

$$S_1 = IZ_L - V$$

$$S_2 = V + V_P$$

where

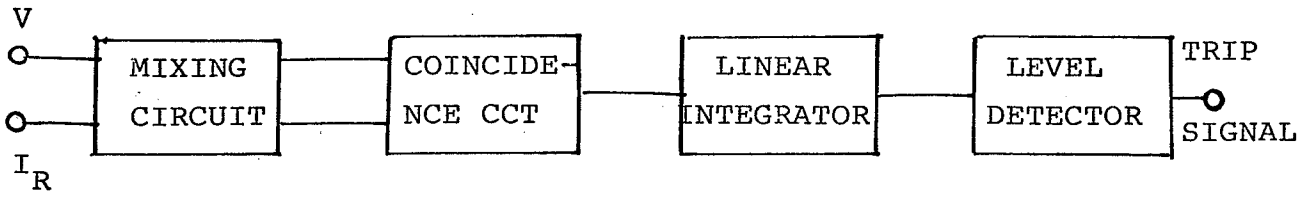
S_1 and S_2 are the outputs of mixing circuit unit;

I and V are fault current and voltage respectively; and

V_P is the polarizing voltage.

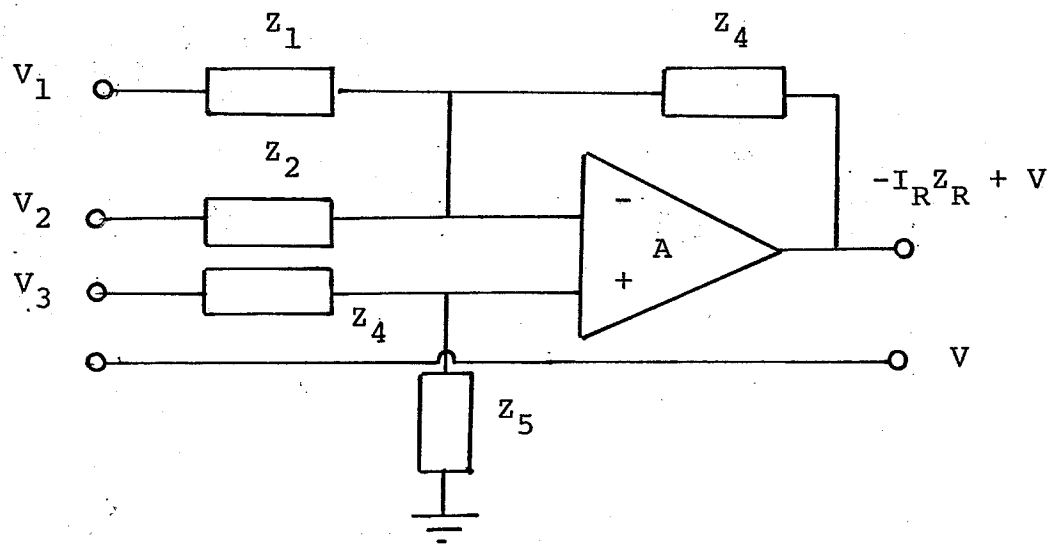
The coincidence circuit produces standard output pulses which are positive when the input signals (S_1 and S_2) are of the same polarity and are negative when they are of the opposite polarity. A typical output is shown in Fig. 2.4 (b).

The output of the coincidence circuit is fed to the integrating circuit. The integrating circuit produces an output which increases linearly when the input pulse is positive and falls at the same rate when the polarity reverses as shown in Fig. 2.4 (c).



Basic block diagram of an electronic Mho relay using a block average comparator

(a)

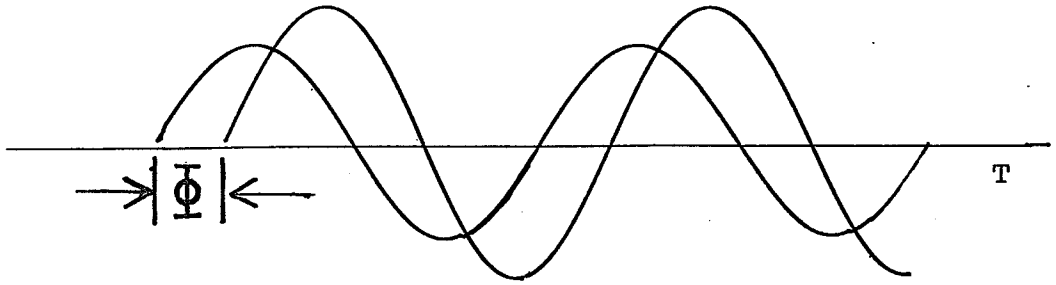


V_1 = part of the relay input current, V_2 = relay input current, V_3 = relay input voltage

Mixing circuit using an operational amplifier

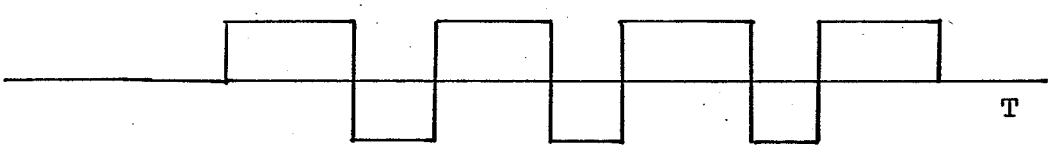
(b)

Fig. 2.3



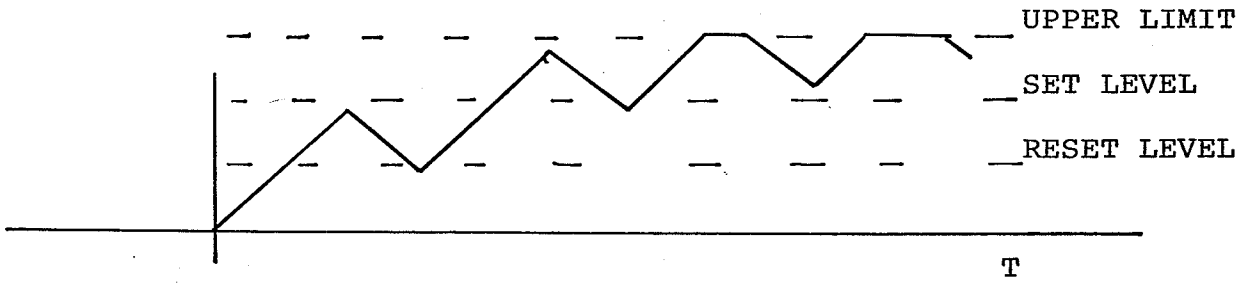
Output of mixing unit

(a)



Output of coincidence unit

(b)



Output of integrator unit

(c)

Fig. 2.4

The final element of the relay is a level detector which switches when the integrator output exceeds the set level and resets when the output of the integrator falls below the reset level. This is illustrated in Fig. 2.4 (c). Jackson, Patrikson and Wedepohl [14] suggested that the optimum set level of the detector is about two thirds of the maximum integrator excursion limit.

2.4 Simulation of Test Waveforms

In this static test, it is necessary to generate simulated voltage and current signals. The generated waveforms have a 'staircase' shape as shown in Fig. 2.5 (a). Obviously when the sampling period is infinitely small, the simulated waveforms approach the ideal simusoid. However, the minimum sampling time or the maximum number of samples that can be used is limited by the amount of memory locations that are available in the minicomputer. In their literature, Mann and Morrison [13] and Rockefellor [10] recommended a sampling time of 0.5 msec.* For the present work, it is decided that a sampling time of 0.833 msec of twenty samples per cycle is sufficient. At this sampling rate, the magnitudes of the 19^{th} and 21^{st} harmonics are each about five percent. The table in Fig. 2.5 (b) gives the summary of the harmonic contents for several typical sampling rates. It can be shown that [17] the harmonics occur at frequencies

$$(NM \pm 1)60 \text{ Hz} \quad \text{for} \quad N = 1,2 \ldots$$

with corresponding amplitudes

$$\frac{1}{NM \pm 1}$$

* Their work was, however, concerned with signal detection rather than signal generation.

where

M is the number of samples per cycle.

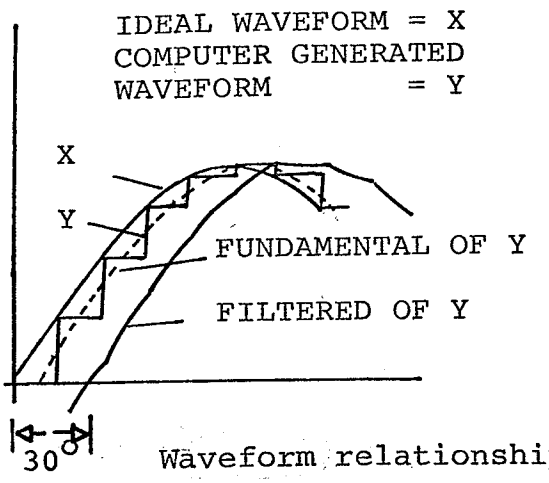
The test waveforms are filtered to reduce the harmonics using the conventional RC filter as shown in Fig. 2.5 (c). The filter has an added advantage in that it also provides a buffer between the computer and the relay, and prevents possible loading of the D/A. The details of the filter design are given in the Appendix D. The filter causes a phase shift of about -21^{o}. However, two identical RC filters are used for the voltage and current channels. Hence, there is no relative shift that could cause possible error, being introduced to the relay by the filters.

It should be made clear at the outset that the "current" waveform to the relay is really a voltage. In other words, the relay uses a voltage proportional to current, generated by the computer, as its "current" input. For some relays, it may be necessary to use voltage-controlled-current-sources (large operational amplifiers) to provide current to the relay under test.

2.5 Detail Procedure of Testing

2.5.1 Main BASIC Program

The flow diagram of the main BASIC program of the steady state test is shown in Fig. 2.7. The main program in BASIC starts with the initialization of the graphics for the display of the R-X characteristic of the Mho relay under test. The initialization routine is stored and saved separately as a display file. The display file is called once during each run and is subsequently removed from the core to save store locations.



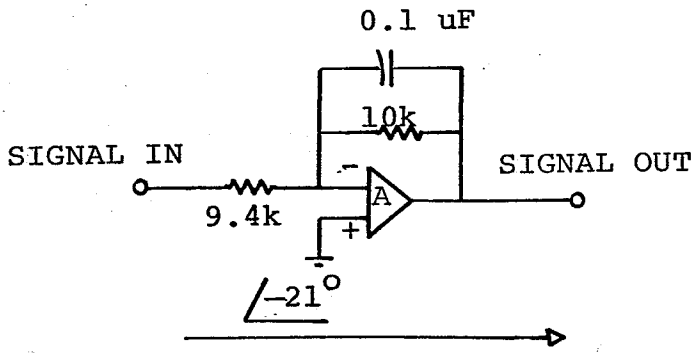
Waveform relationships

(a)

m	harmonic no:	amplitude
4	1	1.00
	3	0.33
	5	0.20
	7,9 etc	
20	1	1.00
	19	0.053
	21	0.048
	39,41 etc	
60	1	1.00
	59	0.017
	61	0.016
	119,121 etc	

Amplitude of Fourier coefficients for for different number of samples.

(b)



Buffer amplifier and filter

(c)

Fig. 2.5

The main program proceeds to request the input parameters such as the level of test current, the phase angle between current and voltage and the number of iterative 'revolutions'. The phase angle input specifies the phase angle of the impedance in the relay R-X plane.

Owing to the fact that the waveform of the voltage and current that are used in the test is periodic in nature, the program is only required to compute the initial cycle of the test waveforms. The expressions defining the twenty samples of the first cycle of the simulated waveforms are:

$$C(I) = C_0 \text{ Sin } (WT_I - \phi) \qquad 0 \leqslant T_I \leqslant \frac{2\pi}{W}$$

$$V(I) = V_0 \text{ Sin } (WT_I)$$

where

I is the integer number between 1 and 20;

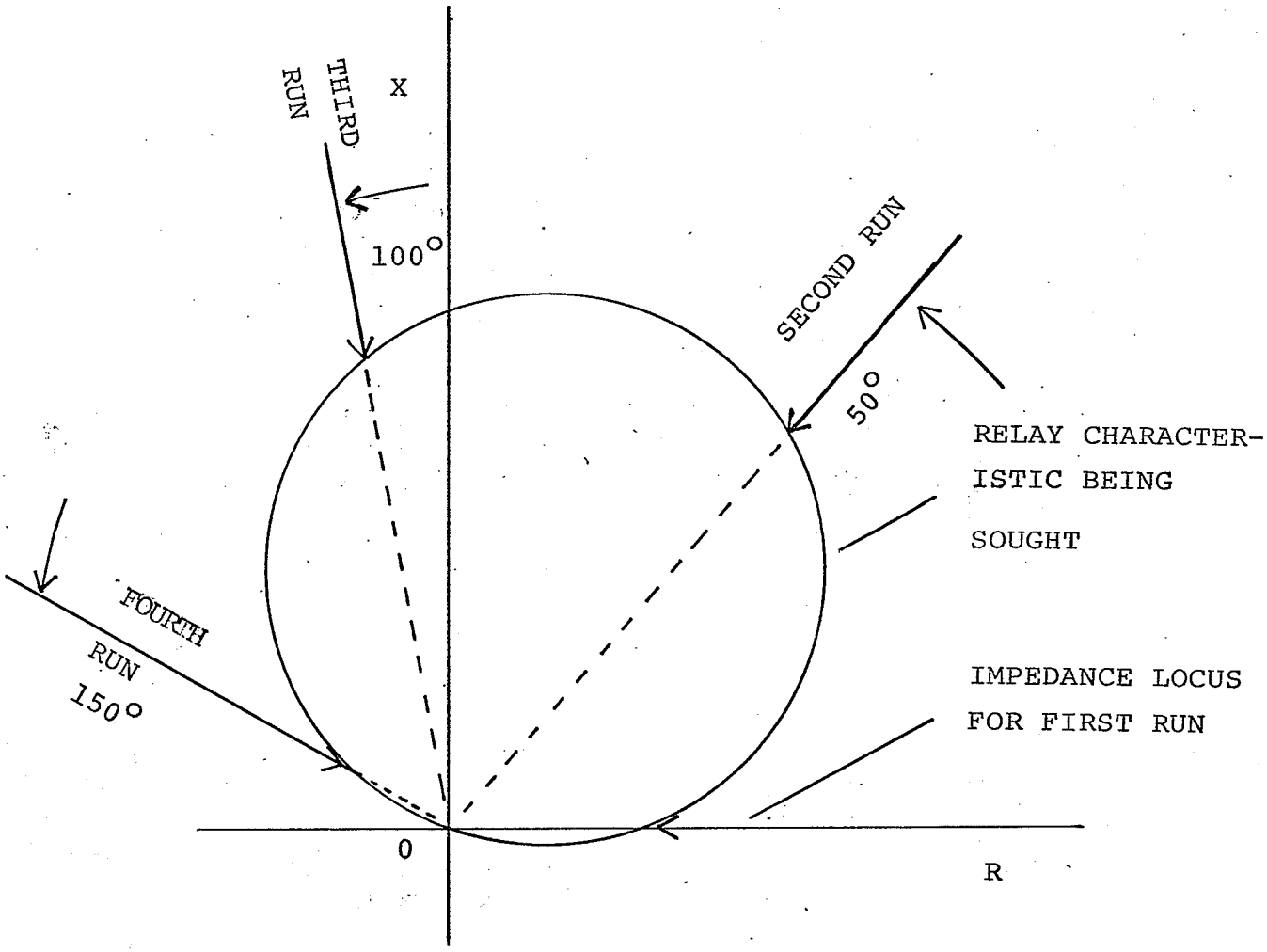
C(I), V(I) are the magnitude of current and voltage at the sampling instances respectively;

C_0, V_0 are the amplitude of the initial current and voltage respectively;

T_I is the sampling time; and

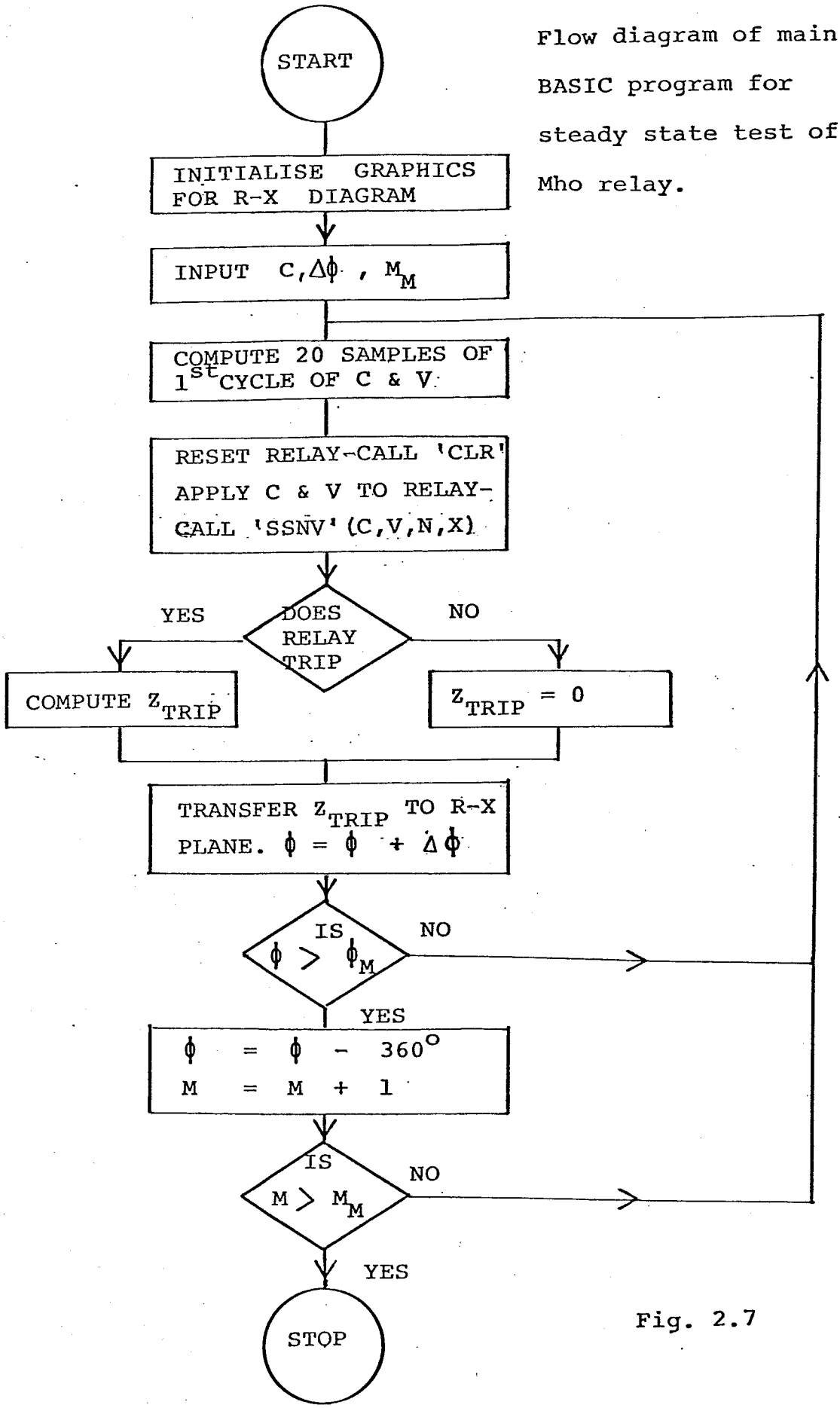
ϕ is the phase angle.

The decreasing amplitude of the voltage test waveform is simulated in the Assembly Language subprogram. The magnitude of the current is kept constant at a specified level. The magnitude of the test waveforms can only take values between zero and five volts. This constraint is placed by the D/A device of the Lab peripheral system of the computer.



Impedance locus during steady state test

Fig. 2.6



Flow diagram of main BASIC program for steady state test of Mho relay.

Fig. 2.7

The D/A device holds the last value of the signal it received until a new numerical value is sent to its buffer. Hence, it is necessary to ensure that the outputs of the D/A channels are at zero voltage level before the test waveforms can be applied to the relay. This procedure of resetting the relay is incorporated in the subprogram "CLR" and is accessed from the main program.

The main program then requests for the second Assembly subprogram via a command CALL "SSNV" (C, V, N, X), where

C and V are the array containing magnitude of voltage and current samples;

N is the number of cycles of test waveform applied to relay; and

X is the state of tripping condition (1 or 0).

The Assembly subroutine "SSNV" applies the generated test voltage and current waveforms to the relay. The subroutine also checks for tripping of the relay and stores the number of cycles of test waveform applied to the relay before returning to the main calling BASIC program. The flow diagram of the Assembly program is shown in Fig. 2.8 and further detailed treatment of the subprogram is given in the next section.

The main program now has all the necessary information to prepare for the graphic display. The impedance at which the relay trips, is computed from the tripping condition and the number of cycles of test waveform applied to the relay. This impedance corresponds to a point on the boundary or locus of the characteristic of the Mho relay.

Simulation of the decreasing voltage but keeping the current constant in the test program corresponds to the movement of a point

at an angle towards the origin in the R-X impedance plane of the relay. The graphic display support is used to simulate this impedance movement during each iterative run. A special subroutine in the Assmebly Language written by N.J. Morphy [14] is employed to simulate the movement of the impedance points in real time.

The impedance angle is then incremented by 50^{o} and the "second run" starts. The diagram in Fig. 2.6 illustrates the first four runs of the test.

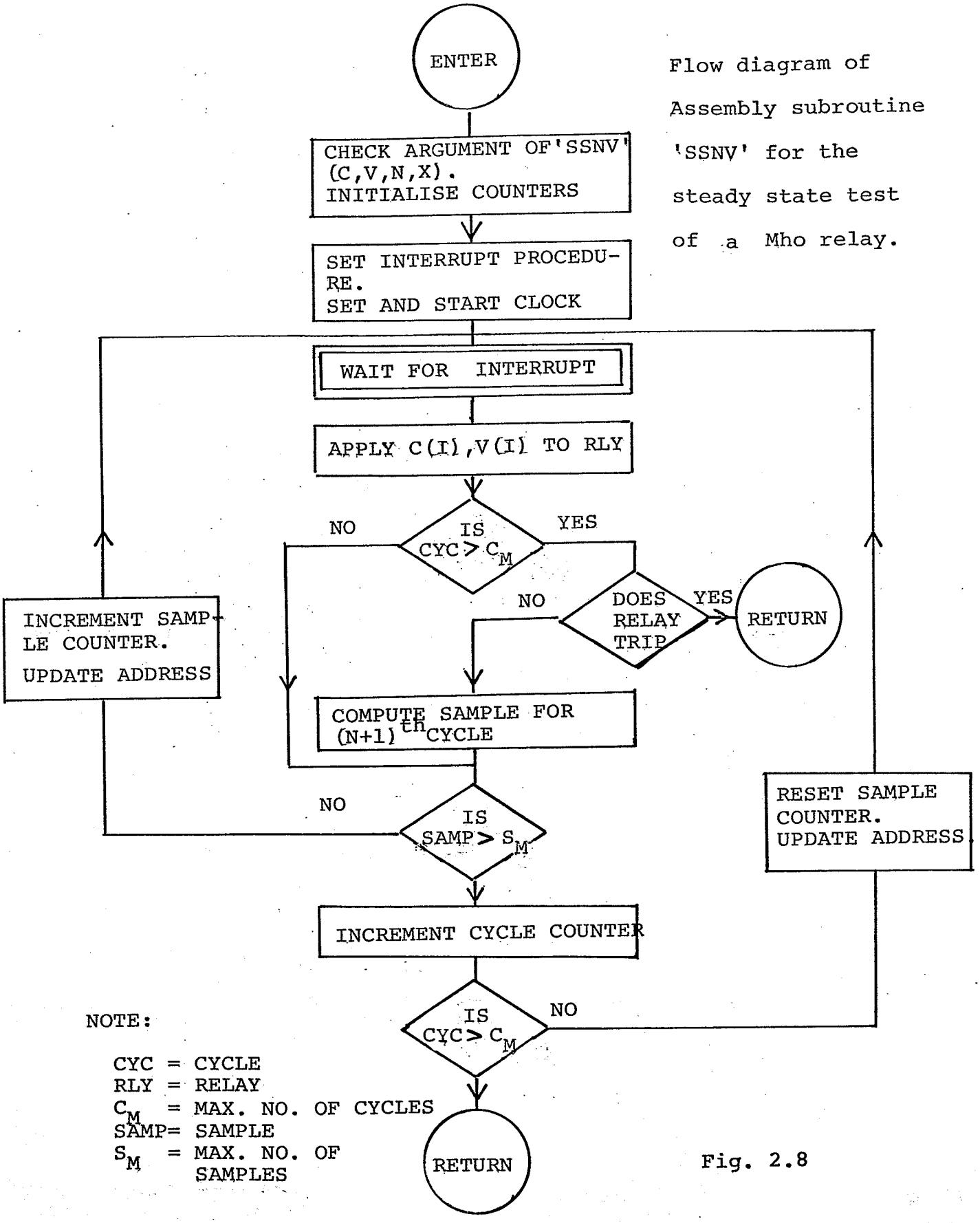
After seven runs, each of which takes only a few seconds, the general shape of the circular characteristic is apparent. The eighth run is at 400^{o} or 40^{o}, the ninth at 90^{o}, and so on. After five "revolutions" the full characteristic is plotted, with points at 10^{o} interval.

Of course, the increment in the impedance phase angle and the number of revolutions are under program user's control and need not be 50^{o} if desired. The listing of the main BASIC program is given in the Appendix B.

2.5.2 Assembly Subprograms

There are three specially written Assembly subroutines which are used in conjunction with the main BASIC program for the steady state test.

One of the Assembly Language subroutines [6,7,8] is requested from the main BASIC Program via the command, CALL "CLR". This Assembly subroutine which is labelled as 'CLEARX' resets the relay. Its input voltage and current are restored to zero level. This is achieved by transferring into each of the buffers of the D/A devices



Flow diagram of Assembly subroutine 'SSNV' for the steady state test of a Mho relay.

NOTE:

CYC = CYCLE
RLY = RELAY
C_M = MAX. NO. OF CYCLES
SAMP= SAMPLE
S_M = MAX. NO. OF SAMPLES

Fig. 2.8

a numerical value of 2048. Depending on the magnitude of the last value of the outputs of the D/A devices, the process of resetting the zero voltage level may cause relay false tripping. Hence, it is necessary for the Assembly subprogram, labelled as CLEARX to wait until the relay reverts back to the no-trip conditions. Subsequently, the program pointer transfers back to the main BASIC calling program. The program listing of the Assembly subroutine is given in the Appendix B.

The command, CALL "SSNV" (C, V, N, X) in the main program requests the Assembly Subprogram which is labelled as 'JAMAL'. Its flow-diagram is shown in Fig. 2.8. The Assembly subroutine is accessed from the main calling BASIC program through the special System Function Table [6, 7].

The first part of the Assembly subprogram 'JAMAL' checks for the syntax of the argument of the call statement, CALL "SSNV" (C, V, N, X). Then, the sample and cycle counter, interrupt procedure and clock registers are set according to the requirements of the test.

When clock is initiated, the Assembly subprogram enters into an idle mode waiting for the clock to interrupt. The first voltage and current samples are fed to the relay through the D/A's upon receipt of the clock interrupt. Before reverting back to the idle mode, the sample counter is incremented and the locations of the data are updated. The run is repeated for several cycles without checking for relay tripping. This routine ensures that the relay is properly brought to a steady state condition.

The test sequence then continues with the voltage being decreased exponentially until the relay trips. After each clock interrupt,

the magnitude of the voltage for the next cycle is also computed and stored in the same location. In addition, the relay is checked for tripping. The magnitude of the voltage for the next cycle is computed using the following expression:

$$V_I(N + 1) = V_I(N) * (1 - \gamma)$$

where

I is an integer number between 1 and 20 representing the sample number;

$V_I(N + 1)$ is the magnitude of the voltage at the sampling time t_I in the $(N + 1)^{th}$ cycle;

$V_I(N)$ is the magnitude of the voltage at the sampling time t_I in the $(N)^{th}$ cycle; and

$(1 - \gamma)$ is the constant multiplier which has the value of 0.981 in this test program.

The detailed derivation of the multiplication factor is given in the Appendix E.

The storage requirement for this steady state test is small because the test waveforms are taken as pure sinusoids. The same memory locations are used to store the samples of the next cycle. Hence, only twenty memory locations are required for each test waveform.

The present minicomputer PDP 11/40 does not have a hardware multiplier. All multiplications are done through the operating system software. The software multiplier is too slow for the present requirements of the test program. The multiplication in the Assembly program which is labelled as 'JAMAL' is realised using a combination of adding and shifting the register containing the data.

The Assembly subprogram returns to the main BASIC calling program when

a) the relay trips, or

b) all the specified number of cycles (C_{max}) of the simulated test waveforms are applied to the relay. The relay is then assumed to have not tripped.

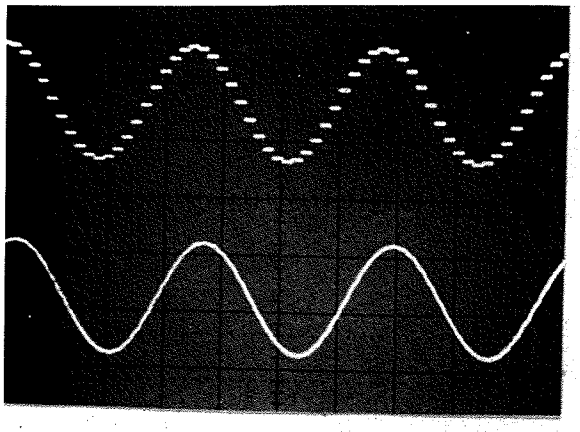
The listing of the Assembly program is given in the Appendix B.

The third and last Assembly subprogram which is used in conjunction with the main BASIC program is labelled as 'TMEX and TMRX'. It was written by N.J. Morphy of the computer centre. The subprogram is used to simulate the movement of the impedance point on the R-X plane of the graphic display in real time. The listing of the subprogram is given in Appendix B.

2.6 Results and Comments

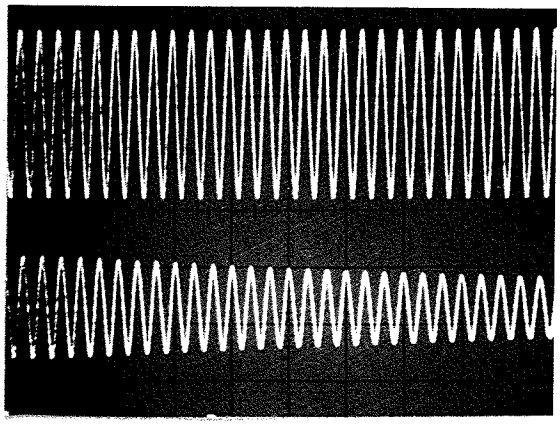
The test waveforms are simulated and generated using a sampling rate of 20 samples per cycle. The diagram in Fig. 2.9 (a) illustrates a typical test waveform. It comprises a series of steps, each occurring for a duration of the sampling period which is 0.833 msec. The test waveform is similar to the output of a 'zero order sampling and holding' device [16] with a sinewave as the input. The other waveform is the resulting filtered waveform using the RC filter. It is typical of the test waveforms that are applied to the relay.

In the performance test, the input current level is kept constant, while the voltage is decreased exponentially. The diagram in Fig. 2.9 (b) exemplifies the typical test voltage and current waveforms. When the relay is found to have tripped, no more test



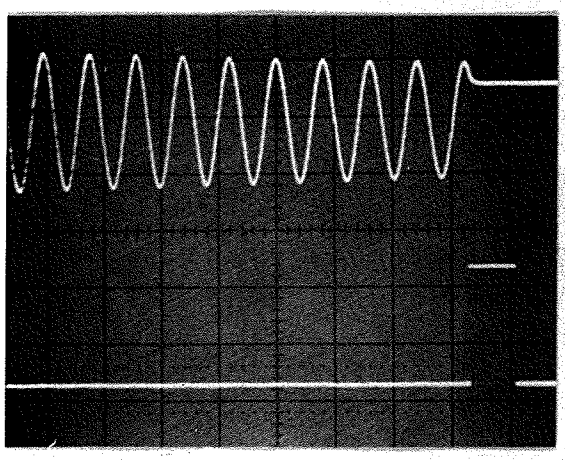
Typical computer generated test signals before and after filtering.

(a)



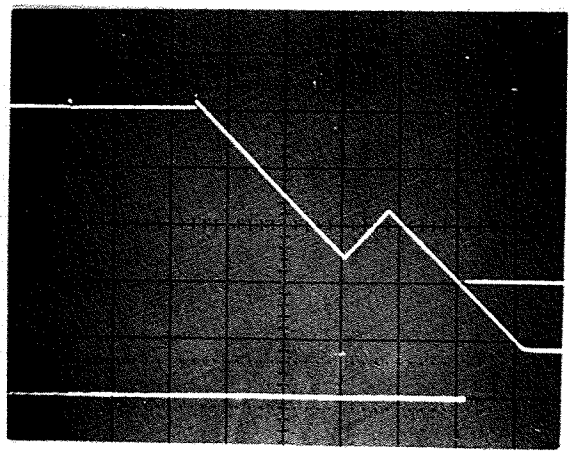
Typical test current and voltage signals.

(b)



Typical test voltage and trip signals.

(c)



Typical output of integrator and trip signals.

(d)

Fig. 2.9

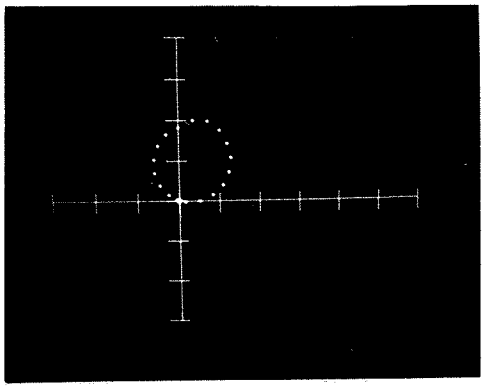
waveforms are applied and the program pointer reverts back to the main BASIC program. The diagram in Fig. 2.9 (c) illustrates a tripping condition of the relay. The trip signal is initiated when the output voltage level of the integrator falls to less than the preset value. Such condition is shown in Fig. 2.9 (d).

When the test is run, the program initially requests the test current level and the iterative specifications. When the computation starts, the points on the circular characteristic of the Mho relay in the R-X plane are plotted automatically on the graphic display of the computer. The pictures in Fig. 2.10 (a) and (b) are typical of the results. It is noticed that there is some reduction in the size of the circular characteristic with the smaller current level. This may be attributed to the sensitivity of the relay to small current level.

The test program illustrated one of its virtues when it detected the imperfections of the experimental static relay in the first test run ever attempted automatically. The defect manifests itself in the form of a 'dimple' in the circular characteristic of the relay as shown in Fig. 2.10 (c). The 'dimple' effect can occur for instance if the zero crossings of the relay comparator are not adjusted properly.

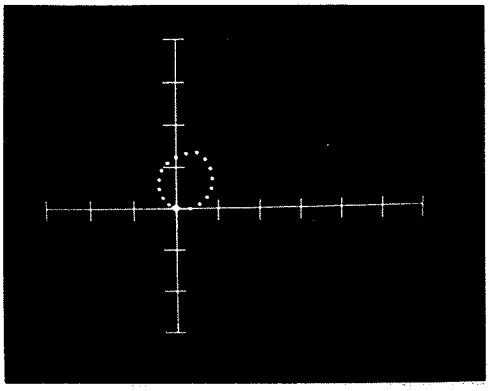
The picture in Fig. 2.10 (d) shows the same circular characteristic of the relay but with the filters removed. There appears to be a slight reduction in size of the characteristic and hence filters may be desirable for the test.

Hence, the proposed automated testing technique can be utilized to establish the static performance of a solid-state Mho relay.



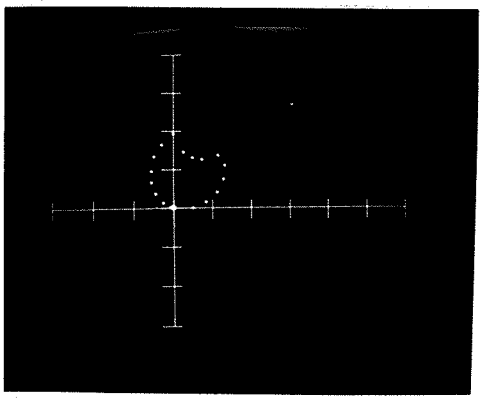
Mho relay steady state characteristic with I=3 A

(a)



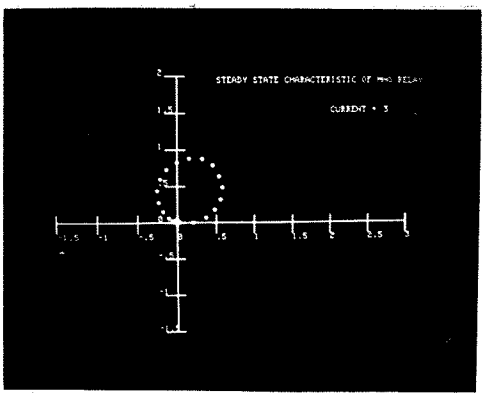
Characteristic with I=2 A

(b)



'Dimple' effect in the characteristic of relay with poorly adjusted zero crossings of comparator.

(c)



Characteristic with V I unfiltered.

(d)

Fig. 2.10

CHAPTER 3

DYNAMIC PERFORMANCE TEST

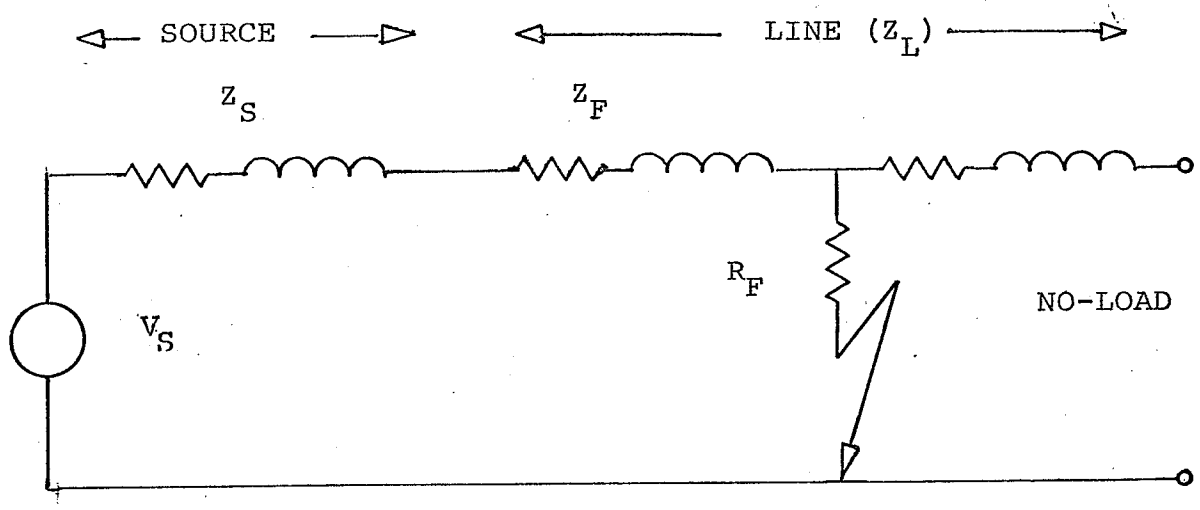
3.1 Brief Description

3.1.1 Determination of the Characteristic Locus

The determination of the characteristic locus of the Mho relay enables its accuracy under transient fault conditions to be assessed [3,14]. A simplified model of a single phase transmission line initially on no-load as shown in Fig. 3.1 (a) is used to simulate the fault waveform conditions. In this test, only the impedance characteristic of the first quadrant is determined. The locus is found by simulating a fault at a fixed distance but with varying fault resistance. When the point on the boundary of the characteristic is established, the point of inception of fault on the line is moved to another position. The diagram in Fig. 3.1 (b) illustrates a typical routine. The procedure is repeated until the section of the locus of the dynamic characteristic of the Mho relay under test in the first quadrant of the impedance is plotted.

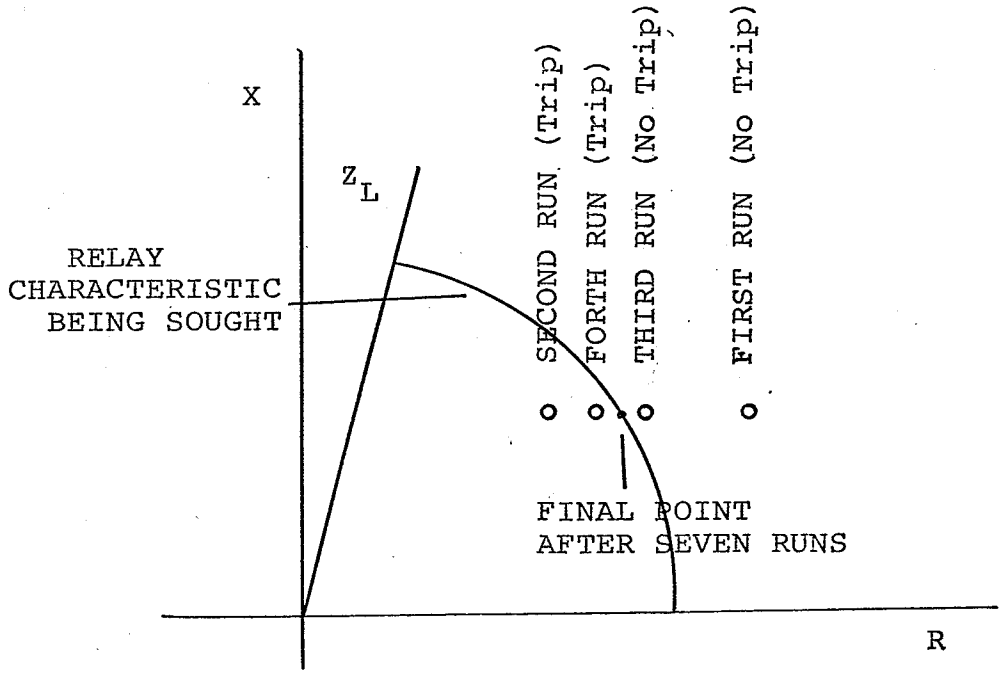
3.1.2 Determination of the Operating Time Characteristic

It is imperative that the operating time performance [3,14] of a Mho relay under fault conditions be appropriately checked. The



The simplified model of the transmission line and source

(a)



Typical set of runs establishing one point of the dynamic characteristic locus

(b)

Fig. 3.1

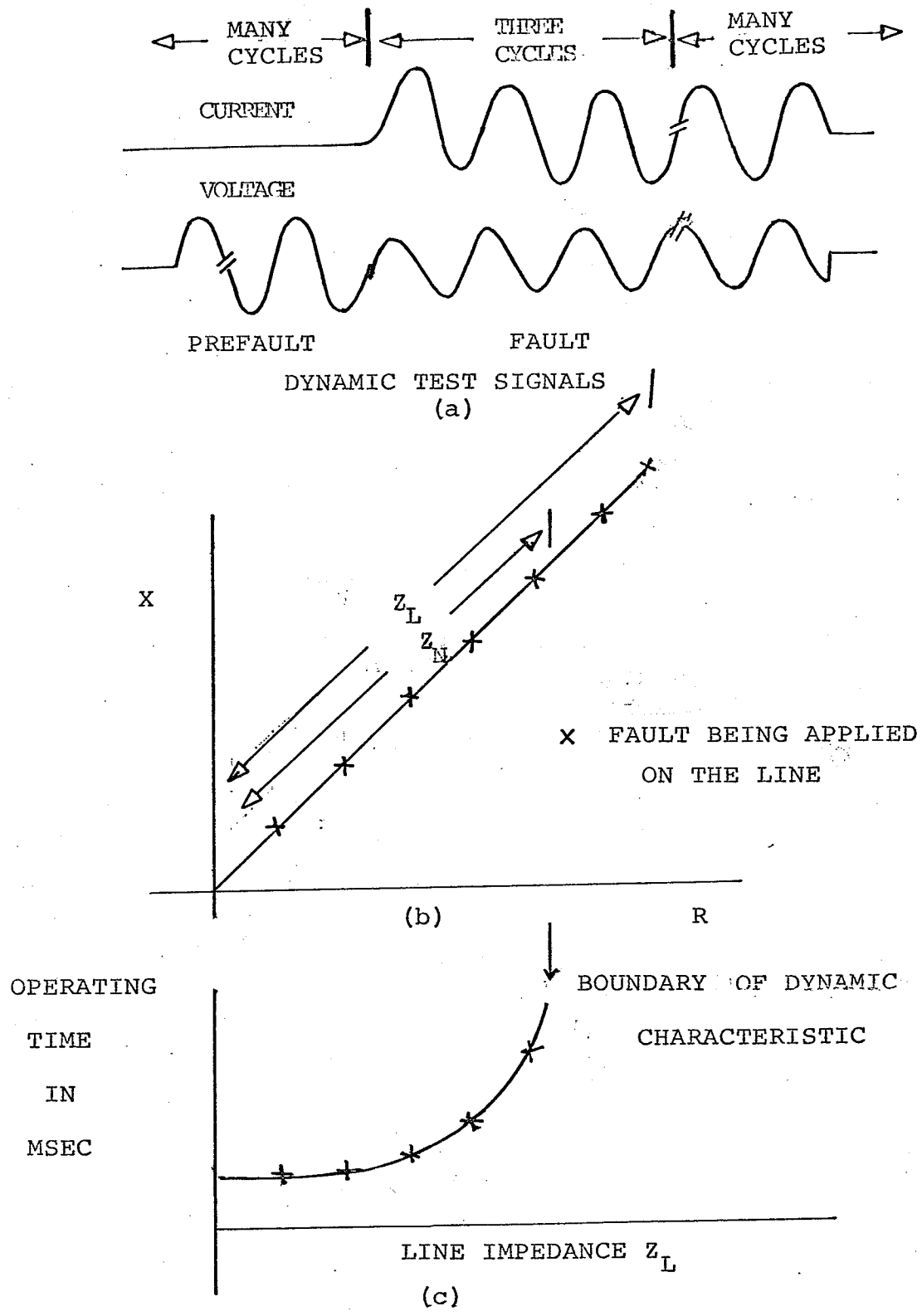


Illustration of relay operating time test. (b) and (c)

Fig. 3.2

operating time is found by simulating fault inceptions along the line from outside the protected zone (the no-trip zone) right up to the relay location. A similar simplified model of the transmission line as shown in Fig. 3.1 (a) is used. However, the fault resistance is assumed to be negligible. The diagram in Fig. 3.2 attempts to illustrate the test procedure.

3.2 Simulation of Fault Waveforms

In a digital simulation as in this work, it is, at first glance, apparent that a numerical technique is the best form of analysis. The dynamics of the system under consideration are represented by the differential equations and can be subsequently solved by the numerous numerical methods and routines that are available such as Euler's and Runge-Kutta methods [15]. However, the accumulated errors inherent in these techniques are quite substantial unless high order sophisticated numerical techniques are employed. Before this approach was pursued further, it was realised that because of the simplicity of the system model as shown in Fig. 3.1 (a), a direct analytical solution of the fault current and voltage waveforms is possible. Hence, it was decided to use the direct analytical approach.

In the simplified transmission line system model, the following assumptions are made:

a) Capacitance to ground is neglected, thus the relay sensitivity to higher harmonics is not determined.

b) that a fault arc is assumed linear. It is well-known that a fault arc is nonlinear [2], but the added computational complexity did not seem justified.

c) A no-load condition exists prior to the fault.

With reference to the diagram in Fig. 3.1 (a) and using the basic theory of differential equations, the following voltage and current equations are established:

$$V_S = V_M \text{Sin } (Wt + \theta)$$

$$I_{SS} = I_M \text{Sin } (Wt + \theta - \alpha)$$

$$I_T = I_C \text{Exp } (-t/T)$$

where

V_S is the source voltage;

I_{SS} is the steady state component of the current after the inception of fault;

I_T is the transient component of the fault current;

I_C is the magnitude of the exponential part of the fault current at time zero;

V_M is the amplitude of the source voltage;

I_M is the amplitude of the steady state fault current;

θ is the phase angle of source voltage;

α is the system phase angle;

t is the time variable;

T is the time constant of the system; and

W is the system power frequency (120π radians)

The fault current is easily deduced and has the following form -

$$I_F = I_T + I_{SS}$$

and hence,

$$I_F = I_C \text{Exp}\ (-t/T) + I_M \text{Sin}\ (Wt + \theta - \alpha) \qquad (3.1)$$

At the inception of fault when time is zero, the fault current (I_F) is negligible. Thus, the initial value of the fault current (I_C) is as follows:

$$I_C = -I_M\ \text{Sin}\ (\theta - \alpha) \qquad (3.2)$$

Hence, the following expression of the fault current is obtained.

$$I_F = I_M \left\{ \text{Sin}\ (Wt + \theta - \alpha) - \text{Sin}\ (\theta - \alpha)\ \text{Exp}\ (-t/T) \right\}$$

$$= I_M \left\{ \text{Sin}\ (Wt)\ \text{Cos}\ (\theta - \alpha) + \text{Sin}\ (\theta - \alpha) \left[\text{Cos}\ (Wt) - \text{Exp}\ (-t/T) \right] \right\} \qquad (3.3)$$

The amplitude of the fault current has the following form:

$$I_M = \frac{V_M}{|Z_T|}$$

where

Z_T is the magnitude of the total system impedance.

The total system impedance is given by

$$Z_T = Z_S + Z_F + R_F$$

where

$Z_S = (R_1 + jX_1)$ is the source impedance;

$Z_F = (R_2 + jX_2)$ is the fault impedance; and

$R_F = (R_3)$ is the fault resistance.

It follows that from the expression in equation (3.4), that the magnitude of the system impedance has the following form:

$$\left|Z_T\right| = \left[(R_1 + R_2 + R_3)^2 + (X_1 + X_2)^2\right]^{\frac{1}{2}} \qquad (3.5)$$

Substituting $\beta = \theta - \alpha$, equation (3.3) becomes

$$I_F = I_M\left\{\text{Sin (Wt) Cos } (\beta) + \text{Sin } (\beta) \left[\text{Cos (Wt) - Exp } (-t/T)\right]\right\} \qquad (3.6)$$

With reference to equation (3.6), the two conditions for maximum and minimum d.c. offset are as follows:

a) A maximum d.c. offset is obtained in the fault current when Sin (β) = -1 or $\beta = 270^{\circ}$.

b) A minimum d.c. offset is obtained in the fault current when Sin (β) = 0 or $\beta = 0^{\circ}$.

In the dynamic test, it was decided to keep the d.c. offset component of the fault current at a constant level. This implies that the phase angle of the source voltage must be adjusted continously depending on the value of the fault resistance. In the special case to determine the operating time of the relay the fault resistance is kept zero and hence, the phase angle of the source voltage need only to be set once during the initial part of the test. The phase angle of the source voltage is given by the following expression:

$$\theta = \beta + \alpha \qquad (3.7)$$

The value of the system phase angle (α) has the following form:

$$= \text{Arctan } \left[(X_1 + X_2)/(R_1 + R_2 + R_3)\right] \qquad (3.8)$$

Using the usual basic circuit theory, the expression for the fault voltage is easily determined.

$$V_F = I_F(R_2 + R_3) + L_2\frac{d}{dt}(I_F) \tag{3.9}$$

where

V_F is the fault voltage waveform; and

L_2 is the inductance of the fault impedance.

Substituting for the fault current (I_F) in equation (3.9) gives

$$V_F = I_F(R_2 + R_3) + L_2\, I_M\left\{ W \text{ Cos } (\beta) \text{ Cos } (Wt) + \text{Sin } (\beta) \left[1/T \text{ Exp } (-t/T) - W \text{ Sin } (Wt) \right] \right\} \tag{3.10}$$

The current and voltage expressions as given in the equations (3.6) and (3.10) respectively, are used to simulate the fault conditions for the dynamic test. Typical test current and voltage waveforms are shown in Fig. 3.2 (a) and 3.6 (a).

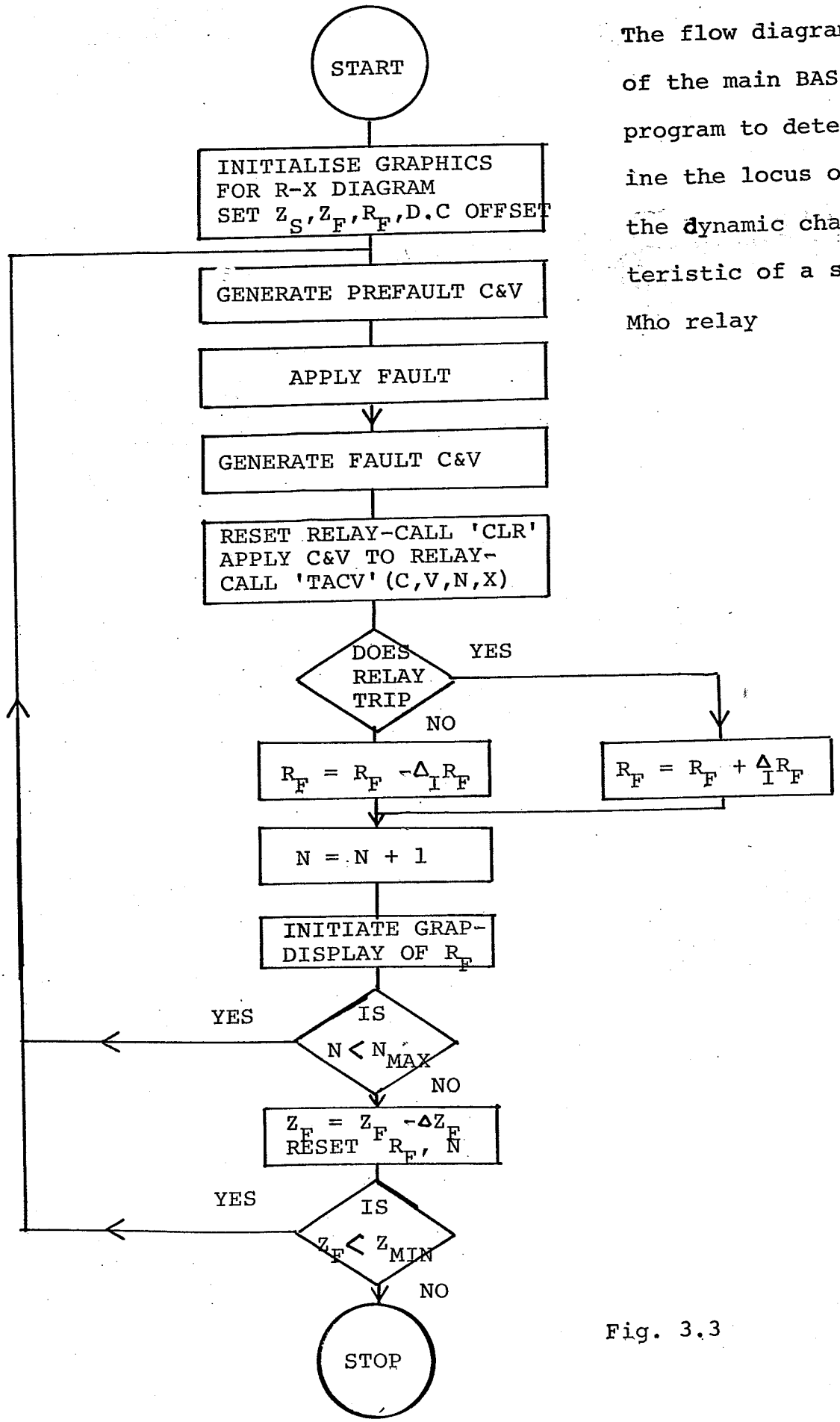
3.3 Detailed Dynamic Testing Procedure

3.3.1 Determination of the Locus of the Dynamic Characteristic

The software support that is required to determine the locus of the dynamic characteristic of the Mho relay entails the use of BASIC and as well as the Assembly routines. The general structure of the BASIC and Assembly programs are similar to that which is used for the steady state test.

The flow diagram of the main BASIC program is shown in Fig. 3.3. The main BASIC program initially requests for:

a) a starting line (fault) impedance somewhat greater than the anticipated replica impedance Z_N;



The flow diagram of the main BASIC program to determine the locus of the dynamic characteristic of a static Mho relay

Fig. 3.3

b) maximum or minimum d.c. offset;

c) Z_S to Z_L impedance ratio; and

d) initial fault resistance for the first iterative run.

The main BASIC program then initializes the graphic display for the plot of the R-X plane of the relay.

Next, the test current and voltage are generated. A certain number of cycles of prefault current and voltage waveforms is necessary to bring the relay to proper steady state condition. In the actual test it was felt that three to five cycles of the prefault test waveforms are sufficient. Since the system is assumed to be initially on no-load prior to the fault, the prefault current is zero. The prefault voltage waveform is generated using the following expression derived earlier:

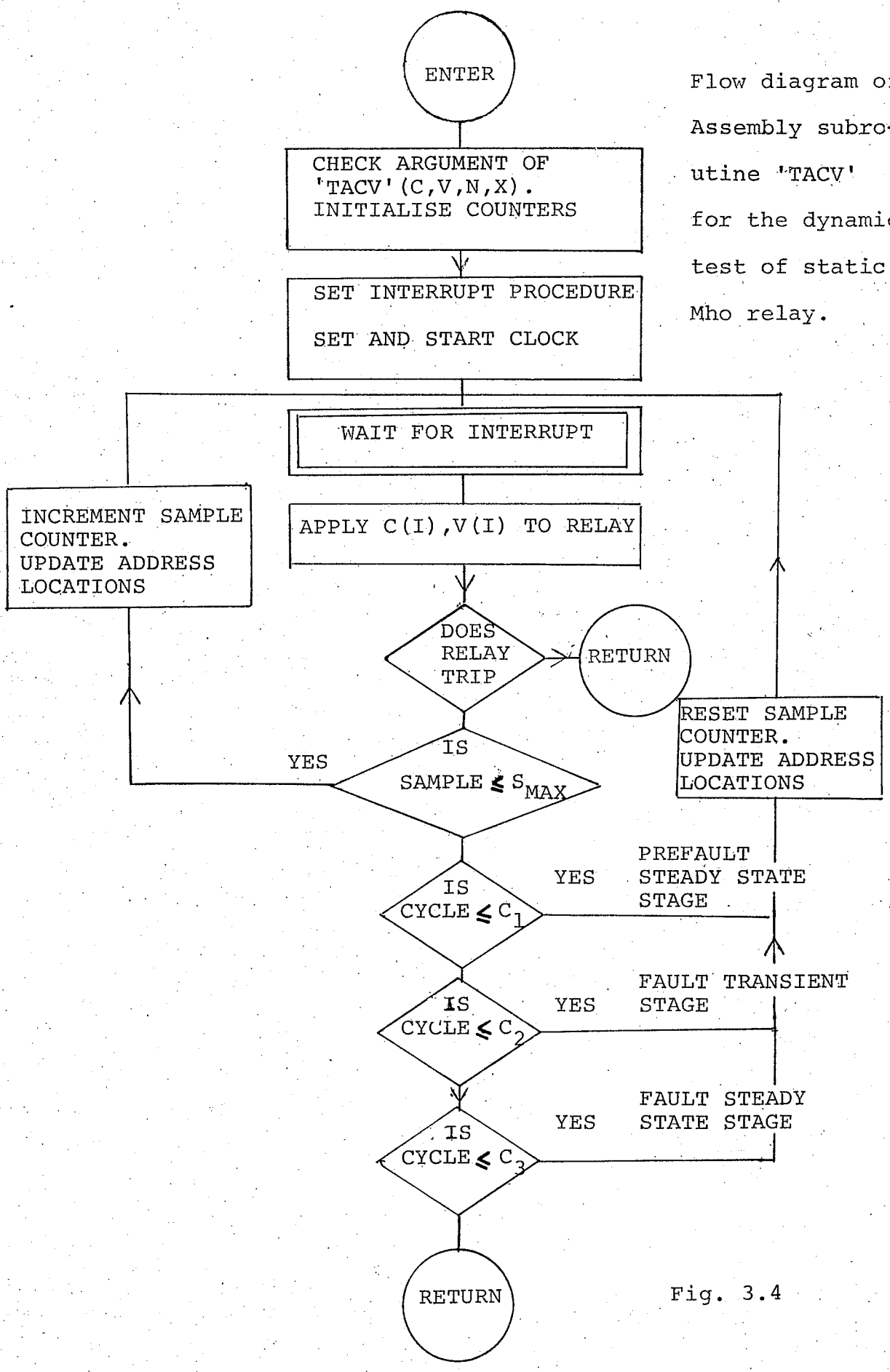
$$V(I) = V_M \text{Sin } (Wt_I + \theta)$$

where

V(I) is the magnitude of prefault voltage at sampling instances; and

I is the integer number between 1 and 20.

The phase angle of the source impedance has been shown to be dependant on the system phase angle which in turn is related to the fault resistance. Hence, during each iterative run the system phase (α) needs to be computed so that the phase angle of the source voltage can be determined. The source voltage and prefault voltage have the same expression for the case of no-load prior to the fault.



Flow diagram of Assembly subroutine 'TACV' for the dynamic test of static Mho relay.

Fig. 3.4

The fault current and voltage are generated using the following expressions which were derived earlier.

$$C(I) = I_M\left\{\text{Sin } (Wt_I) \text{ Cos } (\beta) + \text{Sin}\,\beta \text{ Cos } \left[(Wt_I) \text{ Exp } (-t_I/T)\right]\right\}$$

$$V(I) = C(I)\ (R_2 + R_3) + L_2\ I_M\left\{W \text{ Cos } (\beta) \text{ Cos } (Wt_I) + \text{Sin } (\beta)\ \left[1/T \text{ Exp } (-t_I/T) - W \text{ Sin } (Wt_I)\right]\right\}$$

The relay is reset when the main BASIC program calls for the Assembler subprogram 'CLR'. The routine ensures that the relay input conditions are at zero level and the relay condition is at no-trip.

Once the relay is reset, the simulated and generated waveforms of the fault conditions are applied to the relay. As in the steady state test, an Assembly subprogram transfers the stored data of the samples of the simulated test waveforms to the D/A's which are connected to the input channels of the relay. The test waveforms are filtered too.

The Assembler subprogram which is accessed via a command, CALL "TACV" (C, V, N, X) is similar to that which was used for the steady state test. The flow diagram is shown in Fig. 3.4. Its listing is given in Appendix C. The Assembler subprogram begins with the checking of the syntax of the argument of the call statement, CALL "TACV" (C, V, N, X). Then the interrupt procedure, the sample and cycle counter and the clock registers are set according to the requirements of the test.

When the clock is initiated, the Assembly subprogram enters into an idle mode waiting for the clock to interrupt. The first

samples of the voltage and current are applied to the relay upon receipt of the clock interrupt. Next, the relay is checked for tripping. If the relay trips the program control returns to the main BASIC program. Otherwise, the sample counter is incremented and the address of the next locations of the sampled waveforms are updated. Subsequently, the program reverts back to the idle mode. Similarly, the rest of the test waveforms are fed to the relay. The program pointer returns to the main calling program either when the relay trips or the whole of the simulated waveforms have been applied to the relay.

When the main BASIC program regains control, it places a temporary point on the R-X plot of the graphic display corresponding to the particular value of the fault resistance. The value of the fault resistance for the next iterative run is calculated using its previous value and the trip condition of the relay. The run is repeated with the newly established value of the fault resistance until a sufficiently accurate point on the boundary of the locus of the dynamic characteristic is found.

In the actual test program, the incremental fault resistance is reduced by half for the next run. Seven runs are used altogether and this ensures that the horizontal resolution in the impedance plane is one part in 128 or less than 1% of the initial fault resistance [17]. The diagram in Fig. 3.1 (b) attempts to illustrate a typical set of runs.

The value of the line impedance is then reduced (by say 10%) and the whole process is repeated to establish another point on the characteristic. The test is complete when the portion of the charac-

teristic in the first quadrant of the relay's R-X plane is established on the graphic display.

3.3.2 Determination of the Relay Operating Time Characteristic

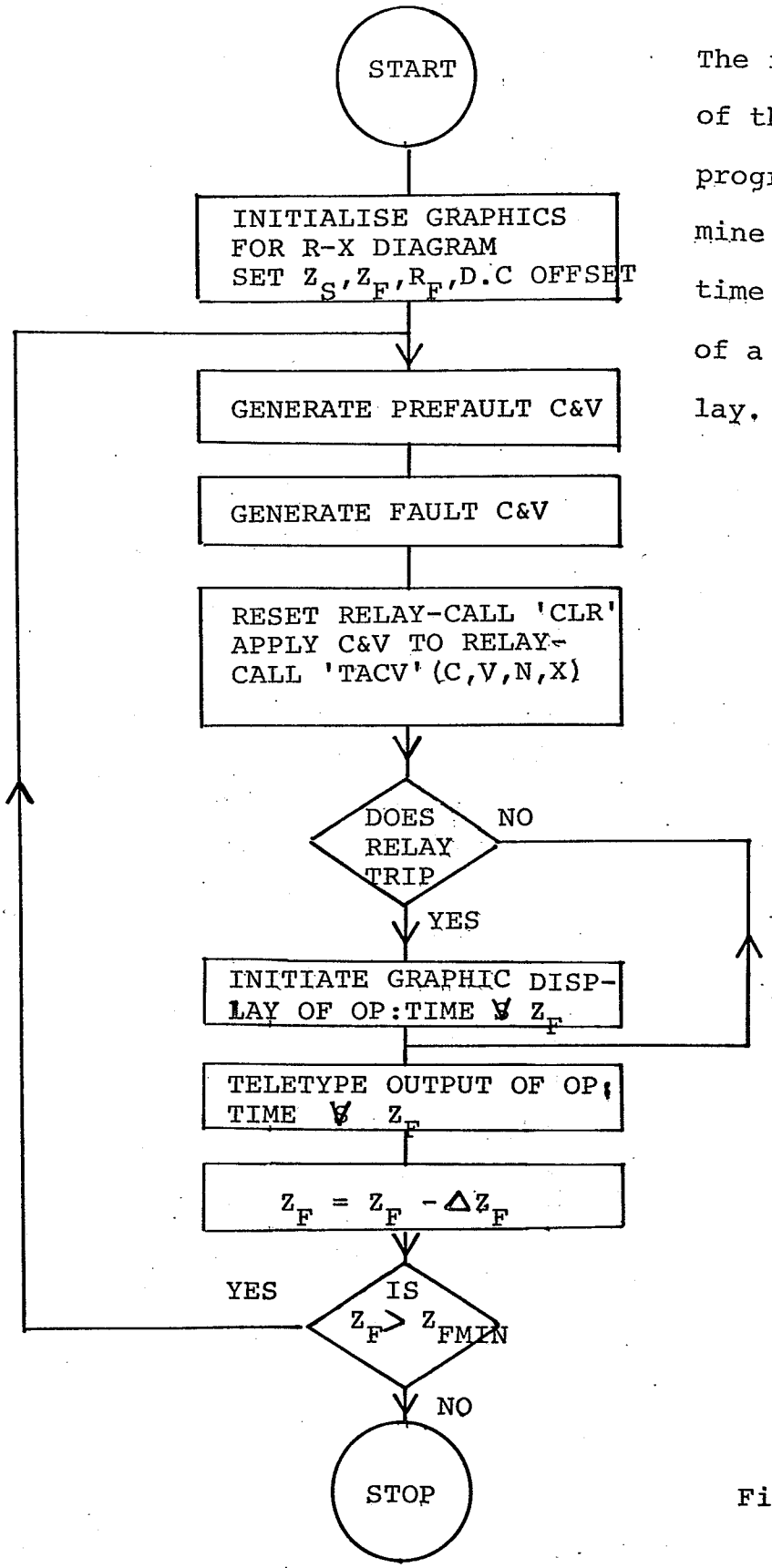
The flow diagram of the BASIC main test program is shown in Fig. 3.5. Its structure is similar to that which is used to determine the characteristic locus of the relay.

A fault is applied on the line of the simplified system as shown in Fig. 3.1 (a). An additional assumption is made here. The fault resistance is assumed to be negligible. The fault current and voltage waveforms are computed using the expressions in equations (3.6) and (3.10) respectively, with the fault resistance assumed to be zero.

The test waveforms are applied to the relay via the Assembly subroutine "TACV". The flow diagram of the Assembly subroutine has the same structure as that which is used for the 'locus' dynamic test. The outputs of the D/A's are filtered using the RC filter before they are fed to the relay.

The program counter returns to the main BASIC test program either when the relay is tripped or when the whole generated test waveforms is applied to the relay. When the relay trips, the information regarding the number of samples and cycles at the instant of tripping are transferred to the main program. If all the test waveforms are applied, the relay is assumed not to have tripped.

The operating time of the relay is computed from the sample and cycle counters data. The operating time is plotted against the line impedance (fault) on the graphic display. If the relay has



The flow diagram of the main BASIC program to determine the operating time characteristic of a static Mho relay.

Fig. 3.5

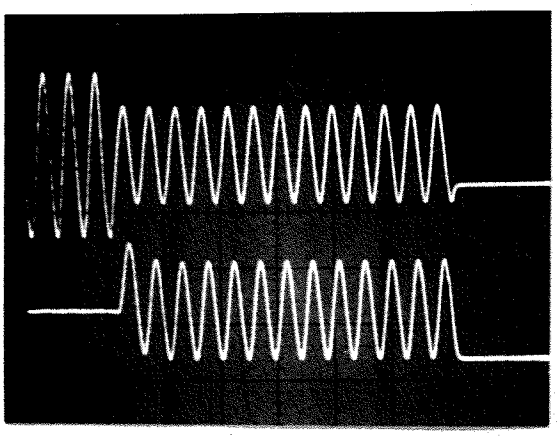
not tripped, the corresponding operating time is assumed to be infinite and no graphic display is initiated. A teletype output of the operating time, corresponding fault impedance, source impedance, cycle and sample counter is also produced.

The procedure is repeated for different fault impedances until the operating characteristic of the Mho relay is displayed on the graphics terminal of the computer.

3.4 Results and Comments

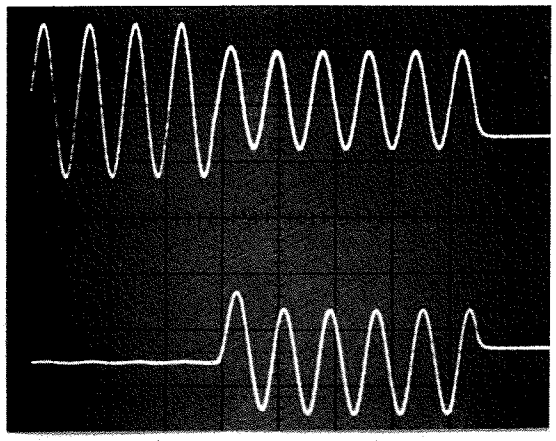
The first dynamic test which determines the locus of the dynamic characteristic of the relay has a facility which enables the d.c. offset condition of the test waveforms to be specified in the initial part of the test program. Typical test waveforms are shown in Fig. 3.6 (a) and (b). In the prefault stage, the current is zero since the system is assumed to be initially on no-load. Three cycles of voltage waveforms are simulated before the fault is applied. The maximum fault duration is sixteen cycles. The diagrams in Fig. 3.6 (b) and (c) illustrate typical tripping conditions of the relay. The trip signal is shown in Fig. 3.6 (c).

The accuracy of the relay under transient fault conditions can be assessed from the locus of the dynamic characteristic. A typical plot of the locus in the first quadrant of the R-X impedance plane is shown in Fig. 3.7 (a). The characteristic of the relay under test is sensitive to filtering as shown in Fig. 3.7 (b), where the RC filters are removed. The plots in Fig. 3.7 (c) and (d) illustrate the cases of polarization and zero d.c. offset.



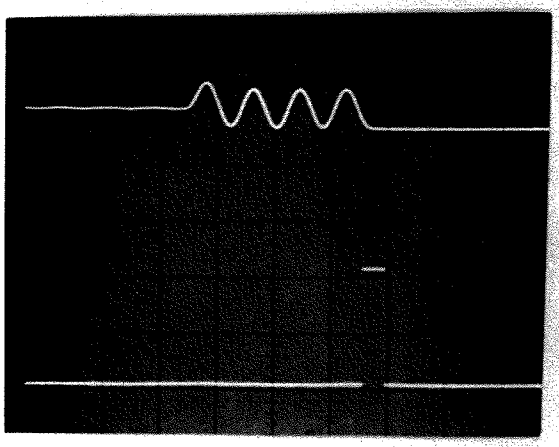
Typical test voltage and current signals (max d.c offset).

(a)



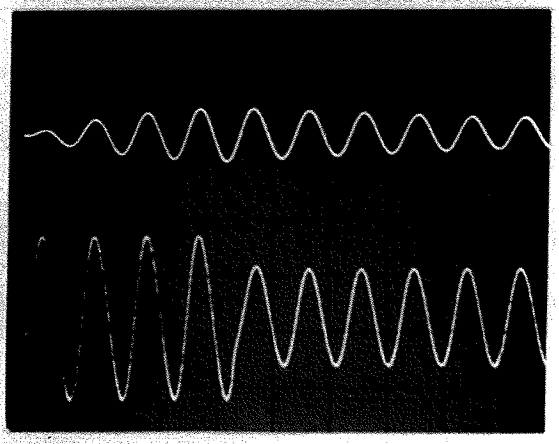
Typical test signals when the relay trips.

(b)



Typical current and trip signals.

(c)



Typical output of memory circuit and test voltage signal.

(d)

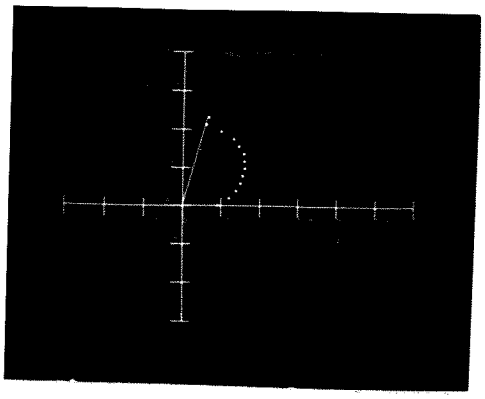
Fig. 3.6

The operating time performance test enables the speed of operation of the relay under transient fault conditions to be checked. The pictures in Fig. 3.8 (c) and (d) are typical of the operating time characteristic when the relay is unpolarized. The plots clearly show the point of uncertainty at the relay position. For a terminal fault, the relay would possibly not trip, especially for large source impedance.

The diagrams in Fig. 3.8 (a) and (b) attempt to illustrate the effect of polarization on the operating time characteristic. The operating time of the relay at its position is now definite and well-defined even for fairly large source impedance.

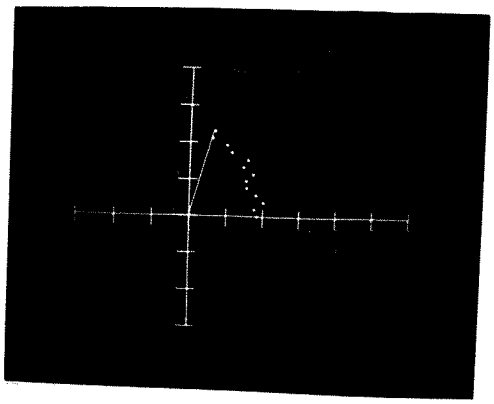
The plot of Z_S/Z_N versus Z_F/Z_N of the relay has been utilized to check its inherent weakness and defects [14]. Typical of such plots of the experimental relay under test are shown in Fig. 3.9 and 3.10.

Hence, the proposed automated technique permits the assessment of the dynamic performance of the relay too.



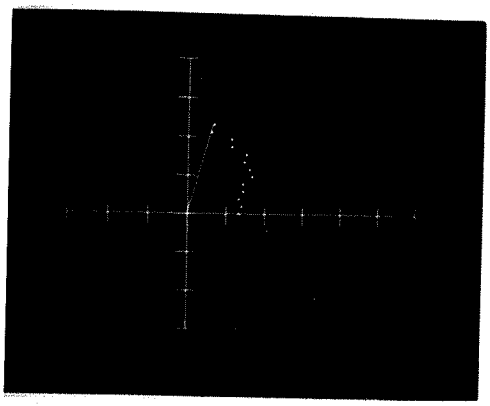
Dynamic characteristic.
Unpolarised,filtered,
and with max d.c offset.

(a)



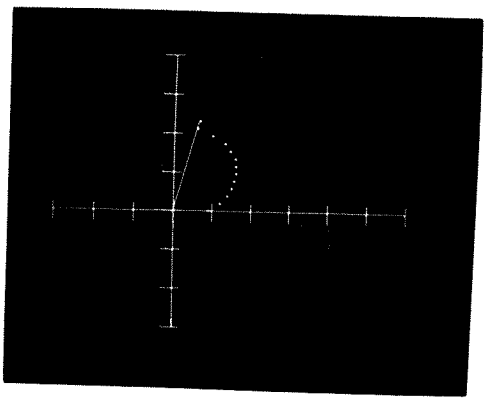
Dynamic characteristic.
Unpolarised,V and I
unfiltered and max d.c
offset.

(b)



Dynamic characteristic.
Polarised,V and I filtered
and max d.c offset.

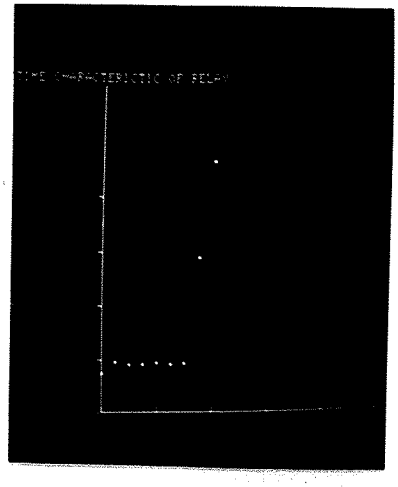
(c)



Dynamic characteristic.
Unpolarised, V and I
filtered but zero d.c offset.

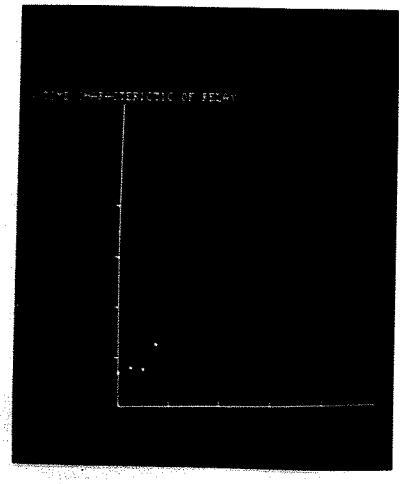
(d)

Fig.3.7



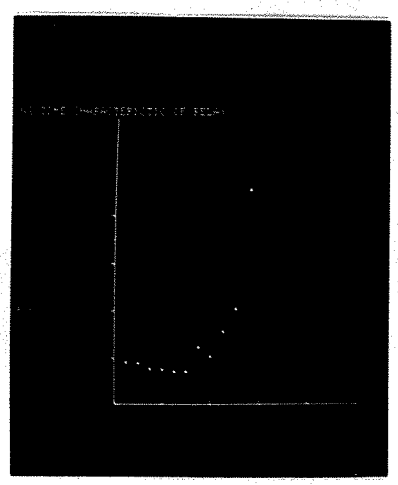
Operating time ¢ Z_L. Polarised and Z_S is 0.7 p.u

(a)



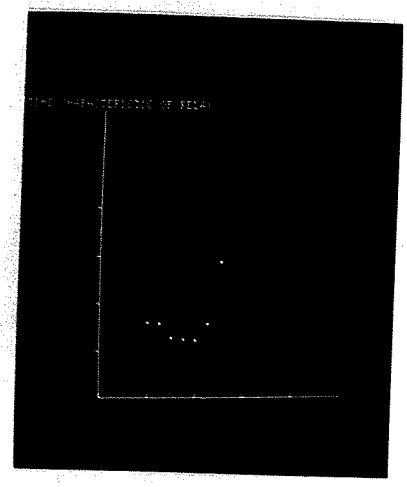
Operating time ¢ Z_L. Polarised but Z_S is large 10 p.u

(b)



Unpolarised and small Z_S 0.7 p.u

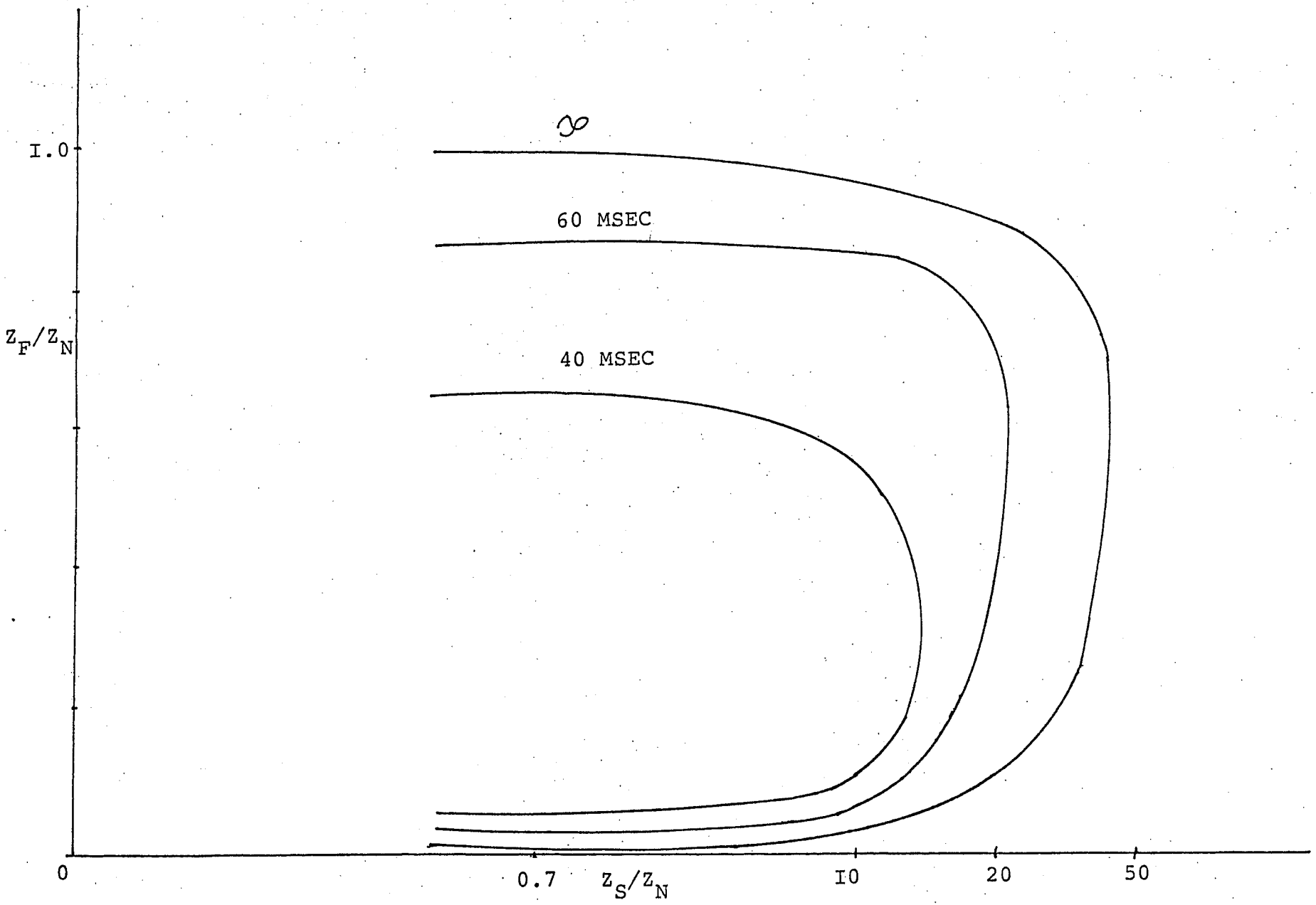
(c)



Unpolarised but large Z_S 10 p.u

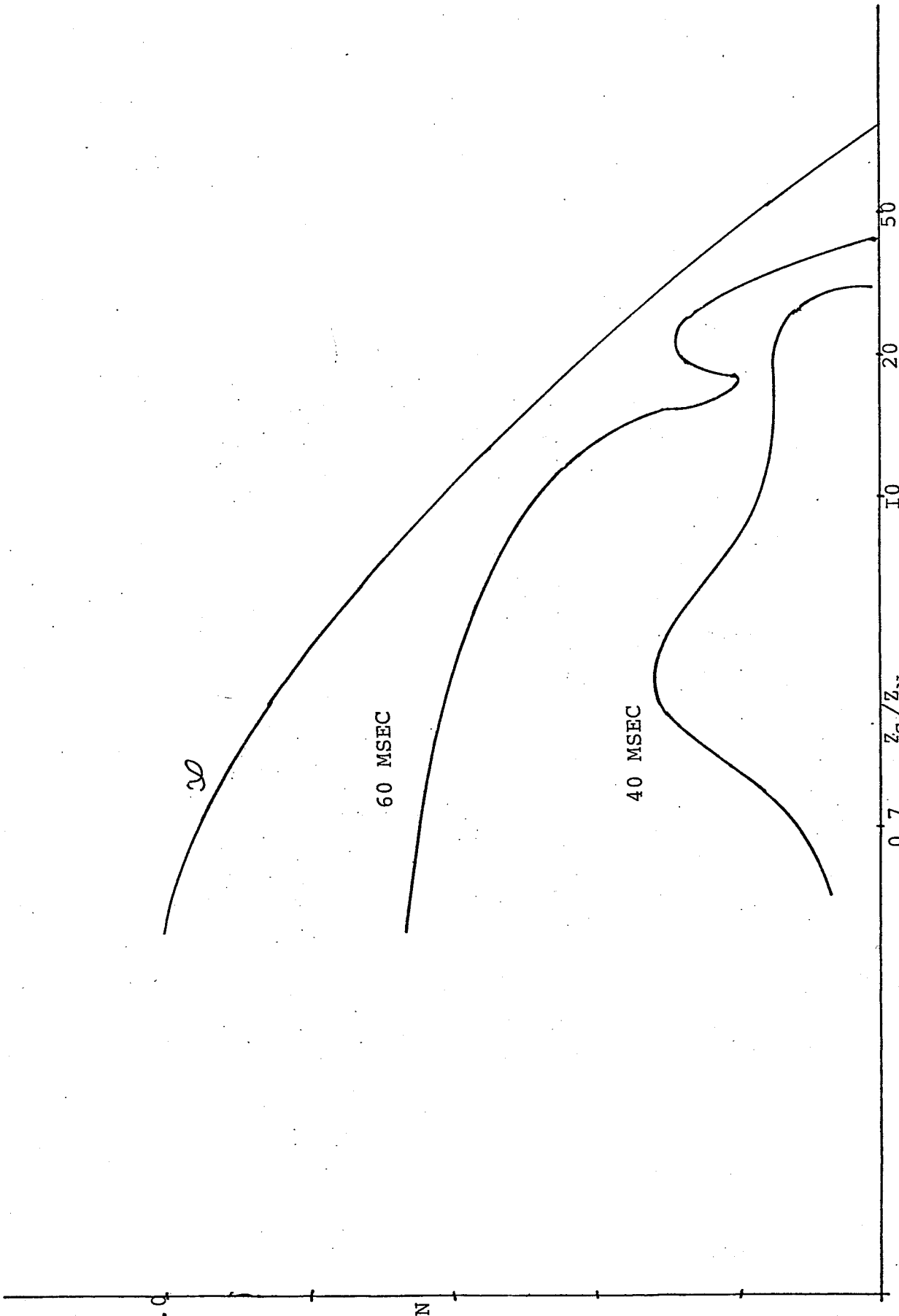
(d)

Fig. 3.8



Plot of normalised distance to fault as a function of normalised source impedance for an unpolarized Mho relay.

Fig. 3.9



Plot of normalised distance to fault as a function of normalised source impedance for a polarized Mho relay.

Fig. 3.I0

CHAPTER 4

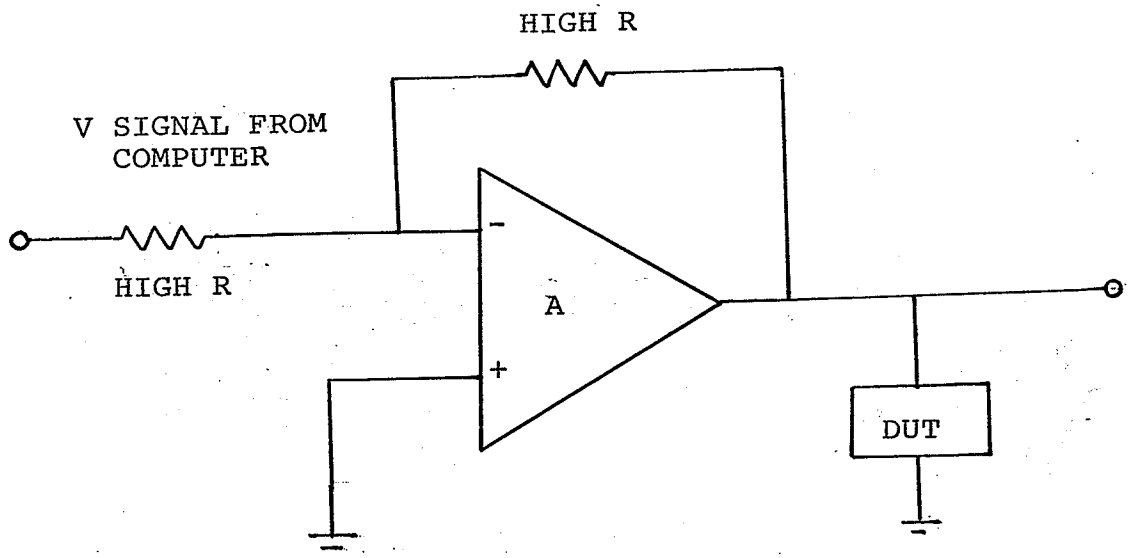
CONCLUSION AND SUGGESTIONS FOR FUTURE WORK

In this work, an automated technique to test a protective relay has been presented. The software support for the static test is developed in Chapter Two. The test routine for the dynamic test is formulated in Chapter Three. The test results are automatically displayed on the graphic terminal of the minicomputer, permitting immediate on-line evaluation of the performance of the relay under test.

In addition to the short turnover test time with the consequential cost saving, there is also increased flexibility over the conventional method.

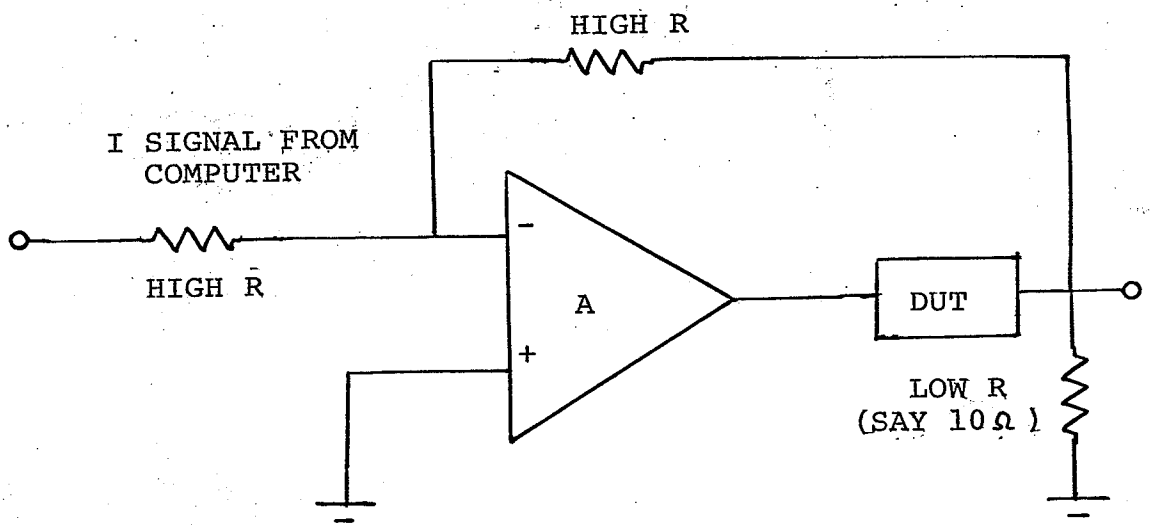
The main limitation of the proposed method is that it assumes the availability of a minicomputer. However, the present modern minicomputer is so versatile and powerful that its acquisition may be justified ultimately.

Even though it is ideal for solid state protective relays, the technique can as well be used to test the classical electromechanical relay. In such a test, a power amplication interface between the minicomputer and the relay is required. In cases where the relay requires actual input current, the circuit configuration



Voltage controlled voltage source

(a)



Voltage controlled current source

(b)

Fig. 4.1

in Fig. 4.1 (b) may be used. The diagram in Fig. 4.1 (a) illustrates a possible amplification circuit for the voltage channel.

The biggest limitation of the present test equipment are space (core memory) and speed (computer multiplication time). A link to the large IBM 370 computer and an addition of a hardware multiplier will permit more sophisticated testing such as:

a) the effect of transmission line capacitance to ground;

b) three phase simulation so as to find the effect of faults in other phases and 'sound phase polarizing';

c) the representation of nonlinear fault arc resistance; and

d) the effect of system power swing.

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APPENDIX A

DESCRIPTION OF THE CIRCUIT CONFIGURATION OF THE MHO RELAY

This appendix describes the detailed circuit configuration of the Mho relay which is used to run the test programs. The block diagram of the relay is shown in Fig. A.1. The diagram in Fig. A.2 attempts to illustrate the signal processing unit in the initial part of the relay. The block average comparator is preferred and the circuit diagrams of the relevent parts of the comparator are shown in Fig. A.3 and Fig. A.4. The integrator and the trigger circuits are shown in Fig. A.5. The memory circuit is shown in Fig. A.6.

With reference to the diagram in Fig. A.7, and using the conventional mesh current analysis, the following voltage expression is established.

$$\frac{V_1-V^-}{Z_1} + \frac{V_2-V^-}{Z_2} = \frac{V^--V_o}{Z_3} \qquad \text{(A.1)}$$

where,

$Z_{IN} = \infty$

$I_4 = I_5$

$$V^+ = V_3 \frac{Z_5}{Z_4 + Z_5}$$

$$I_1 = \frac{V_1 - V^-}{Z_1}$$

$$I_2 = \frac{V_2 - V^-}{Z_2}$$

$$I_3 = \frac{V^- - V_o}{Z_3}$$

$$V_o = A (V^+ - V^-)$$

$$I_3 = I_2 + I_1$$

Upon simplification, equation (A.1) becomes

$$V_1/Z_1 + V_2/Z_2 - V_3/Z_T = -V_o \left[1/Z_3 + \frac{1/Z_1 + 1/Z_2 + 1/Z_3}{A} \right]$$

where,

$$1/Z_T = \frac{Z_5}{Z_4 + Z_5} \left[1/Z_1 + 1/Z_2 + 1/Z_3 \right]$$

Hence,

$$V_o = \frac{-V_1 \, Z_3/Z_1 - V_2 \, Z_3/Z_2 + V_3 \, Z_3/Z_T}{1 + \frac{1 + Z_3/Z + Z_3/Z2}{A}} \qquad (A.2)$$

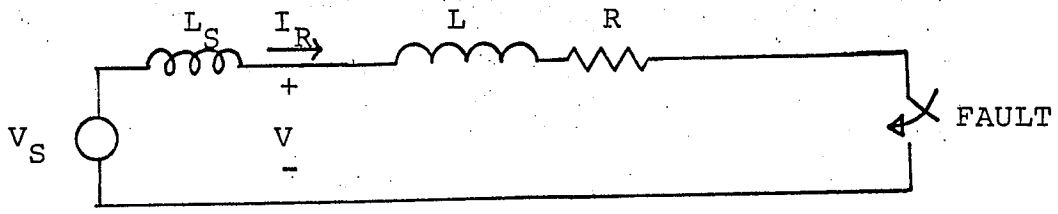
The expression in equation (A.2) is used to realise the inductance of the replica impedance (Z_R) of the relay.

The differentiating circuit is shown in Fig.A.7.2 Its transfer function has the following form.

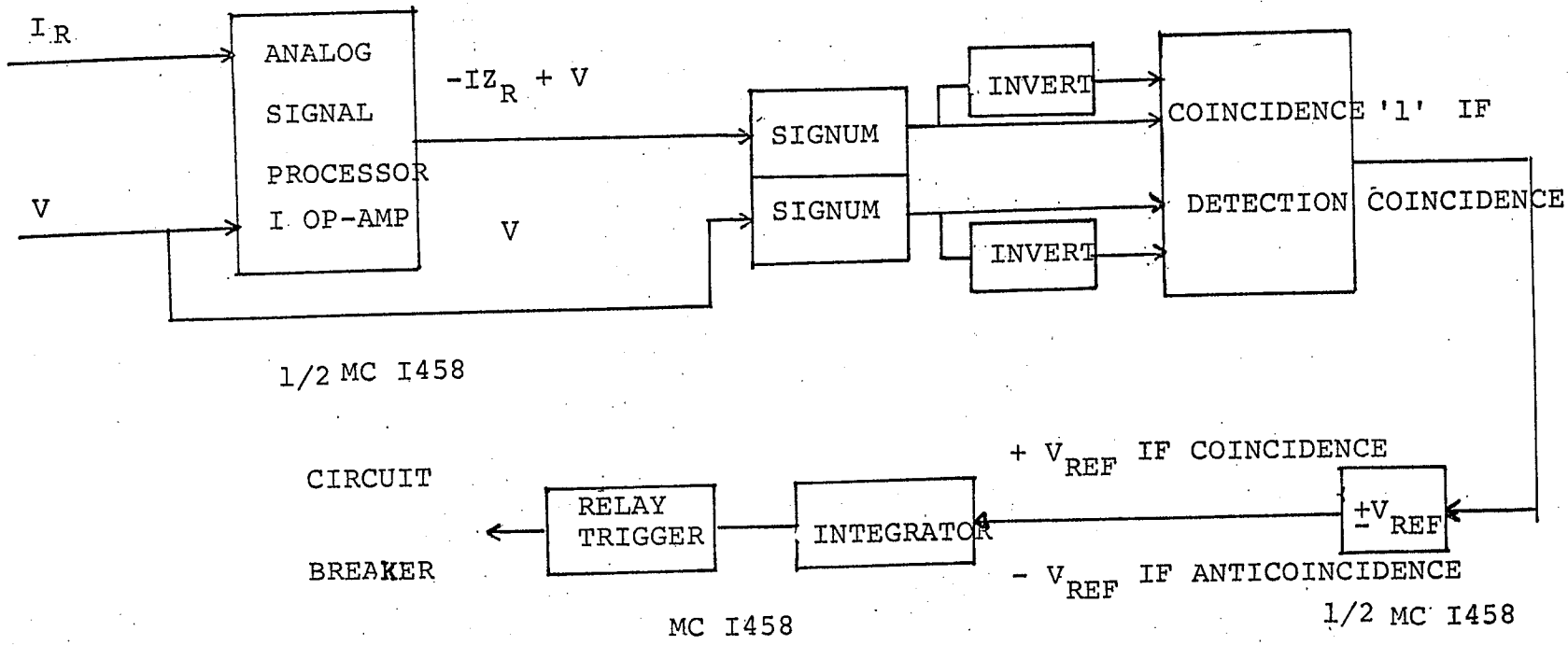
$$H(jw) = \frac{jwRC_d}{1 + jwR_dC_d}$$

The cutoff frequency is set at I80 Hz. The following parameters are subsequently deduced.

$$1/R_dC_d = 2\pi I80$$
$$C_d = 1/377R$$
$$R_d = 0.333R$$
$$Z_4 = R + R_d + 1/jwC_d$$
$$Z_5 = R_d + 1/jwC_d = Z_2$$

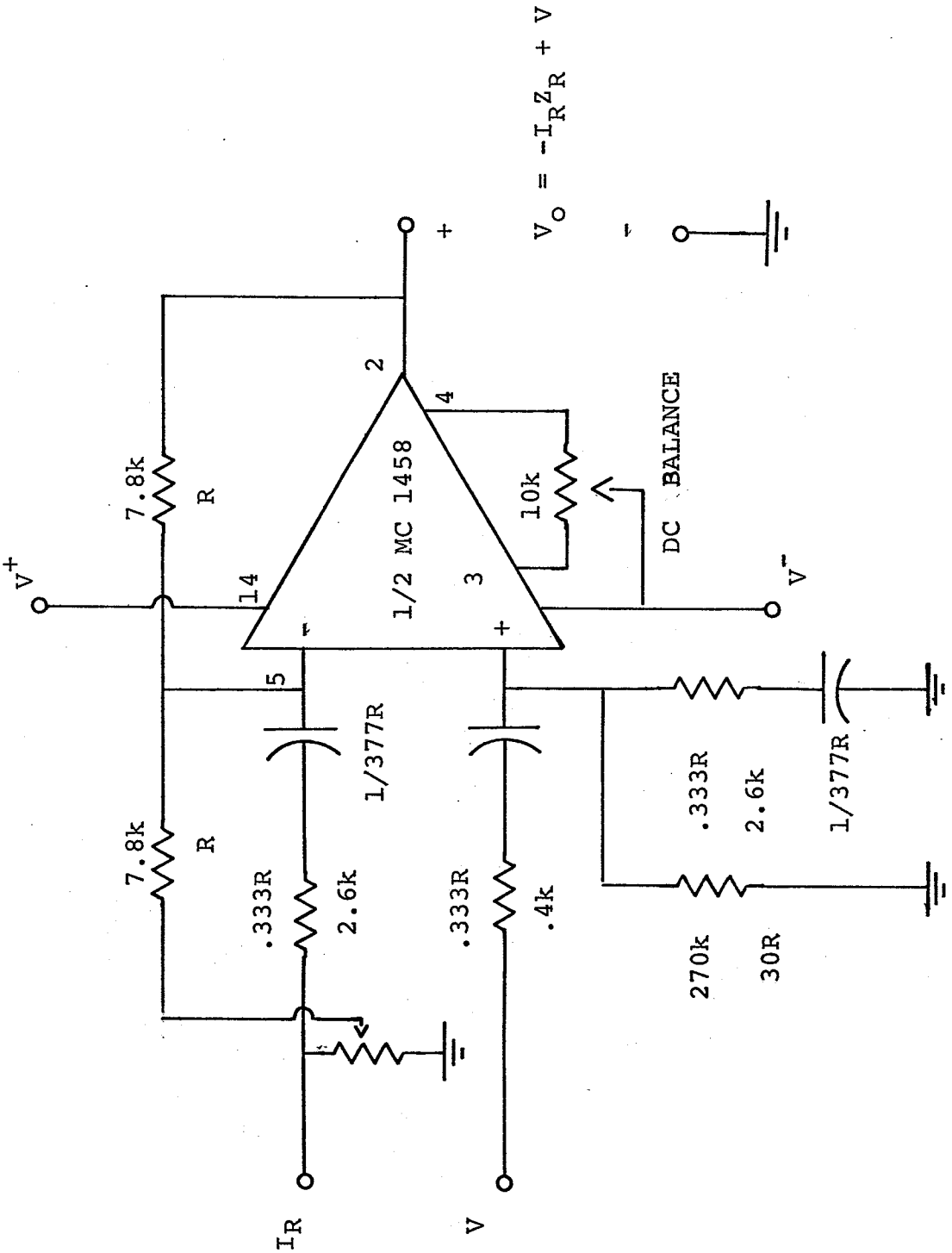


Replica Impedance $Z_R = R_R + jWL_R$



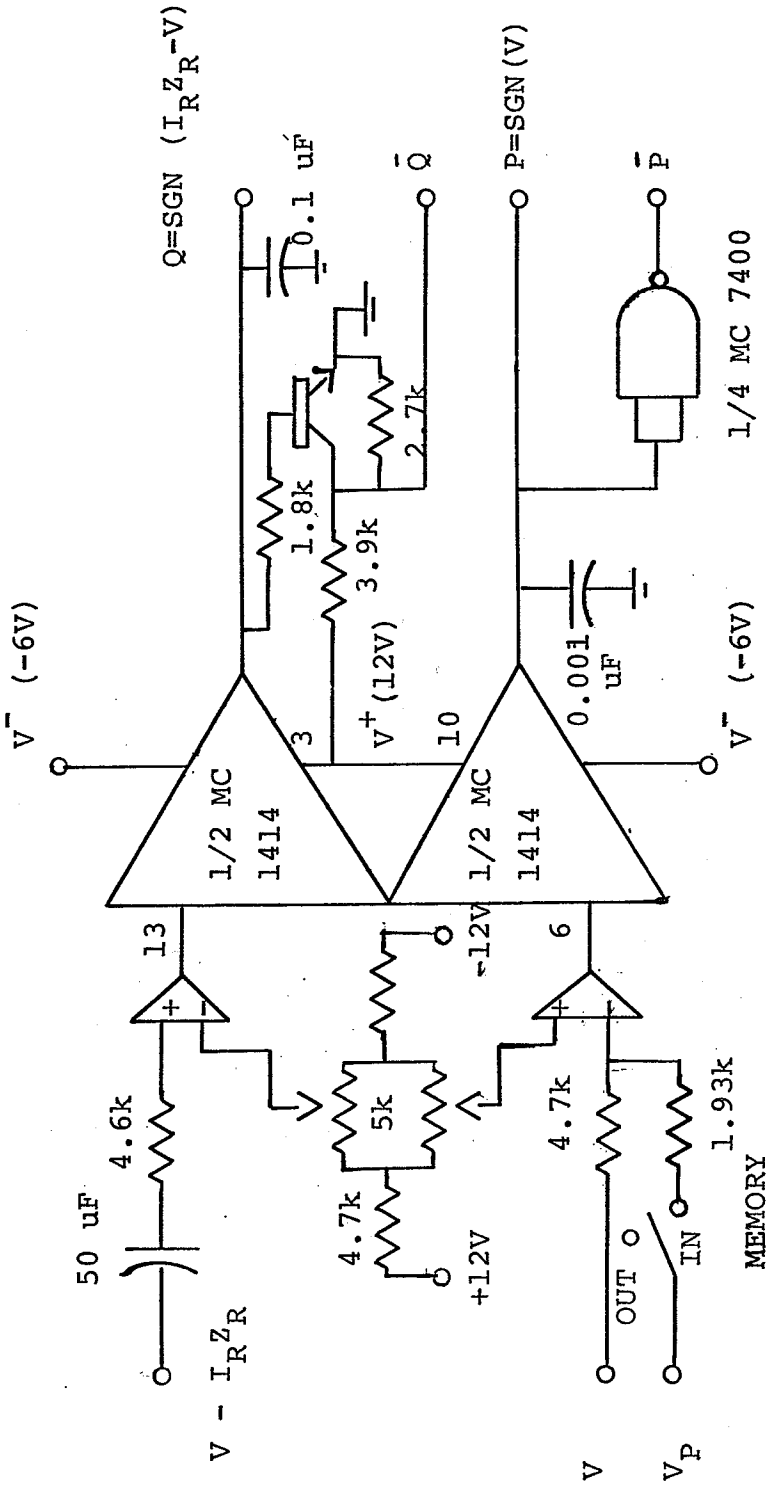
An electronic Relay using a block average Comparator.

Fig. A.1



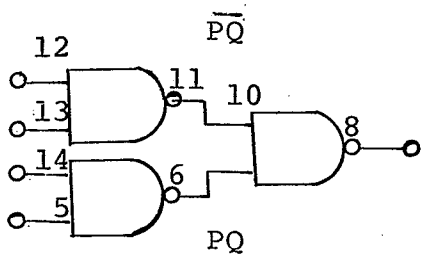
Analog signal processor

Fig. A.2



Circuit configuration for sign detection (Signum Function)

Fig. A.3

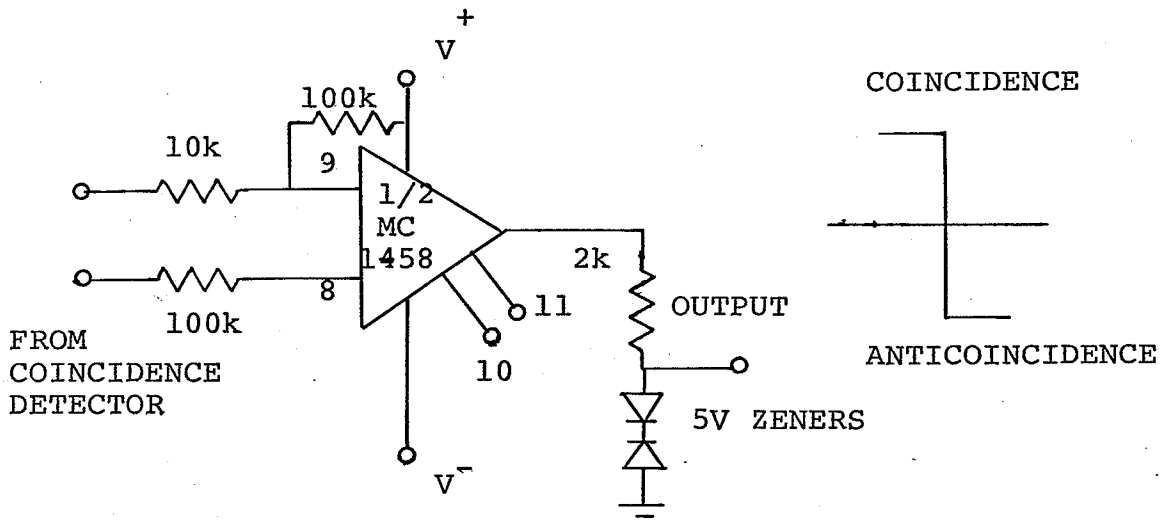


$F = PQ + \overline{P}\overline{Q}$

'1' IF COINCIDENCE

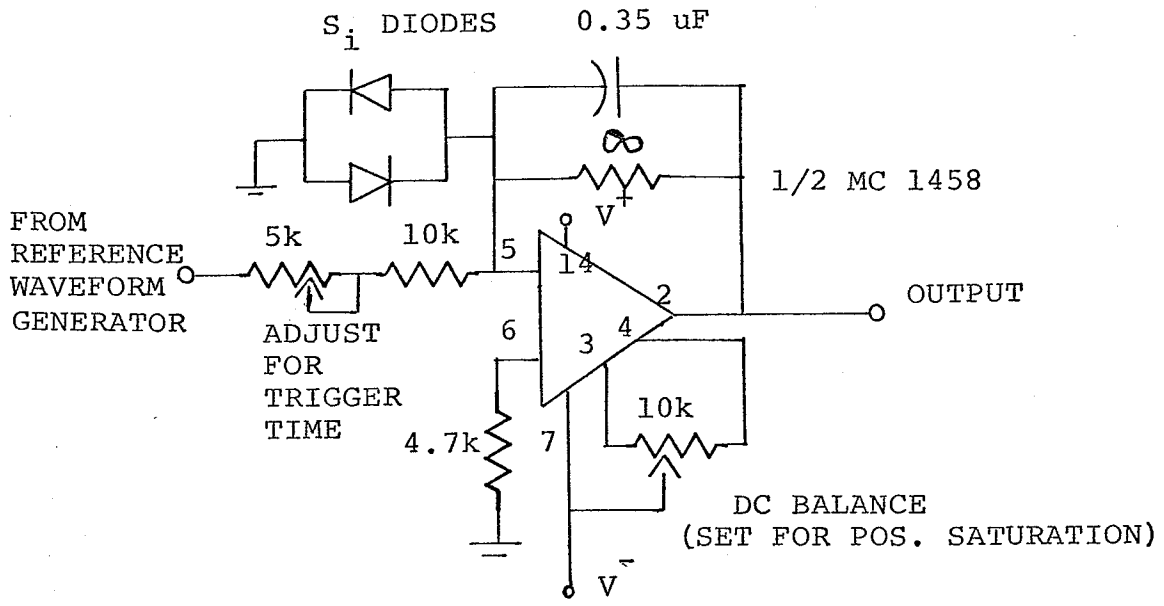
'0' IF ANTICOINCIDENCE

Coincidence Detector

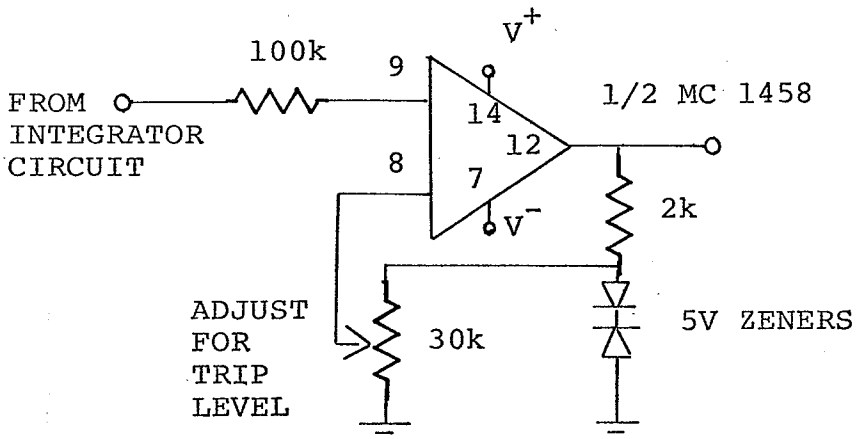


Reference waveform generator

Fig. A.4

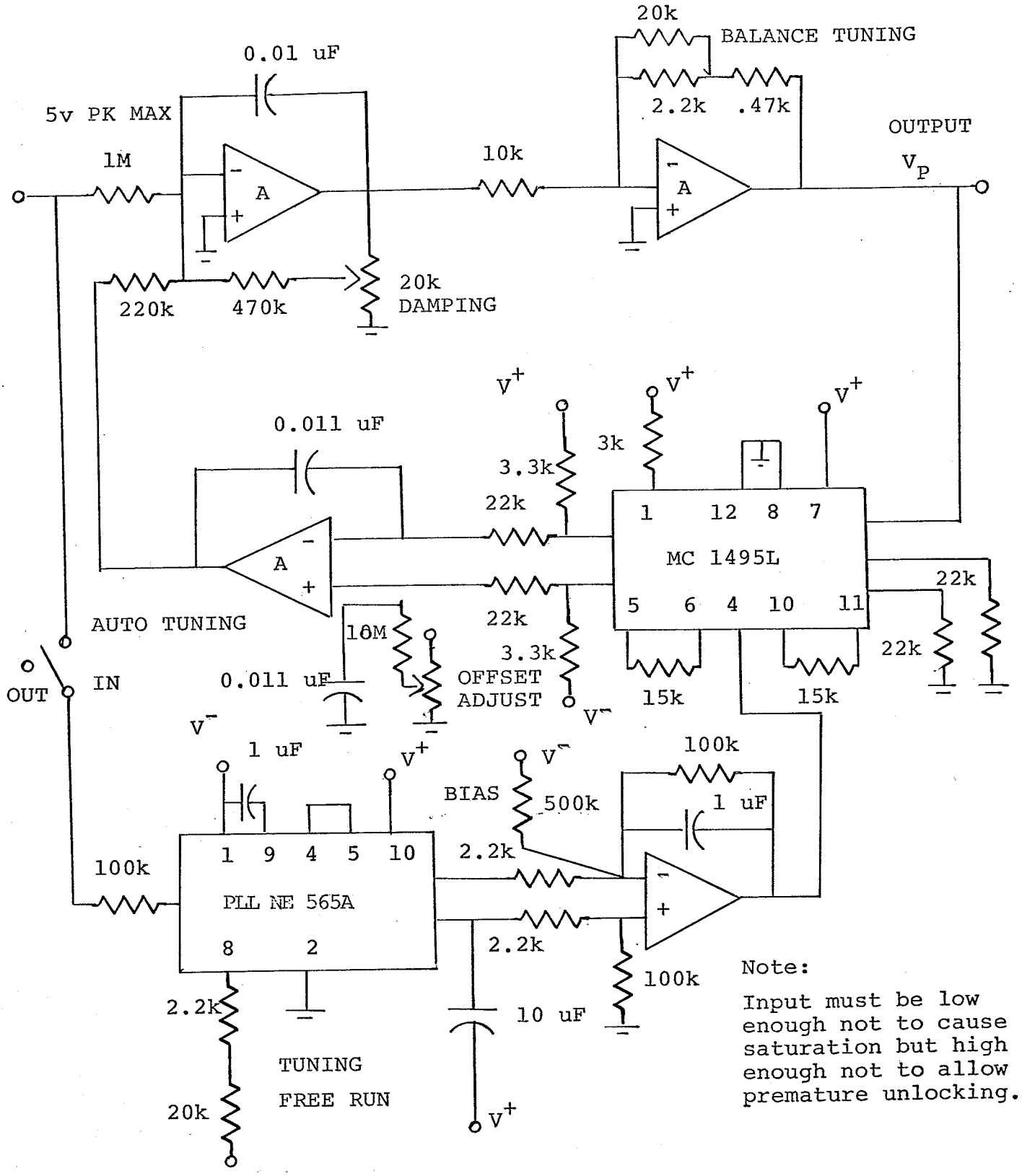


Integrator circuit



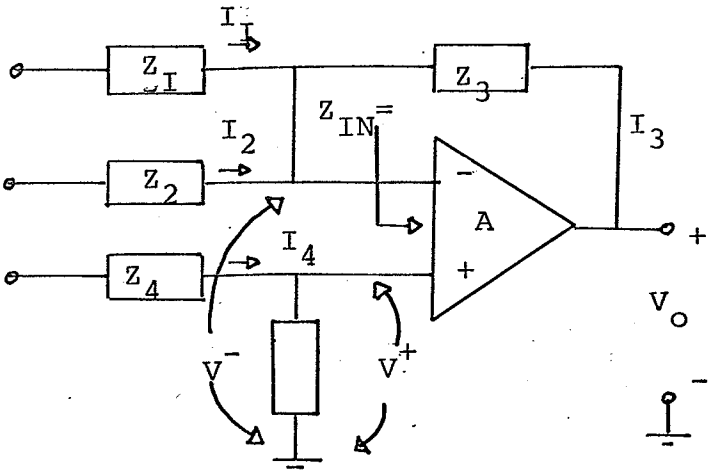
Trigger circuit with hysteresis

Fig. A.5



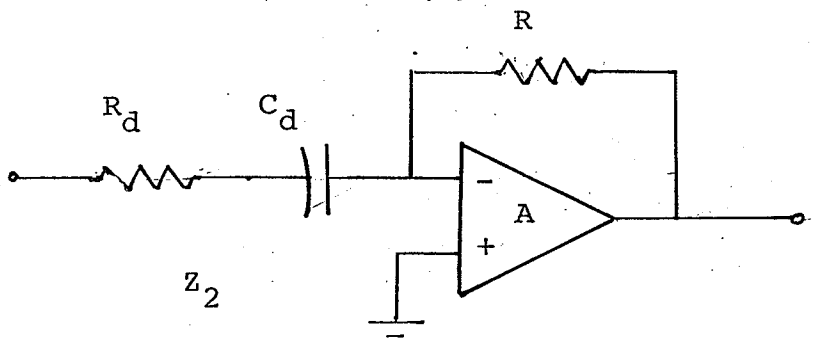
Self-tuning memory circuit

Fig. A.6



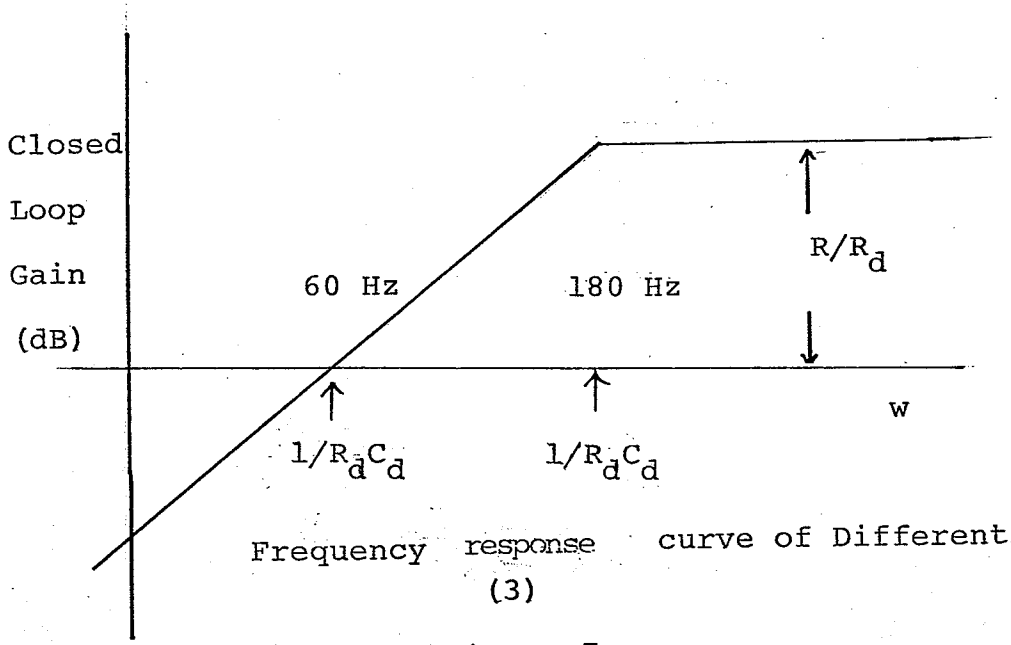
Analog Signal Processor

(I)



Differentiator

(2)



Frequency response curve of Differentiator

(3)

Fig. A.7

APPENDIX B

This appendix gives the listing of the main BASIC program, the Assembly Language subprogram and the System Function Table of the static relay test. The BASIC main program is accessed via the command OLD "JJSS2". When the test is run, the program requests for the relay input current level and the angle and number of revolutions for the iteration. The Assembly Language subprograms which reset the relay, apply the signals to the relay and simulate the time are listed under the title JJSCON. The BASIC version which contains the main test program and the Assembly subprograms is called JJSS2.

THIS STATIC TEST PROGRAM JJSS2 PLOTS THE MHO CIRCLE OF A RELAY

```
10 REM A PROGRAM TO INVESTIGATE THE STEADY STATE
20 REM CHARACTERISTIC OF SOLID STATE RELAY
30 REM JAMAL JARJIS MSC THESIS MAY 1976
40 DIM C(20),V(20)
50 CALL "DFIX"(4000)
60 CALL "INIT"
70 CALL "RSTR"("JJSS1")
80 LET X1=-1.5\X2=3.5\Y1=-1.5\Y2=3.5
90 CALL "SCAL"(X1,Y1,X2,Y2)
200 PRINT "TYPE MAGNITUDE OF CURRENT FROM 0 TO 5"
220 INPUT C1
240 C2=409.5*C1
250 CALL "APNT"(2,1.5,0,-3)
255 CALL "TEXT"("CURRENT =")
260 J$=STR$(C1)
265 CALL "APNT"(2.7,1.5,0,-3)
270 CALL "TEXT"(J$)
305 PRINT "WRITE INCREMENT ANGLE AND N0: OF ROTATION"
306 INPUT P2,N1
307 LET M=0\P1=0


310 REM
320 REM CYCLE OF CURRENT AND VOLTAGE
330 REM
340 REM INITIAL VALUE  OF CURRENT IS 2.5
345 LET T=0
360 T1=8.33000E-04
370 FOR I=1 TO 20
380 C(I)=2047+INT(C2*SIN(376.99*T-P1*.017453))
390 T=T+T1
400 NEXT I
410 REM INITIAL VALUE OF VOLTAGE IS 4.5
415 LET T=0
420 LET V1=4.5\V2=409.5*V1
430 FOR J=1 TO 20
440 V(J)=2047+INT(V2*SIN(376.99*T))
445 T=T+T1
450 NEXT J
460 REM SET UP D/A AND A/D
470 CALL "CLR"
480 REM START TESTING BY  OUTPUT OF
```

```
490 REM FIRST 20 SAMPLES OF CURRENT AND VOLTAGE IN
500 REM FIRST CYCLE. THE SUPPROGRAM JJSSOP COMPUTE
510 REM THE REST OF SAMPLES UNTIL TRIP OR N=360
511 FOR Q=1 TO 1000
512 NEXT Q
520 CALL "SSNV"(C,V,N,X)
530 REM @ VOLT=2047/ FOR TRIP X>2047
550 IF X>2047GO TO 600
560 REM NO TRIP
565 X=0
580 C=4.5\V=0\Z1=0
590 GO TO 650
600 REM TRIP
605 X=1
620 C=2.5*(1.00146^N)
630 V=4.5*(.981^N)
640 Z1=1.8*(.9796^N)
650 REM DISPLAY OF Z ON R-X PLANE
660 REM INITIAL VALUE OF Z =1.8
670 LET Z0=1.8\L=1
680 LET Z=Z0
685 REM
686 CALL "SUBP"(L)
690 X7=Z*COS(P1*.017453)
700 Y7=Z*SIN(P1*.017453)


710 CALL "APNT"(X7,Y7,0,3)
720 S$=STR$(L)
730 CALL "TEXT"(S$)
735 CALL "ESUB"
750 CALL "TIME"(.5*60)
760 CALL "TIMR"(E)
770 IF E<>0 THEN 760
775 CALL "ERAS"(L)
780 Z=Z-.3\L=L+1
790 IF Z>Z1GO TO 685
800 Z=Z1
810 X8=Z*COS(P1*.017453)
820 Y8=Z*SIN(P1*.017453)
830 CALL "APNT"(X8,Y8,0,8)
970 LET N=0\X=0
1000 P1=P1+P2
1020 IF P1<360GO TO 310
1030 M=M+1
1040 IF M>=N1GO TO 1100
1050 P1=P1-360
1060 GO TO 310
1100 END
*
```

THIS ASSEMBLER SUBPROGRAM JJSCON IS USED WITH THE

MAIN BASIC STATIC TEST PROGRAM

```
        .TITLE  JJSCON
        .MCALL  .REGDEF,..V2.
        ..V2..
        .REGDEF
        .GLOBL  ERRSYN,ERRARG
        .GLOBL  JAMAL,.LPAR,.RPAR,.COMMA,CLEARX
        .GLOBL  TMEX,TMRX


CLEARX: CLR     @#170400        ;RECTIFY A/D ERROR
        MOV     @#170402,#0

        TSTB    @#170416        ;CHECK IF LAST D/A DONE
        BPL     .-4
        MOV     #4000,170420    ;SET I-D/A REGISTER
        TSTB    @#170416
        BPL     .-4
        MOV     #4000,170422    ;SET V-D/A REGISTER
SET:    INC     @#170400        ;START A/D
        TST     @#170400        ;TEST FOR A/D BUFFER
        BMI     EIAD            ;IF SO,GOTO ERROR MSG
        TSTB    @#170400        ;CHECK IF LAST A/D DONE
        BPL     SET+4
        MOV     @#170402,R4
        TST     R4
        BNE     SET             ;CHECK FOR SET
        RTS     PC

JAMAL:  CMPB    (R1)+,#.LPAR    ;CHECK IF "(" PRESENT
        BNE     SYNERR          ;IF SO, SYN ERROR
        MOVB    (R1)+,R2
        BMI     SYNERR          ;IF SO SYN ERROR
        SWAB    R2
        BISB    (R1)+,R2
        ADD     (R5),R2         ;OBTAIN ABSOLUTE ADDR OF ARRAY
        CMP     (R2)+,#177776   ;CHECK FOR ARRAY
        BNE     ARGERR          ;IF SO, ARG ERROR
        MOV     (R2)+,FPOAC     ;ADDRESS OF CURRENT ARRAY
        MOV     (R2)+,LPOAC     ;LENGTH OF CURRENT ARRAY
        CMP     (R2)+,#-1       ;TEST FOR 1-D ARRAY
        BNE     ARGERR          ;IF SO, ARG ERROR
```

```
CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
BNE     SYNERR          ;IF SO, SYN ERROR

MOVB    (R1)+,R3
BMI     SYNERR          ;IF SO, SYN ERROR
SWAB    R3
BISB    (R1)+,R3        ;OBTAIN OFFSET ADDR OF VOLTAGE ARRAY
ADD     (R5),R3         ;OBTAIN ABS ADDRESS OF VOLTAGE ARRAY
CMP     (R3)+,#177776   ;CHECK FOR ARRAY
BNE     ARGERR          ;IF SO, ARG ERROR
MOV     (R3)+,FPOAV     ;ADDRESS OF VOLTAGE ARRAY
CMP     (R3)+,LPOAC     ;CHECK EQUALITY OF ARRAY LENGTH
BNE     ARGERR          ;IF SO, ARG ERROR
CMP     (R3)+,#-1       ;TEST FOR 1-D ARRAY
BNE     ARGERR          ;IF SO, ARG ERROR

CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
BNE     SYNERR          ;IF SO, SYN ERROR

MOVB    (R1)+,R4        ;
BMI     SYNERR          ;IF SO SYN ERROR
SWAB    R4
BISB    (R1)+,R4
ADD     (R5),R4         ;OBTAIN ABS ADDR OF CYCLE COUNTER
CMP     (R4)+,#177775   ;TEST FOR NUMERIC SCALAR
BNE     ARGERR          ;IF SO ARG ERROR
CLR     (R4)+           ;CLEAR LOWER BYTE  N
CLR     (R4)            ;CLEAR HIGHER BYTE N

CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
BNE     ARGERR          ;IF SO, SYN ERROR


MOVB    (R1)+,R0
BMI     SYNERR          ;IF SO, SYN ERROR
SWAB    R0
BISB    (R1)+,R0
ADD     (R5),R0         ;OBTAIN ABS ADDR OF TRIP SIGNAL
CMP     (R0)+,#177775   ;TEST FOR NUMERIC SCALAR
BNE     ARGERR          ;IF SO, ARG ERROR
CLR     (R0)+           ;CLEAR X
CLR     (R0)            ;CLEAR X (HIGHER BYTE)

CMPB    (R1)+,#.RPAR    ;CHECK IF ")" PRESENT
BNE     SYNERR          ;IF SO, SYN ERROR

MOV     R4,CLCR         ;ADDRESS OF CYCLE COUNTER
```

```
        MOV     FPOAC,R2            ;ADDRESS OF CURRENT ARRAY
        ADD     #12,R2              ;GETTING CORRECT LOCATION
        MOV     FPOAV,R3            ;ADDRESS OF VOLTAGE ARRAY
        ADD     #12,R3              ;GETTING CORRECT LOCATION
        MOV     LPOAC,R1            ;NUMBER OF SAMPLES(COUNTER)

        TST     R1                  ;INITIALISE COUNTER SAMPLES

        MOV     #INTSIG,@#344       ;INTERRUPT VECTOR-ROUTINE ADDR
        MOV     #240,@#346          ;INTERRUPT VECTOR-PROCESSOR ADDR
        MOV     #40,@#170400        ;SET A/D STATUS REGISTER-CLK OVFL

        MOV     #-1501,@#170406     ;CLOCK COUNTER SET=.833MSEC
        MOV     #503,@#170404       ;START CLOCK AT 1MHZ

J1:     WAIT                        ;WAIT UNTIL INTERRUPT
        BR      J1                  ;GO AND WAIT AGAIN

SYNERR:
        JMP     ERRSYN              ;SYN ERROR
ARGERR:
        JMP     ERRARG              ;ARG ERROR
EIAD:
        CLR     @#170404            ;STOP CLOCK
        CLR     @#170400            ;CLEAR ERROR FLAG
        MOV     @#170402,(R0)       ;MOVE DATA FROM REGISTER
        TRAP    0
        .ASCIZ  "A/D ERROR"         ;PRINT ERROR MSG

INTSIG:
        TSTB    @#170416            ;CHECK IF LAST D/A DONE
        BPL     INTSIG              ;IF NOT, WAIT TILL DONE
        MOV     (R2),@#170420       ;OUPUT SAMPLED CURRENT
        TSTB    @#170416
        BPL     .-4
        MOV     (R3),@#170422       ;OUPUT SAMPLED VOLTAGE

J2:
        TST     @#170400            ;TEST FOR A/D OF RELAY SET
        BMI     EIAD                ;IF SO, GOTO ERROR MSG
        TSTB    @#170400            ;CHECK IF LAST A/D DONE
        BPL     J2
        MOV     #6000,R4            ;SET LEVEL FOR TRIP
        SUB     @#170402,R4         ;CHECK FOR TRIP
        BPL     J3                  ;IF NOT, GOTO J3
        MOV     @#170402,(R0)       ;TRANSFER TRIP SIG TO R0
        CMP     @CLCR,#5            ;SKIP FIRST 5 CYCLES
        BLT     J3
        BR      J7                  ;BRANCH TO OUTPUT ROUTINE
```

```
J3:     CMP     @CLCR,#5
        BGE     J4
        CMP     (R2)+,(R2)+     ;UPDATE SIGNAL ADDRESS
        CMP     (R3)+,(R3)+
        DEC     R1
        BEQ     J5
        RTI
J4:     TST     (R2)+           ;UPDATE CURRENT LOCATION
        TST     (R2)+           ;SIMILARLY

        MOV     (R3),R4         ;MULT VOLTAGE SAMPLE BY 0.981
        MOV     #1,-(SP)
        SUB     #2048.,R4       ;OBTAIN ABS VALUE OF SAMPLE
        BPL     L3              ;TEST FOR SIGN
        NEG     (SP)
        NEG     R4
L3:     MOV     R4,RES1         ;FACTOR 1
        CLR     R5              ;DOUBLE PRECISION ADDITION
        CLR     RES2            ;THE SECOND WORD OF RESULT
        ASL     R4
        ASL     R4
        ADD     R4,RES1         ;FACTOR OF 4
        ASL     R4
        ASL     R4
        ADD     R4,RES1         ;FACTOR OF 16
        ADC     RES2
        ASL     R4
        ROL     R5              ;PUT CARRY BIT INTO R5
        ASL     R4
        ROL     R5
        ADD     R4,RES1         ;FACTOR OF 64
        ADC     RES2
        ADD     R5,RES2         ;RES1 & RES2 CONTAINS MULT 85
        MOV     RES1,R4
        MOV     RES2,R5

        ASL     R4              ;DIVISION BY 2 TO POWER 11
        ROL     R5
        ASL     R4
        ROL     R5
        ASL     R4
        ROL     R5
        ASL     R4
        ROL     R5
        ASL     R4
        ADC     R5
        TST     (SP)+           ;CHECK FOR SIGN
        BPL     L4              ;IF NEG, MAKE PSITIVE
        NEG     R5
```

```
L4:     SUB     R5,(R3)+
        TST     (R3)+           ;OBTAIN NEXT SAMPLE
        DEC     R1              ;DECRE SAMPLE COUNTER
        BEQ     J5
        RTI
J5:     INC     @CLCR           ;INCRE CYCLE COUNTER
        CMP     @CLCR,#360.     ;CHECK IF COUNTER = 360
        BNE     J6
        BR      J7
J6:     MOV     LPOAC,R1        ;RESET SAMPLE COUNTER
        TST     R1
        MOV     FPOAC,R2        ;OBTAIN ADDRESS OF C-ARRAY
        ADD     #12,R2
        MOV     FPOAV,R3        ;OBTAIN ADDRESS OF V-ARRAY
        ADD     #12,R3
        RTI
J7:     CLR     @#170404
        MOV     2(SP),@#177776
        CMPB    (SP)+,(SP)+
        RTS     PC
FPOAC:  .WORD   0
FPOAV:  .WORD   0

LPOAC:  .WORD   0

CLCR:   .WORD   0

RES1:   .WORD   0

RES2:   .WORD   0

;TIME FUNCTIONS

        .GLOBL  GETARG,STORE,INT
FAC1    =40
FAC2    =42
;"TMEX"(X)

TMEX:   MOV     PC,R2
        MOV     #A1,R0
        JSR     PC,GETARG
        .BYTE   1,0
        MOV     A1,FAC1(R5)
        BEQ     L1
        MOV     A2,FAC2(R5)
        JSR     PC,INT
        MOV     FAC2(R5),A2
        MOV     FAC1(R5),A1
```

```
L1:     ADD     #CLKINT,R2
        MOV     R2,@#344
        MOV     #240,@#346
        MOV     #177777,@#170406
        MOV     #717,@#170404
        RTS     PC

;"TMRX"(X)

TMRX:   MOV     #B,R0
        JSR     PC,GETARG
        .BYTE   2,0
        MOV     A1,FAC1(R5)
        MOV     A2,FAC2(R5)
        MOV     #B,R0
        JSR     PC,STORE
        RTS     PC
A1:     .WORD   0
A2:     .WORD   0
B:      .WORD   0,0,0
;INTERRUPT ROUTINE

CLKINT: DEC     A2
        BNE     RETURN
        DEC     A1
        BLE     .+12
        MOV     #-1,A2
        BR      RETURN
        CLR     @#170404
        CLR     A1
RETURN: RTI
        .END
```

THIS SYSTEM SYMBOL TABLE IS USED BY THE MAIN BASIC TEST PROGRAM

TO ACCESS THE USER WRITTEN ASSEMBLY LANGUAGE SUBPROGRAMS

```
R EDIT
*EDERJJTBL.MAC$$


        .CSECT  BASICR
        .GLOBL FTBL

        .CSECT
FTBL:
        .GLOBL  AGET,APNT,APUT,CONT,ERAS,ESUB,FPUT
        .GLOBL  FIGR,FPUT,INIT,LPEN,RDOT
        .GLOBL  SCAL,STAT,DSTP,SUBP,TEXT,TRAK
        .GLOBL  VECT,XGRA,YGRA,FIX,FREE
        .GLOBL  NOSC,ON,OFF,SAVE
        .GLOBL  RSTR,JAMAL,CLEARX,TMEX,TMRX
        .ASCII  /SCAL/
        .WORD    SCAL
        .ASCII  /VECT/
        .WORD    VECT
        .ASCII  /RDOT/
        .WORD    RDOT
        .ASCII  /APNT/
        .WORD    APNT
        .ASCII  /STAT/



        .WORD    STAT
        .ASCII  /TEXT/
        .WORD    TEXT
        .ASCII  /SUBP/
        .WORD    SUBP
        .ASCII  /ESUB/
        .WORD    ESUB
        .ASCII  /LPEN/
        .WORD    LPEN
        .ASCII  /NOSC/
        .WORD    NOSC
        .ASCII  /DON/
        .BYTE   0
        .WORD    ON
        .ASCII  /ON/
        .WORD   0
        .WORD   ON      ; SECOND NAME
        .ASCII  /OFF/
        .BYTE   0
        .WORD    OFF
        .ASCII  /TRAK/
        .WORD    TRAK
```

```
.ASCII  /ERAS/
.WORD    ERAS
.ASCII  /INIT/
.WORD    INIT
.ASCII  /DSTP/
.WORD    DSTP
.ASCII  /STOP/   ;SECOND NAME
.WORD   DSTP
.ASCII  /DCNT/
.WORD    CONT
.ASCII  /CONT/   ;SECOND NAME
.WORD   CONT
.ASCII  /XGRA/
.WORD    XGRA
.ASCII  /YGRA/
.WORD    YGRA
.ASCII  /AGET/
.WORD    AGET
.ASCII  /DFIX/
.WORD   FIX
.ASCII  /FIX/    ;SECOND NAME
.BYTE   0
.WORD    FIX
.ASCII  /FREE/
.WORD    FREE


.ASCII  /APUT/
.WORD    APUT
.ASCII  /FIGR/
.WORD    FIGR
.ASCII  /FPUT/
.WORD    FPUT
.ASCII  /DSAV/
.WORD    SAVE
.ASCII  /SAVE/   ;SECOND NAME
.WORD   SAVE
.ASCII  /RSTR/
.WORD    RSTR
.ASCII  /TACV/
.WORD   JAMAL
.ASCII  /CLR/
.BYTE   0
.WORD   CLEARX
.ASCII  /TIME/
.WORD   TMEX
.ASCII  /TIMR/
.WORD   TMRX
.WORD   0        ;END OF THE BASIC FUNCTION TABLE.
.END
*
```

APPENDIX C

This appendix gives the listing of the Main BASIC program and the Assembly Language subprograms of the dynamic relay test. The BASIC main program is assessed via the command OLD "JJTR1". The command OLD "JJTR3" calls for the BASIC main program which tests the relay for its operating time characteristic. The Assembly Language subprograms are listed under the title JJTALR. The BASIC version which contains the main test program and the Assembly subprogram is called JJBV1.

THIS DYNAMIC TEST PROGRAM JJTR3 PLOTS THE OPERATING TIME

CHARACTERISTIC OF THE RELAY

```
JJTR1   30-JUN-76  BASIC V01-05

10 REM A PROGRAM TO INVESTIGATE THE TRANSIENT
20 REM CHARACTERISTIC OF SOLID STATE RELAY
30 REM JAMAL JARJIS MSC THESIS MAY 1976
40 DIM C(100),V(100)
50 CALL "INIT"\CALL "DFIX"(3200)\CALL "RSTR"("JJTR1")
70 LET X1=-1.5\X2=3.5\Y1=-1.5\Y2=3.5
80 CALL "SCAL"(X1,Y1,X2,Y2)
110 LET Z1=.2\REM Z1 IS  SOURCE
120 LET Z2=1\REM Z2 IS  LINE
130 LET R3=1.5\REM R3 IS  FAULT
135 LET P1=85*.017453\P2=85*.017453
137 LET R7=.2\REM R7 IS THE INCRE
140 R2=Z2*COS(P2)\X2=Z2*SIN(P2)
142 CALL "APNT"(0,0,0,-3)\CALL "VECT"(R2,X2)
150 R2=Z2*COS(P2)\X2=Z2*SIN(P2)
155 R1=Z1*COS(P1)\X1=Z1*SIN(P1)
160 LET W=377\V=3
180 A=(R1+R2+R3)*W/(X1+X2)
190 B=(V*W)/(X1+X2)\D1=(B*W)/(A^2+W^2)
210 D2=SQR(B/(W*D1))\E1=-ATN(W/A)
230 L2=X2/W\T1=8.3333*1.00000E-04
231 Z8=X1^2+X2^2+R1^2+R2^2+R3^2
232 Z9=SQR(Z8)
233 IF Z9<=.5GO TO 1310
250 REM STEADY STATE  PART OF SIGNAL
270 V5=V*409.5\T=T1
290 FOR I=1 TO 20
300 C(I)=2047\V(I)=2047+INT(V5*SIN(W*T))
320 T=T+T1
330 NEXT I
350 REM TRANSIENT
360 T=0
370 FOR I=21 TO 80
390 C2=D2*SIN(W*T+E1)
400 C(I)=D1*(EXP(-A*T)+C2)
405 C(I)=INT(C(I)*409.5)+2047
420 V1=L2*D1*(-A*EXP(-A*T))*409.5
430 V2=L2*D1*D2*W*COS(W*T+E1)*409.5
440 V(I)=INT((R1+R2)*(C(I)-2047)+(V1+V2+2047))
450 T=T+T1
```

```
460 NEXT I
500 REM STEADY STATE
510 F1=R1+R2+R3\F2=X1+X2\B1=ATN(F2/F1)
540 F3=SQR(F1^2+F2^2)\F4=R3+R2\F5=X2
570 B2=ATN(F5/F4)\F6=SQR(F4^2+F5^2)
575 PRINT Z2,R3,F6,F3
590 T=0.
610 FOR I=81 TO 100
620 C(I)=INT((V5/F3)*SIN(W*T-B1)+2047)
630 V(I)=INT(V5*(F6/F3)*SIN(W*T-B1+B2)+2047)
640 T=T+T1
650 NEXT I
710 REM OUTPUT CURRENT AND VOLTAGE
730 CALL "CLR"
750 CALL "TACV"(C,V,N,X)
900 REM
960 IF X>2047GO TO 1030
970 REM NO TRIP
980 X=0\R5=R4\R4=R3
990 IF R4>R5GO TO 1020
1000 R3=R4-(R5-R4)/2\GO TO 1100
1010 REM TRIP
1020 R3=R4-(R4-R5)/2\GO TO 1100
1030 REM TRIP
1040 X=1\R5=R4\R4=R3
1050 IF R4>R5GO TO 1070
1060 R3=R4+(R5-R4)/2\GO TO 1100
1070 R3=R4+(R4-R5)/2
1100 REM GRAPHICS
1110 M=M+1\CALL "SUBP"(M)
1120 X9=Z2*COS(P1)+R4\Y9=Z2*SIN(P1)
1130 CALL "APNT"(X9,Y9,0,3)
1140 S$=STR$(M)\CALL "TEXT"(S$)\CALL "ESUB"
1150 T$=STR$(X)\CALL "APNT"(X9,Y9+.1,0,3)
1160 CALL "TEXT"(T$)
1170 CALL "TIME"(.5*60)
1180 CALL "TIMR"(E)
1190 IF E<>0 THEN 1180
1200 CALL "ERAS"(M)
1300 IF M<=6GO TO 180
1310 CALL "APNT"(X9,Y9,0,7)
1320 Z2=Z2-.15\R3=1.5\IF Z2<=0GO TO 1400
1325 R4=0\R5=0\M=0
1330 GO TO 150
1400 END
```

THIS DYNAMIC TEST PROGRAM JJTR1 PLOTS THE LOCUS IN THE

FIRST QUADRANT OF THE R-X PLANE OF THE RELAY

JJTR3 BASIC V01-05

```
10 REM A PROGRAM TO INVESTIGATE THE OPERATING
20 REM TIME OF SOLID STATE RELAY
30 REM JAMAL JARJIS MSC THESIS MAY 1976
40 DIM C(100),V(100)
50 CALL "INIT"\CALL "DFIX"(3200)\REM CALL "RSTR"("JJTR1")
70 LET X1=-.5\X2=4.5\Y1=-.5\Y2=4.5
80 CALL "SCAL"(X1,Y1,X2,Y2)
82 REM SCALE Z AXIS
84 FOR I=1 TO 5
86 J5=I/2\J6=J5/5\J9=.5/.1
88 CALL "APNT"(J5+1.5,.05,0,-3)
90 CALL "VECT"(0,-.05)
91 CALL "APNT"(J5+1.5,-.1,0,-3)
92 A1$=STR$(J6)
94 CALL "TEXT"(A1$)
96 NEXT I
100 PRINT "SOURCE","LINE","FAULT","TIME"
110 LET Z1=.7\REM SOURCE
120 LET Z2=1\REM Z2 IS  LINE
125 P9=.017453
135 P1=85*P9\P2=P1\P3=175*P9\P4=90*P9
140 R2=Z2*COS(P2)\X2=Z2*SIN(P2)
142 CALL "APNT"(0,1,0,-3)\CALL "VECT"(R2,X2+1)
150 R2=Z2*COS(P2)\X2=Z2*SIN(P2)
155 R1=Z1*COS(P1)\X1=Z1*SIN(P1)
160 LET W=377\V=3
180 REM MAX OFFSET =175, MIN=85
200 T1=8.33330E-04
250 REM STEADY STATE  PART OF SIGNAL
270 V5=V*409.5\T=T1
290 FOR I=1 TO 20
300 C(I)=2047\V(I)=2047+INT(V5*SIN(W*T+P3))
320 T=T+T1
330 NEXT I
350 REM TRANSIENT
360 F1=R1+R2\F2=X1+X2\B1=ATN(F2/F1)
370 F3=SQR(F1^2+F2^2)
380 B2=ATN(X2/R2)\F6=SQR(R2^2+X2^2)
390 T9=F2/(F1*W)\L2=X2/W
400 S1=0\REM =COS(P4) MAX
410 S2=1\REM =SIN(P4)
```

```
420 C9=(V5/F3)\T=0
430 FOR I=21 TO 80
440 C5=S1*SIN(W*T)
450 C6=S2*(COS(W*T)-EXP(-T/T9))
460 C(I)=INT(C9*(C5+C6))+2048
470 V1=W*S1*COS(W*T)
480 V2=S2*((1/T9)*EXP(-T/T9)-W*SIN(W*T))
490 V3=(C(I)-2048)*R2
500 V(I)=INT(V3+L2*(V1+V2)*C9)+2048
510 T=T+T1\NEXT I
610 FOR I=81 TO 100
620 C(I)=INT((V5/F3)*SIN(W*T-B1+P3)+2047)
630 V(I)=INT(V5*(F6/F3)*SIN(W*T-B1+B2+P3)+2047)
640 T=T+T1\NEXT I
710 REM OUTPUT CURRENT AND VOLTAGE
730 CALL "CLR"
750 CALL "TACV"(C,V,N,X)
900 REM
925 IF N>16GO TO 935
930 T9=(N-3)/60+(C(1)/20)/60\T9=T9*1000\GO TO 940
935 T9=99999
940 PRINT C(1),N
950 PRINT Z1,Z2,R3,T9
960 IF X>2048GO TO 1010
970 REM NO TRIP
980 X=0
990 GO TO 1100
1010 REM TRIP
1040 X=1
1100 REM GRAPHICS
1110 M=M+1
1120 9=Z2*COS(P1)\Y9=Z2*SIN(P1)
1130 CALL "APNT"(X9,Y9+1,0,6)
1150 T$=STR$(X)
1160 CALL "TEXT"(T$)
1170 CALL "TIME"(5*60)
1180 CALL "TIMR"(E)
1190 IF E<>0 THEN1180
1200 Z2=Z2-.1
1210 IF Z2>=0GO T 150
1220 END
READY
```

THIS ASSEMBLER SUBPROGRAM JJTALR IS USED WITH

THE BASIC DYNAMIC TEST PROGRAM

```
        .TITLE  JJTALR
        .MCALL  .REGDEF,,,V2,,
        ,,V2,,
        .REGDEF
        .GLOBL  ERRSYN,ERRARG
        .GLOBL  JAMAL,,LPAR,,RPAR,,COMMA,CLEARX
        .GLOBL  TMEX,TMRX


CLEARX: CLR     @#170400        ;RECTIFY A/D ERROR
        MOV     @#170402,#0
        TSTB    @#170416        ;CHECK IF LAST D/A DONE
        BPL     CLEARX
        MOV     #4000,170420    ;SET I-D/A REGISTER
        MOV     #4000,170422    ;SET V-D/A REGISTER
SET:    INC     @#170400        ;START A/D
        TST     @#170400        ;TEST FOR A/D BUFFER
        BMI     EIAD            ;IF SO GOTO ERROR MSG
        TSTB    @#170400        ;CHECK IF LAST A/D DONE
        BPL     SET+4
        MOV     @#170402,R4
        SUB     #4000,R4
        BPL     SET             ;CHECK FOR SET
        RTS     PC

JAMAL:  CMPB    (R1)+,#.LPAR    ;CHECK IF "(" PRESENT
        BNE     SYNERR          ;IF SO, SYN ERROR
        MOVB    (R1)+,R2
        BMI     SYNERR          ;IF SO SYN ERROR
        SWAB    R2
        BISB    (R1)+,R2
        ADD     (R5),R2         ;OBTAIN ABSOLUTE ADDR OF ARRAY
        CMP     (R2)+,#177776   ;CHECK FOR ARRAY
        BNE     ARGERR          ;IF SO, ARG ERROR
        MOV     (R2)+,FPOAC     ;ADDRESS OF CURRENT ARRAY
        MOV     (R2)+,LPOAC     ;LENGTH OF CURRENT ARRAY
        CMP     (R2)+,#-1       ;TEST FOR 1-D ARRAY
        BNE     ARGERR          ;IF SO, ARG ERROR

        CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
        BNE     SYNERR          ;IF SO, SYN ERROR
```

```
MOVB    (R1)+,R3
BMI     SYNERR          ;IF SO, SYN ERROR
SWAB    R3
BISB    (R1)+,R3        ;OBTAIN OFFSET ADDR OF VOLTAGE ARRAY
ADD     (R5),R3         ;OBTAIN ABS ADDRESS OF VOLTAGE ARRAY
CMP     (R3)+,#177776   ;CHECK FOR ARRAY
BNE     ARGERR          ;IF SO, ARG ERROR
MOV     (R3)+,FPOAV     ;ADDRESS OF VOLTAGE ARRAY
CMP     (R3)+,LPOAC     ;CHECK EQUALITY OF ARRAY LENGTH
BNE     ARGERR          ;IF SO, ARG ERROR
CMP     (R3)+,#-1       ;TEST FOR 1-D ARRAY
BNE     ARGERR          ;IF SO, ARG ERROR

CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
BNE     SYNERR          ;IF SO, SYN ERROR

MOVB    (R1)+,R4        ;
BMI     SYNERR          ;IF SO SYN ERROR
SWAB    R4
BISB    (R1)+,R4
ADD     (R5),R4         ;OBTAIN ABS ADDR OF CYCLE COUNTER
CMP     (R4)+,#177775   ;TEST FOR NUMERIC SCALAR
BNE     ARGERR          ;IF SO ARG ERROR
CLR     (R4)+           ;CLEAR LOWER BYTE  N
CLR     (R4)            ;CLEAR HIGHER BYTE N

CMPB    (R1)+,#.COMMA   ;CHECK IF "," PRESENT
BNE     ARGERR          ;IF SO, SYN ERROR


MOVB    (R1)+,R0
BMI     SYNERR          ;IF SO, SYN ERROR
SWAB    R0
BISB    (R1)+,R0
ADD     (R5),R0         ;OBTAIN ABS ADDR OF TRIP SIGNAL
CMP     (R0)+,#177775   ;TEST FOR NUMERIC SCALAR
BNE     ARGERR          ;IF SO, ARG ERROR
CLR     (R0)+           ;CLEAR X
CLR     (R0)            ;CLEAR X (HIGHER BYTE)

CMPB    (R1)+,#.RPAR    ;CHECK IF ")" PRESENT
BNE     SYNERR          ;IF SO, SYN ERROR

MOV     R4,CLCR         ;ADDRESS OF CYCLE COUNTER


MOV     FPOAC,R2        ;ADDRESS OF CURRENT ARRAY
ADD     #12,R2          ;GETTING CORRECT LOCATION
MOV     FPOAV,R3        ;ADDRESS OF VOLTAGE ARRAY
ADD     #12,R3          ;GETTING CORRECT LOCATION
MOV     #20.,R1         ;NUMBER OF SAMPLES(COUNTER)
```

```
        TST     R1                  ;INITIALISE COUNTER SAMPLES

        MOV     #INTSIG,@#344       ;INTERRUPT VECTOR-ROUTINE ADDR
        MOV     #240,@#346          ;INTERRUPT VECTOR-PROCESSOR ADDR
        MOV     #40,@#170400        ;SET A/D STATUS REGISTER-CLK OVFL

        MOV     #-1501,@#170406     ;CLOCK COUNTER SET=.833MSEC
        MOV     #503,@#170404       ;START CLOCK AT 1MHZ

J1:     WAIT                        ;WAIT UNTIL INTERRUPT
        BR      J1                  ;GO AND WAIT AGAIN

SYNERR:
        JMP     ERRSYN              ;SYN ERROR
ARGERR:
        JMP     ERRARG              ;ARG ERROR
EIAD:
        CLR     @#170404            ;STOP CLOCK
        CLR     @#170400            ;CLEAR ERROR FLAG
        MOV     @#170402,(R0)       ;MOVE DATA FROM REGISTER
        TRAP    0
        .ASCIZ  "A/D ERROR"         ;PRINT ERROR MSG

INTSIG:
        TSTB    @#170416            ;CHECK IF LAST D/A DONE
        BPL     INTSIG              ;IF NOT, WAIT TILL DONE
        MOV     (R2),@#170420       ;OUPUT SAMPLED CURRENT
        MOV     (R3),@#170422       ;OUPUT SAMPLED VOLTAGE

J2:
        TST     @#170400            ;TEST FOR A/D OF RELAY SET
        BMI     EIAD                ;IF SO, GOTO ERROR MSG
        TSTB    @#170400            ;CHECK IF LAST A/D DONE
        BPL     J2
        MOV     #5000,R4            ;SET LEVEL FOR TRIP
        SUB     @#170402,R4         ;CHECK FOR TRIP
        BPL     J4                  ;IF NOT, GOTO J3
        MOV     @#170402,(R0)
        CMP     @CLCR,#3            ;RESTORE S.S STATE -NO TRIP
        BLE     J4

        MOV     FPOAC,R2            ;TEMP STORE OF SAMP CTR
        ADD     #12,R2
        MOV     R1,(R2)
        BR      J8                  ;BRANCH TO OUTPUT ROUTINE

J4:     CMP     (R2)+,(R2)+         ;UPDATE CURRENT SAMP POS:
        CMP     (R3)+,(R3)+         ;UPDATE VOLTAGE SAMP POS:
        DEC     R1                  ;DECRE SAMPLE COUNTER
        BEQ     J5                  ;BRANCH TO J5 IF ZERO
        RTI
```

```
J5:     INC     @CLCR           ;INCRE CYCLE COUNTER
        CMP     @CLCR,#3        ;BRANCH TO J6 AFTER 3 CYCLE
        BGT     J6
        MOV     #20.,R1         ;RESET SAMPLE COUNTER
        SUB     #80.,R2         ;RESET CURRENT POSITION
        SUB     #80.,R3         ;RESET VOLTAGE POSITION
        RTI
J6:     CMP     @CLCR,#6        ;BRANCH TO J7 AFTER 6 CYCLE
        BGT     J7
        MOV     #20.,R1         ;RESET SAMPLE COUNTER
        RTI
J7:     CMP     @CLCR,#16.      ;BRANCH TO J8 AFTER 16 CYCLE
        BGT     J8
        MOV     #20.,R1         ;RESET SAMPLE COUNTER
        SUB     #80.,R2         ;RESET CURRENT LOCATION
        SUB     #80.,R3         ;RESET VOLTAGE LOCATION
        RTI
J8:     CLR     @#170404        ;STOP CLOCK.
        MOV     2(SP),@#177776  ;RESTORE PSW-PROGRAM STACK
        CMPB    (SP)+,(SP)+     ;RESET STACK
        RTS     PC              ;RETURN TO CALLING PROGRAM

FPOAC:  .WORD   0

FPOAV:  .WORD   0

LPOAC:  .WORD   0

CLCR:   .WORD   0

;TIME FUNCTIONS

        .GLOBL  GETARG,STORE,INT
FAC1    =40
FAC2    =42
;"TMEX"(X)

TMEX:   MOV     PC,R2
        MOV     #A1,R0
        JSR     PC,GETARG
        .BYTE   1,0
        MOV     A1,FAC1(R5)
        BEQ     L1
        MOV     A2,FAC2(R5)
        JSR     PC,INT
        MOV     FAC2(R5),A2
        MOV     FAC1(R5),A1
```

```
L1:     ADD     #CLKINT,R2
        MOV     R2,@#344
        MOV     #240,@#346
        MOV     #177777,@#170406
        MOV     #717,@#170404
        RTS     PC

;"TMRX"(X)

TMRX:   MOV     #B,R0
        JSR     PC,GETARG
        .BYTE   2,0
        MOV     A1,FAC1(R5)
        MOV     A2,FAC2(R5)
        MOV     #B,R0
        JSR     PC,STORE
        RTS     PC
A1:     .WORD   0
A2:     .WORD   0
B:      .WORD   0,0,0
;INTERRUPT ROUTINE

CLKINT: DEC     A2
        BNE     RETURN
        DEC     A1
        BLE     .+12
        MOV     #-1,A2
        BR      RETURN
        CLR     @#170404
        CLR     A1
RETURN: RTI
        .END
```

APPENDIX D

The voltage and current signals from the D/A's of the computer are filtered before they are applied to the relay under test. Two identical filters are used for each channel. The filter also has a dual role of providing a buffer stage between the relay and the computer. The circuit configuration of the filter is shown in Fig. (D.1)

The transfer function of the filter has the following form.

$$G(jw) = \frac{R_2/R_1}{1 + jwR_2C}$$

The upper cutoff frequency is set at 180 Hz.

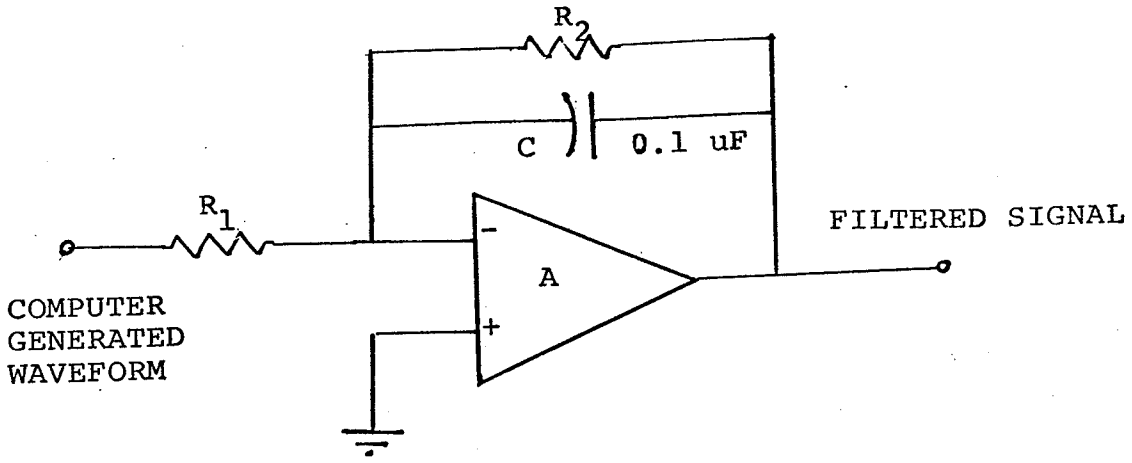
Hence,

$$R_2 = 8.8\ k\ (\text{say } 10k)$$

where C has a value of 0.1 uF.

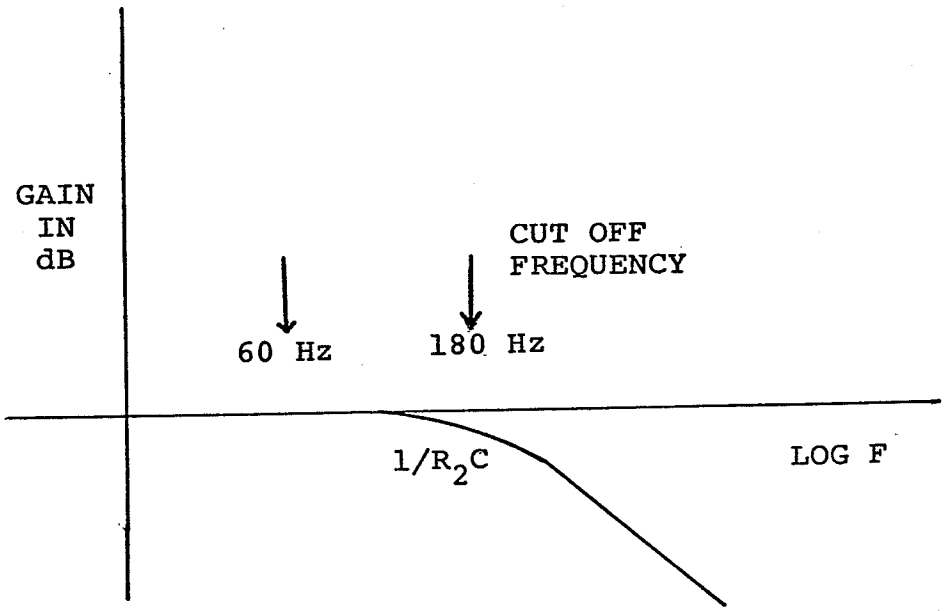
The gain at the fundamental frequency (60 Hz) is 0.995. This could be compensated by making the filter gain as 1/0.995.

A phase shift of (-21^{o}) is introduced at the fundamental frequency by the filter. Since two identical filters are used, there is no relative phase shift being introduced in the input current and voltage signals of the relay.



Filter and Buffer of the test system

(1)



Filter frequency responce

(2)

Fig. D.1

APPENDIX E

In the static test, the current is kept constant while the voltage is exponentially decreased to zero as shown in Fig.(E.I).The value of the voltage initially in the first cycle is taken as 4.5 volts. This constraint is placed by the D/A of the computer. Two conficting requirements are imposed on the duration of the decay of the voltage signal. The volage decay should be sufficient to ensure that the change is slow enough for a static test. But it must not be excessive otherwise the test turnover time would be too long.

The following expression describes the voltage relationship.

$$V_{FINAL} = V_{INITIAL} (1 - \gamma)^{N}$$

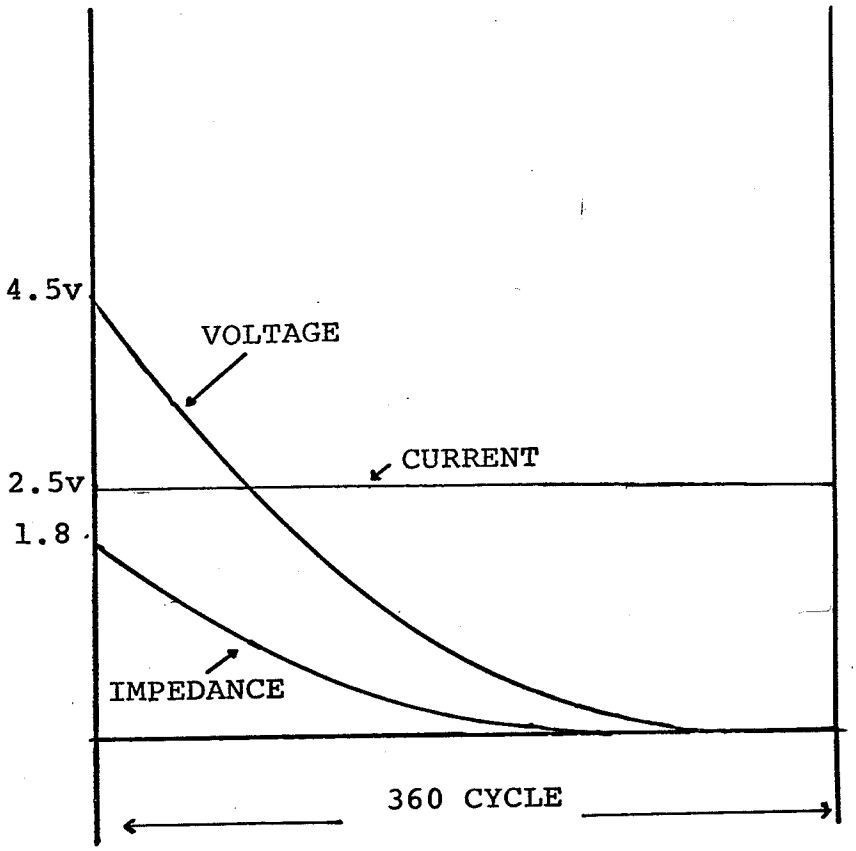
where,

V_{FINAL} = 0.001 $\simeq$ 0

$V_{INITIAL}$ = 4.5 Volts

N = 360 cycles.

From the above expression, the value of γ is deduced and has a value of 0.0I9 or $(1 - \gamma) = 0.98I$. This is the value of the multiplying factor which is used in the static test to simulate the decreasing voltage signal.



Signal profile of the static test.

Fig. E.1