OPTIMIZING THE PARTITIONING OF TANDEM AGV SYSTEMS USING GENETIC AND MEMETIC ALGORITHMS

by

Sijie Liu

A Thesis submitted To the Faculty of Graduate Studies of

The University of Manitoba

in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

Department of Mechanical and Manufacturing Engineering
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THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

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To my dearest mother, Changrong Chen

for her love, encouragement and support

ABSTRACT

An integrated circuit was designed to access and read a prototype chemical sensor array. The addressing was accomplished using row and column decoders with master-slave D flip flops. The analog output circuit, containing logarithmic trans-impedance amplifiers, source follower circuits and transistor switches, converted the logarithmic sub-threshold sensor current to a voltage signal, and read out the voltage from the sensor. To demonstrate the feasibility of this approach, the circuits were integrated and fabricated with a 2×2 "pseudo-sensor" array on a chip using CMOS technology. Functional testing of the fabricated design verified that the integrated circuit accessed and read each sensor successfully. The experimental V_{out}-I_{sensor} curves from a single sensor confirmed the expected logarithmic relationship between current and output voltage from the sensor. A cross talk experiment demonstrated that the row and column decoders in the digital circuit efficiently routed digital signals to their respective rows and columns. Given the feasibility of the design has been verified, this type of circuit could be used to realize a truer "electronic nose" where a much large float-gate, FET sensor array could be used.

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Chapter 1 Introduction

1.1 Motivation

The human nose can be used as a sensing tool to assess the quality of products in various industries, which include food, liquor and perfumes. Although it can detect odours of low concentration (less than a few parts of per billion) [1], the assessment results are affected by the variation of health and fatigue from person to person. The application of human olfaction is limited to non-toxic substances as exposure to toxic chemicals can be lethal. For these reasons, chemical analysis techniques have been utilized. For example, gas chromatography separates the components of a mixture and detects odour compounds. However, the equipment used to perform the analysis techniques is often expensive and cumbersome.

One solution to the shortcomings of the human olfaction and these analytical techniques is the "electronic nose" (e-nose). E-nose systems utilize an array of chemical sensors to react to a given odour [2], and convert these reactions to an electronic signal. This signal is then analyzed for odour identification and discrimination. These sensor array systems have been reported to have a wide variety of application areas including food, environmental monitoring and medical diagnostics [3].

The utilization of sensor arrays in the "electronic nose" systems has many advantages over an individual sensor. The sensing system, containing an array of different sensors, can detect different chemical molecules. As such, it increases the selectivity to discriminate chemicals in a mixed-sensing environment. The array can also consist of the same sensors, with each responding to the same chemical molecule. Averaging the outputs of individual sensors avoids random fluctuation in sensor

operation. Thereby, the data is more robust than the output of any single sensor. In order to gain both high selectivity and robustness, the array can be a hybrid architecture that is a combination of homogeneous and heterogeneous sensors.

Among diverse sensor types for the "electronic noses", a field-effect transistor (FET) with a chemically sensitive gate is commonly used as a sensor array element. This type of FET sensor is attractive because it has many advantages. It is compatible with semiconductor fabrication processes and can be made to be small, have low cost and high sensitivity. It may also be integrated with electronic circuits onto a chip. [4]

In this project, a floating-gate, FET is used as an element of the chemical sensor array, as it possesses advantages over other FET-based sensors that include greater programmability and higher sensitivity. This particular sensor has a large extension area attached to the floating gate. To make the device sensitive to a given chemical molecule, a chemically sensitive polymer layer can be deposited on this extension area. When this sensor is exposed to a chemical molecule, the molecule may react with the sensitive polymer film on the extension area. This causes the threshold voltage of the sensor to shift. By comparing the threshold voltage before and after the exposure, this floating-gate, FET sensor can convert the chemical reaction to an electronic signal [5].

The aim of this thesis work is to design and fabricate an integrated circuit to access and read each sensor in a prototype-2×2 array of 4 floating-gate, FETs. This integrated circuit was composed of a digital array-addressing circuit and an analog output circuit. The digital circuit activates individual row and column lines to access and program each sensor in the array. The analog output circuit, used to read the outputs from individual sensors, converts the logarithmic subthreshold sensor current to a voltage

signal. The voltage is then converted to an 8-bit value using an external analog-to-digital (A/D) converter for further analysis. The digital and analog circuits were integrated and fabricated with a 2×2 "pseudo-sensor" array on a chip using CMOS 0.35 μm technology.

1.2 Thesis Structure

In Chapter 2, several types of chemical sensors typically used to construct sensor arrays are introduced. This chapter emphasizes the floating-gate field effect transistor as it was used in the sensor array of this project. The operation mechanism of this sensor is described, and its advantages over other sensors are discussed.

Two operational modes (i.e., programming and sensing) of the sensor array are introduced in Chapter 3. The block diagram of the integrated circuit for implementing both operation modes is described. Each component of the integrated circuit (i.e., a digital array-addressing circuit and an analog output circuit) is discussed.

In Chapter 4, the integrated circuit design for a 2×2 sensor array is described in detail. The digital array-addressing circuit design, including the master-slave D flip-flop design, row and column decoder design, is presented. For the analog output circuit, two design schemes are compared. The implementation of the analog output circuit is also demonstrated.

The schematic simulation of the integrated circuit is presented in Chapter 5. The description of the timing scheme for the digital array-addressing circuit is given. The simulation results of both the digital and the analog circuits are discussed. The simulation results of the pseudo sensor are compared with the test results of the sensor device.

What is discussed in Chapter 6 is the physical layout design of the digital array-addressing circuit and the analog output circuit. The methods for minimizing noise in this

mixed-signal sensor system are discussed. The final chip layout is presented, followed by the discussion of the layout verification.

The experimental measurement apparatus of the fabricated chip is described in Chapter 7. The experiments performed, including the circuit functionality test and A/D conversion for a single sensor and the 2×2 sensor array on the chip, are discussed. The test results are also demonstrated.

In Chapter 8, the thesis work is summarized and conclusions are made. The discussion about future work focuses on a scheme for further sensor signal processing. A method to protect the integrated circuits from the sensing environment is also given.

Chapter 2 Introduction to Chemical Sensors

A chemical sensor is a device that converts chemical information, such as concentration and composition, into an analytical signal. When a chemical sensor is exposed to an analyte (e.g. vapour molecules), it experiences a physical change that alters one or more of its electrical parameters. This change is converted into an electrical signal, which is then processed for identification analysis.

The mechanism responsible for the physical change depends on the type of chemical sensor. For example, in conductivity sensors, a chemical gas changes the resistance of the sensing material. With piezoelectric sensors, gas absorption changes the sensor mass and hence changes the resonant frequency. [3]. In chemically sensitive field effect transistors (ChemFETs), a chemical reaction changes the charge stored on the gate and shifts the sensor's threshold voltage. In this chapter, conductivity sensors and ChemFETs are described since they are compatible with semiconductor fabrication processes, which are used to construct the floating-gate sensor of this work.

2.1 Conductivity Sensors

In conductive sensors, the conductivity is typically proportional to the analyte concentration in the sensing environment [6]. There are three main categories of conductivity sensors; 1) metal oxide, 2) intrinsically conducting polymer, and 3) conducting polymer composite sensors, with each dependent upon the type of material used for the sensing application. In this section, the operation mechanisms and applications of these three sensors are described. Their advantages and disadvantages are also discussed.

2.1.1 Metal Oxide Sensor

A metal oxide sensor is typically composed of a chemically sensitive metal oxide film and a silicon substrate. There are two common types of films: n-type (tin oxide or zinc oxide), which are sensitive to reducing gases (H_2, CH_4, CO and H_2S); or p-type (nickel oxide or cobalt oxide), which respond to oxidizing gases (Cl_2, O_2, NO and NO_2) [2]. When a metal oxide sensor is exposed to an analyte, the analyte reacts with the oxygen in the metal oxide film. The reaction either releases electrons as in an n-type sensor, or removes electrons and produces holes as in a p-type sensor. This variation in the concentration of charge carriers causes a subsequent change in the sensor's conductivity.

It has been reported that metal oxide sensors have fast response time [3]. For example, the response time of some tin oxide sensors has been found to range typically from 5 to 35 seconds with gas concentrations between 0 and 400 parts per million (ppm), and at temperatures between 250°C and 500°C [3]. The tin oxide sensors responded more quickly than the other conductivity sensors which typically have response time of 20 ~200 seconds [3]. Another advantage of these thin (6-1000 nm) metal oxide film sensors is that they can be integrated with measurement circuits, due to their compatibility with standard semiconductor fabrication process. However, it has been reported that these sensors typically operate at high temperatures (200-500°C) in order to achieve an appreciable response to the vapor of interest [6]. This in turn increases the power consumption of the devices and limits their application.

2.1.2 Intrinsically Conducting Polymer Sensor

An intrinsically conducting polymer sensor consists of a substrate (silicon or glass), a pair of interdigitated electrodes, and a conducting organic polymer. Typically, polypyrrol, polyaniline and polythiophene are used as conducting polymers [2]. In this case, the adsorption of an analyte swells the conducting polymer and results in the conductivity variations [5]. These sensors are used to detect gases such as ethanol (CH_3CH_2OH) [7], methane (CH_4), chloroform ($CHCl_3$), and ammonia (NH_3) [2].

Conducting polymer sensors operate at room temperature, thereby simplifying the required system setup [2]. They can also be easily integrated with measurement circuits. However, these sensors typically have a relatively short lifetime, 9-18 months, which often results from the oxidation of the polymer [2].

2.1.3 Conducting Polymer Composite Sensor

A composite sensor contains conducting particles (e.g., carbon black) dispersed in an insulating polymer. Upon exposure to an analyte, the composite polymer swells, causing conductive particles to move further apart from each other [1]. Consequently, the sensor conductivity is decreased. Composite conducting sensors have been employed to identify vapours such as acetone (CH_3COCH_3), chloroform ($CHCl_3$), ethyl acetate ($CH_3COOC_2H_5$), and methanol (CH_3OH) [9].

Like conducting polymer sensors, composite sensors also operate at room temperature. They can be easily integrated with measurement circuits. It has been reported that a sensor array using conducting polymer composites has higher selectivity than both tin oxide and conducting polymer sensor arrays [10].

2.2 Chemically Sensitive Field Effect Transistors

Chemically sensitive field effect transistors (ChemFETs) are another class of chemical sensors. They also can be integrated with measurement circuits onto a chip. Their structure is similar to silicon-based insulated gate field-effect transistors except that the gate typically contains chemically sensitive material.

When the gate material reacts with an analyte, the threshold voltage of ChemFET is shifted. Since the source-drain current of a field effect transistor has an exponential relationship with the threshold voltage in the subthreshold region, a small change in the threshold voltage can induce an exponential change in the current. Therefore, the FET-based sensors (i.e., ChemFETs) may have higher sensitivity than conductivity sensors. Four types of ChemFETs are discussed in the following section: 1) an ion sensitive field effect transistor, 2) an enzymatically sensitive field effect transistor, 3) a work function field effect transistor and 4) a floating gate field effect transistor.

2.2.1 Ion Sensitive Field Effect Transistor

An ion sensitive field effect transistor (ISFET) is a metal oxide semiconductor field effect transistor (MOSFET) in which the normal polysilicon/metal gate is replaced with an ion-conducting liquid solution and a reference electrode. An ion sensitive layer is deposited on the top of the traditional gate oxide (SiO_2) to contact the solution, as illustrated in Figure 2-1. The ISFET threshold voltage is dependent upon the electrode potential and the interfacial potential of the electrolyte /sensitive layer interface [11]. When analytes are present, the ion concentration of the bulk solution is changed. Surface charge is generated along the interface between the electrolyte and ion sensitive layer.

Consequently, the interface potential is altered, which subsequently shifts the threshold voltage of the ISFET.

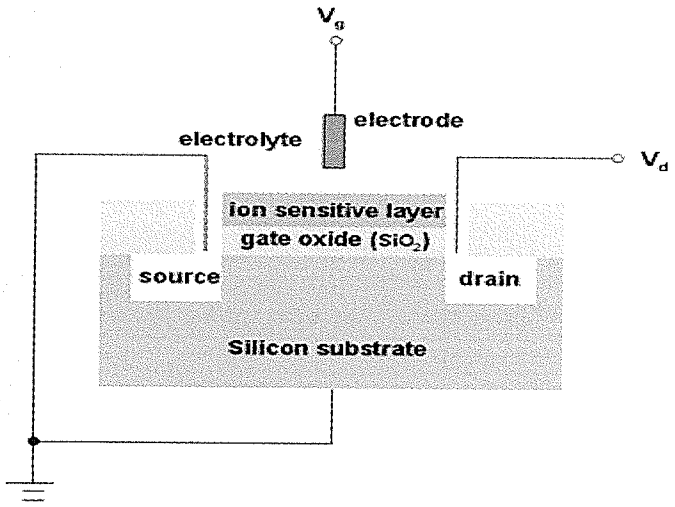


Figure 2-1: General configuration of an ISFET device

One application of ISFETs is its use in clinical assaying. For example, ISFETs have been employed to measure the potassium ion (K^+) concentration variation in human blood during or after surgery [12]. In electro-physiological experiments, an ISFET catheter tip sensor has been developed to detect changes in the pH of the blood of a patient during an operation [11]. Although an ISFET gate may have small dimensions (typically in the μm range), the electrode and electrolyte combination reduces the practical appeal of such devices [6].

2.2.2 Enzymatically Sensitive Field Effect Transistor

Enzymatically-sensitive, field-effect transistors (ENFETs) can be fabricated from an ISFET by applying a chemically sensitive enzyme gel on the ion sensitive layer, as shown in Figure 2-2.

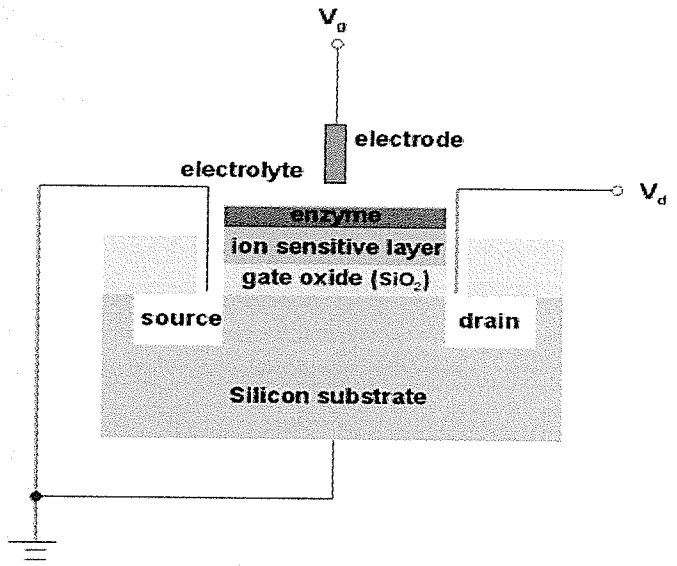


Figure 2-2: General configuration of an ENFET device

The enzyme layer, which acts as a biological catalyst, makes ENFETs able to detect electrically neutral species [13]. Upon exposure to an anlyte, the enzyme on top of an ion sensitive layer catalytically hydrolyzes the analyte. The ion concentration of electrolyte is thereby changed. The ion sensitive layer then responses to the variation in ion concentration and induce a surface charge [14]. As a result, the surface potential is changed and the threshold voltage of the device is shifted.

Enzymatically sensitive field effect transistors can be used as biosensors to measure the concentration of different substances. It has been reported that an ENFET was developed to measure urea in rat blood [14].

2.2.3 Work Function Field Effect Transistor

A ChemFET may also measure electrically neutral species, and is referred to as a work function field effect transistor (WF-FET) [13]. It has a MOSFET structure with a chemically sensitive, conducting gate layer. The gate material can be either a metal

(typically palladium) or a conductive polymer (typically polyaniline). The general structure of a WF-FET is shown in Figure 2-3.

When the sensor is exposed to a particular analyte, the gas molecules are adsorbed at the gate metal/SiO_2 interface, forming an electric dipole with an associated electric field. This changes the gate work function, causing a shift in the threshold voltage of the sensor [15].

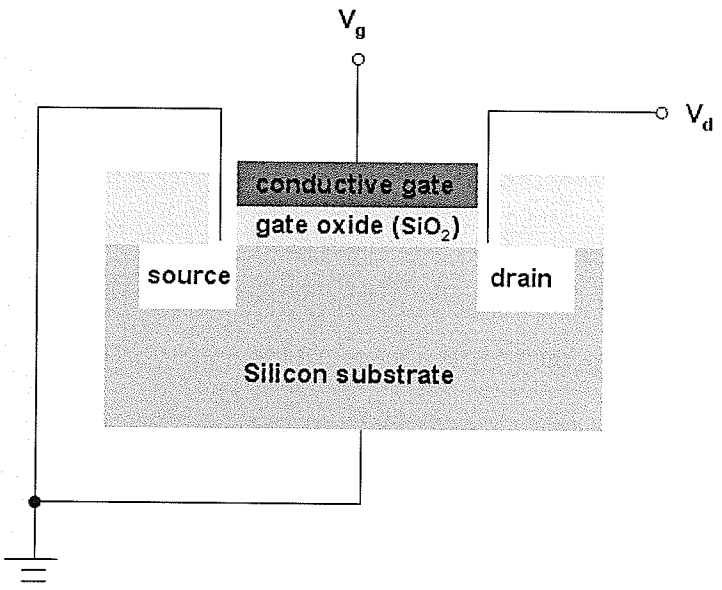


Figure 2-3: General configuration of a WF-FET device

The main advantage of WF-FETs is that they do not require a reference electrode. The silicon substrate, which is sealed by silicon dioxide (SiO_2), can serves as a stable, internal reference electrode. Therefore, these devices are ideally suitable for miniaturization and construction of silicon based sensor arrays [13].

2.2.4 Floating Gate Field Effect Transistor

The floating gate field effect transistor (FG-FET) is like a traditional MOSFET, except that it has two separate gates: a control gate and a floating gate. The gates are isolated by an insulating layer (e.g., SiO_2), as shown in Figure 2-4. The floating gate is attached with a large extension area (to be shown in chapter 3). This extension area was designed to make the device sensitive to a given analyte by depositing a chemically sensitive polymer layer on it. Since a larger floating gate extension produces a larger area of reactive polymer, this extension area was significant larger than the gate area of the transistor [5].

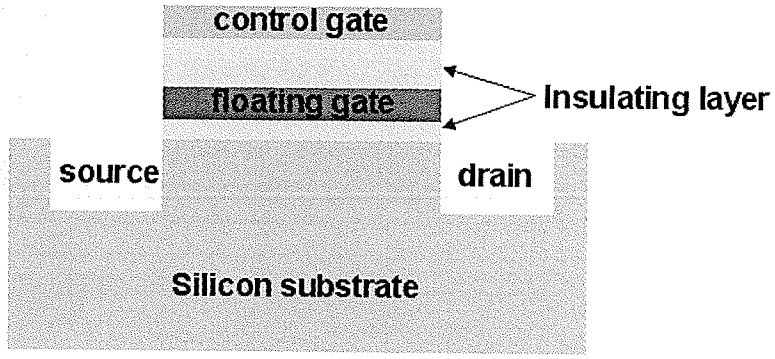


Figure 2-4: A cross-section of a floating gate FET. The floating gate can be attached with the extension area, onto which a chemically sensitive polymer is deposited.

During the sensing operation, no external voltage is directly applied to the floating gate. When a voltage is applied to the control gate, it is capacitively coupled to the floating gate. The analyte may react with the chemically sensitive film on the extension area, which results in a charge variation on the floating gate and causes the

threshold voltage shift. By comparing the threshold voltages before and after the sensor is exposed to the analyte, the FG-FET can convert the chemical reaction to an electrical signal.

There are three main advantages of the FG-FET over other types of chemical sensors. First of all, the sensor with a floating gate structure can be programmable. This is realized by applying a bias to the floating gate to deposit a chemically sensitive polymer layer onto the extension area. Different polymers can be used to sense different analytes. Therefore, a sensor array can be easily designed to detect various analytes in a given mixture by depositing different polymers in each sensor floating gate. Secondly, this sensor can possess higher sensitivity since it has a larger sensing extension area attached to the floating gate. All charge variations directly affect the shift of the threshold voltage. Thirdly, it can be fabricated by a standard CMOS fabrication process, as this device is essentially a metal oxide semiconductor field effect transistor. For these reasons, the floating gate structure was selected for the sensor design in this project.

Chapter 3 System Description

The integrated sensor system (see Figure 3.1) consists of an m×n array of sensing devices, digital array-addressing circuit and analog output circuit. The sensors in the array are individually addressed by digital signals through the array-addressing circuit. Two separate voltage signals (i.e., sensor program and sensor control) are applied to the addressed senor for the two different modes of operation: programming mode and sensing mode. The analog output circuit reads the output voltage from the sensor array, which is then further processed to obtain the analysis of the olfactory molecules. The design is based on the CMOS 0.35μm technology since it was the only available technology with CMC Microsystems that provided two polysilicon layers which were required to produce two gates for the sensing device (i.e., floating-gate FET).

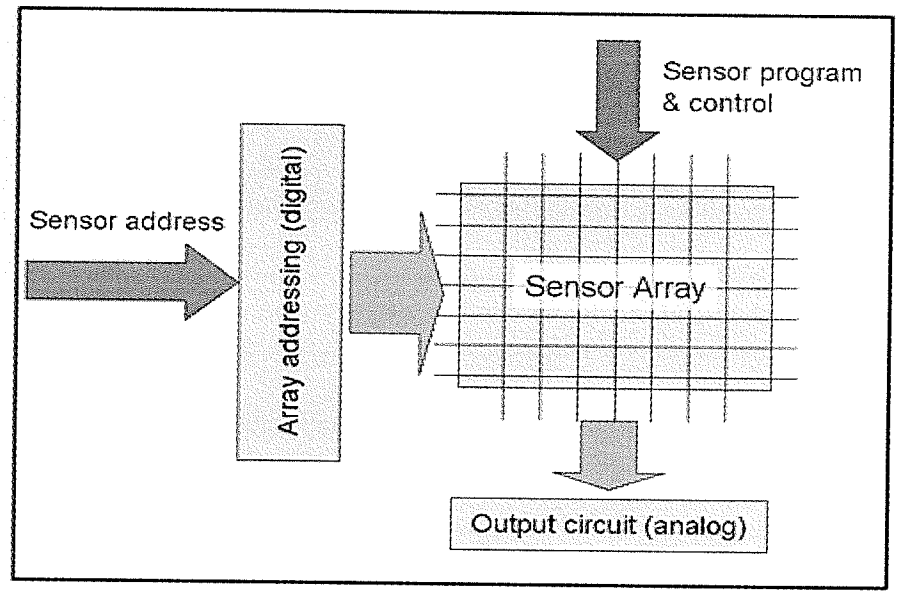


Figure 3-1: Block diagram of the integrated sensor system

3.1 Sensor Array

An array of sensing devices is integrated onto a chip, which leads to advantages over an individual sensor. For example, the performance of an array which contains the same type of sensors working under identical conditions is more robust than that of any of the individual sensor. However, an array which is made up of different types of sensors has the ability to detect a complex mixture of molecules. Therefore, the selectivity of the sensing system is improved. Furthermore, an array can also be implemented in a hybrid architecture that is a combination of homogeneous and heterogeneous sensors to gain both high selectivity and robustness.

The sensing devices in the sensor array in this work are implemented using floating-gate field-effect transistors. The transistor structure is easily fabricated using a standard CMOS process. It has five terminals: floating (programming) gate, control gate, drain, source and substrate, as shown in Figure 3-2 [5]. In order to make the device sensitive to a given olfactory molecule, the extension area must be coated with a chemically sensitive polymer layer. This leads to two separate and distinct modes of operation for the sensor: programming mode and control mode.

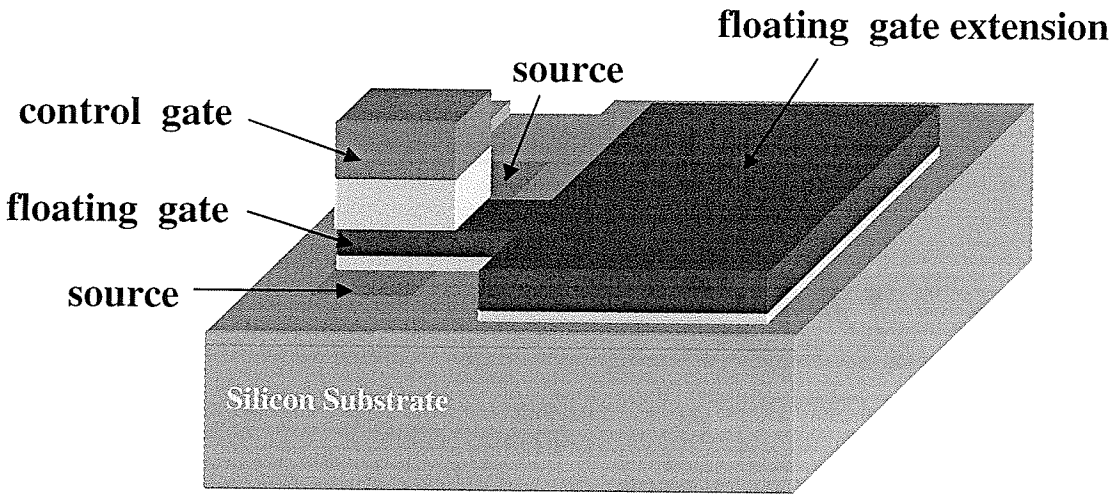


Figure 3-2: One version of the sensor design with a floating-gate FET structure [5].

In the programming mode, a voltage is applied to the floating (programming) gate to allow the electrochemical deposition of a given polymer layer onto the extension area. This particular polymer is chosen to be sensitive to a certain individual or groups of olfactory molecules. Once the floating gate has been programmed or "sensitized", a voltage is applied to the control gate of the sensor during the sensing operation.

In the sensing mode, chemicals in the environment react with the floating gate which causes the shift of the threshold voltage of the transistor. The sensor device is biased in subthreshold regime where the source-drain current (I_{ds}) is exponentially dependent upon the threshold voltage. Therefore a small change in the threshold voltage results in an exponential change of the current (I_{ds}). The exponential dependence of I_{ds} provides the floating-gate sensors with a very high sensitivity.

3.2 Integrated Circuit

In order to access, program and read the sensor array, the integrated circuit was designed and integrated with the sensor array onto a chip. It consists of digital array-addressing and analog output circuits, as shown in Figure 3-3.

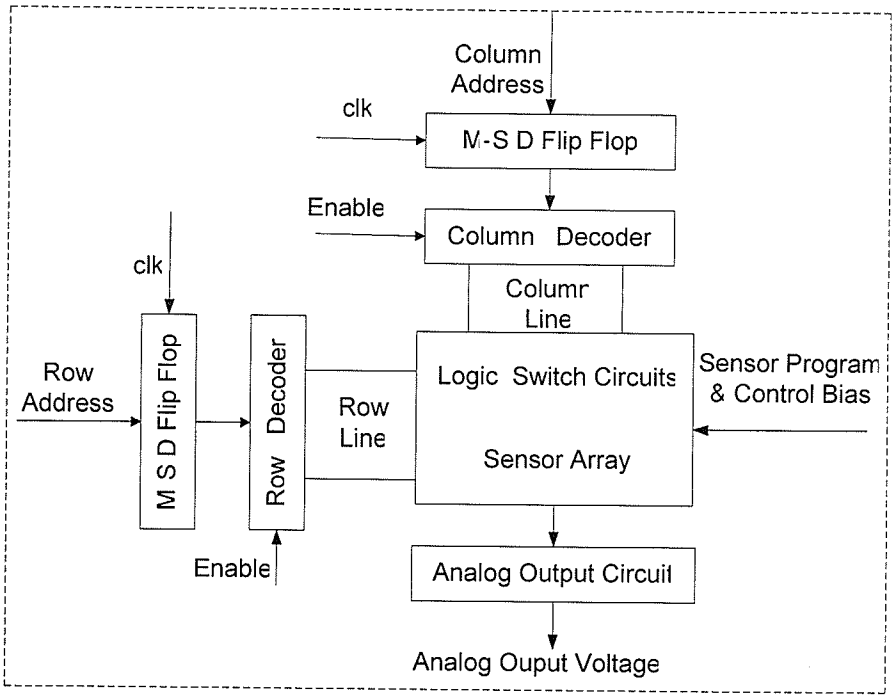


Figure 3-3: Block diagram of the integrated circuit in the sensor system

The digital array-addressing circuit is composed of row and column decoders, master-slave D flip flops, and logic switch circuits. The master-slave D flip flops are required to realize the synchronous operation of the overall system. Row and column decoders activate individual row or column lines in order to access an individual sensor. There are four digital input signals associated with the array-addressing circuit: row and column address signals, a clock signal (clk) for the operation of both master-slave D flip

flops, and an Enable signal for enabling the operation of both the Row and the Column decoder.

The logic switch circuit connects the programming gate of the sensor to the voltage supply V_{pg}, as illustrated in Figure 3-4. The switch comprises two n-type transistors in series, with each gate connected to the row line (Row_m) and the column line (Col_n) respectively.

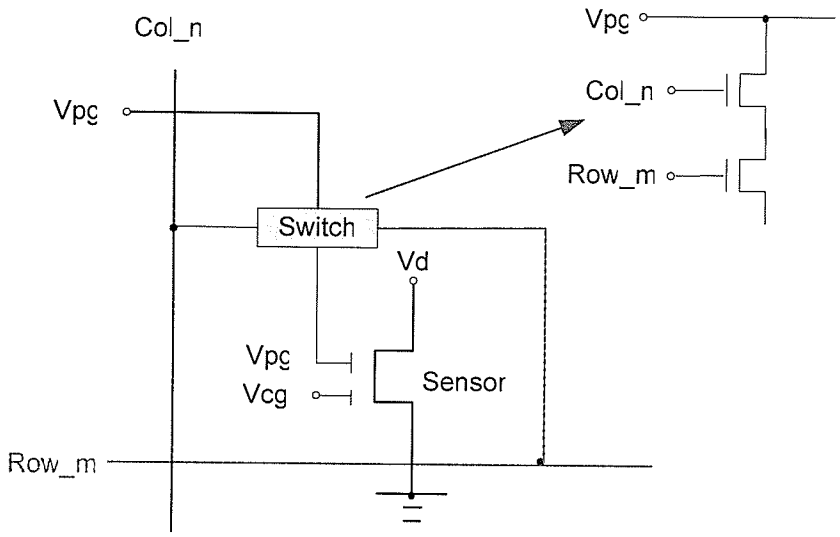


Figure 3-4: Implementation of the programming mode

When both the row line and the column line are active, the switch is closed. The voltage bias V_{pg} is applied to the programming gate of the sensor, which allows electrochemical deposition of the chemically sensitive polymer layer. The timing scheme for activating the row and column lines can be designed to ensure that only one sensor is addressed at a time.

The analog output circuit is made up of logarithmic trans-impedance amplifiers, source follower circuits and transistor switches. During the sensing operation, a voltage is applied to the control gate of the sensor, causing a sensor current to flow through the

logarithmic trans-impedance amplifier. The output of this amplifier is the voltage which is linearly proportional to logarithm of the sensor current. The digital address signals activate the row and column line, selectively closing the corresponding transistor switches. Finally, the source follower circuits and transistor switches connect a particular sensor voltage to the output bus for the further analysis of the olfactory molecules.

Chapter 4 Integrated Circuit Design

The integrated circuit was designed to access and read each sensor (a floating-gate FET structure) in the array. However, difficulties and time issues occurred while exposing the floating gate extension area, making a real sensor impractical. In order to still demonstrate the "circuit" feasibility, a pseudo-sensor was used. This pseudo-sensor (a standard n-type MOSFET with a 5μm /0.8μm W/L ratio) was implemented into the current design to emulate the electrical characterization of the sensor device.

In this chapter, the design of the digital array-addressing circuit and analog output circuit is described. An electronic design environment (Cadence) was utilized in the design. It was provided by CMC Microsystems. From the many CMOS technologies available, the CMOS 0.35 μm technology was selected in order to ensure the overall system compatibility as mentioned previously. This 0.35 μm-CMOS process was provided by Taiwan Semiconductor Microelectronic Company (TSMC).

4.1 Digital Array-Addressing Circuit Design

To demonstrate the feasibility of the design, a 2×2 array of 4 sensors was used in the current system. The block diagram of the digital array-addressing circuit is shown in Figure 4-1.

Activating one of the 2 row lines is performed by a row decoder that has a 1-bit address input signal. A column decoder with a 1-bit address input activates one of the 2 column lines. When both a row line and a column line are activated, one given sensor is selected. As shown in Figure 4-1, the signals $\boldsymbol{A}$ and $\boldsymbol{B}$ are the 1-bit address signals for the row and column decoders respectively.

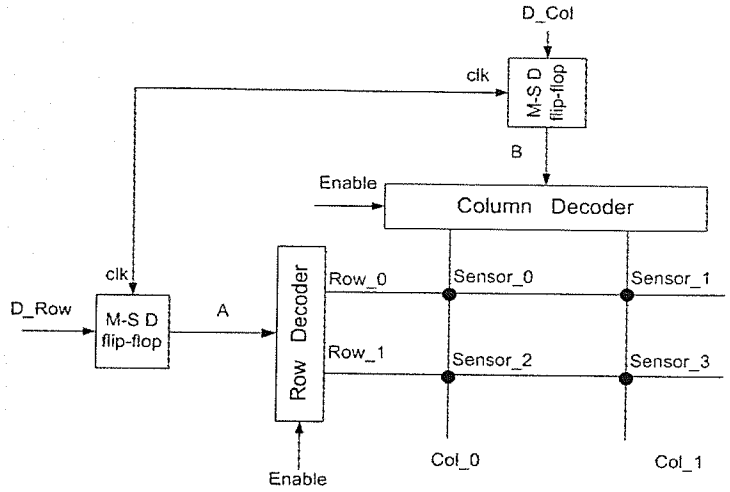


Figure 4-1: The block diagram of the digital array-addressing circuit

The master-slave D flip flops act as buffers for the row and column decoders to realize the synchronous operation of the system. Each flip flop has two inputs; an address signal and a clock signal. As shown in Figure 4-1, the signal ***D_Row*** is the input of the flip flop on the row side. The signal ***D_Col*** is the input of the flip flop on the column side. The outputs of the both flip flops (***A*** and ***B***) are synchronized to the common clock signal (***clk***). They are also the address input signals of the row and column decoders respectively.

4.1.1 Master-Slave D Flip Flop Design

A master-slave D flip flop is either rising or falling edge triggered. Designers can choose either, subject to their own personal preference. In this project, the master-slave D flip flop was designed to be falling edge triggered. The CMOS implementation of the circuit is shown in Figure 4-2. Each stage is composed of one latch and two CMOS transmission gates (TG).

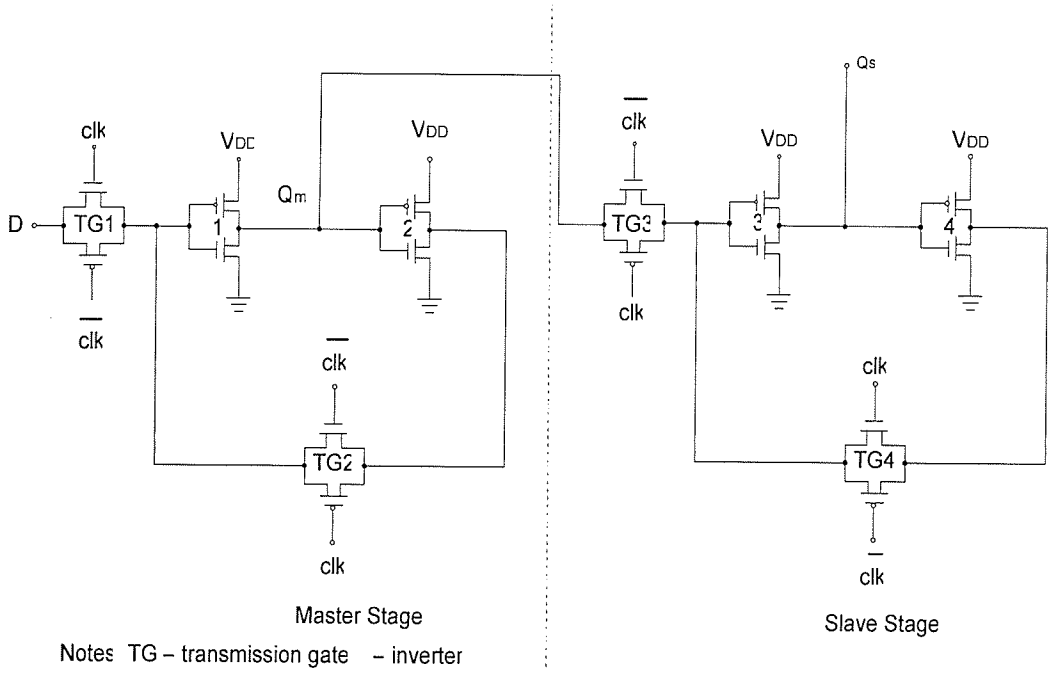


Figure 4-2: Implementation of the Master-Slave D Flip Flop Circuit

The master-slave D flip flop samples the input only on the negative edge of the clock pulse. When the clock is high (***clk***=1), TG1 is on and TG2 is off. The input ***D*** is sampled and inverted. The inverted signal, $\overline{D}$, is passed onto the node Q_m. During this period, TG3 is off and TG4 is on. The slave stage latches the previous value. When the clock changes from high to low, the master stage stops sampling the input and latches the output. At this point, TG1 is off and TG2 is on. The inverter loop in the master stage then latches the value on the node Q_m ($\overline{D}$). The transmission gate TG3 is on while TG4 is off. The slave stage accepts the output of the master value $\overline{D}$ at Q_m and inverts it at the output of the slave stage Q_s. The input is now isolated from the output as the master stage is separated from the ***D*** input. When the clock changes positively from low to high, the slave stage latches the data ***D*** and the master stage starts sampling the input again [16].

According to the specifications of CMOS 0.35μm technology, a 3.3V voltage supply was used for the circuit. The design parameters for the transistors size are shown in Table 4-1. The *W/L* ratio of the p-type and n-type transistors was selected to achieve matching devices with a symmetric voltage transfer characteristics.

Table 4-1: Design parameters for the Master-Slave D Flip Flop circuit

TRANSISTORS	WIDTH/LENGTH (um/um)
n-type	1/0.5
p-type	3.6/0.5

4.1.2 Row and Column Decoders Design

In this project, the decoders provide digital signals to activate the row and column lines and selectively close the corresponding transistor switches. Consequently, the sensor associated with the transistor switch is accessed. The voltage across the addressed sensor is then passed to the analog output circuit.

The row lines are connected to n-type MOSFET switches [18], which are turned on when the row line supplies a high voltage ("1"). Conversely, the column lines are connected to p-type MOSFET switches [18], which are turned on when the column line supplies a low voltage ("0").

The row decoder has two inputs; an address signal ***A*** and an ***Enable*** signal. It also has two outputs; ***Row_0*** and ***Row_1***, as shown in Figure 4-3. The truth table for the row decoder is in Table 4-2.

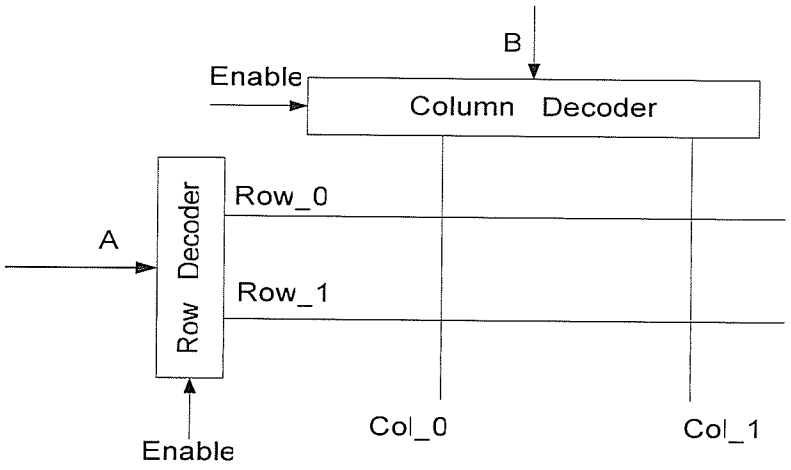


Figure 4-3: Block diagram of the row and column decoders

Table 4-2: Truth table of the row decoder

Row Decoder Inputs		**Row Decoder Outputs**	
E (Enable)	*A*	*Row_1*	*Row_0*
0	X (don't care)	0	0
1	0	0	1 (activated)
1	1	1 (activated)	0

The outputs ***Row_1*** and ***Row_0*** can be expressed as Boolean function of the inputs $\boldsymbol{E}$ and $\boldsymbol{A}$ such that

$$\boldsymbol{Row\_1} = EA = \overline{\overline{EA}}, \tag{4.1}$$

$$\text{and } \boldsymbol{Row\_0} = E\overline{A} = \overline{\overline{E\overline{A}}}. \tag{4.2}$$

The row decoder, based on the equations 4.1 and 4.2, can be implemented with two NAND gates and three inverters, as illustrated in the Figure 4-4.

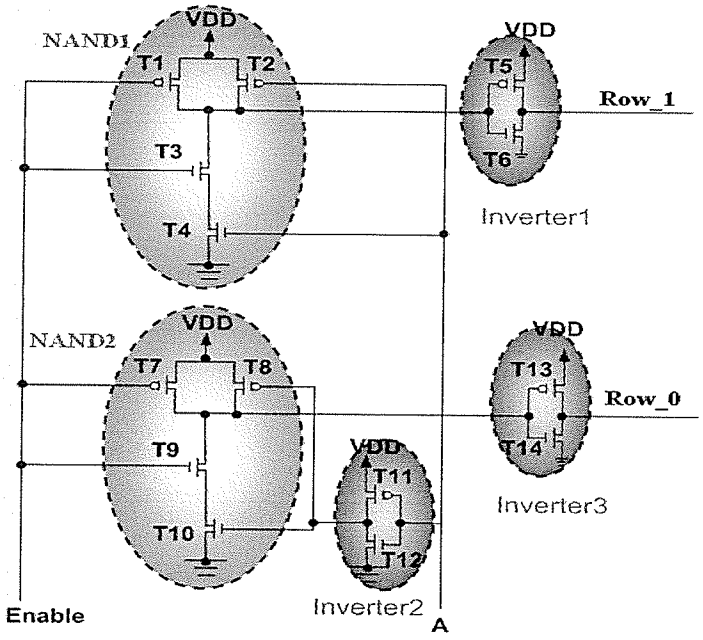


Figure 4-4: CMOS implementation of the row decoder

The NAND gate was implemented using two n-type transistors connected in series and two p-type transistors in parallel. In the design, the *W/L* ratio of each n-type transistor in the NAND gates is twice as large as that of n-type transistor in the inverter. However, the *W/L* ratio of each p-type transistor in the NAND gates and inverter is equal. This ensures that a NAND gate has a capacitor charge/discharge current at least equal to that of an inverter at the output [17]. The values of the design parameters for all transistors in the row decoder are shown in Table 4-3.

Table 4-3: Transistor sizes for the row decoder

Transistors	W/L (um/um)	Transistors	W/L (um/um)
T1	3.6/0.5	T8	3.6/0.5
T2	3.6/0.5	T9	2/0.5
T3	2/0.5	T10	2/0.5
T4	2/0.5	T11	3.6/0.5
T5	3.6/0.5	T12	1/0.5
T6	1/0.5	T13	3.6/0.5
T7	3.6/0.5	T14	1/0.5

Like the row decoder, the column decoder also has two inputs; an address signal ***B*** and an ***Enable*** signal, and two outputs; ***Col_0*** and ***Col_1***. This is shown schematically in Figure 4-3. The truth table for the column decoder is in Table 4-4.

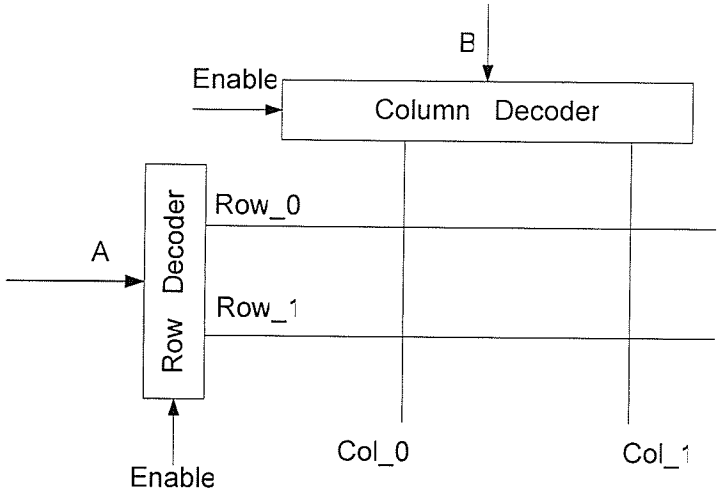


Figure 4-3: Block diagram of the row and column decoders

The outputs ***Col_1*** and ***Col_0*** can also be expressed as Boolean function of E and B, where

$$\boldsymbol{Col\_1} = \overline{EB}, \tag{4.3}$$

$$\text{and } \boldsymbol{Col\_0} = \overline{E\overline{B}}. \tag{4.4}$$

Table 4-4: Truth table of the column decoder

Column Decoder Inputs		**Column Decoder Outputs**	
E (Enable)	*B*	*Col_1*	*Col_0*
0	X (don't care)	1	1
1	0	1	0 (activated)
1	1	0 (activated)	1

As with the row decoder, the column decoder can also be implemented using two NAND gates and an inverter, as illustrated in Figure 4-5.

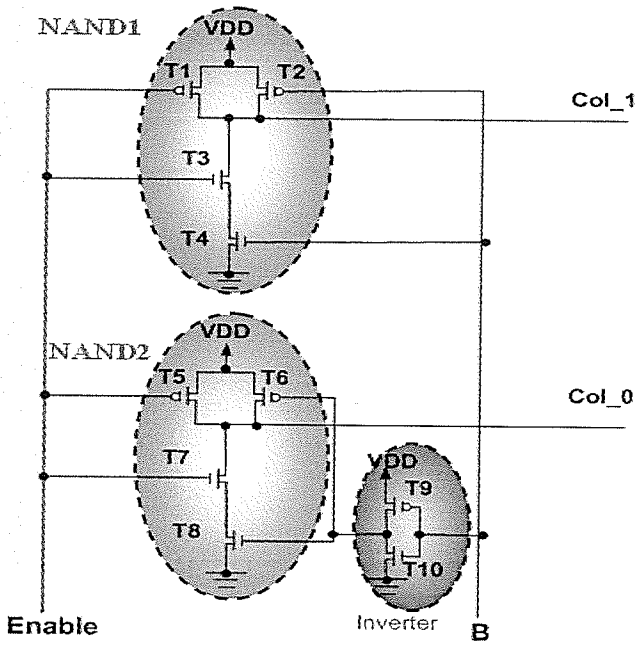


Figure 4-5: CMOS implementation of the column decoder

The values of the design parameters for all transistors in the column decoder are shown in Table 4-5. The selection of the *W/L* ratios of the transistors follows the same rules as mentioned in the row decoder design.

Table 4-5: Transistor sizes for the column decoder

Transistors	W/L *(um/um)*	Transistors	W/L *(um/um)*
T1	3.6/0.5	T6	3.6/0.5
T2	3.6/0.5	T7	2/0.5
T3	2/0.5	T8	2/0.5
T4	2/0.5	T9	3.6/0.5
T5	3.6/0.5	T10	1/0.5

4.2 Analog Output Circuit Design

During the normal sensing operation, a bias would be applied to the control gate of the sensor. When both the row line and column line are activated, the output voltage

across a single sensor is read through the analog output circuit. In this section, two design schemes of the analog output circuit are presented, followed by its implementation.

4.2.1 Design Schemes of the Analog Output Circuit

One design scheme is illustrated in Figure 4-6. A buffer and a current source make up a source follower circuit to amplify the output voltage dropped across the sensor (V_{sensor}). A transistor switch was used to connect each sensor to the output bus. The on/off state of each switch was controlled by both the row and column signals. When both a row line and a column line are activated, the corresponding switch turns on. The source follower circuit and transistor switch then connect the particular sensor voltage to the output bus for the further analysis.

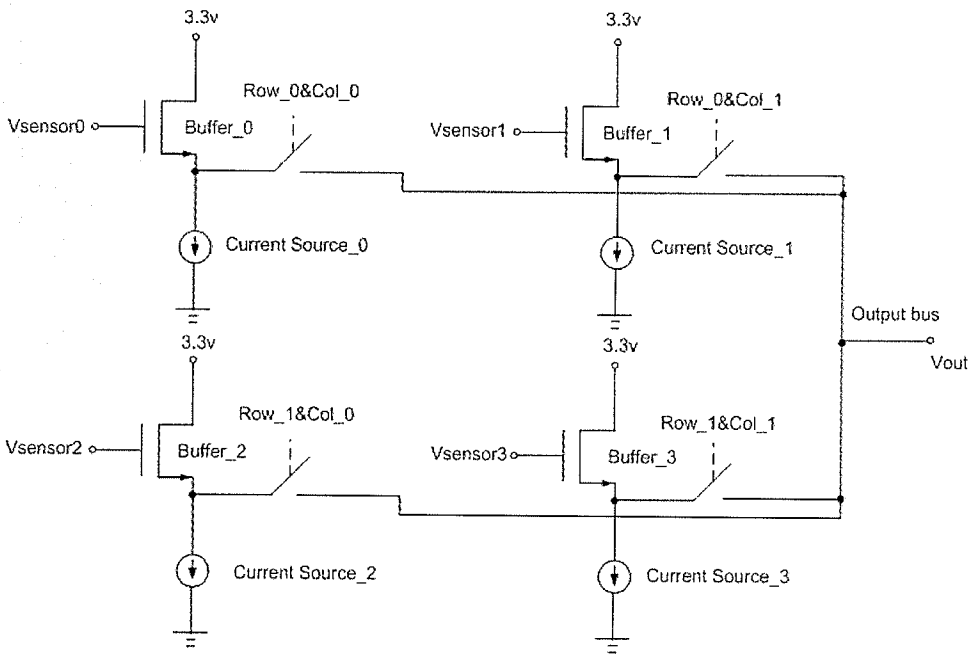


Figure 4-6: The first design scheme of analog output circuit

In this design scheme, each sensor requires a current source. For example, an m×n sensor array system requires a total of m×n current sources, where m and n are the

number of the row lines and column lines respectively. With the number of the sensors increasing, power dissipation in the circuit can be an issue.

A second improved design scheme is shown in Figure 4-7. There are a total of 6 transistor switches in the 2×2 sensor system. The open/close operation of the switches (S_0 ~ S_3) is controlled by the row signals. When a row line is activated, the corresponding switches turn on. For example, the switches (S_0 and S_1) turn on when signal ***Row_0*** is active. The buffers (Buffer_0 and Buffer_1), switches (S_0 and S_1) and the current sources (Source_1 and Source_2) then form source follower circuits. The sensor voltages ($V_{sensor0}$ and $V_{sensor1}$) are connected to the inputs of the column output buses.

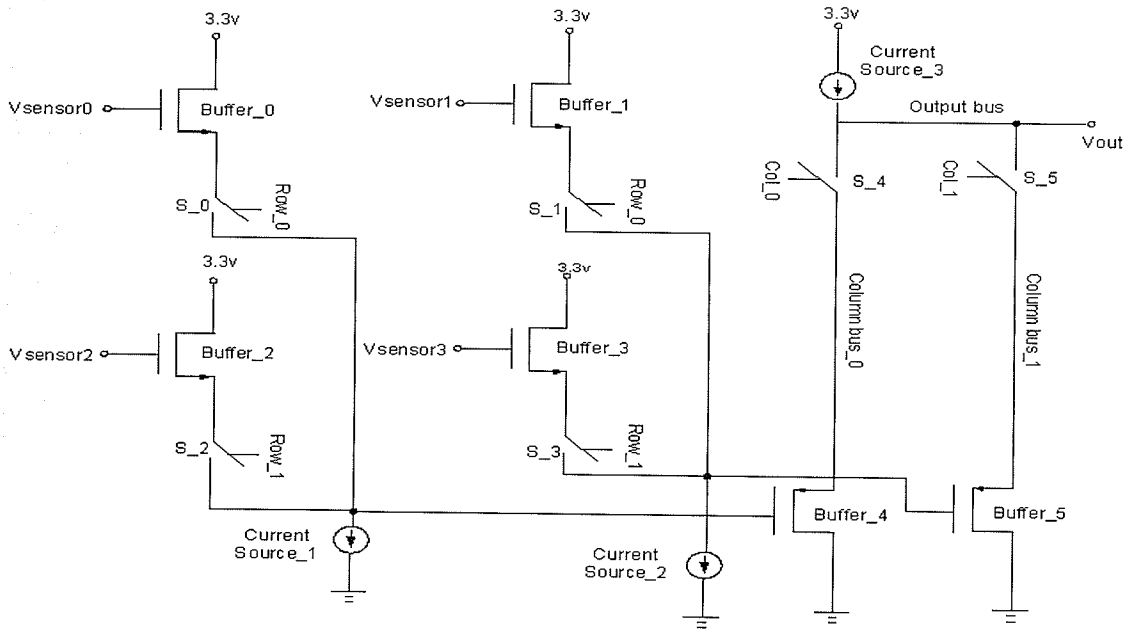


Figure 4-7: A second improved design scheme of analog output circuit

There are another 2 switches (S_4 and S_5) in the two column buses. The open/close operation of these two switches is controlled by the column signals. When a

column line is activated, the corresponding switch turns on. For example, the switch S_4 turns on as signal ***Col_0*** is active. The switch S_4, Buffer_4 and Current Source_3 then form a source follower circuit, which connects the Column bus_0 output to the output bus. [18] Consequently, the voltage signal across the Sensor_0 ($V_{sensor0}$) is read out from the array for the further analysis.

In this scheme, there is only one current source for all the sensors located on the same column line, and only one current source for the output bus. Consequently, an m×n sensor array system only requires a total of n+1 current sources, where m and n are the number of the row lines and column lines respectively. As the number of the sensors increases, the circuit dissipates much less power than that in the first scheme. For this reason, the second design scheme was selected.

4.2.2 Implementation of The Analog Output Circuit

The analog output circuit is made up of logarithmic trans-impedance amplifiers, source follower circuits and transistor switches. The implementation of one sensor-reading circuit is illustrated in Figure 4-8.

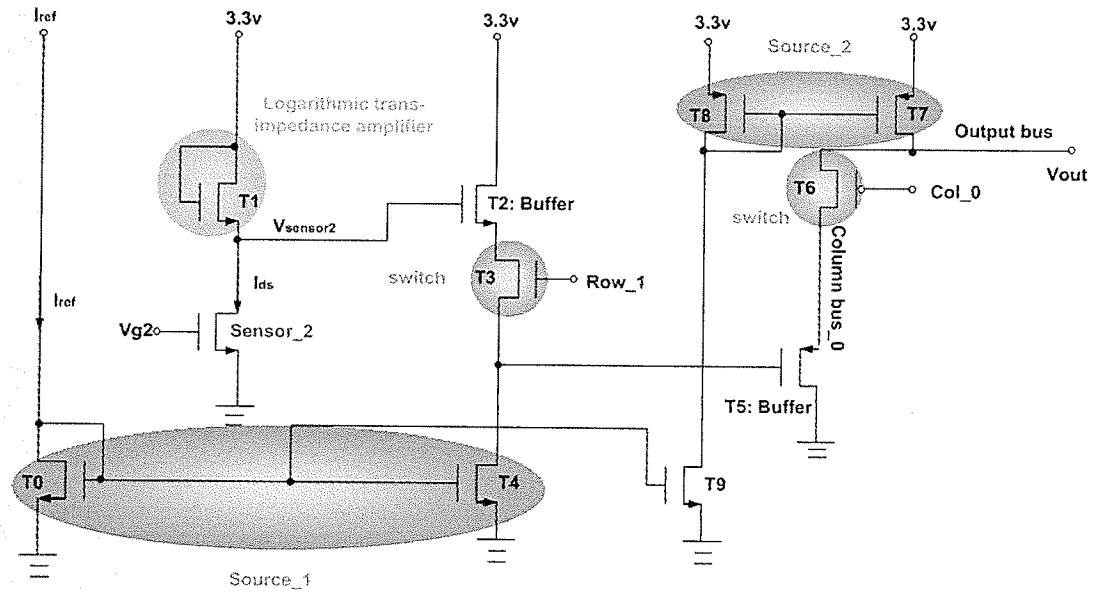


Figure 4-8: CMOS implementation for reading out one sensor [18]

The pseudo-sensor (Sensor_2) is located on the intersection of row1 and column0, as shown in Figure 4-1. Transistor T1 is the logarithmic trans-impedance amplifier, which is connected in series with Sensor_2. The sensor current (I_{ds}) flows through transistor T1. When transistor T1 runs in weak inversion, it produces a logarithmic function between current (I_{ds}) and the voltage across Sensor_2 ($V_{sensor2}$). Transistor T3 and T6 are the switches, whose open/close operations are controlled by the signal Row_1 and Col_0 respectively. The current mirrors T0 and T4 make up the Source_1 while T7 and T8 make up the Source_2. An external constant DC current (called a reference current I_{ref}) was replicated at Source_1 and Source_2 to bias the circuit.

During the sensing operation, a voltage (V_{g2}) is applied to the gate of Sensor_2. This causes a sensor current (I_{ds}) to flow through the logarithmic trans-impedance amplifier (T1). The output of the logarithmic trans-impedance amplifier is the voltage

($V_{sensor2}$), which is linearly proportional to logarithm of the sensor current (I_{ds}). When the digital address signals (***Row_1*** and ***Col_0***) are activated, transistor switches T3 and T6 turn on. The buffer (T2), switch (T3), and current source (Source_1) then form an nMOS source follower circuit. The voltage dropped across the Sensor_2 ($V_{sensor2}$) is connected to the gate of the buffer (T5). At that time, the buffer (T5), switch (T6) and current source (Source_2) form a pMOS source follower circuit. It connects the Column bus_0 output to the output bus. Therefore, the voltage across the Sensor_2 ($V_{sensor2}$) is read out from the array for the further analysis.

The parameters for the transistor sizes in Figure 4-8 are shown in Table 4-6. The result of the circuit simulation showed the feasibility of these parameter values.

Table 4-6: Transistor sizes in Figure 4-8

Transistors	**W/L *(um/um)***	**Transistors**	**W/L *(um/um)***
T0	10/1	T1	180/0.5
T2	180/0.5	T3	78/0.5
T4	10/1	T5	180/0.5
T6	78/0.5	T7	10/1
T8	10/1	T9	10/1

The approach to reading other sensors in the system follows the same scheme as described above. Figure 4-9 shows the implementation of the analog output circuit for a 2×2 sensor array. It can be seen that different row and column signals are used to open or close the transistor switches associated with the different sensor. For example, when both the digital signals ***Row_0*** and ***Col_0*** are active, the corresponding switches turn on. The voltage across the Sensor_0 is then read through the analog output circuit. As with the same scheme, the signals ***Row_0*** and ***Col_1*** are used for reading the Sensor_1. In

order to read the Sensor_3, the signals ***Row_1*** and ***Col_1*** are used. As such, each sensor may be individually addressed.

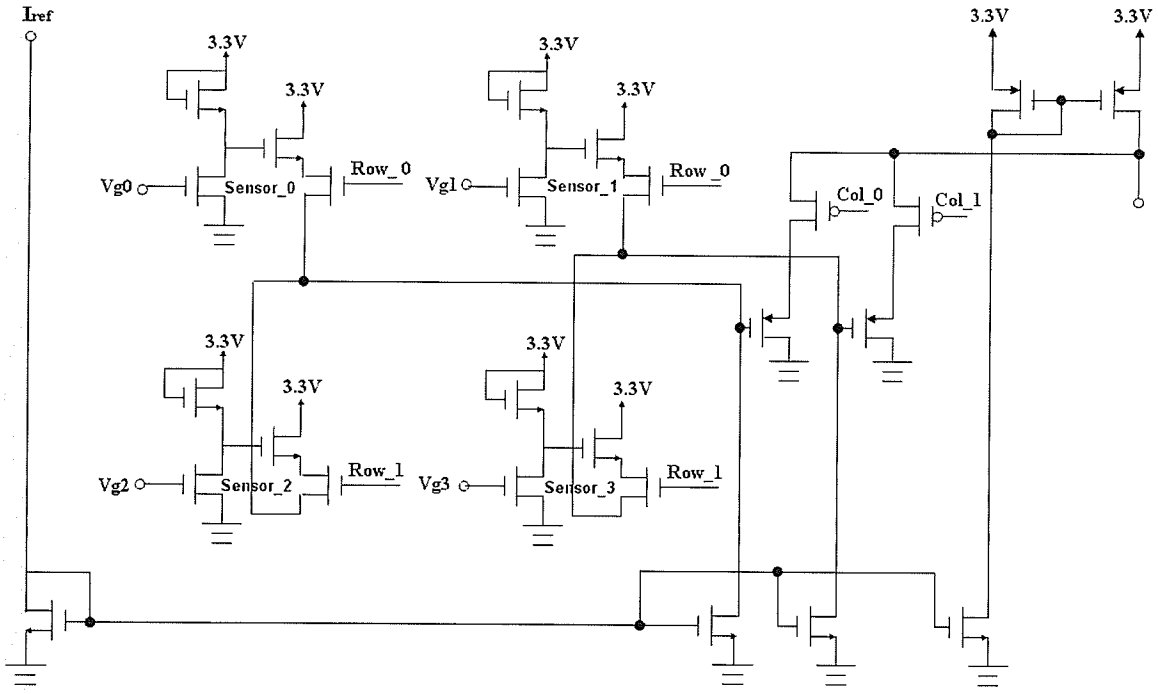


Figure 4-9: CMOS implementation of the analog output circuit for a 2×2 sensor array

Chapter 5 Schematic Simulation

After the schematic transistor–level description of the integrated circuit was completed, it was simulated using the integrated circuit simulator (*Spectre*). In this chapter, the timing scheme for the digital array-addressing circuit is described. The results of simulation for five circuits, i.e., Master-Slave D Flip Flop, Decoders, Pseudo sensor, Logarithmic amplifier circuit and the analog output circuit, are presented.

5.1 Timing Scheme for the Digital Array-Addressing Circuit

The addressing operation is performed by activating the row and column lines. When both the row and column lines are activated, one given sensor is selected and read. As shown in Figure 5-1, sensors in an m×n array are accessed starting from Row_0 through Row_m-1. In each row, sensors are read from Col_0 first then sequentially to Col_n-1. For this reason, the frequency of the column line signal is n times faster than the frequency of the row line signal.

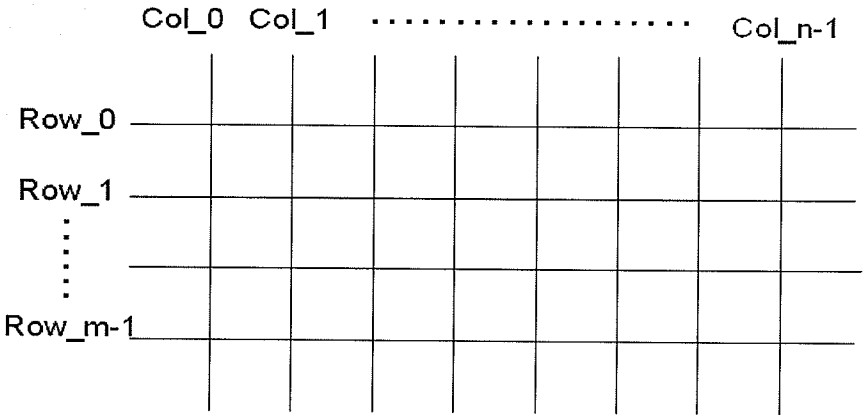


Figure 5-1: An m×n array with m rows and n columns

In the current 2×2 sensor system shown in Figure 5-2, there are two lines for both the row and column, i.e., m=n=2. The truth table of the row and column decoders is illustrated in Table 5-1.

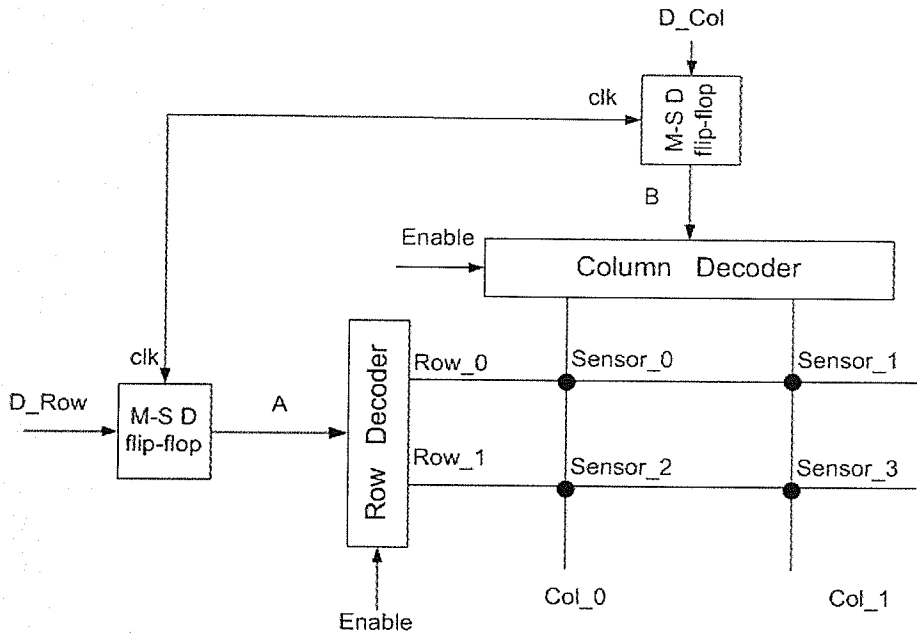


Figure 5-2: The block diagram of the digital array-addressing circuit

Table 5-1: Truth table of the row and column decoders

Input Address Signals		Output Signals				Sensor Selected
A (Row)	*B (Column)*	*Row_1*	*Row_0*	*Col_1*	*Col_0*	
0	0		Activated		Activated	Sensor_0
0	1		Activated	Activated		Sensor_1
1	0	Activated			Activated	Sensor_2
1	1	Activated		Activated		Sensor_3

As seen from the above truth table, the frequency of the input column address signal ***B*** is twice (n=2) as fast as the frequency of the row address signal ***A***. The output row and column line signals follow the same timing scheme, i.e., $f_{Col} = n \times f_{Row}$, where n is the number of the column lines.

As shown in Figure 5-1, the address signal is generated from the master-slave D flip flop, which does not change the frequency of the input. Therefore, the input signals ***D_Row*** and ***D_Col*** have the same frequency relationship as the outputs ***A*** and ***B***, i.e.,

$$f_{D\_Row} = f_A, f_{D\_Col} = f_B, \tag{5.1}$$

$$f_{D\_Col} = n \times f_{D\_Row}, \text{ where } n=2. \tag{5.2}$$

In the operation of the master-slave D flip flop, the state change of the output only occurs on the negative edge of the clock. Therefore, the period of the output signal ***B*** is twice than the period of the clock, i.e., $T_B = 2T_{clk}$, $f_B = f_{clk}/2$. According to the equation (5.1) and (5.2), the timing scheme for the input signals ***D_Col*** and ***D_Row*** is as follows.

$$f_{D\_Col} = \frac{1}{2} f_{clk}, \tag{5.3}$$

$$f_{D\_Row} = \frac{1}{n} f_{D\_Col} = \frac{1}{4} f_{clk}, \text{ where } n=2. \tag{5.4}$$

Since the response time of chemical sensors is not fast, typically from milliseconds up to minutes [2], a clock signal with the frequency of 200 kHz is sufficient to operate the system. A 200 kHz clock was used in the following simulations.

5.2 Master-Slave D Flip Flop Simulation

The simulated input and output waveforms of the master-slave D flip flop on the row decoder side are shown in Figure 5-3. The clock signal ***clk*** ran at the frequency of 200 kHz, while the input address signal ***D_Row*** operated at 50 kHz. In order to avoid the occurrence of an erroneous output, the input signal ***D_Row*** was kept stable for a short time before the negative clock transition. This was done to ensure that the input data had time to propagate from the master stage to the output of the slave stage. If the input signal were to switch immediately, i.e., prior to the clock transition occurs (set-up time

violation), the master stage would fail to latch the correct value, and the slave stage would produce an incorrect output [16].

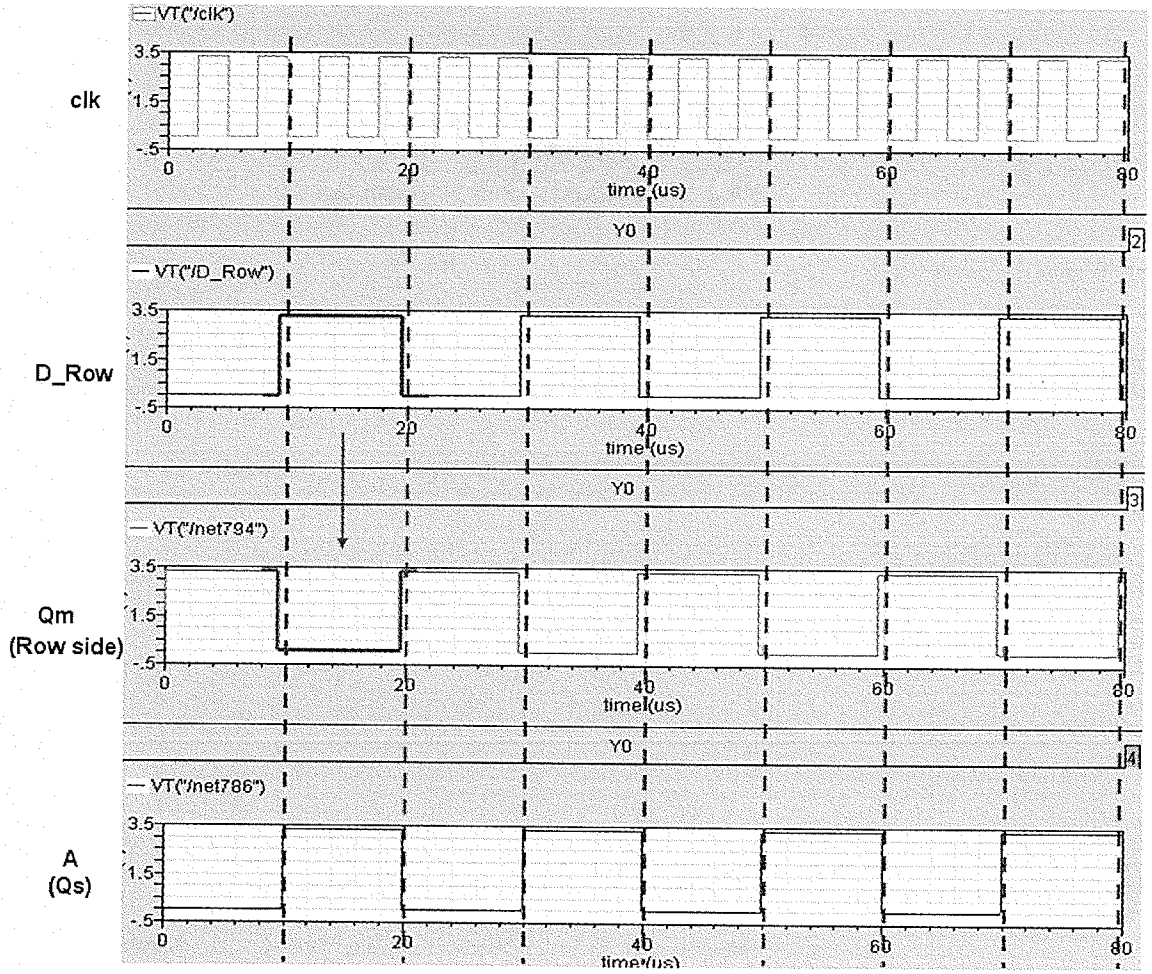


Figure 5-3: Simulated result of the master-slave D flip flop on the row decoder side

As seen from the simulated result, the output of the master stage ($\boldsymbol{Q_m}$) latched the inverted input ($\overline{\boldsymbol{D\_Row}}$) when the clock signal ***clk*** was "1". The output of the slave stage ($\boldsymbol{A}$ or $\boldsymbol{Q_s}$) accepted the output of the master value ($\overline{\boldsymbol{D\_Row}}$) and inverted it when the clock signal dropped to "0". Thus, the master-slave D flip flop sampled the input at every falling edge of the clock pulse. This verifies that the designed master-slave D flip flop on the row decoder side is negative-edge triggered.

The simulated input and output waveforms of the master-slave D flip flop on the column decoder side are illustrated in Figure 5-4. The input clock signal ***clk*** was run at the frequency of 200 kHz, while the input address signal ***D_Col*** operated at 100 kHz.

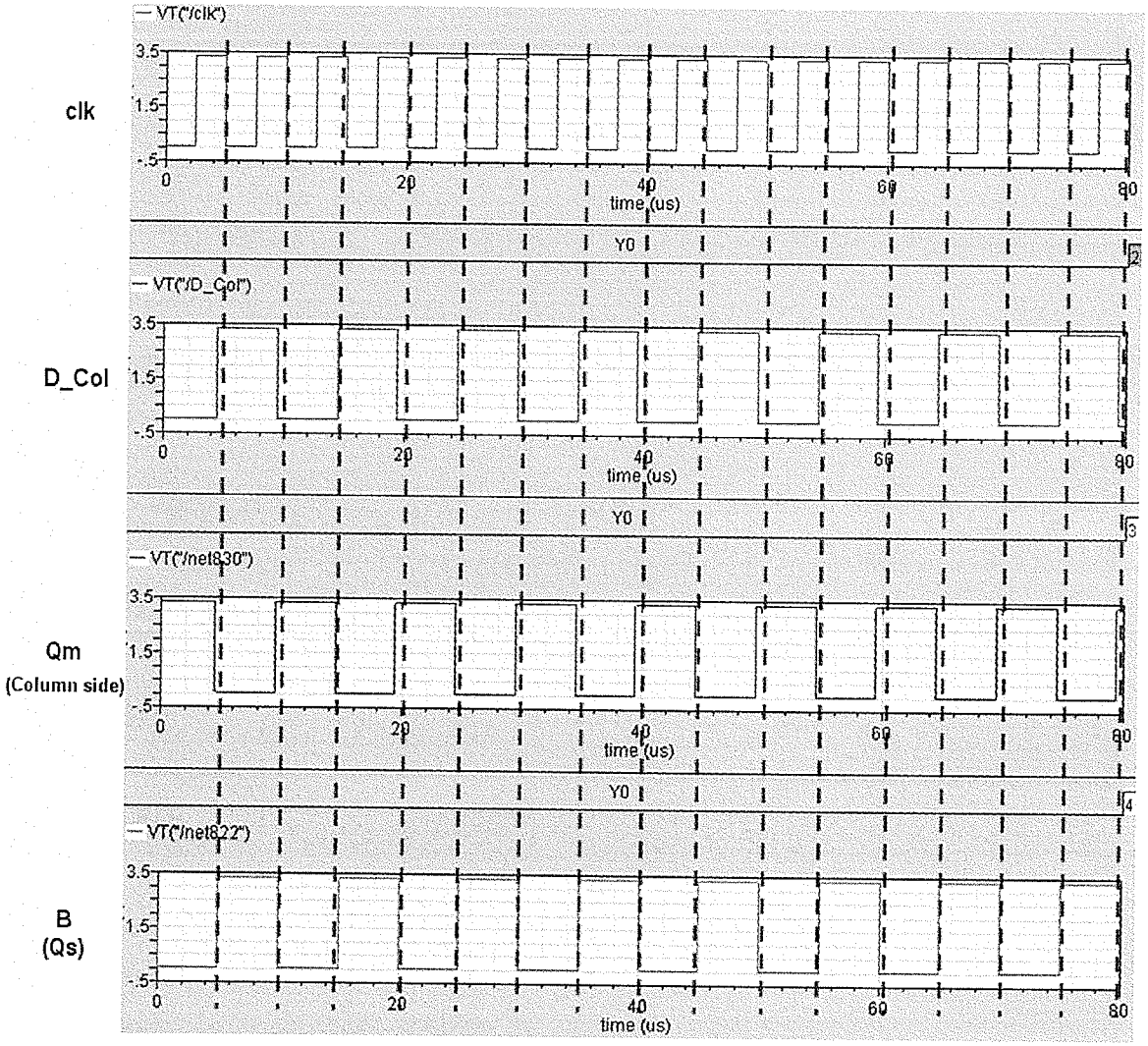


Figure 5-4: Simulated result of the master-slave D flip flop on the column decoder side

The master-slave D flip flop on the column decoder side is also negative-edge triggered, since the state change of the output (***B***) only occurs on the falling edge of the clock. It can also be seen that the output of the flip flop on the column decoder side (***B***)

ran twice as fast as the one of the flip flop on the row decoder side (***A***). This result agrees with the truth table in Table 5-1, and verifies the functionality of the designed master-slave flip flops for both the row and column decoders.

5.2 Decoder Simulation

There are two decoders in the system: a row decoder and a column decoder, as was illustrated in Figure 4-4 and 4-5 respectively. The simulated input and output waveforms of the row decoder are shown in Figure 5-5. The input address signal (***A***) comes from the output of the master-slave D flip flop on the row side. It was run at the frequency of 50 kHz. When the input enable signal (***Enable***) was active "1", the states of the two outputs (***Row_1*** *and* ***Row_0***) varied with the state change of the address input (***A***).

As shown in Figure 5-5, when the input signal ***Enable*** was "1", the output ***Row_1*** was activated if the address input ***A*** was "1". On the contrary, the output ***Row_0*** was activated when the address input ***A*** was "0". The simulated result matches the truth table of the row decoder (Table 4-2) and verifies that the designed row decoder illustrated in Figure 4-4 was functional.

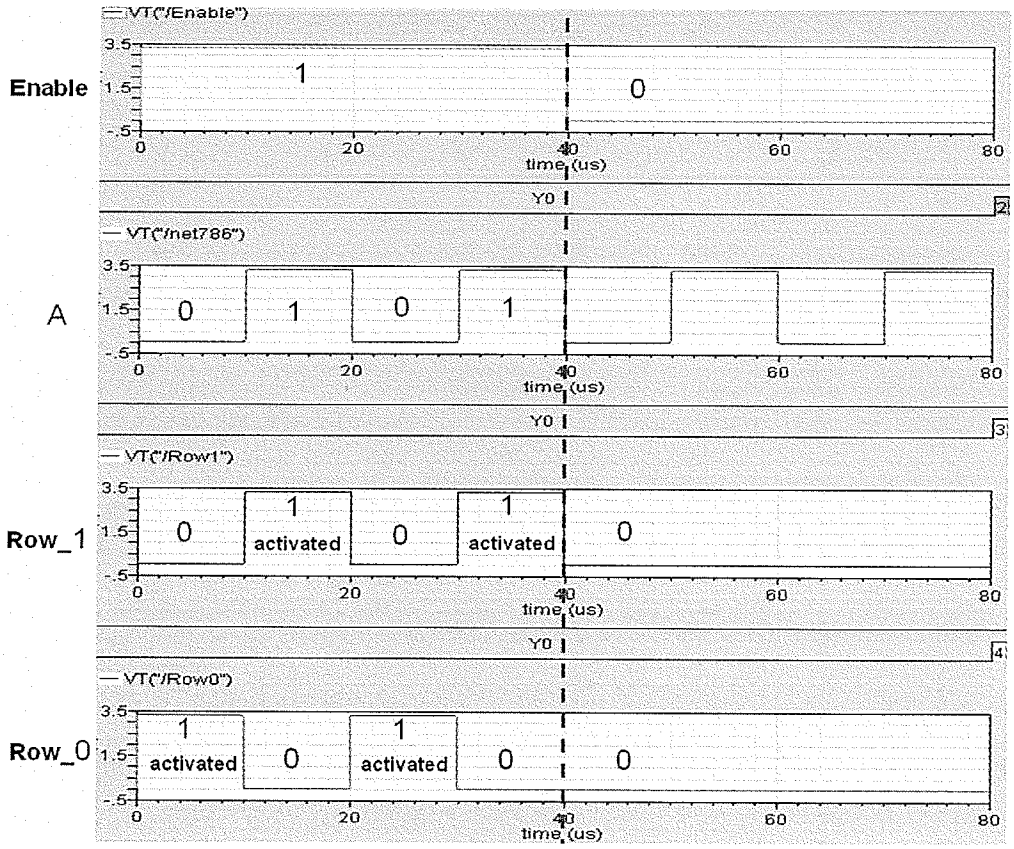


Figure 5-5: Simulated result of the row decoder

The simulated input and output waveforms of the column decoder are illustrated in Figure 5-6. The input address signal (***B***) comes from the output of the master- slave D flip flop on the column side. It was run at the frequency of 100 kHz.

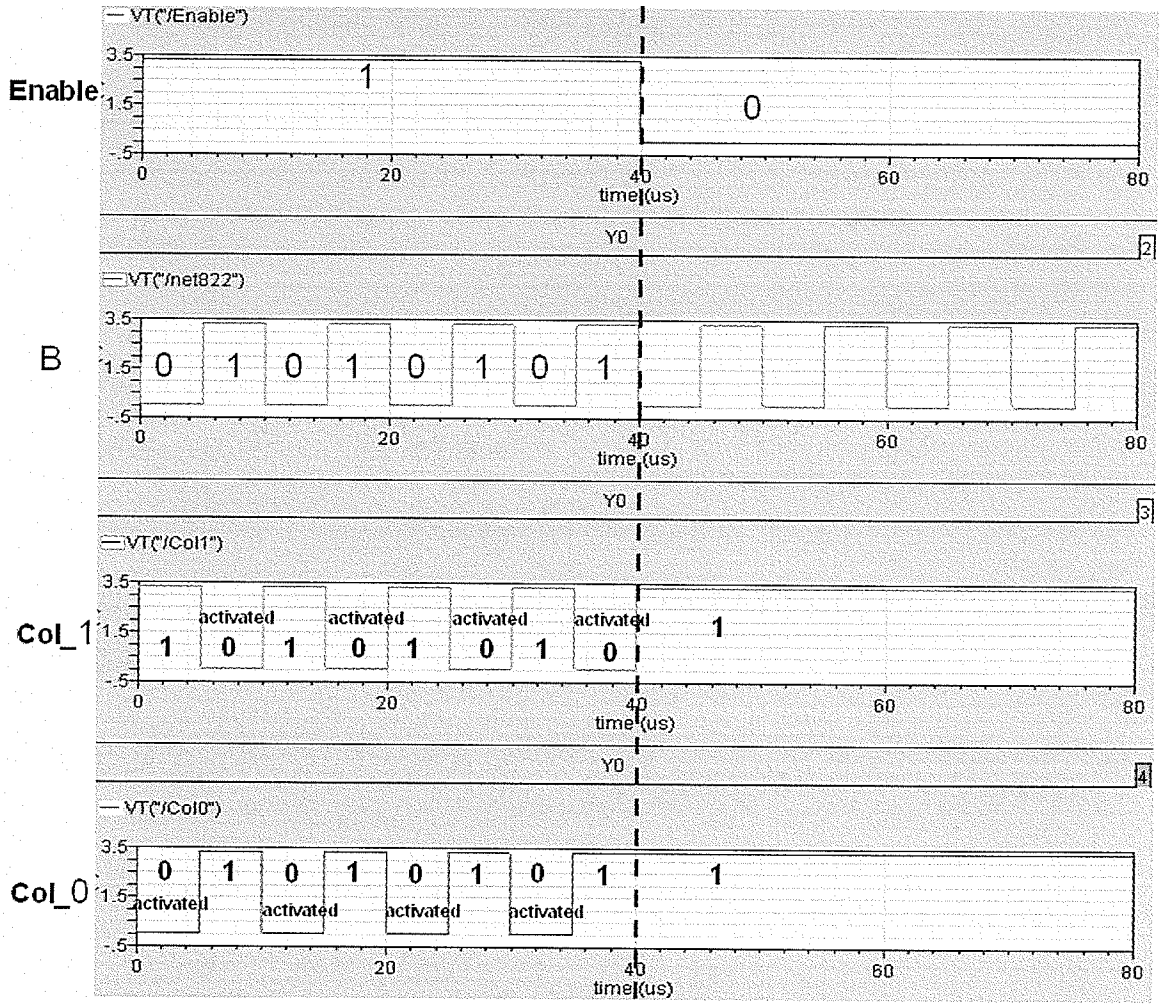


Figure 5-6: Simulated result of the column decoder

As with the row decoder, the column decoder function was also verified using this simulated result. When the signal ***Enable*** was "1", the output ***Col_1*** was activated if the address input ***B*** was "1". The output ***Col_0*** was activated when the address input ***B*** was "0". The simulated result matches the truth table of the column decoder (see Table 4-4).

5.3 Pseudo-Sensor Simulation

The simulated current-voltage (I_{ds}-V_{gs}) characteristics of the pseudo-sensor for three different drain-source voltages (V_{ds} = 0.5, 2.0, and 2.7 V) are shown in Figure 5-7. It can be seen that the I_{ds}-V_{gs} curves for V_{ds} =2 V and 2.7 V overlap in the sub-threshold region. This is due to the fact that in the sub-threshold region the current I_{ds} is independent of the drain voltage once V_{ds} is larger than a few kT/q (i.e. about 25mV) [19], where k is Boltzmann's constant, T is absolute temperature and q is electronic charge.

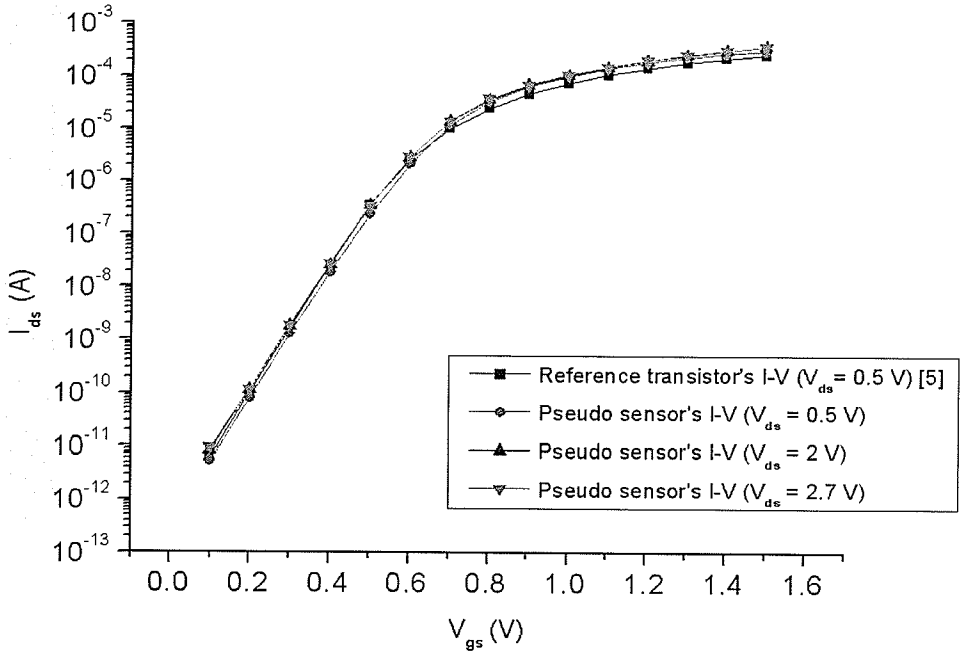


Figure 5-7: The I_{ds}-V_{gs} characteristics of the reference transistor and the pseudo-sensor

An experimental I_{ds}-V_{gs} curve from a reference transistor was used to provide the "ideal" I-V characteristic of the actual sensor [5]. This characteristic is also presented in Figure 5-7. The "ideal" curve agrees well with the two simulated I_{ds}-V_{gs} curves (for V_{ds} =2 V and 2.7 V) in the sub-threshold region. As a result of the strong agreement between

the experimental and "ideal" curves, the pseudo-sensor was used as a reasonable substitute to demonstrate the feasibility of this integrated circuit design in this work.

5.4 Logarithmic Amplifier Circuit Simulation

The logarithmic amplifier was designed to convert the sub-threshold sensor current to a voltage, which would be linearly proportional to the logarithm of the sensor current. In Figure 5-8, transistor T1 is the logarithmic trans-impedance amplifier, through which the sensor current I_{ds} flows. The simulated I_{ds}-V_{sensor} characteristic of this amplifier circuit is demonstrated in Figure 5-9. It can be seen that the voltage across the sensor is linearly proportional to logarithm of the sensor sub-threshold current. The simulated result verifies the functionality of the logarithmic amplifier circuit.

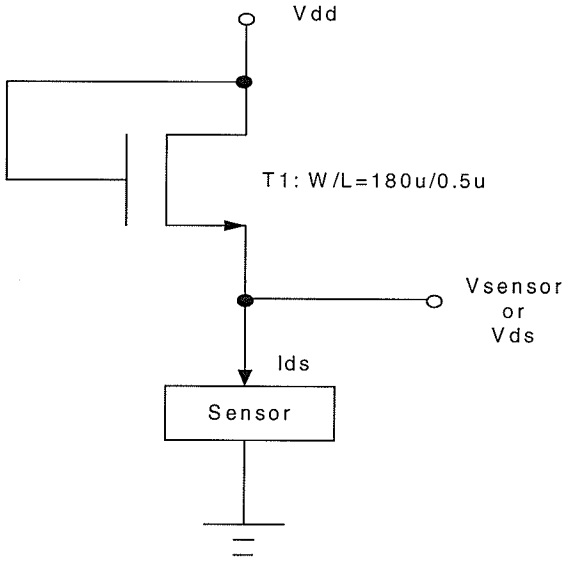


Figure 5-8: The logarithmic amplifier circuit

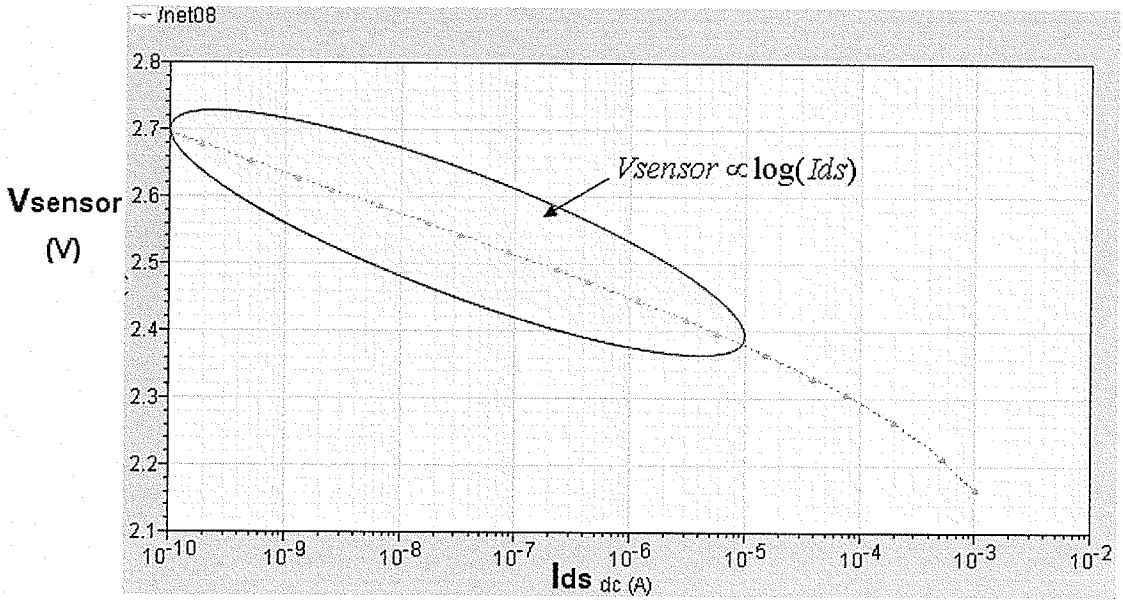


Figure 5-9: Simulated I_{ds}-V_{sensor} characteristic of the logarithmic amplifier circuit

5.5 The Analog Output Circuit Simulation

There are nine input signals in the analog output circuit: four digital signals (i.e., ***Row_1***, ***Row_0***, ***Col_1*** and ***Col_0***) and five bias signals (i.e., I_{ref}, V_g0, V_g1, V_g2 and V_g3). The four input digital signals were produced by the row and column decoders, as were shown previously in Figures 5-5 and 5-6. The enable signal was set high in the first 40 μs to enable the decoders. During this period, the corresponding row and column signals were activated. Different voltages (0.2V, 0.3V, 0.4V and 0.6V) were assigned to the gate bias (V_g0, V_g1, V_g2 *and* V_g3) of each individual sensor. The different gate voltages generated a different sub-threshold sensor current (I_{ds}) [19] for each sensor. The sensor current produced an output voltage that was proportional to $\log(I_{ds})$. This was done to distinguish between each of the sensors during full circuit operation. The reference current (I_{ref}) was set to be 50 μA in the simulation. The output data from of the

simulation is shown in Figure 5-10. After 40 μs, the enable signal was set low to disable the row and column decoders. During this time, the corresponding row and column signals became inactive, the analog output circuit was disabled, and no voltage was read from the sensors.

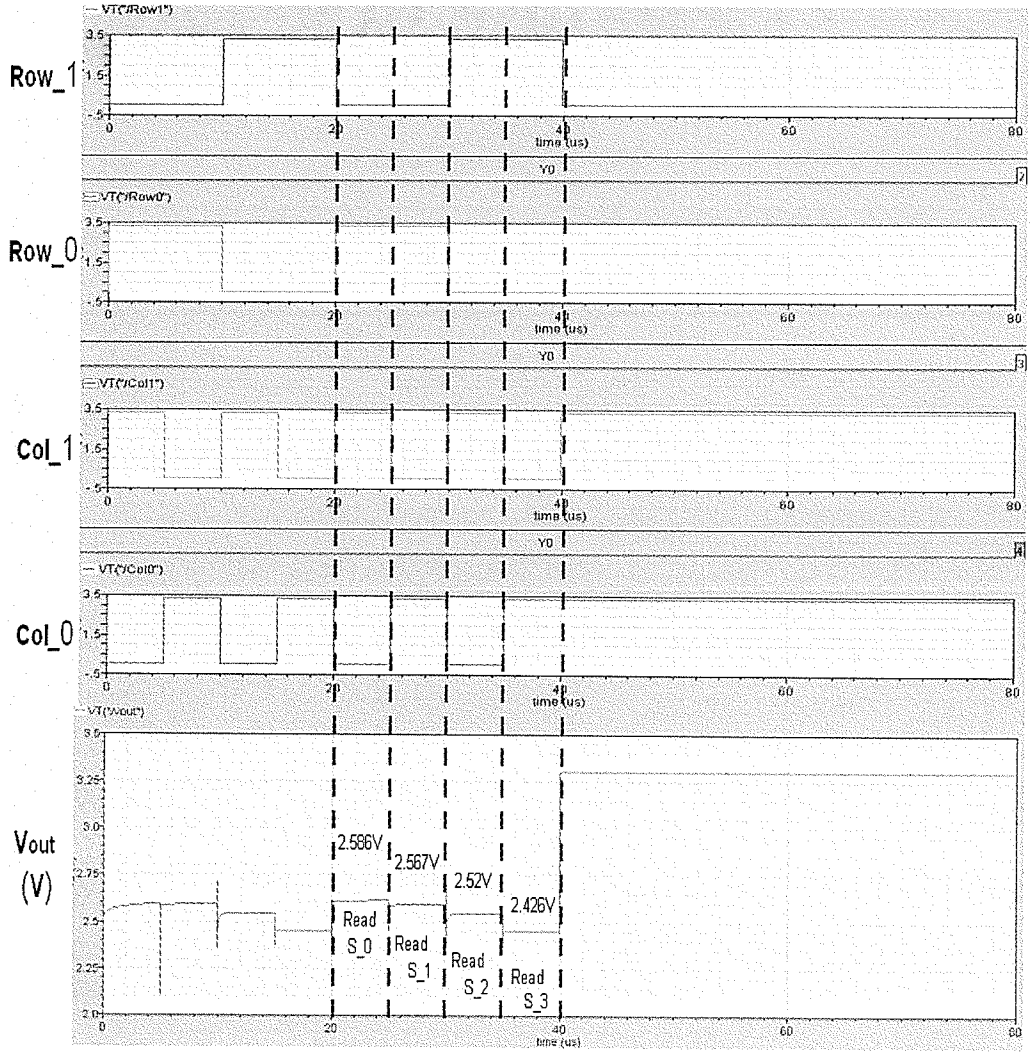


Figure 5-10: Simulated result of the analog output circuit for reading a 2×2 sensor array

Chapter 6 System Layout Design and Layout Verification

Once the verification of the circuit functionality was fulfilled in the simulation, the circuit physical layout was created manually using the Cadence *Virtuoso Layout Editor*. It followed the design rules as defined by TSMC for the CMOS 0.35μm process. In this chapter, the layout design of the digital array-addressing circuit and the analog output circuit is described. The methods for minimizing noise in this mixed-signal sensor system are discussed. The final chip layout is presented, followed by the introduction of the layout verification.

6.1 The Digital Array-Addressing Circuit Layout

The digital array-addressing circuit contains two master-slave D flip flops, row and column decoders. The layout design for both the row and column decoders is the same. Therefore, the layout description, presented in this chapter, of the digital array-addressing circuit will focus on the row decoder and master-slave D flip flop.

All transistors were built on a "p-type substrate". The n-type transistors were built directly in the p-type substrate, while n-well regions were added to accommodate p-type transistors. As shown in Figure 6-1, all transistors were placed in between the two power rails (V_{DD} and Gnd). They were oriented with the drain and source running in the horizontal direction. The p-type transistors were embedded in n-wells. They were placed close to V_{DD} rail while the n-type transistors were closer to the ground. The n-well contacts of p-type transistors were connected to the power supply V_{DD}, and the p-substrate contacts of n-type transistors were connected to the ground. This avoids the formation of a low impedance current flow path from V_{DD} to Gnd (i.e., Latch-up) [20].

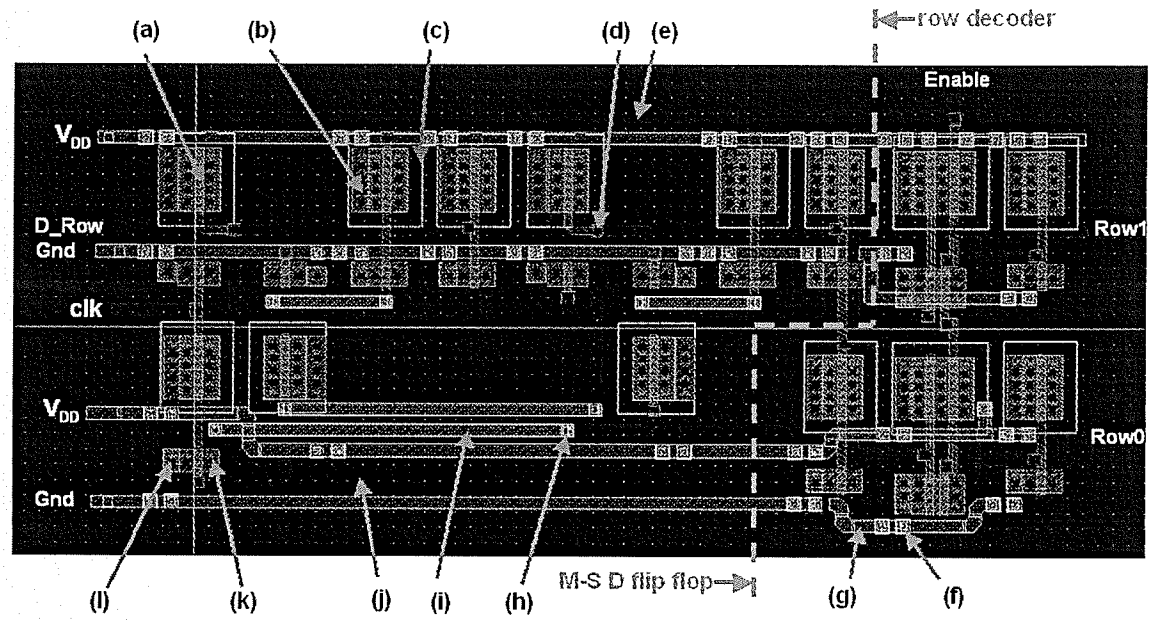


Figure 6-1: The layout of a master-slave D flip flop and a row decoder. (a) poly; (b) n-well voltage contact; (c) n-well; (d) poly-metal1-contact; (e) metal1; (f) via13; (g) metal3; (h) via12; (i) metal2; (j) p-substrate; (k) active contact; (l) substrate ground contact

Four conductive layers were utilized in: poly, metal1, metal2 and metal3. The poly layer was used for the gates of all of the transistors. Metal1 and metal2 were used to implement the interconnections between the transistors. The power supply (V_{DD}) and ground (Gnd) were routed using the metal3 layer. These layers were electrically isolated from each other. Different vias and contacts were created manually to realize electrical contact between the conducting layers. For example, a via12 provided an electrical connection between metal1 and metal2. The poly-metal1-contact connected metal1 to the poly gate, as shown in Figure 6-2.

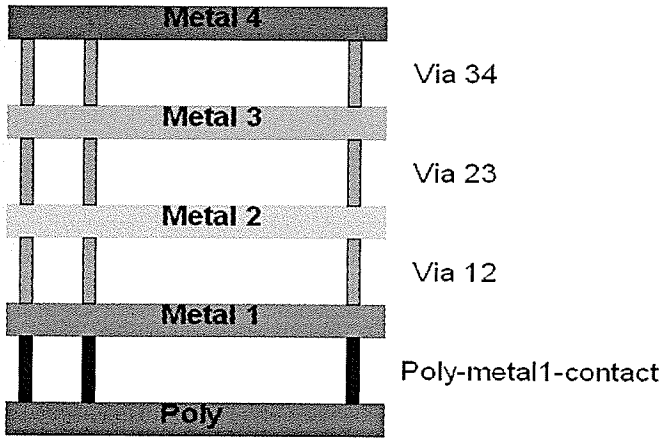
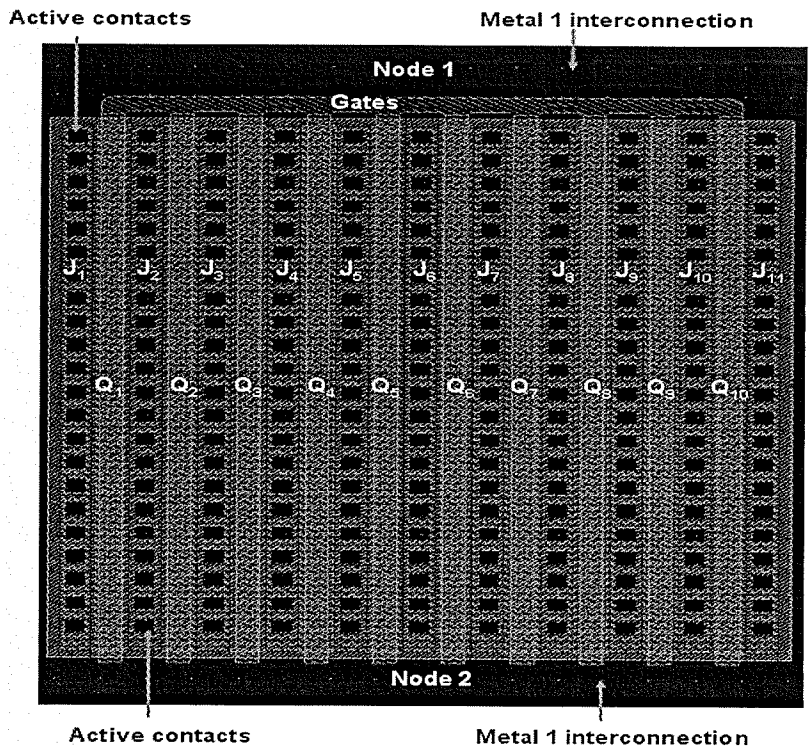


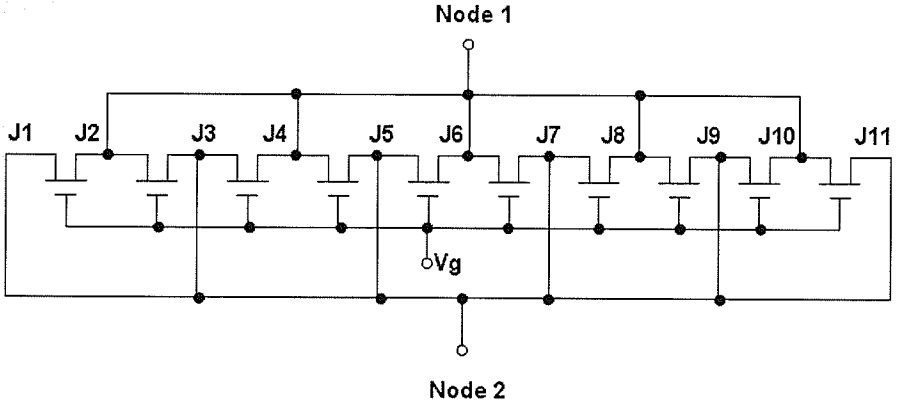
Figure 6-2: A cross-section illustrating the connections between conducting layers

6.2 The Analog Output Circuit Layout

Wide transistors were used in the analog output circuit. For example, the logarithmic trans-impedance transistor, which has a W/L ratio of 180μm/0.5μm, is required to produce the required logarithmic voltage dependence over a wide current range. Since the design rules require a minimum distance between adjacent transistors, this large transistor, which would be extremely long, would be difficult to be efficiently placed in the layout [21]. In order to produce a compact layout design, smaller transistors were connected in parallel to act as a single transistor of the same effective size as the original large one. The layout and circuit corresponding of this large transistor is illustrated in Figure 6-3 (a) and Figure 6-3 (b) respectively. The transistors are drawn in the same relative positions [22].



(a)



(b)

Figure 6-3: (a) The layout of a transistor with a *W/L* ratio of 180μm/0.5μm; (b) The corresponding equivalent schematic circuit

In the wide transistor layout design, a large number of active contacts were added in junction regions to minimize the contact impedance, as shown in Figure 6-3 (a) [21]. The layout design for the other wide transistors in the analog output circuit followed the same approach as described above.

In Figure 6-4, the layout of the analog output circuit for the sensor array is presented. As with the layout design for the digital array-addressing circuit, all transistors in the analog output circuit were placed between the two power rails (V_{DD} and Gnd). They were oriented with the drain and source running in the horizontal direction. The n-well contacts of the p-type transistors were connected to the power supply V_{DD}, while the p-substrate contacts of the n-type transistors were connected to the ground in order to prevent latch-up.

The four pseudo-sensors were placed closed to either side of the circuit periphery, so that the bias voltages (V_g0~V_g3) can be easily applied. This also simplified the arrangement for the metal interconnection. The poly, metal 1, metal 2 and metal 3 layers were also utilized in the analog output circuit layout. The contacts and vias were created to realize electrical contact between these conductive layers.

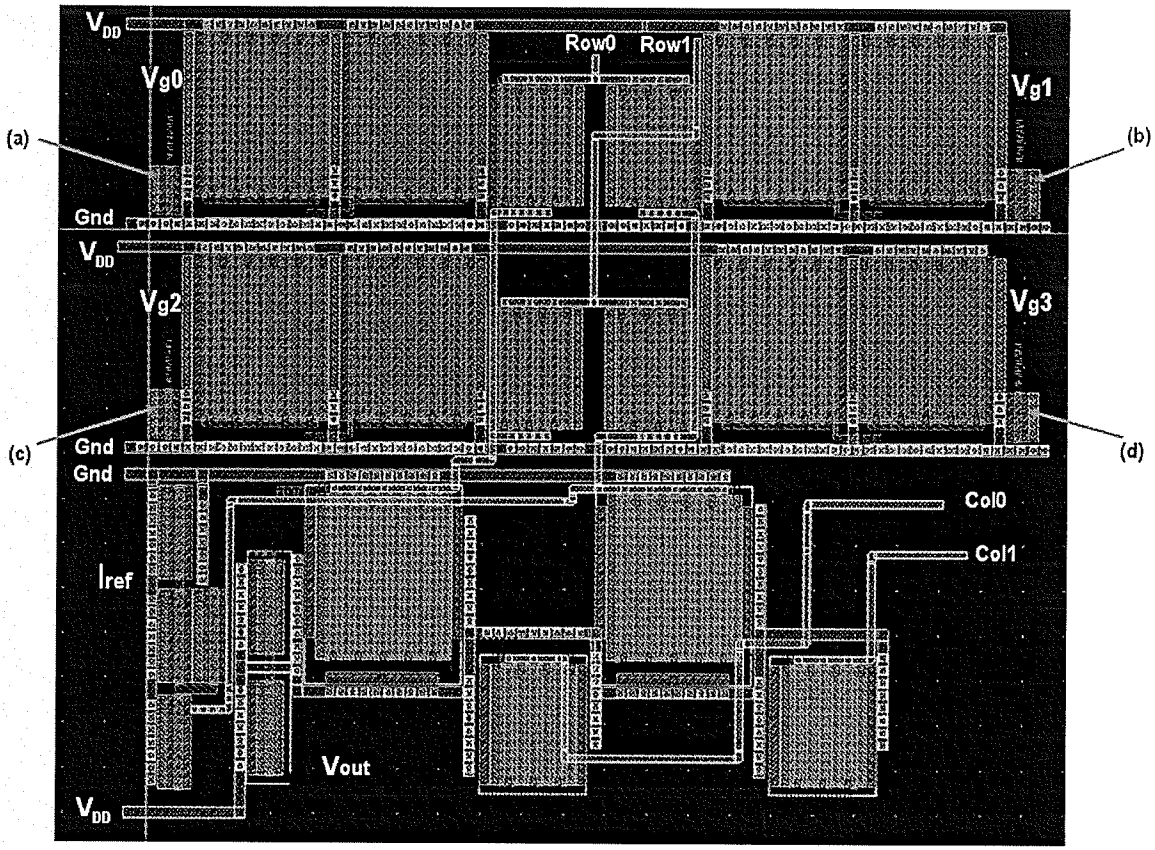


Figure 6-4: Layout of the analog output circuit for reading the 2×2 array of 4 sensors: (a) pseudo-sensor 0; (b) pseudo-sensor 1; (c) pseudo-sensor 2; (d) pseudo-sensor 3

6.3 The Mixed-Signal Sensor System Layout

This sensor system is a mixed signal system, which contains both a digital array-addressing circuit and an analog output circuit. Since digital switching may produce a glitch either in the substrate and/or the power supply [22], the following two methods were used to minimize noise that could affect the analog circuit.

One approach was to have two separate power supplies and ground connections for the digital and analog circuits. As shown in Figure 6-5, V_{DD1} and Gnd1 were used for the digital array-addressing circuit, and V_{DD2} and Gnd2 for the analog output circuit.

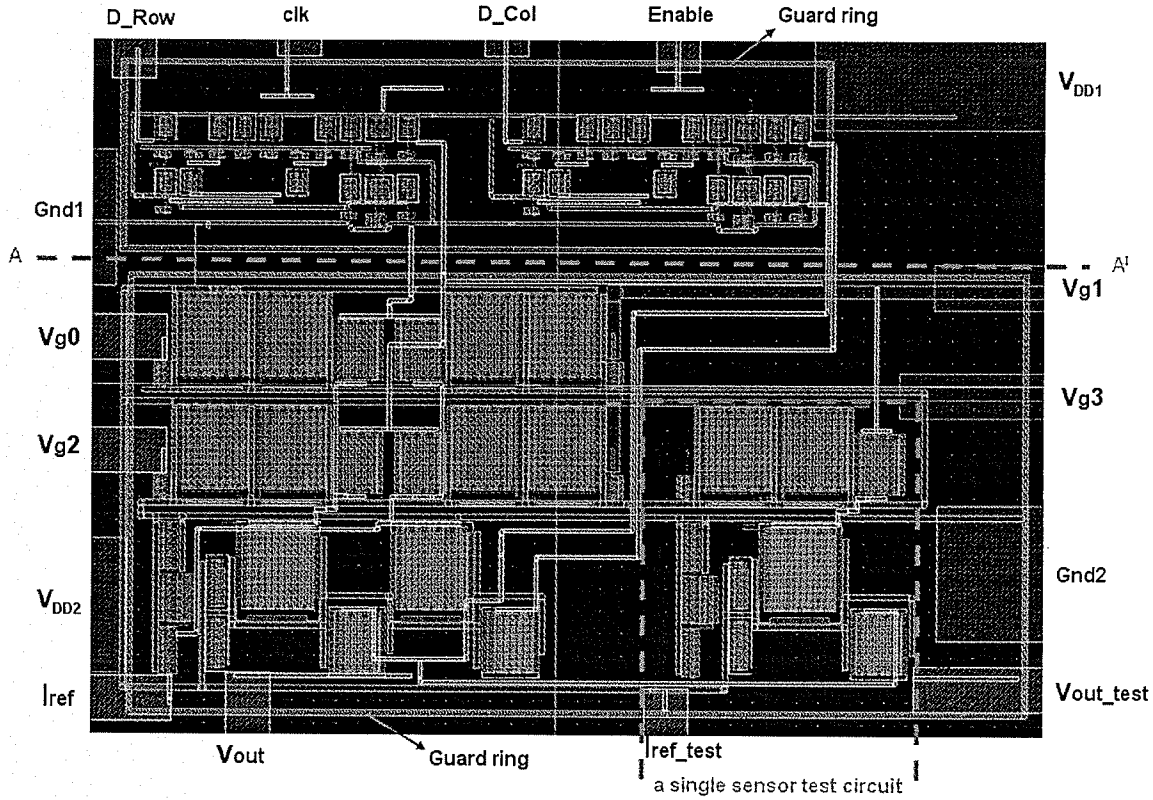


Figure 6-5: Layout of a mixed-signal 2×2 sensor array system

The other method was to lay out the digital and analog circuits in isolated sections of the chip [22]. As is shown in Figure 6-5, the digital array-addressing circuits were placed in the area above the line AA^1, while the analog output circuit was placed below the line AA^1. These two sections were also separated by two guard rings connected to the separated grounds (Gnd 1 and Gnd 2) to keep a low-impedance path between the substrate and ground [22].

As shown in Figure 6-5, a layout of a single sensor test circuit was embedded in the system. This test circuit contains a single pseudo-sensor and its own analog output

circuit. The schematic was presented in Chapter 4 (see Figure 4-8). It was used to test the functionality of the digital addressing and analog output circuit for a single sensor in the array. The operational details of these circuits will be described in Chapter 7.

6.4 The Final Chip Layout

The dimension of the final chip was 1051.9μm×1151.95μm. Sixteen bond pads were used for delivering signals and power supplies, as shown in Figure 6-6. Dummy bond pads were added at four corners, as they were required by the TSMC design rules.[20] The design rules also stipulate a minimum density of the poly layer and all the metal layers. Therefore dummy pads on these levels were also included.

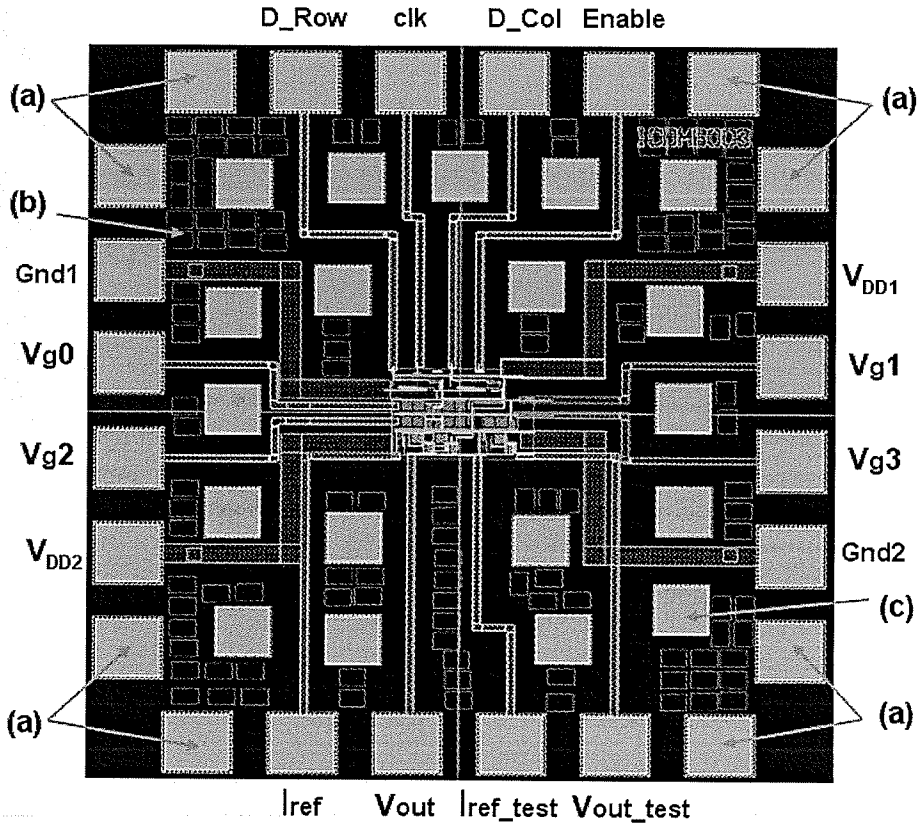


Figure 6-6: The final chip layout. (a) dummy bond pads; (b) dummy poly and metal patterns; (c) dummy pads with smaller size (80μm×80μm)

6.5 Layout Verification

In this section, two layout verification tools are introduced: the design rule checker (DRC) and "Layout versus Schematic" check. These were also provided in Cadence *Virtuoso Layout Editor.*

6.5.1 Design Rule Check

The Design rule check (DRC) is a process to ensure that the layout meets all of the physical constraints of fabrication process [23]. For example, the width and spacing of every metal line in the layout were checked to ensure that they do not violate the minimum specified values [20]. During the layout design, the DRC was performed frequently to ensure that all layout errors were removed before the entire design was completed.

6.5.2 Layout vs. Schematic Check

Once the layout had satisfied all the design rules, the layout versus schematic check (LVS) followed next. Circuit extraction was performed to create a detailed netlist. A "netlist" is a list of all the circuit elements, their positions and all interconnections. The transistors, the interconnections and parasitic capacitances between the layers were identified in this step. Consequently, the LVS check was used to compare the original circuits, designed at a schematic level, with the one extracted from the layout. This process ensured that the layout properly emulated the schematic design. Therefore, the LVS check provided an addition confidence in the integrity of the design. From the LVS output of the integrated sensor system, it was found that the netlists from both the schematic circuit and the layout extraction were identical. This verified that the physical layout was a correct realization of the circuit topology.

Chapter 7 Experiments

After the chip was fabricated and packaged through CMC Microsystems, the performance of the chip was tested. In this chapter, the experimental set-up for the digital and analog circuit functionality test, and A/D conversion is described. The testing results of both a single sensor and the 2×2 sensor array system are presented.

7.1 Experimental Set-up

The experimental set-up used for testing this chip is shown in Figure 7-1. It consisted of a buffer, an amplifier circuit, an A/D converter, a logic analyzer and the test chip. The output voltage of the test chip was fed into the buffer and the amplifier prior to the A/D conversation. The 8-bit digital output code was then sent to a 1681 AD logic analyzer for analysis.

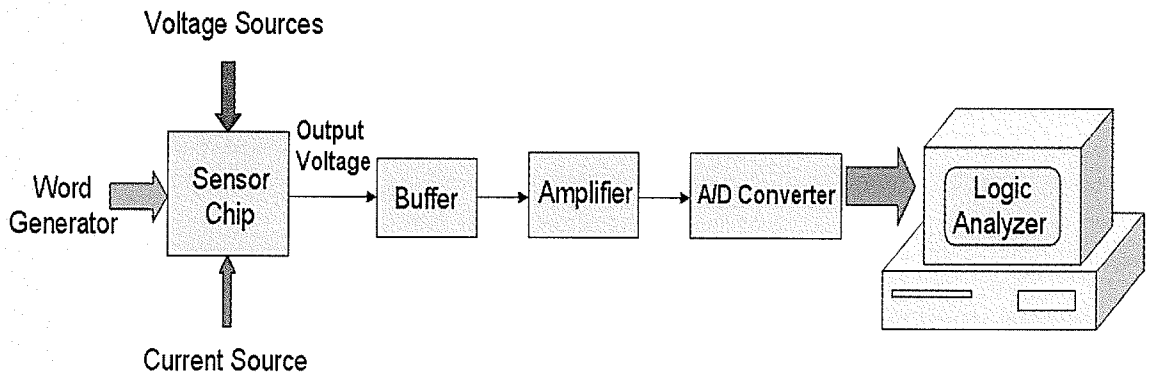


Figure 7-1: The experimental set-up for the functionality test and A/D conversion

Separate voltage sources were used to provide supplies for the digital and analog circuits on the sensor chip (V_{DD}) as well as the sensor gate biases (V_{g0}, V_{g1}, V_{g2} and V_{g3}). The reference bias current $\boldsymbol{I_{ref}}$ was supplied by a programmable current source. An

8016A word generator was used to generate the four digital input signals: the clock signal ***clk***, the two address signals ***D_row***, ***D_Col*** and the enable signal ***Enable***.

In an attempt to eliminate signal attenuation and cross-talk, a buffer amplifier was utilized. As shown in Figure 7-2, the buffer was constructed by connecting the output of the LM 741 to the inverting input, and connecting the output of the chip to the non-inverting input. This buffer amplifier had a unity gain.

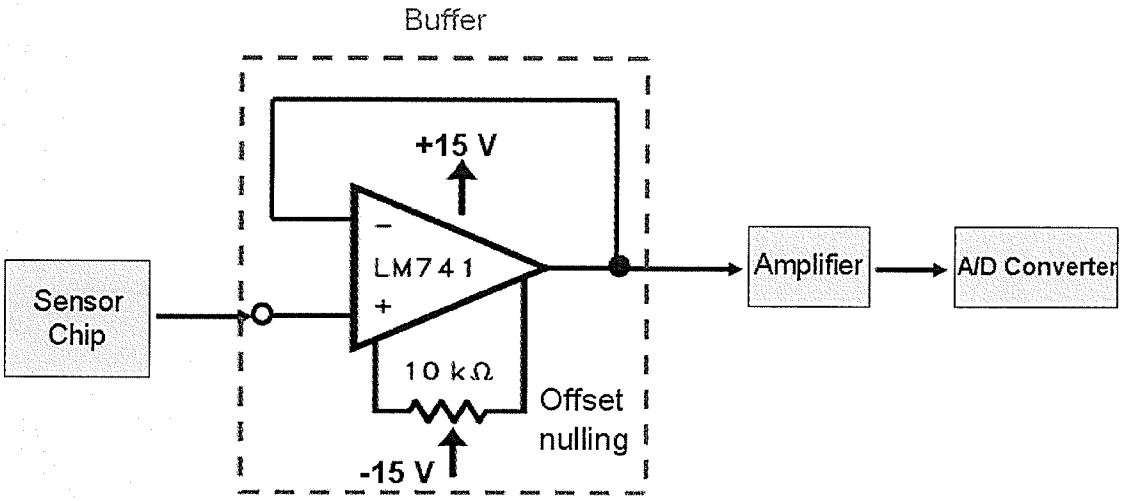


Figure 7-2: The buffer circuit

The output of the buffer was connected to an operational amplifier prior to the A/D conversion. This additional amplifier was used to increase the gain of the V-log(I_{sensor}) characteristic from the sensor chip. It was also used to provide the A/D converter with the input analog full-scale voltage range (0V ~5.12V), as shown in Figure 7-3.

An 8-bit ADC0804 was used for the analog to digital conversion. Its connection with the amplifier and a logic analyzer is shown in Figure 7-4. In order to minimize noise

pickup, a 0.1 μF bypass capacitor [24] was placed at the analog input (pin 20). A 10 μF filter capacitor [24] was also added to the voltage supply (pin 20) to reduce noise spikes.

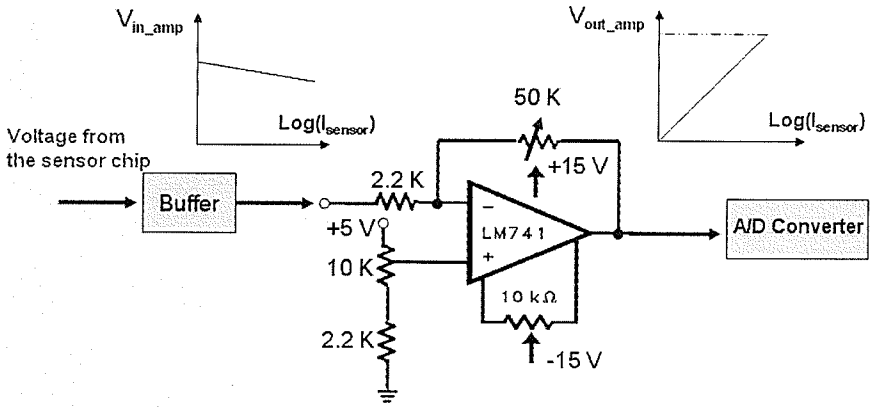


Figure 7-3: The amplifier circuit

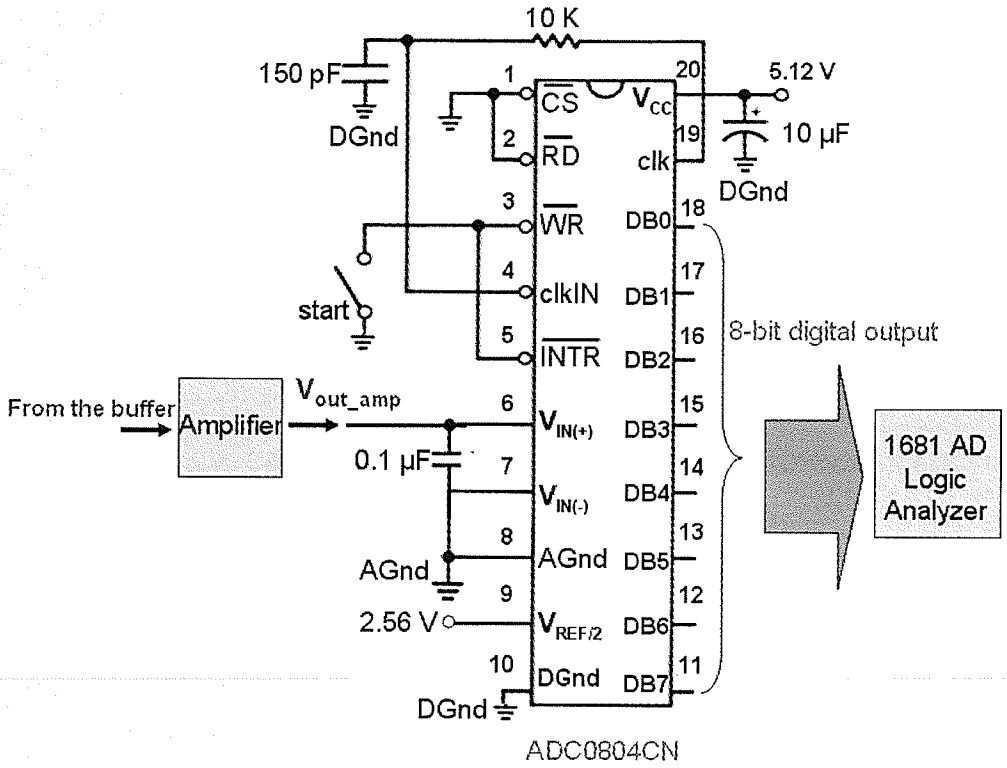


Figure 7-4: The A/D converter circuit

To start the A/D converter, an external write signal ($\overline{WR}$ pulse) was required after power-up. Once a digital 8-bit binary data was transferred to output, an interrupt was asserted (i.e. $\overline{INTR}$ made a high-to-low transition) [24]. Since the write input (low is active signal for $\overline{WR}$) was connected with the interrupt pin, a new conversion started. The data output was continuously enabled since the two active low signals: chip select ($\overline{CS}$) and read ($\overline{RD}$) were both grounded, as shown in Figure 7-4. The digital output data was displayed on a logic analyzer.

The converter was run at 640 kHz since this is the highest frequency where the accuracy of the converter is still within the range of ± 1LSB. The reference voltage ($V_{REF}/2$) was supplied with 2.56 V and a voltage supply voltage of 5.12 V was used. This provided an LSB value of 20 mV. [24]

7.2 Testing a Single Sensor Circuit on Chip

To partially test the functionality of the digital addressing and analog output circuit, a V_{out}-I_{sensor} experiment for a single sensor was conducted. The output voltage from the sensor was then converted to a digital value using an A/D convertor. In this section, the test procedures are described and the results are discussed.

7.2.1 V_{out} - I_{sensor} Test

The "V_{out}-I_{sensor} Test" was used to investigate the relationship between the current through and output voltage from a single sensor. A schematic diagram of the test circuit is shown in Figure 4-8 below. As each individual sensor is addressed individually, for this test the addressing function was fulfilled by activating the digital signals ***Row_1*** and ***Col_0***.

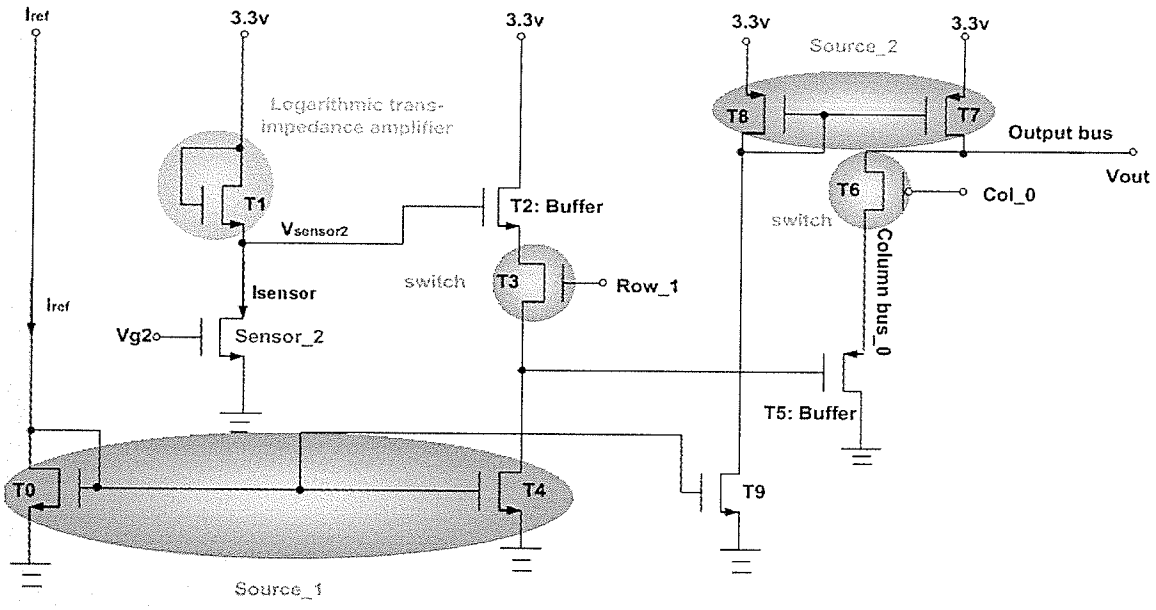


Figure 4-8: CMOS implementation for reading out one sensor

The pseudo-sensor current could not be measured directly from the chip, since the corresponding testing pads were omitted to meet the strict fabrication deadline. Therefore, the current was obtained from the simulated I_{ds}-V_{gs} curve of the pseudo-sensor (see Figure 5-7).

The following steps were taken to determine the V_{out} vs. I_{sensor} relationship. A bias (V_g) was applied to the gate of the sensor, and the corresponding output voltage (V_{out}) was measured. The sensor current ($I_{sensor} = I_{ds}$) was then "extracted" from the simulated I_{ds}-V_{gs} curve to obtain the V_{out} vs. I_{sensor} relationship.

A voltage, ranging from 0 - 2 V, was applied to the sensor gate and a reference current (158 μA) was fed into the circuit. A 200 kHz signal was connected to the clock input. In order to address the pseudo-sensor, the signal ***D_row*** was set high ("1") and ***D_Col*** was set low ("0"). The enable signal was kept active to realize the continuous

operation of the digital addressing circuit. The V_{out}-V_g and V_{out}– I_{sensor} characteristics are shown in Figure 7-5 and Figure 7-6 respectively.

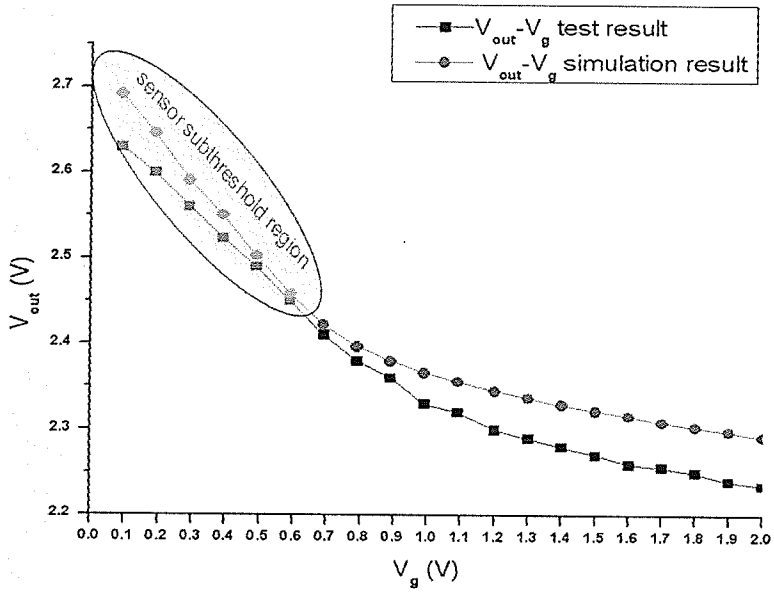


Figure 7-5: The V_{out}-V_g test result and the simulation result

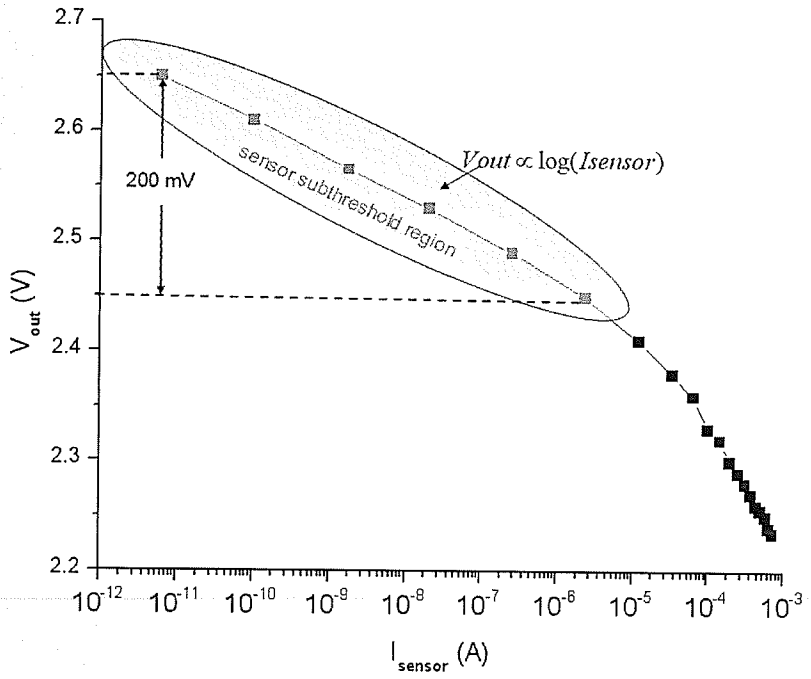


Figure 7-6: The V_{out}-I_{sensor} characteristic

From Figure 7-6, it can be seen that the output voltage of the test circuit is linearly proportional to the logarithm of the sensor sub-threshold current, demonstrating that this part of the integrated circuit performed correctly over a specific current range. The output voltage, V_{out}, changed ~ 200 mV for a sensor current change of 5 orders of magnitude; a gain of only 43 mV/decade. To increase the gain, the reference current to the analog circuit was decreased, but only maximum gain of 48 mV/decade was achieved. In Table 7-1, the data shows that gain for different reference currents and shows that these changes had only a minor effect on the gain. Therefore, an additional operation amplifier was added prior to the A/D circuit.

Table 7-1: The effect of the reference current on the circuit gain

I_{ref} (μA)	20	50	80	100	158	200
Gain (mV/decade)	48	48	46	45	43	44

The output voltage of the sensor chip was connected to the inverting input of a LM741 operational amplifier through the buffer, as shown previously in Figure 7-3. The test chip was biased using a 50 μA reference current as this yielded the maximum gain. A voltage ranging from 0 - 0.7 V was applied to the sensor gate to ensure that it was being operated in the sub-threshold region. As in the V_{out}-I_{sensor} test, the signal ***D_row*** was set high ("1") and ***D_Col*** was set low ("0"). The enable signal was kept active continuously.

The output voltage from the sensor (V_{out_sensor}) was measured at the input of the amplifier. As shown in Figure 7-7, the sensor output voltage changed only ~ 320 mV for a current change of 7 orders of magnitude. Therefore an amplifier was required to boost the gain.

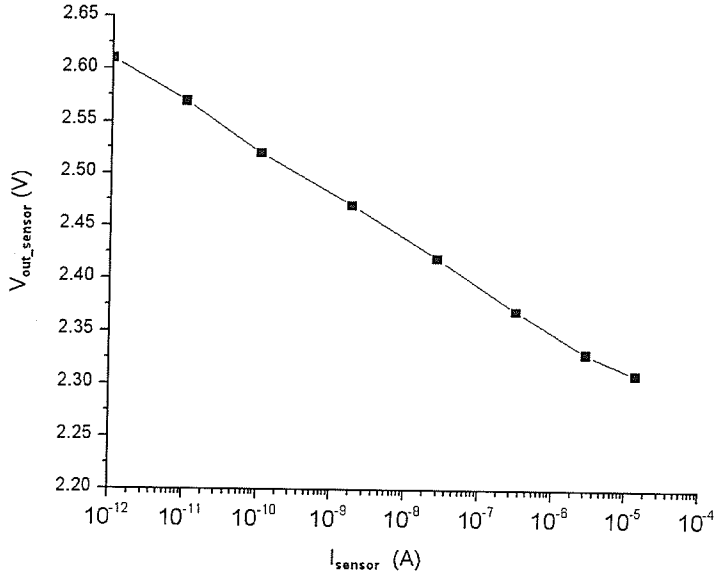


Figure 7-7: Sensor output voltage as a function of the logarithm of sensor current

The output voltage of this amplifier was measured as a function of the voltage-sensor current characteristic, and the results are shown in Figure 7-8. It can be seen that the gain of the V-log(I_{sensor}) characteristic was successfully increased and the output voltage was scaled to cover the range 0–5.12 V, which is the required A/D full input voltage range.

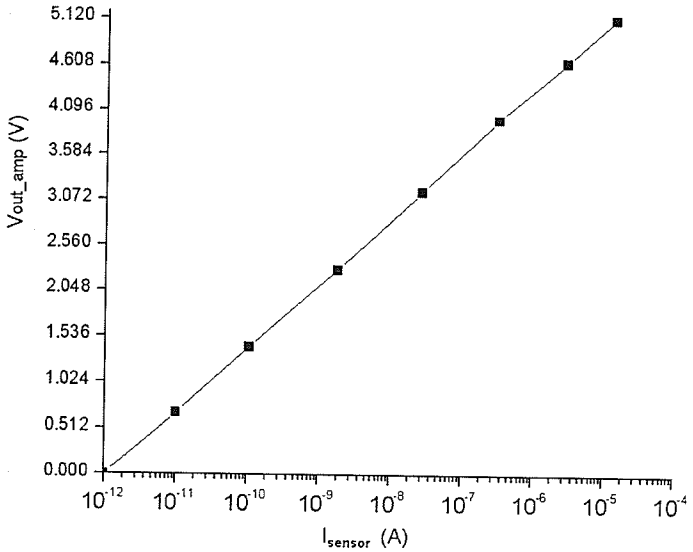


Figure 7-8: Output amplifier voltage as a function of the logarithm of sensor current

7.2.2 A/D Conversion Experiment

The input to the A/D converter was the output of the previously discussed amplifier which had been scaled to 5.12V. Since the A/D converter is an 8-bit converter, a full scale input voltage should result in a "FF" (Hex) or 255 (decimal) digital output. The full scale input, i.e. 7 orders of magnitude of sensor current, or 0-5.12 V from the amplifier, does indeed produce what appears to be a linear curve and does extend out to full range of the A/D converter.

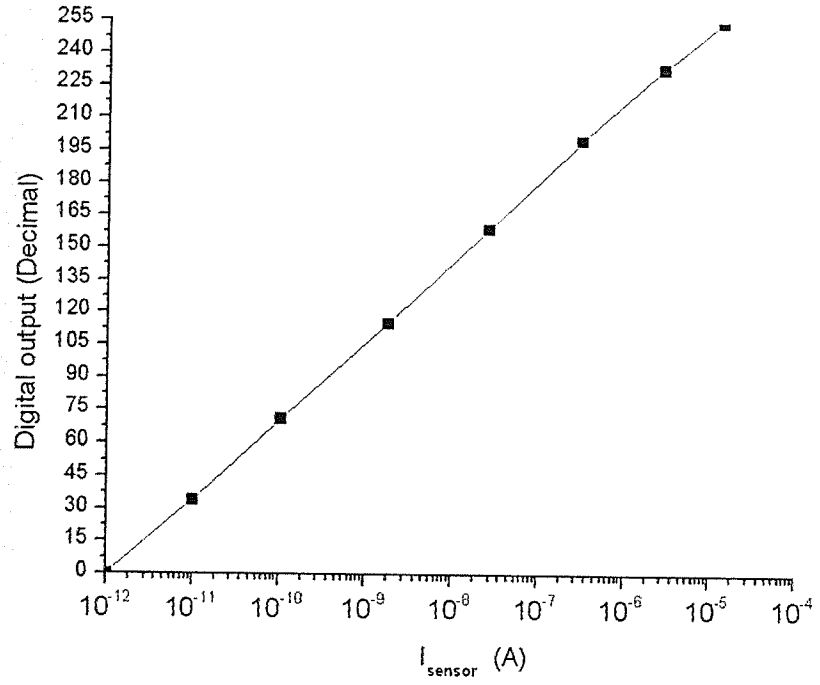


Figure 7-9: The decimal output data versus the sensor current

7.3 Testing the 2×2 Sensor Array System

To fully test the sensor array and the associated integrated circuits on the chip, the functional test, the A/D conversion and cross talk experiments were conducted. The test procedures are described and the results are presented in this section.

7.3.1 Functional Testing

Functional testing was performed to assess the ability of the integrated circuit to access and read the voltage from each individual sensor. In this test, four different voltages (0.1 V, 0.3 V, 0.5 V, and 0.7 V) were applied to the gate of each sensor, to mimic a different current for each pseudo-sensor. The analog output circuit was biased with a reference current of 50 μA. The digital address input signals (***D_Col*** and ***D_Row***) were driven at a frequency of 100 kHz and 50 kHz respectively. The enable signal was kept active to realize the continuous operation of the digital addressing circuit. The clock frequency running on the integrated circuit was set at 200 kHz.

The output voltage was read from the 2×2 sensor array, and the result is shown in Figure 7-10. During the first 5 μs, Sensor_0 was accessed and read. The other three sensors were then individually addressed and read in the following 15 μs at 5 μs intervals. The process repeated every 20 μs.

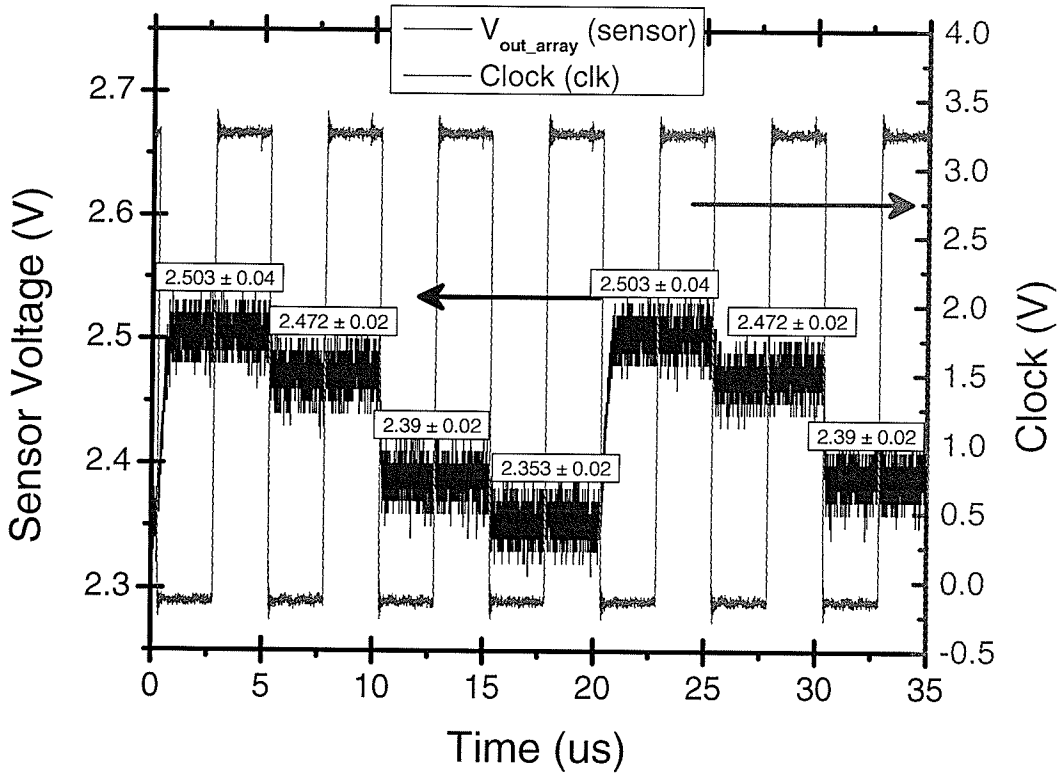


Figure 7-10: The output voltage from the 2×2 sensor array

Table 7-2: The corresponding output voltage values of the 2×2 sensor array system

V_g (V)	0.1	0.3	0.5	0.7
Sensor addressed and read	Sensor_0 (During the first 5 μs)	Sensor_0 (During the first 10 μs)	Sensor_0 (During the first 15 μs)	Sensor_0 (During the first 20 μs)
V_{out_array} (V)	2.503 ± 0.04	2.472 ± 0.02	2.390 ± 0.02	2.353 ± 0.02

The output voltage of the individual sensors contains the noise with an average value of 25 mV, as shown in Table 7-2. Since the signal can be measured when signal to noise ratio is greater than one, the minimum measurable output voltage of this integrated circuit should be greater than 25 mV. For a 10μm×10μm floating-gate extension area,

assuming there are 10^{12} molecules in one square centimeter and only one analyte molecule in this whole extension area. The analyte molecule concentration on this floating-gate extension area is 1ppm in this case. If the chemical reaction caused by this analyte molecule can produce one electron charge, the sensor threshold voltage shift (ΔV_{th}) is as following

$$\Delta Vth = \frac{\Delta Q}{C} = \frac{q}{(\frac{\varepsilon A}{d})} \quad [5] \tag{7.1}$$

where ΔQ is a total charge change stored on the floating gate, C is the capacitance between the floating gate and the control gate, ε ($=0.84\varepsilon_o$ [5]) is the permittivity of the inter layer dielectric (ILD) between the two gates, A is the area of the floating-gate extension, and d is the thickness of the ILD layer between the two gates. The minimum analyte molecule concentration that the integrated circuit can measure is listed in the Table 7-3. It can be seen that the sensitivity of the integrated circuit as a function of analyte concentration is dependent upon the capacitance of the ILD layer between the two gates (thickness, area and permittivity). This integrated circuit can measure an analyte molecule concentration of 1 ppm if the sensor has a 1μm×1μm floating-gate extension area and the ILD thickness of 1 μm.

Table 7-3: The predicted minimum measurable analyte molecule concentration

d (μm)	ΔV_{th} (μV)	Minimum analyte molecule concentration (ppm)
0.2	43.084	580.26
0.5	107.71	232.10
1	215.42	116.28

As shown in Figure 7-10, the output voltage, V_{out_array}, changed only 150 mV for a sensor gate voltage change of 0.6 V, mimicking a 6 order of magnitude change in sensor current. This level was adjusted using a LM741 operational amplifier prior to being applied to the A/D converter.

7.3.2 A/D Conversion for the 2×2 Sensor Array System

In order to allow the required minimum100 μs conversion time of the ADC0804 converter, the clock frequency running on the sensor chip was originally set to 10 kHz. However, this frequency was found too fast. The A/D converter did not have enough time to perform a full conversion. The output digital values were either incorrect or missed. As a result, lower clock frequencies were used and the optimal results were obtained at a clock frequency of 5 kHz. The digital addressing inputs and the digital output from the A/D conversion circuit are shown in Figure 7-11. The input sensor gate voltage and the corresponding digital output value are listed in Table 7-4.

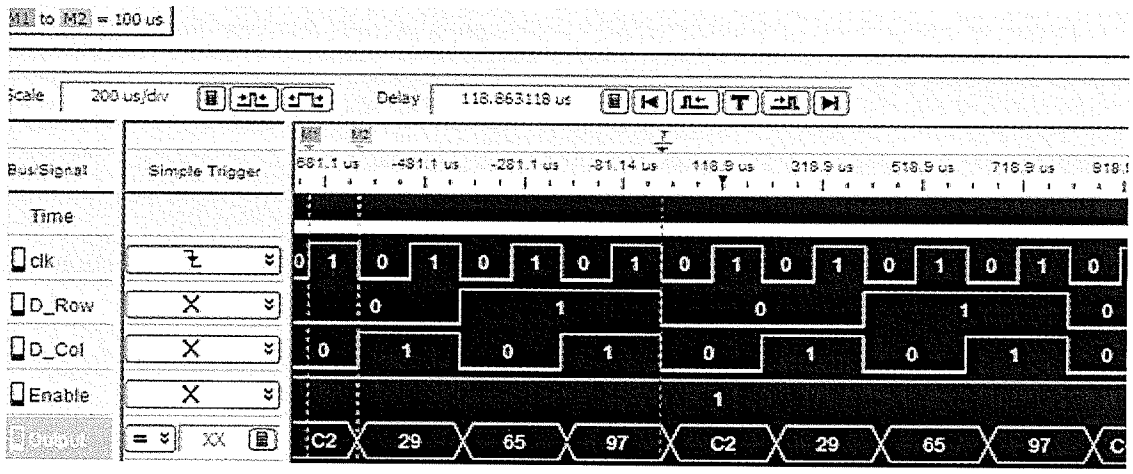


Figure 7-11: The digital addressing inputs and the hexadecimal output displayed on the 1681 AD logic analyzer in the A/D conversion experiment

Table 7-4: The input sensor gate voltage and digital output values in the above A/D conversion experiment

V_g (V)	0.1	0.3	0.5	0.7
Sensor addressed and read	Sensor_0 (During the first 200 μs)	Sensor_1 (During the second 200 μs)	Sensor_2 (During the third 200 μs)	Sensor_3 (During the fourth 200 μs)
Digital output (Hex)	29	65	97	C2

In the 2×2 sensor array, each component sensor was designed to be identical. As such, the outputs of the sensors should be also identical for a given gate voltage. However, due to process variation during fabrication, the outputs of individual sensors were slightly different. This variation is shown in Figure 7-12.

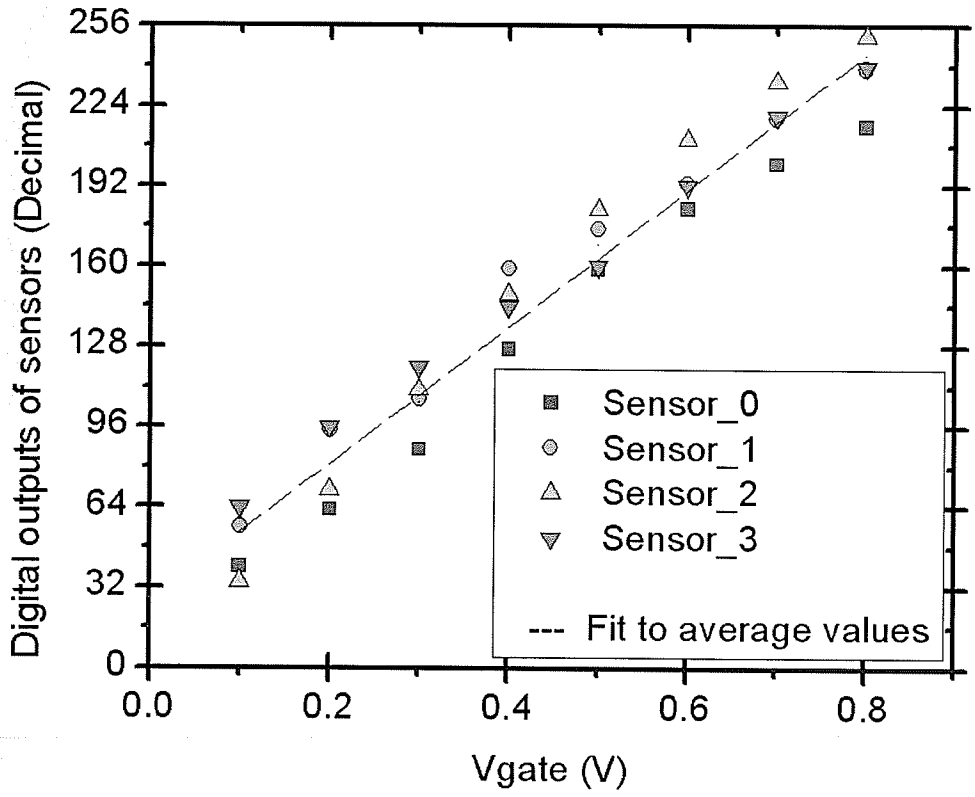


Figure 7-12: The digital outputs of the sensors in a 2×2 array versus the gate voltages

In order to improve the reliability of the sensor data for subsequent signal processing, averaging the outputs of individual sensors within the array would lead to a robust data. The average digital output of the sensors in the 2×2 array is shown in Figure 7-13. The error bars in the figure represent the standard deviation of the output from the array.

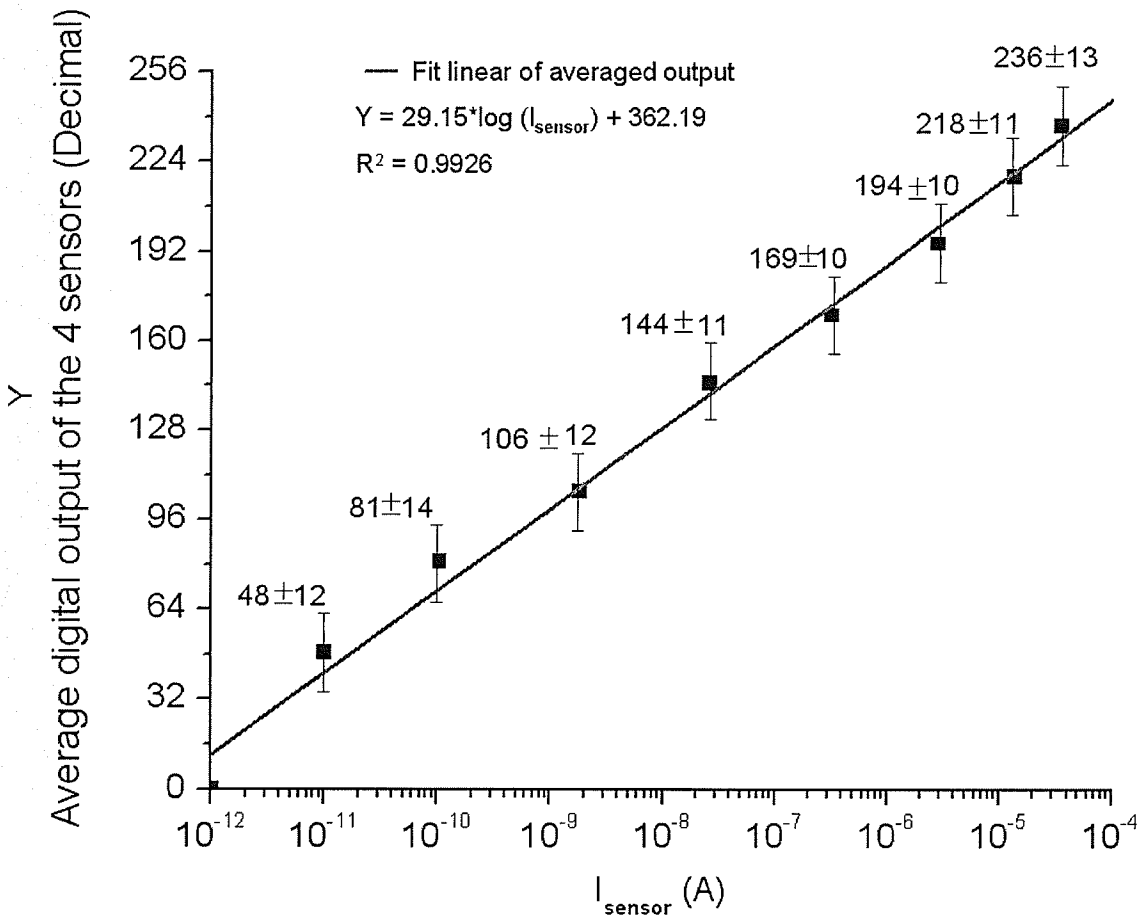


Figure 7-13: The average digital output of the four sensors and the standard deviation versus the sensor current

7.3.3 Cross Talk Experiment for the 2×2 Sensor Array System

To test for cross-talk between the might occur between different sensors, a gate bias, that was applied to a single sensor was changed. The performance of the other sensors was then monitored.

A gate voltage was applied to the sensor (Sensor_3) and was then was suddenly changed from 0.4 V to 0.5 V. With constant gate voltages on the other three sensors, it was found that the variation of the input gate voltage only affected the sensor to which the voltage was changed, and not any of the other sensors. In Table 7-5 (a) these results are shown. To ensure some level of constancy, this experiment was repeated with another sensor where gate bias change was made on another sensor (Sensor_2). The corresponding results are illustrated in Table 7-5 (b). The cross talk experiment verified that the row and column decoders in the digital circuit efficiently routed digital signals to their respective rows and columns and ensured that all sensors functioned independently.

Table 7-5: The cross talk experiment of the 2×2 sensor array system

Table 7-5 (a)

Sensor addressed and read	Input gate voltage V_g (V)	Digital output (Hex)	
		Before V_g change	After V_g change
Sensor_0	0.1	2A	2A
Sensor_1	0.3	6B	6B
Sensor_2	0.6	CE	CF
Sensor_3	Varied from 0.4 to 0.5 V	90	A0

Table 7-5 (b)

Sensor addressed and read	Input gate voltage V_g (V)	Digital output (Hex)	
		Before V_g change	After V_g change
Sensor_0	0.1	2A	2A
Sensor_1	0.3	6B	6C
Sensor_2	Varied from 0.5 to 0.6 V	B2	CE
Sensor_3	0.6	C0	C0

Chapter 8 Conclusions

In this research, an integrated circuit was designed to access and read a prototype 2×2 chemical sensor array. The integrated circuit consisted of a digital array-addressing circuit and an analog output circuit. The digital circuit activated individual row and column lines to access each sensor in the array. The analog output circuit converted the logarithmic sub-threshold sensor current to a voltage signal, and read out the voltage from the sensor.

In order to investigate the feasibility of the integrated circuit design, four pseudo-sensors was used to make up the sensor array. The electrical performance of the pseudo-sensor was simulated using an integrated circuit simulator (*Spectre*). Good agreement between its I_{ds}-V_{gs} curve and that from a previous sensor design [5] showed that the pseudo-sensor was a reasonable substitute of the floating-gate, FET sensor. Simulated results from the integrated circuit demonstrated that the digital array-addressing and the analog output circuits worked properly.

After simulating the integrated circuit, its physical layout was designed and fabricated. Functional testing of the fabricated design verified that the integrated circuit accessed and read each sensor successfully. The experimental V_{out}-I_{sensor} curves from a single sensor confirmed the expected logarithmic relationship between current and output voltage from the sensor. The cross talk experiment demonstrated that the row and column decoders in the digital circuit efficiently routed digital signals to their respective rows and columns. This ensured that all sensors functioned independently. The derivation of the integrated circuit sensitivity as a function of analyte concentration showed that the minimum measurable molecule concentration is dependent upon the capacitance of the

ILD layer between the floating gate and the control gate (area, thickness and permittivity).

The integrated circuit can be extended to operate a system that contains more sensors. For example, the clock frequency was 200 kHz in the current system. The read cycle was 5 μs (1/200 ms) for each sensor. Since the response time of some conducting polymers has been reported to be as short as one millisecond [25], this integrated circuit could operate an array containing a maximum of 200 sensing elements. If the clock frequency is increased to 512 kHz, this integrated circuit could work for an array of 512 (32×16) sensors since the read cycle for each sensor would be 1.953 μs (1/512 ms). For such a 32×16 sensor array, the designer could use a 5-bit row decoder and a 4-bit column decoder. The fundamental approach to design these decoders would then be identical to the one described in Chapter 4.

In a future design for chemical sensing, a differential scheme can be used to detect the chemical reaction. In this case, the active sensors may be accompanied by corresponding reference sensors (insensitive to a given analyte), which can provide a baseline for measurement [2]. The respective output voltages may be sent to a differential amplifier. As such, their voltage difference (indicator of the chemical reaction) can be detected and amplified. Noise and drift that occur over the lifetime of the sensor can also be eliminated through this differential scheme [2]. The amplified voltage difference may then be converted into a digital value that can be stored in an SRAM (memory) for off-chip data analysis. In future on-chip designs, it will be important to protect the integrated circuit from chemicals in the sensing environment. This may be solved by coating the circuit surfaces while exposing sensors to the sensing environment.

In future work, this type of circuit and a much larger floating-gate, FET sensor array could be integrated onto a chip to realize a truer "electronic nose".

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