Application of Genetic Algorithms in Control Design for Advanced Static VAR Compensator at ac/dc Interconnection

by
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A Thesis

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Department of Electrical and Computer Engineering

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APPLICATION OF GENETIC ALGORITHMS IN CONTROL DESIGN

FOR ADVANCED STATIC VAR COMPENSATOR AT ac/dc INTERCONNECTION

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Abstract

Several aspects of design of the Advanced Static VAR Compensator (ASVC), and design of a control system for optimum performance of the ASVC at an ac/dc interconnection are presented in the thesis.

One of the most important aspects of the designing process of the ASVC is reduction of harmonic components in the ASVC output voltage. To meet a requirement regarding the maximum contents of harmonics in the voltage a configuration of the ASVC and the size of its components have to be properly selected. A method based on harmonic analysis has been used to design the ASVC power circuit. The importance of such analysis under both balanced and unbalanced conditions have been identified.

A new design methodology of control systems is proposed here. It relies on a combination of advanced system simulator - $EMTDC^{TM}$ and genetic computation. In contrast with standard approaches used in control systems design, this framework provides realistic full-scale modeling abilities accomplished via the simulator along with the optimization versatility of Genetic Algorithms.

This new methodology has been used to design a control of the ASVC. Using capabilities of genetic computation for multiobjective and multivariable optimization a structure of a control system has been designed and the values of control parameters have been adjusted. A concept of switching control has also been investigated. A fuzzy controlled switching between two sets of parameter values has been used to design an ASVC control for the case of the inverter close-in single phase to ground fault. The results show a better performance of the ASVC when compared to its performance with a standard type of control. A control scheme using different sets of control parameter values in a control procedure, depending on the state of a system, has been used to investigate the performance of the ASVC at an ac/dc interconnection. Using this approach the values of control parameters which are optimal for a given event are used.

Acknowledgments

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Chapter 1

Introduction

1.1 Motivation

The importance ascribed to HVdc transmission in recent years is the result of the technical properties and the economical advantages of HVdc links. Long-distance transmissions, asynchronous ties and power links using long submarine cables are some of the applications of HVdc systems.

It is a well known fact that HVdc converters consume reactive power in the range of 50 to 60 per cent of the real power transmitted at full load. Any changes in the reactive power demand, associated with the changes in dc power, have an effect on the ac voltage at the converter site. An excess of reactive power leads to overvoltages at the ac bus, while a deficit in reactive power leads to undervoltages. The variations in voltage magnitude are more critical in those cases where HVdc links are connected to weak ac systems[1]. The following aspects of ac/dc interactions then become more significant: harmonic instability; transformer core saturation instability; power/voltage instability; recovery from disturbances; overvoltages and harmonic resonances [11]. Some of the difficulties of operation of an HVdc system with a weak ac system can be reduced by the application of dynamic voltage control devices (VCD), such as synchronous condensers or static var compensators (SVC).

In the mid-eighties, the Electric Power Research Institute introduced a concept called

[1] A system is called a weak system when the short circuit ratio (SCR), defined as the ratio of system short circuit level MVA to the dc power MW, is between 2.0 and 3.0 [12]; from the system impedance point of view, SCR is defined as the ac system admittance expressed in per unit of dc power.

Flexible AC Transmission Systems (FACTS). This concept represents a new approach to increase utilization of existing electrical power systems and to an improvement in their flexibility. Development of fast acting, thyristor controlled devices which allow high speed control of system parameters is the subject of many projects within the FACTS framework.

The Advanced SVC (ASVC) is one of the newly developed devices. It is built as a voltage-source inverter with gate turn-off (GTO) thyristors. Compared to its conventional counterpart which employs thyristor-switched capacitors and reactors, the ASVC has several advantages. The most important advantages are related to its ability: to adjust instantaneously the output of reactive power to compensate for voltage variation; to maintain maximum capacitive output current even at greatly reduced system voltage; and to withstand transient overcurrent in both the capacitive and inductive operating regions.

An application of fast acting devices, such as FACTS components and HVdc links in power systems has led to the increased importance of control design processes and a need for electromagnetic control coordination [54]. The complexity and non-linear characteristics of electrical power systems have resulted in the application of analog and digital simulators to support the methods of control synthesis and control analysis. At the same time, in order to design a control which gives behavior of a system close to ideal, the design process should include methods of minimization of some measures which represent a deviation from ideal behavior of the system. Such measures are usually provided by performance indices, whose values indicate how well the actual performance of the system matches the desired one. Design of a control which minimizes the values of performance indices leads to the design of an optimal control. The choice of appropriate performance indices and an optimization technique is an important part of the design process.

Up to now, most of the research related to the Advanced SVC has been focused on an application of the ASVC to improve the loadability of long transmission lines (e.g. [10]). Only one paper [61] investigating the dynamic performance of the ASVC at the HVdc converter station has been published so far with no information about an ASVC control system. An application of the ASVC at an ac/dc interconnection means that complex, non-linear, and fast acting devices – the ASVC and the HVdc converter, have

to cooperate. For this reason, the design of the ASVC and its control system should be carried out in such a way that the whole controlled system, represented as realistically as possible, is considered. Such an approach can lead to the improved performance of ac/dc system, even when an HVdc link is connected to a very weak (SCR< 2.0) receiving ac system.

1.2 Scope of the Thesis

The investigation of dynamic behavior of the ASVC at an ac/dc interconnection and design of an ASVC control are the two main objectives of this thesis. The results of the research conducted are presented in the dissertation in this following order:

- a description of the Advanced Static VAR Compensator, its characteristic, features and some elements of a design process are presented first, different approaches to reduce harmonics generation are described, together with a harmonic-based method for selecting the values of components of 12-pulse ASVC;
- a new control design method for complex systems is presented next, the method is based on the connection of an advanced system simulator ($EMTDC^{TM}$) with a new optimization tool - Genetic Algorithms;
- the design of an optimal control for the ASVC and an investigation of the dynamic performance of the ASVC at an ac/dc interconnection under faulted conditions and overvoltages are presented at the end.

All studies related to the application of the ASVC have been performed using the electromagnetic transient program $EMTDC^{TM}$ [8].

Chapter 2

Description of Advanced Static VAR Compensator (ASVC)

Static VAR Compensators (SVCs) were developed in the late 1960s to provide fast reactive power (VAR) compensation for large, fluctuating industrial loads. They use either thyristor-switched capacitors (TSCs) or a thyristor-controlled reactor (TCR) with fixed capacitor. In the late 1970s, SVCs were successfully used in the dynamic compensation of power systems to provide voltage support, to increase transient stability, and to improve damping. These SVCs require fully rated capacitors and reactors to generate or absorb reactive power, and an electronic switching circuit (thyristor valves). For this reason, current SVCs are large systems which involve a number of major components (transformer, capacitors, reactors, switchgear, thyristor valves) and require a considerable size facility with significant labor installation.

Development of a new generation of thyristors called gate turn-off thyristors (GTO), with power handling levels comparable to conventional thyristors [26], made it possible to design a new type of static VAR compensator. GTO-based converters, which operate as voltage or current sources and which produce reactive power essentially without capacitors or reactors, by circulating energy among the phases of the ac system [18], are basic components of this new device. The SVC, which uses this particular type of solid state switching converter, is called the Advanced Static VAR Compensator (ASVC).

2.1 Basic Operating Principles

The Advanced Static VAR Compensator (ASVC) is a GTO-based power converter connected to the ac system through a series inductance (the transformer leakage). A three-phase output voltage, in phase with the system voltage, is produced by the inverter. By varying the magnitude of this voltage, the reactive power exchange between the ASVC and ac system can be controlled. When the magnitude of the converter output voltage is greater than the system voltage, the ASVC generates reactive (capacitive) power for the system; when the magnitude of the output voltage is lower than the ac system voltage, the ASVC absorbs reactive (inductive) power. When both voltages are equal, the reactive power exchange is zero. Based on this description, it should be noted that the characteristics of ASVC are very similar to those of a rotating synchronous condenser. For this reason, the ASVC has also been named the STATic CONdenser (STATCON) [18].

The basic building block for the ASVC is a voltage source inverter that converts the dc voltage at its input terminals into a three-phase set of output voltages. In its simplest form, it is composed of six GTOs, each of which is shunted by a reverse parallel connected diode. The ASVC with the six-pulse voltage source inverter is illustrated in Figure 2.1, together with a line-to-line output voltage waveform (in practice a waveform such as this would produce unacceptable harmonics, methods of harmonics reduction are presented in chapter 3, page 11). The operation of the ASVC can also be explained by considering the relationship between the output and input powers of the inverter – the net instantaneous power at the ac output terminals must always be equal to the net instantaneous power at the dc input terminals (neglecting the losses in the semiconductor switches). Since the inverter supplies only reactive power, the real input power provided by the dc source (charged capacitor) must be zero. Furthermore, since reactive power on the dc side is zero, the dc capacitor plays no role in the reactive power generation. One could say that the inverter establishes a circulating power exchange among the phases. The need for the dc storage capacity is due to equality of the instantaneous output and input powers. A quasi-squarewave waveform of the output voltage causes fluctuations in the net instantaneous output power, and in order not to violate the equality of the instantaneous output and input powers, the inverter must draw a fluctuating ("ripple")

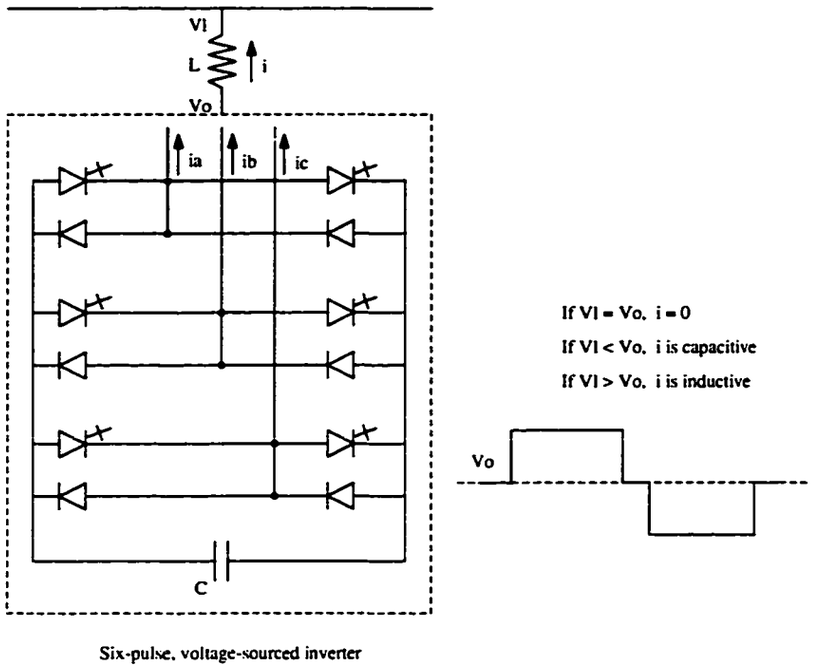


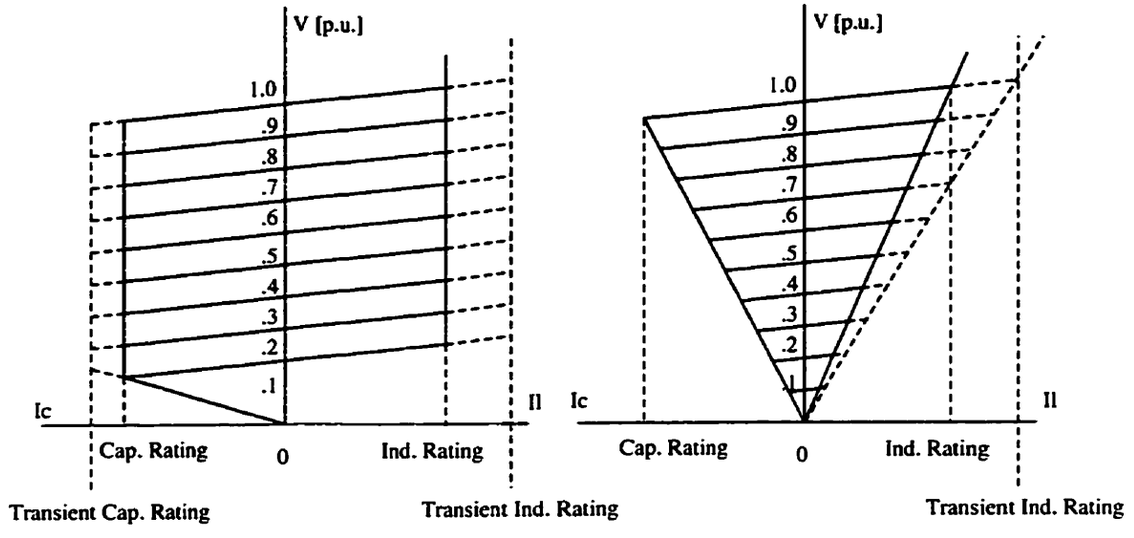
Figure 2.1: Six-pulse voltage source inverter and line-to-line output voltage.

current from the dc storage capacitor (a form of this current depends on the converter output voltage waveform, section 3.3, page 18).

In a practical ASVC, the semiconductor switches of the inverter are not without loss. To replenish these losses and to keep the capacitor voltage at the desired level the output voltage has to lag the ac system voltage by a small angle. This allows the inverter to absorb a small amount of real power from the system. The same mechanism is used to increase or decrease the capacitor voltage, which results in changes of magnitude of the inverter output voltage. In this way the var generation or absorption is controlled.

2.2 Operating Characteristic, Features

The nature of ASVC operation results in natural and instant adjustments of the reactive power output to compensate for system voltage variations. The superior operating characteristics of the ASVC are illustrated in the system voltage versus the reactive output current (V–I) characteristic, Figure 2.2. In contrast to a conventional thyristor-



(a) Advanced SVC (b) Conventional SVC

Figure 2.2: V-I characteristic of (a) the advanced SVC and (b) its conventional counterpart.

controlled compensator, the ASVC is capable of supplying full capacitive current under reduced voltage conditions. It also has transient overload capability in both inductive and capacitive regions. The maximum attainable transient over-current in the capacitive region is determined by the maximum current turn-off capability of the GTO devices. In the inductive region the GTOs are naturally commutated and the current can theoretically be raised above the GTO maximum turn-off level. In both cases, the overload is dictated by the need to keep the junction temperatures of the power semiconductors below their allowable limits.

In addition to superior controllability, the ASVC is able to store energy which gives interesting opportunities for the improvement of system securities. Unbalanced control is also possible – negative-sequence voltage can be produced with a controlled amplitude and phase to achieve the desired performance objective. Harmonics of GTO-based compensator are expected to be lower than for SVC of comparable ratings (method of harmonics reduction are presented in chapter 3, page 11).

On the other hand, the ability to deliver rated current at off-nominal voltage is the

primary feature which makes the ASVC similar to a synchronous condenser in performance [26]. Creation of a controlled voltage with low distortion, the ability to obtain an inertia-like response (inclusion of some energy storage with the ASVC), and overload capability (although the synchronous condenser is generally superior in magnitude and duration) are additional similarities between these two devices. In addition, the ASVC possesses several advantages compared with a synchronous condenser: fast response, lower fault current, the ability to store energy, the ability to provide an unbalanced control (up to some degree), smaller size and lower maintenance and installation costs.

2.3 Elements of Design

In power system applications of the ASVC, the six-pulse voltage source inverter considered so far would not meet requirements for power rating, as well as for harmonics contents either in the output voltage or the input capacitor current. To overcome these drawbacks, some choices have to be made regarding the structure of the ASVC and the size of its components. Problems and solutions of power rating requirement are presented below, and approaches used for harmonics reduction are presented in detail in chapter 3, page 11.

The ASVC with several voltage source inverters has to be used together with a series connection of GTOs in the arms of inverters to obtain the power ratings typically required for high power applications. Simple inverters, such as the one presented in Figure 2.1, or complex ones, such as a multi-level inverter, can be used as the building blocks of the ASVC. Application of multi-level inverter increases the power rating compared to the simple (2-level) inverter. For example, a 3-level voltage source inverter allows the dc voltage level to double and therefore doubles the power rating. A simple description of a multi-level voltage source inverter and its benefits regarding harmonics reduction are presented in chapter 3. In order to design the ASVC with few inverters using presently available GTO thyristors of limited current rating, the inverters must be operated at relatively high dc voltage. This necessitates the connection of a relatively large number of GTO thyristors in series to form a valve for the inverter. For successful operation of a GTO thyristor valve, the voltage distribution in the series stack must be maintained to such a degree that the maximum instantaneous voltage across any single device does not

exceed the rated voltage under any condition. The different transient voltage stresses would occur due to the differences in the switching characteristics of individual GTO thyristors. It is especially seen during the turn–off process. This process is characterized by three times: *storage time* (the period during which the charge is being swept out of the gate-cathode junction with no noticeable effect on the anode current); *fall time* (the period during which the anode current decreases, very rapidly, to about 10 per cent of its peak value); and *tail time* (the period during which the GTO thyristor is blocking anode voltage with slowly decreasing anode current due to recombination of trapped charge in the device). Inequalities in these times (especially in *storage time* which is in the range of 15–23 μs) of the individual devices in the valve result in different voltage stresses. Three different solutions are proposed to handle this problem – selection of devices, intelligent turn-off control, and optimized gate-currents [56].

Some problems of ASVC design, such as power rating and harmonics reduction, can be solved with the help of well-known methods used for solving similar problems in related areas (e.g. application of thyristors in HVdc systems, motor drive application of voltage source inverters). On the other hand, the ASVC is a new device and its behavior in a power system environment needs further investigation, which may result in some new solutions to the control and/or structure of ASVC.

One aspect which needs further research is a control algorithm. So far in most cases (except [24] where PWM technique is used, see section 3.1, page 11), only one control parameter is used to control the amount of reactive power the ASVC generates or absorbs. It is the phase angle of the power inverter voltage in reference to the ac system voltage. There are already two problems with the dynamic behavior of the system, which do not seem to be sufficiently manageable with this control algorithm [56]:

- the reactance on the ac side and the capacitor on the dc side give the system a low damped resonance behavior; occurrence of fast events in the the power system, e.g. load step, stimulate oscillations in line currents and dc voltage, which can lead to overcurrent or overvoltage faults;

- asymmetry in the power system causes strongly asymmetrical line currents and

because of the close coupling of the three phases through the dc circuit, it is not possible to control the phase currents separately.

In consideration of these problems, a second control parameter seems desirable. While the phase angle of output inverter voltage is well suited to control the power flow between the ac and dc sides, a variable modulation index (one of the parameters of PWM operation mode of inverter, see section 3.1, page 11) would help react to variations of amplitude and asymmetry.

A very interesting approach to extend a control of the ASVC is presented in [56] where a 3–level voltage source inverter is used as a building block of the ASVC. The parameter β (see section 3.2.1, page 14), which is normally used to minimize certain harmonics, could represent the second control parameter to handle dynamic problems of the ASVC. During periods of fast action in the power system, the β parameter could be used to improve the dynamic behavior of the ASVC.

Another aspect of ASVC design which needs further investigation is related to the selection process of the dc capacitor value. Besides such objectives as ripple in direct voltage and performance requirements under unbalanced conditions (see section 3.3, page 18), resonance behavior has to be taken into account [7].

Chapter 3

Harmonics Reduction Methods for ASVC

Reduction of harmonic components in the output current and the dc voltage is one of the most important aspects of ASVC design. To obtained a desired level of harmonics in ac current and dc voltage three elements have to be considered in the designing process:

- the firing sequence of GTOs;
- the structure of a GTO-based power converter;
- the selection of power circuit components.

All three design aspects are presented in the sections which follow.

3.1 GTO Firing Sequence

The six–pulse voltage source inverter can produce a set of three quasi–square voltage waveforms of a given frequency by connecting the capacitor sequentially to the three output terminals via the appropriate inverter switches (GTOs). When considering the switching frequency of GTO (that is the frequency of connecting the capacitor to the output terminal), two modes of operation can be distinguished:

- *Fundamental Frequency Modulation* (FFM) – every GTO is turned on and off once during each fundamental period;

- *PulseWidth Modulation* (PWM) – GTOs are turned on and off several times during each fundamental period [1].

FFM mode means the lowest switching frequency and therefore losses in the voltage source inverter with this switching are minimal. Unfortunately in the spectrum of output voltage the low-order harmonics (5th, 7th, 11th, 13th,...) appear with large amplitudes. To reduce harmonic contents other methods have to be used such as the selection of ASVC configuration (section 3.2, page 13) or the choice of size of ASVC components (section 3.3, page 18).

In the case of PWM technique the switching frequency is high. Application of this mode in a power converter with high power GTOs, which have limitations in the switching frequency, causes increased losses in the GTO devices and their snubber circuits. This mode, however, gives very good results in reducing low-order harmonics (PWM "shifts" energy from the low to high frequency range – high-frequency harmonic components are generated). There are many ways to generate the switching function. Some of these are improved versions of the original sine PWM technique (e.g. the modified sine PWM, the third-harmonic injection PWM, the harmonic injection PWM [2]), while other ones are called programmed PWM techniques [34], [35]. The latter are recommended for reactive power compensation applications. They offer better voltage utilization, as well as lower switching frequencies. Using the programmed PWM technique a selected number of harmonics can be eliminated.

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[1] PWM technique means that a train of constant amplitude pulses is produced by switching the output on and off rapidly a number of times during each half-period. Control of the amplitude of the inverter output voltage, together with reduction in harmonics is obtained by varying the pulse widths in a cyclic manner for a constant number of pulses per half-period. A proper switching sequence for all GTOs in the inverter (the valves of the same phase operate in the complementary manner: the upper is ON when the lower is OFF, and vice-versa) is obtained using different methods which are more or less similar to the method used in the original Sinusoidal PWM technique. In the case of the original PWM a sine wave of the same frequency as the inverter output – $S_m(t)$ (called a modulating signal) is compared with a synchronized triangular carrier signal – $S_c(t)$. The triggering of the valves is based on the relationship of these signals, and is described by the switching function – $S_s(t)$ which takes on either of two values:

$$S_s(t) = +1 \qquad for \quad S_m(t) > S_c(t) \tag{3.1}$$

$$S_s(t) = -1 \qquad for \quad S_m(t) < S_c(t) \tag{3.2}$$

The ratio of the amplitude of the modulating signal $S_m(t)$ to the amplitude of the triangular carrier signal $S_c(t)$ is defined as the modulation index.

Despite the fact that large GTOs cause considerable switching losses, the application of PWM strategy for inverters in a high-power area seems justifiable. Several approaches have been proposed to reduce losses caused by the high frequency of switching: namely the application of minimum–loss vector based PWM [51], the modification of the original PWM [55], the special arrangement of inverters [58], [47], or specially designed snubber circuits [1], [22]. Moreover, further developments in power electronics technology suggest that PWM techniques may be within the range of high power applications.

A very interesting approach, which is worth mentioning at this point, is presented in [58]. In this concept, a power converter acts as a special matrix of identical voltage source inverters with the PWM technique. Then by phase-shifting of the switching instances of the valves in the different inverters, the effect of very high frequency switching is created even though the switching rate of the individual valve is low. The switching losses can then be kept at a low level using presently available GTOs.

A dynamic behavior of the ASVC with the PWM technique is investigated in [25]. Using this technique, a static var compensator could be controlled very quickly without any changes in the dc voltage.

A confirmation that the PWM technique will find its application in power systems is a 50MVA Self-Commutated SVC developed by the Tokyo Electric Power Company and Toshiba Corporation [24]. It uses the world's largest GTOs (6kV, 2.5kA) and the PWM technique. The switching frequency is 150Hz and the phases of the four voltage source inverters (it is a multi-pulse configuration, see section 3.2.2, page 16), are displaced to reduce harmonics.

3.2 Structure of GTO-based Power Converters

The output voltage and input current of the six-pulse voltage source inverter contain harmonic components with frequencies of $(6k \pm 1)f$ and $6kf$ respectively (f is the fundamental output frequency and $k = 1, 2, 3, ...$). The ASVC with a single six-pulse inverter as a power converter would produce the output voltage with an unacceptable contents of harmonics. In order to eliminate and/or attenuate some of them, a special connection of several inverters and/or different structure of the inverter has to be used. In order to reduce harmonics contents a number of solutions are proposed.

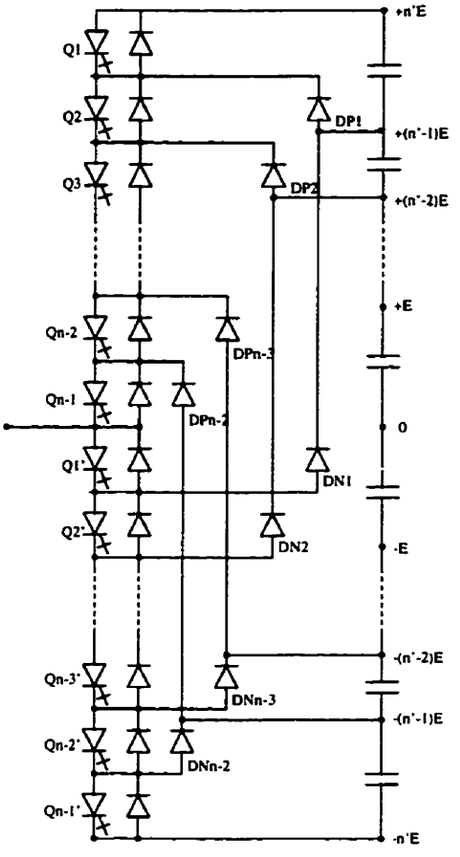


Figure 3.1: One phase of a multi-level GTO inverter.

3.2.1 Multi–level Inverter

One of the interesting approaches to reduction of harmonic components, which also presents promising solutions for some control problems, is a multi-level inverter. It represents a special kind of series connection of devices. A generalized structure of one phase of an n-level GTO inverter is shown in Figure 3.1, where $n' = (n-1)/2$. The advantage of this structure is that the GTOs have to block only the voltage of its own level and not the full dc voltage.

The lower group of GTO thyristors requires the complementary gating pulses of the upper group of the same number. That is, if Q_2 is on, then Q_2' must be off. It should be mentioned that for each voltage step, only one thyristor needs to turn on and one

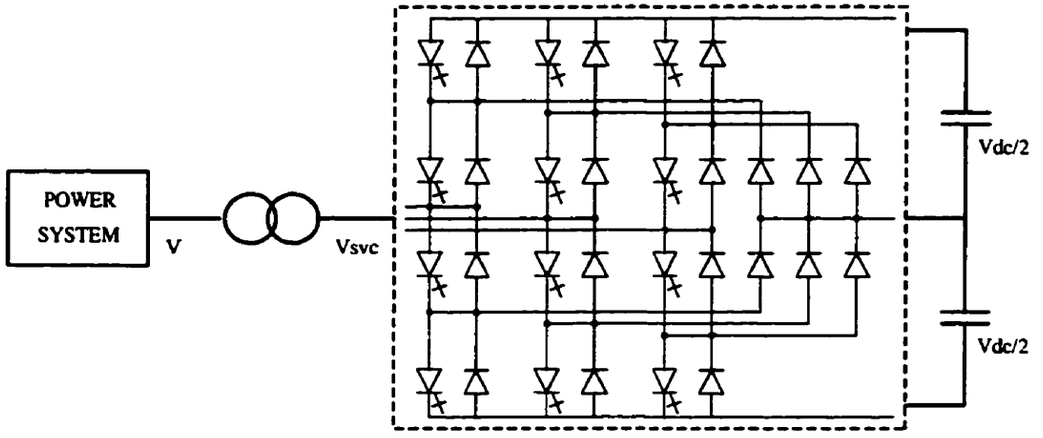


Figure 3.2: 3-level inverter.

thyristor needs to turn off. For example, if Q_1 is off and Q_2, Q_3, ... Q_{n-1} and Q'_1 are on, then the terminal $+(n'-1)E$ is connected to the output terminal through DP_1, Q_2, Q_3, ... Q_{n-1}. The correct switching logic is necessary in order to obtain the various output voltage levels.

The advantages of the multi-level voltage source inverter can be illustrated by using the relatively simple 3-level voltage source inverter shown in Figure 3.2. The clamping diodes to the middle point of the dc-circuit guarantee that every GTO has to block only half the dc voltage which doubles the power rating compared to a 2-level inverter. Reduction of harmonics and the extended features for controlling the inverter voltage make the 3-level inverter very attractive. Figure 3.3 shows that even with FFM, the amplitude of voltage is variable without changing the dc voltage. During the interval β the phase-voltage is connected to the middle point of the dc circuit. For symmetry reasons all three inverter legs have to be run with the same β. With increasing β the fundamental component of voltage becomes smaller, harmonic components also depend on the β value:

$$V_{n=1} = \frac{\sqrt{2}V_{dc}}{\pi} cos(\beta) \tag{3.3}$$

$$V_{n>1} = \frac{\sqrt{2}V_{dc}}{n\pi} cos(n\beta) \qquad n = 5, 7, 11, 13, ... \tag{3.4}$$

Full modulation ($\beta = 0$) means identical waveforms and harmonics with a 2-level

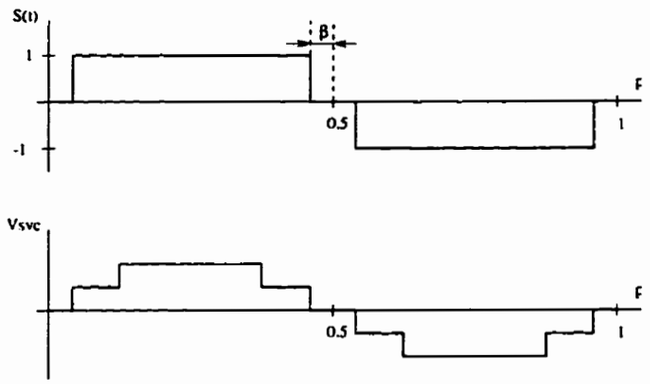


Figure 3.3: FFM with 3-level inverter.

(six-pulse) voltage source inverter.

The parameter β can be used to counteract either one of two of the special problems:

- minimization of certain harmonics, in this case the value of β is chosen to reduce specific harmonics and is kept the same all the time, for example $\beta = \pi/12$ results in reduction (to 25 per cent compared to full modulation) of the 5th and 7th harmonics and the 17th and 19th, 29th and 31th etc. are minimized as well.
- dynamic problems of ASVC: in this case β represents the desired second control parameter (section 2.3, page 8).

3.2.2 Multi–pulse Converter

The most popular method of harmonic elimination is high–pulse operation of the ASVC. This can be achieved by application of several voltage source inverters connected together through a transformer with separated secondary windings. Any kind of voltage inverters, 2- or multi-level ones, with FFM or PWM techniques (see section 3.1, page 11), can be used as the building blocks of such ASVC. In all practical realizations of the ASVC described in the literature so far, 2-level (six-pulse) voltage source inverters with FFM are used (for the only case of inverter with PWM see section 3.1). Application of multi-level inverters is still considered to be at the theoretical level [56], [60].

In the case of a general P-pulse converter composed of n FFM inverters ($P = 6n, n = 1, 2, 3, ...$), the frequencies of the harmonics present in the output voltage and input

current are $(Pk \pm 1)f$ and Pkf respectively, that is the harmonic spectrum improves with increasing pulse number. All n six–pulse inverters are operated from a common dc source with a successive $2\pi/6n$ phase–displacement. Each of the generated output voltage waveforms is shifted by a transformer with an appropriate secondary winding configuration to cancel the phase–displacement of the inverter. A somewhat different secondary winding configuration is required for each inverter, which makes this solution unattractive from both design and application viewpoints. The transformed outputs of all inverters are summed by the series connection of all corresponding primary windings. Several examples of ASVCs with multi-pulse converter can be found in the literature:

- a 36-pulse converter, with 10 degrees phase displacement between voltages, was developed as the first ASVC [48];
- a 48-pulse converter system was developed in [32]; in this case, the phase-displacement is 7.5 degrees, and a special multiple transformer was designed;
- an 18-pulse converter, 20 degrees of phase-displacement, was used in [52], the secondary windings of the nine single-phase transformers were connected in a zig-zag manner;
- a 12-pulse configuration with a displacement of 30 degrees was used in 1 MVA ASVC prototype [6]; a phase-shifting transformer was used as an output transformer;
- a 48-pulse configuration is used in the first large ASVC in USA rated at 100MVA; it was installed at the Tennessee Valley Authority [44], [45].

An interesting approach is presented in [18]. A "quasi" multi–pulse configuration using transformers with customary wye to wye and wye to delta windings is proposed. In this case, identical 12-pulse modules are used as building blocks. Each module incorporates two six-pulse voltage source inverters, one operated from a wye to wye transformer, and the other from a wye to delta transformer. The inverters in the 12-pulse module operate with $\pi/6$ phase-displacement. In general a quasi $12m$-pulse arrangement can be built, where $m = 1, 2, 3, ...$ means a number of 12-pulse modules. In this case each 12-pulse

module operates with a successive $\pi/6m$ phase-displacement and the corresponding primary windings of all transformers are connected in series.

3.3 Power Circuit Design

Harmonic distortions of dc voltage and output ac current depend on the values of the dc capacitor and the leakage inductance of the coupled transformer. A proper selection of these values can reduce harmonic components to the desired level. The method developed by Moran [29] can be used to design ASVC components according to the maximum possible contents of harmonics. The original version of the method can be applied to design components of the ASVC which is built using a single 2-level voltage source inverter with PWM or FFM switching technique. The extension of the method for a twelve-pulse ASVC is proposed. The original method and its extension are presented first, and the results of application of these methods are shown next.

3.3.1 Harmonic Based Method for Power Circuit Design

Determination of the values of inductance and capacitance is based on the requirement that given maximum harmonic distortions of ac output current and of dc voltage will not be exceeded. The following assumptions are made:

- that ac voltages are balanced,
- that switching elements are ideal,
- that dc voltage V_{dc} is ripple-free,
- that the phase values of voltage – V_{an} and fundamental component of output current – I_{a1} are assumed as 1 p.u.

Design of X_l

The total harmonic distortion in the output ac current – TDH_i is given by:

$$THD_i = \frac{\{\sum_{k>1}^{\infty} I_{ak}^2\}^{\frac{1}{2}}}{I_{a1}}. \tag{3.5}$$

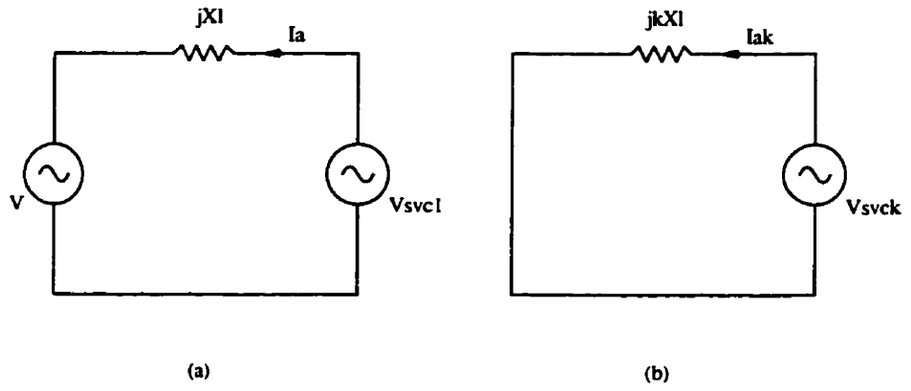


Figure 3.4: An analytical model of the ASVC and ac system for leading var compensation (a) single phase equivalent at fundamental frequency and (b) single phase equivalent for harmonics.

According to the equivalent circuit of the ASVC connected to the ac system for *kth* harmonic, Figure 3.4, one can write:

$$I_{ak} = \frac{V_{SVCk}}{kX_l}, \tag{3.6}$$

and finally

$$X_l = \frac{1}{THD_i\ I_{a1}} \{\sum_{k>1}^{\infty} (\frac{V_{SVCk}}{k})^2\}^{\frac{1}{2}}. \tag{3.7}$$

Harmonic components of the inverter output voltage V_{SVCk} can be calculated using the Fourier series expansion of switching function $S(\omega t)$ of the inverter:

$$S(\omega t) = \sum_{k=1} A_k sin(k\omega t), \tag{3.8}$$

then

$$V_{SVCk}(\omega t) = S(\omega t) * V_{dc} \tag{3.9}$$

and

$$V_{SVCk} = \frac{V_{dc}}{\sqrt{2}}\ A_k. \tag{3.10}$$

Now, the expression for X_l is:

$$X_l = \frac{V_{dc}}{\sqrt{2}\, THD_i\, I_{a1}} \{\sum_{k>1}^{\infty} (\frac{A_k}{k})^2\}^{\frac{1}{2}}. \tag{3.11}$$

The determination of X_l should be done for the worst operating condition of the ASVC. This occurs when the ASVC is supplying rated leading reactive power. Assuming $\sigma = 0$, where σ is the angle shift between V_{an} and V_{SVC1}, one can write:

$$Q_{ASVC_{1\phi}} = \frac{V_{an}\ (V_{SVC1} - V_{an})}{X_l} = \frac{V_{an}\ \Delta V}{X_l}, \tag{3.12}$$

and the value of V_{dc} for the ASVC in leading operation condition is:

$$V_{dc_{lead}} = \frac{\sqrt{2}}{A_1} (V_{an} + \frac{Q_{ASVC_{1\phi}}\ X_l}{V_{an}}). \tag{3.13}$$

The final equation for X_l calculation is presented below:

$$X_l = \frac{V_{an}\ \{\sum_{k>1}^{\infty} (\frac{A_k}{k})^2\}^{\frac{1}{2}}}{A_1\ THD_i\ I_{a1} - \frac{Q_{ASVC_{1\phi}}}{V_{an}}\ \{\sum_{k>1}^{\infty} (\frac{A_k}{k})^2\}^{\frac{1}{2}}}. \tag{3.14}$$

Subtraction in the denominator of equation 3.14 means that there is a limit, for given switching function, in the minimum value of harmonic distortion THD_i. For the phase values of voltage – V_{an} and the fundamental component of output current – I_{a1} equal to 1 p.u.:

$$THD_i > \frac{\{\sum_{k>1}^{\infty} (\frac{A_k}{k})^2\}^{\frac{1}{2}}}{A_1} \tag{3.15}$$

Design of X_c

The value of X_c can be evaluated based on the constraint that harmonic components of dc voltage, ripple factor – K_v, will not exceed a given value. According to the expression:

$$K_v = \frac{\{\sum_{k>1}^{\infty} (V_{dck})^2\}^{\frac{1}{2}}}{V_{dc}}, \tag{3.16}$$

where

$$V_{dck} = \frac{X_c}{k} I_{dck}, \tag{3.17}$$

and I_{dck} is the RMS value of kth harmonic current component through the dc capacitor, the final expression for X_c is:

$$X_c = \frac{K_v \; V_{dc}}{\{\sum_{k>1}^{\infty}(\frac{I_{dck}}{k})^2\}^{\frac{1}{2}}} \tag{3.18}$$

The calculation of X_c should also be carried out for the worst operating condition of the ASVC. This case occurs when the ASVC is in the operation of supplying the lagging reactive power. The value of V_{dc} is then minimal. Finally, the formula for X_c, with the value of $dV_{dc} = \frac{\sqrt{2}\; Q_{SVC_{1\phi}}\; X_l}{A_1\; V_{an}}$ can be rewritten in the form:

$$X_c = \frac{K_v \; (V_{dc} - \frac{\sqrt{2}\; Q_{ASVC_{1\phi}}\; X_l}{A_1\; V_{an}})}{\{\sum_{k>1}^{\infty}(\frac{I_{dck}}{k})^2\}^{\frac{1}{2}}} = \frac{K_v \; \frac{\sqrt{2}}{A_1} \; (V_{an} - \frac{Q_{ASVC_{1\phi}}\; X_l}{V_{an}})}{\{\sum_{k>1}^{\infty}(\frac{I_{dck}}{k})^2\}^{\frac{1}{2}}}. \tag{3.19}$$

The current across the dc capacitor $I_{dc}(\omega t)$ is given by equation:

$$I_{dc}(\omega t) = I_a(\omega t)\; S(\omega t) + I_b(\omega t)\; S(\omega t - 120) + I_c(\omega t)\; S(\omega t + 120) \tag{3.20}$$

where

$$I_a(\omega t) = I_a \; sin(\omega t - \phi) \tag{3.21}$$

$$I_b(\omega t) = I_b \; sin(\omega t - 120^\circ - \phi) \tag{3.22}$$

$$I_c(\omega t) = I_c \; sin(\omega t + 120^\circ - \phi) \tag{3.23}$$

The values of I_{dck} can be obtained analytically by solving the above equation or using computer-aided Fourier Analysis.

3.3.2 Extensions to the Original Method

To use the method presented for design components of 12-pulse ASVC, some modifications are needed in the equations for X_l (equation 3.14) and X_c (equation 3.19). Application of two transformers, wye to wye and wye to delta rated $S_{T_{small}}$, $V_{LL_{small}}$, introduces some changes in the expressions for V_{SVCk} and I_{dck}. In this case the expression for $V_{dc_{lead}}$ is given by:

$$V_{dc_{lead}} = \frac{1}{\sqrt{2}\ A_1}\ (V_{an} + \frac{Q_{ASVC_{1\phi}}\ X_l}{V_{an}}), \tag{3.24}$$

then

$$X_{l_{total}} = \frac{V_{an}\ \{\sum_{k>1}^{\infty}(\frac{A_k}{k})^2\}^{\frac{1}{2}}}{2\ A_1\ THD_i\ I_{a1} - \frac{Q_{ASVC_{1\phi}}}{V_{an}}\ \{\sum_{k>1}^{\infty}(\frac{A_k}{k})^2\}^{\frac{1}{2}}}, \tag{3.25}$$

where $X_{l_{total}}$ is the leakage reactance of the fictitious "big" transformer (rated $S_{T_{big}}$, $V_{LL_{big}}$). The value of X_l for each of the "small" transformers is:

$$X_{l_{small}} = \frac{X_{l_{total}}}{2}\ (\frac{V_{LL_{big}}}{V_{LL_{small}}})^2\ \frac{S_{T_{small}}}{S_{T_{big}}} \tag{3.26}$$

The lower limit of the maximum harmonic distortion in the case of 12-pulse ASVC is:

$$THD_i > \frac{\{\sum_{k>1}^{\infty}(\frac{A_k}{k})^2\}^{\frac{1}{2}}}{2\ A_1} \tag{3.27}$$

The value of X_c is evaluated using the expression:

$$X_c = \frac{\frac{K_v}{\sqrt{2}\ A_1}\ (V_{an} - \frac{Q_{ASVC_{1\phi}}\ X_l}{V_{an}})}{\{\sum_{k>1}^{\infty}(\frac{I_{dck}}{k})^2\}^{\frac{1}{2}}}. \tag{3.28}$$

The values of I_{dck} are calculated from the equation:

$$I_{dc}(\omega t) = I_a(\omega t)\ S(\omega t) + I_b(\omega t)\ S(\omega t - 120) + I_c(\omega t)\ S(\omega t + 120) +$$

$$I_a(\omega t - 30)\ S(\omega t - 30) + I_b(\omega t - 30)\ S(\omega t - 150) + I_c(\omega t - 30)\ S(\omega t + 90) \quad (3.29)$$

where:

$$I_a(\omega t) = I_a\ sin(\omega t - \phi) \quad (3.30)$$

$$I_b(\omega t) = I_b\ sint(\omega t - 120° - \phi) \quad (3.31)$$

$$I_c(\omega t) = I_c\ sin(\omega t + 120° - \phi) \quad (3.32)$$

3.3.3 Application of the Power Circuit Design Methods

The methods presented for calculating the capacitance and inductance values for different ASVCs (with PWM inverter, FFM inverter, and 12-pulse inverter) have been implemented as computer programs. Computer-aided analysis is used for calculating the harmonic components V_{SVCk} and I_{dck} (equations 3.9 and 3.20, 3.29 respectively). It is done with an application of Discrete Fourier Transform (DFT) using the following approach.

Having a switching function of the inverter $S(\omega t)$ expressed in terms of its Fourier series components, the Fourier series expression for the output voltage $V_{SVCk}(\omega t)$ is calculated from the product:

$$V_{SVCk}(\omega t) = S(\omega t) * V_{dc}, \quad (3.33)$$

In the same way the Fourier series expression for the inverter input current $I_{dck}(\omega t)$ is obtained:

$$I_{dck}(\omega t) = S(\omega t) * I(\omega t). \quad (3.34)$$

The formulas 3.14, 3.19, 3.25, 3.28 and the values of V_{SVCk} and I_{Idck} are used to perform the final calculations.

Two computer programs have been written: **pwm_ffm** – to calculate the values of X_l and X_c of the ASVC with one Sinusoidal PWM or FFM inverter, and **mpulse** – to design the 12-pulse ASVC elements. The following data are needed for the programs:

- rated voltage – $V_{LL,RMS}$;
- rated value of three phase reactive power of the ASVC – $Q_{ASVC_{3\phi}}$;

- ac frequency;
- carrier frequency ratio (only for **pwm_ffm**);
- modulation index (only for **pwm_ffm**);
- required maximum current harmonic distortion – THD_i;
- required maximum dc voltage harmonic distortion – K_v.

The following resulting data are obtained:

- coupling transformer leakage reactance – X_l;
- reactance – X_c, and capacitance – C of dc capacitor;
- dc voltage across the capacitor when ASVC does not supply any reactive power – V_{dc};
- change in dc voltage which occurs when ASVC supplies rated reactive power – dV_{dc};
- data files which contain discrete values of line–to–line output voltage and inverter input dc current.

The original and the modified methods for determination of ASVC components have been verified. The models of three different ASVCs: with an FFM voltage source inverter, with a PWM voltage source inverter, and with a 12-pulse ASVC, have been developed with the $EMTDC^{TM}$ program. The simulation results confirm the analytical approach to designing ASVC components according to the maximum possible contents of harmonics in ac output current and dc voltage [40].

The programs presented can be used, after a few modification, to calculate the values of ASVC power circuit components in the presence of unbalanced conditions. Assuming unbalanced ac currents $I_a(\omega t)$, $I_b(\omega t)$ and $I_c(\omega t)$ calculations of the capacitance value C can be performed and discrete values of inverter input dc current can be obtained using the current version of the programs. As an illustration of this analysis and the influence of unbalanced condition on the size of the capacitance C, an investigation is

carried out when one conductor of a three-phase line is open. The ac currents in each phase are assumed as: $I_a = 1p.u.$, $I_b = -I_a$ and $I_c = 0$. Analysis of the input dc current under unbalanced conditions is performed for the ASVC with a PWM inverter (ac frequency – 50Hz, modulation index – 1.0, carrier frequency ratio – 36 /switching frequency – 1800Hz/) and the ASVC with a 12-pulse inverter structure. The results are presented in Figures 3.5 and 3.6 respectively (it can be seen that ripples in the dc current depend on the structure of the ASVC and a switching technique – section 2.1, page 5). Both ASVCs are designed with required maximum harmonic distortions $THD_i = 0.05$, $K_v = 0.05$. They are rated $Q_{ASVC_{3\phi}} = 100MVA$ and $V_{LL,RMS} = 100kV$. The following data have been obtained:

	with PWM inverter	with 12-pulse converter structure
V_{dc}	163.37 kV	64.11 kV
dV_{dc}	59.22 kV	7.56 kV
X_l	0.36 pu	0.12 pu

In the case of capacitance values, the data are presented separately for balanced and unbalanced conditions:

	balanced conditions	unbalanced conditions
with PWM inverter	5.02 μF	108.39 μF
with 12-pulse converter	25.52 μF	487.82 μF.

An analysis of the ASVC under unbalanced conditions is a very important part of the design process. These conditions influence the behavior of the ASVC during ac system faults [31], [56]. The unbalanced input current generates harmonic components in the dc current. It can be seen in Figures 3.5 (e), (f) and 3.6 (e),(f). Based on the equation for the dc current:

$$\begin{aligned} I_{dc}(\omega t) \;:=\; & I_a\, sin(\omega t - \phi_a) + \sum_{k=1} A_k sin(k\omega t) \\ & I_b\, sin(\omega t - 120^\circ - \phi_b) + \sum_{k=1} A_k sin(k\omega t - 120) \\ & I_c\, sin(\omega t + 120^\circ - \phi_c) + \sum_{k=1} A_k sin(k\omega t + 120). \end{aligned} \tag{3.35}$$

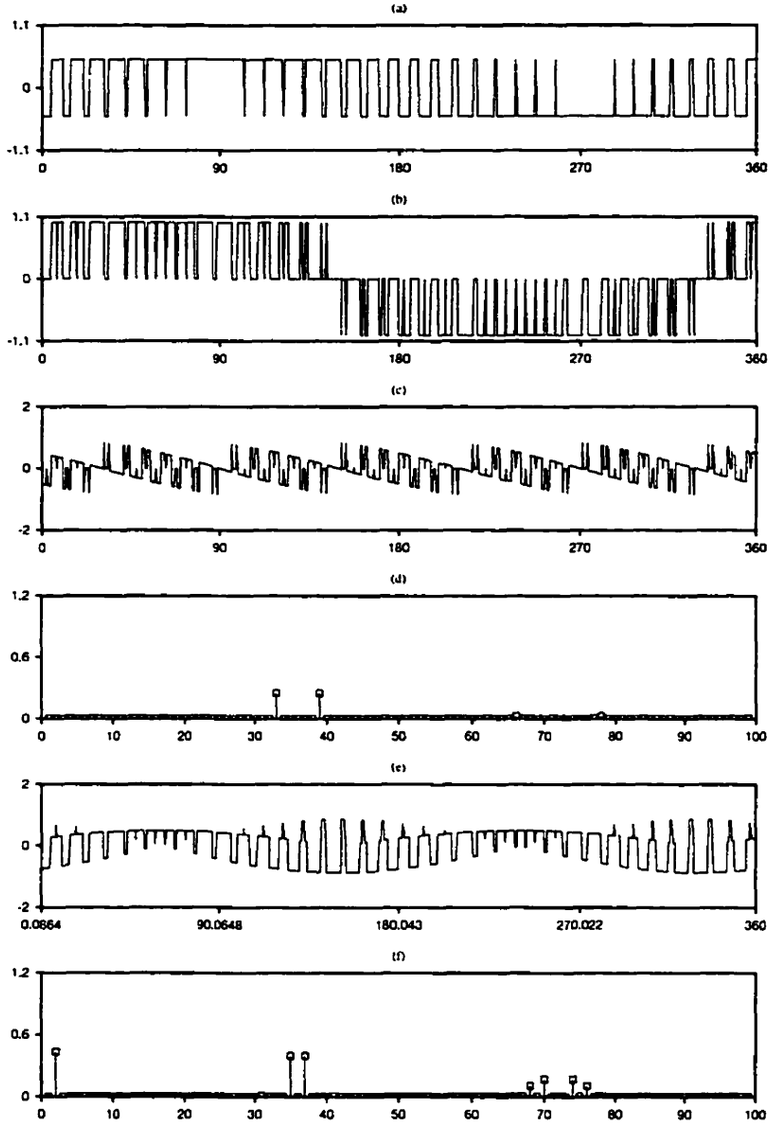


Figure 3.5: ASVC with PWM inverter suppling leading reactive current: (a) switching function phase waveform, (b) output line–to–line voltage waveform, (c) inverter input dc current waveform, (d) inverter input dc current spectrum, (e) inverter input dc current waveform under unbalanced conditions, (f) inverter input dc current spectrum under unbalanced conditions.

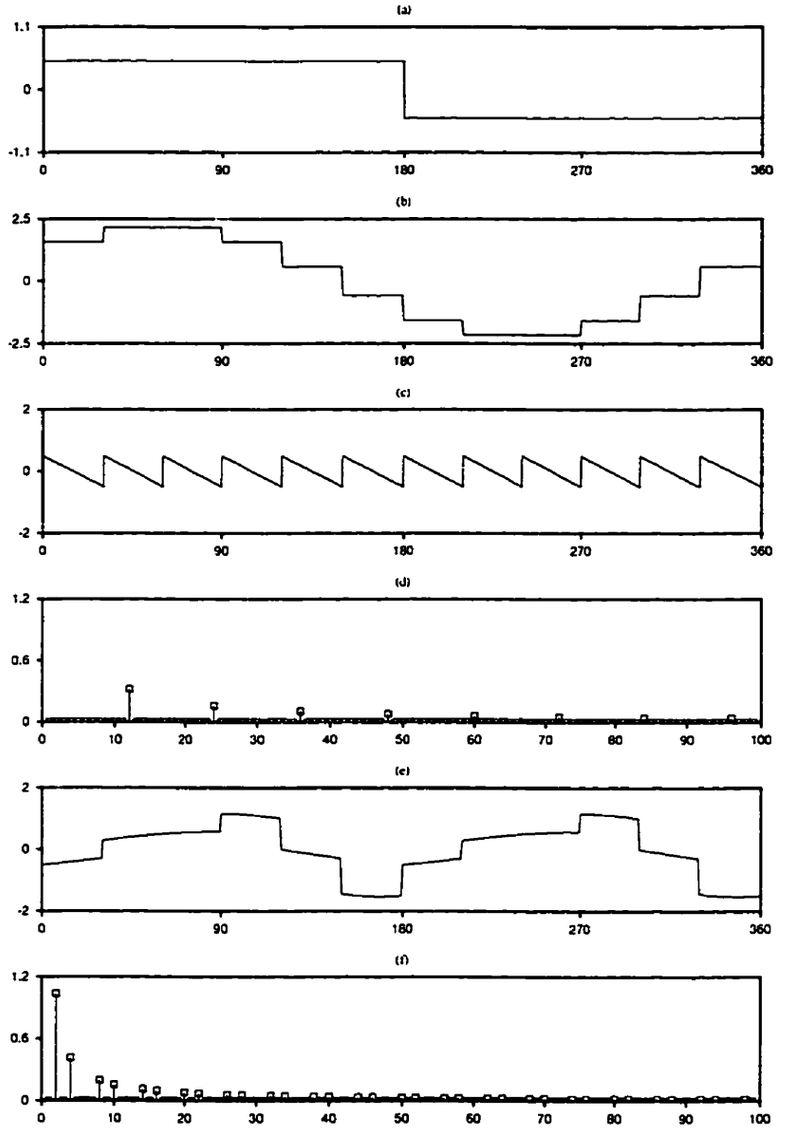


Figure 3.6: ASVC with 12-pulse inverter structure suppling leading reactive current: (a) switching function phase waveform, (b) output line–to–line voltage waveform, (c) inverter input dc current waveform, (d) inverter input dc current spectrum, (e) inverter input dc current waveform under unbalanced conditions, (f) inverter input dc current spectrum under unbalanced conditions.

where $\sum_{k=1} A_k sin(k\omega t)$ is the Fourier series expansion of switching function, the general expression for the second harmonic component of the dc current is given by:

$$\begin{aligned} I_{dc}(2\omega t) \quad := \quad & \frac{-I_a * A_1}{2} cos(2\omega t - \phi_a) + \\ & \frac{-I_b * A_1}{2} cos(2\omega t - 240° - \phi_b) + \\ & \frac{-I_c * A_1}{2} cos(2\omega t + 240° - \phi_c) + . \end{aligned} \tag{3.36}$$

The second harmonic is of concern because its low frequency and relatively large amplitude can considerably increase ripples in the dc voltage. This in turn influences the size of the dc capacitor. The second order harmonic is generated from the interaction of the fundamental component of ac current with the fundamental component of switching function. In this case the value of C has to become large to meet the requirements of maximum harmonic distortion and dynamic behavior of the ASVC in the case of unbalanced conditions. The limited size of C led to putting the 36-pulse ASVC out of operation during ac faults, as is described in [48].

Chapter 4

Model of ac/dc Interconnection

A design process of an optimal control of a system means optimization of performance indices defined in the domain of control parameters. An optimization process can be carried out using conventional control design methods and state-space methods. In general, however, minimization of performance indices can be achieved more easily by using state-space techniques. For this reason an attempt to develop a state-variable model of an ac/dc interconnection has been undertaken. Moreover, the attempt has been actuated by the possibility of using a concept of fuzzy modeling (Appendix A) where a non-linear model can be replaced by several "local" linear models, and the output of the model is a weighted sum of the outputs of all linear models.

4.1 Derivation of Model

A model of an ac/dc interconnection for the normal operating condition has been derived at the beginning. A system to be modeled, built on the basis of the CIGRE Benchmark Model [3], is shown in Figure 4.1 where all underlined symbols represent state variables of the derived model. Derivation of the model has been performed with the assumption that the only place where converter transformers are taken into account are dc equations for rectifier and inverter currents. The transformers are represented by commutating reactance X_c.

Each part of the system is represented by one or two state variable equations. A set of all symbols used in the chapter is included in Appendix B.

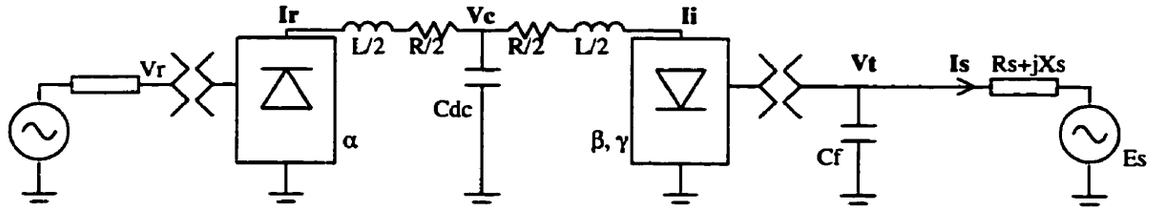


Figure 4.1: ac/dc interconnection: system to be modeled.

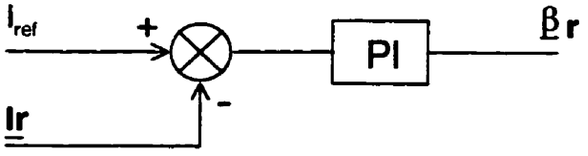


Figure 4.2: Rectifier: current control.

Rectifier

The rectifier current control, Figure 4.2, is represented by the following equation:

$$\beta_r = k_{rp}(I_{ref} - \mathbf{I_r}) + k_{ri}\int (I_{ref} - \mathbf{I_r})dt. \tag{4.1}$$

Taking $\mathbf{I_r}$ and β_r as the state variables, the following equation is obtained as description of the rectifier in the model:

$$\frac{d\beta_r}{dt} = -k_{rp}\,\frac{d\mathbf{I_r}}{dt} + k_{ri}(I_{ref} - \mathbf{I_r}). \tag{4.2}$$

dc Link

A dc transmission line is represented by the T-model, Figure 4.3. The choice of $\mathbf{I_r}$, $\mathbf{I_i}$ and $\mathbf{V_c}$ as the state variables allows the derivation of the following set of equations:

$$\frac{d\mathbf{V_c}}{dt} = \frac{1}{C_{dc}}(\mathbf{I_r} - \mathbf{I_i}), \tag{4.3}$$

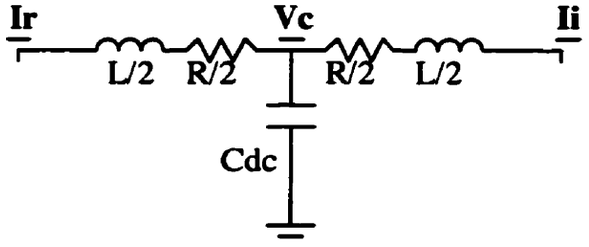


Figure 4.3: dc-link model.

$$\frac{d\mathbf{I_r}}{dt} = -\frac{R}{L}\mathbf{I_r} + \frac{2}{L}(V_{dcr} - \mathbf{V_c}), \tag{4.4}$$

$$\frac{d\mathbf{I_i}}{dt} = -\frac{R}{L}\mathbf{I_i} + \frac{2}{L}(\mathbf{V_c} - V_{dci}), \tag{4.5}$$

where:

$$V_{dcr} = \frac{3\sqrt{2}}{\pi}N\tau_r V_r cos(\pi - \beta_r) - \frac{3X_c}{\pi}\mathbf{I_r}, \tag{4.6}$$

$$V_{dci} = \frac{3\sqrt{2}}{\pi}\frac{N}{\tau_i}\mathbf{V_t} cos\beta_i + \frac{3X_c}{\pi}\mathbf{I_i}, \tag{4.7}$$

and N is a number of six-pulse bridges.

Inverter

Dynamics of the inverter, shown in Figure 4.4, are represented by the gamma control:

$$\beta_i = k_{ip}(\gamma_{ref} - \gamma) + k_{ii}\int(\gamma_{ref} - \gamma)dt. \tag{4.8}$$

Using the above equation and the equation for current at the inverter site:

$$\mathbf{I_i} = \frac{\mathbf{V_t}N}{\sqrt{2}X_c\tau_i}[cos\gamma - cos\beta_i], \tag{4.9}$$

the following equations are derived to represent the inverter in the state variable model:

$$\dot{\gamma} = -\frac{\sqrt{2}\tau_i X_c}{N(sin\gamma + k_{ip}sin\beta_i)}\frac{1}{\mathbf{V_t}}(\dot{\mathbf{I}}_i - \frac{\mathbf{I_i}}{\mathbf{V_t}}\dot{\mathbf{V}}_t) + \frac{k_{ii}(\gamma_{ref} - \gamma)sin\beta_i}{sin\gamma + k_{ip}sin\beta_i}, \tag{4.10}$$

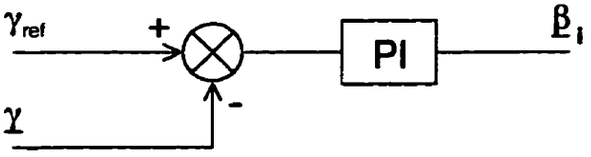


Figure 4.4: Inverter: gamma control.

$$\dot{\beta}_{\mathbf{i}} = -k_{ip}\dot{\gamma} + k_{ii}(\gamma_{ref} - \gamma). \tag{4.11}$$

The angles γ and $\beta_{\mathbf{i}}$ are taken as the next two state variables.

ac System

To derive state variable equations of the receiving ac system, the HVdc link is represented as a current source, Figure 4.5. The following equations are then derived:

$$\frac{d\mathbf{V_{tabc}}}{dt} = \frac{1}{C_f}(\mathbf{i_{abc}} - \mathbf{i_{Sabc}}), \tag{4.12}$$

$$\frac{d\mathbf{i_{Sabc}}}{dt} = \frac{1}{L_s}(\mathbf{V_{tabc}} - R_s\mathbf{i_{Sabc}} - E_{sabc}). \tag{4.13}$$

The subscripts $_{\mathbf{abc}}$ mean that each of the above equations represents three equations for three different phases. Using dq transformation the following equations are obtained:

$$\frac{d\mathbf{V_{td}}}{dt} = \frac{1}{C_f}(\mathbf{i_d} - \mathbf{i_{Sd}}) + \frac{d\theta}{dt}\mathbf{V_{tq}}, \tag{4.14}$$

$$\frac{d\mathbf{V_{tq}}}{dt} = \frac{1}{C_f}(\mathbf{i_q} - \mathbf{i_{Sq}}) - \frac{d\theta}{dt}\mathbf{V_{td}}, \tag{4.15}$$

$$\frac{d\mathbf{i_{Sd}}}{dt} = \frac{1}{L_s}(\mathbf{V_{td}} - R_s\mathbf{i_{Sd}} - E_{sd}) + \frac{d\theta}{dt}\mathbf{i_{Sq}}, \tag{4.16}$$

$$\frac{d\mathbf{i_{Sq}}}{dt} = \frac{1}{L_s}(\mathbf{V_{tq}} - R_s\mathbf{i_{Sq}} - E_{sq}) - \frac{d\theta}{dt}\mathbf{i_{Sd}}, \tag{4.17}$$

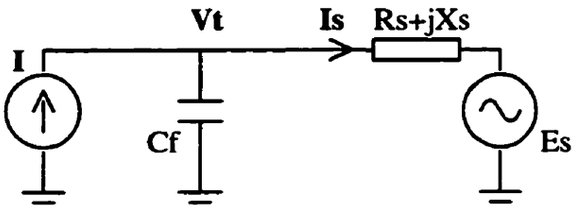


Figure 4.5: ac system.

where θ is a synchronously rotating reference frame. $\mathbf{V_{td}}$, $\mathbf{V_{tq}}$, $\mathbf{i_{Sd}}$ and $\mathbf{i_{Sq}}$ are the next four state variables.

Finally, taking ac voltage $\mathbf{V_t}$ at the inverter bus as the reference frame for dq transformation the following set of equations is used to represent the state variable model of an ac/dc interconnection:

$$\dot{\mathbf{I}}_\mathbf{r} = -\frac{R}{L}\mathbf{I_r} + \frac{2}{L}(\frac{3\sqrt{2}}{\pi}N\tau_r V_r cos(\pi - \beta_r) - \frac{3X_c}{\pi}\mathbf{I_r} - \mathbf{V_c}) \tag{4.18}$$

$$\dot{\beta}_\mathbf{r} = -k_{rp}\ \{-\frac{R}{L}\mathbf{I_r} + \frac{2}{L}(\frac{3\sqrt{2}}{\pi}N\tau_r V_r cos(\pi - \beta_r) - \frac{3X_c}{\pi}\mathbf{I_r} - \mathbf{V_c})\} + k_{ri}(I_{ref} - \mathbf{I_r}) \tag{4.19}$$

$$\dot{\mathbf{V}}_\mathbf{c} = \frac{1}{C_{dc}}(\mathbf{I_r} - \mathbf{I_i}) \tag{4.20}$$

$$\dot{\mathbf{I}}_\mathbf{i} = -\frac{R}{L}\mathbf{I_i} + \frac{2}{L}(\mathbf{V_c} - \frac{2\sqrt{3}}{\pi}\frac{N}{\tau_i}\mathbf{V_{td}}cos\beta_\mathbf{i} - \frac{3X_c}{\pi}\mathbf{I_i}) \tag{4.21}$$

$$\dot{\gamma} = -\frac{\sqrt{3}\tau_i X_c}{N(sin\gamma + k_{ip}sin\beta_\mathbf{i})}\frac{1}{\mathbf{V_{td}}}(\dot{\mathbf{I}}_\mathbf{i} - \frac{\mathbf{I_i}}{\mathbf{V_{td}}}\dot{\mathbf{V}}_\mathbf{td}) + \frac{k_{ii}(\gamma_{ref} - \gamma)sin\beta_\mathbf{i}}{sin\gamma + k_{ip}sin\beta_\mathbf{i}} \tag{4.22}$$

$$\dot{\beta}_\mathbf{i} = -k_{ip}\dot{\gamma} + k_{ii}(\gamma_{ref} - \gamma) \tag{4.23}$$

$$\dot{\mathbf{V}}_\mathbf{td} = \frac{1}{C_f}(\mathbf{i_d} - \mathbf{i_{Sd}}) + \omega\mathbf{V_{tq}} \tag{4.24}$$

$$\dot{\mathbf{i}}_\mathbf{Sd} = \frac{1}{L_s}(\mathbf{V_{td}} - R_s\mathbf{i_{Sd}} - E_{sd}) + \omega\mathbf{i_{Sq}} \tag{4.25}$$

$$\dot{\mathbf{i}}_\mathbf{Sq} = \frac{1}{L_s}(\mathbf{V_{tq}} - R_s\mathbf{i_{Sq}} - E_{sq}) - \omega\mathbf{i_{Sd}} \tag{4.26}$$

where:

$$\mathbf{i_d} = \frac{3\sqrt{12}}{2\pi\tau_i} N\mathbf{I_i} \frac{cos\beta_i + cos\gamma}{2}. \tag{4.27}$$

4.2 Verification of Model

Verification of the model is performed for two types of events: a change of I_{ref}, and a drop of ac voltage at the inverter site. The events under investigation are chosen in such a way that all the signals of the system are within the limits of the normal operating condition of the system. The verification is performed with $\mathbf{V_r}$, $\mathbf{E_d}$ and $\mathbf{E_q}$ considered as inputs to the model (values of these voltages are obtained by $EMTDC^{TM}$ simulation of the system).

A program with the Runge-Kutte integration method of fourth order is used to perform simulations using the state-variable model. The results obtained with this model are compared to the results obtained from $EMTDC^{TM}$ simulations of the modified CIGRE Benchmark Model. The following changes are made in the Benchmark: only the gamma control is used in the inverter control loop, the block calculating the minimum gamma angle over one cycle is removed from the gamma control loop and simplified versions of the receiving system and ac filters are used.

The comparison is performed for very strong ac systems at both ends of the HVdc link. The value of SCR at both ends is equal 16. A change in I_{ref} from 1.0 p.u. to 0.6 and to 0.8 p.u. is investigated first, and the results are presented in Figure 4.6. A drop in the voltage at the inverter ac bus, represented by a change in E_s, is examined next. The results of this examination are shown in Figure 4.7. It can be seen that a fairly good match between the system responses obtained from the simulations using state-variable model and the responses obtained from the $EMTDC^{TM}$ simulations is achieved.

As the next part of verification of the state-variable model, the simulations are performed for the case when the ac system on the inverter site have a small value of SCR (i.e. a weak system). In all the experiments carried out, there are differences between corresponding signals of the system obtained in simulations with the state-

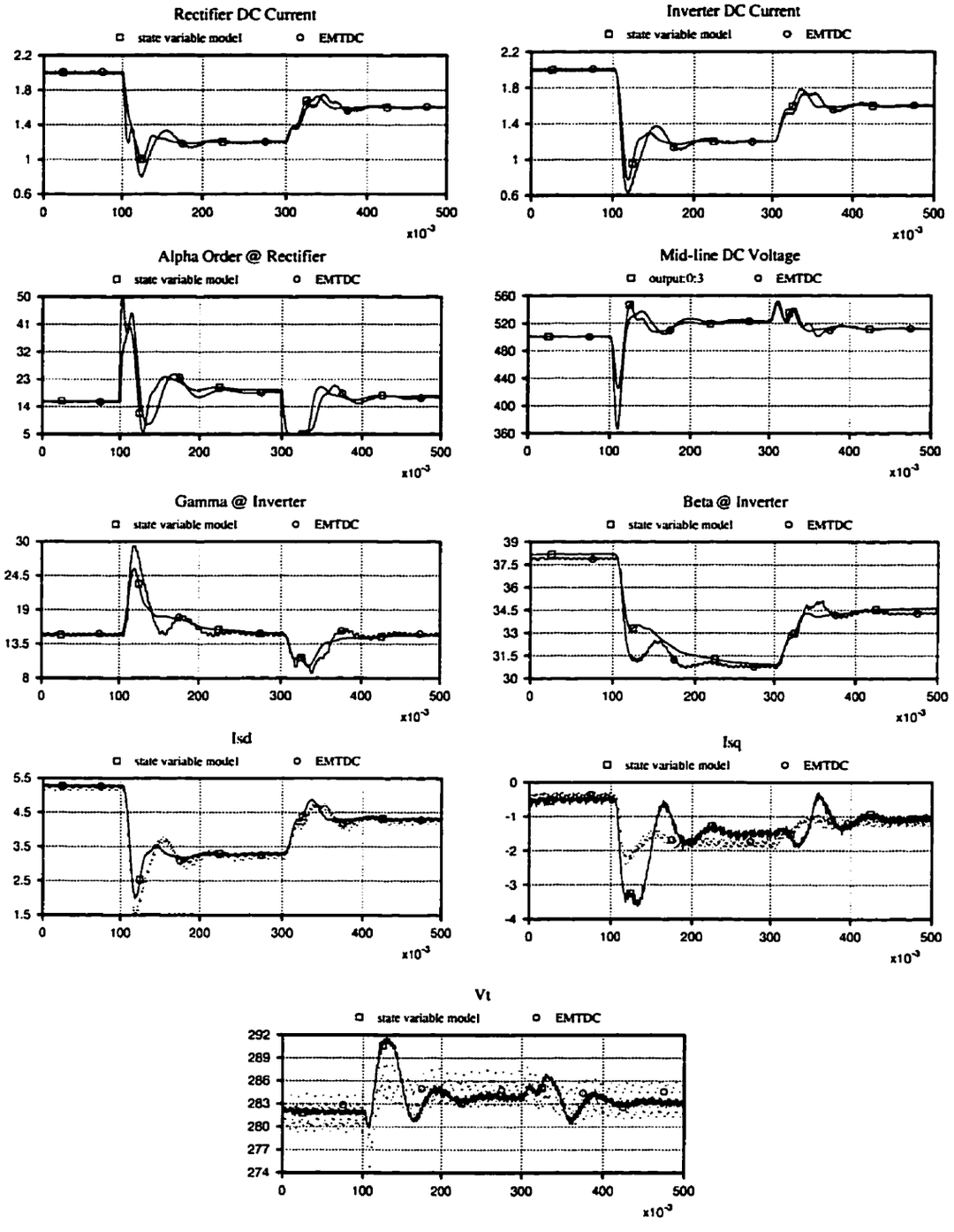


Figure 4.6: Strong ac system: changes of current order from 1.0 to 0.6 to 0.8 p.u.

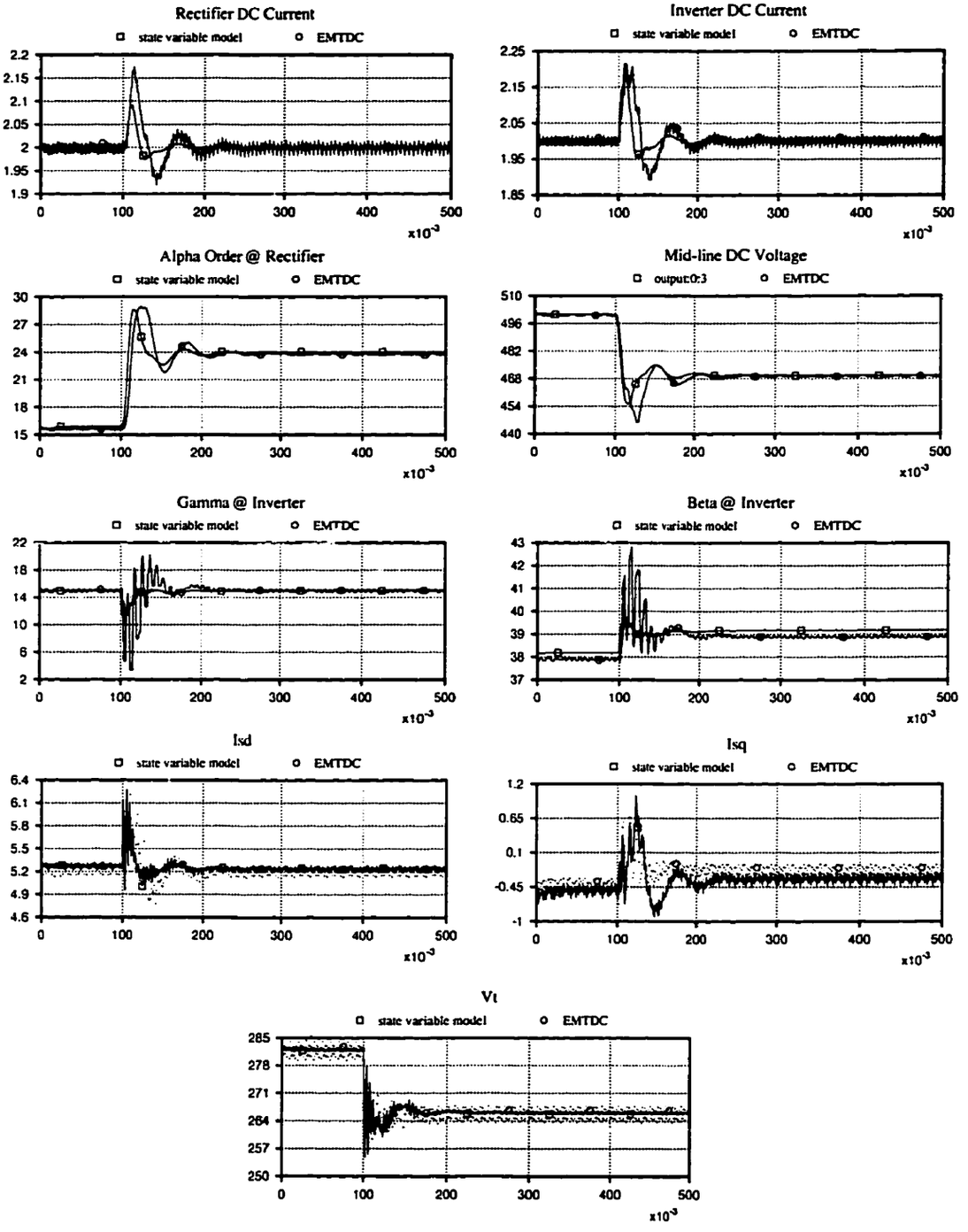


Figure 4.7: Strong ac system: E_s voltage drop from 1.0 to 0.945 p.u.

variable model and simulations using $EMTDC^{TM}$. This suggests that an application of this model to design a control system of the ASVC became questionable, particularly in the case when the ac system at the inverter site is expected to be very weak. After considering the fact that some modification would be necessary, not all state variables are available at the inverter site without a delay, the approach to design an optimal control using the state-variable model had to be left and a search for a different approach has been initiated.

Chapter 5

Genetic Design of Control System

Complex and nonlinear characteristics of electrical power systems mean that derivation of functions which describe relations between signals of a system is difficult (see chapter 4, page 29) and sometimes even impossible. Moreover, even when a model is derived, its complexity limits the usefulness of most control design methods. Frequency and time domain techniques, used in a process of power system control design, allow the derivation of transfer functions, control design and analysis of power system dynamics when simplified, medium-scale models linearized at equilibrium points are used. In many cases methods of control synthesis and analysis are supported by use of analog or digital simulators, for example electromagnetic transients (emt) programs which use the theoretical basis described in Dommel's classic paper [5]. Emt programs possess the capability to model large, non-linear systems with exact representations of all system components. On the other hand, fast acting devices such as static var compensators (SVC), HVdc links and components of flexible ac transmission systems (FACTS), have been introduced as the result of developments in power electronics. Their fast responses to any changes in a system and simultaneous interaction of their control have led to the increased importance of control design processes and to a need for electromagnetic control coordination.

A new design methodology of control systems is presented here. It relies on a combination of advanced system simulator - $EMTDC^{TM}$ and genetic computation. In contrast with standard approaches used in control systems design, this framework provides realistic full-scale modeling abilities accomplished via the simulator along with the

optimization versatility of Genetic Algorithms. In particular, Genetic Algorithms are capable of handling high multivariable and multimodal optimization problems which usually arise in the setting of a complex system.

5.1 Description of Genetic Algorithms

Genetic Algorithms (GAs) are effective search methods based on the principles of natural selection and genetics. They were developed by John Holland to simulate some of the processes observed in natural evolution. Their theoretical foundations are provided in the book 'Adaptation in Natural and Artificial Systems' [21]. Generally, a GA works on a set of potential solutions to a specific problem encoded into chromosome-like data structures. Some of these solutions, chosen on the basis of their performance in solving the problem, are used to create a new set of potential solutions through the use of *operators*. A GA uses this process repeatedly until a particular criterion is met.

GAs are often described in biological terms. Potential solutions are called *chromosomes* and are represented by binary strings or floating point numbers. A set of chromosomes is called a *population* and a problem to be solved is represented by a *fitness function*. The choice of individuals to *reproduce* is performed in a process called *selection* which is based on the *fitness values* assigned to chromosomes. *Genetic operators* such as *crossover* and *mutation* are operators used to create a new population. Crossover permits the exchange of information among individuals in the population and provides the innovative capability of a GA. Mutation ensures needed diversity.

An implementation of a standard GA starts with the creation of an *initial population* which consists of randomly generated chromosomes. An evaluation of chromosomes is next performed. Each chromosome string is broken into substrings which are used as the inputs to a fitness function. The number of substrings depends on the problem to be solved and is unlimited. On the basis of the value of the fitness function and with respect to the other members of the population, the fitness value is assigned to each chromosome. An *intermediate population* is created next. This population is the result of a selection process which can be performed in a number of ways. One of them is a *stochastic sampling with replacement*. In this method the population is mapped onto a roulette wheel where each individual is represented by a space (on the wheel) that proportionally

```
program GeneticAlgorithm
begin
   Initialization                                  {creation of initial population}
   while (not done ) do
      Evaluation                                   {fitness function performed on chromosomes
                                                    of initial/current population}
      if (not termination_condition)
         then
            Selection                              {creation of intermediate population}
            GeneticOperations                      {creation of next population}
          else
            done:=true
   end
end
```

Figure 5.1: Flowchart of Genetic Algorithm.

corresponds to its fitness value. Individuals of intermediate population are chosen by a repetitive spinning of the roulette wheel. Finally, the operations of crossover and mutation are performed which leads to the creation of a *next population.* Crossover is applied to the randomly paired chromosomes from the intermediate population with a probability denoted as p_c. The chromosomes of each pair are split into two parts at the randomly generated crossover point and then recombined. In the case of mutation, all bits in all substrings are altered with a probability p_m. All steps described above are repeated many times, with such a difference that the population being evaluated is named a *current population* and is equal to the next population from the previous iteration. Each iteration is called a *generation.* The flowchart of a Genetic Algorithm is presented in Figure 5.1.

Empirical works and theories currently existing indicate that GAs are powerful tools for solving optimization problems. They possess the ability to solve complex, multi-dimensional problems with numerous, difficult to find optima. Searching methods of GAs based on a population of potential solutions and genetic operators allow GAs to evaluate many different hyperplanes of the search space in parallel which leads to

simultaneously performed multiple search. Moreover, GAs require very little problem-specific information. GAs may be employed in solving most problems. GAs can be applied to virtually any type of problem. Consequently, a wide range of functions: linear, nonlinear, discontinuous, discrete, etc., can be optimized. There is a free choice in a way a problem is implemented.

5.2 Concept of Genetic Design of Control

The ability of GAs to solve difficult, multi-dimensional problems with little problem-specific information has resulted in a new concept of control design [41]. In this concept, there is no need for a mathematical description of a system for which control procedures are designed. The novelty of this approach is to model the system as realistically as possible (including various parts, indices) using advanced system simulators and taking full advantage of genetic computation to optimize system behavior. A usage of the system model developed with an advanced simulator means that all relations between system variable parameters and system signals are implicitly defined. Therefore, a function of system variable parameters which has to be optimized, called a fitness function, is represented by a model of the system and models of performance indices. In this case, the value of a fitness function is a weighted sum of the values of performance indices obtained in a simulation process.

Optimization is performed using GAs. Each chromosome represents a set of values of system variable parameters to be adjusted. An evaluation of each chromosome is done performing a simulation. The value of the performance index obtained in a simulation process is assigned to the chromosome as the fitness value.

Any set of system variable parameters can be used as the input to the optimized function. One can choose any parameters of control loop components and/or any parameters of elements of the system. There is no limit to their number – GAs can perform multi-parameter optimization. The parameters themselves can be either continuous or discrete. Their values are encoded into binary strings or represented using floating point numbers. Each set of them is treated as a single chromosome. Application of an advanced simulation system allows the function to be optimized not only by adjusting the values of system parameters but also by adjusting the structure of the system. In this

case, the values assigned to some input parameters are identifiers of different structures of the system which are initially defined. Each set of the values of these input parameters identifies only one structure which is active at the time of simulation. Finding the optimal structure and the optimal values of system variable parameters is performed simultaneously.

In this concept, fitness functions can be built using a single performance index or a combination of an arbitrary number of performance indices. The indices used for building the fitness function can be the parameters of system transient responses such as the maximum overshoot, the response time, functions of these responses such as square error integral, time multiplied by absolute error integral, or any functions defined by a designer. Any signals of the system can be used as the input to the performance indices. A multi-input multi-output character of relations between system signals and system variable parameters means that in many cases there is a need to perform optimization according to more than one signal of the system. Application of a simulation tool allows the possibility of creating fitness functions which are built using several models of performance indices based on different signals of the system. In this case the value of the function to be optimized is a weighted sum of the values of all performance indices used for building the fitness function.

To design a control procedure which ensures ideal behavior of a non-linear system, each set of values of the chosen system variable parameters (chromosome) has to be evaluated by several simulation runs. Each simulation run is performed for a different operating condition and different change in magnitude of a reference signal. Such an approach allows a significant possibility to apply different optimization criteria for different events, depending upon various operating states of the system.

5.3 Description of *GeneticEMTDC* Program

The approach presented is applied in the area of electrical power systems. A software package is created using an electromagnetic transient (emt) program - $EMTDC^{TM}$ [8] as a simulation environment in which all genetic based optimization is carried out.

A fitness function is implemented by a model of a power system and models of performance criteria which are developed with the $EMTDC^{TM}$ program, Figure 5.2.

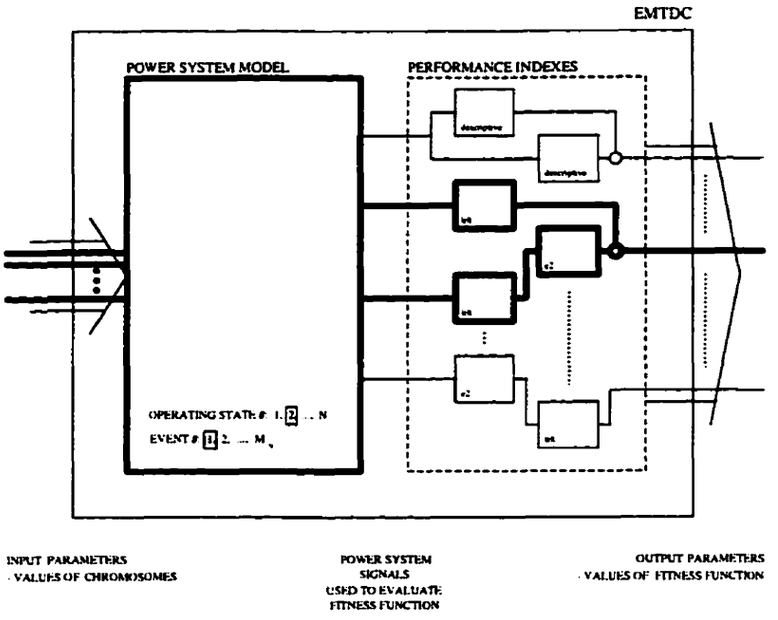


Figure 5.2: *GeneticEMTDC* Fitness Function Implementation.

The parameters of controllers and/or any electrical devices which are important from the point of view of control objectives can be used as the input variables of the fitness function. Objectives of a designed control system are represented by performance indices which can use different signals from a power system. One can choose any signal assumed as important or interesting, e.g. an error between the reference and real values of a signal, or a signal which has direct or indirect connection with the designed control. Control objectives implemented in such a way are functions which are optimized and are named *partial fitness functions.* In this case the value of the fitness function is a weighted sum of the values of all partial fitness functions.

An evaluation process is performed in a way as shown in Figure 5.3. It allows investigating system behavior at different operating conditions and faults. Several simulation runs are performed to evaluate a single chromosome. Each simulation is performed for one operating condition of the system and for one event at a given condition. For the case of each event the performance of a system can be evaluated using different control objectives, it means different partial fitness functions. At the end of performance evaluation of a given chromosome the sum of all values of the partial fitness functions

```
procedure EMTDC_Simulations
begin
  for EachChromosome do
    for EachOperatingCondition do
      for EachEvent do
        SimulaitonRun_of_EMTDC
        Store_PartialFitFunVal
      end
    end
    FitFunValue:=Sum_of_PartialFitFunVals
  end
end
```

Figure 5.3: Flowchart of Evaluation Process in *GeneticEMTDC*.

becomes the fitness value of the chromosome. As it is seen in Figure 5.2, many outputs from the emt program could be defined, but at the time of simulation only one of them is taken as the value of the partial fitness function (this is indicated by the bold line).

The GA used in the program *GeneticEMTDC* is a modified version of the canonical form of GA (see section 5.3, page 42). As a selection method, a stochastic universal sampling is used. According to this method the population is laid out in random order as in a pie graph, where each individual is assigned a space on the pie graph in proportion to its fitness. Next an outer roulette wheel is placed around the pie with N (population size) equally spaced pointers. A single spin of the roulette wheel simultaneously picks all N members of intermediate population.

To improve tuning of parameter values, non-uniform mutation is applied [27]. This allows the space to be searched uniformly at the beginning and then locally at later stages.

To prevent a reduction of selection pressure, a scaling window mechanism [17] is used. It is accomplished by subtracting from the fitness value of all chromosomes a minimum value of fitness which occurred in the last three generations. The strategy of selection to preserve the best chromosome into the next generation is also used. The

Table 5.1: Parameters of GA

Parameter	Value
Number of Generations	100
Population Size (N)	70
Crossover Probability (p_c)	0.9
Mutation Probability (p_m)	0.3679

parameters of GA are presented in Table 5.1 [1].

Binary representation of chromosomes is used. For each optimized parameter i its range $[r_{iL}, r_{iR}]$ and precision p_i are specified. Based on this information, a length of substring n_i which represents this parameter is calculated to fulfill the requirement:

$$2^{n_i-1} < (r_{iR} - r_{iL}) * 10^{p_i} \leq 2^{n_i}. \tag{5.1}$$

The mapping from a binary string $< b_{n_i-1} b_{n_i-2} ... b_0 >$ into a real number is completed according to the formula:

$$r_{iL} + (\sum_{k=0}^{n_i-1} b_k * 2^k) * \frac{r_{iR} - r_{iL}}{2^{n_i} - 1}. \tag{5.2}$$

In all the experiments presented in this chapter, the range of optimized parameters is $< 0.0, 10.0 >$ for proportional and integral gains, and $< 1.0e^{-6}, 10.0 >$ for the case of integral time constant. This range and the requirement regarding the precision of each

[1] The values of GA parameters are found using a multi-level GA. In this approach the objective of the higher-level GA is to find the values of genetic parameters of the lower-level GAs which had to optimized a function. The function which is created on the basis of several simulation experiments of control design is used in this case.

parameter, $p_i = 6$, means that a 24-bit substring is used as a representation of single parameter.

5.4 Application of Genetic Design

To verify the usefulness of the approach, the *GeneticEMTDC* is applied to design the controls of two dc systems: the CIGRE Benchmark Model [3] and the Multi-Terminal dc System [53]. The designing process embraces adjustment of the control parameters (the first two experiments), and simultaneous adjustment of both the control parameters and the control system structure (the third experiment). A detailed description of events which occur in the systems and which are taken into account during a designing process, as well as a description of performance indices used in each case are included here to show the methodology of using *GeneticEMTDC*.

5.4.1 Adjustment of Control Parameters Values

CIGRE Benchmark Model

The CIGRE Benchmark Model, presented in Figure 5.4, is used as a model of HVdc link to design the dc current control. Settings of the parameters of the proportional-plus-integral (PI) controller for the rectifier current control is an objective of the design process.

An adjustment of these parameters needs a comprehensive investigation of system behavior for different dc faults, ac faults and for different changes in a current order at different operating states. Because the purpose of the example is to show a methodology of control design using *GeneticEMTDC*, only four different events are taken into account. The usage of different signals, single and combined performance indices are shown below with the description of the events.

Event 1: a change in the dc current order from 1 p.u. to 0.8 p.u. The system response is optimized by minimizing a single performance index – the integral square–error criterion. The errors between current order and measured dc currents at the rectifier site $e_{I_{rec}} = I_{ord} - I_{rec}$, and at the inverter site $e_{I_{inv}} = I_{ord} - I_{inv}$ are used as the inputs to the performance index. The values of the errors are calculated with reference

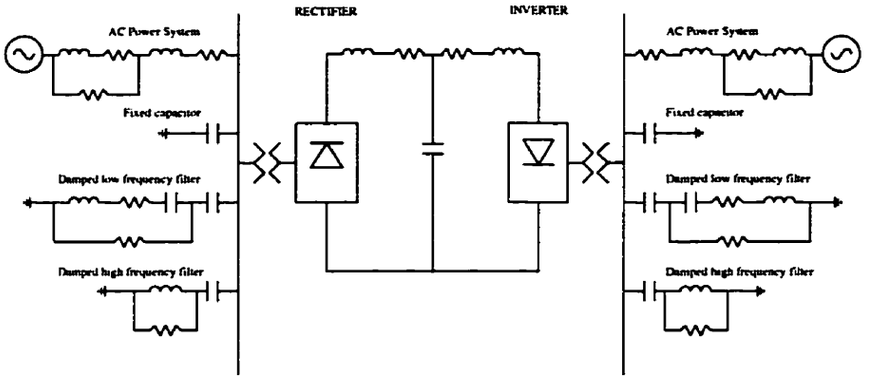


Figure 5.4: CIGRE Benchmark Model.

to I_{ord}. The performance index (PIndex) can be described by the expression:

$$PIndex_1 := \int_0^{t_{sim}} [\ (e_{I_{rec}})^2 + (e_{I_{inv}})^2\ ]dt, \tag{5.3}$$

where t_{sim} means time of simulation.

Event 2: a change in the dc current order from 0.5 p.u. to 0.6 p.u. In this event, descriptive performance indices are used: the overshoot, the steady state error and the settling time. The performance index signals are the same as those used in the previous event. Optimization of the system response means minimization of the overshoot and the steady state error, and maximization of the settling time (used as in the form $PIndex_{2c}$). The performance indices used in the event are as follows:

$$PIndex_{2a} := Overshoot_{I_{rec}} + Overshoot_{I_{inv}}, \tag{5.4}$$

$$PIndex_{2b} := e_{steady\_state_{I_{rec}}} + e_{steady\_state_{I_{inv}}}, \tag{5.5}$$

$$PIndex_{2c} := SettlingTime_{I_{rec}} + SettlingTime_{I_{inv}}, \tag{5.6}$$

where:

$$SettlingTime_I := t_{sim} - min(t_s : \forall t \in (t_s, t_{sim} \mid e(t)_I \mid \leq 0.05). \tag{5.7}$$

Event 3: a change in the dc current order from 0.2 p.u. to 0.16 p.u. Performance index for this event defined the integral-of-time-multiplied absolute-error criterion. The inputs to the index are the same as in previous events. The expression of the performance index is:

$$PIndex_3 := \int_0^{t_{sim}} [\ |\ e_{I_{rec}}\ |\ t + |\ e_{I_{inv}}\ |\ t\ ]dt. \tag{5.8}$$

Event 4: one phase line to ground fault cleared after five cycles. Parallel and series connections in a time domain of different performance indices are used. The integral square-error criterion and the integral-of-time-multiplied absolute-error criterion are used to defined performance indices which are connected in series. Both of them are connected in parallel with a descriptive performance index: the settling time. Besides the current errors the transmitted power in p.u. value is also used as one of the inputs to the indices. The performance indices are presented below:

$$PIndex_{4a} := \int_0^{t_{flt\_clr}} [\ (e_{I_{rec}})^2 + (e_{I_{inv}})^2\ ]dt, \tag{5.9}$$

$$PIndex_{4b} := \int_{t_{flt\_clr}}^{t_{sim}} [\ |\ e_{I_{rec}}\ |\ t + |\ e_{I_{inv}}\ |\ t\ ]dt, \tag{5.10}$$

$$PIndex_{4c} := SettlingTime_{Power}, \tag{5.11}$$

where t_{flt_clr} is the time of fault clearance.

The objective of the process of control design is to minimize all performance indices described above. The exceptions are $PIndex_{2c}$ and $PIndex_{4c}$ which have to be maximized. To accomplish the objective using a GA which optimizes a problem by searching the maximum, the following partial fitness functions are created for each event based on the performance indices:

$$FitFun_i := A_i - B_i * PIndex_i \tag{5.12}$$

for events $i = 1, 3$, and

$$FitFun_i := \sum_{j \in \{a,b\}} (A_{i,j} - B_{i,j} * PIndex_{i,j}) + C_{i,c} * PIndex_{i,c} \tag{5.13}$$

for events $i = 2, 4$, where As, Bs, and Cs are constants.

Using this approach it is possible to change the importance of some criteria and events in the optimization problem. The values of the constants As and Cs decide which event is more important from a control design point of view, and which criterion in a particular event is to be emphasized. The purpose of the constants Bs is to keep values of $PIndices$ in the range of the constants As. Moreover, constants Bs and Cs make it possible to achieve the same units for all performance indices.

To ensure that currents on rectifier and inverter sites are within the limits of steady state error, a penalty function is introduced. This is valid only before the events occur. The expression describing the penalty function is presented below:

$$penalty_{rec|inv} := \tag{5.14}$$

$$\begin{cases} penalty\_val & \text{if } \mid e_{rec|inv} \mid > e_{steady\_state} \\ 0 & \text{otherwise} \end{cases}, \tag{5.15}$$

where the e_{steady_state} and $penalty\_val$ are chosen arbitrary (in our case 0.02 is taken as e_{steady_state}).

The final form of the optimization problem which had been solved by $GeneticEMTDC$ is presented below:

$$max\ (\sum_{i=1}^{4} FitFun_i - penalty_{rec} - penalty_{inv}\ ). \tag{5.16}$$

In the experiment, $GeneticEMTDC$ simulations are performed with the following time parameters:

- time of simulation (t_{sim}): 600 ms,
- time of current order change: 200 ms,
- time of fault application: 200 ms,
- time of fault clearance (t_{flt_clr}): 300 ms.

With the genetically derived values of the parameters of PI controller (after 100 generations), the total value of the performance indices increased by four per cent in comparison with the value of indices obtained with the original values of the parameters provided with the CIGRE Benchmark Model. System responses for all events are better according to the performance indices described above. Results for *Event 1* and *Event 4* are presented in Figure 5.5 and Figure 5.6 respectively.

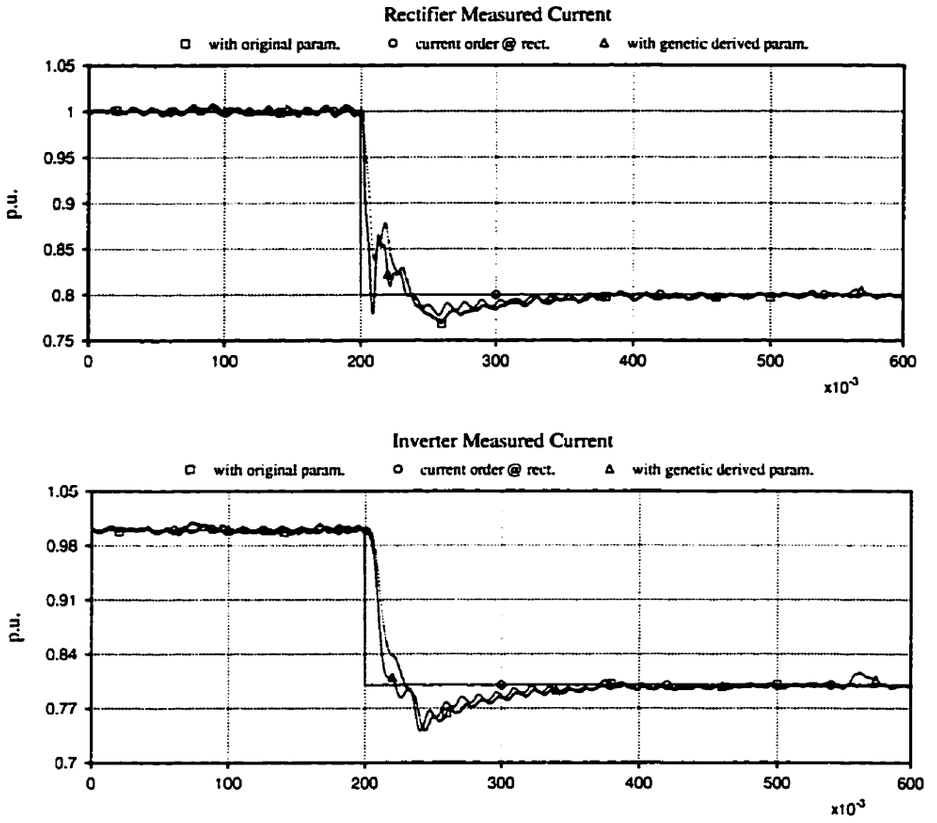


Figure 5.5: System response for *Event 1* with CIGRE Benchmark.

Multi-Terminal dc System

The Multi-Terminal system used in the experiment is the four terminal bipole system with two inverters, one of which is connected to a weak ac system (SCR=1.5), Figure 5.7 [53].

GeneticEMTDC is used to adjust six parameters of the PI controllers. The first two parameters represents proportional gain and time constant of the controllers in the current control loops of the rectifiers, the second two parameters are the PI parameters of the current control loop of the inverter connected to a weak ac system, and the final pair of parameters are the parameters of the gamma control loop of the second inverter.

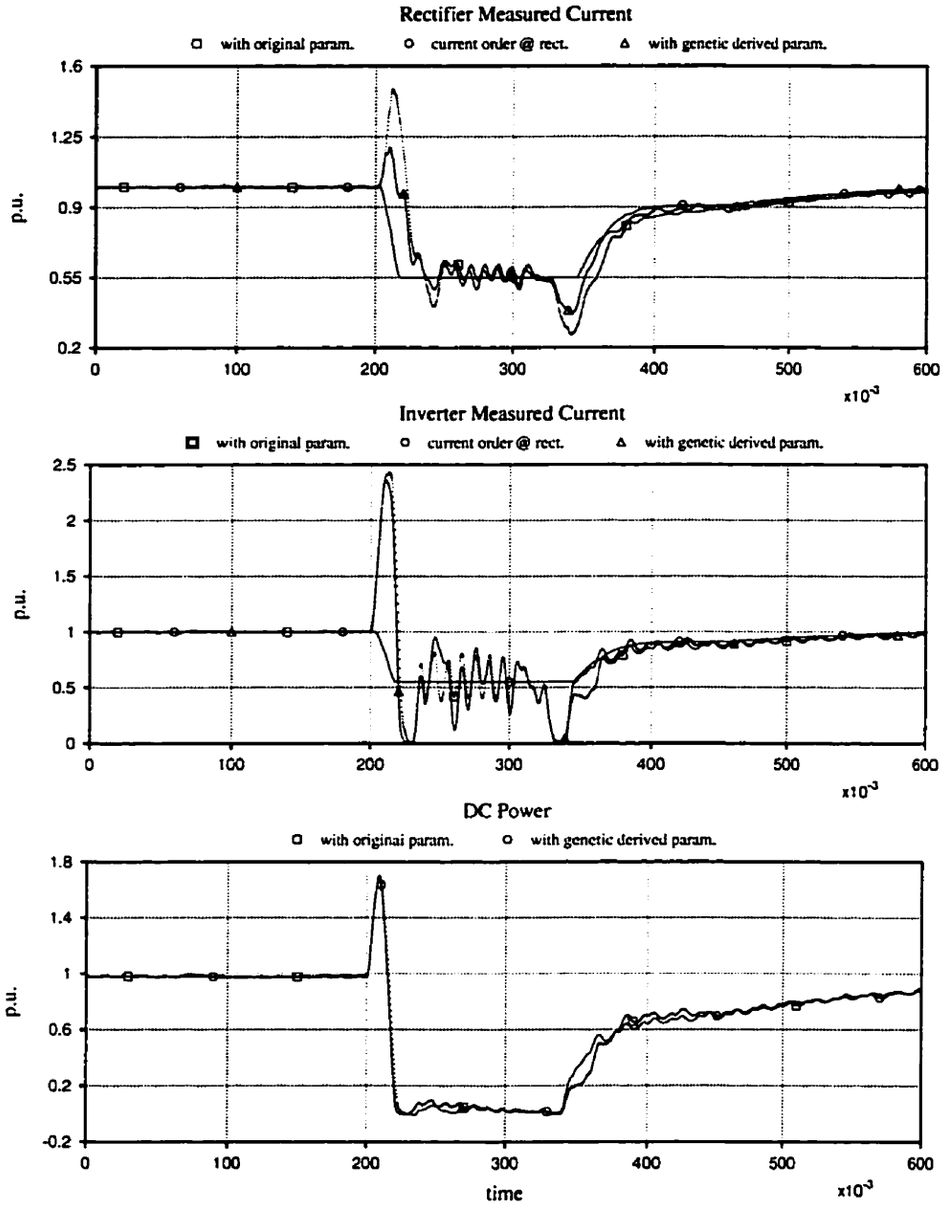


Figure 5.6: System response for *Event 4* with CIGRE Benchmark.

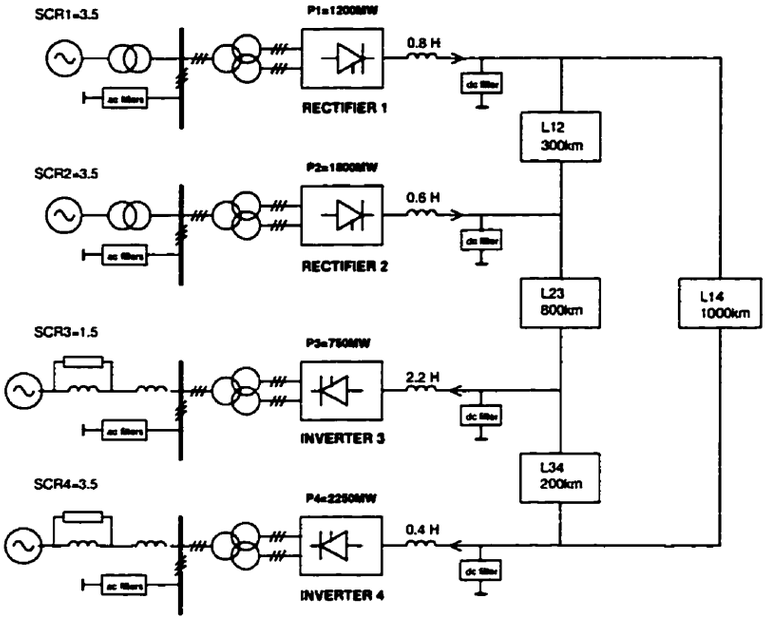


Figure 5.7: Multi-Terminal dc System.

The designing process is performed for five different events:

- *Event 1:* two phase ac fault to ground at rectifier #2;
- *Event 2:* one phase ac fault to ground at inverter #3;
- *Event 3:* three phase ac fault to ground at inverter #4;
- *Event 4:* dc fault at negative pole at line L14;
- *Event 5:* a change of the dc current order from 1.0 p.u. to 0.8 p.u.

All ac faults are cleared after five cycles. In the case of the dc fault, a forced-retard is enforced at each converter after 50 ms from the moment the dc fault occurs. This delay represents line fault detection. The fault is cleared at 100ms, and at 150ms the forced-retard is removed.

For each of the first four events the following partial fitness function is used:

$$FitFun_i := \sum_{j \in \{a,b,c,d\}} (A_{i,j} - B_{i,j} * PIndex_{i,j}) \tag{5.17}$$

with the performance indices:

$$PIndex_{i,a} := \int_0^{t_{flt\_clr}} \sum_k (e_{I_k})^2 dt, \tag{5.18}$$

$$PIndex_{i,b} := \int_{t_{flt\_clr}}^{t_{sim}} \sum_k (\mid e_{I_k} \mid t \,) dt, \tag{5.19}$$

where $k \in \{rec1pos,\ rec1neg,\ rec2pos,\ rec2neg,\ inv3pos,\ inv3neg,\ inv4pos,\ inv4neg\}$,

$$PIndex_{i,c} := \int_{t_{flt\_clr}}^{t_{sim}} \sum_m \mid e_{power_m} \mid t \ dt, \tag{5.20}$$

where $m \in \{inv3pos, inv3neg, inv4pos, inv4neg\}$, and

$$PIndex_{i,d} := \int_{t_{flt\_clr}}^{t_{sim}} \sum_n (e_{gamma_n})^2 dt, \tag{5.21}$$

where $n \in \{inv4pos, inv4neg\}$, for $i = 1, 2, 3, 4$.

For the change of the dc current order, the following partial fitness function is used:

$$FitFun_5 := \sum_{j \in \{a,b\}} (\ A_{5,j} - B_{5,j} * PIndex_{5,j} \ ) \tag{5.22}$$

with the performance indices:

$$PIndex_{5,a} := \int_{t_{change}}^{t_{sim}} \sum_k (\mid e_{I_k} \mid t \,) dt, \tag{5.23}$$

$$PIndex_{5,b} := \int_{t_{change}}^{t_{sim}} \sum_m (e_{gamma_m})^2 dt. \tag{5.24}$$

The errors of current and gamma are calculated using the same formulas as in the case of events 1 to 4.

As in the case of the CIGRE Benchmark Model, the penalty function is used to ensure that the current on any pole at any converter did not exceed the limits. The form of the problem solved by *GeneticEMT* in this case is presented below:

$$max \ (\sum_{i=1}^{4} FitFun_i - \tag{5.25}$$

$$\sum_{j \in \{rec1, rec2, inv3, inv4\}} \ \sum_{k \in \{pos, neg\}} penalty_{j,k} \ ). \tag{5.26}$$

All simulations are performed with the same time parameters as for the CIGRE Benchmark Model case.

Using the genetically derived values of PI controller parameters, the value of a sum of the performance indices increased by 16.5 per cent compared to the value of the performance indices obtained using original [53] values of the parameters. System responses for ac and dc faults are improved except for the event of I_{order} change, where the value of the indices is slightly less than with the original values of the parameters. The best three responses of the system are presented. Values of dc current on the positive pole in the case of ac faults at the inverters are presented in Figure 5.8, and Figure 5.9. For the case of dc fault, values of dc current at the negative pole are shown in Figure 5.10.

5.4.2 Adjustment of Control Parameters Values and Control System Structure

CIGRE Benchmark Model

The CIGRE Benchmark Model, already known from the first experiment, is used here to show that it is possible to choose the optimal structure of the control system at the same time as the values of control parameters are adjusted. In this case the gamma angle control at the inverter site of the dc link is designed. The objectives of the design process are to adjust the parameter values of the proportional-plus-integral (PI) controller and to choose a structure of the gamma control. For a structure choice, a very simple case is investigated. Two possible configuration of gamma control are initially defined: one with a non-linear gain block and the other without, as shown in Figure 5.11. Besides the parameters of PI controller such as proportional gain and the time constant, the values of the parameters of the non-linear gain block are also optimized: break point (BP), low gain (GL) and high gain (GH).

An evaluation of each set of values of the parameters is performed by investigating the system behavior for four different events:

- *Event 1:* a change in the dc current order from 1.0 p.u. to 0.8 p.u.;
- *Event 2:* one phase line to ground fault cleared after five cycles;
- *Event 3:* three phase line to ground fault cleared after five cycles;

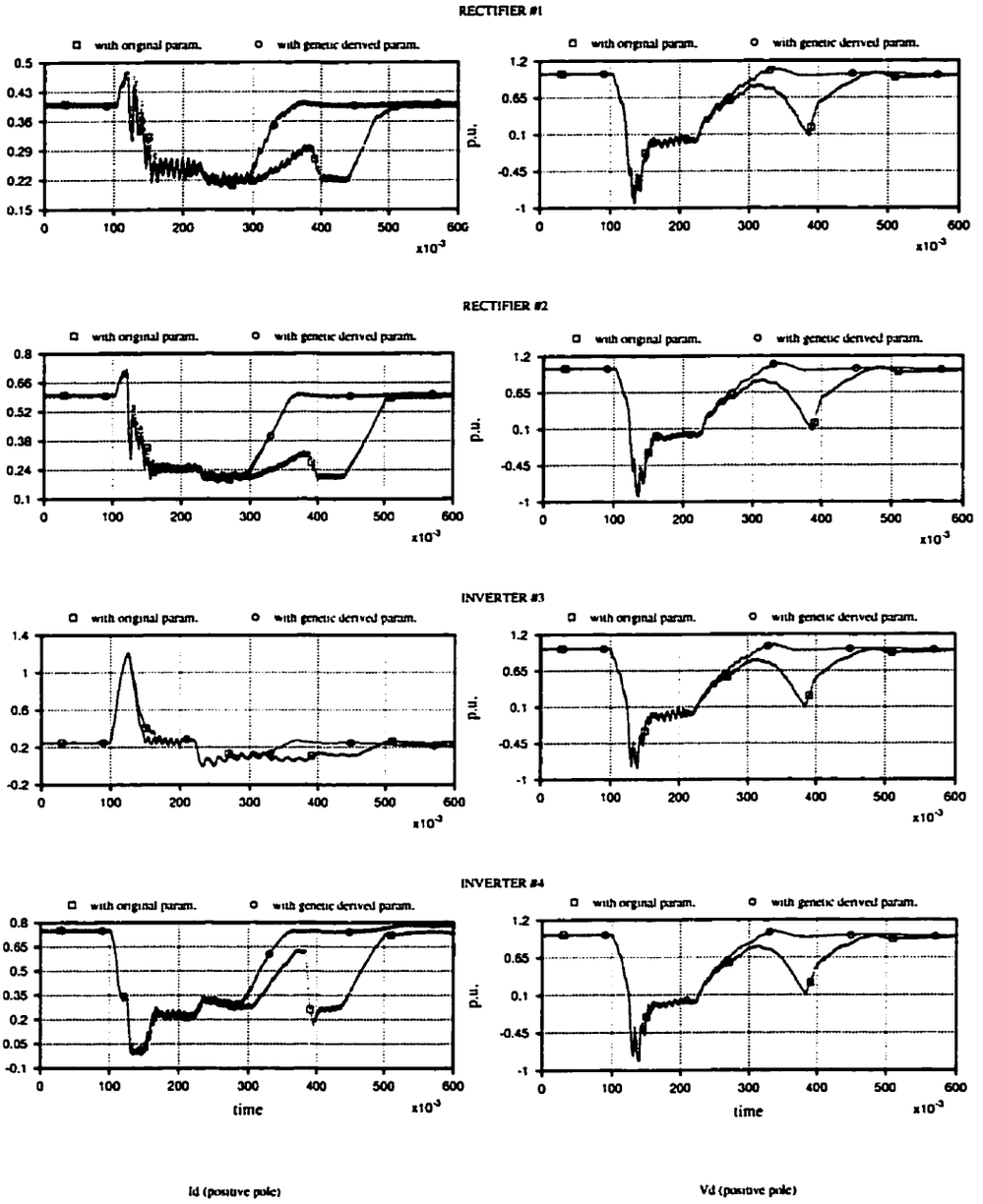


Figure 5.8: System response for one phase line to ground fault at inverter #3 for the Multi-Terminal Model.

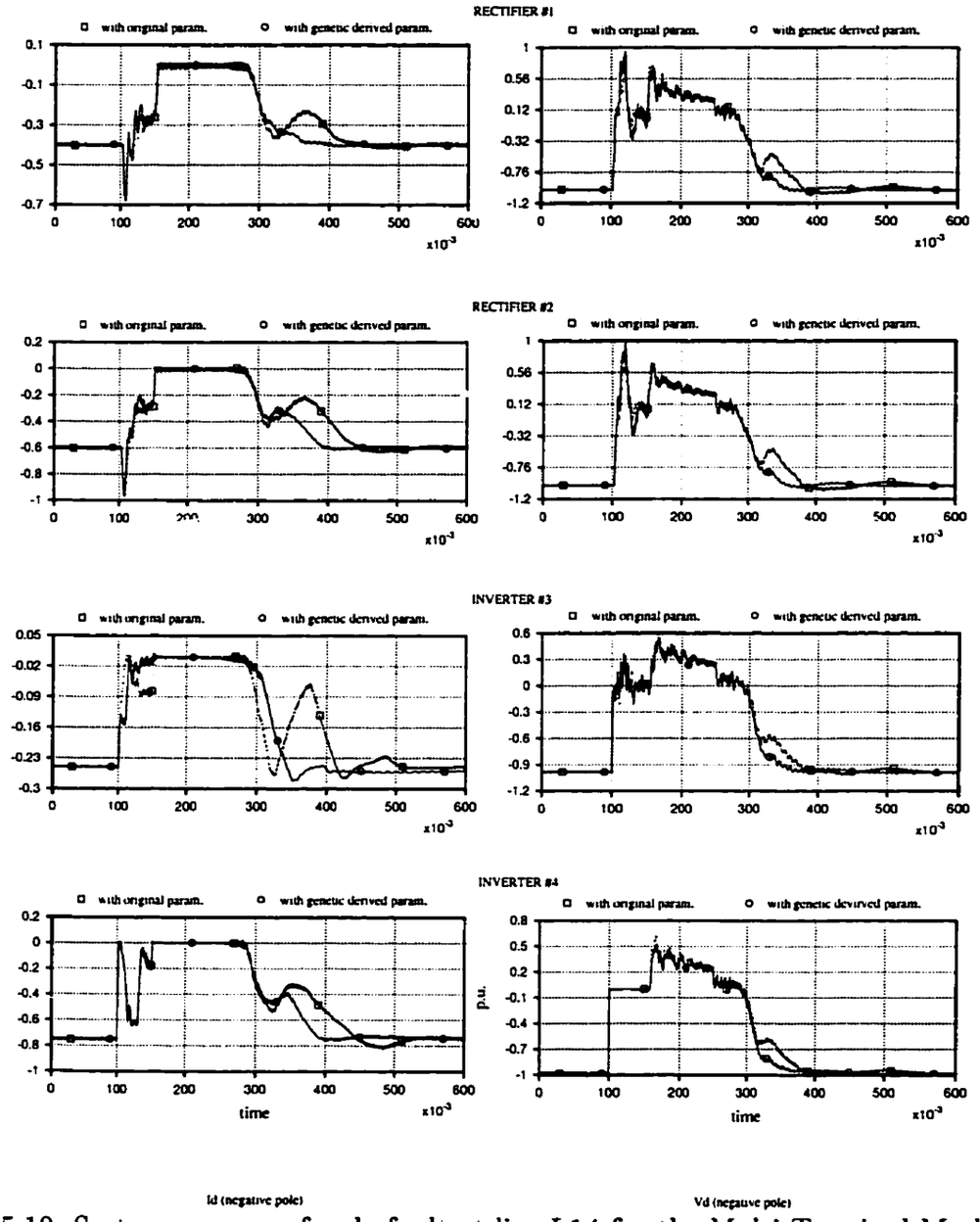


Figure 5.10: System response for dc fault at line L14 for the Multi-Terminal Model.

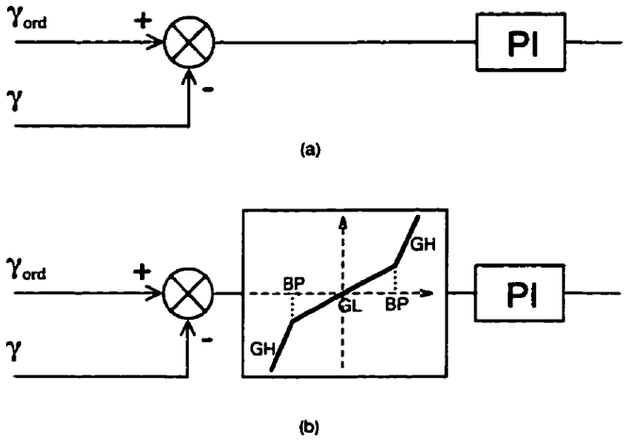


Figure 5.11: Two structures of gamma control: (a) without non-linear gain block, (b) with non-linear gain block.

- *Event 4:* 20 per cent ac voltage drop at the inverter site.

The first event used a performance index which is built using the integral-of-time-multiplied absolute error criterion. The error between gamma order and minimum measured gamma at the inverter site, $e_\gamma = \gamma_{ord} - \gamma_{measured}$, is taken as the input to the index. The value of the error is calculated with reference to γ_{ord}. The performance index is described by the expression:

$$PIndex_1 := \int_0^{t_{sim}} \mid e_\gamma \mid dt, \tag{5.27}$$

where t_{sim} means time of simulation.

In all of the last three events a system response is optimized using parallel and series connections of different performance indices. The index with the integral square-error criterion is connected in series with the index created using the integral-of-time-multiplied absolute error criterion. Both indices use the gamma error as the input, and both indices are connected in parallel with the third performance index. The third index is built using the integral-of-time-multiplied absolute error criterion with the transmitted

power (in p.u. values) as the input. The indices are as follows:

$$PIndex_{i,a} := \int_0^{t_{flt\_clr}} (e_\gamma)^2 \, dt, \tag{5.28}$$

$$PIndex_{i,b} := \int_{t_{flt\_clr}}^{t_{sim}} \mid e_\gamma \mid \; t \, dt, \tag{5.29}$$

$$PIndex_{i,c} := \int_{t_{flt\_clr}}^{t_{sim}} \mid e_{Power} \mid \; t \, dt \tag{5.30}$$

for $i = 2, 3, 4$, where $e_{Power} = Power_{ord} - Power_{measured}$, and t_{flt_clr} is the time of fault clearance.

Based on the indices described above, the following partial fitness functions are created:

$$FitFun_1 := A_1 - B_1 * PIndex_1, \tag{5.31}$$

and

$$FitFun_{Xi} := \sum_{j \in \{a,b,c\}} (A_{i,j} - B_{i,j} * PIndex_{i,j}), \tag{5.32}$$

for $i = 2, 3, 4$, where As and Bs are constants.

The final form of the optimization problem which had been solved by *GeneticEMT* is presented below:

$$max(\sum_{i=1}^{4} FitFun_i). \tag{5.33}$$

In the optimization process, the values of the parameters are changing in the following ranges: for proportional gain and integral time constant – see section 5.3, page 42; for break point of the non-linear gain block – from 0.0 to 0.5; for low gain and high gain of the non-linear gain block – from 0.0 to 2.0. The parameter which identified a structure of the gamma control could have one of two values: either zero or one. In the experiment, *GeneticEMTDC* simulations are performed with the following time parameters:

- time of simulation (t_{sim}): 600 ms,
- time of current order change: 200 ms,
- time of fault application: 200 ms,
- time of fault clearance (t_{flt_clr}): 300 ms.

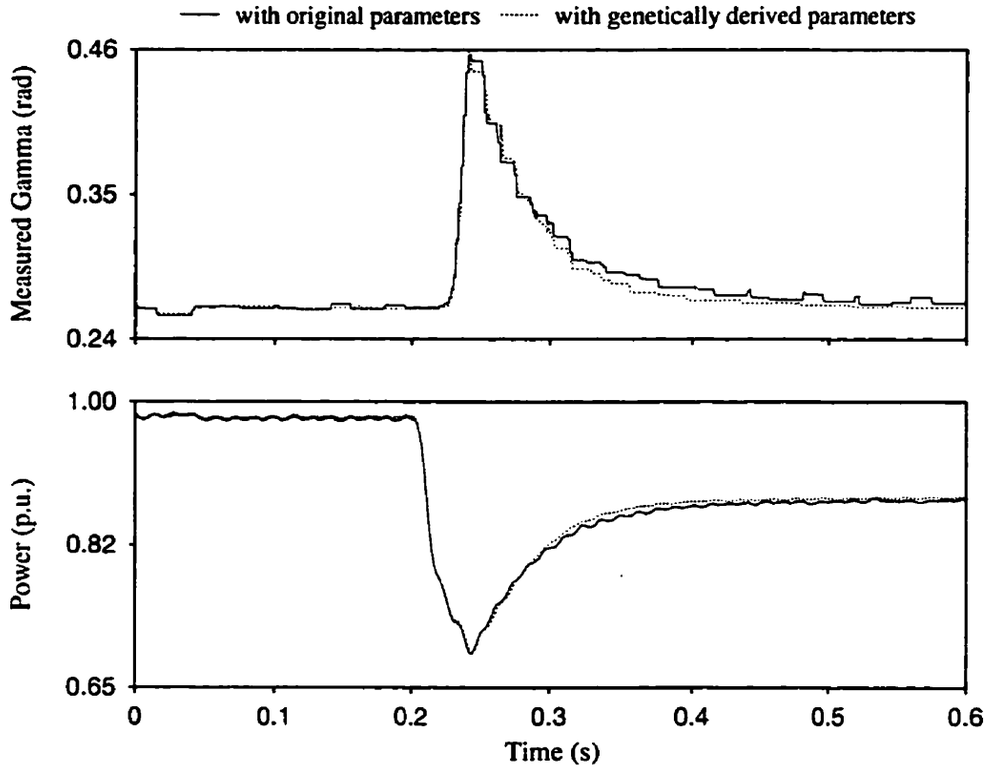


Figure 5.12: System response for *Event 1* with CIGRE Benchmark.

The gamma control with the non-linear gain block is chosen as the result of the optimization process (after 100 generations). With the genetically derived values of the parameters of the PI controller and the non-linear gain block the total value of the performance criteria increased by five per cent in comparison with the value of criteria obtained with the original values of the parameters provided with the CIGRE Benchmark Model. System responses for all events are better according to the performance criteria described above. Results for *Event 1* and *Event 2* are presented in Figure 5.12 and Figure 5.13 respectively.

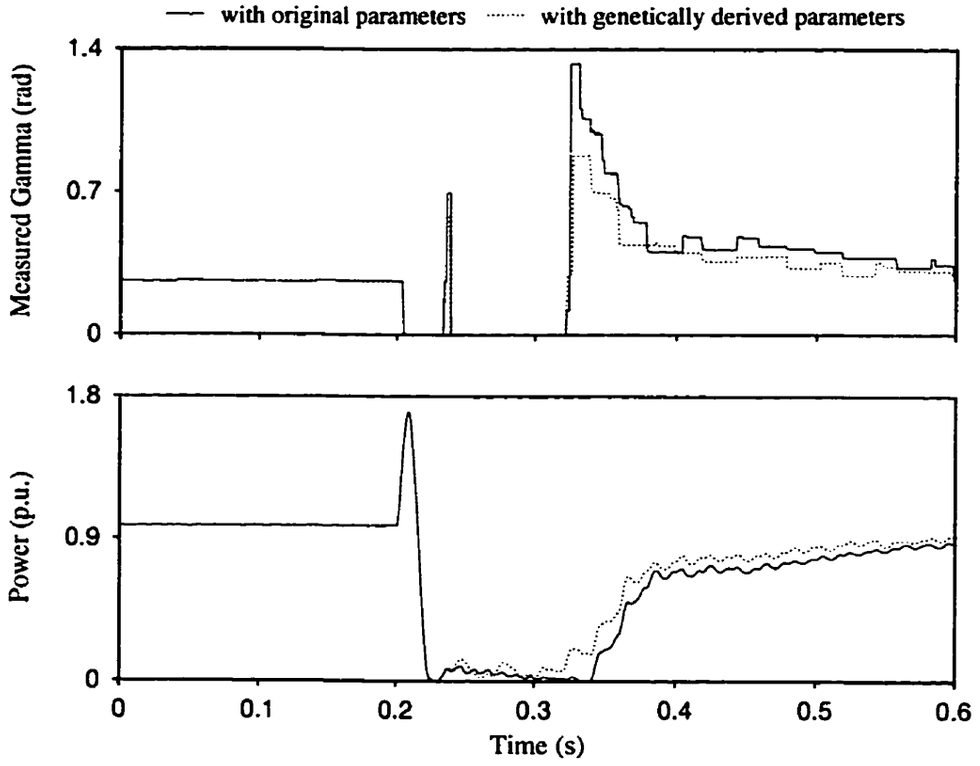


Figure 5.13: System response for *Event 2* with CIGRE Benchmark.

Chapter 6

ASVC at ac/dc Interconnection – the Study System

In order to investigate the performance of ASVC at an ac/dc interconnection some choices have been made regarding a study system, the ASVC, and a tool for control design. The CIGRE Benchmark Model [3] has been chosen as the study system. This choice has been motivated by the fact that the Model has been established to provide a common reference system to researchers conducting comparative performance studies, either of various devices or of control concepts. Some modifications of the system have been carried out to create a very weak ac system at the inverter site. In the case of the ASVC, a 12-pulse ASVC has been chosen. Its components and ratings are discussed here. The *GeneticEMTDC* program has been used to design a control of the ASVC. Its application in designing a control of HVdc systems (presented in section 5.4, page 46), has confirmed its usability. An extension and modification have been carried out to make this tool quicker and more efficient.

6.1 ac/dc System

The study system, shown in Figure 6.1, is developed using the CIGRE Benchmark Model as modified by Om Nayak [33]. It is a 1000MW, 500kV, 12 pulse, monopolar cable HVdc system. The inverter SCR is changed to $1.5\lfloor -75^{\circ}$ corresponding to a very weak ac system. At the inverter site, the damped high frequency and low frequency filters are resized to provide 300 Mvar while keeping their impedance frequency response

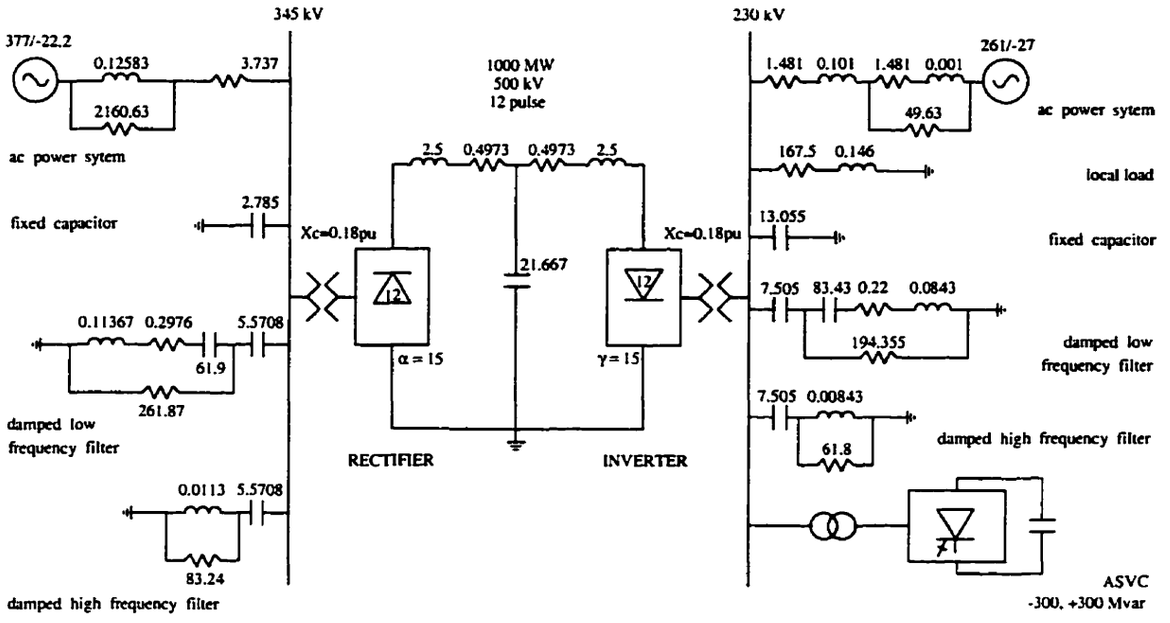


Figure 6.1: Modified Cigre Benchmark model.

profile similar to that in the Benchmark. Fixed capacitor banks are replaced by the ASVC of suitable rating to compensate fully for the inverter reactive power requirement. Additionally, a local R-L load of 300 MVA with a power factor of 0.95 is added at the inverter ac bus to represent the damping and the regulating effects of the local loads. The inverter site ac system is modified accordingly, to ensure that the load flow at the inverter bus is unchanged. The rectifier SCR is $2.5\lfloor -84^{\circ}$ corresponding to a relatively stronger system.

The nominal frequency of the study system is 60 Hz (North American standard) whereas the nominal frequency of the Benchmark Model is 50 Hz (European standard).

6.2 ASVC

The ASVC model used here is a 12-pulse ASVC presented in Figure 6.2. The ASVC transformers are modeled by six single phase transformers with series connections of the corresponding primary windings. The rating of the ASVC is ±300 Mvar. It is the result of requirements for reactive power at the inverter site and dynamic control of

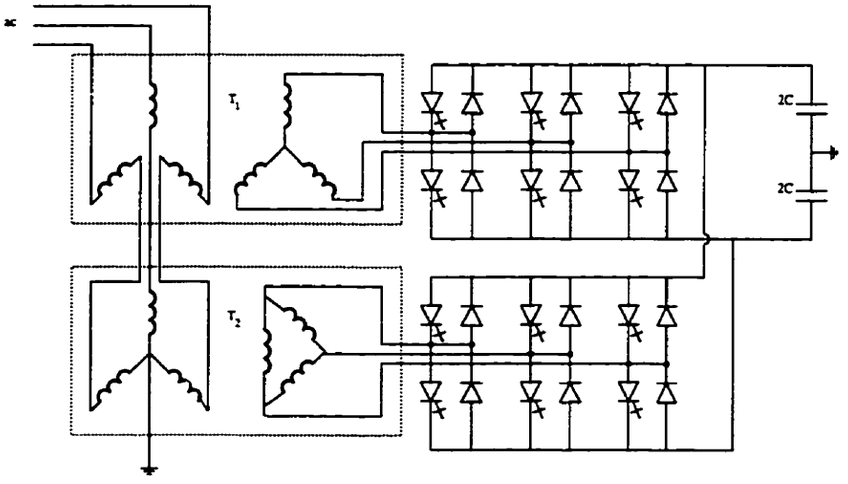


Figure 6.2: 12-pulse ASVC.

the inverter voltage. At the steady state, the filters supply 300 Mvar and the ASVC supplies the remaining 260 Mvar. However, the ASVC of a slightly higher rating is used to provide some additional control range. Since the ASVC behaves symmetrically the inductive rating is equal to the capacitive rating.

In order to meet this rating with currently available GTOs a multi-pulse ASVC with a high number of pulses would be needed. To limit the complexity of the model, a 12-pulse ASVC with ability to produce ±300 Mvar, is used here. With such assumptions the ASVC is designed using the extended version of the harmonic based method for power circuit design (section 3.3.2, page 22). The ratings of the step-down transformer are the same as those of the transformer applied to a synchronous condenser for the Nelson River HVdc system [50]. The turns ratio is 230kV/13.8kV and the transformers reactance is set at 8.5 per cent on a 300 MVA base. According to these data and using the program described in section 3.3.3, page 23, the following values are obtained:

V_{dc}	8.85 kV
dV_{dc}	0.76 kV

The value of $X_l = 0.085$ p.u. results in $THD_i = 0.125$. To prevent further increase in the value of THD_i and to ensure acceptable behavior of the ASVC under unbalanced conditions the requirements regarding dc ripples are specified high: the value of K_V

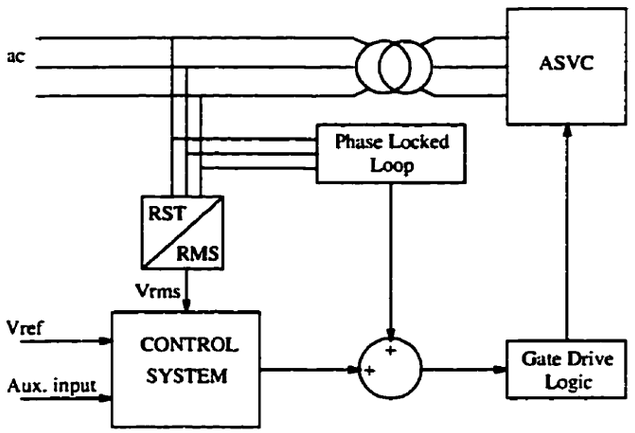


Figure 6.3: The basic control loop for the ASVC.

The master-slave model is used. In this paradigm a "control" program termed "the master" is responsible for process spawning, initialization, collection of results, and the timing of functions. The slave programs perform the actual computation allocated by the master.

In the distributed system which is developed, the master part performs genetic operations such as the creation of the initial population, crossover, and mutation. It also manages the evaluation process. The master part initiates slave programs, each of which is an instance of the *GeneticEMTDC* and it sends sets of parameters for evaluation and collects the results, Figure 6.4.

The master allocates tasks to slaves using a method of dynamic load balancing which is suitable where a computer network consists of fast and slow machines. According to this method, a new set of parameters is sent to a slave after the results of a simulation with previously sent parameters have been received. With such an approach the workload is shared unevenly – faster machines perform more simulations. Some management functions are also implemented within the master program. A special configuration file, which is read after each generation, specifies which machines can be used and at what time. In the case of unnatural termination of a slave, and the addition/deletion of machines, a proper procedure is activated by the master in order to return to the conditions existing before the event occurred.

The *GeneticEMTDC* program used as a slave is a modified version of the program

In the case of GAs used in the *GeneticEMTDC* program, some compromise is achieved. The application of genetic optimization in chapters 7 and 8 means that the values of continuous, as well as binary parameters have to be adjusted. The reason that binary parameters are used is related to the application of *GeneticEMTDC* to optimize a structure of a control system. Therefore, GAs with mixed representation of problem parameters is used. Using this approach, a part of a chromosome is a sequence of floating point numbers, and a part is a string of bits.

Chapter 7

Design of ASVC Control System

The investigation of performance of the ASVC at an ac/dc interconnection has been performed using the ASVC with a simple control system (only the PI controller). In this case it has seemed impossible to obtain an acceptable performance of the ASVC for different ac and dc faults. In order to solve this problem, an attempt has been made to design a new control for the ASVC. The genetic control design method proposed in chapter 5, page 38, has been applied. The optimization process of a function which embraced the objectives of ASVC control system has been carried out to adjust the structure of a control system and the values of control parameters.

A control for the ASVC has been designed for the case of the most severe disturbance at an ac/dc interconnection – the inverter close-in single phase to ground fault.

7.1 Objectives of ASVC Control

Design via optimization means that reasonable performance indices are needed to guide the designing process. Performance indices represent the objectives of a control system, and are quantitative measures showing how far the performance of the system is from a desired one. In the case of the ASVC located at an ac/dc interconnection, four different objectives related to the ASVC, to the ac system, and to the dc system, are taken into account.

The requirement to keep the value of the ASVC current within the specified limits is one of the most important objectives of an ASVC control. Limitation of the current

which flows through GTOs ensures the ASVC can work without interruption. This requirement is represented in the optimization process by the following performance index:

$$PIndex_1 := \int_{t_{flt\_clr}}^{t_{sim}} (e_{I_{ASVCq}})^2 \, dt, \tag{7.1}$$

where $e_{I_{ASVCq}} = I_{ASVCq_{ref}} - I_{ASVCq_{measured}}$, t_{sim} is a time of simulation and is equal 1 *sec.* in all simulation in chapters 7 and 8, and t_{flt_clr} is a time the fault is cleared – in all simulations it is equal 0.075 *sec.* This index is used to create the following partial fitness function:

$$FitFun_1 := A_1 - B_1 * PIndex_1, \tag{7.2}$$

where the constants A_1 and B_1 are used, as defined in section 5.4.1, page 46, for adjustment of the index importance – A_1, and for its normalization – B_1.

Keeping the ac voltage at the inverter bus at the level of 1 p.u. is the main purpose of application of the ASVC as a voltage control device. This objective is expressed by two performance indices:

$$PIndex_{2,a} := \int_{t_{flt\_clr}}^{t_{sim}} (e_{V_{inv}})^2 \, dt, \tag{7.3}$$

$$PIndex_{2,b} := \int_{t_{flt\_clr}}^{t_{sim}} \mid (e_{V_{inv}}) \mid \; t \, dt, \tag{7.4}$$

with $e_{V_{inv}} = V_{inv_{ref}} - V_{inv_{measured}}$. In this case the partial fitness function is built using these indices is as follows:

$$FitFun_2 := \sum_{j \in \{a,b\}} (A_{2,j} - B_{2,j} * PIndex_{2,j}), \tag{7.5}$$

where As and Bs are as described above.

Taking into account the HVdc system, one of the most important aspects of its recovery after a disturbance is a fast return of the dc power to a level above 0.8 p.u. This requirement results in the following different performance indices:

$$PIndex_{3,a} := SettlingTime_{power}, \tag{7.6}$$

where $SettlingTime_{power} := t_{sim} - min(t_s : \forall t \in (t_s, t_{sim} \mid e(t)_{power} \mid \leq 0.05)$,

$$PIndex_{3,b} := \int_{t_{flt\_clr}}^{t_{sim}} \mid (e_{power}) \mid \; t \; dt, \tag{7.7}$$

where $e_{power} = power_{ref} - power_{measured}$, and

$$PIndex_{3,c} := \int_{t_{flt\_clr}}^{t_{sim}} \mid \frac{dpower}{dt} \mid \; dt. \tag{7.8}$$

In the case of $PIndex_{3,c}$ the integration is performed only when the derivative $\frac{dpower}{dt}$ is less then zero. The definition of partial fitness function in the case when one of the indices ($PIndex_{3,a}$) has to be maximized is:

$$FitFun_3 := C_{3,a} * PIndex_{3,a} + \sum_{j \in \{b,c\}} (A_{3,j} - B_{3,j} * PIndex_{3,j}) \tag{7.9}$$

where the meaning of the constant C is similar to that one of the constant B.

An application of the ASVC at an ac/dc interconnection forces one more objective which is directly related to the behavior of the inverter. The ASVC as a voltage control device should prevent commutation failures of the inverter during a recovery time. This objective, already included implicitly in the previous two objectives, is expressed as a special index – a counter of commutation failures.

$$PIndex_4 := counter\_of\_commutation\_failures \tag{7.10}$$

The objectives presented above have different priorities. To reflect this a special arrangement of the partial fitness functions is proposed and applied. The hierarchy of the partial fitness functions is expressed with the help of a ramp function which is defined in the following way:

$$f_{ramp}(x) = \begin{cases} 0.0 & if \; x < 0.0 \\ \frac{1}{threshold} * x & if \; 0.0 \leq x < threshold \\ 1.0 & if \; x \geq threshold \end{cases} . \tag{7.11}$$

The value of *threshold* is equal A_1 for the case of $f_{ramp}(FitFun_1)$, and $A_{2,a} + A_{2,b}$ for $f_{ramp}(FitFun_2 * f_{ramp}(FitFun_1))$. This means that f_{ramp} expresses the idea that the value of a partial fitness function with a lower priority depends on the value of a partial fitness function with a higher priority.

The final form of the fitness function whose value is maximized is presented below:

$$\begin{aligned} FitFun \;:=\; & PIndex_4 * \\ & [FitFun_1 + \\ & FitFun_2 * f_{ramp}(FitFun_1) + \\ & FitFun_3 * f_{ramp}(FitFun_2 * f_{ramp}(FitFun_1))] \end{aligned} \tag{7.12}$$

7.2 Standard Control

Adjustment of a control structure using the *GeneticEMTDC* (see section 5.4.2, page 54), performed via optimization means an automatic choice of the best control structure from a set of alternative control structures prepared by a designer. To design an ASVC control, this method is applied in a form which can lead eventually to automatic design of a control system. The first step is to distinguish a set of all possible signals which can be used as input signals to a control system to be designed. In the case of an ASVC control five signals are chosen: V_{inv}, $error_{V_{inv}}$, I_{ASVC}, $error_{I_{ASVC}}$, and *fault detection* signal. The second step is to prepare many alternative structures of a control system. It is achieved in such a way that many different control system components are arbitrarily connected using binary multiplexers. The control inputs of these multiplexers are used as parameters whose values are adjusted in the optimization process. Each set of the values of these parameters identifies one particular structure of a control system. Controllers (P, PI, PD, PID), components representing different functions (delay, memory, maximum, minimum, product), and multiplexers are connected together and compose a generic structure of a control system; a part of which is represented in Figure 7.1. It contains all those structures from which the best control system is extracted during the optimization process. An application of eight multiplexers results in about one hundred different structures. Fifteen different parameters of control components are also adjusted during the optimization. Finally, the fitness function (section 7.1, page 69), is optimized by finding the values of twenty five parameters: twenty-three parameters regarding the control system – eight of these are binary, and seventeen are floating point; and two parameters of the PLL circuit – proportional gain GP, and integral gain GI (section 6.2, page 63).

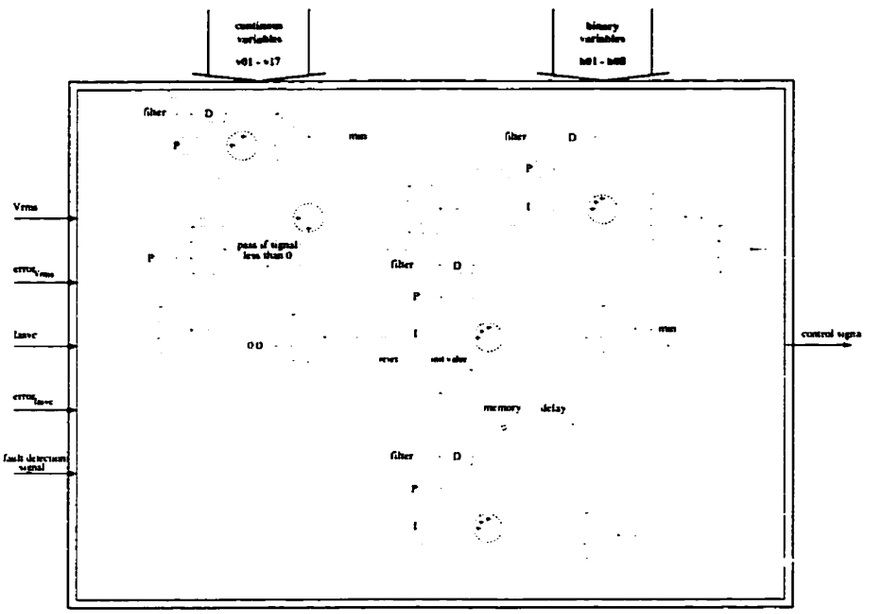


Figure 7.1: Optimization of control structure – idea.

During the design process the *GeneticEMTDC* program is run several times using different values of genetic parameters. Crossover probability is changing in the range from 0.7 to 0.9, mutation probability is between 0.1 and 0.04. The size of population is constant – 100, as well as the number of generations – 150. Two structures of the control system are identified most often as the result of all performed optimizations. The first of these structures, called herein system A, is presented in Figure 7.2. The components of this system (solid line) are chosen from all components of generic structure (some elements of generic structure are indicated by dotted lines). The values of control parameters and GP, GI of PLL are adjusted simultaneously. All values are presented in Appendix C.1. In the case of this control system two signals, $error_V$ and $error_{I_{ASVC}}$, are processed independently and the minimum of both control signals is added to the output of the PLL circuit in order to adjust the GTO firing angle (Figure 6.3). In the $error_V$ path a PID controller which can be reset and initialized at the time of fault is used. A brief description of this controller is presented in section 8.1, page 83. The second structure – system B – is shown in Figure 7.3 as a set of components (solid line) chosen from a generic structure (dotted line). In this system the minimum of $error_V$

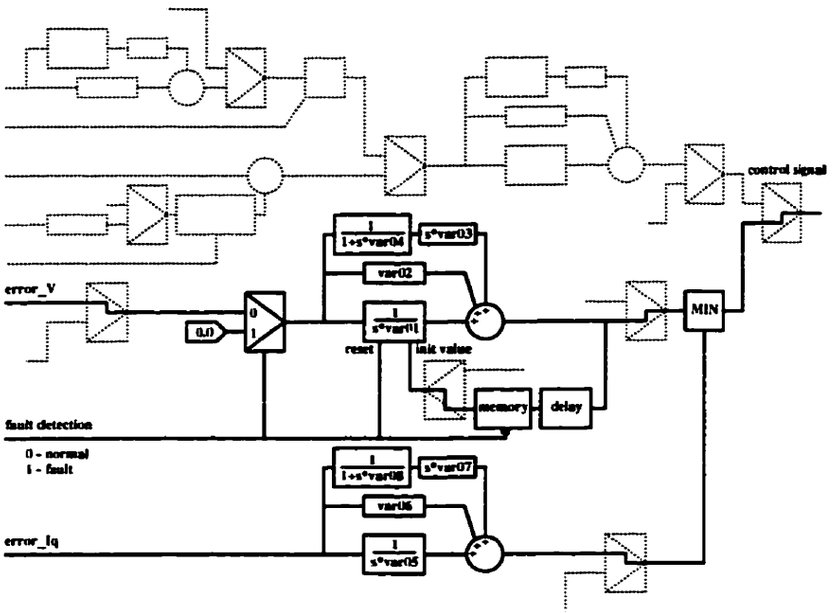


Figure 7.2: Control system A (solid line) obtained in the optimization process as the best system chosen from a generic structure (dotted line).

signal and earlier processed signal $error_{I_{ASVC}}$ is taken as the input to the PID controller. The values of all control parameters for system B, as well as GP, GI of PLL are included in Appendix C.2.

The performances of the ASVC with control system A and control system B in the case of the inverter close-in single phase to ground fault are presented in Figures 7.4 and 7.5 respectively.

As can be seen in both Figures the recovery of ac RMS voltage is fast – V_{INV} reaches 1 p.u. value in 35 ms after the fault is cleared. After a small overvoltage (about 10 per cent in the case of system B) and undervoltage – 15-20 per cent, the value of the ac voltage becomes equal to 1 p.u. (± 2 per cent) at about 335 ms after the fault is cleared. It seems that a very similar pattern is repeated in the case of the dc power. Initially the dc power reaches the value of 0.8 p.u. in about 75 ms and then it decreases to about 0.7 p.u. The value of the dc power is permanently above 0.8 p.u. at about 235 ms after the fault is cleared.

To determine the influence of ASVC current requirement on dc power recovery a

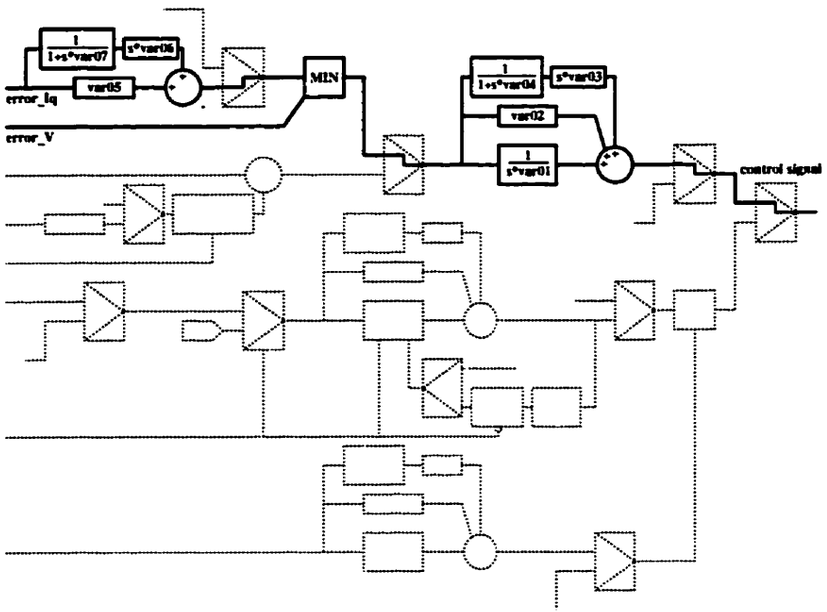


Figure 7.3: Control system A (solid line) obtained in the optimization process as the best system chosen from a generic structure (dotted line).

new experiment is conducted. In this case the fitness function is created using only two partial fitness function $FitFun_1$ and $FitFun_3$, see section 7.1, page 69. These two partial fitness functions are added without using a ramp function:

$$FitFun := PIndex_4 * [FitFun_1 + FitFun_3]. \tag{7.13}$$

As a result of the optimization process a control system, called herein C and presented in Figure 7.6, is chosen. In this control system, signal $error_V$ is modified by the addition of a processed value of I_{ASVC} under the condition that $error_{I_{ASVC}}$ is less than zero. The values of control parameters of this system are included in Appendix C.3.

The ASVC performance is presented in Figure 7.7. In this case the dc power reaches 0.8 p.u value at the time of 65 ms after clearance of the fault. Its value is under 0.8 p.u. and decreases up to 0.75 p.u. for the period of 40 ms. The value of the dc power is above 0.8 p.u. at 165 ms after the fault is cleared. On the other hand, such a recovery is obtained with a 20 per cent overvoltage, as well as large overcurrent in the case of the ASVC.

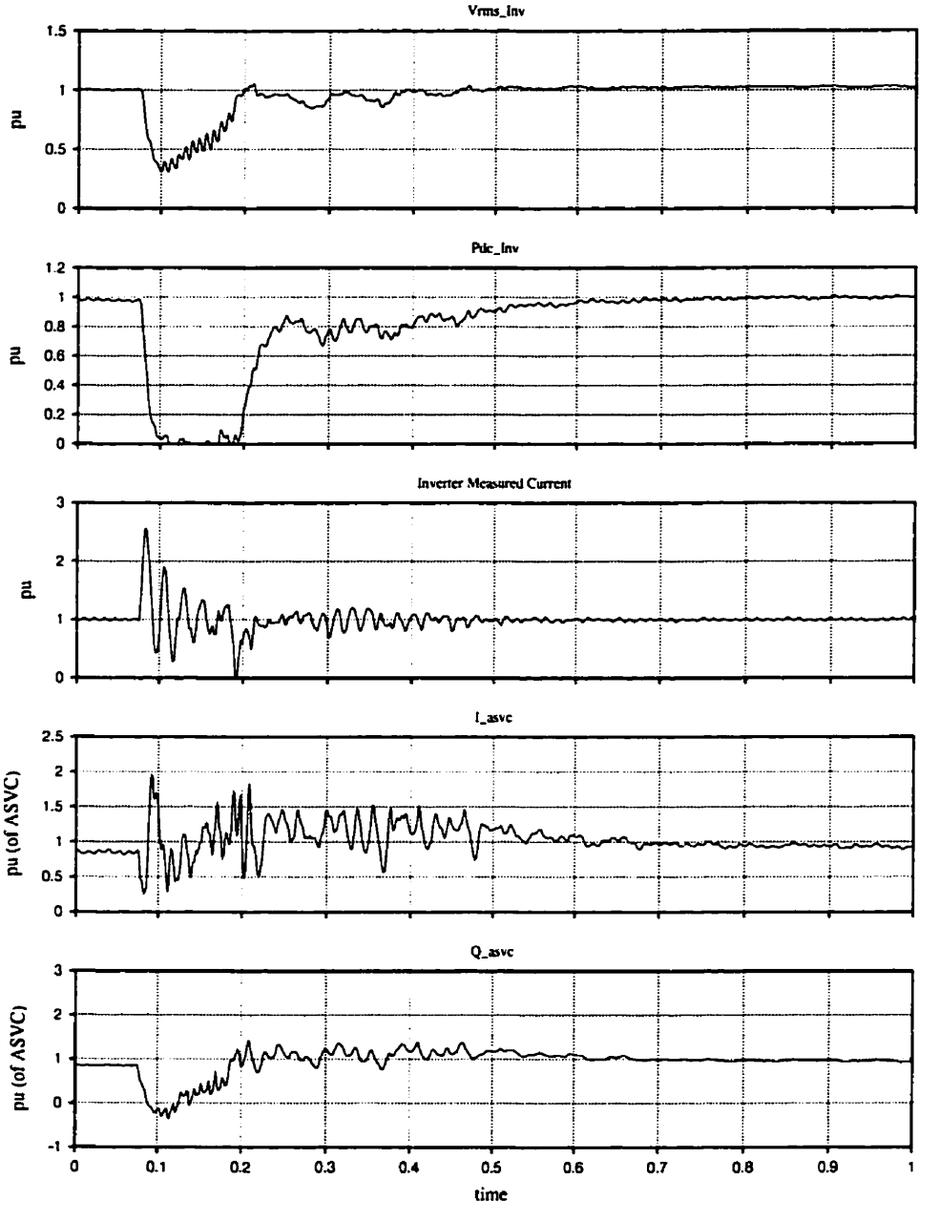


Figure 7.4: Inverter single phase to ground fault – control system structure A.

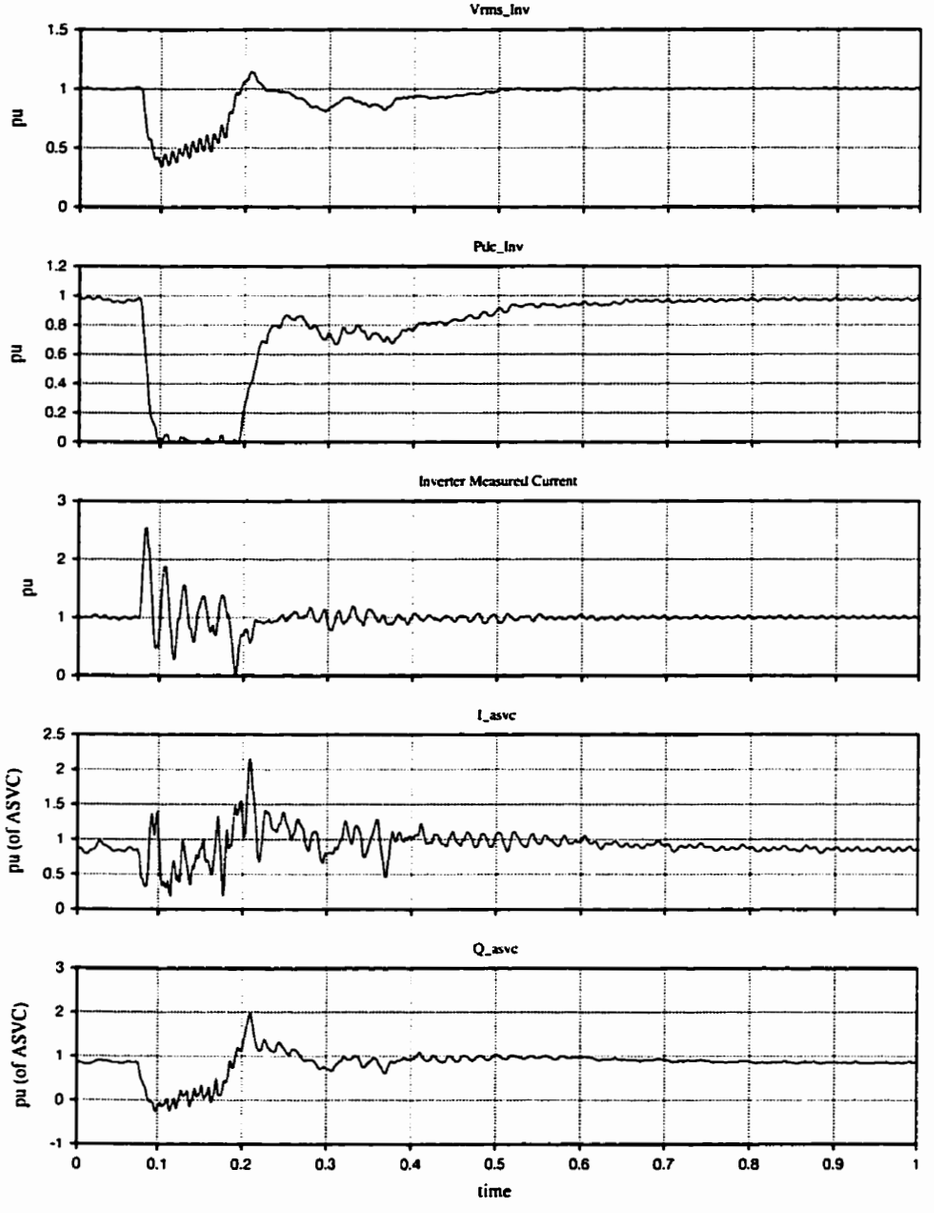


Figure 7.5: Inverter single phase to ground fault – control system structure B.

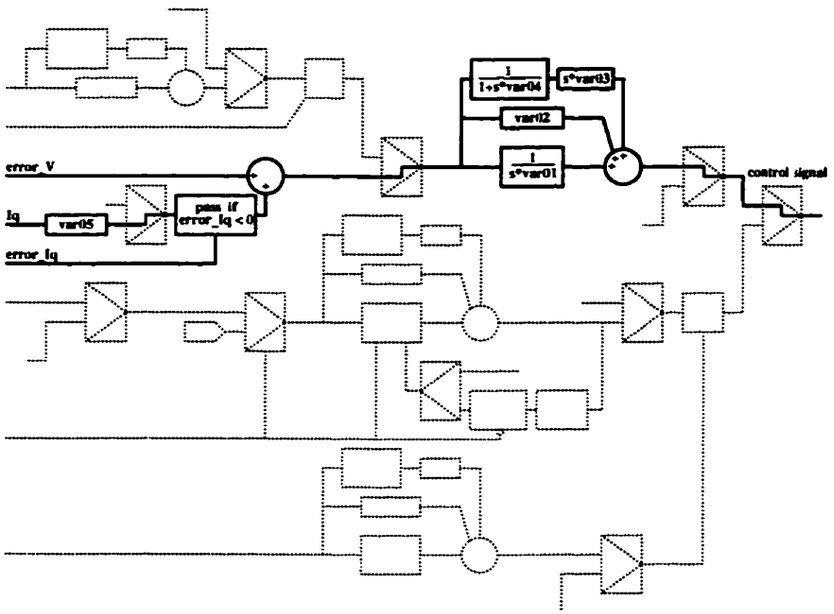


Figure 7.6: Control system structure obtain in the optimization process with loosen requirements.

7.3 Control with Fuzzy Gain Scheduling

An approach using fuzzy gain scheduling of the PID controller is investigated to improve the performance of the ASVC. In the original idea of fuzzy gain scheduling, Figure 7.8, fuzzy logic is used to tune the PID controller on-line if the response of the closed loop system is not acceptable [59]. In the concept presented here, a slightly different approach is applied [57] and fuzzy logic is used to schedule off-line tuned parameters. It means that based on the value of error, different sets of the earlier found or calculated values are assigned to the parameters of PID controllers.

The fuzzy gain scheduling proposed and applied in the case of the ASVC is presented in Figure 7.9. Two different sets of PID parameters are considered: one for the case when the value of $error_V$ is positive and large - $\{Gp_P, Ti_P, Td_P\}$, one for the case when $error_V$ is negative and around zero - $\{Gp_{NZ}, Ti_{NZ}, Td_{NZ}\}$. Two sets of parameter values means that two membership functions have to be defined (see $FUZZY\,RULES$ in Figure 7.9). The value of each membership function, respectively μ_P and μ_{NZ} calculated

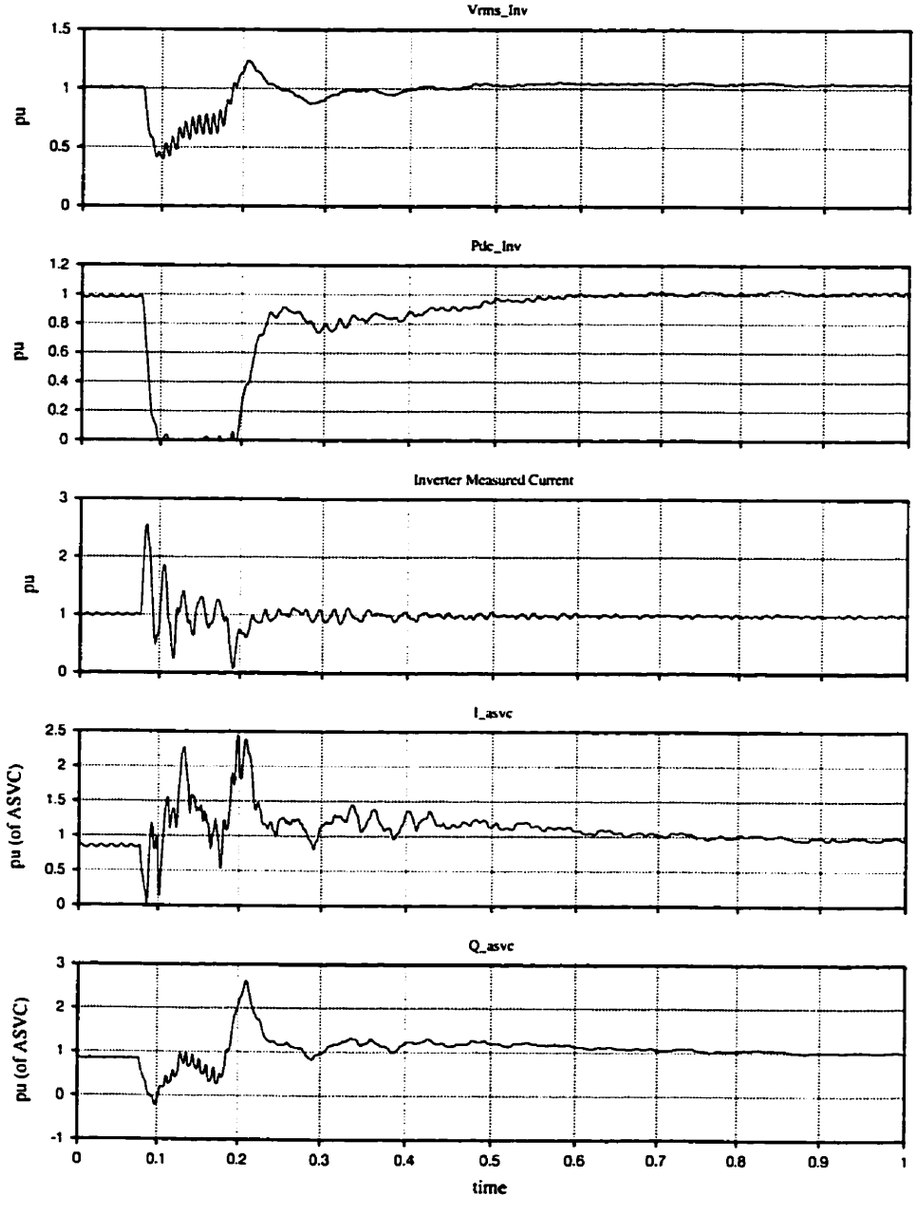


Figure 7.7: Inverter single phase to ground fault – loosen requirements.

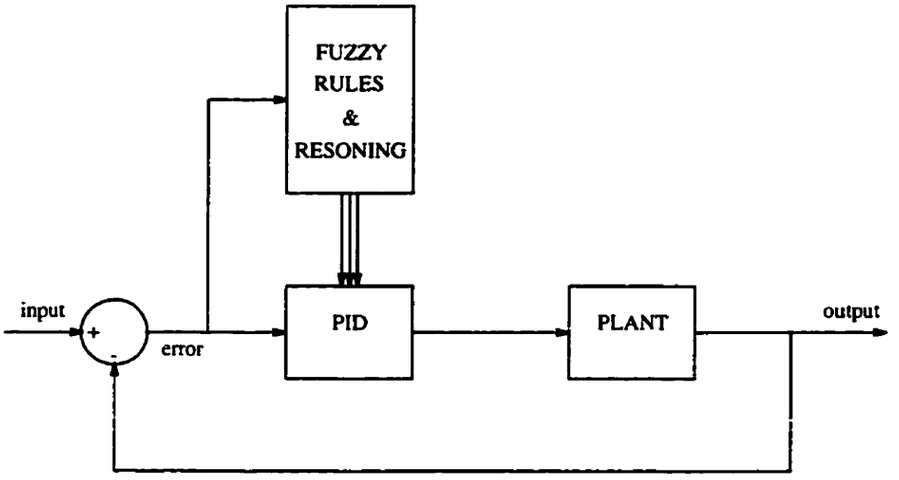


Figure 7.8: Fuzzy gain scheduling – idea.

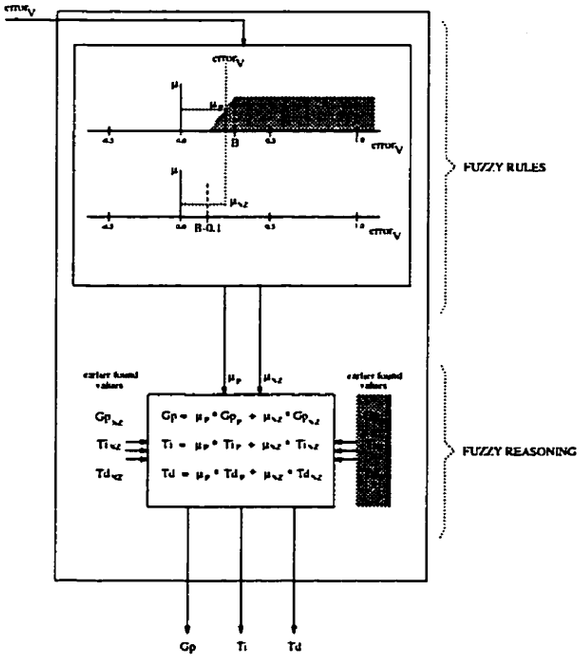


Figure 7.9: Fuzzy gain scheduling – realization.

for a given value of $error_V$, represents the degree of activation of the corresponding set of parameter values. In the approach presented, the following condition regarding membership function values is valid:

$$\sum_{i\in\{NZ,P\}} \mu_i = 1. \tag{7.14}$$

Using μ_P and μ_{NZ} the values of PID parameters are calculated according to the following equations:

$$Gp = \sum_{i\in\{NZ,P\}} \mu_i * Gp_i \tag{7.15}$$

$$Ti = \sum_{i\in\{NZ,P\}} \mu_i * Ti_i \tag{7.16}$$

$$Td = \sum_{i\in\{NZ,P\}} \mu_i * Td_i \tag{7.17}$$

The values Gp, Ti, Td are then assigned to the PID parameters.

Using the optimization process of the $GeneticEMTDC$ the values of Gp_P, Ti_P, Td_P, Gp_{NZ}, Ti_{NZ}, Td_{NZ}, as well as B (see Figure 7.9) are found. The system A (Figure 7.2) is chosen as the ASVC control system. In total, fifteen parameter values are adjusted in this experiment. The values of all these parameters are presented in Appendix C.4. The fitness function defined in section 7.1, page 69, is used here as the optimized function representing the objectives of the ASVC control system.

The performance of the ASVC with fuzzy gain scheduling control is presented in Figure 7.10 together with the performance of the ASVC with the control system C – section 7.2, page 72. The recovery of the dc power in this case seems similar to the one obtained as the result of application of control system C. The difference is that there is no overvoltage and only a small overcurrent. This means that the system performs in a better fashion when the fuzzy gain scheduling concept is applied.

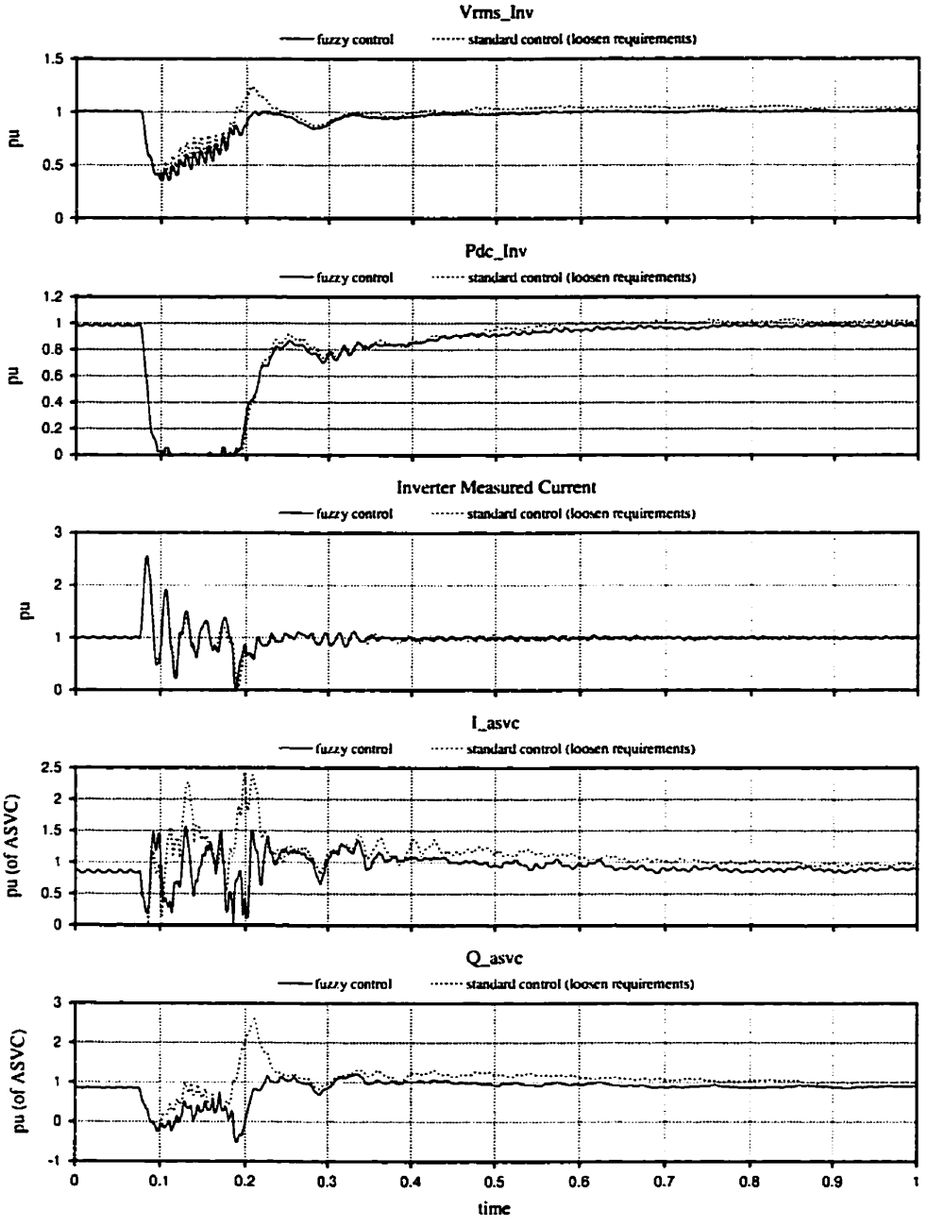


Figure 7.10: ASVC response to 1 phase ac fault: fuzzy control versus standard one (with loosen requirements).

Chapter 8

Performance of ASVC at ac/dc Interconnection

Initial experiments indicated that it is difficult to obtain one set of parameters which would give satisfactory performance for all considered events – ac faults at the rectifier and inverter sites, and dc faults. An application of the concept of changing the values of control parameters depending on the state of the controlled system has been proposed as a solution to this problem.

This approach has been investigated and this chapter includes a description of applied control structure, a process of parameters values adjustment, and the results of simulations.

8.1 ASVC Control Scheme

The concept of changing the values of control parameters depending on the state of the system became realizable due to two control elements: the PID controller which can be reset and initialized, and the fault detector. These components are created on the basis of the real control elements of the Nelson River HVdc link [1]. The PID controller with a special logic for its resetting and initialization is presented in Figure 8.1. Using this kind of controller, the output value can be kept constant and equal to the output value from the past. In the normal operation of a controller, when the signal *event detection*

[1] Personal communication with Peter Kuffel from the Manitoba Hydro Planning Department.

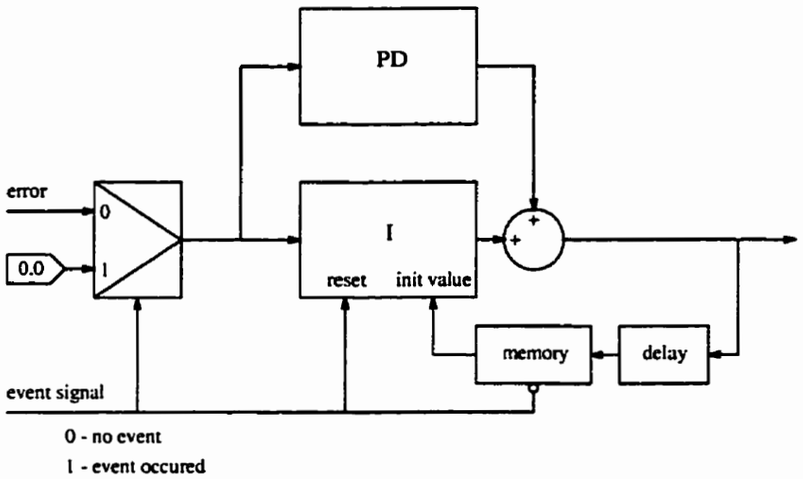


Figure 8.1: PID controller with special logic for resetting and initialization.

equals 0, the PID performs its task and the value of the PID output from the point of time *current time* − *delay* is stored in the *memory*. When an event occurs, signal *event detection* equals 1, the integration part is reset to the value from the *memory*, writing to the *memory* stops (it takes place only when *event detection* equals 0) and the value 0.0 is put to the input of the controller. In this state it is possible to change the values of controller parameters without transient change in the controller output. In the concept proposed, the fault detection signal is used as the *event detection* signal. At the time the fault occurs, the parameters of PID controller are set to the values appropriate for a given fault. The fault detector component is designed to detect single phase to ground fault and three phase to ground fault.

With the possibility of detecting two different faults in the concept proposed it becomes possible to define defining three different sets of the value of PID controller parameters: the first set for single phase to ground fault – called set_{one}, the second set for three phase to ground fault – set_{three}, and the third and final set for all other undetectable faults – ac fault at rectifier site and dc fault, called set_{other}. In such a case the control procedure is as follows. The values of PID parameters are equal to the values from set_{other} all the time when no detectable event occurs. This means that these values are used for the case of dc faults and ac faults at the rectifier site. When the inverter close-in single phase to ground fault is detected, the values of PID parameters

are changed to the values from set_{one}, and in the case of three phase to ground fault the values from set_{three} are assigned to PID parameters. This means that at the moment the fault is cleared, a proper set of parameters values is assigned to the PID. The process of returning to the values from set_{other} takes place after the value of $error_V$ is less than a specified value (here 2 per cent) for a specified period of time (200 ms). This exchange takes place in the following way: the values of parameters are changing in a linear fashion from the values of set_{one} or the values of set_{three} to the values of set_{other} over a specified period of time (400 ms).

Based on the concept of changing the values of PID parameters depending on a state of the controlled system two structures of ASVC control system are defined. One of them, Figure 8.2 (a), is the same as system A from chapter 7, page 69, and the other one, Figure 8.2 (b), is similar to system B, the only difference is in application of PID controller with resetting and initialization.

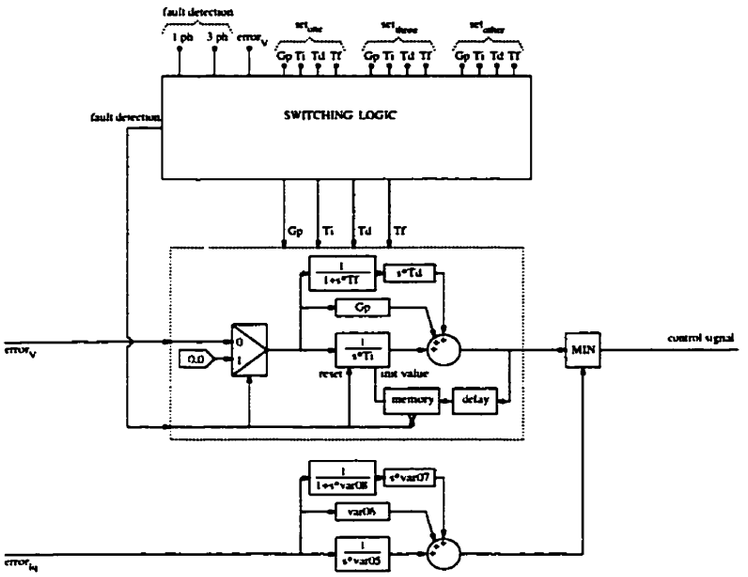
8.2 Optimization of Control System

Design of an ASVC control in the case of the proposed concept is performed in two stages.

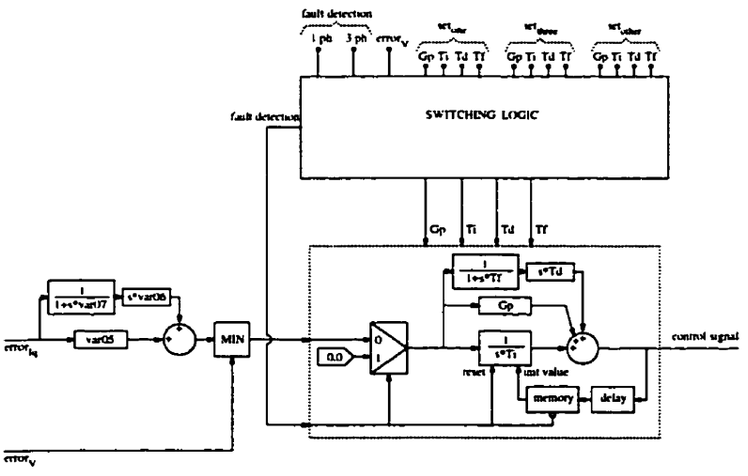
The First Stage

The aim of the first stage of the designing process is to find a structure of control system, the values of parameters of PID controller from set_{other}, the values of parameters of PID or PD controller in the path of $error_{I_{ASVC}}$ signal, and the values of two parameters of PLL circuit: GP and GI. This process is performed using $GeneticEMTDC$ which has optimized the performance of the ASVC for four events:

- the rectifier close-in single phase to ground fault,
- the rectifier close-in three phase to ground fault.
- the dc line fault,
- the permanent dc block,



(a)



(b)

Figure 8.2: Control schema.

The value of the optimized function is the sum of four partial values of fitness function. Each partial value is the result of a simulation run for a given event. In total, four simulations are necessary to evaluate one set of control parameters (section 5.2, page 41). In the case of ac faults the fitness function is the same as the one defined in section 7.1, page 69. For dc faults the fitness function is defined in the following way using partial fitness functions and performance index from section 7.1: $FitFun_1$ – representing the requirement of the ASVC current limit, $FitFun_2$ – representing the objective of keeping the value of V_{inv} at the level of 1 p.u., and index $PIndex_4$ which represents the requirements of preventing commutation failure. The only difference is a lower limit of integrals: instead of t_{flt_clr} (time_of_fault_clearence) the time of fault is used – t_{flt}. In this case the fitness function is as follows:

$$\begin{aligned} FitFun \;:=\; & PIndex_4 * \\ & [FitFun_1 + \\ & FitFun_2 * f_{ramp}(FitFun_1)]. \end{aligned} \tag{8.1}$$

As the result of the optimization process, a structure of control system is identified. In this case the structure presented in Figure 8.2 (b) is chosen. This structure, as well as the values of the parameters from set_{other}, $var05$, $var06$, $var07$, and the values of PLL circuit parameters GP, and GI are used in the second stage of the designing process. The values of parameters obtained in the first stage of the designing are presented in Appendix C.5.1.

The Second Stage

In the second stage, two optimization experiments are performed in an arbitrary sequence. The aim of one experiment is to find the values of the PID controller parameters for the event of the inverter close-in single phase to ground fault – i.e. the values from set_{one}. The same process is repeated for the event of the inverter close-in three phase to ground fault. As a result, the values of set_{three} are found. In both these experiments the fitness functions are the same as the function defined in section 7.1, page 69. The values of parameters from set_{one} and set_{three} are in Appendix C.5.2.

8.3 Disturbances

The sections which follow describe the performance of ASVC at an ac/dc interconnection under different disturbances using the control designed according to the concept proposed, and with the values of control parameters found in both optimization stages. All the ac faults are for a duration of five cycles. Details regarding dc faults are given in related sections.

8.3.1 Rectifier Faults

Rectifier Close-in Single Phase to Ground Fault

The rectifier single line to ground fault, presented in Figure 8.3, is not as severe as the corresponding inverter fault. The recovery time is much shorter. In the case of V_{INV} there are overvoltages and undervoltages, up to 10 per cent, during the fault. The dc power recovers to the level of 0.8 p.u. very quickly – about 30 ms after the fault is cleared. The values of ASVC current and generated power Q are within the limits.

Rectifier Close-in Three Phase to Ground Fault

As in the case of the rectifier single phase fault, this rectifier three phase to ground fault, Figure 8.4, is less severe than the corresponding fault at the inverter bus. The overvoltage and undervoltage do not exceed 15 per cent of p.u. value, and the dc power recovers to the value of 0.8 p.u. in 70 ms after clearance of the fault.

8.3.2 dc Faults

dc Line Fault

Fault on the dc side is created by short circuiting the dc line to ground at the mid-point of the dc cable. The fault is cleared by force-retarding the firing angle at the rectifier and inverter. The firing angle at the converters is increased to 135^o and maintained at that level for 100 ms. After this time the firing angle is gradually ramped back to 0^o during the next 100 ms so that the normal control modes could take over.

Figure 8.5 shows the performance of the system during such a fault. The overvoltage, at the beginning with peak values of 25 per cent, then about 20 per cent, can be observed

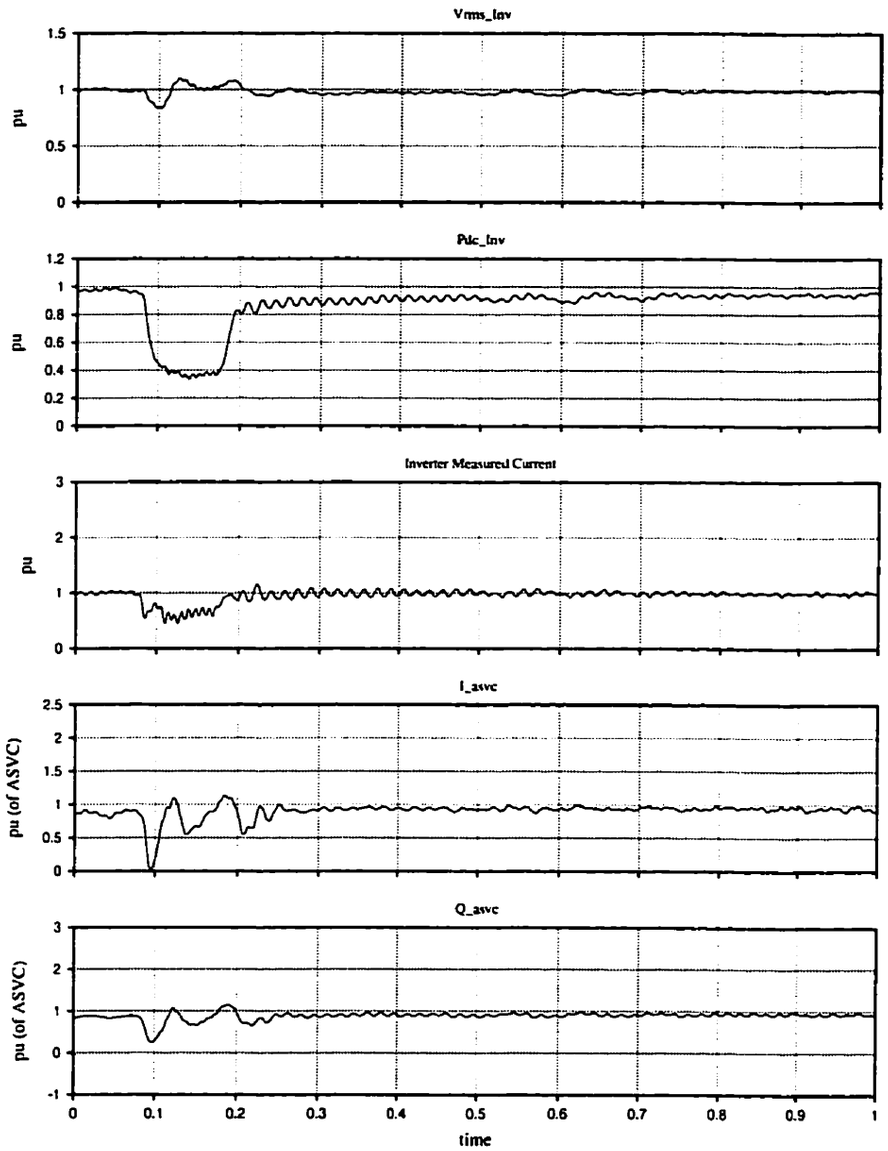


Figure 8.3: Rectifier single phase to ground fault.

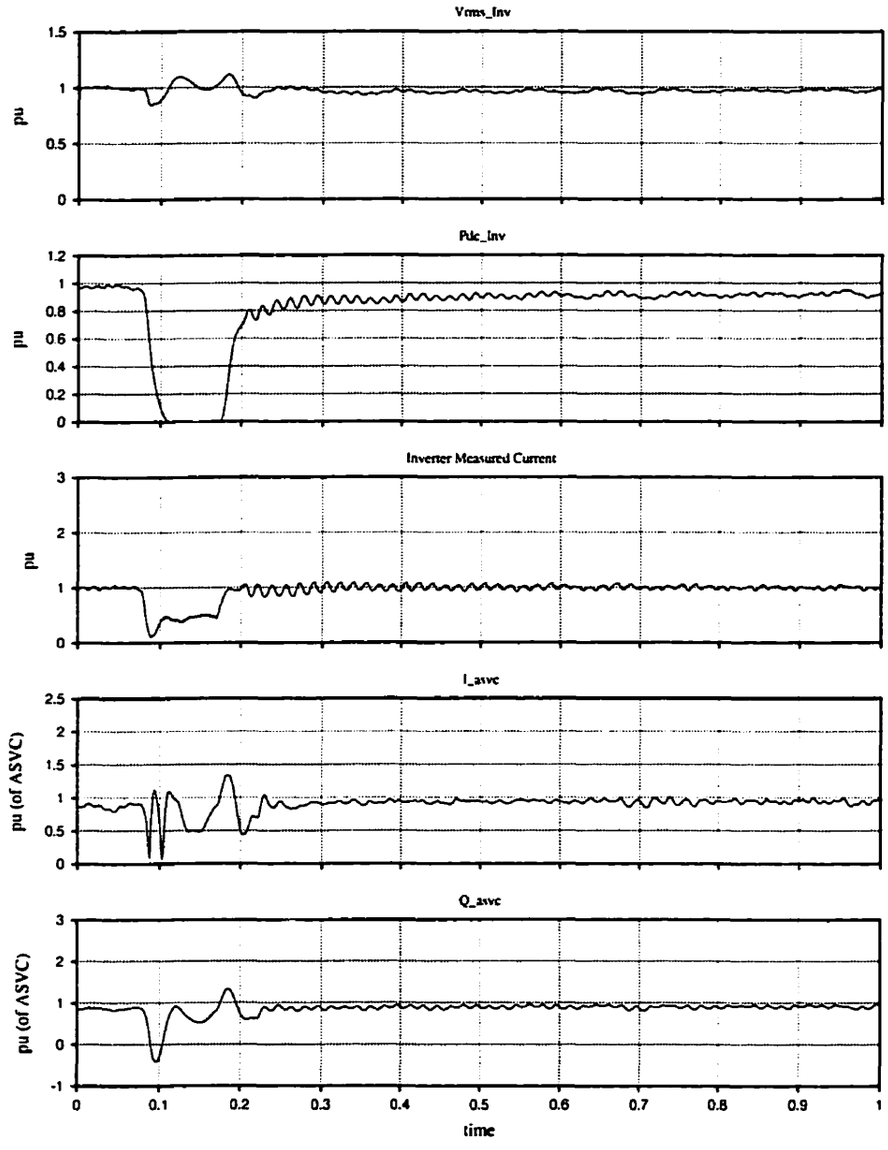


Figure 8.4: Rectifier three phase to ground fault.

during the fault. The dc power recovery is fast and takes about 110 ms.

Permanent dc Block

The voltage at the inverter ac bus is shown in Figure 8.6. The interesting observation is that just at the beginning of the dc block there is undervoltage and no overvoltage. This is because when ac bus voltage attempts to increase while the ASVC voltage remains relatively constant, the current flow is automatically reversed and the ASVC absorbs reactive power. After a while the overvoltage occurred – first up to 17 per cent, then up to 10 per cent.

8.3.3 Inverter Faults

Inverter Close-in Single Phase to Ground Fault

The performance of the ac/dc system in the case of the inverter close-in single phase to ground fault is presented in Figure 8.7. As can be seen, an application of the concept of changing the values of parameters depending on a state of the system results in almost the same system behavior which is obtained when the control system is designed for only one event – single fault to ground, see chapter 7, page 69. With an undervoltage of up to 20 per cent the dc power recovery is slowed down after a fast increase. At the beginning there is a power peak, the level of 0.8 p.u. is passed after 70 ms, and then the value of the dc power decreased. The level of 0.8 p.u. is permanently reached in 255 ms after the fault is cleared.

To confirm the need for the applied control concept and to show that the values of PID parameters from set_{one} are exceptionally good for exactly this kind of fault a comparison is carried out. Using the values of PID controller from three different sets, set_{one}, set_{other} and set_{three}, the behavior of the system in the case of single phase fault to ground is investigated. The results of these experiments are presented in Figure 8.8. As can be seen, only the control with the values from set_{one} gives acceptable results. Using the control concept described in this chapter it is possible to use the values of control parameters which produce the best result, without any compromises, for a given event.

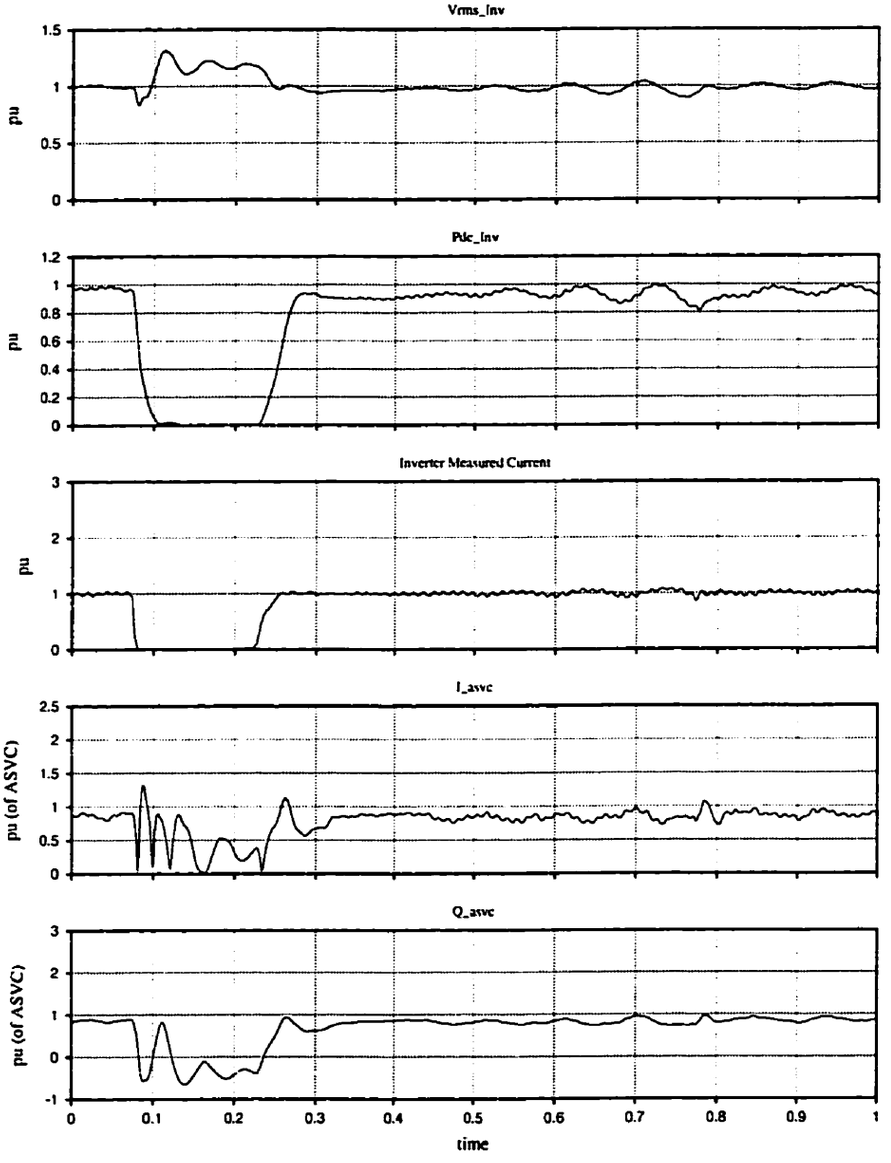


Figure 8.5: dc fault.

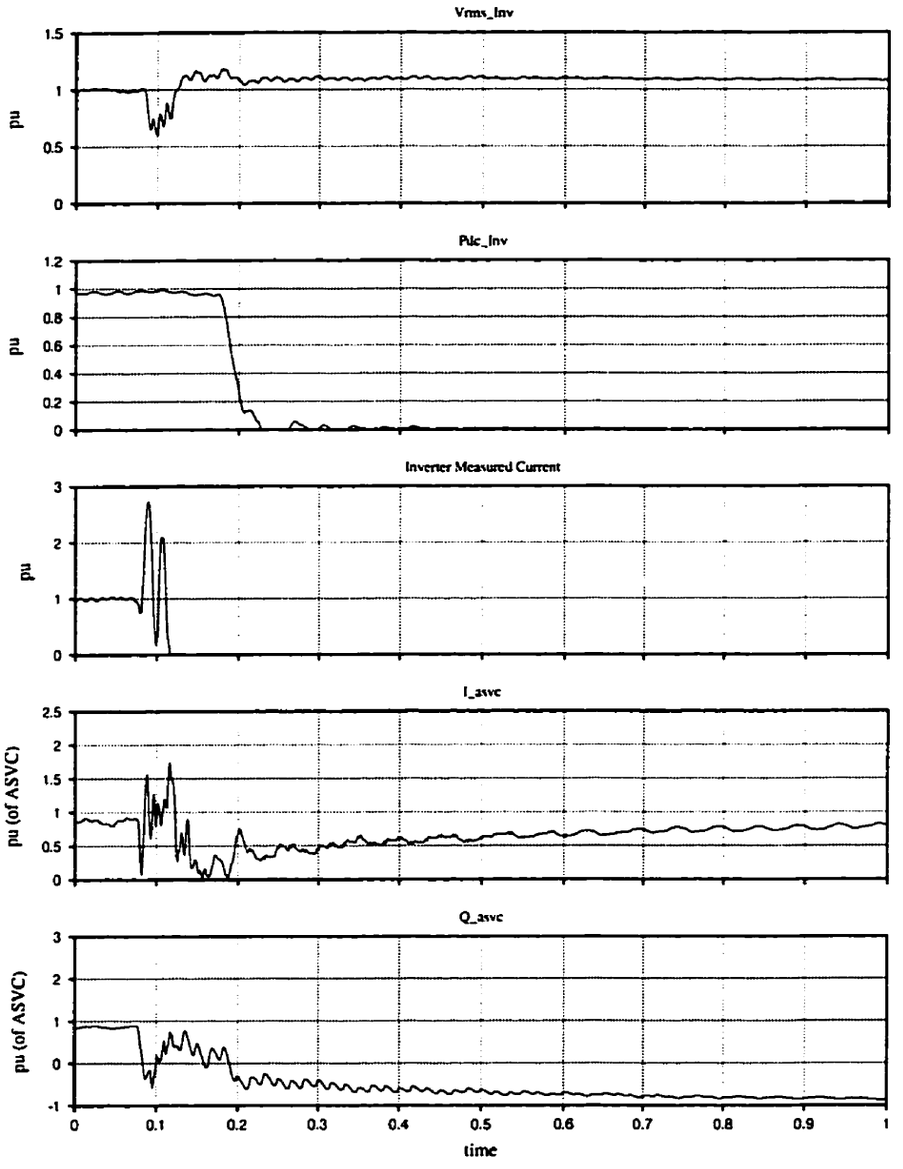


Figure 8.6: dc blocking.

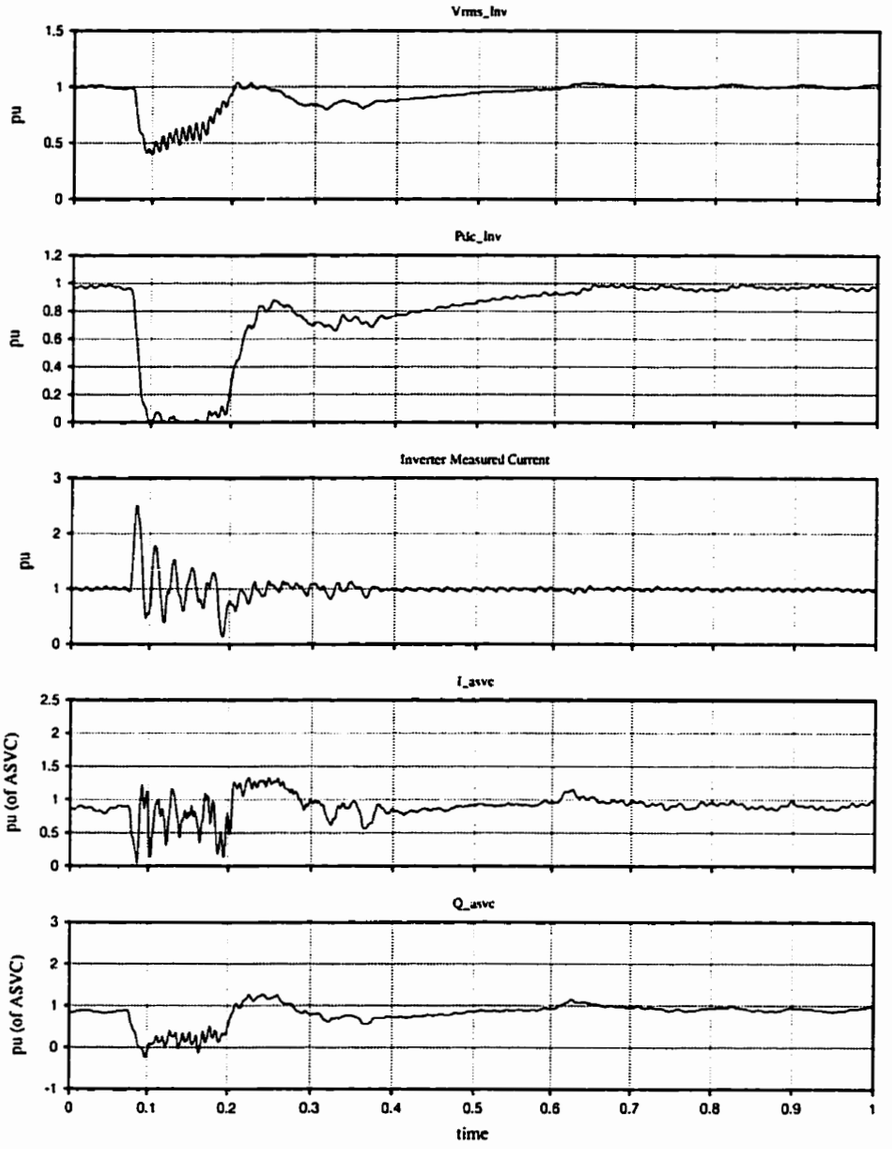


Figure 8.7: Inverter single phase to ground fault.

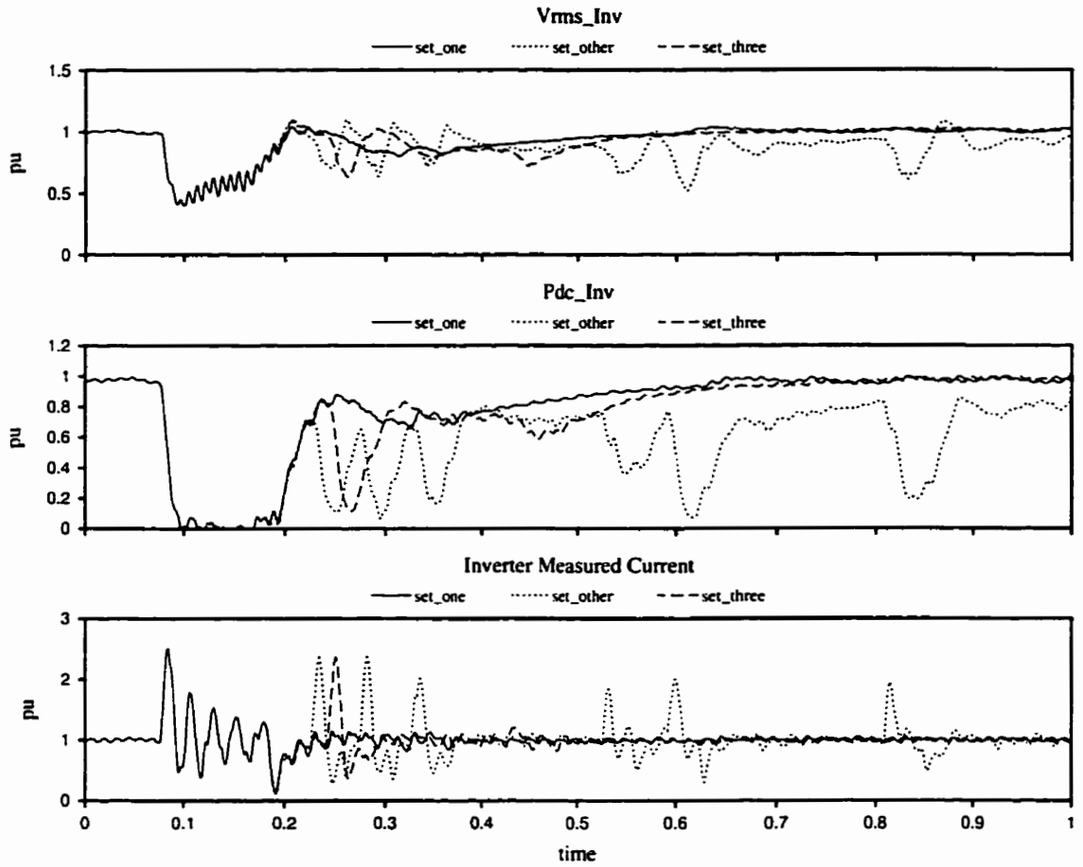


Figure 8.8: Inverter single phase to ground fault – different parameter values.

The effect of changing the values of PID parameters is presented in Figure 8.11 where the values of Ti, Gp, Td and Tf are shown.

Inverter Close-in Three Phase to Ground Fault

The performance of the system for the inverter close-in three phase to ground fault is shown in Figure 8.9. In this case the dc power reached the level of 0.8 p.u. at 210 ms after the fault is cleared.

As in the case of single phase to ground fault, the comparison of system behavior for the control with the values from different sets is carried out. The results of this

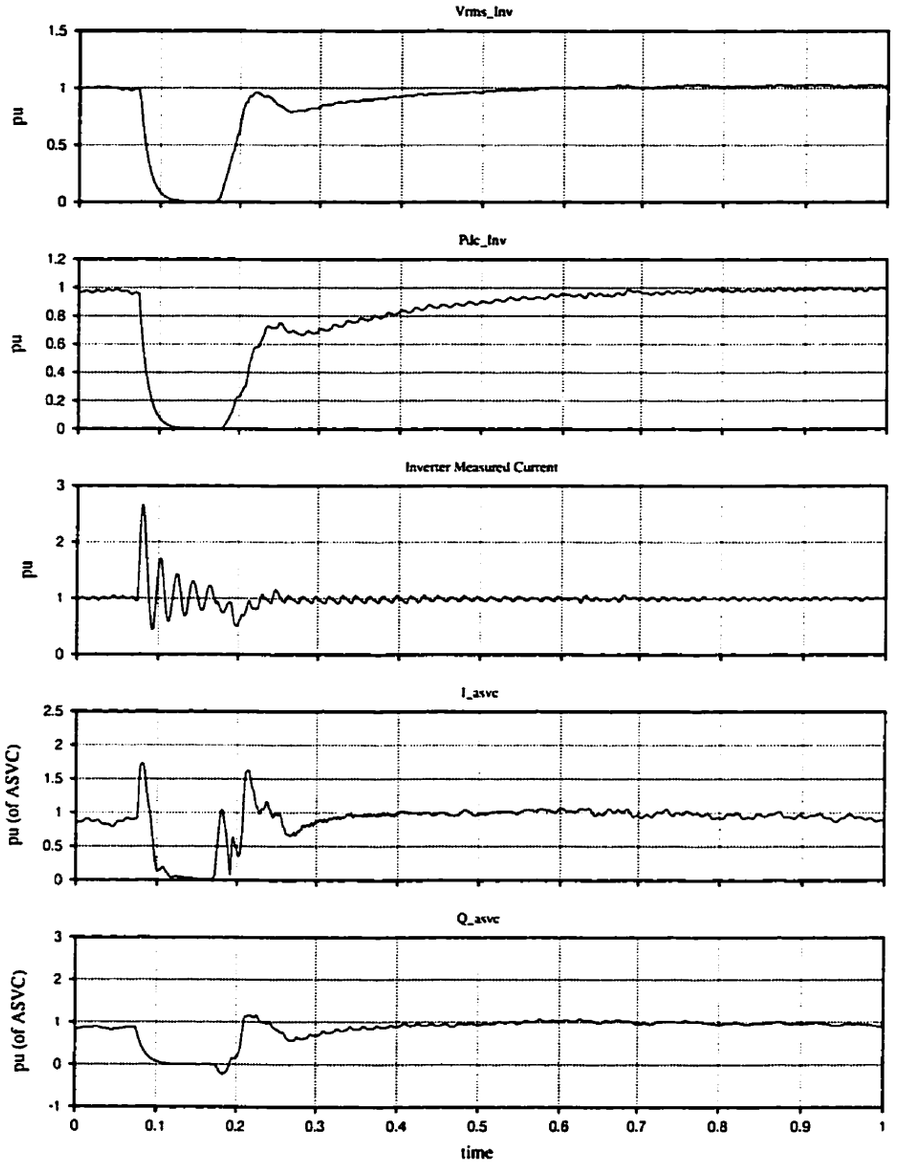


Figure 8.9: Inverter three phase to ground fault.

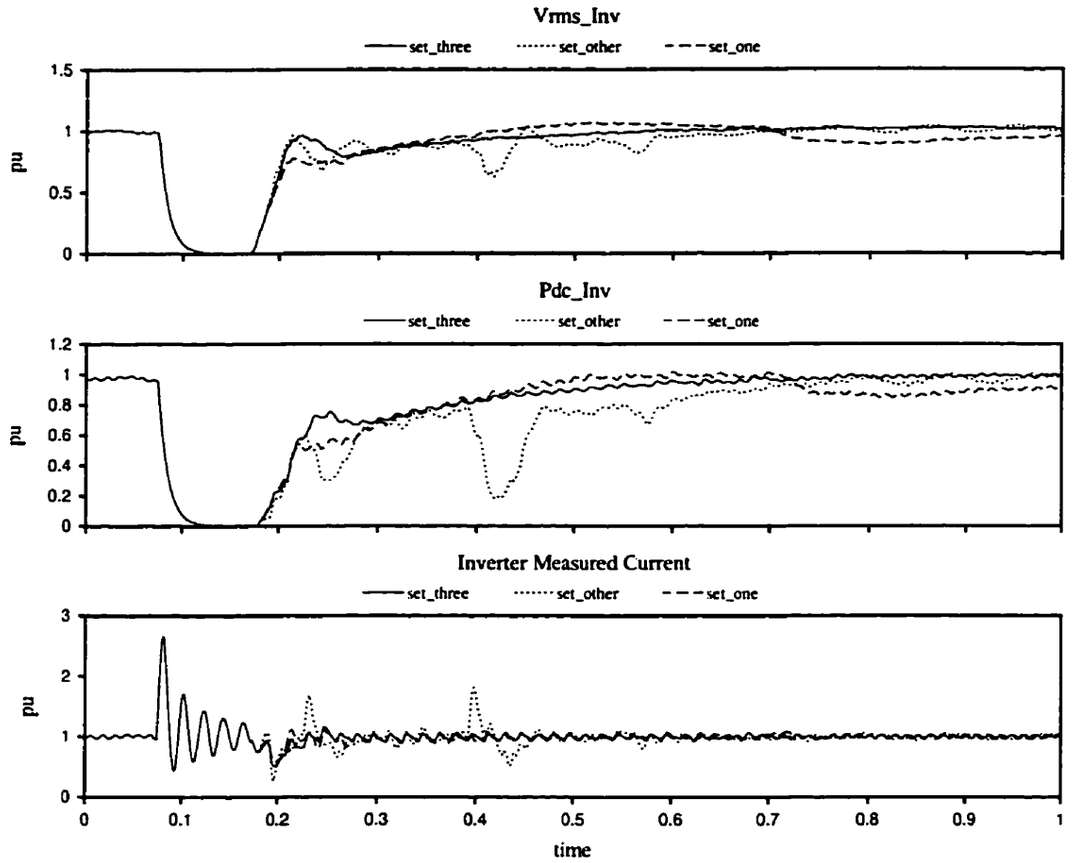


Figure 8.10: Inverter three phase to ground fault – different parameter values.

investigation are presented in Figure 8.10. Also in the case of three phase to ground fault the performance of the system is at its best when the values found only for this kind of fault (set_{three}) are used.

Changes in the values of PID parameters are shown in Figure 8.11.

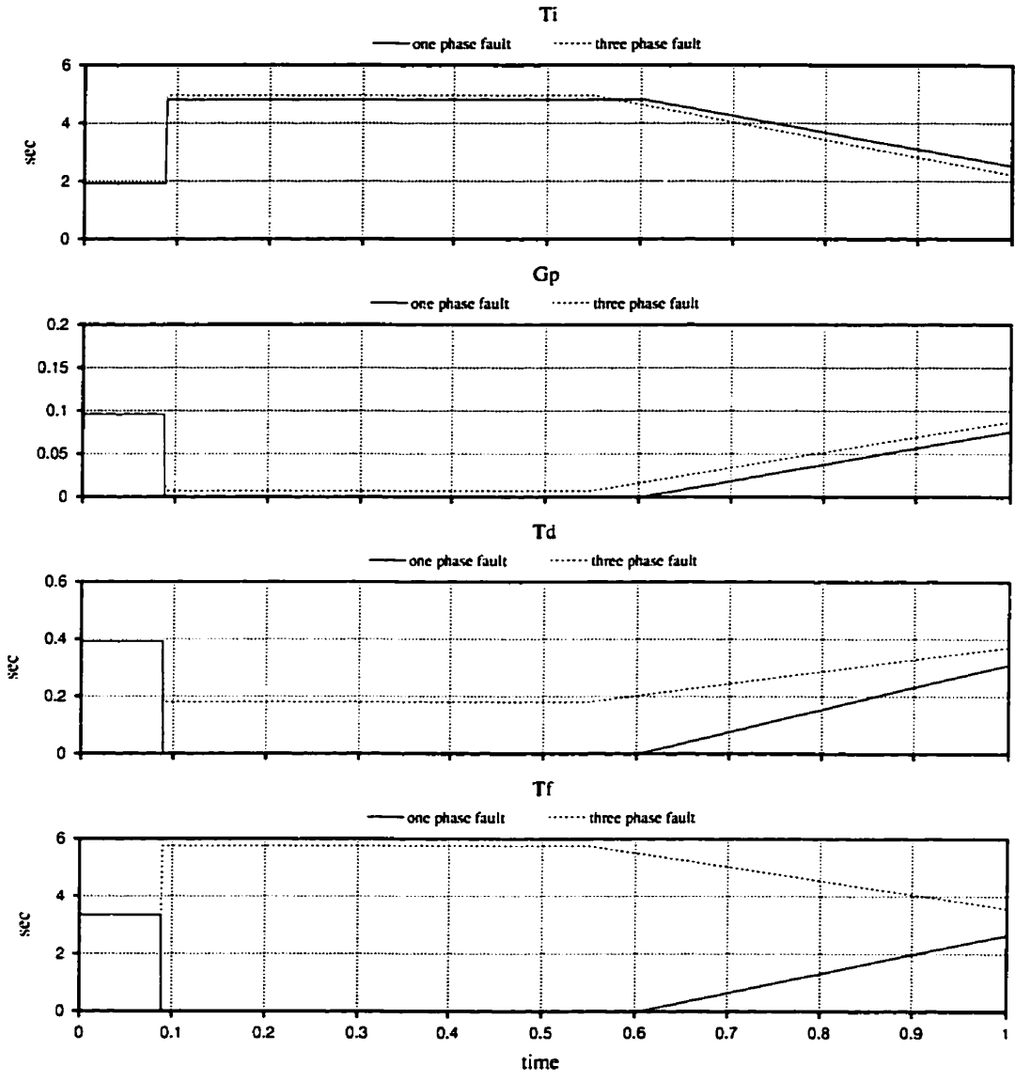


Figure 8.11: Changes in PID parameters values.

Chapter 9

Conclusions

The two main objectives of this thesis were to design an ASVC control system and to investigate the performance of the ASVC at an ac/dc interconnection. In order to achieve these objectives, some aspects of the ASVC design and its control were studied. As a result, modifications to the harmonic based method for design of ASVC components, and a new concept of control system design for complex systems are proposed and developed. Based on the research conducted, the following conclusions can be drawn:

- Reduction of harmonic components in the ASVC output voltage is one of the most important aspects of the designing process. Harmonics reduction has an influence on configuration of the ASVC, as well as on the components of its power circuit. Harmonic analysis of the ASVC results in an adjustment of the values of capacitance of the dc capacitor, the leakage inductance of the step-down transformer, and the transformer ratio.

- The usefulness of a state variable approach for control design seems questionable in the case of complex systems. Derivation of the model is difficult and the set of equations obtained is both complex and non-linear. Moreover, some assumptions and simplifications are needed.

- A combination of an advanced system simulator – $EMTDC^{TM}$ and genetic computation is a promising tool for control design in the area of power systems. This combination permits the design of an optimal control using detailed models developed with $EMTDC^{TM}$, without any simplifications or linearizations. Opti-

mization of the control can be carried out based on various performance indices. They can be either standard performance indices or any complex indices created by the designer. Use of genetic computation means that any number of control parameters can be adjusted, whether they are discrete or continuous.

- A system which combines an advanced system simulator and genetic algorithms can be used to design the structure of a control system. This idea has been applied to the design of an ASVC control and has resulted in a control system which has enabled the ASVC to perform well. This approach can lead to semi-, or to fully-automatic design of control systems.

- The control system of ASVC embraces two functions: first regulation of the voltage at the ac bus, and secondly the limitation of ASVC output current in order to prevent overcurrent situations. The function of current limitation is essential for the uninterrupted working of ASVC, and its action has a significant influence on the realization of the primary function of the ASVC – voltage regulation.

- The concept of switching control has been investigated and successfully applied to the ASVC. A fuzzy controlled switching between two sets of parameters values based on the error value has been used in the ASVC control for the case of the inverter close-in single phase to ground fault. It has given a better performance of the ASVC when compared to its performance when a standard type of control was used.

- An application of the control which permits the use of a different set of parameter values in a control procedure, depending on the system state, has been used to investigate the performance of the ASVC at an ac/dc interconnection. Applying this approach means that the values of control parameters which are optimal for a given event can be used.
  This concept of a control system seems important in the case of the ASVC. Preliminary design of an ASVC control with the value of dc capacitor $C = 404\mu F$ has been completed. The performance of the ASVC in the case of ac faults at the rectifier site, dc faults, and the inverter close-in three phase fault has been

similar or even better than the performance of the ASVC with a large dc capacitor. However, the recovery of the system has been slow and unsteady in the case of the inverter close-in single phase to ground fault. An application of a control which permits the use of an optimal set of the control parameter values for this particular fault seems an interesting approach to solving this problem. Moreover, the behavior of the ASVC in the case of single phase to ground fault confirms the importance of analysis of unbalanced conditions in the design process of the ASVC.

Chapter 10

Future Research

The promising results described here – application of the harmonic based method for designing components of an ASVC power circuit, the genetic design of control system, and the concept of switching control – provide a motivation for further research, namely:

- extending the harmonic based method for power circuit design by:
  - taking into account unbalanced conditions;
  - including analysis of different configurations of the ASVC;
  - adding multi-objective optimization methods;
- improving the *GeneticEMTDC* program in relation to:
  - the application of genetic algorithms designed for multiobjective optimization [23], [9];
  - the creation of hybrid control design approach whereby elements of analytical analysis and synthesis are combined with genetic computation;
  - the implementation of new performance indices: indices which measure the performance of a system at different time intervals, and indices which represent complex performance measures;
  - the development of methods which can search out not only the maximum of optimized function but also such part of the function which has a required shape, like the one proposed by Dr.Pedrycz and the author [38];

  - the development of methods which can search out the maximum of optimized function, taking into account the domain of variables of the function, as well as some constraints regarding the values of these variables [28];
  - the combination of genetic algorithms with genetic programming and the creation of a system for semi- or fully-automatic design of control systems.

- the investigation of different control schemes for the ASVC which can be related to:
  - studies of other control approaches, such as the one based on $d-q$ transformation [43];
  - examination of fuzzy gain scheduling with various numbers of different sets of the parameter values;
  - combination of fuzzy gain scheduling with the concept of switching the values of control parameters depending on the state of a system.

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Appendix A

Fuzzy Modeling of Nonlinear Relationships

A model of a N-dimensional non-linear relationship can be viewed as a collection of M conditional statements:

$$\underline{if}\ x_1\ is\ A_1^1\ and\ x_2\ is\ A_2^1\ and \cdots\ and\ x_k\ is\ A_k^1\ \underline{then}\ y^1 = g^1(\mathbf{x}, \mathbf{a^1}) \tag{A.1}$$

$$\underline{if}\ x_1\ is\ A_1^2\ and\ x_2\ is\ A_2^2\ and \cdots\ and\ x_k\ is\ A_k^2\ \underline{then}\ y^2 = g^2(\mathbf{x}, \mathbf{a^2}) \tag{A.2}$$

$$\vdots$$

$$\underline{if}\ x_1\ is\ A_1^i\ and\ x_2\ is\ A_2^i\ and\ \cdots\ and\ x_k\ is\ A_k^i\ \underline{then}\ y^i = g^i(\mathbf{x}, \mathbf{a^i}) \tag{A.3}$$

where A_k^i are membership functions defined on k-dimension of the space of the input variables, g^i is k-dimensional linear function with vector of parameters $\mathbf{a^i}$, $k = 1, 2, \ldots, N$ and $i = 1, 2, \ldots, M$. Each linear function is called a local model. Based on the work of Takagi and Sugeno [49] the final output of the model is given as the average of the outputs of all local models with the weights which reflect the degree of 'activity' of a given local model, for a given values of input variables. Let us assume the degree of 'activity' of a given model as:

$$\mid y^i \mid = A_1^i(x_1) \wedge A_2^i(x_2) \wedge \cdots A_k^i(x_k) \wedge \tag{A.4}$$

with $A_k^i(x_k)$ denoting value of membership function at a point x_k and $\wedge$ denoting the minimum operation. In this case the final output y of a non-linear relationship is given by the formula:

$$y = \frac{\sum_{i=1}^{N} \mid y_i \mid * y_i}{\sum_{i=1}^{N} \mid y_i \mid} \tag{A.5}$$

The method of determination of fuzzy membership functions A_k^i based on a known formula of non-linear relationship $f(\mathbf{x})$, is proposed by Dr. Pedrycz and the author [36], [37].

In the proposed method, a problem of finding a location and a spread of each membership function is transferred to a problem of optimization. Let us consider that the membership function as Gaussian in the form:

$$\Omega^i(\mathbf{x}, \mathbf{w^i}) = e^{-\sum_{k=1}^{N} \frac{(x_k - m_{ik})}{\sigma_{ik}}} \tag{A.6}$$

where $\mathbf{w^i}$ is the vector of parameters $< m_{i1}, m_{i2}, \ldots, m_{ik}, \sigma_{i1}, \sigma_{i2}, \ldots, \sigma_{ik} >$ of a membership function. Each membership function A_k^i which is used to calculate the final output of a function, is a k-dimension view of Ω^i.

The optimization problem is formulated then as:

$$min_{\mathbf{w^1}, \mathbf{w^2}, \ldots, \mathbf{w^M}} \sum_{i=1}^{M} [D_i - \frac{1}{M} F]^2 \tag{A.7}$$

subject to

$$\sum_{i=1}^{M-1} \sum_{j>i}^{M} \int_{\mathbf{x}} \Omega^i(\mathbf{x}, \mathbf{w^i}) \Omega^j(\mathbf{x}, \mathbf{w^j}) d\mathbf{x} = \varepsilon \tag{A.8}$$

where:

$$F = \int_{\mathbf{x}} (\mid \frac{\partial f}{\partial \mathbf{x}} \mid) = \int_{x_N} \cdots \int_{x_i} \cdots \int_{x_1} (\sum_{i=1}^{N} \mid \frac{\partial f}{\partial \mathbf{x}} \mid) dx_1 \ldots dx_i \ldots x_N \tag{A.9}$$

and

$$D_i = \int_{\mathbf{x}} (\sum_{i=1}^{N} \mid \frac{\partial f}{\partial \mathbf{x}} \mid) \Omega^i(\mathbf{x}, \mathbf{w^i}) \tag{A.10}$$

The use of the Lagrange multipliers technique allows to treat the constraint as a part of the objective function, that vis:

$$V(\mathbf{x}, \lambda) = \sum_{i=1}^{M} [D_i - \frac{1}{M} F]^2 + \lambda(\varepsilon - \sum_{i=1}^{M-1} \sum_{j>i}^{M} \int_{\mathbf{x}} \Omega^i(\mathbf{x}, \mathbf{w^i}) \Omega^j(\mathbf{x}, \mathbf{w^j}) d\mathbf{x}) \tag{A.11}$$

where λ is the Lagrange multiplier. The local minimum of V is obtained through iterative modifications of the values of m_{ik}, σ_{ik} and λ.

Appendix B

List of symbols used in Chapter 4

β_r	rectifier angle of advance
β_i	inverter angle of advance
γ	extinction angle
γ_{ref}	extinction angle reference
I_r	rectifier dc current
I_i	inverter dc current
I_{ref}	dc current reference
k_{rp}	proportional gain of rectifier PI controller
k_{ri}	integral gain of rectifier PI controller
k_{ip}	proportional gain of inverter PI controller
k_{ii}	integral gain of inverter PI controller
V_c	mid-line dc voltage
V_{dcr}	rectifier dc voltage
V_{dci}	inverter dc voltage
τ_r	rectifier transformer ratio
τ_i	inverter transformer ratio
V_t	ac voltage at inverter ac bus

Appendix C

Control Parameters of ASVC

C.1 Parameter Values for Control System *A*

Parameter (as in Figure 7.2, page 74)	Value
$var01$	9.3038
$var02$	0.3257
$var03$	3.7316
$var04$	9.8977
$var05$	4.8812
$var06$	1.1211
$var07$	0.0165
$var08$	6.9514

C.2 Parameter Values for Control System *B*

Parameter (as in Figure 7.3, page 75)	Value
*var*01	7.6966
*var*02	1.3853
*var*03	1.8360
*var*04	3.5790
*var*05	0.1825
*var*06	0.0
*var*07	9.0576

C.3 Parameter Values for Control System *C*

Parameter (as in Figure 7.6, page 78)	Value
*var*01	3.4900
*var*02	0.1117
*var*03	0.0
*var*04	6.8[illegible]0
*var*05	0.0

C.4 Parameter Values for Control System with Fuzzy Gain Scheduling

Parameter (as in Figure 7.2, page 74, and in Figure 7.9, page 80)	Value
Gp_{NZ}	0.0908
Ti_{NZ}	10.0
Td_{NZ}	0.4799
Gp_P	0.0838
Ti_P	9.0602
Td_P	0.0343
B	0.3064
$var04$	6.2429
$var05$	5.1447
$var06$	0.5381
$var07$	2.2451
$var08$	5.0236

C.5 Parameter Values for Control System in Chapter 8

C.5.1 Parameters Obtained in the First Stage of Design

Parameter (as in Figure 8.2, page 86 (b))	Value
$Gp_{set_{other}}$	0.9600
$Ti_{set_{other}}$	1.9280
$Td_{set_{other}}$	0.3919
$Tf_{set_{other}}$	3.3485
$var05$	0.5966
$var06$	1.6516
$var07$	5.9305
$var08$	5.0236

C.5.2 Parameters Obtained in the Second Stage of Design

Values of Parameters for the Single Phase to Ground Fault

Parameter (as in Figure 8.2, page 86 (a))	Value
$Gp_{set_{one}}$	0.0
$Ti_{set_{one}}$	4.8130
$Td_{set_{one}}$	0.0011
$Tf_{set_{one}}$	0.0

Values of Parameters for the Three Phase to Ground Fault

Parameter (as in Figure 8.2, page 86 (a))	Value
$Gp_{set_{three}}$	0.0070
$Ti_{set_{three}}$	4.9624
$Td_{set_{three}}$	0.1811
$Tf_{set_{three}}$	5.7509