# Evaluation Methodology for DC Line Fault Clearance Techniques in a Point-to-Point VSC-HVDC Transmission System

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# Dedication

***To***

***My family for their support:***

***my dear mother, my great father,***

***my lovely wife,***

***and our four year old son***

***Henry,***

# Abstract

This thesis examines and compares various DC fault clearance methods that can be used for the VSC-HVDC transmission system, specifically in the context of a point-to-point VSC HVDC transmission system. The newest conceptual research, prototype development. and real implementations are described in depth through the literature review. An analytical evaluation methodology is developed to compare the performance, capability, losses, and cost of different DC fault clearing techniques. Finally, a comparative analysis is conducted to evaluate the DC fault clearing solution using a full-bridge modular multilevel converter and a half-bridge modular multilevel converter with DC breakers using PSCAD/EMTDC software.

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# List of Symbols

| | |
|---|---|
| $\alpha$ | *Thyristor Firing Angle* |
| ac | *Alternating Current* |
| BIGT | *Bi-Mode Insulated Gate Transistor* |
| CSC | *Current Source Converter, also known as line commutated converter* |
| DB | *Damping Branches* |
| dc | *Direct Current* |
| DCCB | *Dc Circuit Breaker* |
| ETT | *Electrically Triggered Thyristors* |
| FWD | *Free-Wheeling Diode* |
| GTT | *Gate Turn-Off Thyristors* |
| HB | *Hybrid Breaking Units* |
| HSMS | *High-Speed Making Switch* |
| HV | *High Voltage* |
| HVDC | *High Voltage Direct Current* |
| IGBT | *Insulated-Gate Bipolar Transistor* |
| IGCT | *Integrated Gate Commutated Thyristors* |
| LCC-HVDC | *Line Commutated Converter HVDC* |
| LTT | *Light Triggered Thyristors* |
| LV | *Low Voltage* |
| MMC | *Modular Multilevel Converter* |
| MOSA | *Metal Oxide Surge Arrester* |
| MOV | *Metal Oxide Varistor* |
| MPH | *Mechanical and Power Electronic Hybrid* |
| MT HVDC | *Multi-Terminal HVDC* |
| PG | *Pulse Generator* |
| PMPH | *Proactive Mechanical and Power Electronic Hybrid* |
| pu | *Per-Unit* |
| PWM | *Pulse-Width Modulation* |

| | |
|---|---|
| SCR | *Short-Circuit Ratio* |
| SF6 | *Sulfur Hexafluoride* |
| TIV | *Transient Interruption Voltage* |
| TRV | *Transient Recovery Voltage* |
| UPS | *Uninterruptible Power System* |
| VSC-HVDC | *Voltage Source Converter HVDC* |

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# Chapter 1.

# Introduction

In this chapter, voltage source converter technology and its topologies are introduced, by comparing with the line-commutated converter, as key important background references with an emphasis on advancements in the topology of the voltage source converter. Although only point-to-point high voltage direct current transmission systems are examined in this thesis, conceptual high voltage direct current transmission system configurations are briefly discussed. Three techniques based on literature reviews are presented for dc fault clearance. Following these introductions and reviews of the literature, this chapter has discussed the research motivations and objectives before concluding with an overview of the thesis organization.

## 1.1. VSC-HVDC Overview

### 1.1.1. Technology

Since its introduction into commercial use in 1954, *High Voltage Direct Current* (HVDC) transmission has been widely employed to enable long-distance power transmission, under water cable transmission, coupling of asynchronous ac networks, and connection of *alternative current* (ac) systems with different frequencies [1]. Conventional HVDC systems are based on the *line-*

*commutated converters* (LCCs) technology that utilizes thyristor as the key component to convert ac to *direct current* (dc). Through this conversion which is reliant on the ac (line) voltage, the thyristor valve is commanded to "turn on", and can only be "turned off" when the current through it drops to zero [2] [3]. With its robust design, high reliability, and improving semiconductor technology development, the LCC, also known as "Classic" or *Current Source Converter* (CSC), has a high level of maturity and long history of success [3]. According to the Cigré B4 compendium, there are 109 known LCC-HVDC systems installed around the world, with 10 more in planning or construction stages [4]. The LCC, on the flip side, has some operational constraints because its current commutation is driven by ac voltage. It necessitates proper ac system conditions, such as a minimum ac system strength, a sufficient reactive power supply, and low-order harmonic filters installed near the converters.

*Voltage Source Converter* (VSC), contrastingly, is based on fully controllable semiconductor switches, which allow the valve not only to be "turned on", but also to be "turned off" independently of the current that passes through the valve [2]. VSC is able to self-commutate and work around the LCC restrictions listed above because of this distinction. The LCC will also suffer commutation failure and a brief and temporary power interruption during system disturbances when the ac system voltage waveform is significantly distorted [5] [6]. Thanks to its self-driven capability, VSC, on the other hand, is unaffected by this failure. The VSC valve design incorporates fully controllable semiconductors such as *insulated-gate bipolar transistors* (IGBTs) together with an *antiparallel freewheeling diode* (FWD) for bi-directional current flow, as shown in Figure 1-1 [1] [2] [3].

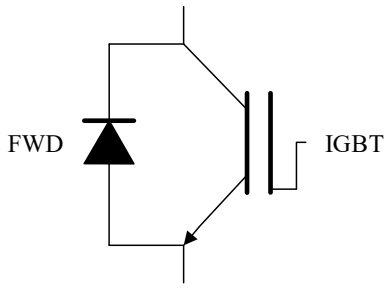



**Figure 1-1: VSC Valve Circuit Schematic with IGBT and FWD**

VSC technology has evolved significantly since the first VSC-HVDC transmission scheme began operation in 1997 [2] [7]. According to the Cigré B4 compendium, 33 VSC-HVDC systems have been installed worldwide, with another 21 planned or under construction [4]. VSC's superior performance properties not only enable it becoming a viable competitor over LCC for long distance point-to-point transmission solutions, but also offer a range of possible new applications, including the following [1] [2]:

- Transmission to/from weak ac systems,
- Supply of passive networks with black-start capability,
- Connection to renewable generations such as wind, wave, or solar power systems,
- And, establishment of multi-terminal system or HVDC networks.

### 1.1.2. VSC Converter Topology

The converter's fundamental objective is to connect and transmit energy in both directions between ac and dc systems. To date, IGBTs are commonly used in the design of VSCs as converter valves (or referred to as switches) with *Pulse-Wide Modulation* (PWM) control methods, in which two,

three, or multilevel converter topologies are used to implement the VSC converters [3]. A two-level converter is formed with two alternately operating valves, as illustrated in Figure 1-2(a) for a single-phase converter configuration, the ac bus voltage $V_{ac}$ varies between the positive dc voltage $+U_d$ and negative dc voltage $-U_d$ [2]. An additional intermediate voltage level is available in a three-level converter with subdivided dc capacitor, or additional dc capacitor added. The term "multi-level" refers to the topology of a converter in which the ac bus can be varied to generate three or more distinct voltage levels [2]. Although a number of early VSC installations used two-level or three-level designs, the *modular multilevel converter* (MMC) with cascaded connection has become the most common solution to date for VSC-HVDC systems [2]. In comparison to the two- or three-level converters design, MMC does not use a common capacitor connecting between dc buses; instead, it functions as a voltage source composed of a large number of controllable sub-modules, each operating independently as a controllable voltage "building block" forming an approximate sine wave. MMC is extendable without requiring excessively complex control systems, which makes it flexible on the system specified converter voltage level.

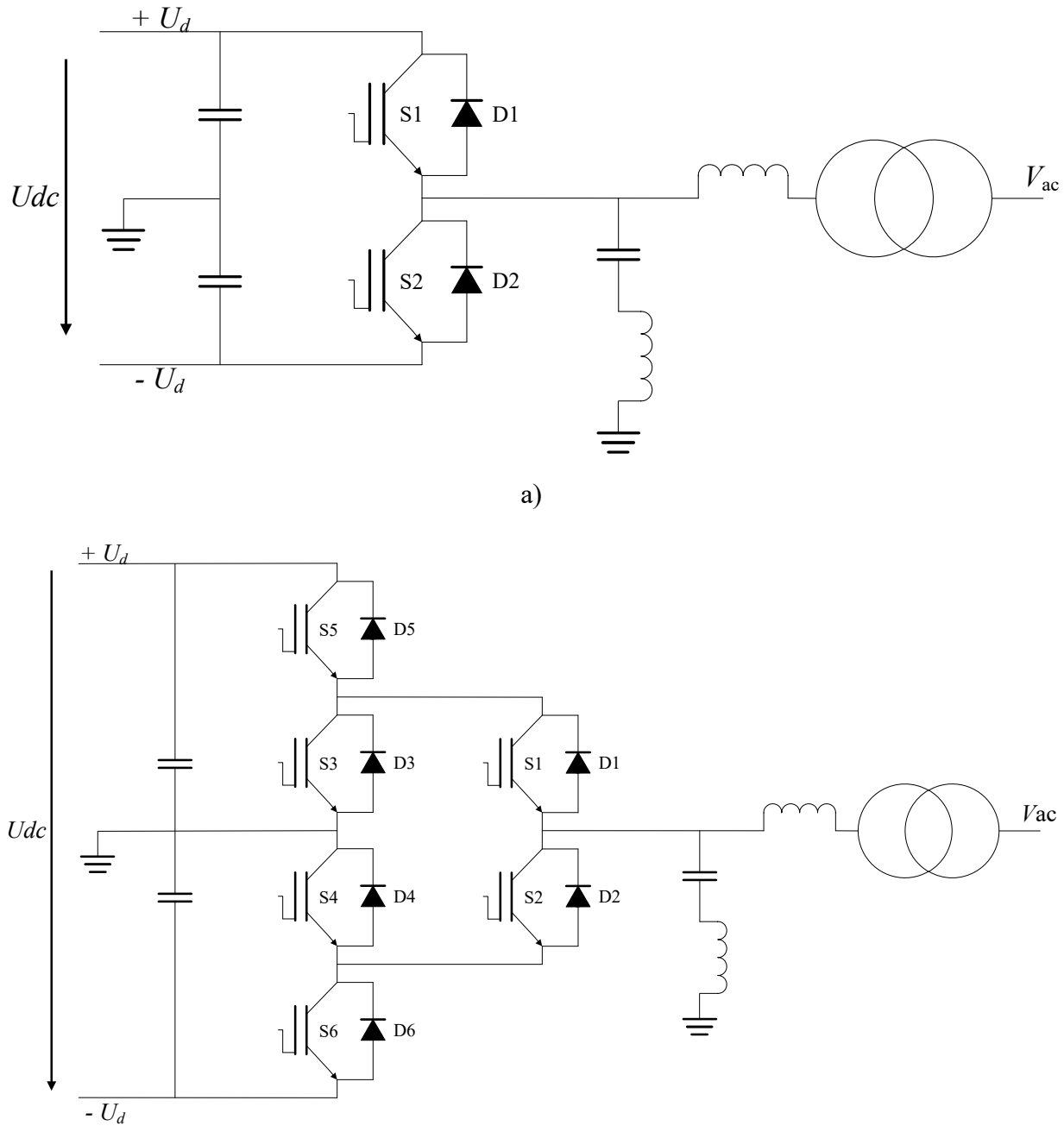



**Figure 1-2: VSC Converter Technologies: a) VSC-HVDC 2 Level Converter Station; b) VSC- HVDC 3 Level Converter Station [2]**

There are two common types of MMC submodule designs, half-bridge design and full-bridge design, which are illustrated in Figure 1-3 [2] [6]. The MMC using half-bridge submodules was

originally invented by Marquardt and his colleagues [8] [9], and this submodule designed with two terminal is series connected to form a converter phase arm in the MMC, each of which features IGBTs and capacitors. The capacitor in the submodule can be charged or discharged depending on the direction of the current; or bypassed by turning on both IGBTs [10]. Each full-bridge submodule can generate three different voltage levels: positive voltage, zero voltage, and negative voltage. During a dc short circuit fault, the additional zero voltage and negative voltage stages of a full-bridge MMC module can be utilized to interrupt or suppress fault current by reversing the voltage polarity and producing a counter electromotive force. [11].

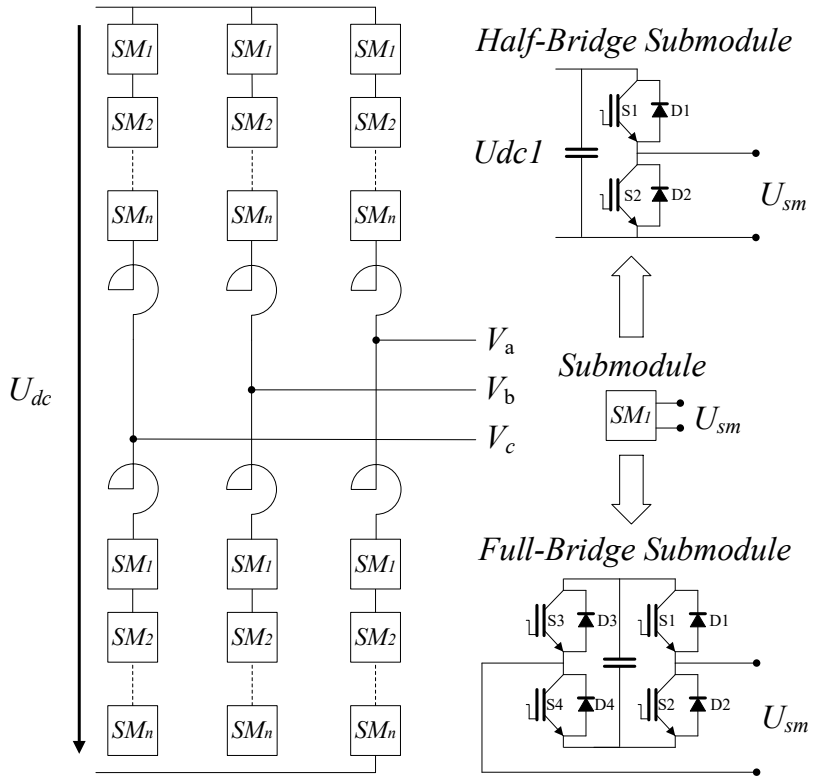
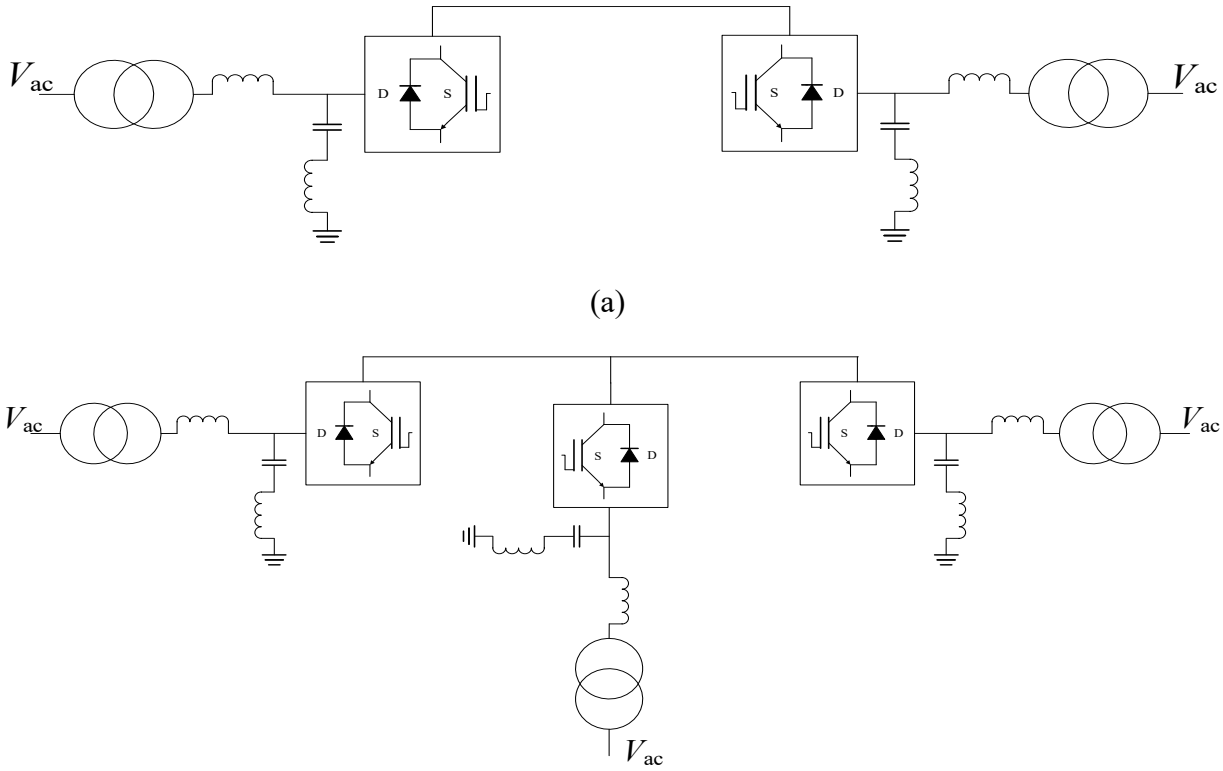



**Figure 1-3**: Main Circuit Principle Diagram of MMC with Half-Bridge and Full Bridge Sub-Modules **[2] [6]**

Conduction and switching losses are the two primary forms of losses related with power electronic switches in VSC [1][2]. Conduction losses are proportional to the number of IGBTs, the conduction resistance of the IGBT and FWD pair, and the dc current. Additionally, switching losses are proportional to the regulated switching frequency based on the control scheme, dc current, and voltage measured at pre- and post-switching event [12]. VSC based on two- or three-level converters requires a higher switching frequency than VSC based on MMC, owing to MMC's significantly reduced switching frequency [13]. The topology of the full-bridge submodule is made up of two parallel half-bridge submodules. As a result, the conduction losses and equipment investment costs associated with the converter's total number of IGBTs are greater than those associated with the half-bridge topology.

### 1.1.3. System Configurations

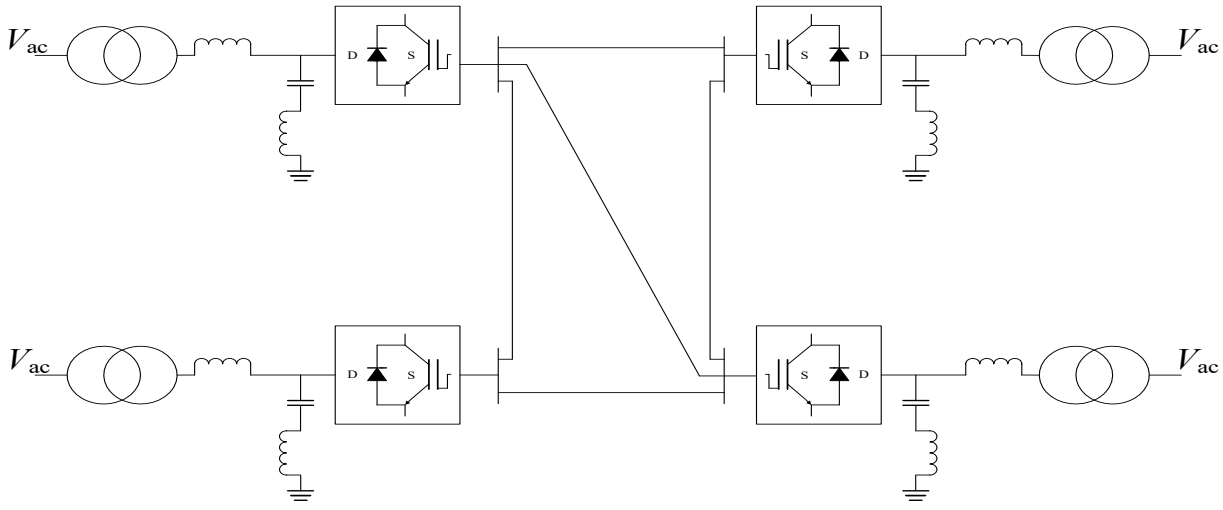
A point-to-point HVDC system, as shown in Figure 1-4a, consists of two converter stations: a rectifier station that converts alternating current to direct current and an inverter station that converts direct current to alternating current for one directional power transfer. The point-to-point HVDC transmission system is connected via long transmission lines or cables, with unidirectional or bidirectional power transmission possibilities. When more than two converter station terminals are connected, a multi-terminal HVDC system with increased power transmission flexibility is formed, as opposed to point-to-point HVDC systems. A multi-terminal HVDC system consists of three or more converter stations, each of which contains at least one rectifier and one inverter. The multi-terminal HVDC system can be configured as a "tapping" system (Figure 1-4b) or as a "meshed" system (Figure 1-4c), which is a more complex configuration that operates like an ac network grid.




(a)




(b)




(c)

**Figure 1-4**: Sample Point-to-Point and Multi-Terminal Configurations:

(a) Point-to Point Configuration; (b) Tapping Configuration with Three Terminals;

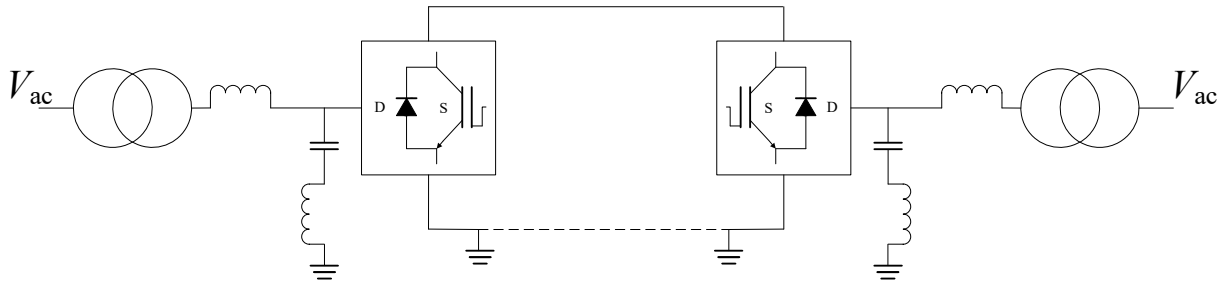
(c) Meshed Configuration with Four Terminals [1] [2] [6] [9]

### 1.1.1. Converter Configurations

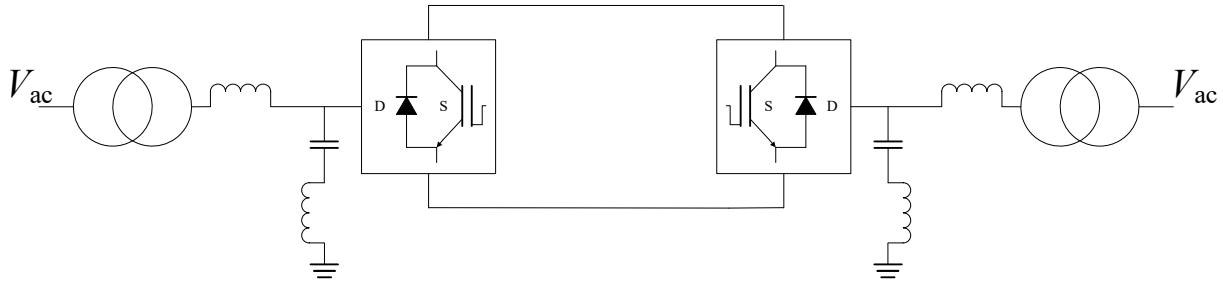
Figure 1-5a shows an asymmetrical monopole converter configuration, which is also called a monopolar HVDC system with ground return [1]. The converters are connected between ground and a high voltage dc pole, and current is flowing from the converter through the high voltage pole to the high voltage pole on the opposite station and returning through the ground electrodes or dedicated metallic neutral return conductor.

Figure 1-5b shows a symmetrical monopolar configuration, in which the converter is connected between two high voltage poles with opposite polarity on the dc side. This configuration which is mainly used for VSC-HVDC does not have the ground reference on the dc lines, but the ground reference can be provided through the high impedance reactors on the ac side or through resistive voltage divider on the dc side to provide a closed path for dc leakage current, due to small voltage unbalance between positive and negative poles [1] [14]. Alternative grounding circuit arrangements are suggested in [14] and [15] to utilize high resistance grounding at star configured converter interfacing transformer secondary wingdings for limiting pole to ground fault current, and preventing transformer saturation during the fault and converter energization.

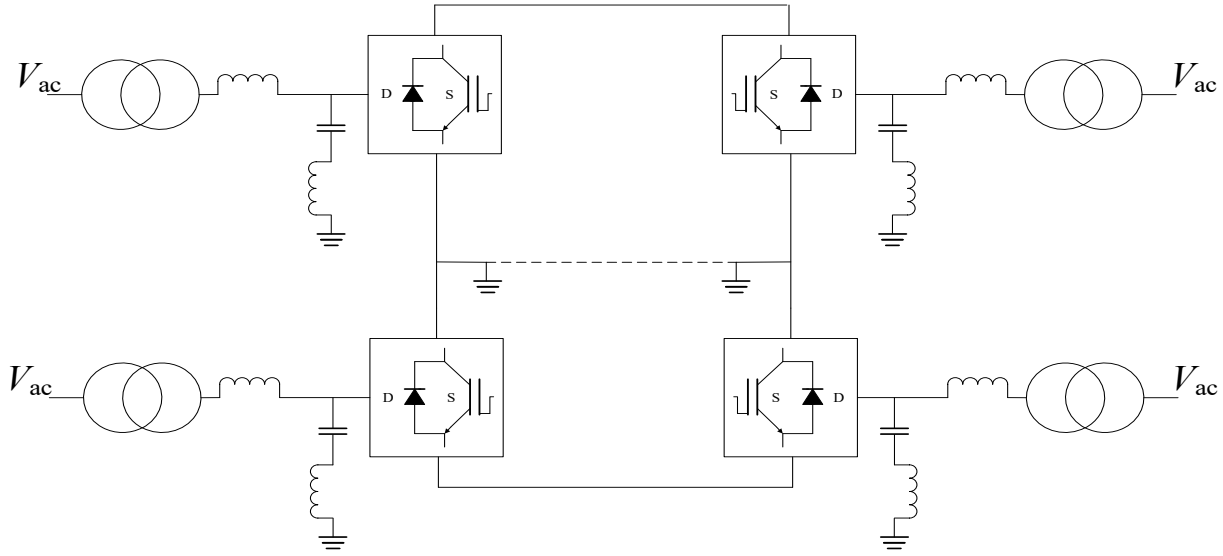
In a monopolar configuration, dc current flows through the two conductors to transmit power, therefore they are operated dependently. If one conductor is out of service, or any dc fault in a monopole system would lead to a loss of power [16]. A bipolar configuration, as shown in Figure 1-5c, is formed by two asymmetrical monopole systems and provides both fail-redundancy and operational flexibility due to the independent operable and controllable poles. Following a dc side fault or pole loss, the remaining pole can operate as an asymmetrical monopole through earth return or metallic return (dedicated conductor) with reduced dc power capacity.




(a) Asymmetrical Monopole Configuration




(b) Symmetrical Monopole Configuration




(c) Bipolar Configuration

**Figure 1-5: Converter Valve Configurations: (a) Asymmetrical Monopole Configuration; (b) Symmetrical Monopole Configuration; (c) Bipolar Configuration. [1] [2] [13]**

## 1.2. DC Line Fault for Point-to-Point VSC-HVDC System

For LCC, when the dc line fault occurs, the current control function can be used to limit the fault current and the valve control and protection can be used to clear the fault current with multiple attempts at different voltage levels. This control sequence takes approximately 20 to 40 milliseconds [17] [18]. While VSC has a number of advantages over LCC they do have one disadvantage, IGBTs can be blocked for self-protection in the event of a dc fault, the FWDs connected in parallel with the IGBTs operate as an uncontrolled bridge rectifier, continuously feeding the fault from the ac system via the formed diodes rectifier bridge [1] [19], as illustrated in Figure 1-6. If the dc system is entirely composed of cables, a fault is highly improbable [2]. For overhead lines, however, dc line faults are highly probable. The fault current from ac systems is limited by the ac network's short-circuit impedance, the transformer's reactance, the phase reactor's reactance, and resistance in the circuit. For the case where *dc Circuit Breaker* (DCCB) or other fault clearing device is not available on the dc side, the short-circuit current is eliminated solely by tripping the ac-side breakers. While tripping the ac-side breaker may appear to be the simplest dc line fault response, due to fault detection and operation delays, the converter will not be isolated immediately following the fault, resulting in fault contribution from ac systems, causing further disturbance to the ac system network.

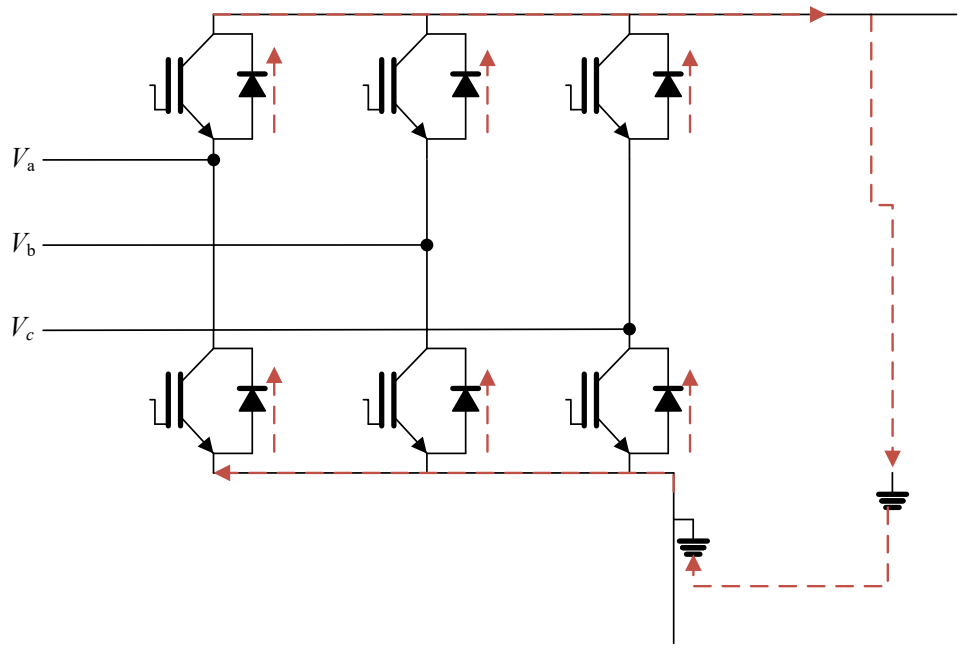



**Figure 1-6**: Conceptual VSC diagram for Current Flow during DC Faults

A dc line fault in VSC-HVDC appears to be a remote fault to the connected ac system; if the fault current relies on ac side circuit breakers to clear, it will take at least a few hundred milliseconds to interrupt and extinguish the fault current [19] [20]. Depending on the dc transmission power capacity, a dc line fault may pose a significant transient stability risk to the connected ac networks. An example of a system study case is Manitoba Hydro's dc line fault performance studies for Bipole III using half-bridge MMC with overhead transmission lines. As in a such case, the ac system voltage at the inverter station was reduced to 0.72 per-unit (pu) following a dc line fault prior to utilizing ac breakers to clear the dc fault [21]. Due to the electrical proximity of the other two existing LCC Bipoles (Bipoles I&II), the study also demonstrated that a dc line fault at Bipole III's inverter end would propagate to the common connected inverter ac bus for Bipole I and Bipole II, resulting in a maximum voltage depression of 25% at the Bipoles I&IIs' inverter ac bus voltage level, which caused in commutation failures of Bipoles I&II LCC HVDC systems. Additionally,

use of ac-side circuit breakers also can result in a much longer power delivery interruption and a further impact on ac system voltage stability because of the time required to re-close in the breakers, and large inrush current generated when re-energizing the converter transformers after the fault clears. After a temporary dc line fault, Manitoba Hydro's study found that it took up to 800 milliseconds for dc power to recover to 90% of its pre-fault dc transmitting power level. [21]. Due to the large potential inrush current generated by transformer energization, the associated ac system voltage level may also be hugely affected during the re-energizing process. Finally, dc faults usually occur temporarily on overhead transmission line when lightning strikes the line or when objects, such as trees, collide with the line. Therefore, in an LCC HVDC system, multiple system restoration can be attempted to ensure dc fault is cleared to improve system availability before transmission system is permanently locked out. However, using ac breaker in this manner is not feasible due to the prolonged recovering time and ac system impact during transformer energization.

As a result, in order to match the LCC dc line fault clearance performance and ensure the connected ac system's stability and availability, a DCCB or other means of interrupting dc faults is a critical requirement for supporting VSC-HVDC technology. Through the literature review, there are a number of techniques available and proposed for dc fault clearance in a VSC scheme which are comparable in speed to a pure LCC scheme utilizing current control. These strategies include the following:

a) Employing dc breakers with or without fault current limiters
b) Modifying VSC MMC submodule topologies to include dc fault clearing capability
c) Utilizing hybrid configuration of LCC and VSC in valve group/system level design

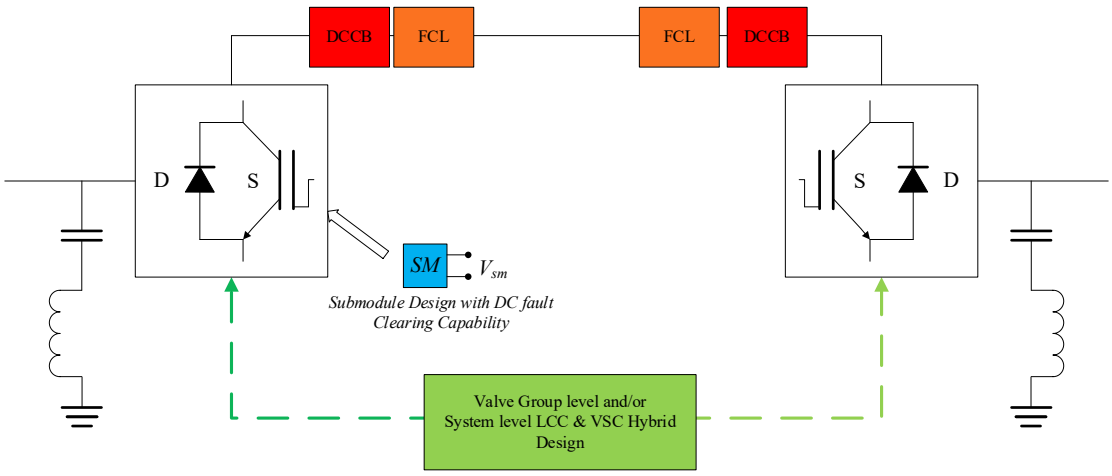



**Figure 1-7: System Layout for DC Fault Clearance Techniques**

## 1.3. Research Objectives

The purpose of this thesis is to develop a comprehensive list of different dc fault clearance techniques and an analytical evaluation methodology for comparing alternative dc line fault clearing techniques in a point-to-point VSC HVDC scheme. In the majority of VSC schemes, the default dc fault clearing mechanism is based on ac breakers, which, as previously explained, is slow in respect of fault clearance and dc link restoration. Given the number of options proposed and becoming available, how would a utility engineer compare and select a preferred method? This thesis will identify important factors such as losses, cost, and performance for evaluating dc fault clearance techniques for point-to-point VSC HVDC scheme.

Two PSCAD-EMTDC models will be developed based on leading options to assess fault clearing performance.

i) Half-bridge VSC MMC with Hybrid dc breaker

ii) Full-bridge VSC MMC converter

## 1.4. Motivations for Research

The Manitoba Hydro transmission system was developed and operated as an integrated system, with the Nelson River HVDC system serving as the backbone, as shown in the Figure 1-8, transporting over 70% of Manitoba Hydro's electric power from northern generating stations to southern load centers as well as for export [22]. Each of the three Bipoles was built with Line Communicated Converter (LCC) technology.

Bipole III, the latest Bipole, entered commercial service in July 2018. VSC technology with half-bridge MMC was studied and investigated during the Bipole III's planning stage as a possible alternative to LCC technology [7] [21] [23]. Studies indicated that dc line fault recovery for a


HVDC transmission capacity: ~ 70%

Bipole I: 890km, ±463.5kV, 1854MW, LCC.
- Pole 1 valves replaced using ETT, valve group control was replaced with analog controls in 1992,
- Pole 2 valves were replaced with LTT interfaced with original group control in 2004.

Bipole II: 930km, ±500kV, 2000MW, LCC.
- Original valves and controls are still in service up to today.

Bipole III: 1,386km, ±500kV, 2000MW, LCC
- Contract was awarded to SIEMENS, ISD 2018

**Figure 1-8**: Manitoba Hydro Nelson River Three-Bipole HVDC system **[22]**

VSC was found to be slower than LCC when fault clearing via ac breakers was assumed, requiring six cycles interruption time with a worst case fault current of 30kA, system restart may not be feasible due to the transformer re-energization causing subsequent communication failures of Bipoles I&II, and suggested further investigation of different dc line fault clearing methods [7]. At the time, there was no comprehensive list of different dc faults clearing techniques with analytical comparisons methodology. The development of such a list and evaluation methodology, along with sample PSCAD-EMTDC models, will aid transmission operators and utilities in evaluating future technology selection and conducting system studies comparing available techniques for VSC fault clearance.

## 1.5. Summary and Thesis Organization

The review and comparison of various dc fault clearing methods requires an understanding of the VSC-HVDC topology, its major components, and the characteristics of dc line faults. This introduction chapter provides pertinent background information, defines the research motivation and primary objectives. The structure of remaining chapters in this thesis is organized in the following order:

Chapter 2 reviews the characteristics of dc line faults for a point-to-point VSC-HVDC scheme with overhead transmission line, before delving into generic configurations using mathematical derivations of current and voltage behavior.

Chapter 3 discusses the various MMC submodule topologies that support dc fault clearing.

Chapter 4 discusses the various DCCB topologies, including the mechanical type, pure power electronic type, and hybrid mechanical/power electronic type, as well as the fault interruption process.

Chapter 5 introduces an evaluation methodology which is used to analyze and compare two solutions: full-bridge MMC and half-bridge MMC with dc breakers in detail using cases studies on PSCAD-EMTDC. The study case models are reviewed in detail and an extensive systematic analysis of performance comparison together with losses and cost evaluations are also presented base on the case study models.

Chapter 6 presents the conclusions, summarizes the contributions of this thesis, and makes recommendations for future work.

While this thesis cannot possibly include or reference every pertinent work, it presents the essential principles underlying the different dc line fault clearance approaches available to date in a systematic manner. The author's intention is to lay the groundwork for readers interested in identifying and further evaluating the most appropriate methodology for their research and study objectives, as well as determining where to go from here.

# Chapter 2.

# DC Faults in VSC-HVDC Systems

## 2.1. Introduction

Generally speaking, voltage source converter with two level, three level or MMC using half-bridge submodule design is susceptible to dc faults, due to its freewheeling diodes connected anti-parallel with controllable power electronic devices such as IGBTs. During the fault, while it is possible to disable the IGBTs for self-protection, doing so does not interrupt the fault current. A typical two-level, three-level, or half-bridge MMC will act as an uncontrolled ac rectifier through the freewheeling diodes, which draw the fault current from the ac network through the converter. A converter using submodules with fault current interruption capability, such as full-bridge MMC topology, can block the fault current contribution from the ac network and limit the fault current within the transient phase [2] [16], which will be discussed further in the Chapter 3. According to this research, the current characteristics of a dc fault are crucial for the design of system components, for fault detection, for the coordination of protection strategy, and for the evaluation of clearance techniques. DC faults can be classified into two types based on the nature of their occurrence: pole-to-pole faults and pole-to-ground faults with a ground connection. The behavior of the VSC converter during the occurrence of pole-to-ground faults and pole-to-pole faults is discussed in detail in this chapter.

## 2.2. Pole-to-Ground Faults

A dc pole-to-ground fault occurs when the positive or negative line conductor is shorted to the ground [16]. This fault can occur temporarily on overhead transmission lines when lightning strikes the line causing voltage surge and flashover across the insulator string through the ionized air [1] or when objects, such as trees, collide with the line; or permanently on a cable conductor due to insulation breakdown. When a pole-to-ground fault occurs on the dc line of a VSC-HVDC, a ground loop is generated between the grounding locations, for example, between the high resistance grounding at the converter transformer's star configurated winding and the ground fault point [24]. In Figure 2-1, an equivalent circuit of the VSC-HVDC with a two-level topology is shown with its positive pole shorted to ground in order to demonstrate the converter's behavior during the fault condition. In this diagram, $R_f$ and $L_f$ represent the fault resistance and inductance, respectively, while $R_d$ and $L_d$ represent the dc line model's equivalent resistance and inductance, $I_{fault}$ represents the dc fault current, $U_{dc}$ represents the voltage across the dc-side capacitor, and $I_{ac}$ represents the ac grid-side current.

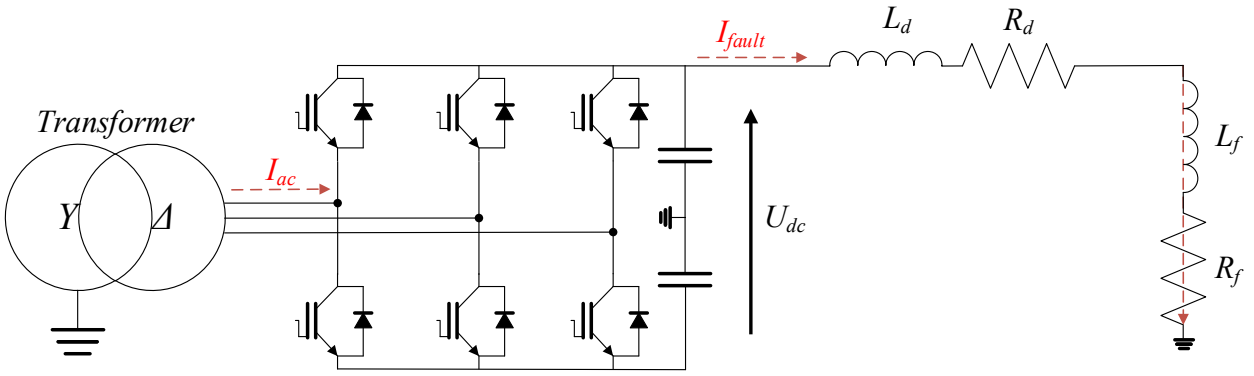



**Figure 2-1**: **Equivalent Circuit Diagram of VSC DC Pole-to-Ground Fault [24] [25]**

During the initial transient stage after the fault occurs, the pre-fault dc voltage $U_{dc}$ is larger than the ac line to line voltage. Therefore, the dc fault current at this stage is mostly from dc capacitor discharging current, and the system can be represented using the equivalent circuit shown in Figure 2-2 [24]. In this initial stage, the capacitance of dc capacitor, filter elements, dc lines, the resistance and reactance associated with dc lines, distance of the fault location, the fault impedance, and the dc reactor size will influence the fault current behavior [24]. The amplitude of the fault current increases with larger capacitance in the equivalent circuit, whereas the resistance in the equivalent circuit provides positive damping to the fault current amplitude [25]. The inductance in the loop will reduce the rate of rise of the fault current. The second-order mathematic representation of the equivalent circuit is given by [24] [25]:

$$(L_d + L_f)C\frac{d^2U_{dc}}{dt^2} + (R_d + R_f)C\frac{dU_{dc}}{dt} + U_{dc} = 0 \qquad (2.1)$$

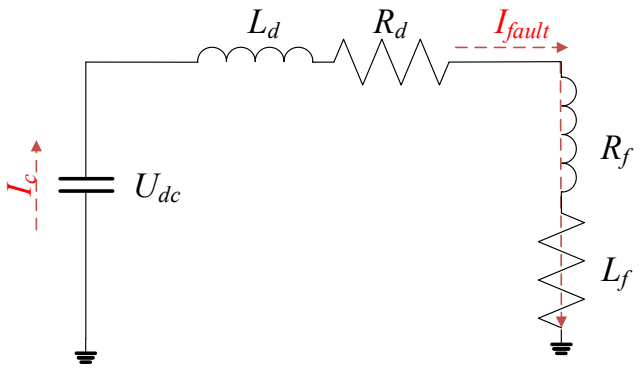



**Figure 2-2: Equivalent Circuit of DC Capacitor Discharging for Pole-to-Ground Faults [24]**

As the discharge of the dc capacitor continues, the dc voltage begins to rapidly decrease. When the ac voltage exceeds the dc voltage, the fault current begins to flow through the converter, triggering self-protective blocking of the IGBTs when the overcurrent exceeds the protective settings of the IGBTs. In this case, it results in the converter operating as an uncontrollable freewheeling rectifier, which draws the fault current from the ac network. During this stage, the fault current increases even more, and its behavior is determined by the ac network short circuit strength, the location of the fault, the converter topology and its configurations, and the impedance associated with the converter transformer and dc lines [10] [16]. The equivalent circuit in the ac network feeding stage is shown in Figure 2-3.

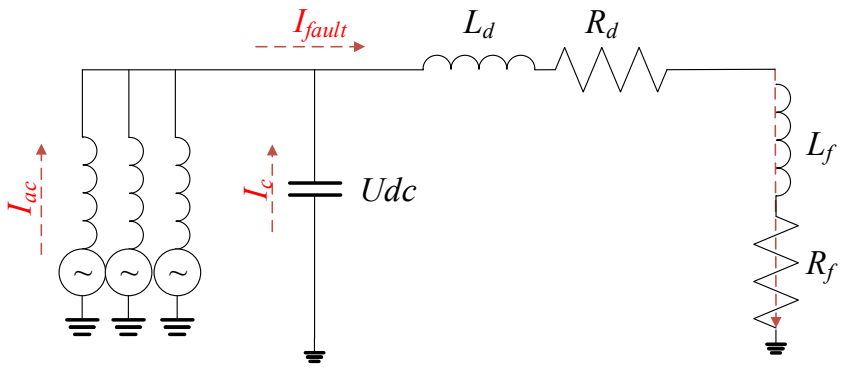



**Figure 2-3: Equivalent Circuit of AC Network Feeding Stage for Pole-to-Ground Faults [24] [25]**

Similar to the initial capacitor discharging stage, the resistance in the formed current loop will limit the amplitude of the fault current. If the converter employs full-bridge MMC or other submodule topologies with fault interruption capability, fault current from the ac network can be blocked, limited or controlled based on the control scheme for dc fault [2] [10] [13]. For asymmetrical monopole configuration with the converter transformer ungrounded on the converter

side, since there is no grounding current path for a pole-to-ground fault, additional transient ac fault current is only drawn from ac system when ac voltage is greater than the dc voltage. Once the voltage levels between the poles have been rebalanced, the fault current draw from the ac system will cease [16].

## 2.3. Pole-to-Pole Faults

Pole-to-pole faults can occur at where the two pole conductors make contact or when insulation breakdown causing a fault across positive and negative poles. Its equivalent circuit can be represented as shown in Figure 2-4. The fault current flows from the positive pole through the fault impedance and returns to the negative pole via the negative line.

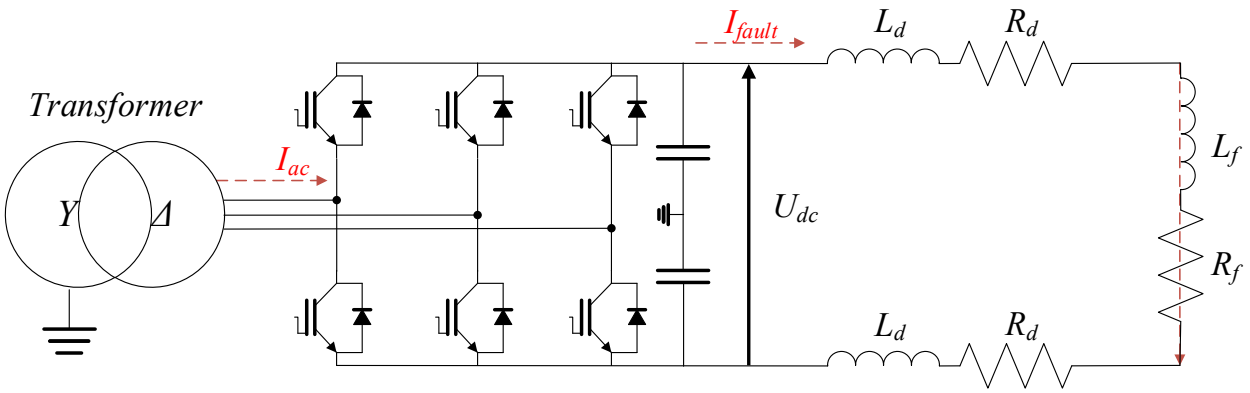



**Figure 2-4: Equivalent Circuit Diagram of VSC DC Pole-to-Pole Fault [25] [26]**

During the initial stage following the fault, the dc capacitor discharges, resulting in a rapid dc voltage collapse. As shown in Figure 2-5, the fault current profile is influenced by the L/R/C

characteristic of the dc networks. The reduction of the dc voltage leads to the fault current being drawn from the ac network and flowing to the fault through the converter's freewheeling diodes.

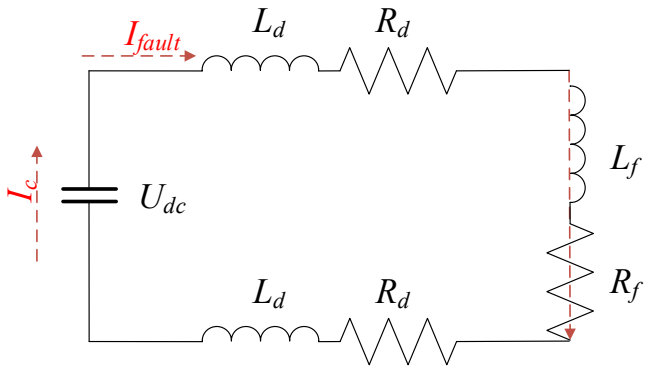



**Figure 2-5: Equivalent Circuit of DC Capacitor Discharging for Pole-to-Pole Faults [25] [26]**

A pole-to-pole fault current during the transient initial stage behaves in a similar manner to a pole-to-ground fault, both of which are dominated by the discharging of the dc capacitor. However, as compared to a pole-to-ground fault, a pole-to-pole fault can be more severe, resulting in a higher fault current and greater impact on the connected system, because of the lower fault resistance of a pole-to-pole fault when compared to a pole-to-ground fault [16] [27].

In a full-bridge MMC, after the fault is detected and submodules are blocked, the fault current momentarily continuous to feed the fault through the FWDs (D1 and D4) as shown in an equivalent circuit diagram Figure 2-6, where a possible fault current path flows across a and b phase through the top and bottom phase arms of the converter. After the energy in the ac arm inductors is discharged, the fault current will decay to zero due to the greater dc voltage $2U_c$ ($U_c$ representing the voltage of the half phase arm's equivalent capacitors) in comparison to the ac line-to-line voltage ($V_{ab}$) [28].

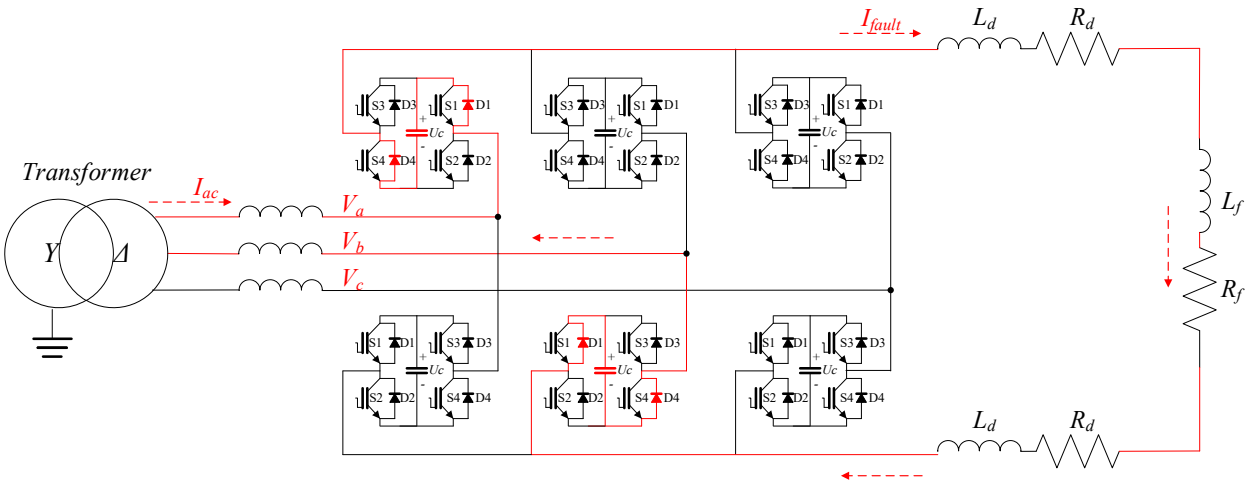



**Figure 2-6: Equivalent Circuit Diagram of Full-Bridge VSC for Pole-to-Pole Fault [13] [28]**

## 2.4. Summary

This chapter analyzes and discusses the behavior of dc line faults in a point-to-point VSC-HVDC transmission system, specifically pole-to-pole faults and pole-to-ground faults with a ground connection. Through this review, system and design parameters were found such as inductance, resistance, fault location on the dc network and ac system strength would affect and determine the fault current behavior. A pole-to-pole fault is regarded more severe compared to a pole-to-ground fault, but less likely to occur in a point-to-point HVDC transmission system utilizing overhead transmission lines. To avoid damage to converter equipment due to excessive fault current and to ensure the stability and availability of interconnected ac networks, the system and design parameters identified in this chapter should be properly considered in dc fault clearance techniques, and in conjunction with properly designed protection strategies.

# Chapter 3.

# MMC Submodule Designs for DC Fault Clearance

## 3.1. Introduction

When implementing a VSC-HVDC design, half-bridge topology is the straightforward and cost-effective option for MMC converter design, and thus the most common type of submodule [29]. However, during a dc line fault, the IGBTs in half-bridge submodules are blocked forming a short circuit that allows continuous fault current to feed into the dc side fault until the ac-side breaker is tripped or, if available, the DCCB is activated. To address the dc fault handling capability, the full-bridge submodule topology was implemented in conjunction with other submodule design variations to enable dc fault clearance [29]. Sections 3.2-3 of this chapter go over the design, operation principle, and dc fault handling capability of the full-bridge and clamp-double submodule designs.

## 3.2. Full-Bridge Submodule design

Each full-bridge submodule in the MMC topology is controlled individually to generate the approximate sine wave shape shown in Figure 3-1. Its four operational modes are as follows:

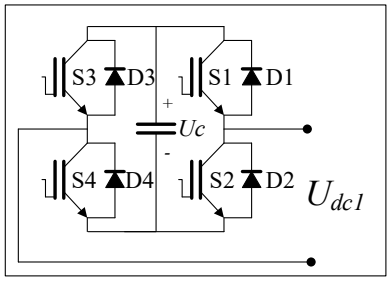
a) Blocking mode: With all IGBTs turned off,

b) Bypassed mode: When S1 and S3 are activated, or when S2 and S4 are activated, the submodule is bypassed.

c) Positive insertion: When S1 and S4 are turned on, the capacitor inserts its voltage $+U_c$, and the capacitor is charged or discharged depending on the direction of the current *i*.

d) Negative insertion: With S2 and S3 are turned on, the capacitor inserts its voltage in the reverse polarity $-U_c$, and the capacitor is charged or discharged depending on the direction of the current *i.*

During a DC fault, the fault current can be controlled/managed by inserting a voltage opposite the ac line voltage; and by blocking all the IGBTs, the submodule naturally blocks the voltage of the same magnitude as the charged submodule capacitor [29].




| Operation States | Gates (ON) |
|---|---|
| Insert + Uc | S1, S4 |
| Insert - Uc | S2, S3 |
| Bypass | (S1, S3) or (S2, S4) |
| Blocked | None |

**Figure 3-1: Full-bridge Submodule and Operation States**

Research and studies have also suggested that respecting the full-bridge submodule operability maintaining current control during a dc line fault, fault current can be suppressed to zero while the converter remains synchronized and connected to the ac system in reactive power control. Both dc and ac system can benefit from a timely post-fault power recovery in the event of the transient dc fault [30]. However, as previously stated, a full-bridge submodule design requires twice the number of IGBTs as a half-bridge design, significantly increasing converter losses and cost.

## 3.3. Clamp-Double Submodule Design

Full-bridge MMC has an additional switching state with the negative voltage insertion; however, it is also a drawback using double the number of IGBTs with double the conduction losses during normal operation. As a result, novel submodule topologies are designed to offer fault current blocking and handling capabilities while also minimizing normal conduction losses through the use of fewer semiconductors. Clamp-double submodules were introduced as an alternative topology to the full-bridge submodule to reduce power losses and to incorporate dc line fault handling capability [31]. The clamp-double submodule, as illustrated in Figure 3-2, is essentially two half-bridge submodules clamped together in series through two additional clamping diodes and one additional IGBT. According to Table 3-1, in normal operations it is equivalent to two half-bridge submodules in normal operation, with an additional IGBT (S5) and three distinct voltage levels across the submodule terminals. During a dc line fault, all IGBTs are switched off, both capacitors for voltage clamping are inserted, and the fault current is reduced to zero. Despite the fact that the clamp-double MMC is capable of blocking the dc side fault, it can only generate half the reverse voltage generated by the full-bridge MMC. Therefore, if the grid voltage is sufficiently high, the fault current can flow [29] [32].

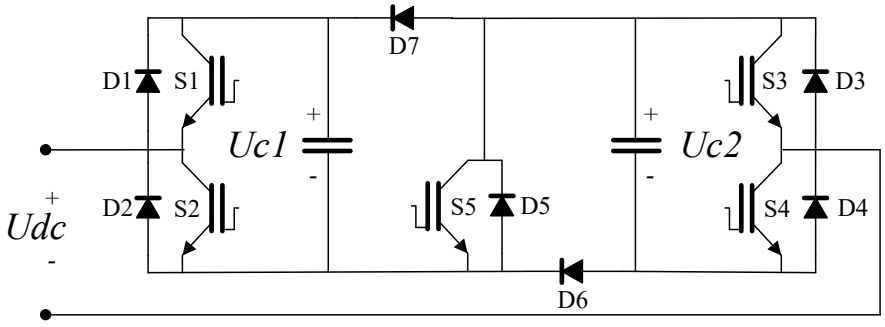



**Figure 3-2: Clamp-Double Submodule of an MMC Valve**

**Table 3-1: Switching States of Clamp-Double Submodule**

| Operation States | Gates (ON) |
|---|---|
| Insert $+U_{c1}$ | S1, S3, S5 |
| Insert $+U_{c2}$ | S2, S4, S5 |
| Insert ($U_{c1}$+$U_{c2}$) | S1, S4, S5 |
| Bypass | S2, S3, S5 |
| Blocked | none |

## 3.4. Summary

This chapter discussed the full-bridge and clamp-double submodule designs. Their component counts and performance were compared to those of half-bridge submodule designs, as summarized in Table 3-2. For the purposes of this comparison, it is assumed that there are a fixed number ($M$) of capacitors per MMC arm. Calculations are made for the number of capacitors and IGBT switches, as well as the average number of IGBT switches in normal operation stages. The clamp-double submodule has a higher conduction loss than the half-bridge submodule but a lower conduction loss than the full-bridge submodule. A clamp-double or full bridge based MMC has both dc fault blocking and fault control capabilities; however, due to the clamp-double based MMC's half equivalent dc reserve voltage, its fault control capability is limited in comparison to a full- bridge based MMC.

**Table 3-2: Comparison of Submodule Designs**

| Submodule Design | NC | NS | NON | DC Fault Blocking | Losses | Voltage Levels |
|---|---|---|---|---|---|---|
| Half-bridge | $M$ | $2M$ | $M$ | No | Low | 0, $U_c$ |
| Full-bridge | $M$ | $4M$ | $2M$ | Yes | High | 0, $\pm U_c$ |
| Clamp-Double | $M$ | $2.5M$ | $1.5M$ | Yes | Moderate | 0, $\pm 1/2U_c$, $U_c$ |

*NC*: Total number of Capacitors per arm
*NS*: Total number of IGBTs per arm
*NON*: Average Number of IGBTs connected during normal operation
$U_c$: Equivalent voltage across one submodule terminals
*M*: Number of capacitors per MMC arm

Due to the thesis's scope and limitations, additional submodule design variations are listed for reference but are not reviewed in detail: a unipolar-voltage full-bridge submodule design based on a full-bridge submodule with S3 replaced by a FWD will reduce the cost and switching power losses associated with a full-bridge submodule design [33] [29]; to further improve the clamp-double submodule design's dc fault handling capability, a five-level cross-connected submodule was proposed in [34]; to further reduce switching power losses, a three-level cross-connected submodule was introduced in [33]; and finally, a number of researchers have focused on hybrid submodule topologies using half-bridge mixed with full-bridge, clamp-double or other submodule designs with dc fault blocking capabilities to reduce the cost and power losses [33] [35] [36] [37].

In conclusion, depending on the scope and specification of the project, a full-bridge based MMC provides a better performance defined by shortest fault clearing time during a dc side fault with a higher equivalent dc reverse voltage for VSC-HVDC systems, disregarding the cost and losses. Additionally, new topologies and hybrid submodule configurations are being introduced and developed with a goal to provide the same level of fault handling capability while featuring lower power losses.

# Chapter 4.

# HVDC Breakers

## 4.1. Introduction

The fundamental difference in realizing dc breakers compared to ac breakers is the absence of the current zero crossing [13]. Additionally, when compared to ac systems, dc systems have a low damping factor. As a result, a dc fault current has a much higher rate of rise, necessitating a fast control and protection system together with a rapid means of interrupting the fault current, such as dc breaker. Consequently, the dc breakers must meet the following requirements [7] [9] [23]:

1) Generating a zero current for fault interruption,
2) Absorbing or dissipating the energy stored in system inductance,
3) Rapid current interruption,
4) Low losses during normal operation, and
5) Ability to tolerate the network's voltage response following current interruptions.

The first two requirements are particularly difficult to fulfil with a single component; however, multiple parallel paths within a breaker assembly can be used to assign the requirements to different elements [19]. A conceptual DCCB arrangement is demonstrated in Figure 4-1, illustrating a typical DCCB configuration, which consists of a nominal current path, a commutation path, and an energy absorption path.

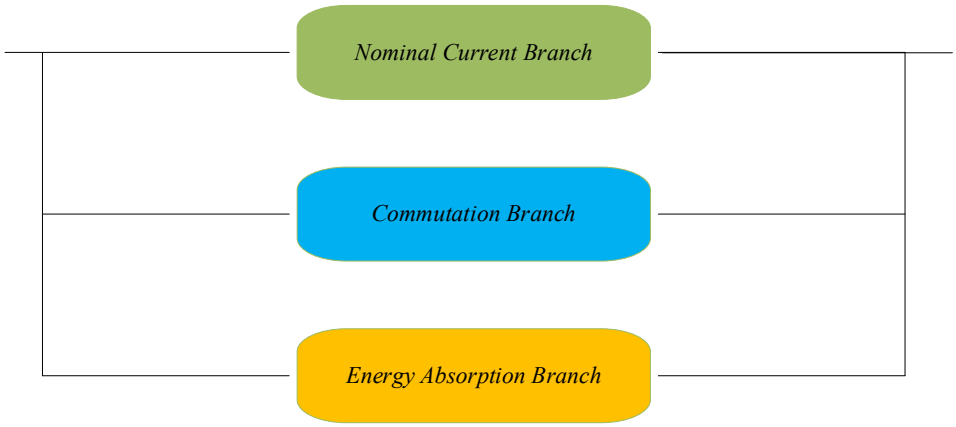



**Figure 4-1: Conceptual Topology of a DCCB**

The nominal current path is comprised of a low-loss main branch interrupter in the closed position. During a dc line fault, the commutation path assists in fault current interruption and commutates line current into the parallel energy absorption path for dissipating the system's inductive energy.

Current can be suppressed to zero in a dc system by generating a counter voltage greater than the system voltage [19]. The greater the counter voltage, the faster the fault current decays to zero and the shorter the time required for an interruption. Different technologies have been used to generate this counter voltage. Three different breaker technologies are discussed in this chapter: mechanical circuit breakers, power-electronic breakers, and proactive hybrid mechanical and power-electronic breakers. The working principle of each circuit breaker type will be presented first, followed by sample prototypes, installation, and research concepts. Finally, their relative advantages and disadvantages are evaluated referencing to published technical papers.

## 4.2. Standard Fault Current Interruption Process and Definitions

CIGRÉ joint working group A3/B4.34 Technical Brochure No. 683 [16] established a standard dc fault current interruption process and also definitions for comparing DCCBs and other clearance methods analytically. Figure 4-2 adapted from [16] illustrates a standardized overview of a fault interruption process, irrespective of breaker type, topology, or design.

1) Prior to the fault inception, the flat line represents the pre-fault current, which is plotted as a solid line, and the voltage across the dc circuit breaker is plotted as a dashed line; 2) The vertical dashed-dotted line with remark of fault inception indicates the instance when the fault occurs; 3) A protection relay needs to detect the fault (detection time) and select faulty line (selection time) before a trip command will be initiated to the circuit breaker. If the proactive type of circuit breaker is used, an intermediate order could also be issued prior to the trip initiating the interruption process; 4) The breaker begins commuting the current from the nominal branch to the energy absorption branch upon receipt of the trip order; 5) During the time required for internal current commutation, the voltage across the dc circuit breaker increases to its peak Transient Interruption Voltage (TIV). The fault current reaches its peak value and begins to decrease as the voltage across the dc circuit breaker builds up to counter the system voltage at the breaker location. 6) The inductive energy in the faulted system is dissipated during the fault current suppression time, and the fault current reduces to the leakage current level, at which a residual current breaker can open to interrupt the fault if it is equipped.

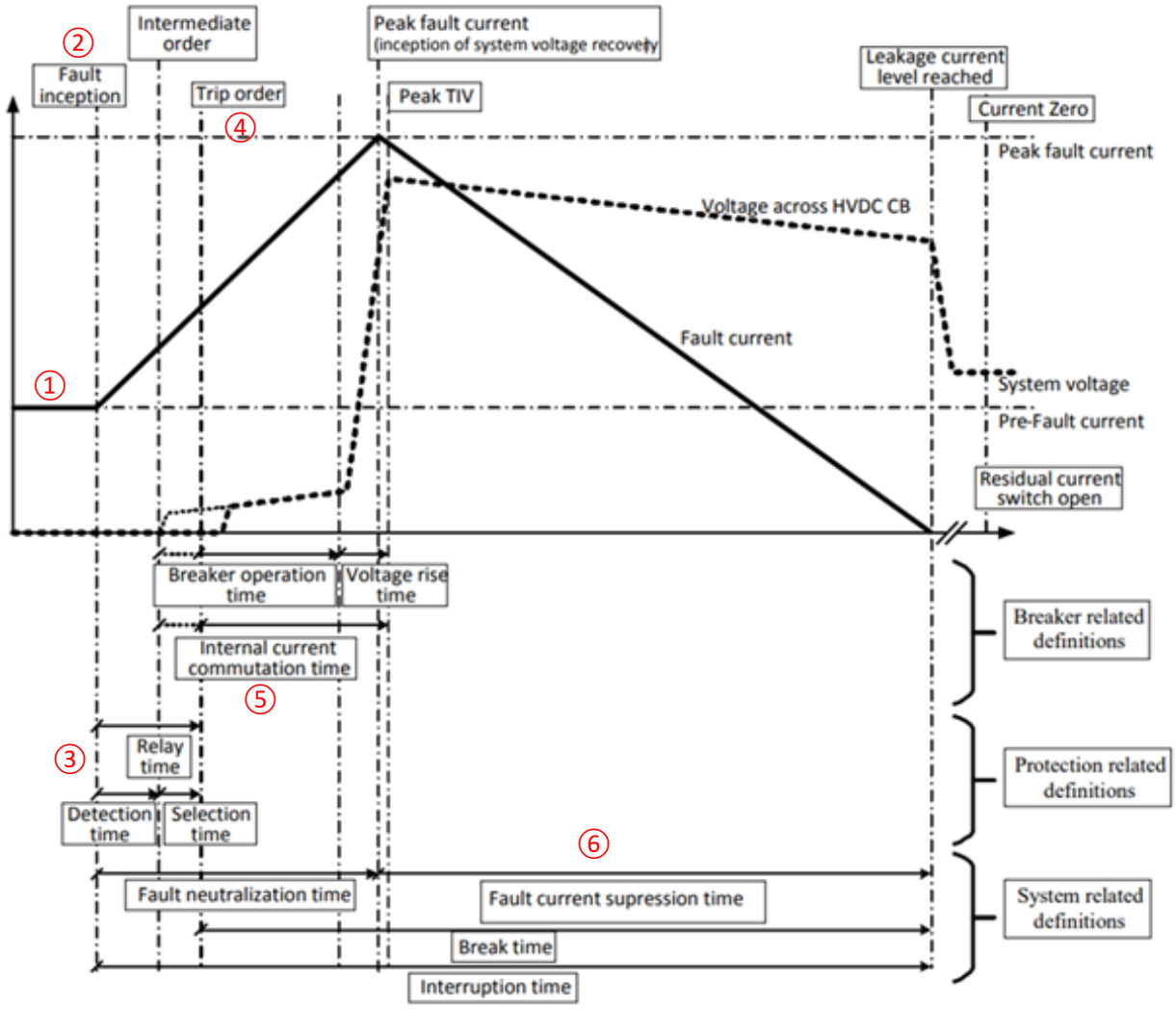



**Figure 4-2: Schematic of a Fault Current Interruption Process [16]**

The critical timing parameters and their definitions are included in Table 4-1. These well-established industry parameters and definitions will be used throughout this thesis for HVDC breaker operating principle descriptions, examination, and evaluation of fault current interrupting performance. Internal current commutation time and fault current interruption capability have been identified as critical technical specifications for evaluating different breaker design topologies. Even though published technical papers and technical references [38] [39] have indicated that the

total interruption time should be within 5ms. Based on the industry recommended guidelines [16] the dc protection system such as dc breaker should be able to clear the dc line fault within 20-40ms, which is comparable with LCC-HVDC; correspondingly, any dc breaker topology investigated in this thesis must have an internal current commutation time of less than 10 milliseconds to meet the HVDC fault clearance requirement, ensuring equipment safety and interconnected ac system stability.

**Table 4-1: Fault Current Interruption Process Definitions [16]**

| Parameters | Definitions |
|---|---|
| Detection Time | The time for protection or control system to detect the fault using sensing device and embedded protection calculation algorithm. The time required for detection is included in the relay time. |
| BRK Operation Time | Between the reception of the trip command and the commencement of the DCCB interruption voltage increase, this time interval is defined as part of the internal current commutation time. |
| Voltage Rise Time | This time period is also included in the internal current commutation time, which ends when the transient interruption voltage (TIV) reaches its peak value. |
| Internal Current Commutation Time | It is the total of the Breaker Operation Time and Voltage Rise Time, beginning with the receipt of the trip order and ending with the peak TIV across the DCCB. |
| Fault Neutralization Time | It is the time interval between the occurrence of a fault and the moment at which the fault current reaches its maximum value. |
| Fault Current Suppression Time | It begins with the maximum value of the fault current and ends with the fault current being decreased to the leakage current level (or below). |
| Break Time | It is the combination of the Internal Current Commutation Time and the Fault Current Suppression Time; from the time the trip order is received to the time the fault current is decreased to the leakage current level (or below) |
| Interruption Time | It is the total time required to interrupt the fault current from the time the fault occurs to the time the fault current is reduced to the leakage current level (or below) |
| Intermediate Order(s) | Any proactive order issued prior to the trip initiating the interruption process particularly for the proactive type hybrid DCCB types |

## 4.3. Mechanical Circuit Breaker

Mechanical dc circuit breakers are frequently used in point-to-point LCC HVDC converter stations for a variety of switching functions, including high-speed bypass switch (HSBS), neutral bus switch (NBS), neutral bus ground switch (NBGS), parallel line switch (PLS), earth/metal/ground return transfer switches (ERTS, MRTS, GRTS), and isolation switches [16] [19]. To meet the specific needs of a high voltage dc fault clearance, two methods, namely passive oscillation and active current injection, are used to interrupt dc fault currents when the current is forced to a zero crossing.

### 4.3.1. Passive Oscillation Mechanical Circuit Breaker

#### *4.3.1.1. Operating Principle and Basic Functionality*

A passive oscillation-type mechanical dc circuit breaker, illustrated in Figure 4-3, is composed of a primary mechanical interrupter, a parallel coupled oscillating circuit consisting of an inductor and a capacitor, and an energy dissipation element. When the main interrupter is opened in response to a trip command, an electric arc forms between the contacts, and a circuit loop consisting of the mechanical interrupter, inductor, and capacitor experiences a negatively damped resonance oscillation. As the amplitude of the oscillation rises, a current zero eventually occurs in the nominal current path presenting an opportunity to interrupt dc current [9] [16] [40] [41].

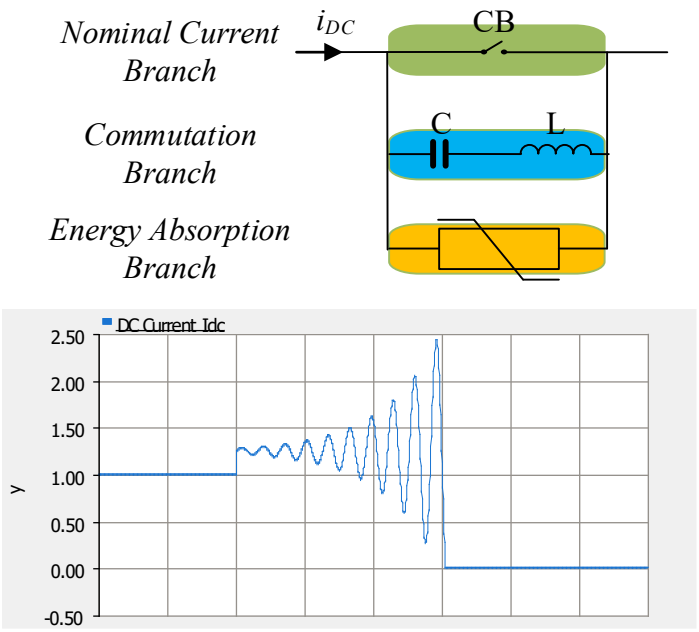



**Figure 4-3**: **Passive Oscillation DC Breaker Operating Principle [16] [42]**

The selection and design of the inductance ($L$) and capacitance ($C$) values define the oscillation frequency, while the counter arc voltage created by the main interrupter opening determines the oscillation amplitude [16]. Following interruption in the nominal current branch, the dc fault current is commutated to the commutation branch and charges the capacitor, while the surge arresters in the energy absorption branch limits the capacitor's maximum voltage to the clipping voltage of the arresters; once the clipping voltage is reached, the current is commutated to the energy absorption branch and dissipated via the low dynamic resistance, effectively reducing the dc current to zero [16] [42] [43].

Internal current commutation time is determined in this design by the dimensions of the L-C components, which are also closely related to the interrupter selection and its arc voltage characteristic [16]. The interrupters' arc voltage characteristic is critical in generating the current

oscillation required to obtain current zeros. While the surge arresters in the energy absorption path have no effect on the commutation time, their clipping voltage level has an effect on the fault current suppression time as part of the overall break and interruption times that influence the voltage stability of the connected ac system [16].

#### *4.3.1.2. Example Prototype Designs*

Two prototypes of passive oscillation dc circuit breakers were designed in the late 1980s [42] [44] [45], and both prototypes were field-tested at the Celilo station of the Pacific Interconnection HVDC scheme. Cigré's joint working group A3/B4.34 reviewed and summarized the design details, component electrical dimensions, and performance in [16]; they are referenced in Table 4-2.

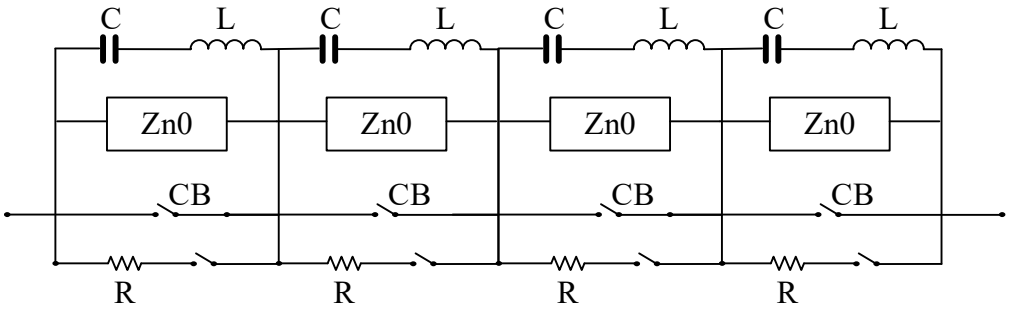



**Figure 4-4: Schematic of Passive Oscillation CB Prototype 1 [44]**

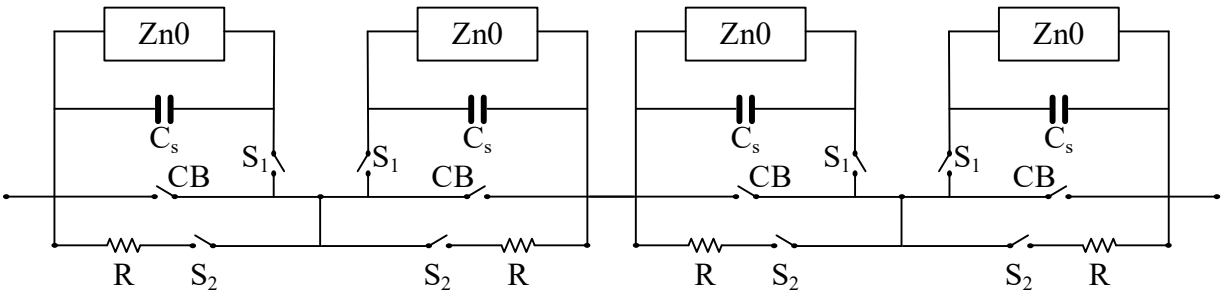



**Figure 4-5**: **Schematic of Passive Oscillation CB Prototype 2 [45]**

**Table 4-2: Specification Summary of Passive Oscillation CB Example Prototypes**

| Prototype | Main Interrupter Type | Num. of Modules | Rated Voltage (kV) | Rated Current (kA) | L (*u* H) | C (*u* f) | f (kHz) | Arrester Type | Arrester Clipping Voltage (kV) | Internal Current Commutation Time | Break Time (mS) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Airblast | 4 | 500 | 4.4 | 400 | 1.25 | 7 | ZnO | 200* | 12 | 30-50** |
| 2 | SF6 | 4 | 500 | 2.2 | 40 | 3 | 14.5 | ZnO | 175* | 14 | 30-50** |

* Rating per module
** Value estimated based on references [44] [45]

Prototype 1 is rated at 500 kV and 4.4 kA with a modular design, consisting of four modules connected in series using ac air-blast circuit breakers, and zinc oxide discs for energy absorption [44]. In the laboratory, this prototype design was tested and found to have an internal current commutation time of 12 ms with a current interruption capability up to 5.5 kA [16]. Instead of using air-blast circuit breakers, example prototype 2 was designed using modified ac Sulfur Hexafluoride (SF6) puffer interrupters. This second topology has a comparable internal current commutation time to prototype 1 but was rated and tested at half of the 2.2 kA rated current. The passive oscillation circuit is commonly used as transfer switch or commutation switch in LCC-HVDC, but this design topology with a break time of over 30 ms, and internal commutation time larger than 10 ms does not meet the technical requirement for dc fault clearing application as defined in the Section 4.2.

### 4.3.2. Active Current Injection Circuit Breaker

#### *4.3.2.1. Operating Principle and Basic Functionality*

In comparison to passive oscillation dc circuit breakers, active current injection mechanical circuit breakers generate the counter oscillating current by actively switching in a commutation branch of

pre-charged capacitor and an inductor using a high-speed switch [16]. Under normal load conditions, referring to Figure 4-6, only the main interrupter $CB_1$ in nominal current branch is closed while $CB_2$ remains open. A station service source may be used to provide a negative pre-charged voltage to the capacitor C in commutation branch [39]. When the interrupting process begins, the main interrupter $CB_1$ is commanded to open in response to a dc fault. Simultaneously, $CB_2$ is closed, the pre-charged capacitor C is oscillatory discharging through the inductor L in a manner similar to that of a passive oscillation mechanical dc breaker, but with faster and higher successful interruption rate due to a larger oscillation amplitude caused by activity switching a pre-charged capacitor [16] [45] [46].

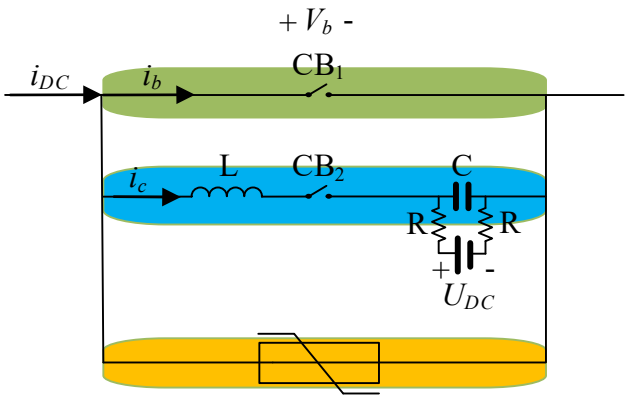



**Figure 4-6: Active Injection DC Breaker Operating Principle [38]**

The key functional and design distinction opposed to a passive oscillation type is that an active injection scheme imposes a discharging current in the opposite direction and of higher magnitude than the dc current to be interrupted. "Almost instantly, a counter voltage is created" effectively suppressing the fault current to zero noted by Cigré joint working group A3/B4 [16, p. 173]. The process of dc current interruption using an active current injection HVDC CB is illustrated Figure

4-7 [16]. Equations (4.1) to (4.4) are excerpted from [16] [46] and re-stated below to express the dc current injection phenomenon.

$$\boldsymbol{i_c = \frac{U_{DC}}{\sqrt{L/C}}} \tag{4.1}$$

$$\boldsymbol{f_c = \frac{1}{2\pi\sqrt{L * C}}} \tag{4.2}$$

$$\boldsymbol{\frac{di_c}{dt} = \frac{U_{DC}}{L} cos(\frac{t}{\sqrt{L * C}})} \tag{4.3}$$

$$\boldsymbol{\frac{dV_b}{dt} = \frac{i_{DC}}{C}} \tag{4.4}$$

where:

| | |
|---|---|
| $U_{DC}$ | : pre-charging voltage |
| $L$ | : reactance in commutation path |
| $C$ | : capacitance in commutation path |
| $f_c$ | : oscillating frequency |
| $i_c$ | : discharging current |
| $V_b$ | : voltage across the breaker |
| $i_{DC}$ | : dc line current |
| $i_b$ | : current through the circuit breaker |
| $di_c/dt$ | : discharging current rate of change |
| $dV_b/dt$ | : transient recovery voltage rate of change |

Based on the equations derived, the key equipment dimensions of the commutation branch C-L, and capacitor pre-charging voltage $U_{DC}$ will determine or be designed for the "injecting current" amplitude and frequency. When the current is interrupted at the point where the capacitor $C$ is completely discharged and the residual voltage is zero, the *Transient Recovery Voltage* (TRV) begins to rise from zero at the rate described in (4.4). However, if current interruption occurs before

the capacitor $C$ is fully discharged with a residual voltage, the initial TRV shown in Figure 4-7 will present across the interrupter [16]. To ensure successful fault current interruption at current zero crossing point, the amplitude of the discharge current $i_c$ must be greater than the fault current $i_{DC}$, and the discharging rate $di_c/dt$ and rate of rise $dV_b/dt$ at current zero point must also be evaluated and set to a values within the safe operating range for which interrupter $CB_1$ was designed [16] [46].

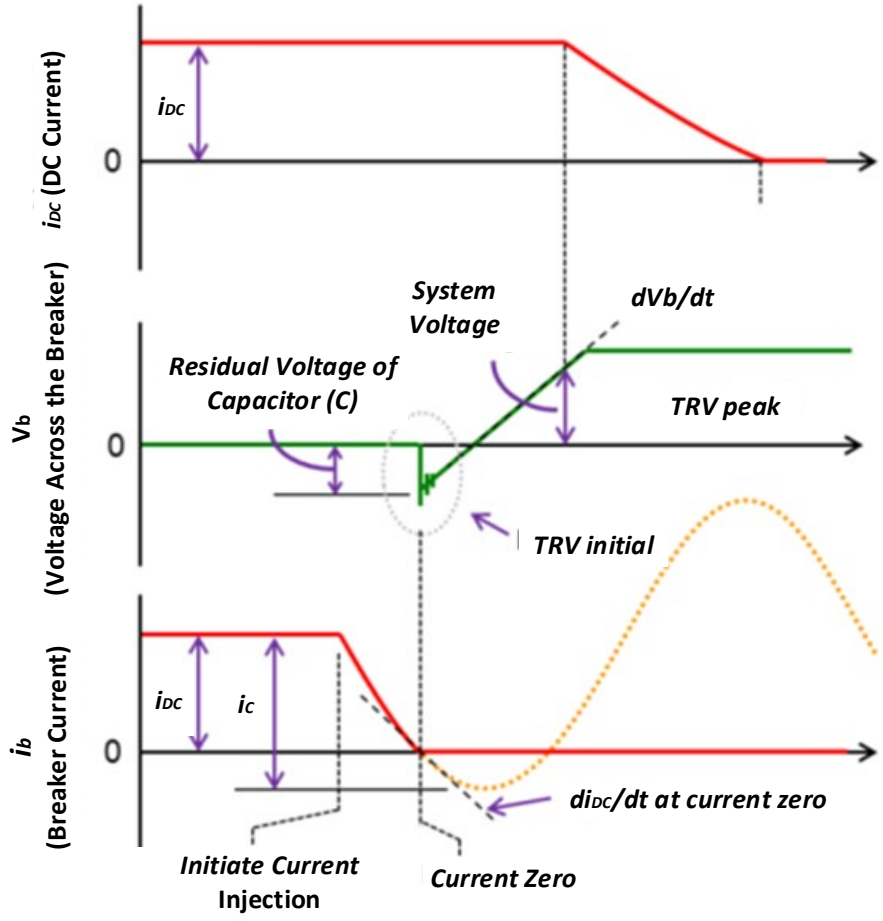



**Figure 4-7: DC Current Interruption Process by Active Injection CB [16]**

Investigations, research, and prototype testing have shown that the active current injection circuit breaker's capabilities and interruption speed are sufficient to meet typical dc fault clearance requirements of under 10 milliseconds internal current commutation time [47].

#### *4.3.2.2. Example Prototype Designs*

Prototype design by Mitsubishi Electric

Mitsubishi Electric developed and tested an active current injection dc circuit breaker prototype as part of the PROMOTioN project. This prototype is rated at 100 kV and has a 16 kA short circuit current interruption capability [47]. The principal schematic of the designed prototype is given in Figure 4-8. This design is composed of a high voltage vacuum interrupter in the nominal current branch, a high-speed making switch to regulate the capacitor discharge in the commutation branch, and energy-absorbing *metal oxide surge arresters* (MOSAs) in the energy absorption branch [47].

Additionally, this prototype design features an additional parallel-connected making switch and pre-charged capacitors, denoted in Figure 4-8 by the dashed line as high-speed making switch 2 (HSMS2). Following the first interruption using the first high-speed making switch (HSMS1), the HSMS2 can be used to inject another high frequency oscillating current to create another current zero for the second interruption [47].

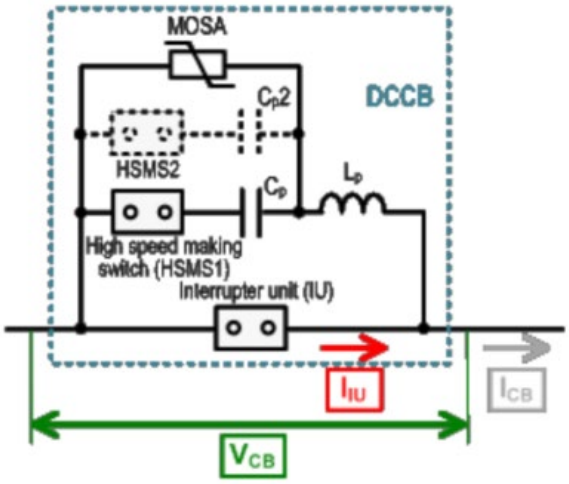



**Figure 4-8: Schematic Circuit Diagram of an Active Current Injection DC Circuit Breaker Prototype designed by Mitsubishi Electric [47]**

The pre-charged capacitor $C_p$ is charged at a constantly applied voltage. After the main high voltage vacuum interrupter received the tripping command, the contacts start to separate. With a few milliseconds delay, the high-speed making switch discharges $C_p$ through $L_p$, and imposes an oscillatory high frequency (in the order of several kHz) counter current forcing the main interrupter's current zero crossing, while the residual current is commutated to the current injection branch, which charges the capacitor [47]. The voltage across the vacuum interrupter is quickly recovered and exceeded over the nominal system voltage, before being clipped by the MOSA limitation voltage, which is chosen at 1.5 pu of the rated system voltage [47]. By stacking modules and utilizing the 100 kV vacuum interrupter unit, a 320 kV HVDC CB was developed and tested to interrupt dc currents of 145 kV and 16 kA with an internal current commutation time of 5.64 ms [47]. Figure 4-9 illustrates the schematic diagram of HVDC circuit breaker, as well as its tested voltage and current waveforms.

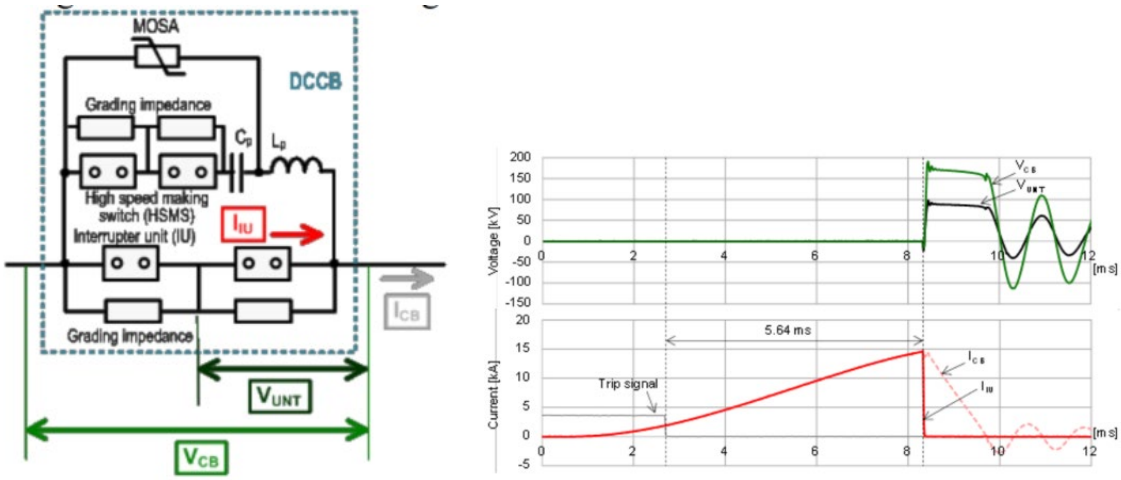



**Figure 4-9: Schematic Circuit Diagram of HVDC Circuit Breaker with Double Breaks and its Testing Results at 145kV 16kA Conditions [47]**

Nan'ao HVDC CB by China Southern Power Grid

Three active current injection HVDC CBs were installed as part of an upgrade to the Nan'ao multi-terminal HVDC system in order to improve dc fault clearance capability. It has a lower component cost, a smaller injection circuit component size, and a compact design due to the use of an air-core coupling reactor [48]. This commercially installed CB is rated at 160 kV and has a short circuit current interruption capability of 9.2 kA, a peak TIV of 272 kV, and a breaker internal current commutation time of 3.9 ms, according to laboratory testing [48]. The detailed layout of an installed active injection breaker topology is depicted in Figure 4-10 (a). The breaker is divided into three major branches:

1) the main branch is composed of four series-connected vacuum interrupters, while the combined RC-grading circuits (grading capacitor $C_j$, static-sharing resistor $R_x$, and damping resistor $R_j$) ensure equal voltage distribution during dynamic events and steady state operation [48],

2) the current injection branch is split into two parts, one for *High Voltage* (HV) side and one for *Low Voltage* (LV) side. The two parts are coupled by an air-core coupling reactor with high coupling factor which enables high energy-transfer efficiencies at high frequencies [48],
3) and the energy absorption branch includes of banks of surge arresters.

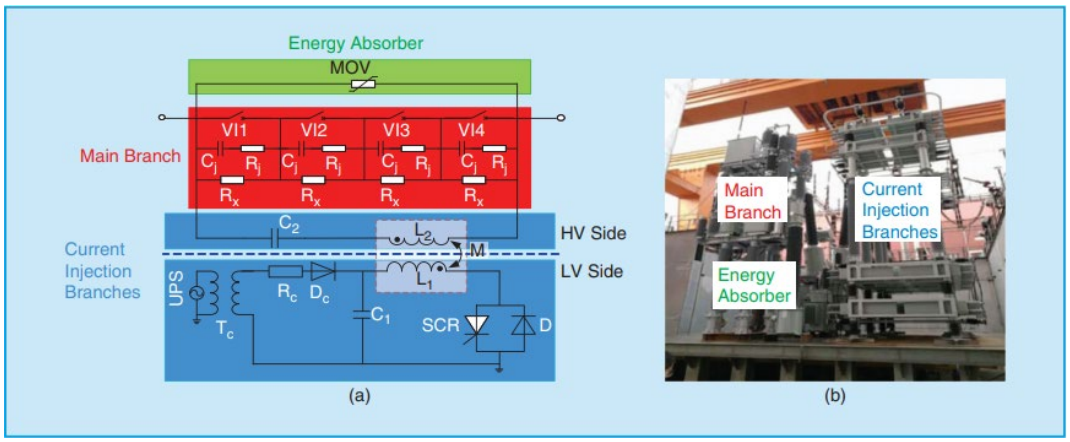



**Figure 4-10: (a) Detail layout of Current Injection DC Circuit Breaker Designed for Nan'ao Multi-Terminal HVDC system; (b) Photo of a Design Prototype [48]**

Nan'ao HVDC CBs use an *uninterruptible power system* (UPS) boost circuit through an isolation transformer $T_c$, which is then rectified into a dc voltage to charge the pre-charging capacitor $C_1$ [48]. When a fault occurs, the main interrupters are commanded to open; and the SCR is triggered for conduction after contact separate to the effective distance to tolerate the recovery voltage and able to interrupt a current. The pre-charged capacitor discharges through SCR and $L_1$. The energy from LV side is transferred to the HV side through the coupling reactor, which generates high-frequency oscillating current on the $L_2$-$C_2$ in the HV side of current injection branch. At the instant of arc extinction, dc current commutates into the $L_2$-$C_2$ injection branch and voltage across

capacitor $C_2$ gradually increases until the surge arresters in the energy absorbing branch reach their threshold voltage. Surge arresters dissipate the energy stored in the dc circuit, effectively reducing the dc current to zero and ultimately interrupting it. In this DCCB design, a thyristor is used to trigger the current injection, resulting in non-arc triggering in comparison to the previous design using high speed making switch; additionally, by utilizing the two voltage level commutation branch (current injection branch), the capacitor $C_1$ only needs to be charged at the low voltage level, reducing insulation requirements and also saving and reducing cost and assembly size [49].

### Proposed Topology Using Pulse Generator and Vacuum Tube

This proposed active current injection topology in a monopolar configuration, as shown in Figure 4-11(a), was introduced in [50], and a brief description is included in [16]. This alternative active current injection CB scheme differs fundamentally from the other topologies, and may be extended to a bipolar configuration, as shown in Figure 4-11b, by adding a second breaker with middle grounding tap [50]. It is composed of five primary components:

- two *Hybrid Breaking Units* (HB) utilizing a vacuum tube switch with low conduction losses and a paralleled diode in the nominal current branch for bidirectional applications;
- two *Damping Branches* (DB) formed by *Metal Oxide Varistor* (MOV) based arresters and a series connected diode to regulate current direction during fault current suppression time;
- one *Pulse Generator* (PG) controlled by a single thyristor stack.

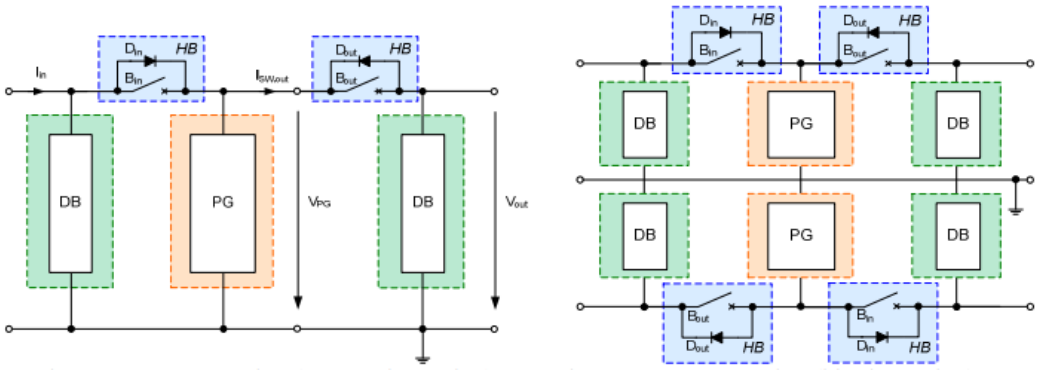



**Figure 4-11: (a) Monopole Layout of a Proposed Current Injection CB (b) Bipolar Layout of the Proposed Current Injection CB [50]**

The pulse generator branch is connected across the dc poles or between the dc pole and ground, depending on the design used; and is constructed with a diode $D_{PG}$ to ensure unidirectional current flow and to prevents capacitor ($C_{PG}$) from discharging into any external fault [16]. Thyristors ($T_{PG}$), as shown in the detailed layout Figure 4-12, are used to trigger pulse generator because they have a higher pulse current capability and simpler gating controls than IGBT [50].

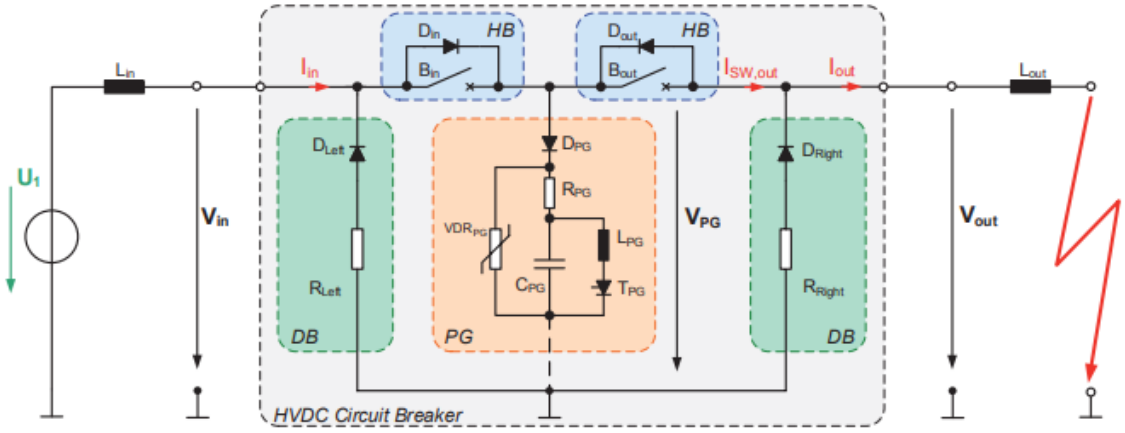
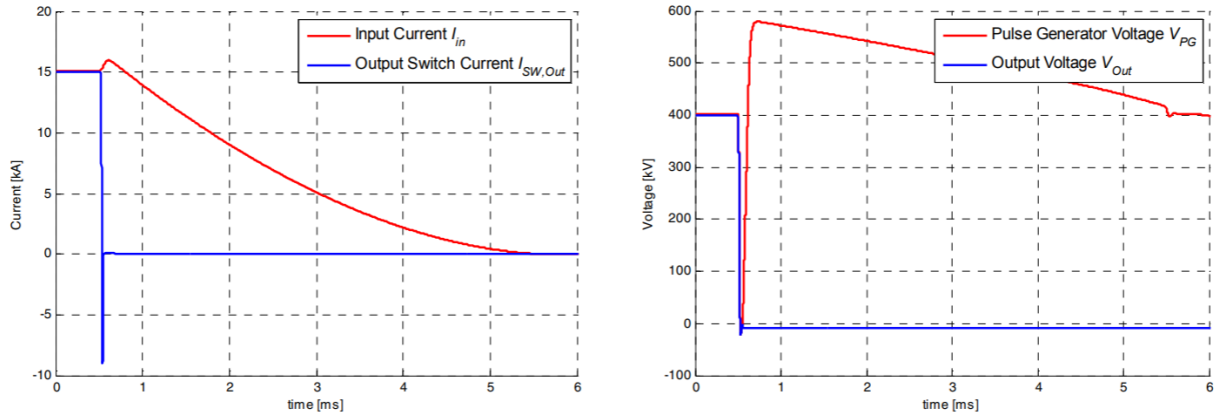



**Figure 4-12: Detailed Layout of the Proposed Current Injection DC CB [50]**

The pulse generating capacitor $C_{PG}$ is permanently charged to the dc line voltage during normal operation, obviating the requirement for auxiliary power supply [51]. As a result, the number of interruptions is not limited by the capacitors or charging supplies.

When a fault occurs, fault current flows from the $L_{in}$ through $L_{out}$ and into the fault, as shown in the Figure 4-12. After the protection system detected the fault, the vacuum tube switch contacts in the HBs are immediately opened, resulting in an interior plasma between the contacts [50]. When the contacts are opened far enough to withstand the transient recovery voltage, the pulse generator will fire the thyristor stack. The capacitor $C_{PG}$ then is discharged through the reactor $L_{PG}$, immediately reversing capacitor's voltage polarity and drawing a large current through the $D_{PG}$ which generating a high pulse current flow through the two damping branches and causing the diodes in the HB to conduct, effectively allowing the interrupter to open at zero current [52]. When the current flowing through the thyristor stack decreases to zero, the thyristor stack is naturally turned off [50]. Finally, the counter voltage generated by the surge arrester will reduce the fault current to zero and eventually interrupt it.

Y. Wang and R. Marquardt's simulation results for a rated 450kV CB employing the proposed topology are presented in Figure 4-13 (a) and (b) [51]. The simulation's CB composed of 15 pulse generator sub-modules, each of which contains a pulse capacitor of $C_{pg}$=70 μF and inductor of $L_{pg}$=10 μH [16]. A dc fault current of 15 kA was interrupted after 3.5 ms, full testing results are summarized and available in technical brochure [16] and Y.Wang and R. Marquardt's technical paper [51].




(a) (b)

**Figure 4-13: (a) Simulation Results Switching Current (b) Simulation Results for Switch Voltage [50]**

## Overview of Performance

In this section three active injection circuit breakers are listed, and their design and performance specification are summarized in Table 4-3.

**Table 4-3: Specification Summary of Active Current Injection Circuit Breakers**

| Prototype | Main Interrupter Type | Num. of Modules | Rated Voltage (kV) | Short Circuit Current (kA) | f (kHz) | Arrester Type | Arrester Clipping Voltage (kV) | Internal Current Commutation Time (mS) |
|---|---|---|---|---|---|---|---|---|
| Mitsubishi Electric | Vacuum Interrupter | 4 | 320 | 16 | NA | MOSV | 480* | 5.64 ** |
| China Southern Power Grid | Vacuum Interrupter | 1 | 160 | 9.2 | 2.5 | MOV | 200 | 3.9 ** |
| Wang & Marquardt | Vacuum Interrupter | 15 | 450 | 15 | NA | MOV | NA | <1* |

* Value based on simulation data

** Value based on Laboratory tested results

## 4.4. Power-Electronic Circuit Breaker

A power electronic circuit breaker consists of two parallel branches as shown in Figure 4-14. The nominal current branch uses semiconductor switches as the normal current conducting path and as well as the interruption means during a dc fault. The nominal current branch is supported by a paralleled energy absorption branch, which is typically formed by MOV and other similar varistor elements. In the event of a dc fault, fault current is stopped by turning off the semiconductor switches in the nominal current branch [38], and rerouted through the energy absorption branch where the varistor elements will protect the semiconductor switches from overvoltage and dissipate the fault current . Due to the absence of mechanical switches, this type of CB is capable of rapidly commutating current and interrupting the fault current in the microsecond range [16].

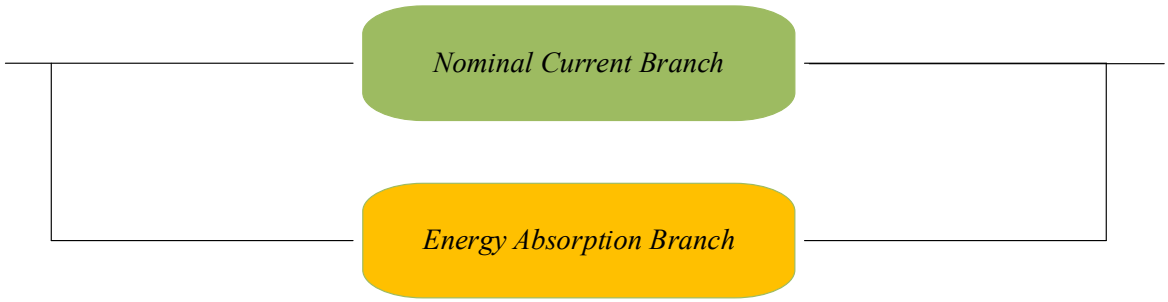



**Figure 4-14: Basic Layout of a Power Electronic Circuit Breaker**

Thermal limits are a critical design consideration for power electronic switches [38]. Typically, a high voltage and/or high current CB is constructed using power electronic switches connected either in parallel to increase the current breaking capability and/or connected in series to increase the voltage rating of the breaker. These switches in the nominal current branch can be IGBTs [53],

or *Integrated Gate Commutated Thyristors* (IGCT) [54], and they can be configured in variety of topologies [55] [56]. At present, due to the high voltage requirement, the HV power electronic switches must be constructed using a large number of series connected devices. Consequently, due to the high cost and power losses (≤30% of the total VSC-HVDC system [38] [57] [58]), pure power electronic circuit breakers are not suitable for the HVDC transmission system application [52]. Therefore, this type of circuit breaker is not further considered in this thesis.

## 4.5. Proactive Mechanical and Power Electronic Hybrid CB

The *Mechanical and Power Electronic Hybrid* (MPH) dc circuit breaker combines the superior properties of mechanical switches for low conduction losses with the fast operation speed of power electronic switches. As shown in Figure 4-15, a typical *Proactive Mechanical and Power Electronic Hybrid* (PMPH) circuit breaker consists of three branches similar to the mechanical CB, as follows:

- The main current branch provides a normal current path with low losses, and is composed of a current commutation switch and a main branch mechanical disconnector,
- The commutation branch employing a power electronic based commutation breaker,
- The energy absorption branch formed by energy absorption devices such as surge arresters,
- And, a line residual current breaker.

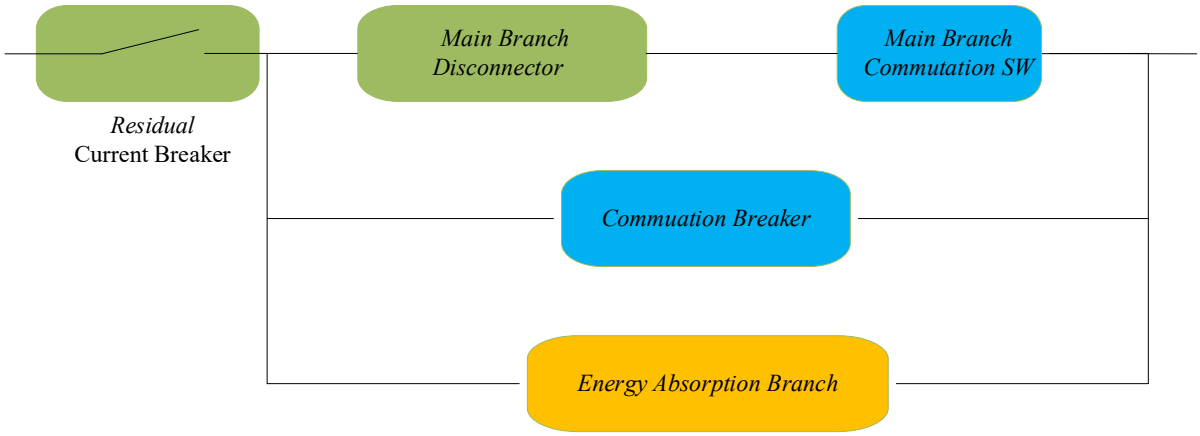



**Figure 4-15: Basic Layout of a Proactive Mechanical and Power Electronic Hybrid CB**

### 4.5.1. Operating Principle and Basic Functionality

The main operational difference between PMPH HVDC CBs and mechanical HVDC CBs is that while mechanical CBs perform fault current interruption inside the mechanical interrupter unit, PMPH CBs perform the fault current interruption in the commutation branch by turning off power electronic switches, that are connected in parallel to the main current branch and energy absorption branch [38]. The following describes the process of fault current interruption. During normal operation prior to $T_0$, referencing Figure 4-16, current only flows through the main current branch with low losses. At $T_0$, a dc fault occurs, increasing line current. Shortly after that the protection detected fault or in a proactive protection logic when a fault is suspected [52], at $T_1$, the commutation breaker is closed in the commutation branch and the main branch current commutation switch opens, immediately commutating the fault current to the commutation branch and allowing main branch mechanical disconnector to open under effectively no current and without arcing [38]. With the mechanical disconnector in open position, the power electronic commutation breaker in the commutation branch can open and interrupt the fault current. At $T_2$ the

commutation breaker opens by turning off the power electronic switches, and the fault current is now commutated into the energy absorption path, which generates a counter voltage to extinguish the fault current, which is suppressed in the absorption devices [16]. After $T_3$, when the fault current has decreased to a safe level, the line residual current breaker opens to interrupt the leakage current through the CB and associated devices.

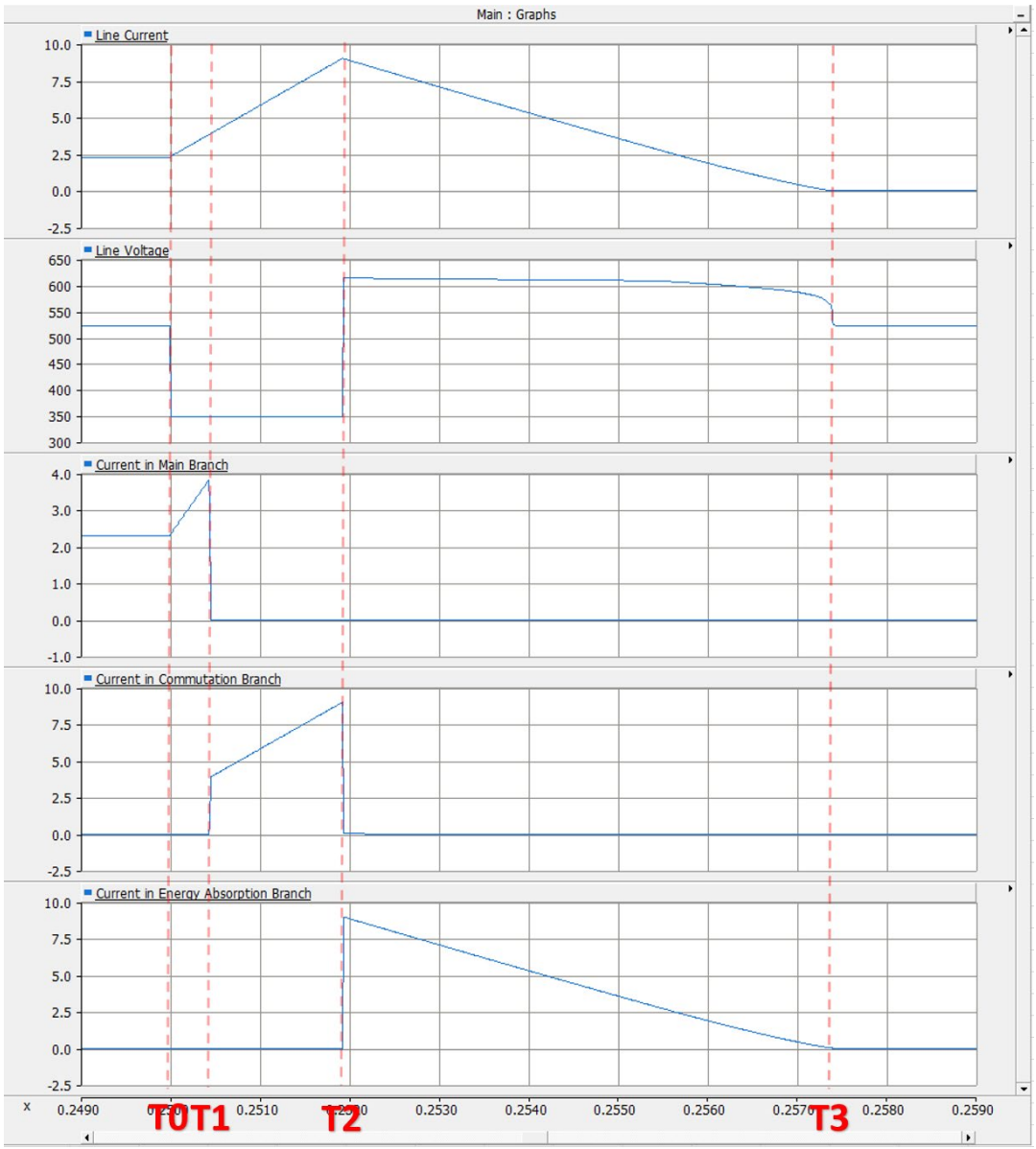



**Figure 4-16: Overall Fault Current Interruption Process for PMPH CB**

In the early stages of the mechanical and power electronic hybrid circuit breaker's development, the basic topology, as illustrated in Figure 4-17, the main current branch only consists of mechanical switches, as opposed to a series connected mechanical disconnector and a power electronic switch used in the PMPH CB. In a MPH CB, the voltage difference between the arc voltage and the forward voltage drop of the semiconductor drives the fault current commutation between the main current path and the commutation path [59], which may result in commutation failure when used in a high voltage level application [52]. By utilizing a conventional mechanical switch, MPH CB also encountered numerous design challenges, including quickly building up voltage across the mechanical switch to commutate the fault current to the commutation branch and rapidly reaching the required insulation strength for the mechanical switch to withstand the transient over voltage before semiconductor switches could be turned off for fault interruption [16].

The proactive design, which incorporates a power electronic current commutation switch and a main branch mechanical disconnector, enables the mechanical disconnector to open at zero current with minimum voltage stress, thereby improving fault current commutation and mitigating the

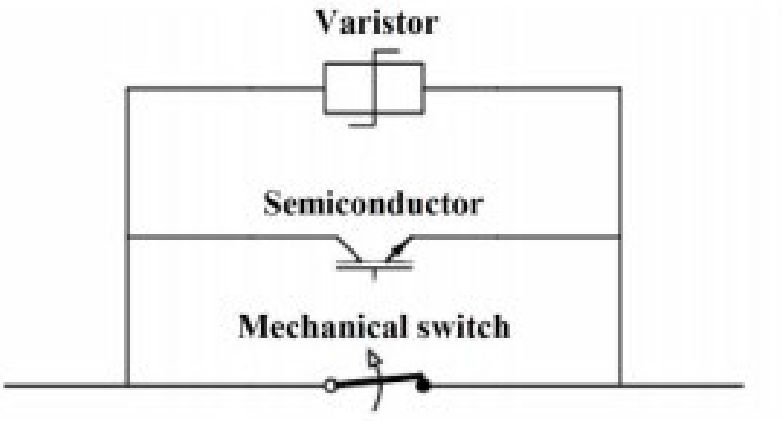



**Figure 4-17: Basic Circuit Diagram of the MPH CB [59]**

design challenges associated with basic MPH CBs. Another key feature "the proactive aspect", which was introduced and described in [58] and later categorized as the PMPH CBs type in [52] , is that current can be commutated from the main current branch to the commutation branch if an overcurrent protection detects a fault. Current can be redirected from the commutation branch back to the main branch if the fault is not materialized [52]. In the event of a genuine dc fault, proactive control compensates for the time delay introduced by the longer mechanical switch opening time by commutating fault current to the commutation branch earlier.

### 4.5.2. Example Prototype Designs

Section 4.5.2.1 and Section 4.5.2.2. present two prototype PMPH CBs that have been developed and installed at the Zhoushan ±200kV five-terminal HVDC systems in China [60], and Zhangbei ±500 kV four-terminal scheme in China [61] for dc fault clearance.

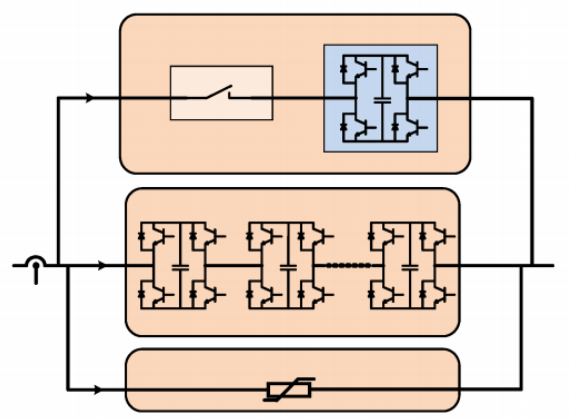
ABB [58] [62, 63] [64], and General Electric (GE) Alstom Grid [65] [66] proposed design prototypes are discussed in Sections 4.5.2.1, and 4.5.2.1 respectively.

#### *4.5.2.1. Zhoushan HVDC System PMPH HVDC CB*

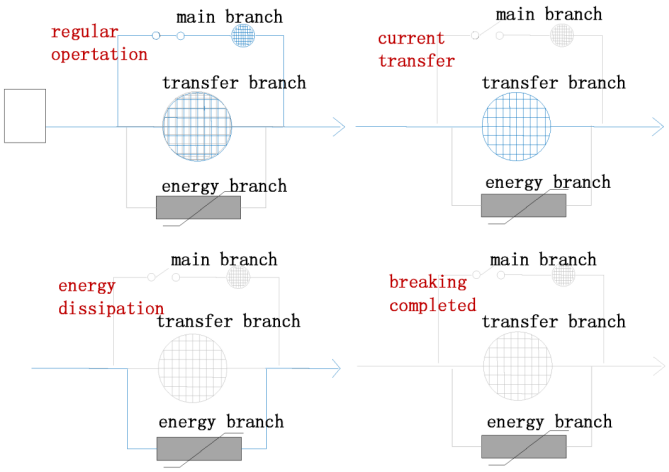
The schematic block diagram for a PMPH HVDC CB used in Zhoushan HVDC system is shown in Figure 4-18a. This CB was designed to operate at a rated voltage of 200 kV, a rated current of 2 kA, and a short circuit current breaking capability of 15 kA with a 3ms breaking time and a 2 ms internal commutation time [60]. The main branch current commutation switch is full-bridge IGBT modules that support bidirectional conduction and current blocking. Three series and two parallel multiple full-bridge cells comprise the commutation branch, which is used to interrupt dc fault current. Figure 4-18b illustrates the various operation states during normal operation and during fault interruption. During regular/normal operation, two diagonally opposite IGBTs are turned on,

current flows through two paralleled top and bottom IGBTs and diodes bypassing capacitor in the sub-module of the main branch current commutation switch [16]. When the dc fault occurs, the full-bridge IGBT modules in main current branch are turned off, and the capacitors in the sub-module act as snubber capacitors, charging through the diodes and transferring current to the commutation branch [52]. The ultra-fast disconnector begins to open during this time. Within about 2 milliseconds, the disconnector opens sufficiently to withstand transient interruption voltage, and the main branch current commutation switch modules are turned off. The fault current is then routed to the commutation breaker, which charges the capacitors in the full-bridge submodule. When the voltage across the commutation breaker exceeds the clipping level of the arresters in the absorption branch, the fault current is commutated into the surge arrester, where the excessive inductive energy is dissipated.

This prototype is constructed in a compact modular manner and can be scaled to accommodate higher system voltages and currents. This dc circuit's overload capacity was determined, and the results are shown in Figure 4-18c.



a)

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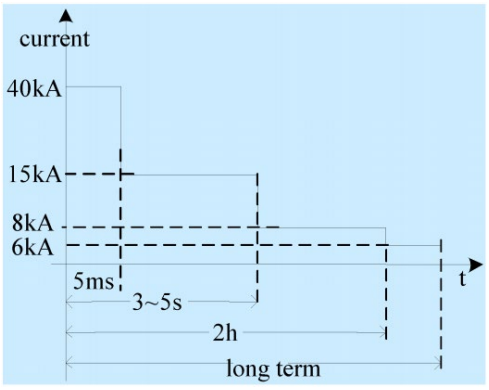



c)

**Figure 4-18: a) Schematic Block Diagram for PMPH CB in Zhoushan HVDC System; b) Operation Principle top-left: regular operation; top-right: current transfer into commutation branch; bottom-left: energy dissipation in energy absorption branch; c) Overload Capacity with Different Current Levels [60]**

#### *4.5.2.2. Zhangbei HVDC System PMPH HVDC CB*

Twelve PMPH HVDC CBs were installed as part of the Zhangbei VSC-HVDC multi-terminal project. The CB design concept, as shown in Figure 4-19 consists of three branches [61]:

- The main current branch includes an ultrafast disconnector connected in series with full-bridge module units,
- the transfer branch (commutation branch) comprised of cascaded diode-based full-bridge module units, and
- Energy absorption branch is made of MOVs connected in parallel to groups of commutation branch submodules.

Similar to the Zhoushan PMPH HVDC CB, the main branch current communication switch incorporates a capacitor in series with a diode. When the switch is turned off, the capacitor and diode act as a snubber circuit, charging through the diode and IGBT antiparallel diodes.

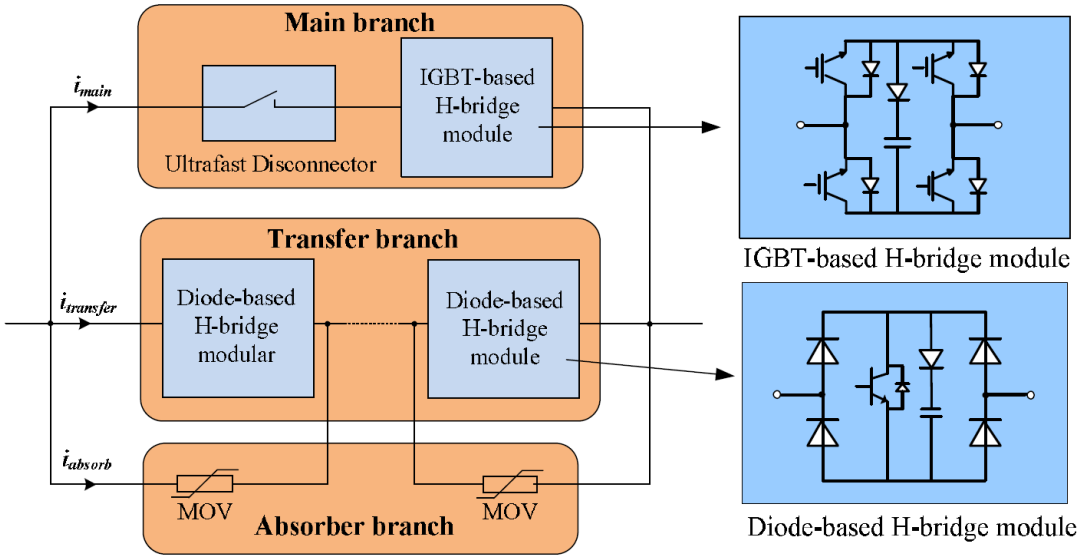



**Figure 4-19: Schematic Diagram of PMPH CB in Zhangbei HVDC System and the Power Electronic Switch Module Topologies [61]**

The diode-based full-bridge module in Zhangbei's design for commutation breaker consists of four fast recovery diodes and IGBTs as well as a snubber capacitors [61], shown in Figure 4-19 and Figure 4-20. It operates as illustrated in Figure 4-20: (a) in the conducting state, regardless of the direction of external current flowing through D1-IGBT-D3 or D4-IGBT-D2, the IGBT can be used to turn off the current; (b) in the blocking state, when the IGBT is turned off, current flows through the snubber circuit, which charging up the voltage across the switch [61].

As with normal operation, current can flow in either direction through the ultra-fast disconnector and sub-modules in the main current branch, all of which have a low on-state impedance. When a fault occurs, the main current branch's semiconductor modules are turned off, forcing the fault current to be commutated to the commutation branch. After the ultra-fast disconnector has travelled a sufficient distance to gain the TIV withstand capability, the diode-based full-bridge modules in the commutation branch are turned off. As a result, capacitors in the commutation branch's submodules are charged until the voltage exceeds the clipping voltage threshold level of the energy absorption branch's surge arresters. The short circuit current is then commutated to the energy absorption path, which is used to dissipate excess system energy.

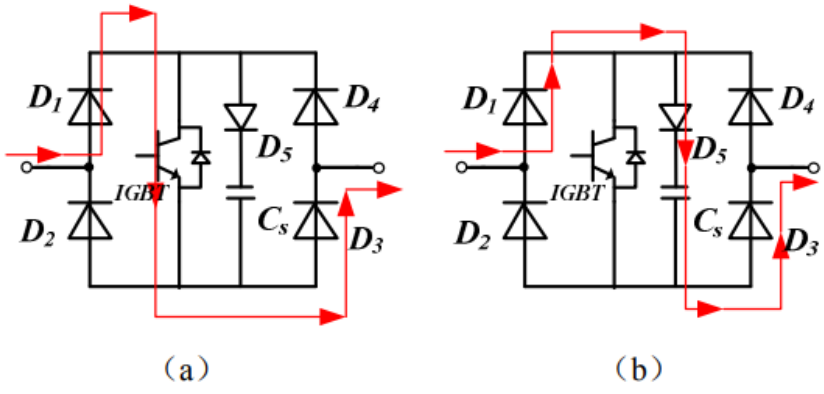



**Figure 4-20: Operation Principle of Diode Based Full-bridge Module: (a) Conducting State; (b) Blocking State [61]**

This circuit breaker is modular in design and rated at voltage value of 535 kV, 3 kA rated current, and tested to 26 kA interrupted current. The results of reclosing test include two short-circuit current breaking tests are shown in Figure 4-21. The fault current begins to rise at time 1ms in the zoomed-in waveform during the first breaking test (left side of figure). When the current reaches 26 kA shortly after time equals 3ms, or approximately 2ms after the fault current begins, the commutation branch is turned off. In this test, the TIV exceeds 810 kV. The second breaking test was conducted 300 milliseconds later with a maximum fault current of 9 kA and a slightly longer time to neutralize the fault. As with the Zhoushan CB, this design is modular and easily adaptable to various voltage levels.

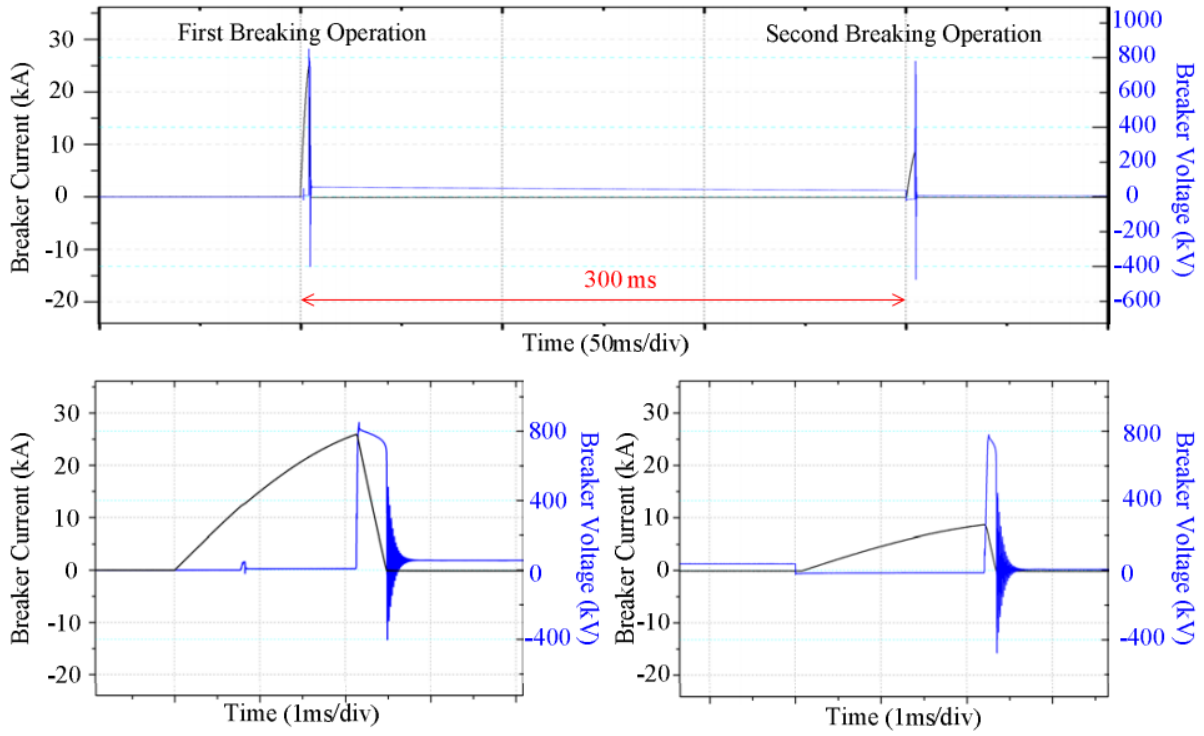



**Figure 4-21: Tests Results of Reclosing Operations with Current (black) and Voltage (blue) across the CB [61]**

#### *4.5.2.1. PMPH HVDC CB Prototype by ABB*

ABB introduced the world's first proactive type mechanical and power electronic hybrid HVDC circuit breaker in 2011, utilizing a fast mechanical switch as the main branch disconnector and series connected new *Bi-mode Insulated Gate Transistor* (BIGT) submodules as commutation switch (auxiliary DC breaker) adapted in the main current branch [58]. The electrical schematic diagram for this breaker is shown in Figure 4-22.

Under normal operating conditions, current flows through the disconnector (fast disconnector) and commutation switch (auxiliary DC breaker) in the main current branch with low on-state losses [58]. Until a trip order is received, the IGBTs that formed the commutation breaker as part of the commutation branch remain off. Once the short circuit fault is detected, the main branch auxiliary DC breaker is turned off, and the fault current is commutated to the commutation branch, with the commutation breaker turned on. Once the fast disconnector is fully opened, the commutation breaker will open to interrupt the short circuit fault. This interruption process relies on the mechanical disconnector's operation speed and its ability to withstand maximum TIV once the

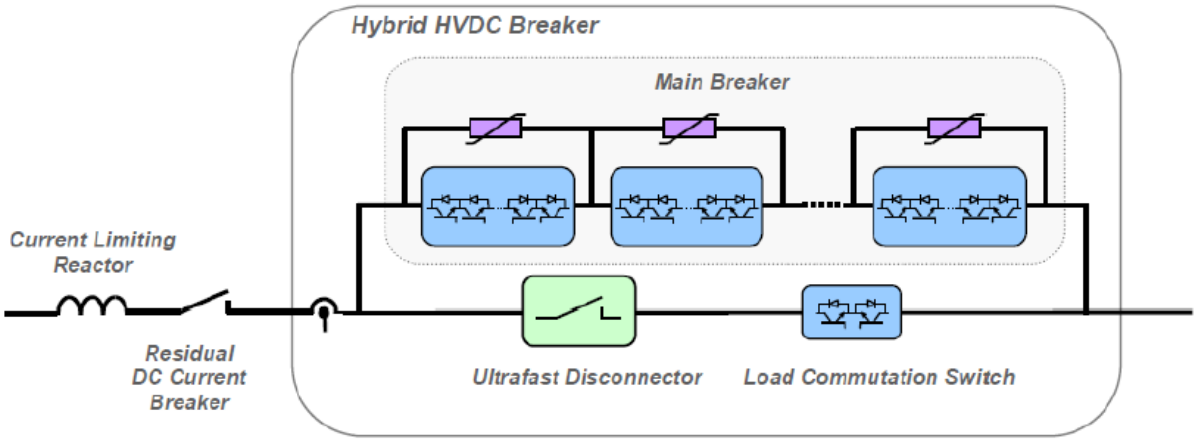



**Figure 4-22: Schematic Diagram of ABB's PMPH HVDC CB [64]**

commutation breaker is turned off, as well as the maximum fault current in the event that sub-component fails during the communication process [63]. To full-fill this requirement, ABB also proposed a new ultra-fast mechanical disconnecting switch in [63].

A prototype 80 kV circuit breaker was constructed and tested with a nominal current of 2.6 kA and a maximum current interruption capacity of 16 kA [16]. The voltage across the commutation breaker and the current flowing through the commutation branch are shown in Figure 4-23 during one of the fault current interruption test. After the test current reaches 1.5 kA, the main branch current commutation switch opens and commutate the current to the commutation branch. Shortly after the commutation switch is opened, the ultra-fast disconnector begins to open and develops dielectric withstand capacity in two milliseconds; at this point, the commutation breaker is switched off and the fault current is commutated to the energy absorption branch. Internal current commutation time in this test is approximately 2.1 ms from the time the test current reaches 1.5 kA to the time when the commutation breaker is turned off [63].

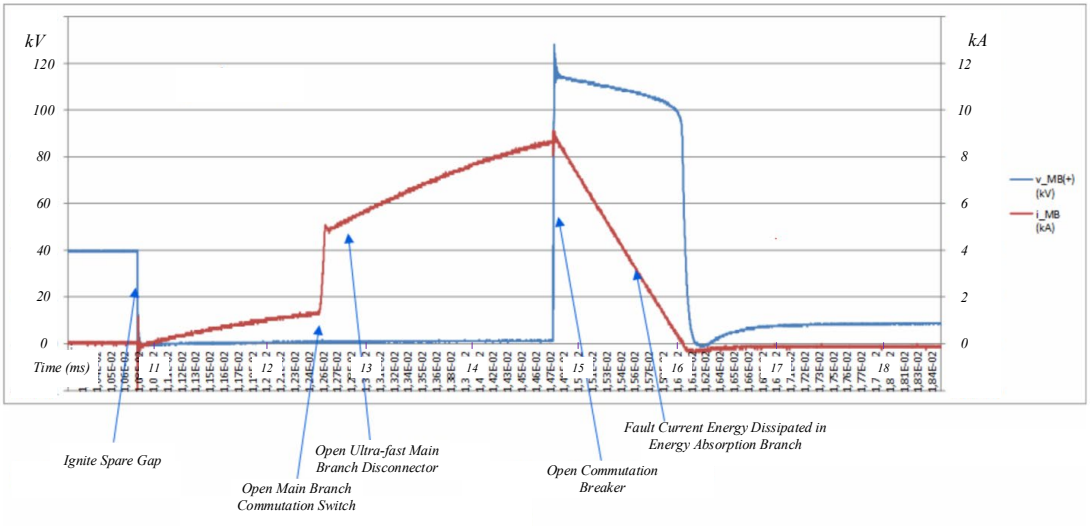



**Figure 4-23: Tests Results of Current Interruption Showing Current (Red) and Voltage (Blue) of ABB PMPH CB [64]**

#### *4.5.2.2. PMPH HVDC CB Prototype by GE Alstom Grid*

GE Alstom Grid developed and tested a PMPH HVDC CB demonstration with support from the European Commission's Twenties EC project [65], and its conceptual schematic diagram is shown in Figure 4-24. As with the PMPH designs previously mentioned, this CB design consists of three branches: The low impedance main current branch is comprised of an ultra-fast mechanical disconnector and a series connection of relatively low-voltage IGBT switches capable of transporting load current with little losses during normal operation. The commutation branch (auxiliary branch) is constructed using multiple paralleled and staged "time-delaying" branches and a "arming" branch, each of which utilizes thyristors tuned on via low voltage gating control and a series connected capacitor and surge arrestor pair to reduce the current to zero, thereby turning off the thyristor.

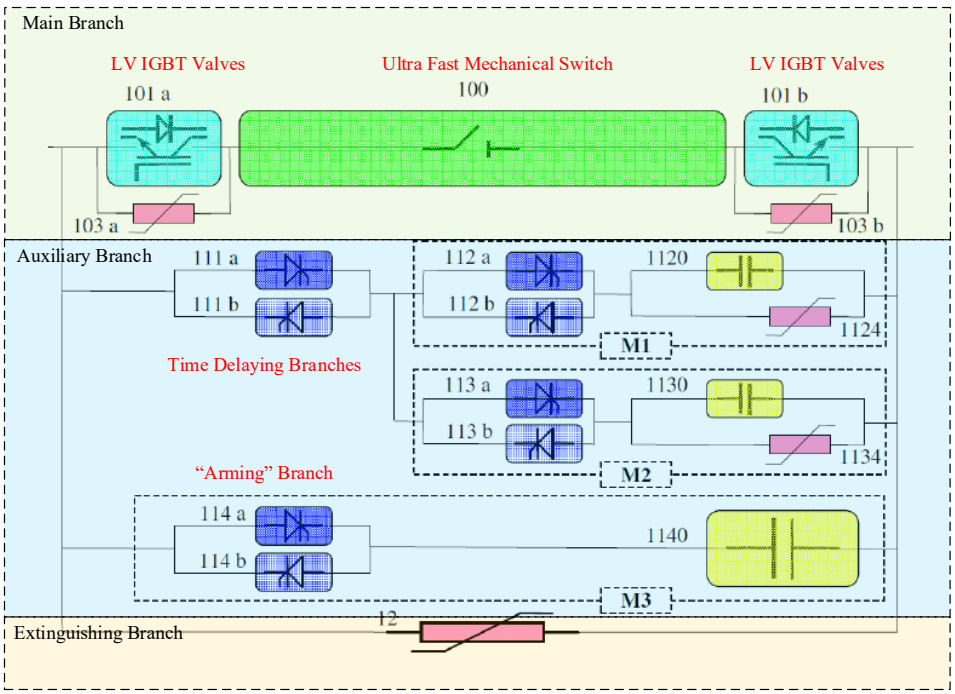



**Figure 4-24: Conceptual Schematic Design of GE Alstom's PMPH HVDC CB [66]**

This topology employs thyristors rather than IGBTs in the commutation branch to take advantage of the thyristor's higher fault current withstand capability while the ultra-fast disconnector is opening, and current interruption in each sub commutation branch is accomplished by connecting a series capacitor to assist in reducing the dc fault current to zero [38] [66]. The commutation branch consists of one “arming” subbranch and multiple “time-delaying” subbranches, which the number of time-delaying branches is depending on the applications and fault current level [65]. The last energy absorption branch (extinguish branch) contains the primary surge arresters for limiting overvoltage and bringing the current to zero.

When a dc fault occurs, the IGBTs in the main current branch are blocked, while the thyristors in the first "time-delaying" auxiliary branch are fired. This switches the current to the first auxiliary path. It is now possible to open the ultra-fast disconnector. Charge will be applied to the capacitor, which suppressed voltage raise, in the first auxiliary path until the parallel surge arrester conducts and clips the capacitor voltage. Following that, the thyristors on the second auxiliary branch are triggered, and insert the second uncharged capacitor. Current is commutated to the second auxiliary branch. Through this commutation, the capacitor in the first auxiliary path discharges into the second auxiliary branch with the opposite polarity of the fault current, generating a current zero crossing the thyristors in the first auxiliary path and so turning them off. As previously indicated, fault current commutates to the third auxiliary branch. Eventually, when the ultra-fast disconnector has successfully opened, the arming branch is fired. When current flows into the arming branch and charges its capacitor, the voltage across the DCCB and across the arming branch's capacitor rapidly increases to the clipping level of the surge arrester in the extinction branch. The counter voltage of the surge arrester leads to fault current suppression and decrease of the voltage across the surge arrester. In a similar manner as previously stated, the arming branch

thyristor will be switched off after the voltage across the CB is decreased to less than the voltage across the arming branch capacitor. The current then flows exclusively through the arrester until the fault current is interrupted.

The demonstration prototype was constructed and tested at 120 kV rated voltage, 1.5kA rated current, and 7.5kA maximum current interruption capability. Figure 4-25 illustrates the interruption test results. The tested breaker tripped when the fault current exceeded 1.5kA, with a current internal commutation time of 2ms [65] [66].

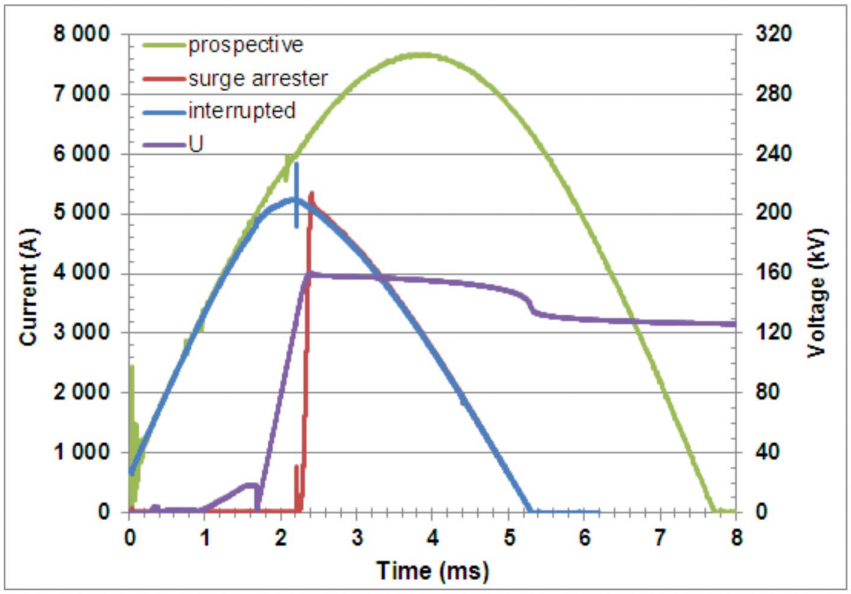



**Figure 4-25: Tests Results of Current Interruption Showing Prospective (Green) and Interrupted Current (Blue), Current Through the Surge Arrester (Red) and Voltage Across the DCCB (Purple) of GE Alstom PMPH CB [66]**

#### *4.5.2.3. Overview of Performance*

In the section, four proposed design and prototype of Proactive Mechanical and Power Electronic Hybrid breakers are described and their design and performance specification are summarized in Table 4-4.

**Table 4-4: Specification Summary of PMPH HVDC Circuit Breakers**

| Prototype | Main Current Commutation SW Type | Commutation Breaker Type | Rated Voltage (kV) | Rated Current (kA) | Short Circuit Current Capability (kA) | Internal Current Commutation Time (mS) | Break Time (ms) |
|---|---|---|---|---|---|---|---|
| Zhoushan | Full-Bridge IGBT | Full-Bridge IGBT | 200 | 2 | 15 | 2 | 3 |
| Zhangbei | Full-Bridge IGBT | Diode-based full-bridge | 535 | 3 | 26 | 1.6* | 2.6* |
| ABB | BIGT | IGBT | 80 | 2.6 | 16 | 2.1* | 3.4* |
| GE Alstom | IGBT | Thyristor, Capacitor and Surge Arresters | 120 | 1.5 | 7.5 | 2* | ~5* |

* Value based on Laboratory tested results

## 4.6. Summary

This chapter discussed the operating principles of nine different types of HVDC circuit breakers in detail, as well as industry-proposed designs and prototypes, including passive oscillation mechanical circuit breakers, active current injection circuit breakers, proactive mechanical and power electronic hybrid circuit breakers. A comparison summary is given in Table 4-5 referencing to the research studies in the literature [16] [39] [38] [52] and takes into account the critical parameters stated in Section 4.2, as well as voltage and current rating, losses, and costs. Due to the high cost and power losses associated with power electronic circuit breakers, they have been omitted from this list, since they are currently not suitable for high voltage applications [52].

**Table 4-5: DC Circuit Breaker Prototypes Performance Comparison Summary**

| Type | Rated Voltage (kV) | Rated Current (kA) | Short Circuit Current Capability (kA) | Internal Current Commutation Time (mS) | Break Time (mS) | Calculated di/dt (kA/ms) | On-State Losses | Total Costs | Reference |
|---|---|---|---|---|---|---|---|---|---|
| Passive Oscillation | 500 | 4.4 | 5.5 | 12 | 30-50** | 0.5 | Negligible | Lower | Pacific Intertie [44] |
| | 500 | 2.2 | 2.2 | 14 | 30-50** | 0.2 | Negligible | Lower | Pacific Intertie [45] |
| Active Current Injection | 320 | N/A | 16 | 5.64** | 7** | 2.8 | Negligible | Low | Mitsubishi Electric [47] |
| | 160 | N/A | 9.2 | 3.9** | N/A | 2.4 | Negligible | Low | Nan'ao MT HVDC [48] |
| | 450 | N/A | 15 | <1* | <5** | 15.0 | Negligible | Low | Wang & Marquardt [50] |
| Proactive Mechanical and Power Electronic Hybrid | 200 | 2 | 15 | 2 | 3 | 7.5 | Low | Higher | Zhoushan MT HVDC [60] |
| | 535 | 3 | 26 | 1.6** | 2.6** | 16.3 | Low | Higher | Zhangbei MT HVDC [61] |
| | 80 | 2.6 | 16 | 2.1** | 3.4** | 4.6 | Low | Higher | ABB Prototype [58] |
| | 120 | 1.5 | 7.5 | 2* | 5* | 3.8 | Low | Higher | GE Alstom Prototype [65] |

*Value based on simulation data

** Estimated time duration based on Laboratory tested results

### 4.6.1. Short Circuit Current Interruption Capability

The short circuit current interruption capability of a circuit breaker is the maximum fault current that it can interrupt without causing damage or an unacceptable electric arc [16] [38]. Mechanical passive oscillation breakers have a maximum current interruption capability up to 5.5 kA, while active current injection breakers can interrupt currents up to 16 kA. For these topologies, the maximum fault current interruption capability is defined and limited by the interrupter type's design and its contact separation speed. In [67] , a newly proposed active current injection CB topology was discussed for the Zhangbei ±500 HVDC transmission project, utilizing a modular design (10 series connected modules), external charging for capacitor and current injection through IGCT, with simulation analysis demonstrating 25kA fault current interruption capabilities. Along with the interruption capability to peak fault current, interrupting lower fault current is more difficult with an active current injection type mechanical DCCB, due to the residual voltage of pre-charged capacitor and initial TIV imposed across the main interrupter [68]. Therefore, it should also be considered in addition to the maximum short circuit current interruption capability through design and evaluated during performance assessment for active injection type DCCB.

For proactive hybrid circuit breaker topology fault current interruption level has been proved experimentally and in commercial service for 26 kA. The hybrid circuit breaker's maximum fault current interruption capability can be expanded and configured to meet a higher fault current requirement due to the hierarchical and modular design.

### 4.6.2. Internal Current Commutation Time

The interruption time, along with the short circuit current interruption capability, are the key criterion for evaluating the suitability of a breaker design or topology for meeting HVDC system

fault clearance requirements. As described in the Cigré technical brochure no. 683, through interruption process, the complete interruption time includes "fault neutralization time which includes relay times (influenced by the protection control), internal current commutation time (influenced by the breaker topology) and fault current suppression time (influenced by the breaker-network insulation coordination, its inductance and energy dissipation element)" [16, p. 202].

Internal current commutation time is compared amongst the different topologies to determine the true performance of the CB during a dc fault. Active current injection circuit breakers can neutralize fault current within 4ms as demonstrated in laboratory testing, and less than 1ms in theory and simulation studies. Hybrid circuit breakers with an internal current commutation time of 1.6-2.1 ms also demonstrated a good performance and have been used in projects to meet the protection requirements of VSC HVDC systems [60] [61].

### 4.6.3. Calculated Rate of Rise of Fault Current

In a point-to-point HVDC system, a DCCB will typically be installed between the converter and dc line (or cable) with a line reactor to limit the rate of rise of fault current to the DCCB design fault current interruption capability [52]. The total inductance of the dc system influences the rate at which the fault current rises. The summary table calculates the rate of rise of the fault current based on the maximum short circuit capability and internal commutation time.

A DCCB that designed with a fault current limiting component such as resistor [69] [70], inductor [71] [72] or superconductor [73] [74] [75], is capable to reducing both the peak as well as rate of rise of fault current, therefore reducing fault current suppression time, overall breaker interruption time and the capital cost of the breaker design due to the reduced interruption capability requirements. The superconductor type of the fault current limiter benefits from low on-state losses,

and fast fault current limiting response of the material physical property can be integrated into the hybrid DCCB design either under normal current branch connected in series with the commutation switch [76] or by replacing the commutation branch together with energy absorption branch, with integrated power electronic switches effectively functioning as a two branch circuit breaker [77]. Additionally, a current limiter may be inserted in the nominal current branch or incorporated into the proactive hybrid type of circuit breaker as an extra current limiting branch to form a four-branch DCCB [78]. Due to the thesis's time constraints, analysis or investigation of the impact of a dc reactor or a dc fault current limiter was not conducted. Additional study and analysis should be undertaken to determine the effect of the reactor or limiter on the rate or rise of fault current, as well as design and the topology selections for dc breakers.

### 4.6.4. On-State Losses

For the mechanical passive oscillation and active current injection circuit breakers with no semiconductor devices in the normal current branch, the power losses are only associated low voltage drop across the metal contacts, and insulated power supply for capacitor charging if it is required for current injection circuit breaker; therefore the on-state losses are negligible [16], and are estimated to be less than 0.001% of the VSC station power losses [39].

The hybrid circuit breakers utilize semiconductor devices in the normal current branch with continuous cooling. The on-state losses are low and are anticipated to be no more than 0.1% of power losses of a VSC station [39].

### 4.6.5. Total Cost

Cost is critical, given the large component count and complexity of HVDC systems. However, because the project agreement is sensitive and confidential, it is difficult to assess the DCCB's

costs. Therefore, the summary table provides only a qualitative and comparative evaluation based on the expected components within different DCCB design topologies.

A passive oscillation mechanical circuit breaker's main components include fast mechanical circuit breakers, reactors, capacitors, and MOSA in the energy absorption branch. Depending on the topology of the active current injection circuit breaker, a semiconductor valve or a mechanical switch may be used. Hybrid topologies incorporate extremely fast disconnectors (or circuit breakers), energy absorbing MOSAs, and a substantial number of semiconductor devices in both the normal current and commutation branches, as well as continuous cooling systems and complex controls. The CIGRÉ joint working group A3/B4.34 technical brochure 683 estimates that the cost of an unidirectional hybrid circuit breaker is "not more than a sixth of the cost of a converter station" [16, p. 204].

In an ac system, a breaker and a half, a breaker and a third or ring bus configurations are used to improve availability, and redundancy from system failure or maintenance outage. In a project using dc breakers for dc fault clearance, redundant semiconductor switches and/or mechanical disconnects should be evaluate and assessed to ensure reliability, availability, and maintainability of the HVDC systems (i.e., adding a second breaker in series would help with reliability, but it would also result in more parts for potential failure and maintenance). As a backup option, an ac breaker may be used to clear the dc fault, but at a considerably slower speed; consequently, if used, converter equipment must be rated for extended fault duration and a higher fault current magnitude.

# Chapter 5.

# Evaluation Methodology and Case Study

In this chapter, a systematic evaluation methodology for dc line fault clearance techniques is proposed and applied to compare dc fault clearing performance of full-bridge MMC described in Section 3.2 and half-bridge MMC with proactive hybrid HVDC breakers of ABB's prototype described in Section 4.3.2.2 using PSCAD/EMTDC Voltage Source Converters benchmark model developed by Cigré Working Group B4.57 [13]. Other comparative assessment considerations, such as losses and cost are explored based on the case model's parameters and the power electronic device specifications. Additionally, a base case model utilizing an ac breaker and a half-bridge model, as well as its fault clearance performance, is presented as a benchmark solution comparison to the two dc fault clearing strategies stated previously.

## 5.1. DC Fault Clearance Evaluation Methodology

The following section describes a step-by-step procedure, as represented in Figure 5-1, for systematically evaluating dc fault clearance solutions. It is critical to understand that the suggested evaluation technique considers only solutions with dc fault clearing and recovery capabilities as a subset of the total system or solution performance.

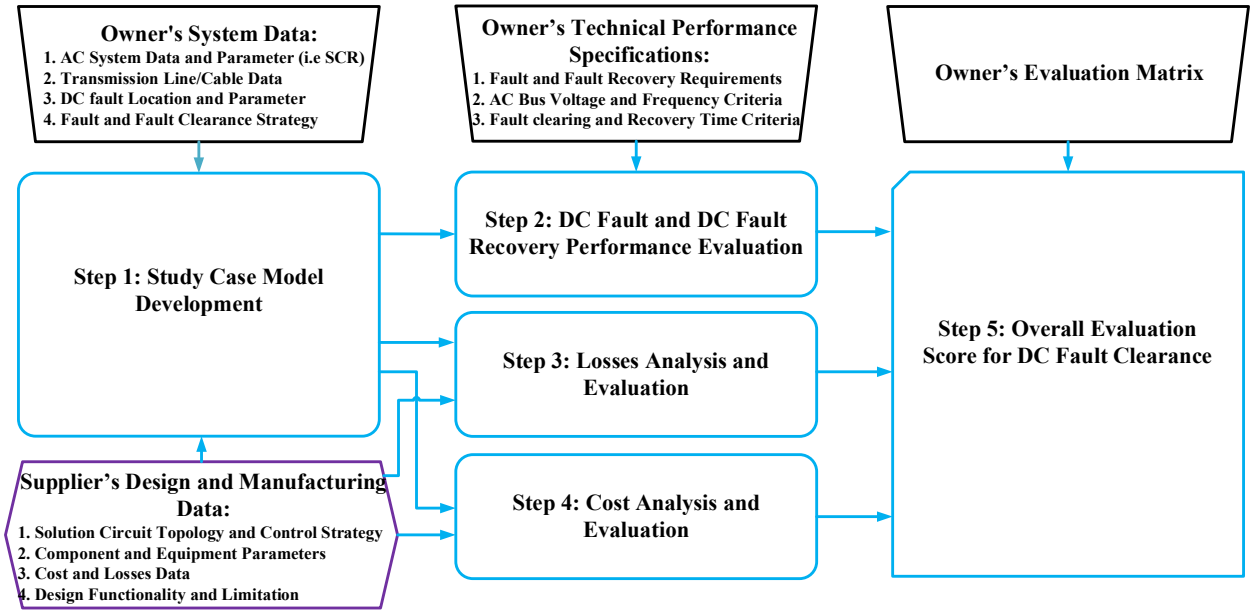



**Figure 5-1: Evaluation Methodology Flowchart for DC Fault Clearing Solutions**

*Step 1: Create study case models based on the owner's system data and the supplier's proposed dc fault clearing design and solution:* If dynamic equivalent network models are not provided, the owners' system data should include the system model or Thevenin equivalent data (SCR) for interconnected point-to-point dc systems. Additionally, it should include pre-defined fault locations and parameters, as well as a fault clearance strategy. To ensure the quality of the evaluation, it is important to gather all necessary design and manufacturing data from potential or selected suppliers. This ensures that optimal designs are achieved by fully considering the functionality and limitations of their solutions, as well as their associated costs and losses. For example, if a line reactor or fault current limiter is utilized, the peak fault current and the rate of rise of the fault current can be affected, impacting the fault interruption time, as well as overall equipment losses and cost. Sensitivity analysis is recommended in some cases to determine the optimal design parameters (such as DCCB inductance, internal commutation time, peak current

interruption capability and energy absorption capability) through a large number of time domain simulations while taking into account various system operation modes, control strategies, grid configurations, and other design constraints, as well as relevant trade-offs between parameters to be selected [79] [80].

*Step 2:DC fault and dc fault recovery performance evaluation:* It is important to conduct simulation studies and evaluate the performance of the dc fault clearing and fault recovery performance against the owner's technical performance specification and assessment criteria, including interconnected ac bus voltage and frequency requirements, fault clearing and recovery time requirements, and other functional or performance requirements. While such owners' technical performance requirements can be generalized, they are required to be set on an individual basis and are not restricted to the three items indicated in Figure 5-1.

*Step 3: Determine and evaluate the system losses:* It is to determine the losses associated with the primary equipment required for fault clearance, which should include not only conduction and switching losses associated with power electronic devices such as thyristors, IGBTs, and diodes, but also auxiliary systems such as cooling system. To simplify the cost evaluation process, losses could also be converted to dollar values and evaluated as part of the lifetime operating cost.

*Step 4: Determine and evaluate the system costs:* Costs are supplier and project dependent and should take into account the entire project life cycle costs, including capital, operating, maintenance, and decommissioning.

Steps 3 and 4 require input from potential or selected suppliers, as well as engineering analysis based on the optimized case model developed in Step 1. Depending on the stage of the project life cycle at which this evaluation or comparison is conducted, the degree of data accuracy must be

determined appropriately. For instance, to reduce time and effort in a high-level conceptual review, the common type of equipment can be removed from the cost and loss evaluation, i.e. identical converter transformers, or arm inductors are used between solutions

*Step 5: Determine the overall performance score of an evaluated dc fault clearing design or solution:* It is the final stage, which incorporates the evaluation results or scores, if a quantitative measure was used to produce performance scores in Steps 2–4 and generates the overall performance score used to selecting the dc fault clearing technology or solution. The owner's evaluation matrix serves as the foundation for deriving overall performance in the form of a letter grade or performance score. As an example, consider the evaluation output from Step 2; the evaluation of dc fault and dc fault recovery performance can result in a letter grade rating of Good, Fair, Poor, or Unsatisfactory, or in a numeric value established in the evaluation matrix.

Using the evaluation methodology proposed, the following sections summarizes a case study and their evaluation results between a base case using half-bridge and ac circuit breaker, a solution using full-bridge MMC, and a solution using half-bridge MMC together with dc circuit breakers on their dc fault clearing capabilities.

To evaluate the case study, Manitoba Hydro's technical performance specification for dc fault and fault recovery [81] is used as a baseline and adjusted to serve as the assessing criteria, as detailed in Table 5-1. The evaluation performance criteria are established as pass/fail, with failure to achieve them resulting in an unsatisfactory rating.

**Table 5-1: DC Fault and DC Fault Recovery Performance Evaluation Criteria**

| Performance Criteria | Unsatisfactory |
|---|---|
| AC System Frequency | ≤ 0.98 pu for > 65 ms |
| AC System Bus Voltage | ≤ 0.9 pu for > 150 ms |
| DC Fault Recovery Time * (with Fault De-Ionization Time Between 100 ms to 500 ms) | ≥ 800 ms |

* DC system recovery, upon reaching 90% of the pre-fault dc power transfer level.

## 5.2. Description of the System Models

The case study models are based on a symmetrical monopole point-to-point cable VSC-HVDC model created by Cigré Working Group B4.56. To accommodate the expectations of the dc faults clearance study, modifications are made that include the following:

1) replacing cable with overhead transmission line;

2) modeling ABB's proactive hybrid dc breaker with associated control and fault detection logic;

3) developing three HVDC point-to-point transmission models: one with full-bridge MMC valves and two with half-bridge MMC valves;

4) adjusting firing pulse generation and associated control for full-bridge valve control;

5) implementing dc fault insertion and de-ionization delay logic; and

6) modifying and developing simple fault detection time delay and converter blocking logic.

To the fact that the primary scope of the investigation is on the dc fault clearance, the AC systems' short-circuit ratio (SCR) were selected at 4 and 4.7 according to the base model SCR settings, and

settings of inner and outer HVDC control were unmodified, thus the suggested settings from [13] were selected. Table 5-2 summarizes the common system parameters and component data for all the study cases.

**Table 5-2: Study Base Model Common System Data Summary**

| **AC System Thevenin Equivalent Strength** | |
|---|---|
| Short-Circuit Ratio (SCR) on 800 MW base (A1) | 4 |
| Short-Circuit Ratio (SCR) on 800 MW base (C1) | 4.7 |
| **AC System (A1)** | |
| AC System Voltage (L-L, RMS) | 380 kV |
| Transformer Capacity | 800 MVA |
| Transformer Ratio | 380 kV/220 kV |
| Transformer leakage inductance | 35 mH |
| Frequency | 50 Hz |
| **AC System (C1)** | |
| AC System Voltage (L-L, RMS) | 145 kV |
| Transformer Capacity | 800 MVA |
| Transformer Ratio | 145 kV/220 kV |
| Transformer leakage inductance | 35 mH |
| Frequency | 50 Hz |
| **DC Overhead Line** | |
| DC Bus Voltage | ±200 kV |
| Length of DC Line A1C1 | 200 km |
| DC Line Conductor data reference | 2156MCM ACSR |
| DC Line Conductor Resistance @ 20°C | 0.0266 Ω/km |
| **AC-DC Converter Data (A1)** | |
| Power Rating | 800 MVA |
| Numbers of Sub-Modules per arm | 200 |
| Sub-Modules Capacitance | 10 mF |
| Sub-Modules Conduction Resistance (Ron) | 1.361 mΩ |
| **AC-DC Converter Data (C1)** | |
| Power Rating | 800 MVA |
| Number of Sub-Modules per arm | 200 |
| Sub-Modules Capacitance | 10 mF |
| Sub-Modules Conduction Resistance ($R_{on}$) | 1.361 mΩ |

Figure 5-2 shows the three models structured for the dc faults analysis. In all models, converter Cm-A1 controls the dc-side voltage, and Cm-C1 regulates the dc power transmitted from C1 to A1 through a double conductor dc overhead lines of 200 km. In the first base case, hall-bridge MMC is used with ac circuit breaker for fault clearance, in the second study case full-bridge MMC is used, and in the third study case the valve is constructed with half-bridge MMC with additional four dc breakers installed on both the positive and negative poles for each converter station.

The number of submodules for MMC was determined by the dc voltage level and was selected to be 400 for a bridge phase arm. The associated conduction resistance for IGBT and diode pair $R_{ON}$ can be calculated based on the conduction loss equation in [13]:

$$P_{cond} = 3N_{SM}R_{ON}\left[\left(\frac{I_{dc}}{3}\right)^2 + \left(\frac{I_{ACRMS}}{2}\right)^2\right] \quad (5.1)$$

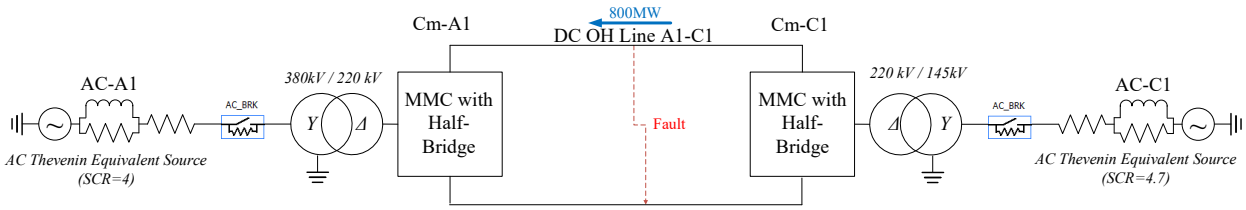
$P_{cond}$ : conduction losses of a converter (set as 0.3% of dc power rating)

$N_{SM}$ : number of submodules per phase arm

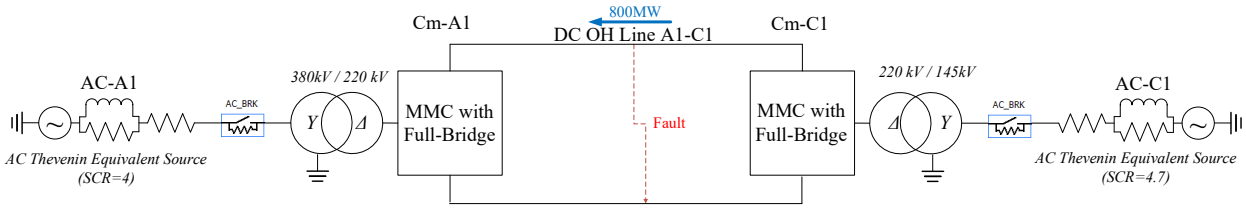
$R_{ON}$ **:** equivalent conduction resistance of a submodule

$I_{dc}$ : rated dc currents and

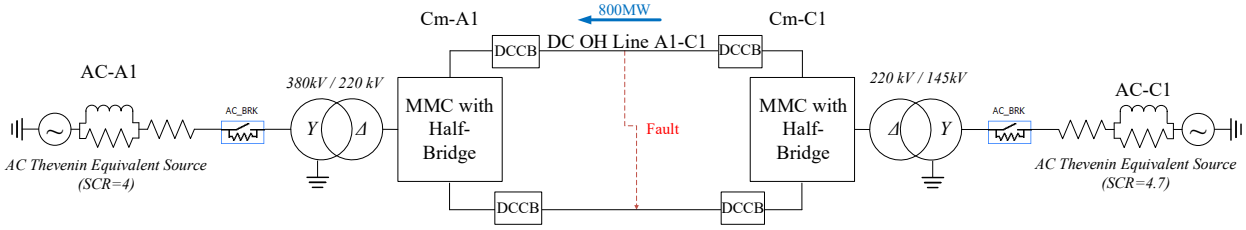
$I_{ACRMS}$ **:** ac RMS currents




(a) With Half-Bridge MMC and AC Circuit Breaker for DC Fault Clearance




(b) With Full-Bridge MMC




(c) With Half-Bridge MMC and DC Circuit Breakers

**Figure 5-2: Point-to-Point Monopolar HVDC with Different DC Faults Clearance Techniques: (a) With Half-Bridge MMC and AC Circuit Breaker for DC Fault Clearance; (b) With Full-Bridge MMC; (c) With Half-Bridge MMC and DC Circuit Breakers**

The submodule capacitor rating was selected and calculated using (5.2) from [9] [13]. $E_{MMC}$ is the energy per MVA stored in each submodule, $S$ is the nominal base (800MVA), $\upsilon_C$ is the capacitor

voltage rated value of 2 kV. In the case model created by model created by Cigré Working Group B4.56, $E_{MMC}$=30 kJ/MVA was used as the default value to minimize the submodule voltage ripple within a range of ±10% [13]; The calculated submodule capacitance (*C*) is 10 mF. The default arm inductor values were used from the base model at 0.15pu. (29mH).

$$C = \frac{2SE_{MMC}}{6N_{SM}\upsilon_C{}^2} \tag{5.2}$$

## 5.3. DC Breaker Model Description

The third model included four dc breakers, one for each converter pole. The ABB proactive hybrid dc circuit breaker was chosen for this case study because it was one of the earliest prototypes of its kind and also represented the latest DCCB development. The commutation breaker is the primary means of interruption that must sustain the highest pole-to-ground voltage. To be consistent with the converter valve design, a single IGBT module was rated at 1 kV, implying a requirement for 200 IGBT modules. Due to the breaker's bidirectional functionality, an additional set of 200 IGBT modules is connected in anti-series pair. In this study, it was assumed the IGBT module will have the peak current breaking capacity not exceeding 3 kA; therefore, to fulfill the short-circuit interruption capability the parallel connection of IGBT modules will be required. With the default PSCAD I-V characteristic, the energy absorption surge arrester voltage is set at 1.5 times the rated dc pole voltage at 300 kV, based on the recommendation in [16] [43], to create the required counter voltage dissipating the fault current. Key components' ratings are summarized in the Table 5-3.

**Table 5-3: DC Breaker Model Data Summary**

| DC Breaker | |
|---|---|
| Number of IGBT Module in Commutation Breaker | 800 |
| Number of IGBT Module in Commutation Switch | 6 |
| Sub-Module Conduction Resistance | 1.361 mΩ |
| Current Limiting Reactor | 0.1 H |
| Mechanical Branch Disconnector Close Resistance | 0.005 Ω |
| Energy Absorption Surge Arrester Voltage Rating | 300 kV |

## 5.4. DC Fault Clearance Strategy

To compare the dc fault clearing performance of base case model and solutions using full-bridge MMC and half-bridge MMC with dc breakers effectively, it is necessary to design and run the models in such a way that the internal current commutation time and break time can be easily compared. This means that because the relay time, including detection and selection time, is not the primary focus of this investigation, the models' dc fault detection logic that is based on valve current or dc voltage drop were disabled for better result comparison; as a result, a fixed 2 ms relay time delay was used between fault inception and trip command. The dc fault clearance strategy used for the base case model is present in Figure 5-3. The dc fault clearance strategy for both solutions is depicted in Figure 5-4.

In the base case model, where an ac circuit breaker is utilized to clear dc faults, the following dc fault and restart process according to Manitoba Hydro's study technical reference is used [21] and explained below:

Step 1: The dc line to line short circuit occurs at $t_0$=1.02 s, after both converters have been fully deblocked and transmit 800 MW dc power at a current of 2 kA dc.

Step 2: After the fault is detected at $t_1$=1.022 s, a valve group blocking command is issued, which blocks the IGBTs in the MMC half-bridge submodule.

Step 3: At $t_2$, fault clearing starts using ac breakers opening within 6 cycles (120 ms) after the fault is detected and valve group blocking of the MMC,

Step 4: At $t_3$, a fault deionization timer is started once the dc fault current is reduced to the 1 A, where residual breaker can open,

Step 5: Following a 200 ms fault deionization time, system recovery begins at $t_4$ with both stations energizing the converter transformers and re-deblocking their converters.

Step 6: At $t_5$, dc power is restored to 90% of its pre-fault level.

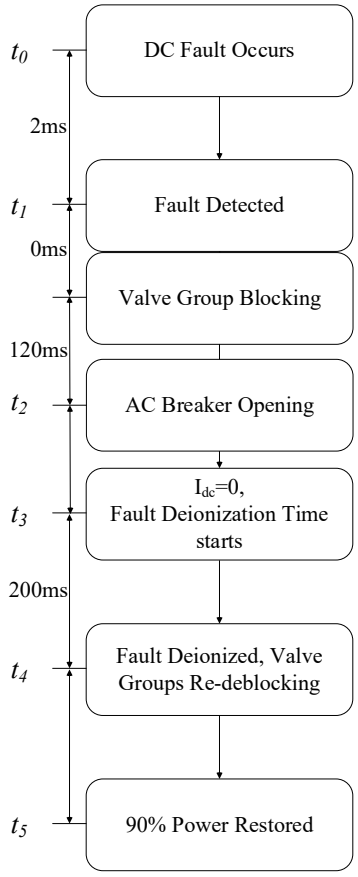



**Figure 5-3: DC Faults Clearance Strategy Flowchart for Base Case Model**

The dc fault clearance strategy based on full-bridge MMC is as follows:

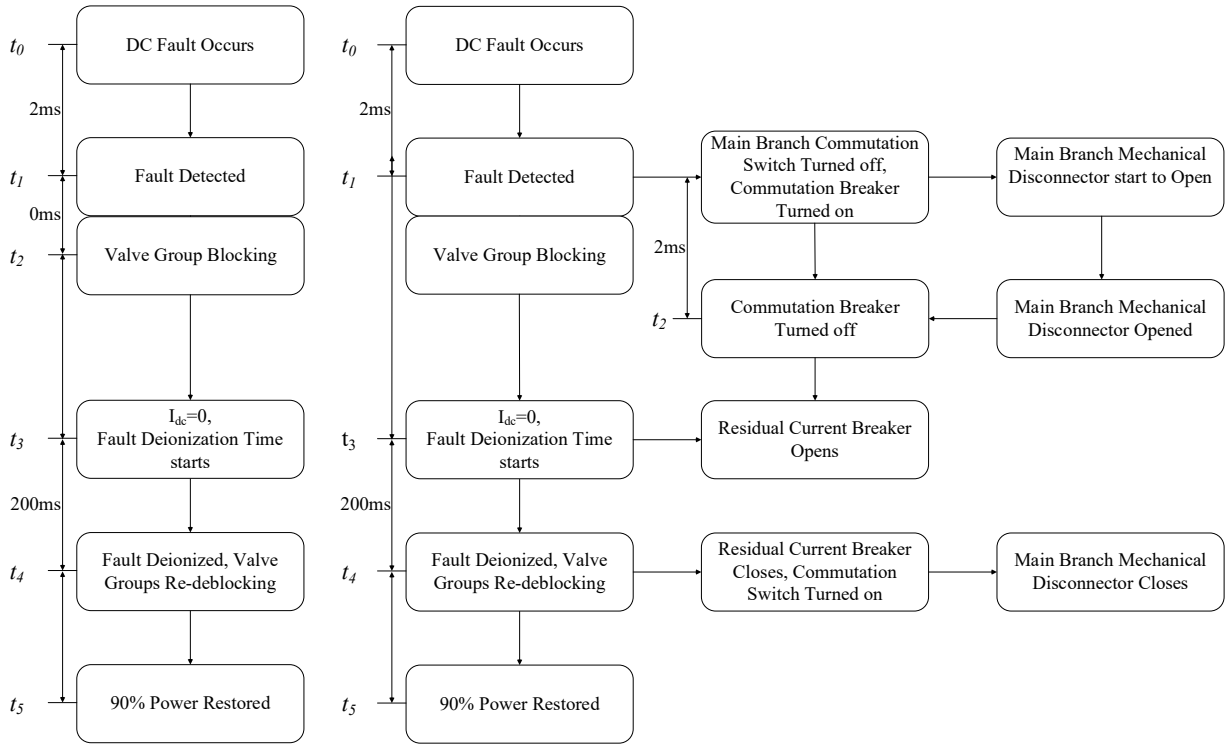
Step 1: The dc line to line short circuit occurs at $t_0$=1.02 s, after both converters have been fully deblocked and transmit 800 MW dc power at a current of 2 kA dc.

Step 2: After the fault is detected at $t_1$=1.022 s, a valve group blocking command is issued, which blocks the IGBTs in the MMC full-bridge submodule.

Step 3: At $t_3$, a fault deionization timer is started once the dc fault current is reduced to the leakage current level of 1 A.

Step 4: Following a 200 ms fault deionization time, system recovery begins at $t_4$ with both stations re-deblocking their converters.

Step 5: At $t_5$, dc power is restored to 90% of its pre-fault level.




(a) For Full-Bridge Solution (b) For Half-Bridge with DC Breakers Solution

**Figure 5-4: DC Faults Clearance Strategy Flowcharts (a) For Full-Bridge Solution (b)For Half-Bridge with DC Breakers Solution**

The following is the dc fault clearance strategy for the solution with half-bridge MMC and dc breakers:

Step 1: At $t_0$=1.02 s, the dc line to line short circuit occurs after both converters have been fully deblocked and transmit 800 MW dc power at a current of 2 kA dc.

Step 2: Take immediate action following the detection of the fault at $t_1$=1.022 s; a valve group blocking command is issued, along with an interruption command issued to the dc breaker. The dc breaker's power electronic commutation breaker is turned on while the main branch commutation switch is turned off, in order to commutate the dc fault current from the main branch to the commutation branch. Once the fault current is commutated to the commutation branch, the main branch mechanical disconnector begins to open, and after 2 ms the required electrical withstand is reached, mechanical disconnector is opened and the main commutation breaker is turned off, commutating the fault current into the energy absorption branch.

Step 3: At $t_3$, a fault deionization timer is begun once the dc fault current has been decreased to the leakage current threshold of 1 A, at which point the dc breaker's residual current breaker is opened to complete the dc fault isolation.

Step 4: Following a 200 ms fault deionization time, system recovery begins at $t_4$ with both stations re-deblocking the converter and restoring the dc breaker with residual current breaker closed, main branch mechanical disconnector closed, commutation switch turned on and commutation breaker remaining open.

Step 5: At $t_5$, dc power is restored to 90% of its pre-fault condition.

## 5.5. Simulation Case Study Results and Evaluation

### 5.5.1. Half-Bridge Base Case Model

In the base case model, after a dc line fault occurred at $t$ = 1.02 s in the middle of dc line A1-C1 with a fault resistance of 0.01 Ω, the converters were blocked and after a 6-cycle delay, the ac circuit breakers at both stations were tripped. Figure 5-5 illustrates the converter's dynamic response in terms of dc voltage, current, and power.

At converter CmC1, the peak dc fault current reached up to 7.1 kA (3.55 pu) when measured at the positive pole on the dc line. After a six-cycle delay, the ac circuit breakers were tripped at $t$ = 1.142 s, and the fault current was suppressed to below the leakage current level 289 ms after the fault was initiated.

On the ac side of the converter CM-C1, when a fault is applied, the ac current increases to feed the fault, lowering the ac terminal voltage to 0.60 pu. At the converter CM-A1, the ac terminal voltage was lowered to 0.56 pu. For 135 ms, the ac bus voltage was less than 0.9 pu. As illustrated in Figure 5-7, the total time required to restore the 90% pre-fault power following a dc failure is 642 ms, which includes 200 ms for fault deionization. If the fault de-ionization time is set to 500 ms, the overall recovery time will be 942 ms, exceeding the fault recovery time performance criteria.

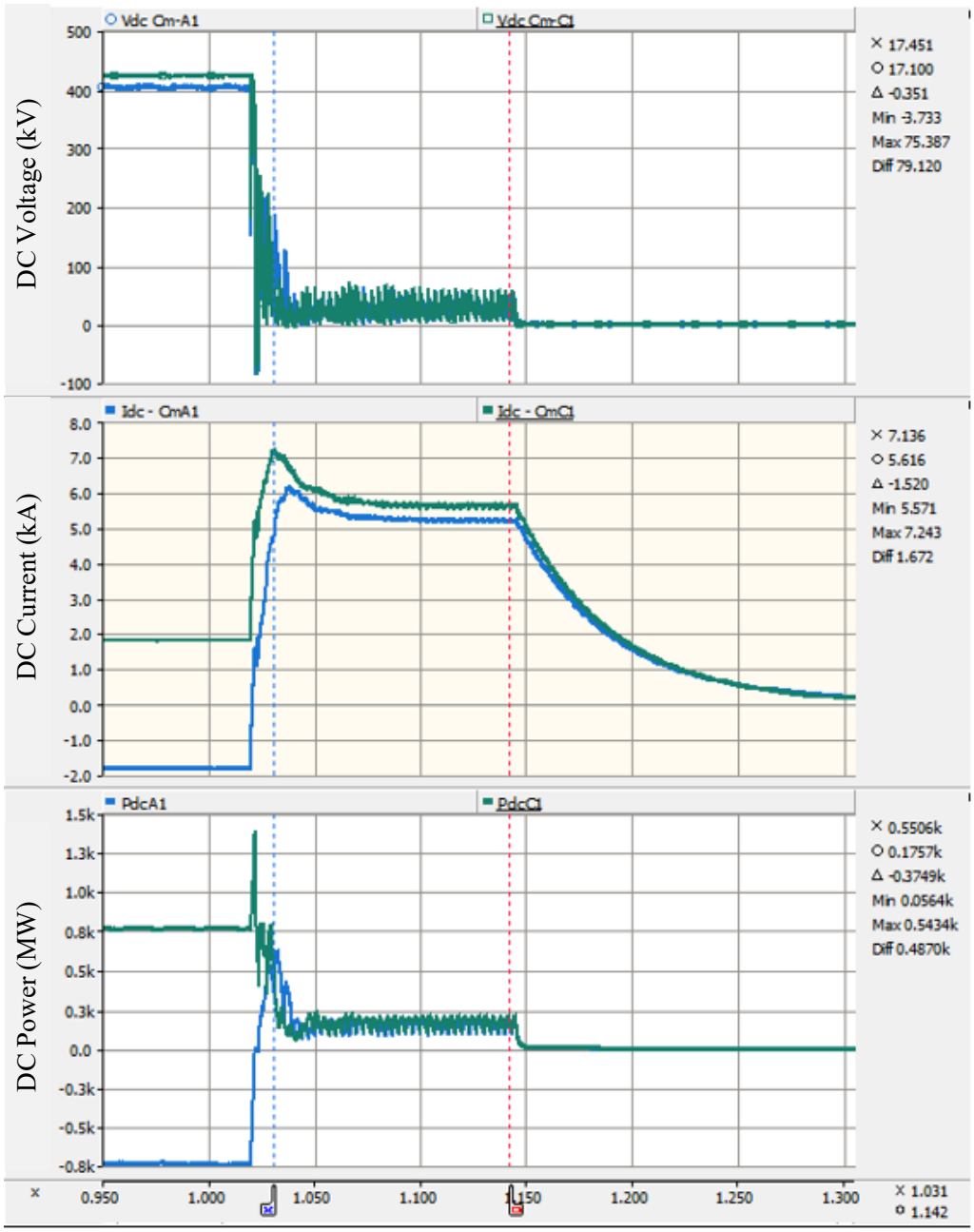



**Figure 5-5: Dynamic DC System Response of the Base Case Model**

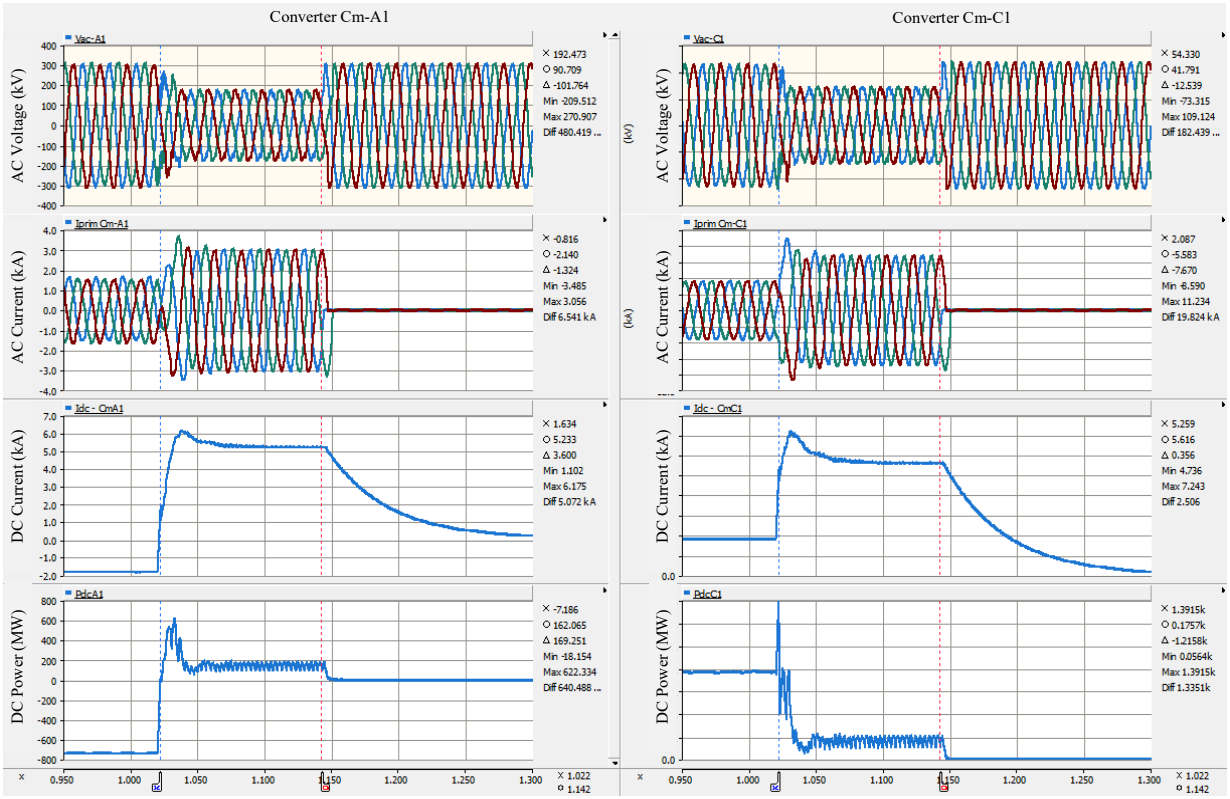



**Figure 5-6: Dynamic ac System Response of Base Case Model**

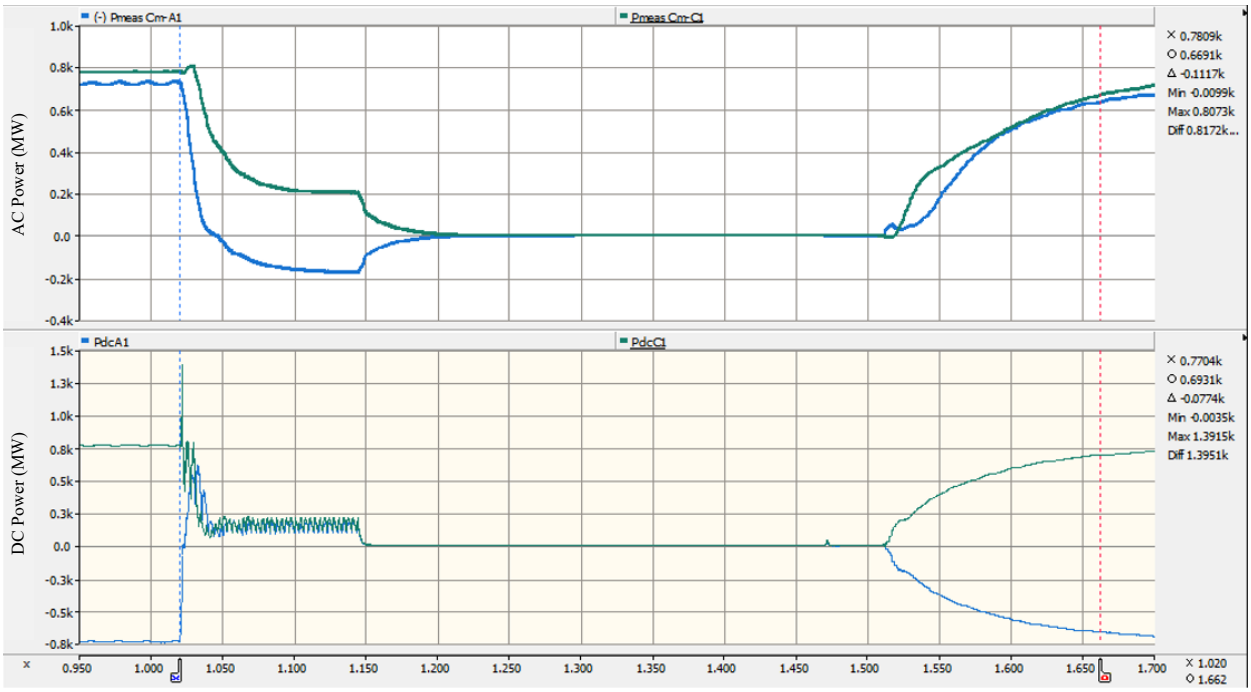



**Figure 5-7: System Recovering after DC Fault for Base Case Model**

### 5.5.2. Solution with Full-Bridge MMC

A pole-to-pole fault is applied at $t$ = 1.02 s at the middle of the dc line A1-C1 with a fault resistance of 0.01 Ω. In the full-bridge MMC solution, the converters were blocked for fault clearing. The dynamic response of the converter dc voltage, current and power are observed in Figure 5-8.

The peak dc fault current reached up to 5.3 kA (2.65 pu) at converter CmC1, measured at positive pole on the dc line. MMC valve was blocked at $t$ = 1.022 s, following which the fault current was suppressed to below leakage current level within 2.7 ms. With the low impedance fault crossing the poles the dc voltage measured across the converter did not collapse until the MMC was blocked and the dc voltage then displayed some oscillations, which are attributed to the ac network and RLC characteristics of the selected dc lines. The calculated rate of rise of the fault current is 1.73 kA/ms.

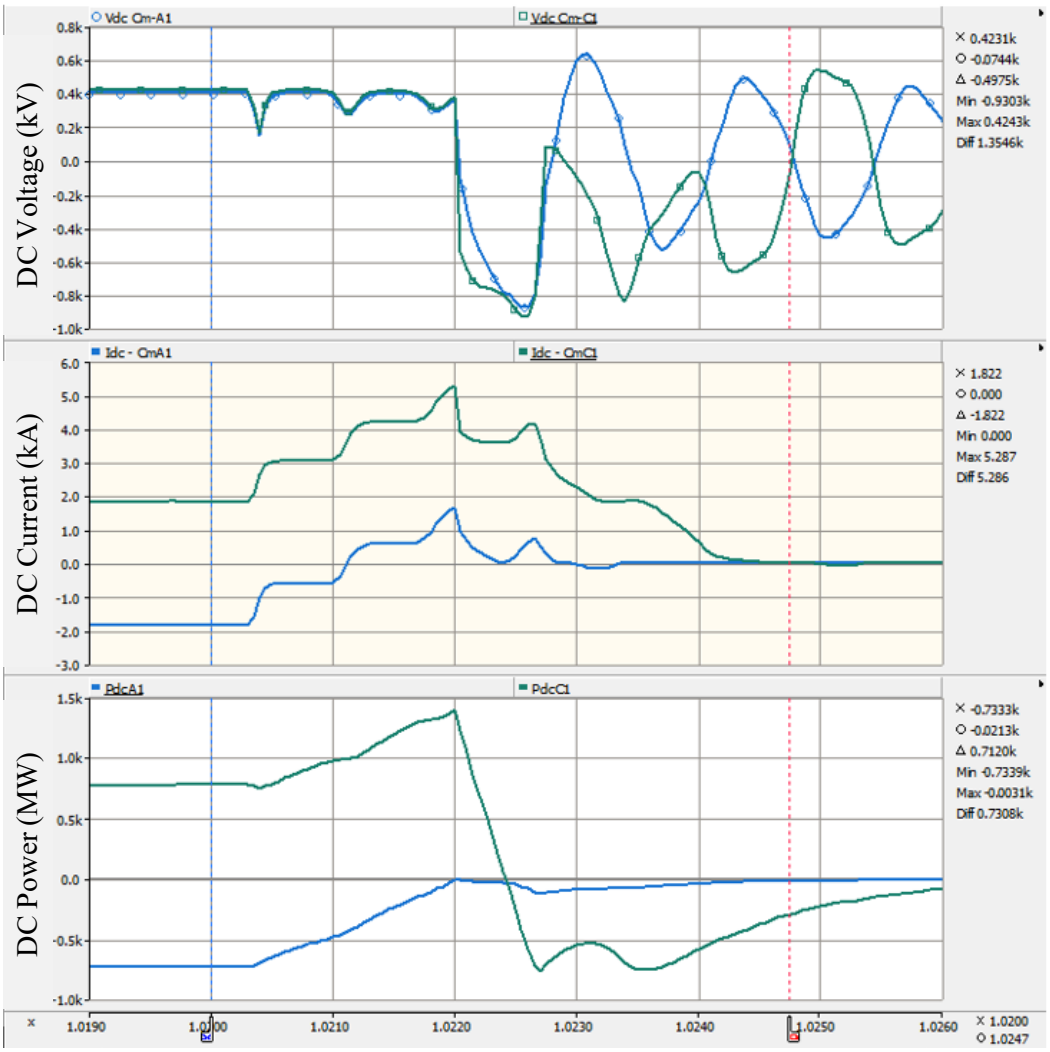



**Figure 5-8: Dynamic DC System Response of the Full-Bridge MMC Solution**

On the ac side at converter CM-C1, after the fault is applied, the ac current begins to increase to feed the fault, resulting in a decrease in the ac terminal voltage. After the MMC valve is blocked, the dc fault is seen on the ac terminal as a phase to phase fault until the current is completely suppressed to zero.

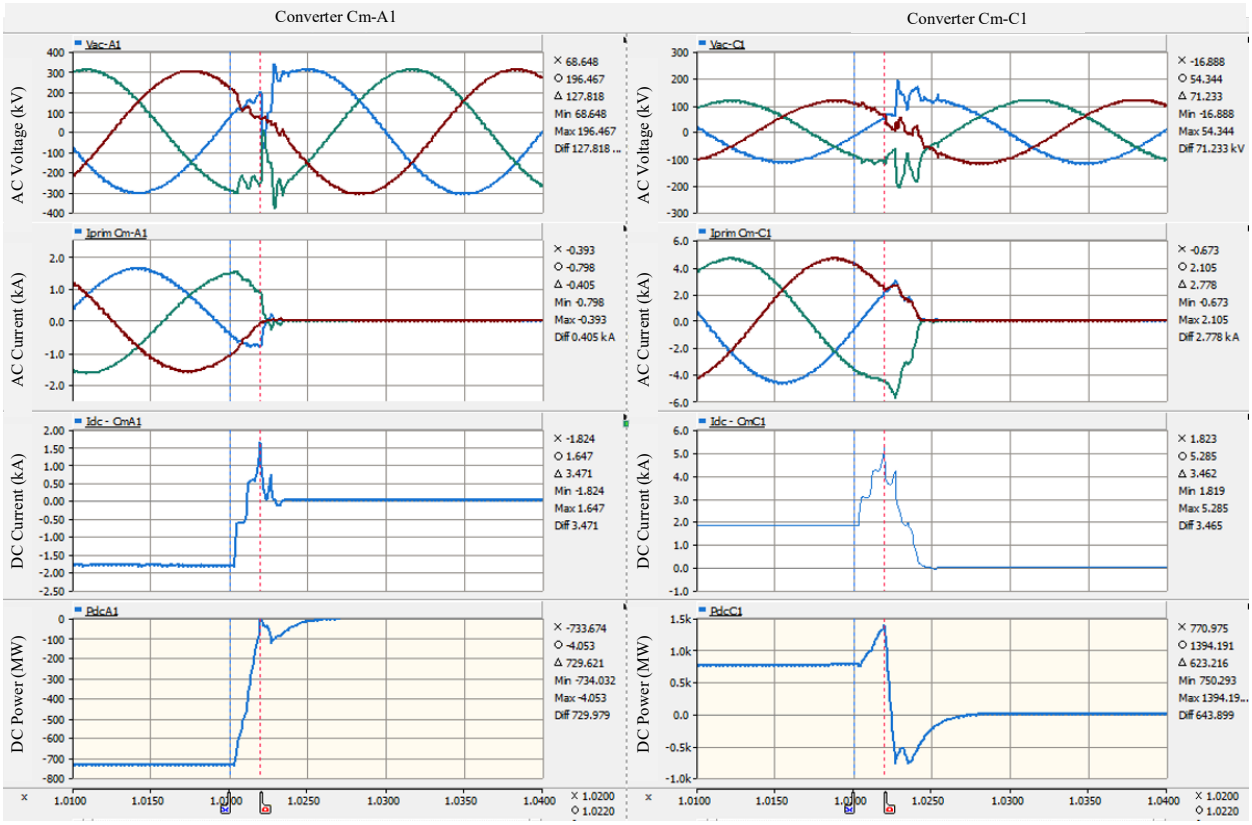



**Figure 5-9: Dynamic ac System Response of the Full-Bridge MMC Solution**

At the receiving end, converter Cm-A1, as the dc current reversed its direction, the alternating current decreased at first and then increased as the dc fault current increased. The same as with the sending end converter, after the valve group was blocked, it manifested as a phase-to-phase fault, which persisted until the fault current was suppressed from the ac side of the converter.

As shown in the Figure 5-10, the total measure restore time after dc fault is 402 ms, which includes 200 ms for fault deionization.

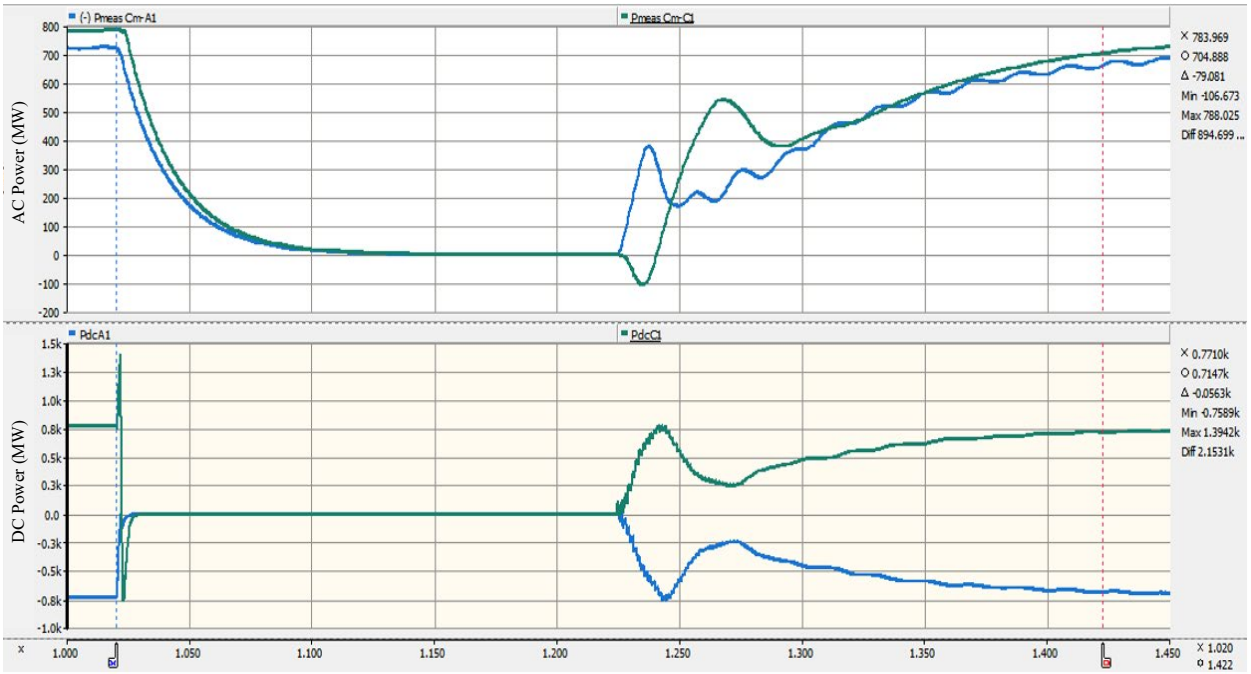



**Figure 5-10: System Recovering after DC Fault for Full-Bridge MMC Solution**

### 5.5.3. Solution with Half-bridge MMC and DC Breakers

In contrast, the half-bridge MMC solution with dc breakers, the peak dc fault current reached up to 5.45 kA (2.72 pu) at converter Cm-C1, measured at positive pole on the dc line. In this solution, the dc breaker was tripped at $t$ = 1.022 s, following which the fault current was suppressed to below leakage current level within 3.7 ms. The calculated rate of rise of the fault current is 1.57 kA/ms. The dc voltage drops first and quickly recovered as dc breaker commutates the fault current to the energy absorption branch at $t$ = 1.024 s. Figure 5-11 shows the dynamic response for dc voltage, current and power.

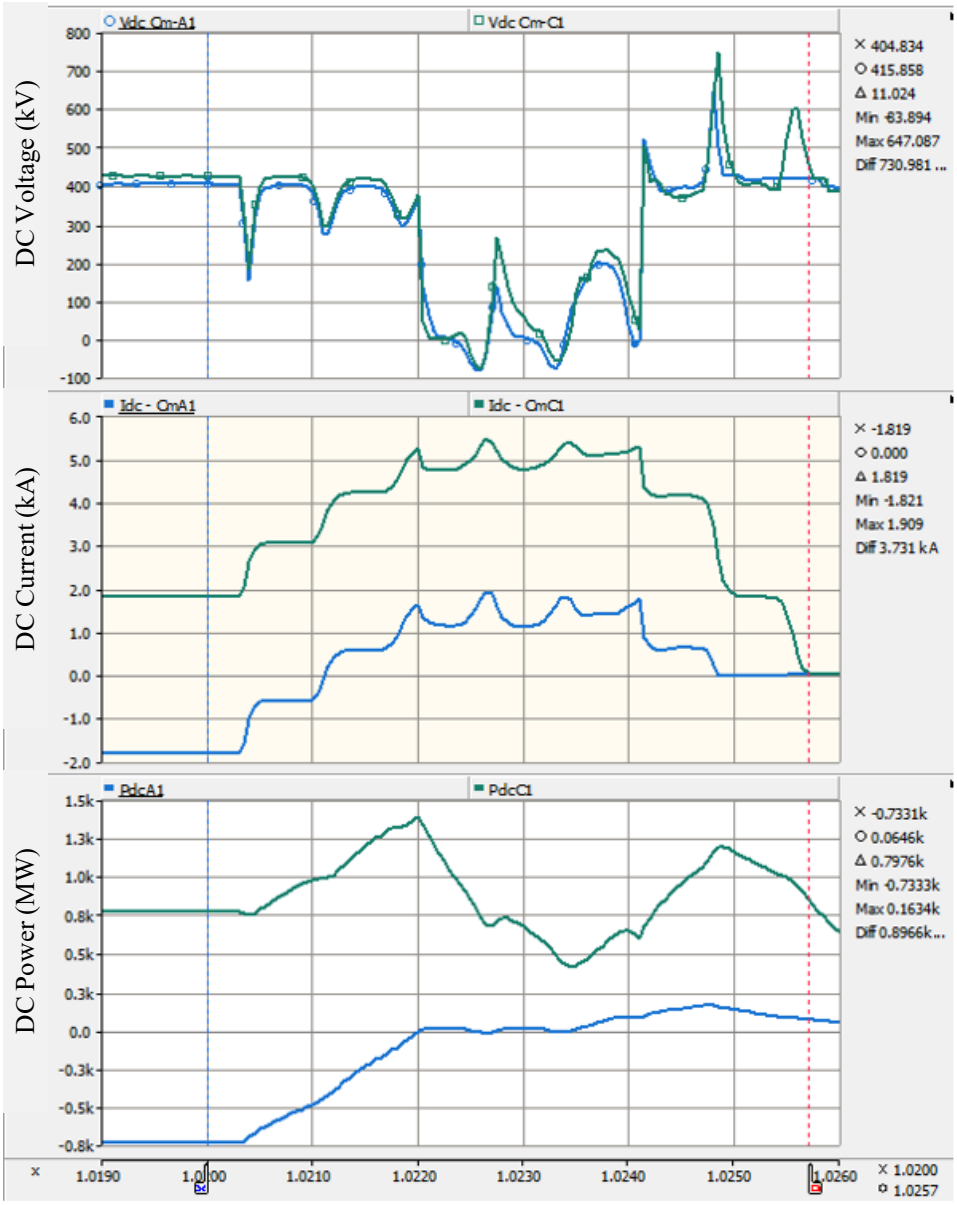



**Figure 5-11: Dynamic DC System Response of the Half-Bridge MMC with DC Breaker**

Since blocking the half-bridge MMC will not interrupt the fault current feeding from the ac system to the fault due to the freewheeling diode rectification the ac terminal voltage reduced as a result of the large fault current drawn from the ac network to the dc fault. At converter CM-C1, the ac side overcurrent as high as 1.8 pu.

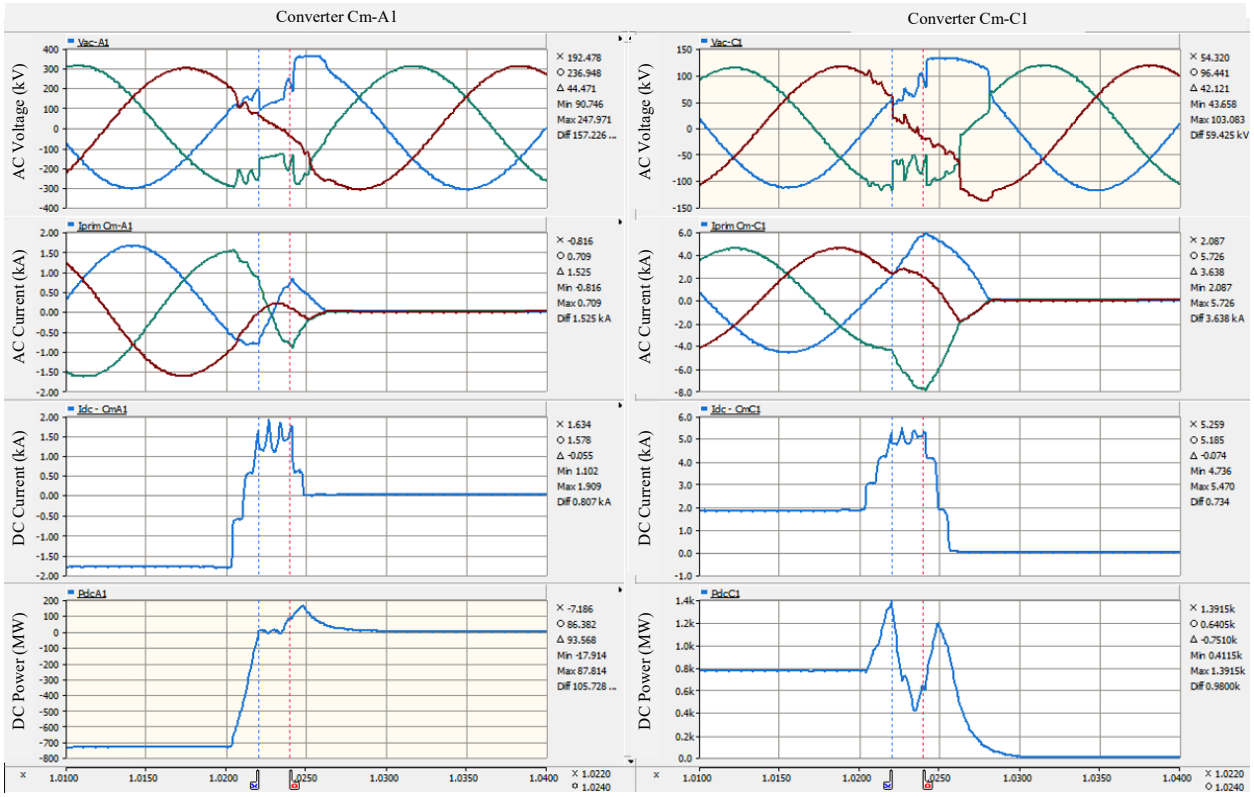



**Figure 5-12: Dynamic ac System Response of the Half-Bridge MMC with DC Breaker Solution**

In the dc breaker shown in Figure 5-13, the current flowing through the main branch increases rapidly once the trip command is received, as can be seen in the graph. At $t$= 1.022 s, when the fault is detected, and the commutation switch is turned off, causing the fault current to be commutated to the commutation branch after a delay of 250 µs. Approximately 2 ms after, the main commutation breaker is turned off with the mechanical disconnector opened, and the energy is dissipated through the surge arrester within the next 1.7 ms. The dc fault was isolated in 3.7 ms after the fault was detected, with a peak current of 5.45 kA flowing through the dc breaker at that time.

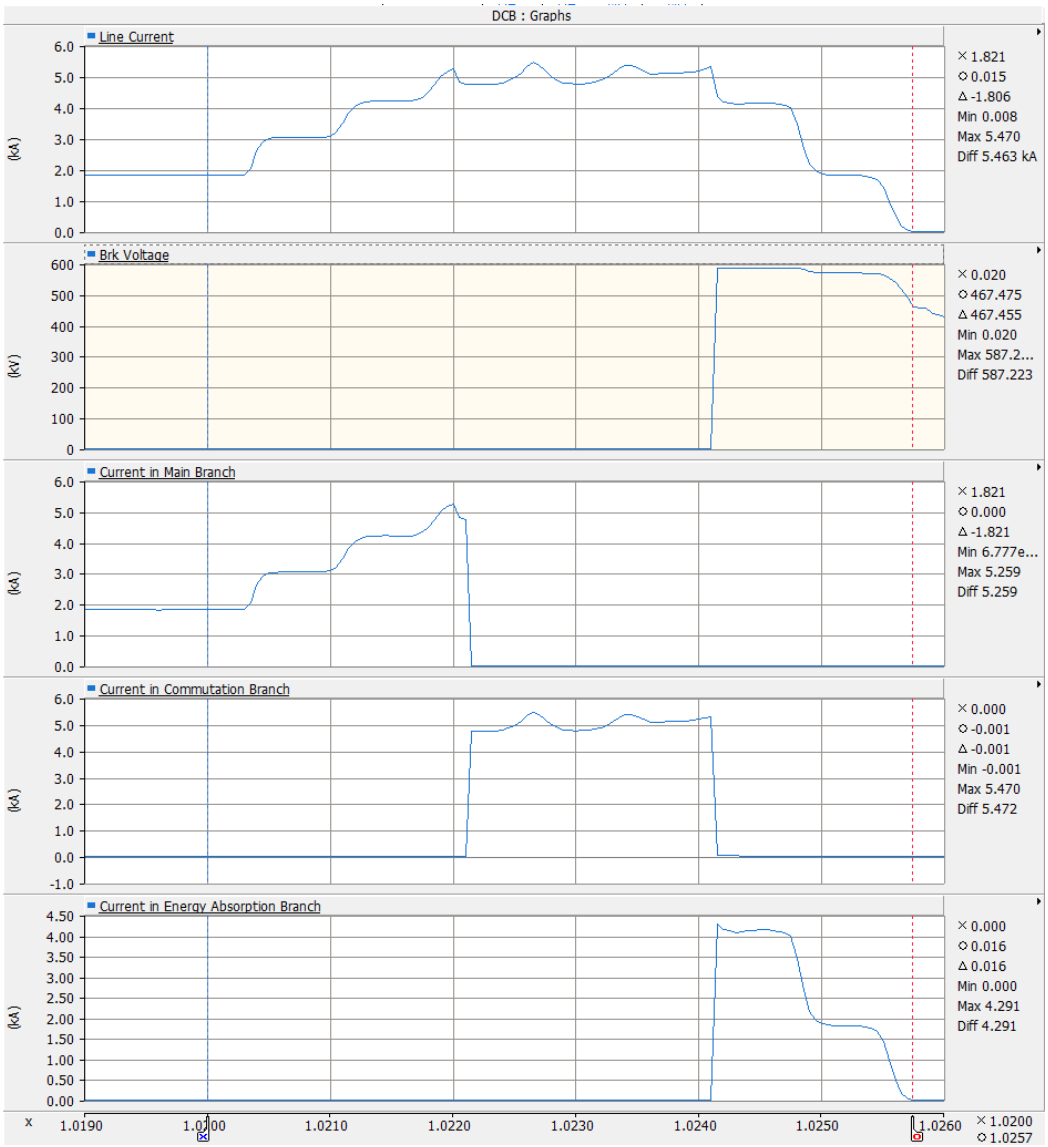



**Figure 5-13: DC Breaker Current and Voltage Waveforms**

As illustrated in the Figure 5-14, the overall measured restore time after a dc fault is 387 ms, which includes 200 ms for the fault deionization.

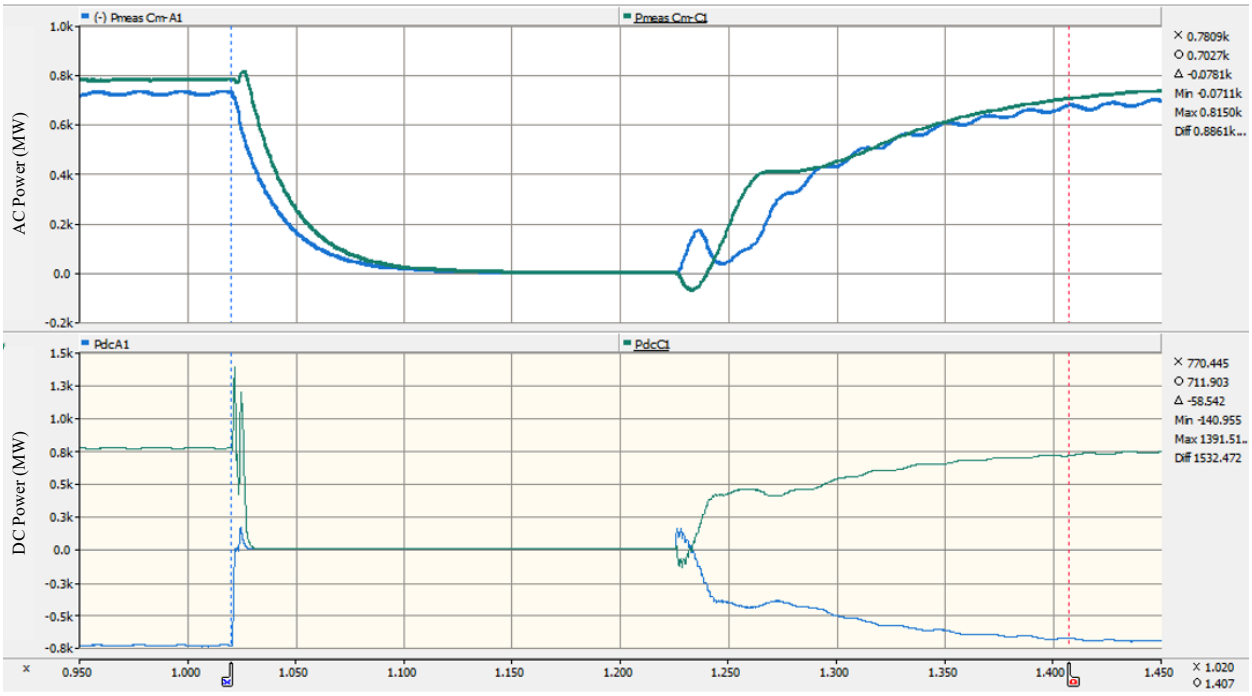



**Figure 5-14: System Recovering after DC Fault for Half-Bridge MMC with DC Breaker Solution**

The sensitivity of the ac network short circuit level to the dc breaker design was investigated by incrementally increasing the CM-C1 interconnected ac SCR from 4.7 to 47. As illustrated in Figure 5-15, the peak dc fault current increased from 5.45 kA with SCR = 4.7 to 5.744 kA with SCR = 47, while the interruption time increased from 5.7 ms to 6.2 ms. The SCR level changes proportionally to the peak current level and break time; however, the effect is insignificant.

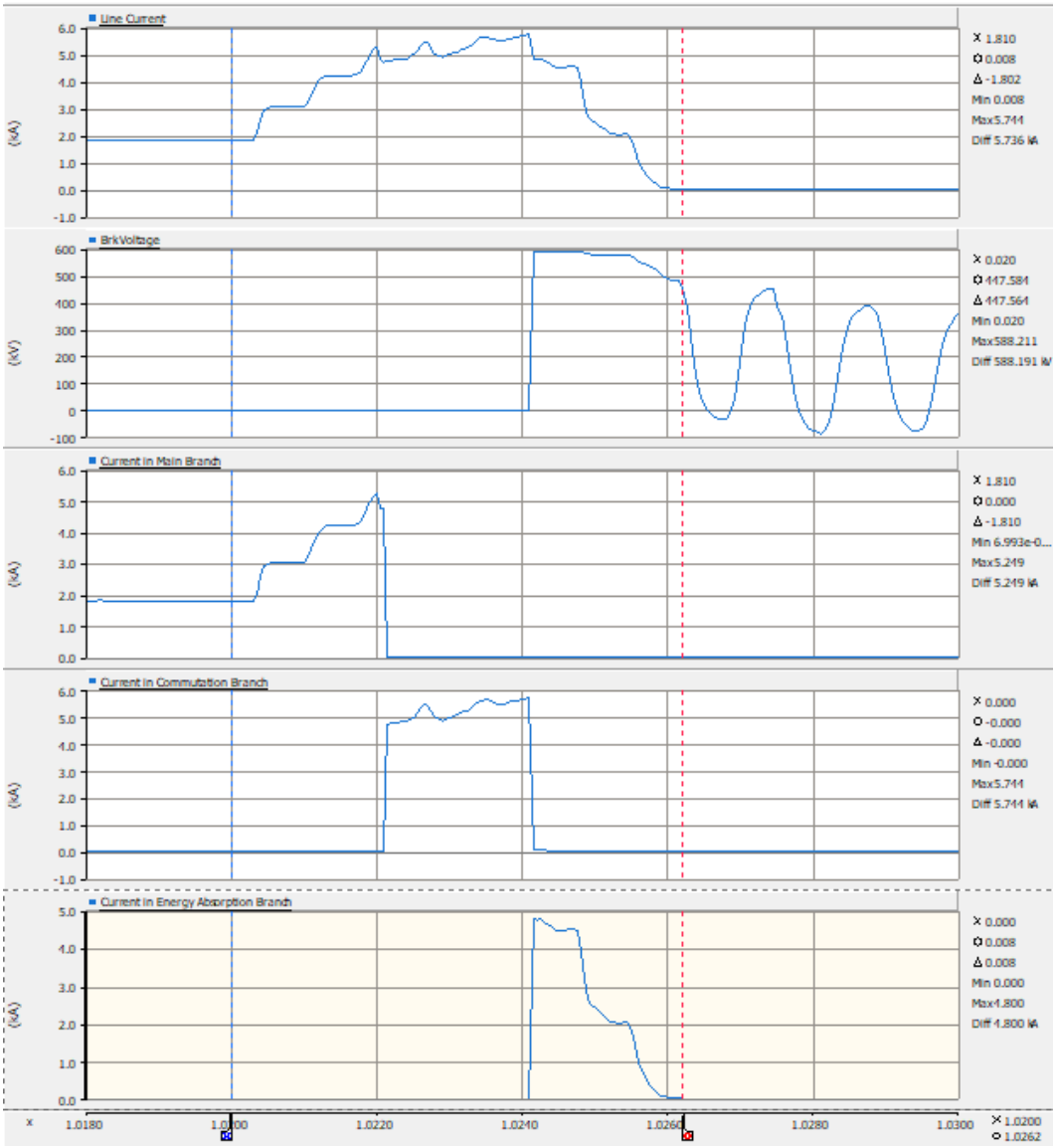



**Figure 5-15: DC Breaker Current and Voltage Waveforms (Cm-C1 SCR set to 47)**

### 5.5.4. DC Fault and DC Fault Recovery Performance Evaluation

According to the results of the simulation studies, the full-bridge MMC solution with the predetermined system and component parameters has a better fault clearance performance with respect of break time, peak fault current level, and impact on the interconnected ac systems based on the performance evaluation criteria listed in Table 5-1. With the full-bridge MMC, the fault

current from the ac system can be reduced immediately by the use of fast dc controls. Whereas half-bridge MMC and dc breakers do not give the same system performance as full-bridge MMC, they also provide a superior and comparable fault clearance capability and fault clearing time to ensure adequate power system stability of interconnected ac systems. Based on the case study, for the solution utilizing a half-bridge MMC with dc breakers the system restoration time was less than with a full-bridge solution, as shown in the summary table below. However, reference [30] has indicated that with a properly designed control algorithms, full-bridge submodules can remain deblocked and provide STATCOM ac voltage control through the dc fault event to further support the connected ac system during loss of infeed and achieve faster fault recovery since submodule capacitor can remain balanced for immediately power restoration. This detail control for dc fault handling and restoration was not implemented in this case study.

**Table 5-4: Case Study Performance Comparisons Table**

| Solution Type | Peak Fault Current (kA) | Break Time (ms) | DC Fault Recovery Time to 90% of Pre-Fault Power (ms) | DC Fault and Fault Recovery Performance Rating |
|---|---|---|---|---|
| Half-Bridge Base Case Model | 7.13 | 287 | 642 | Unsatisfactory |
| Full-Bridge MMC | 5.3 | 2.7 | 402 | Satisfactory |
| Half-Bridge MMC with DC BRK | 5.45 | 3.7 | 387 | Satisfactory |

The overall dc fault and fault recovery performance of the base case model with half-bridge MMC and ac breaker is assessed as "Unsatisfactory" due to the fact that the maximum dc fault recovery time is exceeded when the fault de-ionization time is set to 500 ms. Both alternative solutions satisfied performance standards and were deemed "Satisfactory."

### 5.5.5. Analysis of Losses and Evaluation

The converter losses data in the base study model developed by Cigré working group B4. 57 were estimated based on real project and distributed as follows [13]:

- Switching losses estimation is difficult especially for high accuracy calculation as it will also depending on the control and switching scheme [12]. Based on the model development technical brochure [13], switching losses were negated in this study case model due to their smaller magnitude in comparison to conduction losses.
- Total conduction losses were estimated to be 1% of dc transferring power and divided to:
    - 0.3% for valves and arm reactor conduction losses
    - 0.1% for cooling and auxiliary system losses and
    - 0.6% for losses with converter transformer.

In the monopole converter study cases, the primary equipment is identical, such as converter transformer, transmission line model, line and arm reactors, and the total number of IGBTs for full-bridge and half-bridge MMC submodules calculation can be summarized in Table 5-5.

**Table 5-5: Requiring IGBTs Count with Different MMC Submodule Topologies**

| ±200 kV Monopolar HVDC Converter | | |
|---|---|---|
| **MMC Configuration** | **Full Bridge MMC** | **Half-Bridge MMC** |
| Number of SMs Per Arm | 400 | 400 |
| Number of IGBTs per SM | 4 | 2 |
| Number of IGBTs per Arm | 1600 | 800 |
| Number of IGBTs per Station | 4800 | 2400 |

When using dc breakers in the solution, it was decided to include one dc breaker per line for each station, which resulted in two (# of line multiplier index) dc breakers per station in the final design. To determine the number of IGBTs required for each breaker, it was necessary to consider two components: the commutation switch within the main branch, which required a few modules to commutate fault current to the commutation branch, and the commutation breaker within the commutation branch, which was specified by the pole to ground voltage level. When utilizing a bidirectional multiplier index, it was determined that the monopolar point-to-point example supports bidirectional power transmission; as a result, the breaker was regarded to be able to break and clear dc faults on both direction of the dc current. The peak current breaking capacity of the IGBT was taken into consideration when determining the parallel index. If the HiPak 5SNA 1500E330305 IGBT module from ABB [82] is used for this application, with an $I_{peak}$ rating of 3 kA and a necessary peak short circuit breaking capability of 6 kA, a paralleled connected commutation breaker will be required to successfully meet the breaking requirement. It is determined and summarized in Table 5-6 with consideration of IGBTs with 3 kA $I_{peak}$ rating, as well as the quantity of IGBTs used.

**Table 5-6: Requiring IGBT Count for DC Breaker**

| DC Breaker | |
|---|---|
| **IGBT Current Breaker Capability ($I_{peak}$)** | 3 kA |
| **Number of SMs for Commutation Breaker** | 200 |
| **Number of SMs for Commutation Switch** | 3 |
| **Bi-Directional Multiplier Index** | 2 |
| **# of line Multiplier Index** | 2 |
| **Parallel Index** | 2 |
| **Number of IGBTs per Station** | 1612 |

The conduction losses for the converter can be calculated using Equation 5.1 [13], and the conduction losses for the dc breaker are calculated as in (5.3).

$$\boldsymbol{P_{cond} = I_{dc}{}^{2}(N_{SM}R_{on}/N_{p} + R_{mc})} \quad \textit{(5.3)}$$

$P_{cond}$ : conduction losses

$N_{SM}$ : number of submodules

$R_{ON}$ **:** equivalent conduction resistance of a submodule (1.361mΩ)

$I_{dc}$ : rated dc current (2kA)

$R_{mc}$ **:** Mechanical disconnector close resistance (0.005Ω)

$N_P$ **:** Parallel index

The converter conduction power losses for the two solutions comparing to a base model using half-bridge MMC without fault current capability are listed in the Table 5-7, where indicates that the solution consists of half-bridge and dc breaker has negligible conduction losses since during the normal operation the dc current only flow through the main current branch. On the contrary the power loses for the solution with full-bridge MMC doubled comparing to the base model.

**Table 5-7: Power Losses Comparison to Base Model Case per Station**

| | Half-Bridge Base Model | Solution with Full-Bridge MMC | Solution with Half-Bridge MMC and DC Breaker |
|---|---|---|---|
| Total Number of IGBTs | 2400 | 4800 | 4012 |
| Power Losses (% of Rated DC Power) | 0.30% | 0.60% | 0.30004% |
| Extra Power Loss Compare to Base Model | 0 | 100.00% | 0.01% |
| Extra IGBTs required compare to Base Model | 0 | 2400 | 1612 |

### 5.5.6. Cost Analysis and Evaluation

In aspects of investment costs, with the power electronic valve being the majority of the converter station's costs, the total numbers of IGBTs required for both solutions are summarized in Table 5-7. If the peak current ratings of the IGBTs are rated to 6 kA, the total number of IGBTs required for the solution using a dc breaker is reduced by approximately 25% when compared to the number of IGBTs required for using 3 kA rated IGBTs. In this case study, a bi-directional HVDC scheme was used, which doubled the number of IGBTs as compared to a unidirectional dc breaker. Overall, the investment in power electronic valves for the solution utilizing half-bridge MMC and dc breakers will be cheaper than the cost in power electronic valves for the solution utilizing full-bridge MMC. In addition to the IGBT specification and the scheme's requirement for short circuit current interruption, there haven't been any discussions of the costs associated with real estate and valve installation footprint, as well as construction costs, which can be significantly different between offshore installations and onshore installations. On each project, these considerations and analyses should be carried out in order to make comparisons. Lastly, from a reliability perspective, a utility engineer needs to conduct reliability analysis based on each project between the options using full-bridge MMC with built-in fault clearing capability and purchasing additional dc breakers based on performance specification, operating and maintenance strategies.

## 5.6. Summary

In this chapter, case studies in PSCAD-EMTDC were conducted to compare the two dc fault clearing solutions: using full-bridge MMC and using half-bridge MMC with dc breakers. Both solutions are evaluated for their feasibility and performance aspects during dc fault clearance and after fault system restoration. Using the PSCAD-EMTDC, a proactive hybrid dc breaker model was developed that is capable of breaking and isolating dc faults for a symmetrical monopolar

HVDC scheme based on the proposed prototype from ABB. The two solutions were subjected to a systematic evaluation of their fault clearing capability and performance using standardized and predetermined dc fault clearance strategies, which were then compared. After conducting a thorough analysis of the study's findings, it was discovered that the full-bridge MMC solution provides overall superior performance in fault clearance and ac system integrity for the interconnected ac networks. In contrast, a solution using a half-bridge and dc breakers has also demonstrated comparable fault clearance capability. As determined by the examination of the conduction loss and the equipment investment cost, the solution combining the use of dc breakers has competitively low conduction losses and reduced investment costs.

**Table 5-8: Overall Evaluation Summary**

| | **Half-Bridge Base Case Model** | **Full-Bridge MMC** | **Half-Bridge MMC with DC BRK** |
|---|---|---|---|
| **DC Fault and Fault Recovery Performance Rating** | Unsatisfactory | Satisfactory | Satisfactory |
| **Power Loss Compare to Base Case Model** | 100% | 200% | 100.01% |
| **Cost of IGBTs required compare to Base Case Model** | 100% | 200% | 167.17% |

Using the performance evaluation criteria stated in Table 5-1, the overall performance evaluation comparison for the base case and two alternative solutions can be summarized in Table 5-8. Based to its significantly lower cost and loss, half-bridge MMC with dc breaker is the preferred solution with its satisfactory dc fault and dc fault recovery performance. Due to this evaluation criterion's stringent recovery time requirement, the half-bridge base case model was unable to satisfy the performance requirement. As previously stated, the performance criteria and evaluation matrix are dependent on the system requirements of the owner and must be addressed on an individual basis.

# Chapter 6.

# Contributions, Conclusions, and Recommendations for Future Work

## 6.1. Contributions

The main contributions of this thesis are summarized in below:

1. Review of VSC-HVDC technology together with its converter and system configurations,
2. Review of the current dc fault clearance techniques,
3. Review and present MMC submodule topologies with dc fault clearing capability,
4. Review and present the latest dc breaker developments,
5. Develop a methodology to evaluate the performance, capability, loss and cost for comparing different dc fault clearance techniques, and
6. Develop a proactive hybrid dc breaker model based on ABB's prototype in PSCAD-EMTDC.

## 6.2. Conclusions

This thesis researched dc fault clearance methods for the VSC HVDC system and developed a framework for evaluating the various dc fault clearance techniques based on their feasibility, capability, performance, losses, and cost. Understanding the operational bases, different converter topologies, and system configuration for VSC HVDC are critical foundations for this investigation.

The investigation began by comparing the principles of VSC and LCC HVDC. Additionally, a comprehensive investigation of the dc fault characteristic in respect of pole-to-ground and pole-to-pole faults was undertaken in a VSC HVDC transmission system, during which the detrimental effect of VSC on the venerability of dc faults was revealed and discussed in Chapter 2.

Two techniques for dc fault clearance were investigated in detail. Chapter 3 discussed MMC submodule topologies that include dc fault clearing capability. The working principles of full-bridge and clamp-double MMC topologies were described, along with a quick comparison of their fault current clearing capability, as well as associated losses and costs.

In Chapter 4, a comprehensive review of the different dc breaker topologies presented the latest state of arts dc breaker prototypes with each of the breaker type described separately: first, the detail single line diagram and working principle were provided; then, an overview of the sample design prototypes and installations from different projects was presented to give an overall design specification; and finally, the suitability of VSC-HVDC dc fault clearance application was carefully reviewed. A technical framework developed for HVDC dc circuit breakers by Cigré working group A3/B4.34 was used to create an evaluation methodology comparing the performance specification of different dc breakers, and this methodology was then used to analyze dc fault clearance techniques in the case study.

In Chapter 5, systematic analysis of a pole-to-pole dc fault in a monopole point-to-point VSC-HVDC system using two clearance techniques was conducted in PSCAD-EMTDC. It was concluded that dc fault clearance solution using full-bridge MMC has a superior performance in fault clearance speed in comparing with the other solution using half-bridge MMC and dc breakers. Through the case study the losses and cost are also evaluated using the evaluation methodology

developed through the early research. The simulation findings indicated that the solution utilizing dc breakers has a fault clearance capability comparable to that of the full-bridge MMC but at a cheaper cost and with significantly lower conduction losses. In contrast, the full-bridge MMC solution has much higher conduction loss which has a large impact on the operating costs throughout the asset's life.

## 6.3. Suggestions for Future Research

Due to time constraints, this thesis evaluated and studied only dc breaker and MMC submodule topologies with fault current clearing capability. Fault current limiting technology is currently being explored and developed for HVDC applications due to its low on-state losses, rapid response, automatic resetting capability, and multiple operation abilities. Future research should investigate and analyze the effectiveness and performance of current limiting reactors, solid state fault current limiters, and superconductor current limiters utilizing the suggested evaluation methodology.

With the development of multi-terminal HVDC grids, hybrid LCC and MMC VSC HVDC systems are being studied and constructed that utilize thyristor based LCC technology to achieve quick dc fault interruption. In a hybrid HVDC system, the advantages and benefits of LCC-HVDC and VSC-HVDC are inherited and can be realized at the converter level, where LCC and VSC converters can be connected in series or parallel to form a hybrid converter [83]; or at the bipolar station level, where one pole utilizes LCC-HVDC technology and the other pole utilizes VSC-HVDC technology [83]; or at the system level for point-to-point or multi-terminal HVDC system, in which one station serving as sending end using LCC-HVDC technology and other stations as receiving ends using VSC HVDC technology [83] [84] [85] and possible DCCB [86].

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