Design and Implementation of a Grid-Connected Solar Micro-Inverter using a Single-Stage Galvanically Isolated Topology with Integrated Magnetics

by

Hafis Kolapo Umar-Lawal

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Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Canada

Abstract

Solar panels have been steadily increasing in capacity and decreasing in cost over the past few years. Given this context, and other incentives designed to increase renewable energy penetration, residential solar adoption is becoming more economically attractive. The solar AC module stands out amongst alternative residential solar technologies, for better modularity, higher efficiency, and ease-of-use. The Micro-Inverter (MI) topology bundled with the AC module then becomes a key factor in the overall cost, safety, and capacity of the system. The Flyback (FB) MI topology is a popular choice, thanks to its low component count and enhanced safety, but as modern residential solar panels trend towards 400 W and up, non-interleaved FB MIs, typically rated around 200 W, must become interleaved. Conventional FB MI interleaving is High Frequency (HF) interleaving, which adds a potentially bulky magnetic device to the topology. This thesis proposes and tests the application of an alternate topology, called the Isolated Manitoba Inverter (ISOMBI). The ISOMBI uses integrated magnetic devices and Low Frequency (LF) interleaving, to match the power rating of HF-interleaved FB MIs, without the extra bulky component. ISOMBI operating principles and analyses are disclosed, and an experimental prototype is constructed to test its ability as a grid connected power generator. The results show near unity Power Factor (PF), acceptable DC current levels and promising Total Demand Distortion (TDD). Overall, these results indicate that the LF-interleaved ISOMBI can be considered as a viable alternative to the HF-interleaved FB MIs in AC modules.

Dedication

To Mom

Acknowledgements

My sincere and utmost gratitude goes to Dr. Carl Ho. My teacher and mentor. 6 years ago, I met you in the undergrad electronics 2 course, and on the verge of quitting electrical engineering. The guidance, mentorship, and most of all passion that you showed inspired me to stick around, and here I am, preparing a master's thesis. I cannot imagine my career progression, without your incredible levels of patience, and the development environment you fostered, where I felt safe and boldened to pursue research. I hope someday you will be proud of having trained me.

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List of Acronyms

24/7	-	24 hours, 7 Days
A.T.	-	Ampere-Turns
AC	-	Alternating Current
ADC	-	Analog to Digital Converter
BW	-	Bandwidth
CCM	-	Continuous Conduction Mode
CCS	-	Code Composer Studio
CL	-	Capacitor-Inductor (Low pass filter)
COVID-19	-	Coronavirus Disease 2019
DC	-	Direct Current
DCM	-	Discontinuous Conduction Mode
DSP	-	Digital signal processor
EMI	-	Electromagnetic Interference
ePWM	-	Enhanced Pulse Width modulation
ESR	-	Equivalent Series Resistance
FB	-	Flyback
GM	-	Gain Margin
HF	-	High frequency
IDE	-	Integrated development environment
IEA	-	International Energy Agency
IEEE	-	Institute of Electrical and Electronics Engineers
IGBT	-	Insulated Gate Bipolar Transistor
ISOMBI	-	Isolated Manitoba Inverter (The proposed topology)
ISR	-	Interrupt Service Routine
KCL	-	Kirchoff's Current Law
LPF	-	Low Pass filter
MATLAB	-	Matrix Laboratory (software)
MI	-	Micro-Inverter
MLPE	-	Module Level Power Electronics
MMF	-	Magnetomotive force
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor

MPPT	-	Maximum Power Point Tracking
NEC	-	National Electric Code (of the USA)
PCB	-	Printed Circuit Board
PF	-	Power Factor
PLECS	-	Piecewise Linear Electric Circuit Simulator (simulation software)
PLL	-	Phase Locked Loop
PM	-	Phase Margin
PV	-	Photovoltaic
PWM	-	Pulse Width Modulator
RC	-	Resistor-Capacitor
RCD	-	Resistor-capacitor-Diode
RHP	-	Right-Half-Plane (of the complex axes)
RMS	-	Root Mean Square
TDD	-	Total Demand Distortion
TF	-	Transfer Function
THD	-	Total Harmonic Distortion
TI	-	Texas Instruments
US	-	United States (country)
USB	-	Universal Serial Bus

Chapter 1 - Introduction

1.1 Problem Definition

The US department of energy projects significant cost reductions for solar panels, due to efficiency gains in solar cell research [1]. This could improve the economic appeal of solar power and promote its residential application. As such, AC modules, which consist of solar panels bundled with Micro-Inverters (MIs), and are primarily targeted at residential installations now trend in research and commercially [2]–[7]. The rise of the AC module is largely due to its ease-of-use over the alternative (solar panel with string-inverter arrangement). MIs are power electronics devices that process power from a single solar panel and enable the AC module's plug-and-play (ease-of-use) functionality [8]. However, residential grade solar panels, previously limited to a range of 200-250 W now peak at about 400 W, thanks to improved solar cell efficiency [1], [9]–[11]. MI topology power ratings must therefore be evaluated to keep up with modern solar panels and maintain AC module functionality.

The Flyback (FB) MI topology emerged in MI research, as an efficient single-stage topology, with low component count (low costs), and galvanic isolation (boosts safety), making it a choice MI topology for AC modules [12], [13]. However, in order to match the increasing power output of modern solar panels, the FB MI found in commercial products is applied with High-Frequency (HF) interleaving [12]–[14]. HF-interleaving assists the FB MI to increase output power efficiently, whilst maintaining advantageous single-stage conversion and galvanic isolation. On the other hand, HF-interleaving adds an extra magnetic device to the FB MI, potentially increasing costs, and bulk. This research proposes an alternative, by investigating the application of a new FB-type topology to AC module MIs. The proposed topology uses LF-interleaving and functionally integrated magnetics, to avoid the extra magnetic device associated with HF-interleaving.

1.2 Research Scope

The work done in this thesis investigates the use of a new single-stage FB-type topology as an AC Module MI. The topology, called the Isolated Manitoba Inverter (ISOMBI) uses functionally integrated magnetic components and LF-interleaving for grid synchronized DC-AC power conversion. The thesis also provides a comprehensive analysis of FB MI operating characteristics and proposes a double loop current control strategy for grid-connected FB MIs. Figure 1-1 provides a visual summary of the research scope which explores the following themes:

a) Review contemporary FB MI topology variants and study their operating principles.

b) Investigate and compare the ISOMBI topology with contemporary FB MI variants

c) Derive and validate operating principles for using the ISOMBI topology as a MI, supported by analyses, simulation, hardware implementation, and laboratory experiments.

d) Design and use functionally integrated magnetic devices for reduced component count.

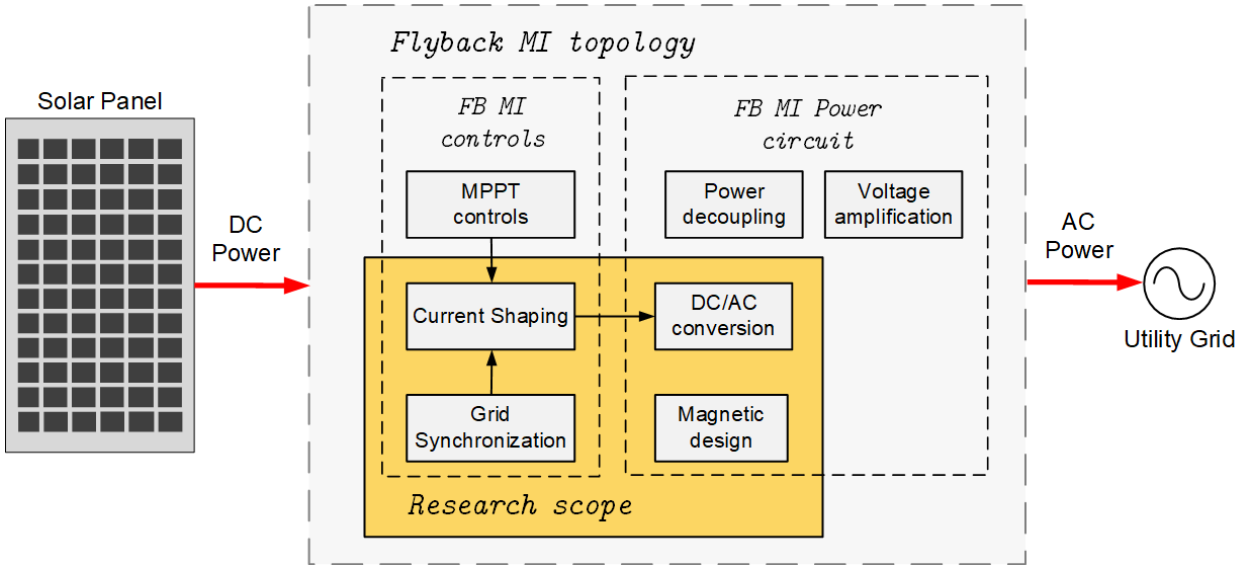


Figure 1-1. Visual summary of research scope

1.3 Background

Electricity is vital to sustaining today's 24/7 digital economy, especially recently, where COVID-19 pandemic restrictions have catalyzed the adoption of remote activities [15]–[17]. These new forms of work, play and learning have caused a shift in energy profiles [15], such that despite an overall decrease in total energy consumption, residential demand is at an all-time high [15]. The situation thereby introduces an opportunity to restart the economy from clean energy sources [17]–[21]. If remote activity continues to sustain high residential demand, residential solar adoption would be decisive in meeting the International Energy Agency's (IEA) sustainable development goals, of having 49% renewable penetration by 2030 [22].

In residential solar installations, photovoltaic (PV) modules, also known as solar panels, mounted on a rooftop or on the ground, convert incident light photons into Direct Current (DC) electrical energy, to be processed into Alternating Current (AC) by an inverter [23], [24]. The inverter is an active and controllable power processing device, whose basic responsibilities include: Converting DC power to AC power synchronized with the utility grid's phase and frequency, extracting maximum possible power from incident solar radiation, decoupling pulsating AC output power from constant DC input power, and sometimes boosting low DC input voltage to match the peak of the utility grid voltage [8], [25]. Each inverter function is the subject of intense research, resulting in proposals of various topologies, system arrangements and control algorithms [6], [8], [25], [26].

This introductory chapter highlights basic inverter functions and residential solar installation arrangements; introduces the AC module concept; and compares inverter technologies against each other in terms of benefits, drawbacks, and challenges. These discussions are used to support the research scope, and contributions. The chapter concludes by presenting a brief outline for the rest of this thesis.

1.4 Basic Functions of a Residential Solar Inverter

Three basic functions can be identified for all types of residential solar inverters, these are: Maximum Power Point Tracking (MPPT), power decoupling and DC-AC power conversion [8]. With all the aforementioned, MIs specifically are further required to provide voltage amplification, to match the output voltage of a single solar panel with the peak amplitude of the AC grid [12]. These four basic functions are discussed in following subsections.

1.4.1 Maximum Power Point Tracking (MPPT)

To maximize the solar energy harvested by the installation, the operating parameters of a solar panel must be managed by the inverter, such that the panel generates the maximum possible power under prevailing atmospheric conditions [8], [27]. The solar panel is made up of solar cells that generate electric power in proportion to irradiance levels and surrounding temperature. Figure 1-2 demonstrates this by showing the I-V characteristic curves of the Kyocera KC200GT solar panel, obtained from [27].

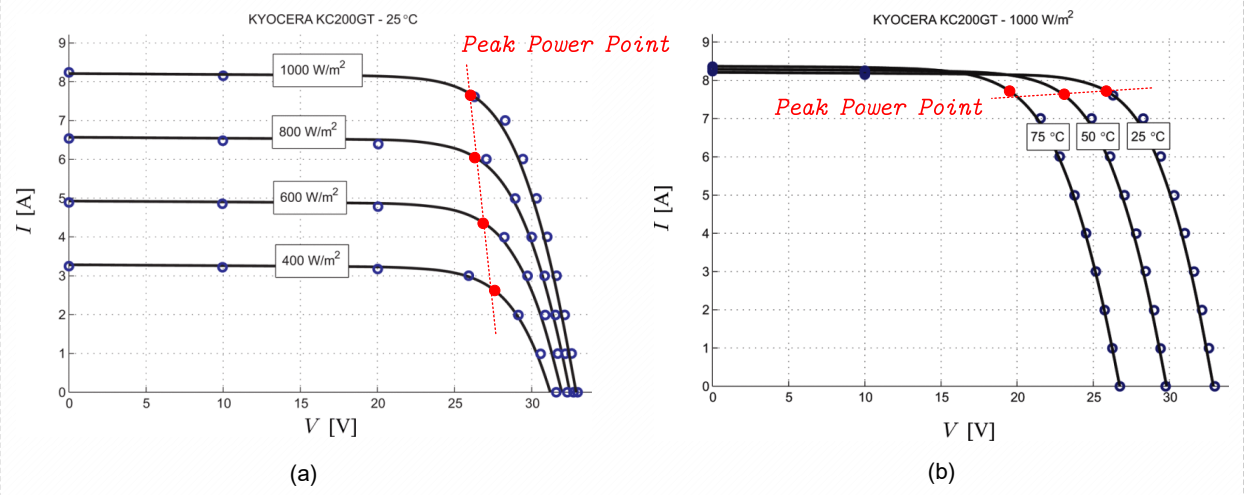


Figure 1-2. Illustrating variance in panel operating parameters with irradiance level and temperature for the Kyocera KC200GT solar panel (a) I-V curves under different irradiation levels at 25°C, (b) I-V curves at different temperatures [25].

In Figure 1-2(a), operating parameters vary with irradiance level, while in Figure 1-2(b) they vary with temperature [27]. In both figures, A dotted line indicates the optimal operating point, where maximum power can be extracted across varying conditions. Consequently, inverters must employ MPPT algorithms to manage the operating voltage or current of the panel, if they are to extract maximum possible power, despite dynamic changes in atmospheric conditions.

1.4.2 DC-AC Power Conversion

The main function of a grid-connected residential inverter is to convert DC energy into AC energy and synchronize with the AC utility grid. This makes the installation a grid connected power generator. As such, it faces strict requirements governing the quality of power sent to the grid [8]. For instance, a prominent California utility requires residential inverters to maintain unity PF by default (and limit variations between 0.9 leading and 0.9 lagging), limit current TDD to below 5%, and DC current injection to less than 0.5% of the rated current [28].

To meet such requirements, designers place constraints on the design of output filters used by the inverter and actively shape the current using control algorithms. The ideal AC current for unity PF is a pure sine wave at the same phase and frequency as the grid voltage. Hence, current control schemes include tracking and shaping algorithms must ensure phase and frequency synchronization. While output filters are used to smooth and deliver continuous sinusoidal current.

1.4.3 Power Decoupling

Residential solar installations are single-phase AC power systems, which create a pulsating power component at twice the grid frequency on the AC side [8], [12]. To maintain instantaneous equilibrium between the DC input power and AC output power, the pulsating component is reflected onto DC input parameters, [8], [12]. The double line frequency component on the DC input voltage, negatively impacts MPPT, as it causes operating parameters to deviate from the

optimal point [8]. To restore effective MPPT, the DC voltage ripple must be kept below 8.5%, by decoupling instantaneous power between the AC and DC sides [8].

Power decoupling may be active or passive [12]. Passive power decoupling places a high value electrolytic capacitor between the solar panel and the utility grid which reduces DC ripples and buffers the power supplied to the AC side [8], [12]. Electrolytic capacitors are used because they offer higher energy density than other types [29]. However, they are also known to age poorly under temperature extremes, and become a limiting factor in the harsh operating environment of some inverters [8], [29]. This has led to the development of active power decoupling techniques, such that more resilient, lower value film capacitors can be used to achieve the same objectives.

1.4.4 Voltage Amplification

This requirement is unique to MIs, which convert power from a single low-voltage solar panel. The alternative, string-inverter, avoid voltage amplification by using series connected solar panels to increase the DC voltage [8]. A residential grade solar panel, consists between 60 and 72 photosensitive PN junction cells [30], [31], each operating between 0.5 and 1.0 V [8]; Hence, the typical residential panel operates in a voltage range between 24 and 60 V. However, the North American power grid offers a 170 V amplitude at the most accessible interface [32], and as a result, the MI, converting a single panel's power must amplify the voltage to match the grid level.

1.5 Configuration of Residential Solar Installations

Figure 1-3 is a simple infographic illustrating a sample grid-connected residential solar energy project [33]. Roof mounted solar panels transfer DC energy to an inverter, which subsequently outputs AC energy to household loads and the utility grid. The depicted inverter is a string-inverter which processes power from all the solar panels. Residential solar installations are classified based on the type of inverter deployed. Hence, they are either string-inverter-based (like Figure 1-3) or micro-inverter-based systems. These are the two distinct inverter types used in residential installations and their impacts on system configuration are presented in following subsections.

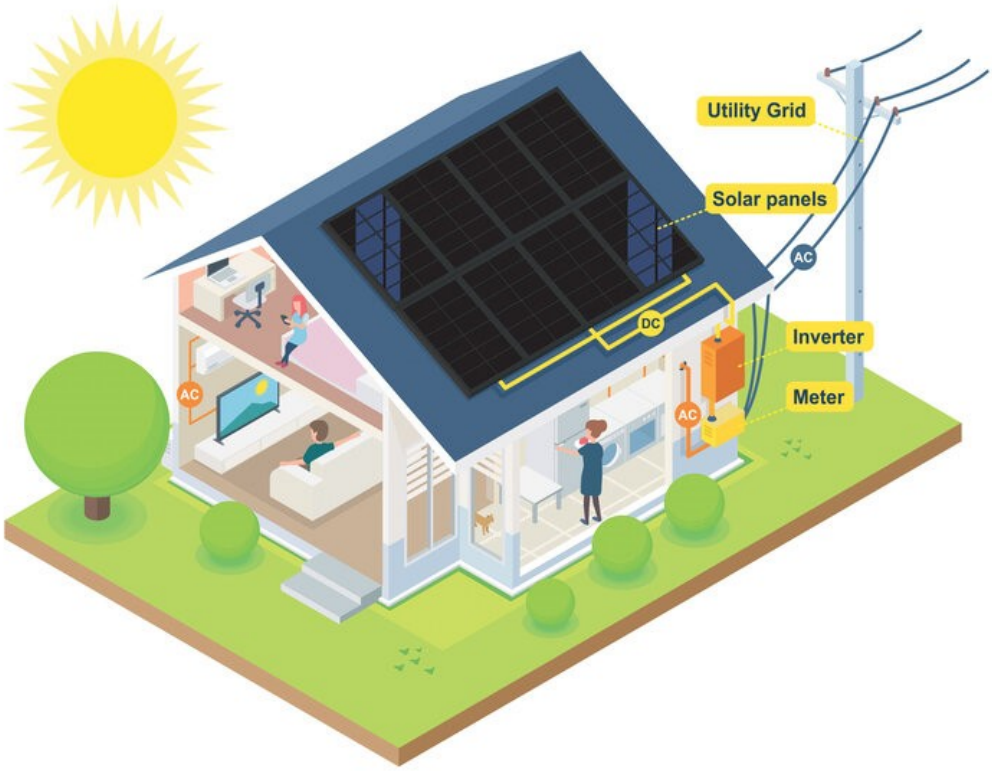


Figure 1-3. Residential solar infographic [33].

1.5.1 String-inverter System Configuration

Figure 1-4 shows a simplified schematic of a basic string-inverter system [34]. Energy from the solar array travels through protective disconnects and a string-inverter to household loads and the utility line. Solar panels in a string-inverter based system are series connected (to form strings), such that the series voltage exceeds the grid voltage, and they do not need extra voltage amplification [8]. The string-inverter is so called due to the string-like connection of panels, which form a single DC input to the Inverter. As depicted in Figure 1-4, the string-inverter is responsible for power decoupling, MPPT and DC-AC power conversion of the entire solar array [8].

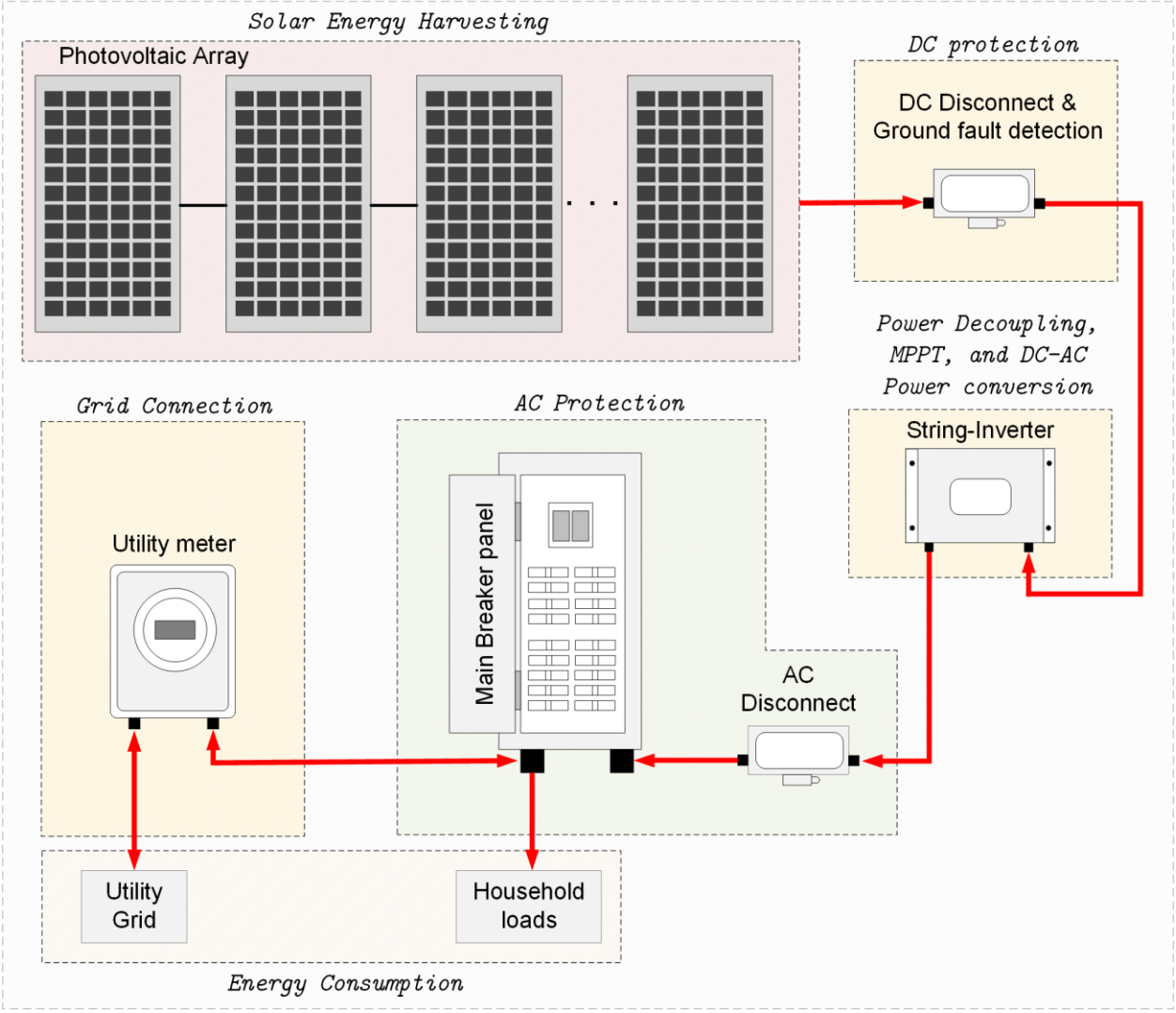


Figure 1-4. String-inverter PV system schematic, adapted from [34]

There are three different methods of configuring a string-inverter system [7], [8]. All three methods are illustrated in Figure 1-5. The standard string-inverter configuration of Figure 1-5(a) is one where the solar strings are directly connected to the inverter. About 16 to 20 panels may make up one string to avoid exceeding the voltage ratings of conventional power semiconductors (1000 V) [8], and the use of one string is typical in residential applications to avoid the costs of duplicating inverters, protection equipment and a more demanding installation process.

The arrangement of Figure 1-5(b), is called the Multi-string configuration [8], where the MPPT of a single string is first performed by a DC-DC optimizer stage. Then subsequently, optimized DC outputs are converted to AC power using a single string-inverter, which also handles power decoupling. This configuration is uncommon in residential projects, where a single string is often used, and the DC-DC stage offers no additional benefits over the standard String setup to justify the additional cost of acquiring a DC-DC optimizer.

Finally, Figure 1-5(c) called the “Module-Level Power Electronics (MLPE) optimized” string configuration, introduces MLPE DC-DC optimizers that perform individual MPPT for each panel [7]. Optimized DC outputs are then processed by a single string-inverter into AC with power decoupling. Since MPPT is performed for each panel, the system is not held back by weak, damaged, or shaded modules. The main drawback of this final arrangement is the additional cost of acquiring the MLPE DC-DC optimizers, which place it above the previous arrangements in terms of acquisition costs.

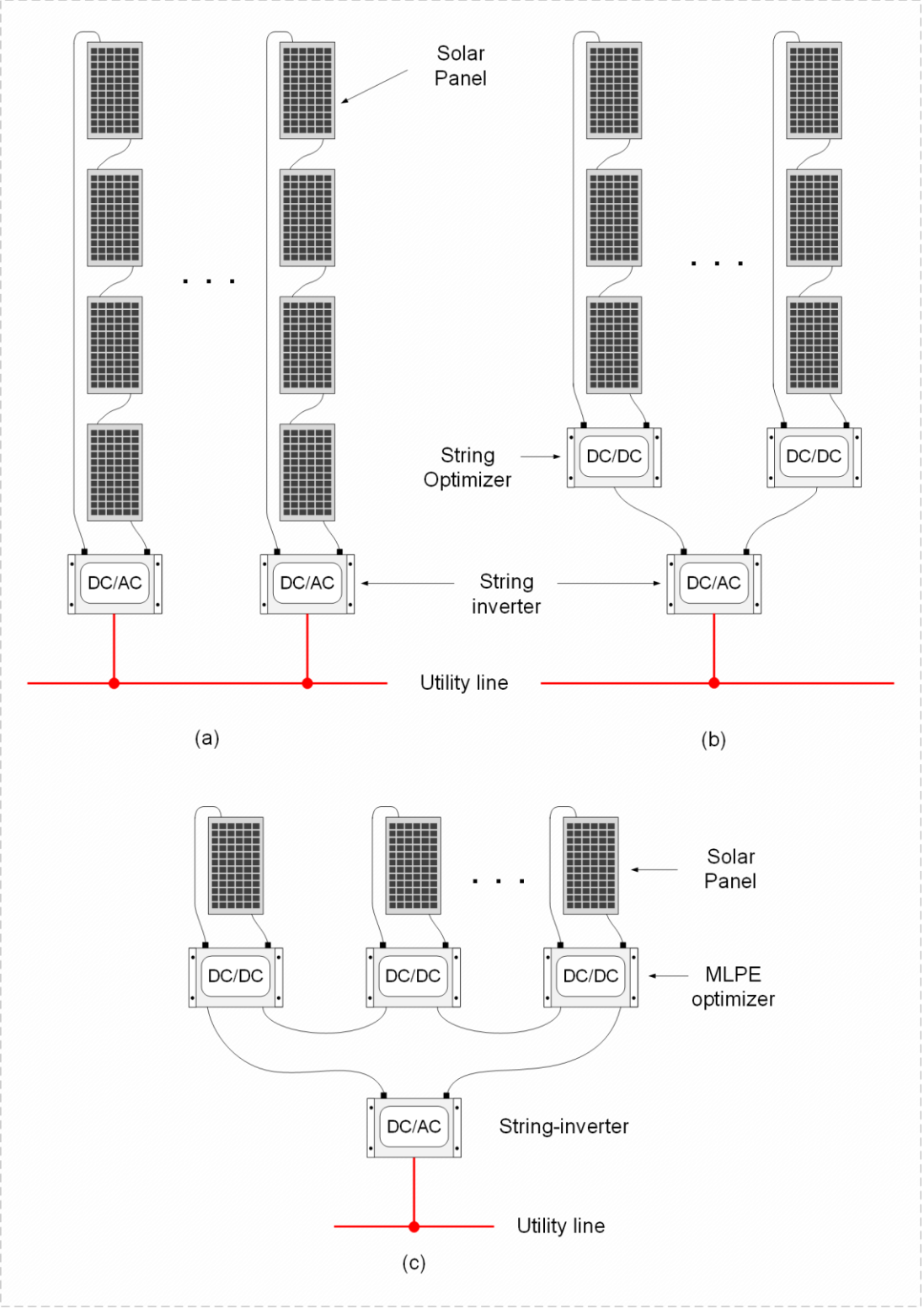


Figure 1-5. String-inverter system configurations, adapted from [7], [8].
(a) Standard string connection (b) Multi-string connection (c) MLPE-string connection.

The use of a single string-inverter for centralized DC-AC conversion of an entire solar panel array facilitates access to the device for maintenance and diagnostics. This also lowers the difficulty of design compared to a potential distributed system and is translated into low acquisition costs [35]. However, the system also becomes susceptible to single-point failures because the malfunction of the sole string-inverter will halt operations. The other main disadvantage of centralizing DC-AC Power conversion for a string of panels, is losing access to individual panel parameters (except for the MLPE-string arrangement). This means that MPPT cannot be truly optimized for every panel, and the weakest, shaded or otherwise damaged panels will hold back the entire system.

It is also relatively tasking to plan and install a string-inverter based systems. String lengths must be carefully configured, considering panel and inverter characteristics, desired power output and budget. The calculations are relatively simple, but quickly become exhausting, considering the large inventory of panels and inverters available at different price points. Yet upon installation, the system is inherently low in modularity and deters capacity upgrades. Adding extra panels may be simple as reconfiguring string wiring, but it is more likely to involve string-inverter resizing. In essence, because string-inverter do not enable plug-and-play functionality, have low modularity, and are complicated to plan, their ease of use is inhibited.

1.5.2 Micro-Inverter System Configuration

The MLPE-string setup from the previous section represents progress towards solving the issues plaguing string-inverter systems. By decoupling MPPT from DC-AC power conversion at the panel level, it solves the issues of sub-optimal MPPT. However, it disappoints by relying on centralized DC-AC conversion. MIs are essentially MLPE DC-AC devices that convert a single panel's DC energy into AC energy, synchronized with the utility grid. This introduces full system decentralization as well as plug-and-play functionality [7]. Since a MI focuses on an individual panel, the system requires as many MIs as there are solar panels, reflected in Figure 1-6, which

shows the basic setup of a MI system [7]. The name “Micro-Inverter” signifies the devices’ low power handling capability, as each MI only processes a fraction of the system power (around 200 to 400 W). Yet, despite such low power handling, the MI design process is much more involved than designing string-inverter [12].

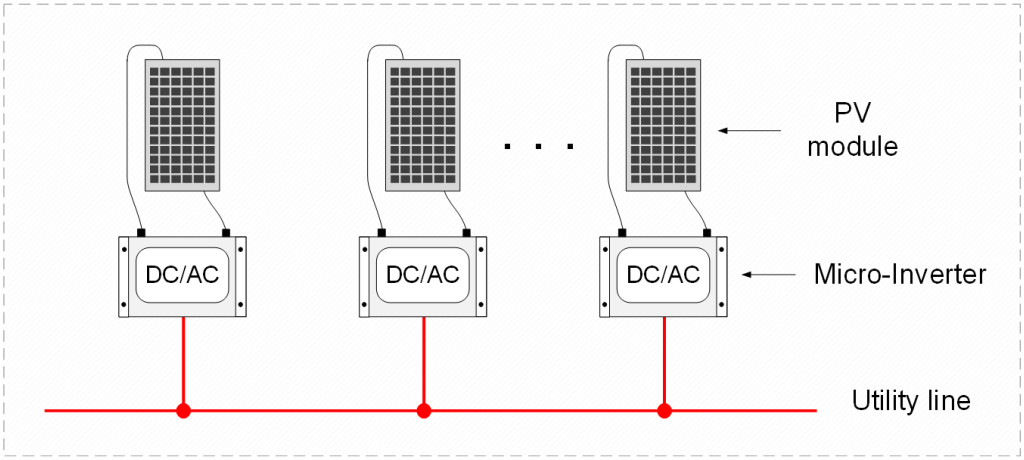


Figure 1-6. MI system configuration, adapted from [7]

First, MIs are intended to be paired with individual solar panels, and reside on rooftops, where harsh environmental conditions complicate their mechanical and thermal design [12]. Then the MI (unlike a string-inverter) must boost the voltage of an individual panel to match the peak of the utility grid [8], [12], and, the MI is still tasked with MPPT and power decoupling [12]. Finally, due to the distributed nature of the system and high number of devices, MIs might include extra control- and auxiliary- electronics to synchronize AC outputs together, and with the utility grid [12]. Despite these challenges however, the advantages of using MIs include unlocking full system modularity, removing single-point failure, and simplifying planning or upgrade processes. From a homeowner’s perspective, these benefits outweigh design difficulties, hence, MI design attracts a lot of research attention.

1.5.3 AC Modules – Enabled by MIs

An AC module is a modular device consisting of a solar panel physically bonded to a MI. For example, Figure 1-7 shows the Panasonic N330E HIT ® AC module, which combines a Panasonic HIT ® panel, with an Enphase IQ 7X MI [36]. The AC module is so called because it has no DC terminals and is intended to be used as an AC device through the inverter output terminals.

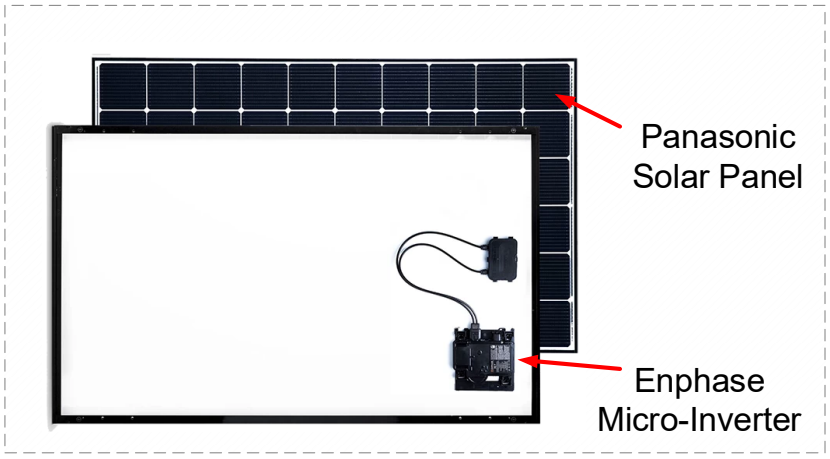


Figure 1-7. An Enphase-Panasonic AC module [36]

AC modules simplify wiring and present the opportunity to be used in “plug-and-play” fashion. Figure 1-8 presents the simplified schematic of an installation using AC modules [37]. Compared with the string-inverter scheme of Figure 1-4, the system is much more user friendly. Each module connects in parallel, through to an AC junction box, and onwards to the utility grid and household loads. A branch may contain up to 15 AC modules sharing one junction box, limited only by the protective current ratings of the subsequent AC breaker. The system is characteristically modular, such that a project could start as one AC module, build up to the maximum modules per branch, and further to multiple branches. The only limit will be the number of breakers in the AC sub panel, and these expansions could be carried out with minimal rewiring, recalculations, and no resizing of components as in string-inverter based systems. By using AC modules, the system also avoids the use of DC protection equipment.

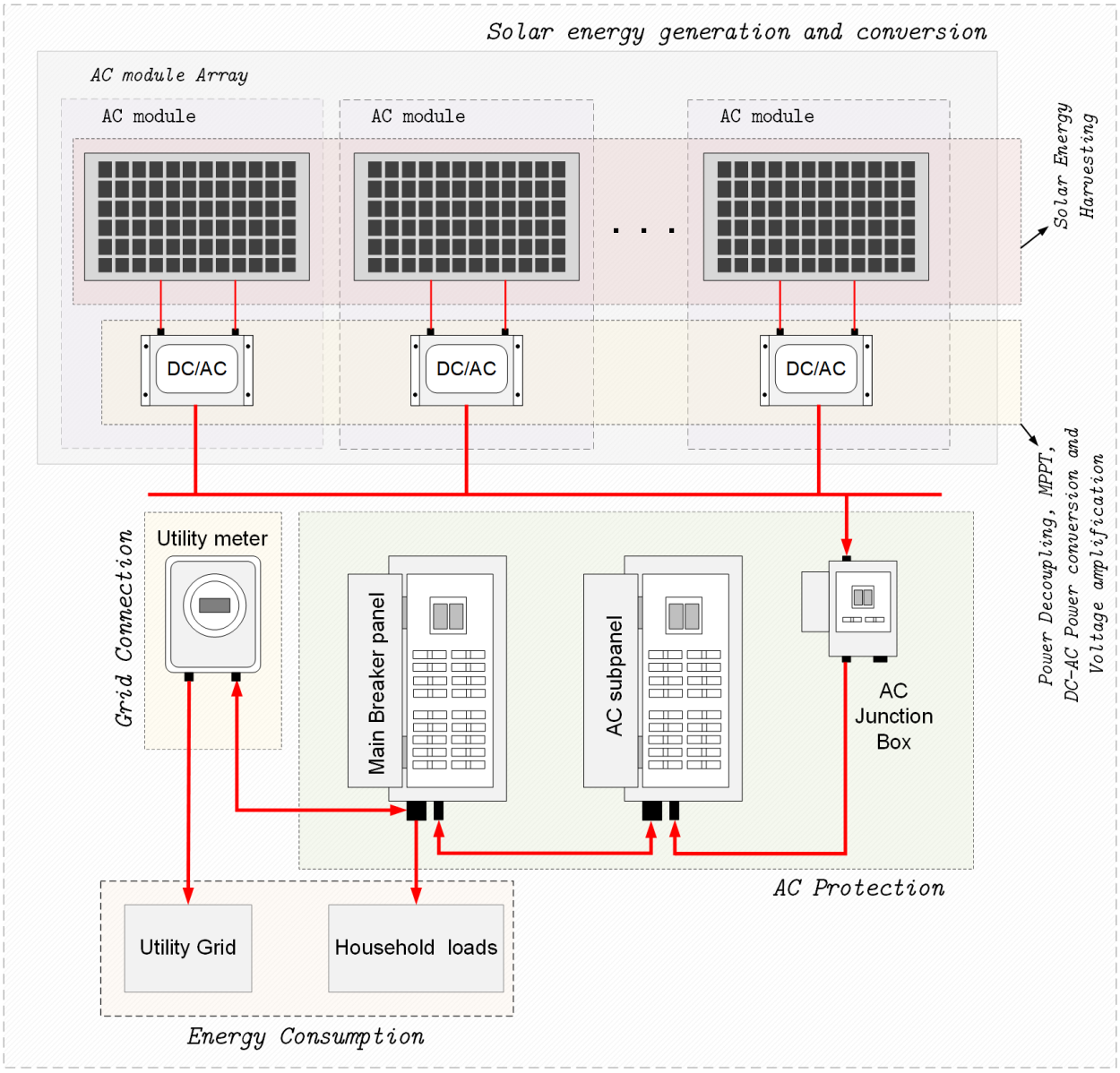


Figure 1-8. PV system schematic with AC modules, adapted from [37]

1.5.4 Comparisons between PV System Configurations

The average residential solar installation will vary in capacity from 2 to 10 kW_{DC} [34], while a single residential grade solar panel produces around 200 to 400 W [9], [10]. This results in a system size of 5 to 50 panels. The system configuration and inverter choice are therefore a critical factor for the overall system cost, ease of installation and system reliability. Table 1-1 summarizes the comparison of residential solar installation options, the discussion of which continues below.

Table 1-1. Comparison of PV system configurations

PV configuration	Control level	Modularity	System efficiency	Inverter serviceability	System cost	Inverter type
Standard string	String level	Low	Low	Easy	Low	*String inverter*
Multi-string	String level	Good	Low	Easy	Moderate	
MLPE-string	Module level	Better	Better	Easy	High	
Micro-inverter	Module level	Best	Best	Difficult	Highest	*Micro-inverter*

String-inverter systems are less user friendly, offer lower modularity, potentially complex planning/installation and possibly inhibited MPPT performance (impacting system efficiency), when compared with MIs. However, by being more pocket friendly, string-inverters have the cost advantage [35]. MLPE systems including the MLPE-string and MI setups improve system reliability by using a distributed architecture and improve efficiency with panel level MPPT. However only the MI setup avoids single point failure. Both MLPE systems also command greater acquisition and installation costs than alternatives.

In terms of modularity, the MI triumphs because of its use in plug-and-play AC modules, which simplifies upgrades and decommissioning of damaged panels. The MLPE-string setup is not far behind, retaining capability of the latter feature but not the former. In terms of efficiency, lack of panel level MPPT hinders the standard-string and multi-string arrangements. While the double

power conversion (DC-DC and DC-AC cascade) of the MLPE-string places it behind the potential singular DC-AC power conversion of the MI system.

However, the MI system falls short in serviceability and system cost. Cost is driven up by design complexity and total number of units required per project. While serviceability is impacted because the solar panel is bundled with the inverter as a roof-mounted AC module. Hence, inverter access is not as easy compared with garage- or utility closet- residing string-inverters. The MLPE-string benefits from the easy inverter access of the string-inverter for servicing but follows right behind MI systems with high costs. MLPE-string optimizers are not as complex to design, but multiple units are needed for the project leading to high costs.

Lastly, the failure of a single MI or AC module panel does not cause a single-point failure as with String-inverter, hence it is still more reliable, and faulty AC modules can be taken out of service to operate the system at lower capacity, without losing efficiency. In contrast, damaged panels in a string-inverter system must be bypassed with diodes placed in the path of full string current and reducing efficiency. Ongoing MI research, including this thesis aim to tackle some MI challenges, in hopes that the cost disadvantage of MIs may become a distant memory.

1.6 Thesis Structure

This thesis is organized in 6 chapters. A brief introduction and summary of each chapter follows below, and part of the work presented in this thesis is included in the conference paper:

H. K. Umar-Lawal, C. Ngai Man Ho, and K. K. Man Siu, "An Isolated Single-Stage Single-Phase Micro-Inverter Topology with Integrated Magnetic Components," 2019 IEEE Energy Conversion Congress and Expo. ECCE 2019, pp. 4339–4344, 2019.

***Chapter 1: Introduction**:* Chapter one opens the thesis by presenting research problem and scope, followed by background information related to the research work. An overview of residential solar installations is provided, to outline inverter technologies. Then, the concept of an AC module is introduced and discussed before the chapter concludes with a comparison of Inverter technologies.

Chapter 2: Review of the Flyback Micro-Inverter Topology: Chapter two presents a review of FB MI topologies found in research literature. First it distinguishes between single-stage and two-stage topologies as background information for introducing the FB topology as a single-stage MI topology. Then three variants of the FB MI topology are explored briefly, with their operating principles. A discussion of the challenges faced by FB MIs, and comparison between the variants concludes the chapter.

Chapter 3: The Isolated Manitoba Inverter Topology: Chapter three introduces the Isolated Manitoba Inverter (ISOMBI) topology and its operating principles. Operation modes are based on the positive and negative cycles of the grid voltage, and demonstrate crafty use of functionally integrated magnetic components. Magnetic device models are explained, to explore properties that facilitate functional integration. Steady-state characteristics prove that the ISOMBI can

function like conventional FB MIs, and detailed derivation principles are presented for calculating circuit parameters.

Chapter 4: The Isolated Manitoba Inverter Control System: Chapter four details the proposed control system design for the ISOMBI topology. Starting with small-signal dynamic modelling, a procedure is prescribed for designing the control system. The small-signal modelling is verified by simulation and numerical analysis. Finally the controller implementation is presented as a double loop digital compensator using a Digital Signal Processor (DSP). The chapter closes with flowchart descriptions of DSP algorithms.

Chapter 5: Prototyping and Experimental Verification – Chapter five presents experimental results obtained from the research work. The experimental prototype and its specifications are detailed, including constructive results for magnetic component design. Then the experimental setup and measurement instruments are introduced briefly. Finally, measurement waveforms and other experimental data is presented to support theories proposed in chapters 3 and 4.

Chapter 6: Conclusion and Future work Recommendations – Chapter six concludes the thesis, with a reflection and evaluation of the work done in respect to prescribed themes. It discusses and summarizes experimental results, and looks to the future for improvement opportunities. This chapter closes the thesis and is followed by the Bibliography.

Chapter 2 - Review of the Flyback Micro-Inverter Topology

2.1 Overview of FB MIs

MI topologies are judged by their conversion efficiency, component count, harmonic injection, reliability, power density and isolation [6], [12], [25], [26]. The FB MI is a choice topology that ranks highly in almost all categories. It has built-in galvanic isolation through its FB transformer, is capable of high efficiency operation, enjoys a low component count, and can maintain low TDD, with high reliability [25], [26], [38]–[40]. The FB MI is also a single-stage topology, that transforms DC power to AC power, using a single power processing stage. In most reviewed literature, however the FB MI circuit is rarely used above 200 W [8], [13], [38]–[41], mainly because it is difficult to design an efficient high power FB transformer [13]. The topology is further held back by high peak current stresses and voltage clamping requirements, [5] ,[38]–[43]. These factors combine to necessitate interleaving for increasing FB MI power ratings.

Single-stage power processing allows the FB MI to maintain a low component count, essential for high reliability and superior power density. Likewise, built-in galvanic isolation is highly desirable. Consider for instance, the US National Electrical Code (NEC) 690 standard, which calls for system grounding and monitoring of solar panels operating above 50 V [8]. Some high-capacity solar panels may operate between 50 and 60 V. Meanwhile, the AC service entry of a residential electrical system is already grounded, so adherence to the standard leads to dual grounding. In non-isolated systems, dual grounding introduces lossy leakage currents [8], [44] [26], but the low interwinding capacitance of a FB transformer is extremely effective at preventing leakage current flow [7], [26]. Also, the enhanced safety leads some electricity boards forgo solar panel grounding altogether in the presence of galvanic isolation [8], and lastly, isolated topologies have been observed to achieve lower TDD, when compared to non-isolated counterparts [26].

2.2 Single-Stage vs Two-Stage MIs

Generally, MI topologies can be divided into single-stage (like the FB MI) and two stage [12], [25], [26]. The key difference between single and two-stage MIs, besides the number of power processing stages and task distribution between them, is where the power decoupling capacitor is placed [8]. Both are reviewed briefly to provide background information for introducing FB MI variants as single-stage topologies.

In a two-stage MI topology, illustrated in Figure 2-1, an input DC-DC conversion stage handles voltage amplification and MPPT, while grid current control is tackled by a subsequent DC-AC converter. Passive power decoupling is inherently built into the intermediate DC link capacitor, which does not need to be large because the DC link voltage is relatively high (few 100 volts), and the ripple requirement is loose (few 10's of volts). The DC-DC stage is often an isolated topology to reap the safety benefits of galvanic isolation and minimize leakage currents.

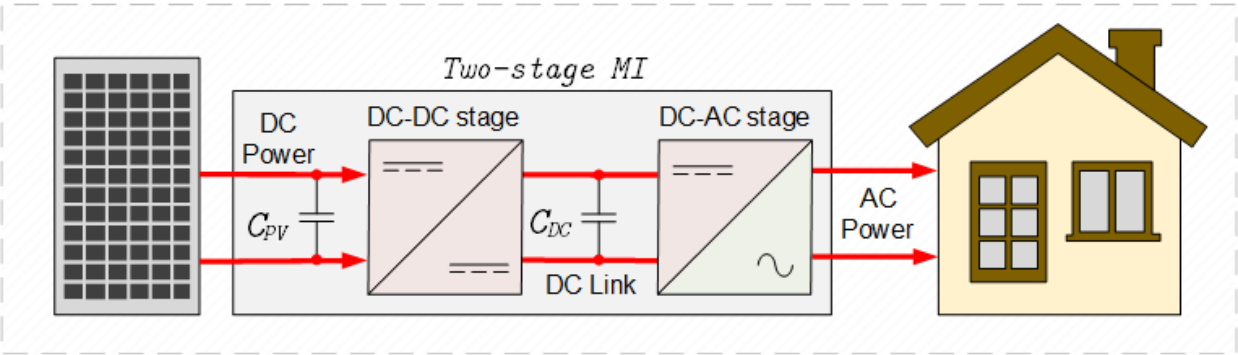


Figure 2-1. Two-stage MI illustration

This configuration allows both stages to be optimized individually, with the control objectives distributed amongst the two stages. Whilst this greatly simplifies the design procedure, the power losses incurred from two High-Frequency (HF) power processing stages negatively affects the total conversion efficiency, and housing two HF power converters also increases component count, resulting in both bulkiness and higher costs.

The single-stage MI depicted in Figure 2-2 performs all its functions in a single power conversion. This poses some unique challenges to the designer. First, the power decoupling capacitor must necessarily be placed on the PV side (C_{PV} in Figure 2-2), to meet ripple requirements for acceptable MPPT function [8]. Then the control system design must manage MPPT, voltage amplification and DC-AC conversion through a single HF power processing stage. Figure 2-3 shows the detailed system diagram of a single-stage MI, which is divided into the topology (power processing) and its associated control system. The topology is further divisible into power decoupling, power circuit (DC-AC switching stage) and a low-pass filter to smooth the output current. The MI controls consists of MPPT, grid synchronization and an AC current control algorithm, used to shape the grid current while transferring maximum possible power.

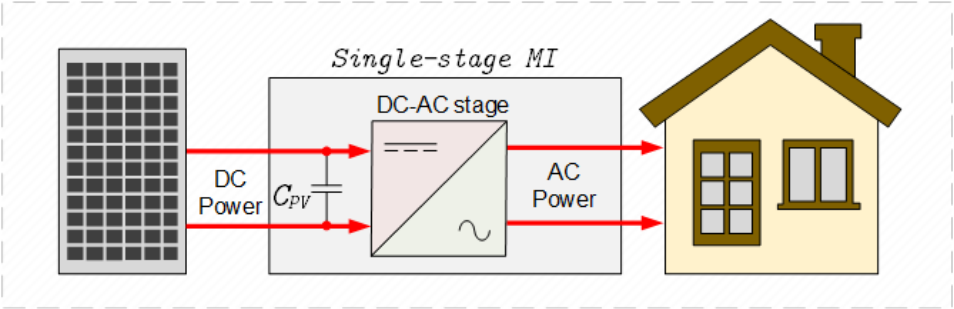


Figure 2-2. Single stage MI with PV side decoupling, adapted from [8]

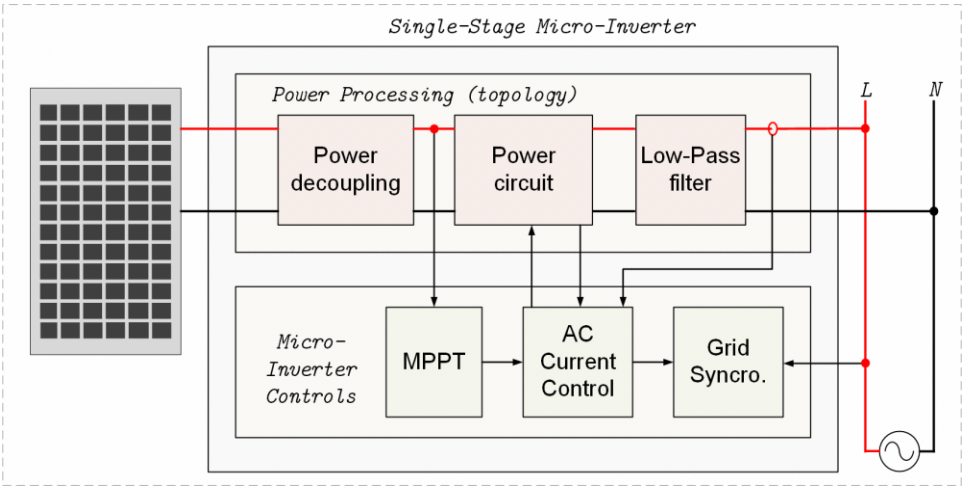


Figure 2-3. Single stage MI detailed system diagram

Because the decoupling capacitor is placed on the PV side, where the input voltage is low (10's of volts) and the ripple requirement is tight (few volts), the required capacitance tends to be relatively large (few millifarads), and energy dense electrolytic capacitors become the obvious choice. However, these electrolytic capacitors do not fare well in the harsh rooftop environment, where an AC module MI will operate. The ambitious objectives of single-stage MI topologies also tend to result in unconventional arrangements, which become difficult to model and control.

The FB MI is popular because it is viewed as one of the simplest single-stage MI topologies. However, even the FB MI has control challenges, because a varying Right-Half-Plane (RHP) zero in its main Continuous Conduction Mode (CCM) control-to-output transfer function [40], [41] makes it difficult to guarantee control stability over the entire range of operation. This often results in designers choosing to operate the FB MI in the Discontinuous Conduction Mode (DCM), where the current stresses are higher than observed in CCM and may result in lower efficiencies [41].

Table 2-1. Comparison Summary of Single and Two-Stage MI topologies

	Efficiency	**Power Density**	**Cost**	**Reliability**
Single stage MI	Higher	Higher	High	Lower
Two-stage MI	High	Good	Higher	Higher

Table 2-1 summarizes the key differences between single-stage and two-stage MI topologies. Single-stage MIs have better efficiency and power density thanks to their single power conversion. Both are costly (relative to string-inverters), but two-stage MIs are generally more expensive than single-stage MIs. Also, the application of electrolytic power decoupling capacitors impacts the reliability of single-stage MIs, compared with two-stage MIs that can naturally use smaller film capacitors. The single-stage MI challenges are well known, and receive a lot of research attention, specifically aimed at the FB MI that has been recognized for its simplicity, and potential to dominate the single-stage MI category [8], [25]. For instance, active power decoupling techniques,

that allow the use of smaller and more reliable film capacitors have been developed [45]. While, modelling and control techniques that promote CCM operation are also popular topics [38]–[41].

2.3 FB MI Topology Variants

The FB MI is based on the popular DC-DC FB topology, but with a modification that replaces the FB output with a pseudo-DC link, whose potential difference is a sinewave (sometimes rectified), coupled to the utility grid through a line frequency unfolding circuit and low-pass filter. The basic variant of the FB MI topology is shown in Figure 2-4(a). Its pseudo-DC link output is a rectified sinewave, where an active full bridge unfolding circuit and *CL* filter are placed, to deliver continuous low ripple current to the grid [40].

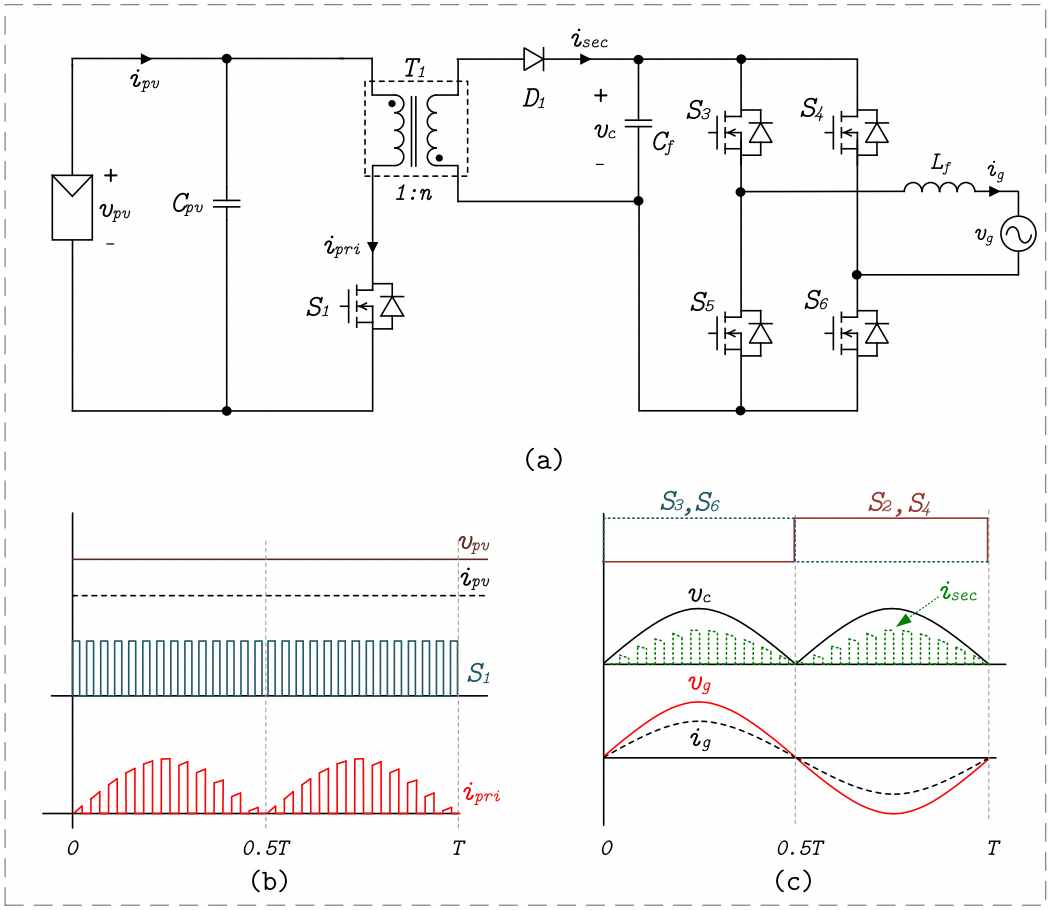


Figure 2-4. single-stage FB MI with active unfolding and *CL* filter
(a) Topology (b) Primary side operating waveforms (c) Secondary side operating waveforms

By switching S_1 at High frequency (HF), the control system shapes the primary current (i_{pri}) into a HF waveform that has a squared-sine envelope (Chapter 3 shows why it is a squared-sine envelope). Then the HF current is transferred through the FB transformer (T_1) to the secondary side as i_{sec}, where it is unfolded by the full bridge circuit, smoothed by a low-pass *CL* filter (formed by C_f and L_f) and fed to the grid (i_g). The full bridge switches S_4 and S_5 conduct positive cycle current, while S_3 and S_6 conduct on the negative cycle. The FB transformer is always used in a step-up configuration, and this considerably helps the control system of the FB MI achieve its voltage amplification objective. The FB MI can be operated in either CCM or DCM. In DCM, the primary switch is subjected to high current peaks. Hence DCM might lead to lower efficiencies [41]. However, control system design in CCM is more complicated, due to the presence of a varying RHP zero on the control (duty cycle) to output (grid current) transfer function [40], [41]. This RHP zero makes it difficult to optimize controller gain and guarantee stability for the whole range of operation [39], [41].

It should be noted that even during CCM operation, the primary current always appears discontinuous. The nature of a FB circuit is such that ampere-turns (MMF) transfer back and forth between windings of the FB transformer, which functions like a coupled-winding-inductor. Given this context, the operation is defined as CCM when the total ampere-turns of primary and secondary windings never dwell at zero [46]. The FB action also generates another problem for this topology. Only energy stored in the magnetizing inductance is transferred to the output as ampere-turns travel back and forth between primary and secondary windings, while energy stored in the leakage inductance does not [42], [43]. All FB transformers, no matter how well constructed, will have non-zero leakage inductance because it is impossible for windings to occupy the same physical space, as needed for lossless energy transfer between them [47].

If no alternate path is provided for the leakage energy, it diverts to the semiconductors, where it resonates with parasitic capacitances to trigger HF ringing and voltage spikes, which then cause Electromagnetic Interference (EMI) issues and threaten semiconductor breakdown. It is therefore necessary to include voltage clamps in the design to limit such voltage spikes and attenuate resonant ringing. On the primary side, an RCD clamp is often used, which consists of a parallel resistor-capacitor branch placed in series with a diode across the primary winding. The leakage energy is then diverted by the diode into the capacitor and subsequently discharged into the resistor. A similar idea is applied on the secondary but using an RC clamp across the secondary diode. By including a resistor, these types of clamps are dissipative and impact both efficiency and ability to scale power ratings. Thus some researchers have been looking into less-dissipative and energy recycling active clamps [48].

Another popular variant of the FB MI is depicted in Figure 2-5. In this configuration, a three-winding transformer is used, with one primary and two secondary windings. This allows for a simpler unfolding circuit because each of the secondary windings receives the ampere-turns transferred from the primary for only half of the line cycle (positive or negative) [41]. Hence, just two switches are needed to activate the appropriate secondary winding, in place of the four-switch full-bridge unfolder included in the first variant. On the positive cycle, S_2 conducts the HF current (i_{sec1}) and connects D_2 to the FB switching cell, whilst on the negative cycle S_3 conducts the HF current (i_{sec2}) and connects D_3 to the FB switching cell. As such, the pseudo-DC link FB voltage is a full sinewave. The fundamental FB MI control tasks remain similar, where the primary current (i_{pri}) is shaped into a HF waveform with a squared-sine envelope, and the transformer still aids with voltage amplification.

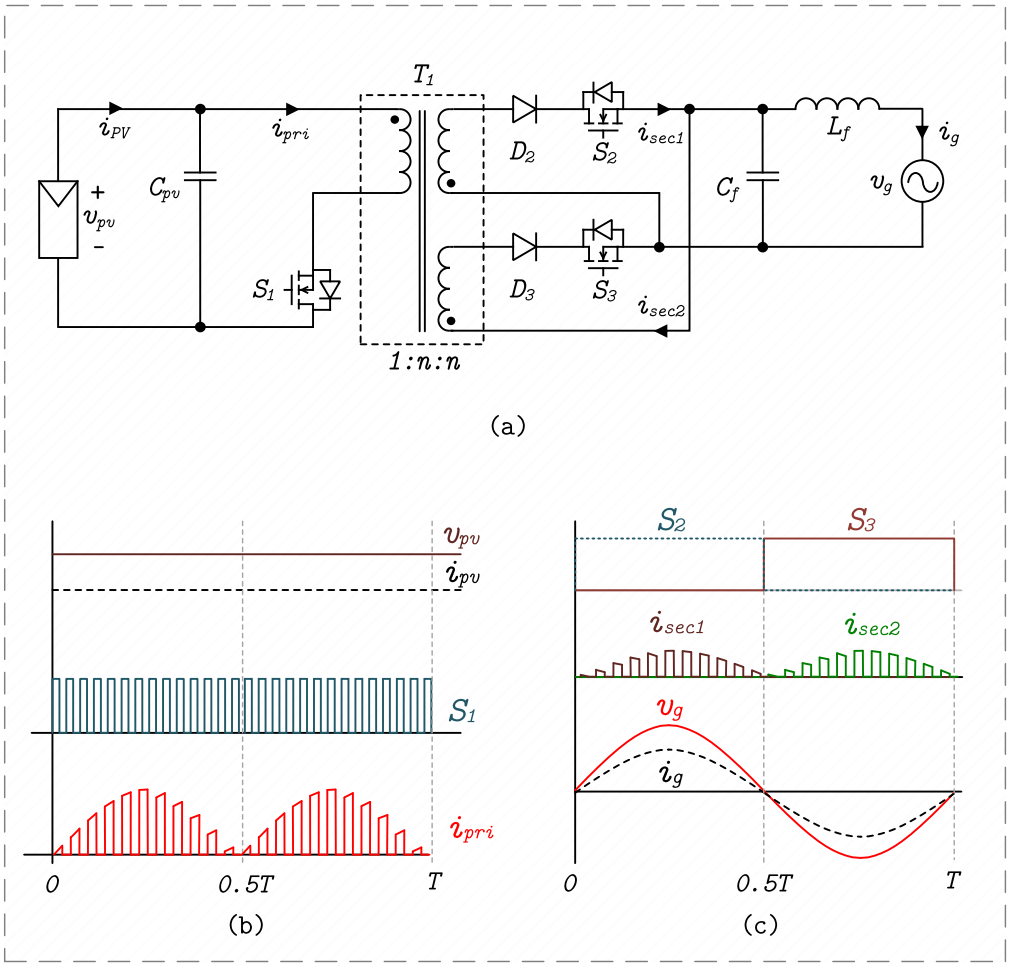


Figure 2-5. Centre-tapped transformer variant of the FB MI
(a) Topology (b) Primary side waveforms (c) Secondary side waveforms

The FB MI variants of Figure 2-4 and Figure 2-5 both use a single HF switch and will subsequently be referred to collectively as non-interleaved FB MI variants. The final variant to be discussed is HF-interleaved variant of the FB MI circuit, presented in Figure 2-6. In this circuit, two non-interleaved FB MIs (of the type in Figure 2-4) are HF-interleaved and share a Pseudo-DC link output where their currents add up for filtering and grid consumption. The advantages of HF-interleaving are that both circuits will share the load equally, while reducing input and pseudo-DC link voltage ripples [38]. Taken individually, each FB MI circuit works as described previously for the non-interleaved circuit in Figure 2-4, but the HF switching commands for S_1 and S_2, must be complementary to avoid transistor shoot through, and are therefore phase-shifted by 180°.

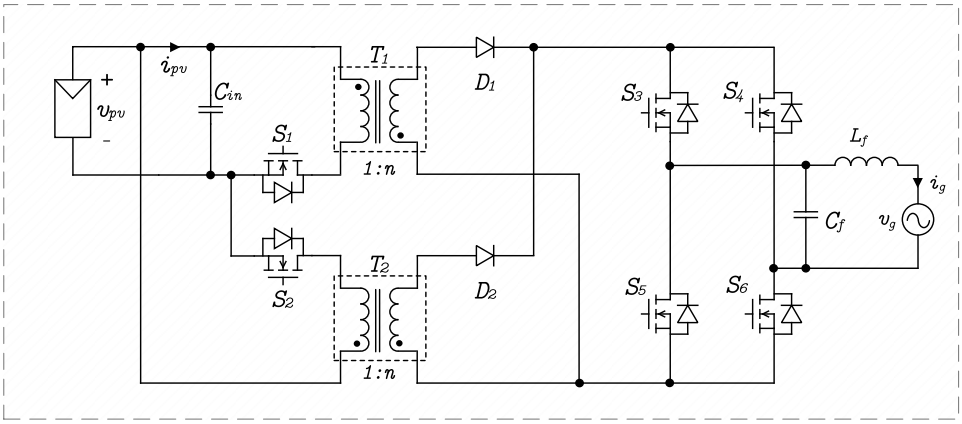


Figure 2-6. HF-Interleaved variant of the FB MI

The HF-interleaved variant of the FB MI is valued because it can double the power rating of a similarly constructed non-interleaved FB MI, and it does so while reducing ripples on the input voltage and output current. However, the power rating boost comes with increased component count and concurrent use of two HF switches. Table 2-2 presents a comparison between the reviewed variants of the FB MI and the ISOMBI topology, which uses LF-interleaving and will be introduced in the next chapter.

Table 2-2. Comparison of FB MI variants, with the ISOMBI.

Topology	**Typical Power Range**	**Semiconductors**			**Magnetic core**	**Copper Winding**	**Caps**	**Total**
		HF Switch	LF Switch	Discrete Diode				
Basic FB MI	160-250	1	4	1	2	3	2	10
Centre tapped variant	160-250	1	2	2	2	4	2	9
Interleaved FB MI	160-500*	2	4	2	3	5	2	13
ISOMBI	160-500*	2[a]	6	0[c]	2	4	2	12

[a] The HF switches do not operate concurrently
[c] The anti-parallel diodes of LF IGBTs are incorporated into the proposed topology
*Theoretical projection from similarly equipped non-interleaved variants

At first glance, comparing the 13-count total of the HF-interleaved FB MI variant with the others seems trivial. However, Magnetic components are often the bulkiest singular components in a power converter and eliminating one can boost power density whilst also reducing costs [13]. The HF-interleaved FB MI uses 3 Magnetic cores with 5 windings, compared to 2 cores and 4 winding maximums for the others and is the only variant that operates two HF switches simultaneously, requiring extra control arrangements. Depending on the control implementation, this could either be additional auxiliary electronics (analog controller) or extra computation (digital controller). With the LF-interleaved ISOMBI, HF switches are not operated simultaneously, keeping a simple control structure, and using integrated magnetic devices avoids the extra magnetic device. The next chapter introduces the ISOMBI and provides a detailed breakdown of its steady-state characteristics and parameter derivations.

Chapter 3 - The Isolated Manitoba Inverter Topology

The proposed Isolated Manitoba Inverter (ISOMBI) topology is a current unfolding FB MI topology which uses LF-interleaving and functionally integrated magnetic devices. This chapter introduces the ISOMBI, depicted in Figure 3-1 with key operating waveforms, by detailing its operating modes, integrated magnetics function, steady-state characteristics, and circuit parameter derivations. Part of the work presented in this chapter is included in [49]

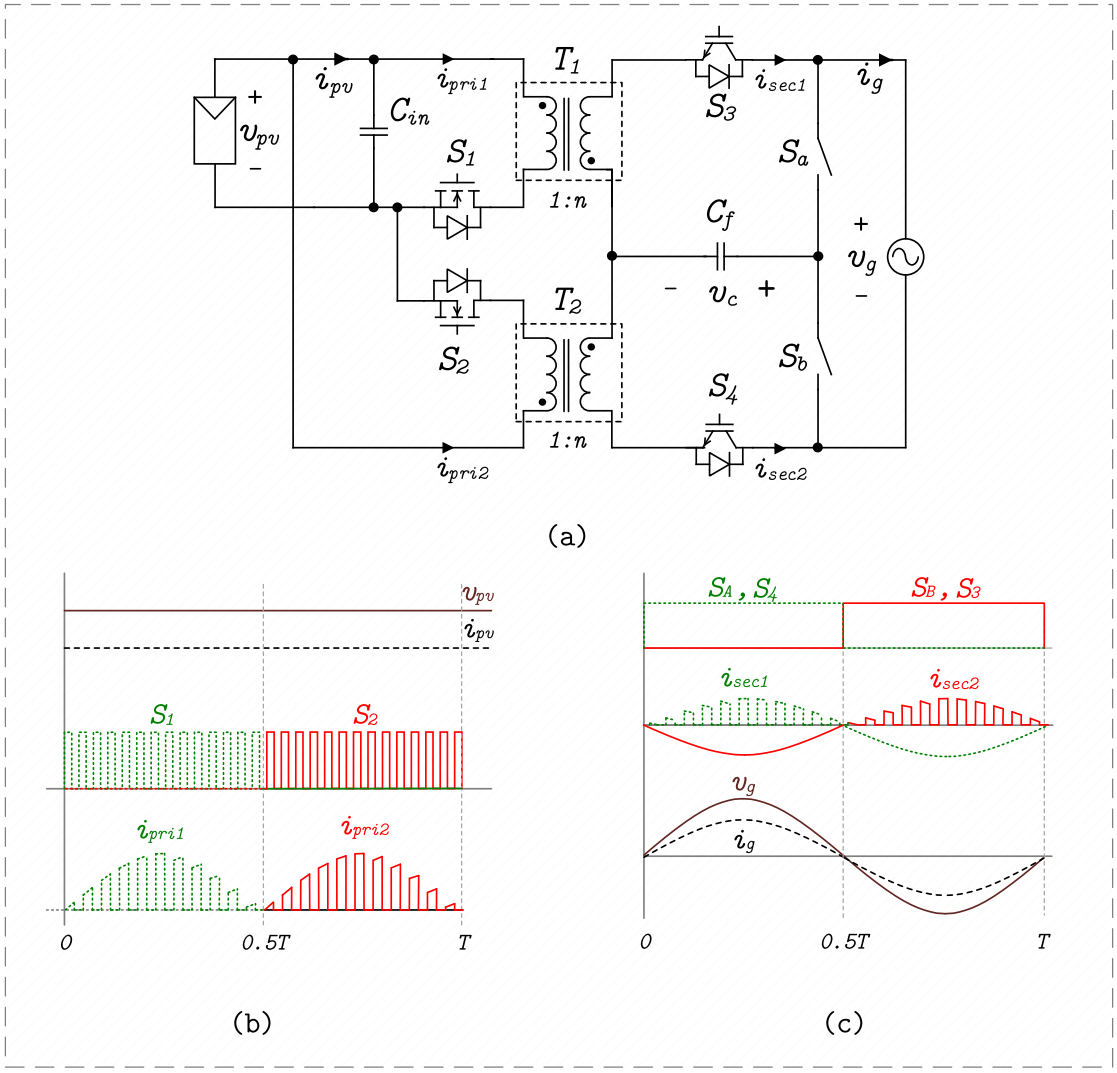


Figure 3-1: Isolated Manitoba Inverter topology (a) Topology (b) Primary waveforms (c) Secondary waveforms

3.1 Operating Principles

The ISOMBI shares some characteristics with the HF-interleaved FB MI of Figure 2-6 by including two FB circuits that share the power processing duties equally. However, since they are LF-interleaved, the ISOMBI operates only one HF switch at any time. This is reflected in the key operating waveforms of Figure 3-1(b), where on the positive cycle, S_1 is the primary HF switch, transferring energy across T_1, while on the negative cycle S_2 is the primary HF switch transferring energy across T_2.

T_1 and T_2 are functionally integrated magnetic devices, which means they perform two distinct functions in the same circuit. From Figure 3-1(c), switches S_a, S_b, S_3 and S_4 are synchronized with the line cycle, leading to the circuit configurations of Figure 3-2, where, on the positive cycle, T_1 and T_2 are FB transformer and grid filter inductor respectively, and on the negative cycle the roles reverse with T_1 as grid inductor and T_2 as FB transformer. This shows in the waveforms of Figure 3-1 (c), where the secondary windings of the magnetic devices conduct HF current and smooth grid current on alternating line cycle periods. In this way the devices integrate the functions of FB transformer and grid inductor into one component.

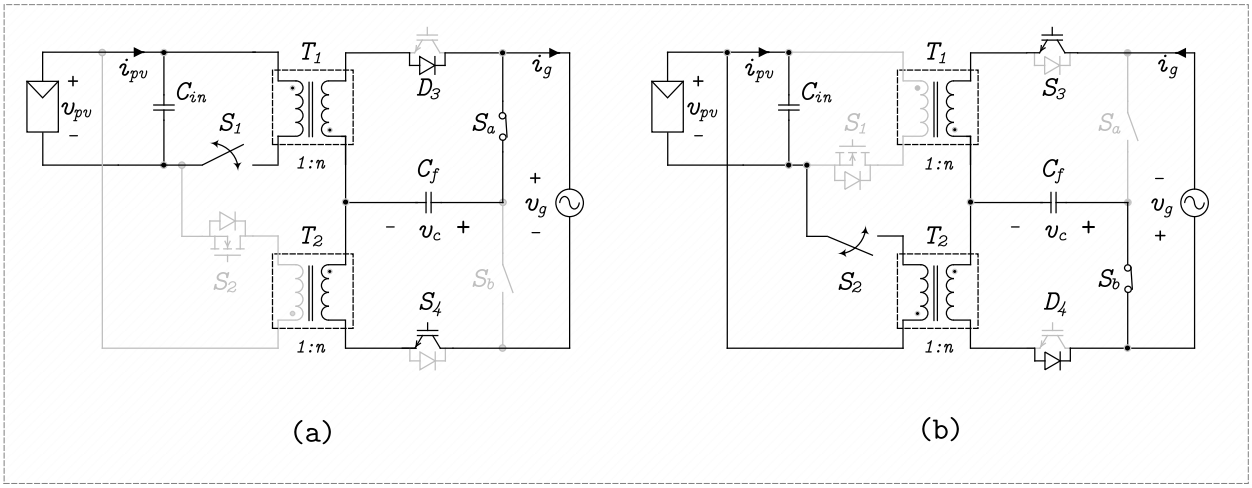


Figure 3-2. ISOMBI circuit configurations in (a) Positive line cycle, and (b) Negative line cycle

3.1.1 Positive line Cycle Operation

From Figure 3-2, the positive line cycle circuit configuration of the ISOMBI can be further reduced to the equivalent circuit of Figure 3-3. In this mode, S_1 is the HF switch and T_1 is the FB transformer, while bidirectional switch S_a is gated ON to connect the line terminal of the grid to the filter cap C_f, and S_4 is gated ON to incorporate the secondary winding of T_2 (denoted L_2 in Figure 3-3) into a *CL* filter with C_f. The second bidirectional switch S_b, and S_2 are gated OFF to disconnect the negative cycle FB circuit during the positive cycle, and finally, S_3 is gated OFF, but its anti-parallel diode (denoted D_3 in Figure 3-3) completes the FB switching cell. Given this configuration, the positive line cycle equivalent circuit is a FB MI whose output is a pseudo-DC link that delivers low ripple current to the grid through a *CL* filter.

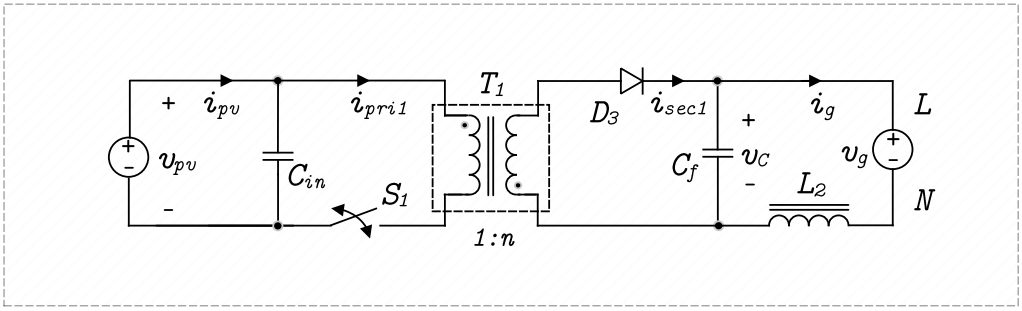


Figure 3-3. ISOMBI Positive line cycle equivalent circuit

3.1.2 Negative line Cycle Operation

From Figure 3-2, the negative line cycle circuit configuration of the ISOMBI can be reduced to the equivalent circuit of Figure 3-4. In this mode, S_2 is the HF switch and T_2 is the FB transformer, while bidirectional switch S_b is gated ON to connect the neutral terminal of the grid to the filter cap C_f, and S_3 is gated ON to incorporate the secondary winding of T_1 (denoted L_1 in Figure 3-4) into a *CL* filter with C_f. The second bidirectional switch S_a, and S_1 are gated OFF to disconnect the positive cycle FB circuit during the negative cycle, and finally, S_4 is gated OFF, but its anti-parallel diode (denoted D_4 in Figure 3-3) completes the FB switching cell. Given this configuration, the negative

line cycle equivalent circuit is also a FB MI, whose output is a pseudo-DC link that delivers low ripple current to the grid through a *CL* filter.

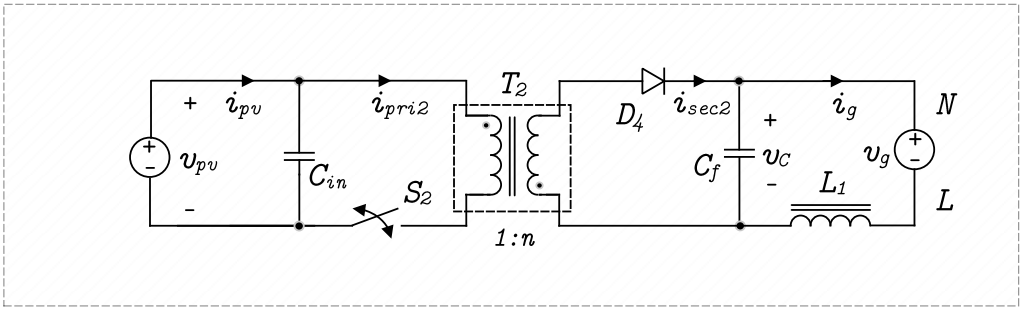


Figure 3-4. Negative line cycle equivalent circuit

3.1.3 Summary of Operating Principles

The positive and negative line cycle equivalent circuits show that the ISOMBI is a FB MI variant, and the functions of FB transformer and grid inductor are integrated into singular components. This is achieved by creating a virtual reference point where the secondary windings of T_1 and T_2 intersect, which becomes the virtual ground reference of the pseudo-DC link voltage. The switches S_a, S_b, S_3 and S_4 are used to maintain the virtual ground, by reconfiguring the output filter based on the line cycle, such that potential difference, v_c, across the pseudo-DC link capacitor (C_f) is always positive, and the output current unfolds into the grid appropriately. On the primary side S_1 and S_2 are the primary HF switches respectively for the positive and negative line cycles. With the described switching sequences, the ISOMBI topology shares power processing responsibility between two HF switches and can potentially match the power ratings of the HF-interleaved topology, but it also keeps the simplicity of operating only one HF switch at a time.

3.1.4 Integrated Magnetics

In FB transformer mode, the magnetic devices do not actually perform transformer action as implied by its name. Proper transformer action involves an instantaneous transfer of energy between primary and secondary, with little or no storage in between [47]. Instead, the FB

transformer functions as a coupled-winding inductor, where multiple windings share the same magnetic core and transfer energy between each other with intermediate magnetic energy storage [47]. Energy from the input is stored in the magnetic core (and airgaps), through the primary winding's ampere-turns (MMF) and later retrieved from the secondary winding's ampere-turns, as controlled by the switching cell [46], [47]. Neither winding claims total control of the ampere-turns, and the device cannot be designated as a singular proper inductor. However, the magnetic core (and airgaps) is exposed to the total ampere-turns ripple and behave like a single inductor core [46]. In this way, the FB transformer device acts as a coupled-winding inductor.

The construction of a FB transformer as a coupled-winding inductor is exploited by the ISOMBI in FB transformer mode. However, the same device is used as grid filter inductor, where the primary winding is completely disconnected, and the secondary winding is statically connected to the circuit. This allows the secondary winding to dictate the total ampere-turns seen by the magnetic core (and airgaps) and behave like a single-winding inductor that stores and retrieves energy from the magnetic domain (core and gaps) through the same winding. Also, since voltage amplification is one of the functions of the MI, the FB transformer is applied with a step-up ratio between primary (input) and secondary (output) windings, meaning that the secondary inductance is a significant multiple (n^2, where n is the turns ratio between primary and secondary) of the primary inductance [50]. This reinforces its capability as grid inductor, because the large secondary inductance is desirable for filtering ripples in the grid current.

Figure 3-5 depicts the functional integration of the magnetics device, the illustration simplifies the ISOMBI operation by only representing the current flows around the magnetics. In Figure 3-5(a), the magnetic device functions as a FB transformer, using both windings to work as a coupled-winding inductor, while Figure 3-5(b) uses only the secondary as a single-winding grid inductor.

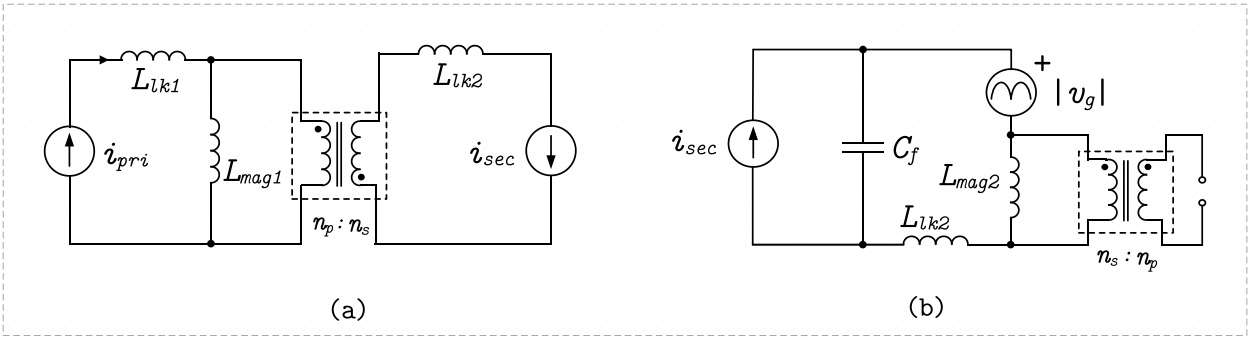


Figure 3-5. Integrated magnetics functionality, (a) as coupled-winding inductor in FB transformer mode, and (b) as single-winding grid filter Inductor

Figure 3-5 also illustrates relevant magnetic parameters. L_{mag1} and L_{mag2} are the respective magnetizing inductance values of the primary and secondary windings, while L_{lk1} and L_{lk2} are the respective leakage inductance values for the primary and secondary windings. In FB transformer mode, L_{mag1} models the magnetic energy storage, while L_{lk1} and L_{lk2} are parasitic elements, which introduce undesired ringing and voltage spikes. In grid inductor mode, however, L_{mag2} represents the single-winding inductance, but this time L_{lk2} is not a parasitic, because it increases the grid filter inductance value (although not significantly, L_{mag2} is typically 100's of μH, while L_{lk2} is few μH) and is good for filtering. In summary, by exploiting the coupled-winding inductor magnetic properties of a FB transformer, the ISOMBI can use the same magnetic device as FB transformer and grid Inductor, thus the component is said to be functionally integrated.

3.2 Steady-State Analysis

In the previous section, the positive and negative line cycle equivalent circuits of the ISOMBI were shown to be analogous. Hence, the FB circuit of Figure 3-6 is presented as a generic equivalent circuit for analyzing the steady-state characteristics of the ISOMBI.

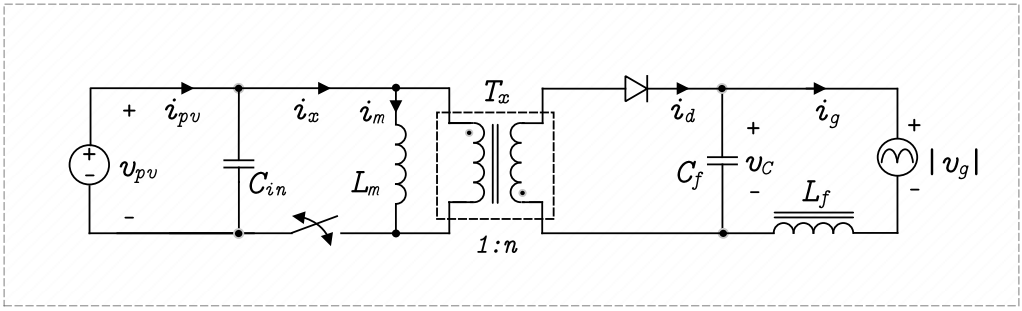


Figure 3-6. ISOMBI steady-state equivalent circuit

In this equivalent circuit, the ideal transformer is placed in parallel with a magnetizing inductor, L_m, which models the non-zero core reluctance (energy storage) of a practical FB transformer [51]. The grid voltage is replaced by an equivalent rectified sinewave v_g, the currents i_{pv}, i_x, i_m, i_d *and* i_g represent the PV current, primary current, magnetizing current, secondary current, and grid current respectively, v_{pv} is the PV voltage, v_c is the pseudo-DC link voltage, n is the turns ratio of FB transformer T_x, C_{in} is the power decoupling capacitor, L_f is the grid filter inductor, and C_f is the pseudo-DC link/filter capacitor. The steady-state analysis includes expressing the duty ratio, magnetizing current and pseudo-DC link voltage in terms of circuit parameters. Two basic assumptions are consistently applied throughout the steady-state analysis of the ISOMBI topology. First, a distinction is to be made between AC-steady-state and quasi-steady-state, followed by a discussion of the operating mode of the topology, described in terms of the magnetizing current.

3.2.1 Steady-State Analysis Assumptions

The MI output is an AC voltage or current, which causes the MI operation to vary according to the utility grid's AC period. However, because the MI is controlled under HF switching, and the switching period (10's of micro-seconds) is very much smaller than the AC line period (10's of milliseconds), the converter can be justifiably said to settle into a "quasi-steady-state" around instants of the AC period that are much larger than the switching period [41]. Similarly, AC-steady-state is observed in the quantities that change on the order of the line cycle and maintain a uniform period. To complete AC-steady-state analysis, it is assumed that the input power decoupling capacitor is large enough that the input, v_{pv}, remains constant over an AC cycle and can be used with other AC-Steady-State variables. In summary, AC-steady-state variables change significantly on the order of the line cycle period, while quasi-steady-state variables change significantly on the order of the switching period.

The second concept examines the operation mode, characterized by the current conducted through the FB transformer. When operated with a constant switching frequency, the FB MI is either in DCM or CCM [38], [40]. In DCM, the total ampere-turns of the FB transformer windings is allowed to reach and/or remain at zero during operation, while in CCM mode the total ampere-turns of FB transformer windings never reach or dwell at zero [46]. However, complete CCM operation over the line cycle is never certain because the FB MI inexorably slips into DCM around zero-crossing instants of the AC line cycle [40], [41], Hence CCM is more appropriately called a "hybrid mode" because it has both CCM and DCM scenarios.

It should be noted that regardless of operating mode, the current in individual windings of the FB transformer is highly discontinuous [46]. This is typical of FB action, where the current transfers back and forth (or "flies-back") between primary and secondary windings at the switching frequency [46]. The operating mode of a FB topology is therefore determined by the total ampere-turns of all windings and not of individual winding currents. The proposed ISOMBI is intended to

be a CCM design and quasi-steady-state principles will be combined with AC-steady-state variables to describe its steady-state characteristics, such as duty ratios, CCM magnetizing current, CCM primary switch current, and CCM pseudo-DC link voltage. Lastly, it is assumed throughout the analysis, that the ISOMBI meets its design objective and delivers only real power via a continuous in-phase sinusoidal grid current.

3.2.2 Pseudo-DC link Voltage

a) Pseudo-DC link Average Voltage (AC-steady-state variable)

The Pseudo-DC link voltage is the output voltage of the ISOMBI circuit. It is assumed that the MI's output AC current is sinusoidal, and in phase with the grid voltage. Hence the MI only sends real power across the filter inductor. Equation 3-1 expresses the inductive power transfer relation.

$$P_o = \frac{|V_c||V_g|}{\omega_o L_f} sin\delta \qquad 3\text{-}1$$

Where: P_o - Real output power

V_c - Peak amplitude of Pseudo-DC link voltage

V_g - Peak amplitude of grid voltage

ω_o - Nominal grid frequency in radians

L_f - Output filter inductance value

δ - Phase difference between pseudo-DC link voltage and grid voltage

The variables V_c, V_g and, ω_o in equation 3-1 are known to be of the same order of magnitude (few 100's). Hence, we can say $sin\delta$ is directly proportional to L_f. Since we know that L_f is small in magnitude (100's of μH), it follows that $sin\delta$, and consequently δ, are also small. This small phase difference means there is minimal voltage drop across L_f, and the average pseudo-DC link voltage is somewhat equal to the grid voltage. Hence:

$$v_c(t) \approx \left|v_g(t)\right| = V_g|sin\ (\omega_o t)| \qquad 3\text{-}2$$

Where: $v_c(t)$ - Average pseudo-DC link voltage

$v_g(t)$ - Instantaneous grid voltage

a) Pseudo-DC link Voltage Ripple

Based on the circuit of Figure 3-6, when the primary switch is in the *ON-state*, the grid current can be expressed by equation 3-3:

$$\left|i_g(t)\right| = C_f \frac{\Delta v_c(t)}{D(t)T_s} \qquad 3\text{-}3$$

Where: $i_g(t)$ - Instantaneous grid current

C_f - Output filter capacitor value (also pseudo-DC link capacitor value)

$D(t)$ - Duty ratio

$\Delta v_c(t)$ - Pseudo-DC link voltage ripple

T_s - Switching period

From this, it is easy to calculate the Pseudo-DC-Link Voltage ripple as:

$$\Delta v_c(t) = \frac{|i_g(t)|D(t)}{f_s C_f} \qquad 3\text{-}4$$

Where: f_s - Switching frequency

3.2.3 Primary Magnetizing Current

a) Average Primary Magnetizing Current (AC-Steady-State variable)

The average magnetizing current represents the amount of energy (average ampere-turns) transferred to the magnetic domain. It can be derived through quasi-steady-state averaging of the Pseudo-DC link capacitor current. Referring to the circuit of Figure 3-6, this is found as:

$$\langle i_c(t)\rangle_T = \frac{-|i_g(t)|D(t)T_s + \left[(-i_m(t)/n) - |i_g(t)|\right]\left(1 - D(t)\right)T_s}{T_s} = 0 \qquad 3\text{-}5$$

Where: $\langle i_c(t)\rangle_T$ - Filter Capacitor Current Averaged over switching period

$i_m(t)$ - Average Primary Magnetizing Current over AC cycle

n - Ratio of Secondary transformer turns to Primary Turns

From equation 3-5, the magnetizing current is calculated as:

$$i_m(t) = \frac{n}{1 - D(t)} |i_g(t)| \quad \text{3-6}$$

b) Magnetizing Current Ripple

Based on the circuit of Figure 3-6, when the primary switch is in the *ON-state*, the DC input voltage can be expressed as:

$$V_{pv} = L_m \frac{\Delta i_m(t)}{D(t) T_s} \quad \text{3-7}$$

Where: V_{pv} - DC input voltage

L_m - Primary magnetizing inductance

$\Delta i_m(t)$ - Magnetizing current ripple

From equation 3-7, it is easy to calculate the magnetizing current ripple as:

$$\Delta i_m(t) = \frac{V_{pv} D(t)}{f_s L_m} \quad \text{3-8}$$

3.2.4 Hybrid Mode Duty Ratios

In the hybrid mode, the system functions in both DCM and CCM, hence duty ratios for both modes are derived as follows. In both cases, the converter is assumed to be lossless.

a) DCM Duty Ratio

In the DCM operating mode, the primary current reaches, and dwells at zero for some portion of the duty cycle as shown in Figure 3-7 below. The average primary switch current is also shown over one switching period T_s.

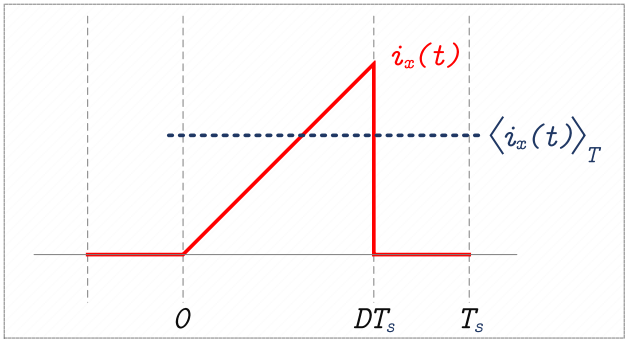


Figure 3-7. DCM current waveform

Assuming the converter operates without losses, and the input capacitor is large enough to keep the input voltage constant, the average AC-steady-state power balance equation is:

$$V_{pv} I_{pv} = V_{rms} I_{rms} \tag{3-9}$$

Where: V_{pv} - Average PV voltage

I_{pv} - Average PV current

V_{rms} - Root Mean Square (RMS) voltage

I_{rms} - RMS current

Similarly, the quasi-steady-state power balance equation is:

$$V_{pv} \langle i_x(t) \rangle_T = v_g(t) i_g(t) = 2 V_{rms} I_{rms} \sin^2 \omega t \tag{3-10}$$

Where: $i_x(t)$ - Instantaneous primary switch Current

$\langle i_x(t) \rangle_T$ - Primary current averaged over switching cycle

ω - Grid frequency in radians

Combining equations 3-9 and 3-10, gives the primary current in equation 3-11, which shows that the primary current is of squared-sine shape (also applies to CCM, where the quasi-steady-state power balance is the same).

$$\langle i_x(t) \rangle_T = 2 I_{pv} \sin^2(\omega t) = \frac{2 V_{rms} I_{rms}}{V_{pv}} \sin^2(\omega t) \tag{3-11}$$

The average primary current over one DCM switching period can also be calculated from Figure 3-7 as:

$$\langle i_x(t)\rangle_T = \int_0^{T_s} i_x(t)dt = \frac{1}{2}\frac{(D(t)T_s)\Delta i_x(t)}{T_s} \quad \text{3-12}$$

Where: $D(t)$ - DCM duty Cycle

$\Delta i_x(t)$ - DCM primary current ripple

Based on the circuit of Figure 3-6, When the primary switch is in the *ON-State*, the primary magnetizing inductor voltage and primary current ripple can be written as:

$$v_L(t) = L_m\frac{\Delta i_x(t)}{D(t)T_s} = V_{pv} \quad \rightarrow \quad \Delta i_x = \frac{D(t)\cdot V_{pv}}{L_m f_s} \quad \text{3-13}$$

Finally, combining equations 3-11, 3-12, and 3-13 gives the DCM duty ratio as:

$$D_{DCM}(t) = 2\cdot\sqrt{\frac{V_{rms}I_{rms}L_m f_s}{V_{pv}^2}}\,|\sin(\omega t)| \quad \text{3-14}$$

b) CCM Duty Ratio

In CCM, the duty ratio is derived through quasi-steady-state averaging of the magnetizing inductor voltage. Referring to the circuit of Figure 3-6, this is found as:

$$\langle v_L(t)\rangle_T = \frac{V_{pv}D(t)T_s + (-|v_g(t)|/n)(1-D(t))T}{T_s} = 0 \quad \text{3-15}$$

Where: $\langle v_L(t)\rangle_T$ - Average magnetizing inductor current over switching period

$D(t)$ - CCM duty cycle

The resulting CCM duty cycle is found from 3-15 as:

$$D_{CCM}(t) = \frac{|v_g(t)|}{nV_{pv} + |v_g(t)|} \quad \text{3-16}$$

3.2.5 Peak Primary Current

The peak primary current is used to assess the current stress on the primary switch, and it can be obtained using the magnetizing current. Assuming the converter operates in CCM, the peak primary current is obtained by adding the peak value of the average magnetizing current (equation 3-6) to half of the peak ripple component (equation 3-8). This is given as:

$$I_{sw,peak} = \frac{n}{1 - D_{pk}} \left| i_{g,pk} \right| + \frac{V_{pv}}{2 L_m f_s} D_{pk} \qquad 3\text{-}17$$

3.3 Component Parameter Derivations

3.3.1 Primary Magnetizing Inductance

The primary magnetizing inductance (L_m) is a vital parameter in a FB MI. Based on equation 3-17, a large L_m reduces magnetizing current ripple, and therefore reduces the peak current burdens of the primary switch. but a large L_m also increases the transformer size, because inductance is a factor of n^2 times related to the number of turns [50]. The system should be designed for acceptable primary switch current stress based on equation 3-17, but this is not the only circuit consideration. Due to hybrid mode operation, there exists a critical inductance value, below which the MI will never even reach CCM. Hence, if CCM operation is desired for its lower current stresses [41], it is necessary to determine the critical inductance. If the critical inductance is significantly exceeded, the CCM operation is nearly pure, except for negligible instances around the zero-crossing where insufficient ampere-turns (MMF) prevent it.

a) Critical Inductance Value

The critical inductance value is obtained by equating the DCM and CCM duty ratios (equations 3-14 and 3-16) and is given by:

$$L_{mc} = \frac{V_{pv}^2}{4 V_{rms} I_{rms} f_s \left[\left(n V_{pv} / \sqrt{2} V_{rms} \right) + 1 \right]^2} \qquad 3\text{-}18$$

3.3.2 Input Decoupling Capacitor

The input decoupling capacitor is sized to buffer energy (or power) and limit the input voltage ripple. For this analysis, it is assumed that ripple component buffers instantaneously, an amount of power equal to the average output power. The instantaneous energy stored in the capacitor is given by equation 3-19, expressed as:

$$E_c = \frac{1}{2} C_{in} v_c^2(t) \quad \text{3-19}$$

Where: E_c - Instantaneous energy stored in the decoupling capacitor

C_{in} - Decoupling capacitor value

$v_c(t)$ - Instantaneous voltage of the capacitor

Then the instantaneous power delivered by the capacitor is obtained by taking the derivative of its energy in equation 3-20.

$$P_c(t) = \frac{dE_c(t)}{dt} = \frac{1}{2} C_{in} \frac{dv_c^2(t)}{dt} \quad \text{3-20}$$

Where: $P_c(t)$ - Instantaneous power delivered by the capacitor

Next, the capacitor voltage $v_c(t)$ is broken down to its two components, namely the average voltage and the time-varying 2nd order voltage, This reveals similar components in the instantaneous power, as expressed by equation 3-21.

$$P_c + \Delta p_c(t) = \frac{1}{2} C_{in} \frac{d}{dt} (V_c + 2V_c \Delta v_c + \Delta v_c^2(t)) \quad \text{3-21}$$

Where: P_c - Average power supplied by the capacitor

$\Delta p_c(t)$ - Instantaneous power supplied by the capacitor due to the 2nd order ripple component

V_c - Average capacitor voltage

$\Delta v_c(t)$ - Ripple component of the capacitor voltage

The ripple component of the power is then isolated from equation 3-21, by ignoring higher order terms (Δv_c is 2nd order and small, hence Δv_c^2 is 4th order and much smaller, hence negligible) and average terms to get Δp_c in equation 3-22.

$$\Delta p_c = C_{in} V_c \frac{d}{dt}(\Delta v_c) \quad 3\text{-}22$$

In the Laplace domain, $\Delta p_c(s)$ is given as (to eliminate the time dependence for simplicity):

$$\Delta p_c(s) = sC_{in} V_c \Delta v_c(s) \quad 3\text{-}23$$

Where: $s = j(2\omega_o)$

And finally, by equating 3-23 to $V_{rms} I_{rms}$, which is the average output power. The decoupling capacitor value is calculated and given by 3-24.

$$C_{in} = \frac{V_{rms} I_{rms}}{2\omega_o V_c \Delta v_c} \quad 3\text{-}24$$

3.3.3 Output *CL* filter

The Output *CL* filter is a low-pass filter used to stifle high frequency harmonics in the grid current, for complying with TDD requirements (<5% per IEEE 519). However, its use may also induce phase delays between the current source output of the FB MI and the voltage source grid. Also, the *CL* filter exhibits a resonance (infinite gain) at its cut-off frequency, which may amplify any harmonics found there. This makes resonance peak damping and quality factor optimization worthy research goals. However, this thesis focuses only on proving the basic functionality of the ISOMBI as a MI. Hence the *CL* filter design only targets high frequency harmonic reduction and managing phase delays to prevent excess power Factor (PF) deviations.

High frequency harmonic distortion factor (hence TDD) is reduced by appropriately setting the filter cut-off above the grid current control system bandwidth, but well below the switching frequency, The *CL* filter exhibits a -40 dB roll off rate after its cut-off. Hence this strategy allows the grid current compensator to process desired low frequency components, while switching ripple components are highly attenuated. Phase delays are reduced by managing reactive power. Leading PF is observed when too much reactive power is sent to the grid, and lagging PF is

caused when too much reactive power is drawn from the grid. To meet PF targets, the *CL* filter is designed to manage reactive power at grid extremes as summarized in Table 3-1.

Table 3-1. PF requirements summary based on [28], [52]

	Apparent Power (S)	**Real Power (P)**	**Reactive Power (Q)**	**Phase angle (ϕ)**
0.9 Lead	$0.20\ p.u.$	$0.18\ p.u.$	$-0.0872\ p.u.$	$25.84°$
0.9 Lag	$1.00\ p.u.$	$0.90\ p.u.$	$0.4359\ p.u.$	$-25.84°$

PF limits in Table 3-1 is based on California's Rule 21 guidelines for grid connected generators, which include residential solar installations [28]. Figure 3-8 depicts the real and reactive power flows used in the analysis, which covers a range from 20% to full rated power as recommended in [52]. It is assumed throughout that the ISOMBI is an ideal current source that neither produces nor consumes reactive power, hence, all the reactive power in the circuit is produced by the filter capacitor, absorbed by the filter inductor, and balanced by the utility grid [52].

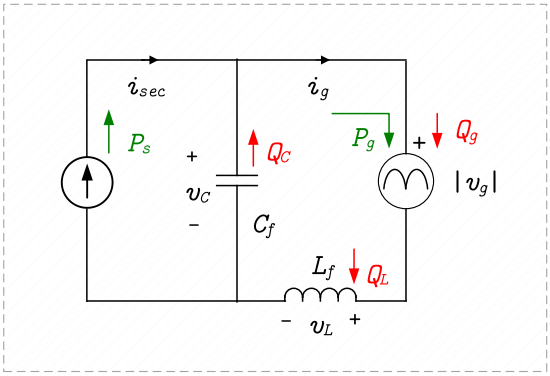


Figure 3-8. Real and reactive power flow diagram, arrows pointing up indicate supply, arrows pointing down indicate dissipation/absorption.

The following analysis is based on Figure 3-8, and used to derive filter parameters based on PF standards of Table 3-1. The analysis is completed in per unit for simplicity and is based on the methodology prescribed in [52].

$$Q_g = Q_L - Q_C \quad \text{3-25}$$

Where: Q_g - Reactive power sent to the grid

Q_L - Reactive power absorbed by the inductor

Q_C - Reactive power produced by capacitor

The reactive power absorbed by the inductor is given as:

$$Q_L = I_g^2 X_{Lf} = I_g^2 L_{fn} \quad \text{3-26}$$

Where: I_g - RMS grid current in per unit

X_{Lf} - Filter inductor reactance in per unit

L_{fn} - Filter inductance in per unit

The reactive power supplied by the capacitor and its voltage are given as:

$$Q_C = \frac{V_C^2}{X_c} = V_C^2 C_{fn} \quad \text{3-27}$$

Where: V_C - RMS capacitor voltage in per unit

X_c - Filter capacitor reactance in per unit

C_{fn} - Filter capacitor value in per unit

$$V_C = V_g - V_L = 1 - jI_g \omega_n L_{fn} \quad \text{3-28}$$

Where: V_g - Grid voltage in per unit

V_L - Normalized voltage drop across inductor in per unit

ω_n - Normalized grid frequency in per unit

Excess PF lead is caused when too much reactive power sent to the grid, hence this condition limits the maximum filter capacitance. In the absence of any inductance, All the reactive power generated by the capacitor is sent to the grid, and the maximum C_{fn}, can be obtained by solving equations 3-25, 3-27, 3-28 using leading PF parameters from Table 3-1, $L_{fn} = 0\ p.u.$, and $I_g = 0.2\ p.u.$, to obtain $C_{fn} = 0.0872\ p.u.$ It is noted that the leading PF case is most difficult to meet when the MI operates at 20% ratings (hence why $I_g = 0.2\ p.u.$) [52]. As inductance gets added in

the circuit, however, some of the capacitor's reactive power is absorbed by the inductor, and as a result, the maximum C_{fn} can increase, such that the PF standard is maintained.

Similarly, excess PF lag is caused when too much reactive power is drawn from the grid, hence this condition limits the maximum amount of filter inductance. When there is no capacitance, All the reactive power absorbed by the Inductor comes from the grid, and the maximum L_{fn}, can be obtained by solving equations 3-25, 3-26, 3-27, and 3-28, using lagging PF parameters from Table 3-1, $C_{fn} = 0\ p.u.$, and $I_g = 1.0\ p.u.$, to obtain $L_{fn} = 0.4359\ p.u.$ It is noted that the lagging PF case is most difficult to meet when the MI operates at full ratings (hence why $I_g = 1\ p.u.$) [52]. As capacitance gets added to the circuit, however, some of the Inductor's reactive power is supplied from the capacitor, and as a result, the maximum L_{fn} can increase, such that the PF standard is maintained. These principles are applied in chapter 5, where an acceptable region of parameters is plotted and used to design the *CL* filter parameters.

3.4 Chapter summary

This chapter introduced the isolated Manitoba inverter topology, which is a single-stage, FB topology suitable for AC module MIs. Its operating principles were outlined for positive and negative cycles of the utility grid; the use of multi-function integrated magnetic devices was described; steady-state analysis derived key expressions for Pseudo-DC link voltage, primary magnetizing current, CCM and DCM duty ratios and the peak primary current; Finally, component parameter derivations for sizing the primary magnetizing inductance, input (passive) decoupling capacitor, and output *CL* filter were shown. The simplification of the proposed topology into a FB MI variant circuit was vital to the steady-state analysis and deriving component parameters. Having fully characterized the ISOMBI topology for MI application, and detailing its principles, the next chapter follows with discussions of a compatible control system.

Chapter 4 - The Isolated Manitoba Inverter Control System

The preceding chapter disclosed the operating principles and characteristics of the ISOMBI, culminating in a common steady-state FB equivalent circuit for both positive and negative line cycle periods of the utility voltage. In this chapter, a compatible control system is detailed, which ensures that the ISOMBI delivers proposed steady-state expectations and can work as an AC module MI. Figure 4-1 depicts the proposed ISOMBI control system using the equivalent circuit established in chapter 3. The control objectives are to ensure MPPT, as well as shaping (sinusoidal) and synchronizing the output AC current with the utility grid voltage. Figure 4-1 identifies the main control loops responsible for meeting both objectives.

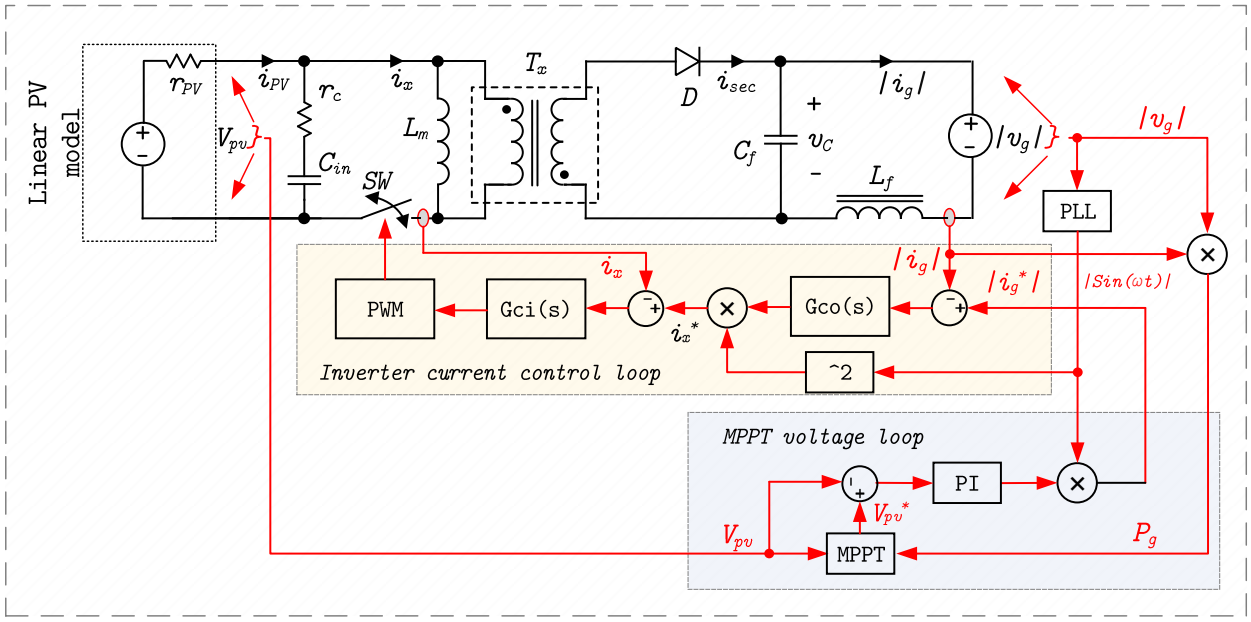


Figure 4-1. ISOMBI control system

The outer MPPT voltage loop regulates the PV voltage, by dictating the output AC current amplitude (consequently, power) to an inner inverter current control loop which regulates, shapes, and synchronizes the output AC current with the utility grid. Only the inverter current control loop is investigated by this thesis to demonstrate the ISOMBI's applicability as a single-stage and

single-phase MI. Upon proving this, single-phase MPPT techniques like the one proposed in [53] can be added on in future research. This thesis presents a unique dual control loop strategy for regulating single-stage FB MI output AC current.

4.1 Inverter Current Loop Overview

Two main challenges arise in the inverter current control loop design. First, the topology presents a fourth-order dynamic system, evidenced by the presence of four energy storage elements in Figure 4-1. Then there is a varying Right-Half-Plane (RHP) zero in the control (duty) to output (grid current) Transfer Function (TF) of the system. Some researchers resolve the fourth-order modelling challenge by approximating the topology using a second-order equivalent circuit (Figure 4-2) which ignores the *CL* filter dynamics, and either the primary or secondary current is controlled. The varying RHP zero proves more difficult to deal with because it imposes limits on the controller gain, such that the minimum (worst-case) RHP zero, which occurs at the peak of the grid voltage must be accommodated, leading the system to provide low gain, low bandwidth, and poor tracking at low instantaneous voltage levels [41].

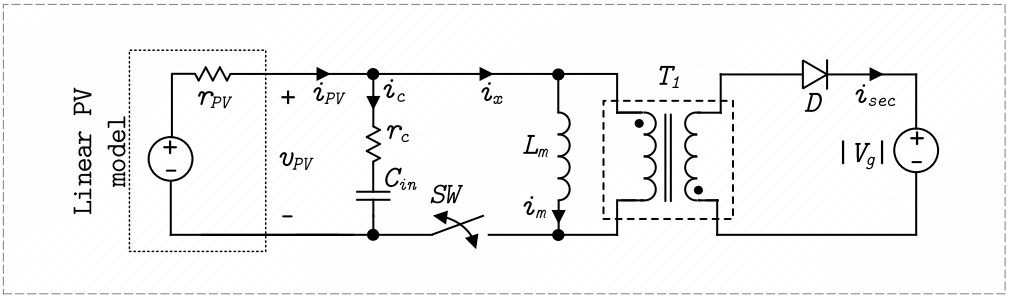


Figure 4-2. Approximate second-order equivalent circuit for small signal modelling

Some researchers have bypassed the RHP zero problem by controlling the primary current only, because the control (duty) to output (primary current) TF does not have a RHP zero [39], [41]. In this case, it is demonstrated that the dynamic response between the primary current and secondary current has no substantial phase delay, hence the secondary current can be indirectly

regulated through the primary current compensator [39]. However, the second order approximation used in designing the primary current compensator neglects the *CL* filter dynamics, and treats the grid current as if it is equal to the secondary current, so with no further regulation of the grid current like in [39], [41], oscillations may arise [38]. This happens because *CL* filter dynamics have been ignored by the control system [38] and to ensure proper stability, the full fourth order model should be considered.

The ISOMBI inverter current control loop presented in Figure 4-1, adopts a dual control loop strategy, where an inner loop regulates the primary current (because controlling the primary current avoids the effects of the RHP zero) while the outer loop regulates the grid current to account for *CL* filter dynamics. the inner loop compensator design is based on the second-order model of Figure 4-2, while the outer loop design extends the model to the full fourth order system. An approximation made between the inner loop and outer loop designs is that due to the insignificant phase difference (at frequencies of interest) between primary and secondary currents, the secondary current is simply a scaled version of the primary current (this bypasses the RHP zero) and the outer loop TF is approximated only by the *CL* filter. The small-signal dynamic modelling presented in the next section is used to design the control system.

4.2 Small-signal Model and Transfer functions

Small-signal modelling is used to generate transfer functions that describe the dynamic behavior of the MI. In the proposed ISOMBI control system, interests lie in how duty cycle (control input) changes affect the primary current (inner loop output) and in turn, how primary current (outer loop input) changes affect the grid current (outer loop output). The following analyses demonstrate that the duty-to-primary-current TF is easily derived by modelling the duty-to-magnetizing-current TF and the primary-current-to-grid-current TF is primarily influenced by the output *CL* filter. Both structures are deemed valuable for designing and evaluating closed loop compensators.

The small signal model for the duty-to-primary-current is based on the second-order equivalent circuit of Figure 4-2, which excludes the *CL* filter. While the primary-current-to-grid-current extends the model to include the filter dynamics. The effect of the RHP zero would normally be included in the primary-current-to-secondary-current TF, however, the dual loop compensation structure will be designed to ensure the inner loop regulates the primary current much faster (about 10 times or more) than the outer loop BW. It will also be shown that an insignificant phase shift occurs between the primary and secondary currents at the frequencies of interest and within the Bandwidth (BW) of the outer loop.

Combining a fast-responding inner loop (relative to the outer loop) with the negligible phase shift between primary and secondary currents (within outer loop BW), it is reasonable to assume that the dynamics of the primary-current-to-secondary-current TF has negligible impact on the primary-current-to-grid-current dynamics. Hence, the primary-current-to-grid-current TF can be approximated solely by the *CL* filter dynamics and transformer turns ratio. Therefore, the varying RHP zero is bypassed just like in [39], [41], but the grid current is not left uncompensated. The

following subsections detail the small-signal model derivation, which is based on the perturb and linearize techniques detailed in [51].

4.2.1 Inner Loop: Duty-to-primary-current TF

In Quasi-steady-state, the primary current is the same as the magnetizing current when the primary switch is in the *ON-state* and is given as:

$$i_x(t) = D(t) \cdot i_m(t) \tag{4-1}$$

Where: $i_x(t)$ - Primary current

$D(t)$ - Duty cycle

$i_m(t)$ - Magnetizing current

Applying a small-signal perturbation to all the time-varying quantities gives:

$$I_x(t) + \tilde{\imath}_x(t) = D(t)I_m + D(t)i_m(t) + \tilde{d}(t)I_m + \tilde{d}(t)\tilde{\imath}_m(t) \tag{4-2}$$

Where: $I_x(t)$ - Large signal primary current

$\tilde{\imath}_x(t)$ - Small-signal primary current

$I_m(t)$ - Large-signal magnetizing current

$\tilde{\imath}_m(t)$ - Small-signal magnetizing current

$D(t)$ - Large-signal duty cycle

$\tilde{d}(t)$ - Small-signal duty cycle

Collecting the small-signal terms and linearizing the results and expressed in the frequency domain, the duty-to-primary-current TF is found as:

$$\frac{\tilde{\imath}_x(s)}{\tilde{d}(s)} = D\frac{\tilde{\imath}_m(s)}{\tilde{d}(s)} + I_m \tag{4-3}$$

Equation 4-3 reveals that the duty-to-primary-current TF is a function of the duty to magnetizing current TF. This makes sense because the magnetizing inductance represents the energy storage of the FB transformer, hence is responsible for the dynamic behavior of the primary current. The expression $\tilde{\imath}_m(s)/\tilde{d}(s)$ is then derived by perturbing and linearizing the magnetizing inductor's dynamic expression, given by equation 4-4. The analysis follows below:

$$L_m \frac{d(I_m + \tilde{\imath}_m)}{dt} = \left(D + \tilde{d}(t)\right)\left[V_{pv} + \tilde{v}_{pv}(t)\right] - [D' - \tilde{d}(t)](-|V_g|/n) \quad \text{4-4}$$

Where: L_m - Magnetizing Inductance

V_{pv} - Large signal PV DC input voltage

$\tilde{v}_{pv}$ - Small-signal PV DC input voltage

D' - 1 – duty cycle (complement of duty cycle)

V_g - Instantaneous grid voltage

n - FB Transformer turns ratio

Collecting the small-signal terms, linearizing, and expressing equation 4-4 in the frequency domain gives:

$$sL_m\tilde{\imath}_m(s) = D\tilde{v}_{pv}(s) + \tilde{d}(s)(V_{pv} + |V_g|/n) \quad \text{4-5}$$

And applying KCL at the input node gives, and substituting for $i_x(s)$ from equation 4-3 yields:

$$\tilde{\imath}_{pv}(s) = \tilde{\imath}_c(s) + \tilde{\imath}_x(s) = i_c(s) + D\tilde{\imath}_m(s) + \tilde{d}(s)I_m \quad \text{4-6}$$

$\tilde{\imath}_{pv}(s)$ is given by $-\tilde{v}_{pv}(s)/r_{pv}$ according to the small-signal PV model derived in [54] and $\tilde{\imath}_c(s) = sC_{in}v_c(s)$, based on the frequency domain impedance of the capacitor. Applying KVL to the input loop then gives $\tilde{v}_c(s) = \tilde{v}_{pv}(s) - sC_{in}r_c v_c(s)$. Hence $\tilde{\imath}_c(s) = (sC_{in}\tilde{v}_{pv}(s))/(1 + sr_cC_{in})$. It follows then, that by substituting $\tilde{\imath}_{pv}(s) = -\tilde{v}_{pv}/r_{pv}$, and $\tilde{\imath}_c(s) = (sC_{in}\tilde{v}_{pv}(s))/(1 + sr_cC_{in})$ in equation 4-6 above, that $\tilde{v}_{pv}$ can be expressed as:

$$\tilde{v}_{pv}(s) = \frac{D\tilde{\imath}_m(s) + \tilde{d}(s)I_m}{(1/r_{pv}) + (sC_{in}\tilde{v}_{pv}(s))/(1 + sr_cC_{in})} \quad \text{4-7}$$

Where: r_{pv} - PV dynamic model resistance (linearized at MPP)

r_c - Input Capacitor Equivalent Series Resistance (ESR)

C_{in} - Input Capacitance

Finally, by combining equations 4-5 and 4-7 and simplifying, the duty-to-magnetizing current TF is expressed as:

$$\frac{\tilde{\imath}_m(s)}{\tilde{d}(s)} = \frac{s\left[\left(r_c + r_{pv}\right)C_{in}\left|V_g\right|/(nD) - Dr_{pv}r_cC_{in}I_m\right] + \left[\left|V_g\right|/(nD) - DI_mr_{pv}\right]}{s^2\left(r_c + r_{pv}\right)L_mC_{in} + s\left(L_m + D^2r_cr_{pv}C_{in}\right) + D^2r_{pv}} \quad 4\text{-}8$$

Then combining equations 4-3 and 4-8 gives the duty-to-primary-current TF as:

$$\frac{\tilde{\imath}_x(s)}{\tilde{d}(s)} = D\left(\frac{s\left[\left(r_c + r_{pv}\right)C_{in}\left|V_g\right|/(nD) - Dr_{pv}r_cC_{in}I_m\right] + \left[\left|V_g\right|/(nD) - DI_mr_{pv}\right]}{s^2\left(r_c + r_{pv}\right)L_mC_{in} + s\left(L_m + D^2r_cr_{pv}C_{in}\right) + D^2r_{pv}}\right) + I_m \quad 4\text{-}9$$

It is noted that the perturb and linearize method is similar to [39] and the results obtained are identical. The derived analytical model of equation 4-9 will later be calculated in MATLAB and compared with a PLECS switching circuit model, prior to being used for compensator design.

4.2.2 Outer Loop: Primary-current-to-grid-current TF

The small-signal model of the duty-to-primary-current TF was derived based on the second order circuit. That model satisfactorily captures the circuit dynamics needed to design the inner loop compensator. However, the outer loop grid current compensator requires that the dynamics of the *CL* filter be modelled in its design, and the circuit in Figure 4-3 shows that the secondary-current-to-grid-current TF is solely dependent on the *CL* filter dynamics.

The filter inductance is modelled in series with its ESR, which helps with damping and is a practical consideration, given the copper winding of the magnetic device. Besides this, other sources of damping may include the capacitor ESR and transistor resistance, but these are not characterized, hence not modelled. It will later be proved (during compensator design), that there is minimal phase-shift in the primary-current-to-secondary current TF at frequencies of interest, hence the *CL* filter dynamic is sufficient for the outer loop compensator design.

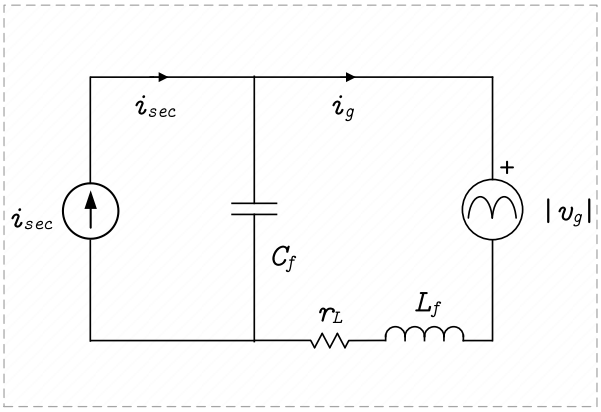


Figure 4-3. secondary-current-to-grid-current dynamic model

The derivation of the secondary-current-to-grid-current TF follows from Figure 4-3. Applying current division to Figure 4-3 with small-signal perturbation of time-varying quantities gives:

$$I_g + \tilde{\imath}_g(s) = (I_{sec} + \tilde{\imath}_{sec}(s)) \times \frac{1/sC_f}{(1/sC_f) + r_L + sL_f} \quad 4\text{-}10$$

Where: C_f - Filter Capacitance

L_f - Filter Inductance

r_L - Filter Inductor ESR

The small signal relationship between grid and secondary currents, can then be expressed as:

$$\frac{\tilde{\imath}_g(s)}{\tilde{\imath}_{sec}(s)} = \frac{1}{1 + sr_L C_f + s^2 C_f L_f} \quad 4\text{-}11$$

The *CL* filter dynamic expression of equation 4-11, shows quadratic pole response, i.e., 0 dB gain up to the resonant frequency, where the gain is then equal to the filter quality factor, Q. Beyond the resonant frequency, the response rolls off with a -40dB decade [51]. The resonance frequency is given as:

$$\omega_r = \frac{1}{\sqrt{L_f C_f}} \quad 4\text{-}12$$

Where: ω_r - Resonant Frequency

And the Quality factor is calculated as:

$$Q = \frac{1}{r_L}\sqrt{\frac{L_f}{C_f}} \quad 4\text{-}13$$

Where: Q - Quality Factor

The primary-current-to-grid-current TF is given by:

$$\frac{\tilde{\imath}_g(s)}{\tilde{\imath}_x(s)} = \frac{\tilde{\imath}_g(s)}{\tilde{\imath}_{sec}(s)} \times \frac{\tilde{\imath}_{sec}(s)}{\tilde{\imath}_x(s)} \quad 4\text{-}14$$

However, around 120 Hz (which is the frequency of the rectified grid current) the expression for $\tilde{\imath}_{sec}(s)/\tilde{\imath}_x(s)$ can be shown to induce minimal phase delay, and the magnitude scaling is the same as the FB transformer turns ratio. Hence the outer loop transfer function can be approximated by the filter dynamic equation scaled by the FB transformer turns (equation 4-15), provided that the outer loop Bandwidth (BW) is limited to a range in which $\tilde{\imath}_{sec}(s)/\tilde{\imath}_x(s)$ maintain low phase difference, and both the filter resonance frequency and the inner loop BW are much higher than the outer loop BW (factor of 10 or more). The next section applies the small-signal models derived here to design compensator structures.

$$\frac{\tilde{\imath}_g(s)}{\tilde{\imath}_x(s)} \approx \frac{\tilde{\imath}_g(s)}{\tilde{\imath}_{sec}(s)} = \frac{n}{1 + sr_L C_f + s^2 C_f L_f} \quad 4\text{-}15$$

4.3 Compensator Design

It is necessary to specify circuit parameters for compensator design. Table 4-1 summarizes the prototype circuit parameters, calculated based on the derivations of chapter 3 and further used in chapter 5. Both the inner and outer loop compensators will be using Bode plots. The prototype specifications are based on the SunPower SPR-E19-310-COM [55], whose specifications are also summarized in Table 4-1. The compensator designs assume a working MPPT, such that the PV is always operating at the maximum power voltage. The analysis also takes place around the peak instantaneous output power (peak grid voltage) which is where the

MI experiences its lowest damping characteristic [38] and is where the maximum system BW is set.

Table 4-1. ISOMBI prototype specifications and circuit parameters

Prototype specs			**Circuit parameters**			**Solar panel electrical data**		
V_{pv}	30 to 70	V	L_m	61.2	μH	P_{mp}	310	W
V_g	120	V_{rms}	n	4	-	V_{mp}	54.7	V_{DC}
f_o	60	Hz	C_{in}	5400	mF	I_{mp}	5.67	A_{DC}
f_s	100	kHz	r_c	0.05	Ω	V_{oc}	64.4	V_{DC}
P_{rated}	390	W	C_f	2.2	μF	I_{sc}	6.05	A_{DC}
$P_{nominal}$	310	W	L_f	979	μH			

To validate the duty-to-primary-current small signal equation 4-9, it is evaluated in MATLAB and compared with the PLECS circuit simulation model. Both models use the MI specifications and parameters in Table 4-1. Figure 4-4 shows the result of the comparison. Since there is an agreement between the analytical expression and the switching circuit models, the inner loop compensator design proceeds using the analytical expression.

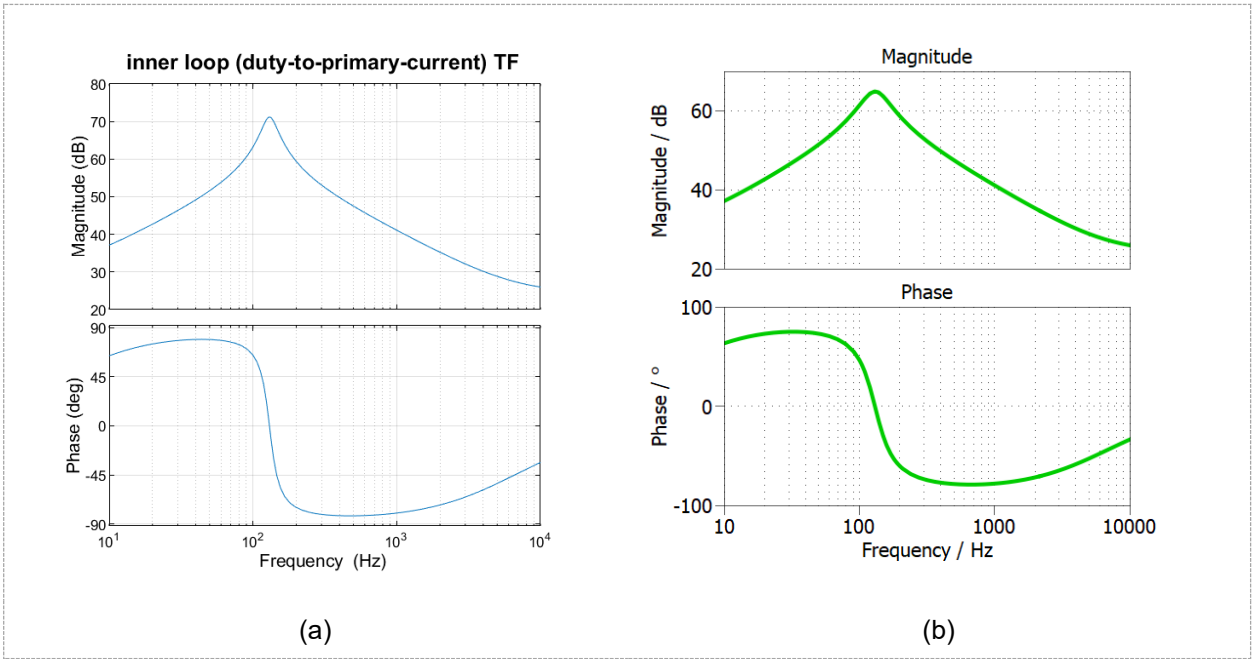


Figure 4-4. inner loop TF (a) MATLAB analytical model (b) PLECS simulation model

To verify the outer loop TF approximations, the phase difference between $\tilde{\imath}_x(s)$ and $\tilde{\imath}_{sec}(s)$ is evaluated. This is done by calculating $\tilde{\imath}_{sec}(s)/\tilde{d}(s)$, which can be divided by $\tilde{\imath}_x(s)/\tilde{d}(s)$ to obtain $\tilde{\imath}_{sec}(s)/\tilde{\imath}_x(s)$. The derivation of $\tilde{\imath}_{sec}(s)/\tilde{d}(s)$ follows the same approach as deriving $\tilde{\imath}_x(s)/\tilde{d}(s)$, noting that the secondary current is the same as the magnetizing current when the primary switch is in the *OFF-state*. Hence, the small-signal perturbation is applied to equation 4-16 and after linearization, the small-signal TF is given by equation 4-17.

$$i_{sec}(t) = [1 - D(t)]i_m(t) \tag{4-16}$$

Where: $i_{sec}(t)$ - Secondary current

$$\frac{\tilde{\imath}_{sec}(s)}{\tilde{d}(s)} = \frac{D'}{n}\frac{\tilde{\imath}_m(s)}{\tilde{d}(s)} - \frac{I_m}{n} \tag{4-17}$$

Where: D' - 1 – Duty cycle

n - Transformer Turns ratio

Combining equations 4-3 and 4-17 gives the primary-current-to-secondary-current TF. The bode plot of the resulting TF is shown in Figure 4-5, which confirms that there is almost no phase shift ($\pm$10°) between the quantities in the frequency range from about 100 Hz to 350 Hz. From this result, and given that the control variable is a 120 Hz waveform (rectified grid current), the approximation of equation 4-15 holds under the following conditions:

i. The compensated outer loop BW falls below 350 Hz (approximately).

ii. The inner loop BW is much greater than the outer loop BW (factor of 10)

$$\frac{\tilde{\imath}_{sec}(s)}{\tilde{\imath}_x(s)} = \frac{\tilde{\imath}_{sec}(s)/\tilde{d}(s)}{\tilde{\imath}_x(s)/\tilde{d}(s)} = \frac{1}{n}\frac{D'[\tilde{\imath}_m(s)/\tilde{d}(s)] - I_m}{D[\tilde{\imath}_m(s)/\tilde{d}(s)] + I_m} \tag{4-18}$$

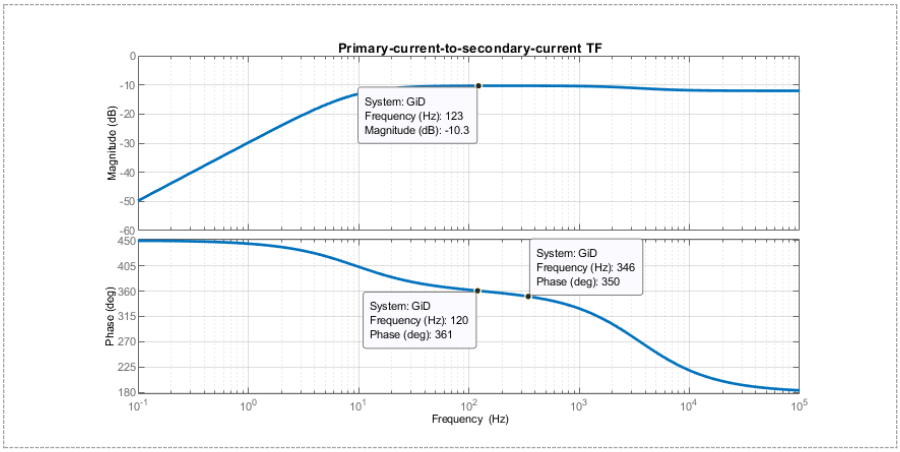


Figure 4-5. Primary-current-to-secondary-current TF

Figure 4-6 shows the ISOMBI control block diagram for the inverter current control loop, with both the inner loop ($G_{Ci}(s)$) and outer loop ($G_{Co}(s)$) compensators. The blocks $G_{ix\_d}(s)$ and $G_{ig\_ix}(s)$ represent previously derived dynamic models for the duty-to-primary-current TF (equation 4-9) and the primary-current-to-grid-current TF (equation 4-15) respectively.

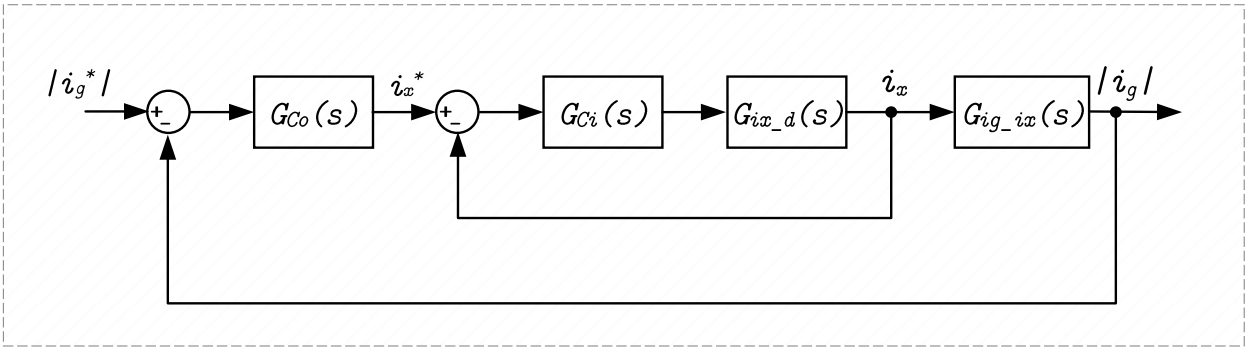


Figure 4-6. ISOMBI Control Block diagram

4.3.1 CCM/DCM Hybrid mode

Recall that the ISOMBI inevitably operates in hybrid DCM/CCM modes. however, given the specifications of Table 4-1 , the critical inductance derived in chapter 3 (4.6 μH), which is the minimum value for guaranteeing CCM operation is vastly exceeded (L_m = 61.2 μH), hence DCM operation is restricted to zero crossing instants, where the current is very low (observed in PLECS

simulation to be less than 150 μs per 8.3 ms half line-cycle). Hence, the design overwhelmingly operates in CCM and compensator design is CCM focused. This is further explored by plotting the anticipated steady-state DCM and CCM duty ratios derived in chapter 3 with the specified circuit parameters.

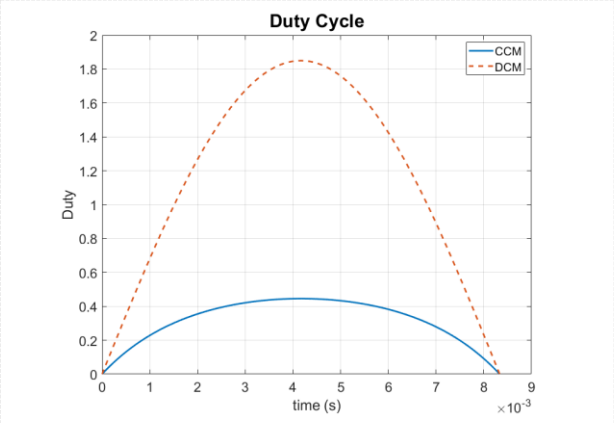


Figure 4-7. Steady-State DCM and CCM duty ratios

Figure 4-7 shows that there is no overlap between DCM and CCM. In proper hybrid mode designs [41], the DCM duty is initially lower than the CCM duty expression, hence the design operates in DCM, then at a given transition point, the curves intersect and the lower CCM duty becomes preferable, then the hybrid mode MI transitions into CCM. The ISOMBI has been designed primarily in CCM and only operates in DCM briefly, near zero-crossing instants, when there is not enough ampere-turns (MMF) to significantly magnetize the transformer. Hence the upcoming compensator designs only considers CCM operation.

4.3.2 Inner loop compensator design

The inner loop control block diagram is shown in Figure 4-8. It consists of the inner loop compensator ($G_{Ci}(s)$), the Pulse Width Modulator ($PWM(s)$), the inner loop converter TF ($G_{ix\_d}(s)$) and the sensor TF ($K_{ix}(s)$). The converter TF is generated by substituting circuit parameters into equation 4-9, at the peak instantaneous power point, and the transfer functions are summarized below in Table 4-2 below.

Table 4-2. Inner Loop Control block diagram TFs

Block	Content	Transfer Function
$G_{Ci}(s)$	Type II Lead Compensator	$\frac{3.0204e05}{s}\frac{(s+4500)}{s+7551e04}$
$PWM(s)$	Trailing edge PWM	$\frac{1}{1000}$
$G_{ix\_d}(s)$	Converter TF	$\frac{(12.71)s^2+(7.195e05)s+1.544e07}{s^2+(183.1)s+6.733e05}$
$G_{ig\_ix}(s)$	Converter TF	$\frac{0.25}{(2.154e-09)s^2+(7.04e-07)s+1}$
$K_{ix}(s)$	Single Pole Filter	$\frac{3.142e05}{s+3.142e04}$

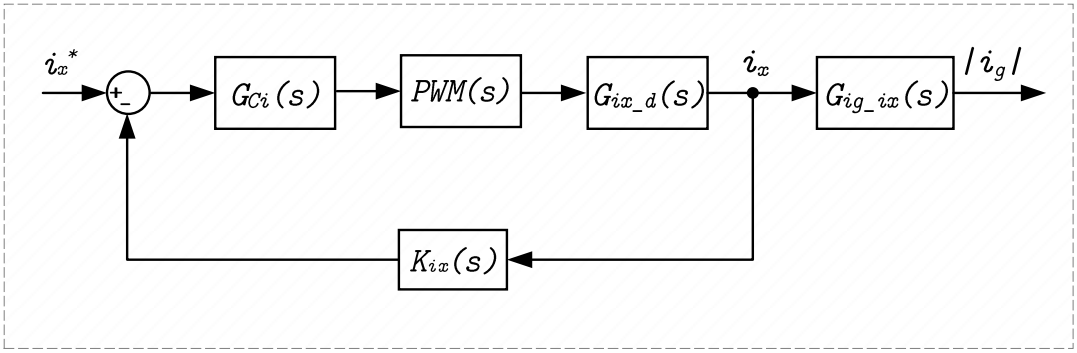


Figure 4-8. Inner loop control block diagram

The compensator is a type II Lead compensator, consisting of an integrator, a pole and a zero. The PWM block is a trailing-edge (up-count) digital PWM whose amplitude is 1000 and dynamic response is the same as the equivalent analog PWM in cascade with a sample-and-hold delay given by e^{-sDT_s}, where D is the duty cycle and T_s is the switching period [56]. It is assumed that the switching period is sufficiently small (10's of μs) that the delay is effectively negligible ($e^{-sDT_s} \approx 1$, for all s), hence the PWM block is approximated by its analog equivalent. Lastly, the sensor is a continuous-time single pole filter, implemented by a hardware circuit.

Figure 4-9 shows the bode plots of the inner loop control block diagram. In Figure 4-9(a), the uncompensated system consists of the converter TF and the PWM ($G_{ix\_d}(s) \cdot PWM(s)$), based on its frequency response, the compensation strategy aims to boost the low-frequency loop gain

(reduce tracking error and increase disturbance rejection) and restrict high-frequency loop gain (attenuate switching and measurement noise).

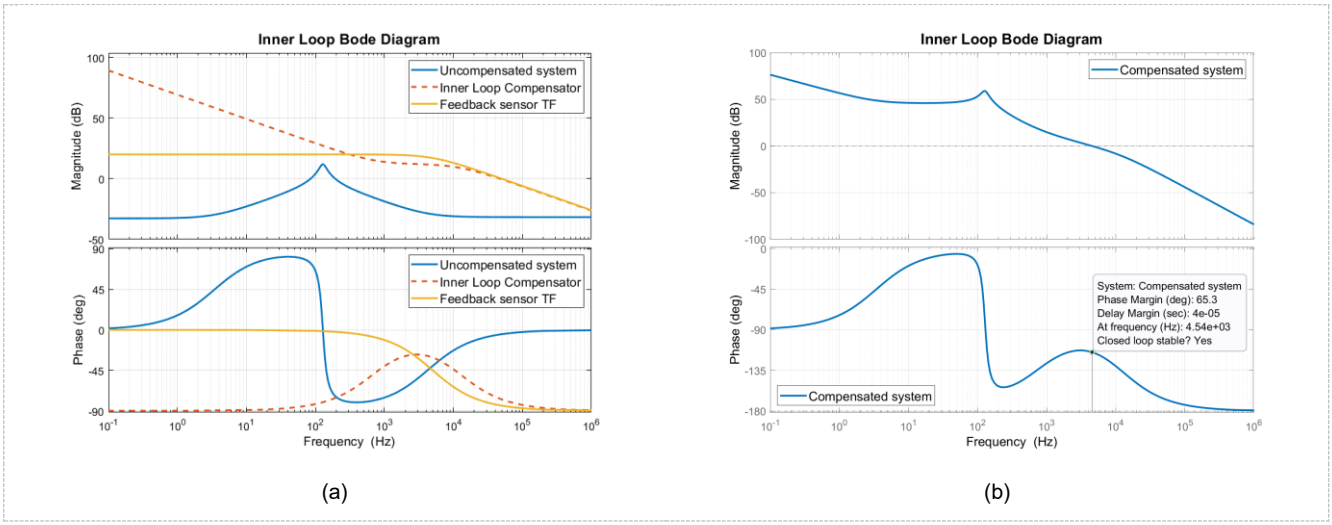


Figure 4-9. Inner Loop Bode plots (a) Uncompensated system (b) Compensated system

The type II lead compensator begins with a constant proportional gain for boosting the low-frequency loop gain but has an integrator (pole at the origin) that reduces the gain boost by -20dB/decade, so only the low-frequency loop gain is increased. However, the integrator causes the system phase to drop by 90°. At around 800 Hz, a zero is introduced, which boosts the phase and ensures adequate phase margin at the crossover frequency. The zero also causes the integrator to stop decreasing the system loop gain, which then rolls off by -20 dB/decade.

At around 12 kHz, a second pole is introduced to ensure attenuation of high frequency switching components, this pole combines with the feedback sensor filter to provide a -40 dB/decade roll off rate. Figure 4-9(b) shows the compensated system bode plot, where the crossover frequency (open loop BW) is 4.54 kHz, which is fast enough to track the 120 Hz reference and respond to the outer loop, the phase margin is acceptable at 65.3°, and the gain margin is infinite, hence the inner loop compensator satisfies design requirements.

4.3.3 Outer loop compensator design

The outer loop control block diagram is shown in Figure 4-10. It consists of the outer loop compensator ($G_{Co}(s)$), the closed loop TF of the inner loop ($T_{ixl}(s)$), the outer loop TF ($G_{ig\_ix}(s)$) and the sensor TF ($K_{ig}(s)$). The compensator is a type II Lag compensator, consisting of an integrator, a pole and a zero. The sensor is a continuous-time single pole filter, implemented by a hardware circuit, and the transfer functions are as summarized below in Table 4-3 below.

Table 4-3. Outer loop control block diagram TFs

Block	Content	Transfer Function
$G_{Co}(s)$	Type II Lag Compensator	$\frac{1057.5}{s}\frac{(s+1.996e04)}{s+1750}$
$T_{ixl}(s)$	Converter TF	$\frac{(3839)s+8.243e04}{s^2+(3.184e04)s+8.272e08}$
$G_{ig\_ix}(s)$	Converter TF	$\frac{0.25}{(2.154e-09)s^2+(7.04e-07)s+1}$
$K_{ig}(s)$	Single Pole Filter	$\frac{3.142e05}{s+3.142e04}$

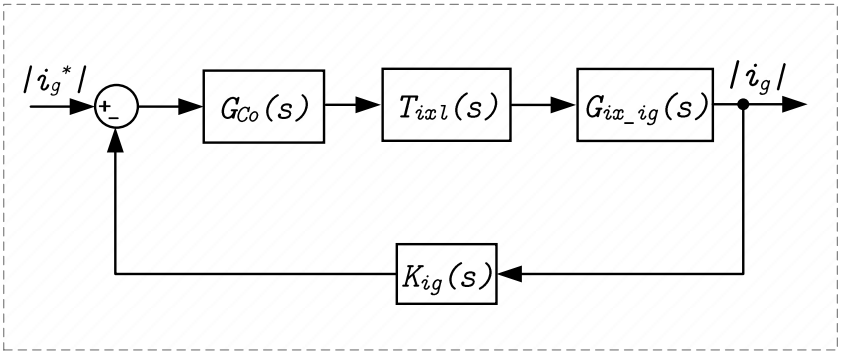
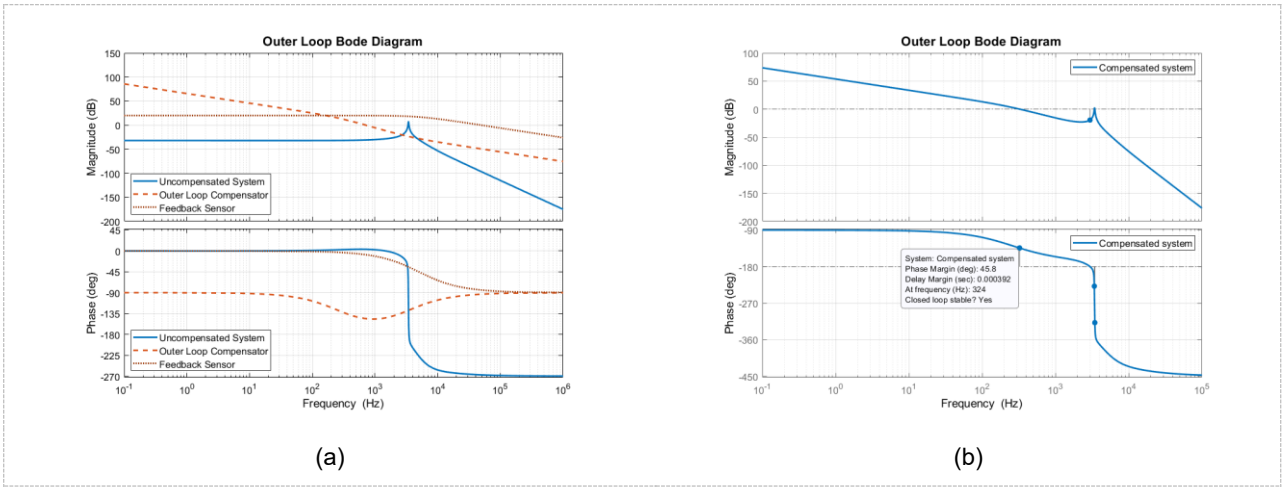


Figure 4-10. Outer loop control block diagram

Figure 4-11 shows the bode plots of the outer loop control block diagram. In Figure 4-11(a), the uncompensated system is the converter TF ($G_{ig\_ix}(s)$). Here, the compensation strategy is to boost the low-frequency gain and attenuate high-frequency gain, however, unlike the inner loop, the *CL* filter dynamics causes a sharp phase change around the resonant frequency around which the gain margin should be scrutinized.



(a) (b)

Figure 4-11. Outer loop bode plots (a) Uncompensated system (b) Compensated system.

The type II lag compensator, the begins with a proportional low-frequency gain boost, with an integrator (pole at origin) that rolls off the low-frequency gain boost by -20 dB/decade. At around 275 Hz, another pole is introduced to accelerate the roll-off rate to -40 dB/decade, which ensures that the attenuation of the filter resonance and that the system can achieve a reasonable gain margin. However, the use of two poles tends to reduce phase margin, hence a zero is added at around 3200 Hz, to boost the phase and restore acceptable phase margin. Figure 4-11(b) shows that the compensated system has a crossover frequency (open loop BW) of 324 Hz, which is fast enough to track the 120 Hz reference, and more importantly slow enough not to interact with the dynamics of the inner loop. The phase margin is an acceptable 45°, and the gain margin is 19 dB, hence the outer loop compensator satisfies design requirements.

4.4 Digital controller implementation

Despite designing continuous-time compensators, both inner and outer loop compensation structures will be implemented on a Texas Instruments (TI) TMS320F28377S Digital Signal Processor (DSP), which is a digital (discrete-time) device. The DSP is chosen for its flexibility, as it can be customized in software much faster than a hardware analog circuit and will provide real time monitoring and diagnostic information. Besides DSPs have since become widely used in

controlling modern power electronics devices [57]. To facilitate the control implementation, the continuous-time compensators will be translated to the discrete-time domain, which can then be implemented digitally using difference equations [58]. This section of the thesis details the controller discretization results as well as program flowchart structures used to execute the compensation loops. However, the issue of maintaining equivalent performance must be considered when transforming continuous-time compensators to the discrete-time domain.

The stability assessment was completed using continuous-time techniques (Bode plots), that do not generally transfer and apply to discrete-time systems [58]. Continuous-time analysis and design of the compensator was deemed more rigorous, because the MI is a continuous-time system, and this approach models its continuous behavior [59]. In contrast, a discrete-time analysis will only provide information at discrete intervals of a certain period [59]. The discrepancy between design and implementation is resolved by adopting the Bilinear transform, because it provides the closest mapping of continuous-time frequencies in the discrete domain, on condition that the sampling period is selected to minimize delays, and thus retain the frequency response properties of the original continuous time system [58].

a) Controller Discretization

A type II compensator, which consists of an integrator, a pole and a zero, can be expressed as a cascade of a PI compensator with a single pole filter as in equation 4-19.

$$G(s) = \frac{A}{s} \cdot \frac{s+\omega_z}{s+\omega_p} = \left(\frac{A}{\omega_p} + \frac{A\omega_z}{s\omega_p}\right)\left(\frac{\omega_p}{s+\omega_p}\right) = \left(K_p + \frac{K_i}{s}\right)\left(\frac{\omega_p}{s+\omega_p}\right) \quad \text{4-19}$$

Where:

A	-	Proportional gain of the type II compensator
ω_z	-	Type II compensator zero location (radians)
ω_p	-	Type II compensator pole location (radians)
$K_p = A/\omega_p$	-	PI compensator proportional gain
$K_i = (A\omega_z)/\omega_p$	-	PI compensator integral gain
$\omega_p/(s+\omega_p)$	-	Single pole filter

Applying the bilinear transform to the single pole filter component of the type II compensator yields the difference equation expressed below:

$$y[kT] = (1 - 2a)y[kT - 1] + a(e[k] + e[k - 1]) \quad \text{4-20}$$

Where: $a = \frac{\omega_p \cdot (T/2)}{1 + \omega_p(T/2)}$ - Filter coefficient

T - Discrete time-step

$k = 1,2,3, \ldots$ - Sample number

$e[k]$ - Error in the k'th time-step

Similarly, applying the bilinear transform to the PI compensator component of the type II compensator yields the difference equation expressed below (4-21)

$$y[kT] = m_p[kT] + m_i[kT] \quad \text{4-21}$$

Where: $m_p[kT] = K_p \cdot e[kT]$ (proportional part) 4-22

$m_i[kT] = T \cdot K_i \cdot \left(\frac{e[kT] + e[(k-1)T]}{2}\right)$ – (integral part) 4-23

The sample time of the discrete-time system is a critical factor which determines how closely the digital compensators match the analog design. According to [58], the bilinearly transformed discrete system approximately maps the frequency response of the continuous-time system, only when equation 4-24 is satisfied.

$$\frac{\omega T}{2} \leq \frac{\pi}{10} \quad \text{4-24}$$

Where: ω - s-domain frequency

T - Sample time

Given that the compensated inner loop and outer loop BWs are ~5 kHz and ~400 Hz respectively, the maximum allowable time-steps are 20 μs and 250 μs respectively for inner and outer loops. In implementation, the time-steps are selected as 10 μs and 20 μs, for the inner and outer loops,

respectively. Both are significantly below the maximum allowed; hence the discrete-time system is deemed to be a precise representation of the continuous-time design.

b) Digital controller Algorithms

Based on the discrete transformation of the continuous-time compensators into difference equations, the software programming of the control system is straightforward and simple using conditional statements and Interrupt Service Routines (ISRs). This section presents the algorithms used in the digital control system. Figure 4-12 shows the control software overview flowchart. The program begins in the main function, where peripheral configuration, sensor calibration, data structures initialization, PLL/Flag resets, and ISR vector installation is completed. Then the program enters an infinite loop, waiting for ISRs, which is where the compensator algorithms run and control the MI switches.

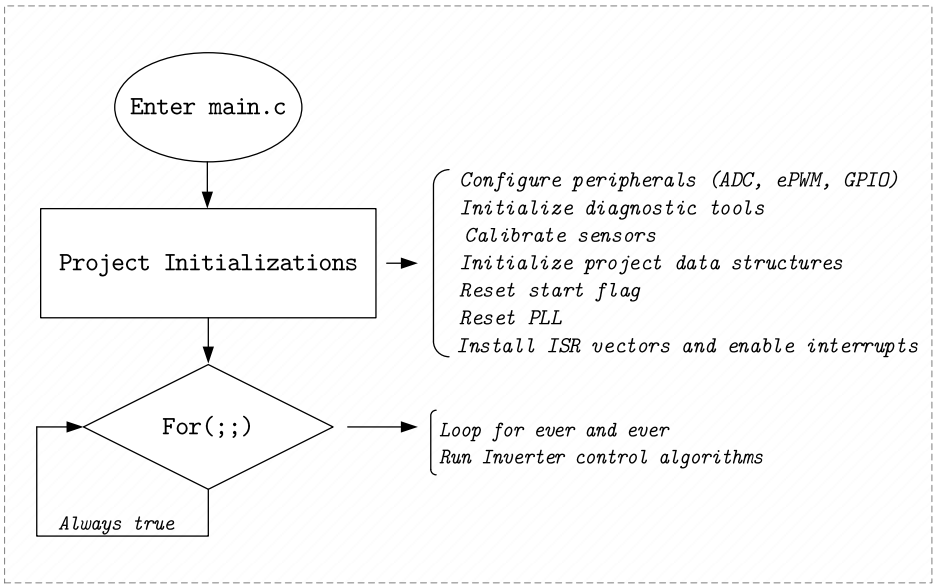


Figure 4-12. Control Software overview flowchart

The program uses three ISRs, which are set up according to Table 4-4. Flowcharts for all three ISRs are provided and discussed. A feedforward term computed from equation 3-16 is also added to the controller to speed up its response, and a phase locked loop (PLL) algorithm is used to

synchronize with the utility grid. The PLL is the only non-custom algorithm, obtained from a TI library [60] and its output is used to shape the grid and primary currents. It also ensures that the inverter control algorithms start or end safely at zero-crossing instants and indicates whether the positive or negative cycle is active, with a deadtime in between the transitions where all the switches are turned off to prevent transistor shoot-through.

Table 4-4. ISR information table

ISR	Frequency	time-step	Function(s)
Outer loop ISR	50 kHz	20 μs	Outer loop compensator, PLL, zero-crossing detection, feedforward computation and retrieving ADC results
Inner Loop ISR	100 kHz	10 μs	Inner loop compensator
Synchronization ISR	12.5 kHz	80 μs	Line cycle detection, Switching control

Figure 4-13 represents the flowchart of the outer loop ISR, which triggers every 20 μs. This is smaller than the maximum time-step required to match the outer loop continuous-time compensator and has the following functions:

1. Transfer Analog to Digital Converter (ADC) conversion results from the ADC registers to the project data registers.
2. Run the Phase Locked Loop (PLL) algorithm based on the most recent sample in the measured grid voltage.
3. Detect the zero-crossing point of the grid voltage, to raise initial start flag for commencing MI operation.
4. Generate and shape the pre-programmed outer loop reference based on the PLL output (normally the amplitude would be obtained from an MPPT voltage loop).
5. Compute the instantaneous feedforward quantity based on equation 3-16.
6. Decide which primary current measurement (i_{x1} or i_{x2}) to send to the inner loop compensator based on the operating line cycle.

7. Execute the outer loop type II compensator difference equations.
8. Shape the inner loop reference based on the PLL output and obtain the amplitude from the outer loop compensator difference equations.

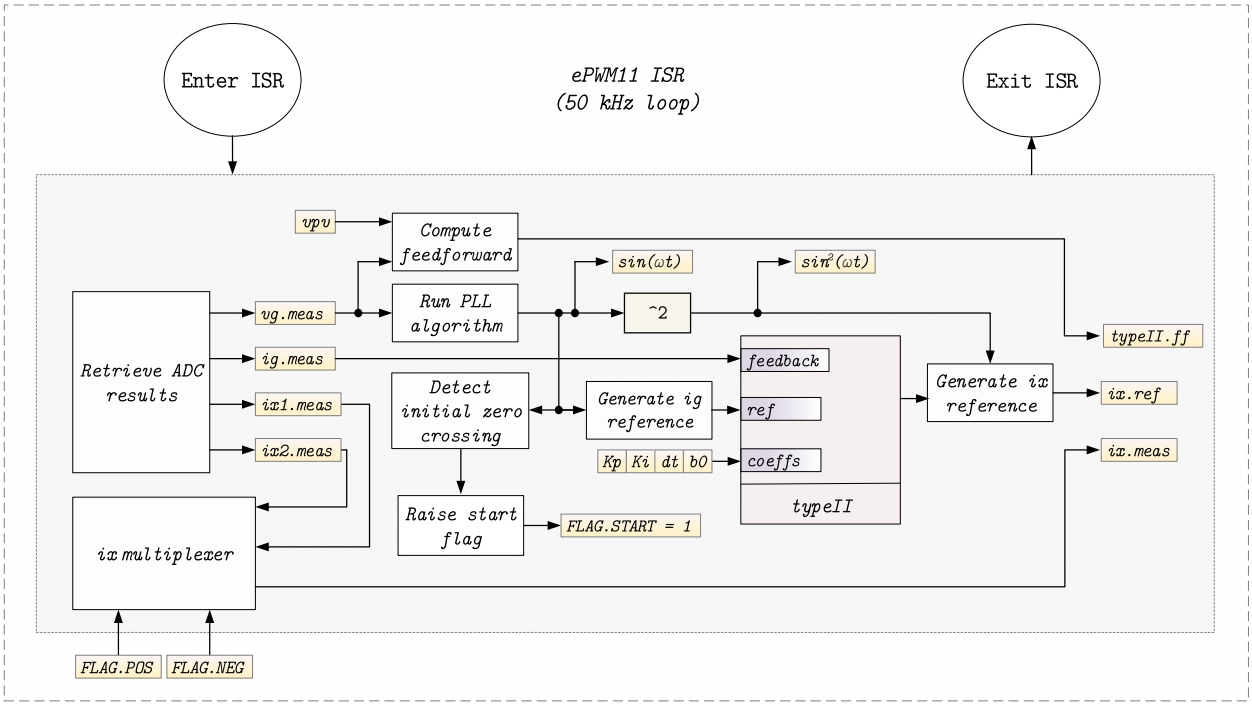


Figure 4-13. Outer loop ISR flowchart

Figure 4-14 presents the flowchart of the inner loop ISR. This interrupt triggers every 10 μs, which is lower than the maximum time-step required to mimic the inner loop continuous-time compensator and has only two following functions:

1. Check for overcurrent in the grid and primary currents and shut-down all switches without waiting to detect a zero-crossing.
2. Run the inner loop compensator, add the feedforward, and write the appropriate duty cycle to the PWM peripheral registers.

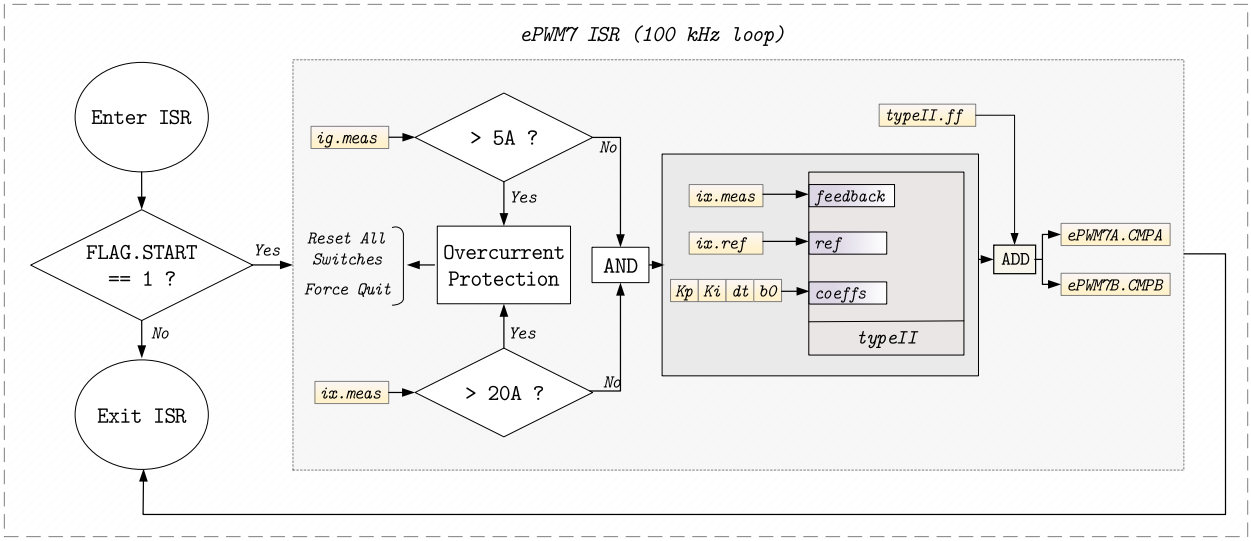


Figure 4-14. Inner loop ISR flowchart

Figure 4-15 presents the flowchart of the synchronization ISR. This interrupt triggers every 80 μs and has two functions:

1. Use the PLL output to detect which cycle is presently running.
2. Control the output of switches based on the following conditions:
   a. Deadtime: Turn off all switches.
   b. Positive cycle: Turn-on S_A and S_4, restrict HF switching on S_2, and Allow HF switching on S_1.
   c. Negative cycle: Turn-on S_B and S_3, restrict HF switching on S_1; and allow HF switching on S_2.

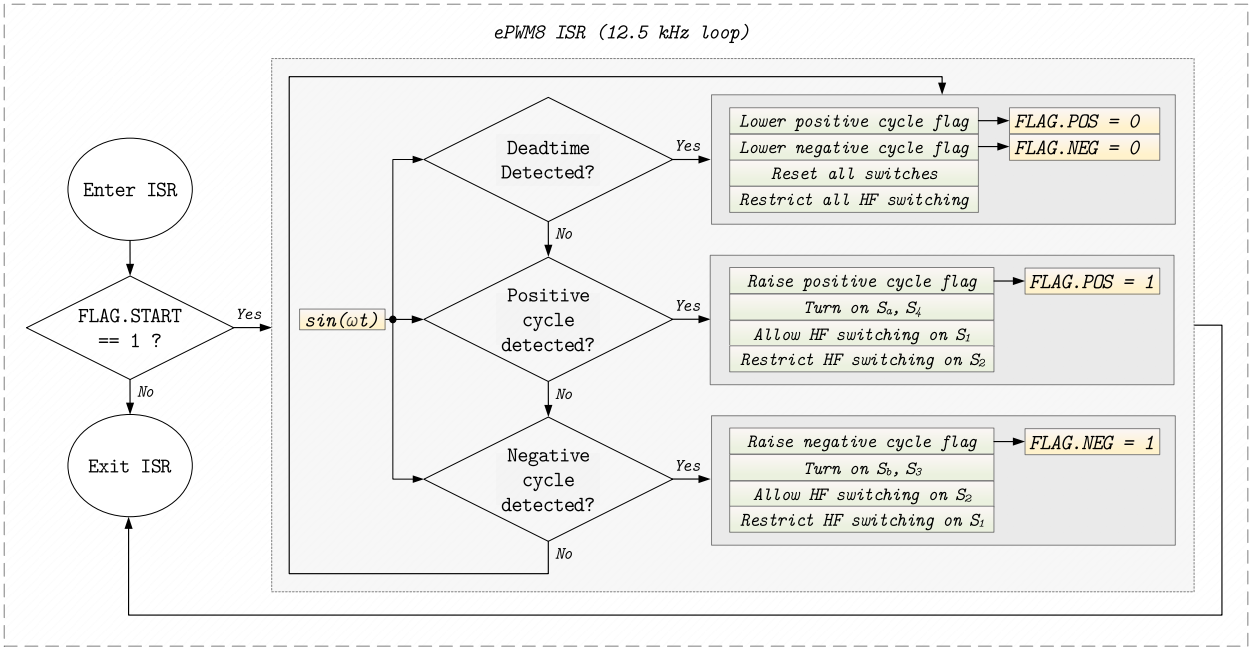


Figure 4-15. Synchronization ISR flowchart

By applying these control algorithms, operating principles and steady-state characteristics described in chapter 3 can be verified.

4.5 Chapter summary

The ISOMBI inverter current control system implements a dual loop compensation structure, a reasonably fast inner loop regulates the primary current, while a much slower outer loop regulates the grid current. To simplify the analysis, the fourth-order circuit was approximated by a second-order model (which excluded the *CL* filter) for the inner loop design, this second order model sufficiently captured the dynamics influencing the primary current, but not the grid current. Hence, the model was extended to include the *CL* filter for designing the outer loop compensator. It was demonstrated that the inner loop compensation indirectly compensated the secondary current within the bandwidth of the outer loop compensator, so, it was adequate to approximate the outer loop dynamics by representing the secondary current as a scaled version of the primary current, and the outer loop dynamics were approximated by the second-order *CL* filter.

Small-signal models were derived, which were then used in designing type II compensator structures for both inner and outer loops. The final section of the chapter applied the bilinear transform to the continuous-time compensator structures and selected discrete sample times, such that the frequency behavior of the continuous-time compensator mapped approximately to the same response in the discrete domain. Then the digital control algorithm flowcharts were presented and explained. Three interrupt service routines, functioning primarily for inner loop compensation, outer loop compensation and grid synchronization respectively were designed. The next chapter presents the prototyping and experimental results obtained from combining the theoretical works of this and the previous chapter.

Chapter 5 - Prototyping and Experimental Verification

In this chapter, an ISOMBI prototype is developed and tested. The prototype applies derived parameter expressions and operating principles obtained in chapter 3, with control algorithms from chapter 4 to verify the functionality, steady-state expressions, and performance of the ISOMBI topology. Following is a brief discussion of the experimental prototype design and detailed assessment of experimental results. The experimental results are intended to prove that the ISOMBI topology is applicable as an AC module MIs.

5.1 Prototype Specifications and Design

The experimental prototype pictured in Figure 5-1(b), has the technical specifications disclosed in Table 5-1. These specifications were previously introduced for controller design in chapter 4 and are repeated here for convenience. In Figure 5-1, the HF switches are MOSFETs (Infineon IPW60R070P6XKSA1), secondary switches are IGBTs (STMicroelectronics STGW30H60DFB), and the bidirectional unfolding switches are constructed using two discrete MOSFETs in common-source configuration (same part as the HF switches). The filter cap is concealed by the IGBT heatsinks in the pictured experimental prototype, but it is a film capacitor. Lastly, the experimental prototype uses auxiliary electronics such as voltage sensors, current sensors, and gate drivers, in conjunction with a DSP to achieve its closed loop control.

Table 5-1. Technical Specifications of the ISOMBI prototype

Prototype specs			**Circuit parameters**		
V_{pv}	54.7	V	L_m	61.2	μH
V_g	120	V_{rms}	n	4	-
f_o	60	Hz	C_{in}	5400	mF
f_s	100	kHz	r_c	0.05	Ω
P_{rated}	300	W	C_f	2.2	μF
$P_{nominal}$	200	W	L_f	979	μH

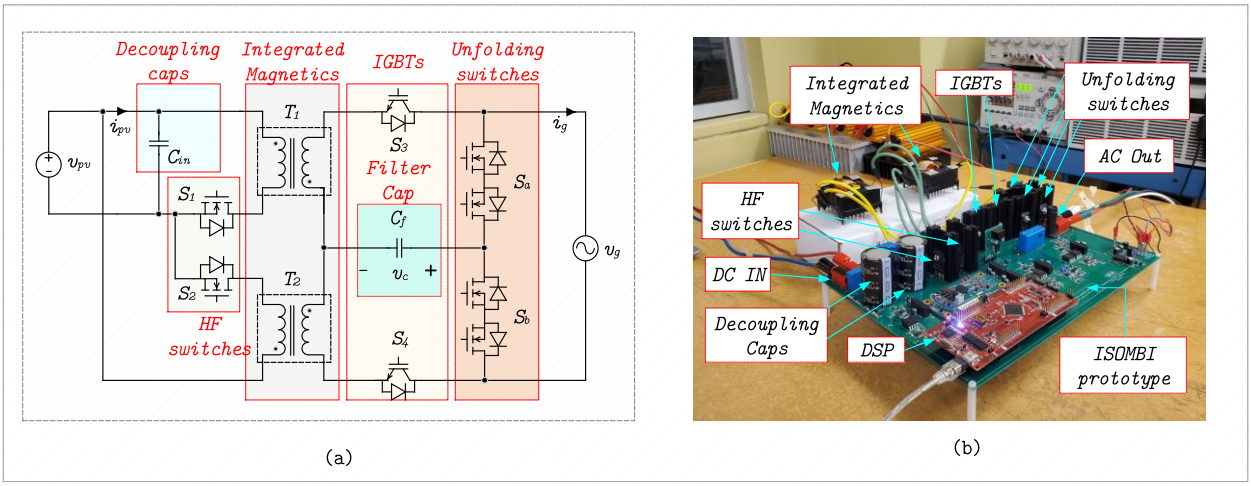


Figure 5-1. ISOMBI prototype (a) circuit diagram (b) Experimental prototype

The prototype design prioritizes manual assembly and repairability over power density which can be improved in future work. Hence relatively large (physical size) passive components are used, and the PCB stack-up consists of only two layers.

5.1.1 *CL* filter

The *CL* filter's primary function is to reduce HF switching ripples in the grid current. However, its inclusion also introduces the possibility of excess reactive power exchange and low PF due to phase shifts in the grid current [52]. Fortunately, the analysis performed in chapter 3 proves instrumental in obtaining parameters that allow near unity PF. This is applied in Figure 5-2 where capacitance and inductance limits are derived based on that analysis. Operating far away from these limits, will increase the likelihood of unity PF. Two additional curves representing 600 Hz and 10 kHz are overlayed in Figure 5-2 to further restrict the design region (600 Hz is 10 times the fundamental frequency, to allow sufficient outer loop BW and 10 kHz is 0.1 times the switching frequency, for attenuating switching components). The selected design point represents 0.008 per unit capacitance, and 0.0385 per unit inductance, which yields the specification in Table 5-1 (2.2μF and 0.979 mH), and the filter cutoff is 3429 Hz.

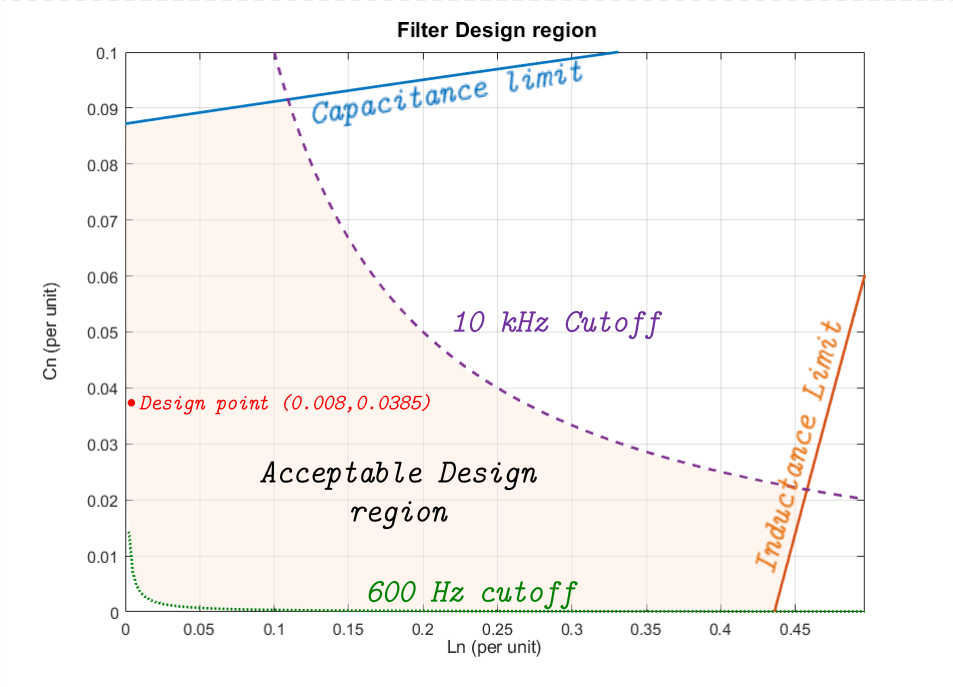


Figure 5-2. CL filter design region

5.1.2 Integrated Magnetic Devices

The secondary magnetizing inductance (L_{m2}) value was derived based on the output *CL* filter requirements. Since the same magnetic device is used as FB transformer and grid filter inductor, and the primary magnetizing inductance (L_{m1}) is proportional to L_{m2}, this directly affects the FB design. First, L_{m1} must be greater that the critical inductance value (equation 3-18). Then the primary peak current, which depends on the magnetizing current ripple is also calculated to ensure it falls within an acceptable range (equation 3-17).

Using the specifications detailed in Table 5-1 with equations 3-17 and 3-18, gives a peak primary current of 20.40 A and critical inductance value of 4.6 μH, for a nominal power output of 200 W, which is where the prototype will be benchmarked. These results allow the design to proceed to construction, because the primary inductance (61.2 μH) significantly exceeds the critical value, and the design will achieve CCM operation. The peak primary current is also within the limits of the selected primary MOSFET switches (63.5 A). Next, the magnetic design was

simulated in ANSYS PExprt, which was used to verify the core selection, flux swing and number of turns. The results obtained from simulation are summarized in Table 5-2.

Table 5-2. Magnetic simulation results

Parameter	Value	Parameter	Value
Core and Bobbin:	*ETD 49*	Wire gauge:	*AWG 20*
Manufacturer:	*Ferroxcube*	Flux swing:	*38.48 mT*
Material:	*3C94*	Maximum Flux:	*186.98 mT*
Air gap:	*6.21 mm*	Leakage *L*:	*791.85 nH*
Primary Winding:	*29 Turns*	Magnetizing *L*:	*61.2 µH*
Secondary Winding:	*116 Turns*	Core temperature (max):	*108.68 °C*

Two identical magnetic components were constructed, pictured in Figure 5-3(a) and (b). The devices were then characterized using a vector network analyzer (Omicron Bode 100) to derive the equivalent circuit parameters as depicted in Figure 5-3(c). The magnetic prototype results are presented in Table 5-3. Since closed loop control is to be employed, the small variations between parameters of the magnetic prototypes are deemed acceptable.

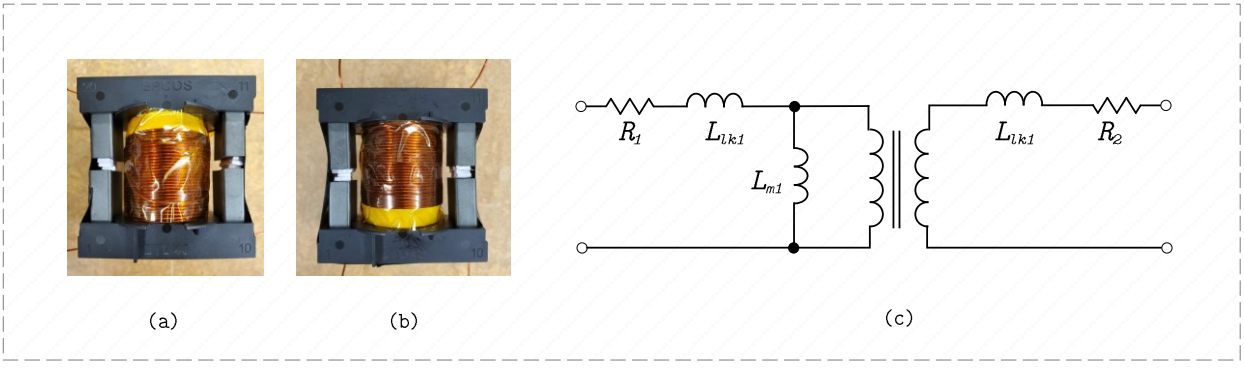


Figure 5-3. Integrated magnetics (a) T_1 (b) T_2 (c) equivalent circuit

Table 5-3. Properties of magnetic prototypes

Parameter	T_1	T_2
R_1	74 mΩ	68 mΩ
L_{lk1}	1.8 μH	1.1 μH
L_{m1}	60.8 μH	64.63 μH
R_2	321 mΩ	321 mΩ
L_{lk2}	29 μH	17.82 μH
L_{m2}	1.02 mH	1.105 mH

5.1.3 RCD snubber

The leakage inductance of the FB transformer, unlike the magnetizing inductance, does not transfer energy between primary and secondary windings, hence under FB switching action where the windings are intermittently open-circuited, energy accumulated in the leakage inductance during turn-on, seeks an alternate path to flow. It often finds a path through the output capacitance of the connected MOSFET. This concept was briefly introduced in chapter 3, where the leakage inductance was described as a parasitic element resulting from the imperfect coupling between primary and secondary windings.

Leakage inductance current flows into the MOSFET capacitance, leading to LC resonance, which induces voltage spikes and ringing in the waveform. To avoid damaging the primary MOSFET, an RCD snubber is implemented, according to the techniques detailed in [42]. The snubber circuit, functions by redirecting leakage inductance current into a dissipative RC circuit and is effective at clamping the MOSFET drain-source voltage at acceptable levels. In this prototype, a fast diode is used with a 1.5 kΩ and 2200 pF capacitor to achieve a clamp level of around 200 V.

5.1.4 DSP Software

The control algorithms of the ISOMBI prototype, detailed in chapter 4 are programmed onto a DSP development kit (see Figure 5-1) used in the prototype, it is programmed using the C programming language.

5.2 Experimental verification

The simplified experimental setup is depicted in Figure 5-4 where a DC power source emulates the solar panel, the ISOMBI prototype synchronizes its phase and frequency with an AC power source, which stands in for the utility grid and a 30Ω resistor bank is placed in parallel with the AC power to consume the output power generated by the ISOMBI prototype. The DSP is programmed via USB, and lastly, an auxiliary power source is used to supply control circuits and power up the DSP.

The actual laboratory setup is shown in Figure 5-5, where the circuit is connected as in Figure 5-4, except that input and output terminals pass through a power analyzer (Yokogawa WT1800E) for power quality measurements, and an oscilloscope (Tektronix MDO3024) is provided to obtain current and voltage measurements. Lastly, a windows PC is used to program the DSP through the Texas instrument's code composer studio IDE. All experimental results presented in the following subsections are obtained from the oscilloscope, power analyzer or DSP samples.

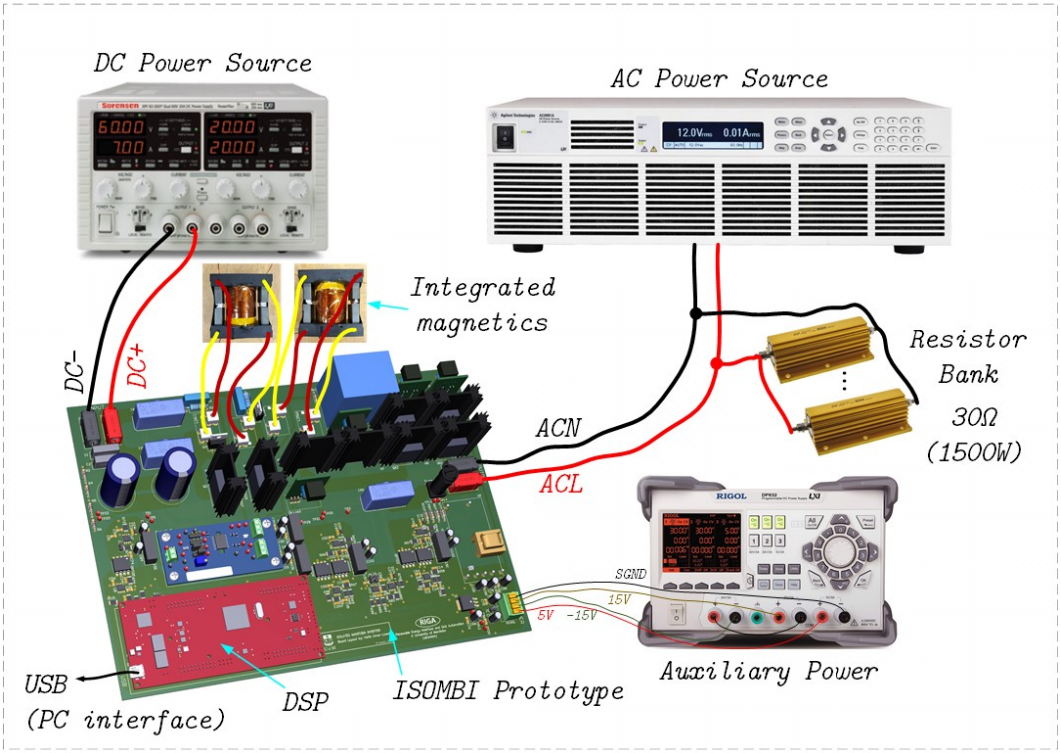


Figure 5-4. Simplified experimental setup

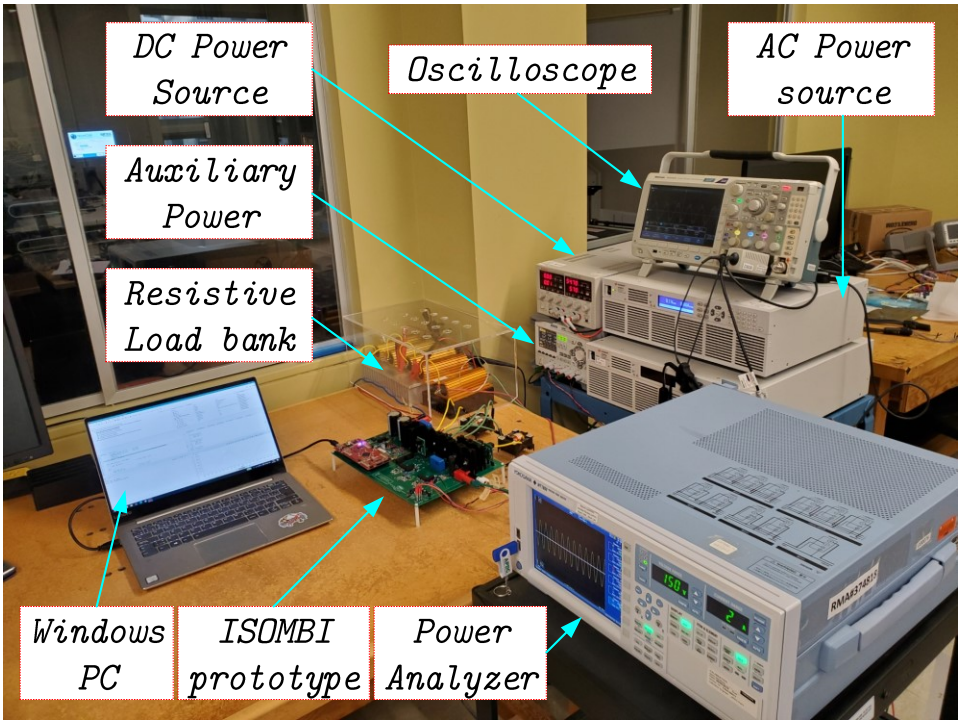


Figure 5-5. Laboratory experimental setup

5.2.1 Operating Principles

This subsection presents experimental waveforms showing that the operating principles proposed in chapter 3 are used to operate the prototype. It verifies the operation of the PLL algorithm and shows that it is effective at synchronizing the switches with the positive and negative Line cycles of the utility grid voltage. Secondary current waveforms are presented to validate the dual function of the integrated magnetic devices and primary MOSFET waveforms demonstrate low-frequency interleaving.

a) Positive cycle switching sequence.

Figure 5-6 shows the synchronization of positive cycle switches with the utility grid voltage. This result follows from the flowchart of Figure 4-15, whereupon detecting the positive cycle, the control system turns on S_a and S_4, and allows HF switching on S_1 (Denoted HF+ in Figure 5-6), otherwise, they are all turned off. From this, it is verified that control system can operate the prototype as intended during the positive half of the line cycle.

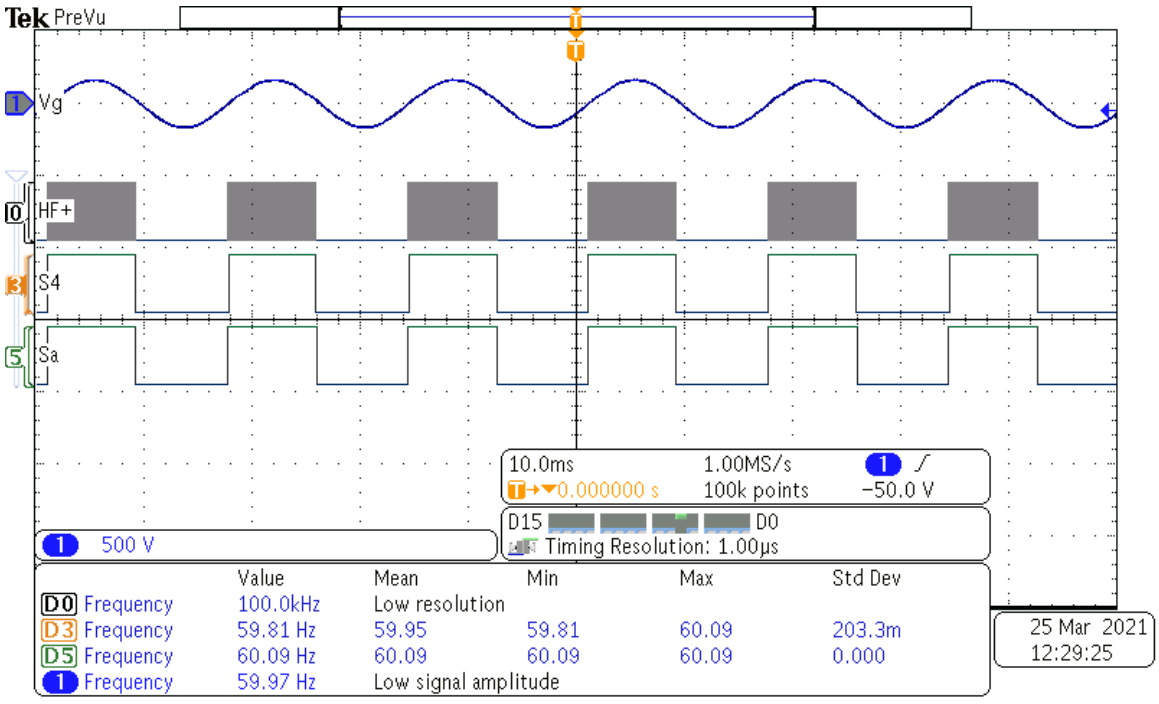


Figure 5-6. Positive cycle synchronization waveforms

b) Negative cycle switching sequence.

Figure 5-7 shows the synchronization of negative cycle switches with the utility grid voltage. This result follows from the flowchart of Figure 4-15, whereupon detecting the negative cycle, the control system turns on S_b and S_3, and allows HF switching on S_2 (Denoted HF- in Figure 5-7), otherwise, they are all turned off. From this, it is verified that control system can operate the prototype as intended during the negative half of the line cycle.

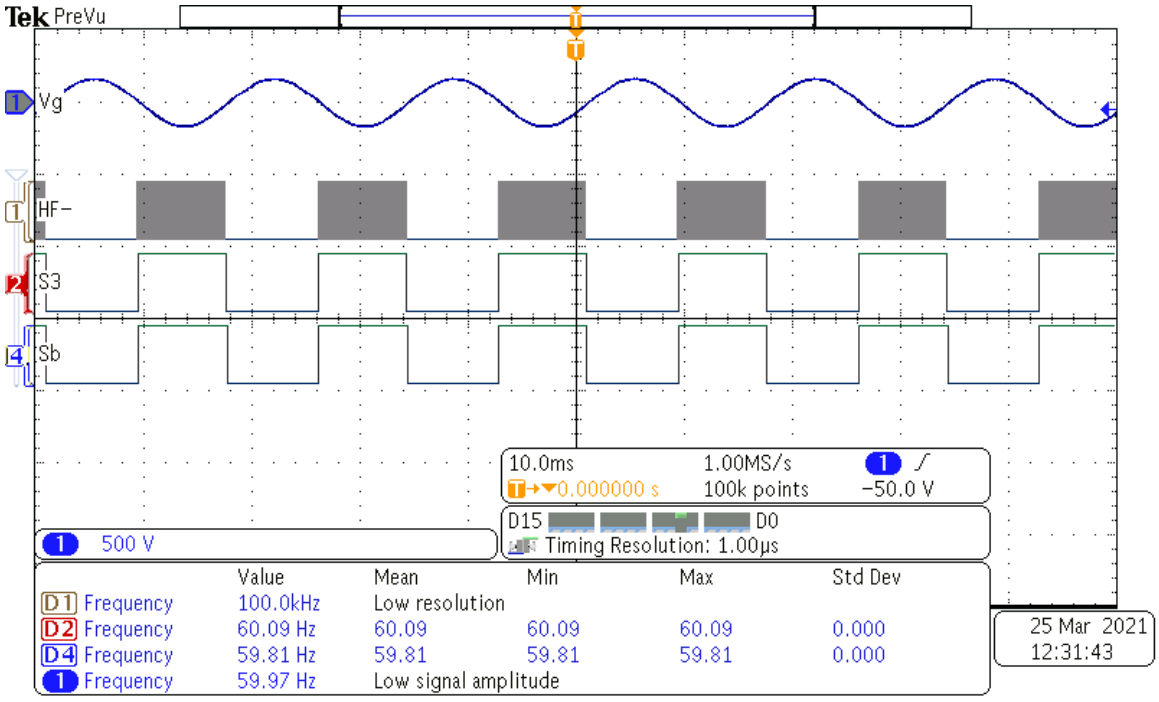


Figure 5-7. Negative cycle synchronization waveforms

c) Integrated Magnetics

Figure 5-8 shows secondary current waveforms obtained from windings of the integrated magnetic devices. It is seen that when the prototype is operated with the switching sequences shown in Figure 5-6 and Figure 5-7, the secondary windings of the integrated magnetics will switch between conducting HF FB current and smooth filtered grid current on alternate cycles of the utility line. As expected from chapter 3, T_1 is the FB transformer on the Positive cycle, while T_2 is the grid filter inductor and during the negative cycle, T_2 is the FB transformer and T_1 is the

grid filter inductor. This verifies that the same device performs the functions of FB transformer and grid inductor and the magnetic devices can be said to be functionally integrated.

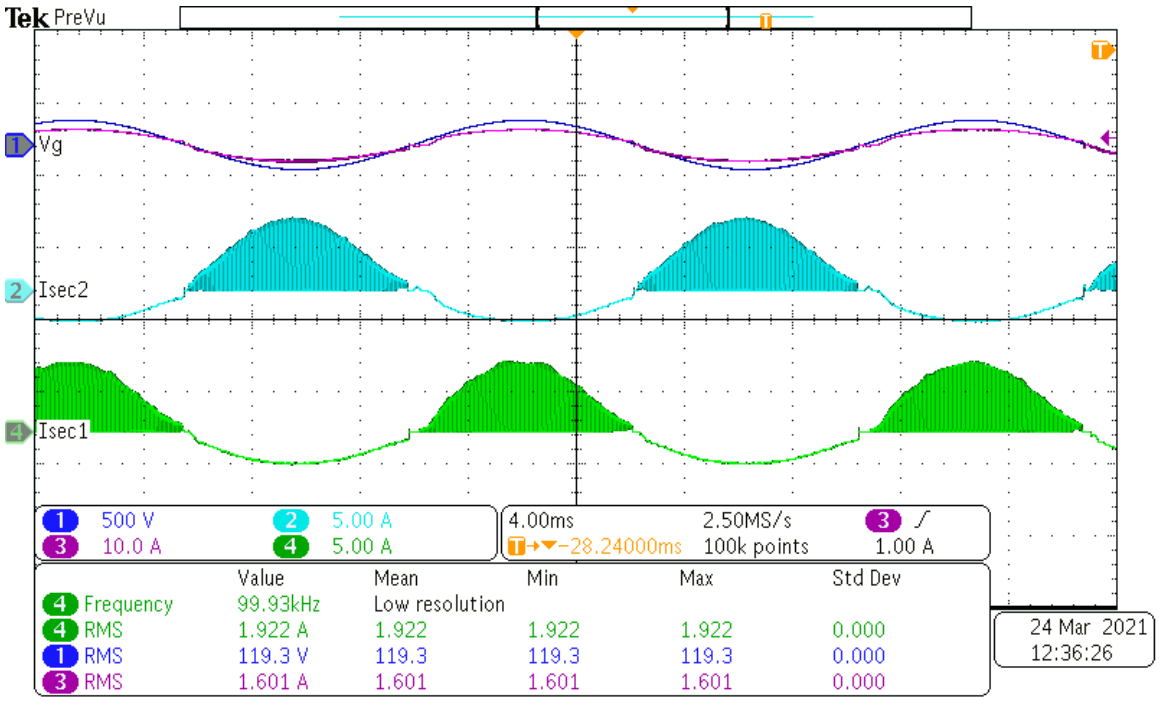


Figure 5-8. Secondary Current waveforms showing integrated magnetics function.

d) Low Frequency Interleaving

Figure 5-9 shows the MOSFET Drain-Source voltages for the primary switches, it verifies that only one primary switch operates at HF at any time, thus each one processes half of the total power. This LF-interleaving arrangement allows the ISOMBI to potentially match ratings for the HF-interleaved FB MI. Figure 5-10 shows the prototype operating at 280 W, based on the operating principles. The output current shows good synchronization with the grid voltage and is sinusoidal. The AC power quality will be further evaluated in an upcoming subsection.

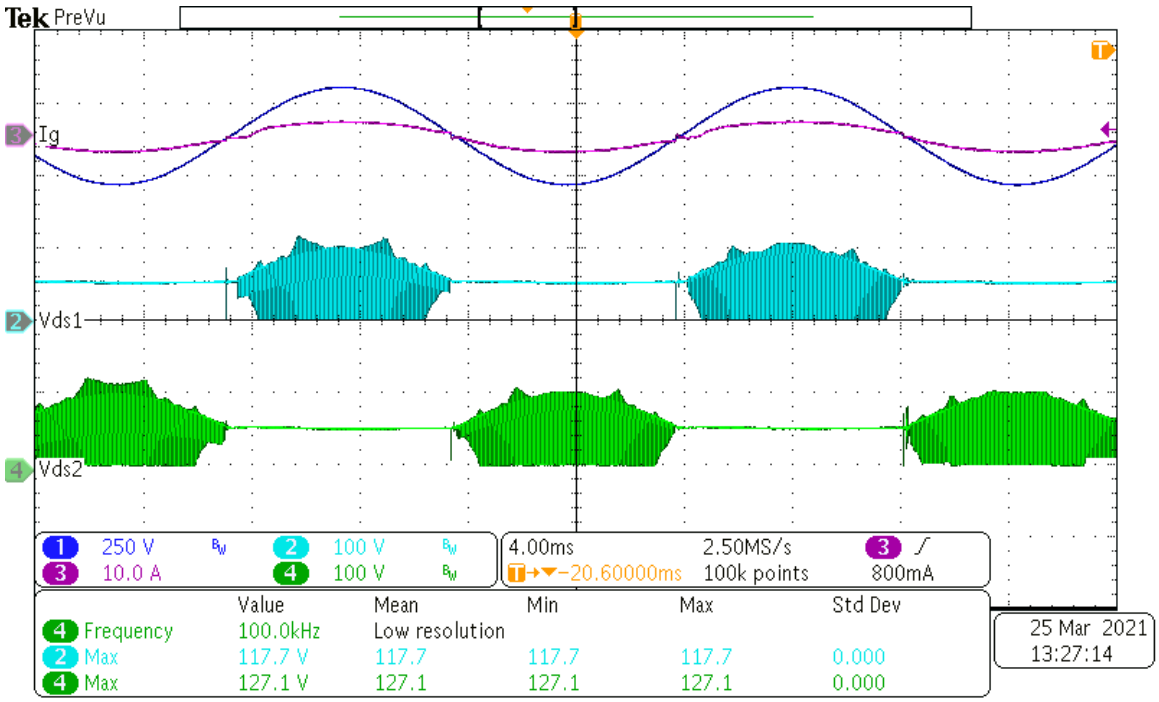
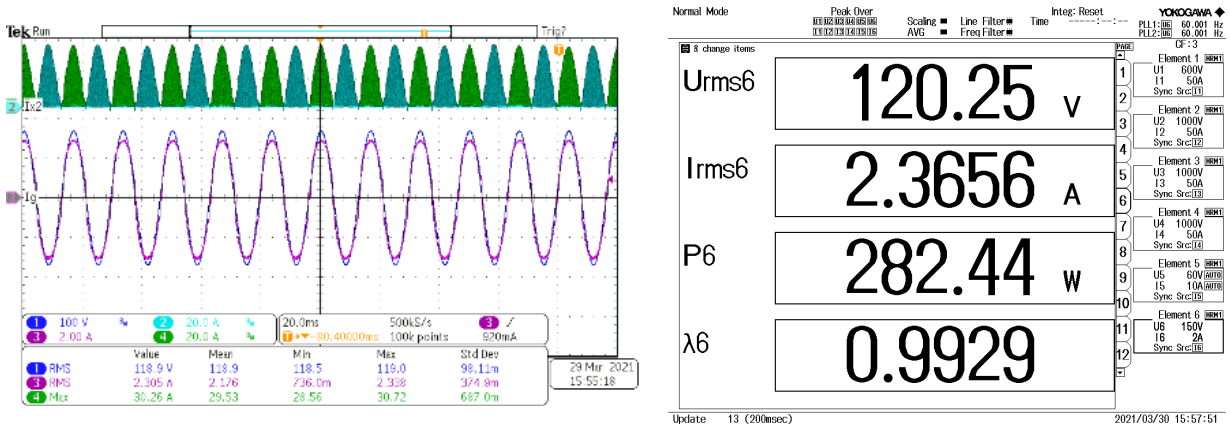


Figure 5-9. Drain-Source voltage of primary switches



(a) (b)

Figure 5-10. ISOMBI operating at 280 W (a) Waveforms (b) Power measurements

5.2.2 Steady state analysis verification

This subsection presents experimental results to validate the steady-state analysis carried out in chapter 3. Test data include the pseudo-DC-link voltage, magnetizing current, duty ratio and primary current. All results in this subsection are obtained when the control system is programmed to demand 1.67 A (RMS) (approximately 200 W) from the AC output of the MI prototype and the operating principles are consistent with the preceding section.

a) Pseudo-DC link Voltage

Figure 5-11 records the pseudo-dc-link voltage of the ISOMBI when the topology is operating in AC-steady-state. It is seen that the pseudo-DC-link voltage has practically the same amplitude and RMS value as the grid voltage but is rectified and pulsates at 120 Hz. This verifies the predictions from chapter 3 and validates equation 3-2.

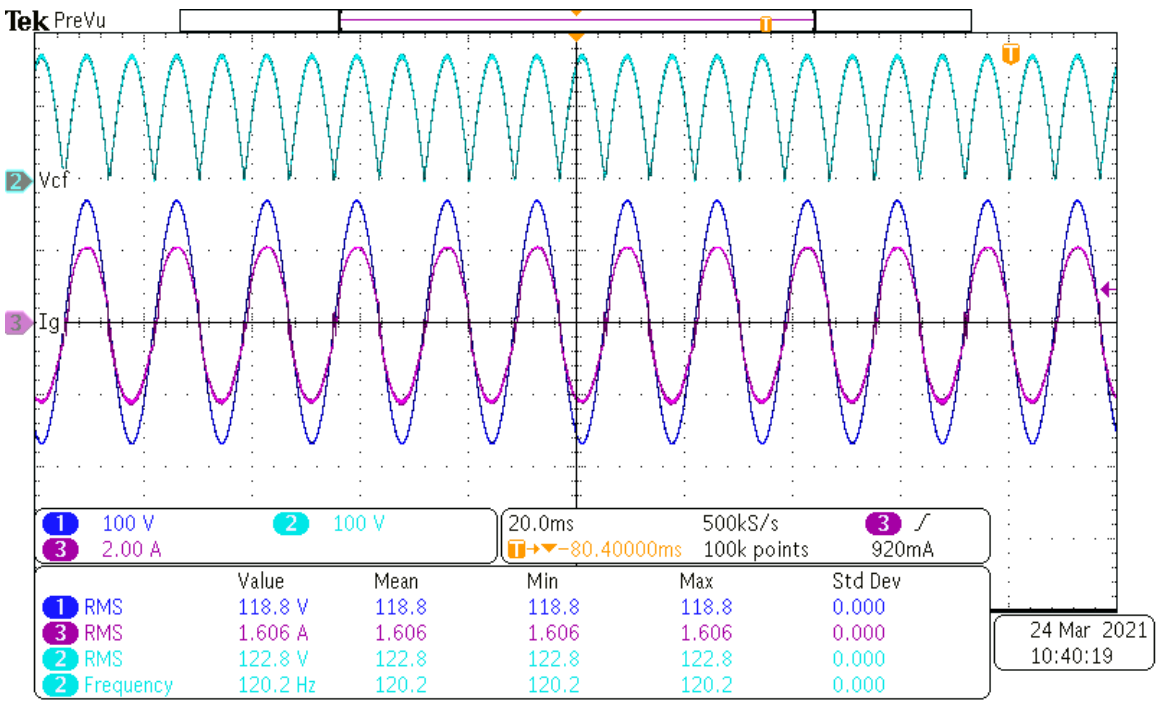


Figure 5-11. Pseudo DC link voltage waveform

Figure 5-12 zooms in on Figure 5-11 to show the peak pseudo-DC link voltage ripple. Equation 3-4 predicts that the peak voltage ripple will be 5.45 V based on the prototype specifications. Hence, there is good agreement with the experimental results which records a 5.41 V ripple component pulsating at the switching frequency.

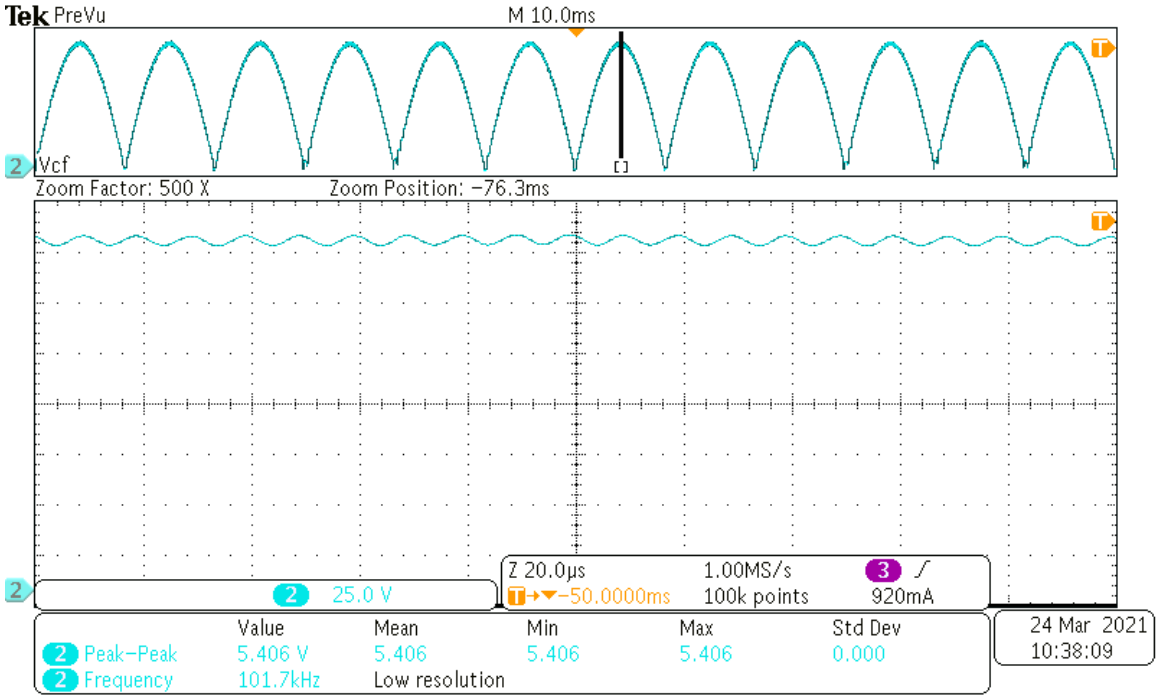


Figure 5-12. Pseudo-DC-link voltage ripple waveform

b) Primary magnetizing Current

For simplicity, the Magnetizing current expression of the FB transformer was derived by referring the magnetizing inductance to the primary winding. However, magnetizing current transfers back and forth between primary and secondary windings. Hence two current probes (primary and secondary) and a math equation was used to measure the magnetizing current. The math is given by:

$$i_m = i_x + 4i_{sec} \qquad 5\text{-}1$$

Where: i_m – Magnetizing current, i_x – Primary current i_{sec} – Secondary current

Figure 5-13 records the magnetizing current for T_1 of the ISOMBI, when the topology is operating in AC-steady-state. It is seen that the magnetizing current has a ripple component when in FB transformer mode and low ripple when in grid filter inductor mode. The AC-steady-state average magnetizing current should peak at 19.25 A based on equation 3-6, with the ripple obtained from equation 3-8 as 4.73 A. This predicts a peak magnetizing current of 21.62 A. Experimentally, the peak magnetizing current is measured as 20.40 A, and Figure 5-14 zooms in on Figure 5-13 to obtain the magnetizing current ripple as 3.12 A, hence the peak AC-steady-state average is 18.84 A. These results are reasonably close to the expected values.

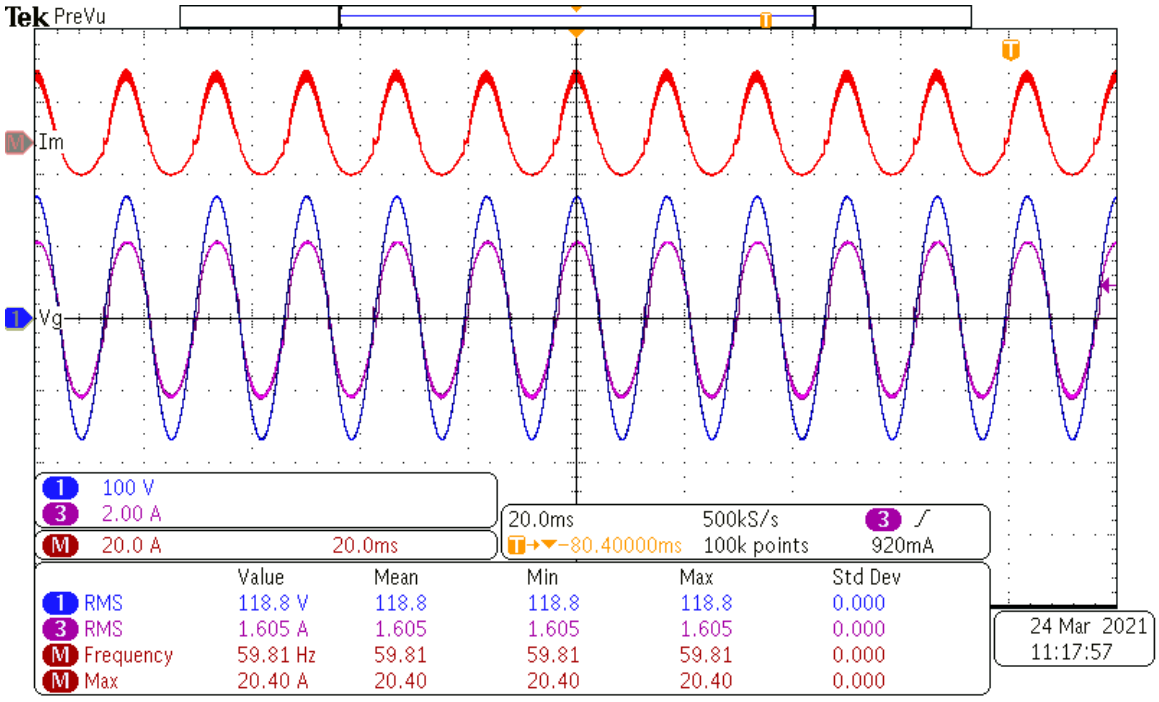


Figure 5-13. Magnetizing current waveform

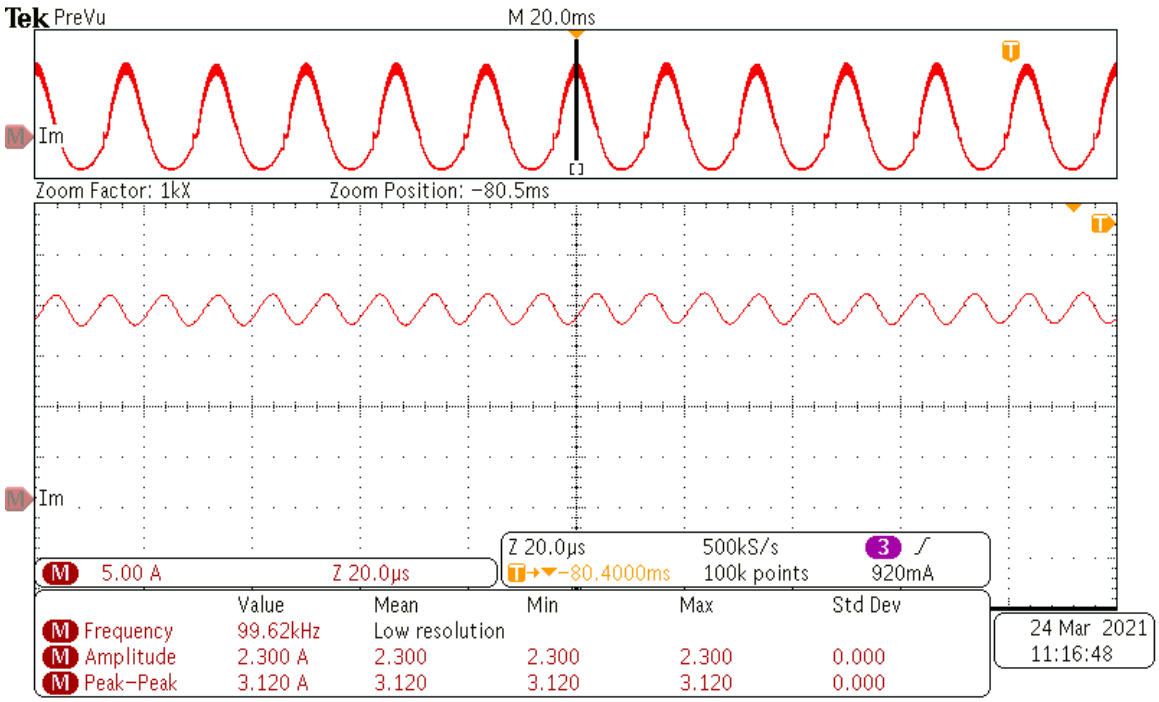


Figure 5-14. Magnetizing current ripple waveform

c) Duty Ratio

The duty ratio commanded by the control system is obtained from the DSP's diagnostic data and plotted in Figure 5-15. The peak duty cycle is around 0.52 (The figure is scaled up by 1000 to match the PWM amplitude). This is not consistent with the calculated peak duty from equation 3-16 which is 0.44, suggesting that the system might be operating close to stability margins. This suggests that further stability assessment such as the Nyquist criterion may prove useful in providing more information about the system stability.

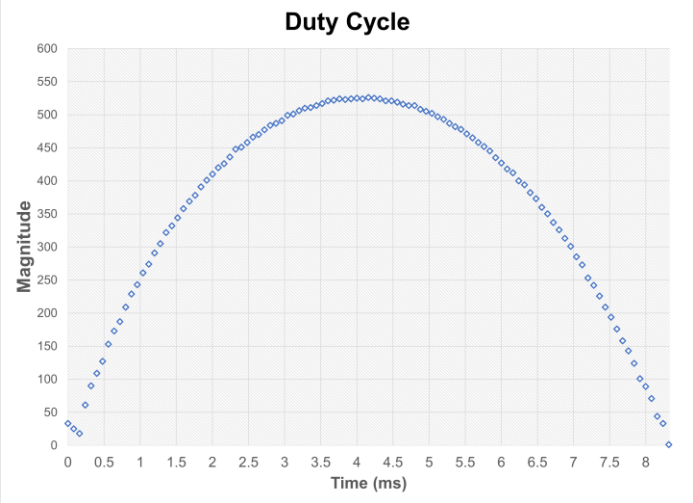


Figure 5-15. Duty ratio

d) Primary Current

Figure 5-16 shows measures the peak primary currents as 20.27 A and 20.95 A through S_1 and S_2 respectively. Both are close to the calculated value of 21.62 A. Figure 5-17 zooms in on Figure 5-16 to confirm that the ISOMBI operates as designed in CCM.

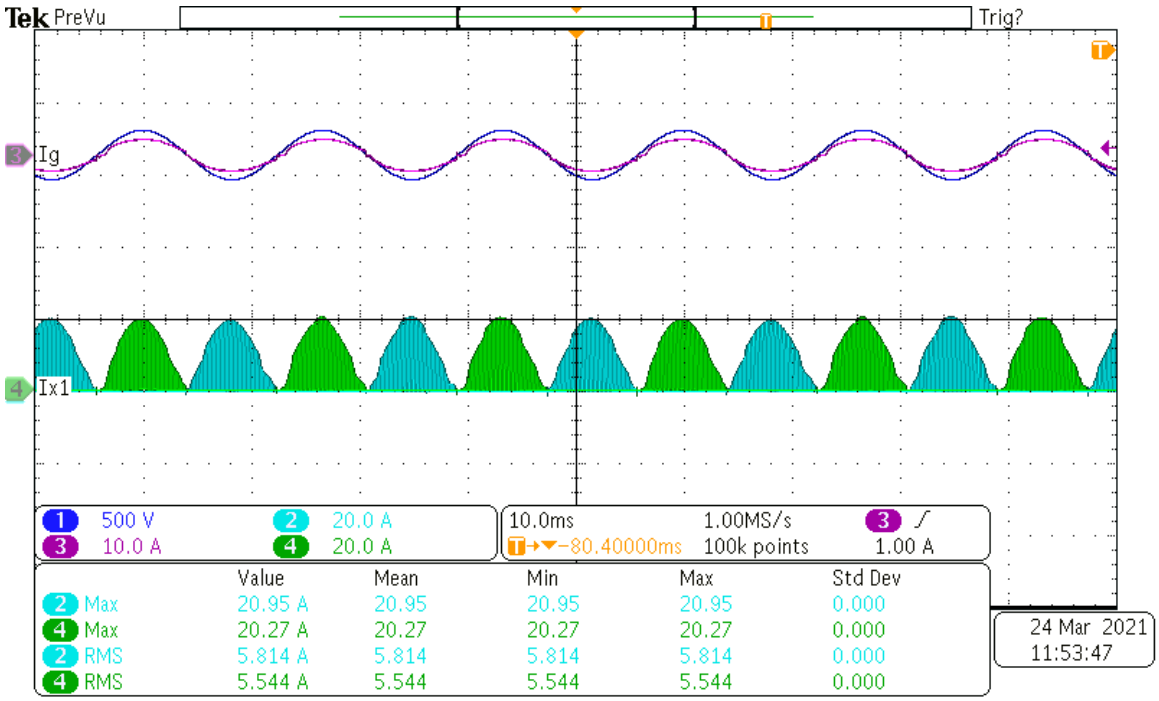
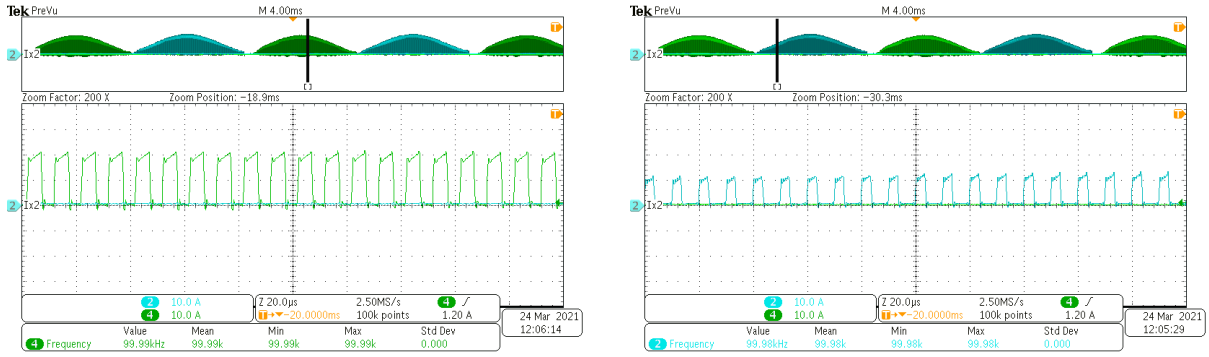


Figure 5-16. Primary Current waveform



(a) (b)

Figure 5-17. Verifying CCM operation (a) close to the peak (b) elsewhere

Figure 5-18 shows the average primary current sensed by the DSP feedback loop. Which peaks at 9.0 A (the feedback sensor gain is 10) at this power level (200 W). It also confirms the shape of the average primary current as a sine-squared function (equation 3-11). The average primary current is expected to peak at around 7.3 A, based on equation 3-11. As with the duty cycle measurement, the slight discrepancy is attributed to the feedback compensator.

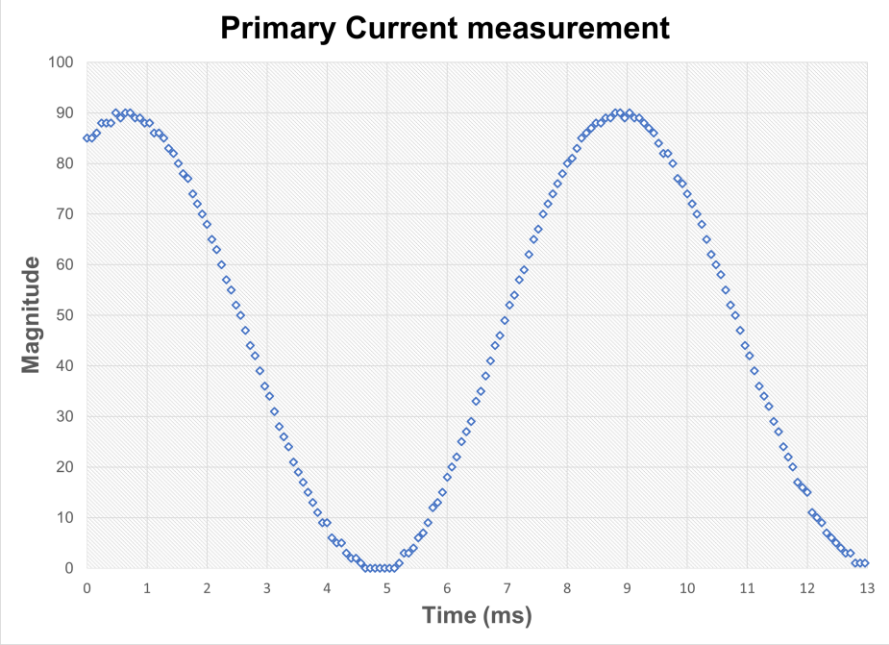


Figure 5-18. Average primary current sampled by DSP

e) Summary of Steady-State characteristics

Table 5-4 summarizes the experimental results of steady-state characteristics.

Table 5-4. Summary of steady-state characteristics at 200 W

Quantity	Analytical value	Experimental Results
Pseudo-DC link voltage (RMS)	120 V	122.8 V
Peak pseudo-DC link voltage ripple	5.45 V	5.41 V
Average primary magnetizing current	19.25 A	18.84 A
Peak primary magnetizing current ripple	4.73 A	3.12 A
Peak Duty Ratio (CCM)	0.44	0.52
Peak primary current	21.62 A	20.40 A
Average Primary current	7.3 A	9.0 A

5.2.3 Control-system Validation

To validate the ISOMBI control system, a step change in the reference is applied for both step-up and step-down scenarios. In the step-up case, the MI prototype begins and reaches steady-state at an output of 1.3 A (RMS) (~160 W), it is operated for 3 seconds before a reference change commands the output to rise to 2.0 A (RMS) (~240 W), representing an instantaneous 80 W change in power output. The same levels are applied for step-down scenario. In both cases, the system adapts to the new reference in less than 4.0 milliseconds.

a) Step-up reference change

Figure 5-19 shows the results of the step-up reference change. As indicated by the measurement, the reference change is programmed to occur exactly 3 seconds into the steady-state operation. Figure 5-20, which is a zoomed in version of Figure 5-19 shows that the control system seamlessly adapts to the new reference and reaches the new peak within 4.0 milliseconds of the reference change.

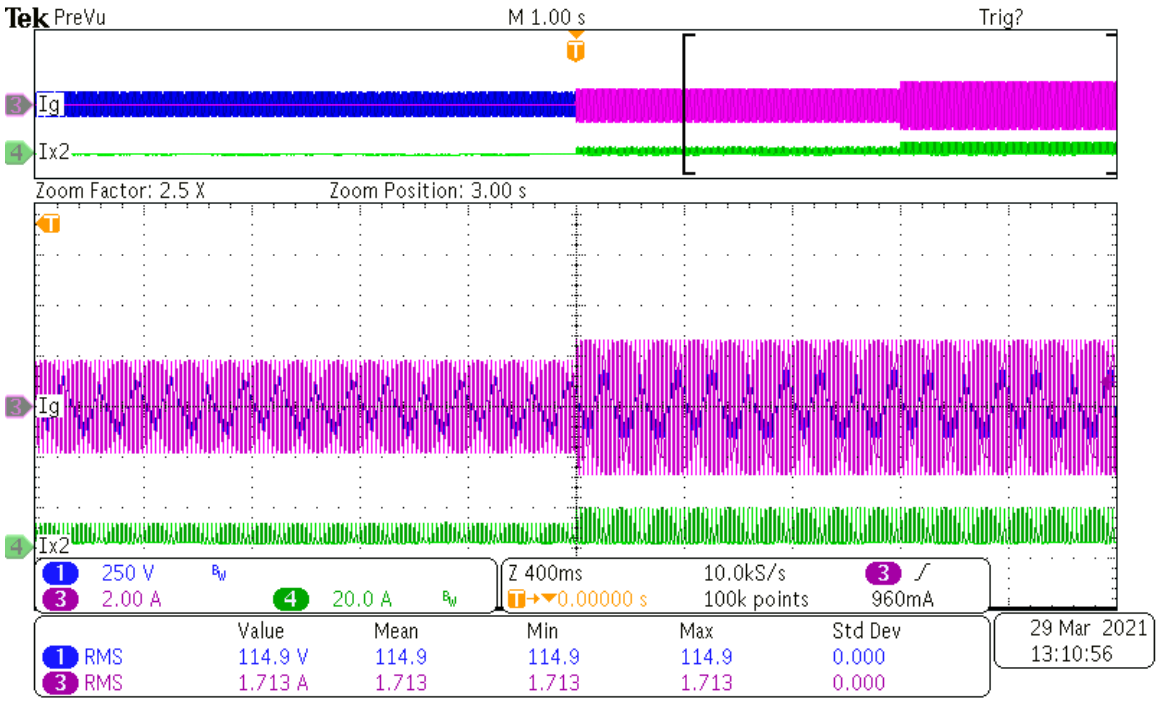


Figure 5-19. Step-up reference change

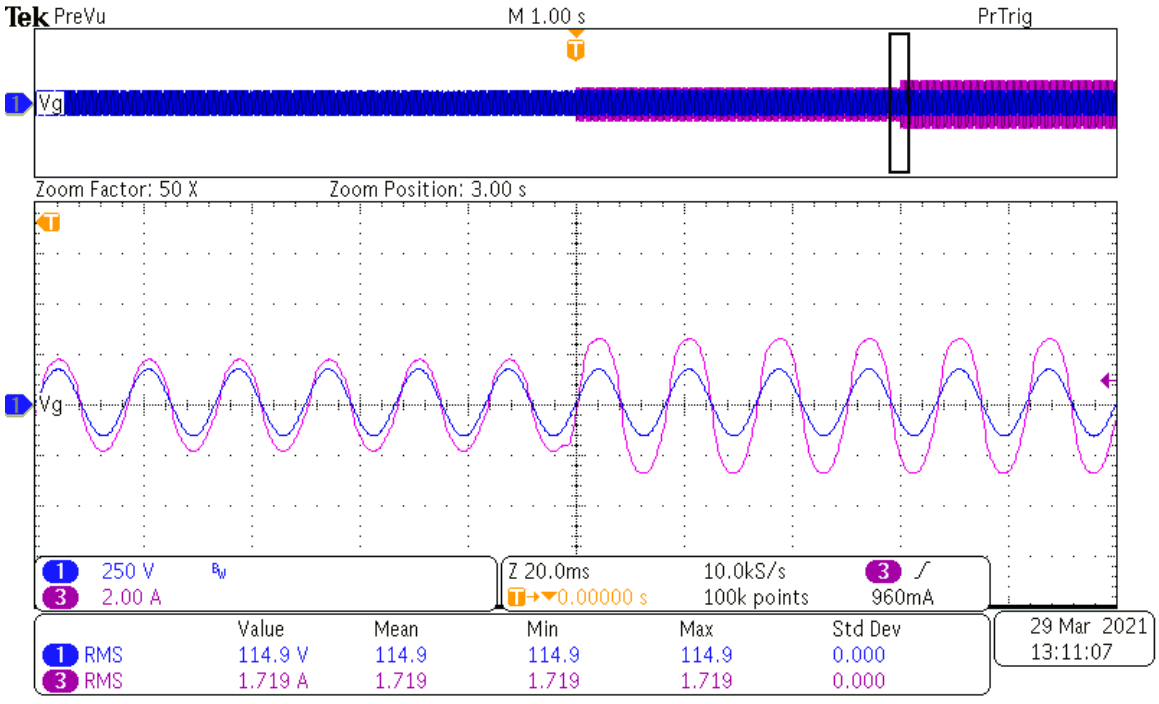


Figure 5-20. Zoomed-in Step up reference change.

b) Step-down reference change

Figure 5-19 shows the results of the step-up reference change. As indicated by the measurement, the reference change is programmed to occur exactly 3 seconds into the steady-state operation. Figure 5-20, which is a zoomed in version of Figure 5-19 shows that the control system seamlessly adapts to the new reference and reaches the new peak within 4.0 milliseconds of the reference change.

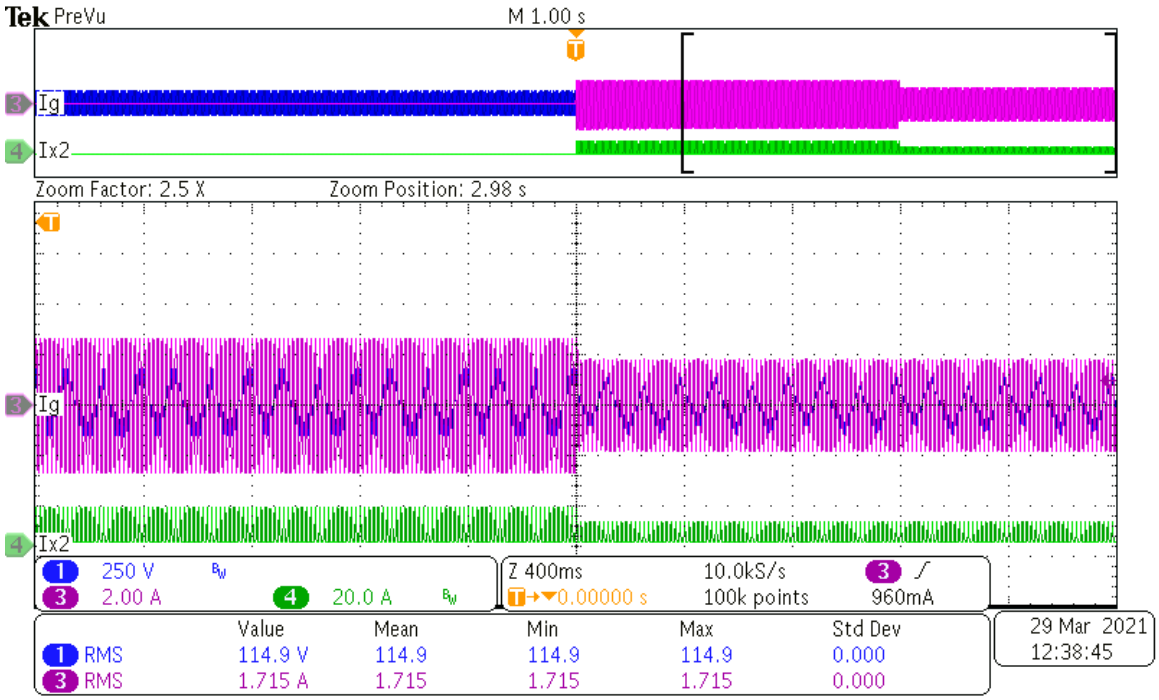


Figure 5-21. Step-down reference change

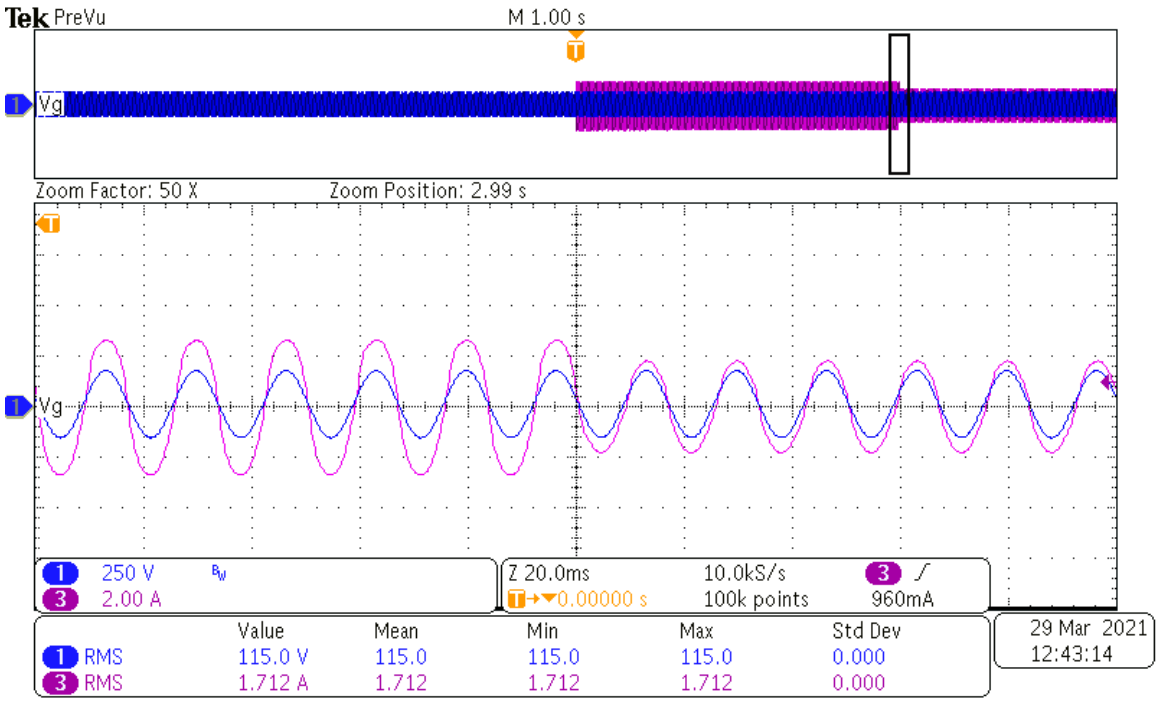


Figure 5-22. Zoomed-in step-down reference change

5.2.4 AC Power Quality

This section tests the MI power quality against prominent standards. The IEEE 1547 Standard states that a “DR (distributed resource) and its interconnection system shall not inject DC current greater than 0.5% of the full rated output current at the point of DR connection” [61], while IEEE 519 limits the Total Demand Distortion (TDD) of the output AC current to less than 5% [62]. Both standards are widely adopted by utilities, and form a significant portion California’s rule 21 requirements, which further prescribes unity PF operation as the default state for MI installations [28]. Rule 21 is important to MI manufacturers because California is the largest solar market in the US, where rooftop solar is mandatory for new homes built after 2020 [63]. The prototype performance in terms of these three metrics (DC current, PF and TDD).

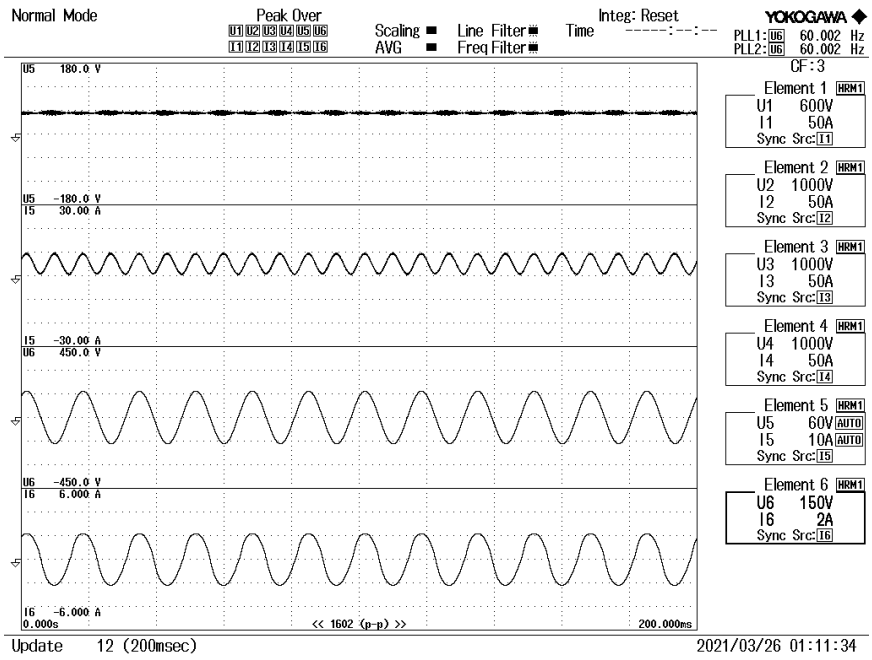


Figure 5-23. Power analyzer waveforms captured at 200 milliseconds intervals, from top to bottom: DC input voltage, pulsating input current, AC voltage, AC output current

According to IEEE 519 requirements, power quality measurements made with digital instruments should utilize a window width of 12 cycles of the AC frequency, which is approximately 200 ms for 60 Hz power systems. Hence all measurements calculated by the Yokogawa power analyzer used in this research are over 12 cycles of the fundamental AC frequency. Figure 5-23 shows that the key quantities are captured at a 200 ms update rate.

a) PF and DC current injection

Figure 5-24 shows the calculation results obtained from the power analyzer. The AC current and voltage are connected to elements 5 and 6 of the power analyzer, which shows that at a 200 W power level, the measured DC current is 4.91 mA, which is lower than the 8.0 mA prescribed by the standard. The PF is also recorded as 0.9963, which is approximately unity.

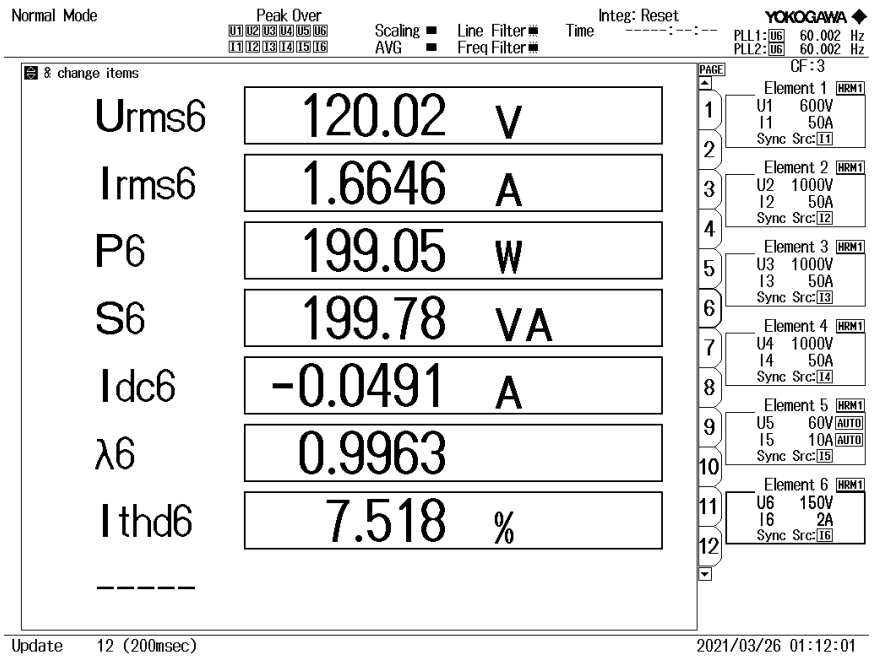


Figure 5-24. Power analyzer measurements showing DC current level and PF

b) Total Demand Distortion

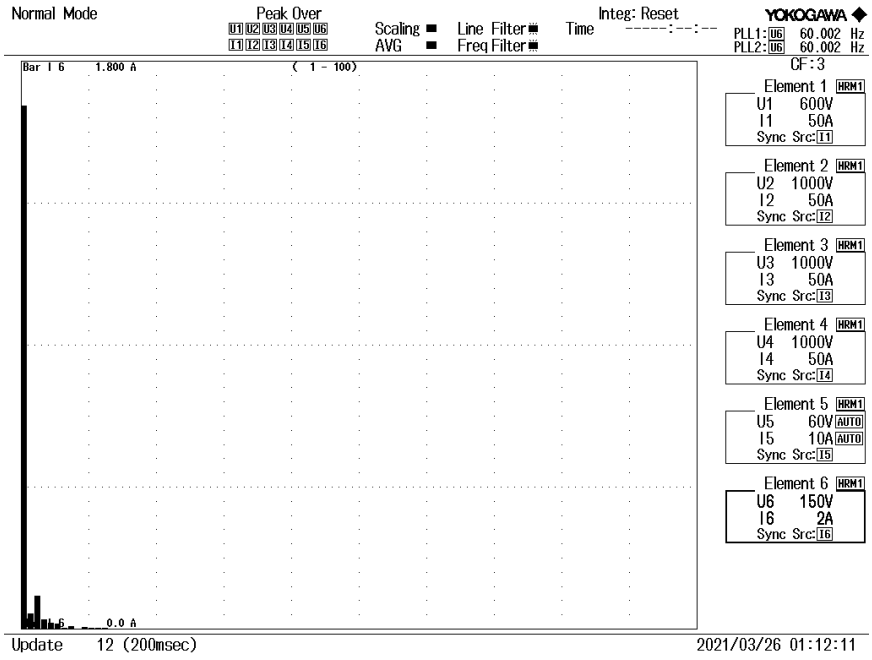


Figure 5-25. Harmonic spectrum obtained from power analyzer

Figure 5-25 shows the harmonic spectrum obtained from the power analyzer. The IEEE 519 TDD calculation is different from the THD measured in Figure 5-24, which the instrument computes using 100 harmonic orders of the AC current. IEEE 519 TDD emphasizes treatment of odd harmonics. Hence raw data is extracted from the instrument and characterized according to standard. The results are presented in Table 5-5 below.

Table 5-5. Total Demand Distortion of odd harmonic components

	Harmonic order, h, (odd harmonics only)					
	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 < h$	TDD
IEEE 519 Maximum Distortion	4.0	2.0	1.5	0.6	0.3	5.0
Prototype results	6.34	0.31	0.12	0.07	0.03	6.35

These results show that the higher order harmonics are properly attenuated and meet the IEEE 519 standard. However, the lower order harmonics, which fall below the cut-off frequency of the *CL* filter cause the prototype to fall short of the standard. Harmonic data extracted from the power analyzer reveals that the 3rd harmonic has an individual Harmonic Distortion Factor (HDF) of 6.324% and contributes the bulk of lower order harmonic distortion. A 50% reduction in the 3rd harmonic component will significantly improve the results, reducing the low order HDF from 6.34% to 3.35%, and the TDD from 6.35% to 3.36%, which will meet the IEEE 519 standard. This can be achieved by adding a selective harmonic compensator to the control system, which is the technique used by [40] to target the 3rd, 5th and 7th harmonic components and achieve low TDD.

5.2.5 Power Conversion Efficiency

The ISOMBI prototype power conversion efficiency measured by the Yokogawa Power analyzer is 70%, when the prototype supplies 200 W of power to the grid. Table 5-6 provides an estimated loss breakdown model for the prototype using its parameters. Although, the loss model only accounts for about 65% of experimental losses (due to difficulties in incorporating AC

proximity effects into AC winding resistance models), it still presents a reasonable approximation of dominant losses. From this, it is seen that the low efficiency can be primarily attributed to the FB transformer, which accounts for about 59% of modelled losses and 38% of experimental losses despite the neglect of AC proximity effect losses.

Table 5-6. ISOMBI prototype loss estimation model

Source	Type of loss	Value
Magnetics	Primary conduction loss	*12.00 W**
	Secondary conduction loss	*1.08 W**
	Leakage loss	*17.63 W*
	Core loss	*0.17 W*
Primary HF switch	Primary Switch Conduction loss	*2.45 W*
	Dynamic (Turn-on and Turn-off) loss	*5.37 W*
HF Diode	Conduction loss	*0.61 W*
	Reverse-recovery loss	*9.31 W*
Unfolding Circuit	IGBT conduction loss	*2.48 W*
	Bidirectional MOSFET loss	*0.36 W*
ESR losses	Filter inductor ESR loss	*0.82 W*
Total		*52.28 W*

* Neglecting AC proximity effects.

The loss breakdown is calculated based on techniques detailed in [64], [65], which do not include modelling techniques for proximity effects. It is predicted from [66] that modelling these effects would significantly increase the AC resistance, provide a better approximation of magnetic conduction losses and potentially account for the rest of the prototype's losses. This is because the wire used in constructing the FB transformer has a diameter (0.81mm) about 4 times larger than its penetration depth (0.21 mm), which according to [66] will at least double AC resistance and conduction losses. Magnetic leakage losses are also substantial, resulting from using a dissipative snubber to protect the primary MOSFET. Both sources of magnetic losses (conduction

and leakage) can be considerably reduced by improved magnetic design, such as using Litz wire [66] and applying interleaving techniques [47], [66]. Reverse recovery of the HF diode is another major source of power loss, and this can be eliminated by substituting the Silicon diode with a Silicon-Carbide (SiC) Schottky diode that exhibits virtually no reverse recovery.

5.3 Chapter Summary

This chapter presented prototyping and experimental results for the proposed ISOMBI topology. The prototype specifications were determined based on expressions derived in chapter 3 and controlled according to the techniques of chapter 4. The experimental setup was presented followed by results used to validate the steady-state analysis, demonstrate LF-interleaving, and verify closed loop control. Lastly, the performance of the ISOMBI was evaluated with respect to prominent standards such as IEEE 519, IEEE 1547, and California's rule 21. The results successfully validate the operating principles of the topology, proving that the ISOMBI can be applied as an alternative to conventional HF-interleaved MIs.

Steady-state expressions derived in chapter 3 were validated, and the closed loop transient response to an instantaneous 80 W change in power level verified the proposed dual loop compensation strategy. The prototype performed well in terms of PF and DC current levels, recording near unity PF (0.9963) and acceptable DC current (0.3%) levels. Although, a significant third harmonic HDF prevented the prototype from achieving low overall TDD, the solution is already familiar to FB MI designers, and a selective harmonic compensation scheme could be added to the ISOMBI in future iterations to improve its performance. Summarily, the experiments were successful in validating the ISOMBI's applicability as a MI.

Chapter 6 - Conclusions and Future Work recommendations

This concluding chapter summarizes the experimental results, followed by future work recommendations and finally, connects the results of the research back to the background information and research objectives presented in the introduction.

This research applied a novel single-stage FB topology as a LF-interleaved FB MI variant with a unique control strategy. A laboratory prototype was built and experimentally validated, with the following summary results:

6.1.1 Operating Principles

The operating principles of the proposed topology rests on two main concepts, namely the use of integrated magnetics and LF-interleaving. Both were successfully validated as it was proved experimentally that the same magnetic device could indeed be used as FB transformer and grid filter inductor, and that power processing could be shared between two HF switches without operating them simultaneously.

6.1.2 Steady-State Characteristics

The steady-state characteristics of any power conversion device need to be understood for specifying its circuit parameters, understanding component stresses, and choosing discrete components. As such, the steady-state characteristics of the ISOMBI topology were derived in chapter 3. Subsequently, these expressions were validated with experimental results that showed good agreement.

6.1.3 Control System

Closed loop compensation was applied to control the shape, magnitude, and phase of the MI prototype's AC output current. The ISOMBI topology presented a fourth-order system, which was approximated by second order systems to simplify controller design. AC output current control

was implemented using a dual control loop strategy. The experimental results show that the control system maintains steady-state stability, and responds to transient changes in power level. An 80 W instantaneous power step-up and step-down is used to verify this. The control system adapts satisfactorily.

6.1.4 AC Power Quality

Three AC power quality metrics are emphasized by utilities and standards. These are default PF, DC current level and TDD. The ISOMBI prototype performs well in the first two areas, and narrowly misses the TDD standard due to a significant HDF in the 3rd harmonic. The experimental results (obtainable at 200 W) show almost unity default PF at 0.9963, low DC current level of 4.9 mA (0.3%) and a TDD of 6.35%. Benchmark standards (at this power level) prescribe a default PF of 1, DC current level of 8 mA (0.5%) and TDD of 5%. While the ISOMBI passes the PF and DC current level standards, the TDD standard is narrowly missed by 1.35%. However, this can be improved in future work by adding a 3rd harmonic compensator into the controller as some other FB MI researchers have done.

6.1.5 Power Conversion Efficiency

Low power conversion efficiency (70%) is recorded by the experimental prototype. However, loss breakdown models show that this poor performance is primarily due to magnetic device conduction and leakage losses, resulting from crude manufacturing. Hence, improved magnetic manufacturing can be carried out in future work to aid the prototype achieve high efficiency.

6.2 Future work recommendations

This thesis focused primarily on validating the operating principles and DC-AC conversion capability of the ISOMBI when used as a FB MI topology. Having verified these, the research can be extended in the following ways:

- MPPT, and active power decoupling can be added to the ISOMBI. The MPPT voltage loop can be designed based on techniques presented in [53], which seems well suited to the ISOMBI and should be investigated further for possible adaptation. Similarly, some of the techniques presented in [67] could inspire active power decoupling techniques for the ISOMBI, and avoid using electrolytic capacitors.
- The prototype achieved default unity power factor operation. However, potential reactive power support can be explored. Although, phase-shifting the grid current compensator will result in severe distortion of the output grid current [65], A current decoupling circuit similar to [65] can be investigated. It may even be possible to achieve active power decoupling and reactive power control through the same current decoupling circuitry.
- The prototype's performance was not optimal, as its design prioritized manual assembly. Especially for magnetics, where a better design will reduce losses. Also, the prototype applied a dissipative RCD snubber to clamp voltage and protect the primary HF switch from the ringing caused by the FB transformer leakage. The work could be extended to investigate non-dissipative clamps to further improve efficiency. Then thermal performance could be evaluated and compared with the other FB MI variants.
- The TDD of the MI was close to the IEEE 519 standard but did not meet it, due to 3rd harmonic distortion. Future research could account for this by adding a 3rd harmonic compensator to the outer loop compensator. Even if only the third harmonic component is targeted halved, the standard will be met. Selective harmonic compensation can be found in the work of [40], which can be studied and adapted to the ISOMBI.

6.3 Thesis reflections

This thesis investigation was motivated by trends in the solar industry, such as increasing panel capacity, lower panel costs and increasing use of AC modules. Hence, it was deemed important to investigate FB MI topologies. The HF-interleaved FB MI was seen as a logical step for increasing the power rating of FB MIs, but it added an extra magnetic device to the bill of materials. This thesis proposed using the novel ISOMBI topology as an alternative MI, that uses LF-interleaving to avoid the additional magnetic device. The reflections of the thesis with respect to the themes presented in chapter 1 are as follows:

a) The research focused on FB MIs, due to their simplicity and built-in galvanic isolation. Three variants of the FB MI were reviewed, two of which are non-interleaved and the last one being HF-interleaved. The HF-interleaved variant has been proven capable of doubling the power rating FB MIs, with the primary cost being an added magnetic component. The review concluded by comparing and introducing the ISOMBI topology as a yet to be proven, LF-interleaved alternative to the HF-interleaved FB MI that avoids adding the extra magnetic component.

b) Following the review of FB MI topologies and their basic operating principles, the ISOMBI topology was presented as a potential LF-interleaved FB MI variant. ISOMBI operating principles, were designed around functionally integrated magnetic devices, and unfolding switches to create virtual reference points on alternate line cycles. This combination demonstrated how the ISOMBI could operate as a LF-interleaved MI topology.

c) The presented operating principles were used to derive an equivalent circuit, which was subsequently analyzed to reveal steady-state characteristics, parameter derivation, and small-signal dynamic models. Control system design posited that the main control difficulty (varying RHP zero) could be bypassed, by combining an inner loop primary current

compensator with an outer loop grid current compensator. The results of the analysis and control system design were verified experimentally. The AC power quality was also verified by measuring PF, TDD and DC current level, which were reasonable. TDD was slightly higher than expected but could be reduced using selective harmonic compensation in future iterations. Overall, the results show that the ISOMBI can be used as an AC module Micro-inverter topology.

d) The design of the proposed topology explored the properties of a step-up FB transformer that make it suitable for use as an integrated magnetic component. In FB transformer mode, two windings sharing a single-core control the flow of ampere-turns, while in grid filter inductor mode, one winding controls all the ampere-turns. Regardless of operating mode, however the magnetic core and gaps were exposed to the full ampere-turns. The ISOMBI topology and its operating principles were built around this integrated magnetics function, which was validated experimentally.

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