

Advanced Controls of Power Electronic Modules for  
PV-Based Plug-n-Play Dc Microgrids and Dc-Ac  
Grids Interface

by

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# Abstract

Billions of people are still living in energy poverty or living with no access to electricity. However, the conventional energy solution with large power plants and long transmission lines is no longer effective in these areas due to the high cost and geographical limitations. Meanwhile, to power up billions of people with conventional fuel-burn plants could generate giga tons more of carbon emission. Alternatively, photovoltaic (PV) based microgrid systems have been provided with new business models to make electricity affordable to households. At the same time, the price dropping of photovoltaic (PV) panels & energy storage devices and development of power electronic technologies make dc microgrid an attractive solution for the future distribution systems, especially for electrification in rural areas.

Microgrid, which integrates generation, energy storage and load, has become an important way of renewable energy harvesting. However, it still requires centralized plan, design and installation, which cause high capital investment and long leading time. These drawbacks have been strangling the development of microgrid, especially in rural areas. Plug-n-Play (PnP) microgrid has become a hot topic to address this problem. The PnP feature of microgrid can significantly simplify the design and installation process. The PnP feature also increases the expandability and flexibility of microgrids that the users can easily expand the microgrid system as their demand growing by simply adding new components.

However, the conventional hierarchical control method which relies too much on communication and central controller that has limited the development of PnP microgrid. This thesis studies advanced control methods for power electronic converters to achieve real PnP feature in dc microgrid systems and furtherly converting it to the utility ac grid. The proposed methods

have considered specific application criteria of each power electronic converter, while maximizing the modularity and scalability. In general, the dc part of the microgrid utilizes dc bus signaling technology with ultra-high modularity, while the dc-ac grid interface part utilizing communication-based control to achieve accurate power sharing and voltage regulation.

This thesis provides a thorough research on advanced control methods of power electronic converters for PnP microgrid and its interface to ac grids. Prototypes with proposed control methods are built. All studies are supported by experimental verifications.

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## Contributions of Authors

This thesis is comprised of five IEEE journal papers. Four of them have been published and one is under review. All the papers are with multiple authors. Dong Li is the first author in all the papers. The contributions of all authors for these papers are stated below.

**Chapter 2: D. Li and C. N. M. Ho, "A Module-Based Plug-n-Play Dc Microgrid with Fully Decentralized Control for IEEE Empower a Billion Lives Competition," *IEEE Trans. on Power Electronics*, Early Access.**

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared by me and reviewed by both authors. C. N. M. Ho provided guidance on the work. I carried on background studies, detailed control design, simulation verification, system implementation, and experimental evaluation.

**Chapter 3: D. Li and C. N. M. Ho, "Decentralized PV-BES Coordination Control with Improved Dynamic Performance for Islanded Plug-n-Play Dc Microgrid," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, major revision.**

In this chapter, I developed the idea and carried out background studies, analytical studies, simulation verification, system implementation and experimental test. C. N. M. Ho reviewed the manuscript and provided critical comments.

**Chapter 4: D. Li and C. N. M. Ho, "A Delay-Tolerable Master-Slave Current-Sharing Control Scheme for Parallel-Operated Interfacing Inverters with Low-Bandwidth Communication," *IEEE Trans. on Industry Applications*, vol. 56, no. 2, pp. 1575-1586, March-April 2020.**

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared

by me and was reviewed by both authors. I carried out background studies and developed detailed control method to solve the problem. The system implementation and experimental test are also done by me with guidance from C. N. M. Ho.

**Chapter 5: D. Li, C. Ho, and K. Siu, “Current Unbalance Problem of Paralleled Grid-connected Unipolar PWM Inverters with Common Dc Bus”, *IEEE Trans. on Industry Applications*, vol. 55, no. 6, pp. 7595-7603, Nov.-Dec. 2019.**

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared by me and was reviewed by other co-authors. C. N. M. Ho provided guidance on the work and K. Siu helped on developing experiment testbed and provided valuable advice on it. I carried on background studies, analytical studies, system implementation and experimental evaluation.

**Chapter 6: D. Li, C. Ho, L. Liu, and G. Escobar, “Reactive Power Control for Single-phase Grid-tie Inverters using Quasi Sinusoidal Waveform,” *IEEE Trans. on Sustainable Energy*, vol. 9, no. 1, pp. 3-11, Jan. 2018.**

In this chapter, the initial idea was developed by C. N. M. Ho. C. N. M. Ho did background study and provided guidance on the work. L. Liu helped on mathematical analysis. G. Escobar reviewed the paper and provided valuable comments and suggestions. The manuscript was prepared by me and was reviewed by another co-authors. I carried on mathematical analysis, system implementation and experimental evaluation.

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- D. Li and C. Ho, "A Module-Based Plug-n-Play Dc Microgrid with Fully Decentralized Control for IEEE Empower a Billion Lives Competition," *IEEE Trans. on Power Electronics*, Early Access. Chapter 2 of this thesis contains materials from this paper.
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- D. Li, C. Ho, L. Liu, and G. Escobar, "Reactive Power Control for Single-phase Grid-tie Inverters using Quasi Sinusoidal Waveform," *IEEE Trans. on Sustainable Energy*, vol. 9, no. 1, pp. 3-11, Jan. 2018. Chapter 6 of this thesis contains materials from this paper.

# Chapter 1 Introduction

## 1.1 Background

### 1.1.1 Microgrid

Nowadays, with the pressure from exhaustibility of natural resources, the electricity industry is moving from conventional energy sources to renewable energy sources. Different from conventional centralized generation plants, most of renewable energy sources have a distributed and intermittent characteristic. Microgrid integrates distributed generation (DG), energy storage and loads with local autonomous management [1.1][1.2], has become an important way to utilize renewable energy resources [1.3]-[1.5].

A microgrid can operate in grid-tied mode or islanded mode. In grid-tied mode, power exchange between microgrid and the utility grid allows trading activities which could provide revenue for the microgrid owner [1.6]. Microgrid could also support the main grid by exchanging reactive power or providing staggering power generation/consumption [1.7]. In islanded mode, microgrid could manage local power flow balance and maintain the local voltage and frequency (for ac microgrid) stability [1.8][1.9]. The ability of islanded mode operation provides users higher power availability towards the main grid power outage [1.10][1.11]. Islanded microgrid is also highly suitable for electrification in rural areas where the utility grid cannot reach due to economic or geographical reasons [1.12][1.13].

As the debate of ac power grid or dc power grid which has last more than decades, the debate also exists on microgrid. In general, there are ac microgrid, dc microgrid and dc-ac hybrid microgrid, which have been proposed and practically used [1.2].

### 1.1.2.1 AC Microgrid

Figure 1-1 shows the diagram of a typical ac microgrid. The ac microgrid takes advantage of grid connecting that it can be connected to the utility grid with point of common coupling (PCC) directly, and most bulk loads (motors) and generators are still in ac format. Due to the ac nature of traditional electric power system, ac microgrid is the most commonly used structure for microgrid applications in past years, especially for relatively large scale microgrids, e.g. marines [1.14] and remote diesel-powered communities [1.15].

However, ac microgrid requires complex power electronic converters and complicated control (reactive power control, frequency control, etc.) due to the system being ac-coupled [1.16][1.17]. It may require more than one power conversion stages for some components, like battery and PV, to connect to the ac bus, which will increase cost, power loss and reduce system reliability.

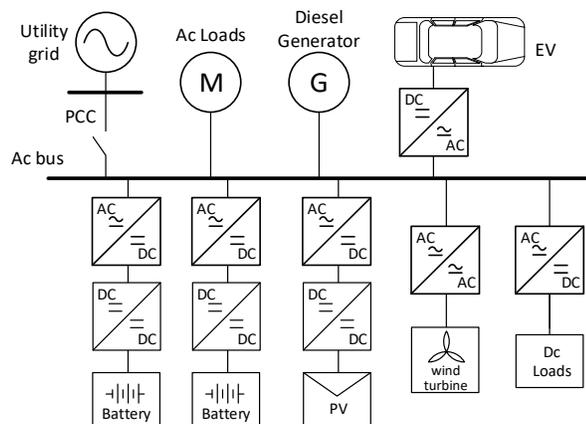


Figure 1-1. Structure of a typical ac microgrid system.

### 1.1.2.2 DC Microgrid

Figure 1-2 shows the diagram of a typical dc microgrid. Dc microgrid is an emerging technology due to the increment of modern dc loads and dc micro-sources (PV, battery) [1.18]. Compared to ac microgrid, dc microgrid has less power conversion stages and simple converters can be used [1.19]. It also has less power quality and stability issues [1.20][1.21]. More and more recent commercial microgrids are tending to use dc architecture, e.g. for data centers [1.22], and even replace ac microgrids in many areas e.g. marine [1.23] and remote communities [1.24].

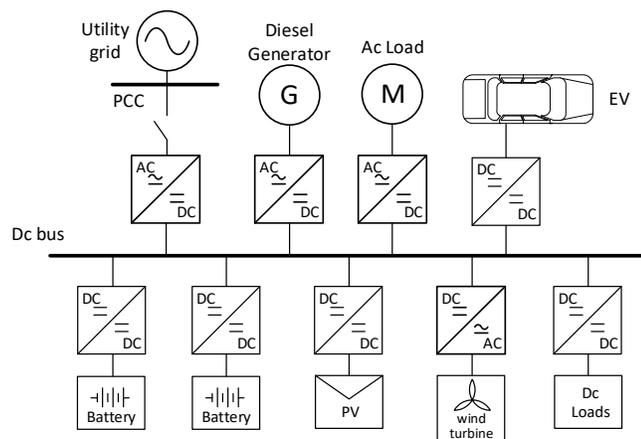


Figure 1-2. Structure of a typical dc microgrid system.

### 1.1.2.3 AC-DC Hybrid Microgrid

Figure 1-3 shows the diagram of a typical ac-dc hybrid microgrid. Due to the presence of dc loads, dc distributed sources and dc energy storage, and considering the century long ac power system, ac-dc hybrid microgrid has gained growing interests. The topology of hybrid microgrid is basically a combination of ac microgrid topology and dc microgrid topology with an interlinking

ac-dc converter [1.25][1.26]. Hybrid microgrid structure has also been widely used in many commercial projects [1.27]-[1.29].

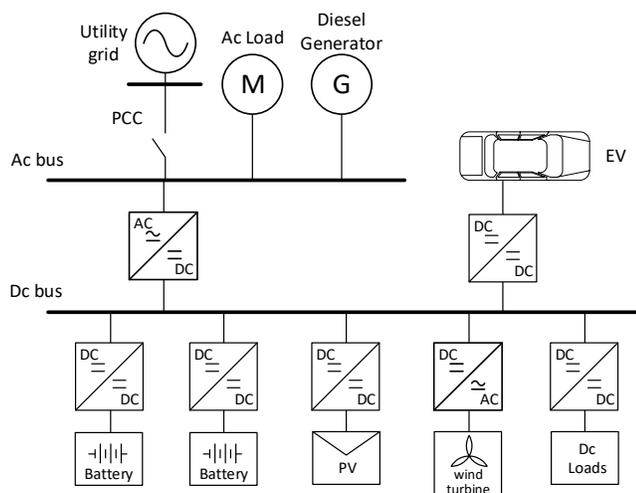


Figure 1-3. Structure of a typical ac-dc hybrid microgrid system.

The study of advanced control of power electronic converters for PnP microgrid in this paper is mainly targeting dc microgrid, due to its advantages of high efficiency, better power quality, low cost and simple control. The study can also be extended to ac microgrid or hybrid microgrid.

### 1.1.2 Power Electronic Converters in DC Microgrids

Power electronic converters are key elements of a microgrid as interfaces of various of microgrid components. Power conversion, power flow control and voltage regulation in a microgrid all rely on coordination of power electronic converters. In this section, several typical converters used in microgrids are introduced, in terms of functions, topologies and control.

### 1.1.2.1 DC-DC Converter for PV

The output of PV cells has a complex relationship with solar irradiance, temperature, etc., which produces a non-linear output characteristic [1.30]. The major task of a PV converter is to achieve Maximum-Power-Point-Tracking (MPPT). PV converter with MPPT control can keep the PV panel at its maximum conversion efficiency. The input voltage of PV converter varies due to the MPP change, and the output voltage is usually maintained at a nominal value by other microgrid components as a voltage source.

Due to that PV panel operating voltage is always less than a certain open circuit voltage, the output voltage is usually designed to be higher than the maximum PV string voltage. Thus, a boost type converter is commonly used for PV converters [1.31]. For interconnection to an ac grid, topologies with isolation are usually used to address the leakage current problem [1.31].

In certain cases of islanding mode operation, e.g. energy storage cannot absorb surplus power, PV converter should be able to operate under off-MPPT mode [1.32]. The simplest way is to completely shut down the PV converter which reduces PV output power to zero. With advanced methods, the PV converter can operate in output voltage control mode, e.g. droop control, to maintain the output voltage by adjusting PV operating point [1.33][1.34]. In chapter 3 of this paper, an advance PV converter control method is proposed and studied.

### 1.1.2.2 DC-DC Converter for Battery Energy Storage

Energy storage system is important for a microgrid system that it can restrain the power fluctuation of distributed renewable energy resources. A battery energy storage (BES) system is comprised of serial and parallel connected battery cells. The energy balance of battery cells is taken care by Battery Management Systems (BMS), which is not studied in this thesis. The dc-dc power converter system controls output voltage and current of the BES system with proper power sharing [1.35].

Besides basic charging/discharging control, the BES converter should have ability to regulate bus voltage and achieve power-sharing among paralleled BES systems. Usually droop control is used in BES converters to achieve both voltage regulation and power sharing simultaneously as primary control. To prolong the service life of BES systems, the State of Charge (SoC) of each BES system should be kept balanced with the others [1.36]. The conventional way to achieve SoC balance requires communication which reduces system modularity and reliability. Paper [1.35][1.36] proposed SoC automatic balance techniques with modified droop control that, by changing droop coefficient according to SoC, a self-convergence characteristic can be achieved.

### 1.1.2.3 DC-DC Interfacing Converter

In a dc or hybrid microgrid system, multiple dc buses with different voltage levels can be used. For example, for a household level, 48V is reasonable for safety considerations with acceptable distribution loss in a small area. However, for a community dc bus, the voltage should be higher, e.g. 200V-400V, to guarantee high distribution efficiency. The dc-dc interfacing converter interfaces different dc buses as a dc-dc power electronic transformer. The dc-dc interfacing

converter should be isolated, bidirectional and have a high boost ratio. Usually Dual Active Bridge (DAB) and LLC resonant topologies are used for dc-dc interfacing converters [1.37]. Depending on microgrid operation mode, the dc-dc interfacing converter could control one of the low-voltage side voltage and high-voltage side voltage or at constant power control.

#### 1.1.2.4 DC-AC Interfacing Converter

The dc-ac interfacing converter connects the main dc bus to ac bus or the utility grid. In islanded mode, for hybrid microgrid, the dc-ac interfacing inverter need to maintain the ac bus voltage (magnitude and frequency). For the study of dc microgrid in this thesis, the dc-ac interfacing converter will be cut off in islanded operation. In grid-tied mode, the dc-ac interfacing converter need to control dc bus voltage or at constant power control. Furthermore, as requested by recent regulation, the grid-tied PV system should have ability to provide leading or lagging reactive power to the grid [1.38], which relies on reactive power delivery of dc-ac interfacing converters.

Due to the application of interfacing a microgrid to the utility grid, the power flow on this interfacing converter could vary a lot due to generation and load conditions. To avoid light load effect, using parallel dc-ac modules instead of a single bulky dc-ac converter can keep the system always operate around rated value [1.39][1.40].

Full-bridge converter is the most commonly used dc-ac topology. In this thesis unipolar full bridge converter is used due to its low semiconductor cost, high efficiency and small current ripples [1.41][1.42].

### 1.1.3 DC Microgrid Control Methods

A microgrid system consists of various distributed energy sources, energy storage systems and loads, and it can operate under grid-tied and islanded mode. Thus, microgrid control system is a complex multi-target control system dealing with issues of power sharing, voltage regulation and power flow control, SoC balance etc. Usually the hierarchical control is used on most of conventional microgrid systems [1.43]. Table 1-I shows each layer's function in the hierarchical control structure.

TABLE 1-I MICROGRID HIERARCHICAL CONTROL

Primary control	Local voltage/current control and load sharing
Secondary control	Voltage restoration (compensate droop control steady state error)
Tertiary control	Power flow control between MG and grid, SoC balance, Optimization, etc.

#### 1.1.3.1 Primary Control

Primary control is for local voltage & current regulation and power sharing among microgrid units. Generally, there are two types of primary control, droop-based control and communication-based control [1.44].

Droop control is most commonly used primary control method. It takes advantage of easy implementation and only require local information but has drawbacks of inaccurate power sharing and a steady state voltage regulation error. Figure 1-4 shows the mechanism of typical droop control.

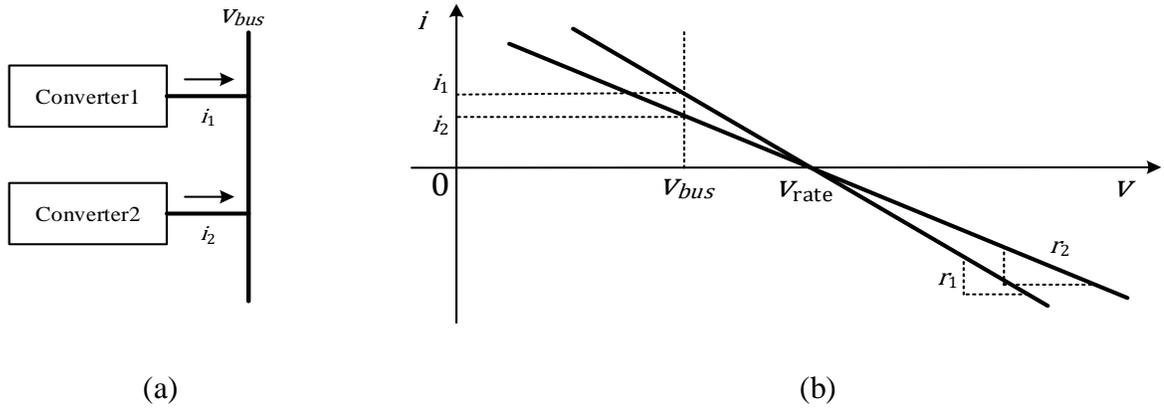


Figure 1-4. Power sharing mechanism of droop control.

Two types of droop controllers are commonly used, namely V-I droop control and I-V droop control [1.45]. Figure 1-5 (a) shows the control diagram of a typical V-I droop control system, which is generated from the following equation,

$$v_{bus,ref} = V_{rate} - r \cdot i \quad (1-1)$$

Where  $r$  is the virtual droop resistance. While V-I droop control provides a voltage reference, I-V droop control, as shown in Figure 1-5 (b), directly provides a current reference to the converter following,

$$i_{ref} = m(V_{rate} - v_{bus}) \quad (1-2)$$

Comparing (1-1) and (1-2), the equations of V-I and I-V droop control are equivalent by making  $m = 1/r$ .

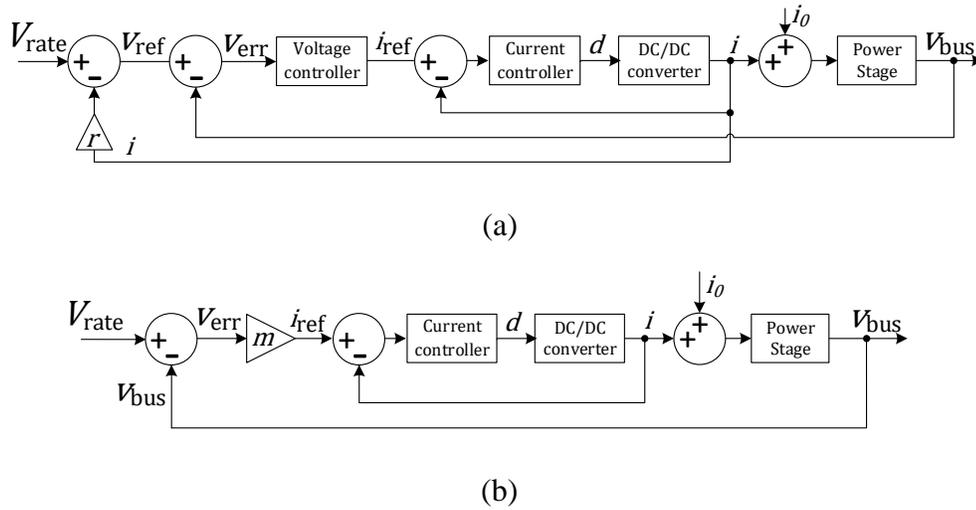


Figure 1-5. Diagram of (a) V-I droop control, and (b) I-V droop control.

Communication-based control, of which the most popular one is master-slave control, has accurate power sharing and voltage regulation performance but requires communication to share local information to other units. Figure 1-6 shows the diagram of a typical master-slave control system. Each slave converter has a current controller. A sole voltage control is located in the master module, which sending out current reference to all slave modules. Thus, it is usually used in applications require very high performance or operating flexibility [1.46].

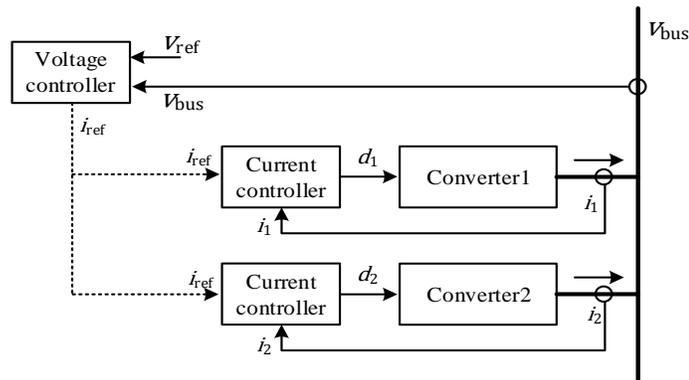


Figure 1-6. Typical communication-based power sharing control.

### 1.1.3.2 Secondary Control

Secondary control is an improvement to droop control to improve the power sharing accuracy and remove voltage regulation error. It can be achieved by a central controller or a distributed multi-agent system [1.47][1.48]. Figure 1-7 shows a typical diagram of microgrid secondary control. The system is still stable without the secondary controller. The secondary controller monitors dc bus voltage and power sharing error and provide a compensation information (an add-on to  $V_{rate}$ ) for each droop-controlled converter to remove voltage error and power-sharing error.

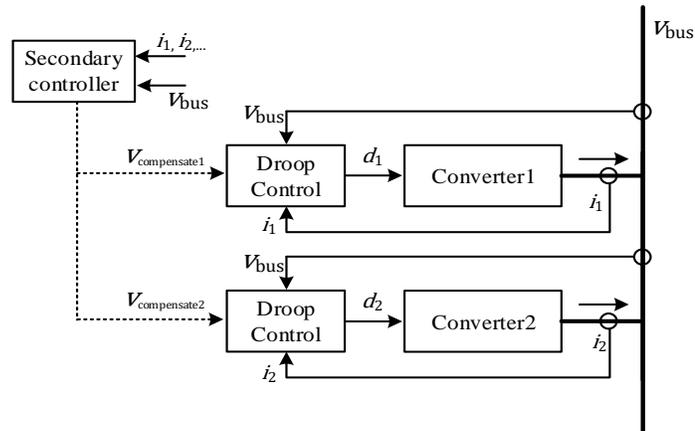


Figure 1-7. Diagram of microgrid secondary control.

### 1.1.3.3 Tertiary Control

Different from primary and secondary control focusing on short-term power management, the objective of tertiary control is to achieve long-term energy management in an optimal way [1.49]. Tertiary control determines microgrid operation mode and power flow between microgrid and the upper level grid. Tertiary control also monitors SoCs of all BES systems and provide adjustment to achieve SoC balance [1.36]. Tertiary control needs to collect data from all microgrid

components. Like secondary control, it can be achieved by a central controller or a distributed multi-agent system [1.43].

Secondary and tertiary control rely on communication networks and a central controller or distributed agents, which could significantly reduce system modularity and reliability. This thesis focuses on primary control of power electronic converters to achieve full-function plug-n-play microgrid systems with less dependency on secondary and tertiary control.

#### 1.1.3.4 Decentralized Control

The hierarchical control as introduced above highly depends on communication network. The control structure can be classified into centralized control (if a central controller is used) and distributed control (if multiple clients are used instead of a central controller) [1.51][1.52]. Another control structure is called decentralized control structure, where the conventional hierarchical control cannot be applied. Decentralized control has ultra-high resiliency with no risk of single point failure and ultra-high flexibility & scalability that no manager is need. However, it is very challenging to set up a fully decentralized control system for microgrid due to complicated coordination [1.53]. This thesis looks forward to achieving fully decentralized control in PV-based dc microgrids.

#### 1.1.4 Plug-n-Play Microgrid with Power Electronic Modules

As mentioned, microgrid integrates distributed generation, energy storage and load, which is a promising distribution format in future smart grid, especially for remote power supply. However, the common approach to establish a microgrid requires a central design, installation and operation

process. As a result of this top-down approach, professionals are required, the cost (including design, installation and operating) are high, the lead time is long, and the future expansion of MG will be difficult. These drawbacks are strangling development of microgrids, especially in rural areas.

To overcome the drawbacks of conventional central microgrid, plug-and-play (PnP) microgrids are proposed to achieve deploy flexibility. Concepts like flexible microgrid structures, modular microgrids and microgrid clusters have been proposed. Paper [1.50] has pointed out few major concerns to achieve PnP in dc microgrid system, among which the most important is how to avoid communication which may spoil the scalability and reduce system reliability, and how to design a decentralized control system independent from total number of modules to achieve a real scalable design. Paper [1.53][1.54] studied distributed control technologies of microgrid clusters based on peer-to-peer communication. Paper [1.55][1.56] provided decentralized solutions that the MG system can become independent from communication and realize PnP. However, most of these existing scalable solutions have limitations in terms of,

1. Single expansion level limits system scale.
2. Extra converters are required to interconnecting multiple units.
3. Can only achieve basic power balance. Features like SoC balance and mode adaption are not considered.

### 1.1.5 Proposed Design

This thesis studies advanced controls of power electronic modules for dc PnP microgrid and technologies interfacing it to the ac utility grid. Figure 1-8 shows the microgrid structure with

proposed design. It can be analyzed in two separated parts with specific design considerations for each part, as yellow circles indicated in Figure 1-8.

Part 1 is a dc microgrid consists of multiple microgrid clusters. In each cluster, multiple power units are connected to low voltage dc bus. Each unit has a PV generation module and a BES module. Multiple clusters are connected to a high voltage public dc bus with gateway converters, which could be a simple boost converter to increase the voltage from 48 V to 200 V. Part 1 consists of PV modules, BES modules and gateway converter modules. The key design consideration for part 1 is modularity and availability, that users may need to establish a network in short time with basic electrical engineering knowledge. Thus, the voltage level is low (48V) to guarantee safety that untrained people may operate but high enough to get good distribution efficiency for a household range. The control in part 1 is completely decentralized that the installation can be further simplified, and the reliability & robustness can be improved by getting rid of the risk of communication failure. While all equipment being coupled to dc buses with power electronic converters, certain amount of voltage variation is allowed on the dc buses. Thus, dc bus voltage signaling can be used for the decentralized control in part 1. Chapter 2 and chapter 3 of this these will introduce this part 1 in detail.

Different from part 1 which is a free growing network down to the household level, part 2 is a grid interface, which is operated by professionals and have a high requirement on performance. This part should have ability to operate under constant power control (active/reactive power) or dc bus voltage control (scheduled BES charging/discharging) both of which requires a command input. And the paralleled dc-ac converter modules are located close to each other. Thus communication-based control is developed for part 2 to achieve advanced functions and better performance. To keep high modularity and low cost, the communication is based on wireless

modern low-bandwidth digital communication modules. Chapter 3 to chapter 5 of this thesis will introduce part 2 in detail.

Table 1-II shows comparison of design considerations of part 1 and part 2.

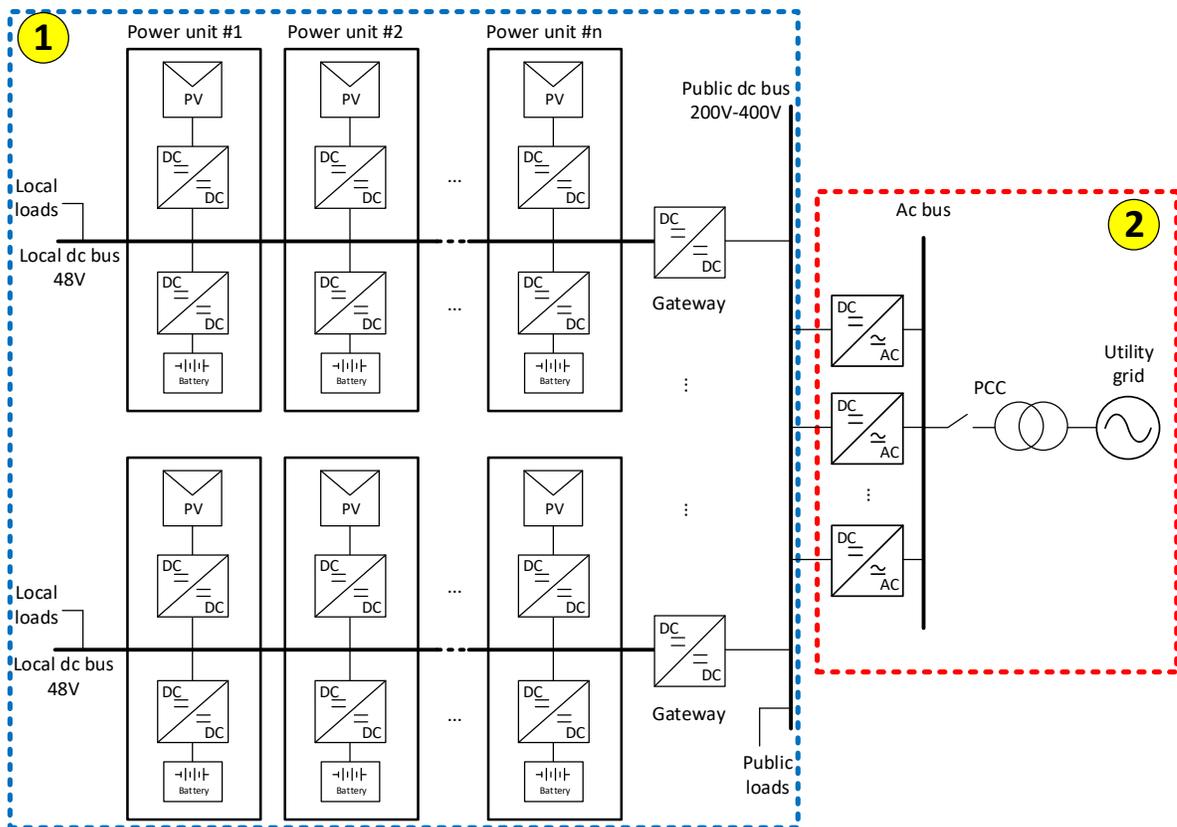


Figure 1-8. Microgrid structure with proposed power electronic modules.

Table 1-II DESIGN CONSIDERATIONS FOR POWER ELECTRONIC MODULES

	<b>Part 1 – dc microgrid cluster</b>	<b>Part 2 – grid-interface</b>
<b>Involved converters</b>	PV converter, BES converter, dc-dc interfacing converter	dc-ac interfacing converter
<b>Involved person</b>	Users or untrained people.	Professionals.
<b>Distance among modules</b>	Clusters can be far from each other.	Converter modules are located close to each other.
<b>Key consideration</b>	Modularity, power availability, robustness, safety.	Power quality, efficiency.
<b>Control method</b>	Distributed control.	Communication-based control.
<b>Design challenges</b>	Coordination of different type of modules without communication.	Apply low-cost and high-efficiency topologies and communication devices in parallel operation.

## 1.2 Research Objectives

Microgrid, as an emerging technology and an important format to harvest renewable energy, plays an increasingly critical role in the future smart grid. However, the conventional centralized design, implementation and operation method is strangling development of microgrid. Plug-n-Play (PnP) microgrid with modular power electronic converters becomes a hot topic in both academic and industry areas. The PnP of power electronic converters is a challenge to microgrid control technology. The ultimate goal of this thesis is to develop advanced control technologies for enabling PnP dc microgrid and its dc-ac interface to achieve high modularity, flexibility and

relatively high reliability, robustness and cost-effective design. The specific research objectives are,

- Identification of the different application criteria and control requirement on different power electronic converters connected to microgrid.
- Use dc bus voltage signaling technique to achieve mode adaption and converter coordination in dc microgrid with two voltage levels. Achieve automatic SoC convergence and PV off-MPPT mode transition with modified droop control simultaneously with dc bus voltage signaling.
- Study system stability in storage-dominating mode and generation-dominating mode. Design control method with BES compensation to improve generation-dominating mode performance.
- Use master-slave control to achieve accurate power sharing in grid interfacing converters. Design controller robust to communication delays.
- Design controller to enable usage of high-efficiency low-cost unipolar topology in parallel operation and enable reactive power delivery to meet the industrial standard.

### 1.3 Research Contributions

The outcomes from this research work can help the development of PnP microgrid, where a series of new control methods is introduced. While the thesis using a dc microgrid as example, the control design methods for power electronic modules can be expanded to other types of microgrids. All designs are tightly related to application requirement.

For dc clusters part, the control is designed in a fully decentralized manner, to achieve high modularity and reliability. Design of controllers for each type of converter is introduced. Automatic SoC convergence, seamless mode transitions can be achieved simultaneously with dc bus voltage signaling using the proposed control design.

For the grid interface part, a communication-based master-slave controller is used, with reactive power deliver ability and tolerability to communication delays. A communication delay compensation method is developed to stabilize parallel converter system towards communication delays involved by modern communication tools. The thesis also studies current unbalance problem in paralleled unipolar PWM converters with a control method, which enables usage of unipolar PWM converter in parallel operation. A reactive power delivery method which is suitable for parallel unipolar PWM converters with low-band-width communication is also proposed, which could also solve the problem of reactive power delivery with unfolding topologies.

The developed control methods can efficiently and effectively manage the power balance of a dc microgrid with similar capability as conventional hierarchical control. They also offer more flexibilities, cost-effectiveness and robustness compared to conventional microgrid control with the plug-n-play capability.

Besides grid-tied microgrids, the PnP feature provided by proposed control methods could benefit most the rural electrifications. The power electronic modules are portable, and the installation does not need professionals. An off-grid dc microgrid can be created in very short time with PnP microgrid modules. The expansion is also flexible by simply adding more modules. These features allow users to bottom-up build a power network in an organic way, which is promising to help electrification in energy poverty area.

To demonstrate the viability of the designed control methods, experimental prototypes has been built and test with proposed control methods. Three dc power units are built to test the microgrid dc side operation. Each unit consists of a PV converter and BES converter. Two unipolar full-bridge converters with Zigbee communication modules are built to test the operation of grid interface. The measured results agree analytical studies well.

## 1.4 Thesis Structure

This thesis is in a journal-paper-based sandwich thesis where the core of this thesis is comprised of five journal papers. Four of them have been published and one is under review. A total of seven chapters are presented in this thesis.

In Chapter 1, an introduction is given which covers the concept and typical configurations of microgrids, common power electronic converters in microgrids, common microgrid control methods and the development of Plug-n-Play microgrid. The research objective, advanced control methods of power electronic modules for PnP microgrid, is explained and contributions of this thesis are stated.

In **Chapter 2**, a PnP dc microgrid with fully decentralized control is introduced. It introduces the idea of mode adaption using dc bus voltage signaling technology. Control for each type of converter is introduced in detail. PV converter can operate in MPPT mode and voltage control mode with seamless mode transition. BES converter has a SoC self-convergence character with modified droop control, which also creates a SoC-voltage ramp character on dc bus, which can be further used to balance SoC among clusters.

In **Chapter 3**, among the proposed control structure in last chapter, the PV-BES coordination

control is specifically studied. The stability of dc microgrid under generation-dominating mode (PV voltage control) is studied with small signal analysis. The variation of PV parameters could significantly affect the control bandwidth and phase margin. A PV-BES coordination control is proposed with BES high-pass-filter loop, makes the system more robust towards PV parameter variations and improves system voltage regulation performance under PV voltage control.

Different from the last two chapters which focus on decentralized control for the dc network, this chapter studies modular design of dc-ac grid interface, which uses communication-based control to achieve accurate power sharing and voltage regulation. In **Chapter 4**, the effect of low-bandwidth communication in a master-slave controlled system is studied with small signal analysis. A slave module low-pass-filter and feedforward loop design are proposed. With proposed design, the system is more robust towards communication delays, which makes low cost modern communication tools, e.g. Bluetooth, Zigbee, can be used in control layer.

In **Chapter 5**, to apply unipolar PWM full bridge topology to parallel operation, a switching current sensor method is proposed to solve the unbalance inductor current problem. Small signal models are established to identify the problem, which is caused by interfered current control loops. With proposed method, unipolar topology can be used in parallel operation while keeping its low cost and high efficiency, by simply adding one more current sensor.

With low-cost communication devices and unipolar topology as discusses in the last two chapters, the reactive power delivery will be a challenge that a tiny mismatch of phase information could cause significant short circuit. In **Chapter 6**, a quasi-sinusoidal current waveform is proposed for reactive power delivery. The proposed method keeps same zero-crossing point of grid current and voltage but can deliver reactive power by adding harmonics. Using conventional four-quadrant reactive power delivery method, the parallel unipolar converters may operate with

different phase shift which will cause short circuit on dc link. The proposed method enables reactive power delivery to meet the industrial standard VDE-AR-N 4105 on unfolding topologies and unipolar topologies with a trade-off of harmonic current.

In the last chapter (Chapter 7), according to the work presented in this thesis, conclusions are given and recommendations for future work are listed.

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## Chapter 2 A Module-Based Plug-n-Play Dc Microgrid with Fully Decentralized Control

The work described in this chapter was published in the following paper: D. Li and C. N. M. Ho, "A Module-Based Plug-n-Play Dc Microgrid with Fully Decentralized Control for IEEE Empower a Billion Lives Competition," *IEEE Trans. Power Electron.*, Early Access. The work was also presented in part as a conference paper at the IEEE Applied Power Electronics Conference and Exposition 2020. Part of the work was also filed as a patent application, US 63/029,913.

In this chapter, a PnP dc microgrid with fully decentralized control is introduced. It introduces the idea of mode adaption using dc bus voltage signaling technology. Detailed design for each type of converter is provided. The mechanism of mode adaption control is explained.

### 2.1 Abstract

In this chapter, a module-based plug-n-play (PnP) dc microgrid is introduced to help rural electrification. It provides a bottom-up way to form a microgrid (MG) with multilayer expandability and Plug-n-Play feature. The module-based MG overcomes the drawback of conventional MG that requires central design and implementation which leads to high upfront cost and long lead time. It provides an organic way to form a MG that allows user to scale up the system as their demands growing, and fully utilize the existing resources. The proposed MG module is expandable on different layers that can meet requirements of customers with different power consumption requirements. Each module, which contains PV generation and energy storage, can work as a standalone solar home system. Multiple modules can be connected as a group to scale

up the local power supply. Groups can be interconnected through a public bus with gateway converter modules to form a community network, which can supply public usages and enables power exchange in a community range with relatively high distribution efficiency. The control of proposed MG is in a fully decentralized manner, that central control and communication network can be omitted, which makes the system more user friendly and highly robust. Detailed design, analysis and implementation of the proposed PnP MG is provided in this chapter. Simulation and experimental results have been provided to verify the concept and analytical study.

## 2.2 Introduction

According to International Energy Agency, over 3 billion people are living in energy poverty and more than 1 billion people are living with no access to electricity [2.1]. It has been a challenge to develop new ways to power up these unelectrified areas. The high cost and geographical limitations in most of unelectrified areas make the conventional power system, which relies on central generation and long-distance transmission, no longer effective to solve the current energy poverty problem [2.2][2.3]. Meanwhile, to power up billions of people with conventional fuel-burn plants could generate giga tons more of carbon emission. Alternatively, Photovoltaic (PV) based off-grid dc microgrid systems have been developed with new business models to make electricity affordable to households in energy poverty areas [2.2].

Most of the less-electrified regions are in Africa and South Asia where is rich of solar resources. This makes solar photovoltaic (PV) generation a competitive way towards conventional generation. The distributed character of PV generation relies on microgrid (MG) as an effective way to utilize solar energy [2.4]-[2.7]. MG integrates generation, load and energy storage, which can constantly provide relatively high power and support a variety of loads. However, the common

approach to build a MG requires a centralized design, installation and operation process. As a result of this top-down approach, professionals are required, the cost (including design, installation and operating) are high, the lead time is prolonged, and the future expansion of MG will be difficult. With conventional approach, the MG capacity will be overdesigned or insufficient in most of time due to its difficulty of expanding. And it is hard for people living in energy poverty to raise money for the upfront investment. These drawbacks are strangling development of MG in rural areas.

To overcome the drawbacks of conventional central MG by making MG plug-and-play (PnP) to be easily scaled up, more and more researches on flexible MG structures, modular MGs and MG clusters have been proposed [2.8]-[2.12]. Paper [2.13] has pointed out few major concerns to achieve PnP in MG system, among which the most important is how to avoid communication which may spoil the scalability and reduce system reliability and how to design a decentralized control system independent from total number of modules to achieve a real scalable design. Paper [2.14][2.15] studied distributed control technologies based on peer-to-peer communication. [2.14] proposed an Open Energy System that allows independent nanogrids being interconnected as a microgrid, which relies on a peer-to-peer control system. Similarly, paper [2.15] proposed a distributed cooperative control system. Though the central controller is eliminated, the system still highly relies on communication network, which may not be preferred in a rural application that communication could increase cost and reduce reliability as well as the scalability. Paper [2.16]-[2.18] provided decentralized solutions that the MG system can become independent from communication and realize PnP. Paper [2.16] proposed a scalable MG architecture based on droop control that only relies on local information which is highly suitable for rural electrification. Similarly, paper [2.17] proposed a scalable MG with centralized generation and decentralized

home power management units (PMUs). Paper [2.18] proposed a Self-Organizing NanoGrid (SONG) system, which is based on a low-cost multiport converter unit.

Figure 2-1 (a) shows a typical structure of scalable MG. Most of prior arts of scalable microgrid are based on this general structure, where the control, topology and scale may vary in different projects. The expansion is based on a dc-dc converter as an interface of each unit. The advantage of this structure is simple control that each unit is isolated by the interfacing dc-dc converter and just needs to manage power balance of its own. However, the disadvantage is also obvious. Firstly, since the house load is connected to local bus, the available power to the load is limited by the rating of interfacing dc/dc converter regardless of number of units. Secondly, when power goes from one unit to another unit, it needs to go through interfacing converter two times, which could be lossy.

Figure 2-1 (b) shows the scalable microgrid structure used in paper [2.12]. Instead of having PV modules in each unit, this structure has a centralized PV generation. The Power Management Units (PMU) installed at each user only contains BES and loads. Thus, the control of each unit can be significantly simplified without local generation. The available power on the 12V bus is also limited by the single converter capacity. Power on the 48V cluster bus is scalable. However, due to the centralized generation, the modularity is reduced that a single unit cannot work without generation, and it is economic viable only for relatively large communities.

Figure 2-1 (c) shows the proposed PnP microgrid structure. Firstly, in this structure, each unit has BES and PV generation which can be used as a standalone unit. Secondly, since the connection of multiple units uses local bus directly without any interfacing converters, the power on the 48V bus is scalable without single converter limit and the loss is reduced without interfacing

converters. Thirdly, to interconnect multiple groups, an interface converter, or called a gateway converter, is used to create a relatively high voltage distribution network.

As shown in Figure 2-1 (c), the proposed MG has three expansion layers. Firstly, a single power unit (PU), can work as a standalone SHS. Each PU contains PV generation and BES with a common 48V dc bus as output. Secondly, multiple PUs can be interconnected directly with the 48V local dc bus as a group. Thirdly, multiple groups can be connected to a public dc link (200V-400V), through gateway converters. Inter-group expansion is at community level and allows power exchange among households and pooling power for public usages.

Conventionally, for central-planned commercial dc microgrid, communication-based hierarchical control structure is commonly used [2.19]-[2.21]. The involvement of control center and communication network significantly reduces system modularity. To better introduce PnP into microgrid, the study on decentralized control become popular. Literatures [2.14]-[2.15] and [2.22]-[2.24] studied decentralized control of microgrid. Though the central controller is removed, they still rely on communication network. Most of studies on communication-less control of microgrid only focus on primary control and system stability [2.25]-[2.27], while some other important aspects of microgrid control, e.g. State-of-Charge (SoC) balancing, control mode selection, are overlooked. In this paper, to keep a high modularity and reliability, a fully decentralized and communication-less control is applied to the proposed MG system. The direct bus connection inside a group increases the difficulty of coordinating all the parallel Battery Energy Storage (BES) converters and parallel PV converters. It is challenging to achieve power sharing, BES SoC balancing, PV-BES coordination, and inter-group coordination at the same time in a communication-less manner. The proposed control is based on modified droop control, of which the stability is as good as common droop-controlled systems. With proposed control methods, units

can be bus interfaced with a well-designed droop control system based on dc bus signaling technology [2.28]-[2.29].

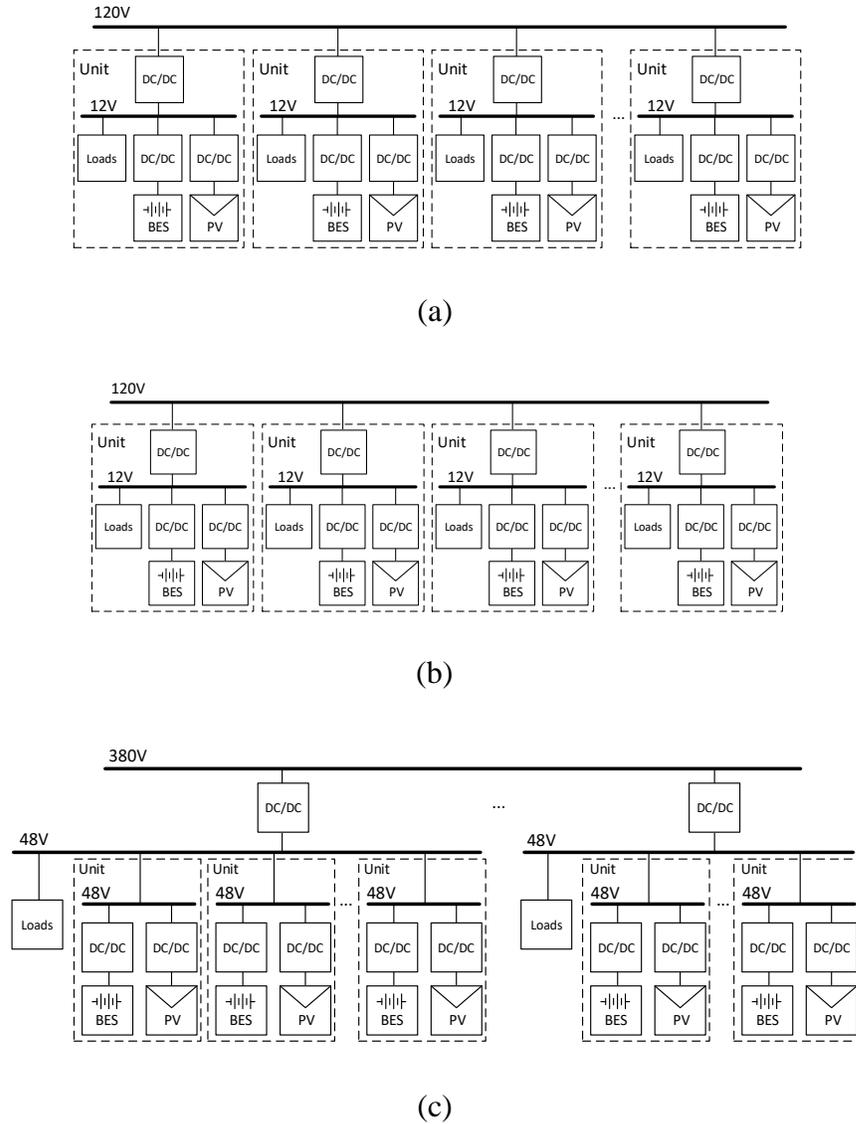


Figure 2-1. Prior-art and proposed scalable microgrid structures, (a) scalable microgrid structure used in [14]-[16], [18], (b) scalable microgrid structure proposed in [17], (c) PnP microgrid proposed by this paper.

Control for each PU is fully decentralized and does not need any modification in different expansion levels and operation modes. Grid-connection is possible when a grid is available.

The proposed MG solution has advantages of,

- 1) It allows a bottom-up way to establish a power network. Users can start with single PU and expand the system as demand and budget growing, and interconnect the system with their neighbors’.
- 2) Separate local household-level bus and public dc bus allows using of two voltage levels. The low voltage 48V household-level bus is safe for untrained people to use and install. High voltage public bus keeps low distribution loss.
- 3) Public dc bus is isolated from each local dc bus with gateway converters. Reliability is improved that failure can be isolated within the local bus range.
- 4) Group expansion can be achieved without interfacing converters, which reduces cost and power loss.
- 5) The modular design of PU and gateway converter could significantly reduce the design cost of MG and enables mass production.
- 6) Fully decentralized control keeps high reliability and robustness, saves cost on communication devices.

The proposed MG has a bottom-up building feature that allows system growing organically as the demands growing. The feature that combines advantages of conventional SHS and central-designed MG could significantly reduce the difficulty of developing MGs in rural developing areas.

This chapter is organized as follows: In 2.3, the architecture of proposed module-based MG is introduced. In 2.4, detailed design of fully decentralized MG control is provided. 2.5

provides simulation and experiment results to verify the analytical study. Conclusion of this chapter is given in 2.6.

## 2.3 Architecture of Proposed PnP Microgrid

As shown in Figure 2-1 (c), MG built with proposed PU has three expansion levels, standalone, group expansion and inter-group expansion. This section will introduce the proposed MG architecture by these three expansion levels.

In standalone mode, a single PU can operate as a SHS, providing basic energy supply. Figure 2-2 shows the diagram of a proposed PU. The PU consists of two power electronic converters, a dc-dc converter for PV generation and a dc-dc converter for battery energy storage (BES). Each PU is controlled by an independent digital controller.

Multiple PUs can be interconnected directly through the local dc link to provide bulk power to users as a group. Figure 2-3 shows the diagram of a MG contains multiple groups. As mentioned in the introduction, direct bus-interfacing could omit interfacing converters, however the control coordination could become challenging, which will be discussed in detail in Section III.

Multiple groups can be interconnected to a public network in a relatively large area to enable power exchange among households and usage of public loads. Figure 2-3 shows the diagram of proposed MG in inter-group expansion. The interconnection of groups requires interfacing converters called as Gateway Converters (GC) in this chapter. The GC boosts the low voltage (48V) on the group side to a high voltage (200V-400V) on the public network side, provides galvanic isolation, and controls power flow between local group and the public network. The public bus control with similar scheme has been studied widely. Thus, this chapter is more focused on local

bus voltage regulation. With proposed control method, GC could compensate net load/generation differences and balance SoCs among groups automatically without communication.

Notice that, the PUs inside a group are very close to each other, where the line resistance among the PUs can be obviously neglected. For the public network, the line resistance can also be neglected to simplify the study considering two facts:

- i. The community network is still in a relatively small scale (in a hundreds-meters range). With proper selection of conductor size and voltage level, the line resistance is very small.
- ii. Each GC only maintains bus voltage at its terminal with droop control, the line resistance only affects the performance of power sharing among groups. The virtual resistance in droop control is much larger than line resistance. Thus, the effect of line resistance on power sharing is also neglectable.

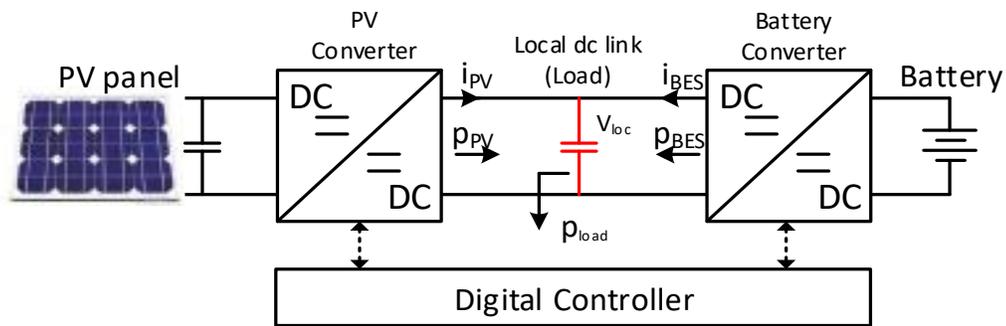


Figure 2-2. Diagram of a proposed power unit (PU).

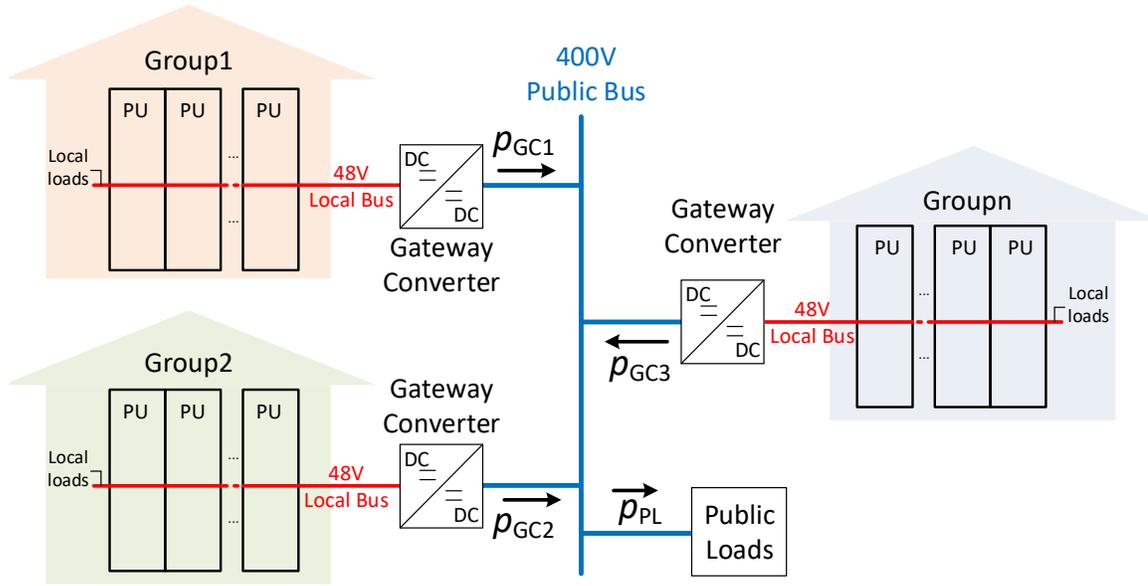


Figure 2-3. Diagram of proposed MG with inter-group expansion.

## 2.4 Decentralized Control Strategy for Proposed Microgrid Modules

To achieve PnP and robust operating in all expansion levels while keeping low cost, a fully decentralized control system independent from communication has been designed in this chapter. Mode transitions of each converter can be achieved seamlessly. The proposed method modifies dc bus signaling control proposed by [2.28]-[2.29], and combines SoC self-convergence control and seamless PV mode adaptive control. This section introduces the detailed design and implementation of proposed decentralized control technology to achieve proposed hierarchical MG in a wireless and seamless manner.

## 2.4.1 BES Converter Control

In a regular operation scenario, the BES converter should regulate local dc bus voltage with droop control to compensate the power mismatch between PV MPPT output and load consumption. Besides voltage regulation, the BES SoCs of parallel PUs should be kept balanced to make full usage of each battery. Paper [2.30] and [2.31] have proposed modified droop control to achieve BES SoC self-convergence without communication, by adjusting the droop resistance. Different from existing solutions, to accommodate dc bus signaling, this paper adds a first order term to the conventional droop control to achieve SoC self-convergence, rather than changing the droop resistance. Figure 2-4 shows the diagram of proposed controller for BES converter. The modified droop control, which is based on I-V droop control, follows,

$$i_{BES} = m_{BES}(V_{loc}^* - v_{loc}) + l(SoC - SoC^*) \quad (2-1)$$

where  $V_{loc}^*$  is the rated local bus dc link voltage and  $SoC^*$  is a reference value of SoC ramp term.

Figure 2-5 shows droop lines of proposed modified BES droop control. Besides the conventional I-V droop term that output current is proportional to voltage error, it contains a SoC ramp term. With the additional term, the output current will slightly increase when BES SoC level is higher than  $SoC^*$ ; the output current will slightly decrease when SoC level is lower than  $SoC^*$ . Thus, an SoC self-convergence characteristic can be created. By properly selecting parameter  $l$ , the voltage deviation can be kept in an acceptable range.

The selection of control parameters  $m_{BES}$  and  $l$  mainly considers the maximum charging / discharging current of BES converter and the acceptable range of voltage deviation from the rated voltage.

It is also shown in Figure 2-4, a saturator is added to the BES current reference. An overcharge protector provides limits for saturation stage based on information of SoC. When SoC is 0% or lower than a minimum SoC level, the current upper limit is set to zero (prevent from over-discharging); when SoC is 100%, the current lower limit is set to zero (prevent from over-charging). When the BES operating is limited by the saturator, the BES converter lost the droop characteristic. At this point, the bus voltage should be maintained by PV converter(s) (when BES is saturated to charging limit) or gateway converter (when BES is saturated to discharging limit).

The proposed MG has to use proposed SoC self-convergence control with a first-order SoC term rather than conventional method as discussed in [1.30]&[1.31], due to the following reasons,

- i. Some other important control parameters are selected based on the BES droop coefficient  $m_{BES}$ . The proposed method has a fixed droop coefficient rather than the conventional method adjusting droop coefficient all the time.
- ii. Another important reason is the linearity, which the conventional method cannot provide. Proposed method provides a linear relationship between local voltage, local SoC, and local net generation/load, which will be used for the GC control to compensate the power mismatch and SoC unbalance among multiple groups.
- iii. The proposed method also takes advantage of consistency in charging and discharging process and stable balancing speed, which is not related to charge/discharge power.

Under BES droop control,  $v_{loc}$  follows,

$$v_{loc} = V_{loc}^* + \frac{l}{m_{BES}} (SoC - SoC^*) - \frac{1}{m_{BES}} i_{BES} \quad (2-2)$$

which is used in the dc bus signaling system design.

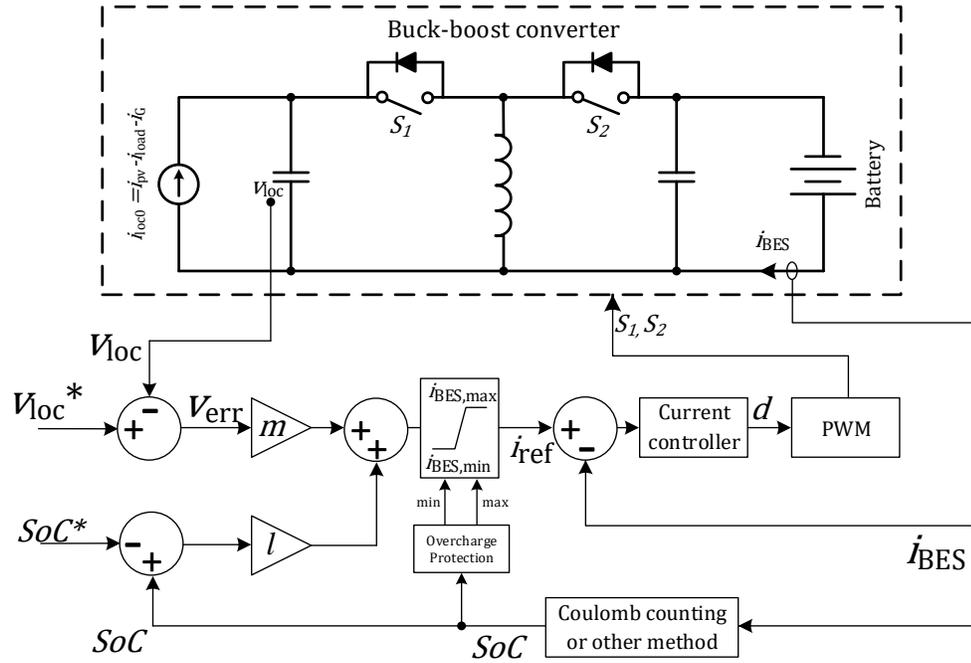


Figure 2-4. Block diagram of SoC-based droop control for BES converter.

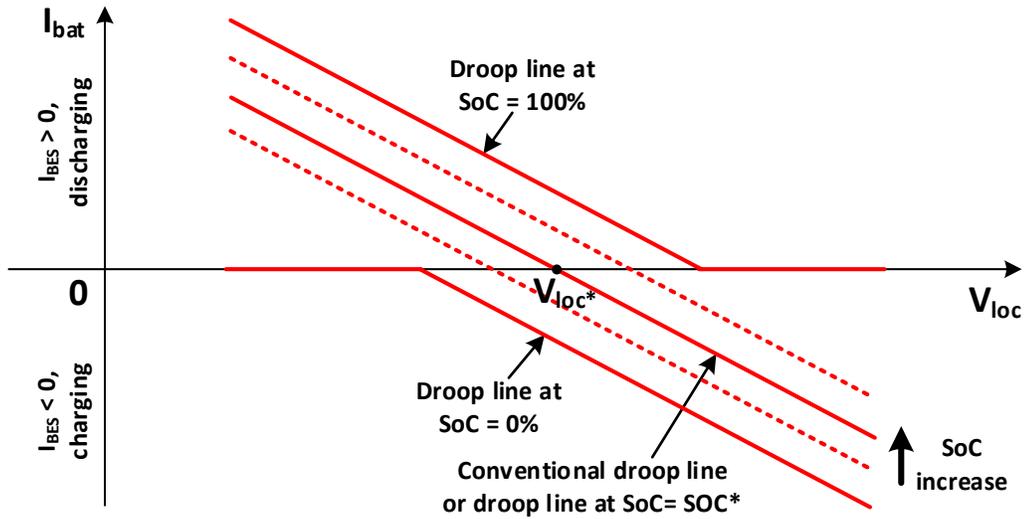


Figure 2-5. Droop lines of SoC-based droop control under different SoCs.

## 2.4.2 PV Converter Control

In a grid-connected PV system, PV panels can always operate under MPPT control theoretically while the grid can always absorb surplus power. However, in a small off-grid system as proposed MG, PV generation has to be able to operate under droop control when BES is fully charged. Paper [2.32] proposed a control for PV sources with a switch choosing two control configurations, which increase system complexity. Paper [2.33] proposed a seamless control for PV sources with an inner control loop to control  $dP/dV$ , which can achieve seamless mode transition by a saturator to  $dP/dV$  reference. However accurate measurement of  $dP/dV$  could be difficult. This paper proposed a PV controller based on similar idea to [2.33] without  $dP/dV$  control loop. Figure 2-6 shows the proposed mode adaptive PV converter control diagram. The inner control loop is a PV voltage loop maintains PV panel voltage. The outer control loop is a V-I droop control loop that maintains local dc link voltage, with a higher reference voltage value compared to BES droop control. The mode transition is seamless that the saturation characteristic of local bus voltage PI controller provides the ability of automatic mode transition.

When the BES is not yet fully charged that the local dc link voltage is well regulated by BES converter,  $V_{ref}$  is always higher than  $v_{loc}$ , with a preselection of  $V_{loc,max}$ . The input of voltage PI controller is constantly positive, so the output of PI controller is saturated to higher limit which is set to MPP voltage. The inner loop will control  $v_{PV}$  to  $V_{MPP}$  which achieves MPPT.

When PUs are fully charged or the BES current already hit the limit of  $i_{BES,min}$  (maximum charging current), the local dc link voltage will rise higher than  $V_{dp,ref}$ . Then the  $V_{PV}$  reference will decrease lower than  $V_{MPP}$ , so PV may operate at a off-MPP mode. Under PV droop control,  $v_{loc}$  follows,

$$v_{loc} = V_{loc,PV}^* - r \cdot p_{PV} \quad (2-3)$$

When load increases that  $p_{PV} < p_{load}$ , the dc link voltage will drop,  $V_{PV}$  will rise until reaching MPP and BES starts to discharge and maintains local dc link voltage.

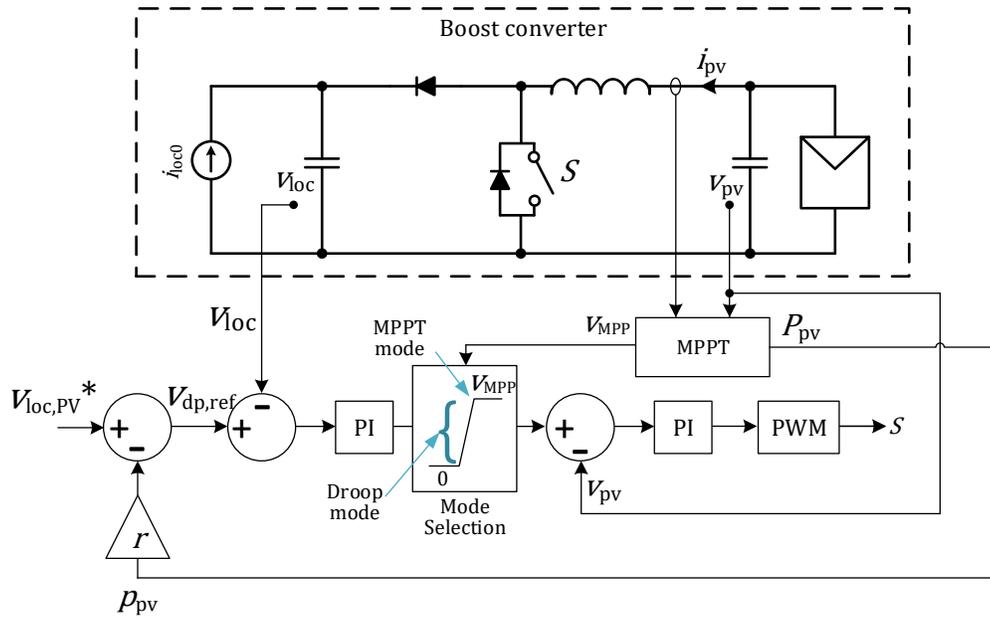


Figure 2-6 Block diagram of PV converter control with seamless mode selection.

### 2.4.3 Gateway Converter Control

Figure 2-7 shows the control diagram of GC in proposed MG architecture. Any bidirectional dc-dc topology can be used for GC, e.g. Boost, Flyback, Forward, Dual-Active-Bridge, etc. And in this paper, Buck-Boost converter is used for GC to demonstrate the general idea. As the interface between local low-voltage dc bus and public medium voltage dc bus, the gateway converter has two operation modes,  $v_{pub}$  control mode and  $v_{loc}$  control mode. Different from PV mode selection, which is completely based on voltage threshold, the gateway converter mode selection uses smaller

current reference from  $i_{ref1}$  (generated by public bus droop control) and  $i_{ref2}$  (generated by local bus droop control). As a result, the power direction change becomes continuous and seamless. Gateway converter and BES converter can work simultaneously under droop control establishing local dc bus voltage.

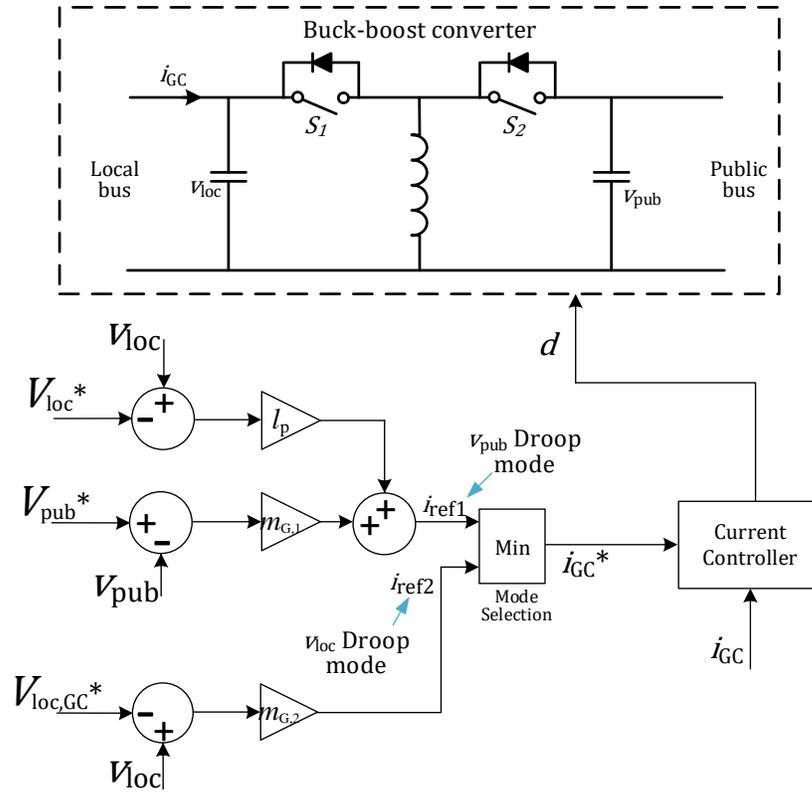


Figure 2-7. Block diagram of gateway converter control with mode selection.

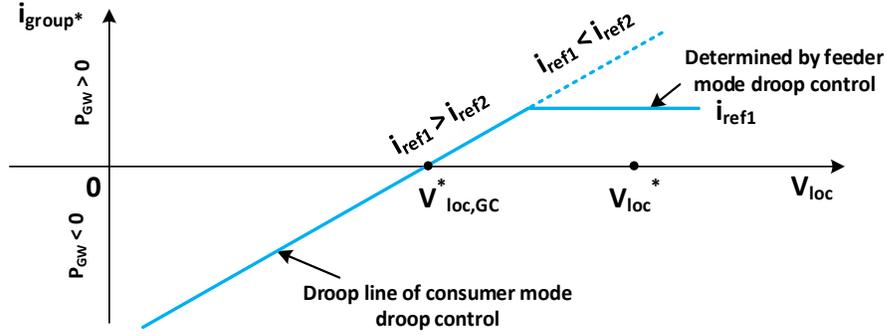


Figure 2-8. Droop line of local bus droop control of gateway converter.

In  $v_{pub}$  control mode, the local group operating in healthy condition, the gateway converter will feed power into the public dc bus with a modified droop control, as  $i_{ref1} < i_{ref2}$  in Figure 2-7.

The current reference in  $v_{pub}$  control mode is given by,

$$i_{ref1} = m_{G,1} (V_{pub}^* - v_{pub}) + l_p (v_{loc} - V_{loc}^*) \quad (2-4)$$

In  $v_{loc}$  control mode, the energy stress of the local group is too high to support public network that  $i_{ref2} < i_{ref1}$ , the GC can reduce output power even to reversely inject power into the local group to maintain the local dc link voltage inside acceptable level. The controller for gateway converter in  $v_{loc}$  control mode uses simple I-V droop control,

$$i_{ref2} = m_{G,2} (v_{loc} - V_{loc,GC}^*) \quad (2-5)$$

where  $V_{loc,GC}^*$  is rated voltage for GC local bus droop control. The selection of  $V_{loc,GC}^*$  will be detailly explained in Section III D.

The mode selection is based on  $i_{ref2}$ , which is actually an indicator of group energy stress. The larger  $i_{ref2}$  is, the less stressed the group is. In  $v_{pub}$  control mode,  $i_{ref2} > i_{ref1}$ , the gateway converter will follow the public bus droop control. In  $v_{loc}$  control mode,  $i_{ref2} < i_{ref1}$ , the gateway

converter will maintain the local dc bus at a minimum level. Figure 2-8 shows the droop line of local bus droop control of gateway converter.

For selecting parameters of GC control, an important difference is GC could be connected to groups with different number of PUs. Thus, the control parameters of GC should be adjusted according to the number of PUs connected to local group to proportionally share power with other groups. The setting of number  $n$  can be achieved by simply using buttons or a knob on the GC, which can be done by any untrained people and will not spoil the PnP feature. Thus,  $m_{G,2}$ ,  $m_{G,1}$  and  $l_p$  should be adjusted accordingly,

$$m_{G,1} = n \cdot m'_{G,1} \quad (2-6)$$

$$m_{G,2} = n \cdot m'_{G,2} \quad (2-7)$$

$$l_p = n \cdot l'_p \quad (2-8)$$

where  $n$  is the number of PUs connected to the local bus,  $m'_{G,1}$  and  $m'_{G,2}$  are droop coefficients per unit for local bus droop control and public bus droop control, respectively,  $l'_p$  is the per unit coefficient for SoC balance among groups.

The values of  $m_{G,1}'$  and  $m_{G,2}'$  could follow regular droop controller design procedure considering the acceptable range of voltage variation towards certain power variation. Specifically, to achieve same voltage regulation performance on local bus under usage-dominating mode as under storage-dominating mode,  $m'_{G,2}$  should be equal to  $m_{BES}$ .  $l'_p$  should also be equal to  $m_{BES}$  to achieve automatic compensation of load/generation mismatch, which will be explained later.

Different from conventional solutions as shown in Figure 2-1 (a) where the interfacing converter, BES converter and PV converter can be controlled by one controller device with shared

information. A challenge for GC is how to achieve power flow control and SoC balance among groups simultaneously without communicating with other devices. The proposed GC control coordinate with proposed BES droop control as introduced in Section III. A, naturally, which achieves automatic power flow control to compensate load/generation mismatch and SoC self-convergence among multiple groups.

As shown in equation (2-4), the GC  $v_{\text{pub}}$  droop control also consists of two terms, one conventional I-V droop control term and a first-order term reflects local voltage. Considering groups could have different numbers of PUs, equation (2-4) can be rewritten as,

$$\frac{i_{\text{GC}}}{n} = m'_{\text{G},1} (V_{\text{pub}}^* - v_{\text{pub}}) + l'_p (v_{\text{loc}} - V_{\text{loc}}^*) \quad (2-9)$$

where  $i_{\text{GC}}$  is the current of the GC on the local bus side.

All GCs are connected to the same public bus, so the first terms in (2-9) are same in all GCs. Thus, the circulating current to balance power and SoC is only generated from the second term,

$$i_{\text{GC},\text{c},\text{p.u.}} = l'_p (v_{\text{loc}} - v_{\text{loc},\text{avg}}) \quad (2-10)$$

where  $i_{\text{GC},\text{c},\text{p.u.}}$  is the per PU circulating current go through GC converters. With local SoC self-convergence control proposed in section III A, the local bus voltage contains information of both group net load/generation and group average SoC. Put (2-2) into (2-10),

$$\begin{aligned} i_{\text{GC},\text{c},\text{p.u.}} &= \frac{l'_p}{m_{\text{BES}}} (i_{\text{BES},\text{avg}} - i_{\text{BES}}) \\ &+ \frac{l'_p l}{m_{\text{BES}}} (SoC_{\text{loc},\text{avg}} - SoC_{\text{global},\text{avg}}) \end{aligned} \quad (2-11)$$

Apparently, the circulating current as in (2-11) consists of two parts. The first term,  $\frac{l'_p}{m_{\text{BES}}} (i_{\text{BES},\text{avg}} - i_{\text{BES}})$ , is used to provide compensation for load/generation mismatch among the

groups. When  $\frac{l'_p}{m_{BES}} = 1$ , the first term becomes exactly the current mismatch of each PU. The second term,  $\frac{l'_p l}{m_{BES}} (SoC_{loc,avg} - SoC_{global,avg})$ , is used to balance the SoCs among multiple groups. Make the difference between  $SoC_{loc,avg}$  and  $SoC_{global,avg}$  to be  $\Delta SoC_{loc,avg}$ , which can be expressed follow the definition of SoC,

$$\frac{d\Delta SoC_{loc,avg}}{dt} = -i_{BES} + i_{BES,avg} \quad (2-12)$$

Put (2-11) into (2-12) and considering  $\frac{l'_p}{m_{BES}} = 1$ ,

$$\frac{d\Delta SoC_{loc,avg}}{dt} = i_{GC,c,p.u.} - l\Delta SoC_{loc,avg} \quad (2-13)$$

Solve (2-13),

$$\Delta SoC_{loc,avg}(t) = \Delta SoC_{loc,avg}(0) + \frac{i_{GC,c,p.u.}}{l} (1 - e^{-lt}) \quad (2-14)$$

Thus the SoC difference can be converged to,

$$\Delta SoC_{loc,avg}(\infty) = \frac{i_{GC,c,p.u.}}{l} \quad (2-15)$$

From (2-15) it can be seen, the SoC converge performance on GC converters is different from BES converters. It cannot guarantee SoC difference converging to zero but only to a certain value related to GC operating condition. Though the SoCs among groups will have difference, the trend is kept from divergence. This difference is caused by different load/generation conditions in multiple groups. Only when the net load/generation per PU of all groups are equal,  $\Delta SoC_{loc,avg}(\infty)$  is equal to zero. Considering the per unit net load/generation in each group would be similar in a large time scale, the SoCs among groups can be kept balanced in long term dynamically.

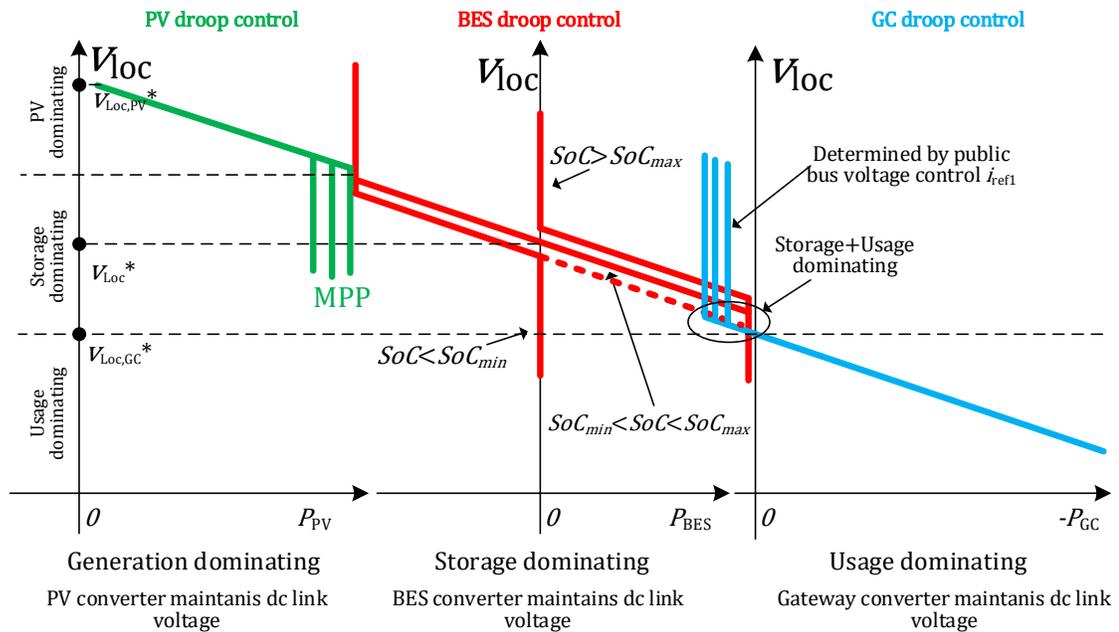


Figure 2-9. Coordination of local dc bus droop control.

#### 2.4.4 Control Coordination

As mentioned, for each group, multiple PUs are directly bus-interfaced. The coordination of parallel PV, BES and GC converters is the key challenge in proposed MG architecture. While the public dc bus control is much simple and have been studied by many researchers, this section will be more focused on the local group control coordination.

TABLE 2-I SUMMARIZE OF CONVERTER MODES AND CRITERIA

	Mode 1	Mode 2	Mode transition criteria
<b>BES converter</b>	$v_{loc}$ droop control	saturated	SoC level
<b>PV converter</b>	MPPT	$v_{loc}$ droop control	$v_{PV}$ reference saturated to $V_{MPP}$ or not
<b>Gateway converter</b>	$v_{pub}$ droop control	$v_{loc}$ droop control	Comparing $i_{ref1}$ and $i_{ref2}$

With proposed controllers for each converter, the coordination, including mode transition, power sharing and SoC balance can be achieved simultaneously in a fully decentralized manner. As introduced above, generally, each converter in the proposed MG generally has two operation modes, which can be concluded as TABLE 2-I. All mode transitions are based on a seamless manner.

Besides modes of each converter, the overall system operation can be put into three modes. Figure 2-9 demonstrates the coordination of PV, BES and GC droop control. Based on which part is dominating droop control, the three modes are generation dominating mode, storage dominating mode and usage dominating mode [2.28]. The local dc link voltage  $v_{loc}$  works as an indicator of operation mode. To achieve wireless and seamless mode transition, the parameters for each converter controller should be carefully designed.

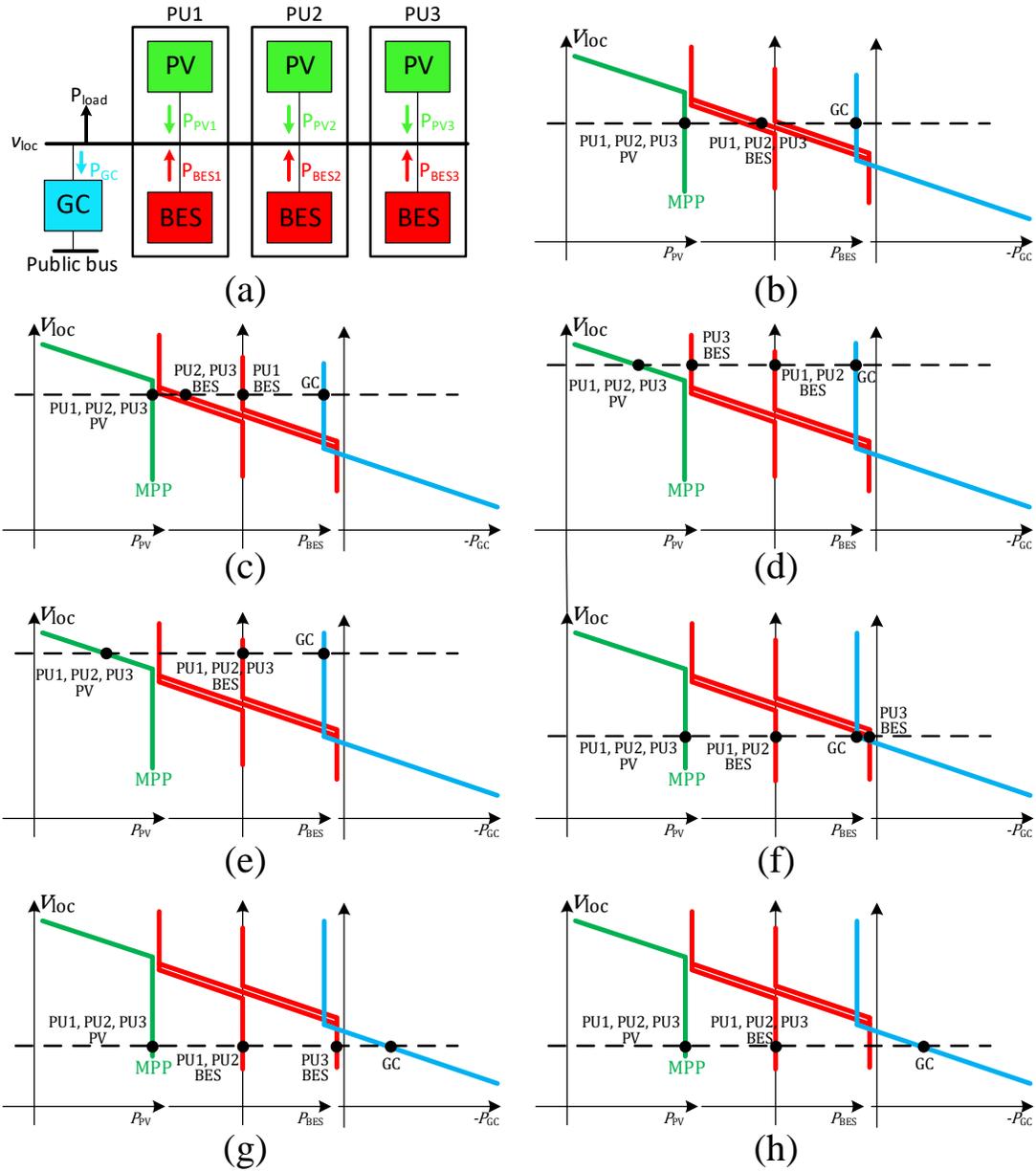


Figure 2-10. Typical operating modes of a group in proposed MG, (a) group diagram, (b) storage dominating mode with all batteries available, (c) storage dominating mode (PU1 drained), (d) PV dominating mode (PU1&PU2 fully charged, PU3 at charging current limit), (e) PV dominating mode (all PUs fully charged), (f) storage dominating mode + usage dominating mode (PU1&PU2 drained), (g) Usage dominating mode (PU1&PU2 drained and PU3 at discharging current limit), (h) Usage dominating mode (all PUs drained).

PV should operate under MPPT control whenever BES can maintain  $v_{loc}$ . By (2-2) and (2-3), the parameters should satisfy,

$$V_{loc,PV}^* - r \cdot p_{PV,max} > V_{loc}^* + \frac{l}{m_{BES}} (SoC_{max} - SoC^*) - \frac{1}{m_{BES}} I_{BES,min} \quad (2-16)$$

And noticing that the power range of PV is dependent on MPP power, a voltage gap between PV-droop control and BES droop control is inevitable, which will not have any negative influence on the system stability or reliability.

Different from having a relatively clear boundary between PV dominating mode and storage dominating mode, the storage dominating mode can have an overlapping area with usage dominating mode. It is allowed to have  $v_{loc}$  under droop control simultaneously from BES and GC. This overlap can reduce the stress of local BES at low SoC level and make the mode transition process smoother. The overlap is generated naturally from the selection of parameter  $V_{loc,GC}^*$ . Reaching the local voltage reaching  $V_{loc,GC}^*$  means the BESs cannot further provide any power. Any further decrease of local bus voltage should be compensated by injecting power from GC. Thus, it makes sense to set GC power equal to zero at  $V_{loc,GC}^*$  and  $V_{loc,GC}^*$  should follow,

$$V_{loc,GC}^* = V_{loc}^* - \frac{1}{m_{BES}} I_{BES,max} \quad (2-17)$$

The width of overlapping is determined by  $i_{ref1}$ , which is generated from public bus voltage droop control.

Figure 2-10 shows typical operating scenarios of a group consists of three PUs and one GC under different operation modes. Figure 2-10 (a) shows the group connection diagram. Figure 2-10 (b) shows a regular condition that all PUs are available, batteries can absorb or release energy to maintain the local bus voltage with droop control, the system is under storage dominating mode.

The operating points of three BES converters are on the droop line, three PV converters are under MPPT control and GC can be regard as load feeding power into public dc link. In Figure 2-10 (c), though PU1 is fully charged that the operating point is saturated to zero current, the other PUs still can absorb surplus power, the group still operates under storage dominating mode. In Figure 2-10 (d), PU1 and PU2 are fully charged and PU3 hits the maximum charging power, all PUs cannot further absorb surplus power. Thus  $v_{loc}$  rises and PV converters operates under droop control to maintain  $v_{loc}$ , which makes the system PV dominating mode. In Figure 2-10 (e), all PUs are fully charged and the group is kept in PV dominating mode, until PV output cannot meet the load consumption, batteries will start to discharge and change back to storage dominating mode. In Figure 2-10 (f), PU1 and PU2 BESs are drained and saturated to zero output power, though both PV are under MPPT control,  $v_{loc}$  is at a relatively low level due to the high load. GC operates under droop control with reduced power consumption. The system  $v_{loc}$  is dominated by both storage and usage. In Figure 2-10 (g), PU1 and PU2 are still drained, and PU3 BES is saturated to its maximum output power, BES losses the ability of  $v_{loc}$  control. Only GC operates under droop control. The system is under usage dominating mode. Figure 2-10 (h) is similar to Figure 2-10 (g), but with all PU BESs drained. GC operates under droop control. The system is still under usage dominating mode.

With the proposed control system design, with a certain  $v_{loc}$ , a unique operating point can be determined for each converter in the group. In all operating scenarios and expansion levels, the system can be kept stable and robust. Therefore, true PnP can be realized with low cost and high reliability.

## 2.5 Simulation and Experimental Study

### 2.5.1 Simulation Study

Simulations based on PLECS are performed to evaluate the proposed MG architecture and the fully decentralized control technique. TABLE 2-II shows parameters used in simulation.

Figure 2-11 shows the simulation results of a group consists of three PUs, where (a) shows the whole scope and (b)-(e) show the zoomed in waveforms during transients. In  $t_0 - t_1$ , all BESs of three PUs are under droop control and all PVs are under MPPT control (with different MPP power). At  $t_1$ , BES of PU1 is fully charged and is no longer under droop control. In  $t_1 - t_2$ , BESs of PU2 and PU3 can still absorb surplus power to maintain  $v_{loc}$  with droop control to a little higher value due to the higher charging current on each BES. At  $t_2$ , BES of PU2 also gets fully charged. In  $t_2 - t_3$ , solely PU3 BES cannot absorb all the surplus power and is saturated to the maximum charging power. The increase of  $v_{loc}$  changes PV converters from MPPT control to droop control which keeps  $v_{loc}$  from further increasement, and PVs can evenly share the power. At  $t_3$ , BES of PU3 also gets fully charged. PVs further reduce their output with droop control to maintain  $v_{loc}$ . At  $t_4$ , a load step change from 100W to 400W happens, that all PVs increase their outputs to MPP still cannot meet the load need. BESs start to discharge and take back droop control.

It can be seen that when BES taking over the droop control, e.g. Figure 2-11 (b) and (e), the transient is much faster (shorter settling time and smaller overshoot) than that of PV taking over droop control, e.g. Figure 2-11 (c) and (d). It can be explained by that, BES converter uses I-V droop control, as shown in Figure 2-4, which has a nature of better transient performance than that of V-I droop control used by PV converter, as shown in Figure 2-6 [2.34]. At the same time, the  $v_{loc}$  PI controller of PV converter has to have a lower control bandwidth to guarantee a stable inner

$v_{PV}$  loop, which could further deteriorate  $v_{loc}$  transient performance. With proper design of parameters and local bus capacitance, the transient can be kept in an accept range as shown in the simulation result (settling time 0.2 s, overshoot 10 V).

Figure 2-12 shows the simulation result of a group consists of two PUs and connected to the public bus with a gateway converter GC. The simulation result shows GC operation mode change between  $v_{pub}$  control mode and  $v_{loc}$  control mode and the case  $v_{loc}$  is regulated by both BES and GC. In  $t_0 - t_1$ , BESs of two PUs are under droop control and PVs are under MPPT control. GC is working feeding power into public bus of which the power is determined by  $v_{pub}$  droop control. At  $t_1$ , a load step change from 100W to 400W happens. In  $t_1 - t_2$ , Both BESs are under droop control with increased output power. Reduced  $v_{loc}$  makes GC also under  $v_{loc}$  droop control that the power drained from local bus is reduced. At  $t_2$ , a solar irradiance drop happens. In  $t_2 - t_3$ , the  $v_{loc}$  is still maintained by BESs and GC. BESs output power are further increased. GC output power is further decreased to negative that start to inject power into local bus. At  $t_3$ , PU1 is drained and PU2 BES hits the maximum output power. In  $t_3 - t_4$ , only GC maintains  $v_{loc}$  with droop control. At  $t_4$ , the load is reduced to 0 from 400W.  $v_{loc}$  rise to a higher value and GC change back to  $v_{pub}$  control. PU2 BES maintains  $v_{loc}$  while PU1 is still drained that cannot provide any power. Notice that both BES and GC droop control are I-V droop control which has a high control bandwidth. As a result, all transients in Figure 2-12 are smooth and fast.

Figure 2-13 shows simulation result of a case consists of three groups, where Group 1 has two PUs, Group 2 has three PUs and Group 3 has three PUs. As shown in Figure 2-13, all PUs start with different SoC, and net load are different in three groups with two transients of net load step change in Group 2 at 1800s and 3200s. In this test case, the GCs are under  $v_{pub}$  control mode to demonstrate power sharing and SoC balancing ability among groups, due to that SoC balancing

and power sharing among groups are only considered under GC  $v_{pub}$  control mode. Firstly, from the result, with proposed SoC self-convergence control, the SoCs inside a group converges fast to a well-balanced state, as well as the current sharing. Secondly, among multiple groups, as analyzed by mathematical derive from equations (2-9)-(2-15), the SoCs of three groups are kept from divergence though with a steady state SoC difference due to different net load/generation condition which agrees to equation (2-15). And the net load/generation mismatch in different groups are compensated that the BES output powers are well shared by each BES in all groups, with the proposed control design and parameter selection as explained by equation (2-11).

TABLE 2-II SYSTEM SPECIFICATION

Item	Symbol	Value	Item	Symbol	Value
Rated local dc bus voltage	$V_{loc}^*$	48 V	Max discharging current	$i_{BES,max}$	4.2 A
Droop reference of PV converter	$V_{loc,PV}^*$	52 V	Max charging current	$i_{BES,min}$	-2.0 A
Droop reference of GC	$V_{loc,GC}^*$	45 V	BES $v_{loc}$ droop coefficient	$m_{BES}$	1
Rated Public dc bus voltage	$V_{pub}^*$	200 V	BES SoC coefficient	$l$	0.02
BES voltage	$V_{bat}$	48 V	PV maximum power	$P_{PV,max}$	100 w
BES capacity	$C_{bat}$	10 Wh	PV droop coefficient	$r$	0.01
maximum SoC	$SoC_{max}$	100 %	GC $v_{loc}$ droop coefficient	$m_{G2}$	2
minimum SoC	$SoC_{min}$	30 %	Typical GC feeding current	$i_{ref1,typical}$	2 A
$SoC^*$	$SoC^*$	50 %	Local bus capacitance	$C_{loc}$	660 $\mu F/unit$
Overlapping voltage	$\Delta V$	2.6 V			

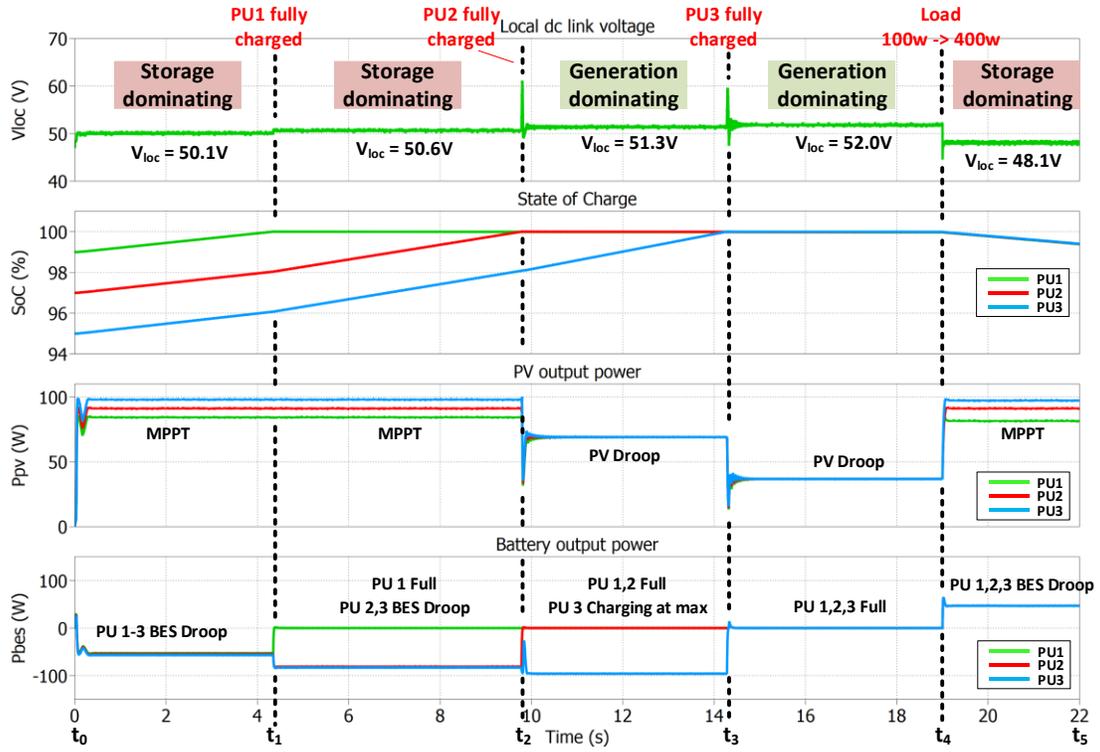
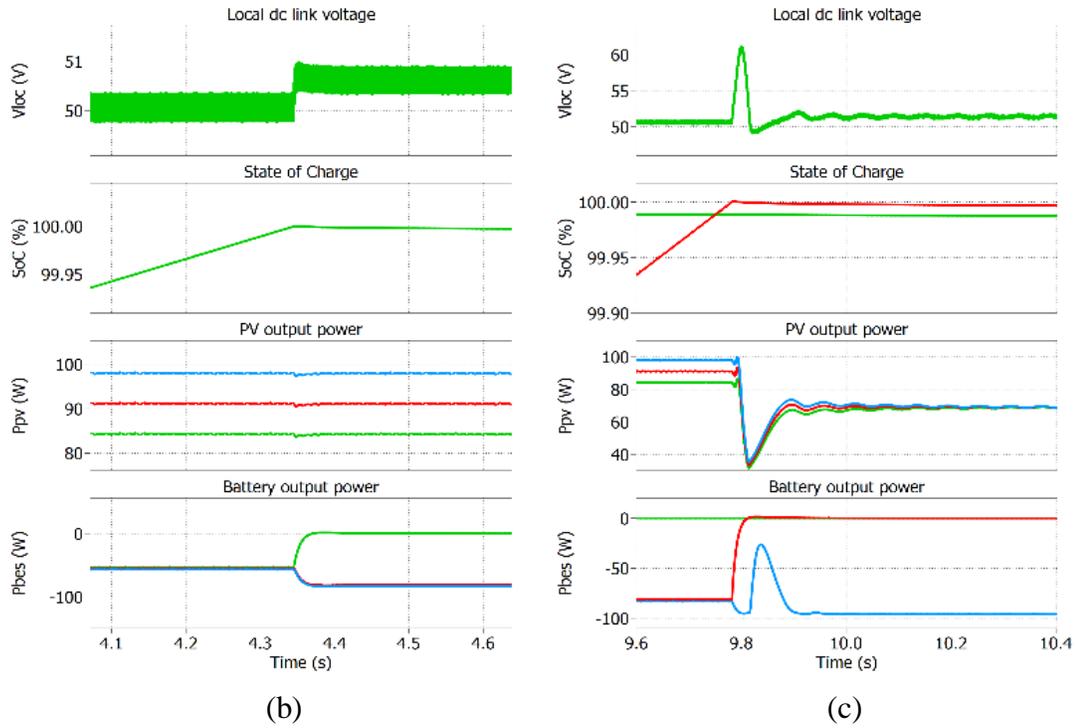


Figure 2-12. (a)



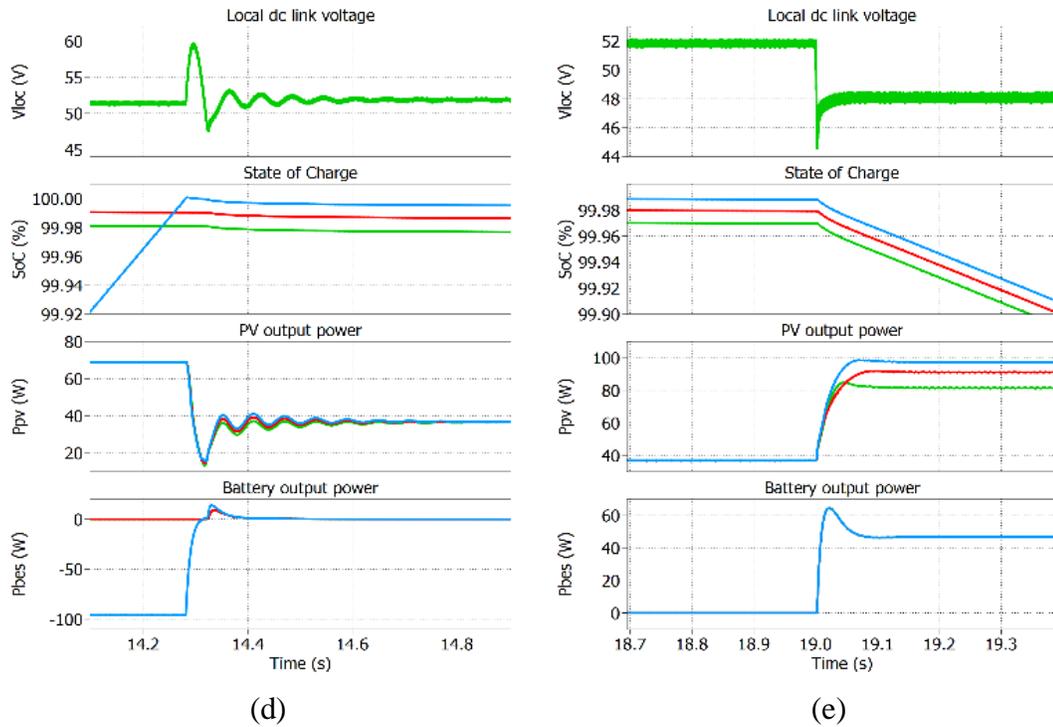


Figure 2-11. Simulation results of a group bus consists of three PUs, (a) operation with group mode transitions, (b) zoomed-in waveforms at time  $t_1$ , (c) zoomed-in waveforms at time  $t_2$ , (d) zoomed-in waveforms at time  $t_3$ , (e) zoomed-in waveforms at time  $t_4$ .

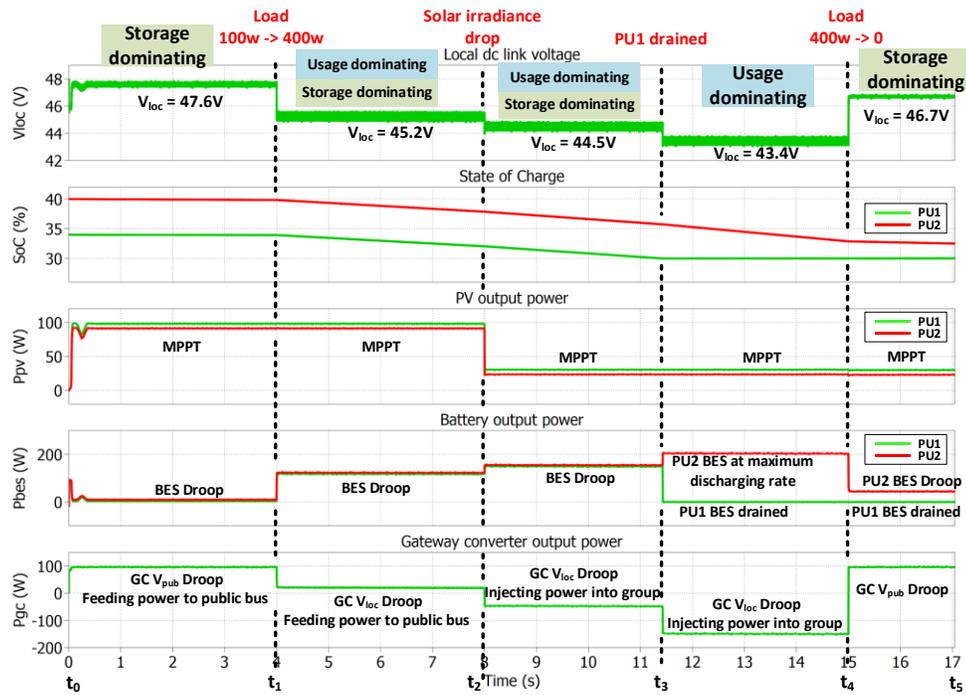


Figure 2-12. Simulation result of GC mode transitions.

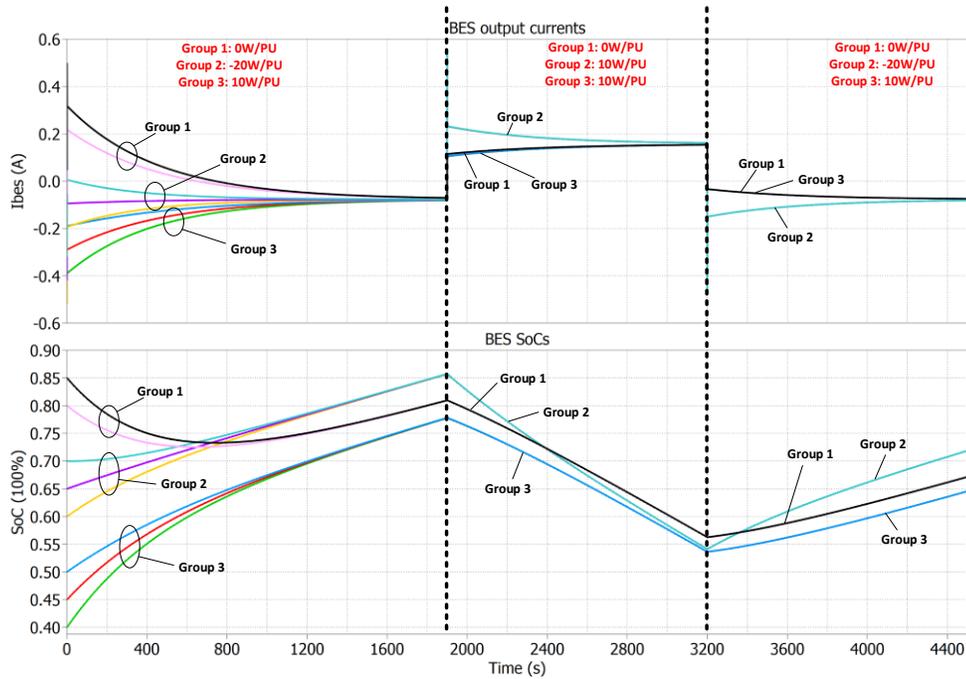


Figure 2-13 Simulation result showing power sharing and SoC balance among BESs inside a group and among groups.

## 2.5.2 Experiment Verification

The proposed MG architecture has been verified by experimental prototypes, of which the setup is shown in Figure 2-14. A MG system with two PUs and one GC converter is tested. The verification focuses more on the group operation. The public bus is emulated as a voltage source with a battery. Each PU is controlled by a TI F28379d DSP. Parameters are set to same as TABLE 2-II.

Figure 2-15 (a) and (b) show the system SoC self-convergence characteristic in charging and discharging process respectively. SoC waveforms are generated by MATLAB with measured information of BES currents. It can be seen that the BES with higher SoC always provides higher

current. A converging trend of two BES SoCs can be observed in both cases. Besides that, with change of system overall SoC, a change on the local bus voltage  $v_{loc}$  can also be observed, which can be used for GC to estimate local group average SoC.

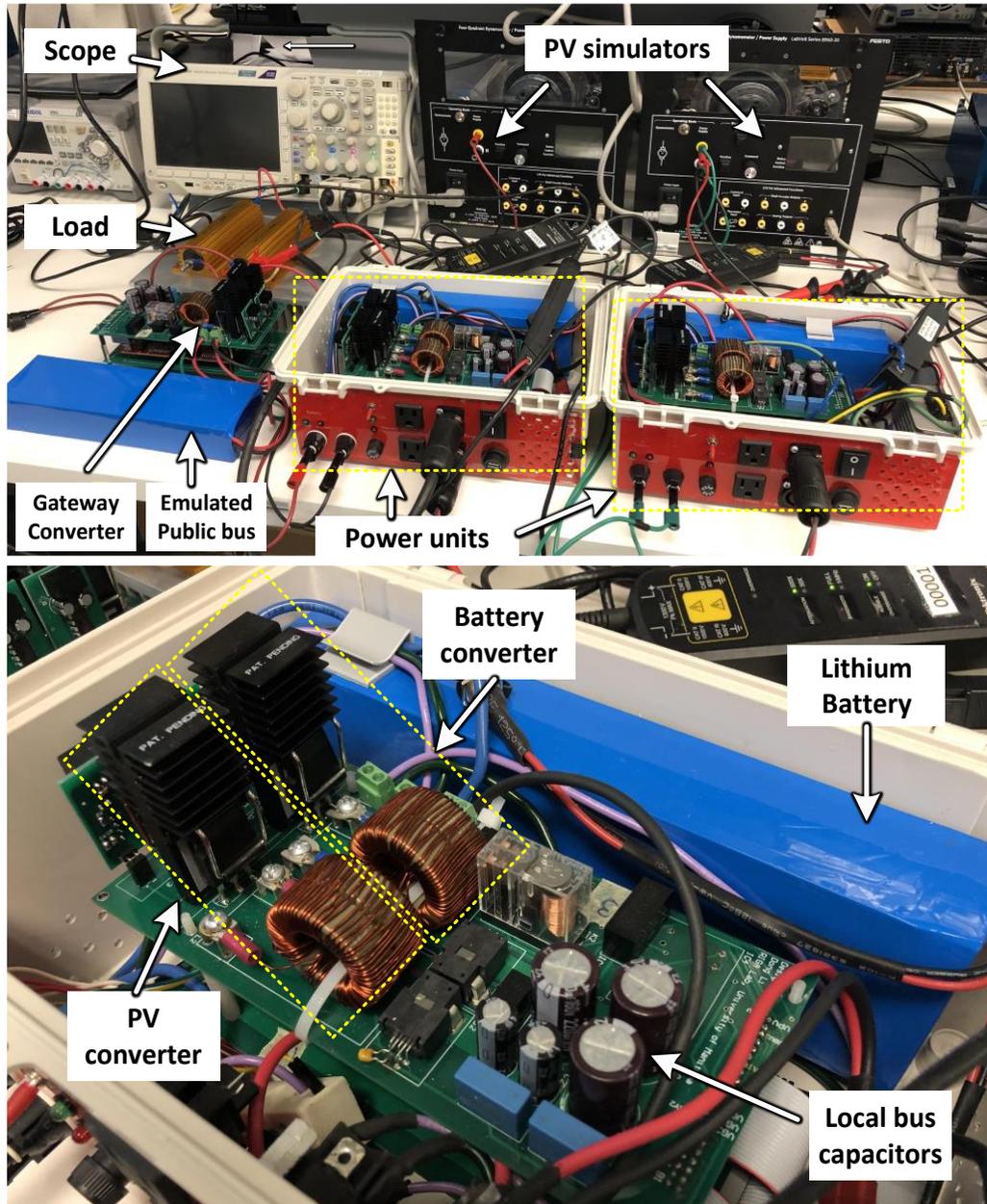


Figure 2-14. Experiment setup.

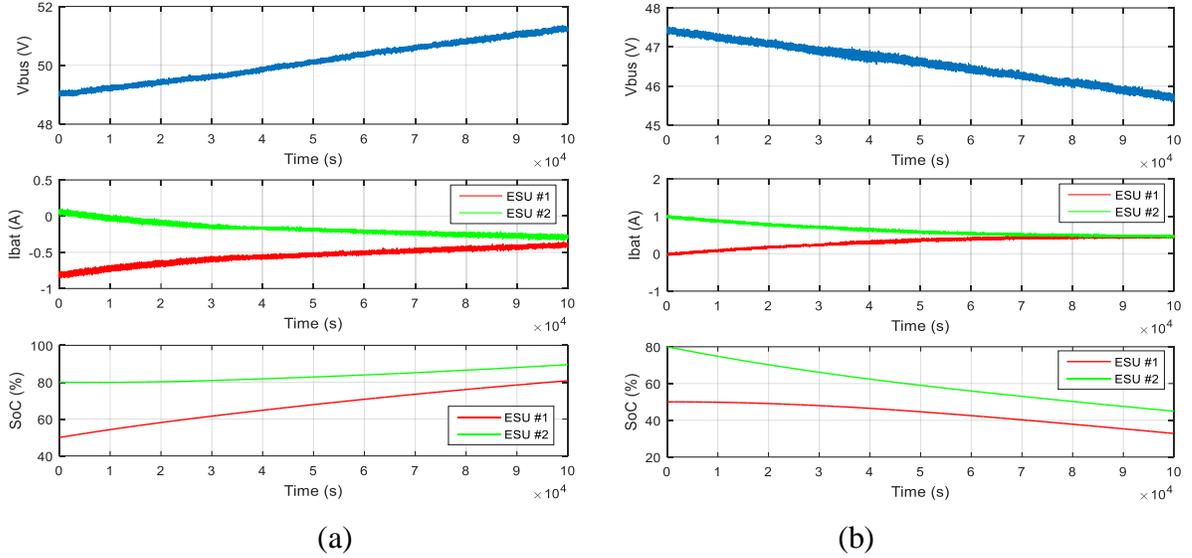


Figure 2-15. Experimental waveforms of SoC self-convergence in (a) charging and (b) discharging.

Figure 2-16 shows operation of a standalone PU showing PV-BES droop coordination. In  $t_0 - t_1$ , BES maintains  $v_{loc}$  with droop control and PV operates at MPP. At  $t_1$ , BES is fully charged, and BES charging current is saturated to zero; PV converter change to droop control and maintains  $v_{loc}$  at a higher level with reduced PV output power. At  $t_2$ , solar irradiance is reduced. While PV converter still under droop control, the output power maintains the same but closer to MPP with increased  $v_{PV}$ . At  $t_3$ , solar irradiance is further reduced. PV converter increases  $v_{PV}$  till reach MPP, but the MPP power cannot compensate the load. BES starts to discharge and maintains  $v_{loc}$  with droop control. At  $t_4$ , solar irradiance is reduced to zero. BES can still maintain  $v_{loc}$  with higher output power. Figure 2-16 (b) illustrates the operating points of PV during mode transitions.

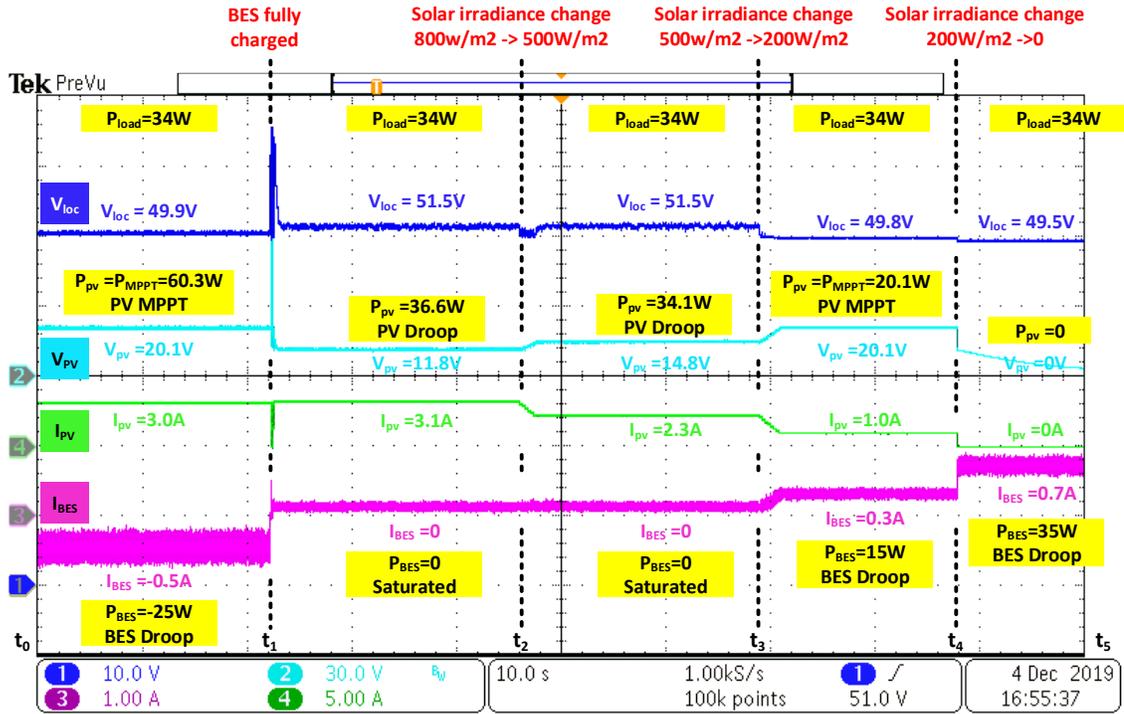
Figure 2-17 shows operation of a group consists of two PUs showing PV-BES droop coordination. Two PV simulators uses different PV curves with different MPP power. In  $t_0 - t_1$ , PV converters operate at each MPP, and BESs maintain  $v_{loc}$  with droop control and equally share power. At  $t_1$ , PU1 BES is fully charged; PU2 BES can still absorb all the surplus power with droop

control; PV converters are kept at MPPT control. At  $t_2$ , PU2 BES is also fully charged that both BESs cannot absorb any surplus power; PV converters change to droop control. At  $t_3$ , solar irradiance is significantly reduced on PV1, PV converters increase their  $v_{PV}$  to maintain the output power. At  $t_4$ , solar irradiance is also reduced on PV2, PV converters can still maintain dc link voltage well with equally shared power. At  $t_5$ , PV1 is completely shut down, PV2 increase its power till reaching MPP, BESs start to discharge to maintain  $v_{loc}$  at lower level with droop control. Figure 2-17 (b) shows detailly how the PV operating points move on two different PV curves during the experiment. In storage dominating mode, each PV can track its own MPP. In generation dominating mode, two PVs can equally share the power.

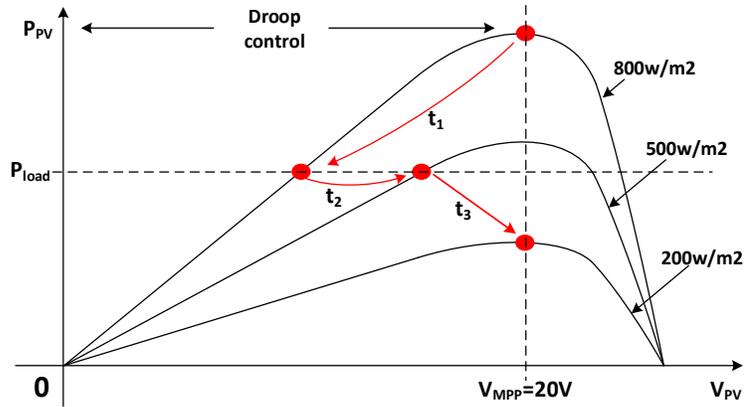
Figure 2-18 shows the zoomed in waveforms of the transient from storage dominating mode to generation dominating mode. Figure 2-19 shows the zoomed in waveforms of the transient from generation dominating mode back to generation dominating mode. It can be seen the transient of the former one has a much longer settling time and overshoot, due to the nature PV characteristic and V-I droop control. With a proper design of bus capacitance, the overshoot can be limited within an acceptable range.

Figure 2-20 shows experimental waveforms of coordination of PU and GC  $v_{loc}$  droop control. One PU and one GC is used to verify the BES-GC coordination. Public bus is emulated using a battery as constant voltage source and  $i_{ref1}$  is set to 1A. In  $t_0 - t_1$ , BES with PV output power can well manage the load of 115W maintaining  $v_{loc}$  at an acceptable level that GC can injecting 1A as given by reference  $i_{ref1}$ . At  $t_1$ , load step changes to 200W;  $v_{loc}$  drops to 45.2V; both BES and GC are under droop control that GC reduces the power injected into public bus to 0.4A. At  $t_2$ , solar irradiance change reduces the PV output power; BES increase its output power and GC further reduce its power consumption till injecting power into local group with 0.2A. At  $t_3$ , PV output

power reduces to zero; BES operates at maximum discharging current; only GC is under droop control to maintain  $v_{loc}$  at a lower level (44.5V). At  $t_4$ , load is reduced to 115W; BES output is reduced and maintains  $v_{loc}$  at a relatively higher level with GC.

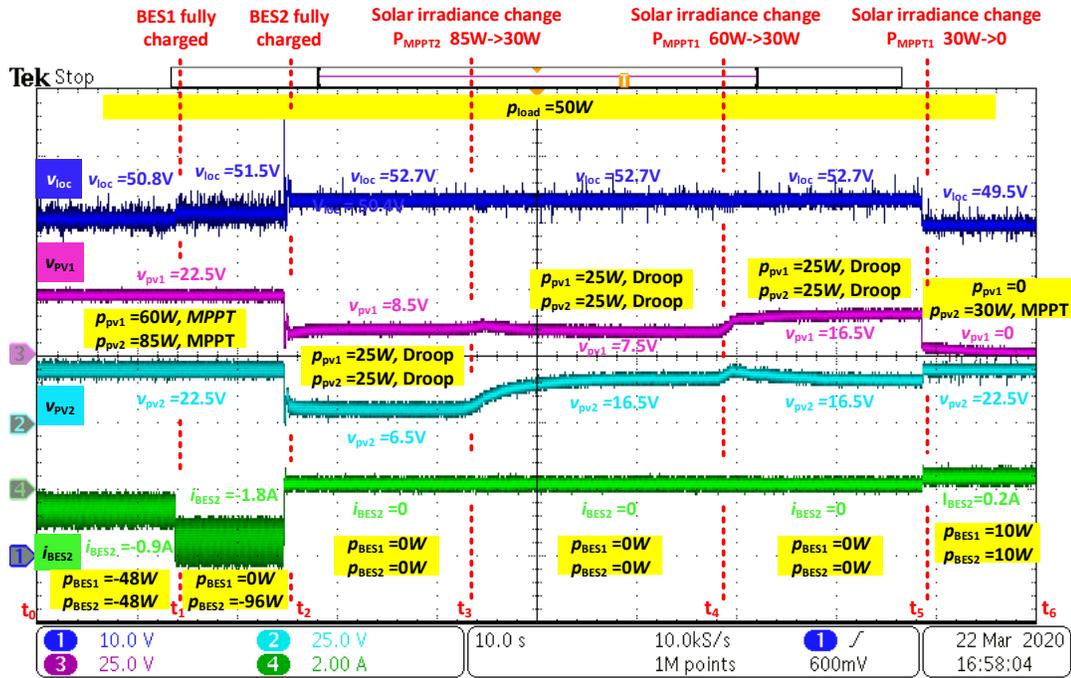


(a)

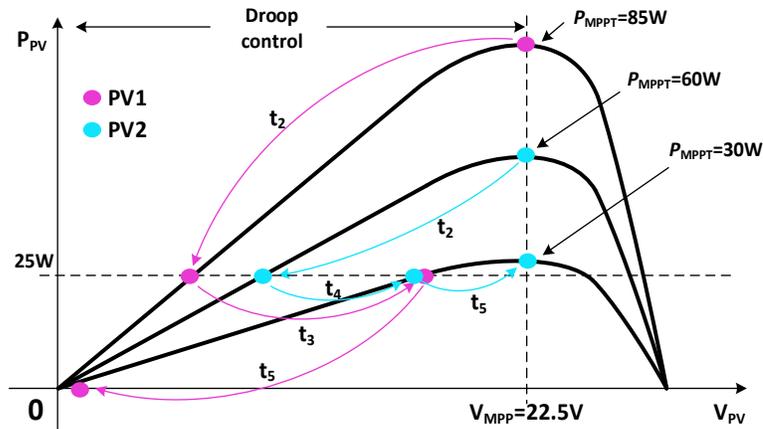


(b)

Figure 2-16. Experimental results of a standalone PU showing PV-BES droop control coordination, (a) waveforms, (b) PV operating points.

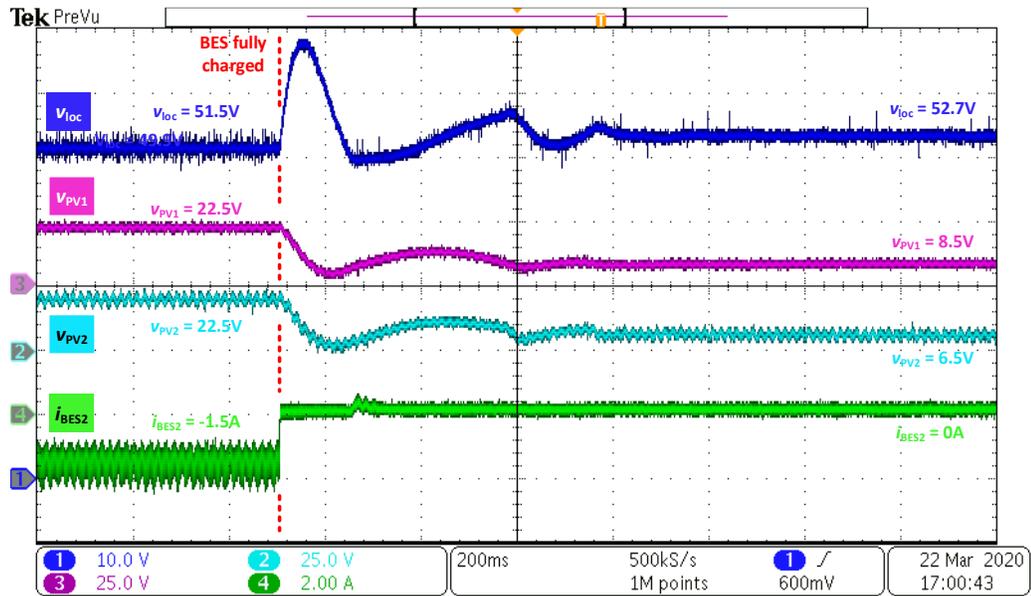


(a)

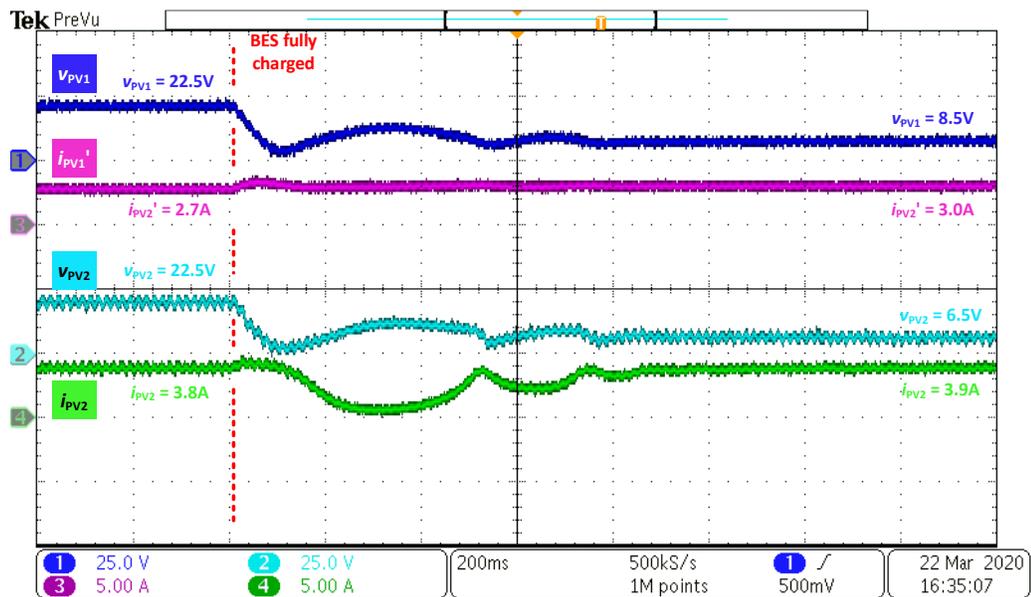


(b)

Figure 2-17. Experimental waveforms of a group consist of two PUs showing PV-BES droop coordination, (a) waveforms, (b) PV operating points.

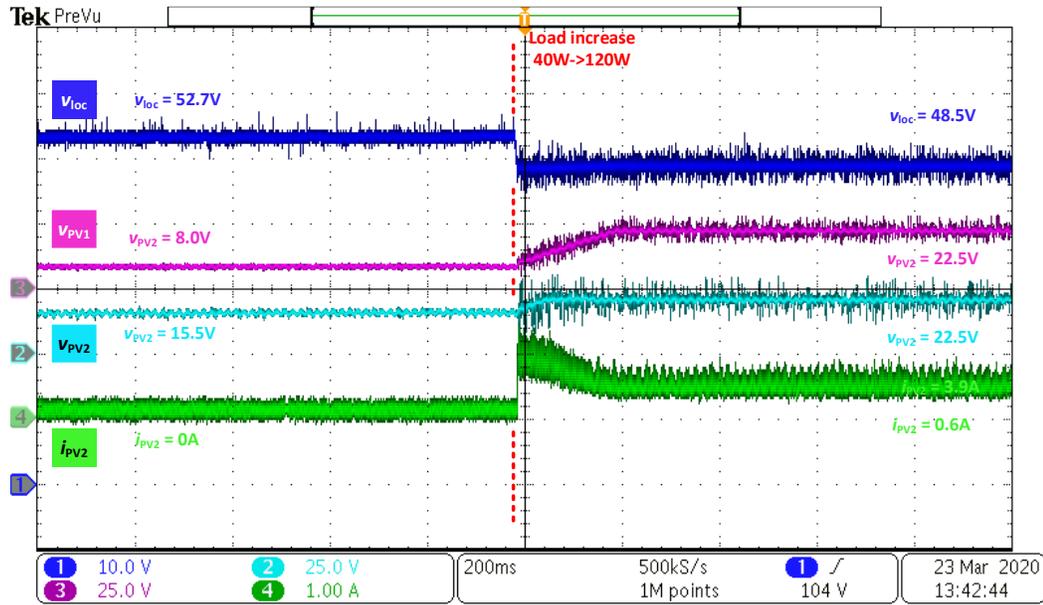


(a)

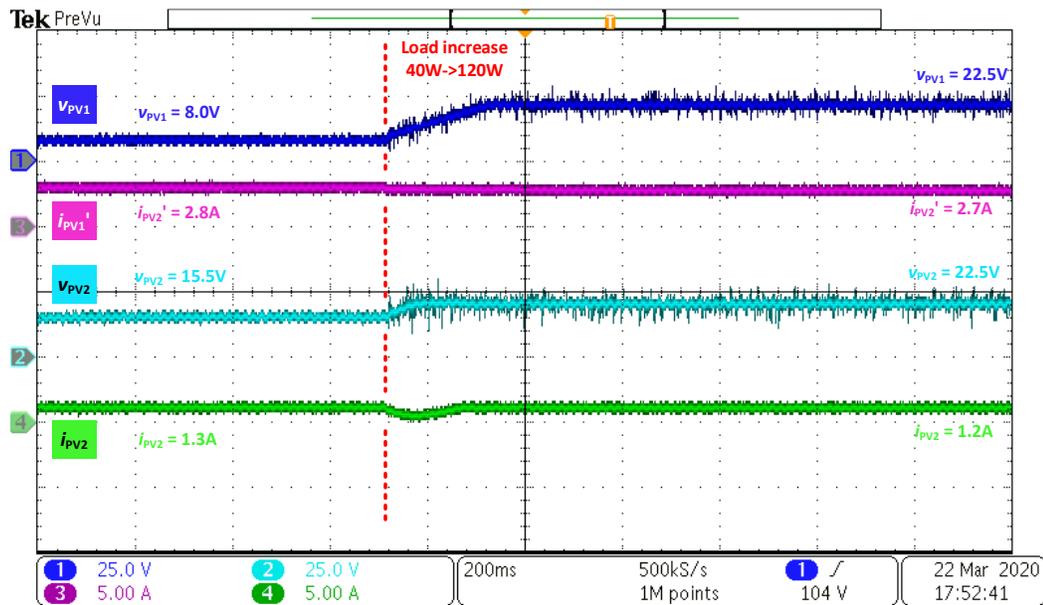


(b)

Figure 2-18. Experimental waveforms of transient that both BESs get fully charged and PV converters change to droop control with  $P_{load} = 50W$ ,  $P_{MPPT1} = 60W$  and  $P_{MPPT2} = 85W$ , where (a) shows local bus voltage, PV panel voltages and BES current, and (b) shows PV panel voltages and currents.



(a)



(b)

Figure 2-19. Experimental waveforms of transient that load step increases by 80W and PV converters change back to MPPT control with  $P_{MPPT1} = 60W$  and  $P_{MPPT2} = 25W$ , where (a) shows local bus voltage, PV panel voltages and one BES current, and (b) shows PV panel voltages and currents.

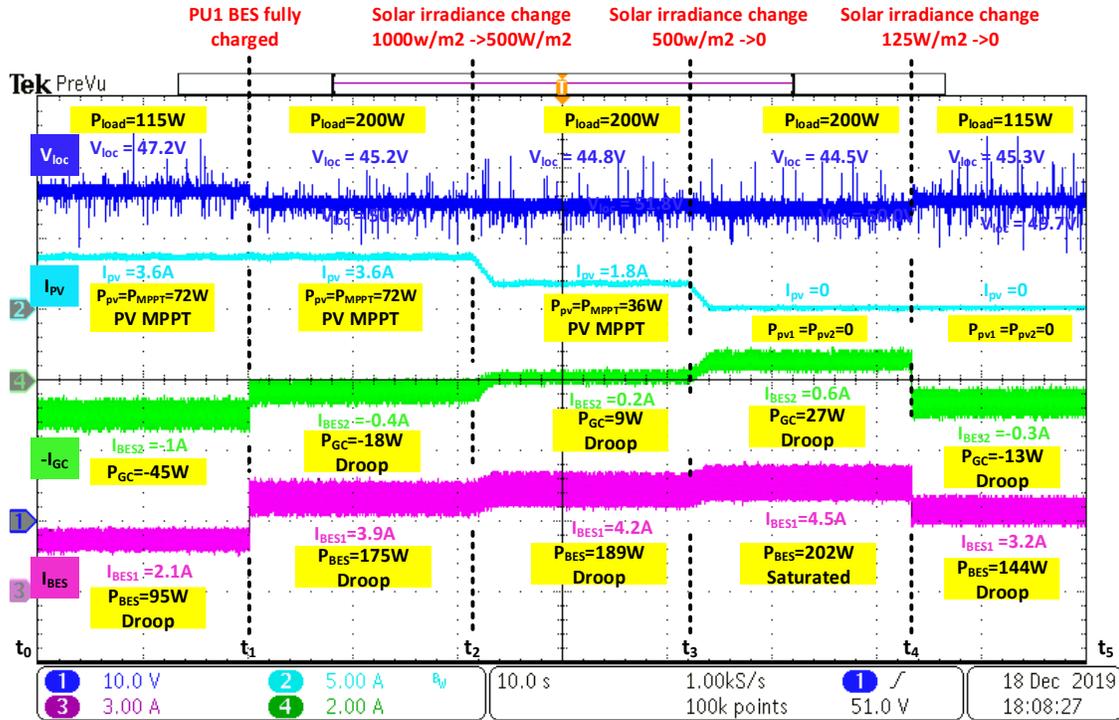


Figure 2-20. Experimental waveforms of a PU and a GC showing BES-GC droop coordination.

## 2.6 Conclusion

In this chapter, a module-based Plug-n-Play (PnP) microgrid (MG) is proposed with fully decentralized control. The proposed MG is based on PnP modules namely power units (PU). Each PU can work as a standalone unit, and with proposed decentralized control technique multiple PUs can be put into a group to scale up the system capacity in an ad-hoc and PnP manner. Groups can be further interconnected through a public bus with gateway converters. Control of each converter just requires local information while power sharing, SoC balancing and mode adaption can be achieved simultaneously in a communication-less manner. The proposed architecture allows people to organically develop power networks in a bottom-up way with PnP modules, which is suitable for electrification in rural areas. The performance of proposed MG and control method are

studied analytically and verified by simulation and experimental tests. The results show that, with the proposed method, an ad-hoc low-cost MG with multilayer expandability can be achieved while keeping high reliability and robustness.

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# Chapter 3 Decentralized PV-BES Coordination Control with Improved Dynamic Performance for Islanded Plug-n-Play Dc Microgrid

The work described in this chapter was submitted for publication as the following paper: D. Li and C. N. M. Ho, "Decentralized PV-BES Coordination Control with Improved Dynamic Performance for Islanded Plug-n-Play Dc Microgrid," *IEEE J. Emerg. Sel. Topics Power Electron.*, major revision.

In this chapter, among the proposed control structure in last chapter, the PV-BES coordination control is specifically studied. The stability of dc microgrid under generation-dominating mode (PV voltage control) is studied with small signal analysis. The variation of PV parameters could significantly affect the control bandwidth and phase margin. A PV-BES coordination control method is proposed with BES high-pass-filter loop, makes the system more robust towards PV parameter variations and improves system voltage regulation performance under PV voltage control.

## 3.1 Abstract

In this chapter, a decentralized PV-BES coordination control method for Plug-n-Play (PnP) dc microgrid (MG) is proposed. With proposed control method, PV units can operate under dc bus voltage control when battery energy storage (BES) units are saturated due to SoC limit or charging/discharging power limit. The mode transition and power sharing are based on a wireless manner. By bypassing communication, the MG system can become more flexible and reliable. The

proposed control system contains controllers for PV converter and BES converter, respectively. The PV converter controller can achieve seamless mode transition between MPPT control and droop control. BES converter controller has a decoupled feature that a high-pass-filter (HPF) path could improve MG dynamic performance under generation-dominating mode. The BES HPF compensation overcomes the issue of poor dynamic performance under PV-dominating mode and makes the system more resistive to PV parameter variation. The Detailed design, analysis and implementation of the proposed PV-BES coordination control is provided in this paper. Simulation and experimental results have been provided to verify the concept and analytical study.

## 3.2 Introduction

Photovoltaic (PV) generation has become a mainstream power source in the past decade. Advantages of wide distribution and zero emission have made PV generation a promising energy solution for remote areas [3.1]-[3.3]. Compared to conventional centralized power system, PV generation has a distributed characteristic, which relies on microgrid (MG) as an effective way to utilize solar energy [3.4]-[3.7]. As an integration of generation, load and energy storage, MG could constantly supply stable power and support a variety of loads, while maintaining a low upfront cost and a short leading time.

Besides common centralize-designed MG, Plug-n-Play (PnP) MG has become a hot topic in both academic and industrial areas [3.8] and [3.10]. A PnP MG could further reduce the design and installation cost and allows user to grow the power network organically as demand growing [3.11]. Among the various types of MGs, dc MG has gained more attentions due to its reliability,

efficiency, and simplicity of control, which is suitable for islanded PnP MG applications [3.8]. To achieve high modularity and scalability in PnP MG, decentralized control independent from communication is usually used. Droop control is the most common used decentralized control method to achieve voltage regulation and power sharing among MG components [3.12].

Different from grid-tied MG systems, there is no main utility grid to support energy or stabilize voltage in islanded MG. The power balance needs to be maintained by local MG components. Usually, Battery Energy Storage (BES) systems are used to balance the power mismatch between generation and load with droop control [3.8]. However, a BES system cannot be available all the time due to its State-of-Charge (SoC) limit and charging/discharging power limit. Thus, it is necessary to have PV generation as bus voltage regulator when BES is saturated [3.13]. Besides Maximum Power Point Tracking (MPPT) mode, PV converters should be able to operate under droop control mode to enhance system capability of dc bus voltage regulation.

Literature [3.14] proposed a decentralized mode-adaptive control technology with dc bus signaling to achieve communication-less droop control coordination. This decentralized control method could provide higher reliability, flexibility and scalability than associating with an additional central controller and a communication link. Figure 3-1 shows the conceptual diagram. When BES is available, dc bus is under BES droop control, namely storage-dominating mode. When BESs are full or at maximum charging power, dc bus voltage will rise up and PV will operate in droop control mode rather than MPPT mode, namely generation-dominating mode. When BESs are drained or at maximum discharging power, dc bus voltage will decrease and MG will inject power from outer network or reduce load, namely usage-dominating mode. For study of islanded MG, this paper is more focused on generation-dominating mode and storage-dominating mode.

Besides mode adaption, PV generation need to be able to operate under bus voltage control mode while most of current PV products only considers MPPT control. However, the conventional droop control is usually used for BES system [3.15]. It would have a poor performance when applying to PV generation. The bus voltage regulation could become very weak under generation-dominating mode, especially at light-load condition. The PV parameters could vary a lot due to different weather conditions, which also increase the design difficulty of control system. As a result, the transient could have very large overshoot which could damage system or cause safety problems [3.16]. Thus, for PV generation, it is neither robust nor safe to simply apply droop control in generation-dominating mode,

Literatures [3.13] and [3.17] have provided some solutions to solve this problem to use other control methods rather than conventional V-I droop control. Paper [3.13] proposed to use model predictive control to achieve both MPPT control and droop control of PV generation system. However, the mode transition relies on a switch to select mode which reduces system robustness and the control algorithm is complicated which requires more advanced computing units. Paper [3.17] proposed a control method that the inner loop controls  $dP/dV$  to overcome the drawback of lack of loop gain at MPP with conventional inner PV voltage loop. However, it highly relies on accurate measurement and derivative calculation which can be expensive and is less robust towards noises. Other approaches use additional devices, e.g. [3.18] used super capacitors, to help voltage regulation under PV-dominating mode, which could increase cost and reduce system reliability due to the additional components.

This chapter proposed a method using existing BES system to compensate the transient energy and keep the voltage regulation at high performance even under generation-dominating mode. The conventional BES controller is separated into two paths, a low-pass-filter (LPF) path and a high-

pass-filter (HPF) path. The LPF path balances power at steady state and the HPF path balances power at transient. The LPF and HPF paths have separate SoC limit and charging/discharging limit. Thus, even when BES is saturated, BES can still provide dynamic compensation. The combined performance of two control paths are same as conventional I-V droop control. With proposed method, the microgrid can be kept stable and robust under generation-dominating mode with PV generation without any additional cost.

The contribution of this chapter:

1) Proposed decentralized control for PV and BES converters respectively are with seamless mode transitions, which is more robust and highly suitable for PnP MG.

2) Provided small signal models for PV converter under bus voltage droop control. The effect of PV parameter variation is analyzed.

3) Proposed a decoupled BES control method that BES can still provide dynamic compensation under PV-dominating mode which enhances voltage regulation performance under PV-dominating mode towards PV parameter variation.

The chapter is organized as following: In 3.3, the proposed control system for PV and BES converters are introduced respectively. In 3.4, small signal analysis of PV bus voltage control is conducted on each control loop and the overall system, the effect of PV parameter variation and proposed BES HPF compensation are studied. 3.5 provides simulation and experiment results to verify the proposed coordination control. And conclusion is given in 3.6.

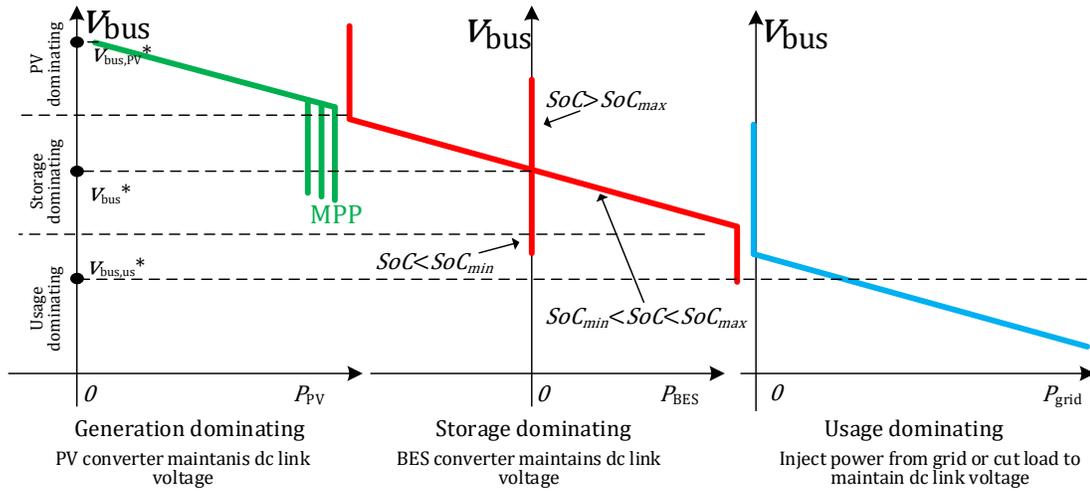


Figure 3-1. Decentralized mode adaptive using dc bus signaling.

### 3.3 Proposed Control System

In order to achieve PnP feature of PV and BES modules in dc microgrids, a fully decentralized control system independent from communication is proposed in this chapter. The control system contains individual controllers for BES converter and PV converter, respectively. With proposed control method, control parameters of existing converters do not need any adjustment when a new PV or BES module is installed into the MG. The robustness and fast response of dc link voltage regulation can be maintained under both storage-dominating and generation-dominating modes. The general droop coordination is based on dc bus voltage signalling as shown in Figure 3-1. Detailed design is given as following.

### 3.3.1 Proposed PV Converter Control Method

Figure 3-2 shows the proposed mode adaptive PV control diagram. There are three control loops where the inner loop controls PV output current, the middle loop controls PV terminal voltage and the outer loop is V-I droop control loop. The output of outer  $v_{bus}$  loop goes through a saturator, of which the upper limit is set to MPP voltage  $V_{MPP}$ . By setting the rated bus voltage of PV droop control,  $V_{bus,PV}^*$ , higher than that of BES converters, the output of  $v_{bus}$  PI controller will always be saturated to  $V_{MPP}$ , as long as the bus voltage is regulated by BES converters. When BESs are overcharged,  $v_{bus}$  will rise higher than  $v_{dp,ref}$ , and, as a result,  $v_{PV,ref}$  will decrease to lower than  $V_{MPP}$ . Thus, the PV module will operate with reduced output power, and the seamless mode transition of PV module can be achieved. Noted that the saturation characteristic of  $v_{PV,ref}$  requires an integrator in the droop control, which explains why V-I droop control is used for PV converter control rather than I-V droop control [3.19].

Different from a typical V-I droop controlled system, the proposed PV controller has three control loops. It requires two loops ( $v_{pv}$  loop and  $i_{pv}$  loop) to stabilize PV output power rather than a simple current loop for BES applications. And since the bandwidth of MPPT control is much slower than the PV voltage loop, in steady state,  $i_{pv}$  is equal to  $i_{pv0}$ . Thus  $i_{pv}$ , rather than  $i_{pv0}$  can be used for MPPT controller to reduce the number of current sensors.

The maximum inner loop bandwidth is limited by switching frequency, and each control loop should typically have a 5-10 times bandwidth difference with their neighbor. As a result, increased number of control loops will deteriorate the outer loop dynamic performance. The controller performance will be discussed in Section III with a small signal analysis. And the proposed BES

converter controller, which will be discussed in next sector, will provide dynamic compensation to help voltage regulation under PV-dominating mode to address this issue.

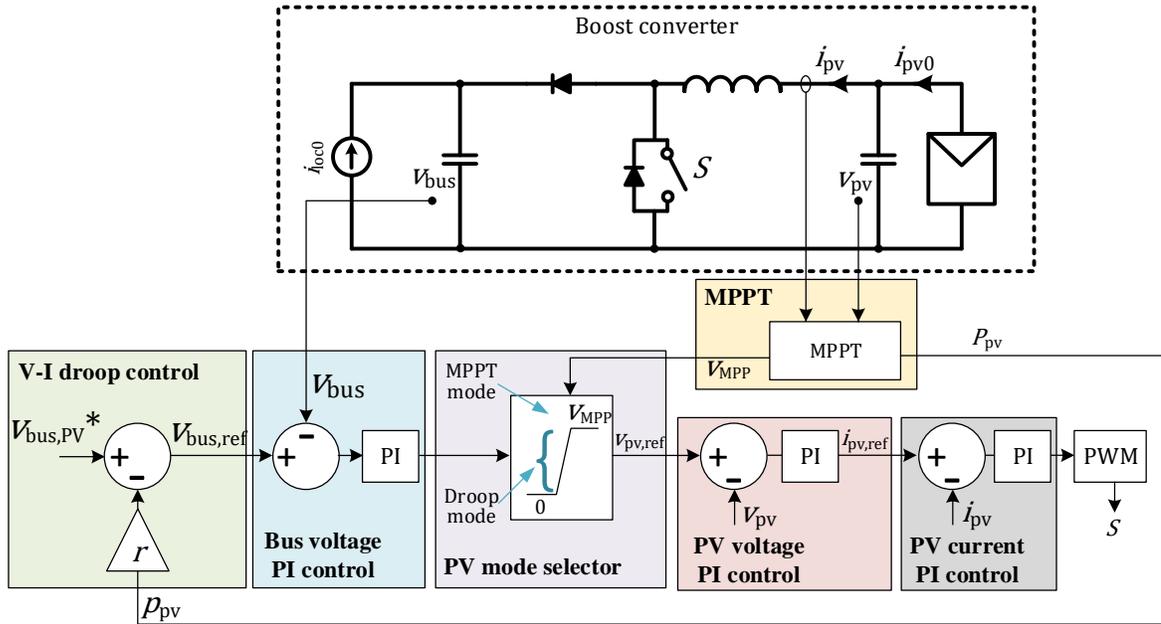


Figure 3-2. Block diagram of PV converter controller with seamless mode selection.

### 3.3.2 Proposed BES Converter Control Method

As mentioned above, PV droop control has a relatively poor dynamic performance on bus voltage regulation. Furthermore, the power flow of PV converter is unidirectional. As a result, at zero load condition, if BESs cannot further absorb energy, the bus voltage will be kept at the peak overshoot value due to the energy cannot be consumed. Thus, it is necessary to keep the ability of dynamic regulation of BES converters even under generation-dominating mode.

Different from PV converter, BES converter does not need complicated mode transition. I-V droop control can be used. Only one current loop is used in I-V droop control. The bandwidth can

be much higher than that of V-I droop control. With BES helping PV droop control, the dynamic response can be kept at high performance under both storage-dominating mode and generation-dominating mode.

Figure 3-3 shows the block diagram of proposed BES controller. The conventional I-V droop control is decoupled into two paths with a low-pass filter (LPF) and a high-pass filter (HPF). The LPF path could provide the ability of power sharing and power balance at steady state. The HPF path which is a dynamic compensation path is used to compensate transient energy. The combined performance is similar to that of conventional I-V droop control if the time constants of LPF and HPF are selected as the same. The decoupled design has following advantages,

1. Different current limits can be put on two paths. The main power flow is determined by the LPF path. The HPF path only has minor effect on energy exchange, which will not affect BES SoC level significantly. Thus, BES dynamic compensation path can be kept active even when LPF path is saturated. TABLE 3-I shows a design example of saturator limits.
2. Different droop coefficient can be applied to two paths. The LPF path can have a large  $m_1$  value to narrow the bus voltage steady state error. The HPF path can have a relatively small  $m_2$  value to avoid impact of noise.

For steady state analysis, the effect of HPF path can be neglected.

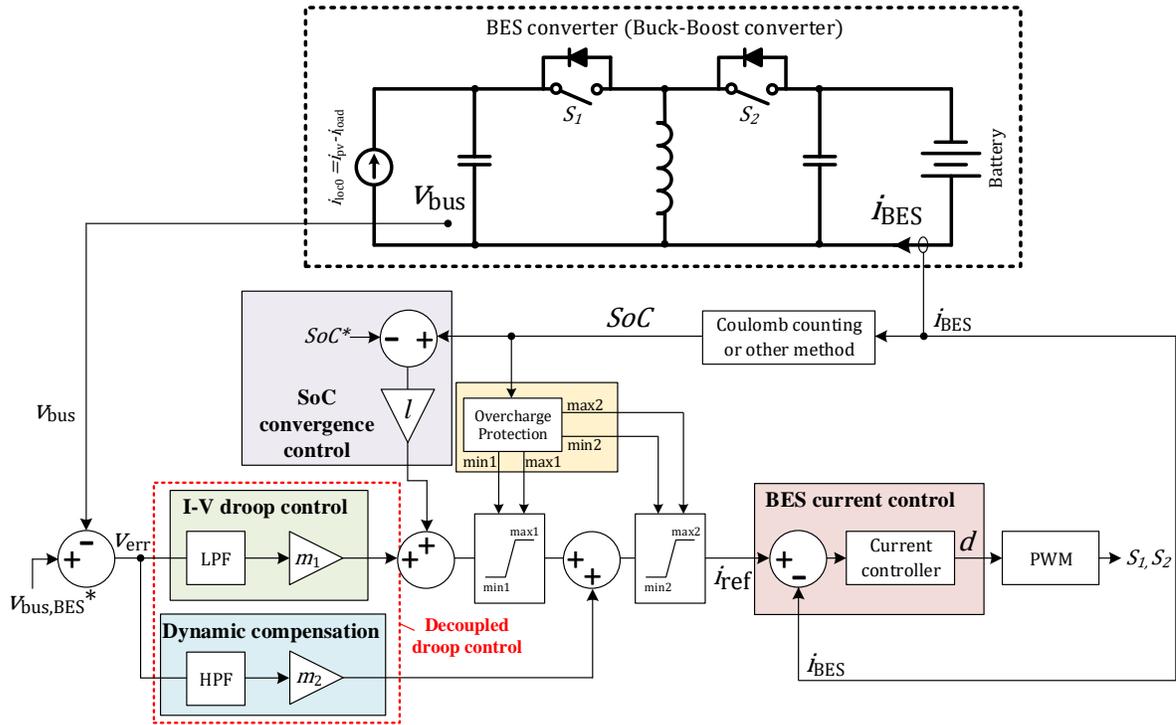


Figure 3-3. Block diagram of SoC-based droop control for BES converter.

A SoC term is also added to the BES I-V droop control to achieve SoC self-convergence. Different from existing SoC self-convergence control that modifies droop coefficient [3.15],[3.20], the proposed control adds an offset to the droop line to better fit the dc bus voltage signaling technology. Besides the conventional I-V droop term that output current is proportional to voltage error, it contains an SoC ramp term. With the additional term, the output current will slightly increase when the BES SoC level is higher than SoC\*; the output current will slightly decrease when SoC level is lower than SoC\*. Thus, SoCs among multiple BESs can get to a convergence.

TABLE 3-I SATURATOR LIMITS DESIGN EXAMPLE

<i>SoC</i> level	Saturator on LPF path		Saturator for combined current reference	
	min1	max1	min2	max2
<i>SoC</i> >100%	0	5A	0	8A
<i>SoC</i> >95%	0	5A	-6A	8A
30%< <i>SoC</i> <95%	-3A	5A	-6A	8A
<i>SoC</i> <30%	-3A	0	-6A	8A
<i>SoC</i> >25%	-3A	0	-6A	0

TABLE 3-II SYSTEM SPECIFICATION

Symbol	Value	Symbol	Value
$V_{bus,BES}^*$	48 V	$V_{bus,PV}^*$	53 V
$C_{bus}$	660 uF	$C_{PV}$	200 uF
$k_{p,bus}$	3.5	$m_1$	1
$k_{i,bus}$	100	$m_2$	1
$k_{p,PV}$	10	$t_{LPF}$	0.01
$k_{i,PV}$	2	$t_{HPF}$	0.01
$r$	1/100	$V_{BES}$	48 V

## 3.4 Small Signal Analysis

As mentioned, with conventional V-I droop control, dc bus voltage regulation has a relatively poor dynamic performance with PV droop control due to the low control bandwidth and lack the ability of bidirectional power flow. A decoupled BES droop control strategy is proposed to improve system performance under generation-dominating mode. This section mainly studies the voltage regulation performance under generation-dominating mode with small signal analysis.

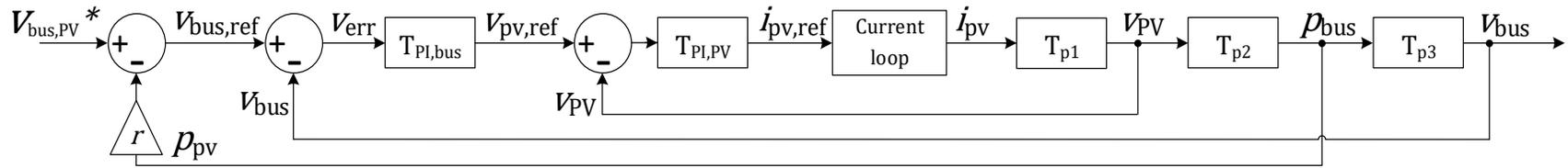
### 3.4.1 System Modeling

Figure 3-4 (a) shows the control block diagrams of  $v_{\text{bus}}$  droop control under generation-dominating mode without BES HPF compensation. Figure 3-4 (b) shows the control block diagram that with BES HPF compensation. It can be seen that the BES HPF compensation could add a feedforward control path to the system.

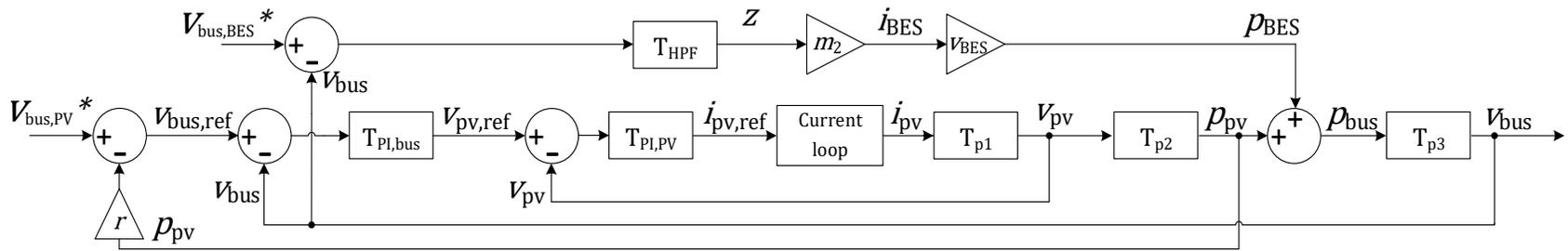
The current controller of PV converter can be achieved with hysteresis controller or PI controller with high control bandwidth. The response speed of PV current loop is much faster than that of outer loops. To simplify the study, the closed-loop transfer function of PV current loop can be regard as 1.

PV arrays has a nonlinear I-V characteristic. Usually a linearized express can be written as,

$$\tilde{i}_{\text{PV}0} = K_{\text{PV}} \tilde{v}_{\text{PV}} \quad (3-1)$$



(a)



(b)

Figure 3-4. Control block diagrams of  $v_{bus}$  droop control under generation-dominating mode, (a) without BES decoupled droop control, and (b) with BES decoupled control.

where  $K_{PV}$  can be expressed as,

$$K_{PV} = \frac{N_p I_{sc,n}}{[\exp(V_{oc,n}/aV_t) - 1] \cdot aN_s V_t} \cdot \exp\left(\frac{v_{PV}}{aN_s V_t}\right) \quad (3-2)$$

$K_{PV}$  is always negative and detailed parameters for PV modeling can be found in [3.21] and [3.22].

By adding perturbation to  $v_{PV}$  differential equation,

$$C_{PV} \frac{d(V_{PV} + \tilde{v}_{PV})}{dt} = I_{PV0} + \tilde{i}_{PV0} - I_{PV} - \tilde{i}_{PV} \quad (3-3)$$

Putting (3-1) into (3-3),  $T_{p1}$  can be expressed as,

$$T_{p1} = \frac{\tilde{v}_{PV}(s)}{\tilde{i}_{PV}(s)} = \frac{1}{-C_{PV} \cdot s + K_{PV}} \quad (3-4)$$

By adding perturbation to  $p_{PV}$  calculation,

$$P_{PV} + \tilde{p}_{PV} = (V_{PV} + \tilde{v}_{PV}) \cdot (I_{PV} + \tilde{i}_{PV}) \quad (3-5)$$

Put (3-4) into (3-5),  $T_{p2}$  can be obtained as,

$$T_{p2} = \frac{\tilde{p}_{PV}(s)}{\tilde{v}_{PV}(s)} = K_{PV} V_{PV} + I_{PV} = K' \quad (3-6)$$

From (3-6), at steady state MPP operation,

$$\frac{dp_{PV}}{dv_{PV}} = K' = 0 \quad (3-7)$$

Figure 3-5 shows the relationships among PV parameters and PV curve. Notice that, to guarantee the system a negative feedback system,  $T_{p2}$  or  $K'$  has to be positive. Thus, PV has to work on the left side of MPP to guarantee stable operation.

By adding perturbation to  $v_{bus}$  energy balance equation,

$$\frac{c_{bus}}{2} \frac{d(V_{bus} + \tilde{v}_{bus})^2}{dt} = P_{bus} + \tilde{p}_{bus} \quad (3-8)$$

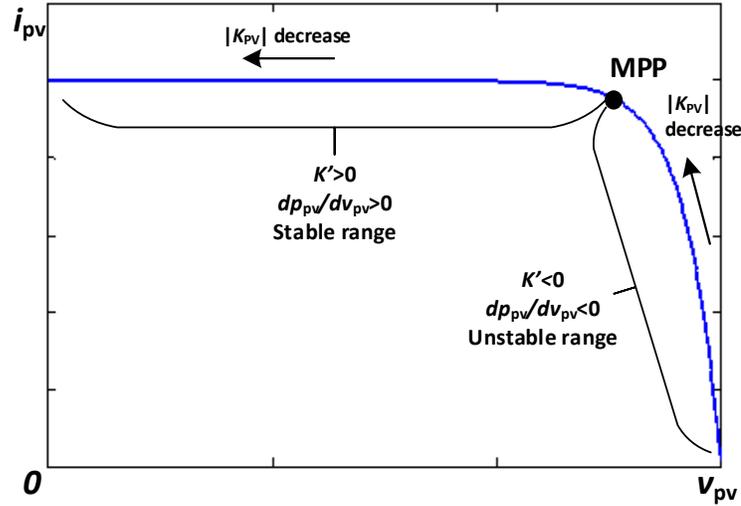


Figure 3-5. PV curve showing parameters variation.

$T_{p3}$  can be obtained as,

$$T_{p3} = \frac{\tilde{v}_{bus}(s)}{\tilde{p}_{bus}(s)} = \frac{1}{C_{bus}V_{bus}s} \quad (3-9)$$

When without BES HPF loop,  $p_{bus} = p_{PV}$ ; when with BES HPF loop,  $p_{bus} = p_{PV} + p_{BES}$ .

Transfer functions of PI controllers for  $v_{bus}$  loop and  $v_{PV}$  loop can be expressed as,

$$T_{PI,bus} = \frac{\tilde{v}_{PV,ref}(s)}{\tilde{v}_{err}(s)} = \frac{k_{p,bus}s + k_{i,bus}}{s} \quad (3-10)$$

$$T_{PI,PV} = \frac{\tilde{i}_{PV,ref}(s)}{\tilde{v}_{pv}(s)} = -\frac{k_{p,PV}s + k_{i,PV}}{s} \quad (3-11)$$

The HPF in BES dynamic compensation loop can be written as,

$$T_{HPF} = \frac{t_{HPF}s}{t_{HPF}s + 1} \quad (3-12)$$

The closed-loop state equations for the system can be expressed as,

$$\dot{X} = A \cdot X + B \cdot U \quad (3-13)$$

For system given in Figure 3-4 (a), the state vector can be selected as,

$$X_1 = [\tilde{v}_{bus} \quad \tilde{v}_{PV} \quad \tilde{v}_{PV,ref} \quad \tilde{i}_{PV}]^T \quad (3-14)$$

From (3-6) and (3-9), the differential equation of  $\tilde{v}_{bus}$  is,

$$\frac{d\tilde{v}_{bus}}{dt} = \frac{\tilde{p}_{bus}}{C_{bus}V_{bus}} = \frac{K'}{C_{bus}V_{bus}} \tilde{v}_{PV} \quad (3-15)$$

From (3-4), the differential equation of  $\tilde{v}_{PV}$  is,

$$\frac{d\tilde{v}_{PV}}{dt} = \frac{K_{PV}}{C_{PV}} \tilde{v}_{PV} - \frac{1}{C_{PV}} \tilde{i}_{PV} \quad (3-16)$$

From (3-10), the differential equation of  $\tilde{v}_{PV,ref}$  is,

$$\frac{d\tilde{v}_{PV,ref}}{dt} = k_{p,bus} \left( rK' \frac{d\tilde{v}_{PV}}{dt} - \frac{d\tilde{v}_{bus}}{dt} \right) + k_{i,bus} (rK' \tilde{v}_{PV} - \tilde{v}_{bus}) \quad (3-17)$$

From (3-11), the differential equation of  $\tilde{i}_{PV}$  is,

$$\frac{d\tilde{i}_{PV}}{dt} = -k_{p,PV} \left( \frac{d\tilde{v}_{PV,ref}}{dt} - \frac{d\tilde{v}_{PV}}{dt} \right) - k_{i,PV} (\tilde{v}_{PV,ref} - \tilde{v}_{PV}) \quad (3-18)$$

From (3-18)-(3-21), the system matrix  $A_1$  can be written as follow,

$$A_1 = \begin{bmatrix} 0 & \frac{K'}{C_{bus}V_{bus}} & 0 & 0 \\ 0 & \frac{K_{PV}}{C_{PV}} & 0 & -\frac{1}{C_{PV}} \\ -k_{i,bus} & a_{32} & 0 & -\frac{rK'k_{p,bus}}{C_{PV}} \\ k_{p,pv}k_{i,bus} & a_{42} & -k_{i,pv} & a_{44} \end{bmatrix} \quad (3-19)$$

where

$$a_{32} = -\frac{rK'k_{p,bus}k_{p,pv}}{C_{PV}} + rK'k_{i,bus} - \frac{k_{p,bus}K'}{C_{bus}V_{bus}}$$

$$a_{42} = -k_{p,pv} \cdot a_{32} + \frac{k_{p,pv}K_{PV}}{C_{PV}} + k_{i,pv}$$

$$a_{44} = \frac{k_{p,pv}(1 - rK'k_{p,bus})}{C_{PV}}$$

For system given in Figure 3-4 (b), the state vector can be selected as,

$$X_2 = [ \tilde{v}_{bus} \quad \tilde{v}_{PV} \quad \tilde{v}_{PV,ref} \quad \tilde{i}_{PV} \quad \tilde{z} ]^T \quad (3-20)$$

Follow the similar approach, the system matrix  $A_2$  can be written as follow,

$$A_2 = \begin{bmatrix} 0 & \frac{K'}{C_{bus}V_{bus}} & 0 & 0 & \frac{mV_{bat}}{C_{bus}V_{bus}} \\ 0 & \frac{K_{PV}}{C_{PV}} & 0 & -\frac{1}{C_{PV}} & 0 \\ -k_{i,bus} & a_{32} & 0 & -\frac{rK'k_{p,bus}}{C_{PV}} & 0 \\ k_{p,pv}k_{i,bus} & a_{42} & -k_{i,pv} & a_{44} & 0 \\ 0 & -\frac{K'}{C_{bus}V_{bus}} & 0 & 0 & -\frac{1}{t_{HPF}} \end{bmatrix} \quad (3-21)$$

where  $a_{32}$ ,  $a_{42}$ ,  $a_{44}$  are same as provided in (3-19).

### 3.4.2 PV voltage loop

With (3-11) and (3-4), the  $v_{PV}$  loop open-loop transfer function can be obtained,

$$T_{OL,VPV} = T_{PI,PV} \cdot T_{p1} = \frac{k_{p,PV}s + k_{i,PV}}{-C_{PV} \cdot s^2 + K_{PV} \cdot s} \quad (3-22)$$

Assuming the PV current loop crossover frequency is around 4000 Hz. The crossover frequency of  $v_{PV}$  loop should be 5 times lesser at least, which is around 800 Hz. With parameters given in TABLE 3-II, bode diagram of  $v_{PV}$  open-loop transfer function can be obtained as Figure 3-6. With  $K_{PV}$  varying in the range of -0.01 to -0.1, the crossover frequency kept close to 717 Hz

with a phase margin in the range of 88.5 to 94.2 degree. Thus, the PV voltage loop is robust towards PV parameters variation.

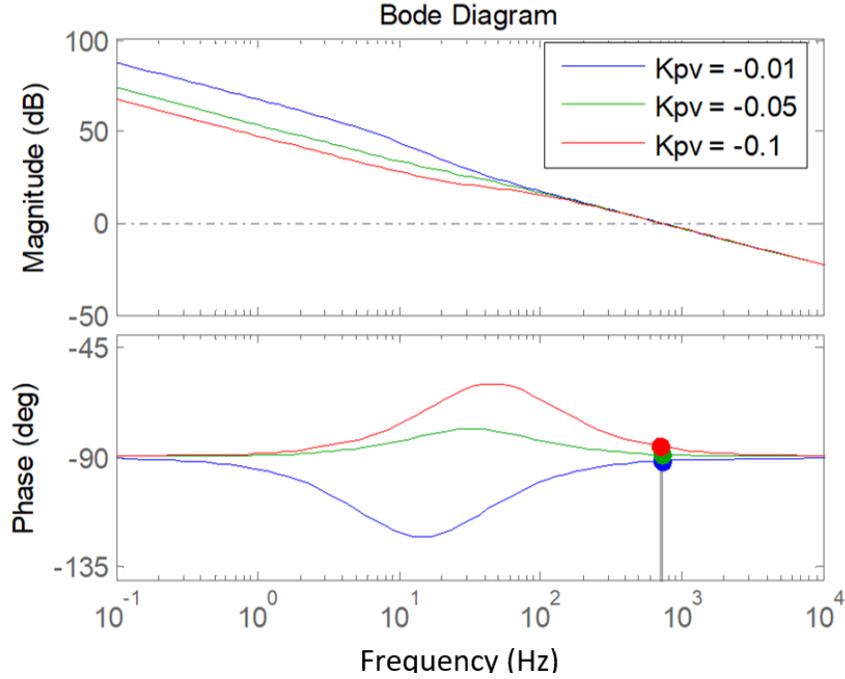


Figure 3-6. Bode diagrams of PV voltage loop.

### 3.4.3 Dc Bus Voltage Loop

#### A. Without BES compensation

The closed-loop transfer function between  $i_{pv}$  and  $v_{pv,ref}$  can be derived as,

$$T_{CL,VPV} = \frac{T_{OL,VPV}}{1+T_{OL,VPV}} \quad (3-23)$$

Without BES HPF loop, the  $v_{bus}$  open-loop transfer function is,

$$T_{OL,Vbus1} = T_{PI,bus} \cdot T_{CL,VPV} \cdot T_{p2} \cdot T_{p3} \quad (3-24)$$

The open loop gain of (3-24) can be derived as,

$$K_{OL,V_{bus1}} = \frac{k_{p,PV} \cdot k_{p,bus} \cdot K'}{C_{PV} C_{bus} V_{bus}} \quad (3-25)$$

Notice that  $K'$  may vary a lot due to different operation conditions of PV generation, which could affect the overall system performance. Especially when the operating point is close to MPP,  $K'$  will be close to zero and slows down the system response.

Figure 3-7 shows bode diagrams of dc bus voltage loop with  $K'$  varying from 0.02 to 1.8. System crossover frequency is badly affected due to  $K'$  change. When  $K'$  is reduced, the control bandwidth decreases significantly (4.8 Hz when  $K'=0.2$ , 1.3 Hz when  $K'=0.02$ ), with insufficient phase margins (45 degree when  $K'=0.2$ , 15.5 degree when  $K'=0.02$ ).

Furthermore  $K'$  has to be positive to guarantee a positive loop gain. Thus, considering (3-7), it is necessary to keep PV generation operating in the range of  $\frac{dp_{PV}}{dv_{PV}} > 0$ . However, the output of MPPT controller changes very slow. The operation could fall into unstable region at transient for a very short time.

Thus, in generation-dominating mode, the voltage regulation solely relying on PV converter has relatively poor performance and less robustness. A compensation from other MG components is necessary to keep the bus voltage regulation under acceptable performance.

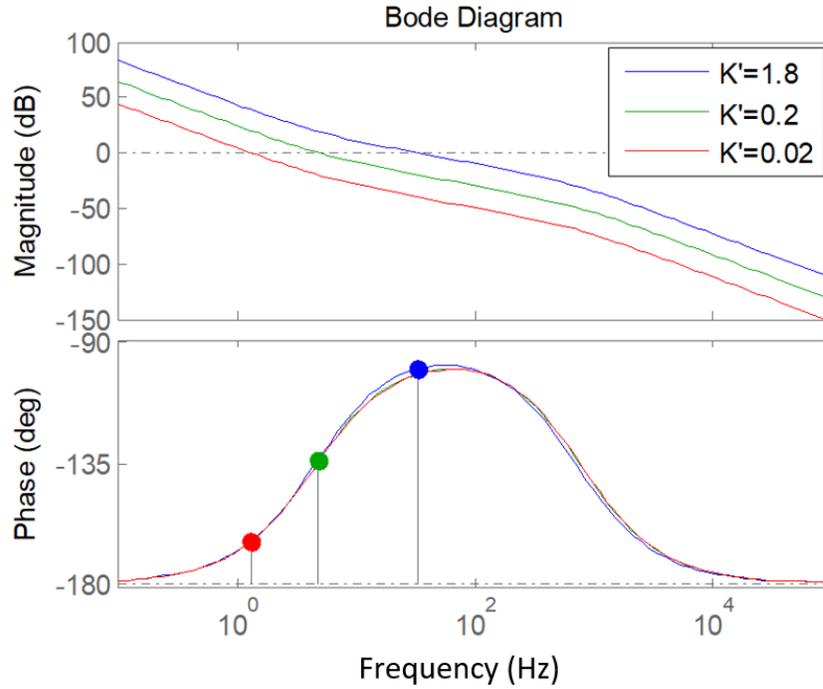


Figure 3-7. Bode diagrams of bus voltage loop without BES compensation.

### B. With BES compensation

As mentioned, a compensation from other MG components is necessary to keep a stable bus voltage regulation performance. This can be achieved by using existing BESs. Though in generation-dominating mode, BES is saturated, it can still provide dynamic compensation which would not cause significant amount of energy flow.

As Figure 3-4 (b) showing the control diagram, the  $v_{bus}$  open-loop transfer function is,

$$T_{OL,Vbus2} = (T_{PI,bus} \cdot T_{CL,VPV} \cdot T_{p2} + T_{HPF} \cdot m_2 \cdot V_{BAT}) \cdot T_{p3} \quad (3-26)$$

Figure 3-8 shows bode plots of transfer function (3-26) with different PV parameters. It can be seen the crossover frequency stays constantly around 1200 Hz with phase margin around 90 degree towards  $K'$  variation. And the crossover frequency can be kept at a relatively high value

despite the inner PV voltage loop restriction. Thus, the BES compensation loop, as a feed-forward loop, which is independent from PV parameters, can make the system more resistive towards PV parameter change and improve system's dynamic performance.

Thus, with BES compensation, even under generation-dominating mode, the dc bus voltage regulation can be kept robust and with a good dynamic performance.

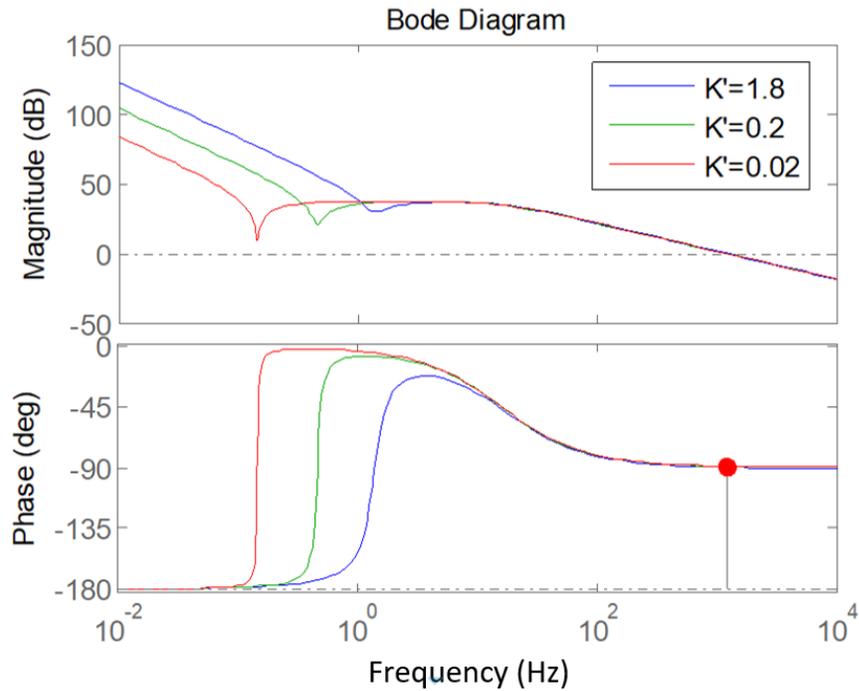


Figure 3-8. Bode diagrams of bus voltage loop with BES HPF compensation.

### 3.4.4 Overall System Analysis

#### A. Without BES compensation

With state matrix given by (19), Figure 3-9 (a) shows changes of dominating poles along with PV operating point change. It can be seen the system is stable as long as  $K' > 0$ . However, when

$K' < 1.03$ , the dominating poles become a pair of conjugate poles with relatively large imaginary parts, which could lead to significant oscillation during dynamic process.

*B. With BES compensation*

With state matrix given by (3-21), Figure 3-9 (b) shows changes of dominating poles along with PV operating point change. The system is stable as long as  $K' > 0$ . And, when  $K' < 0.06$ , the dominating poles become a pair of conjugate poles with small imaginary parts ( $\omega < 1.7$  rad/s).

The system with BES compensation is less likely being oscillated: only when  $K' < 0.06$  (almost on the MPP point), dominating poles become conjugate; oscillating frequency is very low that  $\omega < 1.7$  rad/s.

However, involvement of BES compensation pushes dominating poles closer to imaginary axis due to the HPF. As a result, the dynamic response will be slowed down inevitably. Figure 3-9 (c) shows the loci with different  $t_{HPF}$ . Obviously, there is a trade-off between oscillation and dynamic response speed. In this case of dc bus voltage regulation, slow dynamic response speed is acceptable that the dc bus voltage should not have big step changes during normal operation, which will be discussed in simulation study.

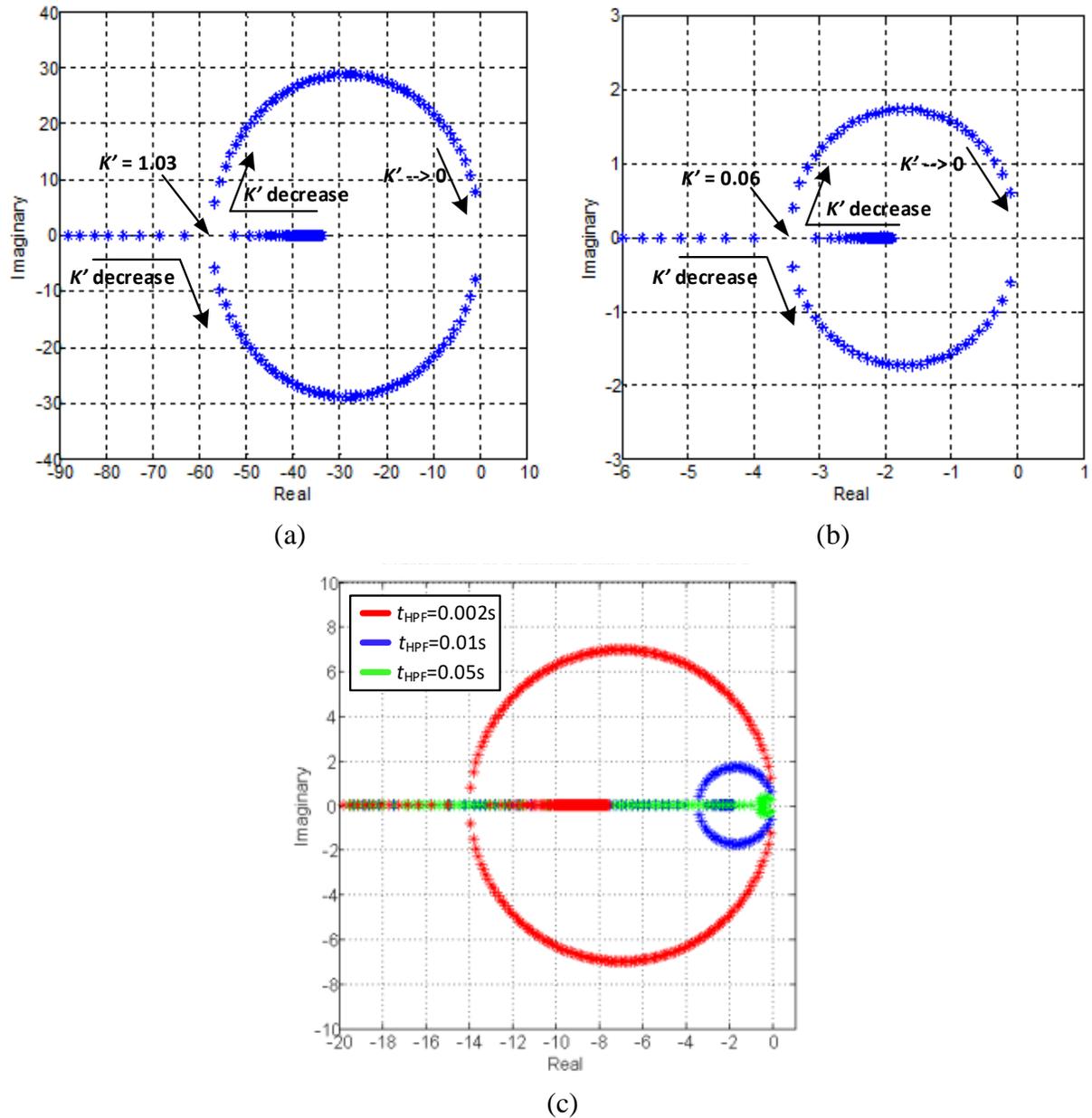


Figure 3-9. Dominating poles of overall system, (a) without BES compensation, (b) with BES compensation, (c) with different HPF time constants.

## 3.5 Simulation and Experiment Study

### 3.5.1 Simulation Study

Simulations based on PLECS are performed to verify the analytical study. TABLE 3-II shows parameters used in simulation. To validate the analytical study, one of the worst scenarios that PV changes from MPPT control to bus voltage droop control at light load is tested in simulation and experiment study.

Simulation results of PV-BES droop control coordination without BES HPF compensation are shown in Figure 3-10. At the transient, BES gets fully charged and PV converter takes over bus voltage droop control. It can be seen in Figure 3-10 (a), at 25W load, the bus voltage has a 14% overshoot at the transient of PV changing to droop control. With lighter load, in Figure 3-10 (b), the overshoot is increased to 20%, which has been far beyond acceptable voltage fluctuation range. With higher PV generation rating or less loads, the voltage spike could even be further increased.

Simulation results of PV-BES droop control coordination with BES HPF compensation are shown in Figure 3-11. In Figure 3-11 (a), at 25W load, the bus voltage only has a 4.8% overshoot at the transient of PV shifting to droop control. At 2.5W load, in Figure 3-11 (b), the overshoot is still kept around 4.7%. Though it requires much longer time to settle down as proved by loci in Figure 3-9, the bus voltage is always kept inside a very small fluctuation range, which has neglectable effect to the MG system. With BES HPF compensation, BES power is not saturated to zero immediately at the transient, it slowly reaches zero which prevent bus voltage from ramping up.

Figure 3-12 shows simulation result of two PV units and two BES units operating in parallel with proposed PV-BES coordination control. In  $t_0$ - $t_1$ , both PVs operate under MPPT (with different MPP powers); bus voltage is regulated by both BES units. At  $t_1$ , BES1 is fully charged while BES2 can still absorb surplus power. Hence in  $t_1$ - $t_2$  both PVs still work under MPPT and bus voltage is regulated solely by BES2. At  $t_2$ , BES2 also gets fully charged, PVs take over bus voltage regulation. With BES HPF compensation, the transient process is smooth with very small overshoot, and the compensated energy from BESs are equally shared by BES1 and BES2. At  $t_3$ , solar irradiance on PV1 is stepped up. With BES compensation, dc bus voltage only has a very small fluctuation towards irradiance change. At  $t_4$ , load is reduced from 30W to 5W, the voltage transient is again kept smooth with BES compensation.

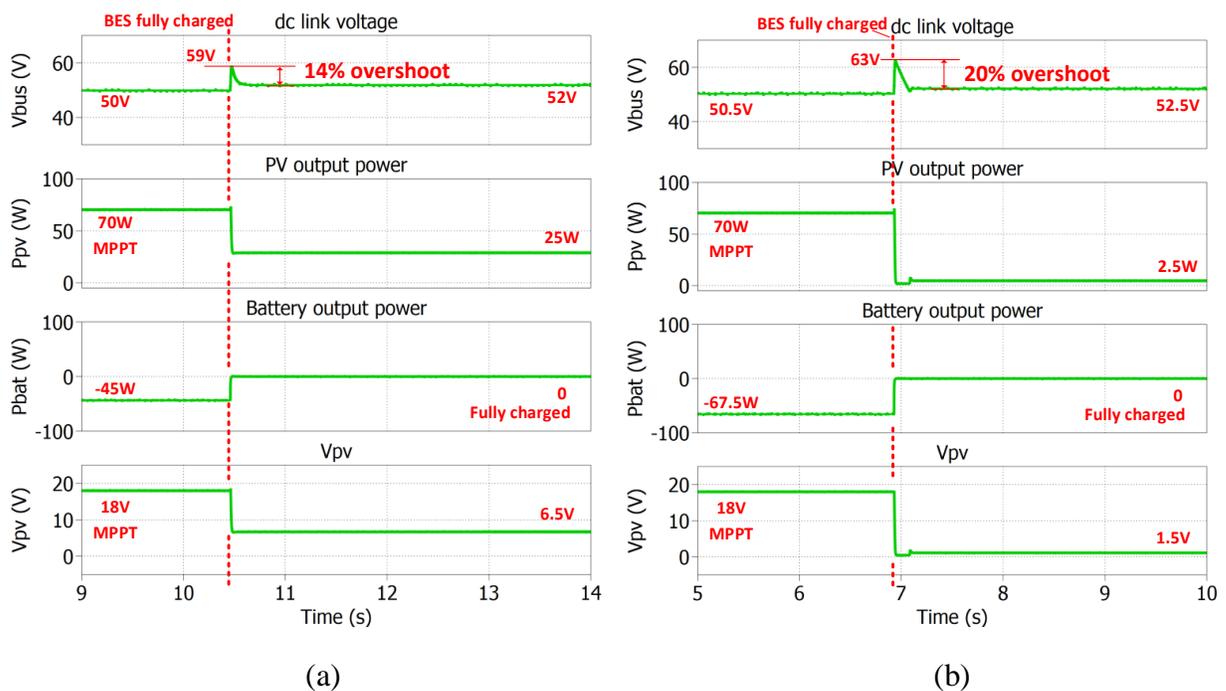


Figure 3-10. Simulation results of PV-BES droop control coordination without BES HPF compensation, (a) with 25W load, (b) with 2.5W load.

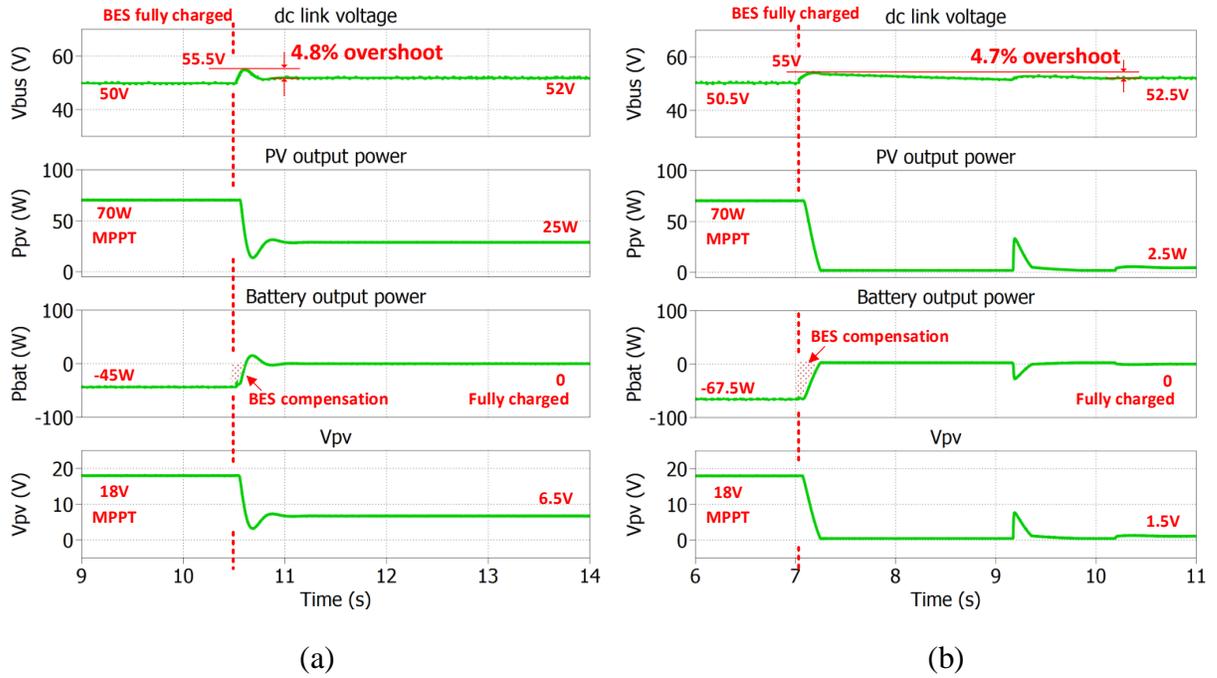


Figure 3-11. Simulation results of PV-BES droop control coordination with BES HPF compensation, (a) with 25W load, (b) with 2.5W load.

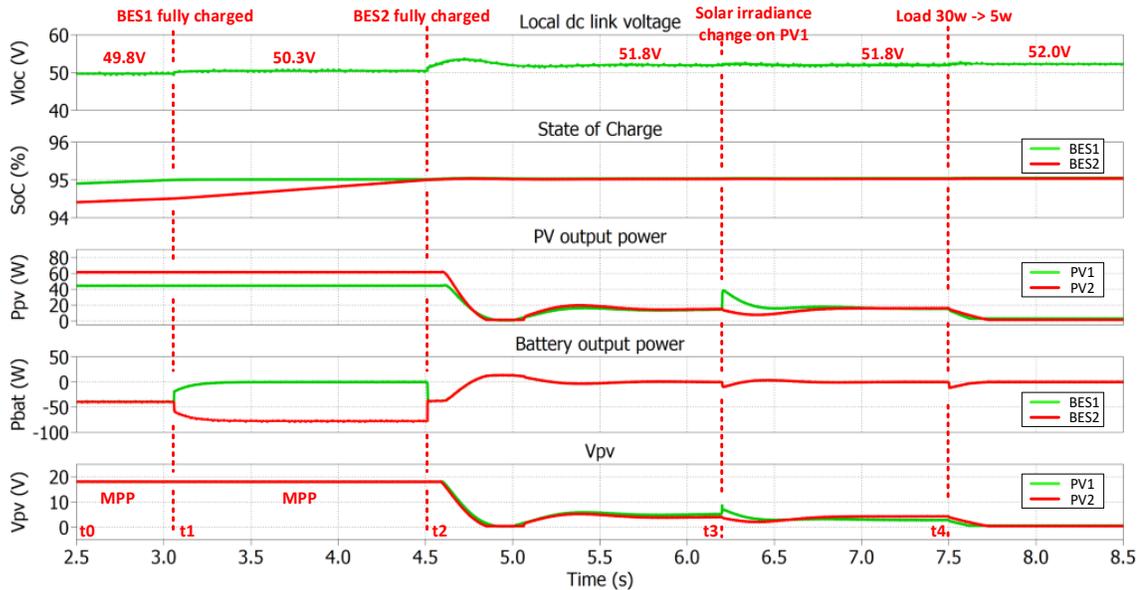


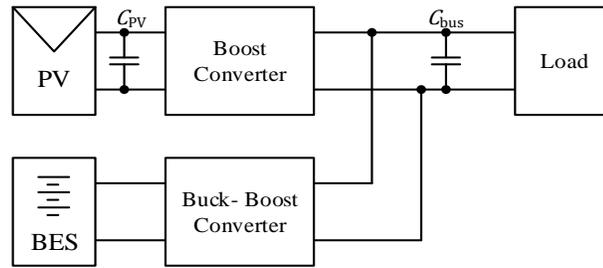
Figure 3-12. Simulation results of power sharing with proposed PV-BES coordination control, with two PV units and two BES units.

### 3.5.2 Experiment Verification

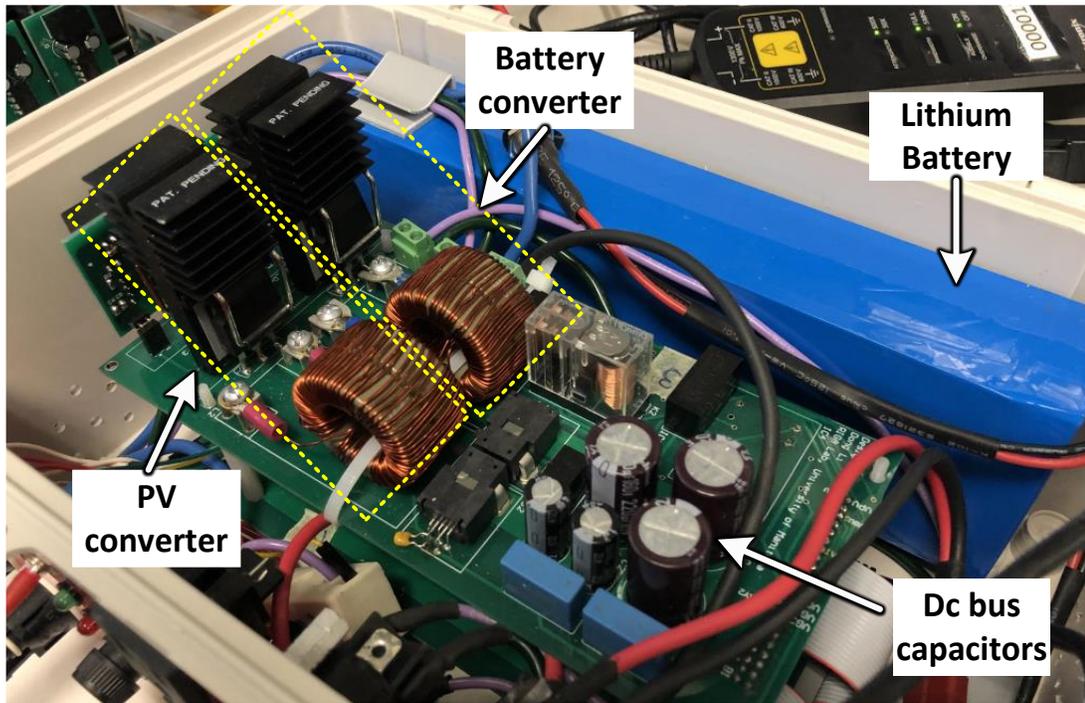
The proposed PV-BES coordination control has been verified by laboratory experiment with one PV unit and one BES unit, of which the setup is shown in Figure 3-13. A PV simulator is used to emulate PV behavior. Converters are controlled by a TI F28379d DSP. Parameters are set same as TABLE 3-II. Figure 3-14 shows experimental results of PV-BES coordination control transient with different BES HPF time constants. In Figure 3-14 (a), BES HPF is inactive or  $t_{\text{HPF}} = 0$ . The transient of PV changing to droop control causes a large overshoot on dc bus voltage, which agrees to simulation result in Figure 3-10 (a). In Figure 3-14 (b),  $t_{\text{HPF}}$  is increased to 0.01. With help of BES HPF compensation, the transient becomes much smoother with a 3V overshoot. In Figure 3-14 (c),  $t_{\text{HPF}}$  is further increased to 0.05, and the transient overshoot is further damped to around 2V, which agrees to simulation result in Figure 3-11 (a).

With proposed BES HPF compensation loop, even under very light load condition, the PV voltage regulation can be kept at a good performance. Figure 3-15 shows the experimental result that PV changing to droop control with 2.5W load. The overshoot is kept around 2V and the waveforms show a good agreement to simulation result Figure 3-11 (b).

It can be observed from all the results, that the transient has three stages (it is more obvious in Figure 3-15 due to the longer settling time). In the first stage, BES gets fully charged, bus voltage raises up, BES charging current decreases slowly due to the HPF path which keeps bus voltage from overshooting too much. In the second stage, PV output power has reduced lower than load, bus voltage decreases. The HPF path will always obstruct bus voltage change. As a result, BES will discharge in this stage. In the third stage, bus voltage reduces to the value set by droop controller; output of BES HPF settles to zero, and new steady state is reached.

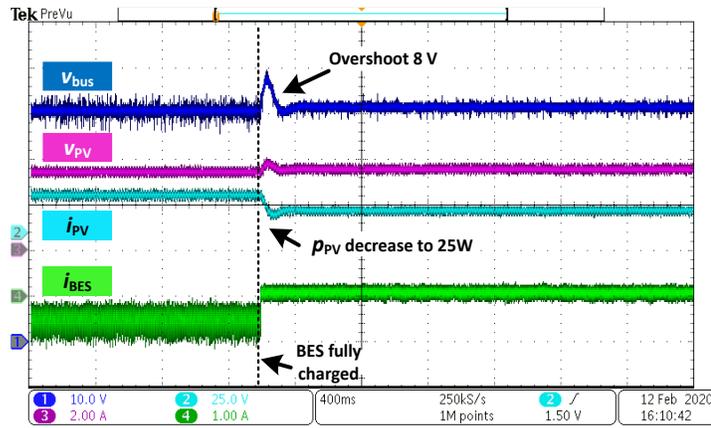


(a)

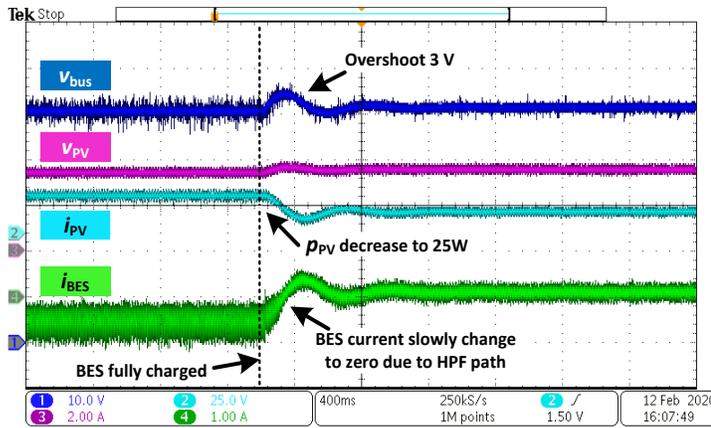


(b)

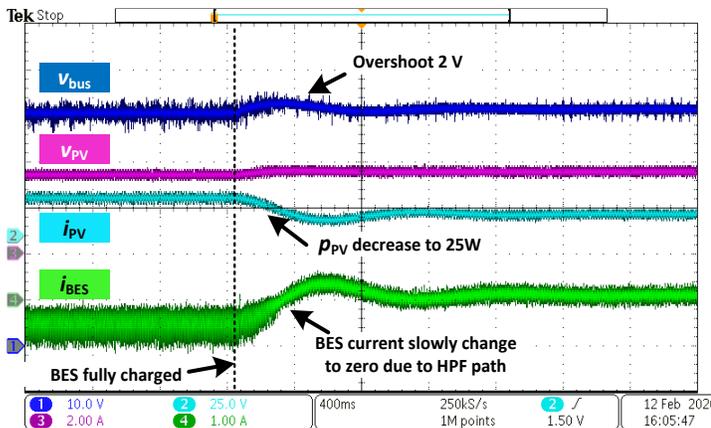
Figure 3-13. Experimental setup, (a) connection diagram, (b) photo.



(a)



(b)



(c)

Figure 3-14. Experimental results of PV-BES coordination control, at transient of PV taking over bus voltage control and load is at 25W, (a) without BES HPF compensation, (b) with BES HPF compensation and  $t_{HPF} = 0.01$ , (c) with BES HPF compensation and  $t_{HPF} = 0.05$ .

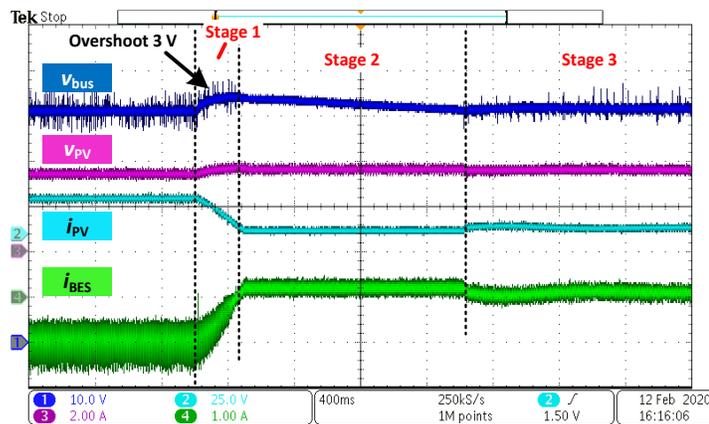


Figure 3-15. Experimental result of PV-BES coordination control, at transient of PV taking over bus voltage control and load is at 2.5W, with BES HPF compensation and  $t_{HPF} = 0.05$ .

### 3.6 Conclusion

In this chapter, a PV-BES coordination control method is proposed to overcome the control issue of bus voltage regulation under PV-dominating mode. The whole control scheme is kept in a decentralized and communication-less manner, which can be used for Plug-n-Play (PnP) microgrid. The proposed method utilizes existing BES systems. With decoupled control loops, BESs can still provide dynamic compensation even under generation-dominating mode. The proposed control method has been analyzed with small signal analysis and verified by both simulation and experimental result.

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## Chapter 4 A Delay-Tolerable Master-Slave Current-Sharing Control Scheme for Parallel-Operated Interfacing Inverters with Low-Bandwidth Communication

The work described in this chapter was published in the following paper: D. Li and C. N. M. Ho, "A Delay-Tolerable Master-Slave Current-Sharing Control Scheme for Parallel-Operated Interfacing Inverters with Low-Bandwidth Communication," *IEEE Trans. Ind. Appl.*, vol. 56, no. 2, pp. 1575-1586, March-April 2020. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2018 [4.1].

Different from the last two chapters which focus on decentralized control for the dc network, this chapter studies modular design of dc-ac grid interface, which uses communication-based control to achieve accurate power sharing and voltage regulation. In this chapter, the effect of low-bandwidth communication in a master-slave controlled system is studied with small signal analysis. A slave module low-pass-filter and feedforward loop design is proposed. With proposed design, the system is more robust towards communication delays, which makes low cost modern communication tools, e.g. Bluetooth, Zigbee, can be used in control layer.

### 4.1 Abstract

Parallel-operated inverters with common dc and ac bus can be used as interface for dc systems connecting to an ac network. High cost and complicated wiring of communication are main

drawbacks of communication-based current-sharing methods for parallel system. Many new communication tools, e.g. Power Line Communication (PLC), Bluetooth and Zigbee modules, are cheap and require no extra wire connection, but have low communication bandwidth and low data rate, which result a large communication delay and zero-order-hold period that could cause stability issues if used to transmit control signals. This paper presents a method to mitigate the instability issue caused by communication effects, in parallel grid-tied inverter system with master-slave current-sharing control. Firstly, the master-slave current-sharing control scheme is introduced. Then, the influence of communication delay and zero-order-hold on the system is analyzed. And design criteria to reduce the influence of low-bandwidth communication (LBCom) is studied and determined. New approaches, by designing current reference low-pass-filter and voltage feed-forward loop in slave modules, are introduced. Performance of proposed control structure and design criteria are experimentally verified. With the proposed method, LBCom tools can be applied to systems with master-slave control architecture, while keeping the robustness and transient performance, with improved modularity and operation flexibility.

## 4.2 Introduction

More and more distributed dc systems, like solar farms and dc microgrids, are connecting to the utility grid as an important way to harvest renewable energy and will keep playing an important role in the future smart grid. Voltage source inverter (VSI) is critical to interface these distributed dc systems with utility ac grid [4.2]. With the growing demands of dc systems, the needs of VSI with larger capacity and higher flexibility have become significant. In most of dc applications, a large-capacity centralized interfacing inverter is commonly used as interface between dc bus and utility grid [4.3]. Besides regulating the output current to be sinusoidal and synchronized to the

grid voltage, the interfacing inverter is also responsible of keeping dc bus voltage stable towards variation of solar power output. The single-operated centralized inverter has many restrictions in terms of flexibility, reliability and scalability, and will face the problem of light load operating and higher loss due to using of high current power semiconductors or bulky passive components, especially for systems with fluctuating power flow [4.4]. Using close-range parallel-operated inverters to replace a central inverter, as shown in Figure 4-1, can reduce the stress of high current by distributing power into multiple modules. Thus parallel-operated inverters take more advantages in some cases that the power can be shared with multiple VSI modules with improved redundancy and flexibility [4.5]-[4.8]. Such parallel module design has been adopted by many commercial products in PV [4.9] and UPS applications [4.10].

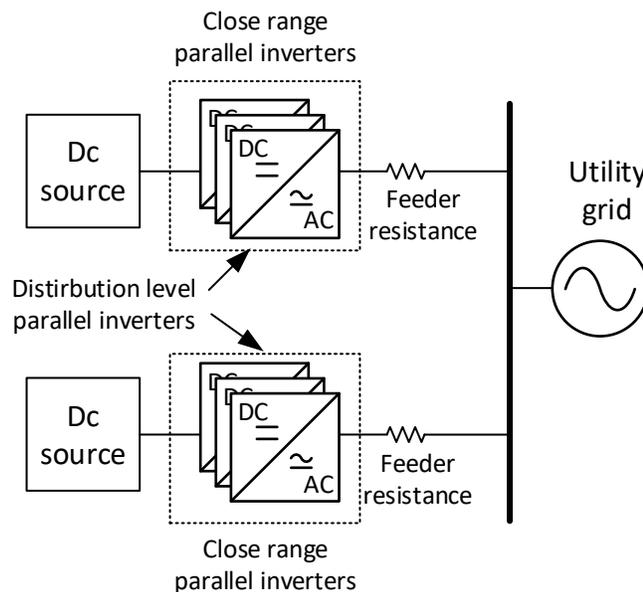


Figure 4-1. Application of close-range parallel inverter system.

To achieve power sharing among parallel-operated converters, droop characteristic-based control and active load sharing control technologies are commonly used [4.11]. While droop control taking advantages of easy implementation and high modularity [4.12]-[4.14], active load

sharing control has better performance in terms of voltage regulation and power sharing, but requires communication among paralleled modules to share information of current reference or current-sharing error [4.15]-[4.17]. Master-slave architecture is one of commonly used architectures, which has respective current loop controller in each slave module and a common voltage controller in master module. Equal current sharing and precise voltage regulation can be achieved simultaneously. This paper is mainly focusing on master-slave control for modular design where compatibility issue is not considered. With master-slave architecture that current reference of each module is given by the master, many smart features can be enabled, e.g. dynamic power sharing [4.6]. With master selection techniques like automatic master [4.18] and democratic master [4.19], plug-n-play and high reliability can also be achieved on master-slave-controlled system. A disadvantage of communication-based control is that it requires interconnection of control signals that relies on high-bandwidth and precise communication, which can be costly (for communication devices, cable and hubs) and the wiring will reduce modularity and may introduce significant noises into control signals. Thus, the master-slave control is commonly be applied only in a close range [4.7].

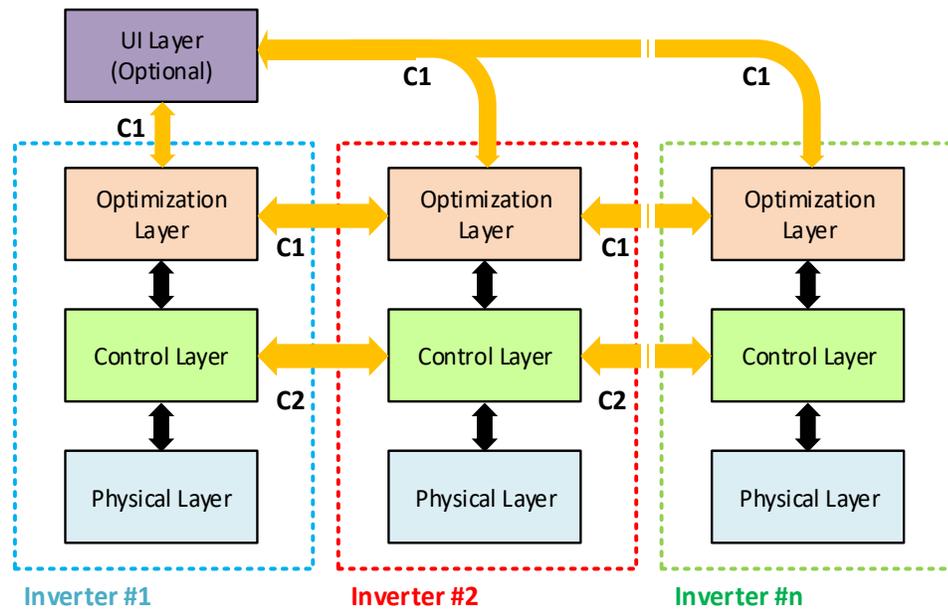
With development of communication technology, new communication tools are available on the market, e.g. Power Line Communication (PLC) module, Bluetooth module and Zigbee communication module. These tools have been widely used in Internet of Things (IOT) and smart grid applications, due to their features of no extra wires, low cost, operation flexibility and distributed intelligence. At the same time, these digital communication modules are equipped with built-in checking rules which are reliable even in a high EMI environment. Furthermore, a single digital communication channel can be multiplexed to transmit several different signals, e.g. amplitude, phase or control commands. It is a trend to use such modular communication devices

in the future smart grid [4.20][4.21]. Combining master-slave controlled parallel inverter system with these new communication technologies can omit the physical wire connection and provide a reliable communication channel resistive to environmental noise. The ad-hoc communication network also enables plug-n-play feature of converter modules. However, as a tradeoff of low-cost, these new communication tools are featured as low-bandwidth and low-rate, which limits the usage of these advanced communication tools mainly in high level coordination, e.g. manual control and data collection, instead of in the control layer. Figure 4-2 (a) shows the common logic structure of a parallel inverter system [4.22]. Communication network C1 can be implemented with LBCom tools. However, the communication network of control layer C2 is usually based on high-bandwidth communication, e.g. analogue or fiber optic, even sometime using sensors to directly sense the output of another converter. Using two separate communication networks is neither convenient nor economic. Figure 4-2 (b) shows a case of proposed parallel inverter system combining two communication networks C1 and C2 into one LBCom network (using Zigbee modules), which can lead to higher modularity and lower cost.

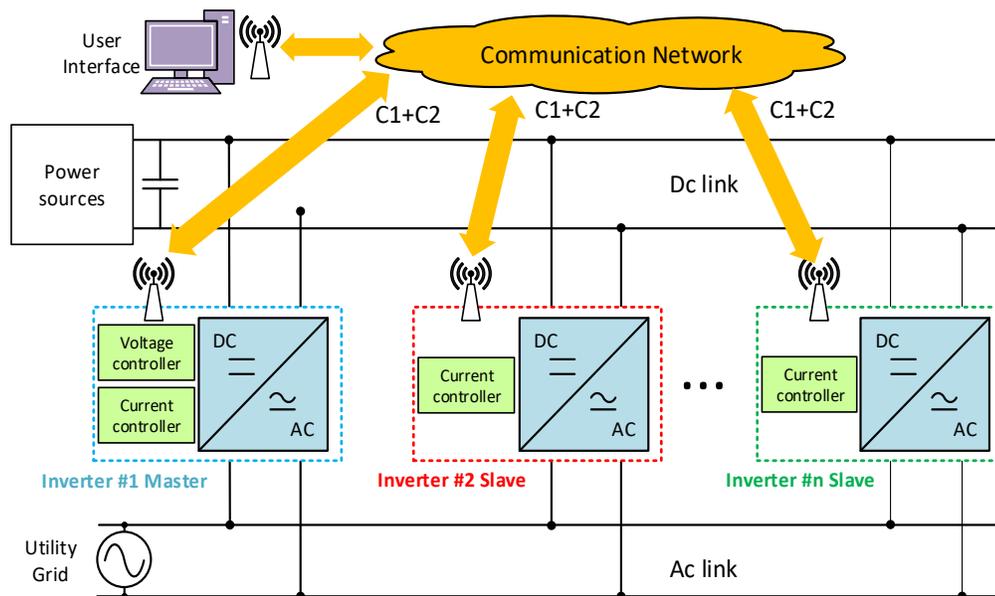
Apparently, the challenge is how to overcome the impact of LBCom delay. The communication delay  $\Delta t_1$  and zero-order-hold (ZOH) step  $\Delta t_2$  of LBCom are shown in Figure 4-3. Large delay and ZOH added in the control loop can result an oscillation even collapse of a master-slave controlled system. The stability issue caused by communication delay has been a topic of research in many areas [4.23]-[4.28]. In most of the researches, only pure delay is considered. However, ZOH  $\Delta t_2$  can be much larger than  $\Delta t_1$  as shown in Figure 4-3, which should also be taken into consideration in the stability analysis, especially when the communication channel is multiplexed for several signals. In this paper, a model considering both pure delay and ZOH is established and Nyquist diagram which can accurately reflecting effect of both time delay and

ZOH is used for stability analysis. Moreover, while previous studies mainly focusing on obtaining the delay bound, this paper provides new approaches to actively increase the system tolerable bound of communication delays.

The contribution of this paper is to propose a design method for master-slave current-sharing control of paralleled inverters to actively increase the tolerability to LBCom impacts. The proposed control scheme is to achieve the following features, 1) Cost-effective low-bandwidth communication device is adopted to transmit current reference from master module to slave modules, and system stability can stand with the impact of communication delay and ZOH, even when towards very high load dynamic changes. 2) Grid current can be evenly shared by inverter modules at steady state. At transient, the inverter modules can be decoupled to avoid oscillation and instability. 3) System is robust to varying communication delay and high EMI noises. In the paper, firstly, the master-slave current-sharing control is introduced. A transfer function model is established. Secondly, the influence of communication delay and ZOH on the parallel inverter system is analyzed. Methods to reduce the influence of LBCom are studied and compared. A slave module Low-Pass-Filter (LPF), which decouples slave modules from master module at transient, is proposed. And a slave module Feed-Forward Loop (FFL) controller that is similar to an adaptive voltage droop controller is introduced, which utilize local compensation to improve the transient performance, to provide system larger stable margin and release master's stress at transient. Performance of proposed control scheme and design criteria are demonstrated with simulation results and experimentally verified on two 800w/120V inverter modules.



(a)



(b)

Figure 4-2. (a) Typical logical structure of parallel inverter system with two separate communication networks C1 and C2. (b) Proposed master-slave controlled parallel inverter system with one LBCom network.

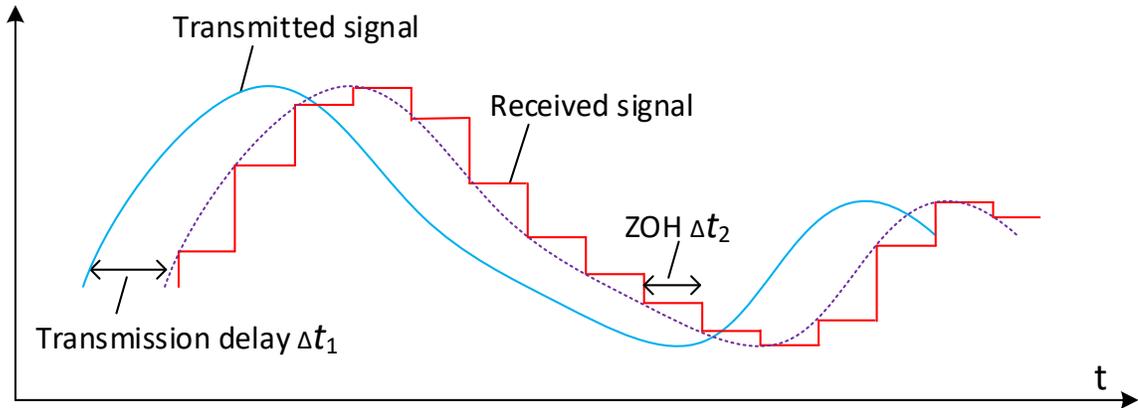


Figure 4-3. Delays of low-bandwidth digital communication.

### 4.3 Model of Master-Slave Controlled Inverters

A typical interfacing inverter system, such as solar farm or dc microgrid interfacing inverter commonly has two control targets, dc bus voltage and ac output current. The two control targets can be achieved by using a double-loop control structure that the outer loop regulates dc link voltage by generating current reference to the inner loop which controls output current [4.29]. In an input-parallel output-parallel inverter system (with first-order L filter), as shown in Figure 4-4, the inputs of inverters are connected to a common dc bus; outputs are gathered together and then get connected to a common grid feeder branch. For this parallel inverter system, a master-slave architecture can be applied to implement the double-loop control. The voltage controller is located in the master inverter module, usually is implemented by a PI controller with low control bandwidth. It monitors the error of dc link voltage and generate current amplitude reference accordingly to all inverter modules. All inverter modules have an independent Phase-Locked Loop (PLL) and current controller. Thus their output currents can be regulated sinusoidal and

synchronized to the grid voltage. The current controller is usually implemented by PI or hysteresis controller with fast dynamic response [4.2]. In this paper, simple stationary frame PI controller is used for inner current loop. The controller for each converter is independent (without any PWM synchronization), hence each module can work as a standalone device or in parallel with other devices.

In the master-slave architecture, output of voltage controller is given to all modules. Thus, at steady state, modules can equally share the power. The output of voltage controller, which is the current reference, is given to slave modules through a communication network with a significant delay and Zero-Order Hold (ZOH) when LBCom is used. At the same time, the current reference transmission inside the master module bypasses communication and has almost no delay. Hence the actual current references received by inverter modules are not synchronized. The unsynchronized current references will significantly affect the performance of voltage loop, for example, dc link voltage oscillation even collapse. The proposed control method could reduce the influence of LBCom, by redesigning slave module LPF and adding an FFL.

Considering the case that consists of one master module and one slave module, the control diagrams are shown in Figure 4-5, of which (a) is the ideal system neglecting communication delay effect; (b) shows the system considering communication impact; (c) shows the proposed system with voltage FFL in slave module. The blocks in blue dash box are processed in master module and the blocks in red dash box are processed in slave module.

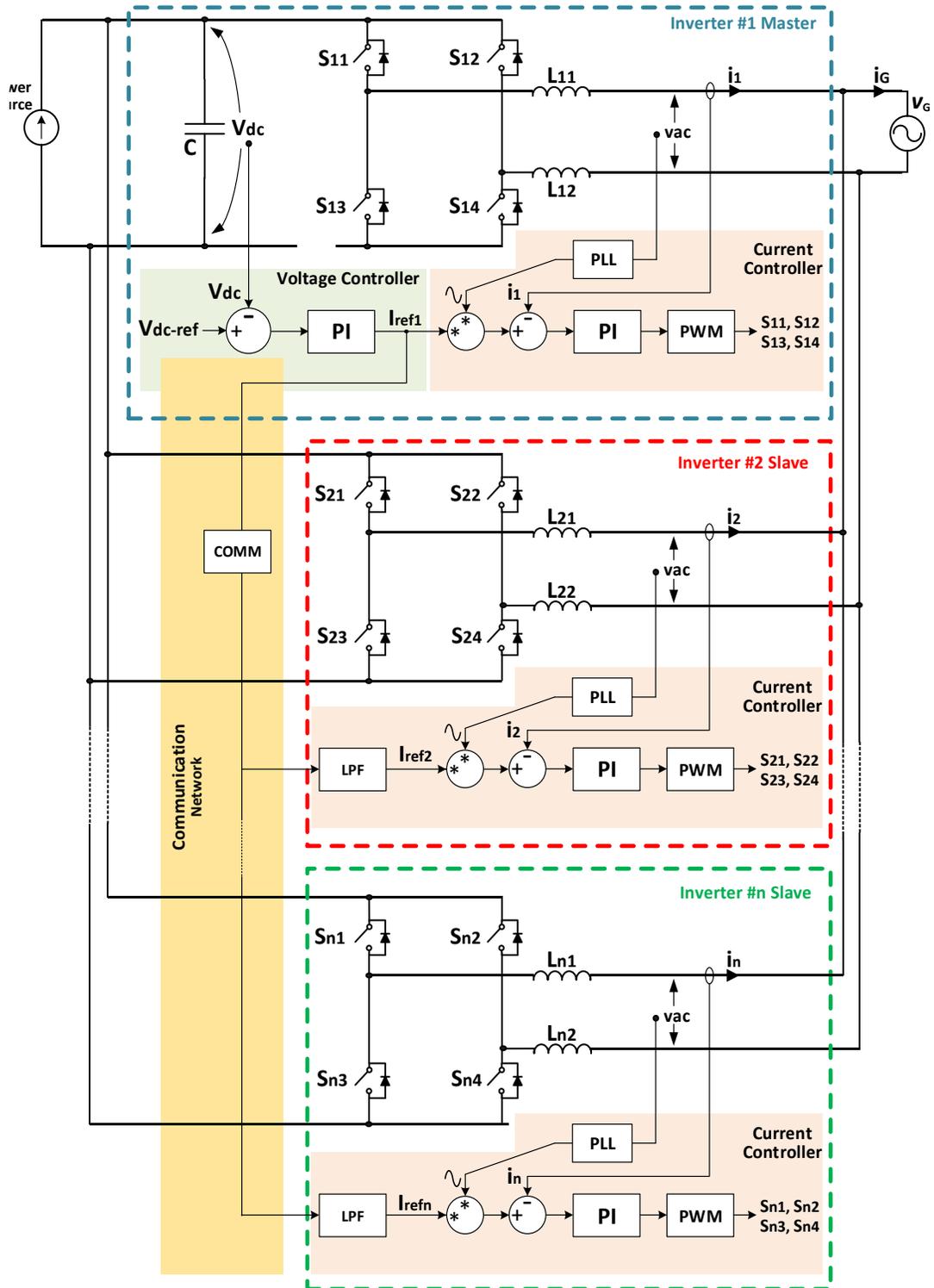


Figure 4-4. Overview of a typical input-parallel output-parallel inverter system with master-slave control architecture.

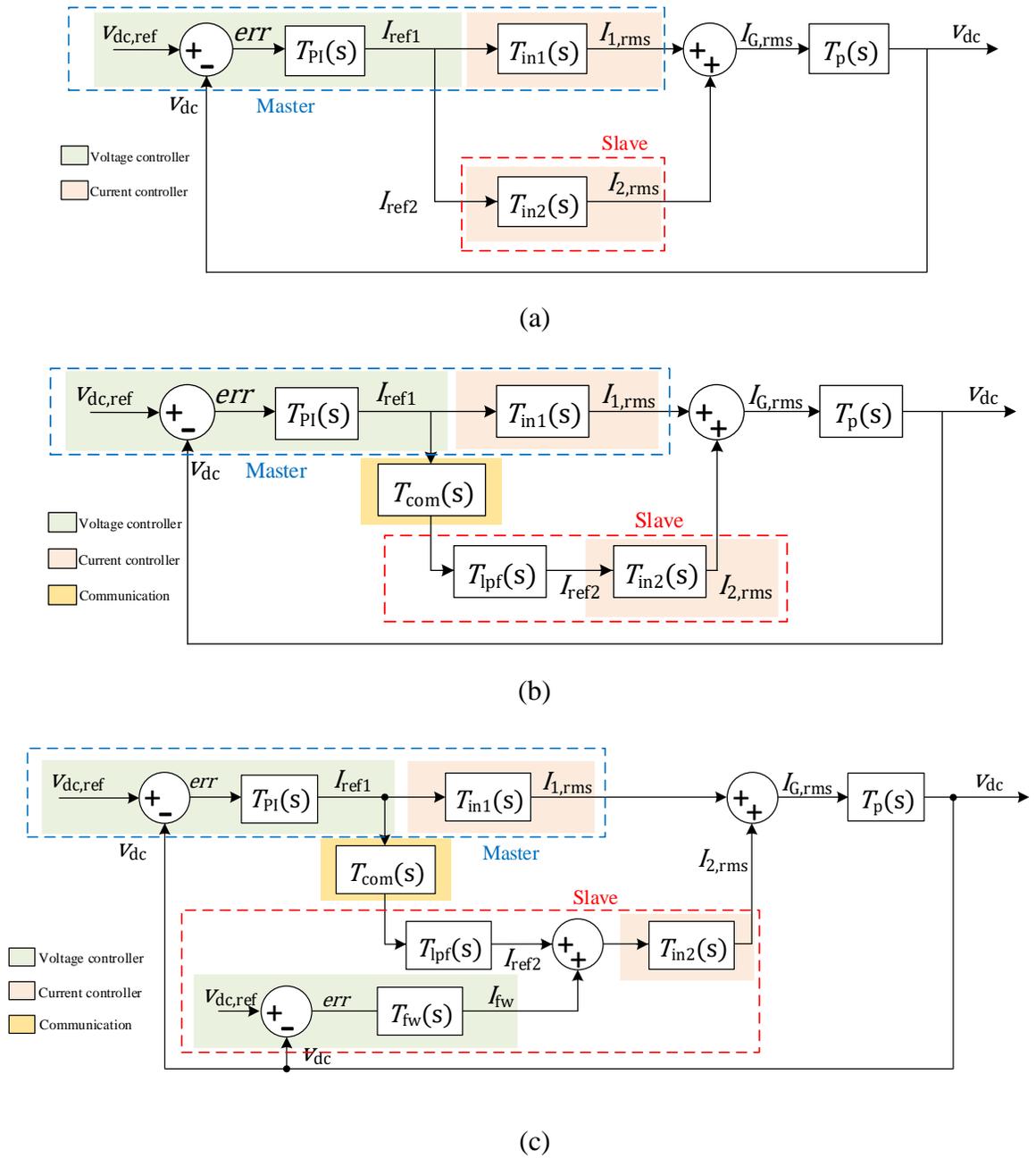


Figure 4-5. Control diagram of one master module and one slave module operating in parallel, (a) without communication impact, (b) with communication impact, (c) with voltage feed-forward loop in slave module.

The master voltage controller is usually implemented by a PI controller, which can be represented as (4-1), where  $k_p$  is proportional gain and  $k_i$  is integral gain. The design of  $k_p$  and  $k_i$  mainly takes consideration of making the voltage loop crossover frequency to be ten times smaller than the double-line frequency to avoid 2<sup>nd</sup>-order harmonic [4.30].

$$T_{PI}(s) = -\frac{k_p s + k_i}{s} \quad (4-1)$$

Due to the power stage transfer function as given in equation (4-3) having a negative sign, the voltage controller also needs to have a negative sign to make the system a negative feedback system.

$T_{in1}$  and  $T_{in2}$  are transfer functions of current loop of master and slave modules, respectively. The dynamic response of inner current loop is much faster than outer voltage loop, so the transfer functions of current loop can be considered as a constant value for study on the outer loop. To get the Root Mean Square (RMS) value of output current,

$$T_{in1}(s) = T_{in2}(s) = \frac{1}{\sqrt{2}} \quad (4-2)$$

The transfer function of power stage can be derived as (4-3),

$$T_p(s) = \frac{\widetilde{v}_{dc}}{\widetilde{i}_{G,rms}} = -\frac{V_{G,RMS}}{V_{dc}Cs} \quad (4-3)$$

where the parameters are indicated as in Figure 4-4.

The communication stage consists of a time delay and a ZOH is as given in (4-4), where  $\Delta t_1$  and  $\Delta t_2$  are defined in Figure 4-3.

$$T_{com}(s) = T_{delay}(s) \times T_{ZOH}(s) = e^{-\Delta t_1 s} \times \frac{1 - e^{-\Delta t_2 s}}{\Delta t_2 s} \quad (4-4)$$

A first order LPF is used for the LPF stage as shown in (4-5).  $t_{lpf}$  is filter time constant,

when  $t_{lpf} = 0$ , the LPF is bypassed.

$$T_{lpf}(s) = \frac{1}{t_{lpf}s+1} \quad (4-5)$$

The FFL can be considered as an I-V based voltage droop controller,

$$T_{fw}(s) = \frac{\widetilde{v}_{fw}(s)}{e\widetilde{r}r(s)} = -K \quad (4-6)$$

For an ideal system without considering communication effect as in Figure 4-5 (a), the overall open-loop transfer function of the system is,

$$T_{ol,i}(s) = T_{PI}T_p(T_{in1} + T_{in2}) = \frac{\sqrt{2}(V_{G,RMS}k_p s + V_{G,RMS}k_i)}{V_{dc}Cs^2} \quad (4-7)$$

For a system considering effect of LBCom as in Figure 4-5 (b), the overall open-loop transfer function is,

$$T_{ol}(s) = T_{PI}T_p(T_{in1} + T_{com}T_{lpf}T_{in2}) = \frac{V_{G,RMS}k_p s + V_{G,RMS}k_i}{\sqrt{2}V_{dc}Cs^2} \times \left( 1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s}}{t_{lpf}\Delta t_2 s^2 + \Delta t_2 s} \right) \quad (4-8)$$

For the system has both LPF and FFL as shown in Figure 4-5 (c), the overall open-loop transfer function is,

$$\begin{aligned} T_{ol}(s) &= T_p(T_{PI}T_{in1} + T_{PI}T_{com}T_{lpf}T_{in2} + T_{fw}T_{in2}) \\ &= \frac{V_{G,RMS}}{\sqrt{2}V_{dc}Cs} \left[ \frac{k_p s + k_i}{s} \times \left( 1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s}}{t_{lpf}\Delta t_2 s^2 + \Delta t_2 s} \right) - K \right] \end{aligned} \quad (4-9)$$

These derived transfer functions can be used to determine the stability of the systems.

## 4.4 Parameter Design to Reduce the Effect of LBCom

In this section, the stabilities of several cases of master-slave controlled parallel inverter systems are analyzed using Nyquist diagram. From (4-7) to (4-9), for all the systems, the number of poles on the right complex plane is zero. According to Nyquist stability criterion, the Nyquist contour should not include critical point  $(-1, j0)$  to guarantee stability.

### 4.4.1 Communication Effect on System Stability

For a typical system with parameters as shown in TABLE I, for an ideal system neglecting LBCom impact, based on (4-7), the system is apparently closed-loop stable.

However, for the system considering communication impact, as modeled in (4-8), while LPF is bypassed, the Nyquist diagram is shown in Figure 4-6. Due to the exponential terms from communication impact, Nyquist contour will rotate around origin. The contour has infinite intersection points with real axis. Therefore, only when all intersection points are on right side of critical point  $(-1, j0)$  can the system be closed-loop stable. In Figure 4-6, with large communication delay and ZOH, an intersection point moves to the left of  $(-1, j0)$ , thus the system becomes closed-loop unstable, due to the influence of communication. Thus, an originally stable system can become instable when communication effect is involved. It is important to properly design the control system to mitigate communication influence.

Figure 4-6 also shows the Nyquist contours with different communication delays and ZOH steps. It can be seen that, larger delay or ZOH step will make the left intersection point further to left, which will lead the system less likely become stable.

TABLE 4-I VALUE OF THE SYSTEM CONDITIONS USED IN THE DESIGN

Parameters	Value	Parameters	Value
$V_{dc,ref}$	300 V	$\Delta t_1$	15 ms
$C$	1.5 mF	$\Delta t_2$	34 ms
$V_{G,RMS}$	120 V	$k_p$	0.008
$P_{input}$	1.5 kW	$k_i$	1.25

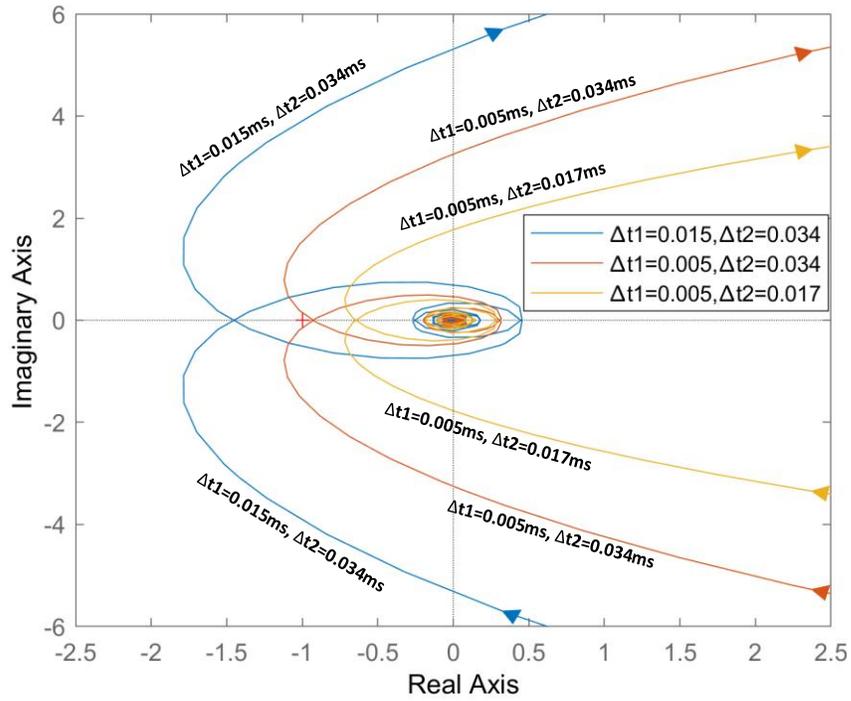


Figure 4-6. Nyquist diagrams of system open-loop transfer function with communication effect and no LPF.

#### 4.4.2 Voltage Loop Controller Design

System transfer function (4-8) can be rewritten as,

$$T_{ol}(s) = \alpha \times \left(\frac{s+\beta}{s^2}\right) \times \left(1 + \frac{e^{-\Delta t_1 s} - e^{-(\Delta t_1 + \Delta t_2)s}}{t_{lpf} \Delta t_2 s^2 + \Delta t_2 s}\right) \quad (4-10)$$

where

$$\alpha = \frac{V_{G,RMS} k_p}{\sqrt{2} V_{dc} C} \quad (4-11)$$

and

$$\beta = \frac{k_i}{k_p} \quad (4-12)$$

While communication delay  $\Delta t_1$  and ZOH step  $\Delta t_2$  are predetermined values, which are considered fixed. Thus, according to (4-10), the parameters can be designed are  $\alpha$ ,  $\beta$  and  $t_{lpf}$ .  $\alpha$ ,  $\beta$  are related to PI parameters and  $t_{lpf}$  is LPF time constant. Parameter  $\alpha$  represents system open-loop gain. By reducing  $\alpha$ , the whole Nyquist contour will scale down to the origin, which means all intersection points on real axis will move closer to the origin. When  $\alpha$  is small enough that all intersection points are on right side of critical point  $(-1, j0)$ , the system becomes stable.

Figure 4-7 shows the Nyquist diagram with different gain  $\alpha$ . The original system described by TABLE I, of which the open loop gain  $\alpha = 1.5$ , is unstable as indicated by blue line in Figure 4-7. When the loop gain decreases, the system becomes more stable. When  $\alpha = 1.0$ , the system is close to the critical stable point. And when  $\alpha$  further decreased to 0.5, the system becomes stable. Hence, by reducing system open-loop gain, the system can be stable even delay and ZOH are involved. However, the reduction of open-loop gain will weaken overall system's ability of transient response.

In (4-10),  $V_{G,RMS}$  and  $V_{dc}$  are fixed, and  $C$  is commonly designed to meet the requirement of dc link voltage ripple. While  $\beta$  is kept as a constant,  $\alpha$  can be changed by simultaneously scaling

down  $k_p$  and  $k_i$ , or changing the sensor gain if sensor gain is considered.

Besides reducing open-loop gain  $\alpha$ , reducing  $\beta$  by keeping  $k_p$  the same and reducing  $k_i$  could also slow down the system response to avoid oscillation between parallel-operated inverters, as shown in Figure 4-8. Reducing  $\beta$  has very similar effect as reducing  $\alpha$ , which will also reduce controller's bandwidth. Hence, in the following paper, we mainly use  $\alpha$  as indicator of bandwidth of voltage controller, while  $\beta$  being kept constant.

Thus, by properly designing voltage controller, system can be kept stable towards communication effects. It requires to reduce control bandwidth of voltage controller to avoid potential oscillation among parallel-operated inverters, which will sacrifice dynamic performance of voltage regulation e.g. settling time and overshoot.

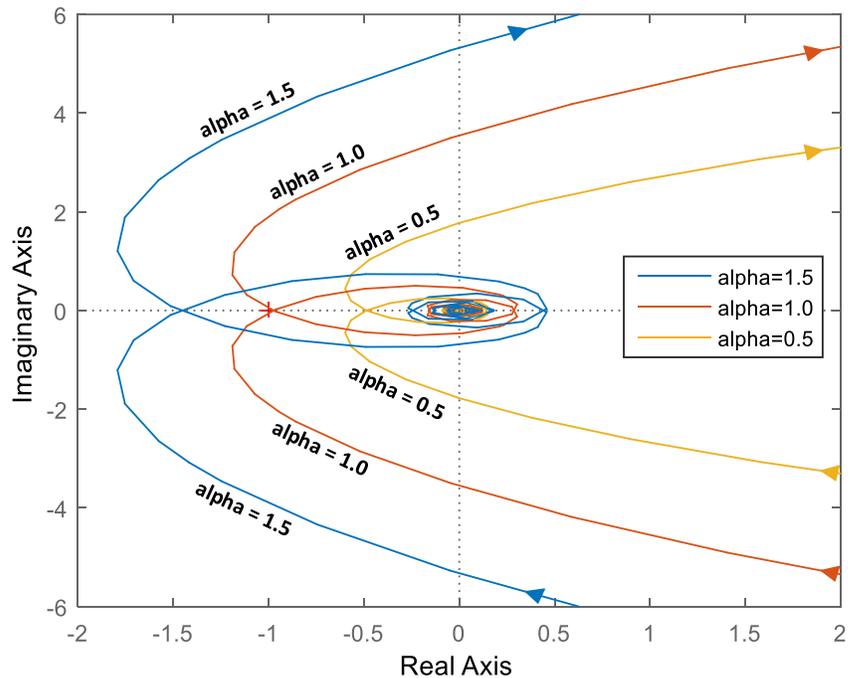


Figure 4-7. Nyquist diagram of system open-loop transfer function with communication effect with different  $\alpha$ .

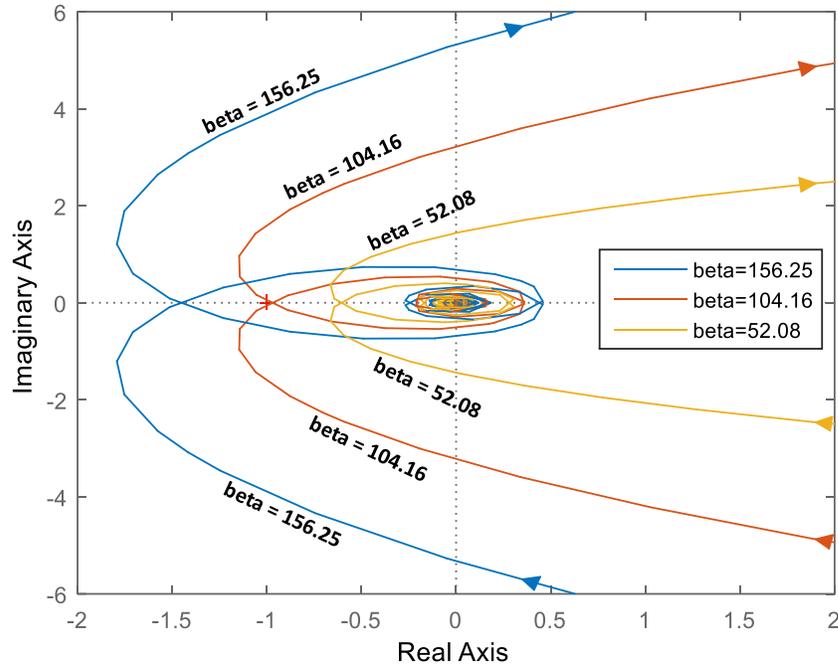


Figure 4-8. Nyquist diagram of system open-loop transfer function with communication effect with different  $\beta$ .

#### 4.4.3 Low-Pass Filter Design

Modifying  $\alpha$  and  $\beta$  which are basically modifying parameters of voltage controller, will influence the performance of overall voltage loop. Thus, mitigating communication impact by only designing  $\alpha$  and  $\beta$  will inevitably slow down the voltage regulation performance. One of proposed solutions is to modify slave module controllers. As shown in the control block diagram Figure 4-5 (b), an LPF is added to each slave module. In the proposed method, the master module can keep the same control performance as a single-operated inverter and slave modules should have lower control bandwidth towards voltage change thus the modules are decoupled and the oscillation can be avoided.

The current reference received by slave modules are piecewise-constant signals due to ZOH.

The slave module controller is commonly equipped with an LPF with relatively high cut-off frequency to smooth the received current reference signal. By simply redesigning the LPF to reduce the cut-off frequency, impact of wireless digital communication can be mitigated.

The received current reference signal at slave module go through the LPF firstly, then be taken by current controller. When the LPF is properly designed, slave modules can only get the low frequency signal in the current reference, which is enough for the modules to achieve power sharing purpose at steady state. At the same time, the relatively high frequency signals, which could cause oscillation or instability, are filtered. Thus, master module and slave modules contribute to dc link voltage in different bandwidths. In the proposed structure, power exchanges during transient, which requires high control bandwidth, will be mainly taken care by the master module. Power exchanges at steady state will be shared among all slave modules and master module.

Therefore, with proposed structure, for voltage regulation, the master module keeps the same ability of transient response as a single-operated inverter. At steady state, power will be evenly shared among all modules. By properly designing LPF, communication impact can be mitigated while keeping voltage regulation with a relatively fast-dynamic response.

As shown in (4-5), a simple first-order LPF is used in the study. To smoothing piecewise-constant signal, an LPF with relatively high cut-off frequency is adequate. For example, when the ZOH sample interval  $\Delta t_2 = 0.034\text{ms}$ , a  $t_{\text{lpf}} = 0.05\text{s}$  is enough to smooth the piecewise-constant signal. However, to mitigating communication impact, a lower LPF cut-off frequency is required.

Figure 4-9 shows the Nyquist diagram of system open-loop transfer function (4-8) with different LPF time constants  $t_{\text{lpf}}$ . While increasing  $t_{\text{lpf}}$ , which means lowering the LPF crossover frequency, Nyquist diagram intersections with real axis get closer to the origin. When  $t_{\text{lpf}} = 0.1\text{s}$ ,

the system is near to the critical point of being stable. When  $t_{lpf} = 0.5s$ , the system is stable with margin.

According to Figure 4-9, an LPF with larger time constant  $t_{lpf}$  in slave module makes the system more stable and robust. A  $t_{lpf}$  tending to infinity means the slave modules will keep a constant current output as their initial settings which are independent from voltage controller. At this point, only master module is involved in voltage control. Thus, the system is as stable and robust as a single operated inverter. However, this has distorted the current sharing purpose of parallel operation. An LPF with cut-off frequency that 5-10 times smaller than the voltage loop natural frequency  $\omega_n$  is rational.

Furthermore, with LPF in slave module, there is more space for PI controller design. As shown in Figure 4-7, when LPF is missing, system can only be stable when open-loop gain  $\alpha$  is less than 1.0. In Figure 4-10, with LPF  $t_{lpf} = 0.5s$ , the system becomes stable even for  $\alpha = 3.0$ , with enough gain margin. Increased open-loop gain with slave module LPF can provide a better transient performance while keeping the system stable.

Assuming  $\beta$  and  $\Delta t_2$  are fixed, a bound of system operating in stable region, which is decided by loop gain  $\alpha$ , LPF time constant  $t_{lpf}$ , and communication delay time  $\Delta t_1$ , can be obtained. The surface in Figure 4-11 shows the bound. The region above the surface indicates system being unstable. The region below the surface indicates system being stable. It can be seen that, when LPF is absent or the time constant is too small, the system can only tolerate a very short communication delay, at a prerequisite of low loop gain. When LPF is added, the system can tolerate longer communication delay even with a larger loop gain.

However, though the LPF can make systems with communication effect theoretically stable and has enough gain margin as shown in Figure 4-10, the phase margins which are  $\eta_1 = 31.3^\circ$  and

$\eta_2 = 9.2^\circ$  still cannot meet the engineering requirement which is  $40^\circ \sim 50^\circ$  [4.31]. Furthermore, as LPF is introduced to slave modules, the master could provide much more power than the slave modules at transient. While the power that master module can provide is limited, considering this current saturation characteristic, at transient the system may have a large voltage sag or swell even a stability issue.

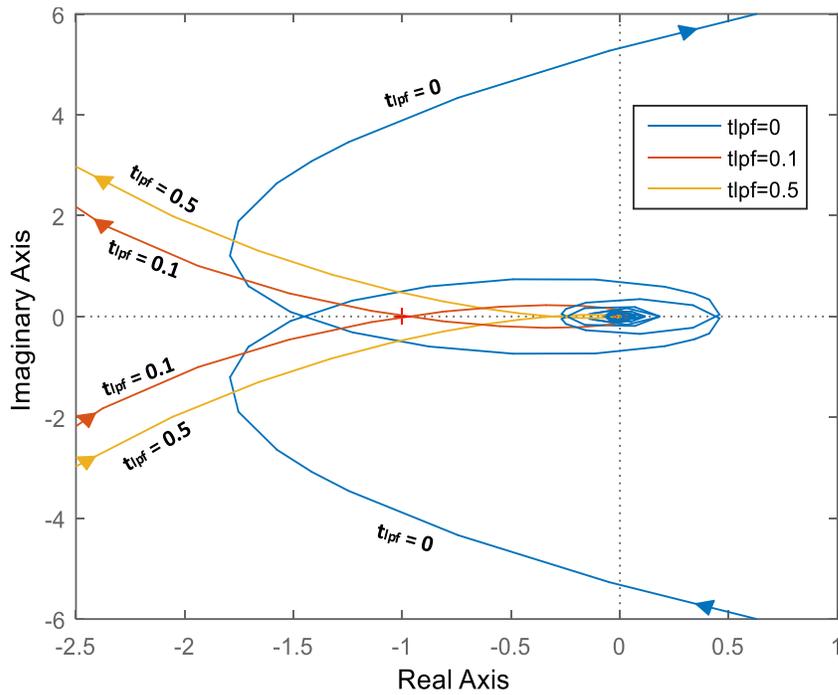


Figure 4-9. Nyquist diagram of system open-loop transfer function with communication effect with different  $t_{lpf}$  in slave module.

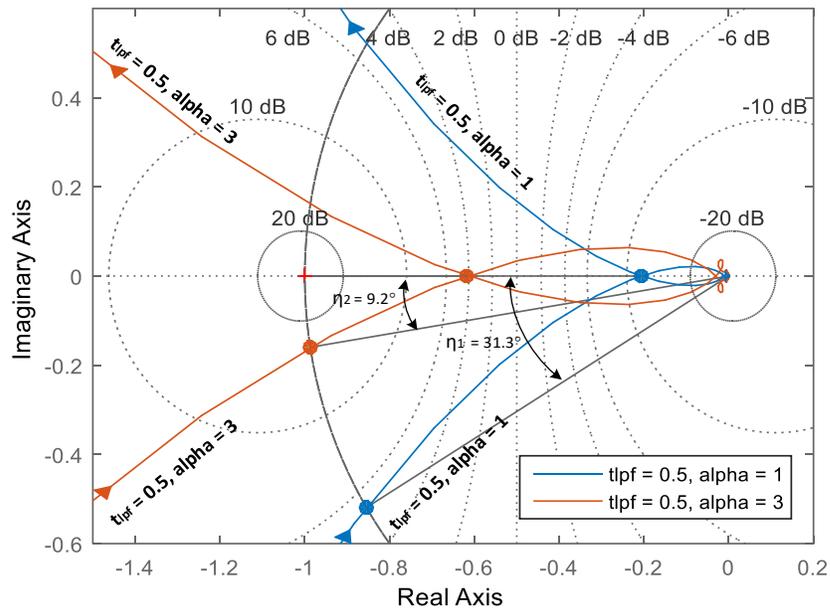


Figure 4-10. Nyquist diagram of system open-loop transfer function with delay effect with different  $\alpha$  when LPF in slave module is functioning.

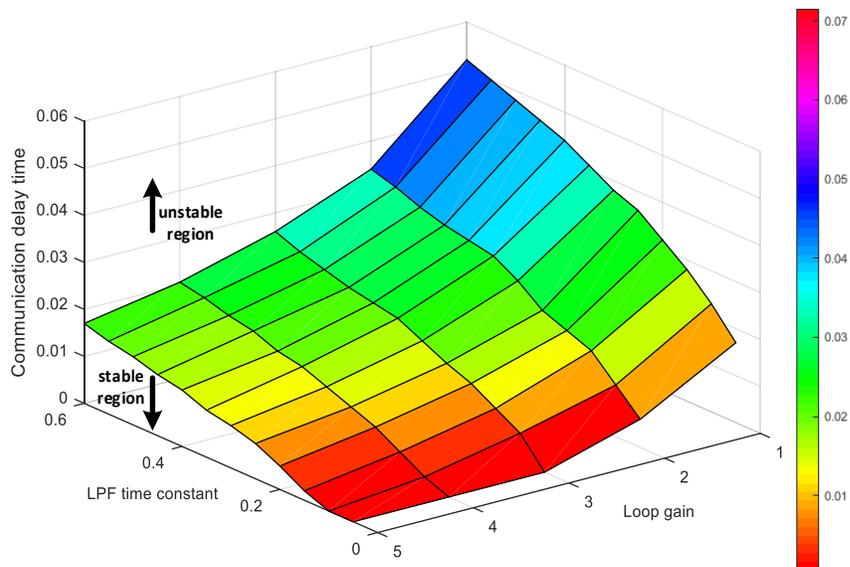


Figure 4-11. Bound for the system operating in stable region,  $\beta$  is fixed to 156.25,  $\Delta t_2$  is fixed to 0.034s.

#### 4.4.4 Feed-Forward Loop Design

As mentioned above, by solely adding LPF in slave modules, the phase margin of system is insufficient, and a high-rating master module may be required. Like neighboring information is used to compensate steady state error in droop-controlled system, local compensation can be used to improve transient performance in master-slave-controlled system. A voltage feed-forward controller is added to each slave module.

Figure 4-5 (c) shows the control diagram that feed-forward loop is added to slave module. To obtain the characteristic that has high feed-forward gain at large voltage error but low gain at small voltage error, any power function can be used for the feed-forward controller. Here the feed-forward controller is selected as a cube function with a gain  $-K_{fw}$ ,

$$I_{fw}(t) = -K_{fw}err(t)^3 \quad (4-13)$$

The linearized transfer function of the feed-forward controller, as an update of (6), is,

$$T_{fw}(s) = -K = -3K_{fw}ERR^2 \quad (4-14)$$

It can be seen from (4-13) and (4-14), at steady state,  $ERR = 0$ , feed-forward loop has no effect to the system, which means the slave module will follow the same current reference as master module. At large transient, the slave module will contribute to compensate dc link voltage error at a high gain due to the square term of  $ERR$ , which could significantly reduce the stress of master module at transient. The controller is actually an adaptive feed-forward voltage droop controller, of which the gain  $K$  is self-adjusted according to  $ERR$  value.

Figure 4-12 shows Nyquist diagrams based on (4-9) with different feed-forward parameters. It can be seen with feed-forward loop, both phase margin and gain margin of system can be increased. And Figure 4-13 shows the delay bound while FFL is involved. Compared to Figure

4-11, with both LPF and FFL in slave module, the tolerable delay time is increased significantly, especially when loop gain is high. Thus, with properly designed LPF and FFL, the system can be tolerable with large time delays while keeping a large stable margin and high loop gain. With a large tolerable margin of communication delay, even the delay varies, the system can still be kept in the stable region and a high loop gain can provide a better transient performance.

In Figure 4-12, the phase margin increases along with increasing FFL gain. However, if the gain is over designed, the robustness of system will be reduced, and the steady state performance may be influenced. Especially, due to the steady state double line frequency ripple on dc link, a large 2<sup>nd</sup>-order harmonic can be generated if FFL is overdesigned.

To avoid FFL affecting steady state performance, the parameter selection should consider the steady state double line frequency ripple on dc link [4.30], which is expressed as,

$$\Delta V_{dc} = \frac{P}{4\pi f C V_{dc}} \quad (4-15)$$

Where  $P$  is total output power of the parallel-operated system,  $f$  is line frequency which is 60Hz in the studied system.

Assume at steady state the magnitude of 2<sup>nd</sup>-order harmonic of output current should be less than  $I_{2nd}$ ,

$$K_{fw} \Delta V_{dc}^3 < I_{2nd} \quad (4-16)$$

Combine (4-16) and (4-17),

$$K_{fw} < \frac{64\pi^3 f^3 C^3 V_{dc}^3 I_{2nd}}{P^3} \quad (4-17)$$

Thus,  $K_{fw}$  should be designed satisfying (4-17) to fulfill requirement of 2<sup>nd</sup>-order harmonic.

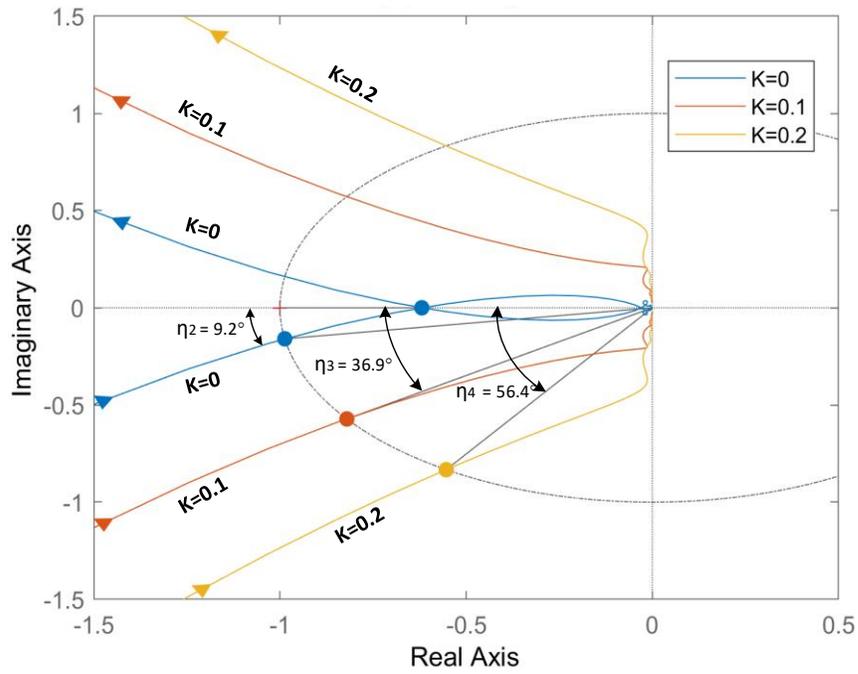


Figure 4-12. Nyquist diagram of system open-loop transfer function with both LPF and FFL in slave module, while  $t_{lpf} = 0.5$  s and  $\alpha = 3$ .

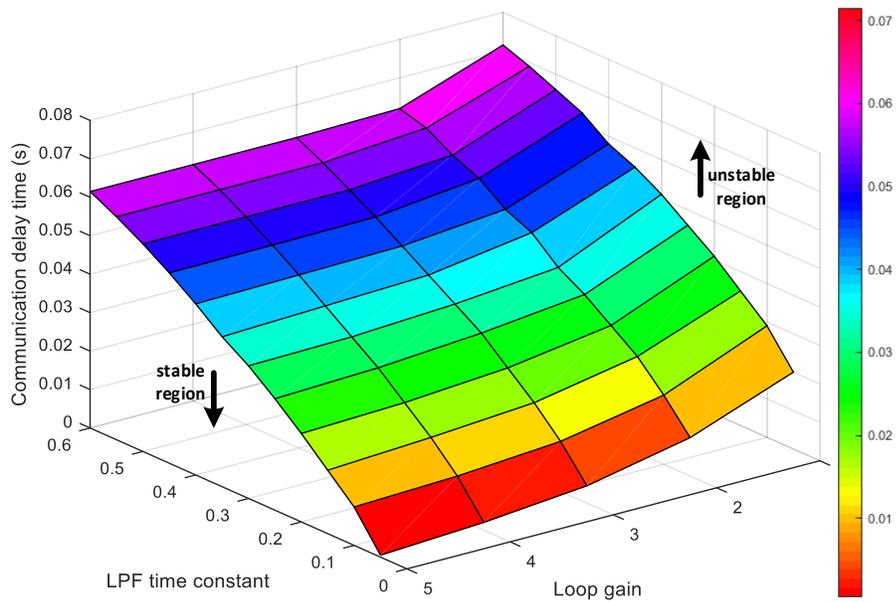


Figure 4-13. Bound for the system stable region while FFL is involved,  $\beta$  is fixed to 156.25,  $\Delta t_2$  is fixed to 0.034s and  $K$  is fixed to 0.0005.

#### 4.4.5 Master Outage

In conventional master-slave control, loss of master will cause failure of whole system. With proposed slave controller, the system can still run when the master converter is down. The FFL in slave module can still form a closed voltage control loop, which is similar to an I-V droop controller, with basic power sharing and voltage regulation performance.

Furthermore, the proposed controller can also be applied to a multi-master system. All modules can be equipped with both master and slave controller, as shown in Figure 4-13. Each module can be switched between master mode control and slave mode control. With proper master-selecting mechanism [4.18]-[4.19], one master will be active, and when the master module is down, one slave module will shift to master mode to send current reference to other modules.

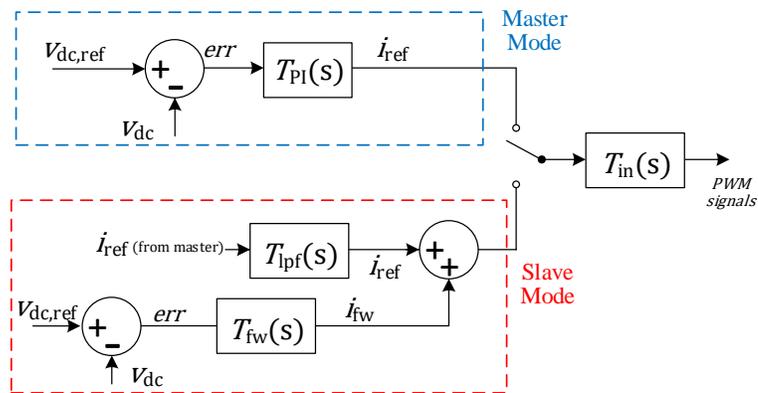


Figure 4-14. Controller diagram with multi-master control ability.

## 4.5 Simulation and Experiment Verifications

### 4.5.1 Simulation Verification

The proposed scheme is simulated using PLECS. Two full-bridge VSI modules with unipolar-PWM are used in verification [4.32]. Simulation parameters are provided in TABLE 4-I, Table 4-II.

Figure 4-15 (a) shows the simulation results of parallel inverter system with conventional master-slave control, of which the control diagram is shown in Figure 4-5 (b). While communication impact being involved, when  $\alpha = 1$ , the system is close to the critical stable point, according to Nyquist diagram in Figure 4-7. Simulation waveforms in Figure 4-15 (a) show a good agreement to it, that dc link voltage and two current references for the two modules are badly oscillating.

For simulation in Figure 4-15 (b) and (c), slave module LPF with  $t_{\text{lpf}} = 0.5$  s is added. The oscillating system in Figure 4-15 (a) become stable even with increased loop gain  $\alpha = 3$ , which approves Nyquist diagram in Figure 4-10.

Figure 4-15 (d) shows simulation results that slave module is equipped with both LPF and FFL. With properly designed FFL, at transient, though both module's outputs still have an overshoot, the oscillation is damped quickly and the power distribution among the modules are better balanced. The dc link voltage transient performance is also improved significantly.

Figure 4-16 (a) and (b) shows simulation results of two parallel-operated inverters using V-I and I-V droop control respectively [4.14]. Secondary voltage regulation based on LBCom is adopted in the simulation, hence for both case, the dc link voltage has no steady state error. For V-I droop control, as shown in Figure 4-16 (a), the settling time is longer and overshoot is larger

towards transient, compared to proposed master-slave control. For I-V droop control, as shown in Figure 4-16 (b), the voltage regulation is very fast. However, the output current is badly distorted by second-order harmonics, which does not occur in V-I droop control or master-slave control. And for both V-I and I-V droop control, the power sharing become unbalanced when a voltage sensing error exists (in this case, 1% voltage sensing error results a 3A current-sharing error). Master-slave control, having only one voltage controller in master module, will not have this current-sharing issue caused by voltage sensing error.

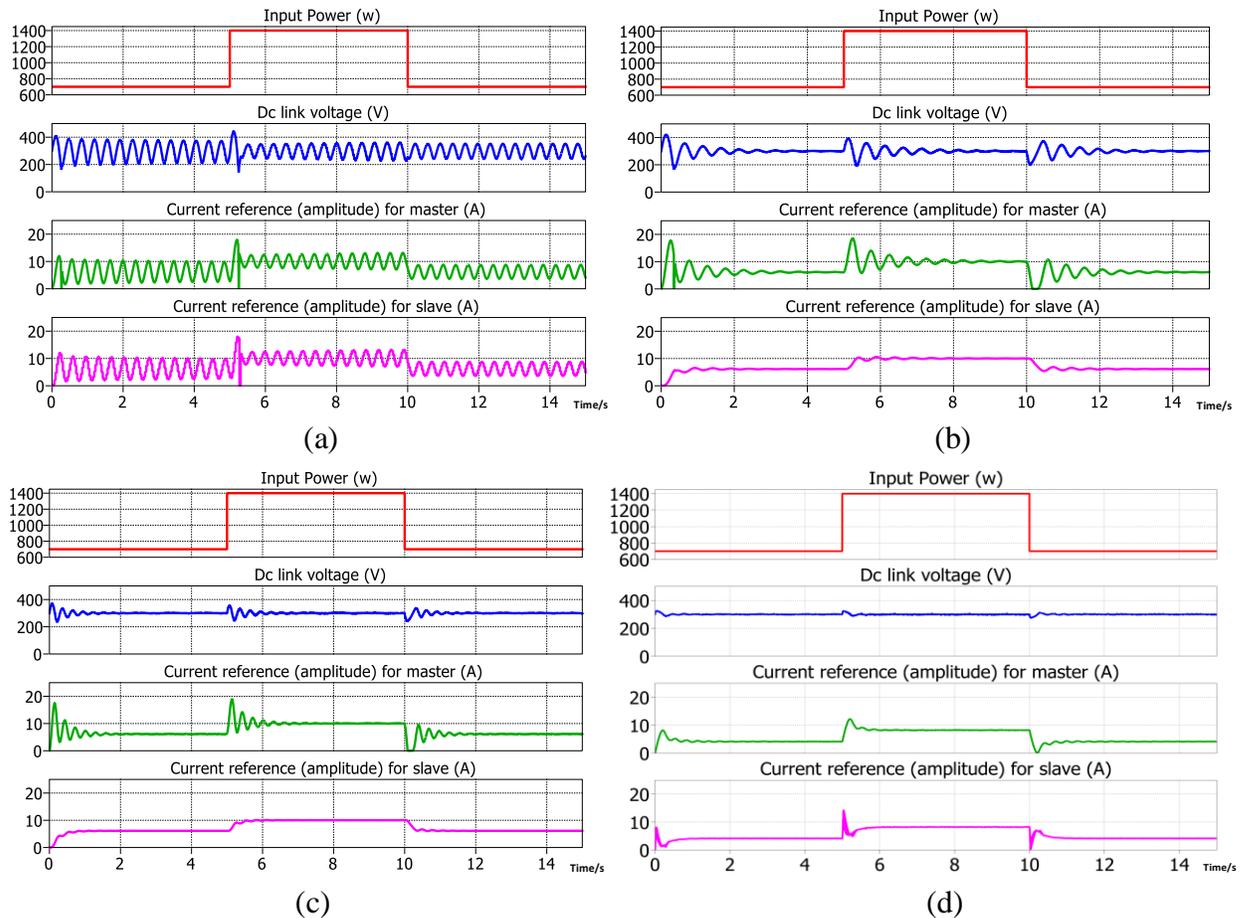


Figure 4-15. Simulation results of two inverters operating in parallel with time delay  $\Delta t_1 = 15$  ms,  $\Delta t_2 = 34$  ms, (a) conventional master-slave control with no LPF and FFL in slave module and  $\alpha = 1$ , (b) modified master-slave control with LPF and no FFL in slave module,  $\alpha = 1$ ,  $t_{lpf} = 0.5$  s, (c) modified master-slave control with LPF and no FFL in slave module,  $\alpha = 3$ ,  $t_{lpf} = 0.5$  s, (d) modified master-slave control with both LPF and FFL in slave module,  $\alpha = 1$ ,  $t_{lpf} = 0.5$  s,  $K_{fw} =$

$5e^{-4}$ .

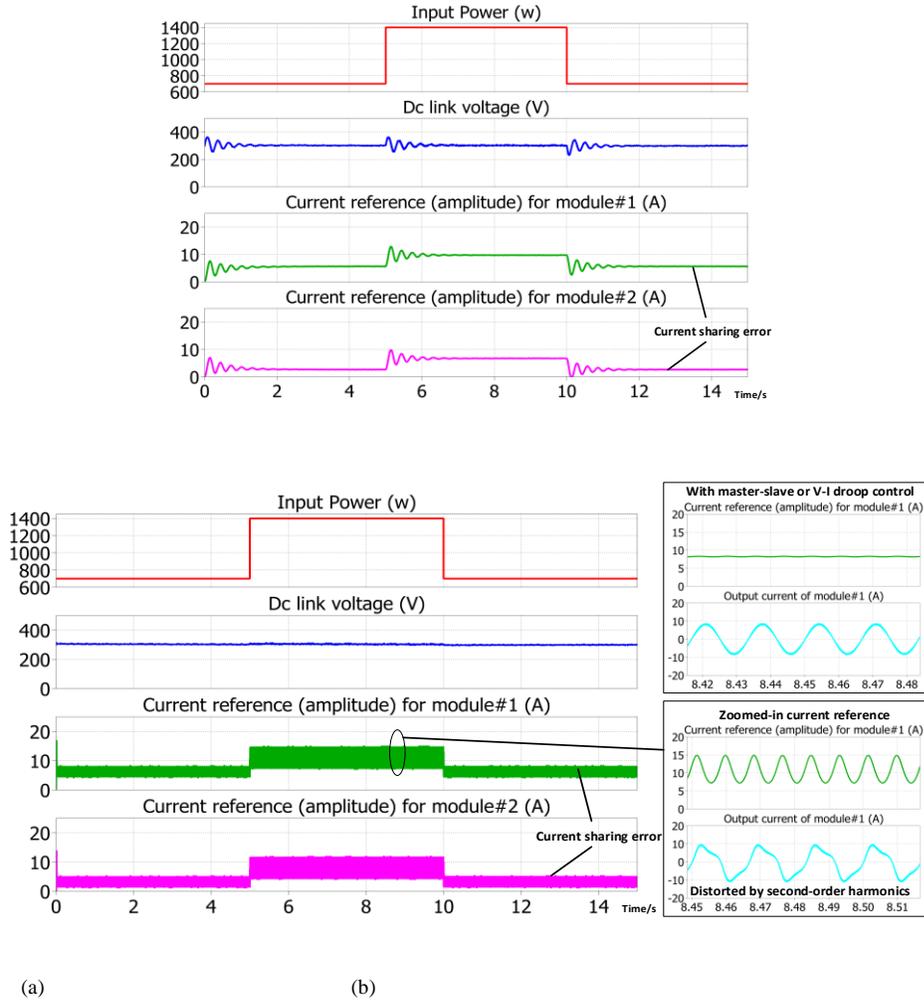


Figure 4-16. Simulation results of two inverters operating in parallel using droop control with secondary voltage regulation, both droop coefficients are set to 10 $\Omega$ , and 1% voltage sensing error is considered, (a) V-I droop control, (b) I-V droop control.

Table 4-II EXTRA SYSTEM PARAMETERS

Parameters	Value	Parameters	Value
$Baud\ rate$	9600 bps	$L_{11}, L_{12}, L_{21}, L_{22}$	2 mH
$P_{rate}$	800 W each	$f_{sw}$	20 kHz

## 4.5.2 Experimental Verification

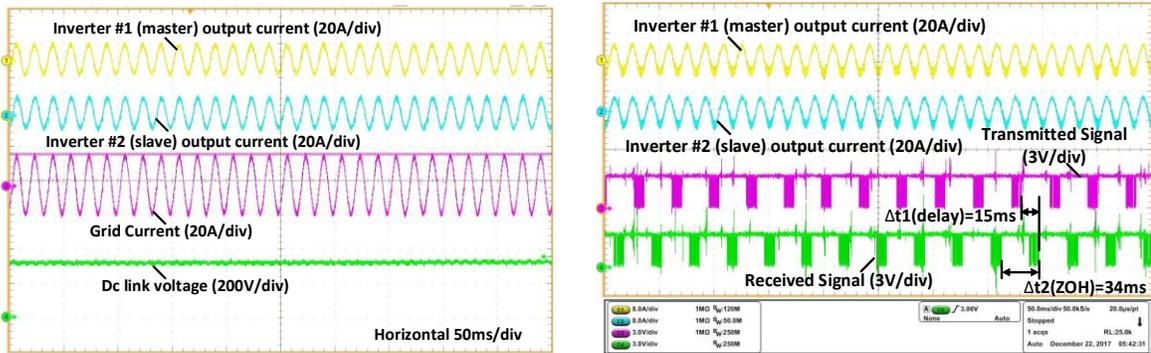
An experimental testbed has been implemented with two grid-connected full bridge inverter modules. Each inverter module is controlled by a TI F28377s DSP individually. Communication is based on DIGI Xbee 802.15.4 wireless communication module, which is based on Zigbee protocol, a wireless mesh network standard. Experiment specifications are as shown in Table I and II. Xbee modules are connected to DSPs using UART communication. The master module will periodically broadcast the current reference  $i_{\text{ref}}$  to all slave modules, of which the time interval will be the ZOH time interval. Checking mechanisms has been built into the communication protocol to guarantee the correctness of wireless digital communication, even in a high-EMI noise environment.

Figure 4-17 (a) shows the experimental waveforms of system steady state performance with proposed master-slave control design. It can be seen that, the dc link voltage is well following the reference voltage, 300 V, and grid current is stable and sinusoidal which is equally shared by two inverter modules. Figure 4-17 (b) shows the measured communication signals at steady state. Transmission delay  $\Delta t_1$  and ZOH  $\Delta t_2$  are shown in the figure. At the same time, the influence of EMI noise on the communication signals can be observed, which is inevitable in power electronic applications. With checking mechanism built in the LBCom modules, the communication is not interrupted. Figure 4-18 shows the transient performances of system when  $t_{\text{ipf}}$  is 0.5 and loop gain  $\alpha$  is 1.0. Figure 4-18 (a) and (b) shows the experimental results of input power step up and step-down changes respectively. Though the system is stable, the transient performance is poor. The overshoot is large and settling time is long. In Figure 4-19, while  $t_{\text{ipf}}$  is kept at 0.5, loop gain  $\alpha$  is increased to 3. It can be seen that the transient performance is improved with increased loop gain. The voltage overshoot and settling time both get smaller, but the voltage sag and swell at transient

are still large.

In Figure 4-20, both LPF and FFL are added in slave module with parameters  $t_{\text{lpf}} = 0.5$  s,  $\alpha = 3$ ,  $K_{fw} = 5e^{-4}$ . It can be seen that the transient performance is improved significantly with FFL involved. The voltage sag or swell at transient is reduced to less than 30V (10%). And the output power variation of master module is reduced.

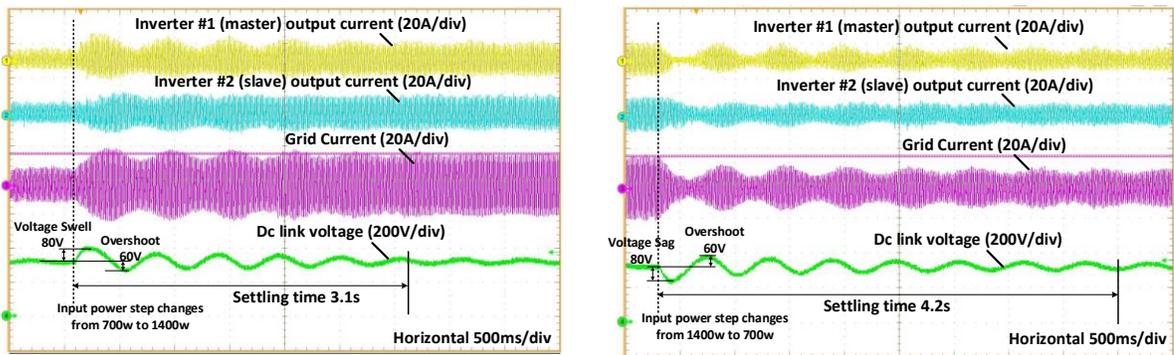
The experiment results verified the validity of master-slave control for parallel-operated inverters using LBCom with proposed design method. It also shows good agreement to the study of parameter selection, that with a proper current reference LPF and FFL in slave module, the system shows good tolerability to LBCom effect while keeping a good transient performance.



(a)

(b)

Figure 4-17. Experimental waveforms of steady state performance at 1400W total output power, (a) showing dc link voltage, (b) showing communication signals.



(a)

(b)

Figure 4-18. Experimental waveforms of transient with LPF in slave module, and  $t_{lpf} = 0.5 \text{ s}$ ,  $\alpha = 1$ , input power step changes (a) from 700W to 1400W, (b) from 1400W to 700W.

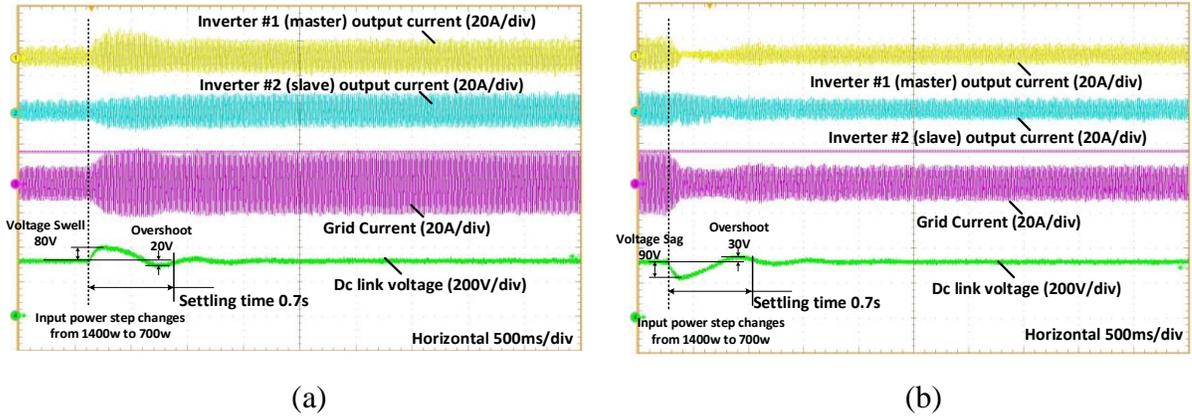


Figure 4-19 Experimental waveforms of transient with LPF in slave module, and  $t_{lpf} = 0.5$  s,  $\alpha = 3$ , input power step changes (a) from 700W to 1400W, (b) from 1400W to 700W.

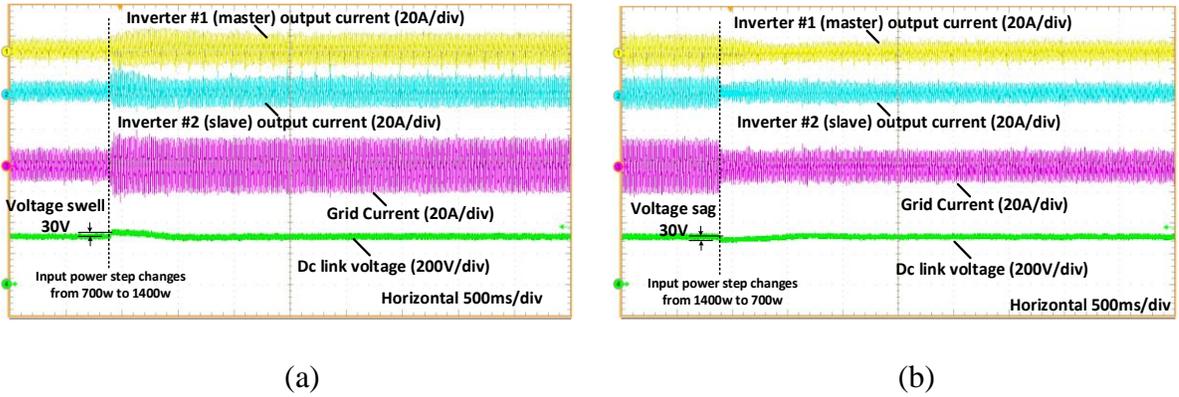


Figure 4-20 Experimental waveforms of transient with LPF and FFL in slave module, and  $t_{lpf} = 0.5$  s,  $\alpha = 3$ ,  $K_{fw} = 0.0005$ , input power step changes (a) from 700W to 1400W, (b) from 1400W to 700W.

## 4.6 Conclusion

The chapter proposed a robust master-slave control scheme for parallel-operated interfacing inverters, which is tolerable to Low-Bandwidth Communication (LBCoM) effects. The effect of communication delay and zero-order-hold (ZOH) on the system is studied. New approaches that design current reference low-pass-filter (LPF) and add voltage feed-forward loop (FFL) to slave

modules are proposed, which can compensate the impact of LBCom to achieve a stable and robust operation while keeping a good transient performance.

Experiment results show good agreements to the analytical study. Conclusions are as following,

1) low-bandwidth low-rate communication tools can be used in master-slave current-sharing control of parallel-operated inverters, with proper controller design.

2) By only adjusting voltage loop controller parameters, system can be stable towards impact of time delay and ZOH, but at a sacrifice of loop gain, which may lead to a bad transient performance. And the margin of tolerable delay time is narrow.

3) By designing current reference LPF to slave modules. The effect of LBCom can be mitigated while having an improved transient performance. However, the phase margin is not enough, and it may require higher rating for master module.

4) By having both LPF and FFL in slave modules. The parallel-operated inverter system with LBCom can have enough phase and gain margins to guarantee a stable and robust operation. At the same time, FFL gives slave modules faster transient response. Balanced power distribution among the modules can be achieved at both transient and steady state.

With the proposed method to increase system's tolerability to communication impact, modern communication tools, like PLC, Bluetooth and Zigbee, which are low-cost and flexible but limited by low-bandwidth, can be applied to master-slave control of parallel interfacing inverter system while keeping good steady state and transient performances, which is conducive to make the inverter cost-effective, intelligent and modular. The method can also be expanded to other parallel converter systems.

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# Chapter 5 A Method for Solving Current Unbalance Problem of Paralleled Single-Phase Grid-connected Unipolar-PWM Inverters with Common Dc Bus

The work described in this chapter was published in the following paper: D. Li, C. Ho, and K. Siu, “Current Unbalance Problem of Paralleled Grid-connected Unipolar PWM Inverters with Common Dc Bus”, *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7595-7603, Nov.-Dec. 2019. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2017 [5.1].

In this chapter, to apply unipolar PWM full bridge topology to parallel operation, a switching current sensor method is proposed to solve the unbalance inductor current problem. Small signal model is established to identify the problem, which is caused by interfered current control loops. With proposed control method, unipolar topology can be used as interface module while keeping its low cost and high efficiency, by simply adding one more current sensor.

## 5.1 Abstract

Unipolar-PWM (UP-PWM) inverter takes advantages of high-power efficiency and small output chokes which is widely used in industry. However UP-PWM inverters cannot be used in parallel operation due to a current unbalance problem. This paper studies the current unbalance problem of paralleled UP-PWM inverters with common dc bus and ac bus. Firstly, the problem of unbalanced inductor current is defined and analyzed. Secondly, a technique to eliminate unbalanced currents is proposed. The proposed current balancing technique only requires one more

current sensor in an inverter module rather than changing converter topology or modulation method, which makes it possible to apply unipolar-PWM inverters in parallel-operation while keeping the advantages of unipolar switching. The proposed current balancing method is verified by both simulation and hardware experiment. Experimental verification is performed on two 1kW, 400V input, and 120V/60Hz output prototypes, which shows a good agreement to the analytical study.

## 5.2 Introduction

Photovoltaic (PV) generation plays an important role in renewable energy and the future smart grids. Voltage Source Inverter (VSI) is an interface of injecting solar power into public ac grid [5.2]. With the growing demands for PV generation, the requirement of larger capacity and higher flexibility on solar inverter becomes more and more significant. Conventional single-operated solar inverter has a lot of restrictions in terms of scalability, reliability and flexibility and will face the problem of light load operating and higher loss due to using of high current power semiconductors or bulky passive components [5.3]. Parallel-operated inverters can reduce the stress of high current by distributing power into multiple modules. Thus, parallel-operated modular converters are preferred in many situations [5.4]-[5.6].

Figure 5-1 shows two typical configurations of distributed PV generation system [5.7]. In both dc-module type and multistring type, power generated from PV panels firstly converted by dc-dc converters with maximum power point tracking (MPPT) controller to a common dc bus, and then go through a dc-ac stage to the public grid. A centralized inverter was commonly used in this dc-ac stage [5.8]. However, a centralized inverter lacks scalability, reliability and flexibility for grid-connected application. Hence, modularized architecture will be preferred for the dc-ac stage in

many cases. Figure 5-2 shows the connection that two inverter modules working in parallel with common dc and ac buses. Using a number of parallel-operated inverter modules takes advantages rather than using a single centralized inverter:

1) Redundancy can be improved by the N+1 configuration realized by multi-module parallel operation, which can increase the system reliability [5.9]-[5.10].

2) System control can be more flexible. Power sharing strategy can be made based on parallel operation, to avoid inverter light-load operating. Each module can operate at its optimized power rating, which can improve system performance [5.11]-[5.14].

3) System can be more scalable. System capacity can be increased by simply adding more inverter modules without removing existing inverters [5.15].

4) Modularized inverters meet the requirement of mass production, which will significantly reduce cost of design and production.

However, there are some problems when inverters operate in parallel mode, of which the most significant one is unbalanced current. In order to analyze and understand the issues and characteristics of paralleling inverters, researchers investigated several cases of parallel-operated grid-tied inverters with different topologies and modulation strategies [5.16]-[5.17]. Among the cases, bipolar PWM (BP-PWM) inverter, Unipolar Double Frequency PWM (UDF-PWM) inverter [5.18], and H5 inverter [5.18] are free of unbalance current problem in parallel operation; full-bridge inverter with Unipolar Pulse Width Modulation (UP-PWM) faces a current unbalance problem in parallel operation. A UP-PWM inverter has only 2 high-frequency (HF) switches and only 1 of the HF switches is switching at one moment, which is less than other modulation methods mentioned above, where the details are given in table I. The switching combination of UP-PWM inverter could provide a lower switching loss and lower semiconductor cost [5.19]-[5.20].

However, the unbalance current problem in parallel operation makes the advantages of UP-PWM inverters cannot be maintained in the parallel-operating mode. Furthermore, there is no study giving any detailed explanation on the causes of generating unbalanced currents or providing any solution to balance the currents without changing topology or modulation method. It makes that UP-PWM inverter has not been widely used for paralleling to scale up the rated power. The proposed method enables parallel operating of UP-PWM inverters with simply adding one more current sensor, and the advantage of low switching loss and low semiconductor cost can be kept.

In order to standardize inverter modules, which are capable of scaling up the handling power by paralleling, this paper proposes a method to achieve the following features in UP-PWM inverters,

- 1) The inverter modules are unipolar switching either in single-module or multi-module operating mode. It provides the advantages of small output choke size and semiconductor losses [5.21]-[5.22].

- 2) Grid current can be evenly shared by the inverter modules.

In this paper, firstly, the problem of unbalanced inductor currents in parallel-operated UP-PWM inverters is defined and analyzed by system equivalent circuits and control loop analysis. The idea of Switched-Controlled (SC) and Non-Switch-Controlled (NSC) inductor, which is resulted by the nature of unipolar switching, was proposed to explain the current unbalance problem. Then a new concept of proposed dual current sensor technique to solve the inductor currents balancing issue is introduced. Two Digital Signal Processor (DSP) controlled, 1kW, 400V input, and 110V/60Hz output inverter modules have been implemented and evaluated in parallel connection. Proposed method is verified by experimental test. The result shows a good agreement to analytical study.

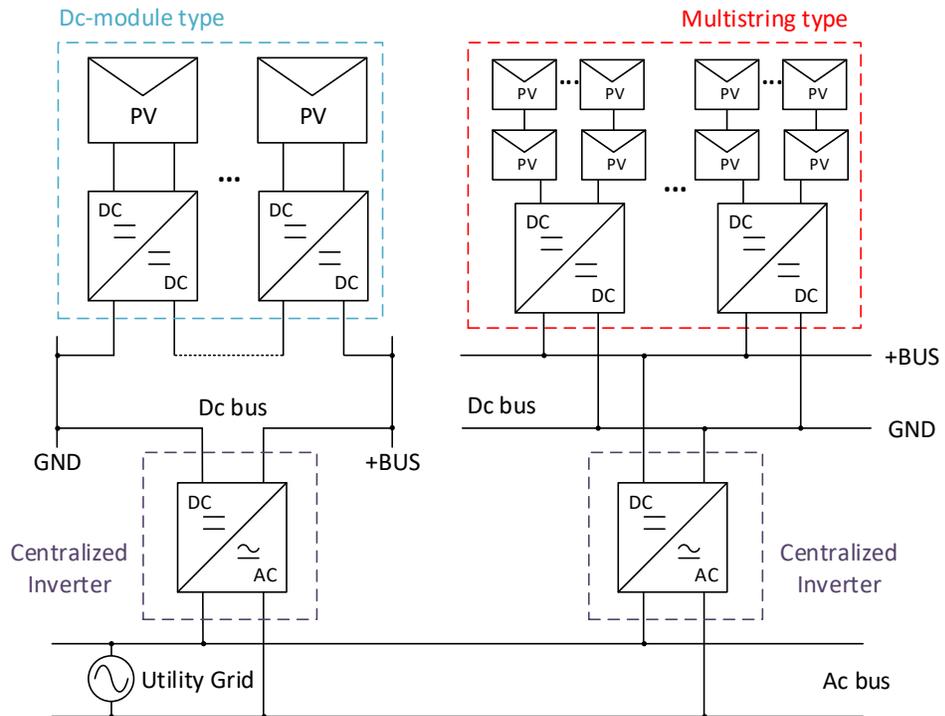


Figure 5-1. Typical distributed PV generation systems.

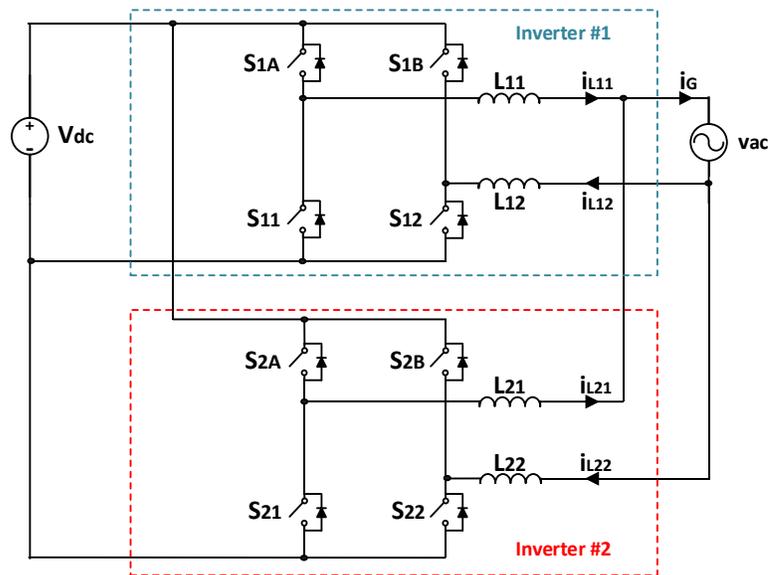


Figure 5-2. Parallel-operated inverters with common dc bus and ac bus.

TABLE 5-I NUMBERS OF SEMICONDUCTORS USED FOR FULL BRIDGE INVERTERS WITH DIFFERENT PWM METHODS OR TOPOLOGIES

	No. of Switches		No. of HF Switches under operating	No. of Switches in the Main Current Path
	HF	LF		
UP-PWM	2	2	1	2
BP-PWM	4	0	4	2
UDF-PWM	4	0	2	2
H5	3	2	2	3

### 5.3 Analysis of Unbalanced Inductor Current

In this section, the cause of unbalanced inductor current problem in conventional parallel-operated UP-PWM inverters is identified and analyzed.

Figure 5-3 (a) shows a typical full bridge grid-connected VSI with two split-filter inductors and its controller block diagram with UP-PWM switching scheme. Figure 5-3 (b) shows a typical unipolar PWM switching pattern for the full bridge VSI.  $S_A$  and  $S_B$  are line frequency (e.g. 60 Hz) switches and  $S_1$  and  $S_2$  are high frequency (e.g. 20 kHz) switches. This combination of semiconductors gives a better switching performance by using MOSFETs and fast diodes [5.23]. It is widely used in industry, especially solar inverters [5.24]. The control algorithm can be easily realized by an analog or digital controller. Figure 5-2 shows the connection that two inverters operate in parallel with common dc bus and ac bus. Ideally, each inverter should be able to work individually or in parallel, so each of them has an independent controller as Figure 5-3 (a) shows.

If parameters of the two UP-PWM inverters are identical, equal current sharing among the

paralleled inverters should be possible. However, in a real application, the inductor current will become unbalanced. The cause of this unbalanced current issue is studied in this section, which is found out to be a misalignment of the current reference or sensor gain.

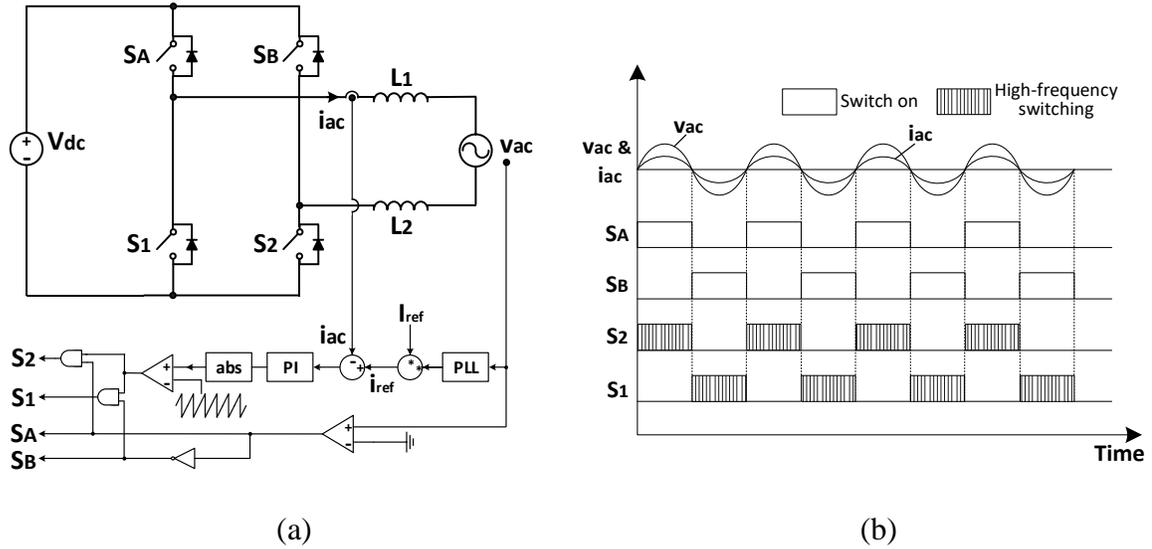


Figure 5-3. Typical full bridge inverter with UP-PWM: (a) topology and control, and (b) switching pattern.

A simulation model was built considering differences in PWM carrier signals and current reference signals. Each inverter module is same as shown in Figure 5-3. The connection is shown in Figure 5-2. Current sensors are set to sense currents on  $i_{L11}$  and  $i_{L21}$ . Simulation parameters are shown in TABLE II. Two carrier sawtooth signals are set to be unsynchronized, in the simulation case, which have a phase difference of half cycle  $\pi$ . Parameter  $K_{ref}$  is used to represent the difference between two reference signals,

$$i_{ref2} = K_{ref} \cdot i_{ref1} \tag{4-1}$$

Figure 5-4 shows the simulation results that  $K_{ref}$  varies from 1 to 0.994. It can be seen in Figure 5-4 (a) that when  $i_{ref1} = i_{ref2}$ , though the current ripples are not symmetrical and varying

due to the unsynchronized sawtooth signals, two inverters can equally share power, and inductor currents are balanced. In Figure 5-4 (b), (c) and (d), though the difference of two reference signals are very small that less than 1 percent, inductor currents  $i_{L12}$  and  $i_{L22}$  become seriously distorted and unbalanced. And while the reference difference getting larger, the currents become more unbalanced. At the same time, grid current  $i_G$  and inductor currents  $i_{L11}$ ,  $i_{L21}$  are still sinusoidal and following references. The unbalanced currents on  $L12$  and  $L22$  could already damage devices and have distorted the power sharing purpose of inverters parallel operating.

Noticing that unbalanced current only happens in half cycle of operation. Based on Figure 5-2 and the switching pattern in Figure 5-3 (b), equivalent circuits with controllers can be obtained when  $v_{ac}$  is in positive cycle and negative cycle, respectively, as shown in Figure 5-5 (a) and (b). Figure 5-6 shows the corresponding control block diagrams.  $T_1$  and  $T_2$  are the open-loop transfer functions of the two inverters.

TABLE 5-II PARAMETERS OF SIMULATED INVERTER MODULES

Parameter	Value	Parameter	Value
$V_{ac-rms}$	120 V	$V_{DC}$	380 V
$I_{ref1}$	5 A	$f_{sw}$	20 kHz
$L_{11}, L_{12}, L_{21}, L_{22}$	2 mH	Sawtooth Signal Phase Difference	$\pi$
$k_p$	0.07	$k_i$	350

TABLE 5-III OPERATING STATUS OF INDUCTORS

	HF switches	$L_{11}$	$L_{12}$	$L_{21}$	$L_{22}$
$v_{ac} > 0$	$S_{12}, S_{22}$	NSC	SC	NSC	SC
$v_{ac} < 0$	$S_{11}, S_{21}$	SC	NSC	SC	NSC

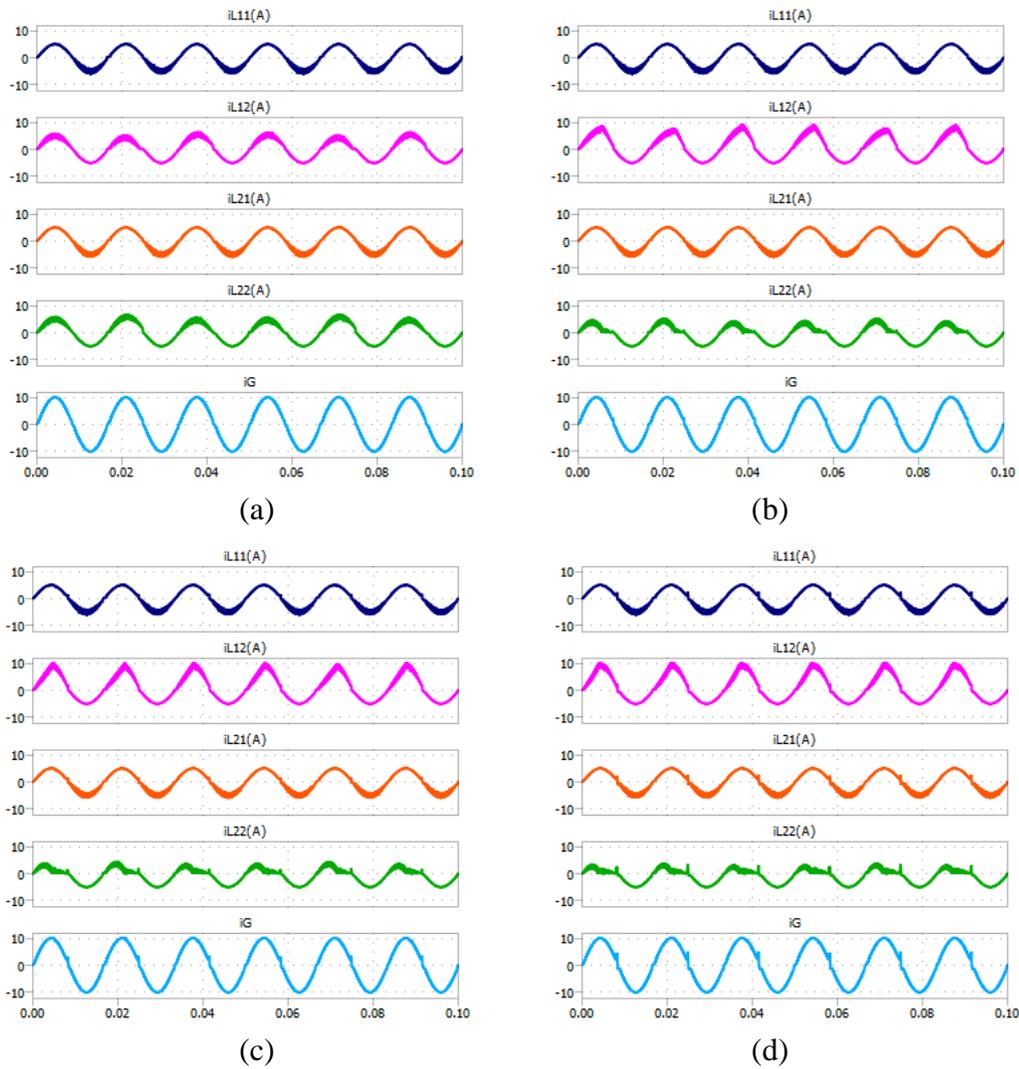


Figure 5-4. Simulation results of two conventional UP-PWM inverters work in parallel: (a)  $K_{ref} = 1$ , (b)  $K_{ref} = 0.998$ , (c)  $K_{ref} = 0.996$ , (d)  $K_{ref} = 0.994$ .

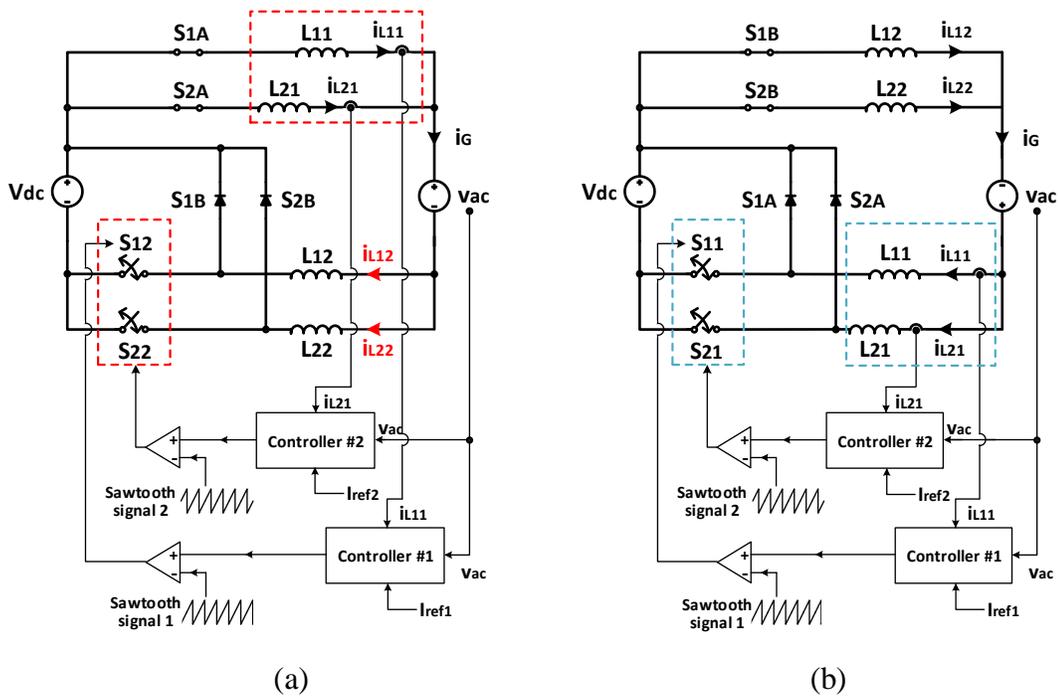


Figure 5-5. Parallel operating equivalent circuits,  $v_{ac}$  is in (a) positive half cycle, (b) negative half cycle.

The position of current sensors is physically fixed to sense currents on  $L_{11}$  and  $L_{21}$ , which makes the parallel operated system in positive and negative cycles different. In Figure 5-5 (a), feedback signals are from  $i_{L11}$  and  $i_{L21}$  on the upper branches, while the PWM signals go to  $S_{12}$  and  $S_{22}$  on the lower branches which are connected to  $L_{12}$  and  $L_{22}$ , as indicated in red dashed line blocks. It can be seen from the simulation results that current unbalance only happens in this half cycle. In Figure 5-5 (b), active switches  $S_{11}$ ,  $S_{21}$  and feedback signals  $i_{L11}$ ,  $i_{L21}$  are both on the lower branches as shown in blue dashed line blocks, in which case it is free of current unbalance problem.

Each UP-PWM inverter has two split inductors and only one high-frequency switch at a moment. Hence, the inductors can be separated into two operating conditions, Switching-Controlled (SC) and Non-Switching-Controlled (NSC). For the SC status, inductors are directly connected to high-frequency switches, so the inductor currents are directly influenced by switching

actions, like  $L_{12}$  and  $L_{22}$  in Figure 5-5 (a) and  $L_{11}$  and  $L_{21}$  in Figure 5-5 (b). For the NSC status, inductors are connected to a closed switch and are parallel with other NSC inductor. They share the grid current simply depending on branch impedance, like  $L_{11}$  and  $L_{21}$  in Figure 5-5 (a) and  $L_{12}$  and  $L_{22}$  in Figure 5-5 (b). Table III shows how the inductors act in two half cycles. Only when the feedback signals are from NSC inductor currents, unbalanced inductor currents will appear.

According to simulation results in Figure 5-4, unbalanced inductor currents only occur in the positive half cycle of  $v_{ac}$ , of which the equivalent circuit is shown in Figure 5-5 (a). In this half cycle,  $S_{12}$  and  $S_{22}$  are working at high frequency, which means  $i_{L12}$  and  $i_{L22}$  are SC inductor currents. However, the current sensors are fixed to measure  $i_{L11}$  and  $i_{L21}$  which are NSC inductor currents. The control block diagram for this half cycle is shown in Figure 5-6 (a). Two control loops are interacting with each other through the common ac bus. Meanwhile in the other half cycle, as shown in Figure 5-6 (b), the two control loops are still independent from each other which is free of unbalanced current problem.

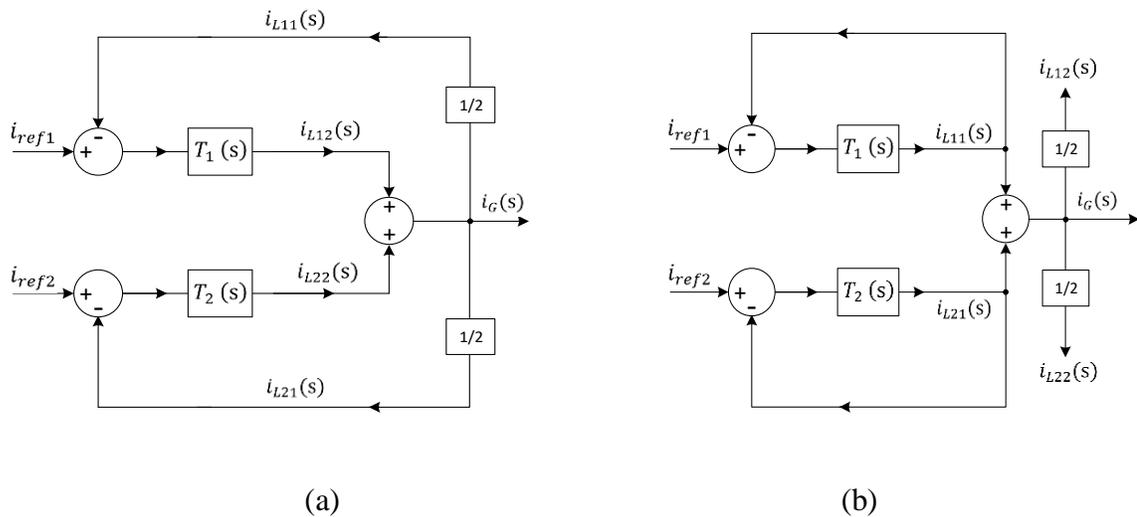


Figure 5-6. Parallel operating control block diagrams,  $v_{ac}$  is in (a) positive half cycle, (b) negative half cycle.

Based on the control block diagram shown in Figure 5-6 (a),  $i_G$  can be expressed as,

$$i_G = (i_{ref1} - i_{L11})T_1 + (i_{ref2} - i_{L21})T_2 \quad (4-2)$$

Assume all branches are identical,  $i_{L11}$  and  $i_{L21}$  will always equally share  $i_G$ ,

$$i_{L11} = i_{L21} = \frac{i_G}{2} \quad (4-3)$$

By putting (4-3) into (4-2),  $i_G$  can be written as,

$$i_G = \frac{i_{ref1}T_1 + i_{ref2}T_2}{1 + \frac{1}{2}T_1 + \frac{1}{2}T_2} \quad (4-4)$$

$T_1$  and  $T_2$  have almost same frequency responses and their gains are much larger than 1,

$$T_1 \approx T_2 \text{ and } |T_1| \approx |T_2| \gg 1 \quad (4-5)$$

Based on (4-4) and (4-5), we can have the expression of  $i_G$  at low frequency,

$$i_G \approx i_{ref1} + i_{ref2} \quad (4-6)$$

Hence, grid current  $i_G$  can well follow the references, and if  $i_{ref1} \approx i_{ref2}$ , NSC inductor currents  $i_{L11}$ ,  $i_{L21}$  could also follow each reference based on (4-3).

From Figure 5-6 (a), we could also have,

$$i_{L12} = (i_{ref1} - i_{L11})T_1 = \left(i_{ref1} - \frac{i_G}{2}\right)T_1 \quad (4-7)$$

By putting (4-1) and (4-4) into (4-7),

$$i_{L12} = \left(\frac{2i_{ref1} + i_{ref1}T_2 - K_{ref}i_{ref1}T_2}{2 + T_1 + T_2}\right)T_1 \quad (4-8)$$

Simplify (4-8),

$$\frac{i_{L12}}{i_{ref1}} = \frac{2T_1 + (1 - K_{ref})T_1T_2}{2 + T_1 + T_2} \quad (4-9)$$

Similarly, for inverter #2, it also can be derived that,

$$\frac{i_{L22}}{i_{ref2}} = \frac{2T_2 + (1 - \frac{1}{K_{ref}})T_1T_2}{2 + T_1 + T_2} \quad (4-10)$$

Putting (4-5) into consideration, (4-9) and (4-10) can be rewritten as,

$$\frac{i_{L12}}{i_{ref1}} = 1 + (1 - K_{ref})T_1 \quad (4-11)$$

$$\frac{i_{L22}}{i_{ref2}} = 1 + (1 - \frac{1}{K_{ref}})T_2 \quad (4-12)$$

Apparently, if  $K_{ref}$  is ideal that equal to one, values of equations (4-11) and (4-12) will both be one, which means inductor currents  $i_{L12}$  and  $i_{L22}$  can follow the references  $i_{ref1}$  and  $i_{ref2}$  respectively. However, even if  $K_{ref}$  is just slightly different from 1, values of equation (4-11) and (4-12) will deviate from one significantly, because gain of  $T_1$  and  $T_2$  is designed to be large enough to obtain smaller steady state error. It means the slight difference of current reference or sensing gain will be amplified. As a result, inductor currents become unbalanced between SC inductor currents  $i_{L12}$  and  $i_{L22}$ , as the simulation results shown in Figure 5-4. Moreover, equations (4-11) and (4-12) also agree the simulation results that the more  $K_{ref}$  is far from 1, the more distorted and unbalanced the currents are.

When  $v_{ac}$  is in the negative half cycle, the feedback signals  $i_{L11}$  and  $i_{L21}$  are SC inductor currents. The equivalent circuit and control diagram are shown in Figure 5-5 (b) and Figure 5-6 (b) respectively. It can be seen from Figure 5-6 (b),  $i_{L11}$  and  $i_{L21}$  are controlled by two independent control loops, that satisfy,

$$i_{L11} = \frac{T_1 i_{ref1}}{1 + T_1} \quad (4-13)$$

$$i_{L21} = \frac{T_2 i_{ref2}}{1 + T_2} \quad (4-14)$$

While considering assumption (4-5),

$$i_{L11} \approx i_{ref1} \quad (4-15)$$

$$i_{L21} \approx i_{ref2} \quad (4-16)$$

And  $i_{L12}$  and  $i_{L22}$  will equally share  $i_G$ ,

$$i_{L12} = i_{L22} = \frac{i_{ref1} + i_{ref2}}{2} \quad (4-17)$$

Therefore, all four inductor currents can follow the reference in the negative half cycle of  $v_{ac}$  which agrees simulation results in Figure 5-4.

Based on the analysis above, the difference of current references of parallel-operated inverters, which is represented by (4-1), is the major reason of unbalanced inductor currents happening. Although individual digital controllers have the same digital reference values, eventually the references can hardly be the same such as in unit feedback equivalent diagrams Figure 5-6, due to the error of sampling circuit, analog-digital conversion and environmental noises. Therefore,  $K_{ref}$  in (4-1) cannot reach one practically.

## 5.4 Proposed Dual Current Sensor Method

While the misalignment of current reference or sensor gain cannot be removed practically, there are other approaches may solve the current unbalance problem.

Based on analysis in Section II, the current unbalance problem is caused by the control structure shown in Figure 5-6 (a) that the feedback signals are from NSC inductor currents when in the positive half cycle of  $v_{ac}$ . When  $v_{ac}$  is in the negative half cycle, the control structure as shown in Figure 5-6 (b) is free of unbalance current problem. To mitigate the unbalanced currents,

the control block diagram should be modified in the positive half cycle of  $v_{ac}$  to change the feedback signal to SC inductor currents. Then in both half cycles, the control structure could be kept as same as in Figure 5-6 (b).

Hence, when the high frequency switches are  $S_{12}$  and  $S_{22}$ , feedback signals should be  $i_{L12}$  and  $i_{L22}$  rather than  $i_{L11}$  and  $i_{L21}$ . Figure 5-7 shows the proposed modification to the control diagram in this half cycle. The proposed technique is to simply add one more current sensor on each inverter module to measure currents on both inductors, then current feedback signal is inter-changed accordingly between two measured current signals in positive and negative half cycles.

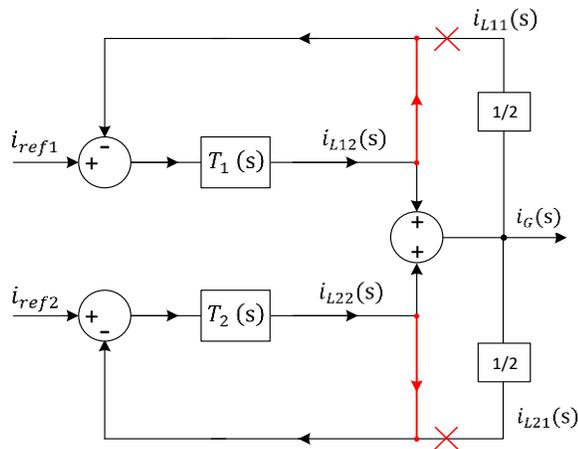


Figure 5-7. Modification to avoid unbalanced inductor currents,  $v_{ac} > 0$ .

The proposed dual current sensor technique is highlighted with a red dash block in the control block diagram in Figure 5-8 (a). Two current sensors are used in each inverter to measure currents on both two split inductors. When  $S_A$  is turned on,  $S_2$  is working at high frequency, SC inductor current  $i_{L2}$  will be taken as the feedback signal. When  $S_B$  is turned on,  $S_1$  is working at high frequency, SC inductor is changed to  $L_1$ , and  $i_{L1}$  will be taken as the feedback signal. By drawing parallel-operating equivalent circuits, when  $v_{ac}$  is in negative cycle, inverters operate the same as

the equivalent circuit in Figure 5-5 (b). When  $v_{ac}$  is in positive cycle, feedback signals change to  $i_{L12}$  and  $i_{L22}$ , and equivalent circuit changes to Figure 5-8 (b). Therefore, the parallel-operated inverters can work symmetrically in positive and negative half cycle, and inductor currents will be well balanced all the time.

With the proposed method, in negative half cycle of  $v_{ac}$ , four inductor currents will keep following equations (4-15) – (4-17). In positive half cycle of  $v_{ac}$ , the four inductor currents now follow,

$$i_{L12} \approx i_{ref1} \quad (4-18)$$

$$i_{L22} \approx i_{ref2} \quad (4-19)$$

$$i_{L11} = i_{L21} = \frac{i_{ref1} + i_{ref2}}{2} \quad (4-20)$$

Hence, while  $i_{ref1} \approx i_{ref2}$ , all inductor currents will be balanced all the time. It also can be seen that, if  $i_{ref1}$  and  $i_{ref2}$  are different, inductor currents will become unsymmetrical in positive and negative half cycles. When the inductor is SC, inductor current will follow one of the reference currents, which is represented by (4-15) - (4-16) and (4-18) - (4-19). When the inductor is NSC, it follows average of two current references, which is represented by (4-17) and (4-20). At the same time the total output current always follows  $i_{ref1} + i_{ref2}$ .

With added current sensor, the control structure of parallel inverter system can always be kept as independent control loops. Every inverter can well regulate its output current as a sinusoidal waveform. Though the added sensor also contains sensing error, it will not affect the controller function.

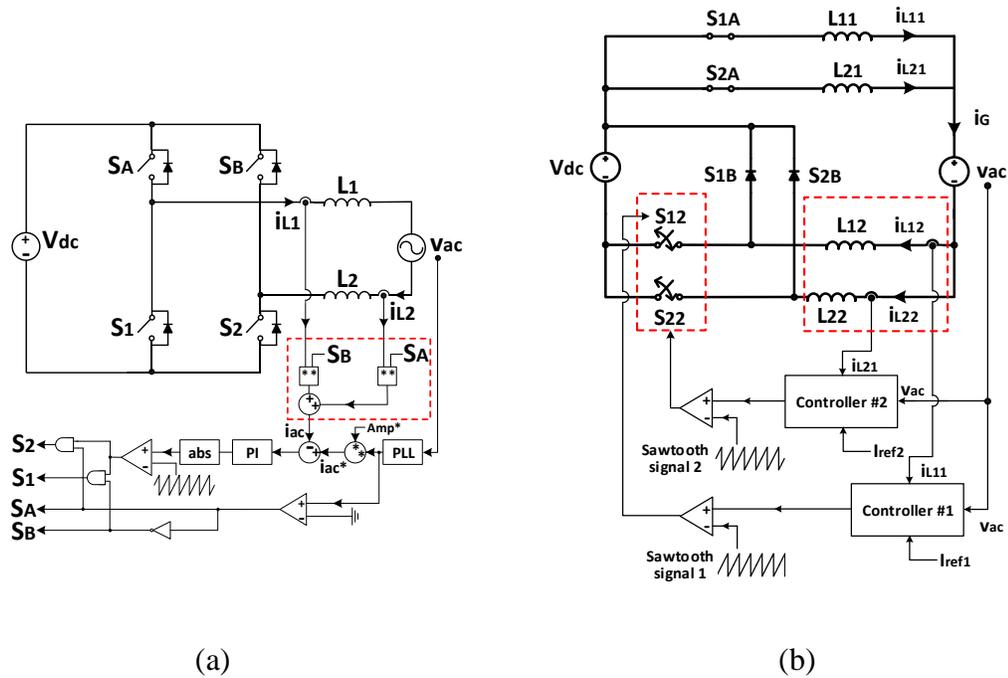


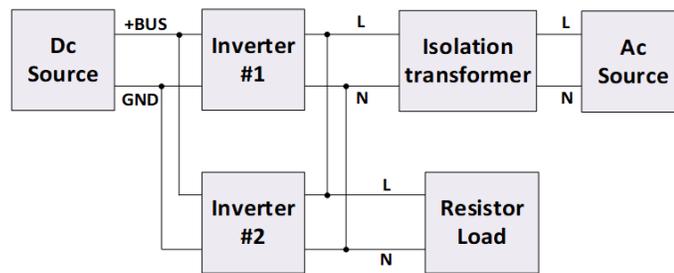
Figure 5-8. Proposed method to balance inductor currents in parallel operation: proposed method, and (b) its parallel operating equivalent circuit when  $v_{ac}$  is in the positive cycle.

## 5.5 Experimental Verification

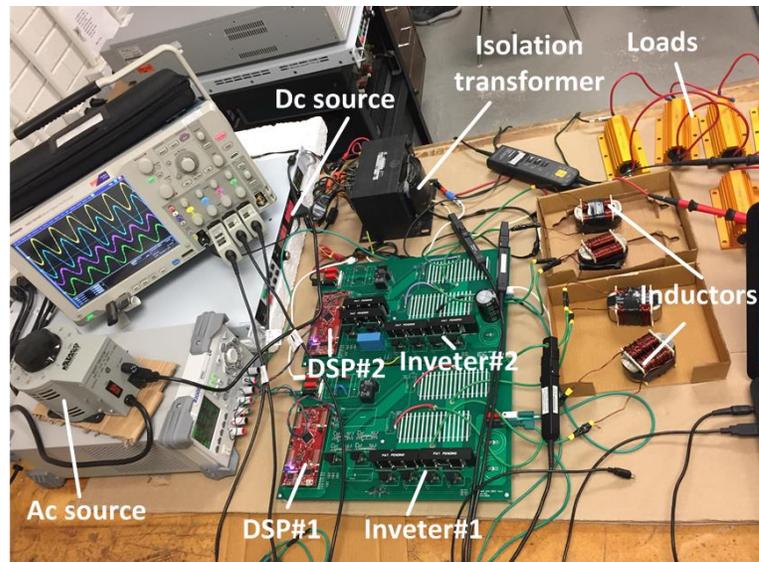
An experimental testbed has been implemented with two 1kW, 380V input, 120V output grid-connected full bridge inverter prototypes, where the 380V is a typical dc link voltage for dc microgrid or solar farm applications [5.24]. The specification is shown in TABLE IV. Each inverter module is controlled by a TI F28377s DSP individually. The connection diagram and a photo of test setup are shown in Figure 5-9 (a) and (b), respectively. The resistor load is used to absorb excess power go through the isolation transformer as a consideration of experiment safety. The current sensor used is hall effect current transducers LEM LAH 25-NP, which have an accuracy of  $\pm 0.3\%$ . This accuracy could promise a minimized harmonic issue may be caused by the switching feedback signals.

TABLE 5-IV SPECIFICATIONS OF EXPERIMENTAL TESTBED

Parameter	Value	Parameter	Value
$V_{ac-rms}$	120 V	$V_{DC}$	380 V
$P_o$	2 kW (1 kW each)	$f_{sw}$	20 kHz
$L_{11}, L_{12}, L_{21}, L_{22}$	2 mH	$k_p$	0.07
		$k_p$	350



(a)



(b)

Figure 5-9. Experimental setup, (a) connection diagram, and (b) testing platform.

Figure 5-10 shows the experimental waveforms that two inverter modules work in parallel using conventional control scheme. Though the total grid current  $i_G$  is stable and sinusoidal, the inductor currents are already unbalanced and distorted. The unbalanced currents only appear when  $v_{ac}$  is in positive half cycle, and one inductor current is almost doubled while the other one is zero. This shows a good agreement to the analytical study in section II. According to equations (11) and (12), how the two inverters share the unbalanced currents is depending on the value of  $K_{ref}$ . In the simulation study,  $K_{ref}$  is set to a fixed value, so the unbalanced currents are periodic as shown in Figure 5-4. However, in a real experiment, the sensing circuit parameters may vary due to temperature, and the performance of phase-lock-loop (who give the sinusoidal shape to the current reference), even noises could affect the value of  $K_{ref}$ . The  $K_{ref}$  fluctuating around 1.0 gives the result as shown Figure 5-10.

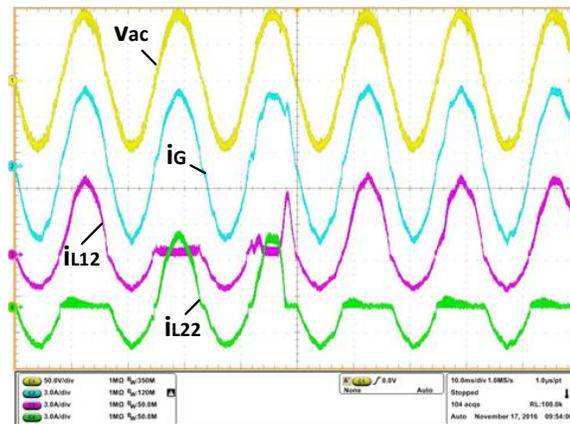


Figure 5-10. Experimental waveforms of two inverters working in parallel using conventional scheme.

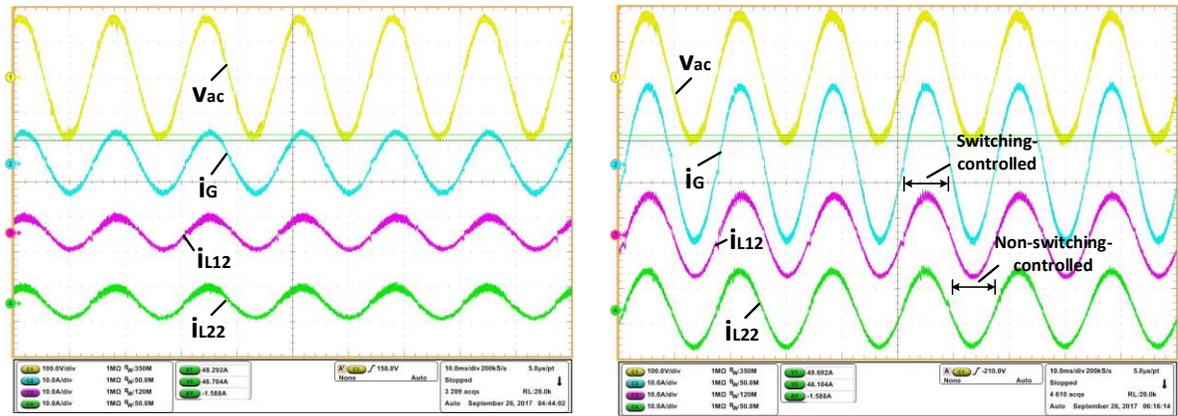
Figure 5-11 shows experimental results that two UP-PWM inverter modules work in parallel using the proposed dual current sensor method. It can be seen that the inductor currents in two inverter modules are well balanced under different load conditions. Measured by power analyzer, at rating of 700w each, the grid current THD is 1.72% and harmonic of each order can fulfill power

quality standard. Thus, with proposed method, full bridge UP-PWM inverters can be applied in parallel-operation.

It also can be seen in Figure 5-11 that current ripples of inductor currents are different in their positive and negative half cycles. When the inductor is SC, as mentioned in Section II, it appears a larger ripple, which is the actual switching ripple. In the other half cycle, when the inductor is NSC, it shows current ripple as half of grid current. The grid current ripple is smaller due to the interleaving effect when there is a phase shift between the PWM signals of two inverters. Thus, the NSC inductor current shows a smaller ripple. Figure 5-12 shows the experimental waveforms of inductor current ripples, where  $i_{L12}$  and  $i_{L22}$  are SC inductor currents and  $i_{L11}$  is one of NSC inductor currents. The different current ripples in positive and negative cycles only appear on the inductor current, instead of grid current, which is harmless to the grid. And for the grid current, it always shows the interleaved current with smaller ripple in both positive and negative cycles.

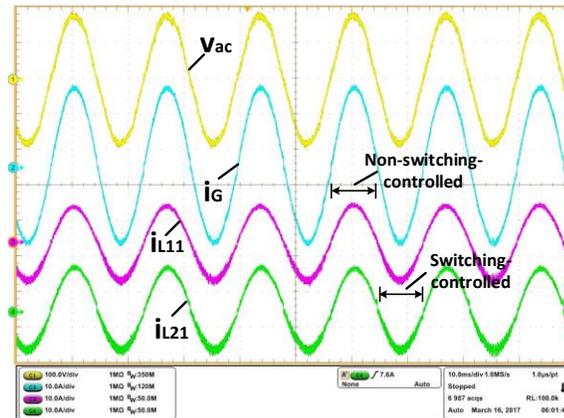
From equations (15) – (20), we can see that while SC inductor currents can strictly follow their own current references, the NSC inductor will just simply share the total current. It means, if the paralleled inverters are at different ratings, the NSC inductor currents cannot be guaranteed to work at its rated power. The experimental result that two UP- PWM inverters operating in parallel with different power rating is shown in Figure 5-13. Inverter #1 is set to operate at 400W while inverter #2 is set to 1000W. It can be seen that when the inductor current is SC, it follows its own reference, when the inductor current is NSC, it equally shares the grid current with the other NSC inductor current. This shows one limitation of UP-PWM inverter in parallel operation that the inverters must be in same rating, otherwise the inverters with lower rating will be over current. It is still suitable for modular inverter application, since the modules are identical to each other, as a requirement of mass production.

Figure 5-14 shows the experimental result that one of the parallel-operated inverters is out of service. At a preset moment, inverter #1 is disconnected (all four switches are turned off). It can be seen that, after one inverter being turned off, the other inverter can still work steadily, even at transient.



(a)

(b)



(c)

Figure 5-11. Experimental waveforms of two inverters working in parallel with proposed dual current sensor method: (a) rated at 400W each, (b) 700W each with showing  $i_{L12}$  and  $i_{L22}$ , (c) 1000W each with showing  $i_{L11}$  and  $i_{L21}$ .

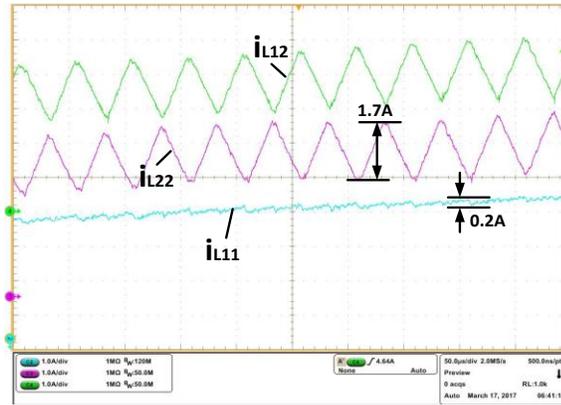


Figure 5-12. Experimental waveforms of inductor current ripples.

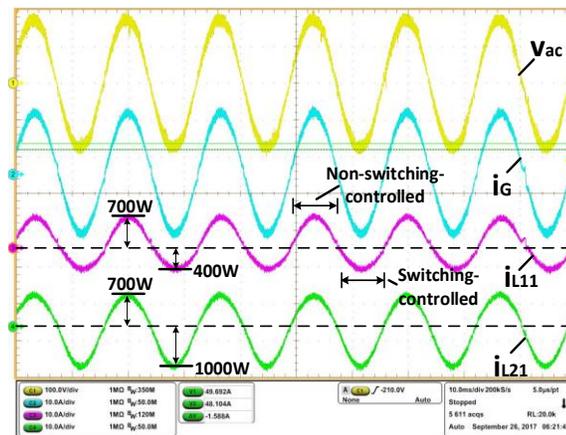


Figure 5-13. Experimental waveforms that two inverters with different ratings operate in parallel with proposed method, inverter#1 is given a 400W reference and inverter#2 is given a 1000W reference.

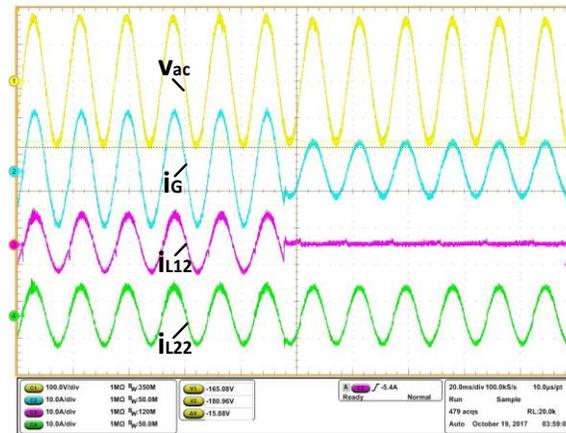


Figure 5-14. Experimental waveforms that one of the parallel-operated inverters is in outage.

## 5.6 Conclusion

The chapter studied the parallel-operation of grid-connected UP-PWM inverters with common dc bus. The problem of unbalanced inductor currents in parallel-operated UP-PWM inverters was studied by equivalent circuit and control loop analysis. The idea of Switched-Controlled (SC) and Non-Switch-Controlled (NSC) inductor, which is resulted by the nature of unipolar switching, was proposed to explain the current unbalance problem. Based on the analysis, the dual current sensor technique was established to solve the unbalanced inductor current problem. The concept is to add one more current sensor to measure both of two split inductor currents in each inverter and select feedback signal alternately in different switching modes. By keeping the feedback signal from SC inductor current, the current unbalance problem can be solved. Analytically and experimentally verifications was demonstrated to verify the found solution and analysis. The study in this paper proves that, by simply adding a current sensor to each inverter module, it is possible to apply UP-PWM inverters in parallel-operation while keeping the

advantages of high efficiency and small output chokes without changing topology or modulation method.

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## Chapter 6 Reactive Power Control for Single-phase Grid-tie Inverters using Quasi Sinusoidal Waveform

The work described in this chapter was published in the following paper: D. Li, C. Ho, L. Liu, and G. Escobar, “Reactive Power Control for Single-phase Grid-tie Inverters using Quasi Sinusoidal Waveform,” *IEEE Trans. Sustain. Energy*, vol. 9, no. 1, pp. 3-11, Jan. 2018. The work was also presented in part as a conference paper at the 42th Annual Conference of the IEEE Industrial Electronics Society, 2016 [6.1].

The key technologies using low-cost communication device for master-slave current-sharing control and utilizing modular full bridge inverter with unipolar switching scheme as a dc/ac grid interface have been discussed in the last two chapters. With the proposed technologies, the reactive power delivery will be challenging that a tiny mismatch of phase information could cause significant short circuit. In this chapter, a quasi-sinusoidal current waveform is proposed for reactive power delivery. The proposed method keeps same zero-crossing point of grid current and voltage but can deliver reactive power by adding harmonics. Using conventional four-quadrant reactive power delivery method, the parallel unipolar converters may operate with different phase shift which will cause short circuit on dc link. The proposed method enables reactive power delivery on unfolding topologies and unipolar topologies with a trade-off of harmonic current.

### 6.1 Abstract

This chapter presents a reactive power control technique for single-phase Photovoltaic (PV) inverters, especially unfolding inverters. The proposed system retains the benefit of the unfolding

inverters having low material cost and semiconductor losses, and tackles the drawback of the standard unfolding inverter not having capability of reactive power injection. It is important to note that reactive power delivery is mandatory for PV inverters according to the recent announced regulations. The concept is based on changing the shape of the grid current waveform but keeping the same zero crossing points as in the unity power factor condition. The current waveform is governed by real power and reactive power, at the price of an acceptable deformation. The operating principles of the proposed technique and mathematical derivations of the grid current function are provided in the paper. Experimental results in a grid-tie inverter prototype have shown a good agreement with the derived theory, and they confirm the feasibility of using the proposed technique in grid-tie inverters.

## 6.2 Introduction

Unfolding grid-tie inverters are generally used in Photovoltaic (PV) and Fuel Cell (FC) applications [6.2]-[6.9]. This is because a simple controller can be applied and it can minimize the number of high frequency switching semiconductors, e.g. MOSFETs. This leads to low component cost and high efficiency. Figure 6-1 shows a typical system block diagram of an unfolding grid-tie inverter [6.4]. The front stage is a dc-dc converter, which converts a dc current from a voltage source, such as PV Cells, to a rectified sinusoidal inductor current. The second stage is a line frequency inverter to unfold the inductor current into a bipolar sinewave current, which is synchronized with the grid voltage [6.10]-[6.12]. Typically, semiconductor switches in the line frequency inverter are SCR thyristors [6.10]. It is well-known that SCR are turned off at zero current with relatively long commutation time which makes difficult for the injection of reactive power. Thus, the impossibility of injecting reactive power is the main drawback of unfolding

inverters. However, a new regulation has been recently published to require that PV inverter products must have the capability to adjust Power Factor (PF) up to 0.95 in either inductive or capacitive modes [6.13]-[6.14]. In consequence, a lot of already designed commercial products are facing the problem of not passing such a regulation. Some advanced modulation methods have been proposed recently to satisfy the PF regulation [6.15]-[6.16], but they cannot be applied to unfolding inverters since the zero crossing points of grid voltage and current are not the same. Thus, manufacturers have to redesign PV inverter system completely using different semiconductors or changing topology to be more complicated and expensive such as Neutral Point Clamped (NPC) inverters to satisfy the regulation in their future products.

Beside the regulation, unfolding inverters give a high efficiency when using MOSFETs in the line frequency inverter stage instead of SCRs. A commercial single phase PV inverter system can achieve 97.8% European efficiency with using Silicon MOSFETs only in the inverter stage [6.17]. The MOSFETs effectively reduce the conduction loss comparing to SCRs. However, the zero crossing points of grid current and grid voltage have to be synchronized, otherwise it will produce a short circuit path by the body diodes, otherwise, a cascaded blocking diode is required for each MOSFET. The high efficiency advantage does not exist anymore due to a high conduction loss at the diodes [6.18]. Nevertheless, reactive power cannot be delivered to the grid. A manufacturer has provided a solution which changes the shape of the grid current waveform to give a capability of generating 0.95 power factor [6.19]. However, there are no further literatures to provide the operating principles and the performance evaluations by using the method.

This paper follows up the idea in the literature [6.19] to propose a control technique for grid-tie inverters, especially unfolding inverters. The delivered grid current is modified to the proposed Quasi Sinusoidal Waveform (QSW) to carry reactive power, and thus satisfying the PF regulations.

The modified current keeps the same zero crossing points as the grid voltage. The injection of reactive power is thus possible at the expenses of an acceptable current shape deformation. Although it contains harmonics during reactive power delivering and it is the drawback of the proposed waveform, the total harmonic distortion (THD) is relatively low. Recall that, during unity power factor, the current satisfies the THD regulation such as IEC61000-3-2 [6.20]. This paper provides the mathematical derivation of the proposed grid current reference function. Numerical and experimental results of the proposed technique applied to an grid-tie inverter are presented to verify the theoretical findings.

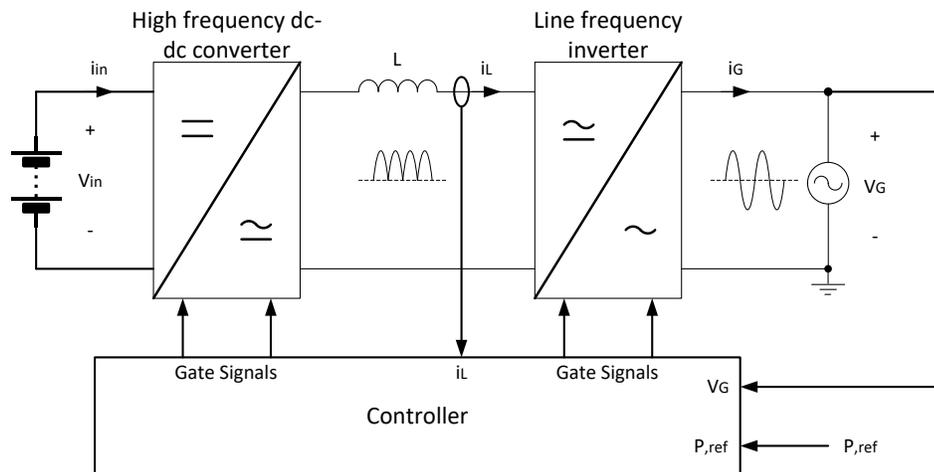


Figure 6-1. A typical single-phase grid-tie unfolding inverter system.

## 6.3 Steady State Characteristic

### 6.3.1 Ideal Quasi Sinusoidal Waveform

In this paper, Quasi Sinusoidal Waveform (QSW) is defined as a waveform which is formed by sinusoidal waveforms with different frequencies. The resultant waveform is close to a sinewave but it includes harmonics in the signal. Figure 6-2 shows the proposed QSW signal indicated by a solid blue line, which is proposed as the reference for the delivered grid current. This waveform is divided into 4 time intervals, where the boundaries are fixed at peaks and zero crossings of this waveform. Notice that each interval consists of a fraction of a sine function that frequency alternates between two different values. The mathematical expression of such a composed function is given by,

$$f(t) = \begin{cases} -A \sin \frac{\omega t + \pi}{2\alpha}, & -\pi \leq \omega t < -(1 - \alpha)\pi \\ A \sin \frac{\omega t}{2(1-\alpha)}, & -(1 - \alpha)\pi \leq \omega t < 0 \\ A \sin \frac{\omega t}{2\alpha}, & 0 \leq \omega t < \alpha\pi \\ -A \sin \frac{\omega t - \pi}{2(1-\alpha)}, & \alpha\pi \leq \omega t < \pi \end{cases} \quad (6-1)$$

where  $\alpha$  adjusts the shape of the curve and is referred as adjusting ratio. For instance, in Figure 6-2,  $\alpha$  is set to 0.75.  $A$  is peak value and  $T$  is period. Figure 6-3 shows QSW signals with different  $\alpha$ . Notice that, for  $\alpha = 0.5$ , a regular sinusoidal waveform is generated, otherwise the peaks of the waveform are shifted.

The frequency of sinusoidal waves that constitute QSW in each interval can be determined by resultant QSW signal frequency  $f_Q$  and  $\alpha$  as,

$$f_I = f_{III} = \frac{f_Q}{2\alpha} \quad (6-2)$$

$$f_{II} = f_{IV} = \frac{f_Q}{2(1-\alpha)} \tag{6-3}$$

These two variables,  $\alpha$  and A, in (6-1) are used to adjust power factor and current amplitude of a current injecting into a grid. Figure 6-3 shows a QSW with different  $\alpha$ . When  $\alpha$  is 0.5, it is a pure sinusoidal waveform, otherwise the peaks of the waveform are shifted. In the graph can be seen that the resultant frequency, and zero crossing points of waveforms are the same.

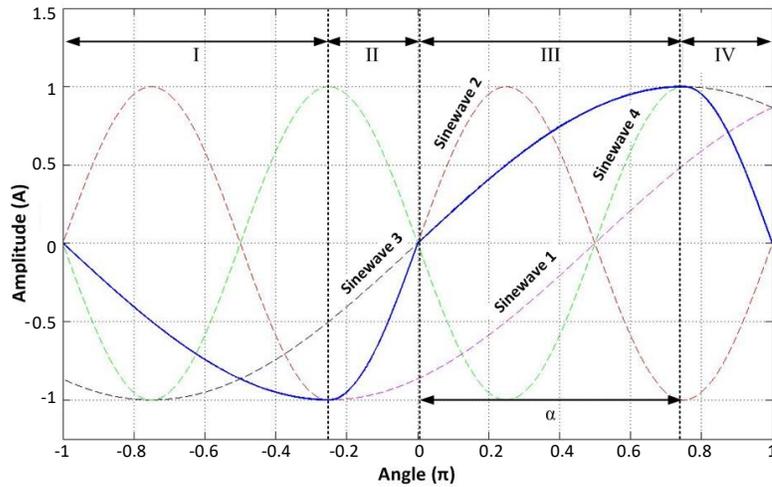


Figure 6-2. Proposed Quasi Sinusoidal Waveform.

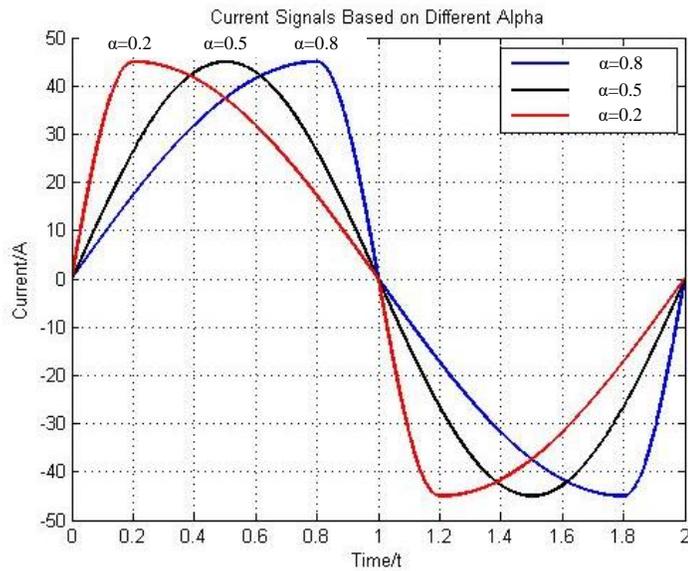


Figure 6-3. Quasi Sinusoidal Waveform with different  $\alpha$ .

### 6.3.2 Fourier Series of Quasi Sinusoidal Waveform

In order to determine the periodic signal function of the QSW, the method of Fourier series is used [6.21]. The current reference,  $i(t)$ , with QSW can be represented by the following equation,

$$i(t) = \sum_{n=1}^{\infty} (a_n \cos n\omega t + b_n \sin n\omega t) \quad (6-4)$$

where  $n$  is the number of harmonics of the current,  $\omega$  is the angular frequency, and

$$a_n = \frac{2A}{\pi} \cdot K_n \cdot [1 - 4n^2\alpha(\alpha - 1) - 2n \sin(\alpha n\pi)] \quad (6-5)$$

$$b_n = \frac{2A}{\pi} \cdot K_n \cdot 2n \cos(\alpha n\pi) \quad (6-6)$$

and  $K_n$  is,

$$K_n = \frac{[1 - (-1)^n] \cdot (2\alpha - 1)}{\{[2n(\alpha - 1)]^2 - 1\} \cdot [(2n\alpha)^2 - 1]} \quad (6-7)$$

A detailed derivation of (6-4) – (6-7) is given in the Appendix.

According to the questions,  $a_n$  and  $b_n$  are function of amplitude of QSW waveform,  $A$ , and the control coefficient,  $\alpha$ . Thus, the waveform can be adjusted by those two parameters.

A periodic signal can be expanded to a fundamental frequency and harmonics. The general form is represented by,

$$i(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta_n) \quad (6-8)$$

where  $I_n$  is magnitude and  $\theta_n$  is phase angle. The parameters can be determined by,

$$I_n = \sqrt{a_n^2 + b_n^2} \quad (6-9)$$

$$\theta_n = \tan^{-1} \left( \frac{a_n}{b_n} \right) \quad (6-10)$$

A detailed derivation of (6-9) – (6-10) is given in the Appendix.

By putting (6-5), (6-6) into (6-9) and (6-10),  $I_n$  and  $\theta_n$  can be expressed by  $A$  and  $\alpha$  as,

$$I_n = \frac{2A}{\pi} \cdot K_n \cdot \sqrt{[1 - 4n^2\alpha(\alpha - 1) - 2n \sin(\alpha n\pi)]^2 + [2n \cos(\alpha n\pi)]^2} \quad (6-11)$$

$$\theta_n = \tan^{-1} \left( \frac{1 - 4n^2\alpha(\alpha - 1) - 2n \sin(\alpha n\pi)}{2n \cos(\alpha n\pi)} \right) \quad (6-12)$$

All harmonic components can be determined based on (6-7), (6-11) and (6-12) by simply assigning values of  $n$ ,  $A$  and  $\alpha$ .

### 6.3.3 Electrical Performance Characteristics

Furthermore, Total Harmonic Distortion (THD), Power Factor (PF), Real Power (P) and Reactive Power (Q) can be determined based on the parameters of the fundamental component and harmonic components of the current reference.

#### A. Total Harmonic Distortion (THD) and Power Factor (PF)

The general equations for total harmonic distortion (THD) [6.22] and power factor (PF) [6.23] are,

$$THD = \frac{\sqrt{\sum_{n=3}^{\infty} I_n^2}}{I_1} \quad (6-13)$$

$$PF = \frac{1}{\sqrt{1+THD^2}} \cos \theta_1 \quad (6-14)$$

By putting (6-11) into (6-13), the THD equation can be rewritten as,

$$THD = \frac{\sqrt{\sum_{n=3}^{\infty} K_n^2 \{ [1-4n^2\alpha(\alpha-1) - 2n \sin(\alpha n\pi)]^2 + [2n \cos(\alpha n\pi)]^2 \}}}{K_1 \cdot \sqrt{[1-4\alpha(\alpha-1) - 2 \sin(\alpha\pi)]^2 + [2 \cos(\alpha\pi)]^2}} \quad (6-15)$$

where  $K_1$  is a term by assigning  $n = 1$  in (6-7).

According to (6-15), THD is independent of amplitude  $A$ . The THD variation with changing  $\alpha$  can be obtained and illustrated in Figure 6-4. It can be seen in Figure 6-4 that QSW gives the lowest THD (pure sine wave) when  $\alpha = 0.5$ . It increases propositionally when  $\alpha$  moves to left or right.

By putting equations (6-12) and (6-15) into (6-14), the PF equation can be rewritten as,

$$PF = \frac{4 \cdot \cos(\alpha\pi) \cdot \sqrt{\sum_{n=1}^{\infty} K_n^2 \{ [1-4n^2\alpha(\alpha-1) - 2n \sin(\alpha n\pi)]^2 + [2n \cos(\alpha n\pi)]^2 \}}}{[4(\alpha-1)^2 - 1] \cdot (2\alpha+1)} \quad (6-16)$$

Figure 6-5 illustrates the PF variation with changing  $\alpha$ . It can be seen that QSW gives  $PF = 1$  when  $\alpha = 0.5$ . It decreases when  $\alpha$  moves to left or right. And it can reach  $PF = 0.95$  when  $\alpha = 0.22$  or  $0.78$ .

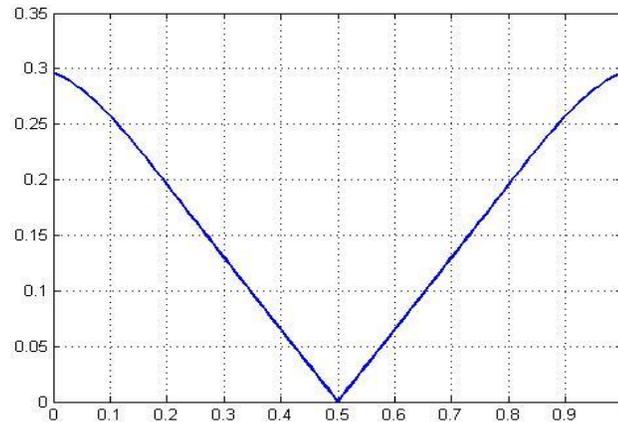


Figure 6-4. THD changes based on different  $\alpha$ .

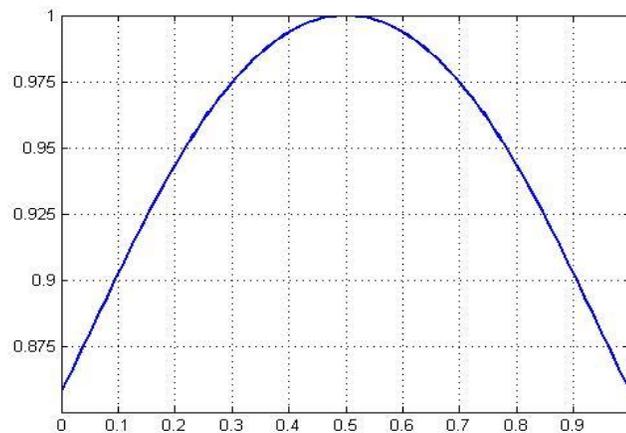


Figure 6-5. Power factor changes based on different  $\alpha$ .

### B. Real Power (P) and Reactive Power (Q)

Based on the power transfer theory, the real power is defined as,

$$P = \frac{V_s I_1}{2} \cos \theta_1 \quad (6-17)$$

By putting  $b_n$  in (6-6) with  $n = 1$  into (6-17), the relationship of  $b_n$  and the fundamental component is shown in (6-A8), the real power equation can be rewritten as,

$$P = \frac{2A}{\pi} \cdot \frac{2V_s \cdot \cos(\alpha\pi)}{[4(\alpha-1)^2-1] \cdot (2\alpha+1)} \quad (6-18)$$

Based on the power transfer theory, the reactive power is defined as,

$$Q = \frac{V_s I_1}{2} \sin \theta_1 \quad (6-19)$$

By putting  $a_n$  in (6-5) with  $n = 1$  into (6-19), the relationship of  $b_n$  and the fundamental component is shown in (6-A7), the reactive power equation can be rewritten as,

$$Q = \frac{2A}{\pi} \cdot \frac{V_s \cdot [1-4\alpha(\alpha-1)-2 \sin(\alpha\pi)]}{[4(\alpha-1)^2-1] \cdot (2\alpha+1)} \quad (6-20)$$

Based on (6-18) and (6-20), the steady-state characteristics of the real and the reactive powers can be obtained by putting the variables  $A$  and  $\alpha$ .

## 6.4 Benchmarking Similar Waveforms

In order to reduce THD while generating reactive power, three different types of waveform were analyzed and compared as shown in Figure 6-6. For Quasi Sinusoidal Waveform (QSW), we have discussed in detail before. The method for controlling reactive power is to insert a control factor  $\alpha$  that can shift the first order harmonic of the current signal by adjusting the shape slant. By using the same control technique, it might be also possible to use four parts of line segment or four parts of parabola to achieve that. (6-21) and (6-22) are equations for Parabola Combined Waveform and Line Segments Combined Waveform, respectively. Corresponding waveforms are shown in Figure 6-6.

Equations of Parabola Combined Waveform:

$$f(t) = \begin{cases} A \cdot \left\{ \frac{[t+(1-\alpha)\frac{T}{2}]^2}{(-\alpha\frac{T}{2})^2} - 1 \right\}, & -\frac{T}{2} \leq t < -(1-\alpha)\frac{T}{2} \\ A \cdot \left\{ \frac{[t+(1-\alpha)\frac{T}{2}]^2}{[(1-\alpha)\frac{T}{2}]^2} - 1 \right\}, & -(1-\alpha)\frac{T}{2} \leq t < 0 \\ A \cdot \left\{ 1 - \frac{[t-\alpha\frac{T}{2}]^2}{(-\alpha\frac{T}{2})^2} \right\}, & 0 \leq t < \alpha\frac{T}{2} \\ A \cdot \left\{ 1 - \frac{[t-\alpha\frac{T}{2}]^2}{[(1-\alpha)\frac{T}{2}]^2} \right\}, & \alpha\frac{T}{2} \leq t < \frac{T}{2} \end{cases} \quad (6-21)$$

Equations of Line Segments Combined Waveform:

$$f(t) = \begin{cases} -\frac{2A}{\alpha T}t - \frac{A}{\alpha}, & -\frac{T}{2} \leq t < -(1-\alpha)\frac{T}{2} \\ \frac{2A}{(1-\alpha)T}t, & -(1-\alpha)\frac{T}{2} \leq t < 0 \\ \frac{2A}{\alpha T}t, & 0 \leq t < \alpha\frac{T}{2} \\ -\frac{2A}{(1-\alpha)T}t + \frac{A}{1-\alpha}, & \alpha\frac{T}{2} \leq t < \frac{T}{2} \end{cases} \quad (6-22)$$

By using the same approach in Section II with the equations (6-4) - (6-20), the Steady-state characteristics of THD and PF can be determined for those two waveforms, Parabola Combined Waveform and Line Segments Combined Waveform, with different  $\alpha$ . Figure 6-6 shows the shape of those three benchmarked waveforms when all three waveforms have the same peak value,  $A$ , and control factor,  $\alpha$ . And it can be observed that the current value of QSW waveform is always in between another two waveforms beside the zero-crossing and the peak points. Figure 6-7 shows the  $\alpha$ -THD relationship of those three waveforms. It can be seen that, in the region near  $\alpha=0.5$ , QSW has a significant lower THD. It means that only QSW can generate pure sinusoidal waveform. Figure 6-8 shows the  $\alpha$ -PF relationship of the benchmarked waveforms. Though Line Segments Combined Waveform has a larger controllable PF range, it cannot reach PF=1.

The goal for this control technique is to achieve reactive power injection with relatively low THD. As shown in Figure 6-9, with same power factor, QSW signal always has the lowest THD

among those three waveforms. QSW also has advantage that the property of sinusoids is widely used in many phase control cases. QSW can achieve a THD of 0 and the PF can be controlled in a relatively big range from 0.86~1. Above all, the proposed waveform, Quasi Sinusoidal Waveform, has ability to shift phase of its first order harmonic with relatively low THD.

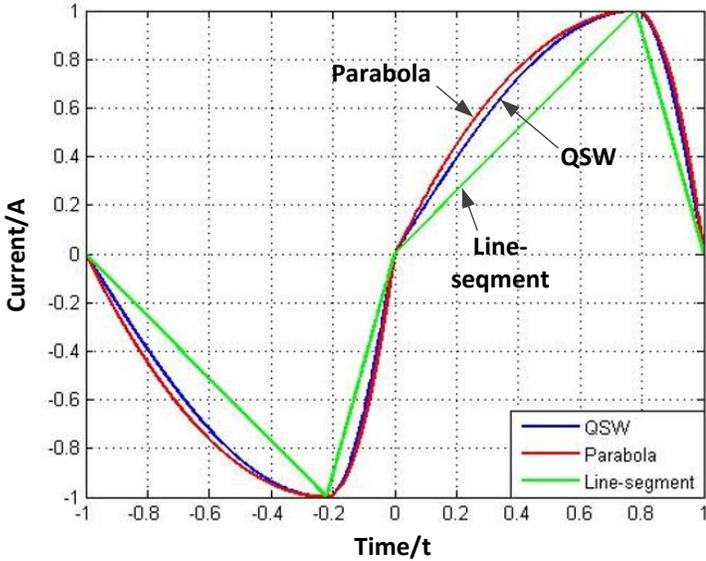


Figure 6-6. Comparison of three types of waveform.

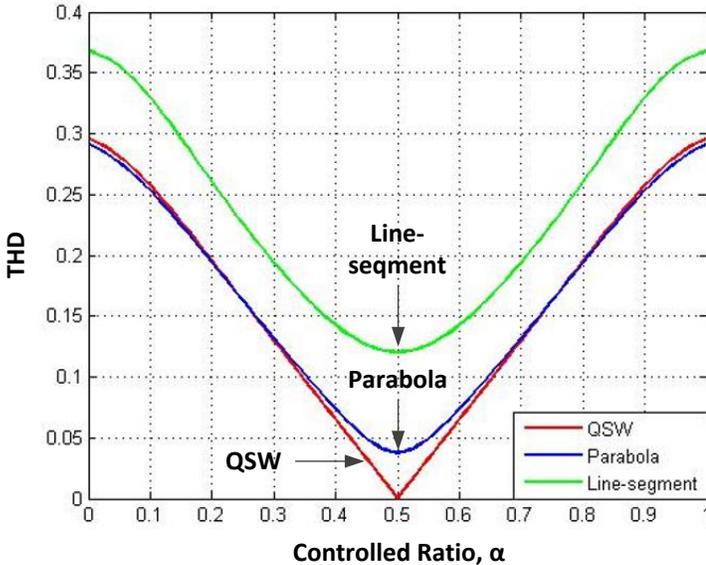


Figure 6-7. Comparison of THD relationships.

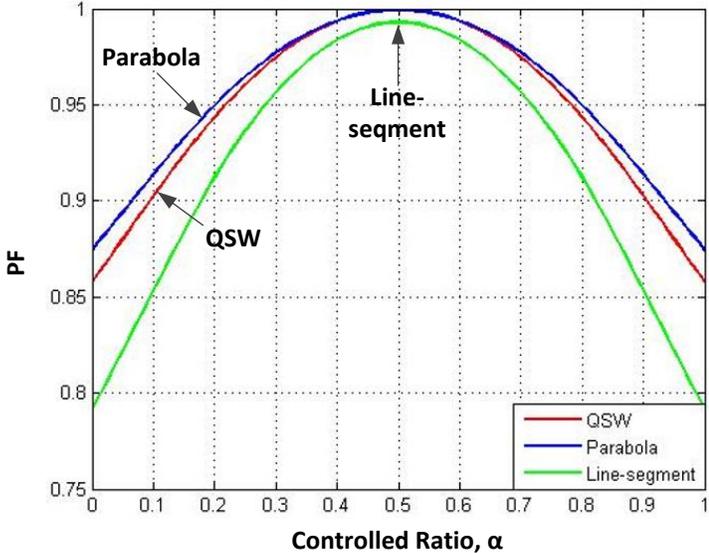


Figure 6-8. Comparison of power factor relationships.

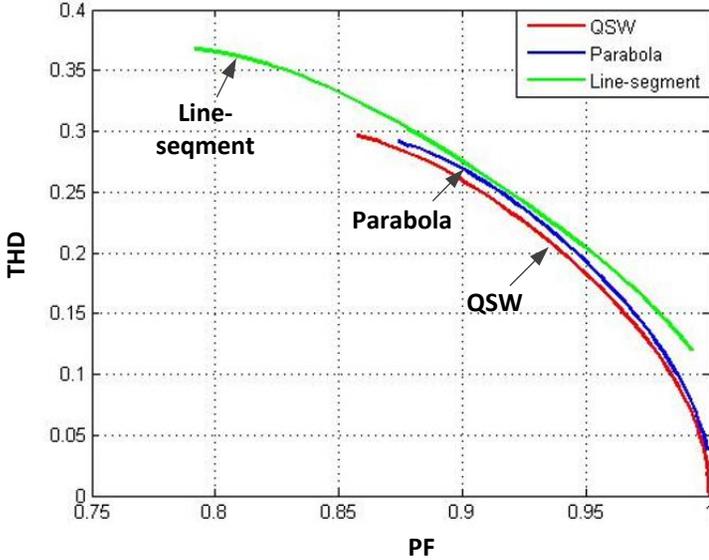


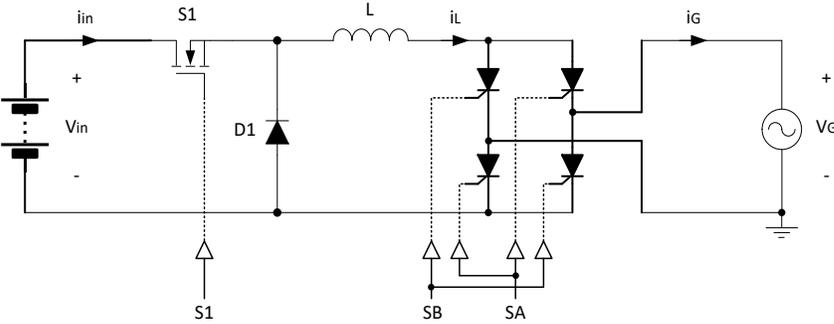
Figure 6-9. Comparison of THD&PF relationships.

## 6.5 Controller Design and Implementation

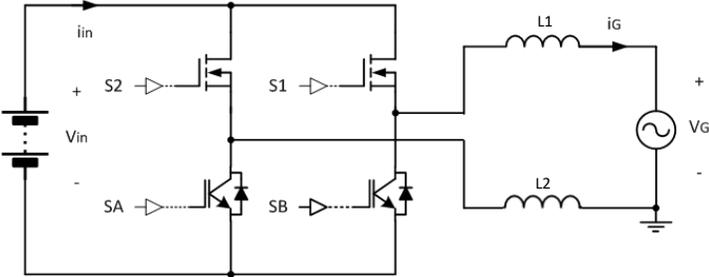
The concept of proposed control is to keep the zero crossing points of grid current and voltage to be the same, but shift the first order component of grid current to carry reactive power. The ideal grid current waveform was shown in Figure 6-2. Since the zero crossing points are the same as those of grid voltage, this same reference can be applied to various types of inverter to inject reactive power into the grid. Figure 6-10 (a) and (b) show two typical grid-tie inverters, an unfolding inverter and a unipolar switching full-bridge inverter [6.24], respectively. The typical gate signals of two converters are identical, SA and SB switch with the line frequency, e.g. 60 Hz, and S1 and S2 switch at a high frequency, e.g. 20 kHz, to shape the inductor current. It is well known that these inverters cannot deliver reactive power or generate considerably large switching losses under standard controllers. By using the proposed technique, these topologies do not require to change any hardware components. In fact, it is only required to add a current reference generator in the control loop to produce the QSW current reference.

Figure 6-11 (a) is a typical control diagram for inverters in Figure 6-10 with no reactive power control [6.25]. The current reference is given by a sinusoidal waveform which is generated by a Phase-Locked-Loop (PLL) with a synchronization of grid voltage, and sometimes the current reference is from sensed grid voltage directly. Figure 6-11 (b) shows the proposed controller block diagram, where QSW current reference generator has been introduced. The dash-line blocks illustrate the modifications of the original control loop. Firstly, a QSW reference generator replaces the simple sinusoidal wave generator. There are two parts in the generator, a sinusoidal wave generator and a controller to transform sinusoidal wave into the QSW. The sinusoidal wave generator gives a sinusoidal wave which is synchronized with the grid voltage through a PLL. Therefore, based on this synchronized signal, doing some transformation to generate QSW current

reference can promise the output QSW current well synchronized with the grid voltage. Secondly, as shown in blue block, for the feed-forward control, original grid voltage should also be processed to QSW shape.



(a)



(b)

Figure 6-10. Typical grid-tie inverter topologies: (a) unfolding inverter, and (b) unipolar switching full-bridge inverter.

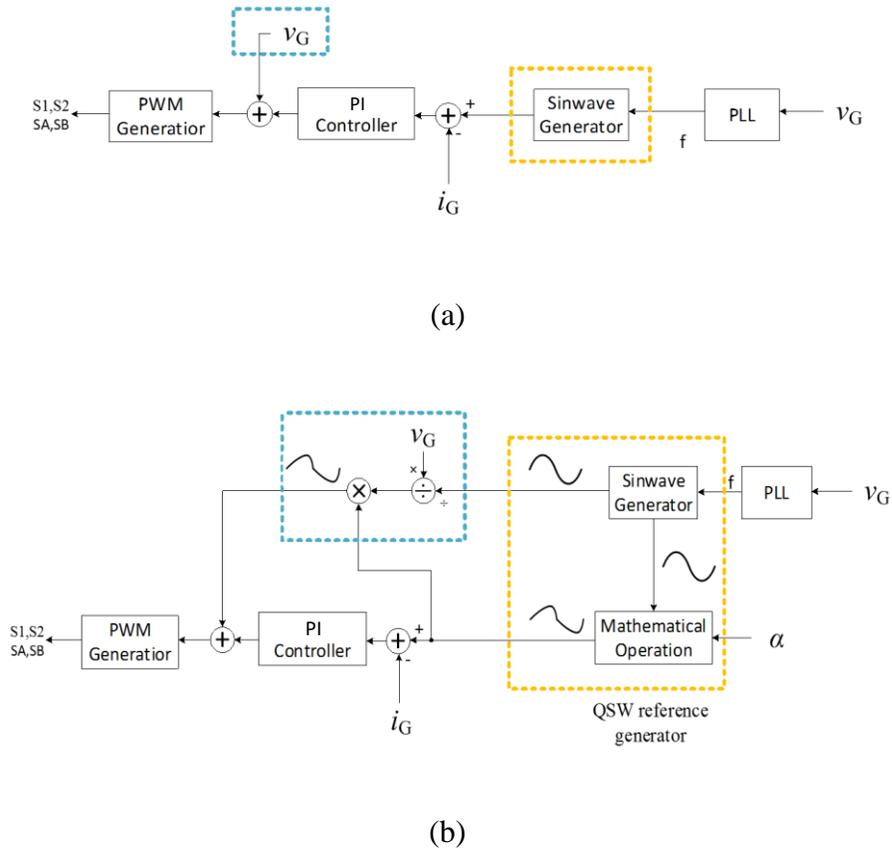


Figure 6-11. Control block diagrams: (a) A typical inverter controller, and (b) controller implementation to guarantee a QSW grid current.

The transformation from a pure sinusoidal wave to QSW only is a simple process. Firstly, based on the value and the slope of a sinusoidal wave, the phase information,  $\omega t$ , can be obtained by using inverse trigonometric computation. Then, the QSW reference value can be calculated using equation (1) with  $\omega t$ . Trigonometric and inverse trigonometric computation can be performed accurately and quickly by any DSP or micro-controller in real time.

The proposed control technique modified the current reference waveforms, which means it does not change anything in small signal analysis. Hence the design of PI controller in Figure 6-11 (b) can be kept as same as the original controller in Figure 6-11 (a).

## 6.6 Experimental Verification

The performance of the proposed controller has been experimentally demonstrated in a prototype of a full-bridge inverter. For the inverter system, a 800W/120V inverter was built, which is a full-bridge inverter with unipolar SPWM, controlled by a TI F28377s DSP. The inverter has the same topology as shown in Figure 6-10 (b). Table I shows the specification of this inverter. In the testbed, DC source voltage is set to be 380V as input voltage of the inverter, AC voltage source which represents grid to be 120V and the peak value of QSW current reference is set to be 9A. Figure 6-12 shows the connection diagram of experimental test setup and Figure 6-13 shows the actual testbed. Figure 6-14 shows the waveforms of grid current when  $\alpha$  is set at 0.22, 0.5 and 0.78.

TABLE 6-I SPECIFICATIONS

Parameter	Value	Parameter	Value
$V_G$	120V	$V_{DC}$	380V
$P_O$	800W	$f_{sw}$	20kHz
$L_1, L_2$	2.0mH		

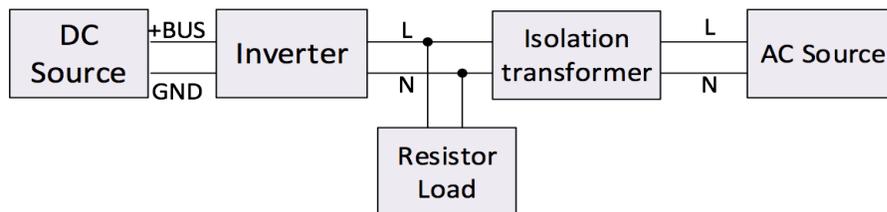


Figure 6-12. Experimental test connection diagram.

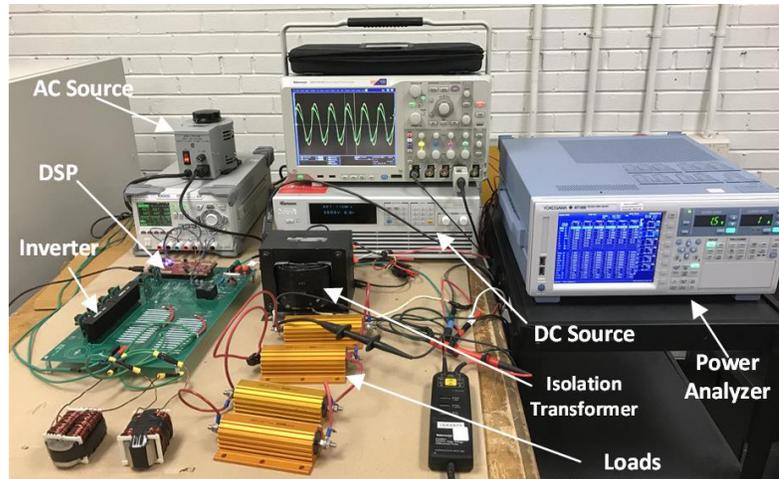
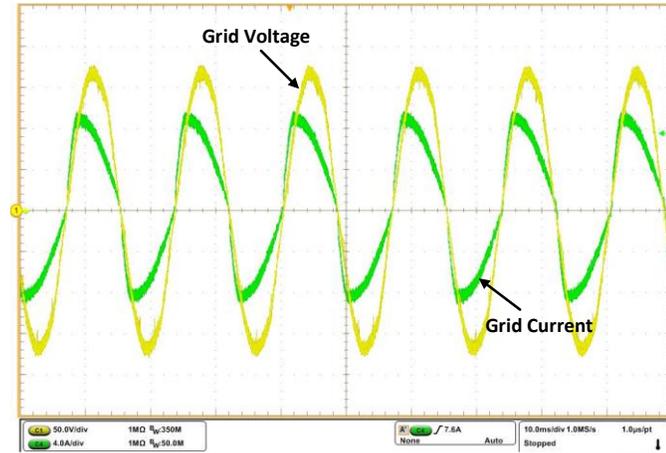
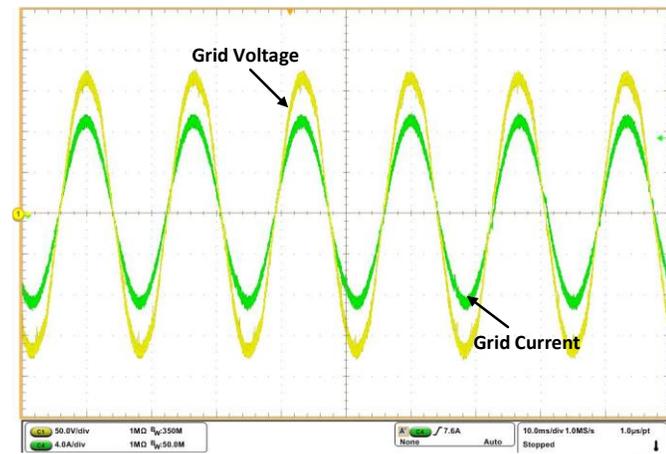


Figure 6-13. Experimental test setup.

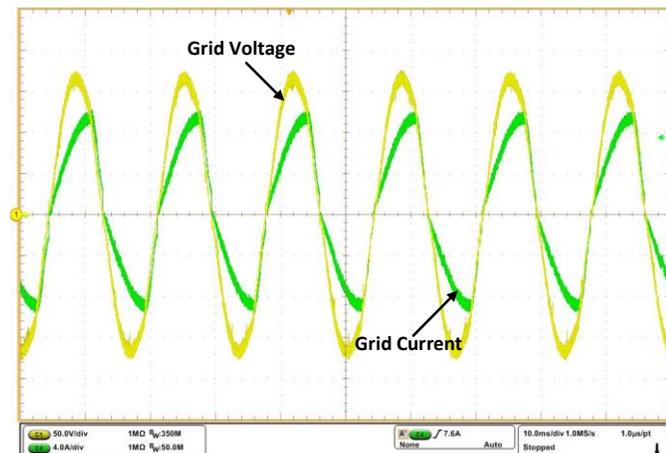
According to (6-16) and Figure 6-5, when  $\alpha$  is set to 0.22, 0.5 and 0.78, theoretically the power factor should be 0.95, 1.0 and 0.95, respectively. Table II shows the power parameters of corresponding waveforms in Figure 6-14 measured by a power analyzer. It shows that the measured power factors are very close to the theoretical results. This means that it is possible to generate reactive power using QSW current, and control the power factor by selecting different  $\alpha$  value. Besides the waveforms show that the proposed control method has the ability to produce an expected QSW current which is well synchronized to grid voltage, and the zero-crossing points of grid voltage and QSW current are accurately locked. This fact promises that the proposed technology can be applied on unfold inverters as shown in Figure 6-10.



(a)



(b)



(c)

Figure 6-14. Steady state responses of delivered grid current and grid voltage for different values of  $\alpha$ : (a)  $\alpha = 0.22$ , (b)  $\alpha = 0.5$ , and (c)  $\alpha = 0.78$ .

TABLE 6-II EXPERIMENTAL RESULTS

$\alpha$	Apparent Power $S$	Active Power $P$	Power Factor $\lambda$
0.22	756.4VA	718.3W	0.9492
0.50	757.1VA	755.2W	0.9982
0.78	767.2VA	732.0W	0.9534

Figure 6-15 shows the measured harmonic values compared with theoretical values. It can be seen that, when set  $\alpha = 0.5$ , the fundamental current is dominating in the frequency spectrum, it means it is very close to a pure sinusoidal wave. In contrast, when  $\alpha = 0.78$  or  $0.22$ , it contains extra 3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup> and 9<sup>th</sup> harmonics. Table III shows the comparison of measured harmonic RMS values and theoretical harmonic RMS values. According to the IEC61000-3-2 standard, all harmonic current amplitudes are within the limits. Furthermore, the comparison shows that experimental value is very close to theoretical value. For  $\alpha = 0.78$ , THD measured by power analyzer is 16.7%, which shows a good agreement with the theoretical value in Figure 6-4.

Figure 6-16 shows the transient characteristic of the inverter using proposed controller. At certain delay time after starting, current magnitude parameter changed from 4A to 9A. As shown, the transient happened near the current peak position which represents the worst case. However, the inverter returns to steady-state quickly with a slight overshoot, while the zero-crossing points are still accurately locked. It shows that the QSW method can be applied to low power or relatively higher power operating conditions and it does not affect the transient performance.

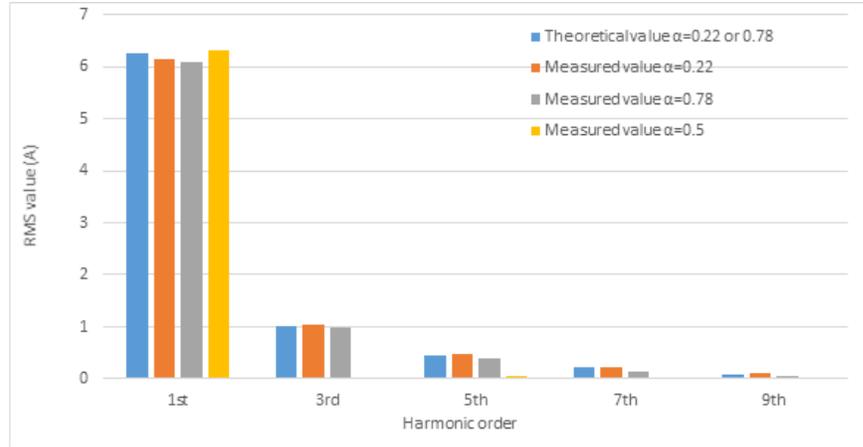


Figure 6-15. Harmonic analysis of test QSW current.

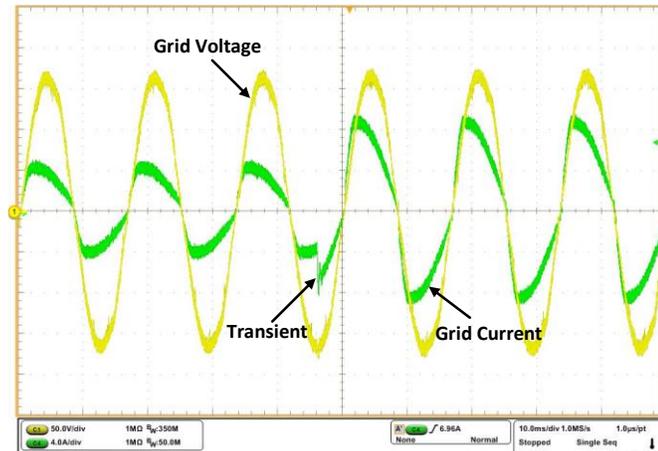


Figure 6-16. Transient characteristic when  $\alpha = 0.78$  and current magnitude changes from 4A to 9A.

TABLE 6-III COMPARISON OF HARMONIC MAGNITUDES

	1st	3rd	5th	7th	9th
Theoretical value (A) $\alpha = 0.22$ or $0.78$	6.260	1.015	0.459	0.221	0.095
Measured value (A) $\alpha = 0.22$	6.150	1.041	0.486	0.217	0.102
Measured value (A) $\alpha = 0.78$	6.309	0.976	0.391	0.141	0.051

## 6.7 Conclusion

This chapter presented a control technique for single phase grid-tie inverters. The control technique allows reactive power injection to unfolding and full bridge unipolar topologies, which were limited to unity power factor operation. The idea was to provide a Quasi Sinusoidal Waveform as a grid current reference to inject reactive power. The mathematical models were provided and explained. A prototype of a unipolar switching full-bridge inverter was built and evaluated for the QSW technique. Working principle of new controller was explained. By comparing measured values and theoretical values, experimental results showed a good agreement with the theory. It was shown that reactive power injection is possible by generating quasi sinusoidal waveform current through the inverter, without changing any hardware components.

## Appendix

### A. Derivation of (6-4) – (6-7):

The general equation of a Fourier series is,

$$f(t) = a_0 + \sum_{n=1}^{\infty} \left( a_n \cos \frac{2n\pi t}{T} + b_n \sin \frac{2n\pi t}{T} \right) \quad (6-A1)$$

By considering the function in (6-1) and Figure 6-2,  $a_0$  is equal to 0 due to no dc offset in the waveform, and

$$\begin{aligned}
a_n = \frac{A}{\pi} & \left[ - \int_{-\pi}^{-(1-\alpha)\pi} \sin \frac{\omega t + \pi}{2\alpha} \cdot \cos(n\omega t) \cdot d\omega t \right. \\
& + \int_{-(1-\alpha)\pi}^0 \sin \frac{\omega t}{2(1-\alpha)} \cdot \cos(n\omega t) \cdot d\omega t + \int_0^{\alpha\pi} \sin \frac{\omega t}{2\alpha} \cdot \cos(n\omega t) \cdot d\omega t \\
& \left. - \int_{\alpha\pi}^{\pi} \sin \frac{\omega t - \pi}{2(1-\alpha)} \cdot \cos(n\omega t) \cdot d\omega t \right]
\end{aligned} \tag{6-A2}$$

$$\begin{aligned}
b_n = \frac{A}{\pi} & \left[ - \int_{-\pi}^{-(1-\alpha)\pi} \sin \frac{\omega t + \pi}{2\alpha} \cdot \sin(n\omega t) \cdot d\omega t \right. \\
& + \int_{-(1-\alpha)\pi}^0 \sin \frac{\omega t}{2(1-\alpha)} \cdot \sin(n\omega t) \cdot d\omega t + \int_0^{\alpha\pi} \sin \frac{\omega t}{2\alpha} \cdot \sin(n\omega t) \cdot d\omega t \\
& \left. - \int_{\alpha\pi}^{\pi} \sin \frac{\omega t - \pi}{2(1-\alpha)} \cdot \sin(n\omega t) \cdot d\omega t \right]
\end{aligned} \tag{6-A3}$$

$a_n$  and  $b_n$  can be determined by simplifying (6-A2) and (6-A3), respectively. The resultant equations are as follows,

$$a_n = \frac{2A}{\pi} \cdot \frac{[1-(-1)^n] \cdot (2\alpha-1)}{\{[2n(\alpha-1)]^2-1\} \cdot [(2n\alpha)^2-1]} \cdot [1 - 4n^2\alpha(\alpha-1) - 2n \sin(\alpha n\pi)] \tag{6-A4}$$

$$b_n = \frac{2A}{\pi} \cdot \frac{[1-(-1)^n] \cdot (2\alpha-1)}{\{[2n(\alpha-1)]^2-1\} \cdot [(2n\alpha)^2-1]} \cdot 2n \cos(\alpha n\pi) \tag{6-A5}$$

By using (6-A1), (6-A4) and (6-A5), (6-4) – (6-7) can be obtained.

*B. Derivation of (6-9) – (6-10):*

By expanding (6-8),

$$i(t) = \sum_{n=1}^{\infty} I_n (\sin \theta_n \cos n\omega t + \cos \theta_n \sin n\omega t) \quad (6-A6)$$

By comparing (6-4) and (6-A6), two equations can be found as follows,

$$a_n = I_n \sin \theta_n \quad (6-A7)$$

$$\text{and} \quad b_n = I_n \cos \theta_n \quad (6-A8)$$

By solving (6-A7) and (6-A8), (6-9) and (6-10) can be obtained.

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# Chapter 7 Conclusion and Future Work

## 7.1 Conclusion

In this thesis, a comprehensive study was done on the advanced controls of power electronic modules in PV-based plug-n-play dc microgrid and its interface to ac grid. To overcome the drawbacks of conventional microgrids with central design, implementation and operation, concept of plug-n-play microgrid has been proposed by many researchers. Due to the limitation of control technologies, real plug-n-play is very hard to achieve in the past. This thesis proposes advanced control methods, with which a PV-based dc microgrid can be built with plug-n-play power electronic modules.

The application criteria of each power electronic converter in dc microgrid has been identified. To meet the different requirements, the control methods can be classified into two parts, for dc network and for dc-ac interface, separately. Dc bus voltage signaling technique is used for the dc network part. Mode adaption, power sharing, SoC balance can be achieved simultaneously in a fully decentralized manner. Master-slave control is used for dc-ac interface converter modules to guarantee a high performance. To keep high modularity and cost-effective in the design of dc-ac modules. Control methods to increase tolerability towards communication delay and new reactive power delivery method have been proposed. Hardware prototypes were built for each discussed converter to verify the proposed control methods experientially. All the performance metrics were met, and all the experimental results were consistent with the theoretical concepts.

## 7.2 Future Work

The work presented in this thesis can be extended. Several extensions and further studies based on this thesis can be explored as follows:

- A power flow controller based on per unit value of local bus voltage and public bus voltage can be studied and developed for gateway converters, and this method can be expanded to other multi-bus microgrids.
- Protection methods integrated to power electronic modules should be studied. The protection system should be able to cut the fault precisely and the rest of system could keep operating. The protection system should also be designed in a decentralized manner. The coordination of protection of each power electronic should be designed cooperatively.
- The design of power electronic converter modules can be further optimized. This thesis more focuses on control of power electronic converters. The hardware design of each converter can be further improved, in terms of topology, semiconductor combination, etc.
- The system level parameter can also be further optimized. The local bus and public bus voltage can be optimized considering cost, distribution loss and safety. The capacity of each PV unit and BES unit can be optimized to get lowest cost. The capacity of gateway converter can also be optimized considering the economic size of each dc microgrid cluster.