Reduced-Order Modeling of the Parallel Hybrid Modular Multilevel Converter

by

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Abstract

As the demand for electrical power continues to increase, so does the attractiveness of high voltage direct current (HVDC) transmission networks to transfer power from generating stations to load centers. Located at either end of the HVDC transmission network are converter stations that convert the AC power into DC power, and vice versa. A voltage source converter (VSC) commonly used in practice is the modular multilevel converter (MMC); however, these converters require many power electronic switches that will significantly increase the cost of such HVDC networks. A cost-effective alternative to these converters is the parallel hybrid MMC (PH-MMC), which is the focus of this thesis.

Modeling VSCs in large electrical networks can be a computational burden as a small time step is required to capture all of the switching transients of the VSC. In some situations, it may not be necessary to simulate every switching instant, and instead a reduced-order model can be utilized. The reduced order model of VSCs retain the behavior of the converters, while being able to run at a larger time step and at a much faster simulation runtime.

The basic principles of MMCs are first derived and the topological changes of the PH-MMC are analyzed. Comparisons between the PH-MMC and conventional MMCs are drawn to showcase the advantages and disadvantages of the PH-MMC. Control algorithms are described for basic operation of the PH-MMC, and control block diagrams are detailed to control the sub-module capacitor voltages as well as the AC terminal outputs. A qualitative fault analysis is provided for both AC and DC side faults, and a reduced-order model is developed to accurately model the PH-MMC in electromagnetic transient (EMT) studies by removing the need to model high frequency switching instants.

Using a simple network model and a more complex network model, dynamic simulations are performed in PSCAD™/EMTDC™ software to validate the reduced-order model against the full, detailed switching model. Simulation results show that the developed reduced-order model is an accurate representation of the PH-MMC, while significantly decreasing the runtime to carry out such simulations as compared to the detailed model. When incorporating PH-MMCs into larger networks, the reduced-order model developed in this thesis can be used to alleviate the computational burden of using a small time step while maintaining the low frequency behavior of the converter.

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Chapter 1 Introduction

1.1 Overview

This thesis discusses a new type of voltage source converter (VSC) known as the parallel hybrid modular multilevel converter (PH-MMC). As a variant to conventional modular multilevel converters (MMCs), the PH-MMC adopts many of the characteristics of conventional MMCs, including both aspects of its topology and its controllers. However, there are many differences that contribute to advantages and disadvantages of using PH-MMCs over conventional MMCs, which are thoroughly discussed in this thesis.

This thesis will also detail the process of developing a reduced-order electromagnetic transient (EMT) simulation model of the PH-MMC. This reduced-order model will greatly decrease the computational burden of simulation software, such as PSCAD^{TM}/EMTDC^{TM}, by removing the necessity of using very small time steps to accurately capture high frequency switching transients introduced by the PH-MMC.

1.2 Motivation

The demand for electrical power continues to grow at a high rate throughout the world [1]. Both developed countries and the developing ones are looking to provide safe and reliable energy to all of their citizens, and are continually looking for more cost effective and clean resources to generate electrical energy. Due to these reasons, electrical utilities are pushing for renewable energy (RE) sources, such as wind, solar, and hydroelectric power, to meet the growing demand [2].

However, such generating plants are generally located far away from load centers, and the electrical power needs to be transferred via high voltage transmission networks over long

distances. It is in these situations where high voltage direct current (HVDC) transmission networks are preferred over traditional high voltage alternating current (HVAC) transmission networks, as the construction of HVDC converters and HVDC transmission lines are more cost efficient over long distances as compared to constructing HVAC transmission lines over the same distance [3]. Technical problems with long-distance AC transmission, such as stability and reactive power compensation issues, also contribute to the merits of HVDC transmission over long distances.

In order to convert the DC power into AC power to be distributed among load centers, HVDC converters are required. The two types of converters commonly used for this purpose are line-commutated converters (LCCs) and voltage source converters (VSCs) [4]. One such type of VSCs are the popular modular multilevel converters (MMCs) [4]. MMCs offer a wide array of functionalities including controllable output active and reactive power, fault blocking, maintaining near-constant DC terminal voltage, and producing AC voltage/current waveforms with harmonics at high frequencies that are easier to filter out than low frequency harmonics, among others [4]. However, as technology and research continues to develop, engineers are continually looking for more cost-efficient converter designs without compromising the performance of existing converters. Such hybrid converters include the alternate arm converter [5], cascaded hybrid converters [6], [7], [8], MMCs incorporating different types of sub-modules [9][10], as well as the series hybrid converter [11].

One such new converter type is the parallel hybrid modular multilevel converter (PH-MMC) [12]. The PH-MMC offers a more cost efficient alternative to conventional MMCs, while bringing in a few disadvantages as well. However, as a new type of converter, not much research is available on this type of converter and, therefore, it is not yet used readily in the industry. This thesis aims

to help bridge the gap to show the potential in a PH-MMC as a viable converter topology while not shortcoming on any of its disadvantages.

In addition, as networks become larger, it becomes a larger computational burden to accurately model every component in an electrical network [13], [14]. When modeling VSCs that require very small simulation time steps to capture every switching transient, simulation runtimes become a burden on engineers who have to wait hours, if not longer, for such simulations to complete before results can be analyzed. For some studies, utilizing reduced order models is a much more convenient and time effective method to remove modeling switching transients that are not required for the specific study while maintaining the essential characteristics of the converters. This thesis details the derivation and validation of a PH-MMC reduced-order model that greatly reduces the computational burden of its simulation while not sacrificing the accuracy of representation of the dynamic behaviour of the converter.

1.3 Statement of the Problem

HVDC is the preferred method of transmission when sending a large amount of power over long distances [3]. A major contributor to the cost of HVDC networks are the converter stations. As a cost efficient alternative to other types of converters, the PH-MMC is analyzed for its merits and demerits against conventional MMCs [12].

When modeling VSCs in an EMT software, a small time step is required to simulate every switching transient of VSCs. However, when VSCs are incorporated into large electrical networks, it becomes a burden to engineers who may have to wait a long time for simulations to complete [13]. In studies where it is not necessary to model every switching transient, a reduced order model can be used instead that preserves the low-frequency characteristics of the converter while

decreasing the computational burden of modeling such converters by ignoring small-magnitude switching details. It is for these reasons that a reduced order model of the PH-MMC is developed and validated in this thesis.

1.4 Objectives

The objectives of this research are as follows:

- Describe the topology changes of the PH-MMC with respect to conventional MMCs
- Discuss the advantages and disadvantages of the PH-MMC over other types of converters
- Describe the controllers needed to operate the PH-MMC
- Analyze the capability of the PH-MMC in blocking both AC and DC faults
- Derive a reduced-order model of the PH-MMC
- Verify the operation of the reduced-order model with respect to the fully detailed switching model.

1.5 Contributions

The contributions of this research to the engineering community are as follows:

- Provide further insight into the validity of the PH-MMC as a cost efficient alternative in high voltage converter stations
- Discuss alternatives to using IGBTs to reduce number of switches required
- Provide a qualitative analysis of the PH-MMC during AC and DC faults
- Provide a reduced-order model that accurately represents the low-frequency behavior of the full, detailed PH-MMC model.

1.6 Thesis Outline

Chapter 2 details the topology and basic operation of conventional MMCs. This is followed by a description of the PH-MMC and the differences in topologies with conventional MMCs. Chapter 2 also describes the several control algorithms required to operate the internal switches to produce the desired output. A qualitative analysis is then provided on the capabilities of the PH-MMC to block AC and DC faults.

In Chapter 3, the reduced-order model of the PH-MMC is derived. The reduced-order model is then validated by comparing its dynamic response using EMT simulations to the full, detailed switching model of the PH-MMC. Two network models are considered: a simple network case with two AC infinite buses, and fully integrating the PH-MMC into the IEEE 12-bus system.

Chapter 4 summarizes the conclusions and contributions from this thesis. While highlighting the advantages of the PH-MMC over conventional MMCs, the challenges of operating PH-MMCs are discussed. In addition, the benefits and the shortcomings of using a reduced-order model of the PH-MMC in EMT studies as opposed to a detailed model are discussed. Potential work for future studies is also discussed in this chapter should further analysis of the PH-MMC continue.

Chapter 2 Parallel Hybrid Modular Multilevel Converter

The parallel hybrid modular multilevel converter (PH-MMC) is a variation of the MMC concept. Many of the design principles and concepts are adopted from the conventional half-bridge MMC, and therefore the conventional MMC is first described.

2.1 Principles of Modular Multilevel Converters

2.1.1 Topology Description

A conventional MMC is shown in Figure 2.1 [15].

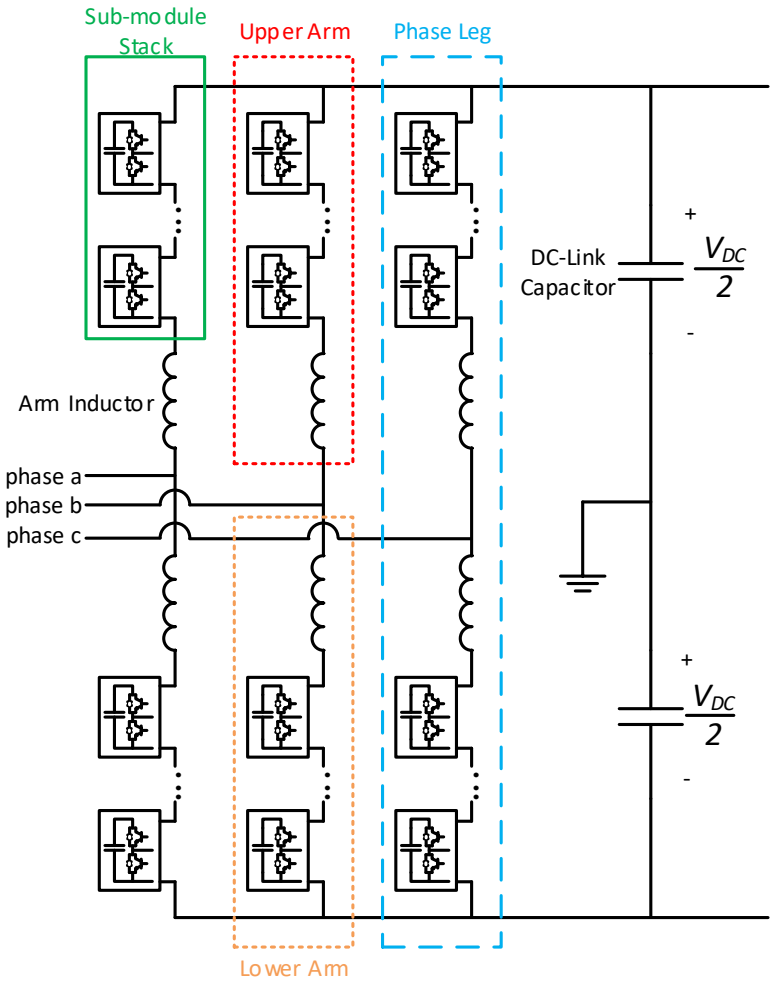

Figure 2.1: Conventional modular multilevel converter (MMC) topology.

A conventional MMC consists of three phase legs, with each phase leg consisting of an upper arm and a lower arm. Each arm consists of an arm inductor and a stack of sub-modules, as indicated in Figure 2.1. Power can be transferred either from the AC side to the DC side or from the DC side to the AC side by reversing the direction of the current.

Each sub-module contains a capacitor that is charged to a specific voltage and a number of switches [4]. The sub-module capacitors are then switched on (inserted) or off (bypassed) in order to create a voltage waveform at the AC terminal of the converter that closely resembles a sinusoid. The sub-modules of each phase are controlled accordingly to create balanced three-phase voltages at the AC terminals of the converter. The arm inductors are added to minimize circulating currents, to smooth out the AC current, and to limit the rate of rise of the fault current during a DC fault [16], [17]. Although not shown in the figure, a three-phase transformer may be required at the AC terminal in order to facilitate the control of AC voltage and power.

At any given time, the number of sub-modules (capacitors) inserted across each phase leg is always constant: whenever one sub-module is inserted in one arm, another sub-module in the second arm of the same phase leg is bypassed [4]. With each sub-module capacitor charged to the same voltage (in an average sense), the total voltage across the DC terminals remains essentially constant. The DC voltage is also maintained by the DC link capacitors, which are generally much larger than the sub-module capacitors. Since the total number of capacitors in each phase is essentially constant, the large DC link capacitors may be removed entirely.

2.1.2 Sub-Modules

Each sub-module contains a capacitor and switch combinations of an IGBT (or MOSFETs in lower voltage/low power applications) and a reverse diode in parallel. IGBTs are used in these applications over other power electronic switches as they are able to be switched on and off at very

high frequencies, which is necessary when crafting the sinusoidal voltage waveform [26]. The two types of sub-modules most commonly used are the half-bridge and the full-bridge, and both are shown in Figure 2.2 [4], [15].

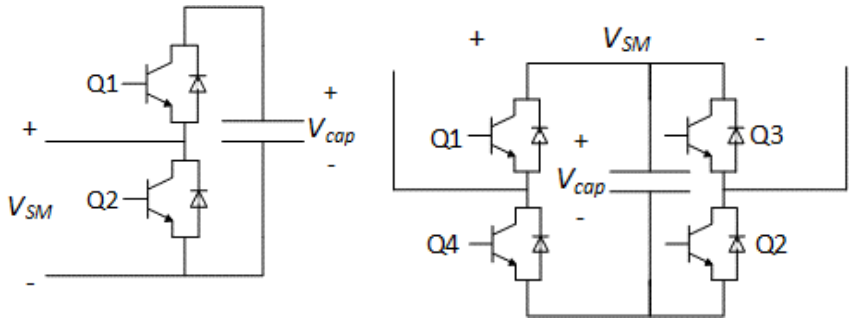

Figure 2.2: Half bridge (left) and full bridge (right) sub-modules.

The switch combinations used to generate different voltages across the sub-modules are shown in Table 2.1 [18].

Table 2.1: Sub-module control.

V_{SM}	Half-Bridge		Full-Bridge			
	Q1	**Q2**	**Q1**	**Q2**	**Q3**	**Q4**
$+V_{CAP}$	ON	OFF	ON	ON	OFF	OFF
0 V	OFF	ON	ON	OFF	ON	OF
			OFF	ON	OFF	ON
$-V_{CAP}$	not possible		OFF	OFF	ON	ON

The full-bridge sub-module offers more functionality since it is able to produce a negative voltage across its terminals, at the expense of requiring more switches that will add to the overall cost of the sub-module, as well as additional switching and conduction losses. While a negative voltage is not necessary in the normal operation of MMCs, full-bridge sub-modules are useful for protecting the equipment during DC faults [15], among other benefits. For the purpose of this thesis, only converters using half-bridge sub-modules are discussed for both the MMC and the PH-MMC.

2.1.3 AC and DC Voltage Calculations

As shown in Figure 2.1, if the total DC voltage is V_{DC}, then each DC link-capacitor is charged to $V_{DC}/2$. In order to produce the desired AC voltage, each sub-module capacitor is charged to a voltage given by

$$V_{SM,cap} = \frac{V_{DC}}{N_{SM}} \tag{2.1}$$

where N_{SM} is the number of sub-modules in each arm. Therefore, the maximum voltage that can be obtained across each sub-module stack is V_{DC}.

If the sub-modules in the upper and lower arm are controlled accordingly, a sinusoidal waveform can be obtained at the AC terminal of the converter. Figure 2.3 shows the corresponding waveforms of the upper arm and of the lower arm in order to obtain the sinusoidal waveform at the AC terminal.

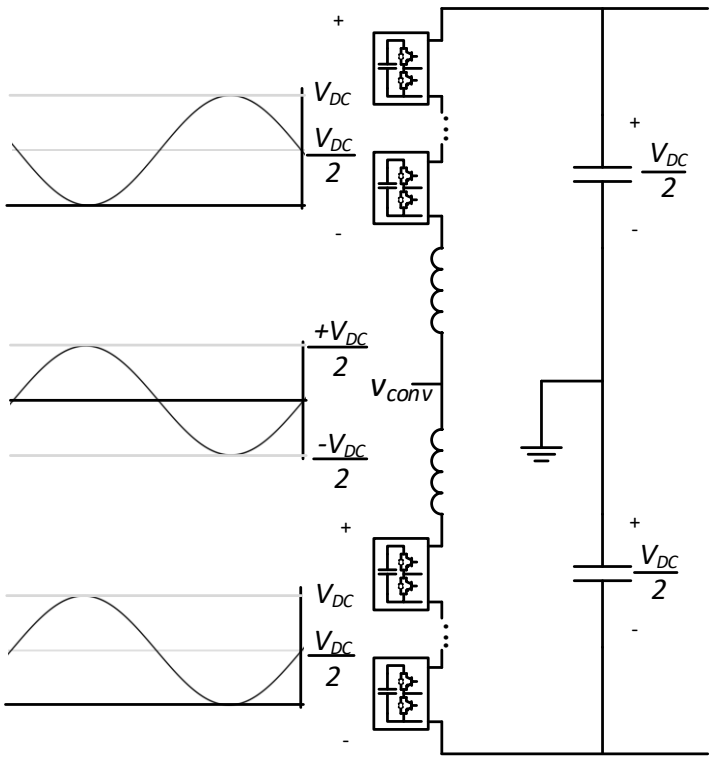

Figure 2.3: Sub-module stack and AC voltage waveforms of the MMC (one phase shown).

As shown in Figure 2.3, at the moment where all sub-modules are bypassed in the upper arm (i.e., 0 V across the upper arm), all sub-modules are inserted in the lower arm (i.e., $+V_{DC}$ across the lower arm) and the voltage at the AC terminal (v_{conv}) is $+V_{DC}/2$. Conversely, at the moment when all sub-modules are bypassed in the lower arm (i.e., 0 V across the lower arm), all sub-modules are inserted in the upper arm (i.e., $+V_{DC}$ across the upper arm) and the voltage at the AC terminal is $-V_{DC}/2$. Thus, the AC terminal voltage can be written as a function of the DC voltage and is given by

$$v_{conv}(t) = \frac{V_{DC}}{2}\sin(\omega t). \tag{2.2}$$

Alternatively, using the sub-module capacitor voltage, the AC voltage is given by

$$v_{conv}(t) = \frac{N_{SM}}{2}V_{SM,cap}\sin(\omega t). \tag{2.3}$$

It is important to note that an ideal sinusoidal AC voltage is impossible to obtain without an infinite number of sub-modules. Due to the finite number of sub-modules, the actual voltage at the AC terminal will be a stepped waveform. Special control algorithms of the sub-modules are utilized to obtain an AC waveform that closely resembles a sinusoid while minimizing harmonics. Such methods are described in Section 2.3.2.

It is also important to reiterate that the number of sub-modules inserted across a phase leg is always constant: if a sub-module is inserted in the upper arm, a sub-module is simultaneously bypassed in the lower arm (and vice versa). Therefore, at any given moment in time,

$$N_{SM} = N_{upper,inserted} + N_{lower,inserted} \tag{2.4}$$

must be true. Hence, the total number of sub-modules (per phase) required to craft the AC voltage in conventional MMCs is $N_{tot} = 2N_{SM}$.

2.2 Parallel Hybrid MMC

The parallel hybrid MMC (PH-MMC) was introduced as a cost efficient alternative to conventional MMCs by reducing losses and the number of sub-modules, and therefore the number of switches, for the same AC voltage profile [12], [19]. The PH-MMC gets its name as it consists of two switching stages comprised of different configurations of switches, and these two stages are connected in parallel. The PH-MMC topology is described in the Section 2.2.1.

2.2.1 Topology Changes

The PH-MMC topology is shown in Figure 2.4.

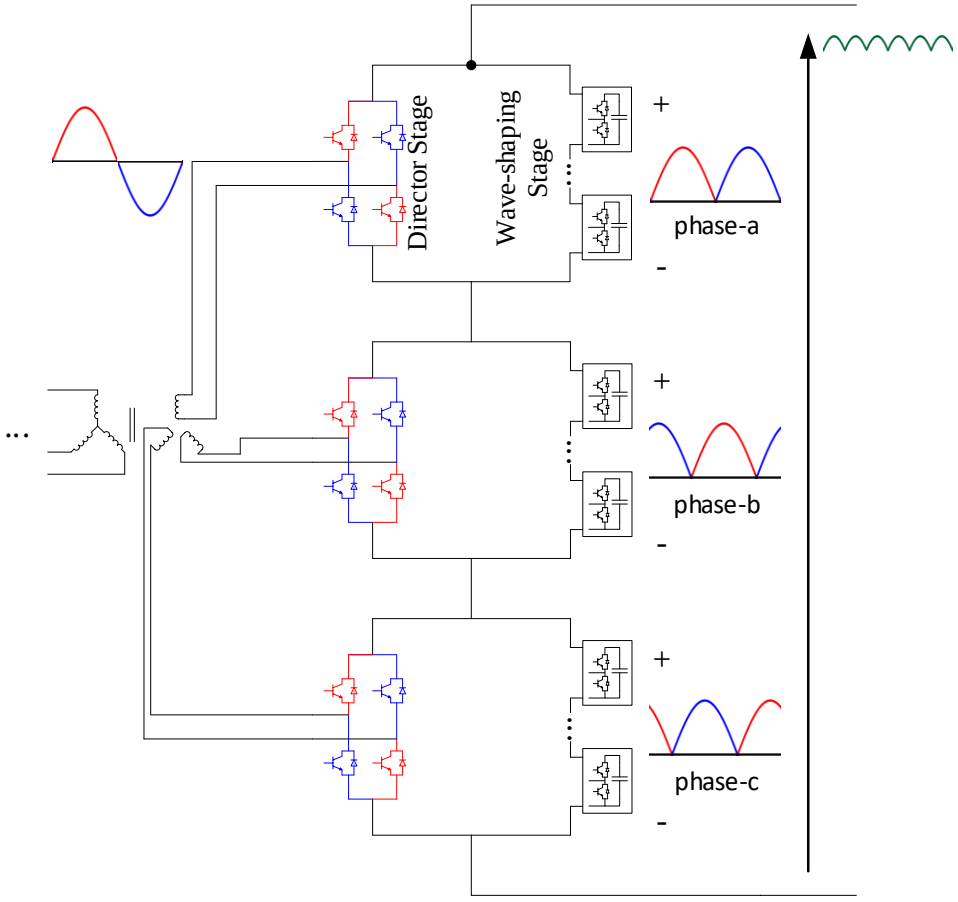

Figure 2.4: Parallel-hybrid modular multilevel converter (PH-MMC) topology.

The PH-MMC consists of two stages: the wave-shaping stage on the DC side of the converter, and the director stage on the AC-side. For each phase, these two stages are connected in parallel, and the phases are connected in series, or in a stack – contrary to conventional MMCs where the phase legs are connected in parallel. The wave-shaping stage consists of sub-modules that are controlled to produce a rectified sinusoidal waveform. The director stage is an H-bridge that is controlled to apply the appropriate polarity of the rectified sinusoid at the AC terminals to create an alternating sinusoidal waveform. Each phase requires its own single-phase transformer to connect the three phases to the AC network. Later in this thesis, the injection of a third-harmonic component will be introduced into the AC voltage. In order to prevent these harmonics from entering the AC grid, the connection of the windings on the AC grid side of the converter should be configured as a non-grounded wye-connection (as shown in Figure 2.4) or as a delta connection.

On the DC side of the converter, each phase produces a rectified sinusoid that is 120° shifted from the other two phases. When these individual waveforms are connected in series, the voltage across all three phases closely resembles the well-known Graetz Bridge's 6-pulse waveform, which contains a large DC component and $6n$ order harmonics.

The DC side can be grounded at the negative DC terminal, or the midpoint of the DC voltage can be grounded by using two DC link capacitors, similarly shown in Figure 2.1. However, due to the $6n$ order harmonics, the DC voltage is not maintained at a constant value, and therefore adding DC link capacitors at the terminal of the converter may cause the sub-module capacitor voltages to fluctuate resulting in larger harmonics in the AC voltage waveforms. This effect can be minimized by adding a smoothing inductor between the DC terminal of the converter and the DC link capacitors.

Similarly to conventional MMCs, PH-MMCs are bi-directional, i.e., power can be transferred from the DC network to the AC network, or vice versa, by reversing the current direction.

2.2.2 AC and DC Voltage Calculations

If each sub-module stack consists of N_{SM} sub-modules and each sub-module capacitor is charged to $V_{SM,cap}$, then the voltage across the stack of sub-modules is given by

$$v_{stack}(t) = V_{SM,cap} m N_{SM} |\sin(\omega t + \phi + \psi)| \tag{2.5}$$

where ϕ is 0°, +120° or -120° for phases a, b and c, respectively. These angles are with respect to the angle of the point of common coupling (PCC), typically located at the grid side of the AC transformers. The voltage angle at the PCC is obtained via a phase-locked loop (PLL).

The factor m (the modulation index) and the constant ψ (a phase shift) in (2.5) are set by controllers to control the AC terminal voltage (or reactive power) and the DC terminal voltage (or active power). These parameters are further discussed in Section 2.3.4.

The voltage at the AC terminal of the converter is therefore given by

$$v_{conv}(t) = V_{SM,cap} m N_{SM} \sin(\omega t + \phi + \psi). \tag{2.6}$$

The DC voltage is the sum of the three phase stacks, given by

$$\begin{aligned} v_{dc}(t) = V_{SM,cap} m N_{SM} (&|\sin(\omega t)| + |\sin(\omega t + 120°)| \\ &+ |\sin(\omega t - 120°)|). \end{aligned} \tag{2.7}$$

The DC component (average value) of the DC voltage of (2.7) is given by

$$V_{DC} = \frac{6}{\pi} V_{SM,cap} m N_{SM}. \tag{2.8}$$

Rearranging (2.8) for the sub-module capacitor voltage is given by

$$V_{SM,cap} = \frac{V_{DC}}{6/\pi \times m N_{SM}}. \tag{2.9}$$

It is important to note that these equations assume an ideal rectified sinusoid across the sub-module stacks, which cannot be true as there are only a finite number of sub-modules. Therefore, the AC voltage will be a stepped waveform similar to that of the conventional MMC, and the voltage across the stack of sub-modules will be a rectified stepped waveform. Hence, the number of sub-modules inserted across each sub-module stack will not be constant, and therefore the number of inserted sub-modules across the DC terminals will not be constant as was the case with the MMC. The implications of this will be further discussed in Section 2.3.5.

2.2.3 Advantages and Disadvantages

The main advantage of the PH-MMC over conventional MMCs is the reduced number of components. While MMCs require arm inductors, no such components are required for PH-MMCs. In addition, due to the two arms of conventional MMCs, the MMC requires double the number of sub-modules as compared to the PH-MMC to produce an AC sinusoid with the same number of discrete voltage levels. The PH-MMC does, however, require higher rated IGBT switches (or a large enough number of smaller rated switches in series) to be used in the H-bridge director stage in order to withstand the peak values of the AC voltage. While additional switches may be required, they are switched at near-zero voltage, and therefore they will have low switching losses [12]. Conversely, lower rated switches can be used in the sub-modules (wave-shaping stage) as compared to conventional MMCs since they are not in the main current path between the AC and DC networks.

An observation can be made that the H-bridge in the director-stage is similar in design to a full-wave single-phase thyristor-based rectifier. Thyristors can be rated for higher voltages as opposed to IGBT switches [26], and therefore fewer switches in series would be required. As will

be discussed in Section 2.3.3, normal thyristors cannot be used in the director stage; however, gate turn-off thyristors (GTOs) are a viable alternative to IGBTs.

A significant disadvantage of the PH-MMC is maintaining the DC voltage. In conventional MMCs, the constant number of inserted sub-modules in the phase leg (and the DC-link capacitors if included) maintain the DC voltage. However, for PH-MMCs, the number of inserted sub-modules across the DC terminals is not constant, which will cause the sub-module capacitors voltage to vary. A special DC voltage control algorithm needs to be implemented in order to maintain the DC voltage, and hence the sub-module capacitor voltages, at a constant value. This DC voltage controller is further discussed in Section 2.3.5.

Another disadvantage is that there is no common reference point for the AC phase voltages on the converter side of the AC transformer. Assuming that the ground reference is at the midpoint of the DC voltage (as is shown in Figure 2.1 for conventional MMCs), the insulation levels required for the AC output of one phase is dependent on the voltages of the other two phases and how the director stages are configured for that specific moment in time. Therefore careful consideration is required when designing the physical converter for real world applications.

2.3 Control of PH-MMC

2.3.1 Sub-Module Control

Up to this point, it was assumed that the voltage across the sub-module capacitors is constant; however, this is not inherently the case. Whenever a sub-module is inserted, current will flow through the sub-module capacitor: if the current is positive, the capacitor will charge and the voltage will increase; if the current is negative, the capacitor will discharge and the voltage will decrease. The sub-modules need to be operated in such a way that the voltage does not significantly

vary and each step in the AC waveform is essentially of the same magnitude. This will reduce the amount of harmonics in the voltage waveform and produce a better AC voltage profile. A process known as ‘voltage balancing’ is implemented [20].

Voltage balancing is a technique used to ensure that all sub-module capacitors have the same voltages. The balancing algorithm first orders the sub-modules based on the measured capacitor voltages. Then, depending on the direction of the measured current through the sub-modules, the algorithm determines which sub-modules are to be inserted. The half-bridge sub-module is shown in Figure 2.5.

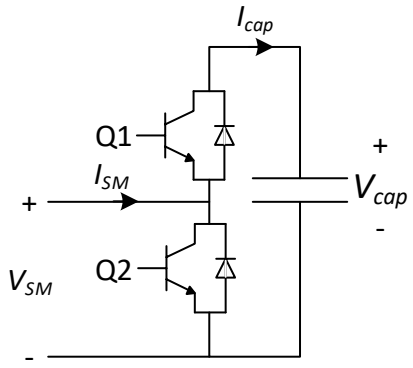

Figure 2.5: Half bridge sub-module.

If the measured current I_{SM} (and hence I_{cap}) is positive, the sub-modules with the lowest capacitor voltages are inserted in order to increase their voltages; if the measured current is negative, the sub-modules with the largest capacitor voltages are inserted in order to decrease their voltages. While voltage balancing is used to have a common voltage across all sub-module capacitors, it does not control what the specific voltage the capacitors are charged to. In other words, balancing does not automatically result in correct voltage regulation.

Careful design considerations are required to effectively control the sub-module capacitor voltages based on voltage balancing. Switching too frequently may produce extra switching losses, while not switching often enough can cause significant drifts in the capacitor voltages and therefore cause distorted AC waveforms with larger harmonics.

One of the simplest methods for ordering the sub-modules is the 'bubble-sort' method [21]. This method orders the sub-modules by compiling the capacitor voltages into a single list, and comparing each element (voltage) with the next in the list: if the next element is greater, then the two elements are swapped; otherwise, no operation is performed. This process is done iteratively throughout the whole list and is repeated until all elements/voltages are ordered, from the smallest to the largest. A simple example of the bubble sort method is shown in Table 2.2 (note: this method can also order the voltages from largest to smallest).

Table 2.2: Simple bubble sort example (smallets to largest)

	Number List				**Operation**
Orig. list:	5	10	8	2	None
Step 1:	5	10	8	2	Swap
Step 2:	5	8	10	2	Swap
Step 3:	5	8	2	10	None
Step 4:	5	8	2	10	Swap
Step 5:	5	2	8	10	None
Step 6:	5	2	8	10	Swap
Step 7:	2	5	8	10	None
Step 8:	2	5	8	10	None

The operation complexity of this method is $O(n^2)$, where n corresponds to the number of items in the list [21]. Other methods may be used to decrease the operation complexity and reduce the number of required computations.

When performing the sorting algorithm, the controller needs to keep track of which measurement belongs to which sub-module. After the sorting is completed, the controller will be able to identify the sub-modules that have the smallest and largest capacitor voltages.

The voltage balancing and sorting algorithms of the sub-module stacks are carried out independently by phase. This is because the current flowing through the sub-module stacks is different between phases, and the number of sub-modules to be inserted is also different between phases.

2.3.2 Sub-Module Stack Control

In order to create a waveform that resembles an AC sinusoid, the sub-modules in the wave-shaping stage are switched in and out (inserted and bypassed). However, since there is a finite number of sub-modules, obtaining a perfect sinusoid is not possible. There are a variety of different discretized waveforms that could be produced that closely resemble a sinusoid, each with different harmonic components.

The simplest method is called Nearest Level Control (NLC) [22]. First, a reference waveform (a sinusoid) is produced using the number of sub-modules in each stack N_{SM}, the modulation index m, and a phase shift $\phi + \psi$, as shown in (2.10)

$$ref(t) = mN_{SM} \sin(\omega t + \phi + \psi) \tag{2.10}$$

Next, each point in the reference waveform is rounded to the nearest integer, which corresponds to the number of sub-modules needed to be inserted in the sub-module stack. An example of a waveform obtained through NLC is shown in Figure 2.6.

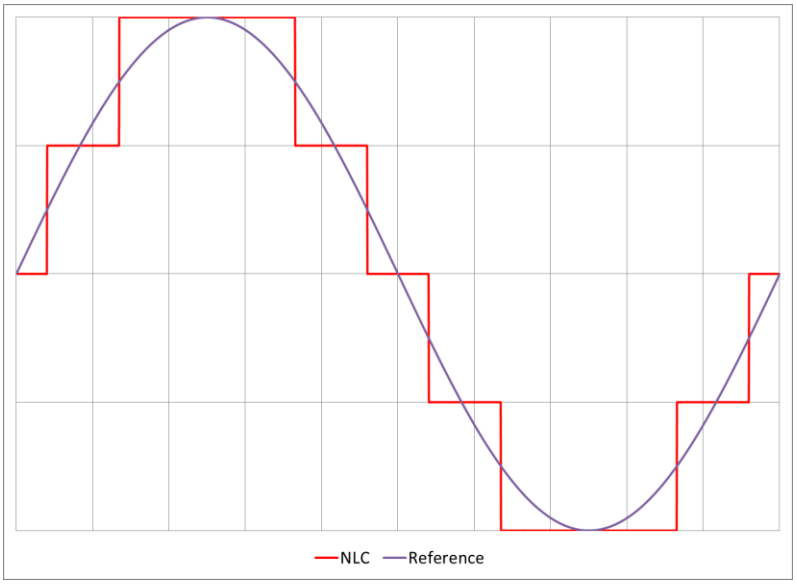

Figure 2.6: Nearest level control (NLC) discretized sinusoid waveform (N = 2, m = 1).

Although the general shape of a sinusoid is obtained, this method introduces many harmonics, specifically low-order harmonics, which may be difficult to filter out. NLC works best when the number of sub-modules is sufficiently large.

In order to reduce the low-order harmonics without requiring a large number of sub-modules, pulse-width modulation (PWM) techniques are implemented. The principle behind PWM is to compare a carrier waveform to the reference waveform and perform sub-module switchings where the waveforms intersect. This will greatly improve the profile of the AC voltage, but will add more switching losses.

The PWM method implemented in this thesis is the level-shifted carrier PWM (LSC-PWM) method [23]. The carrier waveform is a triangular waveform and has a frequency much larger than the reference waveform. The frequency modulation, which is the ratio between the carrier waveform frequency and the reference waveform frequency, is selected to be an odd number (in order to not introduce even-numbered harmonics) and a multiple of 3 (in order for harmonics of

multiples of three to be removed in the line voltages/currents). For the reference waveform in (2.10), the peak-peak magnitude of the carrier is set to 1, and therefore the carrier can be shifted $2N_{SM}$ times to cover the entire range of the reference waveform. Each level shifted carrier can be phase shifted to obtain different harmonic performance [24]. The specific method used in this thesis, where all carriers are in phase with one another, is known as phase disposition PWM (PD-PWM) [23][24].

The same reference waveform in (2.10) is then compared to the carrier waveform: if the reference waveform is greater than the carrier waveform, then the reference waveform is rounded up to the nearest integer; if the reference waveform is less than the carrier waveform, then the reference waveform is rounded down. This rounded integer corresponds to the number of sub-modules to be inserted. An example of this PWM technique using a frequency modulation of 15 is shown in Figure 2.7.

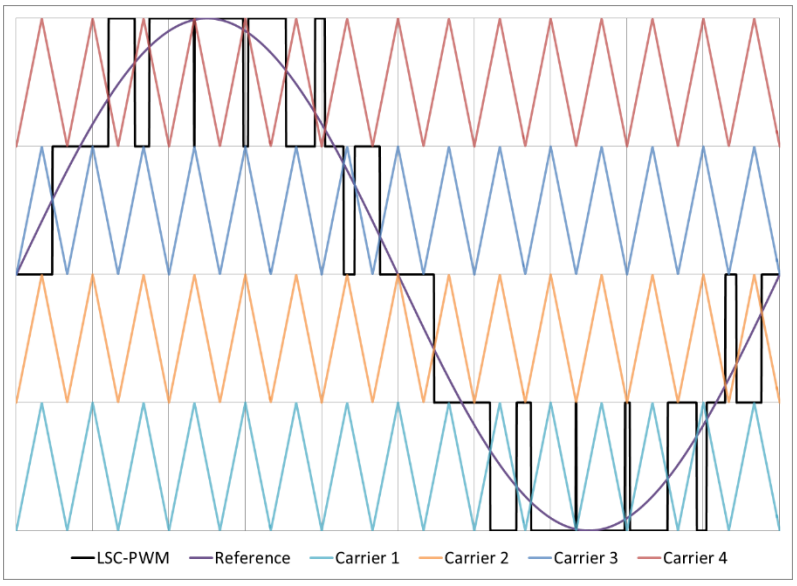

Figure 2.7: Level shifted carrier PWM (LSC-PWM) discretized waveform (N = 2, m = 1, f_m = 15).

Using this method will produce only odd harmonics, with a large frequency component located at the carrier frequency. A higher frequency modulation will push the harmonics to higher frequencies, but will add more switching losses.

It is important to note that although the wave-shaping stages generate a voltage resembling a rectified sinusoid, the reference waveform for the sub-module stack control should be a non-rectified sinusoidal waveform in order to not introduce even-numbered harmonics (since a rectified sinusoid will have double the frequency of the non-rectified sinusoid, *2n* harmonics will be passed into the wave-shaping voltage). Only after obtaining the discretized waveform should the resulting waveform be rectified to obtain the number of sub-modules that need to be inserted.

2.3.3 H-Bridge Control

The H-bridges of the PH-MMC are operated in a much simpler way than the sub-modules. Since the H-bridges contain the director switches, their purpose is to apply the appropriate polarity of the voltage generated by the sub-modules to the AC terminals of the converter. This can be obtained using IGBT switches, similarly to the sub-modules. The corresponding switches to turn on and off to obtain positive and negative voltages at the AC terminals are indicated by a color scheme in Figure 2.8 and in Table 2.3.

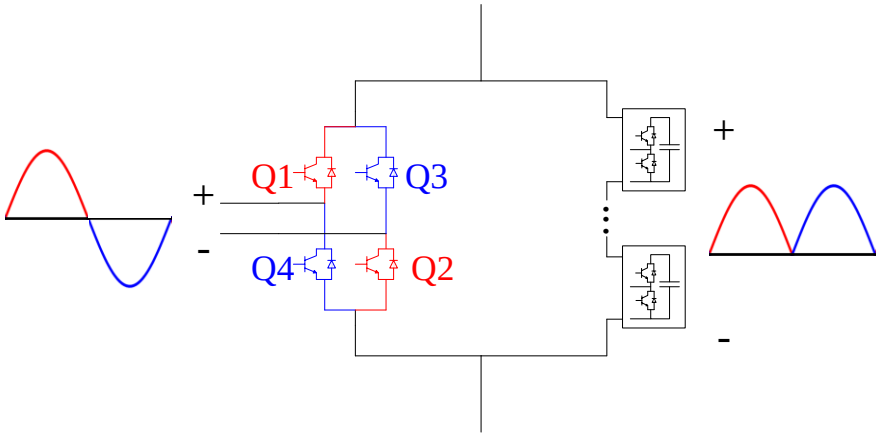

Figure 2.8: Director stage switching.

Table 2.3: Director stage switching of H-bridge.

AC Voltage	Q1	Q2	Q3	Q4
> 0 V	ON	ON	OFF	OFF
< 0 V	OFF	OFF	ON	ON

Note that the switching events occur when the voltage of the wave-shaping stage is 0 V. The timings of these switching events will be shifted ±120° between phases a, b and c.

The waveforms shown in Figure 2.8 are reminiscent of the waveforms obtained in a single-phase full wave rectifier, which uses thyristors instead of IGBT switches. A single-phase full wave rectifier is shown in Figure 2.9 (with power being transferred from the AC side to the DC side) [25].

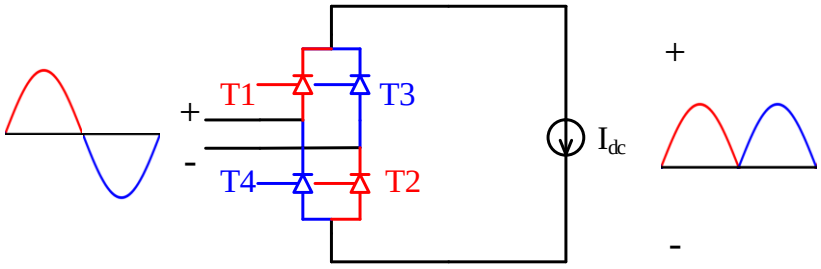

Figure 2.9: Single-phase full wave rectifier (firing angle of thyristors = 0°).

The operation of thyristors are much different than IGBTs, in the sense that thyristors are semi-controllable switches: they can be switched on but cannot be switched off. Thyristors will only conduct current if a firing pulse is sent to the switch when the thyristor is positively biased (voltage across its terminals is positive) and they will stop conducting current if the thyristor becomes negatively biased (voltage across its terminals is negative). The reason why thyristors will not work in place of IGBTs is best shown in an example, as shown in the single-phase PH-MMC in Figure 2.10. Each switch (QX) is comprised of a thyristor TX and a reverse diode DX.

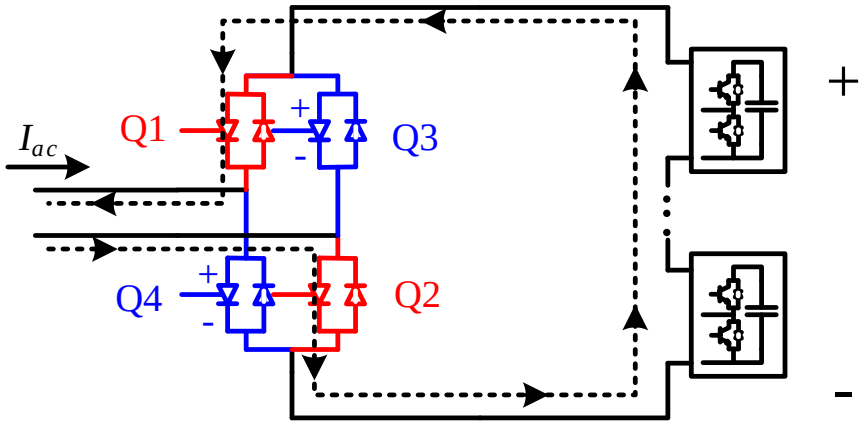

Figure 2.10: Director stage using thyristors: negative Iac current flow

In this analysis, it will be assumed that thyristors T1 and T2 were previously switched on and thyristors T3 and T4 were previously switched off. If I_{ac} in Figure 2.10 is negative, T1 and T2 will be conducting current (as shown by the dotted line), and T3 and T4 will be positively biased. If a firing pulse is sent to T3 and T4, these switches will turn on, and current will begin to flow through these thyristors. However, T1 and T2 will still be positively biased, and therefore will not switch off. With all four thyristors switched on at the same time, a short is created with the wave-shaping stage that will discharge all sub-module capacitors, bringing their voltage and the total DC voltage to zero.

This can be avoided by using gate turn-off thyristors (GTOs) instead of normal thyristors. By using GTOs, T1 and T2 can be forced switched off at the same time when T3 and T4 are switched on, and therefore not shorting out the sub-module capacitors. Hence, either GTOs or IGBTs can be used in the director stage. Using GTOs will be beneficial over IGBTs due to their capability to withstand higher voltages [26]. In addition, since the director switches are switched on or off once every period (50 or 60 Hz) and the switching instances occur at the zero-crossings of the wave-shaping stage voltage, the probability of commutation failure when using GTOs is low.

2.3.4 Decoupled Control

The output AC active and reactive power can be controlled by changing the angle and magnitude of the voltage on the converter side of the transformers, respectively. A simple single line diagram of the converter transformer is shown in Figure 2.11.

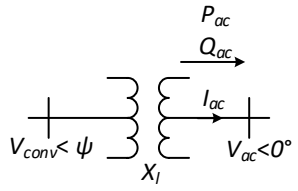

Figure 2.11: Simplified diagram of AC terminal connected to a grid.

The phasor representation of the apparent power on the grid side of the transformer can be calculated by

$$\overrightarrow{S_{ac}} = P_{ac} + jQ_{ac} = \overrightarrow{V_{ac}}\overrightarrow{I_{ac}} \tag{2.11}$$

where $\overrightarrow{I_{ac}}$ is the complex conjugate of the AC current on the grid side of the converter and j is the imaginary number $\sqrt{-1}$. Considering only the transformer leakage reactance, the power can be calculated as

$$P_{ac} + jQ_{ac} = \overrightarrow{V_{ac}}\overline{\left(\frac{\overrightarrow{V_{conv}} - \overrightarrow{V_{ac}}}{jX_l}\right)}. \tag{2.12}$$

Separating the real and imaginary parts of the above equation, the active power can be calculated by

$$P_{ac} = \frac{v_{conv}v_{ac}}{X_l}\sin(\psi) \tag{2.13}$$

and the reactive power at the grid side of the transformer can be calculated by

$$Q_{ac} = \frac{v_{conv}v_{ac}}{X_l}\cos(\psi) - \frac{v_{ac}^2}{X_l}. \tag{2.14}$$

It can be shown that changes in the converter voltage angle, ψ, have a greater effect on the active power and changes in the converter voltage magnitude, V_{conv}, have a greater effect on the reactive power. Therefore, simple proportional-integral (PI) controllers can be used to match the output active and reactive powers to a reference, as shown in Figure 2.12.

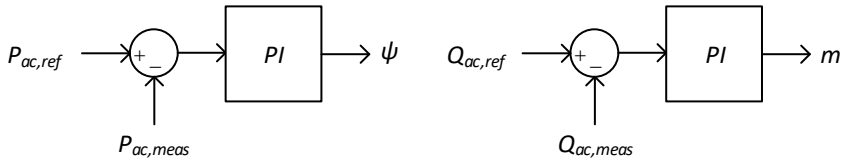

Figure 2.12: Simple PI controllers for controlling output active and reactive power.

In order to make these changes, a phase shift and a modulation index are added to the reference waveform, and is shown in (2.15).

$$ref(t) = mN_{SM}\sin(\omega t + \phi + \psi) \tag{2.15}$$

where m is the modulation index and ψ is the phase shift with respect to the grid voltage. Note that for modulation indices greater than 1, the voltage across the stack of sub-modules will begin to saturate (as there are only N_{SM} sub-modules). The phase shift also needs to be incorporated in the switching of the director switches in the H-bridges to ensure the director switches are switched when the sub-module stack voltage is 0 V.

As indicated in (2.13) and (2.14), the active and reactive powers are both dependent on the converter voltage magnitude and phase angle, and therefore making the change to one reference will impact the other quantity. While not ideal, a decoupled controller allows the change of one reference with little impact on the other quantity.

A decoupled controller is derived from converting the phase a, b and c voltages/currents to a dq0 rotating reference plane using Park's transformation [27]. This converts the time-varying (sinusoidal) quantities into constant values that will allow for easier control. The equations of Park's transformation are

$$\begin{bmatrix} x_q(t) \\ x_d(t) \\ x_0(t) \end{bmatrix} = K(\theta) \begin{bmatrix} x_a(t) \\ x_b(t) \\ x_c(t) \end{bmatrix} \tag{2.16}$$

and

$$K(\theta) = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - 2\pi/3) & \cos(\theta + 2\pi/3) \\ \sin(\theta) & \sin(\theta - 2\pi/3) & \sin(\theta + 2\pi/3) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{2.17}$$

where *x* can be any AC voltage or current and θ is the angle between the 'phase a' reference and the rotating q-axis. A graphical representation is shown in Figure 2.13.

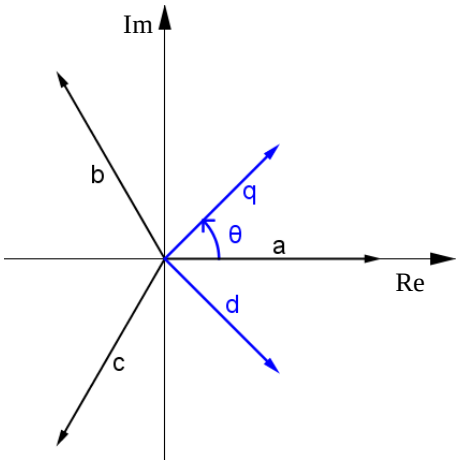

Figure 2.13: Relationship between abc-reference plane and rotating qd0-reference plane.

Taking the time-derivative of the equations of the circuit shown in Figure 2.11, the converter voltage can be calculated as

$$v_{conv,abc}(t) = L_l \frac{d}{dt} i_{ac,abc}(t) + v_{ac,abc}(t). \tag{2.18}$$

Applying Park's transformation, the qd components of the converter voltage can be calculated as

$$v_{conv,qd0}(t) = K(\theta) L_l \frac{d}{dt} \left(K^{-1}(\theta) i_{ac,qd0}(t) \right) + v_{ac,qd0}(t). \tag{2.19}$$

Simplifying and separating the q and d components of the converter voltage results in

$$v_{conv,q}(t) = \omega L_l i_d(t) + L_l \frac{d}{dt} i_q(t) + v_{ac,q}(t) \tag{2.20}$$

and

$$v_{conv,d}(t) = -\omega L_l i_q(t) + L_l \frac{d}{dt} i_d(t) + v_{ac,d}(t) \tag{2.21}$$

where

$$\omega = \frac{d\theta}{dt}. \tag{2.22}$$

For a balanced three-phase system, the 0-axis components are equal to zero.

If the grid voltage $v_{ac}(t)$ is given by

$$v_{ac}(t) = \begin{bmatrix} V_{ac} \sin(\omega_0 t) \\ V_{ac} \sin(\omega_0 t - 2\pi/3) \\ V_{ac} \sin(\omega_0 t + 2\pi/3) \end{bmatrix} \tag{2.23}$$

and we set

$$\omega = \omega_0 \tag{2.24}$$

where ω_0 is the (angular) frequency of the network (i.e. the d/q-axes rotate 360º at the same frequency of the network), then the d-axis component of the grid voltage is

$$v_{ac,d}(t) = V_{ac} \tag{2.25}$$

and the q-axis component of the grid voltage is

$$v_{ac,q}(t) = 0. \tag{2.26}$$

The active and reactive powers can be written as (2.28) and (2.30), respectively.

$$P_{ac}(t) = \frac{3}{2}\left(v_{ac,d}(t)i_d(t) + v_{ac,q}(t)i_q(t)\right) \tag{2.27}$$

$$P_{ac}(t) = \frac{3}{2}V_{ac}i_d(t) \tag{2.28}$$

$$Q_{ac}(t) = \frac{3}{2}\left(v_{ac,q}(t)i_d(t) - v_{ac,d}(t)i_q(t)\right) \tag{2.29}$$

$$Q_{ac}(t) = -\frac{3}{2}V_{ac}i_q(t) \tag{2.30}$$

Therefore, combining equations (2.20), (2.21), (2.25), (2.26), (2.28) and (2.30), the decoupled controllers for active and reactive power references are given in Figure 2.14.

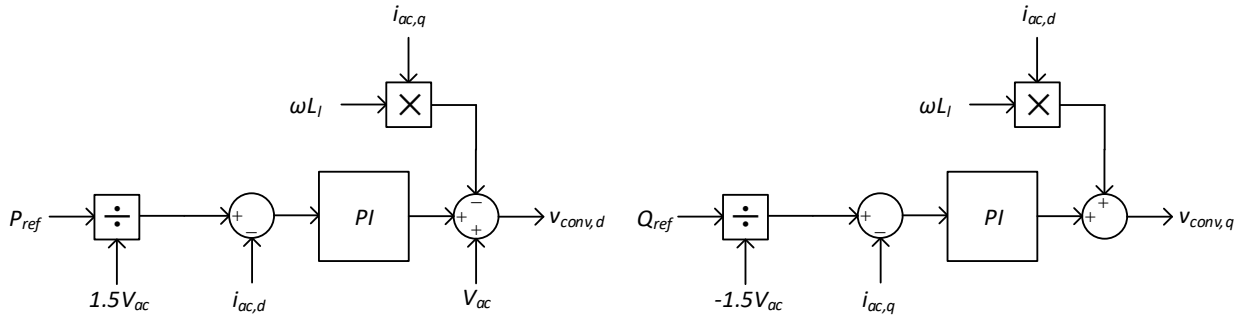

Figure 2.14: Decoupled controllers for controlling output active and reactive power.

The converter voltage magnitude and phase angle are calculated as shown in (2.31) and (2.32), respectively.

$$V_{conv} = \sqrt{v_{conv,d}^2 + v_{conv,q}^2} \tag{2.31}$$

$$\phi = \tan^{-1}\left(\frac{v_{conv,q}}{v_{conv,d}}\right) \tag{2.32}$$

In order to calculate the modulation index *m* to be used in the reference waveform of (2.15), the converter voltage magnitude V_{conv} is divided by the rated AC grid voltage (taking into account the turns ratio of the AC transformer) as shown in (2.33).

$$m = \frac{V_{conv}}{V_{ac,rated} TF_{ratio}} \tag{2.33}$$

Combining (2.33) with the DC voltage equation (2.8), the following relations between the grid AC voltage, the modulation index, the DC voltage and the sub-module capacitor voltage are obtained:

$$V_{ac,rated} = \frac{mN_{SM}V_{SM,cap}}{TF_{ratio}} \tag{2.34}$$

$$V_{DC} = \frac{6}{\pi} V_{ac,rated} TF_{ratio} \tag{2.35}$$

It is preferred to specify the grid-side voltage magnitude directly as opposed to the output reactive power. This is accomplished by adding a PI controller to obtain the equivalent $i_{ac,q}$ reference, as shown in Figure 2.15.

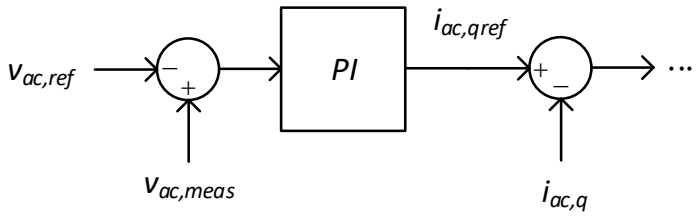

Figure 2.15: PI controller for AC grid voltage control.

Alternatively, the DC voltage can be used as the reference in lieu of the AC active power output. A similar PI controller shown in Figure 2.15 can be used to obtain the equivalent $i_{ac,d}$ reference using the DC voltage as the input.

2.3.5 DC Voltage Control

The average value of the DC voltage can be thought of as the product between the average capacitor voltage of the sub-modules and the average number of inserted sub-modules, as determined by the reference waveform (2.15). Therefore, the DC voltage can be written as

$$V_{DC} = N_{avg}V_{cap,avg} = \left(\frac{6}{\pi}mN_{SM}\right)\left(V_{SM,cap}\right). \tag{2.36}$$

For a given DC voltage, if the modulation index changes, the average number of inserted sub-modules will change, and therefore the sub-module capacitor voltages will change. Varying sub-module capacitor voltages may produce additional harmonics, operate outside the ratings of the equipment, or may increase the difficulty of operating the PH-MMC as desired. Therefore an additional controller is used to maintain the sub-module capacitor voltages while allowing different modulation indices to be used. This controller introduces a third-harmonic component to the reference waveform [12]. The harmonics introduced by this injection will add (or subtract) to the DC voltage, while being canceled out in the AC line voltages and currents on the grid side of the AC transformer.

The reference waveform including this third-harmonic injection is

$$ref(t) = mN_{SM}\left|\sin(\omega t + \phi + \varphi) + \alpha\sin\left(3(\omega t + \varphi)\right)\right| \tag{2.37}$$

where α is the ratio of the third harmonic being injected with respect to the fundamental frequency component. This could be extended by adding additional odd triple-*n* harmonics (9*n*, 15*n*, 21*n*, etc.) to the reference as well [28], [29]; however, only third harmonics are considered in this thesis.

If only using half-bridge sub-modules, the wave-shaping stage cannot produce negative voltages, and therefore α should be limited such that

$$\sin(\omega t + \phi + \varphi) + \alpha \sin\big(3(\omega t + \varphi)\big) \geq 0 \; for \; 0 \leq \omega t \leq \pi \tag{2.38}$$

is satisfied. The above equation can be rewritten as

$$1 + \alpha[4\cos^2(\omega t) - 1] \geq 0. \tag{2.39}$$

Using the maximum and minimum values of $\cos^2(\omega t)$ for the period $0 \leq \omega t \leq \pi$ (1 and 0, respectively), the limits for α are

$$-\frac{1}{3} \leq \alpha \leq 1. \tag{2.40}$$

If full-bridge sub-modules are utilized instead of half-bridge sub-modules, then the wave-shaping stage can produce negative voltages and the third harmonic injection does not need to be limited by (2.40). However, as will be discussed later in this section, a large third harmonic injection requires further considerations to the design of the PH-MMC.

The DC voltage is therefore given by

$$V_{DC} = \left[\frac{6}{\pi} m N_{SM} \left(1 + \frac{\alpha}{3}\right)\right] \left(V_{SM,cap}\right) \tag{2.41}$$

which can be rewritten for the sub-module capacitor voltage as

$$V_{SM,cap} = \frac{V_{DC}}{(6/\pi) m N_{SM} \left(1 + \frac{\alpha}{3}\right)}. \tag{2.42}$$

The AC voltage at the converter terminal remains unchanged from (2.6). With the third harmonic injection, the peak value of the reference waveform is

$$\max\big(ref(t)\big) = m N_{SM} \left(1 + \frac{\alpha}{3}\right). \tag{2.43}$$

Since there are only N_{SM} sub-modules in each sub-module stack, the voltage crafted by the wave-shaping stage will begin to saturate when

$$m\left(1+\frac{\alpha}{3}\right)>1 \tag{2.44}$$

is true. When this occurs, the peak of the crafted rectified sinusoid clips at N_{SM} when $ref(t) > N_{SM}$. This saturation will start introducing low order harmonics into the AC network. If operating deep into saturation, the voltage waveform crafted by the wave-shaping stage begins to look more like a square waveform, which has significant low order harmonics.

In order to prevent operating in saturation, the number of sub-modules in each stack is increased. The number of additional sub-modules needed to avoid saturation can be determined by finding the maximum of the reference waveform. These values are determined by equating the derivative of $ref(t)$ to 0, as shown in

$$\frac{d}{dt}ref(t)=0 \tag{2.45}$$

and

$$\cos(\omega t)\left[1+3\alpha(1-4\sin^2(\omega t))\right]=0. \tag{2.46}$$

Solving the above equation and finding the maximum of the reference waveform (2.37) with N_{SM} constant and assuming $m = 1$, the maximum for $\alpha = -1/3$ is 1.333, i.e., an additional 34% of sub-modules are required to avoid saturation, and for $\alpha = 1$, the maximum is 1.539, i.e., an additional 54% more sub-modules are required to avoid saturation.

One important observation is that the maximum value of the reference waveform is dependent on the modulation index, m. For a smaller modulation index, a larger magnitude of third harmonics can be injected while avoiding saturation, as indicated by (2.44). A second observation is that even

if 54% more sub-modules are added to the phase stack, there will still be fewer sub-modules in the PH-MMC than there would be required in a conventional MMC to produce the same AC voltage.

In order to incorporate the additional sub-modules, it is important that these additional sub-modules are "reserved" to avoid saturation when injecting the third harmonic. While these sub-modules can, and should, be included in the regular operation of the PH-MMC (voltage sorting/balancing, PWM control, etc.), these sub-modules should not be used to essentially increase the number of levels in the stepped AC voltage waveform. For example, if a PH-MMC is designed for N_{SM} = 10 with 50% additional sub-modules for third-harmonic injection (i.e., N_{tot} = 1.5N_{SM} = 15), then the reference waveform of (2.37) should have a maximum of N_{SM} = 10 for m = 1 and α = 0. Only changes in α (or for m > 1, which would also introduce saturation) should result in more than N_{SM} = 10 sub-modules being inserted in the stack.

An additional controller is added for the magnitude of the third harmonic to be injected by the reference waveform [12]. First, a PI controller is used to calculate the DC current reference, assuming a lossless converter, using the change of energy stored in the sub-module capacitors (i.e., their voltage) as the input. Then, depending on the DC voltage (rectifier end) and the DC line parameters, the corresponding voltage at the DC terminal of the PH-MMC is obtained via a second PI controller. The magnitude of the third harmonic injection is then calculated from (2.41). The control block diagrams of this controller are shown in Figure 2.16.

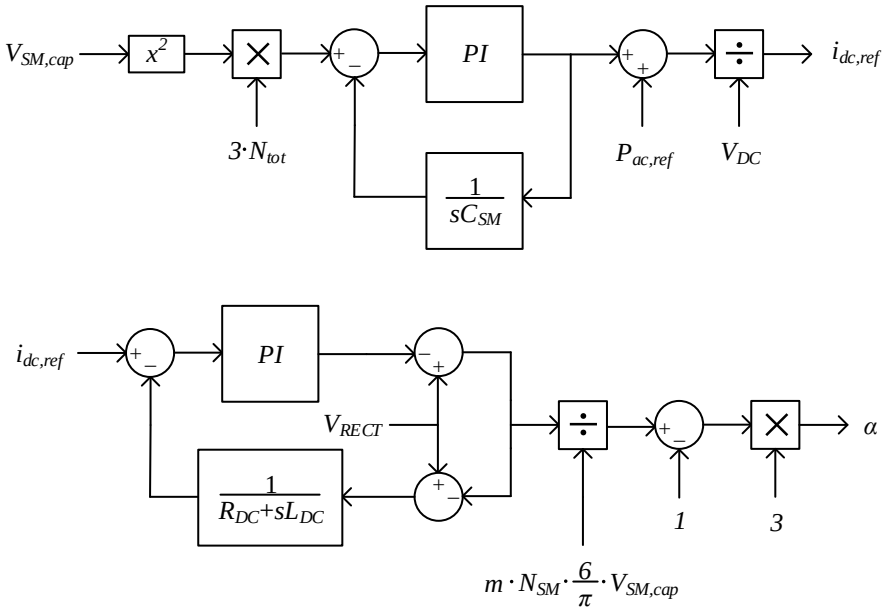

Figure 2.16: Controllers for DC voltage control with third harmonic injection.

In the above diagram, C_{SM} is the capacitance of the sub-module capacitors, R_{DC} and L_{DC} are the DC line resistance and inductance, N_{tot} is the total number of sub-modules in each phase stack (including additional sub-modules for third harmonic injection) and V_{RECT} is the DC voltage at the rectifier end of the DC line.

Similar DC voltage controllers for third harmonic injection are also available, such as the controllers in [30] and [31].

Alternative methods are possible for maintaining the DC voltage, such as the aforementioned triplen harmonics injection of higher frequencies [28]. One alternative is to isolate the AC and DC sides by blocking the director switches for a short period during the zero-crossings of the AC voltage and inserting (or bypassing) all sub-modules in the stack during this time to maintain the average DC voltage [32]. Another is to add full-bridge sub-modules in series with the director stage [33]. The sub-modules in the wave-shaping stage are switched to produce a near-constant

DC voltage, which is then offset by the full-bridge sub-modules to produce the required sinusoidal voltage at the AC terminals of the converter.

One application that may negate the need of DC voltage control is to operate the PH-MMC as a STATCOM to inject reactive power into an AC network [34]. The DC side of STATCOMs are left disconnected, i.e. there is no DC network, and therefore no active power is transferred from the DC side to the AC side. Although it is preferred, it is not necessary to maintain a constant DC voltage (just as long as the sub-module capacitor voltages are maintained at a constant value), and the PH-MMC can operate as a STATCOM without any third harmonic injection.

2.4 Fault Analysis of PH-MMC

A qualitative fault study is performed in this thesis for both AC terminal and DC terminal faults. A more detailed analysis is recommended for future work as discussed in Section 4.2.

2.4.1 AC-Terminal Faults

At the inception of a fault on the AC terminal of the converter, current from the DC network will flow towards the AC network due to the low residual voltage at the faulted bus. This will be true regardless of whether the PH-MMC is on the sending end (rectifier-side) or the receiving end (inverter-side) of the DC network. Once the fault is detected by the converter, a signal can be sent to all IGBT switches to block the firing pulses (i.e., switch off all IGBT switches). A diagram of one phase of the PH-MMC is shown in Figure 2.17, where the IGBT switches are blocked.

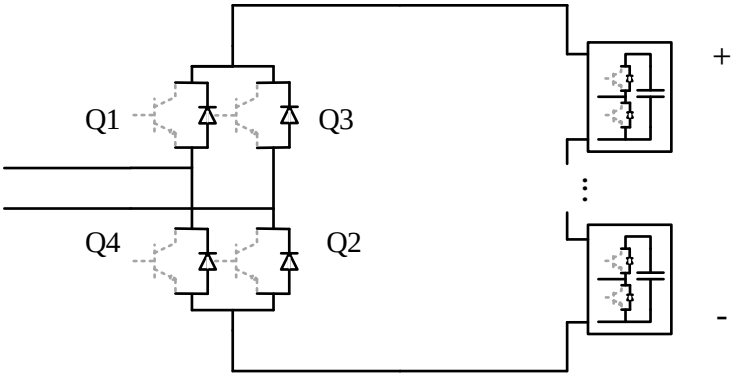

Figure 2.17: Single-phase of PH-MMC with all IGBT switches blocked.

After the IGBT switches in the director stage and wave-shaping stage are blocked, only the reverse diodes are able to conduct current. Due to the orientation of the reverse diodes in the director stage and the polarity of the DC voltage, current from the DC network will not contribute to the fault current on the AC side of the converter, hence, the PH-MMC is able to block AC faults.

One important difference from conventional MMCs is that the sub-modules of the PH-MMC are not in series with the AC terminals, but are instead connected in parallel. Therefore, it is possible to only block the director stage switches to block AC fault contributions from the DC network, while leaving the wave-shaping switches in continuous operation. Between the inception of the fault and the time for the director stage switches to be blocked, the sub-module capacitors (and hence the DC voltage) will stray from their steady state values. After the director stage switches are blocked, the sub-modules in the wave-shaping stage can be switched accordingly in order to bring the capacitor voltages back to their pre-fault value by exchanging power with the AC network on the opposite side of the DC line, and hence, maintain the DC voltage. In doing so, transients could be reduced after the AC fault is cleared and the director stage switches are de-blocked. This functionality is not possible with conventional MMCs as the sub-modules must remain blocked in order to block AC side faults.

2.4.2 DC Pole-Pole Faults

Considering the PH-MMC with all switches blocked in Figure 2.17, a fault across the DC terminals cannot be blocked as easily as an AC side fault. Due to the orientation of the reverse diodes in the director stage, current from the AC side will continually contribute to the DC fault, and blocking this current will not be possible. Additional methods, such as DC breakers, would be required to block DC faults.

Since the wave-shaping stage is connected in parallel with the director stage, utilizing full-bridge sub-modules instead of half-bridge sub-modules will not block DC faults, as was the case with conventional MMCs. Instead, using full-bridge sub-modules in the PH-MMC will block current from flowing through the wave-shaping stage. This will still be some advantage over half-bridge sub-modules, as it will protect the equipment within the wave-shaping stage from overcurrents.

A fully detailed fault analysis is beyond the scope of this thesis, and is recommended as additional work for future studies in Section 4.2.

Chapter 3 Reduced-Order Modelling and Modelling Verification

The purpose of the reduced-order model is to develop an accurate representation of the PH-MMC to model the low-frequency behavior of the converter in order to run EMT-type (low-frequency only) simulations at a fraction of the computation time. Before delving into the details of the reduced-order model, several assumptions need to be made for simplicity:

- The number of sub-modules in each sub-module stack is large enough such that an ideal rectified sinusoid is generated by the wave-shaping stage. This will remove the need of modeling the high-frequency switching events and transients, therefore improving the simulation's computation time at the expense of producing the true staircase waveform.
- The capacitor sorting and balancing algorithms are ideal, and therefore all capacitors in the same sub-module stack (of a given phase) have the same voltage. This allows the use of a single capacitor to represent all sub-module capacitors in the stack.
- The converter is assumed to be lossless.

3.1 Reduced-Order Model of the PH-MMC

In the reduced-order model, the AC and DC terminal voltages are represented as DC voltage sources with variable inputs. Incorporating the assumptions listed above, the output AC voltage (for phase a) is given by

$$v_{conv,a}(t) = mN_{SM}v_{cap,a}(t)\big(\sin(\omega t + \varphi) + \alpha \sin\big(3(\omega t + \varphi)\big)\big). \tag{3.1}$$

Similar equations can be obtained for the other two phases, assuming the proper phase shifts.

The DC voltage is the sum of the voltages across the three phase stacks and is given by

$$v_{DC}(t) = \left|v_{conv,a}(t)\right| + \left|v_{conv,b}(t)\right| + \left|v_{conv,c}(t)\right|. \tag{3.2}$$

In order to determine the equivalent sub-module capacitor voltage, $v_{cap,a}(t)$, consider the following screenshot of one phase (phase-a) of the PH-MMC in Figure 3.1. A similar analysis can be performed for the other phases.

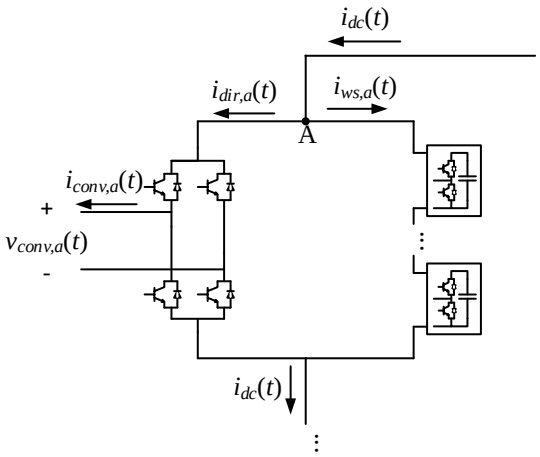

Figure 3.1: Diagram of phase-a stages of PH-MMC.

Using Kirchhoff's Current Law (KCL) at node 'A' yields

$$i_{dc}(t) - i_{dir,a}(t) - i_{ws,a}(t) = 0. \tag{3.3}$$

The current entering the director stage is related to the converter AC current by

$$i_{dir,a}(t) = i_{conv,a}(t) \times sign\left(v_{conv,a}(t)\right). \tag{3.4}$$

The power absorbed by the wave-shaping stage is equal to the power absorbed by all sub-module capacitors in the sub-module stack. Therefore, if the sub-module capacitors are represented by a single capacitor, the current of the capacitor, is shown in (3.6).

$$N_{tot} v_{cap,a}(t) i_{cap,a}(t) = i_{ws,a}(t)\left|v_{conv,a}(t)\right| \tag{3.5}$$

$$i_{cap,a}(t) = \frac{i_{ws,a}(t)\left|v_{conv,a}(t)\right|}{N_{tot}v_{cap,a}(t)} \tag{3.6}$$

Combining the above equations, the state equation for the sub-module capacitor voltage (for phase a) is given in

$$\frac{d}{dt}v_{cap,a}(t) = \frac{1}{C_{SM}}\left[\left(i_{conv,a}(t) \times sign\left(v_{conv,a}(t)\right)\right)\left(\frac{\left|v_{conv,a}(t)\right|}{N_{tot}v_{cap,a}(t)}\right) + i_{dc}(t)\right]. \tag{3.7}$$

where C_{SM} is the capacitance of the sub-module capacitors.

Similar equations are obtained for the other two phases. The DC and AC output currents are measured at their respective terminals and therefore developing state equations for these currents is not necessary for the reduced-order model. The decoupled controller and DC voltage controller are implemented as described in Section 2.3.4 and Section 2.3.5, respectively.

3.2 Model Verification Using Electromagnetic Transient (EMT) Simulations

The reduced-order model of the PH-MMC is compared and validated against the full, detailed switching model in PSCAD™/EMTDC™ software. The same disturbances are applied to the two converter models, operating at the same initial conditions, and the steady state values and dynamic responses are compared. The converters are incorporated into two network cases: a simple network case consisting of two AC grid sources, and with the PH-MMC incorporated into the more complex IEEE 12-Bus System model.

3.2.1 Simple Network Case

The simple network model is shown below in Figure 3.2.

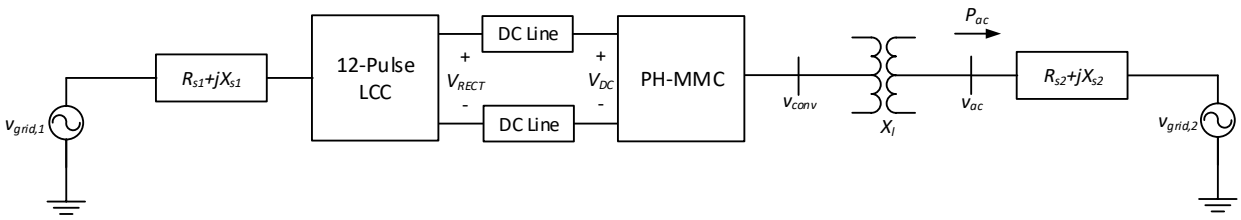

Figure 3.2: Simple network case for reduced-order model validation.

The PH-MMC, on the inverter end of the HVDC transmission network, controls the output active power at its AC terminal (P_{ac}), as well as the magnitude of the AC terminal voltage (v_{ac}). The 12-pulse LCC rectifier controls the DC voltage at its terminal (V_{RECT}). This is accomplished by using a simple PI controller with a feed-forward signal to control the firing angle α_R of the rectifier. The DC voltage of a 12-pulse controlled rectifier is given by

$$V_{RECT} = 2 \times \left(\frac{3\sqrt{2}}{\pi} V_{LL} \cos \alpha_R - \frac{3\omega L_{tf}}{\pi} I_{DC} \right). \tag{3.8}$$

where V_{LL} is the line-line voltage at the AC terminal of the converter, L_{tf} is the leakage inductance of the converter transformers, and I_{DC} is the DC terminal current.

The control block diagram of the rectifier DC voltage controller is shown in Figure 3.3. Note that the second term in (3.8) is omitted and V_{LL} is assumed to be the rated voltage of the AC source $v_{grid,1}$ in the feed-forward path for simplicity.

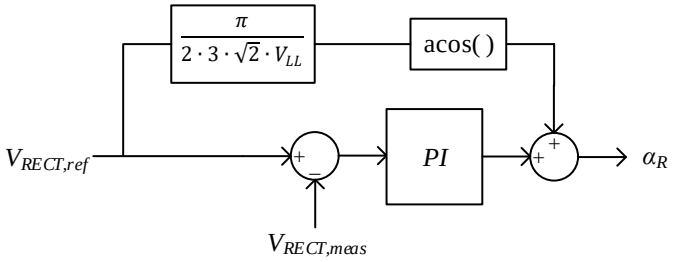

Figure 3.3: Rectifier DC voltage controller.

The DC network, as implemented in PSCAD™/EMTDC™, is shown in Figure 3.4. The DC line is represented as a pi-model with smoothing reactors at the rectifier and inverter terminals, using typical parameters. The H-bridges and sub-modules of the PH-MMC are within the block labeled “Hybrid MMC”.

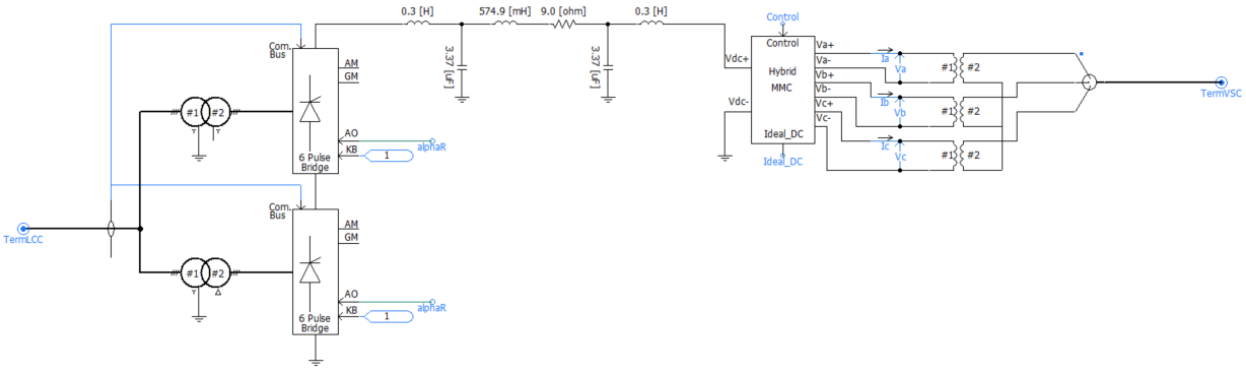

Figure 3.4: DC network and converter stations in PSCAD™/EMTDC™.

The network parameters, as well as the characteristics of the rectifier and the PH-MMC, are shown in the following tables. DC line parameters were selected by using scaled-values of the real world HVDC line Bipole II in Manitoba, and the sub-module capacitance was selected based on similar values used in industry and those found in research.

Table 3.1: AC and DC network parameters.

Network Parameter	Value	Unit
$V_{grid,1}$ Nominal Voltage	240.0	kV
R_{s1}	1.0	Ω
X_{s1}	7.54	Ω
V_{DC} Nominal Voltage	300.0	kV
R_{DC}	9.0	Ω
L_{DC}	574.9	mH
$C_{DC}/2$	3.37	µF
$V_{grid,2}$ Nominal Voltage	230.0	kV
R_{s2}	1.0	Ω
X_{s2}	7.54	Ω

Table 3.2: Rectfier parameters.

Rectifier Parameter	Value	Unit
TF Rated MVA (three-phase)	301.5	MVA
TF Leakage Reactance	0.1	pu
Winding 1 Nominal Voltage	230.0	kV
Winding 2 Nominal Voltage	230.0	kV
DC Smoothing Reactor	300.0	mH

Table 3.3: PH-MMC/inverter parameters.

PH-MMC/Inverter Parameter	Value	Unit
# of Sub-modules/phase (N_{tot})	20	-
Sub-module Capacitance (C_{SM})	15.0	mF
TF Rated MVA (single-phase)	197.0	MVA
TF Leakage Reactance	0.1	pu
Winding 1 Nominal Voltage	199.0	kV
Winding 2 Nominal Voltage	230.0	kV
DC Smoothing Reactor	300.0	mH

In order to validate the reduced order model to the detailed model, a number of reference changes are simulated. These reference changes include a step change in the active power reference of the PH-MMC, and a change in the grid voltage reference of the PH-MMC AC terminal, in order to create three unique operating conditions. The step changes implemented are shown in Table 3.4.

Table 3.4: Reference step changes.

Time [s]	AC Active Power [MW]	AC Voltage Magnitude [kV]
0.0 – 5.0	342.0	228.3
5.0 – 10.0	292.0	228.3
10.0 – 15.0	292.0	220.8

The detailed model was simulated using a 10 µs time step to capture all switching events, and the reduced-order model was simulated with a 10 µs time step and a 50 µs time step. A larger time step can be used for the reduced-order model since the high frequency switching events are not considered in this model, as previously described.

Figure 3.5 shows the AC voltage (converter side of PH-MMC transformer) and AC current (grid side of PH-MMC transformer) waveforms during the first operating point. Figure 3.6 and Figure 3.7 show the RMS voltage, active power and reactive power measurements of the AC network at the grid side of PH-MMC transformer for the first and second disturbance, respectively.

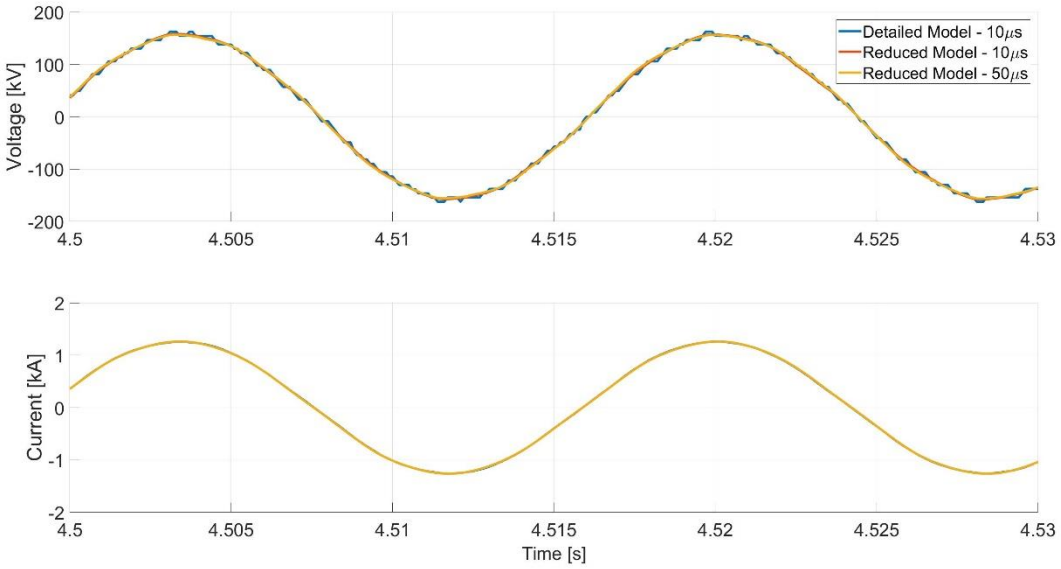

Figure 3.5: Simulation results for simple network case: AC waveforms (1st operating point).

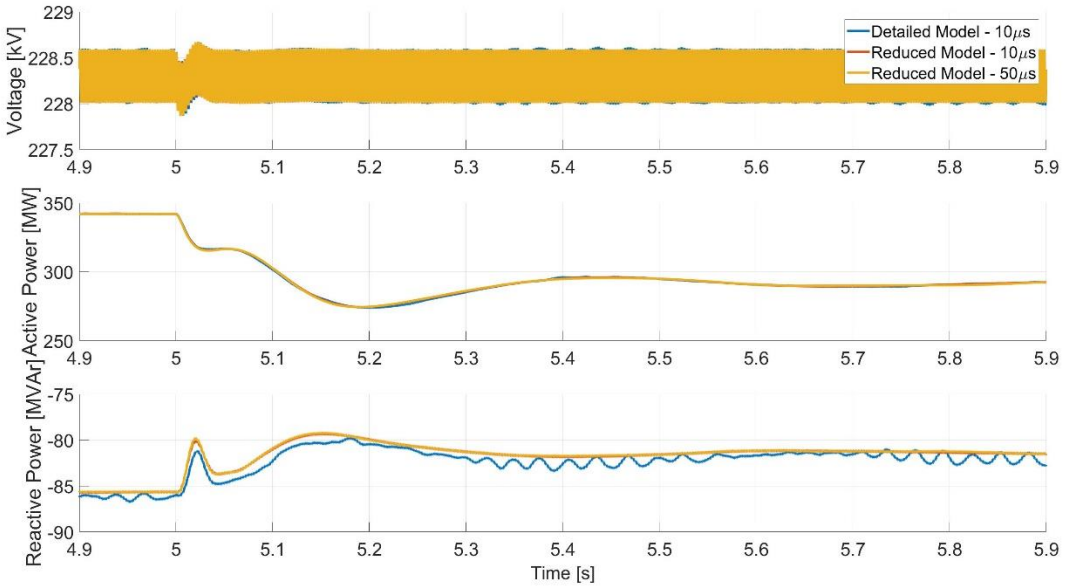

Figure 3.6: Simulation results for simple network case: AC grid quantities (1st transient).

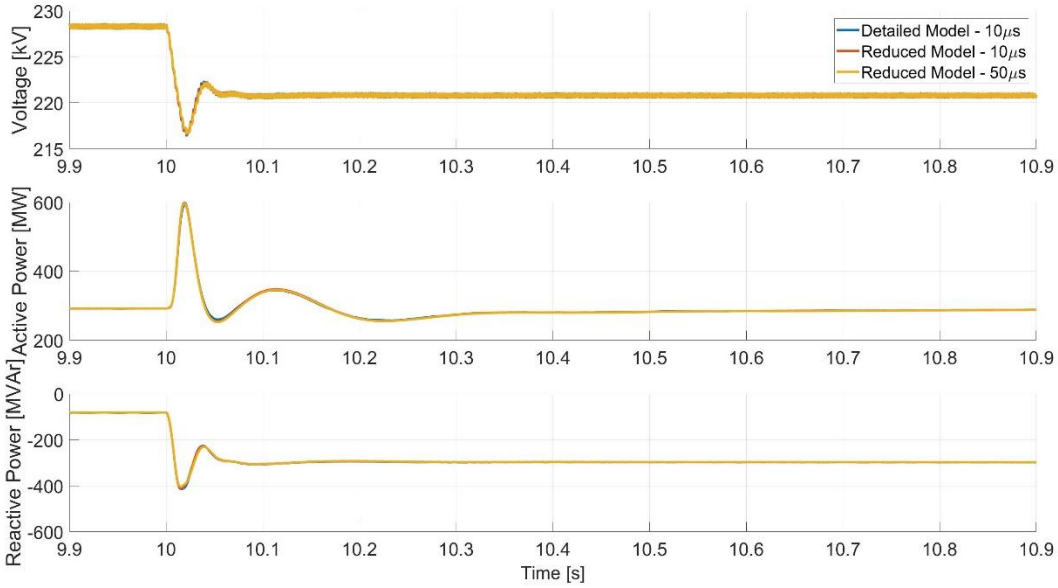

Figure 3.7: Simulation results for simple network case: AC grid quantities (2nd transient).

In the above simulation results, nearly identical results are observed in the AC waveforms. The small differences in the detailed model are due to the discrete voltage steps in the converter voltage.

The low frequency transient behavior of the grid voltage magnitude, active power and reactive power of the reduced-order model matches closely with the detailed model. However, there is a small shift in the reactive power measurements between the detailed model and the reduced-order models. Also in the reactive power, high frequency oscillations are observed in the detailed model but not in the reduced-order model. These oscillations are not observed in the reduced-order model as it is designed to only capture the low frequency behavior of the PH-MMC. The reduced-order model agrees well with the detailed model using a time step of 10 μs and 50 μs.

Additional simulation results are shown in Appendix A.

A comparison of the runtimes is shown in Table 3.5.

Table 3.5: Simulation runtime comparison for the simple network case.

Model	Time Step [μs]	Runtime [s]	Runtime Ratio
Detailed	10.0	150.890	-
Reduced	10.0	41.734	3.6
Reduced	50.0	11.188	13.5

As shown, the computational burden of simulating the reduced-order models is reduced as compared to the detailed model, while accuracy in the dynamic responses is maintained.

3.2.2 Integration into IEEE 12-Bus System

The IEEE 12-bus system is implemented in PSCAD™/EMTDC™ software and is shown in Figure 3.8. The AC transmission line between Bus 1 and Bus 3 is replaced with the LCC rectifier, HVDC line and PH-MMC described in the previous section.

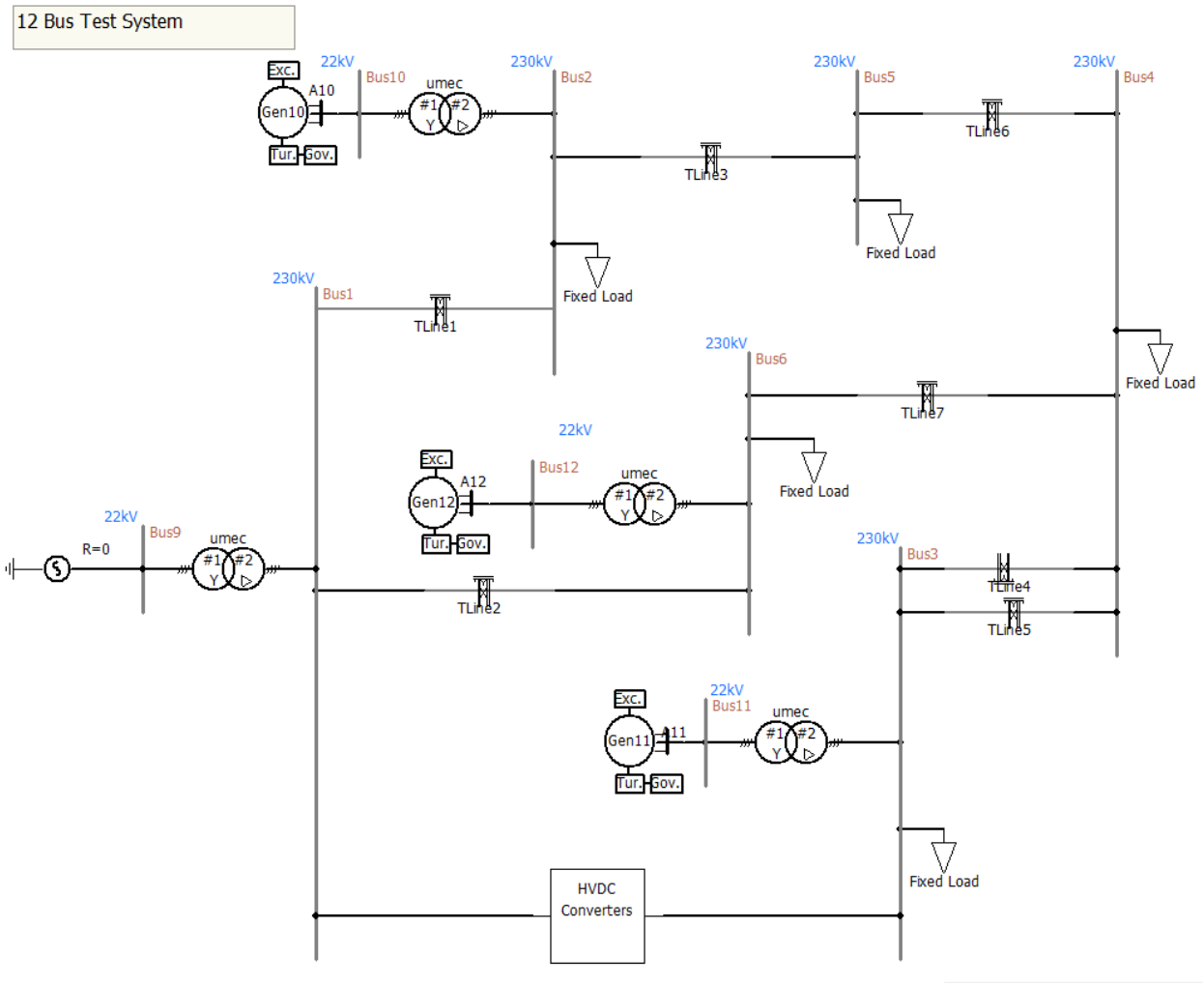

Figure 3.8: IEEE 12-bus system model with HVDC network between buses 1 and 3.

As was done previously, the detailed model of the PH-MMC was simulated using a 10 µs time step to capture all switching events, and the reduced-order model of the PH-MMC was simulated with a 10 µs time step and a 50 µs time step.

The dynamic response and the settling values of the reduced-order model are compared to the response of the detailed model. Figure 3.9 shows the AC voltage (converter side of PH-MMC transformer) and AC current (grid side of PH-MMC transformer) waveforms during the first operating point. Figure 3.10 and Figure 3.11 show the RMS voltage, active power and reactive

power measurements of the AC network at the same location for the first and second disturbance, respectively.

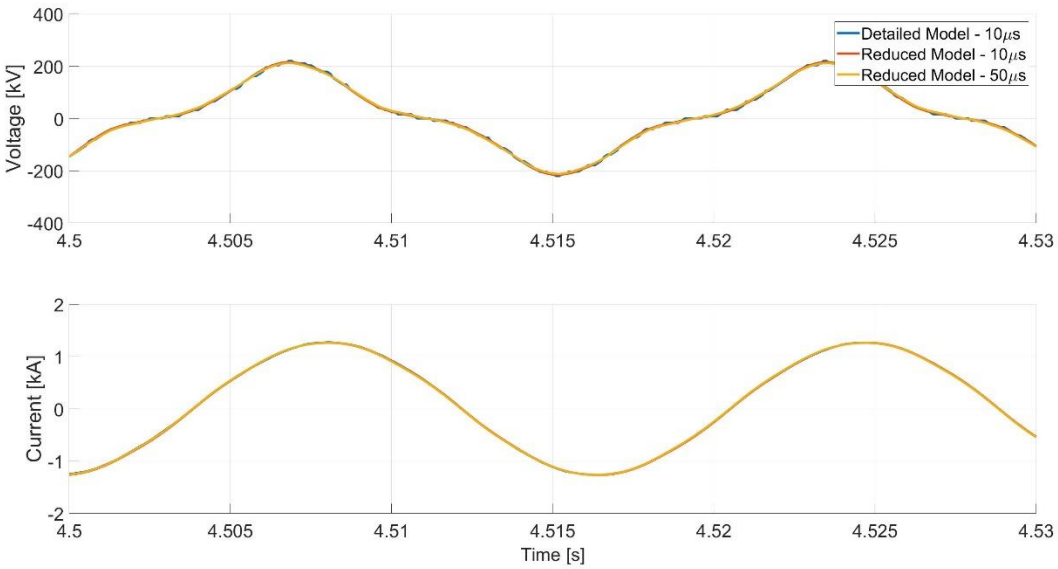

Figure 3.9: Simulation results for IEEE 12-bus system: AC waveforms (1st operating point).

Note: the 'distorted' AC voltage waveform is due to the third-harmonic injection to maintain the sub-module capacitor voltages. Despite this, the AC current waveform is very close to an ideal sinusoid.

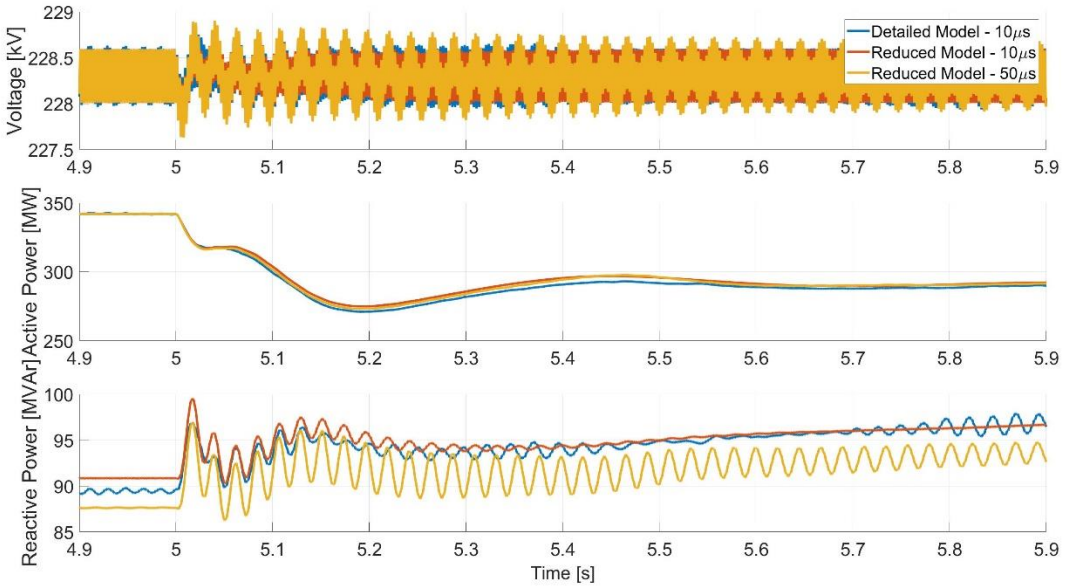

Figure 3.10: Simulation results for IEEE 12-bus system: AC grid quantities (1st transient).

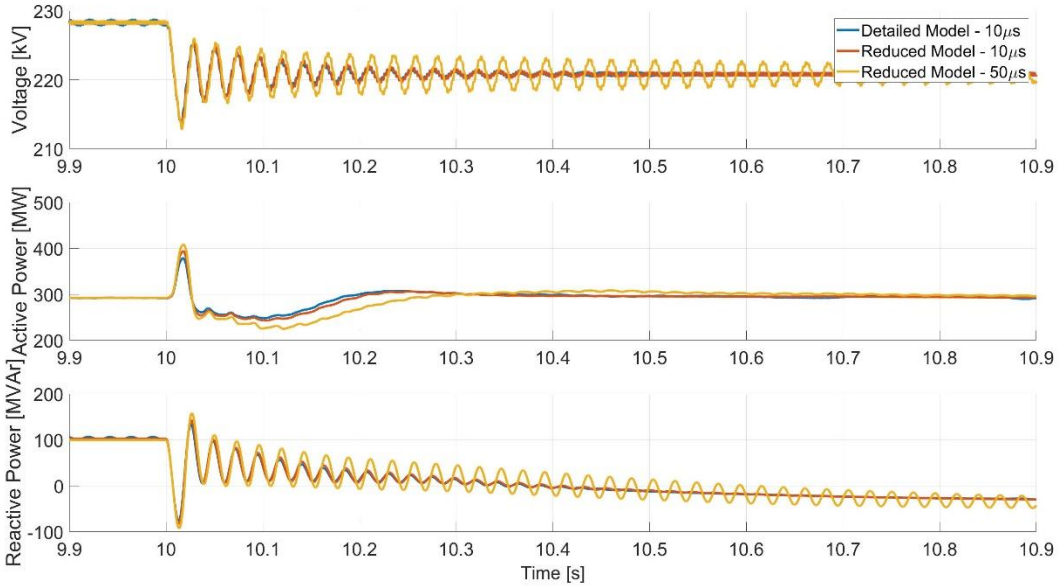

Figure 3.11: Simulation results for IEEE 12-bus system: AC grid quantities (2nd transient).

In the above simulation results, nearly identical results are observed in the AC waveforms. The low frequency transient behavior of the grid voltage magnitude, active power and reactive power

is maintained in the reduced-order model, however, there is a small shift in the reactive power. When using a time step of 50 μs, there is a larger difference in the active power measurement during the transient of the second disturbance. In addition, there are high frequency oscillations that have very low damping in the voltage and reactive power measurements for a time step of 50 μs. However, it can be seen that the low frequency behavior of the reduced-order model using a time step 50 μs is similar to the low frequency behavior of the detailed model. The reduced-order model agrees well with the detailed model using a time step of 10 μs, while there is a small discrepancy in the active power for a time step of 50 μs.

Additional simulation results are shown in Appendix B.

A comparison of the runtimes is shown in Table 3.6.

Table 3.6: Simulation runtime comparison for the IEEE 12-bus system.

Model	Time Step [μs]	Runtime [s]	Runtime Ratio
Detailed	10.0	361.750	-
Reduced	10.0	165.438	2.2
Reduced	50.0	40.437	8.9

As shown, the computational burden of simulating the reduced-order models is reduced as compared to the detailed model. However, this decrease in computation time for the IEEE 12-bus system model is less than what was observed when simulating with the simple network case. This is because of the increased complexity of the IEEE 12-bus system, which includes detailed generator and transmission line components.

As shown in the above simulation tests, the reduced-order model is able to accurately capture the behavior and characteristics of the detailed model using the simple network case and the IEEE 12-bus system. In addition, the reduced-order model is able to run at a larger time step to

significantly decrease the runtime of the simulation, although a larger time step may result in some discrepancies in more detailed network models.

Chapter 4 Contributions, Conclusions and Future Work

4.1 Contributions and Conclusions

The topology and basic operation of the PH-MMC is closely related to conventional MMCs, and therefore the basics of conventional MMCs was discussed. This was also necessary to compare the advantages and disadvantages of PH-MMCs to a VSC type that is commonly used in the industry.

The main advantage of PH-MMCs over conventional MMCs is that the PH-MMC requires a smaller number of sub-modules to produce the same stepped AC voltage waveform as conventional MMCs, resulting in a more cost-efficient VSC alternative. However, the voltage across the DC terminals of the PH-MMC will not be constant due to the switching of the sub-modules. A DC voltage controller is therefore required to maintain the sub-module capacitor voltages at a near-constant value in order to minimize harmonics.

The control of PH-MMCs was then discussed and it was shown to be similar to the control of conventional MMCs. Standard voltage balancing and sorting algorithms to maintain similar voltages across the sub-module capacitors are required for operating PH-MMCs as they were for conventional MMCs. Half-bridge sub-modules are used in the wave-shaping stage to craft a voltage waveform resembling a rectified sinusoid, which can be generated using a reference sinusoid waveform and PWM techniques. In addition, a decoupled controller can be utilized to control the active power output (or DC terminal voltage) and the reactive power output (or AC terminal voltage magnitude) of the converter.

The PH-MMC requires two new controllers: a controller for the H-bridges (director stage) and a controller to maintain the DC voltage. The H-bridges are controlled to apply the appropriate

polarity of the voltage crafted by the wave-shaping stage to the AC terminals of the converter to create an alternating sinusoidal voltage. The DC voltage controller detailed in this thesis adds a third harmonic component to the reference AC voltage waveform in order to maintain the sub-module capacitor voltages while not injecting harmonics to the AC line voltages and currents. However, additional sub-modules are required in order to prevent the voltage across the sub-module stacks from saturating.

The viability of using different types of power electronic switches for the director stage was analyzed. It was shown that GTOs can be used as an alternative to IGBTs, as they are able to switch on and off every period at a low probability of commutation failure. GTOs are rated for higher voltages and therefore fewer GTOs are required to be used in the director stage.

A qualitative fault analysis was also discussed in this thesis. It was shown that AC faults can be blocked by blocking only the director stage switches, which allows the sub-modules in the wave-shaping stage to continue being switched to maintain the DC voltage during the fault. While conventional MMCs can also block AC side faults, the DC- voltage cannot be maintained during the AC fault and it can only be restored after the AC fault is cleared. Conversely, PH-MMCs are unable to block DC faults whereas conventional MMCs are able to by using full-bridge sub-modules. In PH-MMCs, AC current will flow through the reverse diodes in the director stage and continually supply the DC fault. Using full-bridge sub-modules in the wave-shaping stage of PH-MMCs will only prevent current from flowing through the sub-modules, which will protect the sub-modules from overcurrents.

An EMT reduced-order model of the PH-MMC was then developed. The reduced-order model assumes that the number of sub-modules is sufficiently high to craft a near-ideal rectified sinusoid waveform by the wave-shaping stage, and that all sub-module capacitors have the same voltage

across them at all times. This allows the PH-MMC to be developed into a simplified mathematical model that does not require all switching events to be captured, and therefore can be simulated with a larger time step than the full, detailed model.

Using a simple network model and implementing the PH-MMC into the IEEE 12-bus system model in PSCAD™/EMTDC™, a number of reference set point changes were simulated and the dynamic responses of the full, detailed model, the reduced-order model running at the same time step (10 µs), and the reduced-order model running at a larger time step (50 µs) were compared. It was observed that the reduced order model of the PH-MMC was able to maintain accuracy with the detailed model when using a time step of 10 µs, with some discrepancies when using a time step of 50 µs. However, the reduced-order model was able to perform the simulations at a fraction of the runtime required for the detailed model to run. This verifies the developed reduced-order model and showcases its accuracy of representing the detailed model in studies where simulating every switching event may not be necessary, speeding up the simulation runtime and reducing the computational burden.

4.2 Recommendations for Future Work

This thesis serves as an introduction to PH-MMCs and developing a reduced-order model for studies where simulating every switching event is not necessary. Therefore a more in-depth analysis is required of PH-MMCs before they become a more viable alternative to conventional MMCs. For example, a fully detailed fault analysis should be performed considering alternatives to blocking DC side faults, as well as the implications of using full-bridge sub-modules instead of half-bridge sub-modules in the wave-shaping stage. Being the main disadvantage of PH-MMCs, alternative methods of maintaining the sub-module capacitor voltages should be analyzed to identify possible methods that do not require additional sub-modules. In addition, real-time

simulation of a physical prototype of the PH-MMC should be carried out to verify the controller algorithms outside of the simulation software.

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Appendices

A. Dynamic Simulation Results: Simple Network Case

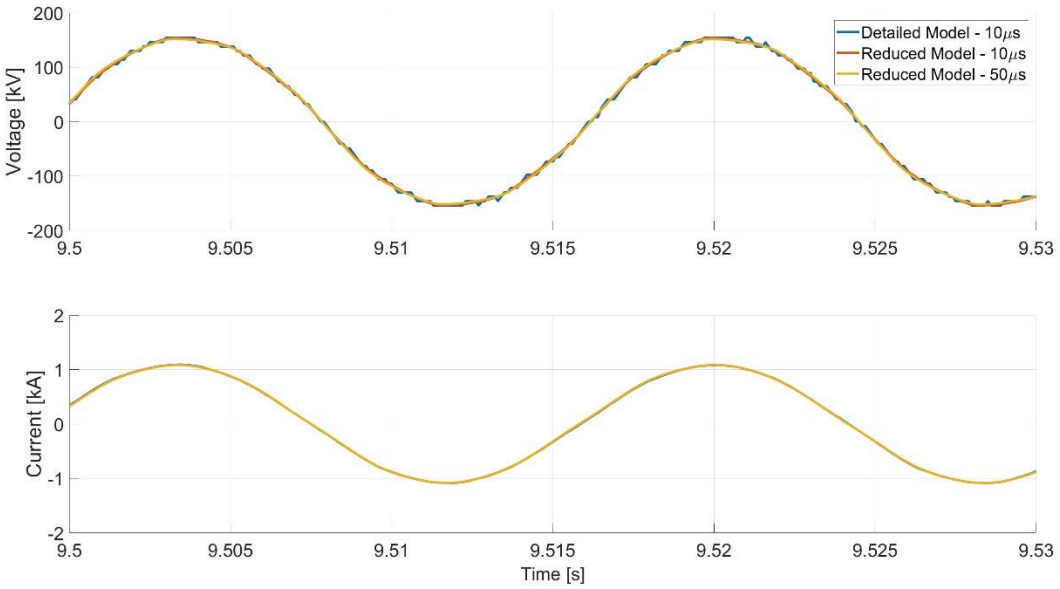

Figure A.1: Simulation results for simple network case: AC waveforms (2nd operating point)

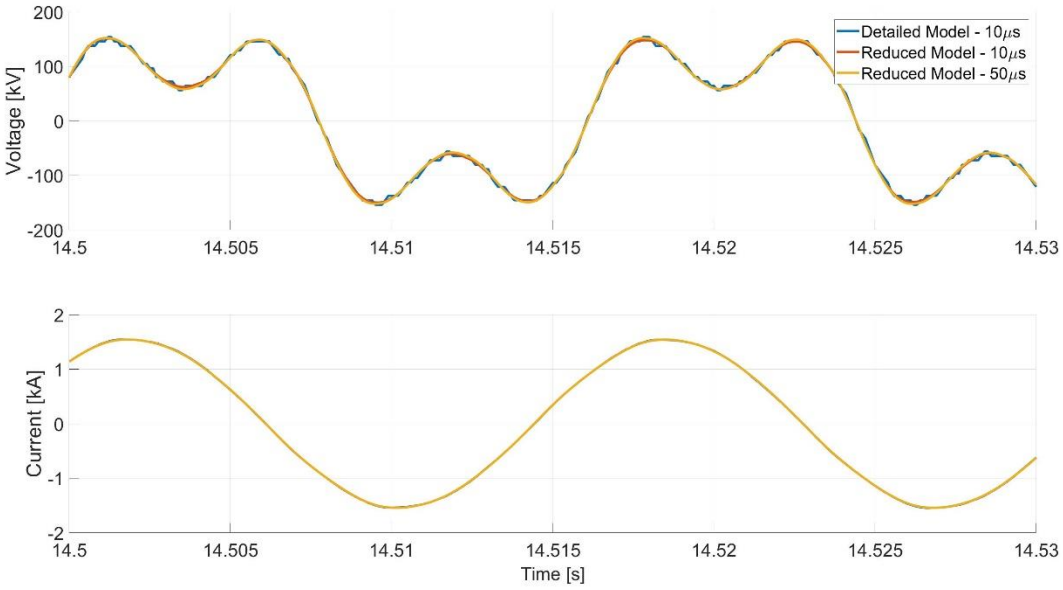

Figure A.2: Simulation results for simple network case: AC waveforms (3rd operating point)

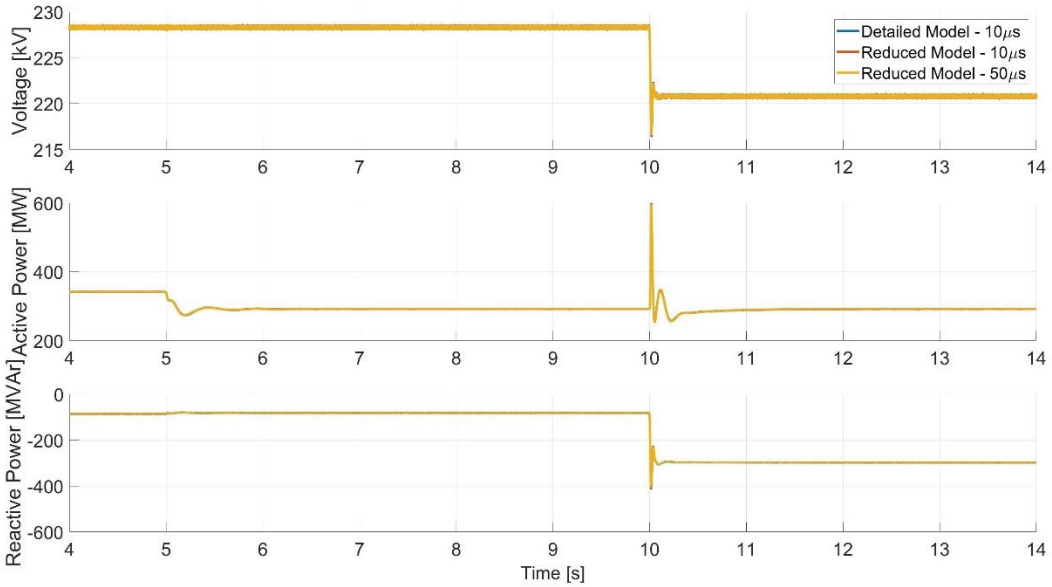

Figure A.3: Simulation results for simple network case: AC grid quantities

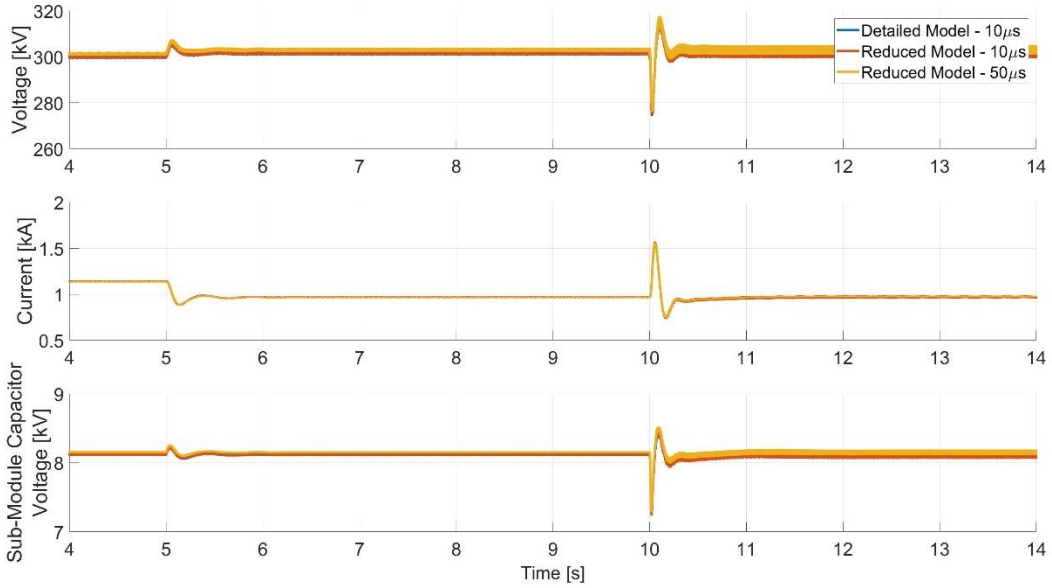

Figure A.4: Simulation results for simple network case: DC quantities

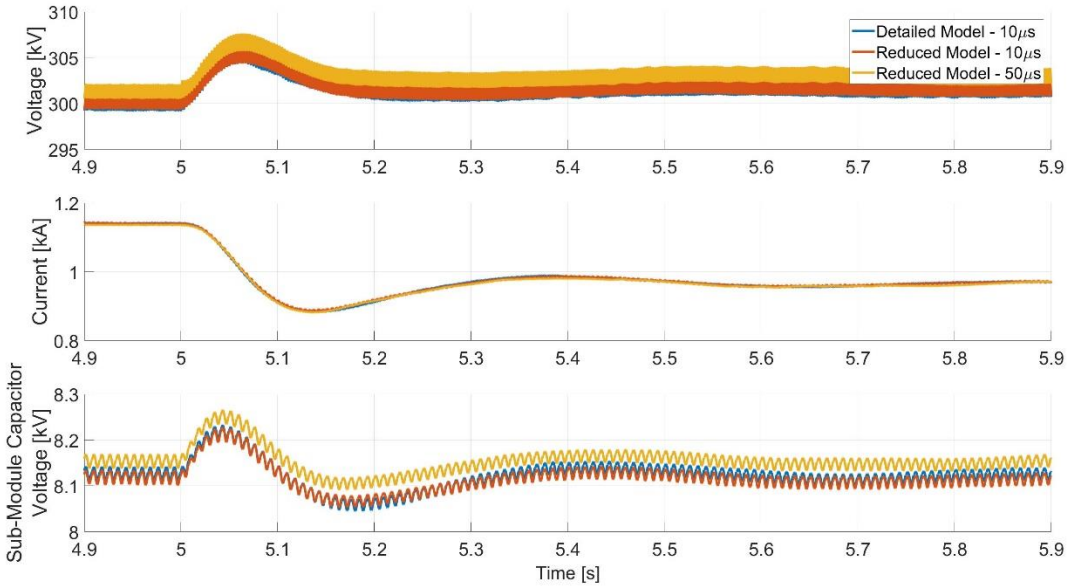

Figure A.5: Simulation results for simple network case: DC quantities (1st transient)

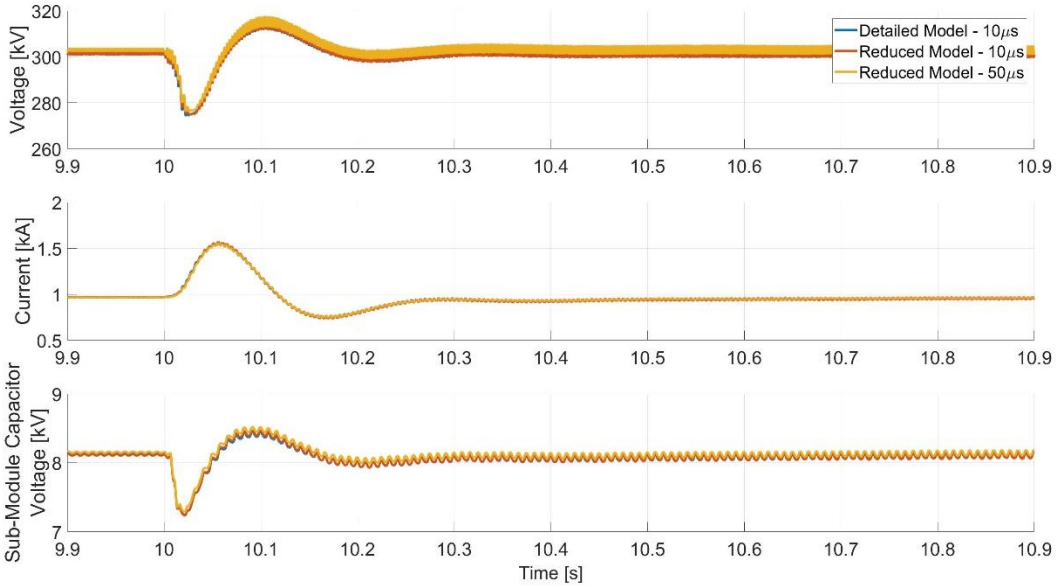

Figure A.6: Simulation results for simple network case: DC quantities (2nd transient)

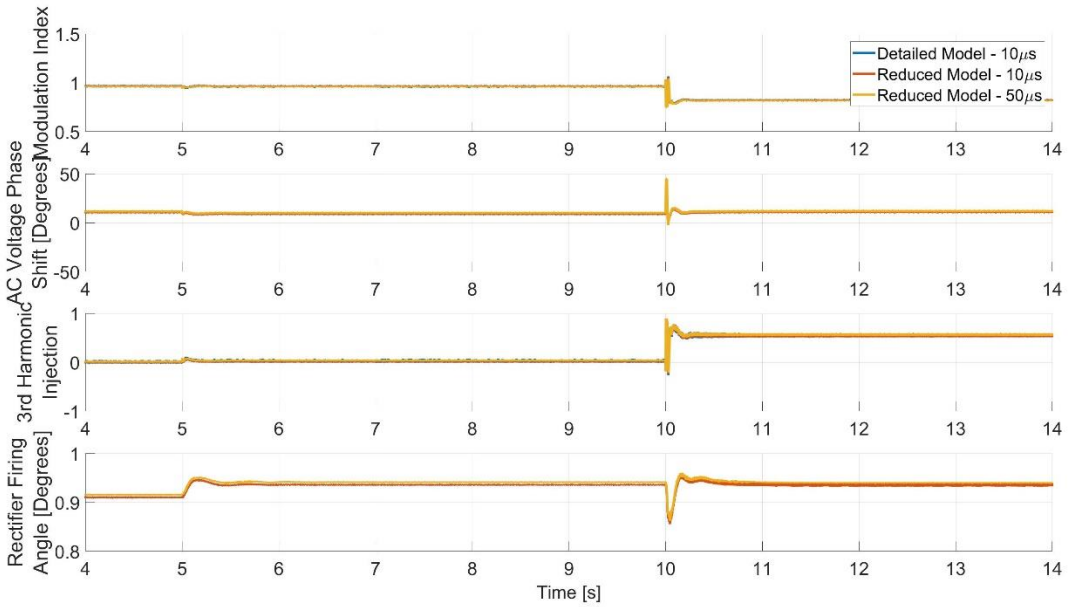

Figure A.7: Simulation results for simple network case: PH-MMC control signals

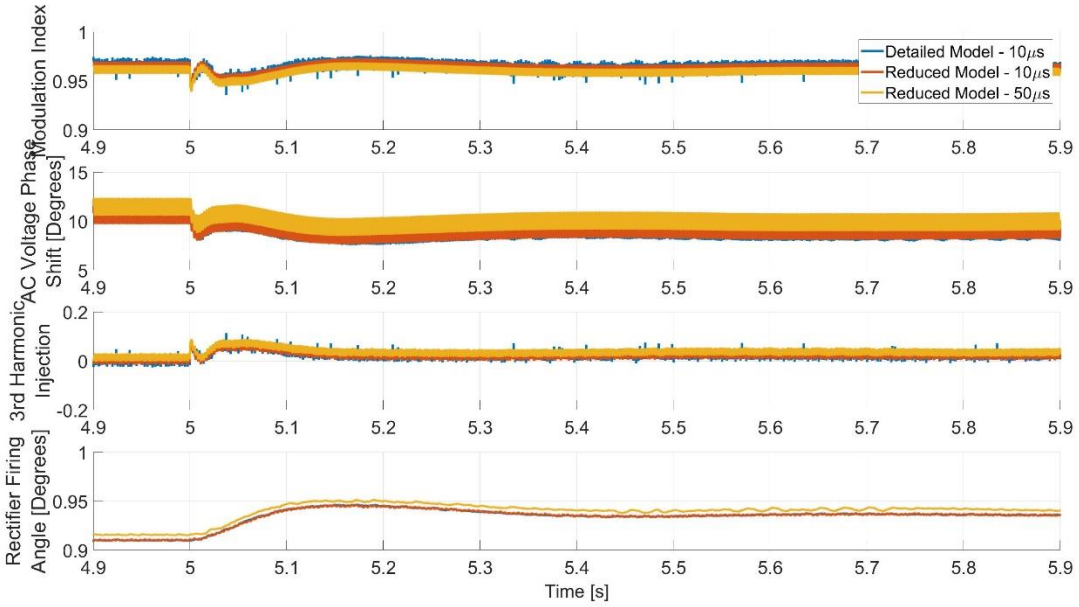

Figure A.8: Simulation results for simple network case: PH-MMC control signals (1st transient)

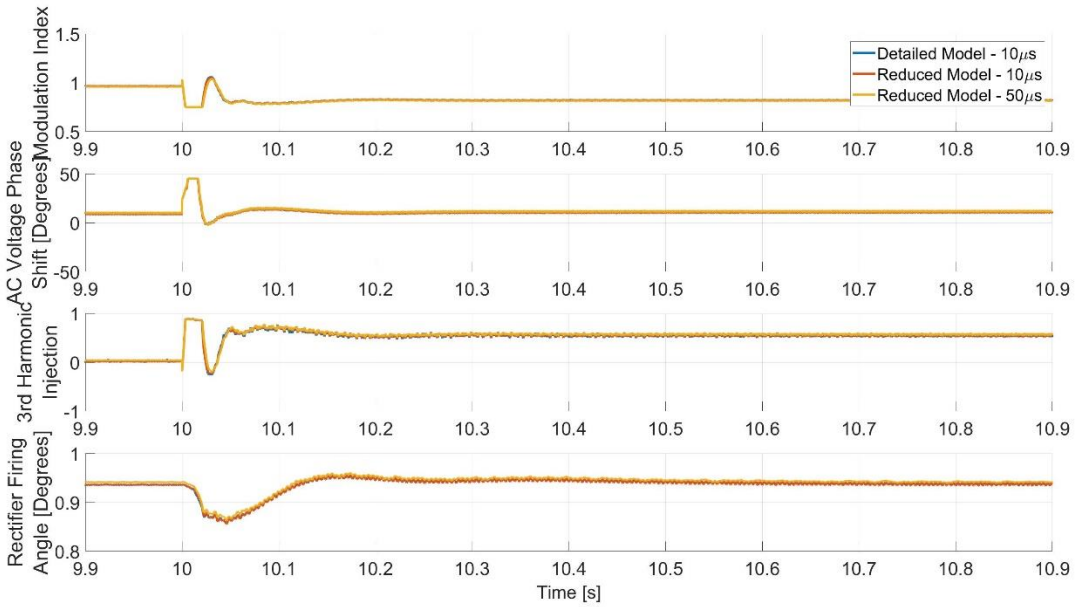

Figure A.9: Simulation results for simple network case: PH-MMC control signals (2nd transient)

B. Dynamic Simulation Results: IEEE 12-Bus System

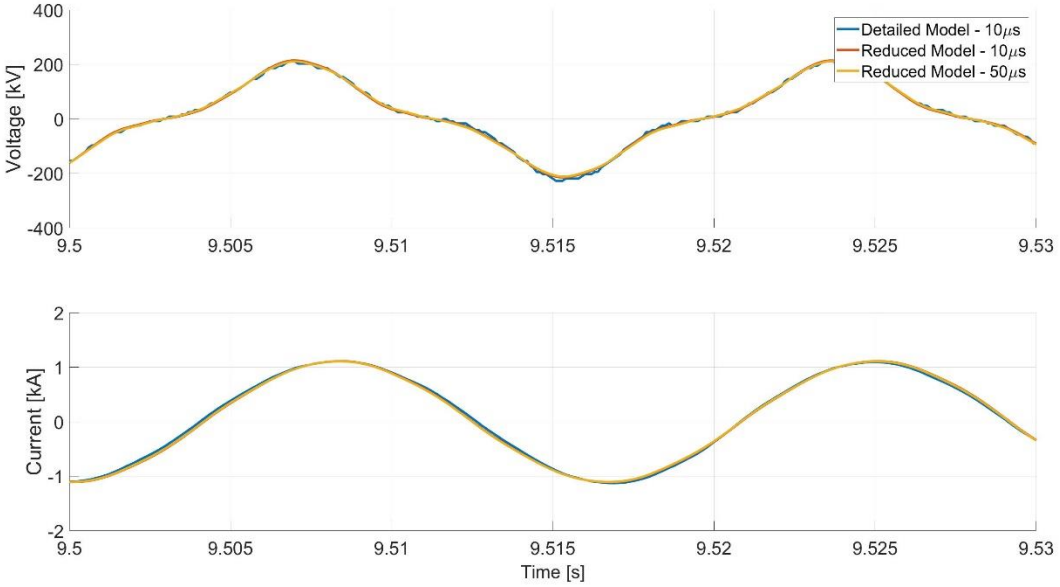

Figure B.1: Simulation results for IEEE 12-bus system: AC waveforms (2nd operating point)

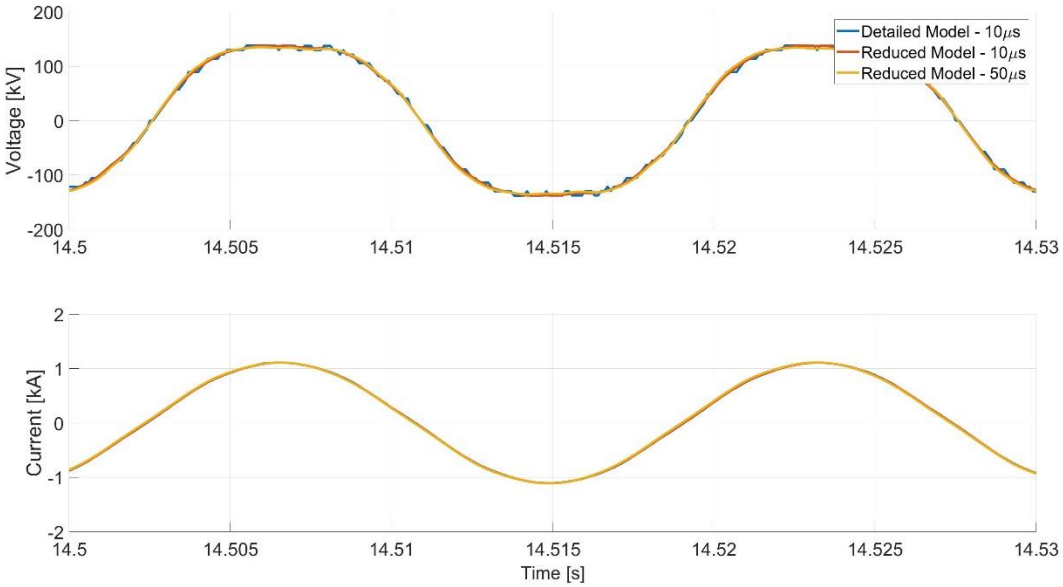

Figure B.2: Simulation results for IEEE 12-bus system: AC waveforms (3rd operating point)

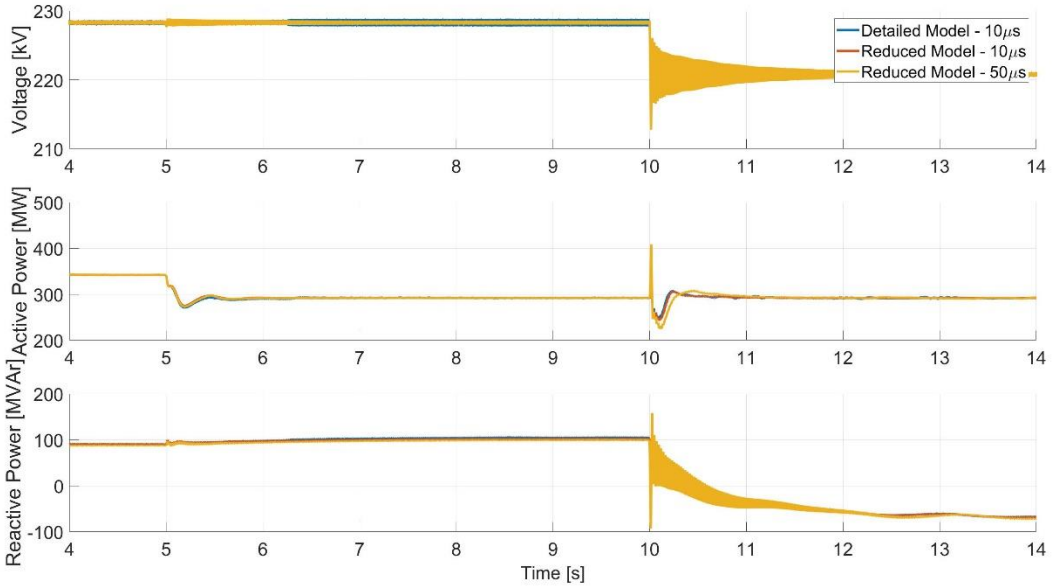

Figure B.3: Simulation results for IEEE 12-bus system: AC grid quantities

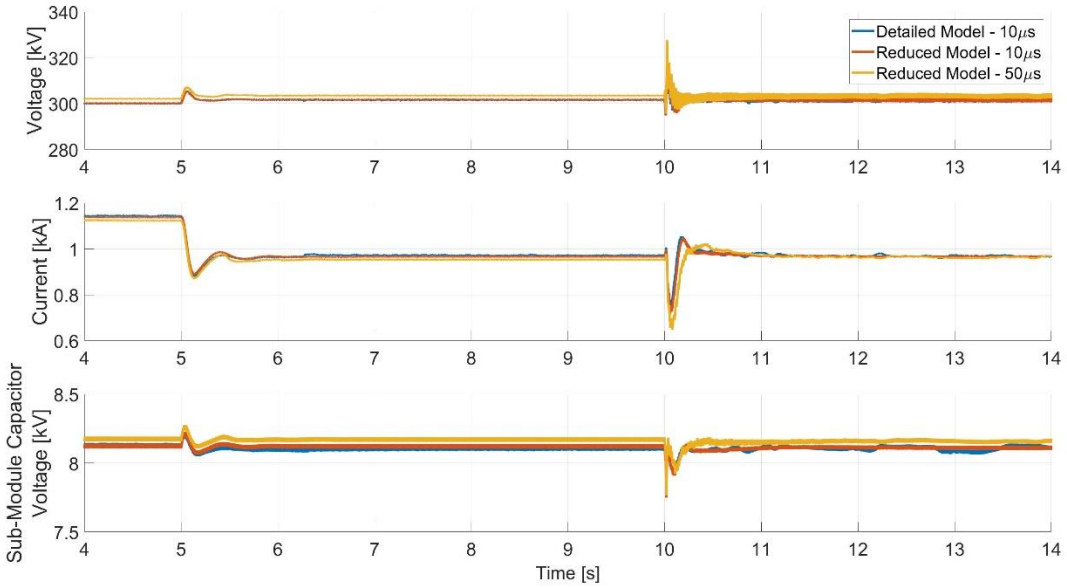

Figure B.4: Simulation results for IEEE 12-bus system: DC quantities

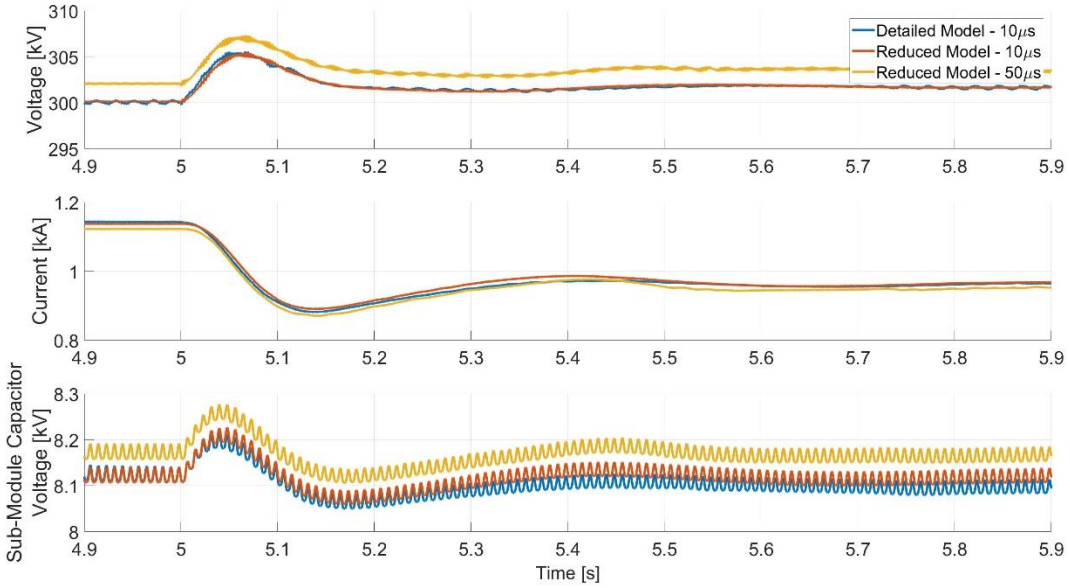

Figure B.5: Simulation results for IEEE 12-bus system: DC quantities (1st transient)

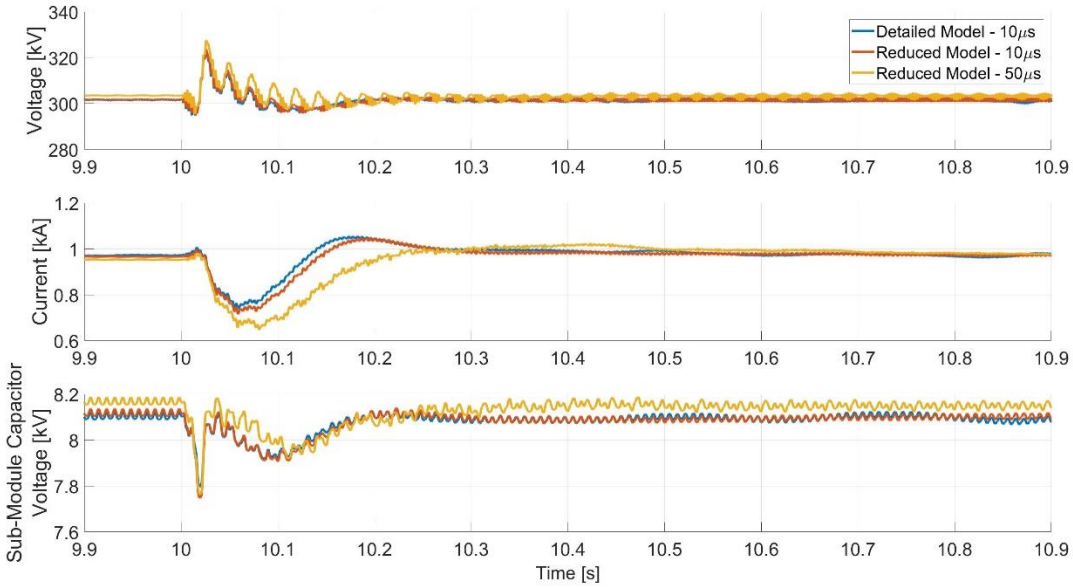

Figure B.6: Simulation results for IEEE 12-bus system: DC quantities (2nd transient)

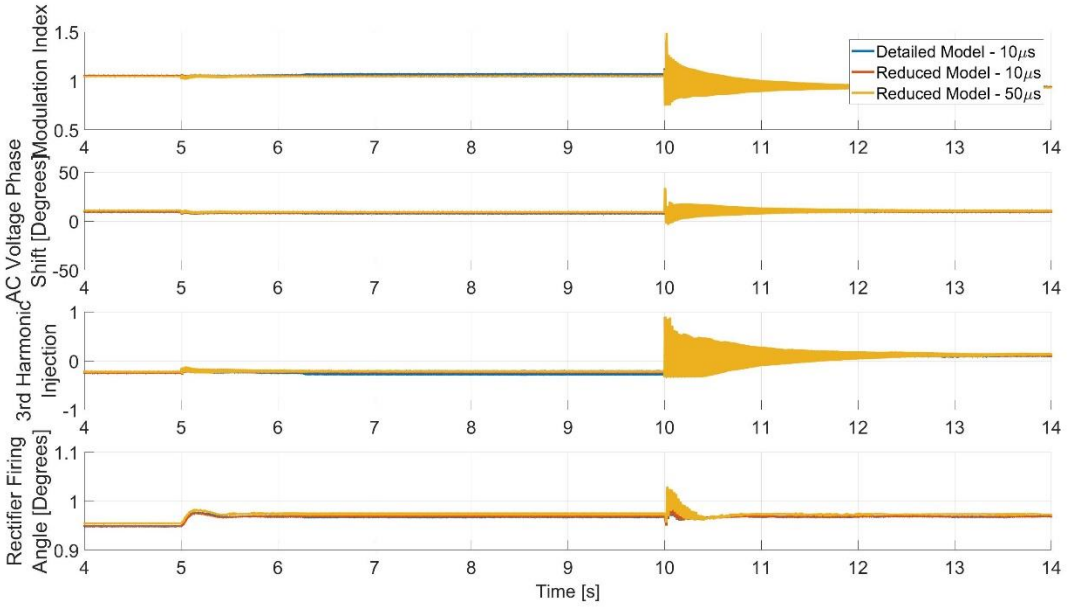

Figure B.7: Simulation results for IEEE 12-bus system: PH-MMC control signals

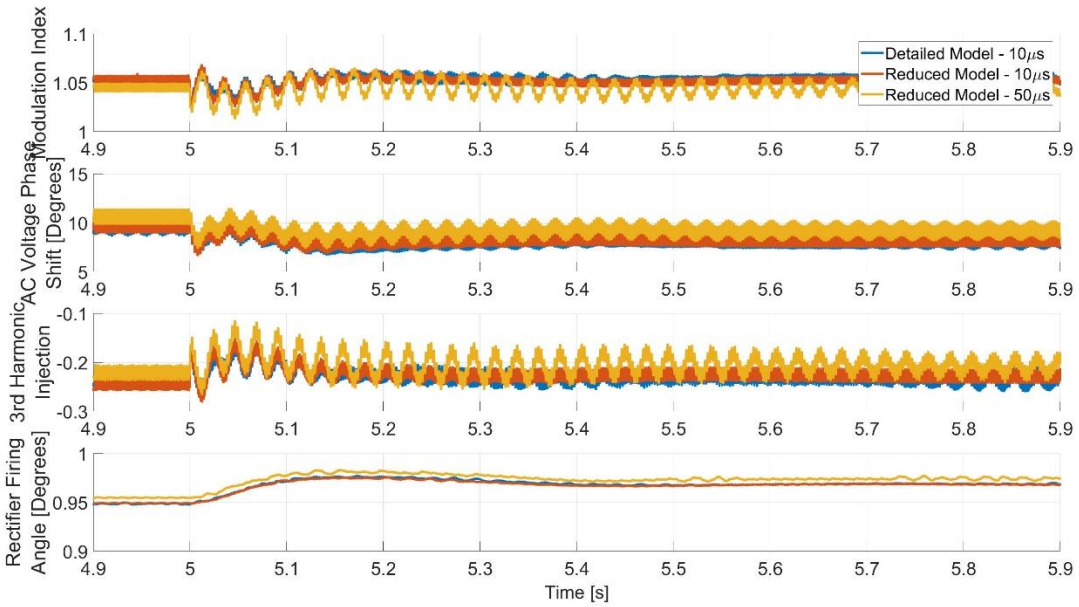

Figure B.8: Simulation results for IEEE 12-bus system: PH-MMC control signals (1st transient)

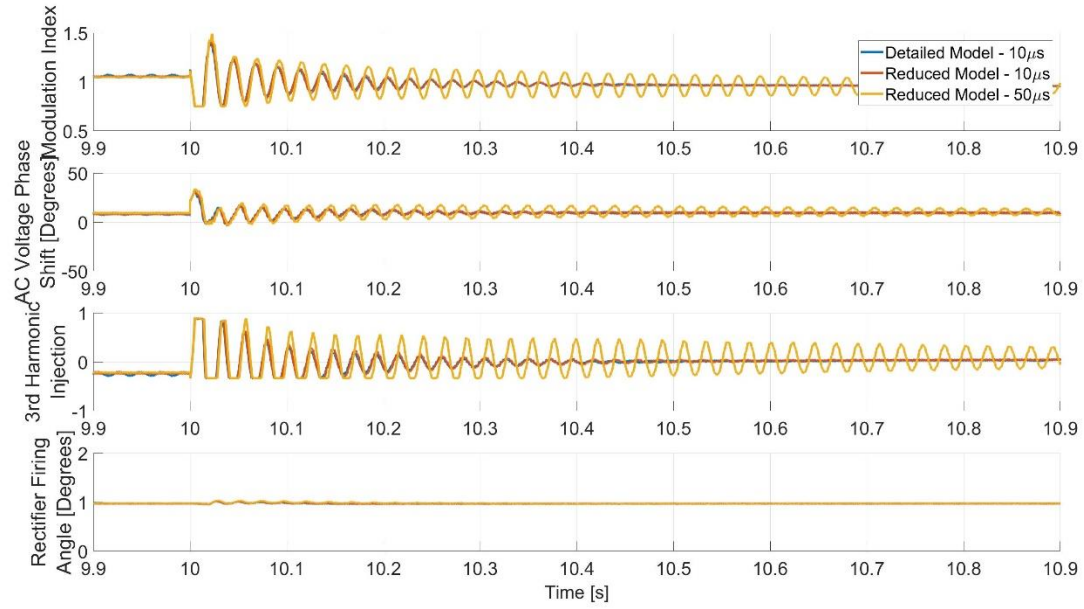

Figure B.9: Simulation results for IEEE 12-bus system: PH-MMC control signals (2nd transient)