Modeling, Analysis, and Control of Circulating Currents in Half-Bridge Modular Multilevel Converters

by

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Abstract

In operating Modular Multilevel Converters (MMCs) the common practice is to eliminate circulating currents using a Circulating Current Suppression Controller (CCSC). This practice reduces converter losses and submodule capacitor voltage ripple; it also allows usage of semiconductors with lower ratings. Although preliminary research has pointed to the possibility of minimizing capacitor voltage ripple or converter losses by injecting circulating currents, little formal analysis has been conducted on how the improvement of one will affect the other, or on how to control the ripple or the losses. This thesis presents a detailed analysis on how to inject a precise amount of circulating currents in order to obtain certain submodule capacitor ripple. A mathematical model that describes the capacitor voltage ripple based on the second-order circulating current contents is used to determine the ripple profile of the converter at a given operating point. Then it is possible to determine what amount of circulating current needs to be injected to obtain a certain ripple. An analysis of how such circulating current injection affects losses is also made. The proposed method is validated using PSCAD/EMTDC simulations, where a high level of accuracy is observed. Validation using a Real-Time Digital Simulator (RTDS) using a Control Hardware-in-Loop (CHIL) scheme is also presented. An implementation in a down-scaled MMC prototype further validates the proposed method. This thesis shows that the optimal operating point (regarding losses and capacitor voltage ripple) for MMCs is not achieved by using a conventional CCSC, as is the common practice today; instead injecting a certain amount of second-order circulating current can reduce both ripple and converter losses simultaneously.

To Laura

who walked with me

every step of the way

"The secret of getting ahead is getting started."

–Mark Twain

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List of Acronyms

CCSC Ciculating Current Suppression Controller

PSCAD Power System Computer-Aided Design

EMTDC Electromagnetic Transient including Direct Current

RTDS Real-Time Digital Simulator

DC Direct Current

AC Alternating Current

HVDC High-Voltage Direct Current

LCC Line-Commutated Converter

VSC Voltage Source Converter

MMC Modular Multilevel Converter

HB Half Bridge

FB Full Bridge

KVL Kirchoff's Voltage Law

PWM Pulse-Width Modulation

PD Phase Disposition

POD Phase Opposition Disposition

APOD Alternate Phase Opposition Disposition

CPS Carrier Phase Shifted

THD Total Harmonic Distortion

NLC Nearest-Level Control

PCC Point of Common Coupling

PLL Phase-Locked Loop

PI Proportional-Integral

PR Proportional-Resonant

PIR Proportional-Integral-Resonant

OP Operating Point

SHC Second Harmonic Controller

SOA Safe Operating Area

EMT Electromagnetic Transients

MCU Mirocontroller Unit

ADC Analog-to-Digital Converter

MSPS Mega-Samples Per Second

DFIG Doubly-Fed Induction Generator

PM Permanent Magnet

Chapter 1

Introduction

1.1 Background

As the human civilization has evolved, there has been a growing need for using and transmitting energy. From the simple act of gathering firewood thousands of years ago, to charging up smart phones today, the society relies on energy.

When the commercial use of electricity started in the 19^{th} century, the early direct current (DC) systems transmitted power over short distances, as generating stations were close to the consumers. Thus a large number of these stations were needed as more and more consumers demanded this new commodity. Lack of reliable technology required to change voltage levels, among other problems, proved impractical to transmit electricity in the DC form in those early days.

When alternating current (AC) transmission showed its superiority in that context, it became possible lo relocate the generating stations further away from cities and populated areas and start meeting the growing demand. Transmitting bulk electric power over long distances was initially achieved using AC transmission.

Over the previous century the always-increasing demand for power has challenged engineers to design power lines that could bear high loading while maintaining stability. The

increase in transmitted power eventually translates into increasing the transmission voltage, which in turn translates into larger and costly transmission equipment. There is a certain point (closely related to the line's length and power capacity) above which it is more feasible to use DC transmission over AC transmission. The development of new technologies (specially in the last half-century) has allowed High Voltage Direct Current (HVDC) transmission technology to gain technical and economical appeal. HVDC offers several benefits over AC transmission and at the same time poses great challenges.

Some of the HVDC transmission benefits are: (i) it allows to transmit more power using the same line than it would using AC; (ii) it allows to interconnect asynchronous systems; (iii) it allows transmitting power over longer distances; and (iv) it has lower losses (as compared to the same capacity using an AC line) [1].

On the other hand, the use of HVDC systems requires the use of converters that are expensive and usually complex to control. For some HVDC converter topologies, extinction of DC fault currents becomes an issue as the DC breaker technology is still in its early stages [2, 3]. Nonetheless, the use of HVDC has been steadily increasing worldwide and today it is a common option for interconnections among power systems and/or renewable generation sources to the power system.

For several decades, Line Commutated Converters (LCCs) were the preferred technology to build HVDC systems. Today, LCCs are a mature and reliable technology. Nevertheless, there are associated drawbacks, including (i) they operate with a low power factor; (ii) they are not best suited for operations involving a black start; (iii) they need to be connected to a relatively strong power system; and (iv) these converters have only one degree of controlability [4].

Over the last couple of decades, thanks to further advancements in semiconductor devices and converter technologies, there has been a great deal of research and development of a type of Voltage Source Converter (VSCs) for HVDC transmission systems. The Modular Multilevel Converter (MMC) was introduced in the early 2000's by Prof. Marquardt [5]. Today

it is considered as the state-of-the-art VSC topology due to its modularity and scalability, small footprint, high efficiency, and improved harmonic performance [6, 7].

When operating an MMC there are many variables that need to be properly controlled to ensure correct operation of the converter. Converter controllers can be divided into two main groups of system-level and converter-level controls. The first group relates to the behavior of the converter within the power system it is connected to. Examples include power flow and voltage control at the point of common coupling (PCC).

Converter-level controls regulate the internal operation of the converter and define how switchings are carried out for different purposes. Converter-level controllers also impact critical operating aspects of the converter such as its efficiency and submodule capacitor voltage ripple. These controls require the implementation of several algorithms for modulation, submodule capacitor voltage balancing, and circulating current control [7–10].

When operating an MMC, how to approach and deal with circulating currents is a decision that needs to be made. The most common practice is to completely eliminate them as this will reduce semiconductor ratings, lower converter losses, and reduce capacitor voltage ripple. Nonetheless, a great volume of research has been made to investigate the use of circulating currents to enhance the MMC performance. Most of this existing research aim at individually minimizing the submodule capacitor voltage ripple or converter losses, but generally they do not consider how one affects the other.

1.2 Problem Definition

Previous work has primarily focused on minimizing the capacitor voltage ripple using circulating currents. For example, the work presented in [11] minimizes ripple by optimizing second-order harmonic circulating current injection; similarly a fourth-order component is also included in the modulating waveform in [12]. The downside of this approach is that the optimization algorithm is reported to take a long time (several days) to converge; also this

work does not present any suggestion to evaluate how this approach affects converter losses. A similar strategy is reported in [13–16] where the main goal is to minimize ripple.

Another approach consists of varying the magnitude and phase angle of a second harmonic component in the modulating waveform and studying how such variations affect the converter's behavior. Such an approach is presented in [17]. This method allows for a controlled reduction in the ripple, but it relies on extensive simulations to determine the magnitude and phase angle of the second-order modulating component that would reduce the ripple to a certain value at any operating point. This work presents an estimate of how the variations in ripple may affect losses using an analytical model.

There is no previous work (at least to the knowledge of the author) that presents a method to gradually reduce capacitor voltage ripple in a MMC, nor is there an analysis on how this will affect converter losses. This thesis uses an existing, straightforward analytical method to calculate capacitor voltage ripple while considering how second-order circulating currents flow within the MMC arms. This method allows obtaining a high-accuracy surface that describes the capacitor voltage ripple profile at any given operating point as a function of the second-order circulating current parameters. A look-up table is suggested to control the capacitor voltage ripple to the desired levels. Finally, a simulation-based loss analysis is conducted using the approach presented in [18], where the semiconductor's model is augmented in an EMT simulator to include switching and conduction losses.

1.3 Thesis Motivation

Since MMCs are becoming increasingly popular in power systems, it is desirable to operate them such that their performance is optimized. Additionally, reducing capacitor voltage ripple can be used to reduce the size of the capacitors and therefore, reduce the converter's footprint and cost. If losses can be further reduced beyond the point where circulating currents are completely suppressed (as is the common practice), the efficiency of the converter

will be also increased. If these two features could be reduced at the same time, the overall efficiency of the MMC will be increased. It would be necessary to analyze what trade-offs this approach imposes when selecting semiconductors, since the peak current values will be affected by the current injection.

1.4 Thesis Structure

The remainder of this thesis is structured as follows: Chapter 2 introduces the operating principles and control strategies for MMCs along with some of their most common control algorithms. Chapter 3 presents the mathematical model used to analytically calculate the capacitor voltage ripple and describes its implementation. Chapter 4 presents validation results including the loss analysis and experimental results. Chapter 5 concludes the thesis by discussing its contributions and conclusions.

Chapter 2

Operating Principles of the MMC

This chapter presents the structure of the MMC in detail as well as its operating principles and associated control schemes.

2.1 MMCs

A schematic diagram of a three-phase MMC is shown in Fig. 2.1. The main building block of the converter is the submodule. The use of building blocks allows one to easily rate the MMC, in terms of its power and voltage, for the required application by selecting the proper type of submodule and its characteristics.

Each arm is formed with N submodules connected in series along with an inductor, and two arms in series form a phase of the converter. The arm inductors are used to absorb any mismatch in the arm's voltage to allow compliance with Kirchhoff's Voltage Law (KVL); they also limit the rate of rise of the fault current through the arm. The output node of each phase is its middle point, where the upper and lower arm inductors meet.

The converter is operated so that the output node of each phase, i.e., V_{A}, V_{B} or V_{C}, delivers an AC voltage. This is achieved by varying the number of submodules inserted in each arm. At every instant of time there are N submodules inserted and N submodules

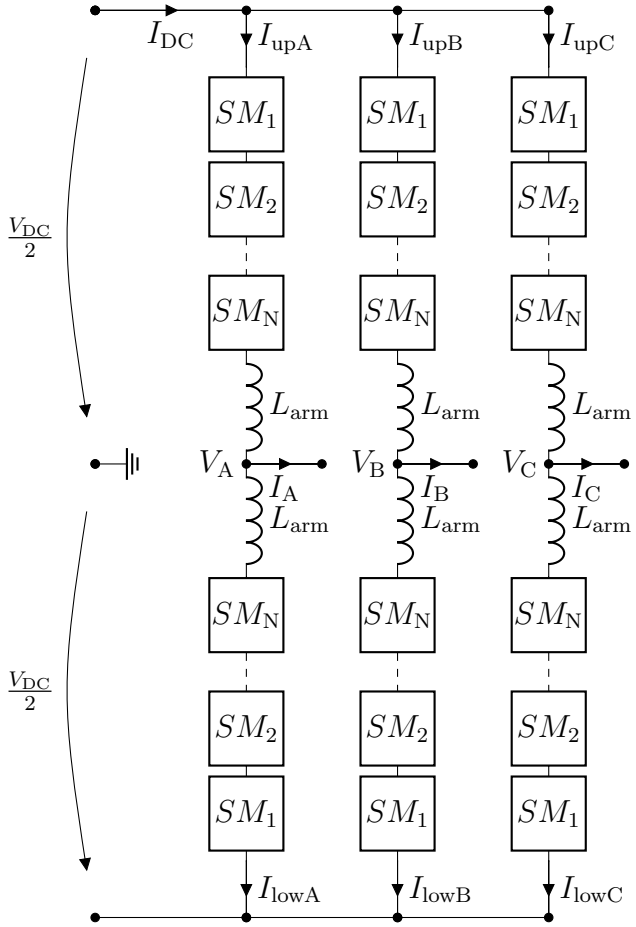


Figure 2.1: Three-phase MMC.

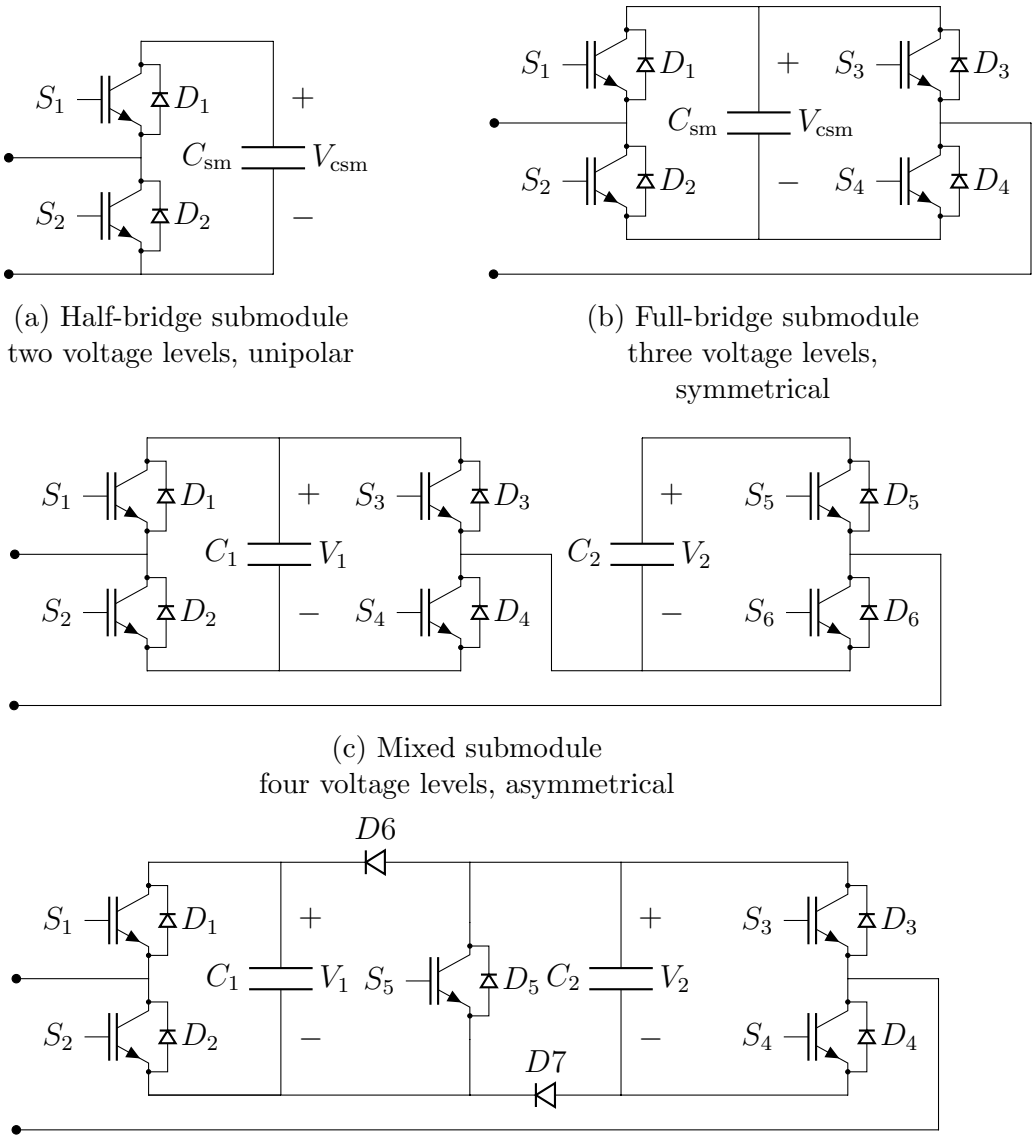
bypassed in each phase [1]. The number of inserted submodules in each arm varies from 0 to N[1] in every cycle; therefore, the output voltage of each phase varies between $\pm V_{\mathrm{DC}}/2$ in steps of V_{csm}, which is ideally equal to V_{DC}/N.

2.2 Submodule Types

There are many different submodule configurations available for use in MMCs [8,19], among which the two most common ones are Half-Bridge (HB) and Full-Bridge (FB) types. Fig 2.2 shows an example of some of these submodule topologies. The simplest topology, the Half-Bridge (HB) outputs two voltage levels of zero or V_{csm}, whereas other topologies output three

[1] This is true only under certain operating conditions that will be discussed later.

levels or more. Accordingly the submodules can be categorized as unipolar, symmetrical, or asymmetrical according to their output voltage levels. The number of switches and capacitors must also be considered when selecting the proper submodule as it will affect its reliability, losses, physical size, and cost.



(a) Half-bridge submodule
two voltage levels, unipolar

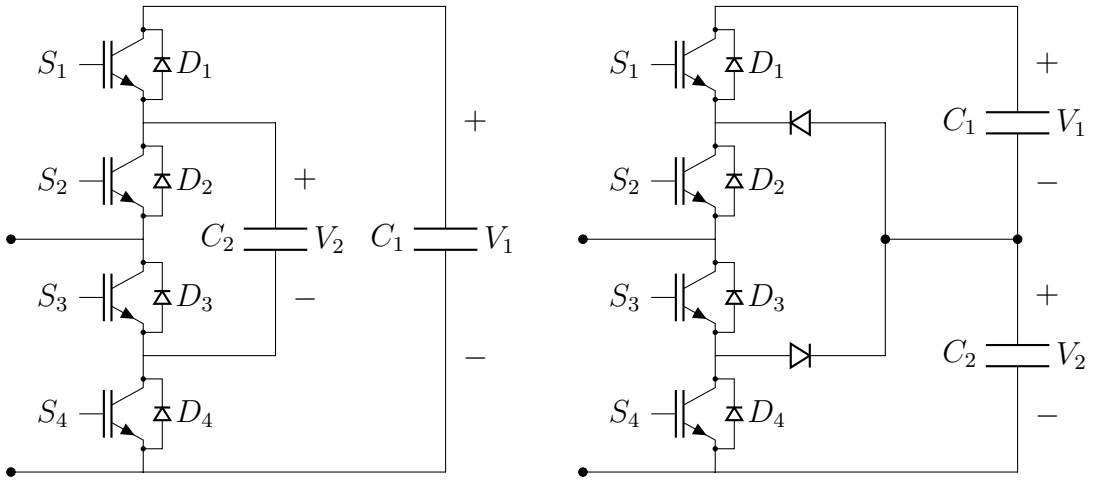
(b) Full-bridge submodule
three voltage levels,
symmetrical

(c) Mixed submodule
four voltage levels, asymmetrical

(d) Clamp-double submodule
four voltage levels, asymmetrical

Figure 2.2: Various submodule topologies.

Most of the research on MMCs is based on converters using either HB or FB submodules since these are the simplest among the available submodules. The FB submodule has a



(e) Three-level floating capacitor
three voltage levels, unipolar

(f) Three-level neutral-point clamped
three voltage levels, unipolar

Figure 2.2: Various submodule topologies (cont.).

particular advantages over the HB submodule: its output can be either positive, zero, or negative voltage, and as such, can be used to limit fault currents. Nevertheless, the major drawback of using a FB submodule is its increased cost and size. These two factors and the better reliability of HB submodules make them the most commonly used topology for MMCs. The work presented in this thesis uses MMCs with HB submodules. The next section will explain the basic operating states of this submodule.

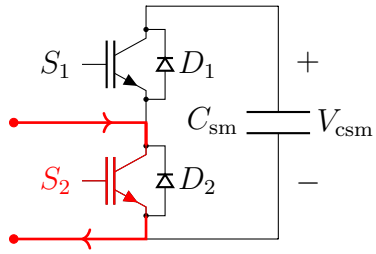
2.2.1 Half-Bridge Submodules

The HB topology is shown in Fig 2.2a. Its output voltage can be either V_{csm} or zero (the voltage drop across the semiconductors is negligible compared to V_{csm}, as such it is ignored).

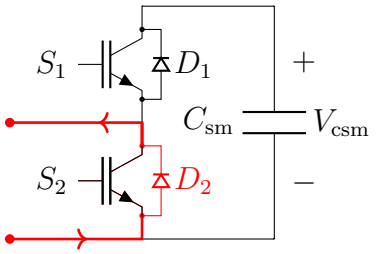
If a SM is to be bypassed, the upper switch will be blocked and the lower one will receive a pulse on its gate terminal. The current will flow through the lower diode or the lower switch depending on its direction. Disregarding current direction the output voltage will be zero. This state is represented in Figs. 2.3a and 2.3b.

If a SM is to be inserted, the upper switch will receive a pulse on its gate terminal whereas

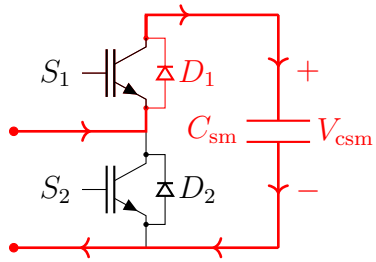
the lower switch will be blocked. The current will flow either through the upper switch or diode depending on the current direction. The output voltage will be V_{csm}. This state is represented in Figs. 2.3c and 2.3d.



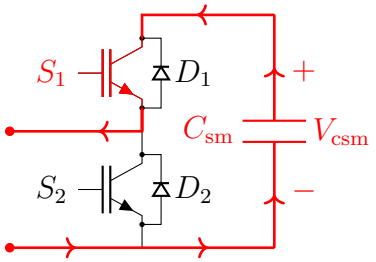
(a) Bypassed (positive current)



(b) Bypassed (negative current)



(c) Inserted (capacitor charges)



(d) Inserted (capacitor discharges)

Figure 2.3: Half-bridge submodule's operating states.

Another state is also possible (not shown) where both switches S_1 and S_2 are fired, but this is a prohibited state as it will short circuit the submodule capacitor. The following table summarizes the previous explanation.

Table 2.1: Half-bridge submodule states

S1	**S2**	**Current direction**	**State**
OFF	ON	Positive	Bypassed
OFF	OFF	Negative	Bypassed
OFF	OFF	Positive	Inserted
ON	OFF	Negative	Inserted
ON	ON	N/A	Short Circuit

The main drawback of this submodule is that it does not have any inherent fault current

limiting ability. This submodule has a capacitor with a theoretical nominal voltage of:

$$V_{\text{csm}} = \frac{V_{\text{DC}}}{\text{N}} \tag{2.1}$$

where V_{DC} is the DC-link voltage, and N is the number of submodules in each arm.

2.3 Modulation Techniques

In order to operate all the submodules such that the output voltage is an AC waveform, a modulation technique must be used. This section presents some of the available modulation techniques.

2.3.1 Pulse-Width Modulation

Basic Carrier-Based PWM Methods

Pulse-width modulation is a popular technique to drive switches in a large class of converters. If a single switch is to modulate a sinusoidal waveform, the most common approach is to compare a triangular wave to an AC reference.

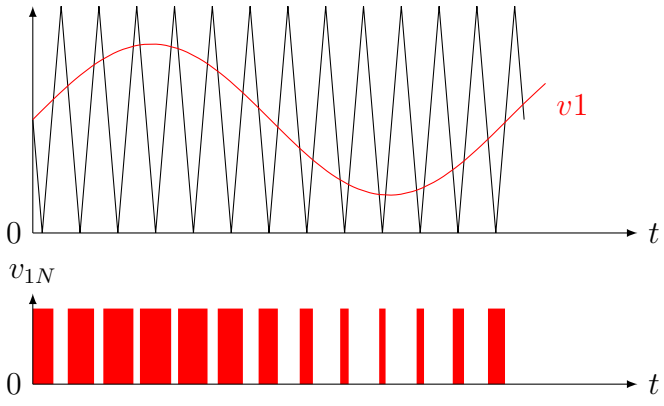


Figure 2.4: PWM modulation principles.

Fig 2.4 shows how PWM works: the upper graph shows a sinusoidal wave, known as the modulating signal or the reference, that is compared with a higher frequency triangular

waveform known as the carrier. The lower graph shows the output of this comparison; when the reference is higher than the carrier, the switch will be ON; otherwise, it will be OFF. By using this firing signal to drive the switch, the low-frequency contents of the output will resemble the reference waveform. The higher the frequency of the carrier the higher the resolution of the modulated output, and the higher the switching losses.

Carrier-Based PWM Techniques for MMCs

A similar single-reference approach, as the one previously shown, can be used for driving MMCs. Nevertheless, small changes need to be implemented. Since there are a large number of submodules in MMCs, and each submodule contains multiple switches, the output of the comparison is used to determine the number of SMs that need to be inserted or bypassed. To specifically determine which switch to fire in a submodule, other factors need to be considered (see Section 2.2.1). The output waveform is obtained by comparing a modulating signal with the carriers. These techniques can be divided into two groups [8, 20]:

Carrier Disposition PWM

There are N identical triangular carrier waveforms displaced symmetrically along the vertical axis where the amplitude of each carrier is $1/N$ p.u.. These techniques are further classified as:

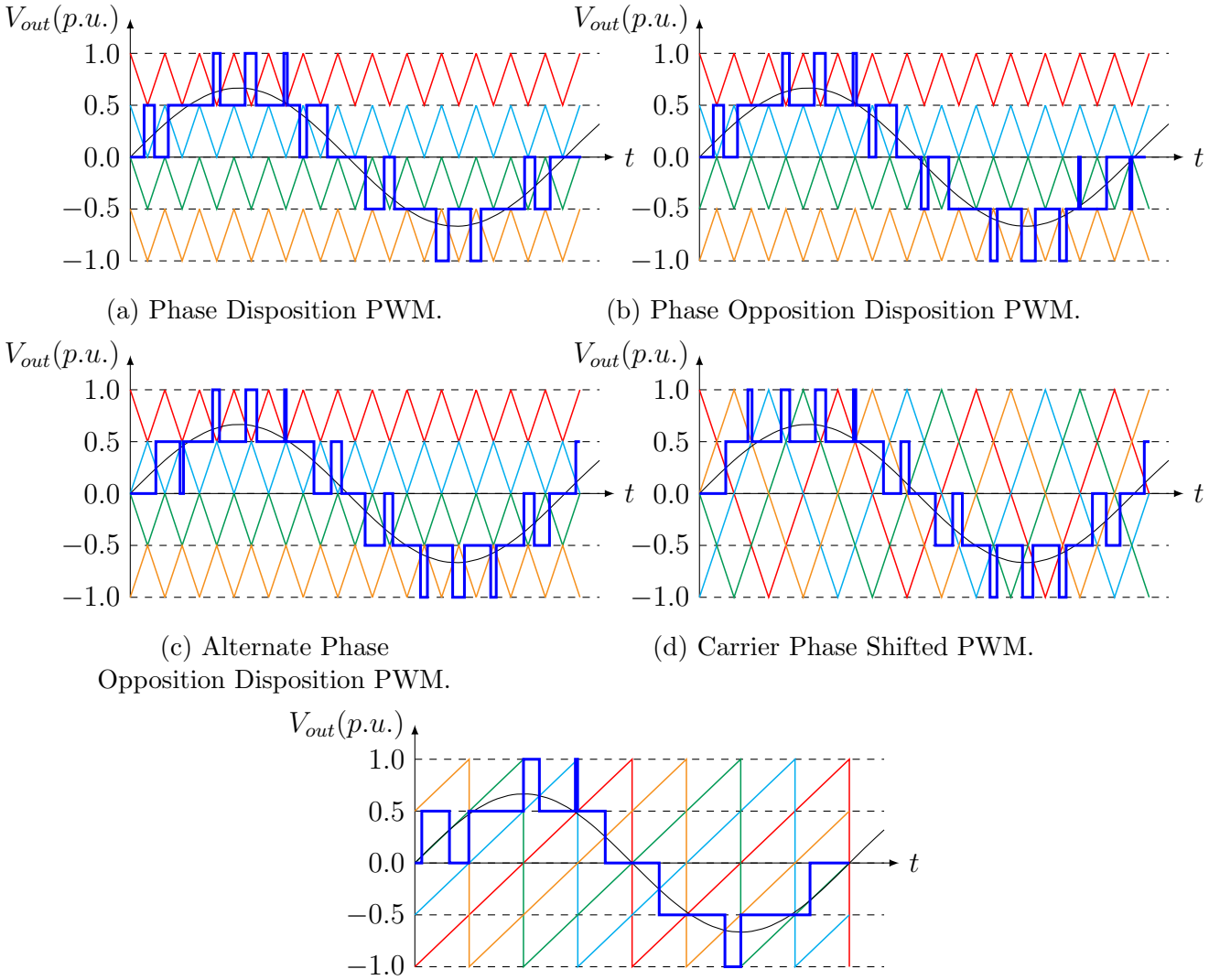
- Phase Disposition (PD), shown in Fig. 2.5a, where all carriers are of the same phase.
- Phase Opposition Disposition (POD), shown in Fig. 2.5b, where carriers in the negative y-axis are 180° phase shifted with respect to those in the positive y-axis.
- Alternate Phase Opposition Disposition (APOD), shown in Fig. 2.5c, where carriers are 180° phase shifted consecutively with respect to one another.

Subharmonic Techniques

There are $2N$ identical triangular carrier waveforms displaced symmetrically with a phase

shift of $360°/(2N)$ with respect to each other, where the peak-to-peak amplitude of each carrier is 2 p.u.. These techniques are further classified as:

- Carrier Phase Shifted (CPS) PWM, shown in Fig. 2.5d, where the carriers are triangular waveforms.
- Sawtooth rotation PWM, shown in Fig. 2.5e, where the carriers are sawtooth waveforms.



(a) Phase Disposition PWM.

(b) Phase Opposition Disposition PWM.

(c) Alternate Phase Opposition Disposition PWM.

(d) Carrier Phase Shifted PWM.

(e) Sawtooth carrier PWM.

Figure 2.5: Various PWM strategies.

It has been reported that the overall Total Harmonic Distortion (THD) level obtained

with these PWM methods are similar [21]. Also, for the same number of switching actions, a comparison between the PD PWM and the subharmonic techniques, the PD PWM ones yield slightly better THD [22].

Since PWM methods use high-frequency carriers, it translates into a large number of switching actions, which causes high losses as compared with low switching frequency methods. Some PWM-based algorithms have been reported to aim at reducing switching events. The work presented in [23] proposes varying some capacitors' reference voltage to ensure they remain inserted longer, thus avoiding unnecessary switching. Although this method successfully reduces switching events, it produces an increase in capacitor voltage ripple and thus higher THD levels. Other methods that use lower switching frequencies, are presented in the following sections.

Space-Vector PWM Methods for MMC

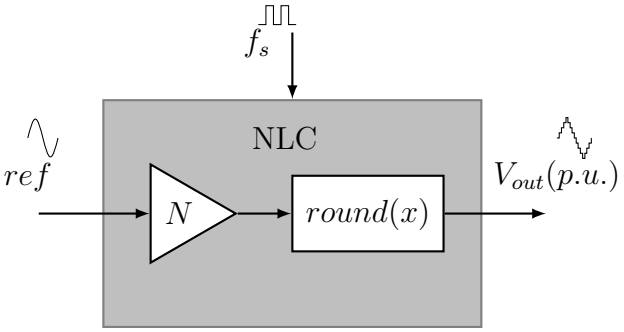
Space-vector PWM is another modulation technique that was initially considered for controlling MMCs [5]. This method is reported [24] to provide flexibility to optimize switching waveforms. Its main disadvantage is the implementation complexity, which makes this method unsuitable for MMCs with more than 5 SMs per arm . This is due to the fact that the controller requires calculating N^3 switching states, and $6(N-1)^2$ triangles in the space-vector diagram, which greatly increases the computational load. These two limitations make this method rarely applicable in MMCs.

2.3.2 Nearest-Level Control

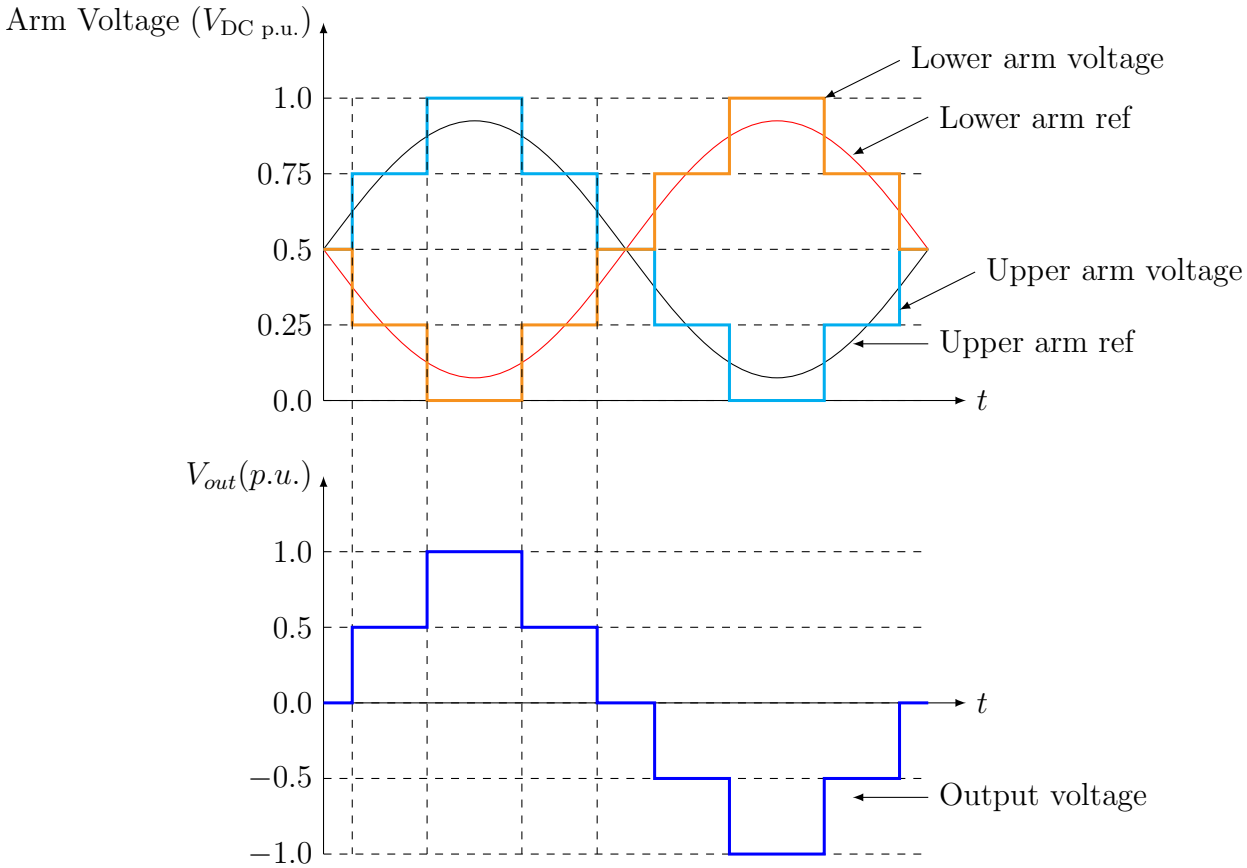
An alternative method to carrier-based PWM methods is the Nearest-Level Control (NLC) method. Its main advantage is that it is simple to implement. NLC works by sampling the reference waveform at high frequency and approximating it with the nearest available levels provided by the discrete submodule steps [25], thus greatly reducing the switching events.

Fig. 2.6a shows a block diagram describing NLC. The reference waveform (in p.u.) is

sampled at the sampling frequency, the sampled value is multiplied by N and rounded to the nearest integer, thus determining the number of submodules that need to be inserted. The output from this algorithm (shown in Fig.2.6b) is a staircase-like sine wave resembling the reference waveform.



(a) NLC's conceptual diagram.



(b) NLC resulting waveform.

Figure 2.6: NLC method.

When using this method, it is necessary to ensure that the sampling frequency is high

enough to guarantee that the output voltages will not change more than one level at each step. This will avoid unnecessarily increasing the output voltage's THD. For this matter, the minimum required sampling frequency can be calculated as [25]:

$$f_0 = \pi N f_\mathrm{s} \tag{2.2}$$

where f_s is the system's frequency.

The number of submodules to insert in each arm (the output of the NLC algorithm) can be calculated using the *round* function as [25]:

$$round(x) = \begin{cases} floor(x), & x < floor(x) + 0.5 \\ ceil(x), & x \geq floor(x) + 0.5 \end{cases} \tag{2.3}$$

where $floor(x)$ is the largest integer lower than x and $ceil(x)$ is the lowest integer higher than x.

The output voltage is obtained by subtracting the lower arm voltage from the upper arm voltage, as seen in Fig. 2.6b.

The higher the number of submodules in an MMC, the higher the resolution of the output voltage and thus the lower its THD. The work in [21] reported that with at least 16 SMs, the THD of the resulting voltage will be less than 5% when using NLC. A similar conclusion is presented in [26] where a comparison between PWM methods and NLC is made while varying the number of SM from 4 to 40. This further shows that NLC is a suitable modulating algorithm for MMCs with an adequately large number of submodules.

NLC Variation

The work reported in [27] presents a variation on the NLC method where an improved THD performance is observed. This is accomplished by modifying the round function, where the round threshold changes from 0.5 to 0.25 for the lower arm and from 0.5 to 0.75 for the upper

arm, shown in Fig. 2.7. The result can be described as delaying the switching events of the lower arm submodules and advancing the switching events of the upper arm submodules. The outcome of such modification is a higher resolution in the output voltage and current waveforms, since the number of output levels is increased from $N+1$ to $2N+1$. The same number of switching events as with the original NLC method is maintained, thus no increase in the switching losses is expected.

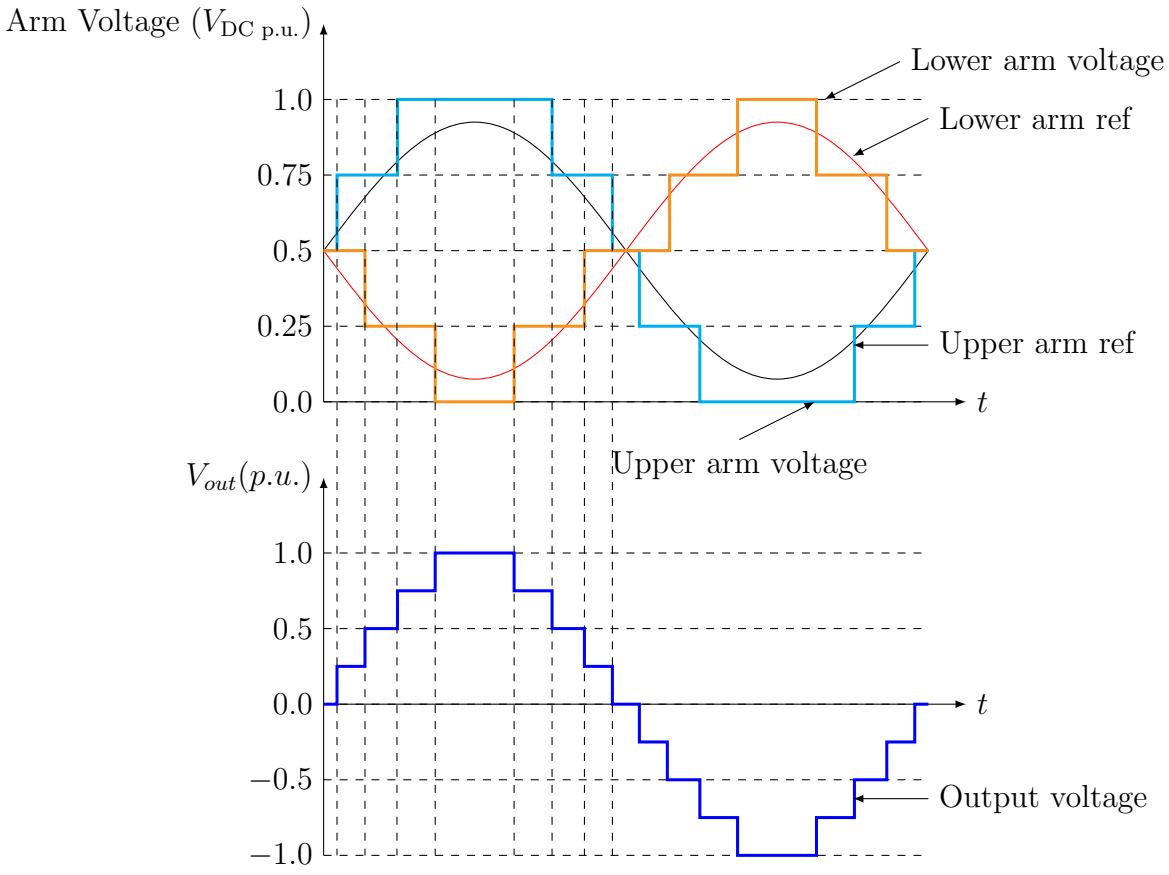


Figure 2.7: Modified NLC.

The main drawback of this method is that it considerably increases the voltage drop across the arm inductors, which in turn translates in higher circulating currents; this refers to harmonics higher than the second one, since CCSC is used to eliminate the second order circulating current [27]. Also, this method does not report considerable improvement in capacitor voltage ripple levels.

Other hybrid modulation techniques that combine carrier-based PWM and other PWM techniques along with NLC, have also been reported [28]. These techniques increase the overall complexity of operating the converter at the expense of modest improvements in either switching losses or hardware complexity. Therefore, due to its simplicity, ease of implementation, low switching losses, and similar THD levels compared with other methods, the NLC method described in subsection 2.3.2 is used for the remainder of this thesis.

2.4 Capacitor Voltage Balancing Algorithms

The MMC is operated under the assumption that all capacitor voltages are the same. As shown in Fig. 2.6b the number of inserted submodules varies throughout each cycle. This causes the voltages in the inserted submodules to change with respect to the ones that are bypassed (assuming that all capacitor's voltages were initially the same). The modulating strategies previously described help determine the number of submodules that must be inserted/bypassed to achieve the desired output voltage, but do not specify which specific submodules within the arm should be inserted/bypassed. In order to address this problem, an algorithm to balance all capacitor's voltages and keep them close to their rated value is needed. Many algorithms have been developed to address this problem, some of which will be presented next.

2.4.1 PWM-Based Algorithms

A method based on PWM modulation was proposed in [29]. Using PWM-based control to determine when each submodule should be inserted, a proportional-integral (PI) controller is implemented for each submodule capacitor based on two control loops: averaging and balancing. For the averaging loop, each capacitor voltage follows the average voltage of all other capacitors in the same arm, whereas the balancing loop modifies the voltage reference for the arm based on the arm's current direction. This method relies on the use of PWM

control schemes for implementation.

The method proposed in [30] uses a balancing algorithm based on the CPS-PWM scheme to control the high frequency components in the arm currents. The proposed balancing method is used to determine the appropriate PWM pulses for each SM. Its main advantage is that it does not require measuring the arm currents, which simplifies the implementation; whereas its main drawback is that it specifically requires CPS-PWM for implementation.

2.4.2 Predictive Control Methods

The method proposed in [31] uses a predictive strategy to simultaneously control the AC-side currents, regulate the SMs capacitor ripple and eliminate the circulating currents. This is achieved by developing a discrete-time model of the system for a one-step forward prediction of the MMC variables, defining a cost function according to the control objectives, and evaluating such function for all possible switching states of the converter. Finally, the switching state that yields the best switching condition is selected. The computational load of this method increases greatly as the number of submodules in the converter increases [32], which makes it impractical to implement in real-time with a real converter. The work in [32] presents improvement over this method by using a sort function and measuring the arm currents.

2.4.3 Sorting and Rotating Algorithm

The sorting and rotating algorithm described in [33] is extensively used. The algorithm is simple and is based on the following principle: when the current in an arm is positive, and a submodule is inserted, it will be charged; if the current were negative, the inserted submodule will be discharged; if a submodule is not connected, its charge will not vary. To implement this algorithm the capacitor voltages in each arm are measured and sorted in descending order. When the modulating algorithm requests for a switching event, if the current is positive, the least charged capacitors will be connected, and vice versa if the current were

negative. Therefore, the algorithm ensures that all capacitor voltages are kept close to each other.

Although, as seen so far, the output voltage of the MMC varies in steps of V_{csm}, it does not necessarily mean that only one submodule will be inserted/bypassed at each switching event. When implementing this sorting and rotating algorithm, several submodules may be inserted/bypassed so as to keep the overall voltage difference as small as possible; therefore, a certain ripple tolerance band should be set so as to avoid unnecessary switching events.

The work in [34] proposes a variation of the previously mentioned algorithm. It consists of inserting/bypassing only one SM submodule every time a switching action is required[2]. If the number of inserted SMs needs to increase and the arm current is positive the least-charged capacitor will be inserted; if the arm current is negative the most-charged capacitor will be inserted. The same procedure will be followed if the number of bypassed submodules increases. If a transition in the output voltage is not required and the voltage difference between the available capacitors is less than a fixed tolerance, no capacitor will be inserted/bypassed. This algorithm successfully reduces the number of switching events and speeds up the control by not requiring a sorting function. It is reported to have been tested on MMCs with a large number of submodules and redundant submodules [34].

A similar approach is used in [23] where a higher tolerance is used to compare the most and least charged capacitors with the inserted/bypassed ones. This method was validated in MMCs with a low number of submodules (MMCs with 12 SMs per arm and 5 SMs per arm were tested) and although switching events were much lower than with the conventional sorting and rotating algorithm, a considerable increase in the capacitor voltage ripple was observed.

Since the sorting and rotating algorithm is a simple implement, and it does not require any specific modulation method it is used for the remainder of this thesis.

[2]Under certain operating conditions the output voltage may vary more than one voltage step, which will force this algorithm to insert/bypass more than one SM at a time

2.5 MMC Control Methods

Since MMCs use fully controlled semiconductors such as IGBTs, there are three levels of controlability over the output voltage (or current): amplitude, phase, and frequency[3]. This allows the converter to achieve full control over active and reactive power separately; thus the MMC is considered a fully controlled converter [35].

The connection to the AC grid can be made by controlling the Point of Common Coupling (PCC) as either a PV or PQ bus, where either the active power and AC voltage or active and reactive power are controlled, respectively. The MMC can also control the DC link voltage if need be. There are basically two methods to implement any of these control methods:

- Direct Control, and
- Decoupled Control.

2.5.1 Direct Control

The relationship between the AC and DC voltage of the converter is defined as:

$$V_{\mathrm{AC}} = m\frac{V_{\mathrm{DC}}}{2} \tag{2.4}$$

where m is the modulation index of the modulating signal and V_{AC} is the output voltage of the converter.

Expression (2.4) assumes that either the DC link voltage is kept constant (presumably by a different converter) or the AC voltage is kept constant; therefore the output power and voltage can be controlled. Also, note that both the AC and DC voltages are linearly related to each other.

If the converter were to be represented as a voltage source, Fig. 2.8 shows the equivalent one-phase diagram of a three-phase system where the converter is connected to an AC system

[3]Although frequency is usually set fixed by the AC system it connects to.

via an impedance.

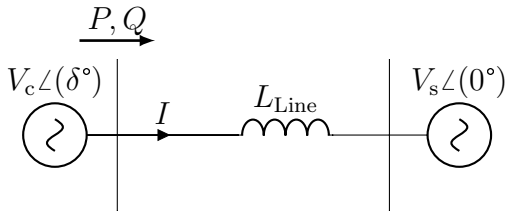


Figure 2.8: One phase equivalent circuit

V_c and I represent the converter's AC voltage and current, respectively, L_{Line} is the line inductance (assuming the line's resistance is negligibly small in comparison to the reactance) and V_s is the system's voltage. The phase angle of the system's voltage is zero as it is assumed that a PLL locks to it in order to provide a reference phase and maintain synchronism. The phase angle of the converter's voltage is defined as δ.

Based on the power expression:

$$S = P + jQ \tag{2.5}$$

The active and reactive power can be calculated as:

$$S = (V_s\angle(0°))I^* \tag{2.6}$$

$$S = \frac{V_s V_c \cos(\delta) - jV_s V_c \sin(\delta) - V_s^2}{-jX_L} \tag{2.7}$$

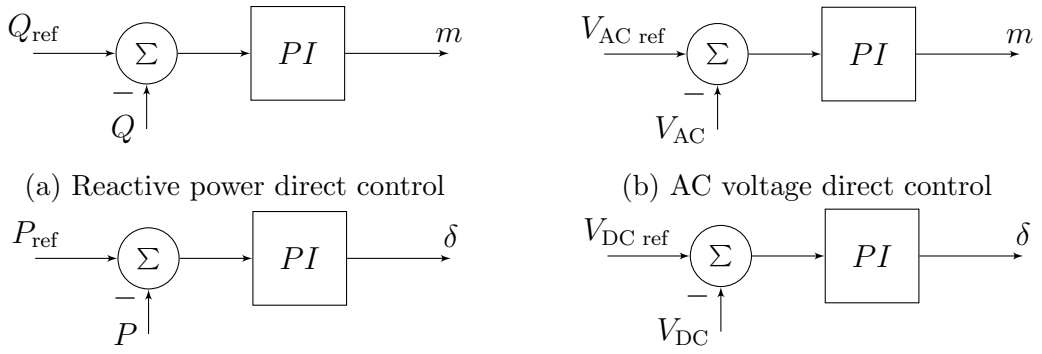
$$P = \frac{V_s V_c \sin(\delta)}{X_L} \tag{2.8}$$

$$Q = \frac{V_s V_c \cos(\delta) - V_s^2}{X_L} \tag{2.9}$$

The right-hand side of (2.8) is significantly affected by δ and as such it is used to control

P, whereas V_c is used to control Q in (2.9). The variation in either δ or V_c affects both P and Q; therefore, any change in δ must be accompanied by a change in V_c to compensate the resulting change in Q and vice versa.

This approach shows the simplest way to implement a controller for the active power and voltage/reactive power of an MMC. The following control loops are commonly used when implemented this type of control.



(a) Reactive power direct control

(b) AC voltage direct control

(c) Active power direct control

(d) DC voltage control

Figure 2.9: Direct control

The controllers in Fig 2.9 show how to control an MMC so that the PCC behaves like either a PV or PQ bus. It is also possible to control the DC bus voltage instead of controlling the output active power by controlling δ.

2.5.2 Decoupled Control

The following section presents the basics of decoupled control. Several variations to this method as well as its implementation have been reported.

Decoupled control is based on transforming the three-phase system from the original abc-domain into a different reference frame that rotates synchronously, as described in [36]. This approach uses Park's transformation for transforming abc quantities to the dq0 quantities

of the rotating frame:

$$\begin{bmatrix} X_{\mathrm{q}} \\ X_{\mathrm{d}} \\ X_0 \end{bmatrix} = T \begin{bmatrix} X_{\mathrm{a}} \\ X_{\mathrm{b}} \\ X_{\mathrm{c}} \end{bmatrix} \tag{2.10}$$

where:

$$T = \frac{3}{2} \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ \sin(\omega t) & \sin(\omega t - \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{2.11}$$

Expression (2.10) shows the direct transformation to obtain the dq0 components of the original abc system. The term ωt is the system's frequency multiplied by time, and in practice it is locked to the system's voltage by using a phase-locked-loop (PLL). The inverse transformation is as follows:

$$\begin{bmatrix} X_{\mathrm{a}} \\ X_{\mathrm{b}} \\ X_{\mathrm{c}} \end{bmatrix} = T^{-1} \begin{bmatrix} X_{\mathrm{q}} \\ X_{\mathrm{d}} \\ X_0 \end{bmatrix} \tag{2.12}$$

where:

$$T^{-1} = \begin{bmatrix} \cos(\omega t) & \sin(\omega t) & 1 \\ \cos(\omega t - \frac{2\pi}{3}) & \sin(\omega t - \frac{2\pi}{3}) & 1 \\ \cos(\omega t + \frac{2\pi}{3}) & \sin(\omega t + \frac{2\pi}{3}) & 1 \end{bmatrix} \tag{2.13}$$

Using this transformation, power can be calculated in both reference frames as:

$$P_{\mathrm{abc}} = \begin{bmatrix} V_{\mathrm{a}} \\ V_{\mathrm{b}} \\ V_{\mathrm{c}} \end{bmatrix}^T \begin{bmatrix} I_{\mathrm{a}} \\ I_{\mathrm{b}} \\ I_{\mathrm{c}} \end{bmatrix} = V_{\mathrm{a}} I_{\mathrm{a}} + V_{\mathrm{b}} I_{\mathrm{b}} + V_{\mathrm{c}} I_{\mathrm{c}} \tag{2.14}$$

$$P_{\mathrm{dq0}} = \begin{bmatrix} V_{\mathrm{q}} \\ V_{\mathrm{d}} \\ V_0 \end{bmatrix}^T \; [T^{-1}]^T T^{-1} \begin{bmatrix} I_{\mathrm{q}} \\ I_{\mathrm{d}} \\ I_0 \end{bmatrix} \tag{2.15}$$

Since $P_{\mathrm{abc}} = P_{\mathrm{dq0}}$, and:

$$[T^{-1}]^T T^{-1} = \begin{bmatrix} \frac{3}{2} & 0 & 0 \\ 0 & \frac{3}{2} & 0 \\ 0 & 0 & 3 \end{bmatrix} \tag{2.16}$$

Then:

$$P_{\mathrm{dq0}} = \begin{bmatrix} V_{\mathrm{q}} & V_{\mathrm{d}} & V_0 \end{bmatrix} \begin{bmatrix} \frac{3}{2} & 0 & 0 \\ 0 & \frac{3}{2} & 0 \\ 0 & 0 & 3 \end{bmatrix} \begin{bmatrix} I_{\mathrm{q}} \\ I_{\mathrm{d}} \\ I_0 \end{bmatrix} \tag{2.17}$$

Finally:

$$P_{\mathrm{dq0}} = \frac{3}{2}(V_{\mathrm{q}} I_{\mathrm{q}} + V_{\mathrm{d}} I_{\mathrm{d}} + 2V_0 I_0) \tag{2.18}$$

When the system under control is balanced, the 0-component obtained from expression (2.10) is zero, and the d and q components are constant values. Then expression (2.18) can be written as:

$$P_{\mathrm{dq0}} = \frac{3}{2}(V_{\mathrm{q}} I_{\mathrm{q}} + V_{\mathrm{d}} I_{\mathrm{d}}) \tag{2.19}$$

The work presented in [37] introduces the following definition for reactive power using the $\alpha\beta$ transformation:

$$Q_{\alpha\beta} = v_\alpha \times i_\beta + v_\beta \times i_\alpha \tag{2.20}$$

This is based on the idea that the instantaneous reactive current is the part of the three-phase current that could be varied without affecting the active power. Therefore, the reactive power can be obtained by multiplying the voltage and current components that are orthogonal to each other in the $\alpha\beta$ plane. Converting this definition into the abc system yields the following equation for reactive power:

$$Q_{\mathrm{abc}} = V_{\mathrm{a}}(I_{\mathrm{b}} - I_{\mathrm{c}}) + V_{\mathrm{b}}(I_{\mathrm{c}} - I_{\mathrm{a}}) + V_{\mathrm{c}}(I_{\mathrm{a}} - I_{\mathrm{b}}) \tag{2.21}$$

or similarly:

$$Q_{\mathrm{abc}} = V_{\mathrm{ab}}I_{\mathrm{c}} + V_{\mathrm{bc}}I_{\mathrm{a}} + V_{\mathrm{ca}}I_{\mathrm{b}} \tag{2.22}$$

Using expression (2.22) as well as the same procedure as previously shown, the dq-domain expression for reactive power is obtained as:

$$Q_{\mathrm{dq0}} = \frac{3}{2}(V_{\mathrm{d}}I_{\mathrm{q}} - V_{\mathrm{q}}I_{\mathrm{d}}) \tag{2.23}$$

Modifying the circuit shown in Fig. 2.8 to include the arm inductance of an MMC yields:

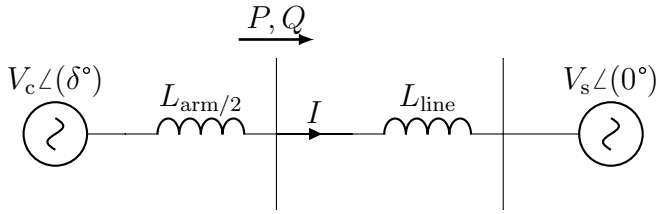


Figure 2.10: One phase equivalent circuit of an MMC.

Using KVL:

$$V_{\mathrm{c(abc)}} = V_{\mathrm{s(abc)}} + (\frac{L_{\mathrm{arm}}}{2} + L_{\mathrm{Line}})\frac{dI_{\mathrm{abc}}}{dt} \tag{2.24}$$

Transforming into the dq0 reference frame yields:

$$V_{\mathrm{c(dq0)}} = V_{\mathrm{s(dq0)}} + (\frac{L_{\mathrm{arm}}}{2} + L_{\mathrm{Line}})\frac{dI_{\mathrm{dq0}}}{dt} + (\frac{L_{\mathrm{arm}}}{2} + L_{\mathrm{Line}})\omega \begin{bmatrix} 0 & 1 & 0 \\ -1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} I_{\mathrm{(dq0)}} \tag{2.25}$$

For details on the transformation for the derivative of the current across a reactance see [38].

Using expressions (2.19), (2.23) and (2.25), it is possible to control the converter so that the PCC will behave like a PV or PQ node, or control the DC link voltage. Expression (2.25) allows decoupling the d and q components so that the active power control will not interfere with reactive power control, as was the case with the Direct Control. A control block showing a controller for a PV bus is shown in Fig 2.11.

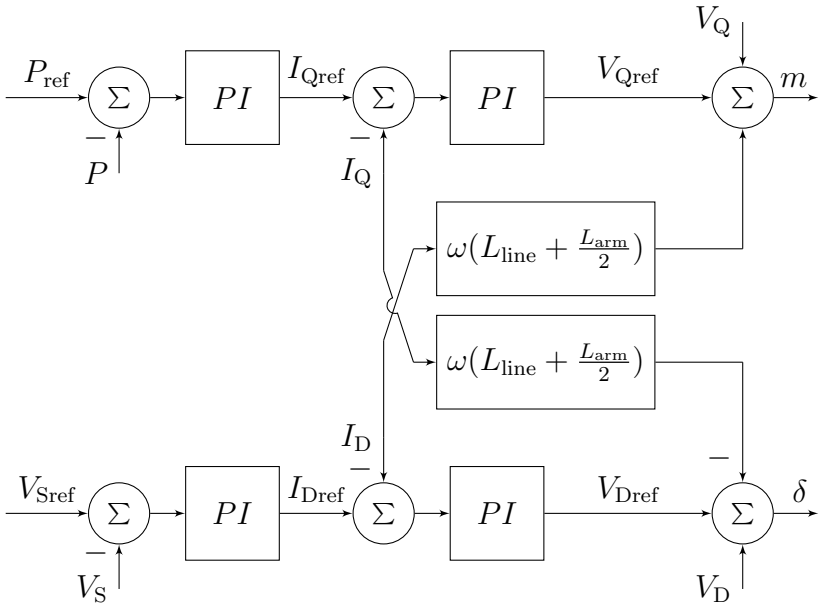


Figure 2.11: Decoupled PV controller for an MMC

2.5.3 Converter-Grid Synchronization

In the previous subsections a PLL was assumed to be in use to lock the converter to the grid's voltage. PLLs are used to obtain the phase angle of the voltage at the PCC, thus

synchronizing the converter with the grid.

One approach to do this [39], is based on the following trigonometric identity:

$$v_\mathrm{s} \sin(\omega_0 t - \delta) = v_\mathrm{s}(\sin(\omega_0 t)\cos(\delta) - \cos(\omega_0 t)\sin(\delta)) \tag{2.26}$$

By forming the expression on the right-hand side of (2.26) the PLL synchronizes to the grid frequency and an integrator derives the phase angle $\delta(t)$. This phase angle is matched to the one of the input V_S voltage by driving the difference between them to zero with a PI controller.

This provides proper synchronization which is required in order to successfully control the converter, avoid inrush currents, etc. Figure 2.12 shows a block diagram of the described PLL.

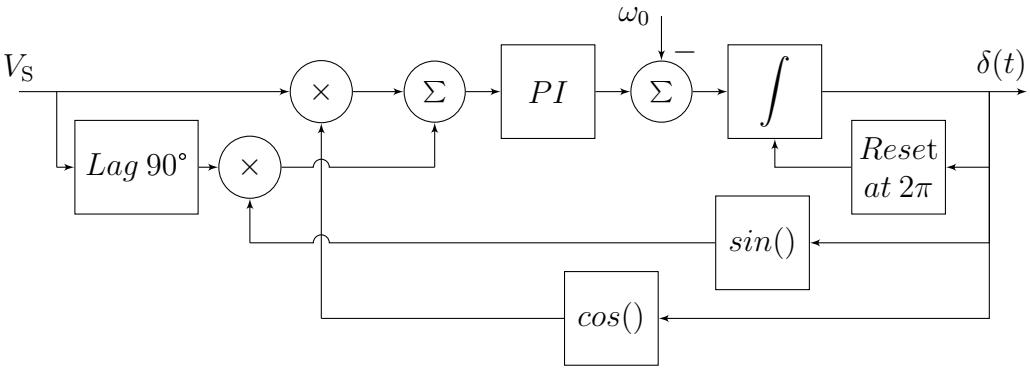


Figure 2.12: Exemplary Phase Locked Loop (PLL) block diagram

2.6 Summary

This chapter introduced the basic operating principles of the MMC. A general explanation of the operation of the converter was given. Some of the most common submodule topologies were presented and a detailed explanation about the operating modes of the half-bridge submodule was shown. Commonly used modulation techniques were also presented; special emphasis was given to PWM techniques and NLC as those are most often used in MMCs.

Several capacitor voltage balancing algorithms were presented in this chapter among which the sorting and rotating algorithm was selected for the work in this thesis. Finally, the two main strategies to control the output voltage and power of the converter were presented along with the operating principle of PLLs.

Chapter 3

Mathematical Model for Capacitor Voltage Ripple Manipulation

3.1 Natural Operation

The term "natural operation" refers to the operation of the converter when no circulating current control is implemented; therefore, circulating currents will arise due to the instantaneous voltage mismatch in the submodule capacitors.

The following mathematical model is based on the work presented in [40]. It only includes expressions for phase A, as the expressions for other phases can be readily obtained by phase-shifting the ones for phase A by 120°. The modulating signals for the upper and lower arms are described as:

$$\begin{aligned} m_{\text{upA}} &= \frac{1}{2}(1 - m\sin(\omega t)) \\ m_{\text{lowA}} &= \frac{1}{2}(1 + m\sin(\omega t)) \end{aligned} \tag{3.1}$$

where m is the modulation index and ω is the system's angular frequency. Equation (3.1), which is in p.u., is used to determine how many submodules to insert in the upper and lower arms over time to obtain the desired AC output voltage. The output voltage of phase A is

obtained as:

$$v_{\mathrm{A}} = m\frac{V_{\mathrm{DC}}}{2}\sin(\omega t) \tag{3.2}$$

Since each phase is connected in parallel to a DC source, under balanced conditions each phase will take one third of the total I_{DC}. Each arm's current will also have an AC component equal to half of the output AC current of that phase. Therefore, it is possible to initially describe the arm currents in steady state as:

$$\begin{aligned} i_{\mathrm{upA}} &= \frac{I_{\mathrm{DC}}}{3} + \frac{\sqrt{2}I_{\mathrm{A}}}{2}\sin(\omega t + \phi) \\ i_{\mathrm{lowA}} &= \frac{I_{\mathrm{DC}}}{3} - \frac{\sqrt{2}I_{\mathrm{A}}}{2}\sin(\omega t + \phi) \end{aligned} \tag{3.3}$$

where I_{DC} is the DC-link current, I_{A} is the RMS value of the phase-A current, and ϕ is the phase-angle difference between the voltage and current waveforms. The output current of phase A can be calculated as:

$$i_{\mathrm{A}}(t) = i_{\mathrm{upA}}(t) - i_{\mathrm{lowA}}(t) \tag{3.4}$$

or

$$i_{\mathrm{A}}(t) = \sqrt{2}I_{\mathrm{A}}\sin(\omega t + \phi) \tag{3.5}$$

The work presented in [40] allows to calculate the capacitor voltage ripple by considering the charge variations in the capacitors. The capacitor voltage is defined as:

$$\begin{aligned} v_{\mathrm{csmUp}}(t) &= \frac{V_{\mathrm{DC}}}{N} + \Delta v_{\mathrm{csmUp}}(t) \\ v_{\mathrm{csmLow}}(t) &= \frac{V_{\mathrm{DC}}}{N} + \Delta v_{\mathrm{csmLow}}(t) \end{aligned} \tag{3.6}$$

where the submodule capacitor voltage is described as a constant DC value plus a ripple

component; the latter can be calculated as:

$$\begin{aligned}\Delta v_{\text{csmUp}}(t) &= \frac{1}{C_{\text{sm}}}\int m_{\text{up}}(t) i_{\text{up}}(t) dt \\ \Delta v_{\text{csmLow}}(t) &= \frac{1}{C_{\text{sm}}}\int m_{\text{low}}(t) i_{\text{low}}(t) dt\end{aligned} \tag{3.7}$$

Substituting (3.1) and (3.3) into (3.7) yields:

$$\begin{aligned}\Delta v_{\text{csmUp}}(t) &= \frac{1}{\omega_0 C_{\text{sm}}}\left[\tfrac{I_{\text{DC}} m}{6}\cos(\omega_0 t) - \tfrac{\sqrt{2}}{4} I_{\text{A}}\cos(\omega_0 t+\phi) + \tfrac{\sqrt{2}}{16} I_{\text{A}} m \sin(2\omega_0 t+\phi)\right] \\ \Delta v_{\text{csmLow}}(t) &= \frac{1}{\omega_0 C_{\text{sm}}}\left[\tfrac{-I_{\text{DC}} m}{6}\cos(\omega_0 t) + \tfrac{\sqrt{2}}{4} I_{\text{A}}\cos(\omega_0 t+\phi) + \tfrac{\sqrt{2}}{16} I_{\text{A}} m \sin(2\omega_0 t+\phi)\right]\end{aligned} \tag{3.8}$$

It is seen that the upper and lower arm capacitor ripple expressions include a fundamental and a second-order harmonic ripple component. The fundamental-frequency ones are differential mode and the second-order ones are common-mode components. Although capacitor voltage balancing algorithms aim to regulate the capacitor voltages to the nominal value, at any given instant of time all the capacitor's voltages in a given arm will not be the same. Their voltage differences will cause higher order voltage components to arise and in turn higher order currents. The arm voltages are described as:

$$\begin{aligned}v_{\text{armUp}}(t) &= m_{\text{up}}(t) N v_{\text{csmUp}}(t) \\ v_{\text{armLow}}(t) &= m_{\text{low}}(t) N v_{\text{csmLow}}(t)\end{aligned} \tag{3.9}$$

Applying KVL to the DC loop yields:

$$V_{\text{DC}} = v_{\text{armUp}}(t) + v_{\text{armLow}}(t) + (i_{\text{up}}(t) + i_{\text{low}}(t)) R_{\text{arm}} + v_{\text{2L}}(t) \tag{3.10}$$

where R_{arm} is the arm resistance, and $v_{\text{2L}}(t)$ is the voltage across the arm inductosr. Substituting expression (3.8) into (3.6), then (3.6) into (3.9), and finally (3.9), (3.1) and (3.4) into

(3.10) and solving for $v_{2L}(t)$ yields:

$$v_{2L}(t) = \frac{N}{\omega_0 C_{sm}} \begin{bmatrix} \frac{\sqrt{2}}{8} I_A m \sin(\phi) + \frac{I_{DC} m^2}{12} \sin(2\omega_0 t) \\ -\frac{3\sqrt{2}}{16} I_A m \sin(2\omega_0 t + \phi) \end{bmatrix} - 2R_{arm} \frac{I_{DC}}{3} \tag{3.11}$$

This expression shows there is a second harmonic voltage in the arm inductors. Since there is no second order voltage canceling out the one naturally occurring in the inductors, second-order harmonic components are present in the arm current. This second-order component is defined as:

$$i_{2nd}(t) = I_{2nd} \cos(2\omega_0 t + \phi_2) \tag{3.12}$$

where I_{2nd} is the peak value of the second harmonic component in the arm current, and ϕ_2 is its phase angle with respect to the arm's voltage. Therefore, the natural arm currents in phase A can be expressed as:

$$\begin{aligned} i_{upA}(t) &= \frac{I_{DC}}{3} + \frac{\sqrt{2}}{2} I_A \sin(\omega_0 t + \phi) + I_{2nd} \cos(2\omega_0 t + \phi_2) \\ i_{lowA}(t) &= \frac{I_{DC}}{3} - \frac{\sqrt{2}}{2} I_A \sin(\omega_0 t + \phi) + I_{2nd} \cos(2\omega_0 t + \phi_2) \end{aligned} \tag{3.13}$$

The voltage across the two arm inductors can be described as:

$$v_{2L}(t) = L_{arm} \left(\frac{di_{up}(t)}{dt} + \frac{di_{low}(t)}{dt} \right) \tag{3.14}$$

Considering only the second-order harmonic, it can be expressed as:

$$v_{2L\text{-}2nd}(t) = -4\omega_0 L_{arm} I_{2nd} \sin(2\omega_0 t + \phi_2) \tag{3.15}$$

Following the same procedure as previously described to calculate ripple, but using (3.13)

instead of (3.3) yields:

$$\Delta v_{\mathrm{csmUp}}(t) = \frac{1}{\omega_0 C_{\mathrm{sm}}} \begin{bmatrix} \frac{I_{\mathrm{DC}} m}{6}\cos(\omega_0 t) - \frac{\sqrt{2}}{4} I_{\mathrm{A}} \cos(\omega_0 t + \phi) \\ + \frac{\sqrt{2}}{16} I_{\mathrm{A}} m \sin(2\omega_0 t + \phi) + \frac{I_{2\mathrm{nd}}}{4}\sin(2\omega_0 t + \phi_2) \\ + \frac{I_{2\mathrm{nd}} m}{4}\left(\frac{\cos(3\omega_0 t + \phi_2)}{3} - \cos(\omega_0 t + \phi_2)\right) \end{bmatrix}$$

$$\Delta v_{\mathrm{csmLow}}(t) = \frac{1}{\omega_0 C_{\mathrm{sm}}} \begin{bmatrix} \frac{-I_{\mathrm{DC}} m}{6}\cos(\omega_0 t) + \frac{\sqrt{2}}{4} I_{\mathrm{A}} \cos(\omega_0 t + \phi) \\ + \frac{\sqrt{2}}{16} I_{\mathrm{A}} m \sin(2\omega_0 t + \phi) + \frac{I_{2\mathrm{nd}}}{4}\sin(2\omega_0 t + \phi_2) \\ - \frac{I_{2\mathrm{nd}} m}{4}\left(\frac{\cos(3\omega_0 t + \phi_2)}{3} - \cos(\omega_0 t + \phi_2)\right) \end{bmatrix} \tag{3.16}$$

Expressions (3.16) show more harmonics components than in (3.8) including a third-order component. Similarly the even-numbered components in (3.16) and (3.8) are of the same polarity whereas the odd-numbered ones are of opposite polarities in the upper and lower arms.

Expressions (3.16) also show that the capacitor voltage ripple depends on both the converter and load parameters. They also show the underlying relationships between the capacitor voltage ripple and the second-order harmonic circulating currents. It is then possible to obtain the second-order circulating current required to achieve a certain capacitor voltage ripple.

Using (3.16) instead of (3.8) and following the previously described procedure to derive $v_{2\mathrm{L}}(t)$ yields:

$$\begin{aligned} v_{2\mathrm{L}}(t) = \frac{N}{\omega_0 C_{\mathrm{sm}}} & \begin{bmatrix} \frac{\sqrt{2}}{8} I_{\mathrm{A}} m \sin(\delta) + \frac{I_{2\mathrm{nd}} m^2}{8}\sin(\phi_2) \\ + \frac{I_{\mathrm{DC}} m^2}{12}\sin(2\omega_0 t) - I_{2\mathrm{nd}}\left(\frac{1}{4} + \frac{m^2}{6}\right)\sin(2\omega_0 t + \phi_2) \\ - \frac{3\sqrt{2}}{16} I_{\mathrm{A}} m \sin(2\omega_0 t + \delta) + \frac{I_{2\mathrm{nd}} m^2}{24}\sin(4\omega_0 t + \phi_2) \end{bmatrix} \\ & - 2R_{\mathrm{arm}}\left(\frac{I_{\mathrm{DC}}}{3} + I_{2\mathrm{nd}}\cos(2\omega_0 t + \phi_2)\right) \end{aligned} \tag{3.17}$$

This result shows that when a second-order harmonic is considered in the arm currents, a fourth-order ripple component shows up in the arm inductors' voltage. It will not be solved

for higher-order harmonic components in the arm currents since those are comparatively small in magnitude, and therefore, will be neglected for the remainder of this analysis. Also the arm resistance in an MMC is typically small and can be ignored without much effect on accuracy in high-voltage applications [40]. Therefore the voltage across the two arm inductors can be expressed as:

$$v_{2\mathrm{L}}(t) = \frac{N}{\omega_0 C_{\mathrm{sm}}} \begin{bmatrix} \frac{\sqrt{2}}{8} I_{\mathrm{A}} m \sin(\phi) + \frac{I_{2\mathrm{nd}} m^2}{8} \sin(\phi_2) \\ + \frac{I_{\mathrm{DC}} m^2}{12} \sin(2\omega_0 t) - I_{2\mathrm{nd}} \left(\frac{1}{4} + \frac{m^2}{6}\right) \sin(2\omega_0 t + \phi_2) \\ - \frac{3\sqrt{2}}{16} I_{\mathrm{A}} m \sin(2\omega_0 t + \phi) + \frac{I_{2\mathrm{nd}} m^2}{24} \sin(4\omega_0 t + \phi_2) \end{bmatrix} \tag{3.18}$$

This analysis has been made on the basis that the modulation waveform is as shown in expression (3.1); therefore, no circulating current control strategy has been implemented. This allows to calculate the amplitude and phase angle of the circulating current that will flow through the converter's arms should no circulating current strategy be implemented. To do this, it is recommended to derive the output current as a function of the DC current by using the power balance equation:

$$P_{\mathrm{DC}} = 3P_{\mathrm{A}} \tag{3.19}$$

$$V_{\mathrm{DC}} I_{\mathrm{DC}} = \frac{3}{2\sqrt{2}} m V_{\mathrm{DC}} I_{\mathrm{A}} \cos(\phi) \tag{3.20}$$

$$I_{\mathrm{A}} = \frac{4 I_{\mathrm{DC}}}{3\sqrt{2} m \cos(\phi)} \tag{3.21}$$

Substituting expression (3.21) in (3.18) allows to describe the second harmonic voltage in the inductors as a function of the DC current. Then, setting expression (3.18) equal to (3.15) and solving for the $\sin(2\omega t)$ and $\cos(2\omega t)$ components, it is possible to compute $I_{2\mathrm{nd}}$ and ϕ_2. Taking these steps, the amplitude and phase angle of the natural circulating current of the

converter are calculated as:

$$I_{2\text{nd}} = \frac{\frac{I_{\text{DC}}}{2}\sqrt{\left(1-\frac{m^2}{3}\right)^2+\tan(\phi)^2}}{8\omega_0^2 L_{\text{arm}}\frac{C_{\text{sm}}}{N}-\frac{1}{2}-\frac{m^2}{3}} \tag{3.22}$$

$$\phi_2 = \tan^{-1}\left(\frac{\tan(\phi)}{1-\frac{m^2}{3}}\right) \tag{3.23}$$

These last two expressions show that the amplitude and phase angle of the natural circulating current depend on the operating point of the converter, as well as on converter parameters.

3.2 Circulating Currents Control

In Section 1.2 the most common approaches used to address circulating currents control in MMCs were described. This section will present a new approach that allows to arbitrarily adjust the capacitor voltage ripple in the converter.

3.2.1 Circulating Current Suppression Controller

The work presented in [40], which introduced the mathematical model used in the previous section, also derives an expression to analytically calculate the amplitude, V_{z}, and phase angle, ϕ_{Z}, of a second-order harmonic component to include in the arm modulating waveform. The addition of this component eliminates the circulating currents in the arms. Nevertheless, it is also specified in [40] that, in practice, this component should be obtained via a closed-loop controller. This is due to the fact that the derivation neglects higher order harmonics, which affect the accuracy of the result.

These closed-loop controllers are known as Circulating Current Suppression Controllers (CCSCs). They are based on measuring the upper and lower arm currents, and driving the second-order circulating current component to zero using a controller. The circulating

currents in each phase is calculated as the mean of the upper and lower arm currents. Using (3.13) for phase A:

$$i_{\text{circA}}(t) = \frac{i_{\text{upA}}(t) + i_{\text{lowA}}(t)}{2} \tag{3.24}$$

$$i_{\text{circA}}(t) = \frac{I_{\text{DC}}}{3} + I_{\text{2nd}} \cos(2\omega t + \phi_2) \tag{3.25}$$

Taking a KVL across the upper arm of phase A:

$$V_{\text{DC}} - \Big(v_{\text{armUp}}(t) + v_{\text{armLow}}(t)\Big) = R_{\text{arm}}\Big(i_{\text{upA}}(t) + i_{\text{lowA}}(t)\Big) + L_{\text{arm}}\Big(\frac{di_{\text{upA}}}{dt} + \frac{di_{\text{lowA}}}{dt}\Big) \tag{3.26}$$

or

$$\frac{V_{\text{DC}}}{2} - \frac{\Big(v_{\text{armUp}}(t) + v_{\text{armLow}}(t)\Big)}{2} = R_{\text{arm}} i_{\text{circA}} + L_{\text{arm}} \frac{di_{\text{circA}}}{dt} \tag{3.27}$$

This means that if there is any voltage mismatch between the upper and lower arm submodules voltages and the DC link voltage, it must be absorbed by the arm's resistance and inductance. Denoting this voltage mismatch, i.e., the left-hand side of (3.27), as v_{z}, and rewriting (3.27) in matrix form for the entire converter yields:

$$\begin{bmatrix} v_{\text{zA}} \\ v_{\text{zB}} \\ v_{\text{zC}} \end{bmatrix} = R_{\text{arm}} \begin{bmatrix} i_{\text{circA}} \\ i_{\text{circB}} \\ i_{\text{circC}} \end{bmatrix} + L_{\text{arm}} \begin{bmatrix} \frac{di_{\text{circA}}}{dt} \\ \frac{di_{\text{circB}}}{dt} \\ \frac{di_{\text{circC}}}{dt} \end{bmatrix} \tag{3.28}$$

Driving the second-order circulating current components to zero is possible by subtracting this mismatch voltage (v_{z}) from the modulating waveform, thus canceling the one naturally occurring in the arm. Using Park's transformation as in (2.10), and assuming a three-phase

balanced system, the previous expression is rewritten as:

$$\begin{bmatrix} v_{\mathrm{zQ}} \\ v_{\mathrm{zD}} \end{bmatrix} = R_{\mathrm{arm}} \begin{bmatrix} i_{\mathrm{circQ}} \\ i_{\mathrm{circD}} \end{bmatrix} + L_{\mathrm{arm}} \begin{bmatrix} \frac{di_{\mathrm{circQ}}}{dt} \\ \frac{di_{\mathrm{circD}}}{dt} \end{bmatrix} + L_{\mathrm{arm}} \begin{bmatrix} 0 & 2\omega_0 L_{\mathrm{arm}} \\ -2\omega_0 L_{\mathrm{arm}} & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{circQ}} \\ i_{\mathrm{circD}} \end{bmatrix} \tag{3.29}$$

As was previously stated, the resistance in the converter arm is negligible for high-voltage application; thus in practice the resistive term in (3.29) is often ignored.

One of the most common approaches to implement this controller is by using PI controllers [14, 41–43]. Fig 3.1 shows the PI controller implementation of a CCSC. It should be pointed out that the second-order circulating current is a negative sequence component, thus Park's transformation is changed to ACB instead of ABC sequence.

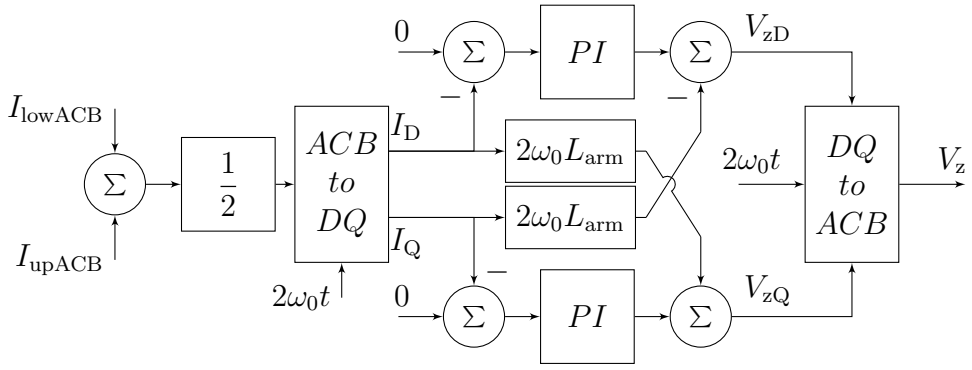


Figure 3.1: Circulating Current Suppression Controller (CCSC)

In order to implement this controller it is necessary to modify the modulating waveform to include a second-order harmonic component. The modulating waveform for phase A can be expressed as:

$$\begin{aligned} m_{\mathrm{upA}} &= \frac{1}{2}(1 - m\sin(\omega t) - V_{\mathrm{z}}\cos(2\omega t + \phi_2)) \\ m_{\mathrm{lowA}} &= \frac{1}{2}(1 + m\sin(\omega t)) - V_{\mathrm{z}}\cos(2\omega t + \phi_2) \end{aligned} \tag{3.30}$$

Similar implementations using different controllers can be found in literature. Proportional-Resonant (PR) controllers are used to control the circulating currents in [44,45]. The work in [10] compares performances of CCSCs implemented with PI, PR, and Proportional-Integral-

Resonant-based (PIR) controllers and proposes a feed-forward controller in order to overcome the limitations of the feedback-based controllers.

The work presented in [46] introduces a controller that considers both the second-order and fourth-order harmonic components in the arm currents and uses a PIR controller to eliminate them. Their results show a modest improvement in eliminating the second-order harmonic in the arm currents, and a 5% reduction in the fourth-order circulating currents. It should be noted that their analysis was validated on a 4-SM converter, which will cause the arm currents to have higher harmonic components than in converters with a large number of SMs.

3.2.2 Circulating Currents Control for Capacitor Voltage Ripple Manipulation

Equation (3.16) shows that given a certain amplitude and phase for the circulating currents, the capacitor voltage ripple under any operating conditions can be modified. Using this approach it is possible to obtain the capacitor voltage ripple profile of a converter. Table 3.1 shows the parameters of a converter used to analytically calculate said capacitor voltage ripple profile; note that the converter is serving an RL load with a power factor of 0.8 lagging. The capacitor voltage ripple profile of this converter at the operating point described in Table

Table 3.1: MMC Parameters

DC voltage (V_{DC}): 45 kV	Number of SMs/arm (N): 20
SM capacitance (C_{sm}): 8 mF	Nominal SM voltage (V_{csm}): 2.25 kV
Arm inductors (L_{arm}): 2.9 mH	Load: 19.37 mH, 9.747 Ω

3.1 and a modulation index of 0.95 is shown in Fig. 3.2. To obtain this profile, the amplitude of the circulating current was varied from 0 to the nominal DC current of 1 kA, whereas the phase angle was varied 360°. The natural operating point, where the circulating current is approximately $I_{2\mathrm{nd}} = 982\angle -47.1^{\circ}$ A, and the ripple is about 22.6%, is marked with a black

dot. The minimum-ripple operating point (OP), where the circulating currents are forced to be $I_{2\text{nd}} = 710\angle 140°$ A, yielding a ripple of 5.77%, is marked with a red dot. Also the CCSC operating point, which is the line where the circulating current is zero in magnitude, yields a ripple of 10.22%. Practical designs of MMCs aim for capacitor voltage ripple values of around 10%. This profile allows for a numerical optimization of the capacitor voltage

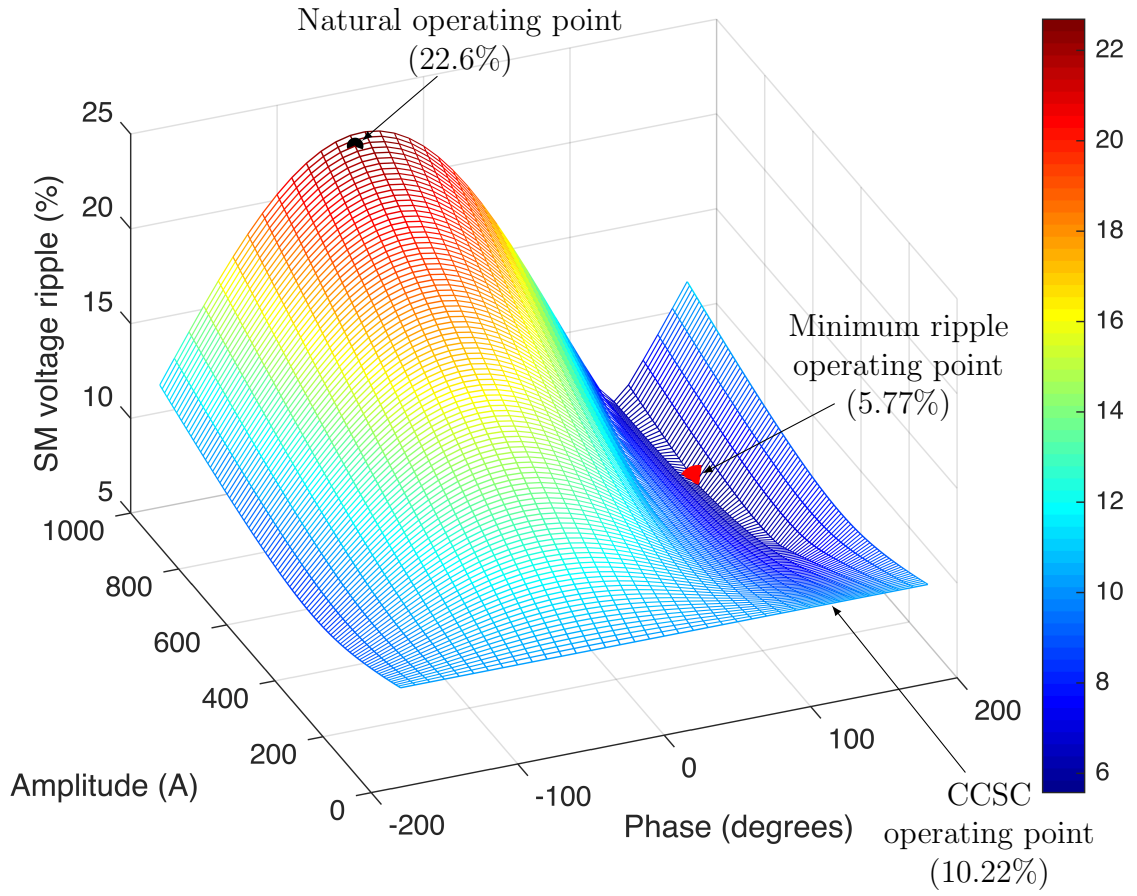


Figure 3.2: Capacitor voltage ripple profile.

ripple or determining the amplitude and phase of the circulating current required to achieve a certain ripple, which can be stored as a look-up table in order to operate the converter.

Using a controller as the one shown in Fig. 3.1, and modifying I_{Dref} and I_{Qref}, it is possible to control the circulating currents to the desired value and thus the capacitor voltage ripple. Using Park's transformation as shown in (2.10), the I_{Qref} and I_{Dref} for the controller shown

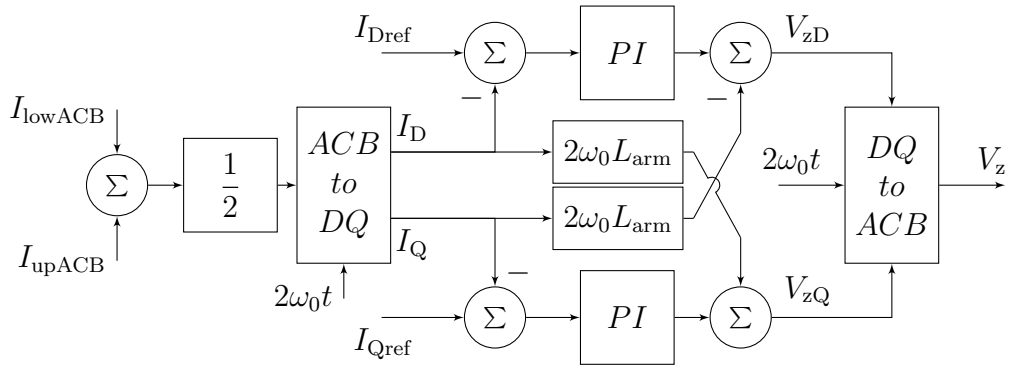


Figure 3.3: Second Harmonic Controller (SHC)

in Fig. 3.3 are calculated as follows:

$$\begin{aligned} I_{\text{Dref}} &= I_{\text{2nd}} \cos(\phi_2) \\ I_{\text{Dref}} &= -I_{\text{2nd}} \sin(\phi_2) \end{aligned} \tag{3.31}$$

where the values for I_{2nd} and ϕ_2 are obtained from the profile in Fig. 3.2.

3.3 Loss Assessment

When injecting circulating currents for capacitor voltage ripple manipulation purposes, there are two quantities of the converter that must be taken into consideration: semiconductor ratings and converter losses.

Since circulating current injection will distort the arm currents, its peak values need to be monitored. It is necessary to make sure that the semiconductors in the converter can tolerate this injection, and thus their operating region will not exceed the limits of its Safe Operating Area (SOA). This analysis can be done analytically by evaluating expression (3.13) over a period, and its outcome be used it to define the limits the semiconductors must not exceed.

Loss assessment is not as straight forward as calculating the peak current. The work presented in [18] reports that the conventional method of estimating the converter losses as a function of the switching frequency is not accurate as it does not consider the current flowing through the semiconductors nor the exact switching frequency, which may change

under certain operating conditions. Also the thermal behavior of the switches must be considered to accurately calculate losses. Therefore, in order to precisely calculate switching losses, the physics governing the semiconductors' behavior must be considered.

Switching events occur in a time frame of several hundred nanoseconds, which makes this approach unsuitable for Electromagnetic Transient-based (EMT) simulation of large systems. The work in [18] proposes using conventional EMT simulation models with ordinary time-steps in the micro-seconds range, while calculating the losses externally using an approximate model that considers only the pre- and post-switching operating voltages and currents. This approach also determines the junction temperatures and heat removal capabilities of the heat sinks. The obtained losses are then injected back into the EMT model in which the semiconductor of interest is embedded. This loss re-injection method eliminates any spurious losses resulting from the integration techniques.

In this thesis, an EMT-based switch model that implements this approach is used to evaluate how losses vary when injecting circulating currents. Fig. 3.4 shows the loss profile of the converter with the characteristics depicted in Table 3.2, while operating at the same OP for which the capacitor voltage ripple profile depicted in Fig. 3.2 was calculated.

It can be seen that at the natural operating point losses are 0.972 MW, which is marked with a black dot. It was found that at the minimum-loss operating point, where the circulating currents are forced to be $I_{2\text{nd}} = 450\angle 70^\circ$ A, losses are 0.599 MW; this OP is marked with a red dot. Also the CCSC operating point (OP), which is the line where the circulating current is zero in magnitude, yields 0.703 MW of losses.

3.4 Summary

This chapter presented the mathematical model used to describe the currents and capacitor voltage ripple in an MMC, which is a charge-based derivation method. The theory and implementation for the circulating current suppression controller was also presented. The

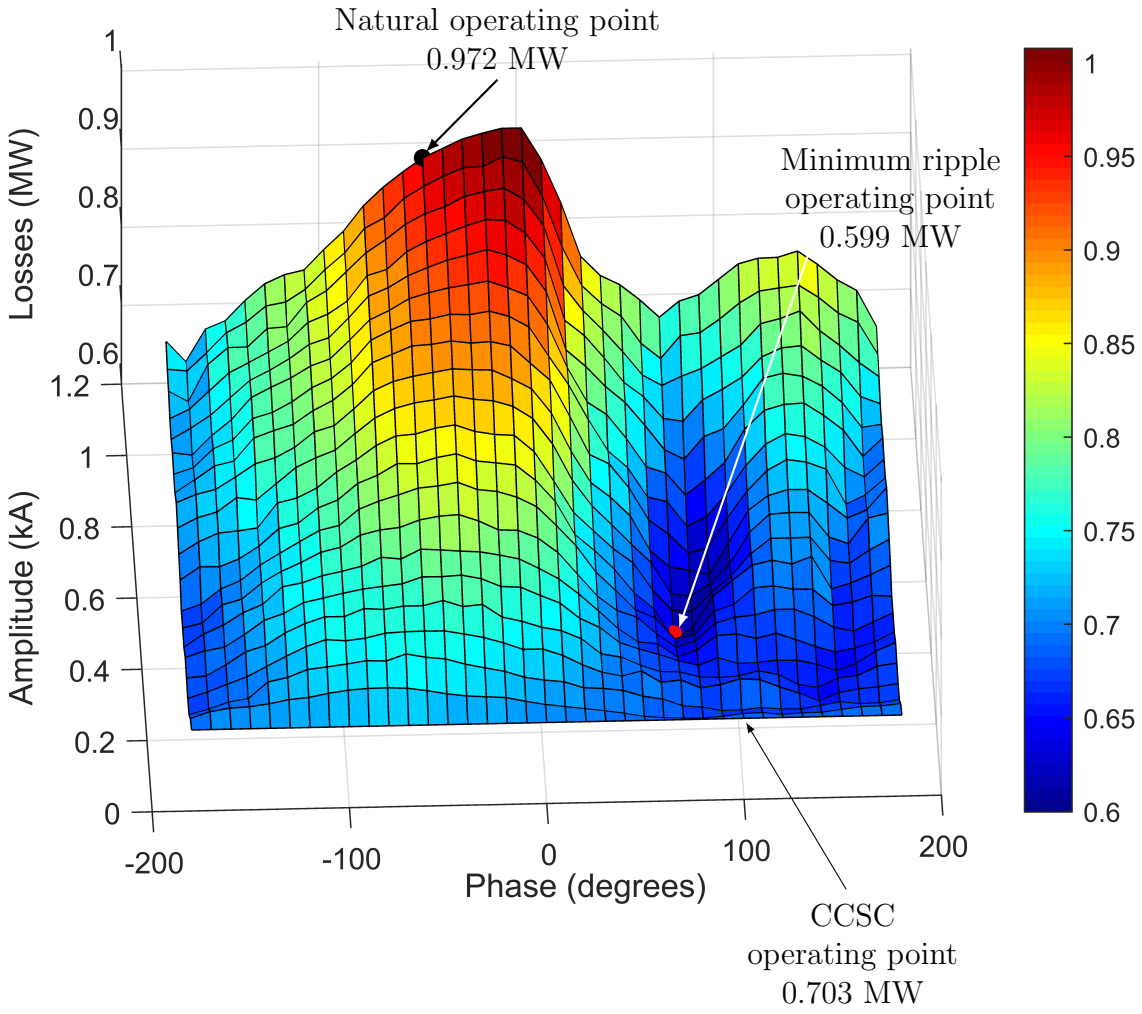


Figure 3.4: Converter loss profile.

capacitor voltage ripple profile of an MMC was calculated and, using it as a look-up table, the circulating current suppression controller was modified to achieve the current that would yield a required ripple. Finally, a method that enlarges the switch model in an EMT-based simulator, was presented to accurately calculate the switching and conduction losses of the semiconductors in a converter.

Chapter 4

Capacitor Voltage Ripple Model Validation and Loss Analysis

This chapter presents the validation for the proposed capacitor voltage ripple control method. Extensive simulation results are presented and the effect of reducing ripple and converter losses on the converter performance is analyzed. Finally implications on the semiconductor ratings will be evaluated.

4.1 Simulation-Based Validation

This section presents results to validate the developed method. EMT simulation results from PSCAD/EMTDC are used as benchmarks to assess the accuracy of the results from the model developed.

4.1.1 Model Accuracy

The accuracy of the analytically calculated capacitor voltage ripple profile is checked using detailed simulation in PSCAD/EMTDC. The converter whose parameters are listed in Table 3.1 is connected to nine separate loads (shown in Table 4.1) where the power factor varies

from 0.8 to 1 (lagging and leading) in steps of 0.05. The modulation index at which the converter is operated varies from 0.8 to 1 in steps of 0.05; therefore, a total of 45 combinations are analyzed. In each case, the amplitude of the injected circulating current is varied from 0 to 1 p.u. in steps of 0.05 p.u., where the base is selected as the corresponding DC link current. The phase of the injected circulating current is varied over the range of $\pm 180^{\circ}$ in steps of 10°. Therefore, for each case a ripple profile with 777 points of data collected from PSCAD/EMTDC simulations is compared to the analytically obtained profile. Similar profiles are also obtained for the converter losses, DC link current, and amplitude and phase angle difference for the circulating current. These other surfaces are studied in order to ensure the obtained results match the analytical model and check for errors. In all cases, the

Table 4.1: Load Parameters

Load 1: 19.37 mH, 9.75 Ω	Load 2: 18.08 mH, 11.00 Ω
Load 3: 15.85 mH, 12.34 Ω	Load 4: 11.98 mH, 13.75 Ω
Load 5: 362.8 µF, 9.747 Ω	Load 6: 388.9 µF, 11.00 Ω
Load 7: 443.9 µF, 12.34 Ω	Load 8: 587.1 µF, 13.75 Ω
Load 9: 15.23 Ω	

error in the capacitor voltage ripple calculation remains below $\pm 1\%$. The error is defined as the difference between the ripple obtained in the detailed model in PSCAD/EMTDC (in percentage of the nominal capacitor voltage) and the analytically calculated ripple. Figure 4.1 shows the error profile when connected to Load 1 with a modulation index of 0.95.

It is worth mentioning that error profile did not show the exact same shape for all the studied cases. It was found that for cases where the circulating current[1] was comparable in magnitude (at least 0.8 p.u.) to the fundamental component of the arm, serving a load with a power factor of 1, the error would increase considerably. The cause for this issue was found to be related to the tuning of the PI controllers of the second harmonic controller. This tuning problem caused large variations in the DC link current, which in turn translated

[1]From this point on, circulating currents is used to refer to the second-harmonic component of the circulating current, unless otherwise specified.

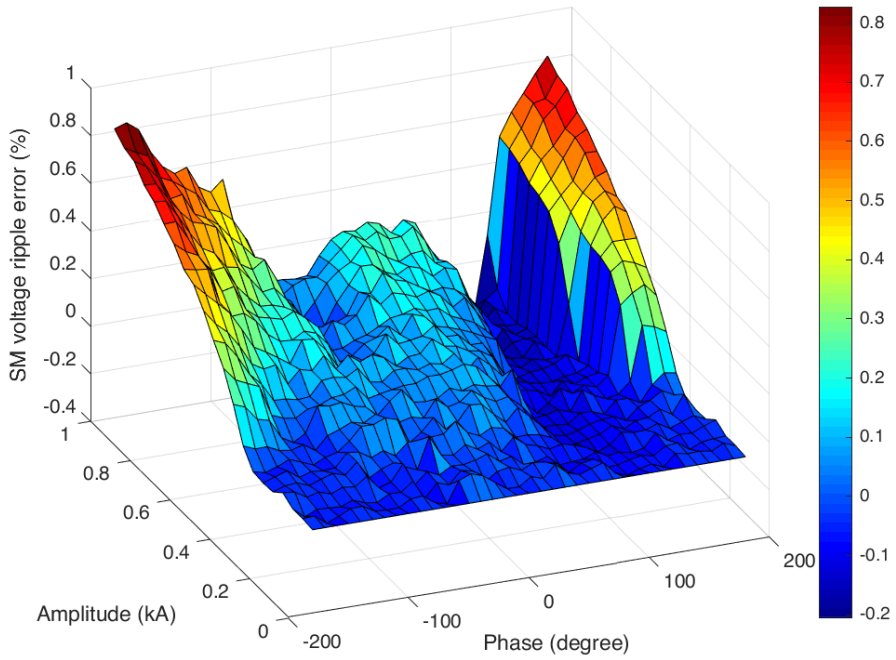


Figure 4.1: Capacitor voltage ripple profile error.

into the capacitor voltage ripple's abnormal variation. Once the controllers were tuned for these operating points, the error was kept below 1%.

Fig. 4.2 shows the situation previously described when serving a load with a unity power factor. In this case the modulation index was 0.85 and the injected current was $760\angle -130°A$. The improper tuning of the PI controllers caused the DC current to swing up to $\pm\,105\%$ its rated value (Fig. 4.2 top graph). This caused, among other problems, the arm currents and the capacitor voltage ripple presenting an improper behavior (middle and bottom graphs, respectively).

After re-tuning the PI controllers, the DC-bus current, arm currents and capacitor voltage ripple showed a stable behavior as shown in Figure 4.3. It can be seen that the ripple obtained from PSCAD/EMTDC in this case was 207 V, which represents a 9.2% ripple, whereas the analytical model ripple was 189 V or 8.4%, thus the error was 18 V or 0.8%.

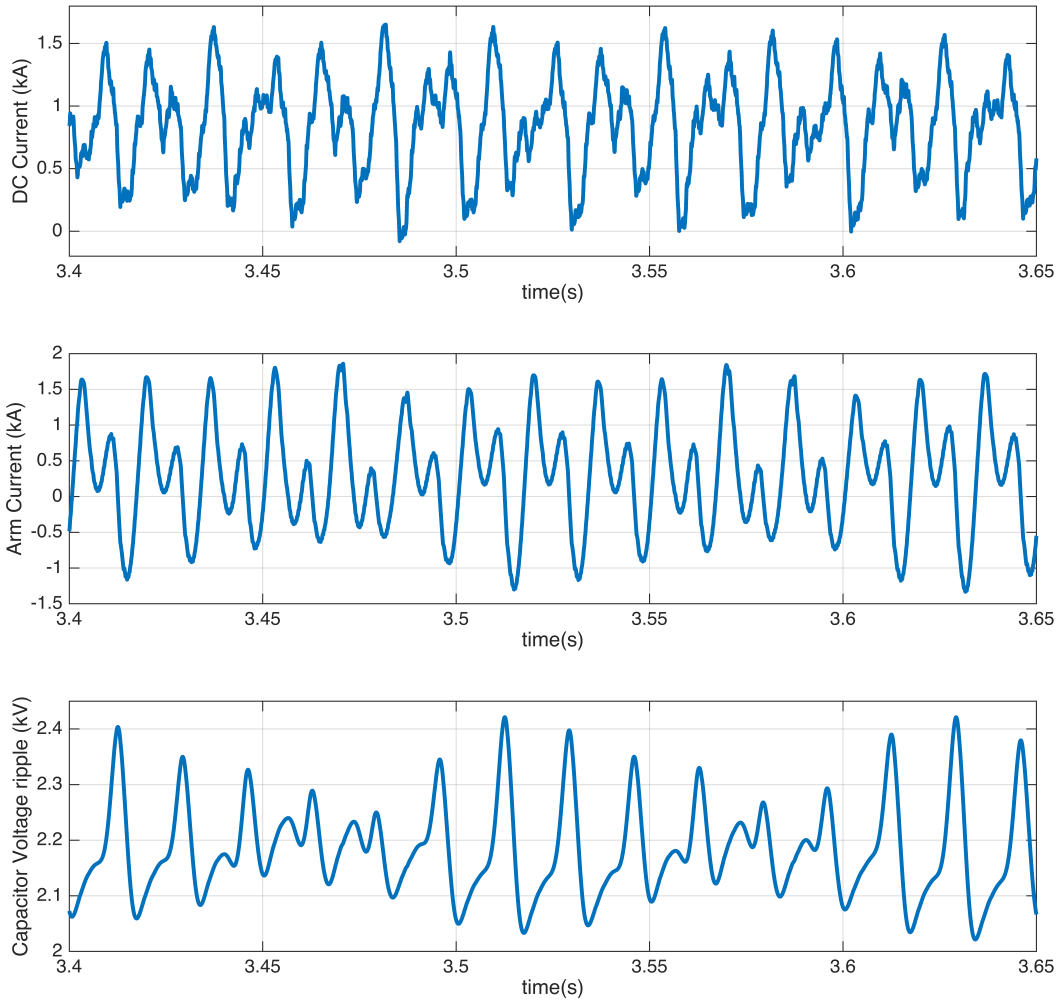


Figure 4.2: Capacitor Ripple error.

4.1.2 Capacitor Voltage Ripple Look-up Tables

Fig. 4.4 shows how the capacitor voltage ripple profile of the converter varies when the power factor of the load changes from 0.8 to 1 lagging (in steps of 0.1); Fig. 4.5 shows the same for leading power factors. In both figures, the "y" and "x" axes represent the respective amplitude and phase angle variations of the circulating current, whereas the "z" axis represents the ripple variation. In these graphs the modulation indexes are kept constant at 0.8, which limits the peak of the maximum injected circulating current to $I_{2\text{nd}} = 700$ A.

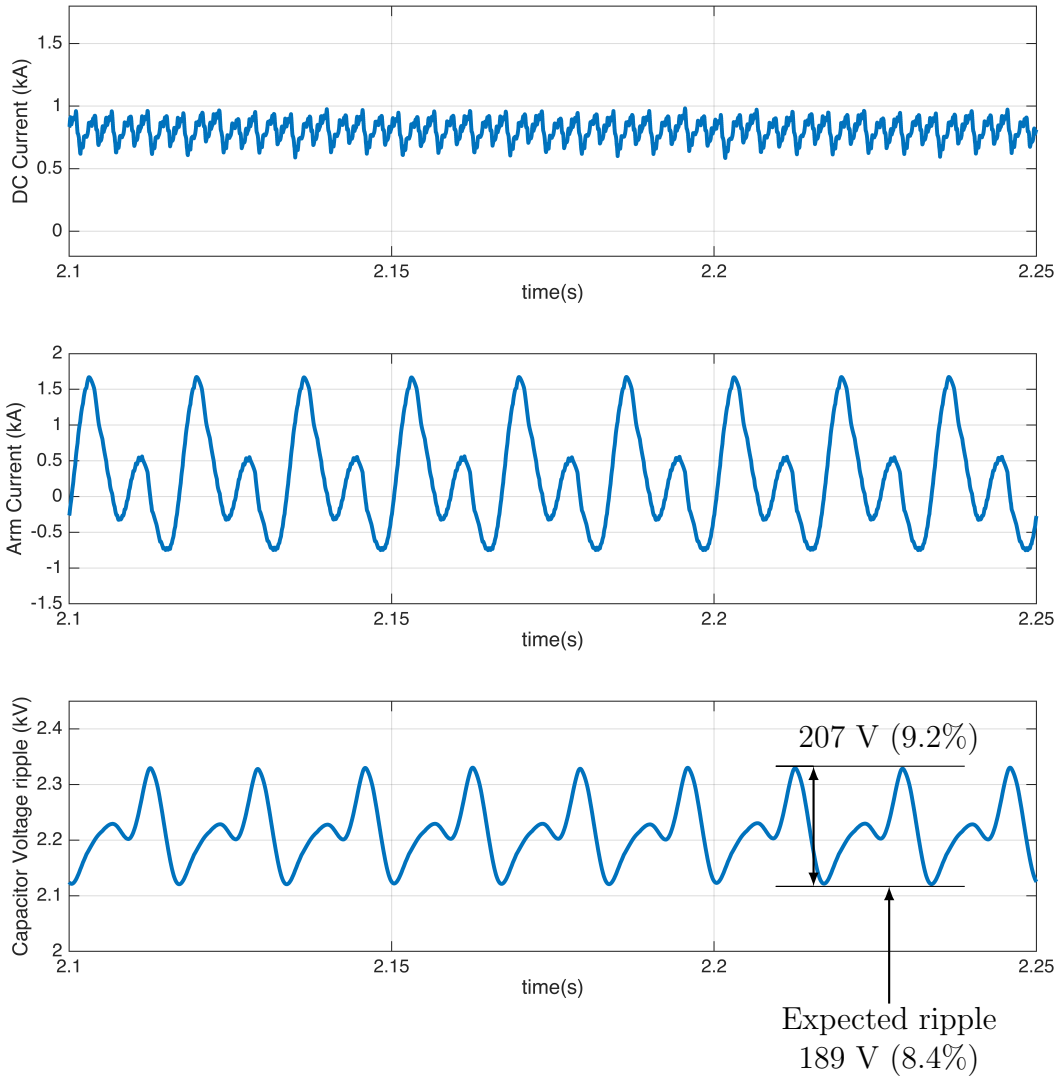
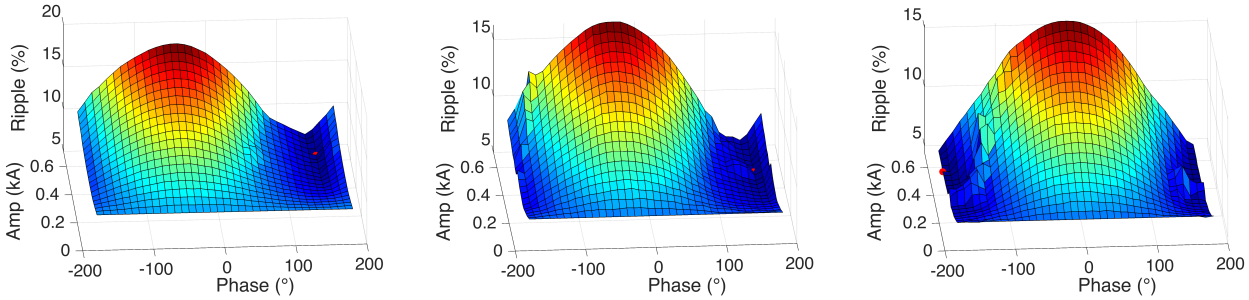


Figure 4.3: Capacitor Ripple error.

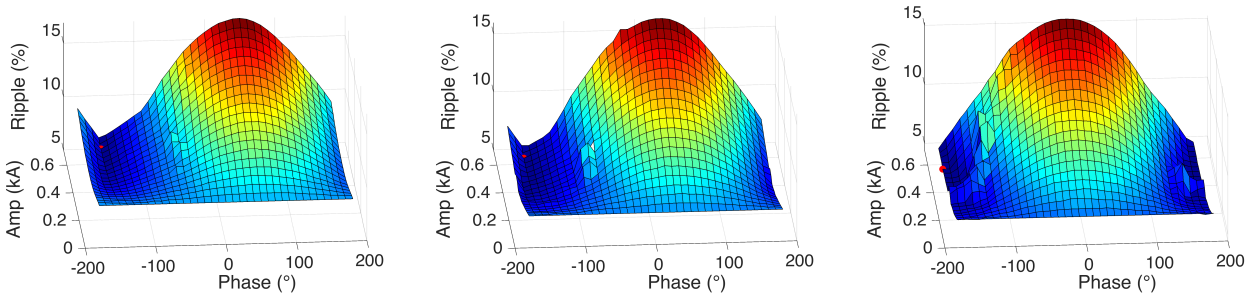
It can be seen that both the magnitude and phase angle of the circulating current that minimize ripple (red dot) move towards the right in the lagging case, and towards the left in the leading case, as the power factor increases. The same displacement is seen for the peak values of the ripple profile.

Similarly, the graphs shown in Figs. 4.6 and 4.7 show how changing the modulation index affects the capacitor voltage ripple profile of the converter. In this case, the power factor of the load is 0.8 lagging for Fig. 4.6 and 0.8 leading for Fig. 4.7. The modulation index of



(a) PF = 0.8 (b) PF = 0.9 (c) PF = 1.0

Figure 4.4: Capacitor voltage profile variation with respect to lagging power factor ($m = 0.8$).



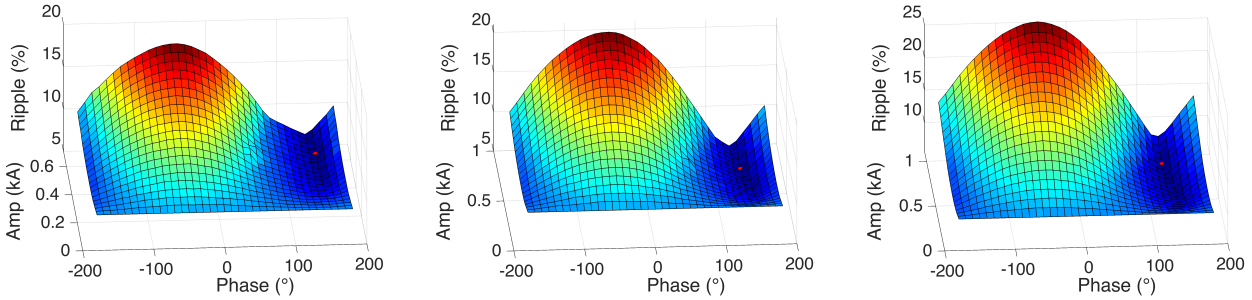
(a) PF = 0.8 (b) PF = 0.9 (c) PF = 1.0

Figure 4.5: Capacitor voltage profile variation with respect to leading power factor ($m = 0.8$).

the converter is varied from 0.8 to 1 in steps of 0.1. This causes the maximum peak of the injected circulating current to vary from $I_{2\text{nd}} = 700$ A when $m = 0.8$, to $I_{2\text{nd}} = 890$ A when $m = 0.95$ and $I_{2\text{nd}} = 1100$ A when $m = 1$. This variation in the modulation index causes the graphs to grow into its "y" and "z" axes; but no horizontal displacement in the "x" axis (phase angle) is seen.

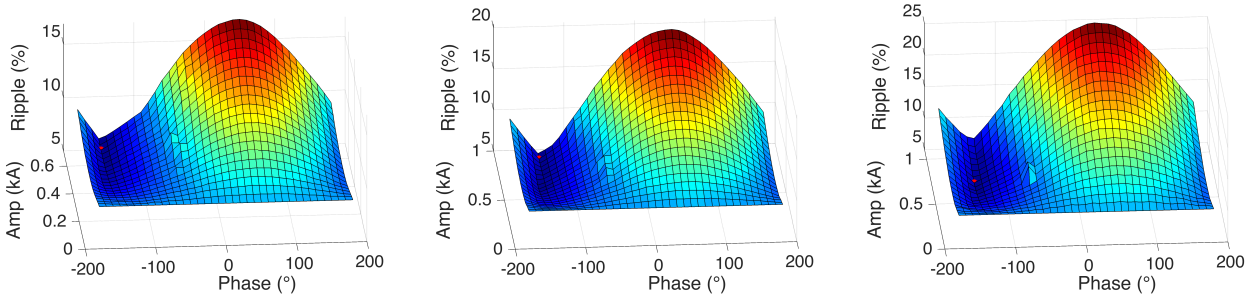
These results show that a change in the power factor of the load primarily translates into the ripple profile moving horizontally in its "x" axis, although this movement does not occur in a linear fashion. The change in the modulation index translates in an increase in the "y" and "z" axes. The same behavior occurs for loads with a lagging or leading power factors.

Figs. 4.8a and 4.8b show the amplitude (in per-unit with the amplitude of the fundamental component of the arm current as the base) that would minimize the capacitor voltage



(a) $m = 0.8$ (b) $m = 0.9$ (c) $m = 1.0$

Figure 4.6: Capacitor voltage profile variation with respect to the modulation index (PF = 0.8 lagging).



(a) $m = 0.8$ (b) $m = 0.9$ (c) $m = 1.0$

Figure 4.7: Capacitor voltage profile variation with respect to the modulation index (PF = 0.8 leading).

ripple for the lagging and leading power factor cases respectively. On the other hand Figs. 4.8c and 4.8d show the phase angle of the circulating current that minimizes the capacitor voltage ripple for lagging and leading power factors and modulation index values. This information may be stored in a look-up table to feed the second harmonic controller in Fig. 3.3.

Notice that the amplitude of the circulating currents for the lagging and leading power factors that minimize ripple (Figs. 4.8a and 4.8b respectively) are very similar to one other. Also, the phase angle of the circulating current that minimizes ripple for the lagging and leading power factors (Figs. 4.8c and 4.8d respectively) are 180° apart. This suggests that the ripple profiles of the MMC for loads with lagging or leading power factors are mirrored around 180°.

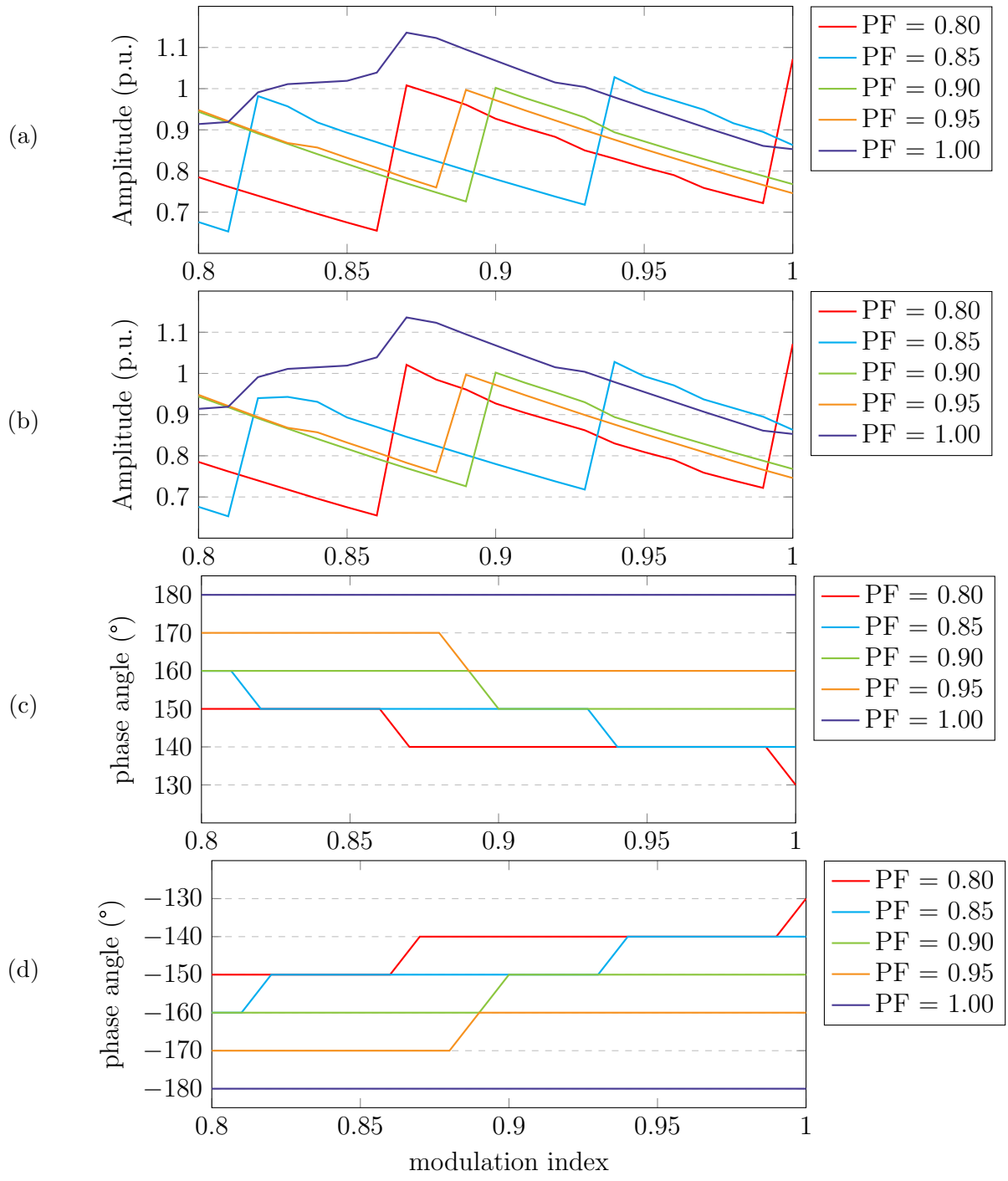


Figure 4.8: Circulating current to achieve minimum ripple, (a) and (b) show amplitudes for lagging and leading PF loads respectively, (c) and (d) show phase angle for lagging and leading PF loads respectively.

The amplitude of the current that minimizes the capacitor voltage ripple follows a highly non-linear behavior, and its amplitude is quite high as compared to the fundamental fre-

quency component in the arm current. This further emphasizes the importance of assessing how the capacitor voltage minimization will affect the semiconductor ratings.

Ripple Comparison: Min Ripple vs. CCSC

In order to evaluate how much the ripple can be minimized, the graph shown in Fig. 4.9 shows how the variation in the modulation index and power factor of the load affects the ripple minimization as compared to the operating point where circulating currents are completely suppressed. On the "y" axis, ripple reduction refers to the relative reduction at the minimum ripple operating point with respect to the operating point where circulating currents are completely suppressed. This graph allows seeing how much further the ripple can be reduced beyond the operating point where circulating currents are completely suppressed for a given modulation index or power factor (either lagging or leading). It can be seen that when the converter is operated with a low modulation index (e.g., 0.8), the ripple could be reduced up to about 35% for any power factor. Whereas the higher the modulation index the higher the ripple reduction; where a maximum ripple reduction of almost 60% is achieved when both the power factor and modulation index are equal to unity.

4.1.3 Look-up Tables for Loss Variations

Fig. 4.10 shows how the loss profile of the converter varies when the power factor of the load changes from 0.8 to 1 lagging (in steps of 0.1) whereas Fig. 4.11 shows the same for a leading power factor. In both figures, the modulation indexes in the graphs are kept constant at 0.8, which limits the peak of the maximum injected circulating current to $I_{2\text{nd}} = 700$ A (as in Section 4.1.2). The minimum loss operating point does not follow a predictable trend with the power factor. Although a change in the power factor of the load primarily translates into the loss profile moving horizontally in its "x" axis, this movement does not follow a predictable behavior as with the capacitor voltage ripple.

Similarly, the graphs shown in Fig. 4.12 show how changing the modulation index affects

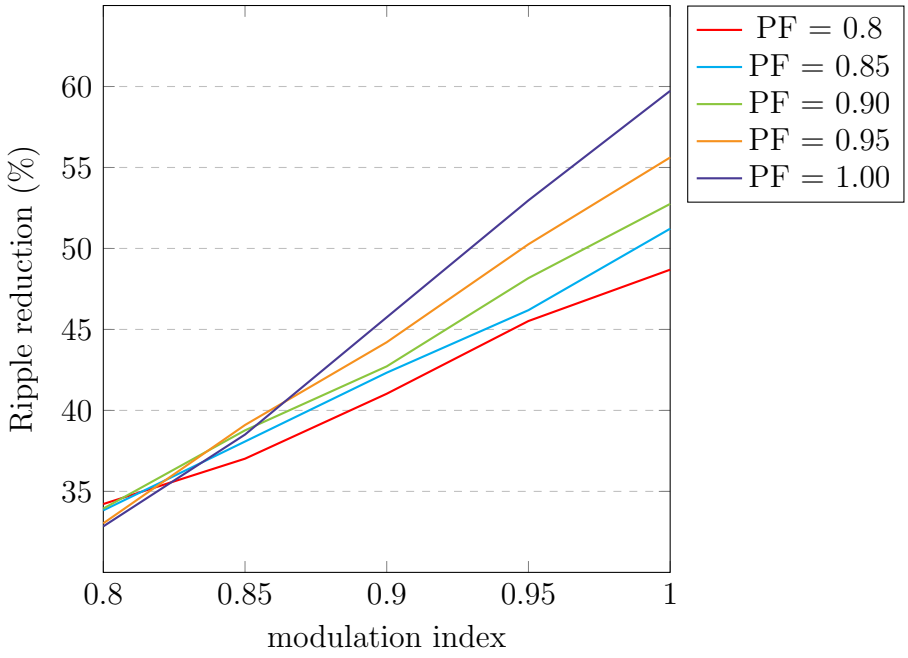
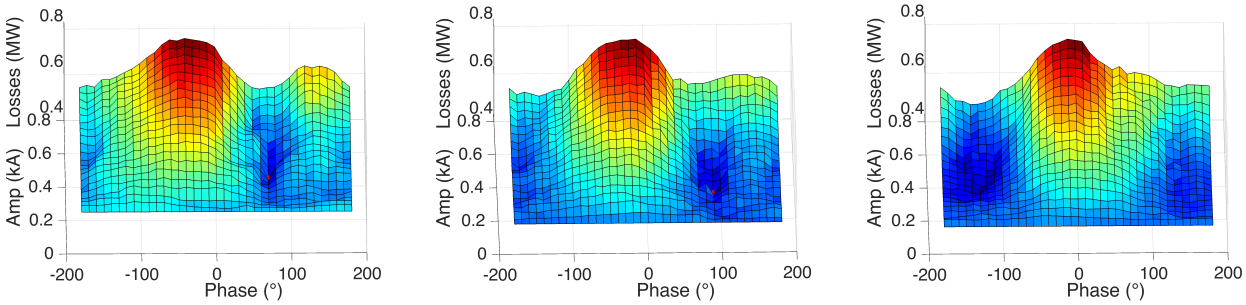


Figure 4.9: Ripple minimization dependence on modulation index for lagging and leading power factor loads

the loss profile of the converter for lagging power factor loads, whereas the ones in Fig. 4.13 show the results for leading power factor loads. In the same way as in Section 4.1.2, the power factor of the load was kept constant at 0.8, whereas the modulation index of the converter was varied from 0.8 to 1 in steps of 0.1. This caused the maximum peak of the injected circulating current to vary from $I_{2\text{nd}} = 700$ A when $m = 0.8$, to $I_{2\text{nd}} = 890$ A when $m = 0.95$ and $I_{2\text{nd}} = 1100$ A when $m = 1$. This variation in the modulation index causes the graph to grow into its "y" and "z" axes.

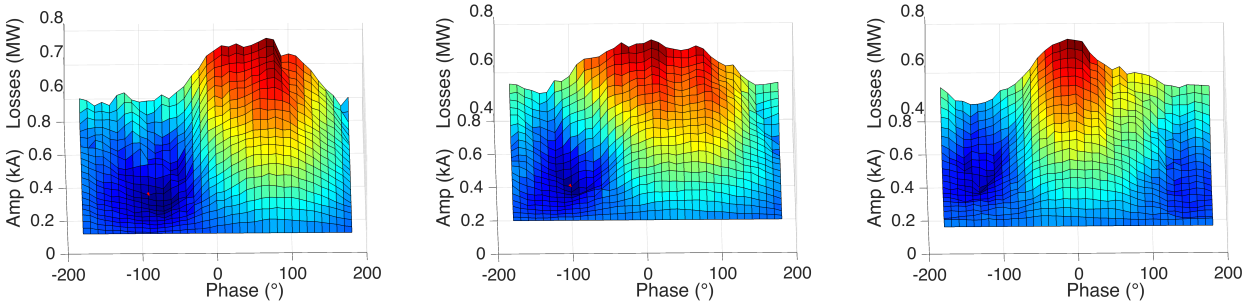
It can also be seen from these graphs that the circulating current that yields the minimum loss operating point (red dot) for the lagging case does not change significantly in terms of phase angle: $I_{2\text{nd}} = 355\angle 70°$ A, $I_{2\text{nd}} = 449\angle 80°$ A, $I_{2\text{nd}} = 443\angle 70°$ A for $m = 0.8$, 0.9 and 1 respectively in Fig. 4.12. Neither does it for the leading power factor case (Fig. 4.13) where the minimums are located at: $I_{2\text{nd}} = 355\angle -90°$ A, $I_{2\text{nd}} = 449\angle -90°$ A, $I_{2\text{nd}} = 443\angle -90°$ A for $m = 0.8$, 0.9 and 1, respectively.

In order to better represent these variations, Figs. 4.14a and 4.14b show the amplitude (in



(a) PF = 0.8 (b) PF = 0.9 (c) PF = 1.0

Figure 4.10: Loss profile variation with respect to lagging power factor ($m = 0.8$).

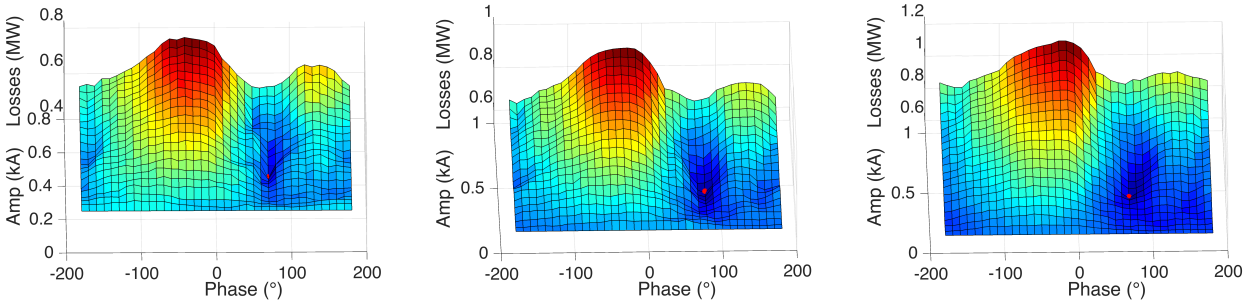


(a) PF = 0.8 (b) PF = 0.9 (c) PF = 1.0

Figure 4.11: Loss profile variation with respect to leading power factor ($m = 0.8$).

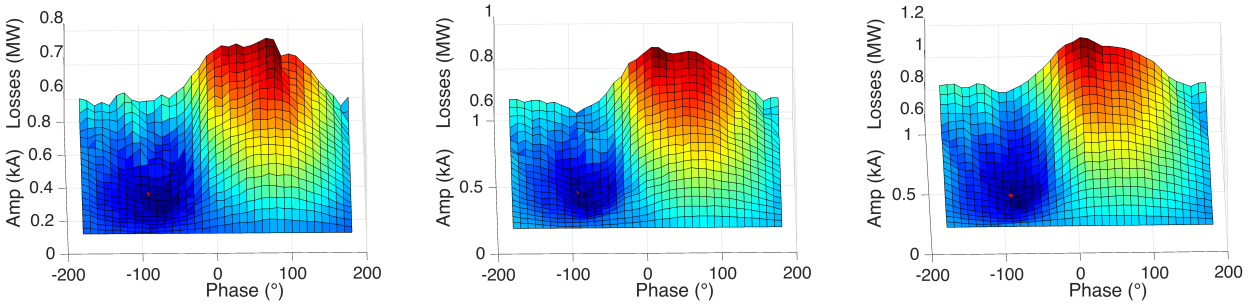
per-unit with the amplitude of the fundamental component of the arm current as the base) of the circulating current that minimizes losses for the lagging and leading power factor cases, respectively. Similarly, Figs. 4.14c and 4.14d show the phase angle of the circulating current that minimizes the losses for the lagging and leading power factor cases. This information may be stored in a look-up table to feed the second harmonic controller in Fig. 3.3.

It can be seen in Fig.4.14a that for most cases, the peak current that minimizes losses for a lagging power factor load is comparatively smaller than the one that minimizes losses for the leading power factor loads in Fig. 4.14b. This suggests that a higher circulating current is required in order to minimize losses when working with a leading power factor load. Nevertheless, it should be noticed that, overall, the peak amplitude of the circulating current that minimizes the losses is comparatively smaller than the ones that minimize ripple. The results obtained in this work show that in the loss minimization case the maximum



(a) $m = 0.8$ (b) $m = 0.9$ (c) $m = 1.0$

Figure 4.12: Loss profile variation with respect to the modulation index (PF = 0.8 lagging).



(a) $m = 0.8$ (b) $m = 0.9$ (c) $m = 1.0$

Figure 4.13: Loss profile variation with respect to the modulation index (PF = 0.8 leading).

amplitude barely exceeds 0.55 p.u. whereas in the ripple minimization case it is up to 1.136 p.u. of the arm current. This difference in the injected circulating current amplitude might prove unfeasible minimizing ripple in MMCs due to semiconductor stress.

Analyzing the phase angles that minimize losses, it can be observed that the total variation in the lagging power factor cases (Fig. 4.14c) is up to 40° when the modulation index varies between 0.8 to 0.95. Nevertheless, for the unity power factor case, the phase angle that minimizes losses is between 100° to 170° away from the other OPs for the same type of load. With the leading power factor cases (Fig. 4.14d), the total variation in the phase angles is up to 50° when the modulation index is between 0.8 to 0.95; and these values are between 10° and 80° away from the unity power factor case. This results suggests that contrary to what was seen in with the ripple minimization analysis, the minimum phase angles are not "mirrored" around any specific phase angle.

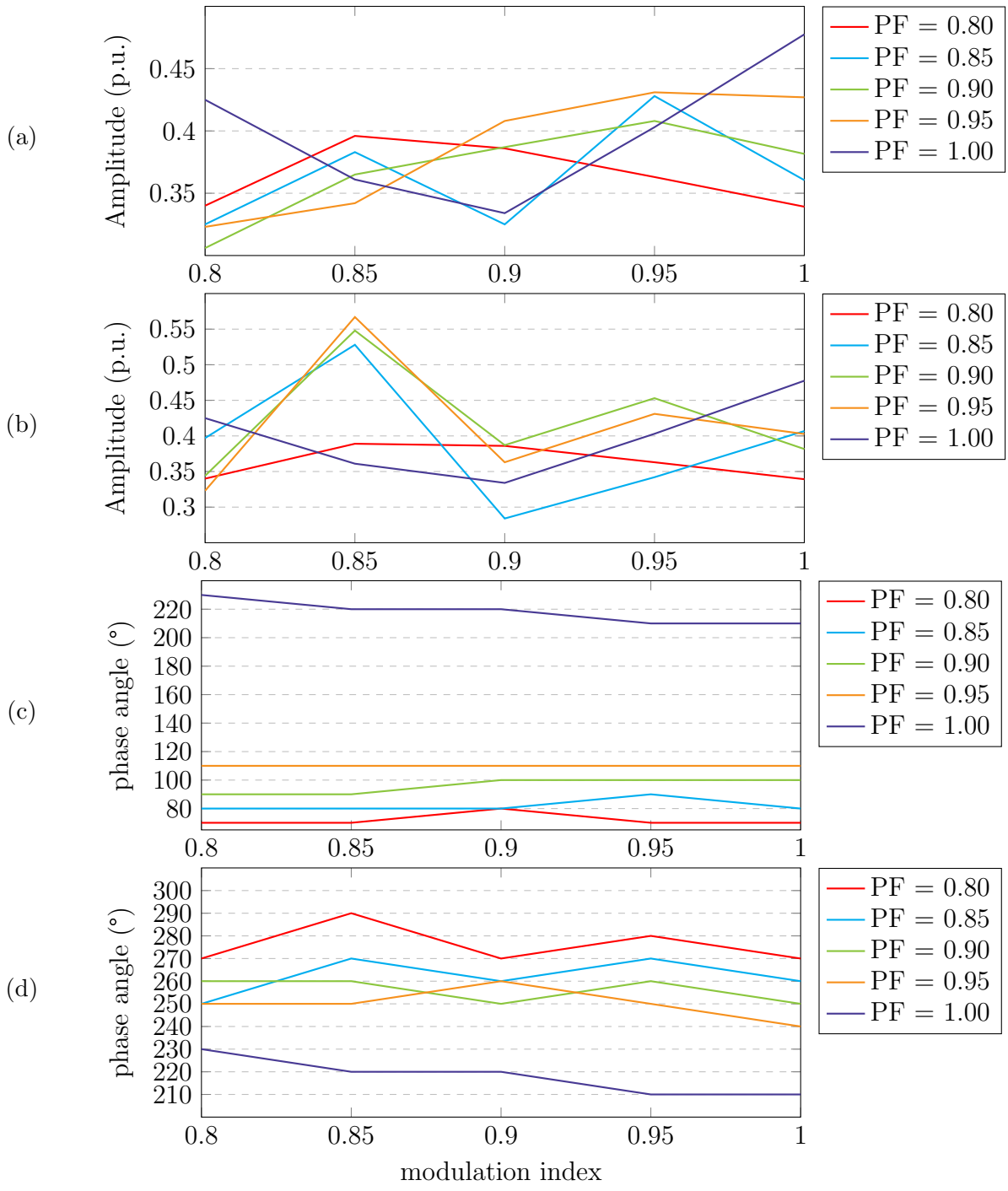
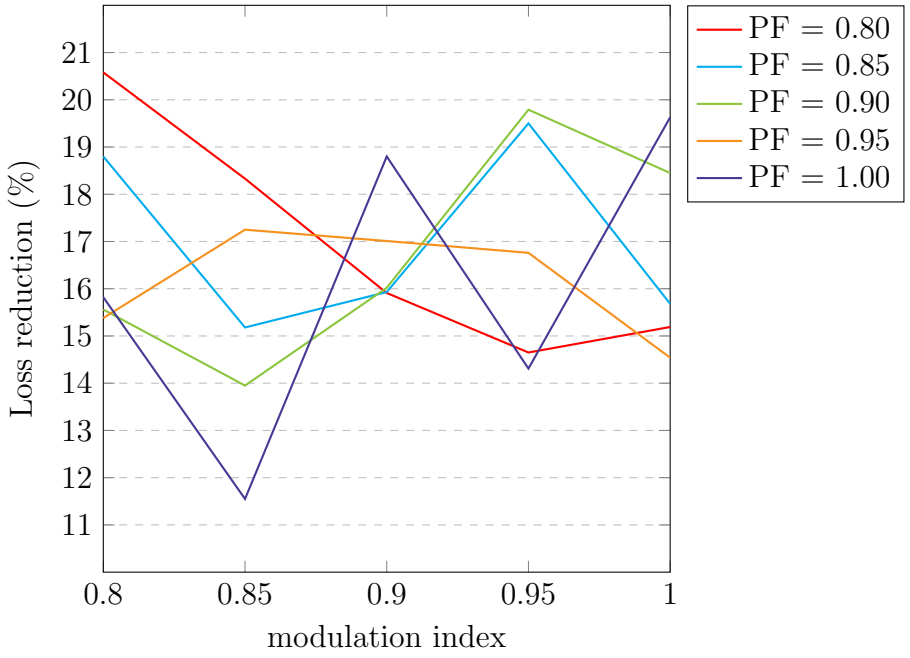


Figure 4.14: Circulating current to achieve minimum losses: (a) and (b) show amplitudes for lagging and leading PF loads respectively, (c) and (d) show phase angle for lagging and leading PF loads respectively.

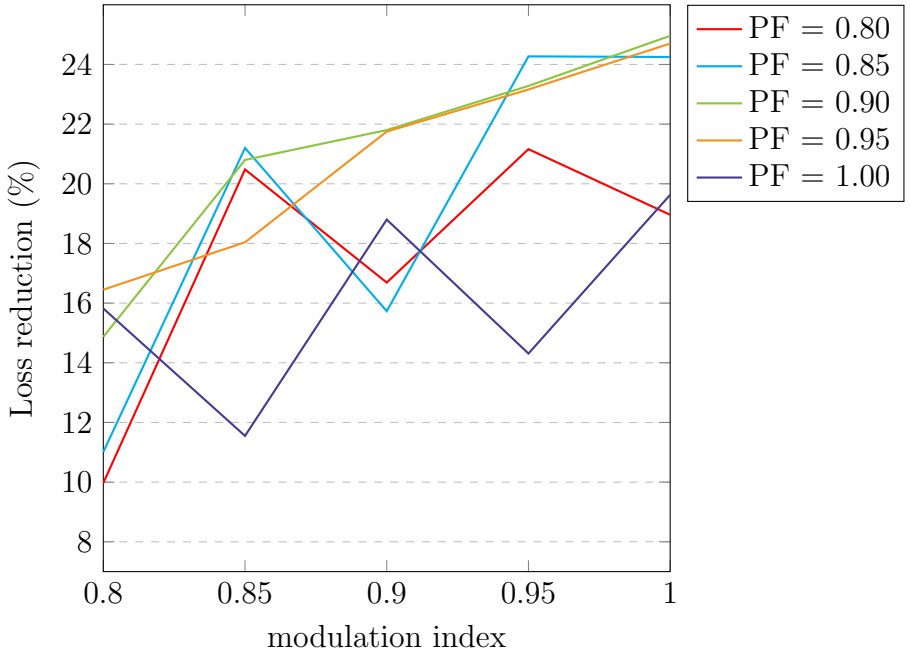
Loss Comparison: Min. Losses vs. CCSC

The graphs below show how much losses are reduced at the minimum loss operating point as compared to the losses at the CCSC operating point for the lagging power factor loads

(Fig. 4.15a) and leading power factors loads(Fig. 4.15b). On the "y" axis, loss reduction refers to the relative reduction in losses at the minimum loss operating point with respect to those at the CCSC operating point.



(a) Loss reduction at the minimum loss OP as compared to the CCSC OP (lagging pf)



(b) Loss reduction at the minimum loss OP as compared to the CCSC OP (leading pf)

Figure 4.15: Minimum loss reductions

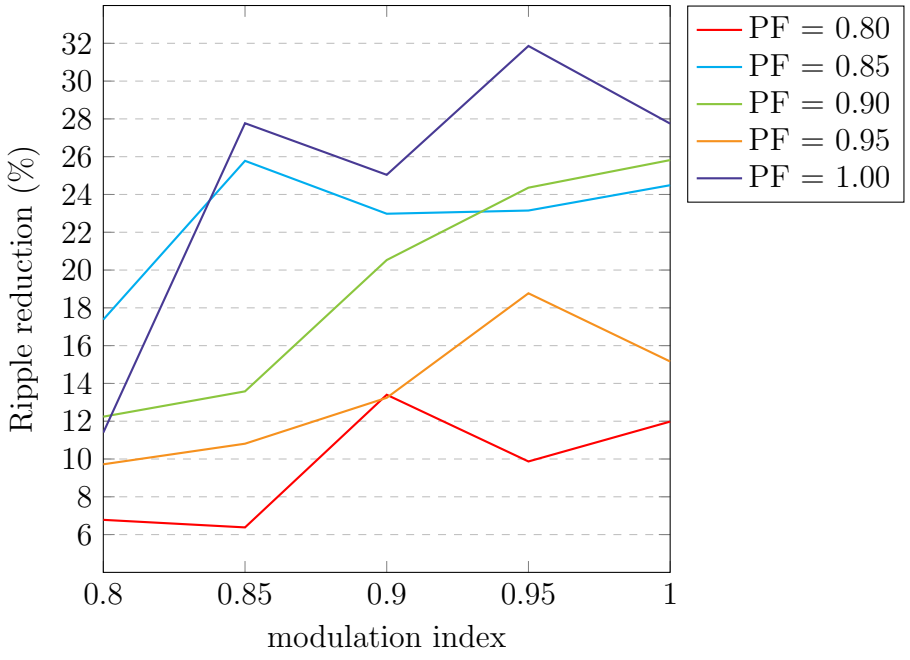
In the case of the lagging power factor (Fig. 4.15a), it can be seen that the behavior of the circulating currents that yield the minimum loss operating point does not follow a predictable trend. Nevertheless, losses can be reduced between 11.5% to almost 21% from its values at the operating point where circulating currents are completely suppressed. In the leading power factor case(Fig. 4.15a), a similar non-predictable behavior is observed. In this case losses can be reduced between 9.97% to almost 25.04% from its values at the operating point where circulating currents are completely suppressed.

These results suggest that the best approach to reduce losses in MMCs is not to completely suppress the circulating currents, but to inject some judicious amount that would minimize the conduction and switching losses. Also, a highly non-predictable behavior for any of the operating points analyzed is observed. Contrary to what was seen with capacitor voltage ripple, the behavior of the circulating current that yields minimum losses is not similar for either the lagging or leading power factor cases; thus the main drawback of this method is its reliance on simulations to obtain look-up tables.

Ripple Comparison: Min Loss Operation vs. CCSC

This section evaluates how operating the converter at the minimum loss operating point affects ripple. On the "y" axis of Fig. 4.16, ripple reduction refers to the relative reduction in ripple at the minimum loss OP with respect to the ripple at the operating point where circulating currents are completely suppressed. Fig. 4.16a shows the results for the lagging power factor loads whereas Fig. 4.16b shows it for the leading power factor loads .

It can be seen that when losses are minimized for loads with a lagging pf (Fig.4.16a), ripple is reduced between 6.38% to 31.86%; whereas for leading power factor loads (Fig. 4.16b) ripple is reduced between 7.14% to 31.86%. This means that minimizing losses also reduces ripple beyond its values at the operating point where circulating currents are completely suppressed. It should be pointed out that the ripple reduction observed at the min. loss operating point is less than half its absolute minimum, nevertheless an important ripple



(a) lagging pf.

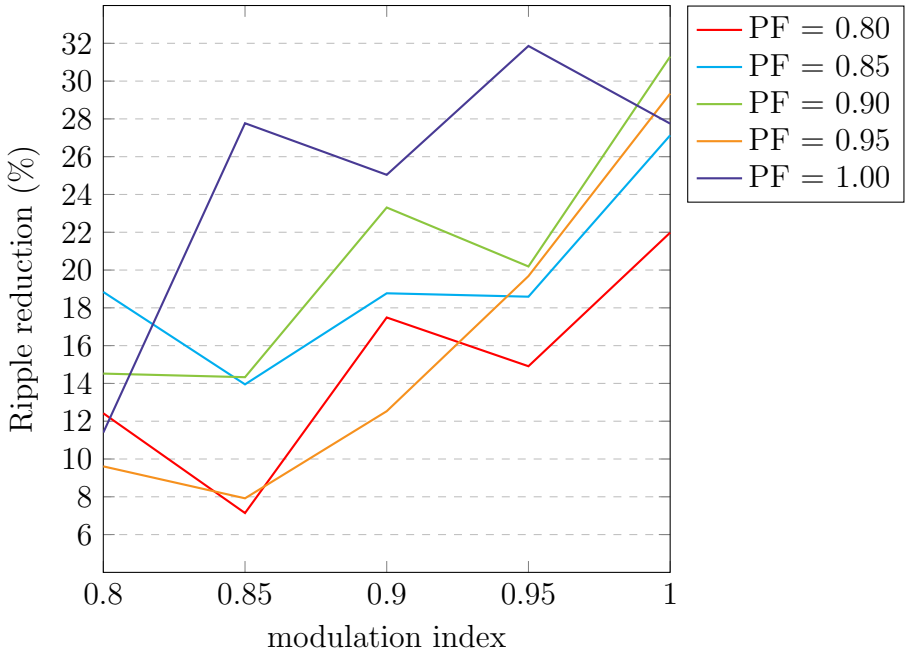
Figure 4.16: Ripple at min loss OP compared to CCSC OP

reduction is achieved by minimizing losses.

Loss Comparison: Min. Ripple Operating Point vs. CCSC Operating Point

This section compares losses at the minimum ripple operating point to those at the operating point where circulating currents are completely suppressed. The graph in Fig. 4.17 shows these results for lagging power factor loads, whereas Fig. 4.18 shows them for the leading power factor loads. The "y" axis on these graphs shows a loss reduction in the minimum ripple operating point as compared to the losses at the operating point where circulating currents are completely suppressed; therefore, a negative value represents a loss increase.

It can be seen in Fig.4.17 that when serving a lagging power factor load with a modulation index between 0.8 to 0.95, operating the converter at the minimum ripple operating point increases losses between 0.32% up to 16.12%. The only cases when losses are reduced at the minimum ripple operating point are when a unity power factor load is served, with a modulation index larger than 0.9. This means that minimizing ripple for lagging power



(b) leading pf.

Figure 4.16: Ripple at min loss OP compared to CCSC OP

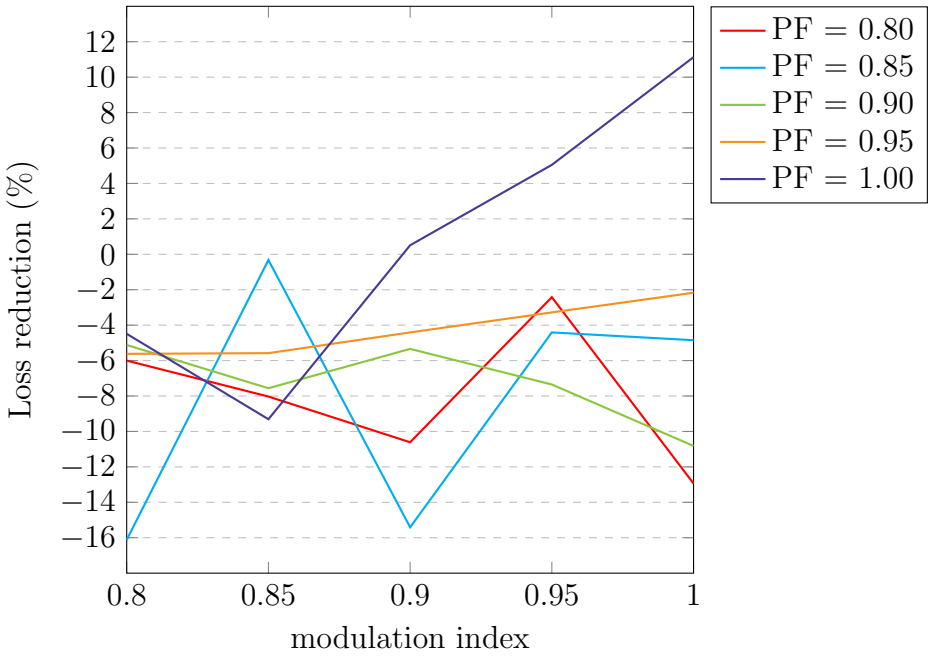


Figure 4.17: Loss reduction at min ripple OP compared to CCSC OP (lagging pf)

factors loads is not the most efficient (loss-wise) way of operating the converter. Note that the loss analysis presented in this thesis considers only the switching and conduction losses

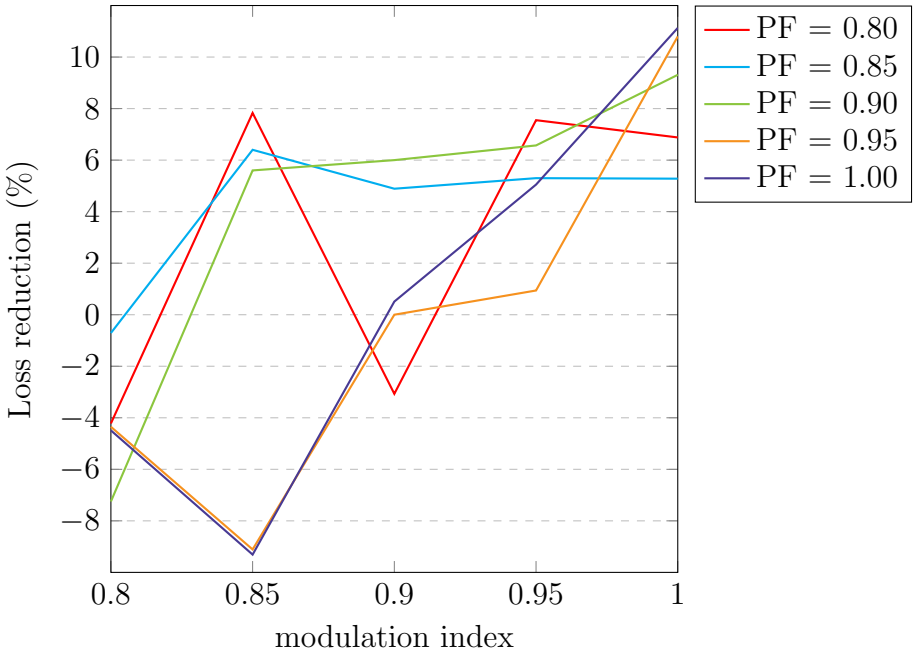


Figure 4.18: Loss reduction at min ripple OP compared to CCSC OP (leading pf)

of the semiconductors; the losses of other components of the converter such as inductors are not considered here.

On the contrary, Fig.4.18, shows that when serving leading power factor loads, for some modulation indices, it is possible to reduce losses when ripple is minimized, however this loss reduction is not even half the reduction at the minimum loss operating point.

These last three subsections show how minimizing ripple or losses affect each other, providing an insight on how to control each of these parameters according the operating conditions of the converter.

4.1.4 Semiconductors Rating Assessment

In order to study the impact of circulating current injection on the semiconductors rating, Figs. 4.19 and 4.20 show how the capacitor voltage ripple and arm current waveforms change when circulating currents are injected. Fig. 4.19 shows these waveforms for a lagging power factor load whereas Fig. 4.20 shows them for a leading power factor load; in both cases the modulation index is 0.95 and the power factor is 0.8. These graphs shows four operating

points: i) Natural OP, ii) CCSC OP, iii) Minimum ripple OP, iv) Minimum losses OP.

In these two figures, the solid blue lines represent the waveforms from the detailed model in PSCAD/EMTDC whereas the red dashed ones show the analytically obtained waveforms. It can be seen that there is a small difference between these two sets of waveforms, thus confirming the accuracy of the presented model.

The capacitor voltage ripple values for these operating points as well as the peak arm current are highlighted in the aforementioned Figures. The arm current waveform is useful for evaluating how the circulating current injection will affect its peak values. Notice that the capacitor voltage waveforms for each operating point in Figs. 4.19 and 4.20 are 180° phase shifted with respect to each other (i.e., flipped vertically). This is not the case for the arm current waveforms, thus the peak currents values for each of the presented operating points are not the same for the lagging and leading power factor loads.

For this analysis the characteristics of the ST1500GXH24 IGBT are taken into consideration. This 4500V, 1500A (RMS) (3000 A non-repetitive peak) IGBT is selected such that there is room to increase the voltage and current stresses on the device when working at the rated power. The nominal arm current of the converter is 1000 A, which will keep the IGBT working at 66.6% its rated capacity at the rated power with CCSC. Nevertheless, the peak value of the current waveform should never exceed 3000 A, as this is the absolute maximum rating of this IGBT. As for the voltage, the rated submodule voltage is 2250 V, which is half of the rated voltage of the semiconductor.

It can be seen in Figs. 4.19 and 4.20 that even when the largest circulating current is injected (i.e., when the ripple is minimized), the peak current, RMS current, and SM voltage do not exceed the rating of the semiconductor. In order to calculate the total RMS arm current, the following expression is used:

$$I_{\text{armRMS}} = \frac{I_{\text{DC}}}{3} + \sqrt{\left(\frac{I_{\text{A}}}{2}\right)^2 + \left(\frac{I_{\text{2nd}}}{\sqrt{2}}\right)^2} \tag{4.1}$$

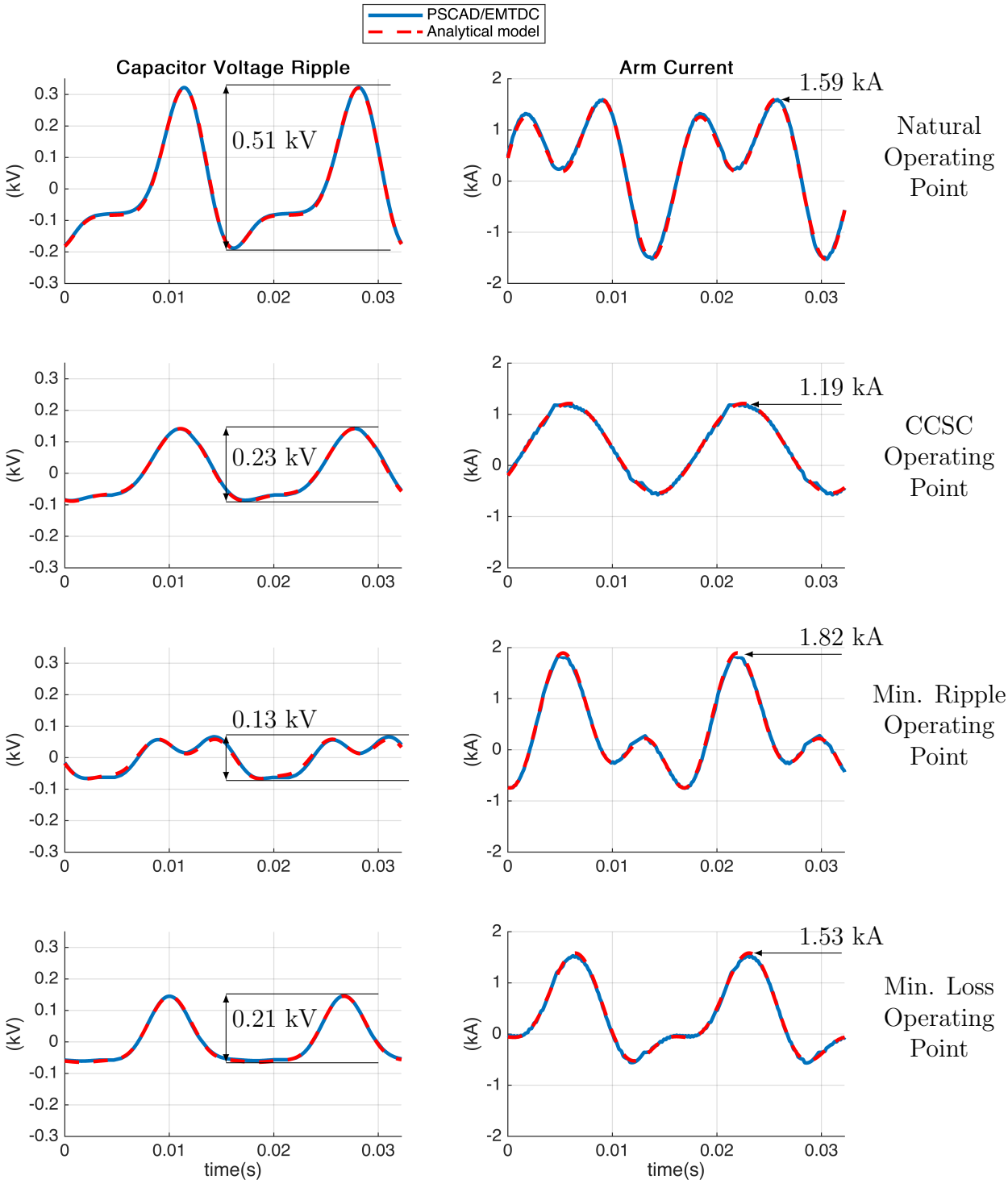


Figure 4.19: Waveform variations, $m = 0.95$, PF $= 0.8$ lagging.

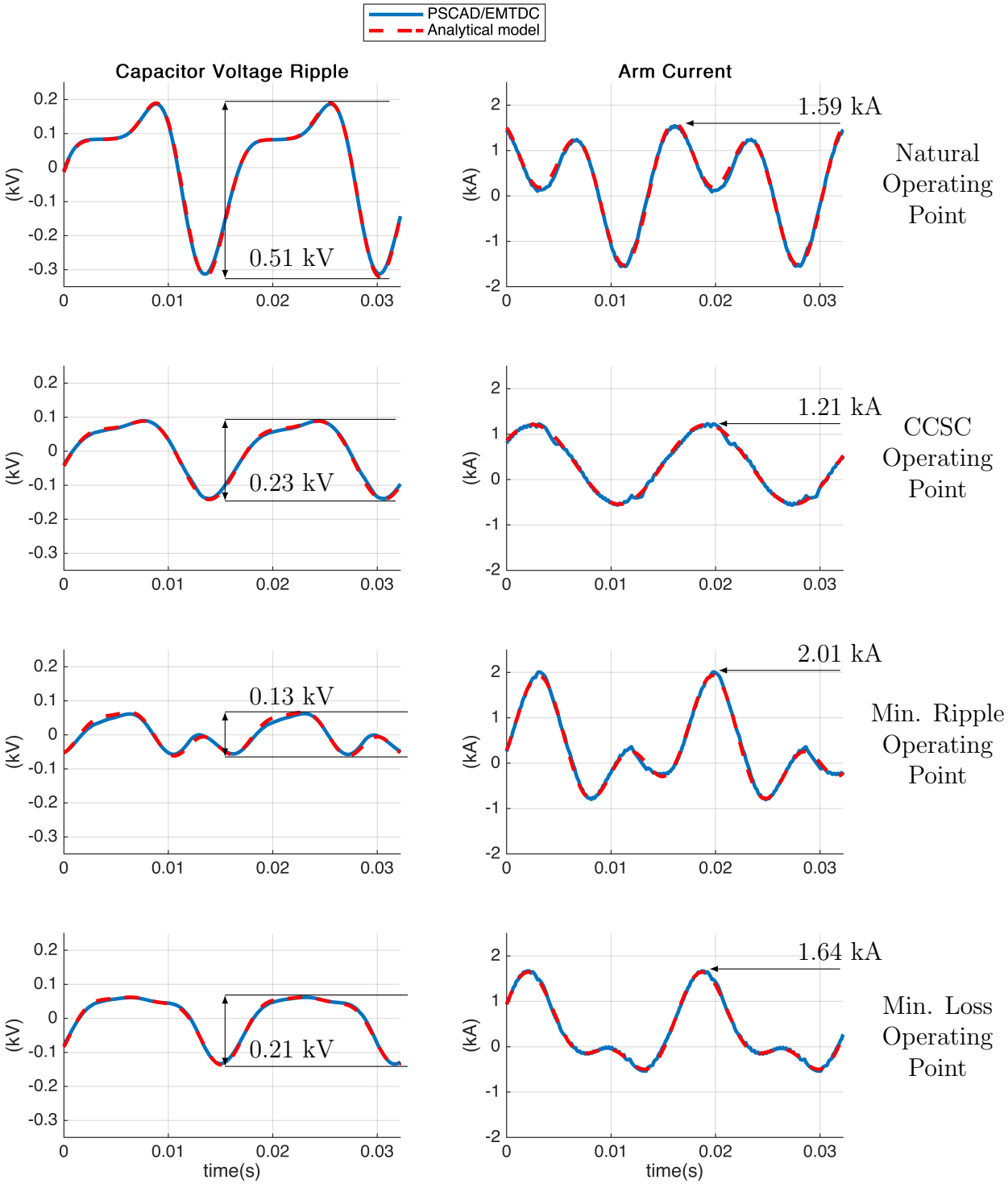


Figure 4.20: Waveform variations, $m = 0.95$, PF $= 0.8$ leading.

For example, considering the operating point with the highest circulating current injection as the worst case scenario among the ones shown in the previous figures (minimum ripple operating point for either the lagging or leading power factor load case). The DC current I_{DC} at this point is 1000 A, the fundamental component of the arm current I_{A} is 1241 A RMS, and the second harmonic component $I_{2\mathrm{nd}}$ is 750 A peak. Substituting these values in (4.1) yields the RMS value of the arm current as 1149 A RMS, which does not violate the RMS rating of the selected submodule. As for the peak value of the arm current, the worst-case scenario is seen for the leading power factor case, where the peak current reaches 2.01 kA, which is still below the absolute maximum value of 3000 A. A similar analysis could be useful to ultimately decide whether to follow any of the proposed reductions and how it will impact on the converter's cost and size.

4.1.5 HVDC Transmission System Case Study

This section presents a case study where the proposed ripple reduction method is implemented and evaluated in an HVDC transmission system [47] modeled in PSCAD/EMTDC. Fig. 4.21 shows a schematic of the system. All the system parameters and components specifications are available at [47].

This case models a VSC-HVDC transmission system linking offshore wind farms with an onshore AC grid. The offshore wind farms are composed of two groups of wind turbines (i): doubly-fed induction generators (DFIG) and (ii) permanent magnet (PM) generators. Each set of wind farms is connected to the sending end of the HVDC system via a 30 km long, 230 kV line.

The VSC-HVDC system is composed of two identical MMC converters connected by a 200 km long, ± 320 kV DC line. The receiving end is connected to an AC system where the short circuit ratio (SCR) at the PCC is equal to 3.0. The system operates with the sending end bus as PV bus, whereas the receiving end is configured to control the AC and DC voltages. The characteristics of the MMC-based HVDC system are presented in Table

4.2.

Table 4.2: HVDC systems characteristics

Rated power: 900 MW	DC line length: 200 km
DC line voltage: ± 320 kV	Number of SMs per arm $N = 76$
Nominal SM voltage (V_{csm}) = 8.42 kV	SM capacitance (C_{sm}) = 2.8 mF
Arm inductance = 50 mH	AC system voltage: 230 kV
Frequency: 50 Hz	PCC SCR = 3.0

The HVDC system is set to operate at its rated power and voltage (900 MW, 230 kV AC, ± 320 kV DC). For this operating condition, the capacitor voltage ripple profile of the converters was calculated and the minimum ripple operating point was determined. Once the system reached steady state, the circulating currents that yield the minimum ripple were injected.

Figs. 4.22 and 4.23 show the capacitor voltage ripple and arm current waveforms for the sending and receiving ends respectively. The system initially operates with a CCSC, then at $t = 4$ s the reference of the controller is changed so that the minimum ripple operating point is reached.

The left-hand side columns of these graphs show the capacitor voltage ripple, whereas the right-hand side ones show the arm current waveforms. The top two graphs in each figure show a 0.8 s window time frame where the transition between operating with a CCSC and operating at the minimum ripple can be seen. These graphs show that there is no overshoot in the arm currents when the operating point changes and that the capacitor voltage ripple quickly reaches its desired operating point.

For the capacitor voltage ripple waveforms shown, a difference of less than 1% between each operating point can be observed between the sending and receiving ends. The voltage drop in the DC line under this operating condition is also around 1% its rated value, which explains this mismatch. It can also be seen that when ripple is minimized, it is reduced 38% and 43% as compared to the CCSC operating point for the sending and receiving ends

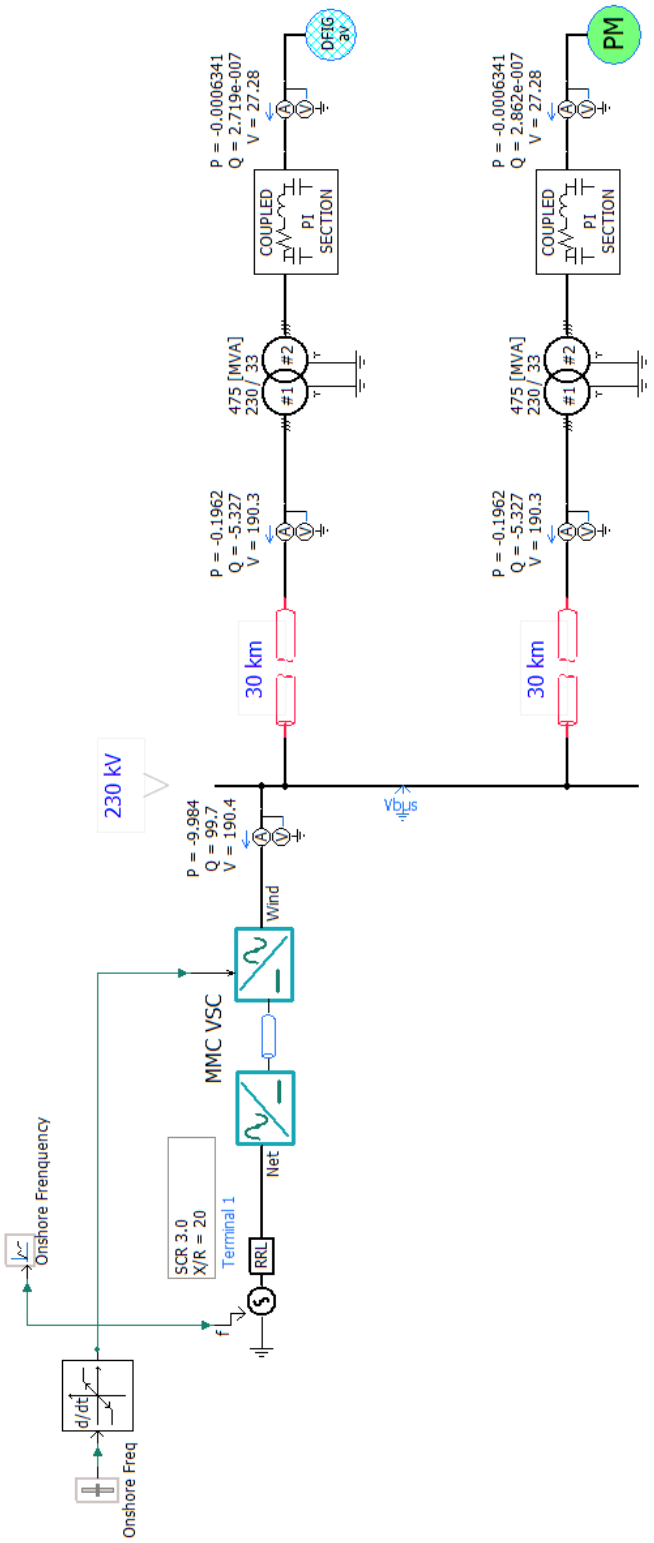


Figure 4.21: Case study schematic.

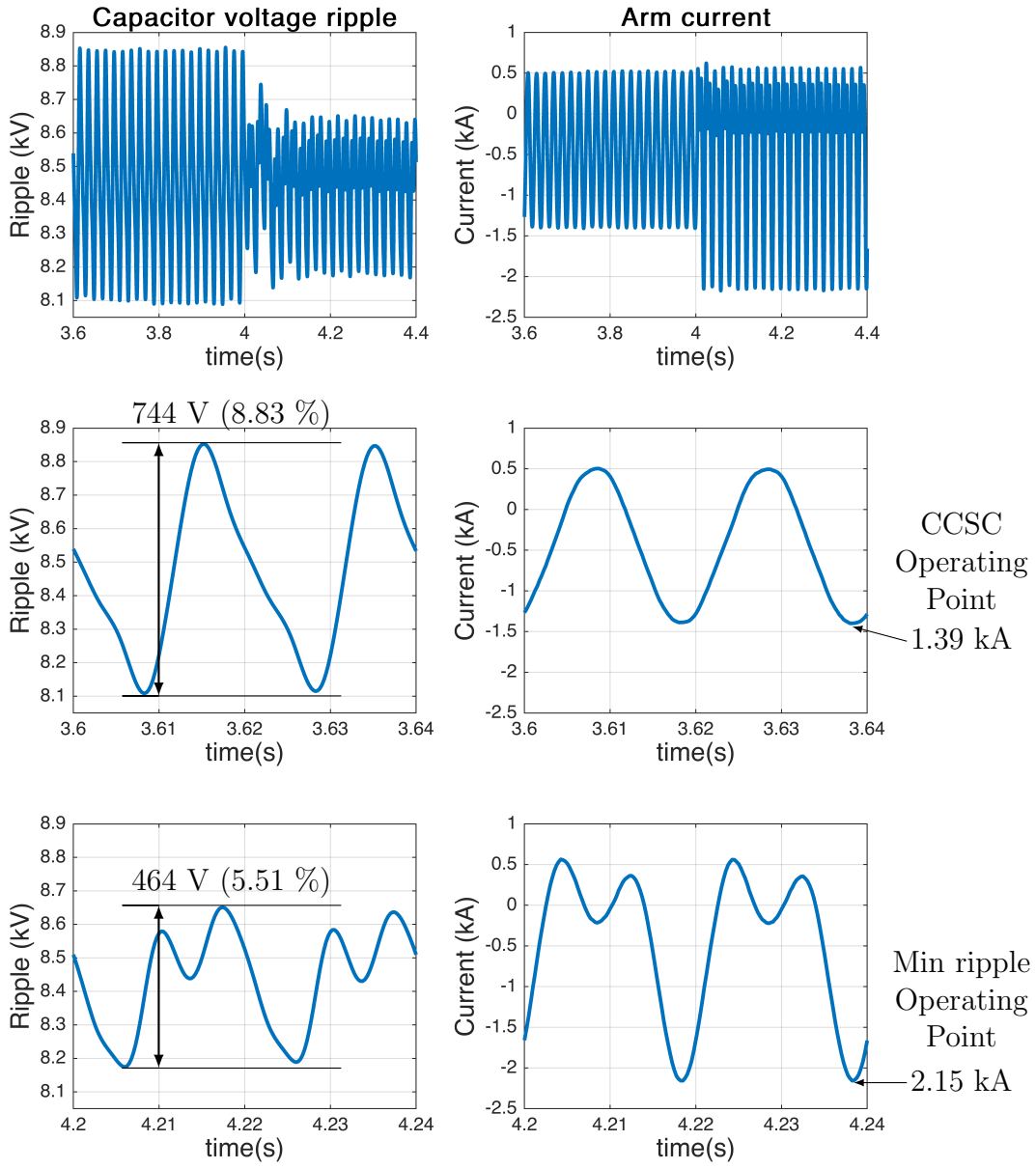


Figure 4.22: Capacitor voltage ripple and arm current at different operating points (sending end).

respectively.

The arm current waveforms in Figs. 4.22 and 4.23 show a 180° phase difference between them. This is easily seen in the minimum ripple operating point graphs (bottom graphs).

Receiving end

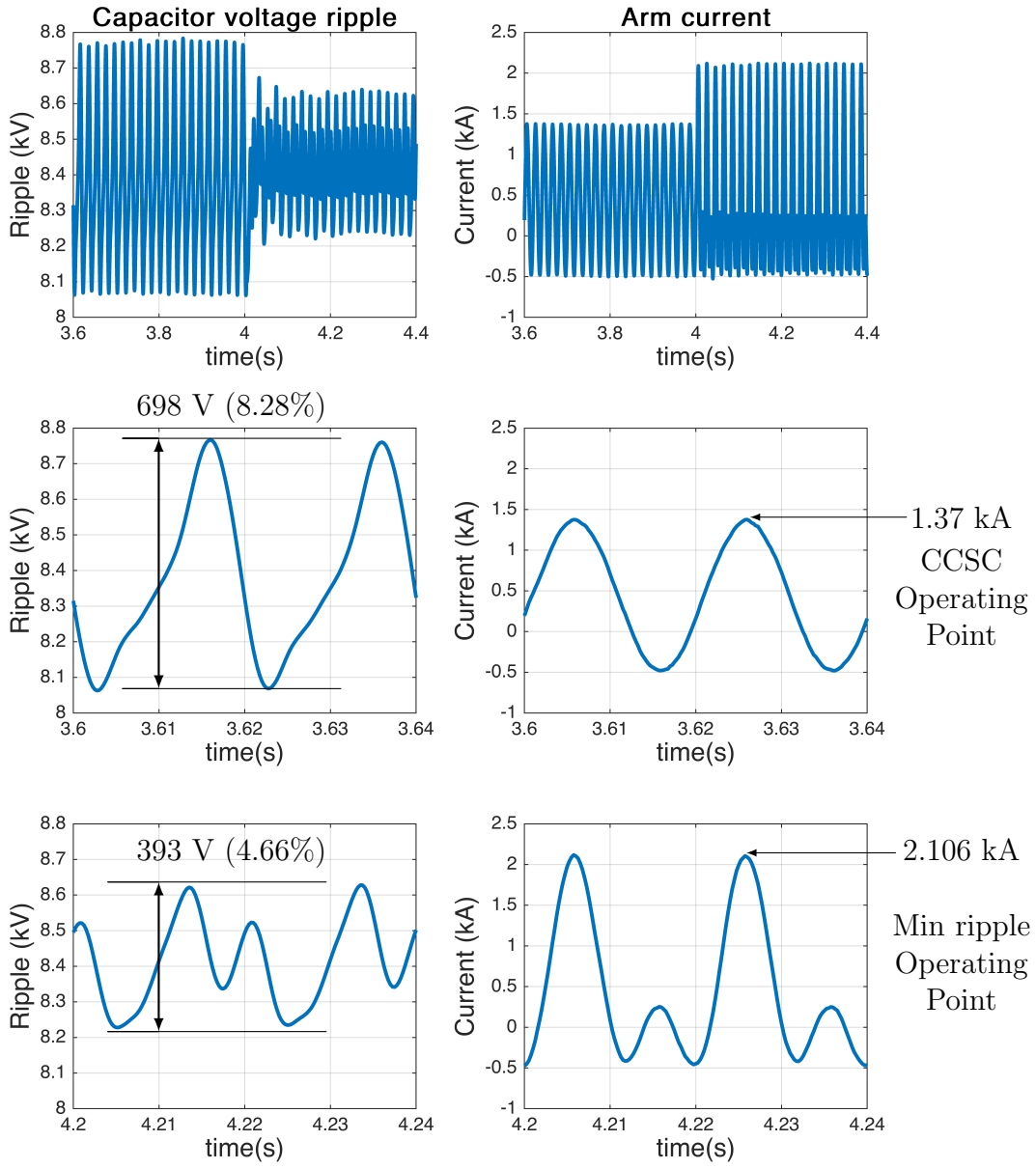


Figure 4.23: Capacitor voltage ripple and arm current at different operating points (receiving end).

This phase angle difference needs to be considered when injecting circulating current in order to properly achieve ripple reduction in both converters simultaneously. This difference is due to the power flow direction and it can be seen that the difference between the peak values is

negligible for the purpose of semiconductor ratings assessment.

A loss analysis is not included for two main reasons: SM voltage ratings and number of submodules. In the first case, to the knowledge of the author, the IGBTs with highest voltage rating available are 6.5 kV [48], yet it is not possible to calculate losses for a real-world semiconductor for the converter shown. As for the number of submodules: calculating losses for two 3-phase MMCs with 76 SM per arm would require enough computing power to ensure practical simulation time, which was not available.

These results show the validity of the proposed method to reduce ripple in MMCs. The ripple difference between the analytical model and the results in PSCAD was less than 1%.

4.2 Hardware Validation

4.2.1 Real-Time Environment Validation

In order to further verify the validity of the proposed ripple reduction method, a converter with the characteristics listed in Table 3.1, and connected to Load 1 from Table 4.1, operated with a modulation index of 0.95 is simulated in a real-time digital simulator (RTDS). It is not possible to verify the loss analysis previously described as there is no model to calculate the losses in the RTDS in a similar way it was calculated in PSCAD/EMTDC.

In this analysis, the second harmonic controller shown in Fig. 3.3 was implemented in the RTDS as shown in Fig. 4.24 and in an STM32 development board in a Control Hardware-in-Loop (CHIL) environment as shown in Fig. 4.25. The results obtained when using this external controller are compared to those obtained when the second harmonic controller is implemented in the RTDS.

The development board used is a STM32-H746ZG, which is a high-performance Microcontroller Unit (MCU). This board's core is the 32-bit ARM®Cortex®M7 CPU running at a frequency of up to 216 MHz. The board also features a 3x12-bit, 2.4 Mega-Samples Per Second (MSPS) Analog-to-Digital Converter (ADC). The specified microcontroller board

only includes two Digital-to-Analog-Converters (DAC) and since three analog signals need to be sent back to the RTDS, an external DAC needs to be used. For this purpose Digilent's PmodDA4 board is used. This 8x12-bit Digital-to-Analog Converter (DAC) connects to the STM32 board via Serial Peripheral Interface (SPI) protocol.

Fig. 4.24 shows a block diagram depicting system when the second harmonic controller is implemented in the RTDS, whereas Fig. 4.25 shows the system when the second harmonic controller is implemented in the development board. In both cases, the converter model in RTDS is simulated using the MMC5 model, which is specifically designed for VSC-type converters in the small time-step environment. The converter runs with a time-step of 2.5 µs, whereas the converter controller (which includes the SHC) runs at 50 µs time step.

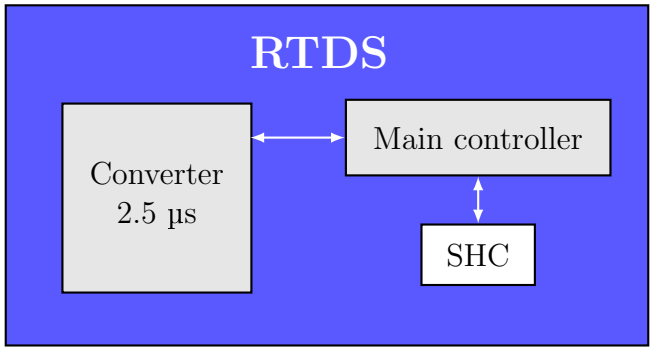


Figure 4.24: Real-time environment setup diagram.

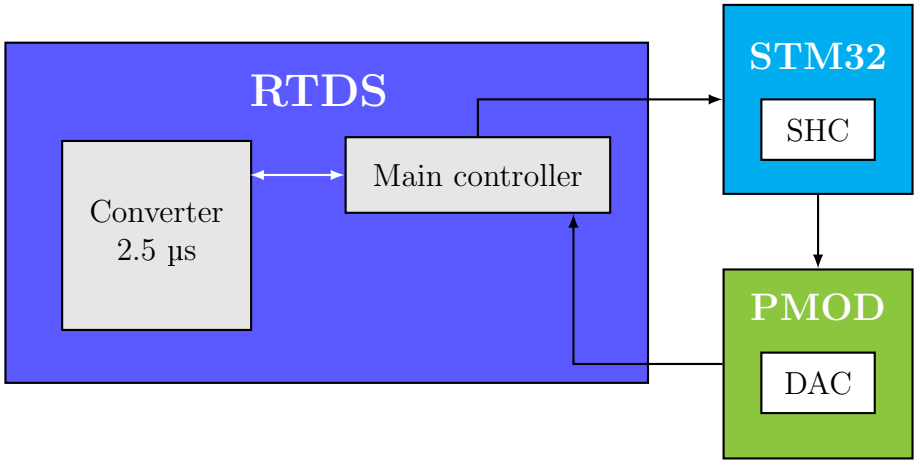


Figure 4.25: Real-time environment setup diagram with Control Hardware-in-Loop.

When using the system depicted in Fig. 4.25 it was verified that the latency between

reading the circulating current information from the RTDS, and injecting back the required modulating waveform is less than 50 μs.

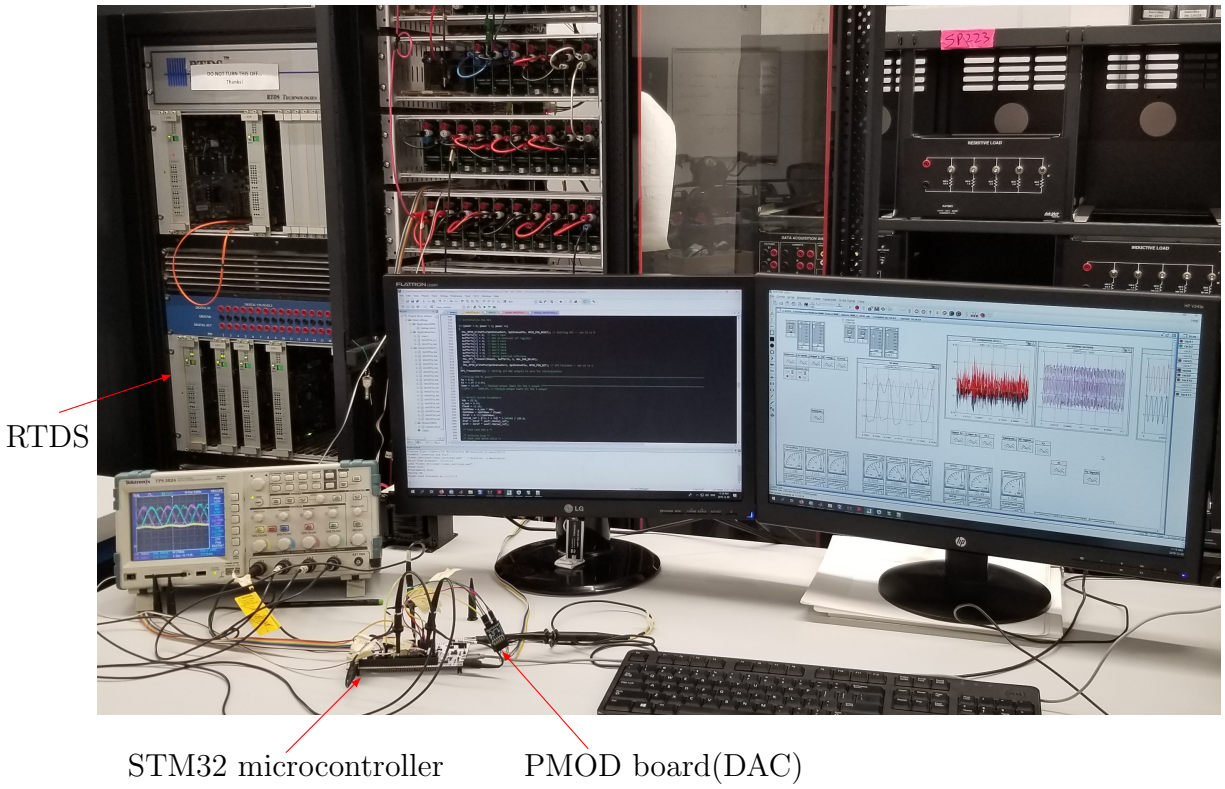


Figure 4.26: CHIL lab setup.

Fig. 4.27 shows the average capacitor voltage ripple waveform for the upper and lower arms (black and red traces respectively) obtained from this analysis. The top two graphs show a six-second window time frame, where the capacitor voltage ripple is varied over three different OPs. The graphs on the left column depict the results when the SHC is implemented in the RTDS whereas the ones on the right column show the results when the SHC is implemented in the STM32 microcontroller.

In the top two graphs when time is between 0 to 0.9 seconds, the converter is operating at its natural operating point, with no circulating current control. This is marked with an "a". From 0.9 to 1.9 seconds, the converter is operated with a CCSC. This is marked with a "b". From 1.9 to 3.9 seconds the converter is operated at its minimum ripple operating point. This is marked with a "c". From 3.9 to 6 the converter is back to its CCSC operating

conditions. It can be seen that the differences between the results obtained when the SHC is implemented in the RTDS and in the STM32 MCU are quite small.

In Fig. 4.27 the "a" graphs show a zoom-in to the ripple waveform. In the RTDS results ripple is 497 V, which is 22% ripple of the nominal capacitor voltage. In the STM32 results, this ripple is approximately 526 V, which represents 23.7 % of the nominal capacitor voltage. It can also be seen that the ripple obtained with the controller on the STM32 MCU is oscillating. This is oscillation is due to noise on the modulating signal component that gets deviated from zero. The theoretical ripple value for this operating point is 22.39%.

The "b" graphs show a much smaller difference between the two controllers' implementation. The difference between them two is 2 V, which makes the error between these two values less than 0.09%. In both cases, the ripple is around 10% the capacitor's nominal voltage, agreeing with the theoretical expected value of 10.23%.

The "c" graph shows the minimum ripple operating point where the difference between the two controllers is 2 V. The theoretical ripple in this case is 128.93 V, which is 5.57% of the nominal capacitor voltage. The errors are 0.136% and 0.047% when the SHC is implemented in the RTDS and the SMT32 MCU respectively, thus confirming the accuracy of the proposed method.

Similar to what was shown in Fig. 4.27, Fig. 4.28 presents the circulating currents for the natural operating point (denoted with "a"), CCSC operating point (denoted with "b"), and the minimum ripple operating point (denoted with "c") when the SHC is implemented in the RTDS and in the SMT32 MCU. The circulating currents of phase a, b and c are represented in black, red and blue traces respectively. It can be seen in the top two graphs that the controller do not cause overshoots in the circulating current when the operating point is changed.

As was previously shown, in the natural operating point case ("a" graph), the circulating currents obtained when the SHC is implemented in the STM32 MCU show some oscillation around its nominal value. In this case, the natural circulating current is 981 A peak, which is

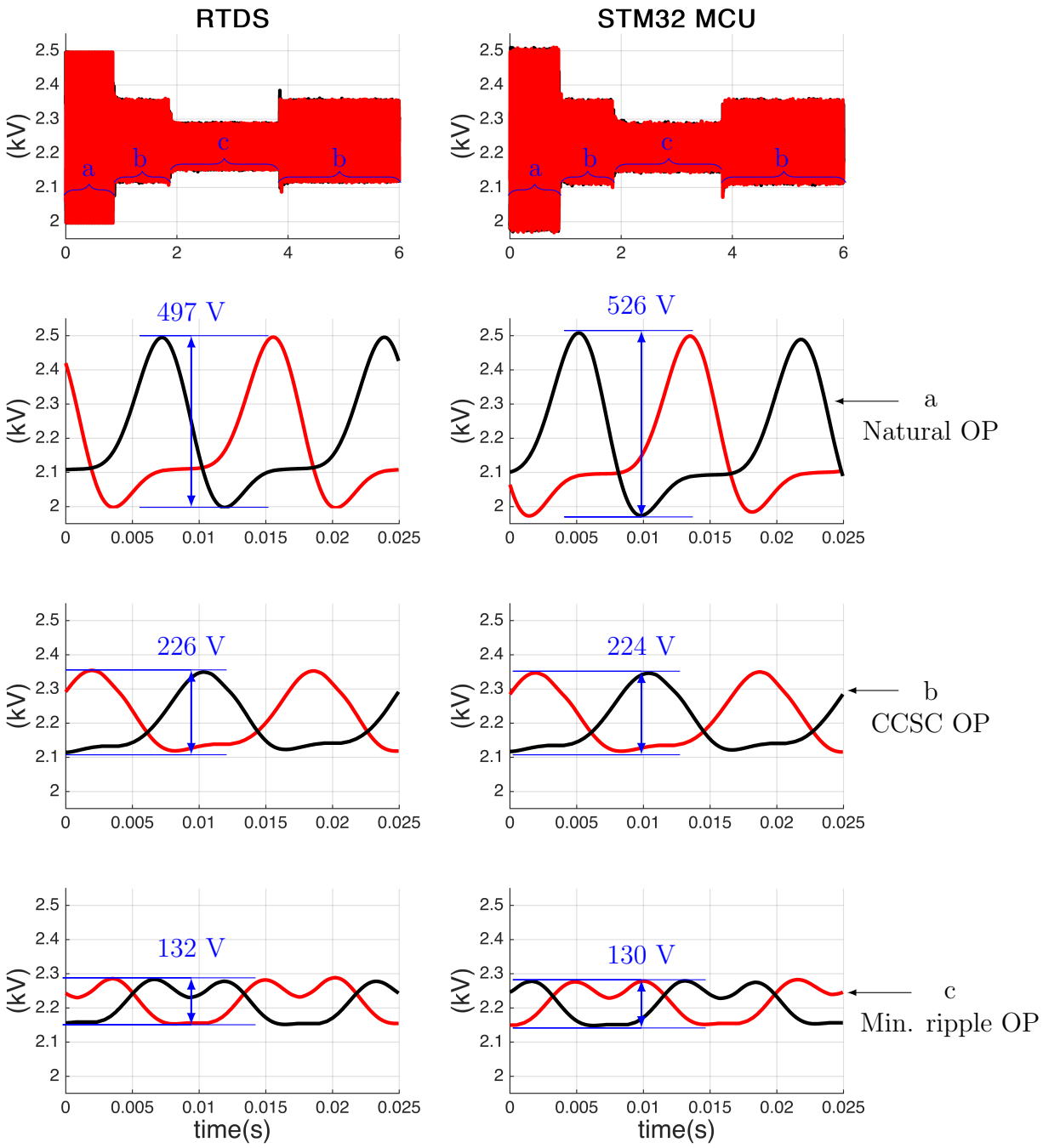


Figure 4.27: Capacitor voltage ripple variation. In the top graph "a" is Natural OP, "b" is CCSC OP, "c" is Min. ripple OP. pf = 0.8 lagging, modulation index = 0.95

the value observed on the RTDS results. In the STM32 MCU case, the circulating currents show how a small variation in the second-order component of the modulating waveform causes the circulating current to vary. This modulating waveform component is supposed to be zero when the SHC is deactivated, so the natural second-order currents will flow. Since there was noise in the signal, variations in the circulating currents are observed.

In the CCSC case ("b" graph) both the RTDS and STM32 results agree to a high extent. There is a remaining higher-order component in the arm currents, but the second-order component is practically zero.

In the minimum ripple case ("c" graph) the theoretical circulating current is 710 A peak, which is used as the reference for the controller in this case. The results show that when the controller is implemented both in the RTDS and in the STM32 board, there is a small variation from this value and also some oscillations are seen (these oscillations are larger on the results from the STM32 MCU). The peak values vary form 700 to 730 A, which yields an error of less than ±3% in each case. Although small deviations from the theoretical values are observed, this error does not affect greatly the overall performance of the controller, as it was previously shown that the ripple error for this specific case is less than 0.2%.

4.3 MMC Prototype Validation

The capacitor voltage ripple variation method proposed is further validated by implementing a ripple minimization on a lab MMC prototype. Table 4.3 lists the converter characteristics, as well as the tests conditions. Fig. 4.29 shows a photo of lab MMC prototype.

Table 4.3: MMC prototype parameters and test conditions

$N_{\text{sm}} = 12$	Arm inductance: 5 mH
C_{sm}: 4700 µF	DC Voltage: 120 V
Load: 10 mH, 13.3 Ω	modulation index = 0.95

For this operating point, the theoretical peak value for the natural circulating currents is

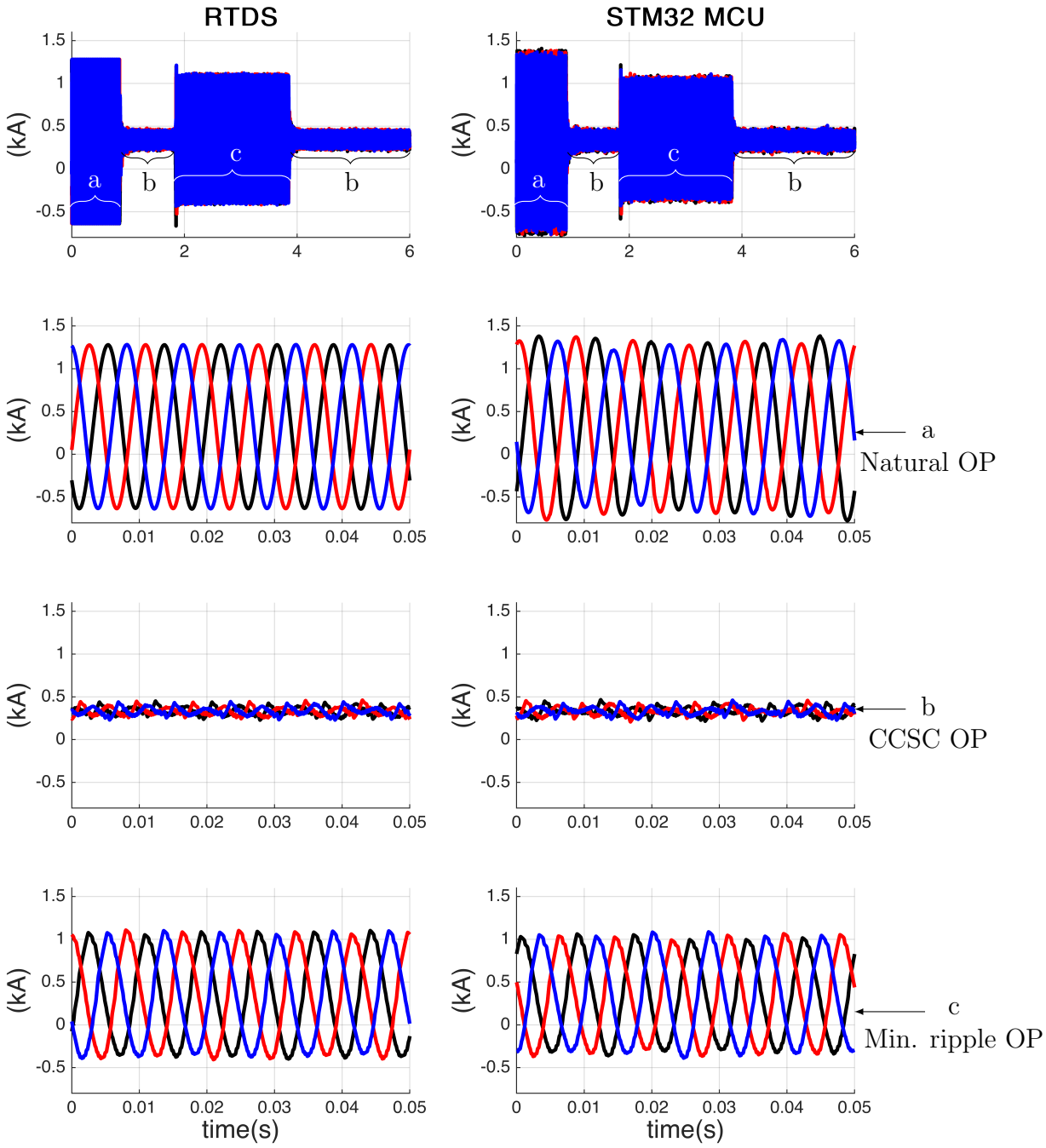


Figure 4.28: Circulating currents for capacitor voltage ripple variation. In the top graph "a" is Natural OP, "b" is CCSC OP, "c" is Min. ripple OP.

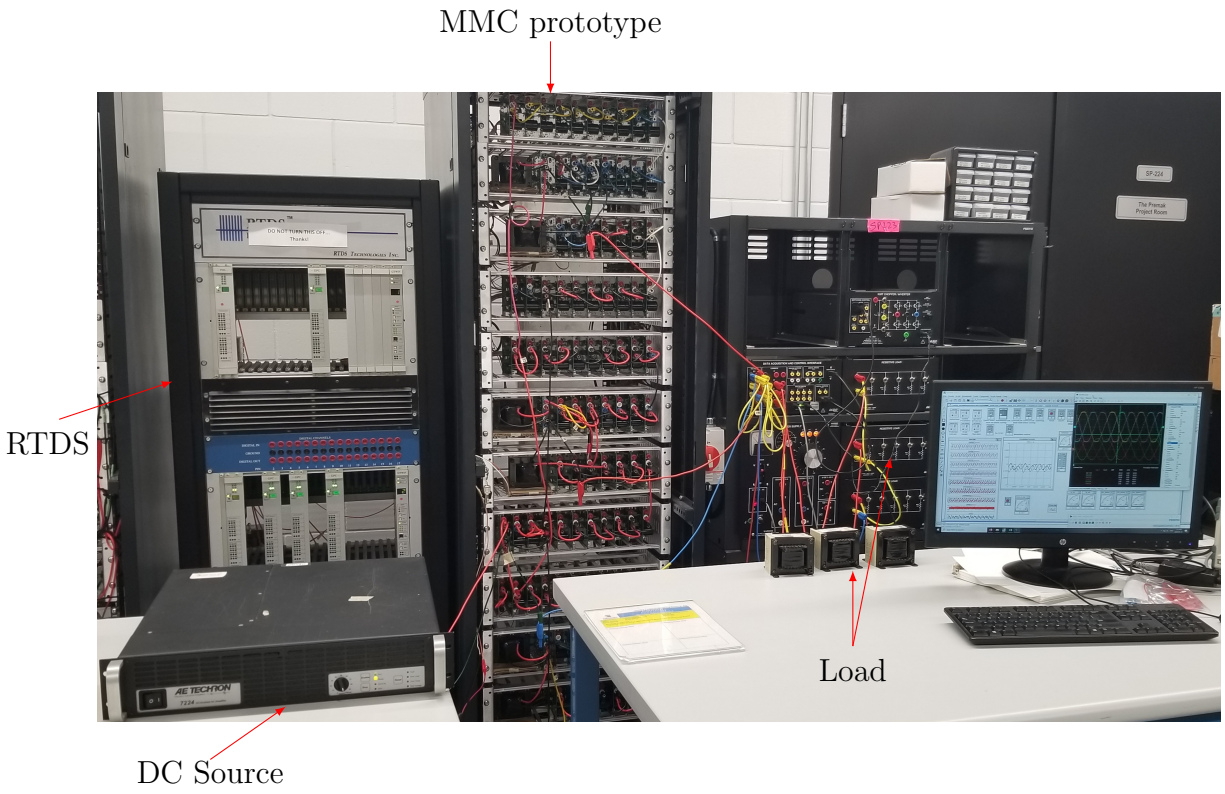


Figure 4.29: Lab. MMC prototype.

0.568 A. The rated capacitor voltage at these operating conditions is 10 V, and the theoretical ripple at the natural operating point is 10.98% of its nominal value, or 1.098 V. At the CCSC OP, the theoretical ripple is 8.41%, or 0.841 V. Finally, at the minimum ripple operating point, a ripple of 4.132 %, or 0.413 V is expected; to achieve this ripple, a circulating current of 1.6 A peak should be injected.

Fig. 4.30 show the resulting capacitor voltage ripple waveforms on the left, and the circulating current waveforms on the right for each of these operating points. On the left hand side, the lower and upper arm average capacitor voltage waveforms are shown in black and red respectively; on the right hand side, the circulating currents from phase A, B and C are shown in black, red and blue respectively. It can be seen that the ripple and circulating current values are not as predicted.

In the natural OP case, a ripple of 1.02 V or 10.2%, is observed for the lower arm capac-

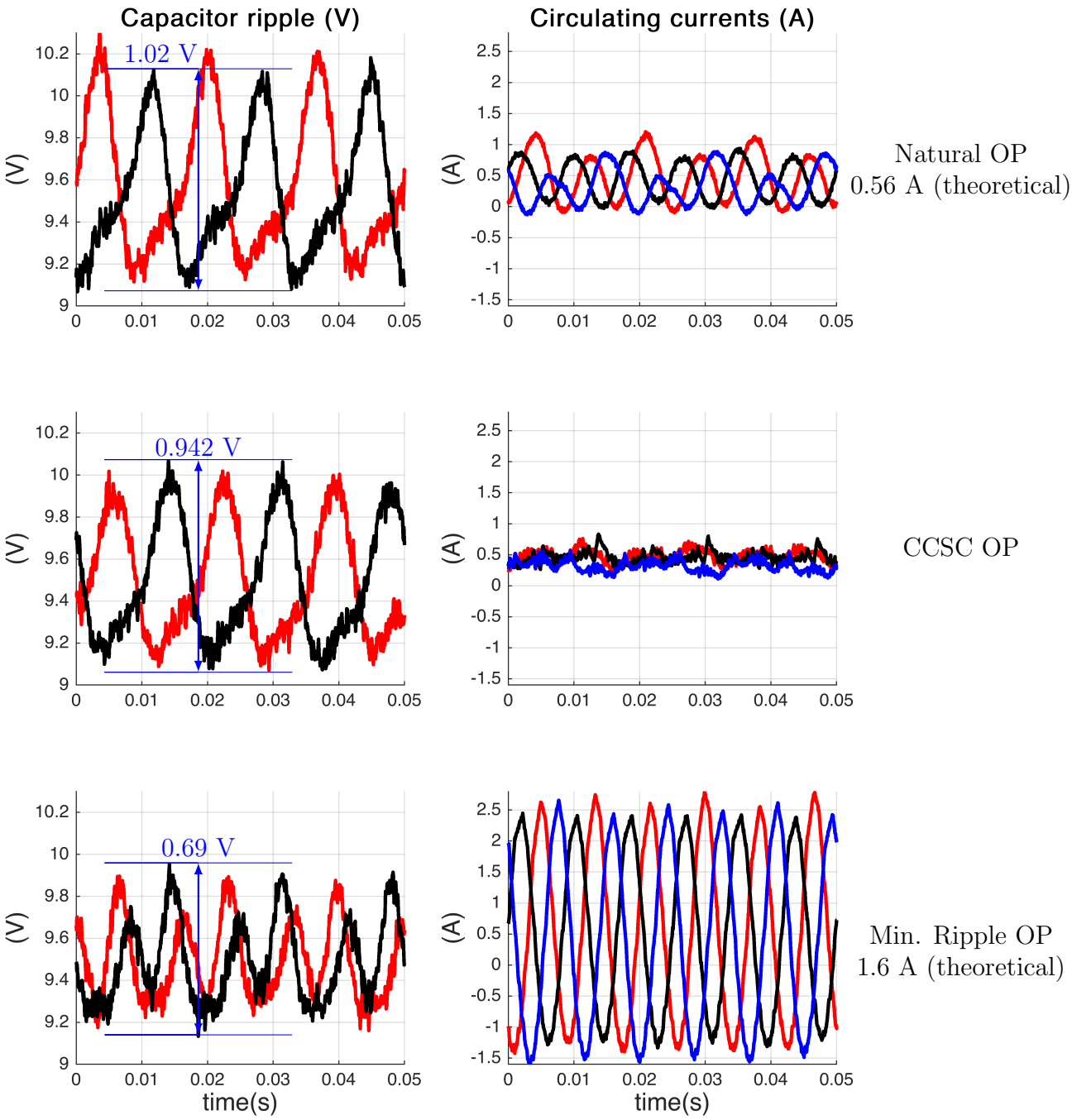


Figure 4.30: Capacitor voltage ripple and circulating currents under unbalanced conditions.

itors (black waveforms), whereas for the upper arm it is 1.18 V or 11.85 % (red waveform, measurement not shown). As for the circulating currents, it can be seen that there is a large variation between phases, indicating there is unbalance in the circuit. Similar outcomes are seen in the CCSC and Min. Ripple OPs graphs, where the results do not match the expected values.

The arm and load inductors were measured using an LCR filter to get precise inductance values and corroborate that the cause for these results was an unbalanced system. It was found that, at 60 Hz, the arm inductances varied between 3.45 mH, to 4.95 mH for the six arm inductors in the converter. Similar results were obtained at 120 Hz, 180Hz, and 360 Hz. This show a variation of 31% of the rated inductance value (taking 5 mH as the reference value).

In the case of the load inductors, their values were between 12.5mH to 13.3mH at 60 Hz. Similar results were observed at 120 Hz, 180 Hz, and 360 Hz. This represents a variation of up to 30% of the rated inductance (10 mH).

The inductors used for the arm and load are Hammond D.C. reactors 195G10 and 195J10, rated at 5 mH and 10 mH respectively at 10 A DC, with a tolerance of 15% on both resistance and inductance.

Since the results presented were using low currents (less than 3 A), the inductors were further tested, up to their rated values using a controlled AC source. The inductance was calculated by measuring current and the voltage drop across them. The obtained results using this method were similar to what was previously described.

This suggests that in order to properly control the capacitor voltage ripple using this method, the converter must be properly balanced. Nevertheless, it can be seen in Fig. 4.30 that although there was unbalance, the minimum ripple OP reduced ripple by 37.15% instead of the expected 62.38% reduction.

Chapter 5

Conclusions, Contributions and Future Work

This chapter summarizes the overall contributions of this work as well as its conclusions. The chapter also suggests directions for future pursuit.

5.1 Contributions and Conclusions

In this thesis an existing method to analytically calculate the submodule capacitor voltage ripple in a HB-MMC was used to develop methods for development of methods to use, rather than eliminate, circulating current. This method considers the presence of second order harmonics components in the circulating current while neglecting any other higher order components. It was verified that neglecting these terms do not affect the accuracy of the method in a significant way.

By varying the amount of second-order harmonic component in the arm currents it was possible to control the capacitor voltage ripple of the HB-MMC within a wide range of values. It was shown that there is a capacitor voltage ripple profile for MMCs where there is a minimum ripple operating point that does not coincide with the operating point when a CCSC is used.

In order to implement the capacitor voltage variation, the reference values of the widely used CCSC were modified. By injecting judicious amount of circulating currents in HB-MMCs it is possible to reduce its capacitor voltage ripple beyond the point where circulating currents are completely eliminated, as is the common practice.

An EMT-based switch model was used to calculate how injecting circulating currents for capacitor ripple variation affects the converter losses. It was found that there is an optimal operating point where both losses and ripple can be further reduced beyond the point where circulating currents are completely suppressed. This suggests that the use of a CCSC might not be the most efficient approach to operate a HB-MMC. The importance of calculating the peak and RMS values of the arm current in order to ensure safe operation of the converter semiconductors was presented.

The proposed method has two main drawbacks: i) it relies on a numerical solution for capacitor voltage ripple reduction, ii) it relies on extensive simulation to determine the minimum loss operating points. Therefore, this method requires the use of look-up tables when operating a converter.

A publication has resulted from the work presented in this thesis:

[1] "Effects of Second-Order Circulating Current Injection on Capacitor Voltage Ripple and Losses in HB-MMCs", in *2020 IEEE PES General Meeting*, Aug. 2020, Montreal, QC, Canada.

5.2 Recommendations for Future Work

An economical assessment of implementing this method to reduce capacitance, converter footprint and losses, while potentially increasing semiconductor ratings might provide an insight of the feasibility of this method.

Developing a minimum-loss-point tracking algorithm to reduce converter losses might be a more feasible approach to reduce losses in a HB-MMC.

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