Single-phase Single-stage Grid-connected Converters using High Frequency Virtually Grounded Technique

by

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Abstract

In the modern power grid, renewable energy has become one kind of major energy resources in the world as it is environmentally friendly and sustainable. To effectively convert the power between the ac grid and different energy sources, power electronic converters are required. They act as an interface to establish a connection between the renewable energy source and the utility grid or microgrid network. Meanwhile, the power converters are also the power interface between different electronic appliances and the ac grid.

This thesis aims to research on high frequency virtually grounded technique and to develop a new set of converter topology that is with high efficiency and low leakage current performance. Different kinds of common-mode migration technique are studied in terms of system performance. By using the theory of high frequency virtually grounded technique as a foundation, the new series of converter topology family is established. According to the needs in different applications, several types of converters have been developed which is high efficiency and low leakage current. In the new converter family, a bridgeless power factor correction rectifier is studied for the general boost-type power factor correction circuit. For applications with reactive power demand, a bidirectional voltage source converter is introduced. In addition, a buck-boost-type bridgeless power factor corrector is proposed for those wide output voltage range grid-connected converter applications. Lastly, a buck-boost-type inverter is discussed in this thesis for those high efficiency wide input voltage range inverter systems.

An in-depth study on the grid-connected converter topologies is provided which includes the detailed operation principles and the corresponding system stability analysis. All of the described topologies are experimentally verified which shows good agreement with the theoretical

knowledge. Moreover, the performance of those converters is measured based on industrial requirements in terms of efficiency, total harmonic distortion, power factor and leakage current.

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Contributions of Authors

The core of this thesis is comprised of six journal papers. Five of them have been published and one is under review. All the papers are with multiple authors. K.M. Siu is the first author in four of these papers and co-author in another two papers. The contributions of the authors of these papers are explained below.

Chapter 3: C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, "Active Virtual Ground—Bridgeless PFC Topology," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017.

In this chapter, the idea was developed by C. N. M. Ho and R. T. Li. The manuscript was mainly prepared by C. N. M. Ho and was edited by all of the authors. C. N. M. Ho conducted on background studies, topology analysis, and characteristic deviations. R. T. Li provided valuable advice on different practical issues during the work. I carried on system implementation and performance evaluation. I also modelled the circuit input filter and evaluated on their high frequency performance.

Chapter 4: K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, "Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3921-3936, April 2019.

In the chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared by me and was reviewed by other co-authors. Y. He helped with the prototype development and provided useful knowledge on conducting the experiments. H. S. Chung and R. T. Li provided valuable advice on different practical issues during the work. I carried on background studies, methodology analysis, system implementation, and performance evaluation.

Chapter 5: K. K. M. Siu, C. N. M. Ho, and R. T. H. Li, "A Four-Quadrant Single-Phase Grid-Connected Converter with only Two High Frequency Switches," *IEEE Trans. Ind. Electron.*, Early Access.

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared by me and was reviewed by other co-authors. C. N. M. Ho provided guidance on the work and R. T. Li provided valuable advice on it. I carried on background studies, system implementation and experimental evaluation.

Chapter 6: K. K. M. Siu and C. N. M. Ho, "Manitoba Rectifier - Bridgeless Buck-Boost PFC," *IEEE Trans. Power Electron.*, Early Access.

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was prepared by me and was reviewed by another co-author. C. N. M. Ho provided guidance and advice on the work. I carried on background studies, system implementation and experimental evaluation.

Chapter 7: C. N. M. Ho and K. K. M. Siu, "Manitoba Inverter—Single-Phase Single-Stage Buck-Boost VSI Topology," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3445-3456, April 2019.

In this chapter, the idea was developed by me and C. N. M. Ho. The manuscript was mainly prepared by C. N. M. Ho and was edited by all of the authors. C. N. M. Ho conducted on background studies, topology analysis, and characteristics deviations. I wrote a design guideline on the paper, carried on system implementation and evaluated the system performance through experimental tests.

Chapter 8: K. K. M. Siu and C. N. M. Ho, "System Model and Performance Evaluation of Single-Stage Buck-Boost Type Manitoba Inverter for PV Applications," *IEEE J. Emerg. Sel.*

***Topics Power Electron.*, submitted and under review.**

In this chapter, the idea was developed by me. The manuscript was prepared by me and was reviewed by another co-author. C. N. M. Ho provided guidance and advice on the work. I carried on background studies, system implementation and experimental evaluation.

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- K. K. M. Siu and C. N. M. Ho, "A critical review of Bridgeless PFC boost rectifiers with common-mode voltage mitigation," in *Proc. IEEE IECON*, pp. 3654-3659, Nov. 2016. Chapter 2 of this thesis contains materials from this paper.
- C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, "Active Virtual Ground—Bridgeless PFC Topology," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017. Chapter 3 of this thesis contains materials from this paper.
- K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, "Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3921-3936, April 2019. Chapter 4 of this thesis contains materials from this paper.
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Chapter 1 Introduction

1.1 Background

1.1.1 Microgrid System

In the past few years, renewable energy resources have become more popular and the growth of renewable energy is more than 14 % per year [1.1]. Different from centralized power generation, the sources of renewable energy are usually distributed in a localized area. Thus. in order to support the development of renewable energy, microgrid systems are usually adopted in the renewable energy distribution networks.

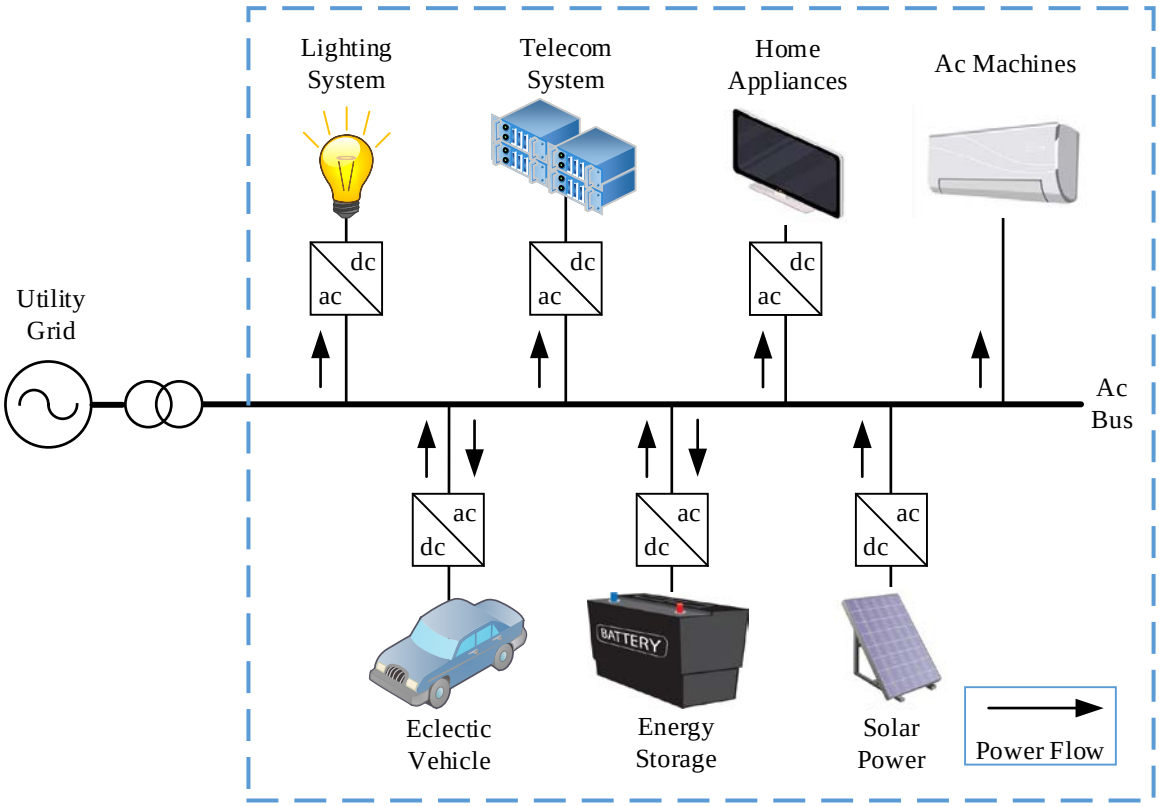


Figure 1-1. Structure of a single-phase microgrid system.

A microgrid, [1.2] - [1.6], is a localized grid network that can be synchronized to the centralized power grid as a grid-connected mode or disconnected with the utility grid to operate as an islanded mode. Based on the system conditions, the system operation can be interchanged between these two operation modes. In the grid-connected operation mode, energy is converted between the utility grid and the microgrid network. The conversion can be bidirectional which supports both real power and reactive power delivery. The islanded mode is an off-grid operation where the energy demands within the network are supported by the power generators inside the system.

A typical structure of a single-phase ac microgrid system is shown in Figure 1-1. It is capable to integrate with the utility grid system and is able to support direct connections to any traditional grid-connected devices. For a typical microgrid system, three main components are involved, which are power generator (PG), power consumer (PC) and energy storage system (ESS). Generally, the major power generation sources in a microgrid system are the various kinds of renewable energy source (RES), such as solar. Power consumers in the network include lighting systems, general equipment, electrical vehicle charging stations, etc. The ESS is used to backup energy, to maintain power quality and to supply electricity to the microgrid system, especially during the islanded mode. As shown in Figure 1-1, most of the power devices need a power interface to adopt the grid energy and to control the power flow. According to the needs of the application and the required specifications, difference kinds of converter structure will be selected, which can be ac-dc, dc-ac or bidirectional ac-dc designs.

1.1.2 Grid-connected Converter Overview

In the process of energy conversion, high switching frequency power converters are always

adopted as the interface between the microgrid system and the grid-connected appliances, such as distributed energy sources and different power consumers. The function of power converters is to transfer electrical energy from one end to the other end in an efficient and high power quality way. Depending on the application, the output voltage format can be different in amplitude or frequency from the input. In the voltage source power conversion, the applied power converters normally are classified into three different types, which are ac-dc, dc-ac and bidirectional power converters. To explain in more details:

1) Converter for energy consumption is defined as ac-dc rectifier and usually named as Power Factor Correction (PFC) Converter.
2) Converter for energy injection is defined as dc-ac inverter and usually named as Voltage Source Inverter (VSI).
3) Converter handles bidirectional power flow and reactive power demands called Voltage Source Converter (VSC).

1.1.2.1 AC-DC Power Rectifier (Power Factor Correction Converter)

Power rectifiers are used to convert the ac power from the grid into a stable dc power. It generally appears in server power supply [1.7], [1.8], lighting system [1.9], [1.10], and household equipment [1.11], [1.12], etc. A typical rectifier structure is shown in Figure 1-2 in which a diode bridge is used to rectify ac voltage into rectified sinewave and a dc-dc converter is applied to generate a stable dc voltage [1.7]. The input grid voltage is varying from zero to 326 V in high line (230 Vac) or to 170 V in low Line (120 Vac). Therefore, a simple buck-type converter is not applied in this application. A buck-boost-type converter is one of the possible options which offers

both step-up and step-down function. It is a typical topology for some low power (<300 W) applications, such as lighting system [1.9], [1.10]. However, it is hard to satisfy the requirements in power quality and in EMC at high power applications. It is because a bulky input filter is required in order to filter out the large discontinuous input current. Conventionally, in the medium to high power (>300 W) applications, such as server power supply [1.7], a boost-type converter is selected to step-up the input voltage to 380 Vdc as bus voltage. As there is a filter inductor in the input side of the boost-type converter, a smooth and continuous grid current is provided. When a lower output voltage is required, a buck converter is implemented to the system second stage and helps to step down the dc bus voltage into the desired value.

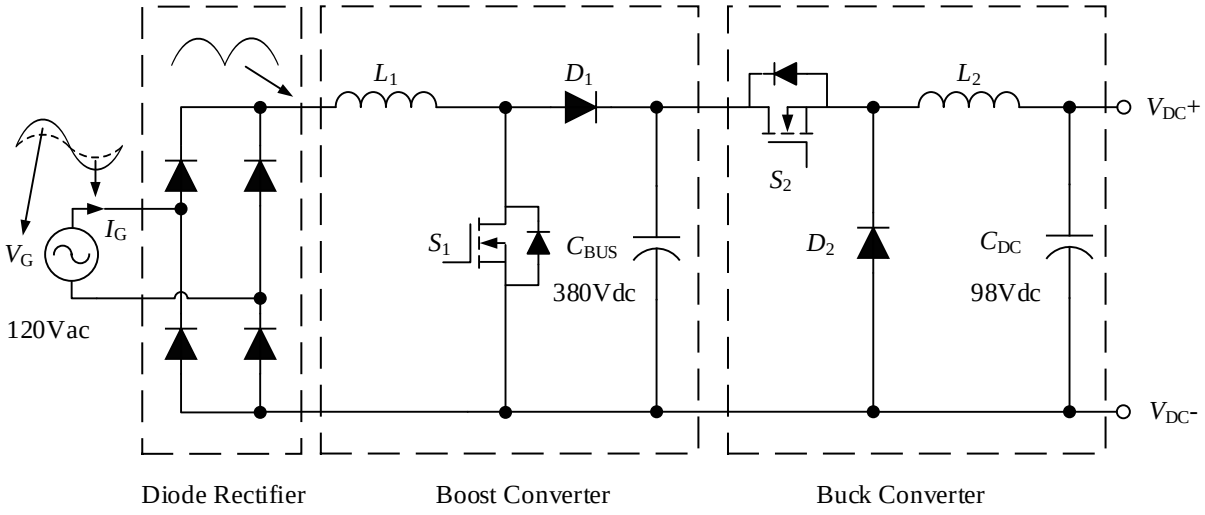


Figure 1-2. A typical topology of non-isolated ac-dc real power conversion.

1.1.2.2 DC-AC Power Inverter (Voltage Source Inverter)

Power inverters are used to convert dc power into grid ac power and to inject power to the grid. Power inverter usually appears in PV system [1.13] - [1.15], backup energy system [1.16] - [1.18], etc. A typical inverter structure is shown in Figure 1-3 [1.13]. The inverter output is

expected to be a harmonic-free sinusoidal grid current and synchronize with the connected grid voltage. Among different VSI topologies, a buck-type inverter is commonly used such as full-bridge inverter and half-bridge inverter. A smooth and continuous grid current is guaranteed by the grid-side inductor. As the inverter output voltage is always lower than the dc input voltage, an additional front stage is required in some low input voltage applications, such as 48 V fuel-cell storing system [1.16]. Generally, a boost converter is applied to convert the input voltage into a high level bus voltage (380 Vdc) and to support the inverter operation.

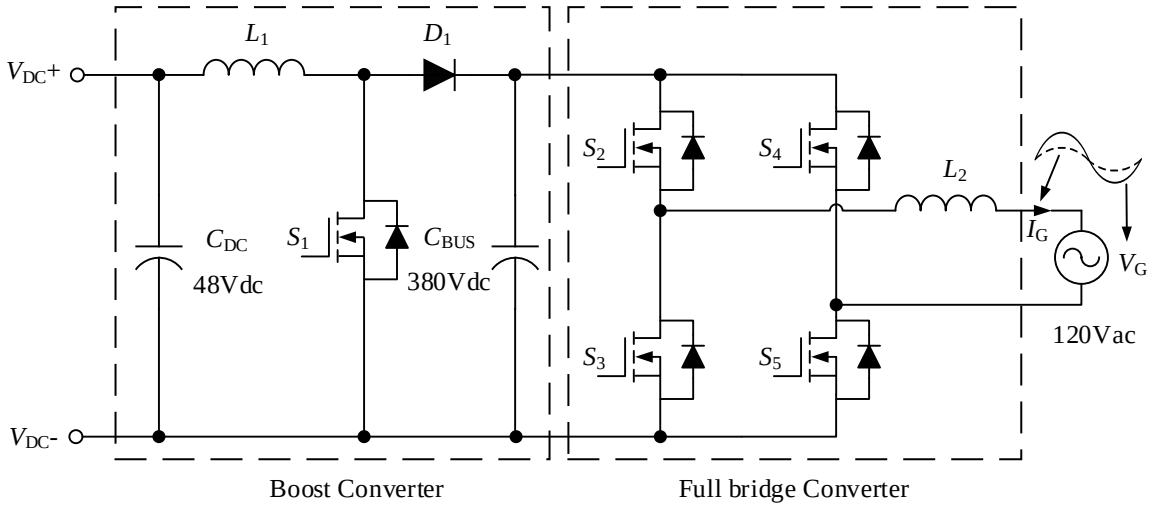


Figure 1-3. A typical topology of dc-ac power conversion with real power injection.

1.1.2.3 Bidirectional Power Converter (Voltage Source Converter)

Voltage source converters are a combination of rectifier and inverter which support the power conversion between the grid ac power and the dc power in both directions, either dc to ac or ac to dc. It is also able to support reactive power during power conversion. It mainly appears in the energy storing system [1.19] - [1.22], reactive power supporting unit [1.23] and active power filter [1.24]. A typical VSC circuit is shown in Figure 1-4 [1.19]. In general, the front stage is a boost-

type converter and a buck converter is used as the second stage of the system for low voltage dc applications. With the use of a full-bridge converter and various modulation methods, bidirectional power flow and reactive power injection are able to be provided. The VSC can operate in rectifier mode, inverter mode, and reactive power mode in either capacitive or inductive.

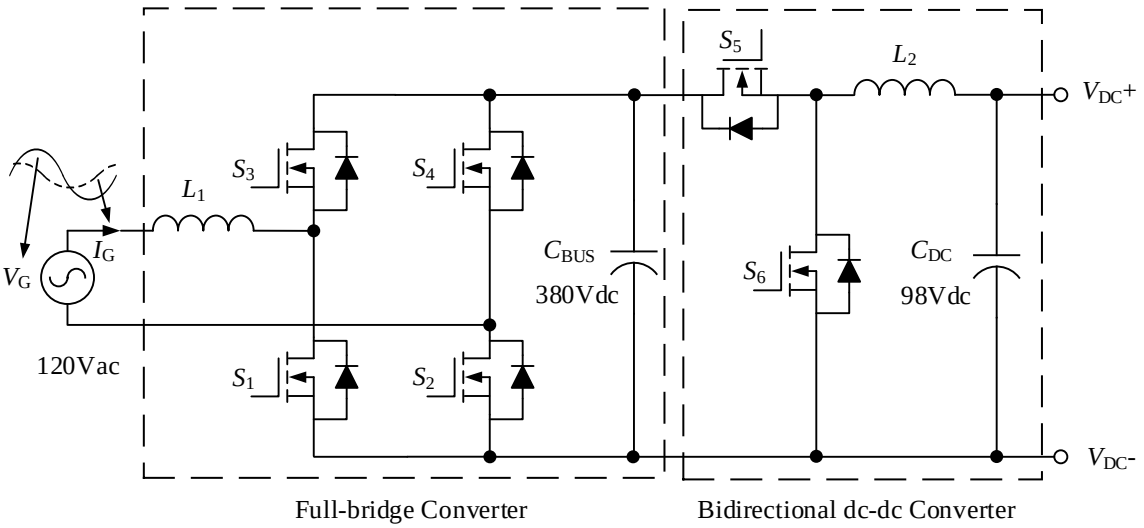


Figure 1-4. A traditional topology of ac-dc bidirectional power conversion.

1.1.3 Performance Requirement

Under the fast technological growth of the past decade, the electronics industry becomes more mature. Many fast switching devices are introduced and many new topologies are proposed. Consequently, power electronics become more popular and the demand for efficient converters are increased a lot. In different applications, the performance requirements of the converters are also different. In each application, the performance of required converters is also standardized and a list of international standards is needed to follow.

To claim as a high performance converter, the following requirements should be achieved:

- High Efficiency
- High Power Quality
- Low Leakage Current
- Low Noise Current

A summary table is given in TABLE 1-I.

TABLE 1-I SUMMARY OF INDUSTRY STANDARDS IN THE DESIGN OF DIFFERENT TYPES OF CONVERTERS

Requirement of Converter Performance	Power Rectifier	Power Inverter	Reactive Power Voltage Source Converter
Efficiency	> 87 % for standard model. (Energy Star)	Both static and dynamic efficiencies are required in PV system. (European & CEC efficiency)	
Power Factor	> 0.9. (Energy Star standard & IEC/EN61000-3-2)		= 0.95 for PV system. (VDE-AR-N4105)
Total Harmonic distortion	Voltage THD < 5 % & current TDD < 5 %. (IEEE 519)		
Leakage Current	< 3.5 mA for information technology equipment & class I motor appliance. (IEC 60950 and IEC 60335)	<300 mA for PV system. (IEC 62109 and VDE 0216-1-1)	

1.1.3.1 Efficiency Requirement

Efficiency is always the most important index to identify the performance of a converter that is highly correlated with energy costs. Converter efficiency, η, is defined as the converter output power, P_{OUT}, over the total input power, P_{IN}. The general formula is defined as,

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}}. \tag{1.1}$$

In general, the major energy loss in power conversion appears in the converter inductors and the semiconductors of the converter. Therefore, these component selections become very critical. In addition, an efficient converter topology is also required, such as those bridgeless converter designs. To be a qualified product, some international standards have to be fulfilled. Every application also has the corresponding minimum efficiency criteria. Energy Star [1.25] is one of the standards which set out an efficiency specification for ac-dc power supplies. In photovoltaic systems, one more efficiency measurement is concerned which is maximum power point tracking (MPPT) efficiency. It is used to describe the power transmission efficiency of a solar energy source. There are two different types of tracking efficiency are involved, which are static and dynamic MPPT efficiencies. According to [1.26], the formula of the static MPPT efficiency, η_{static}, and dynamic MPPT efficiency, η_{dynamic}, are defined as,

$$\eta_{\mathrm{static}} = \frac{I_{\mathrm{PV}} \cdot V_{\mathrm{PV}}}{P_{\mathrm{peak}}}, \tag{1.2}$$

$$\eta_{\mathrm{dynamic}} = \frac{\int_0^{T_{\mathrm{S}}} i_{\mathrm{PV}}(t) \cdot v_{\mathrm{PV}}(t) dt}{\int_0^{T_{\mathrm{S}}} p_{\mathrm{peak}}(t) dt}, \tag{1.3}$$

where I_{PV} and V_{PV} and P_{peak} are PV current, PV voltage and maximum available power from PV panels under a fixed irradiation situation, respectively. T_{S} is a dynamic period defined in [1.26]. i_{PV}, v_{PV} and p_{peak} are PV current, PV voltage and are maximum available power from PV panels during dynamic period, respectively.

1.1.3.2 Power Quality Requirement

Power quality is another index to identify the performance of a converter that is related to

system stability and the efficiency of energy transmission. There are two main indicators which are total harmonic distortion level and power factor. Total harmonic distortion (THD) is defined as the sum of the magnitude in each harmonic currents or voltages over the magnitude of the fundamental unit. Ideally, the power factor is one and the THD is zero in magnitude. However, in general applications, a non-linear load is applied and high frequency (HF) harmonics are generated. In a high harmonic system, serval drawbacks are generated, such as it will influence the interconnected equipment, increase transformer losses, generate skin effect on power cable under HF harmonic contents, etc. Focusing on harmonic issues, some international standards have created. IEEE 519 [1.27] is one of them that is applied to the electric power system. The order of the harmonic content is counted up to 50^{th}. The formula of THD is defined as,

$$THD = \frac{\sqrt{\sum_{n=2}^{50} I_n^2}}{I_1}, \tag{1.4}$$

I_1 is current magnitude at the fundamental frequency and I_n is current magnitude at the n^{th} harmonic.

For a general single-phase grid-connected system, the voltage THD is limited to 5 %. The current THD is also limited to 5 % and each individual harmonic current can't exceed a certain percentage of the fundamental current. This is so it can help to maintain the system quality and stability.

The power factor, *PF*, of an ac power transmission is defined as the ratio of real power consumption, *P*, over the apparent power consumption, *S*, in the system. When a switching converter unit is involved in power transmission, the total harmonic distortion is also needed to be included in the resultant power factor. It is because a non-linear load is adopted. Refer to [1.28], the resultant formula is,

$$PF = \frac{P}{S} = \frac{\cos\theta_1}{\sqrt{1-THD^2}}. \quad (1.5)$$

where θ_1 is apparent power phase angle at fundamental frequency.

Both power quality and power capability of the system will be restricted by a low power factor. Moreover, a large current magnitude will be induced which increases the loss in the grid power transmission, leads to poor voltage regulation and affects the actual power capability of the overall system. High power factor system can be easily achieved by adopting a PFC circuit at the ac input of power equipment. In general household equipment and power supply systems, all the products are required to follow the Energy Star standard [1.25] or IEC/EN61000-3-2 [1.29]. In the Energy Star standard, all the power supplies higher than 100 W are also required to have a power factor of 0.9 or above at 100 % loading. A similar condition is mentioned in the IEC/EN61000-3-2 standard. In the standard, consumer equipment is separated into four classes based on equipment usage and power level. Each of them has different limitations and requirements. For PV inverter, a power factor of 0.95 is required to compensate for the reactive power in the utility grid which describes in the VDE-AR-N4105 [1.30].

1.1.3.3 Leakage Current Requirement

Leakage current also called touch current, is defined as the unwanted electric current which flows from hazardous voltages part of the equipment to the accessible part such as the equipment chassis or protective earth connection point. It is highly related to human safety. In general, between each high voltage HF switching point and the earth connection point, there is an induced parasitic capacitor in the system which results in a possible current path for leakage current. If the equipment is not well protected, once the human body touches the leakage area, current may flow

through the contacting point of the human body back to the earth and cause electric damage. Therefore, different applications also have their strict requirements of leakage current limitations. In some telecom equipment and class I motor appliance, the maximum available leakage current is 3.5 mA, as shown in the standards of IEC 60950 [1.31] and IEC 60335 [1.32] respectively. In photovoltaic inverters, the maximum available leakage current is 300 mA, as shown in the standards of IEC 62109 [1.33] and VDE 0216-1-1 [1.34].

1.1.3.4 Noise Current Requirement

Noise current level is not specifically defined in the design requirements of the converter. However, if the noise level is sufficiently large in magnitude, a bulky electromagnetic interference (EMI) filter is required at the system input in order to satisfy the international electromagnetic compatibility (EMC) requirement [1.35], [1.36]. The bulky EMI filter results in a reduction in system efficiency and an increment in the system power density. Thus, a low noise system is always preferred. In describing the EMI performance of the system, there are two different types of noise that will be considered. One is Common Mode (CM) noise which induces from the noise coupling from the system parasitic capacitors. Here, the leakage current path is formed between those switching points and Earth connection point as mentioned in the above section. The other is called Differential Mode (DM) noise which can be projected from ac grid current. The high amplitude of the grid current ripple will result in a high level of noise in its fundamental operation frequency and its sub-harmonic frequency at the corresponding EMI spectrum.

1.1.4 Transformer and Transformerless Design

In some sensitive applications, such as telecommunication systems and high voltage electric vehicle chargers, [1.37], [1.38], isolation transformers are applied in the power converter designs to provide galvanic isolation and to limit the leakage issue. Generally, the transformer helps to separate the system into the primary and secondary sides which avoids the potential electrical shock from the primary side to the secondary side. However, the bulky transformer limits the power density of the system. In some applications, if the whole system is enclosed and no physically contacting point on top, the isolation transformer can be neglected as a transformerless design. Solar inverter system is one of them [1.15], [1.39]. Without the bulky transformer, the overall system power density can be increased. Also, the system design can be more efficient and inexpensive. Although galvanic isolation is not applied, the leakage current is still needed to be maintained at a certain level in order to avoid any hazardous situations. To deal with system leakage current, a list of topologies and solutions have been developed in the past, such as H5 [1.40] and Heric [1.41] inverters.

1.1.5 Grid-side Filter Selection

Generally, a filter is placed between the grid terminal and a grid-connected power converter so as to maintain the grid current quality by attenuating the HF components generated from the converter. *L*, *LC* and *LCL* filters are three commonly used filter structures [1.42]. All of them are performed as a low pass filter.

Among three of them, *L* filter is commonly used which is with a first-order filter structure. *L* filter is simple in structure, easy of design and no resonance issue. However, in order to meet the

noise attenuation requirement, a large and bulky inductor is required. Also, the dynamic performance of the system will be slowed down due to the high grid impedance. Therefore, a high order filter is generally required and more popular in a noisy system. *LC* filter is a second-order filter and *LCL* filter is a third-order filter. Compared to the first-order filter, they have higher attenuation in HF current and are able to further optimize in size and volume. Depending on the network impedance, the selection of filters is different. For both *LC* and *LCL* filters, selections of filter components are based on a desired cut off frequency which uses to attenuate the unwanted high order noises and to remain the fundamental frequency component in grid current. The drawback is that it may result in a resonance characteristic in the converter. To stabilize the system, passive damping, active damping or boundary control is also one of the possible solutions on it [1.43] - [1.47]. Passive damping is implemented by cascading a resistor on a capacitor to damp the resonance issue that appears in the circuit. Active damping uses a control method to minimize the resonance magnitude that appears inside the converter controller. Boundary control method is able to eliminate the filter resonance in the converter transfer characteristic by simplifying the system order with the use of the boundary law.

1.1.6 High Frequency Virtually Grounded Design

Active Virtual Ground (AVG) is one of the high frequency virtually grounded techniques that can migrate the CM voltage form a grid-connected converter [1.48]. A simplified boost-stage equivalent circuit, as shown in Figure 1-5, is used to explain the operational principle of the high frequency virtually grounded technique. In the figure, a capacitor C_{CM} is used to represent the circuit parasitic capacitor and to indicate the leakage path. The working principle of the virtually grounded technique is to use a filter capacitor to link up the converter dc bus terminal and grid

terminal together. In principle, the Neutral (ac ground) and the negative bus terminal (dc ground) are not connected with each other. However, in HF point of view, the impedance of a capacitor is at a relatively low value. Thus, the potential difference between two terminals becomes nearly zero and both terminals look like virtually connecting with each other in the HF operation. Consequently, both of the voltage ripple in the parasitic capacitor and the induced leakage current of the converter are able to be maintained in a small value. Meanwhile, as a low-pass filter is formed at the grid-side, the grid current ripple is limited to a relatively small value. According to high frequency virtually grounded techniques, a series of topology is generated based on this concept.

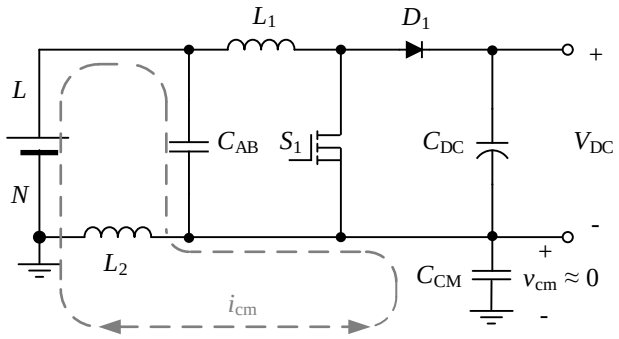


Figure 1-5. Example of high frequency virtually grounded.

1.2 Research Objectives

In a microgrid network, high-performance power interfaces are always required which are used to support the efficient power conversion of different grid-connected power supply units. Based on the requirements of different specific applications, a series of new converter topology is proposed in this thesis which is based on the high frequency virtually grounded technique. Those converters are supported with the theoretical model, mathematics calculations and experimental

verifications. The major work on this thesis are listed in the following:

- Identification of the different application criteria on the different types of microgrid connected appliance.
- Utilization of the high frequency virtually grounded concept to generate a new series of topologies with high efficiency and low leakage current.
- Determination of the detailed characteristics and the principle of operation of different converter topologies with the use of high frequency virtually grounded technique.
- Formulation of a suitable design guideline for different designs in different applications, such as the selection of filter components and the possible combinations of semiconductors.
- Design and implementation of a stabilized control scheme to coordinate with the high frequency virtually grounded technique and to maximize the converter performance of new proposed topologies.

1.3 Research Contributions

The outcomes from this research work can help the development of the microgrid network, where a new series of topologies is introduced. The new design can cover a wide range of applications. All designs feature a single-stage transformerless topology, which helps the system maintain continuous grid current and low leakage current system characteristics. The developed converters efficiently and effective interface different types of power sources including ac grid, dc grid, dc generator, dc bus for a wide range of applications in Microgrid. They also offer more options in the existing power interface selection.

According to the structure of the microgrid, the developed topologies can be divided into three categories, which is power rectifier, power inverter, and bi-directional power converter. Focusing on power consumers, two different types of rectifier topologies are introduced. One is a boost-stage rectifier design, which targets for the power appliances with the needs of high dc bus voltages. Another one is a buck-boost-stage rectifier design, which targets for the transformerless low voltage dc power appliances. Focusing on renewable energy sources, a buck-boost type VSI topology is introduced, which covers a wide range of voltage input and effectively injects the renewable energy to the microgrid system. Lastly, focusing on energy storage systems, a full-bridge type VSC topology is introduced, which supports the bidirectional power flow between two voltage sources.

To demonstrate the applicability of the design topology, two different specify application scenarios have been applied. One is the PFC circuit control in a boost type rectifier design, which shows how to achieve both stable system performance and fast dynamic response in transient action. Another one is the PV inverter control in a buck-boost type VSI design, which shows how to achieve both stable system performance and maximum power point tracking of PV output.

In the application demonstrations, two different types of control methodologies are applied. They are non-linear control and linear control. The difference in implementations are demonstrated and the corresponding advantages are evaluated. In the applied non-linear control, such as boundary method, it can reduce the system order and eliminate the filter resonance from the system. Therefore, stable system performance and high system control bandwidth can be obtained in the designed topology. In the applied non-linear control, such as active damping plus PI control method, it can also result in stable system performance and minimize the filter resonance from the

system. It comes with the advantages of lower sampling point requirements and less dependence on system parameters. In different applications, different control methods are recommended.

1.4 Thesis Structure

This thesis is in a journal-paper-basic thesis where the core of this thesis is comprised of six journal papers. Five of them have been published and one is under review. A total of nine chapters are presented in this thesis.

In Chapter 1, a brief introduction is given which covers the description of a microgrid system and the design requirements of various kinds of grid-connected converters. The key concept of this thesis, high frequency virtually grounded technique, is discussed. In addition, the research objective and the scope of this thesis is presented.

In Chapter 2, based on bridgeless PFC (BPFC) topologies, the CM issue is investigated and different kinds of CM voltage mitigation techniques have been evaluated. Accordingly, a topology classification method is presented. Through the HF models, the noise characteristics of the reviewed topologies are analyzed and the performance of different types of converters are compared in detail.

In Chapter 3, a new bridgeless boost-type Power Factor Correction topology is introduced which is in a bridgeless PFC circuit structure and consists of the high frequency virtually grounded technique. Both of the topology operational principles and system characteristics are determined. A detailed design guideline is offered.

In Chapter 4, the work in Chapter 3 is extended. An advanced digital control methodology is developed which is targeted on the topology that described in the last chapter. The details of the

control law and the operation principle of the integrated state machine are described. The techniques in the digital implementation are shared and corresponding system modelling are derived.

In Chapter 5, focusing on the needs of the application, a four-quadrant boost-type bridgeless PFC topology is built which is also with the high frequency virtually grounded technique. To minimize the number of HF switches, a new modulation scheme is determined. Each operation mode is addressed in detail.

In Chapter 6, a new buck-boost-type bridgeless PFC topology is proposed which is with the high frequency virtually grounded technique. The single-stage buck-boost rectifier structure and system characteristics are deeply explained. The selection criteria of the critical components are also listed.

In Chapter 7, a new buck-boost-type inverter topology is presented which is the inverter version of the topology that described in the previous chapter. Different from the last chapter, the topology structure is distinct. A new modulation method is used and a different control scheme is applied.

In Chapter 8, focusing on PV applications, a comprehensive control scheme is shown to apply to the topology presented in the last chapter. A method of integrating the maximum power point tracking (MPPT) function into the control system is presented. The system bandwidth and the stability range of the design are evaluated in this chapter. The tradeoff in the MPPT performance is described and evaluated through experiments.

In the last chapter (Chapter 9), according to the work presented in this thesis, conclusions are given and recommendations for future work are listed.

Reference

[1.1] "Statistical Review of World Energy 2017," *from BP p.l.c*, Jun. 2017.

[1.2] Y. Yang, Q. Jia, G. Deconinck, X. Guan, Z. Qiu, and Z. Hu, "Distributed Coordination of EV Charging with Renewable Energy in a Microgrid of Buildings," *IEEE Trans. Smart Grid*, vol. 9, iss. 6, pp. 6243-6264, May 2018.

[1.3] R. Atia and N. Yamada, "Sizing and Analysis of Renewable Energy and Battery Systems in Residential Microgrids" *IEEE Trans. Smart Grid*, vol. 7, No. 3, pp. 1204-1213, May 2016.

[1.4] Y. Zhou and C.N.M. Ho, "A review on Microgrid architectures and control methods," *in Proc. of IPEMC-ECCE Asia*, pp. 3149-3156, May 2016.

[1.5] Z. Zhaoyun *et al*., "Application of micro-grid control system in smart park," *Journal of Engineering*, vol. 2019, no. 16, pp. 3116-3119, Mar. 2019.

[1.6] X. Guan, Z. Xu and Q. Jia, "Energy-Efficient Buildings Facilitated by Microgrid," *IEEE Trans. Smart Grid*, vol. 1, no. 3, pp. 243-252, Dec. 2010.

[1.7] L. Huber, Y. Jang, and Milan M, "Performance Evaluation of Bridgeless PFC Boost Rectifiers," *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381-1390, May 2008.

[1.8] F. C. Lee, Q. Li, Z. Liu, Y. Yang, C. Fei and M. Mu, "Application of GaN devices for 1 kW server power supply with integrated magnetics," *CPSS Tran. Power Electron. and Appl.*, vol. 1, no. 1, pp. 3-12, Dec. 2016.

[1.9] P. Fang, and Y. Liu, “Energy Channeling LED Driver Technology to Achieve Flicker-Free Operation With True Single Stage Power Factor Correction,” *IEEE Trans. Power Electron.*, vol.32, no.5, pp. 3892-3907, May 2015.

[1.10] S. T. S. Lee, H. S. H. Chung, and S. Y. R. Hui, “A novel electrode power profiler for dimmable ballasts using DC link voltage and switching frequency controls,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 847-853, May 2004.

[1.11] V. Bist and B. Singh, “An Adjustable-Speed PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2665-2677, Dec. 2013.

[1.12] E. Jang, S. M. Park, D. Joo, H. M. Ahn, and B. K. Lee, “Feasibility Study on All Metal Induction Cooker Systems Considering Topology and Control,” *in Proc. IEEE ECCE*, pp. 936-941, Sept. 2018.

[1.13] C. N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. A. Serpa, and A. Coccia, “Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2835-2845, June 2012.

[1.14] C. N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, and F. Canales, “A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 289-299, Jan. 2013.

[1.15] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292-1306, Oct. 2005.

[1.16] K. R. Sree, A.K. Rathore, E. Breaz, and F. Gao, “Soft-Switching Non-Isolated Current-Fed Inverter for PV/Fuel Cell Applications,” *IEEE Trans. Ind. Appl.*, vol. 52, no. 1, Jan. 2016.

[1.17] M. Jang, M. Ciobotaru, and V. G. Agelidis, “A Single-Stage Fuel Cell Energy System Based on a Buck--Boost Inverter with a Backup Energy Storage Unit,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2825-2834, June 2012.

[1.18] J. Kan, S. Xie, Y. Wu, Y. Tang, Z. Yao, and R. Chen, “Single-Stage and Boost-Voltage Grid-Connected Inverter for Fuel-Cell Generation System,” *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5480-5490, Sept. 2015.

[1.19] Y. Ma, T.Houghton, A. Cruden, and D. Infield, “Modeling the Benefits of Vehicle-to-Grid Technology to a Power System,” *IEEE Trans. Power Syst.*, vol.27, iss. 2, pp. 1012-1020, Jan. 2012.

[1.20] M. C. Kisacikoglu, M. Kesler, and L. M. Tolbert, “Single-Phase On-Board Bidirectional PEV Charger for V2G Reactive Power Operation,” *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 767-775, Mar. 2015.

[1.21] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, “EV/PHEV Bidirectional Charger Assessment for V2G Reactive Power Operation,” *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5717-5727, Dec. 2013.

[1.22] Y. S. Kim, G. C. Parkm, J. H. Ahn, and B. K. Lee, “Hybrid PFC-Inverter Topology for Bidirectional On Board Charger for Range Extended Electric Vehicle,” *in Proc. of ICEMS*, pp. 521-524, Oct. 2015.

[1.23] S.M.R. Islam, S. Maxwell, M.K. Hossain, S.Y. Park, and S. Park, "Reactive Power Distribution Strategy using Power Factor Correction Converters for Smart Home Application," in *Proc. of IEEE ECCE*, pp. 1-6, Sept. 2016.

[1.24] A. Javadi, A. Hamadi, L. Woodward, and K. Al-Haddad, "Experimental Investigation on a Hybrid Series Active Power Compensator to Improve Power Quality of Typical Households," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4849- 4859, Aug. 2016.

[1.25] "Technical Specifications for Single voltage external ac-ac and ac-dc power supplies specification," *from Energy Star*, ver.2, Nov. 2008.

[1.26] *Overall efficiency of grid-connected photovoltaic inverters*, European standard EN 50530:2010, 2010.

[1.27] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE 519-2014, 2014.

[1.28] D. Li, C. N. M. Ho, L. Liu, and G. Escobar, "Reactive Power Control for Single-Phase Grid-Tie Inverters Using Quasi-Sinusoidal Waveform," *IEEE Trans. Sustainable Energy*, vol. 9, no. 1, pp. 3-11, Jan. 2018.

[1.29] *Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤16 A per phase)*, IEC Standard 61000-3-2-2001, 2001.

[1.30] *Power generation system connected to the low-voltage distribution network*, VDE Standard VDE-AR-N 4105, 2011.

[1.31] *Information technology equipment – Safety - Part 1: General requirements*, IEC Standard 60950-1, 2005

[1.32] *Household and similar electrical appliances - Safety - Part 1: General requirements*, IEC Standard 60335-1:2010, 2010.

[1.33] *Safety of Power Converters for Use in Photovoltaic Power Systems—Part 1: General Requirement*, IEC Standard 62109-1-2007, 2007.

[1.34] *Automatic disconnection device between a generator and the public low-voltage grid*, DIN-VDE Std. 0126-1-1, 2005.

[1.35] *Electromagnetic compatibility - Requirements for household appliances, electric tools and similar apparatus - Part 1: Emission*, IEC Standard IEC CISPR 14-1:2016, 2016.

[1.36] *Electromagnetic compatibility of multimedia equipment - Emission requirements*, IEC Standard IEC CISPR 32:2015, 2015.

[1.37] C. Li and D. Xu, "Family of Enhanced ZCS Single-Stage Single-Phase Isolated AC–DC Converter for High-Power High-Voltage DC Supply," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3629-3639, May 2017.

[1.38] B. Singh, S. Singh, A. Chandra and K. Al-Haddad, "Comprehensive Study of Single-Phase AC-DC Power Factor Corrected Converters With High-Frequency Isolation," *IEEE Trans. Ind. Informat.*, vol. 7, no. 4, pp. 540-556, Nov. 2011.

[1.39] T. K. S. Freddy, N. A. Rahim, W.P. Hew, and H. S. Che, "Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters," *IEEE Trans. Power Electron.*, vol. 29, no.10, pp.5358 – 5369, Oct. 2014.

[1.40] M. Victor el at, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage," *US Patent*, No. US7411802 B2, 12/08/2008.

[1.41] H. Schmidt *el at*, "DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current," *US Patent*, No. US7046534 B2, 16/05/2006.

[1.42] H. Cha and T. Vu, "Comparative Analysis of Low-pass Output Filter for Single-phase Grid-connected Photovoltaic Inverter," in *Proc. IEEE APEC*, pp. 1659 – 1665, Feb. 2010.

[1.43] J. Dannehl, C. Wessels, and F.W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers with LCL Filters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380-388, Nov. 2008.

[1.44] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," in *Proc. IEEE APEC*, vol. 33, no. 2, pp. 542–550, Mar. 1996.

[1.45] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Genetic Algorithm-Based Design of the Active Damping for an LCL-Filter Three-Phase Active Rectifier," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 76-86, Jan. 2004.

[1.46] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-Step Controller Design for LCL-Type Grid-Connected Inverter with Capacitor–Current-Feedback Active-Damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239-1253, Mar. 2014.

[1.47] Y. He, H. S. H. Chung, C. N. M. Ho, and W. Wu, "Use of Boundary Control With Second-Order Switching Surface to Reduce the system Order for Deadbeat Controller in Grid-Connected Inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2638-2653, Jun. 2015.

[1.48] N. M. Ho and T. H. Li, "Bridgeless power factor correction circuit," *US Patent*, No. US9093917 B2, 07/28/2015.

Chapter 2 Comparative Analysis of BPFC Topologies with Common-mode Voltage Mitigation Techniques

Part of the work described in this chapter was published in the following paper: K. K. M. Siu and C. N. M. Ho, “A critical review of Bridgeless PFC boost rectifiers with common-mode voltage mitigation,” in *Proc. IEEE IECON*, pp. 3654-3659, Nov. 2016.

2.1 Introduction

Under the fast technological growth in the past decade, the demands of power electronic converters are greatly increased. In the design of those grid-connected converters, the requirements for efficiency and power density are getting higher and higher. Thus, faster power semiconductor devices are needed, higher operating frequency of the converters are forced to have and more effective converter designs are resultant. However, the noise level generated from the converter is also increased. Thus, the common-mode noise problem becomes one of the key concerns in the design and noise migration techniques are needed.

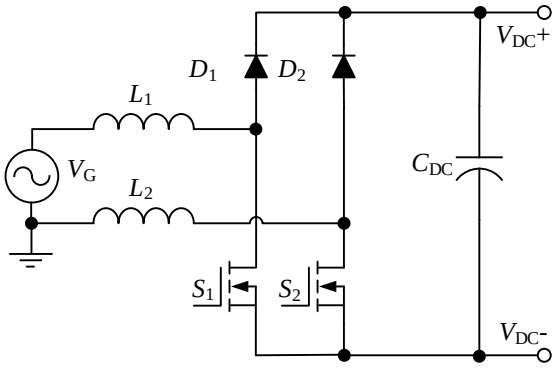
Among of grid-connected power apparatuses, a PFC converter is usually applied to the front power stage to support the power conversion between the ac and dc system, such as motor drives, Electric Vehicle chargers, and telecom power supplies. BPFC is one of them which was introduced in [2.1]. It can improve system efficiency by saving conduction loss of semiconductors. However, a higher CM noise is generated from the BPFC topology structure and high leakage current is resultant. In order to fulfill the international standard on system noise levels, such as CISPR 11 [2.2] for EV and CISPR 32 [2.3] for telecom power application, a bulky and expensive EMI filter is required. Therefore, the use of BPFC is strongly restricted. In the past twenty years, varied

solutions are presented on CM noise migration. Such as, converter designs with snubber circuit to control both switching speed of semiconductor and voltage overshoot level [2.4]; uses soft-switching control method to achieve ZVS or ZCS and to minimize the noise generated from switching devices [2.5], [2.6]; applies with different CM voltage mitigation topologies to optimize the system performance under high frequency (HF) operation [2.7] - [2.22].

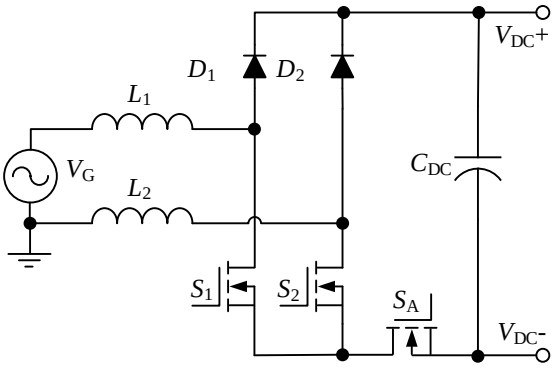
In this chapter, different kinds of CM voltage mitigation BPFC topologies are studied and evaluated in depth. Based on the CM voltage mitigation strategy, a topology classification of BPFC topologies is introduced. Under the BPFC family, four different groups are generated which is electrical isolation, semiconductor clamped, passive component clamped and hybrid clamped. The HF equivalent circuits of each group are presented and the corresponding noise magnitude equations are calculated. The overall performances of different topologies are compared in terms of CM noise voltage magnitude and grid current quality. A 750 W BPFC prototype has been used as a benchmarking platform. The theoretical analysis results are proofed and matched with the experimental findings.

2.2 Review of BPFC technologies with CM Noise Mitigation

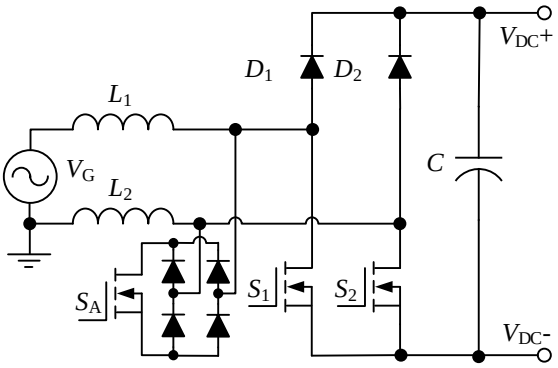
The family of bridgeless PFC is considered which is used as an interface between a single-phase ac grid and a dc bus. To overcome the critical drawback of conventional bridgeless PFC, various solutions have been proposed to mitigate CM noise. Details of prior-art topologies are shown in Figure 2-1 and discussed in this section. Based on the topologies performance, all of the discussed topologies are classified into four different groups. The corresponding family tree of BPFC topologies with CM voltage mitigation is shown in Figure 2-2.



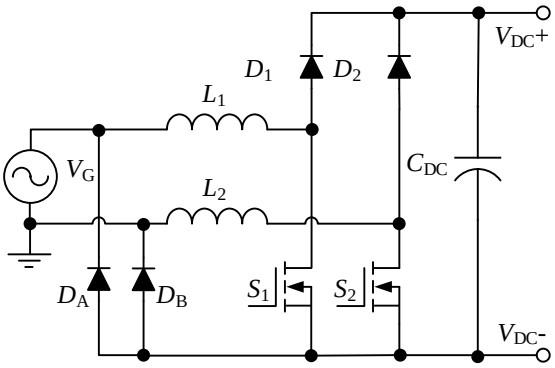
(a) Case 1 [2.1]



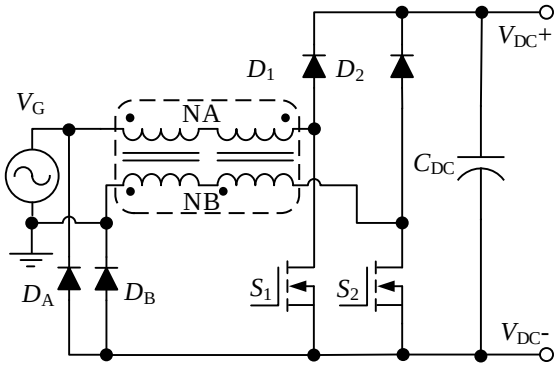
(b) Case 2 [2.7]



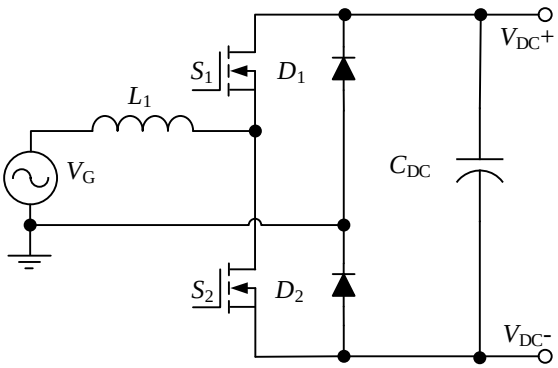
(c) Case 3 [2.8]



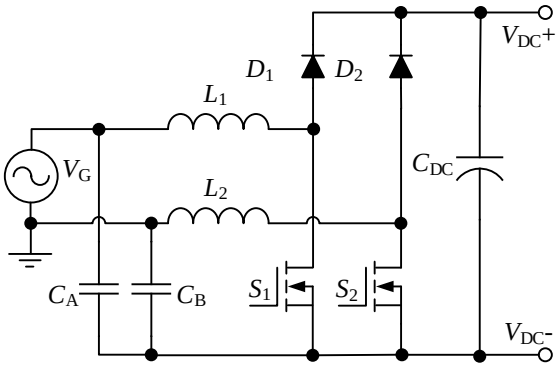
(d) Case 4 [2.10]



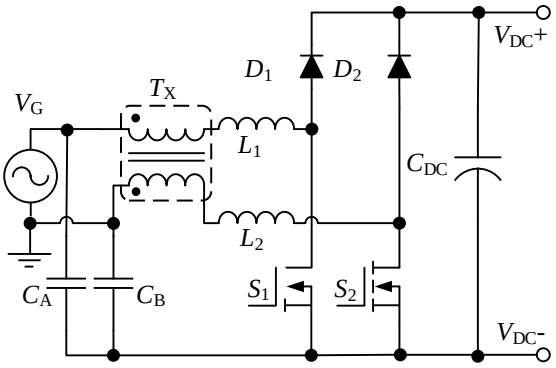
(e) Case 5 [2.15]



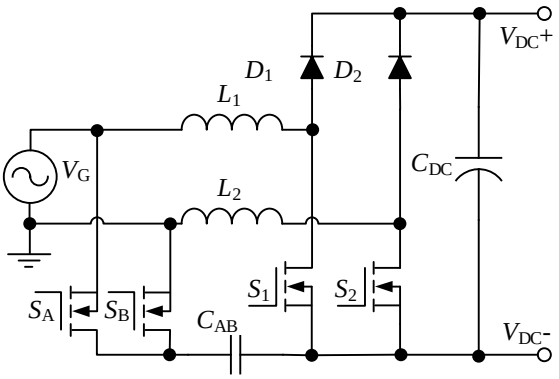
(f) Case 6 [2.16]



(g) Case 7 [2.18]



(h) Case 8 [2.20]



(i) Case 9 [2.22]

Figure 2-1. Family of Bridgeless PFC topologies.

Case 1: Conventional BPFC

The conventional PFC, as shown in Figure 1-2, is in a simple in structure and low cost design since only one active switch is in the circuit. The main drawback is high conduction loss, as there are three semiconductors conducting in each switching cycle. In order to solve the conduction loss issue of conventional PFC, BPFC was proposed in 1983 [2.1] as Figure 2-1(a). It integrates a diode bridge and a boost converter into one power stage. The circuit gives low conduction loss by reduced one semiconductor in the current path. However, more HF semiconductors are required. Moreover, there is a grounding issue because a large CM noise is generated from BPFC comparing

to the conventional PFC. In the conventional PFC converter design, the ground is directly connecting to the grid through the diode bridge to form a low impedance path for current return. In BPFC, the converter inductor is located between the grid and the ground point. Thus, it induces a HF and high voltage noise coupling to the earth. For DM filter requirement is keeping similar to the conventional PFC.

Case 2: BPFC with a series-switch

To fulfill low leakage current requirements and to satisfy the industry standards, serval solutions have been proposed in the past to tackle the leakage current issue in the BPFC. Figure 2-1 (b) shows one of them, a BPFC integrated with a cascaded series semiconductor switch which was proposed in 2013 [2.7]. It is grouped into the division of electrical isolation. The series-switch is synchronized with the main switch for current shaping. Thus, grid terminals are electrically isolated during inductor current charging states and result in a low leakage current to ground. An extra conduction loss is generated, as one more high power semiconductor is conducted in inductor current discharging states. A HF DM noise filter is still required and more floating gate drivers are required which increase the design cost and complexity.

Case 3: BPFC with a zero active branch

Another electrical isolation topology to get rid of the CM voltage issue is to use a bidirectional switch to charge up the converter input inductor which was proposed in 1992 [2.8], as shown in Figure 2-1 (c), and the detailed EMI analysis is presented in [2.9]. It has a similar performance as Case 2. Similarly, the conduction loss of Case 3 is also higher than the loss in conventional BPFC, as three semiconductors are conducted in the inductor charging state. A high power rating and HF semiconductor switch, a diode bridge and a floating gate driver are required which also rise the design cost.

Case 4: Diode-clamped BPFC

Diode-clamped BPFC was proposed in 1999 [2.10] as shown in Figure 2-1 (d). Similar topologies appeared in [2.11], [2.12]. It provides a simple and efficient solution for tackling CM issue. Two line frequency (LF) diodes are added to guarantee almost no CM voltage generated between the ground terminal and the ac source. However, the inductors work alternatively in each half line cycle. Compared to Case 1, in Case 4 a larger DM filter is required. An active switch clamped BPFC was proposed in 2013 [2.13] A similar topology is also found in [2.14]. By using switches instead of diodes, better conduction loss in the current return paths can be expected.

Case 5: Diode-clamped BPFC with common core inductor

In order to solve the problem of expensive magnetic devices in Case 4, a BPFC topology with integrating common-core inductors was introduced in 2007 [2.15] as Figure 2-1 (e). By using this topology, it can increase the utilization of components and power density can be increased due to the integration of magnetic parts. However, the designs of inductors are challenging. The overall performance in EMI is expected to be the same as Case 4 due to the similar structure.

Case 6: Totem-pole BPFC

A totem-pole BPFC was proposed in 1995 [2.16] as shown in Figure 2-1 (f). Comparing to conventional BPFC, the position of switch S_2 and D_1 are switched. Therefore, there is only one MOSFET and one diode which are conducting in each switching cycle. All the time, a LF diode always helps to clamp the CM voltage which is presented between the grid terminal and the negative bus terminal. The diode free-wheeling paths are also located in the HF switches. Therefore, in hard-switching conditions, extra losses will be generated in the main switch during the reserve recovery process. For using MOSFET as the main switches, the topology is only

suitable to operate in discontinuous mode or critical mode. In order to overcome it, the latest semiconductor device – gallium nitride (GaN) HEMT is more suitable. A floating gate driver and a HF DM noise filter are required which similar to Case 1. Pseudo totem-pole BPFC is one of the variations of totem-pole BPFC by using two fast recovery diodes to eliminate the MOSFET body diode stress [2.17]. However, it will behave like diode-clamped BPFC, one of the inductors is losing function in each switching cycle. Therefore, it is not popular in practical applications.

Case7: Capacitor-clamped BPFC

Instead of diodes, capacitors can be used to clamp the HF CM voltage which has been proposed in 2007 [2.18]. Topology in [2.19] is also in the same group. As shown in Figure 2-1 (g), two capacitors are connected between grid terminals and negative Bus voltage separately. By the use of the low impedance characteristic of capacitors at HF region, It ensures low leakage current generating from the system. The cost of capacitor-clamped BPFC is relatively lower than diode-clamped BPFC, as passive components are used. In this case, the grid current ripple is kept the same as the conventional BPFC however the inductor current ripple is double on it. Similar to Case 1, a similar size of DM filter is still required.

Case 8: Capacitor-clamped BPFC with coupling inductor

A built-in coupling inductor was proposed in 2011 [2.20] which is another passive component clamped topology. As shown in Figure 2-1 (h), a coupling inductor connects serially with two boost inductors. Two capacitors are used to provide voltage clamping and filtering function. The filter capacitor generates a low impedance path for returning current and filters the magnetizing current which is generated from the coupling inductor. According to the combined characteristics of coupling inductor and filter capacitors, the grid current is kept the same as conventional BPFC. Therefore, the utilizations of components are maintained. This topology effectively minimizes CM

noise in the circuit, however, comparing to Case 7 one more magnetizing component is required. Also, a DM filter requirement is kept. A further optimal design of this topology is demonstrated in [2.21] which integrated all of the inductors into one magnetic core to increase the power density of the design platform.

Case 9: BPFC with Active Virtual Ground

An Active Virtual Ground (AVG) circuit was proposed in 2015 [2.22] as shown in Figure 2-1 (i). The additional circuit of this hybrid clamped topology includes two-bidirectional LF switches (S_A and S_B) in line frequency and a capacitor (C_{AB}). Isolated drivers are required. The switches switch alternatively and synchronize with LF in order to generate an *LCL* filter to attenuate the high switching frequency in the current loop. Therefore, the grid-side current ripple is reduced. CM noise can also be reduced as the capacitor clamping the potential difference between the ac power source and the ground. In this case, the overall EMI filter can be minimized as both CM and DM noises are also minimized.

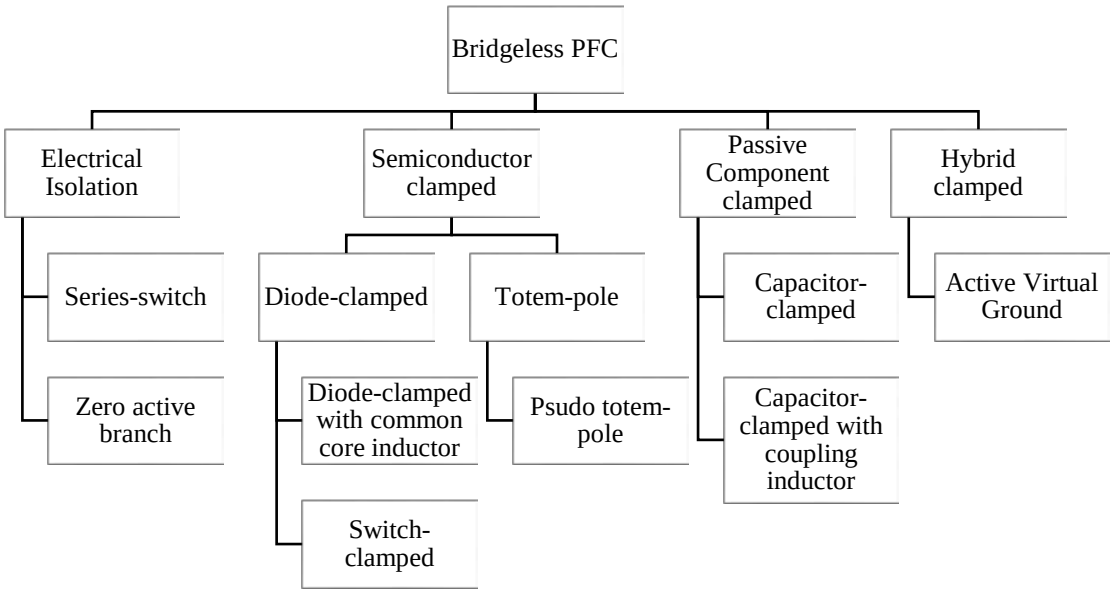


Figure 2-2. Family tree of BPFC topologies with CM voltage mitigation.

TABLE 2-I SUMMARY OF NUMBERS OF SEMICONDUCTOR DEVICES AND EXTRA FILTERING COMPONENTS INVOLVED IN THE SWITCHING TRANSIENTS

Topologies	Case	On State Devices		Off State Devices		LF Devices	HF Devices	Extra Filter Components
		Diode	Switch	Diode	Switch			
Conventional PFC		2	1	3	0	4	2	0
Conventional BPFC	1	0	2	1	1	0	4	0
BPFC with Series-switch	2	0	2	1	2	0	5	0
BPFC with a Zero Active Branch	3	2	1	1	1	0	9	0
Diode-clamped BPFC	4	1	1	2	0	2	4	0
Diode-clamped BPFC with common core inductor	5	1	1	2	0	2	4	0
Totem-pole BPFC	6	1	1	1	1	2	2	0
Capacitor-clamped BPFC	7	0	2	1	1	0	4	2
Capacitor-clamped BPFC with coupling inductor	8	0	2	1	1	0	4	3
BPFC with an Active Virtual Ground	9	0	2	1	1	2	4	1

TABLE 2-II SYSTEM SPECIFICATION

Parameter	**Value**	**Parameter**	**Value**
Input Voltage	120 Vac	Output Voltage	400 Vdc
Switching Frequency (f_{sw})	200 kHz	Output Power	300 W
Inductor value	150 µH	Filter Capacitor	4.7 µF

A summary of component counts is given in TABLE 2-I and a target platform specification is shown in TABLE 2-II. Considered in the 200 kHz platform, apart from Totem-pole BPFC, MOSFETs are suitable to be the main switches for the rest of the topologies.

2.3 CM and DM Noise Analysis

2.3.1 HF Analysis Model of Various Topologies

On describing EMI in converter design, there are two different types of noises. One is CM noise where the noise current is named as leakage current. The leakage current is induced from the parasitic capacitors in the system. The other calls DM noise which can be projected from the HF current ripple on the ac grid.

To analyze the noise current paths in different circuits, HF modelling method is applied and is used to generate the HF equivalent model [2.23], [2.24] of each topology. The traditional BPFC is taken as an example to demonstrate the analysis method in detail. The structure of the BPFC is symmetric in both positive and negative half line cycle. Therefore, only the positive half line cycle, as shown in Figure 2-4, is applied in the following analysis.

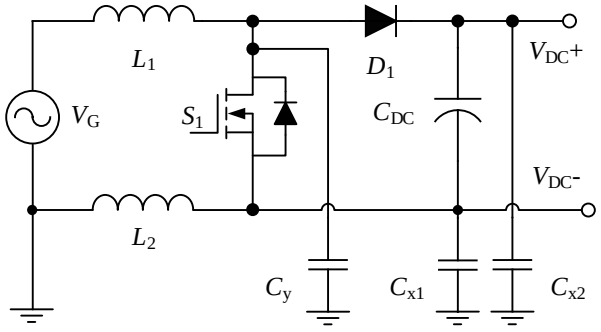
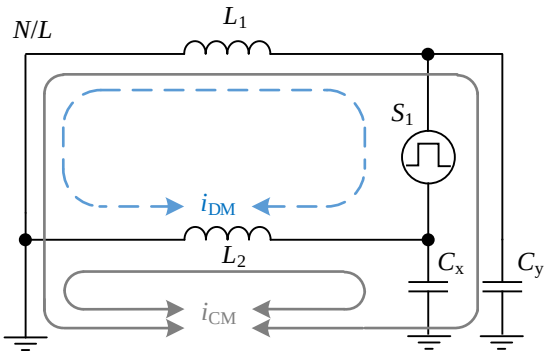
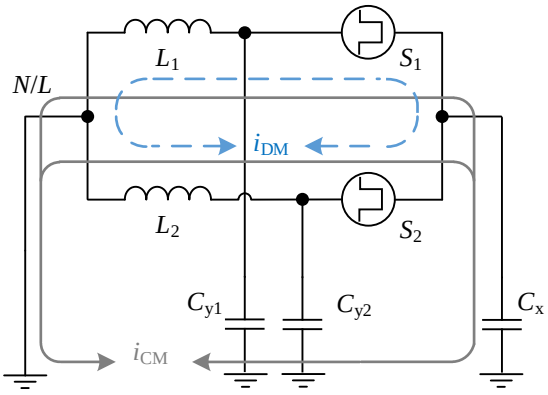


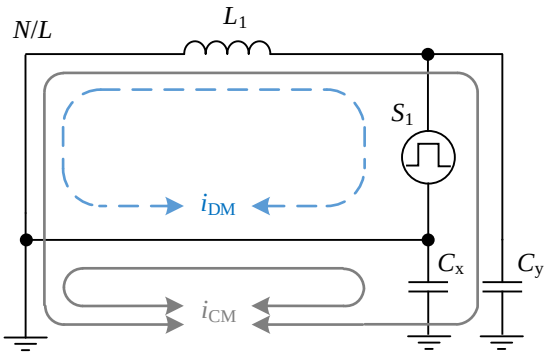
Figure 2-3. Positive half line cycle of BPFC schematic.



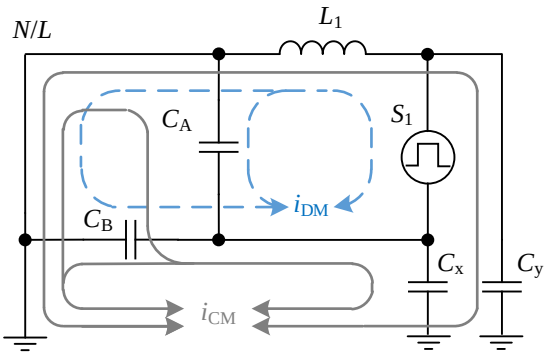
(a) Case1



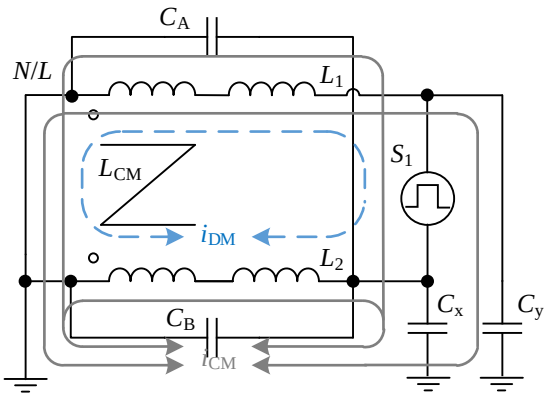
(b) Case 2, 3



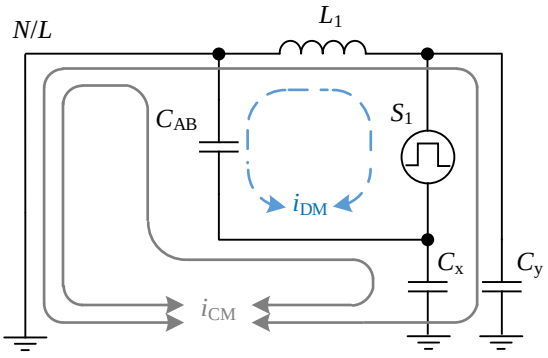
(c) Case 4, 5, 6



(d) Case 7



(e) Case 8



(f) Case 9

Figure 2-4. Positive half line cycle HF equivalent model of BPFC family.

In the analysis, each HF switching point also has a parasitic capacitor located between them and the ground connection point. C_{x1} is the parasitic capacitor between the positive dc Bus and the ground, C_{x2} is the parasitic capacitor between the negative dc Bus and the ground, C_y is the parasitic capacitor between the drain of MOSFET and the ground.

Some guidelines are as follows:

- All ac sources and dc loads are considered as short-circuit.
- All inductors are considered as an open-circuit when a filter capacitor is paralleled with them.
- All switching MOSFETs are considered as a noise source with ripple ΔV_s.

A simplified HF equivalent circuit of Figure 2-3 is shown in Figure 2-4 (a). With the same method, the equivalent models of the whole family topologies are converted into six equivalent circuits as shown in Figure 2-4. In the figures, the blue dotted line is representing the DM noise current path. The grey solid line is representing the CM noise current path related to the coupling capacitor C_x, as the sum of C_{x1} and C_{x2}. In BPFC, the DM noise current equivalent to the inductor ripple current and the CM noise voltage appears in C_x is equal to inductor voltage.

For the electrical isolation group, the system HF model is shown in Figure 2-4 (b). Two noise source currents are presented which are out of phase and have the same amplitude. Therefore, on top of the parasitic capacitor, the noise generated by the two noise sources are canceled with each other, and zero CM noise is resultant in the ideal situation. On the circuit point of view, the leakage current path is always blocked by the circuit diodes. Therefore, no HF leakage current exists. The DM current loop is kept the same as the DM current loop in Case 1.

Both diode-clamped BPFC, diode-clamped BPFC with common core inductor and totem-pole

BPFC are having the same equivalent circuit, as shown in Figure 2-4 (c), which is also the same as the conventional PFC. The CM noise voltage in capacitor C_x will be equal to zero as it would behave like a short circuit under ideal conditions. The DM noise current in the grid is kept the same as the inductor current ripple.

In the capacitor-clamped BPFC, as shown in Figure 2-4 (d), the CM noise voltage appears in the coupling capacitor C_x which is equal to the voltage across by the filter capacitors C_A and C_B. At HF point of view, the impedance of a capacitor is with a relatively small value. Thus, a nearly zero potential path is generated and the CM noise voltage can be maintained as a small amplitude. The DM noise current is half on inductor current and is the same as the DM noise current in Case 1.

The equivalent model of capacitor-clamped BPFC is shown in Figure 2-4 (e). The advantage of this topology is the coupling inductor acting like a CM filter to minimize the CM noise current. In this case, the DM noise current magnitude will be the same as the current magnitude in Case 1.

In the AVG-BPFC, Figure 2-4 (f), the CM noise voltage is equal to the potential difference across the filter capacitor. HF components of the noise voltage are minimized in a small magnitude. In the ideal situation, the HF current ripple is filtered by the grid-side *LCL* filter and results in a low DM noise.

2.3.2 Steady State Characteristics of the HF Components

The CM voltage ripple can be determined from the HF equivalent model and the current ripple can also be found by analyzing the steady state characteristics of the converter and from the structure of the input filters.

According to the specification listed in TABLE 2-II, the transfer function of different input filters is found. The magnitude plot is shown in Figure 2-5.

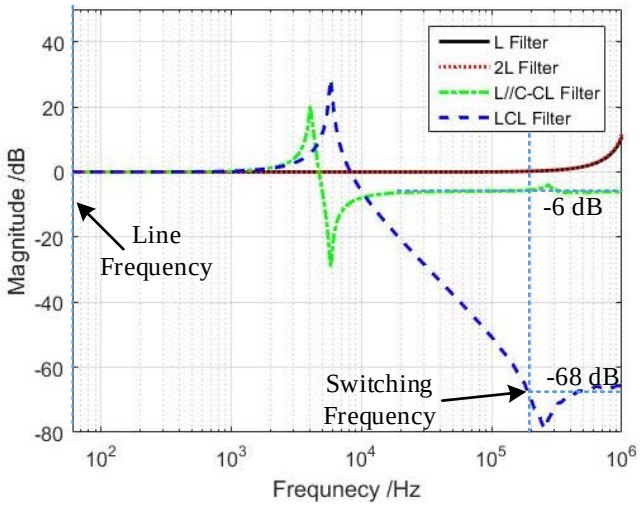


Figure 2-5. Transfer function of different input filters.

From Figure 2-4 (a), the HF CM voltage amplitude of Case 1 (conventional BPFC) is expressed as,

$$\Delta V_{\text{HF CM\_case 1}} = \frac{L_1 \cdot (1-\omega^2 \cdot L_2 \cdot C_{\text{x}})}{L_1+L_2-\omega^2 \cdot L_1 \cdot L_2 \cdot (C_{\text{x}}+C_{\text{y}})} \cdot \Delta V_s \approx \frac{L_1}{L_1+L_2} \cdot \Delta V_{\text{s}}, \tag{2.1}$$

where ω is angular switching frequency.

The value of the coupling capacitor C_{y} is relatively small compared to C_{x}. Therefore, the observed HF CM voltage across the capacitor C_{x} is close to the ripple voltage in the inductor. From the circuit operation, it shows that the input of the converter is an L filter structure where two inductors are in series connection. The grid current ripple is the same as the converter inductor current ripple, thus, the corresponding HF grid current ripple is expressed as,

$$\Delta I_{\text{in\_case 1}} = \Delta I_{\text{L\_case 1}} = \frac{V_{\text{ac\_peak}} \cdot \sin(\omega t)}{L_1 \cdot f_{\text{sw}}} \cdot (1 - \frac{V_{\text{ac\_peak}} \cdot \sin(\omega t)}{V_{\text{out}}}). \tag{2.2}$$

The CM equivalent circuit of Cases 2 and 3 in Figure 2-4 (b) can be further reduced under the symmetric structure. The two ideal noise sources can be combined together as a constant voltage source with the value of $V_{dc}/2$ and the influence of C_{y1} and C_{y2} are cancelled. No HF component appears in the capacitor C_x. The input filter structure of Case 2 is kept the same as Case 1. Therefore, the HF CM voltage and the HF grid current ripple amplitude of the electrical isolation are expressed as,

$$\Delta V_{\text{HF CM\_case 2,3}} \approx 0, \tag{2.3}$$

$$\Delta I_{\text{in\_case 2,3}} = \Delta I_{\text{in\_case 1}}. \tag{2.4}$$

From the equivalent circuit of Cases 4, 5 & 6, as Figure 2-4 (c), for the corresponding HF CM voltage amplitude is expressed as,

$$\Delta V_{\text{HF CM\_case 4,5,6}} = 0. \tag{2.5}$$

In Cases 4 & 5, one of the inductors is disabled by the parallel diode in every cycle. Therefore, the input filter structure is kept as an *L* filter but with a single inductor. The inductor current ripple is twice of the ripple in Case 1. In Case 6, the inductor ripple current keeps the same as the ripple in a conventional BPFC. Therefore, the corresponding HF grid current ripple in both situations is expressed as,

$$\Delta I_{\text{in\_case 4,5}} = 0.5\Delta I_{\text{in\_case 1}}, \tag{2.6}$$

$$\Delta I_{\text{in\_case 6}} = \Delta I_{\text{in\_case 1}}. \tag{2.7}$$

As shown in Figure 2-4 (d) and (e), the CM equivalent circuit of Case 7 is similar to the topologies of Case 8. The only difference is the inductor value in Case 8 is adding the mutual

inductance of the coupling inductor, L_{M}, to the equivalent model. The HF CM voltage amplitude is expressed as,

$$\Delta V_{\text{HF CM\_case 7}} = \frac{1-\omega^2 \cdot L_1 \cdot C_{\mathrm{y}}}{(1-\omega^2 \cdot L_1 \cdot C_{\mathrm{y}}) - \omega^2 \cdot L_1 \cdot + C_{\mathrm{B}} + C_{\mathrm{x}}} \cdot \Delta V_{\mathrm{s}}, \tag{2.8}$$

$$\Delta V_{\text{HF CM\_case 8}} = \frac{1-\omega^2 \cdot (L_1 + L_{\mathrm{M}}) * C_{\mathrm{y}}}{(1-\omega^2 \cdot L_1 \cdot C_{\mathrm{y}}) - \omega^2 \cdot (L_1 + L_{\mathrm{M}}) \cdot (C_{\mathrm{A}} + C_{\mathrm{B}} + C_{\mathrm{x}})} \cdot \Delta V_{\mathrm{s}}. \tag{2.9}$$

From (2.8) and (2.9), it is clearly observed that either increasing the value of the filter capacitor or inductor is able to help the system to generate less CM noise.

In the capacitor-clamped BPFC, one inductor is paralleled with a capacitor and one is coupling between the grid and the negative bus terminal. Therefore, only one inductor is working as the converter-side inductor. The ripple of the inductor current in Cases 7 and 8 is twice as the ripple in Case 1. However, due to the input filter structure, a 6 dB deduction appears on the grid current side. Thus, the corresponding HF grid current ripple in this situation is kept the same as the ripple in Case 1 and is express as,

$$\Delta I_{i\text{n\_case 7,8}} = \Delta I_{\text{in\_case 1}}. \tag{2.10}$$

From Figure 2-4 (f), the HF CM voltage amplitude is determined as,

$$\Delta V_{\text{HF CM\_case 9}} = \frac{1-\omega^2 \cdot L_1 \cdot C_{\mathrm{y}}}{(1-\omega^2 \cdot L_1 \cdot C_{\mathrm{y}}) - \omega^2 \cdot L_1 \cdot (C_{\mathrm{AB}} + C_{\mathrm{x}})} \cdot \Delta V_{\mathrm{s}}. \tag{2.11}$$

In the AVG-BPFC, the input is an *LCL* filter, one inductor acts as the converter-side inductor and one acts as the grid-side inductor. Similarly, the ripple of the inductor current in this is twice as the ripple in Case 1. However, due to the low-pass filter characteristic, the grid-side current ripple is much smaller than the inductor-side current ripple and it is expressed as,

$$\Delta I_{\text{in\_case 9}} = \frac{\Delta I_{\text{in\_case 1}}}{16 \cdot \pi \cdot C_{\mathrm{AB}} \cdot L_1 \cdot {f_{\mathrm{sw}}}^2}. \tag{2.12}$$

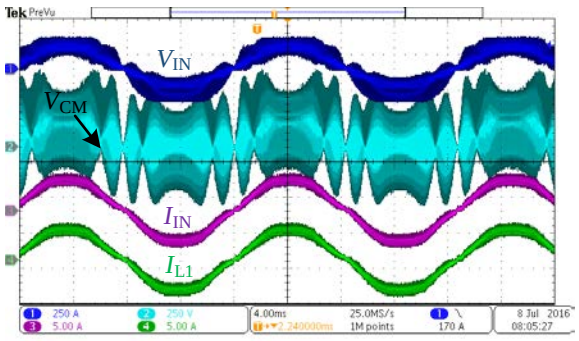
From (2.12), it is clearly observed that the ratio of the grid current ripple in the AVG-BPFC is much smaller than the ripple in other cases. Under the targeting operational frequency, it has a 68 dB reduction in the magnitude. Thus, the corresponding DM noise is the smallest among the reviewed topologies.

2.4 Experimental Verification

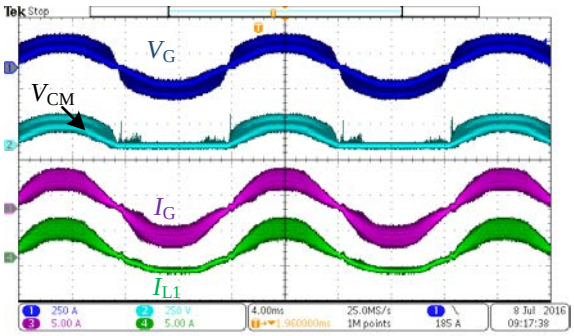
A 110 Vac input, 400 Vdc output, 300 W Bridgeless PFC converter is adopted as a measurement platform to benchmark the listed CM mitigation BPFC topologies. The platform specification is the same as the specification shown in TABLE 2-II. Topologies are verified with an inductive source to simulate the weak grid situation. Figure 2-6 shows the experimental waveforms of 4 key topologies, including (a) Case 1: Simple BPFC, (b) Case 4: Diode-clamped BPFC, (c) Case 7: Capacitor-clamped BPFC, and (d) AVG-BPFC.

From the results, it can be seen that in all of CM voltage mitigation topologies, the HF CM ripple can be successfully minimized compared to the simple BPFC. In the grid current ripple, the AVG-BPFC provided the lowest in value. Overall, Case 9 provided the smallest grid current ripple and also successfully mitigated the CM voltage in the coupling capacitor.

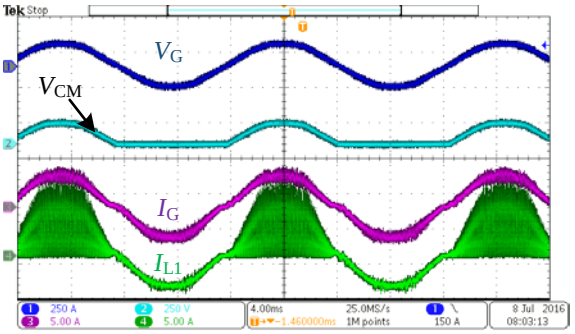
In Case 4, the result was slightly different from the predicted waveform. As in Case 7 and 9, the filter capacitor was helping to clamp the ac voltage but not in Case 4. Therefore, in the weak grid situation, HF voltage ripple was generated from the grid inductor. In a real case scenario, the equivalent model of Case 4 will become similar in half of the switching cycle and a HF CM ripple appeared in the coupling capacitor.



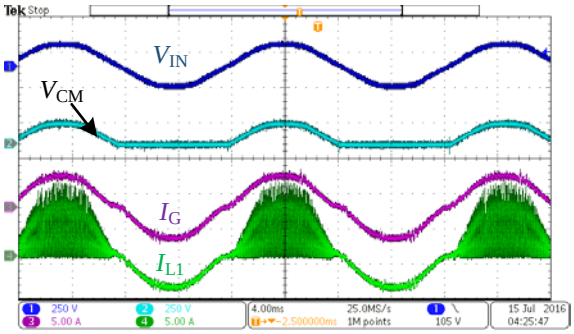
(a) Conventional BPFC, Case1



(b) Diode-clamped BPFC, Case 4



(c) Capacitor-clamped BPFC, Case 7



(d) AVG-BPFC, Case 9

Figure 2-6. Measurement results of different BPFC topologies, CH1: Grid Current, CH2: Inductor Current, CH3: Grid Voltage, CH4: CM Voltage.

2.5 Conclusion

The chapter presented a review and a comparative study of various kinds of BPFC topologies with CM voltage mitigation techniques. A topology family tree was provided based on the classification of the CM mitigation strategy. An EMI noise analysis was provided. The CM mitigating performances of the critical topologies have been experimentally verified and compared in a 300W prototype. Under the EMI consideration, the topology AVG-BPFC (Case 9) resulted in a relatively low HF CM voltage and low DM current which can benefit in the use of the BPFC

topology. Compared with the conventional BPFC, the only drawback of Case 9 is the number of LF semiconductors is increased.

Reference

[2.1] D. M. Mitchell, “AC-DC Converter having an improved power factor,” US Patent, No. US4412277 A, 25/10/1983.

[2.2] *Electromagnetic compatibility - Requirements for household appliances, electric tools and similar apparatus - Part 1: Emission*, IEC Standard IEC CISPR 14-1:2016, 2016.

[2.3] *Electromagnetic compatibility of multimedia equipment - Emission requirements*, IEC Standard IEC CISPR 32:2015, 2015.

[2.4] F. K. A. Lima, C. M. T. Cruz, and F. L. M. Antunes, “A family of turn-onand turn-off non-dissipative passive snubbers for soft-switching single phase rectifier with reduced conduction losses,” in *Proc. IEEE PESC*,vol.5, pp. 3745-3750, Jun. 2004.

[2.5] A. F. de Souza and I. Barbi, “A new ZVS-PWM unity power factor rectifier with reduced conduction losses,” *IEEE Trans. Power Electron.*, vol. 10, no. 6, pp. 746-752, Nov. 1995.

[2.6] Chien-Ming Wang, “A new single-phase ZCS-PWM boost rectifier with high power factor and low conduction losses,” in *Proc. IEEE APEC*, vol. 3, pp. 1458-1464, Feb. 2004.

[2.7] M. Xu and Q. L. Chen, “AC-to-DC conversion apparatus and related control manner thereof,” *US Patent*, No. US20130016545 A1, 17/01/2013.

[2.8] D. Tollik, A. Pietkiewicz, “Comparative analysis of 1-phase active power factor correction topologies,” in *Proc. IEEE INTELEC*, pp. 517- 523, Oct. 1992.

[2.9] P.Kong, S. Wang, and F.C. Lee, “Common Mode EMI Noise Suppression for Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol.23, no.1, pp. 291-297, Jan. 2008.

[2.10] A. F. de Souza and I. Barbi, “High power factor rectifier with reduced conduction and commutation losses,” in *Proc. IEEE Telecommunication Energy Conference*, Jun. 1999.

[2.11] E. Myhre *el at*, “Device arranged for converting an ac input voltage to a dc output voltage,” *US Patent*, No. US20100277837 A1, Nov. 2010.

[2.12] L. Sui *el at*, “Bridgeless PFC circuit for CRM and controlling method thereof,” *US Patent*, No. US7630221 B2, Dec. 2009.

[2.13] H. Mao *el at*, “High efficiency bridgeless PFC converter and method,” *US Patent*, No. US8385032 B1, 26/2/2013.

[2.14] M. A. Liquicia *el at*, “Commutator for bridgeless pfc circuit,” *US Patent*, No. US20130077371 A1, 28/03/2013.

[2.15] Y. Jang *el at*, “Power factor correction rectifier having independent inductive components,” *US Patent*, No. US7265650 B2, Sept. 2007.

[2.16] J. C. Salmon, “Circuit topologies for PWM boost rectifiers operated from 1-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs,” in *Proc. IEEE APEC*, vol 1, pp. 473–479, Mar. 1995.

[2.17] J. Liu, F.C, W. Chen, F.C, J. Zhang, F.C., D. Xu, and F.C. Lee, “Evaluation of power losses in different CCM mode single-phase boost PFC converters visa a simulation tool,” *in Proc. IEEE IAC*, vol. 4, pp. 2455-2459, Oct. 2011.

[2.18] M. Soldano and B. Lu, “EMI noise reduction circuit and method for bridgeless PFC circuit,’ *US Patent*, No. US7215560 B2, 8/05/2007.

[2.19] T. Y. Yang, “High efficiency bridgeless PFC power converter,” *US Patent*, No. US8199541 B2, 12/06/2012.

[2.20] K. D. Wildash, “Bridgeless boost PFC circuits and systems with reduced common mode EMI,” *US Patent*, No. US20110037444 A1, 17/02/2011.

[2.21] Biela, J., Kolar, J. W. and Deboy, G., “Optimal design of a compact 99.3% efficient single-phase PFC rectifier,” in *Proc. of IEEE APEC*, pp. 1397-1404, Feb. 2010.

[2.22] N. M. Ho and T. H. Li, “Bridgeless power factor correction circuit,” *US Patent*, No. US9093917 B2, 07/28/2015.

[2.23] Haoyi Ye, Zhihui Yang, Jingya Dai, “Common mode noise modeling and analysis of dual boost PFC circuit,” in *Proc. IEEE INTELEC*, pp. 578-582, Sept. 2004.

[2.24] M. Shoyama, L. Ge, and T. Ninomiya, “Balanced switching converter to reduce common mode conducted noise,” *IEEE Trans. on Ind. Electron.*, vol. 50, no. 6, pp. 1095-1099, Dec. 2003.

Chapter 3 Active Virtual Ground – Bridgeless PFC Topology

The work described in this chapter was published in the following paper: C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, "Active Virtual Ground—Bridgeless PFC Topology," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2016.

3.1 Abstract

The chapter presents a new bridgeless Power Factor Correction (PFC) topology, using a recently proposed controllable *LCL* filter, namely Active Virtual Ground (AVG) to achieve efficient power conversion and high frequency (HF) common mode voltage (CM) reduction. The proposed PFC circuit consists of HF semiconductors for shaping inductor current, and low frequency semiconductors to form two different *LCL* structures for different conditions. This reduces grid differential mode (DM) current ripple or inductance. Besides, the PFC CM voltage, the main problem of bridgeless PFCs, is significantly reduced, since the capacitor in the *LCL* filter clamps the voltage between the grid and the converter ground. The performance of the proposed PFC is experimentally verified. The results show that the proposed PFC guarantees sinusoidal input current, low HF common-mode voltage noise and has a good agreement with the theoretical findings.

3.2 Introduction

Power Factor Correction (PFC) circuit is a front-end power stage of a grid-connected power converter, such as power supply, motor drive and electronic ballast [3.1] - [3.7]. It is used to meet international grid current standards, such as IEEE519 and IEC-61000-3-2 (for 1-phase). And those standards are also applied to the single phase grid network which is typical as an ac power source for low power industrial applications and household devices. By using a PFC in a system, it ensures sinusoidal input current and stable output dc voltage. It can be foreseen that PFC will be a very important device to ensure good power quality in the further complex grid network. Among PFC topologies, Bridgeless PFC (BPFC) was proposed in the early 80s [3.8] and it is promising in terms of efficiency due to fewer semiconductors in the current paths [3.9]. However, common mode (CM) voltage issue leading to leakage current issue is the limitation of the topology in a lot of applications [3.10]. The CM voltage issue creates Electro-Magnetic Interference (EMI) problems.

Some methodologies have been proposed to solve the CM voltage issue for BPFC, they can be classified into three categories. The first is to give an electrical isolation. Generally, it gives an additional current circulating path [3.11] or disconnects the leakage current path [3.12] by using additional semiconductors. However, they increase semiconductor cost and conduction losses, as extra full power rating semiconductor devices are required and they are in the main PFC current path. The second is to use additional semiconductors to clamp the common mode voltage to be zero either using diodes [3.10], [3.13] or active switches [3.14], [3.15]. The method effectively suspends the common mode voltage due to physically connecting the converter-ground to a grid terminal, but the inductors are not fully utilized which cause high differential mode (DM) current to the grid. The third is to use capacitors to clamp the common mode voltage [3.16] - [3.18]. It is a good approach to give low impedance paths for the high frequency (HF) components, but the

large HF DM current is still presenting in the grid terminals due to two capacitors are in parallel for HF components and the grid is in between. Therefore, the methods can solve the CM voltage issue, but they create other problems such as higher semiconductor conduction losses, larger grid current ripple and higher system or component design complexity.

This chapter proposes a new bridgeless PFC topology to transform single phase ac voltage to dc voltage. Figure 3-1 shows the proposed topology. The PFC consists of a conventional BPFC and an additional circuit. The additional circuit can change the input filter to different *LCL* structures depending on grid voltage polarities by using the built-in BPFC inductors. This results in a reduction of grid-side DM current ripple or required inductance of the input chokes. Besides, the PFC can mitigate the conventional CM voltage issue, since the capacitor in *LCL* filter clamps the voltage between the grid and the negative terminal of dc bus and provides a low impedance path for HF components. Thus, this technique is namely Active Virtual Ground (AVG). This chapter will define the problems, explain the operating principle of the proposed converter, provide steady state characteristics, and experimental results will be demonstrated to verify the proposed concept. A simple add-on AVG circuit and a 300W BPFC have been built. The AVG circuit can be simply connected in front of the BPFC then it will give the advantages of 1) low CM voltage, and 2) low grid-side DM ripple current and will keep the low conduction loss advantages of BPFC, since the AVG circuit only manages the HF current and it is in parallel with the main current path.

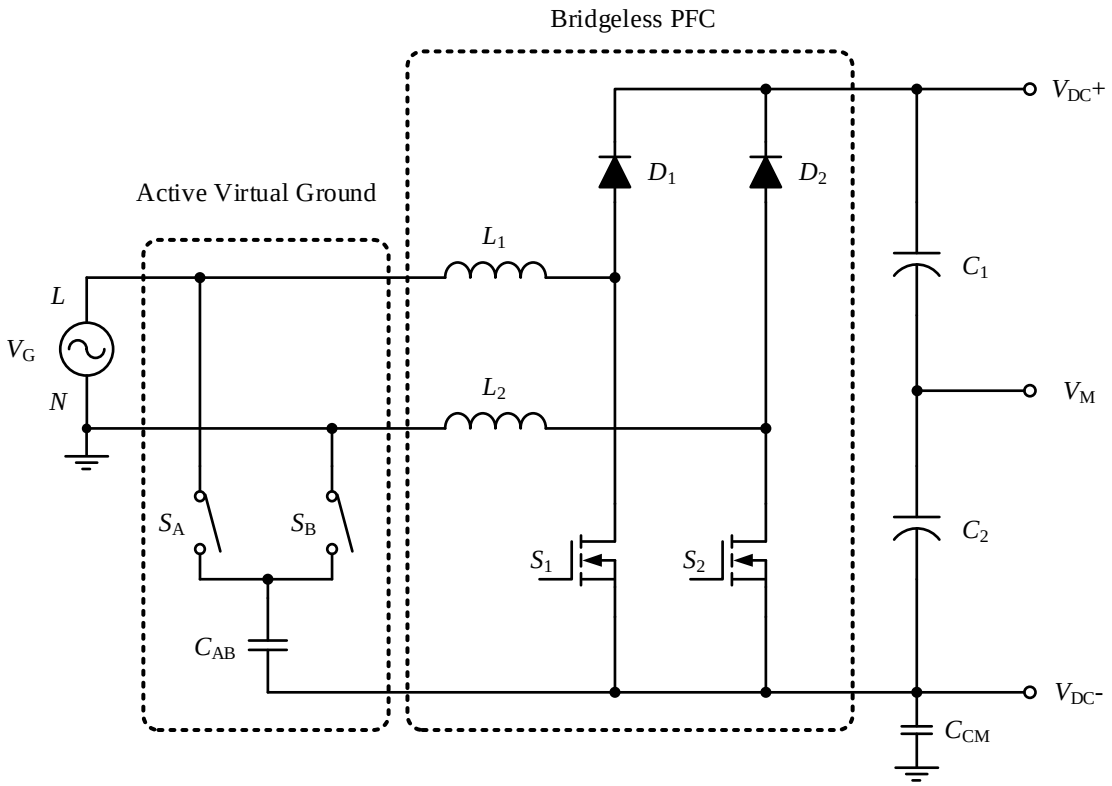


Figure 3-1. The proposed single phase bridgeless PFC topology.

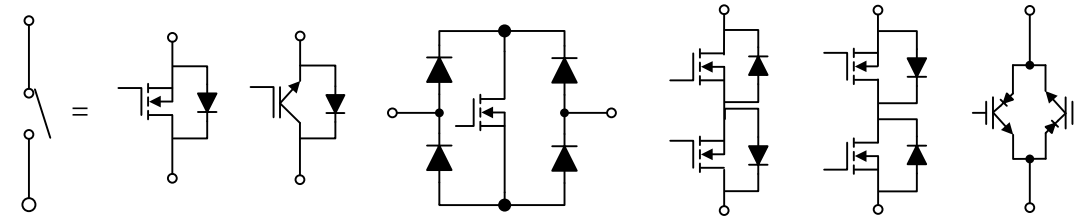
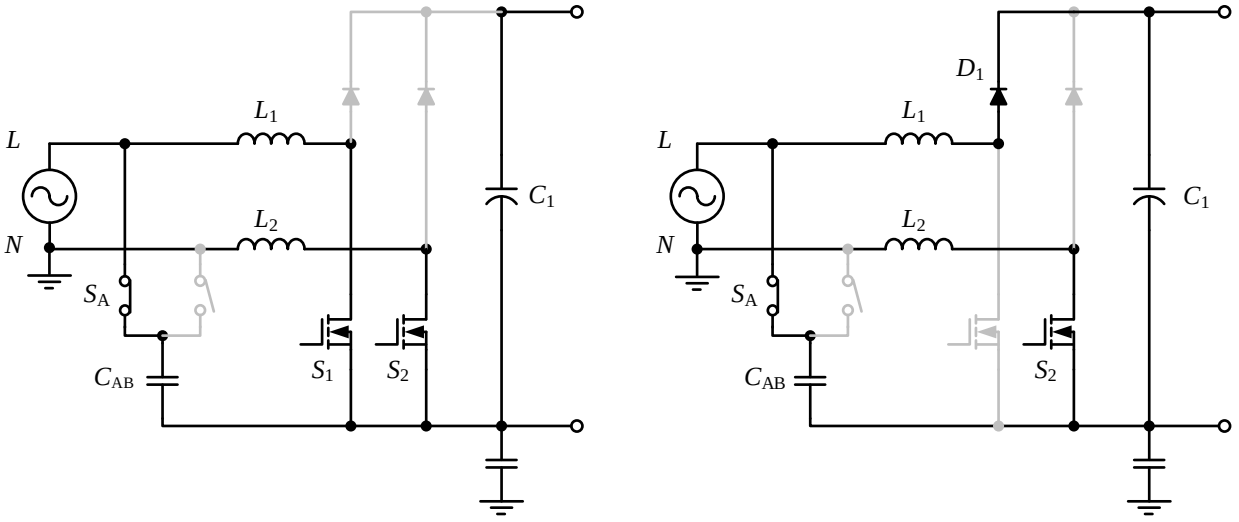


Figure 3-2. Bidirectional current switch arrangements, (a) Ideal switch, (b) MOSFET, (c) IGBT, (d) Diode bridge, (e) Common emitter back-to-back, (f) Common drain back-to-back, and (g) anti-paralleled reverse blocking IGBTs.

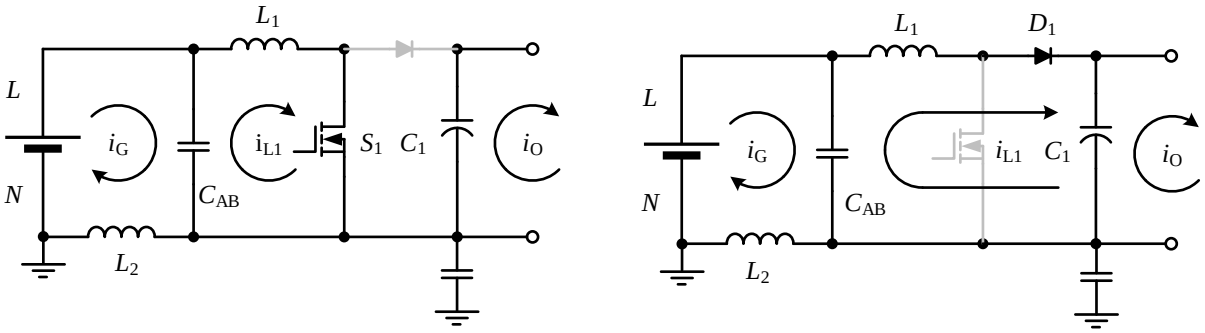
3.3 Principles of Operation

Figure 3-1 shows that the proposed bridgeless BPFC boosts an ac grid voltage to a higher dc bus voltage and regulates the dc component of the dc bus voltage to the desired value. The circuit includes a typical BPFC circuit and an AVG circuit. The AVG circuit filters out HF components which are generated by the BPFC during switching. It avoids the HF components flowing through the ac grid. The additional circuit consists of two bidirectional current switches (S_A and S_B) connecting in series, and they are coupled to a Line (L) and Neutral (N) of the grid separately. The bidirectional current switches (S_A or S_B) can be realized by connecting two MOSFETs back-to-back in series or other configurations which are shown in Figure 3-2. The switches switch alternatively and synchronize with the line frequency. The AVG circuit also includes a capacitor (C_{AB}) that is coupled between the junction point of the two bidirectional current switches (S_A and S_B) and any point of the dc bus, such as the negative of dc bus (V_{DC-}). It is used to clamp the potential difference between the ac power source and the converter ground. From a HF noise's point of view, there is a very low impedance path between the dc link and the system ground. And the path is different in positive and negative half line cycles, it requires semiconductors to reconfigure the HF path. Thus, the circuit and technology are named as Active Virtual Ground (AVG) [3.19], [3.20].



(a) (b)

Figure 3-3. Current conducting paths of the AVG-BPFC in positive line cycle, (a) S_1 is ON, and (b) S_1 is OFF.



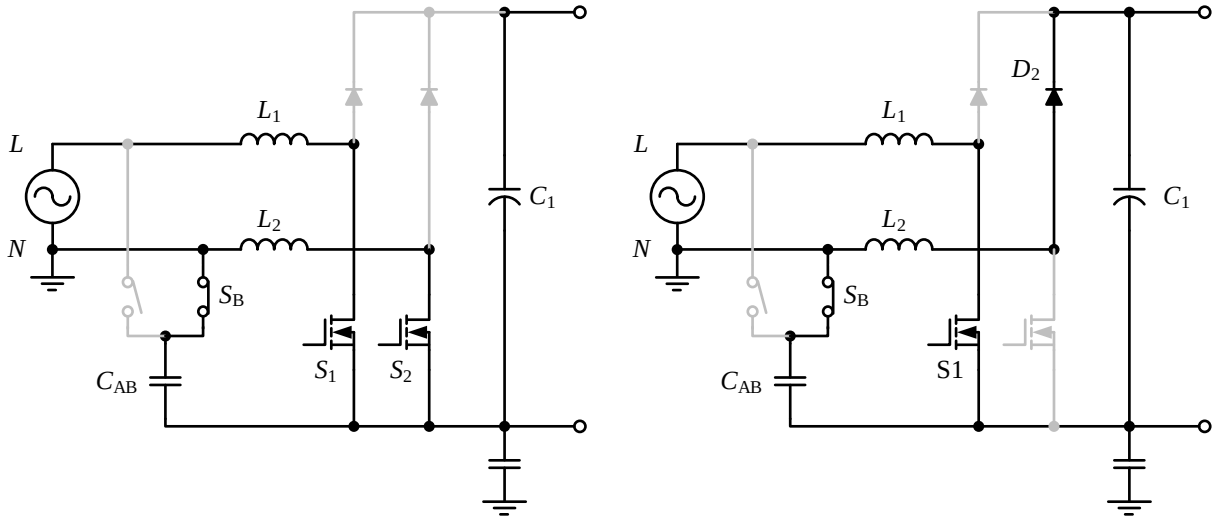
(a) (b)

Figure 3-4. Equivalent circuits of the AVG-BPFC in positive line cycle, (a) S_1 is ON, and (b) S_1 is OFF.

A. Operating Mode: Positive half line cycle

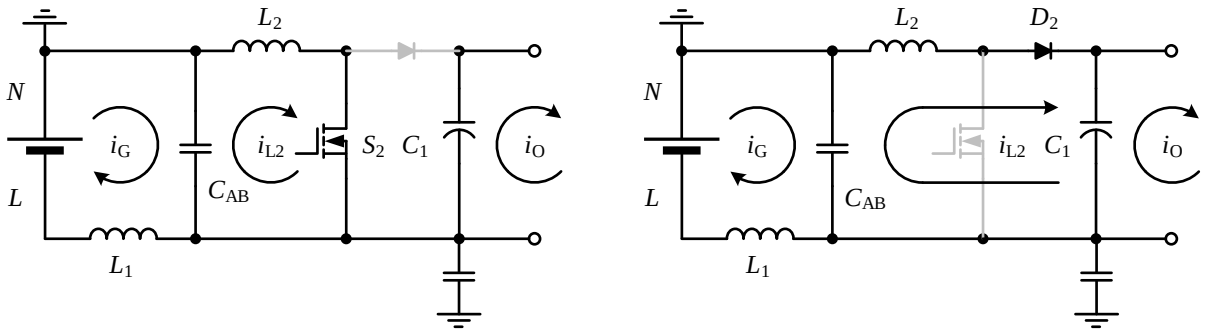
In Figure 3-3, there are two switching states in the proposed BPFC during a positive half line cycle. In this half line cycle, the filter capacitor (C_{AB}) is connected to L of the grid voltage source

through the bidirectional current switch (S_A), the main switch (S_2) is always conducting and the main switch (S_1) is switching at a HF. Figure 3-3 (a) and (b) show the circuit when the main switch (S_1) switching on and off, respectively. Figure 3-4 (a) and (b) are corresponding equivalent circuits of Figure 3-3 (a) and (b), note that S_2 is always conducting thus it is not shown in the circuits. It can be seen that L_1, C_{AB} and L_2 form an *LCL* filter between the grid and the switching cell S_1 and D_1. In this case, L_2 takes the role of grid inductor L_G, then a low grid differential mode (DM) current ripple is achieved. And C_{AB} is coupled between the L and the negative terminal of dc bus, the potential difference between them is clamped, therefore, a low CM leakage current is achieved.



(a) (b)

Figure 3-5. Current conducting paths of the AVG-BPFC in negative line cycle, (a) S_2 is ON, and (b) S_2 is OFF.



(a) (b)

Figure 3-6. Equivalent circuits of the AVG-BPFC in negative line cycle, (a) S_2 is ON, and (b) S_2 is OFF.

B. Operating Mode: Negative half line cycle

In Figure 3-5, there are two switching states in the proposed BPFC during a negative half line cycle. In this half line cycle, C_{AB} is connected to N of grid voltage source through S_B, S_1 is always conducting and S_2 is switching at a HF. Figure 3-5 (a) and (b) show the circuit when S_2 switching on and off, respectively. Figure 3-6 (a) and (b) are corresponding equivalent circuits of Figure 3-5 (a) and (b). It can be seen that L_2, C_{AB} and L_1 form an *LCL* filter between the grid and the boost converter. In this case, L_1 takes the role of L_G, then a low grid DM current ripple is achieved. And C_{AB} is coupled between N and the negative terminal of dc bus, the potential difference between them is clamped, therefore, a low CM leakage current is achieved.

C. Modulation Scheme

Control methodology of the AVG circuit is simple. Figure 3-7 shows an example of a controller for a BPFC with the proposed AVG circuit. In principle, the controller is compatible with a conventional BPFC. It consists of an outer voltage controller to regulate the dc bus voltage and an inner current controller to shape the converter-side inductor L_C currents. The AVG gate

signals, S_A and S_B, are taken from the outputs of a Polarity Detector to synchronize the AVG gate signals and the grid voltage v_G. Figure 3-8 shows simplified gate signals for the proposed topology. The AVG gate signals, S_A and S_B, are with the line frequency and complementary. The main switches, S_1 and S_2, switch at HF in a half line cycle alternately to shape the currents of L_1 and L_2, respectively. It is important to note that semiconductor losses can be minimized by the modulation scheme,

- Switching losses of the main switches: There is only one pair of switching cell with HF switching at all time.
- Conduction losses of the main switches: When the main switch is not with HF switching, it is turned on to let the reverse current go through the channel instead of the body diode. Generally, the channel of a MOSFET has a lower voltage drop than a body diode of a MOSFET [3.21].
- Switching losses of the AVG switches: The AVG switches switch at grid voltage zero crossings. In principle, it is also the zero crossing points of the grid current, thus it is zero current switching. Besides, the switching frequency is the line frequency, e.g. 60 Hz. Thus, switching losses of the AVG Switches can be neglected.
- Conduction losses of the AVG switches: The fundamental PFC current component does not pass through the AVG circuit. The circuit only conducts the HF inductor ripple current. Generally, a root-mean-square value of inductor ripple current is small, thus the conduction losses are also small.

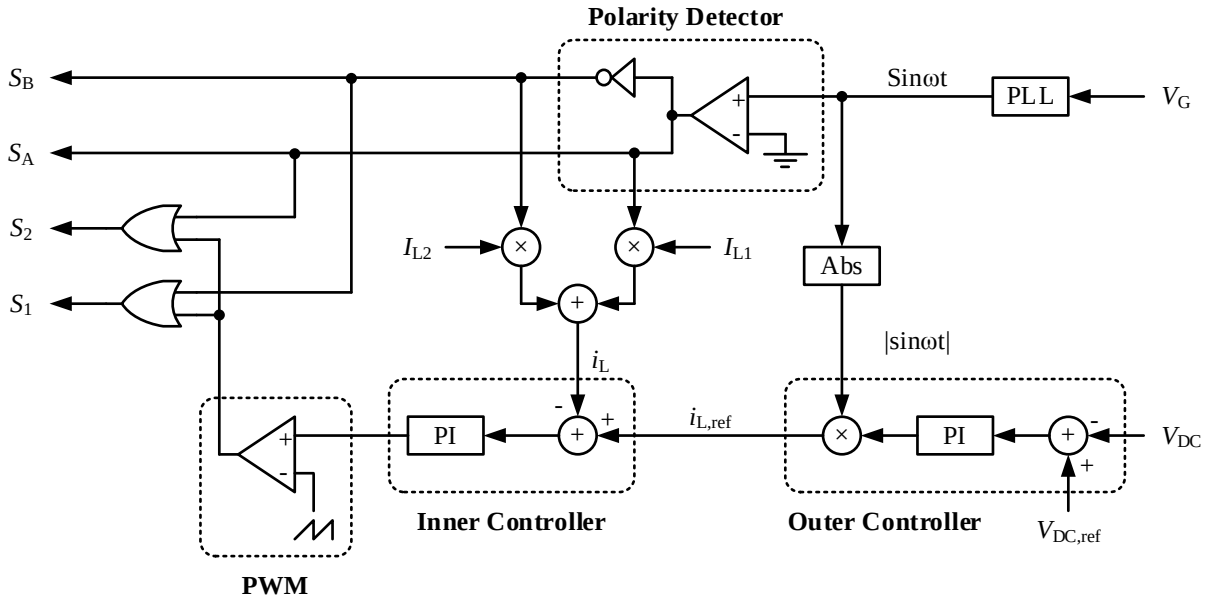


Figure 3-7. Controller block diagram for the AVG-BPFC topology.

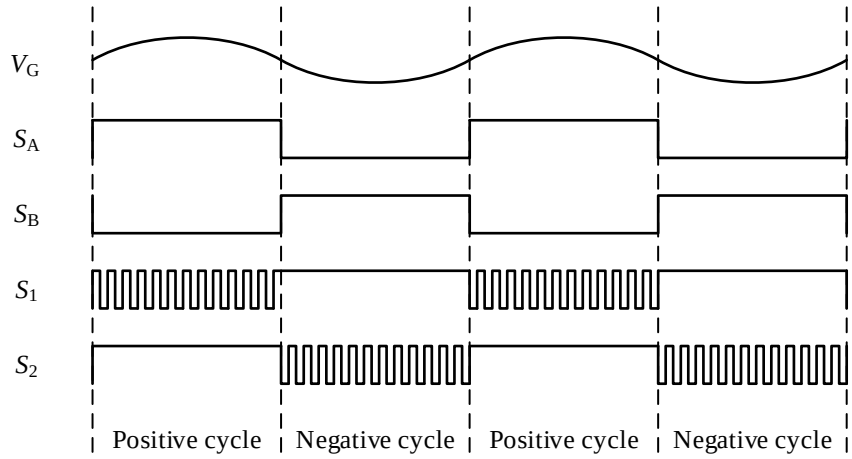


Figure 3-8. Simplified gate signals for the AVG-BPFC topology.

3.4 Steady State Characteristics

A. Duty Ratio

The inductors, L_1 and L_2, act as converter-side inductors L_C and grid-side inductors L_G, which

depends on the grid voltage polarity. In the case of the positive half line cycle, L_1 is the converter-side inductor L_C, and Figure 3-4 (a) and (b) indicate the equivalent circuits of on and off states.

Neglecting the voltage drop on the grid inductor, the AVG capacitor voltage v_C is the same as the grid voltage, thus,

$$v_C(t) \approx v_G(t) = V_G \sin \omega t, \tag{3.1}$$

where v_G is the instantaneous grid voltage, V_G is the peak amplitude of grid voltage, and ω is the angular line frequency.

Figure 3-4 and Figure 3-6 shows the on and off states of the main switches. The PFC operation is the same as a simple boost converter. Thus, the duty ratio D can be expressed by,

$$D(t) = 1 - \frac{V_G}{V_{DC}} \sin \omega t, \tag{3.2}$$

where V_{DC} is output dc bus voltage.

A detailed derivation of (3.2) is given in the Appendix.

B. Converter-side Inductor Current Ripple

The duty ratio is time varying in a line cycle following the change of grid voltage, which is shown in (3.2). Besides, in order to simplify the calculations, the inductances of L_1 and L_2 are assumed as identical and represented by L_X, i.e. $L_X = L_1 = L_2 = L_C = L_G$. If a constant switching frequency and continuous-conduction mode inductor current are considered, the converter-side current ripple Δi_{LC} can be found as,

$$\Delta i_{LC}(t) = \frac{(V_{DC} - V_G \sin \omega t) V_G \sin \omega t}{V_{DC} L_X f_{sw}}, \tag{3.3}$$

where f_{sw} is the switching frequency.

A detailed derivation of (3.3) is given in the Appendix.

C. AVG Capacitor Voltage Ripple

The voltage ripple of AVG capacitor is mainly contributed by the current ripple of the converter-side inductor, thus the voltage ripple peak to peak value Δv_{C} is,

$$\Delta v_{\mathrm{C}}(t) = \frac{(V_{\mathrm{DC}} - V_{\mathrm{G}} \sin \omega t) V_{\mathrm{G}} \sin \omega t}{8 V_{\mathrm{DC}} C_{\mathrm{AB}} L_{\mathrm{X}} f_{\mathrm{sw}}^2}, \tag{3.4}$$

where C_{AB} is capacitance of the AVG capacitor.

A detailed derivation of (3.4) is given in the Appendix.

D. Grid-side Inductor Current Ripple

The grid current is the same as the grid-side inductor current. The current ripple peak to peak value Δi_{G} is,

$$\Delta i_{\mathrm{G}}(t) = \frac{(V_{\mathrm{DC}} - V_{\mathrm{G}} \sin \omega t) V_{\mathrm{G}} \sin \omega t}{16 \pi V_{\mathrm{DC}} C_{\mathrm{AB}} L_{\mathrm{X}}^2 f_{\mathrm{sw}}^3}. \tag{3.5}$$

A detailed derivation of (3.5) is given in the Appendix.

E. Common-mode Voltage

The CM parasitic capacitor C_{CM} is shown in Figure 3-1. Figure 3-6 shows the HF (HF) equivalent circuit of the BPFC with AVG. It can be seen that the CM capacitor is in parallel to the AVG capacitor. Thus, the HF CM voltage ripple is the same as the AVG capacitor ripple. By modifying (3.4), the HF CM voltage ripple Δv_{CM} can be obtained,

$$\Delta v_{\mathrm{CM}}(t) = \frac{(V_{\mathrm{DC}} - V_{\mathrm{G}} \sin \omega t) V_{\mathrm{G}} \sin \omega t}{8 V_{\mathrm{DC}} (C_{\mathrm{AB}} + C_{\mathrm{CM}}) L_X f_{\mathrm{sw}}^2}, \tag{3.6}$$

where C_{CM} is capacitance of the parasitic CM capacitor.

Typically, the value of the parasitic CM capacitor is much smaller than that of the AVG capacitor, e.g. 4.7 nF and 4.7 μF, respectively. According to that assumption, the HF CM voltage is almost the same as the AVG capacitor ripple voltage.

F. Common-mode Leakage Current

The HF CM leakage current is defined as the current passing through the CM capacitor and the grid terminals, it is shown with dash line in Figure 3-9. According to the HF CM equivalent circuit in Figure 3-9, the HF CM leakage current is from the converter-side inductor ripple current, and the current is shared by the AVG capacitor. Thus, a current divider equation can be used to determine the HF CM leakage current Δi_{HFCM} in the circuit,

$$\Delta i_{\mathrm{HFCM}}(t) = \frac{c_{\mathrm{CM}}}{c_{\mathrm{AB}}+c_{\mathrm{CM}}} \Delta i_{\mathrm{LC}}(t). \tag{3.7}$$

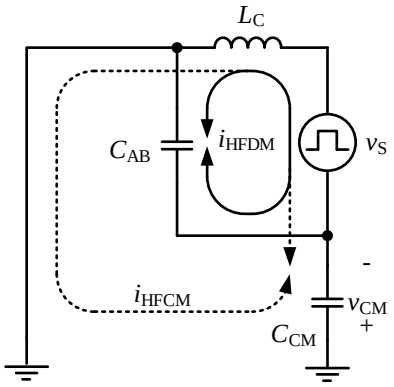


Figure 3-9. High frequency common mode equivalent circuit of a BPFC with AVG.

G. Frequency Response of AVG filter

The proposed AVG circuit is used to change a first-order *L* filter to become a third-order *LCL* filter. The equivalent circuits were shown in Figure 3-4 and Figure 3-6. Thus, the conventional *LCL* filter transfer function can be applied to the AVG filter [3.22], [3.23],

$$G_{\mathrm{AVG}}(\mathrm{s}) = \frac{-i_{\mathrm{G}}(\mathrm{s})}{u_{S1/S2}(\mathrm{s})} = \frac{-1}{\mathrm{s}(L_1 L_2 C_{\mathrm{AB}} \mathrm{s}^2 + L_1 + L_2)}, \tag{3.8}$$

where $u_{S1/S2}(s)$ is the voltage across S_1 or S_2, that is the HF signal source of the *LCL* filter.

The grid and converter inductances of the AVG circuit are identical. Thus, (3.8) can be simplified as,

$$G_{\mathrm{AVG}}(\mathrm{s}) = \frac{1/2L_{\mathrm{X}}}{\mathrm{s}\left(\frac{L_{\mathrm{X}} C_{\mathrm{AB}}}{2}\mathrm{s}^2 + 1\right)}. \tag{3.9}$$

The AVG circuit's characteristic resonance frequency, ω_{r}, can be determined as,

$$\omega_{\mathrm{r}} = \sqrt{\frac{2}{L_{\mathrm{X}} C_{\mathrm{AB}}}}. \tag{3.10}$$

3.5 Variants of AVG-BPFC

The AVG concept can be implemented by various topologies to operate as the modes in Figure 3-4 and Figure 3-6. And the control methodology and the gate signals in Figure 3-7 and Figure 3-8 can be applied.

Figure 3-10 (a) is a "Common-Source" type AVG-BPFC. It spits the AVG capacitor (C_{AB}) into two independent capacitors (C_{A} and C_{B}), and they only operate in a half line cycle by controlling the AVG switches, S_{A} and S_{B}. The advantage of the circuit is that it simplifies the gate drive circuit, since all active semiconductor devices refer to one point, in other words, no isolation is required for gate drive and sensing circuits. However, there are one additional AVG capacitor is required. It is suitable for low power and low cost applications.

Figure 3-10 (b) is an "X-Type" AVG-BPFC. It is similar to "Common-Source" type topology, it uses two independent AVG branches, one switch and one capacitor in series. The branches

connect to the boost inductors (L_1 and L_2) in "X-Shape". The advantage of the X-Shape type topology is easily adding the AVG circuit in an existing BPFC without connecting to the negative terminal of the dc link capacitor. However, it requires two low frequency floating gate drivers for the AVG switches.

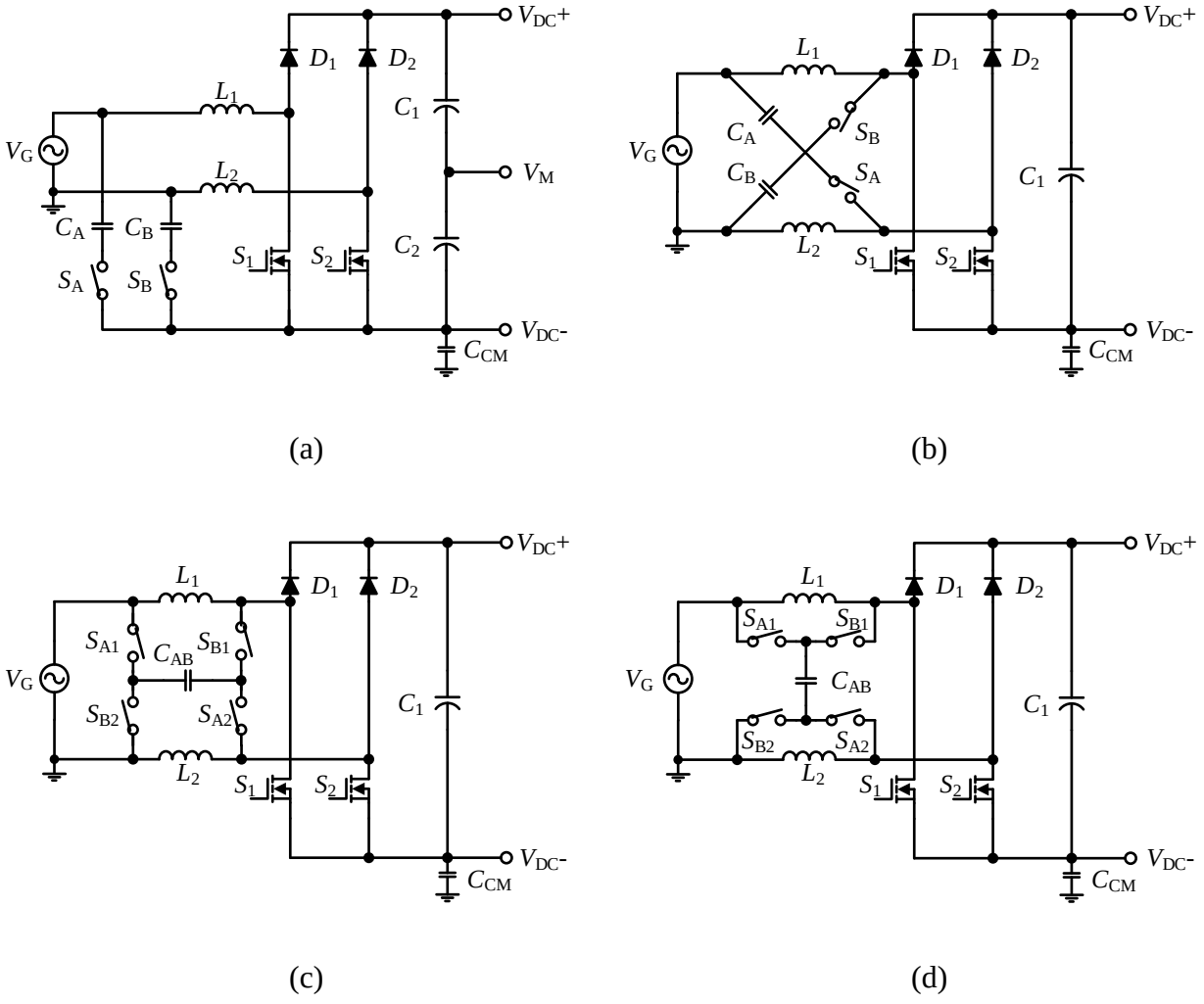


Figure 3-10. Four AVG variants for BPFC, (a) Common-source, (b) X-shaped, (c) H-shaped and (d) 2Y-shaped.

Figure 3-10 (c) and (d) are "H-Type" and "2Y-Type" AVG-BPFCs, respectively. The concept of the topologies is similar to "X-Type" but using one AVG capacitor. Thus, the advantage and

the disadvantage are the same as the “X-Type” circuit. All in all, all types of AVG circuits are good for high power applications, since the AVG circuit is only managing the HF ripple current.

3.6 System Implementation

A 300 W, 120 V/60 Hz input, 400V output voltages BPFC converter prototype has been used to evaluate the proposed topology, the specification is shown in TABLE 3-I. The BPFC is a commercial product, Texas Instruments (TI) HV Bridgeless PFC Developer's Kit [3.24], [3.25], with removing the HF input filter. A 60 Hz switching frequency AVG circuit has been implemented. Figure 3-11 (a) and (b) show a testbed photo and a system block diagram of the laboratory setup, respectively, for evaluating the proposed AVG-BPFC topology. The photo shows two PCBs, the right hand side one is the conventional BPFC, another one is the AVG circuit. The AVG circuit works like an “add-on” circuit by connecting three terminals to the BPFC, which is shown in Figure 3-11 (b). A TI designed BPFC controller is used [3.26]. It is a peak current controller and is implemented by a Digital Signal Processor (DSP). The AVG controller is a simple open-loop analog polarity detector with dead time circuits. It turns on S_A when v_G is a positive voltage and turns on S_B when v_G is a negative voltage. A 300 W resistive load bank is used and connected to the dc bus of the BFPC. The AVG capacitor, C_{AB}, value is chosen as 4.7 μF which is based on two criteria,

1. Maximum leakage current, there are some industrial standards to limit the leakage current to be suppressed to a certain level, such as 30 mA [3.27] and 7 mA [3.28], to protect equipment and human beings. And a typical stray capacitance (C_{CM}) for a PFC is about 5 nF [3.29]. Thus, according to the (3.3) and (3.7), the AVG capacitor value is limited by,

$$C_{\mathrm{AB}} \geq \frac{C_{\mathrm{CM}}}{\Delta \hat{\imath}_{\mathrm{HFCM}}} \frac{(V_{\mathrm{DC}} - \hat{V}_{\mathrm{G}})\hat{V}_{\mathrm{G}}}{V_{\mathrm{DC}} L_{\mathrm{X}} f_{\mathrm{sw}}} - C_{\mathrm{CM}}. \tag{3.11}$$

By the use of the circuit values from TABLE 3-I and setting the maximum leakage current as 7mA, the minimum capacitor value of C_{AB} is calculated as 2.32 μF based on (3.11).

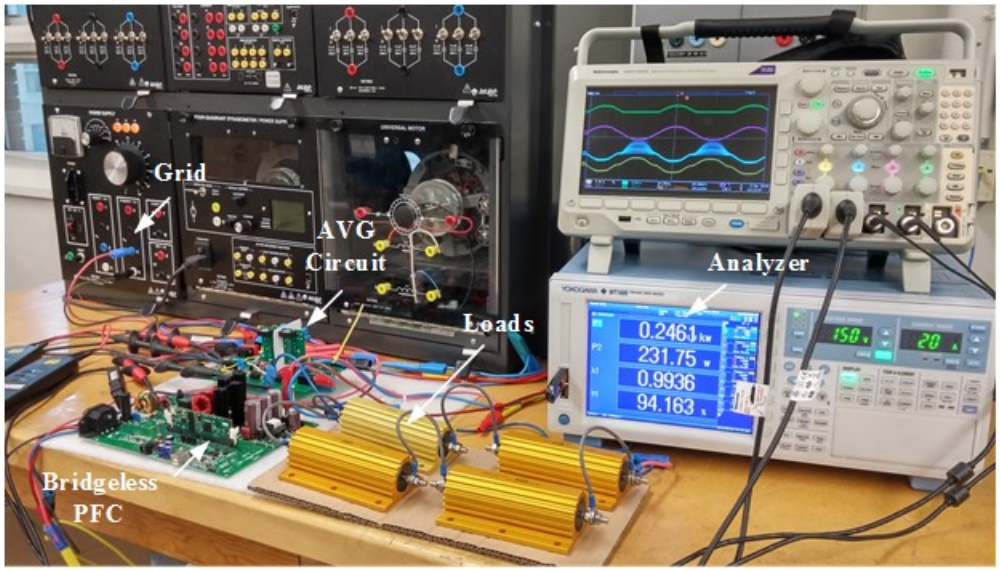
2. Maximum resonance frequency, in order to avoid the interferences between the resonance frequency and the switching frequency, at least 20 times difference is chosen. By using the (3.10), the AVG capacitor is limited by,

$$C_{\mathrm{AB}} \geq \frac{2}{L_{\mathrm{X}}} \left(\frac{20}{2\pi f_{\mathrm{sw}}} \right)^2. \tag{3.12}$$

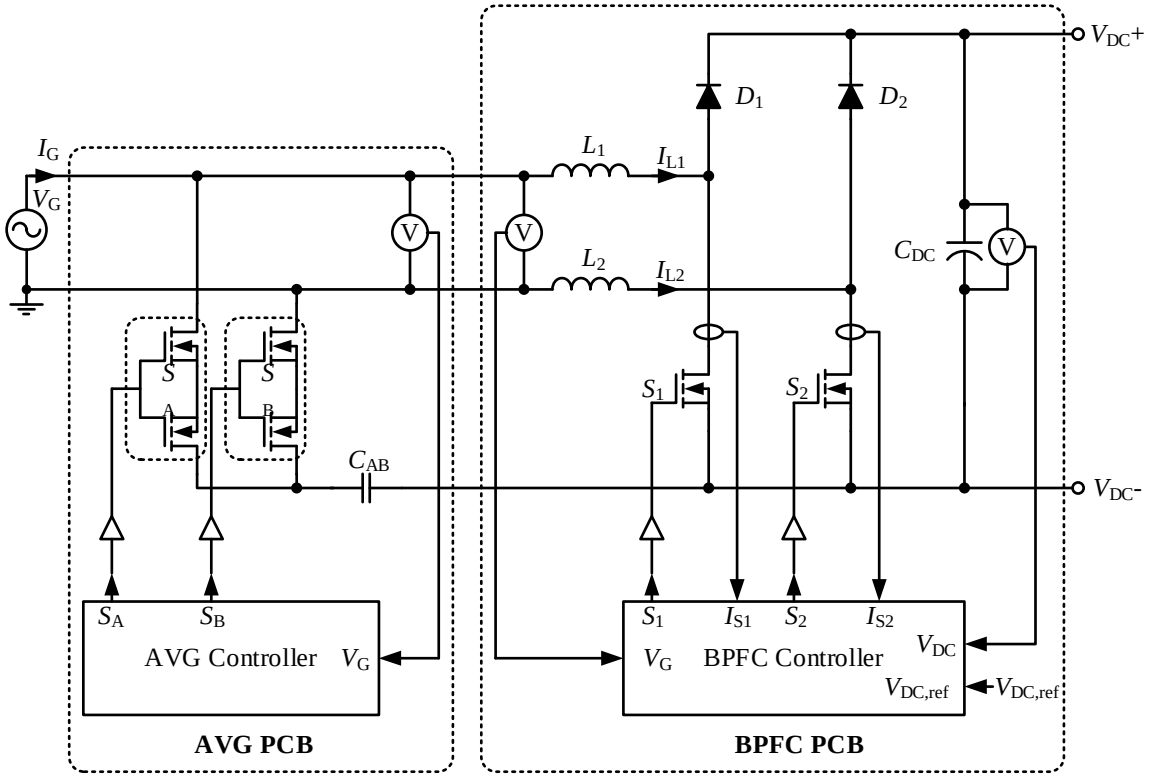
By putting the values from TABLE 3-I into (12), thus C_{AB} must be bigger than 3.37 μF for the frequencies interference point of value.

Thus, a standard value 4. 7 μF is chosen as the value of the AVG capacitor in the prototype which can be satisfied both of the above criteria.

Although the AVG circuit is implemented as an “add-on” circuit for a commercial BPFC for demonstrating the AVG circuit can change the conventional BPFC topology to the AVG-BPFC without any converter or system controller modifications, the AVG circuit also can be integrated into the BPFC when designing a new converter. All necessary signals for the AVG circuit will be outputted by the system DSP. In other words, it requires extra two semiconductor switches and their gate drivers, and an ac capacitor only.



(a)



(b)

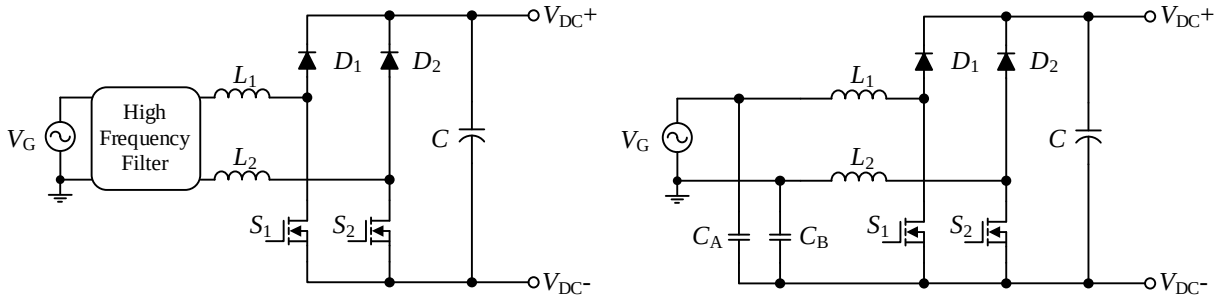
Figure 3-11. Experimental setup.

TABLE 3-I SPECIFICATION OF THE PROTOTYPE OF AVG-BPFC SYSTEM

Parameter	Value	Parameter	Value
v_G	120 V	V_{DC}	400 V
P_O	300 W	f_{sw}	200 kHz
L_1, L_2	150 μH	C_{AB}	4.7 μF

3.7 Experimental Verification

Performances of the built prototype are experimentally demonstrated in the section. In contrast, two other conventional HF DM and CM mitigation techniques, cascading a HF filter and capacitor-clamped circuit respectively, are compared experimentally. The schematics are shown in Figure 3-12.



(a) (b)

Figure 3-12. Conversional BPFCs with (a) high frequency filter, and (b) capacitor-clamped circuit.

A. DM and CM noises mitigating performance.

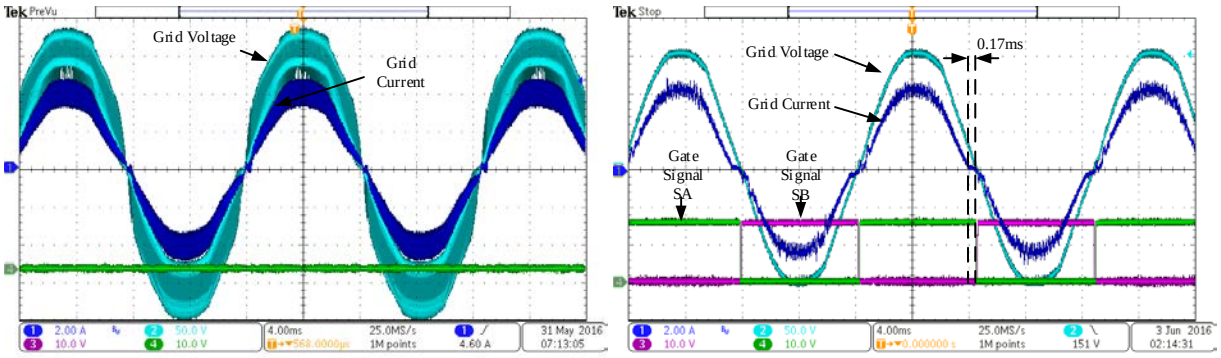
Figure 3-13 (a) and (b) show experimental results of the BPFC without and with the AVG circuit, respectively. It shows that the BPFC generates HF noise to interference the grid voltage

without the AVG circuit in Figure 3-13 (a) and the grid current ripple is large. It is improved significantly by adding the AVG circuit as shown in Figure 3-13 (b), the grid current ripple reduced and the grid voltage did not have interference since the filter becomes an *LCL* filter in the converter. And the switches in the AVG circuit are switching at low frequency (60 Hz) and synchronized with the grid voltage.

Figure 3-14 (a) to (d) show experimental results of the BPFC without and with different DM and CM noises mitigation methods. Figure 3-14 (a) shows that there is a huge HF CM voltage in the conventional BPFC. Besides, the grid current and inductor current are identical where HF current ripples are in both positive and negative half line cycles. The DM and CM noises affect the shape of the input voltage. Figure 3-14 (b) shows the BPFC operating with a cascaded HF filter which is shown in Figure 3-12 (a). The corresponding structure of the TI pre-installed HF filter is shown in Figure 3-15 [3.25]. The grid current quality is improved, a detailed explanation of the equivalent circuit model is given in Appendix E. However, the HF CM voltage remains large amplitude and it affects the grid voltage quality. Figure 3-14 (c) shows the BPFC with the capacitor-clamped circuit which is shown in Figure 3-12 (b) and was proposed in [3.16] where two 4.7 μF capacitors were used. The HF CM noise is minimized which can be seen by the CM voltage waveform, however, the gird current carries a HF DM current. The reason is that there are two HF paths (two capacitors) for high frequencies returning to the noise source. One of the paths is in series with the grid source, therefore, the HF noise appears in the grid current, a detailed explanation of the equivalent circuit model is given in the Appendix E. But in Figure 3-14 (d), it shows the HF CM voltage is minimized by the AVG circuit. And the inductor current has a large current ripple in the positive half line cycle, since the inductor acts as a converter-side inductor in the *LCL* filter. The inductor current has very small current ripple in the negative half line cycle, since the inductor acts as a grid-side inductor in the *LCL* filter. There is a low frequency CM

voltage in the results of the capacitor-clamped and the AVG BPFCs, since the grid voltage is in between the measurement points (Line terminal to negative terminal of dc link) during the positive half line cycle. But the low frequency CM voltage does not generate leakage current. Similarly, there is a HF CM voltage in the results of the capacitor-clamped and the AVG BPFCs. Those two techniques do not completely suspend the HF CM voltage, they reduce the voltage to an acceptable level to avoid generating high leakage current. The HF CM voltage amplitude of the capacitor-clamped and the AVG BPFCs are presented in (3.6) and (A3.12), respectively. Besides, the measured power factor of AVG-BPFC converter can achieve 0.9953.

The experimental results proved that the DM and CM noises of a BPFC converter can be improved at the same time by simply adding an AVG circuit in the front without any modification of the main circuit of BPFC and its controller.



(a) (b)

Figure 3-13. Experimental results, (a) conventional, and (b) with proposed circuit.

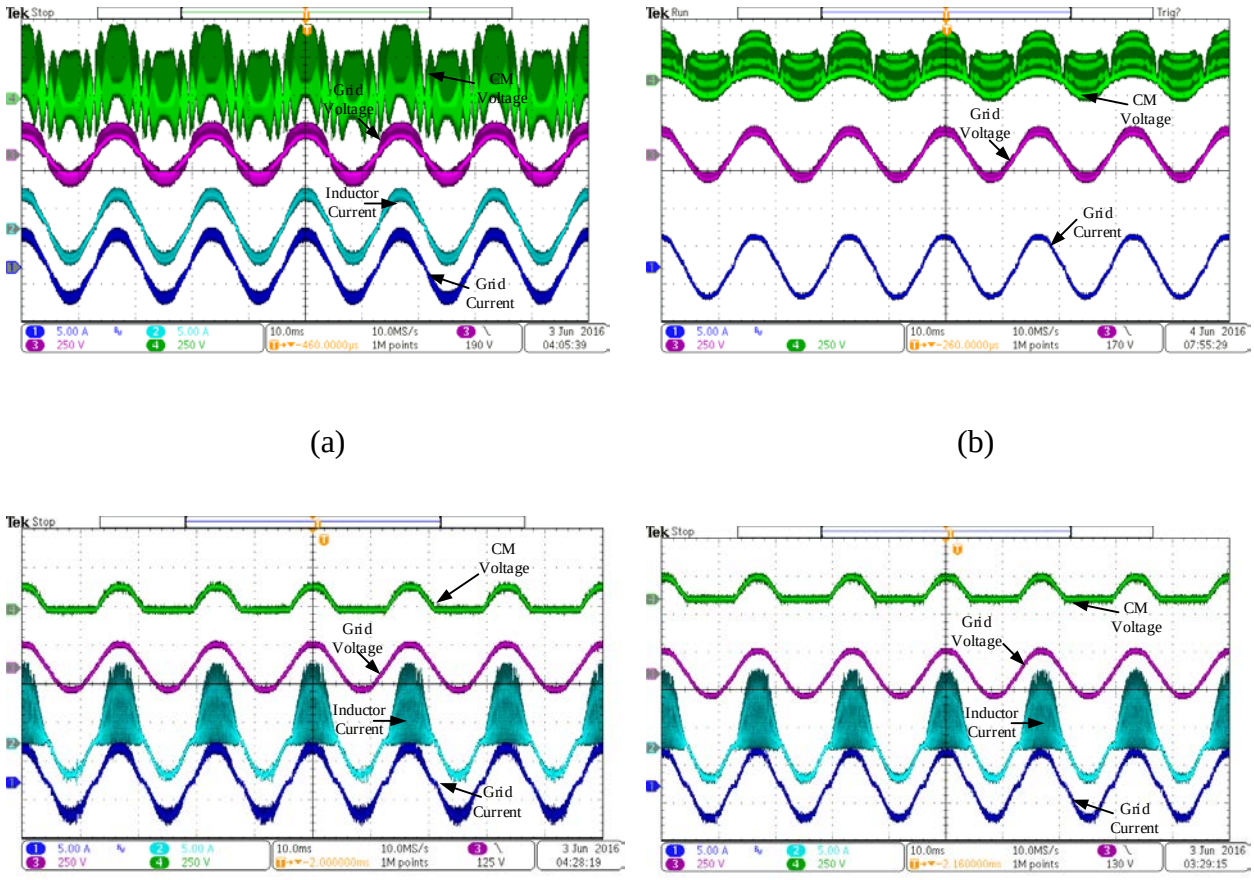


Figure 3-14. Experimental results, (a) conventional, (b) with HF filter, (c) with capacitor-clamped circuit and (d) with the proposed AVG circuit.

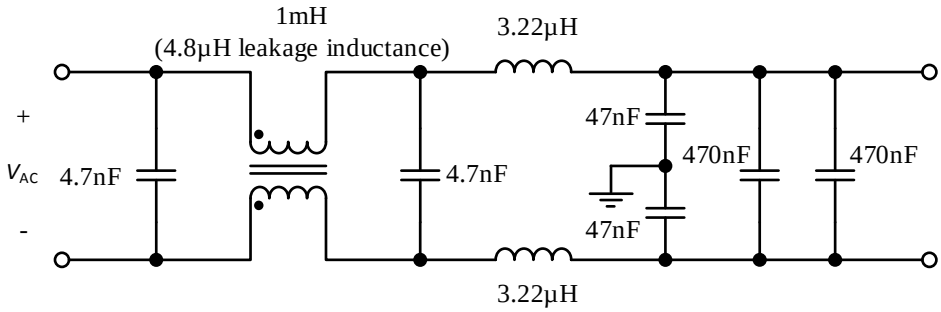
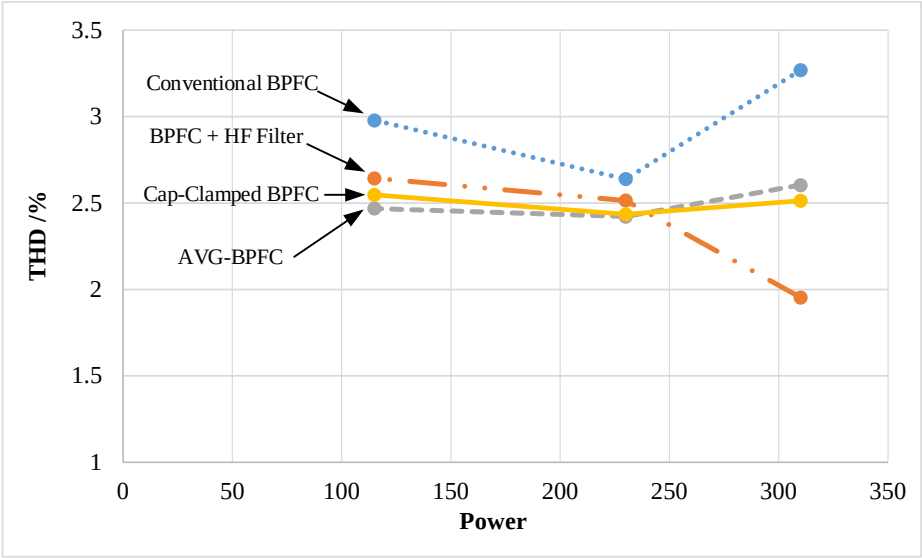


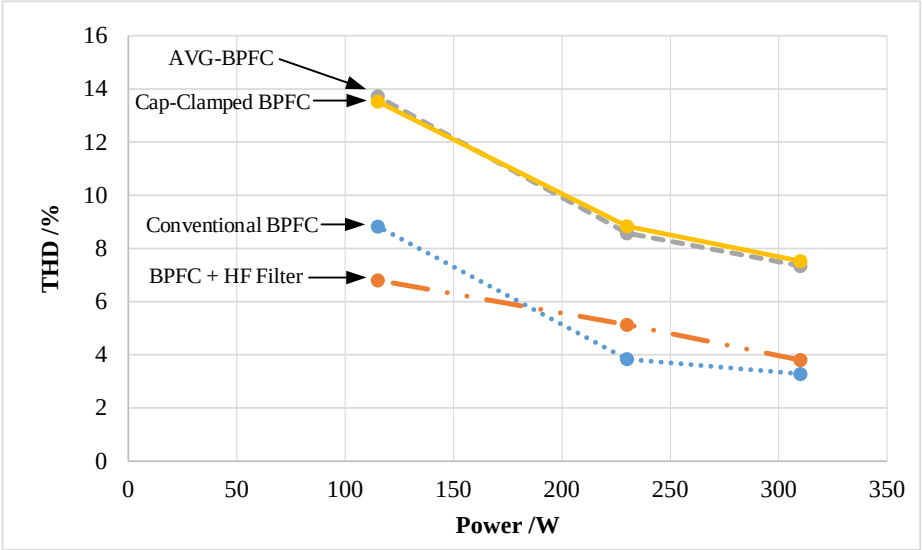
Figure 3-15. A high frequency filter for the BPFC [3.25].

B. Grid-side voltage quality and current quality

The grid current waveforms are shown in Figure 3-13 (b) appears a short dead zone (0.17 ms) at the zero crossing. This dead zone affects the grid current quality. The possible reason of generating that dead zone is the TI built-in controller is optimized for the original first-order filter, when the AVG circuit is applied, it forms a third-order *LCL* filter. The built-in controller controls the converter-side inductor current to be sinusoidal and in-phase with the grid voltage. Thus, the phase of the grid current is shifted due to the AVG capacitor, C_{AB}, contributing a reactive current. As a result, although the add-on AVG circuit improves the THD of grid voltage, which is shown in Figure 3-16 (a), due to lower CM voltage, it increases the THD of grid current due to the zero crossing distortion. Figure 3-16 shows a comparison of the THDs of different CM and DM noises mitigating approaches. The AVG-BPFC is measured as 7.3 % current THD at the full rated power, but all harmonics currents, which are shown in Figure 3-17, are under the limits in the industrial standard of IEC 61000-3-2:2001 [3.30]. It can be believed that the current distortion can be improved by using some recently proposed grid current control strategies [3.22], [3.31] - [3.33].



(a)



(b)

Figure 3-16. THDs for different BPFC topologies, (a) Grid voltage, and (b) Grid current.

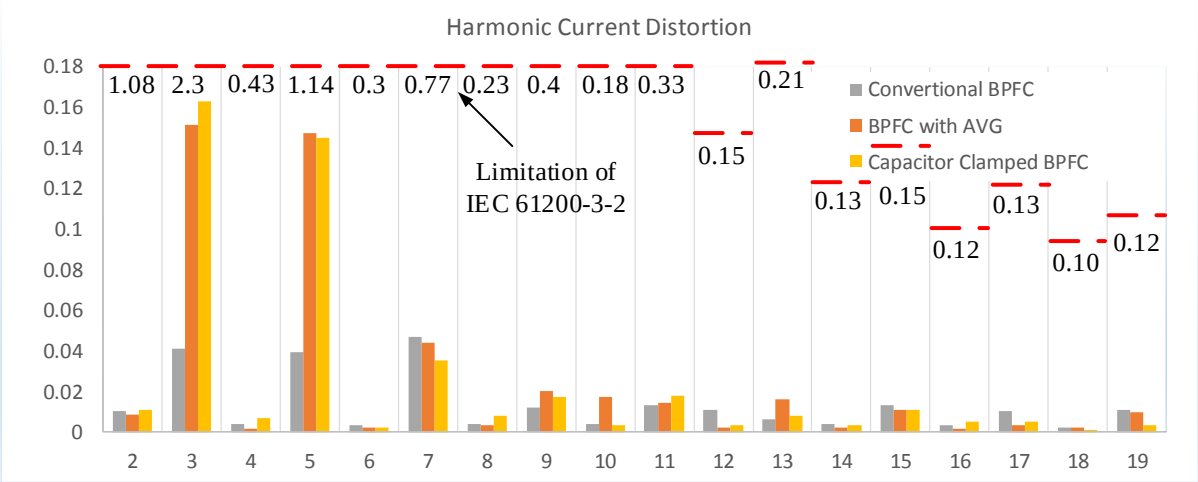


Figure 3-17. Measured current harmonics.

3.8 Conclusion

The chapter has presented a proposed topology of bridgeless PFC using Active Virtual Ground technology. The PFC guaranteed a small grid current ripple and a low HF leakage current. The concept is to use an additional low frequency switching circuit to reconfigure the built-in inductors of a BPFC to become an *LCL* filter, thus the grid current ripple is minimized. Furthermore, since the filtering capacitor connects in between the dc bus and one of the grid terminals by using the proposed AVG circuit, the HF common mode voltage is minimized. The switching states and the steady state characteristics of the proposed topology were explained in detail. A 120 V, 60 Hz, 300 W prototype has been built in order to verify the concept. The performance of the AVG-BPFC was demonstrated and compared to conventional BPFCs by experimental results. There is good agreement between theoretical analysis and experimental results.

Appendix

A. Derivation of (3.2)

The duty ratio of a boost converter with a time varying input voltage can be defined as,

$$D(t) = 1 - \frac{v_{\mathrm{C}}(t)}{V_{\mathrm{DC}}}. \tag{A3.1}$$

By using (A3.1) and (3.1), (3.2) can be obtained.

B. Derivation of (3.3)

The inductor charging characteristic is defined as,

$$v_{\mathrm{LC}} = L_{\mathrm{X}} \frac{di_{\mathrm{LC}}}{dt}. \tag{A3.2}$$

Assume that the switching frequency is much higher than the line frequency, i.e. $f_{\mathrm{sw}} > 1000 \cdot f$. When the main switch is turned on, the equivalent circuit is in Figure 3-4 (a), the current is charging up linearly, thus, (A3.2) can be changed as,

$$v_{\mathrm{LC}} = L_{\mathrm{X}} \frac{\Delta i_{\mathrm{LC}}}{T_{\mathrm{ON}}}, \tag{A3.3}$$

where T_{ON} is the turn-on period in a switching cycle.

By using duty ratio D and switching frequency f_{sw} to replace T_{ON} in (A3.3), the converter-side current ripple can be found,

$$\Delta i_{\mathrm{LC}}(t) = \frac{v_{\mathrm{C}}(t)D(t)}{L_{\mathrm{X}} f_{\mathrm{sw}}}. \tag{A3.4}$$

It shows that the current ripple size is time varying in a line cycle. And by putting (3.1) and (3.2) into (A3.4), (3.3) can be obtained.

C. Derivation of (3.4)

The capacitor voltage ripple peak to peak value is defined as,

$$\Delta v_{\mathrm{C}} = v_{\mathrm{C,max}} - v_{\mathrm{C,min}} = \frac{1}{C_{\mathrm{AB}}} \int_0^{T_{\mathrm{S}}/2} i_{\mathrm{C}}(t)dt, \tag{A3.5}$$

where i_{C} is the current of AVG capacitor, and T_{S} is the switching period.

The capacitor voltage ripple is basically contributed by the converter-side inductor current and it is a triangular waveform, thus (A3.5) can be modified with the triangle area equation.

$$\Delta v_{\mathrm{C}} = \frac{T_{\mathrm{S}} \cdot \Delta i_{\mathrm{LC}}}{8C_{\mathrm{AB}}} \tag{A3.6}$$

By putting (A3.4) into (A3.6),

$$\Delta v_{\mathrm{C}}(t) = \frac{v_{\mathrm{C}}(t)D(t)}{8C_{\mathrm{AB}}L_{\mathrm{X}}f_{\mathrm{sw}}^2}. \tag{A3.7}$$

It shows that the voltage ripple size is time varying in a line cycle. And by putting (1) and (2) into (A3.7), (3.4) can be obtained.

D. Derivation of (3.5)

The grid current ripple peak to peak value is defined as,

$$\Delta i_{\mathrm{G}} = i_{\mathrm{G,max}} - i_{\mathrm{G,min}} = \frac{1}{L_{\mathrm{X}}} \int_0^{T_{\mathrm{S}}/2} v_{\mathrm{LG}}(t)dt, \tag{A3.8}$$

where v_{LG} is the grid inductor voltage.

The grid current ripple is basically contributed by the AVG capacitor voltage and it is close to a sinusoidal waveform, thus (A3.8) can be modified as,

$$\Delta i_{\mathrm{G}} = \frac{1}{L} \frac{\Delta v_{\mathrm{C}}}{2} \int_0^{T_{\mathrm{S}}/2} \sin 2\pi f_{\mathrm{sw}} t \, dt, \tag{A3.9}$$

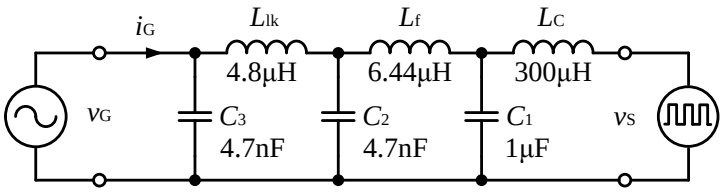
$$\Delta i_{\mathrm{G}}(t) = \frac{\Delta v_{\mathrm{C}}(t)}{2\pi L_{\mathrm{X}} f_{\mathrm{sw}}}. \tag{A3.10}$$

It shows that the current ripple size is time varying in a line cycle. And by putting (3.4) into (A3.10), (3.5) can be obtained.

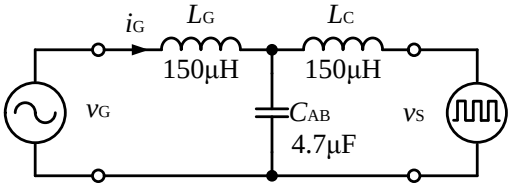
E. Discussion of Filter Response

The built-in TI HF filter, which is shown in Figure 3-15, is using a two-stage HF filter. From DM performance point of view, the HF filter is a high-order filter, the equivalent circuit with measured values are shown in Figure 3-18 (a). The transfer function of the filter is,

$$G_{\mathrm{AVG}}(\mathrm{s}) = \frac{-i_{\mathrm{G}}(\mathrm{s})}{u_{\mathrm{S1/S2}}(\mathrm{s})} = \frac{-1}{L_{\mathrm{c}}L_{\mathrm{f}}L_{\mathrm{lk}}C_1C_2\mathrm{s}^5 + C_2L_{\mathrm{lk}}(L_{\mathrm{f}}+L_{\mathrm{c}})\mathrm{s}^3 + C_1L_{\mathrm{c}}(L_1+L_{\mathrm{f}})\mathrm{s}^3 + (L_1+L_{\mathrm{f}}+L_{\mathrm{c}})s}. \tag{A3.11}$$



(a)



(b)

Figure 3-18. Filter structures, (a) HF filter in conventional BPFC, and (b) AVG filter.

However, the AVG circuit is a single stage third-order *LCL* filter which is integrated into the converter, the equivalent circuit with measured values are shown in Figure 3-18 (b), and the transfer function is in (3.9). Figure 3-19 shows the frequency response of two filter configurations.

It shows that the filtering performances of both filters are quite similar, the crossover frequencies are both at 3.3 krad/s (or 525 Hz). Thus, grid current ripple amplitude of the BPFC with the HF filter is similar to that of the AVG circuit in Figure 3-14 experimental results.

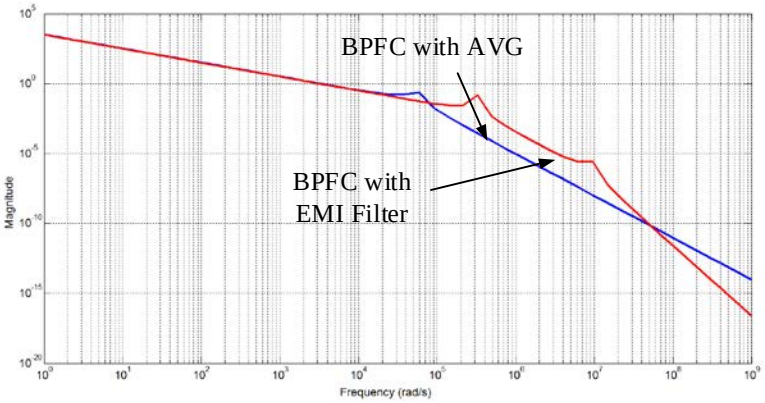


Figure 3-19. Filter performance in the DM circuit.

F. Discussion of Capacitor-Clamped Circuit

The capacitor-clamped circuit gives slightly higher measured efficiency (94 % and 93.8 % for the capacitor-clamped and the AVG circuits, respectively) and effectively mitigates the CM voltage and, but it consists of large current ripple in the grid current which is shown in the experimental results in Figure 3-14. The steady state characteristics are studied in this section. Figure 3-20 shows the positive half line cycle HF equivalent circuit of the BFFC with the capacitor-clamped circuit which is in Figure 3-12 (b). The capacitors C_A and C_B are in parallel in the structure to clamp the CM voltage, V_{CM}, and they share the same HF DM current. However, the HF DM current path of C_B is in series of the gird source, thus the ripple of grid current is the same as the current go through C_B. In principle, the grid current ripple is half of the inductor current ripple Δi_{LC}. Thus, the capacitor-clamped circuit consists of larger current ripple in the grid current comparing to AVG circuit. And it is the disadvantage of the capacitor-clamped circuit.

The CM voltage is similar to the AVG model in (3.6), since two capacitors are in parallel, the equation is,

$$\Delta v_{\mathrm{CM}}(t) = \frac{(V_{\mathrm{DC}} - V_{\mathrm{G}} \sin \omega t) V_{\mathrm{G}} \sin \omega t}{8 V_{\mathrm{DC}} (C_{\mathrm{A}} + C_{\mathrm{B}} + C_{\mathrm{CM}}) L_{\mathrm{X}} f_{\mathrm{sw}}^2}. \tag{A3.12}$$

Similarly, the HF leakage current can be obtained by,

$$\Delta i_{\mathrm{HFCM}}(t) = \frac{C_{\mathrm{CM}}}{C_A + C_{\mathrm{B}} + C_{\mathrm{CM}}} \Delta i_{\mathrm{LC}}(t). \tag{A3.13}$$

By comparing (3.6) and (A3.12), and (3.7) and (A3.13), and assuming $C_{\mathrm{A}} = C_{\mathrm{B}} = C_{\mathrm{AB}}$, the CM voltage and leakage current of the capacitor-clamped circuit is half of the AVG circuit. However, the advantage is not significant since both systems are within the leakage current limit. And the CM voltage mitigating capability of the AVG circuit can simply increase the value of AVG capacitor, C_{AB}. But it is not easy to reduce the grid current ripple of the capacitor-clamped circuit since it requires a front stage HF filter or bulky boost inductors.

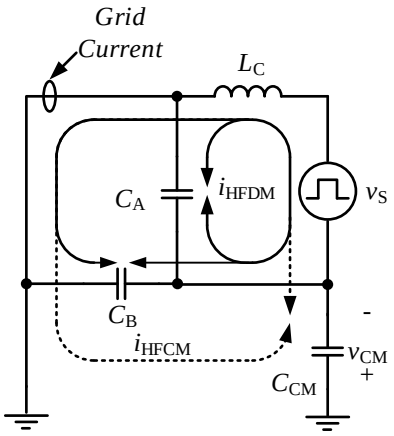


Figure 3-20. HF equivalent circuit of a BPFC with capacitor-clamped circuit.

Reference

[3.1] J. Y. Lee, Y. M. Chang, and F. Y. Liu, “A new UPS topology employing a PFC boost rectifier cascaded high-frequency tri-port converter,” *IEEE Trans. Ind. Electron.,* vol. 46, no. 4, pp. 803-813, Aug. 1999.

[3.2] J. Y. Chai and C. M. Liaw, “Development of a switched-reluctance motor Drive with PFC front end,” *IEEE Trans. Energy Conversion.,* vol. 24, no. 1, pp. 30-42, Mar. 2009.

[3.3] Y. Cho and J. S. Lai, “Digital Plug-In Repetitive Controller for Single-Phase Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 165-175, Jan. 2013

[3.4] V. Bist and B. Singh, “PFC Cuk Converter-Fed BLDC Motor Drive,” *IEEE Trans. Power Electron.*, vol. 30, no. 2, pp. 871-887, Feb. 2015

[3.5] J. H. Kim, I. O. Lee, and G. W. Moon, “Integrated Dual Full-Bridge Converter With Current-Doubler Rectifier for EV Charger,” *IEEE Trans. Power Electron.,* vol. 31, no. 2, pp. 942-951, Feb. 2016

[3.6] J. Y. Lee and H. J. Chae, “6.6-kW Onboard Charger Design Using DCM PFC Converter With Harmonic Modulation Technique and Two-Stage DC/DC Converter,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 3, pp. 1243-1252, March 2014

[3.7] F. J. Azcondo, F. J. Díaz, C. Brañas, and R. Casanueva, “Microcontroller power mode stabilized Power Factor Correction stage for high intensity discharge lamp electronic ballast,” *IEEE Trans. Power Electron.,* vol. 22, no. 3, pp. 845-853, May 2007.

[3.8] D. M. Mitchell, “AC-DC Converter having an improved power factor,” *US Patent,* No. US4412277 A, 25/10/1983.

[3.9] L. Huber, Y. Jang, and M. M. Jovanovic, “Performance Evaluation of Bridgeless PFC Boost Rectifiers,” *IEEE Trans. Power Electron.*, vol. 23, no. 3, pp. 1381-1390, May 2008.

[3.10] A. F. de Souza and I. Barbi, “High power factor rectifier with reduced conduction and commutation losses,” in *Proc. Telecommunication Energy Conference*, Jun. 1999.

[3.11] A. Maejima, T. Igarashi, and Y. Kato, “Power conversion apparatus and air conditioner using the same,” *US Patent*, No. US6181539 B1, 30/01/2001.

[3.12] M. Xu and Q. L. Chen, “AC-to-DC conversion apparatus and related control manner thereof,” *US Patent*, No. US8780597 B2, 15/07/2014.

[3.13] Y. Jang and M. Jovanovic, “A bridgeless PFC boost rectifier with optimized magnetic utilization,” *IEEE Trans. Power Electron*., vol. 24, no. 1, pp. 85-95, Jan. 2009.

[3.14] H. Mao, D. Fu, and B. Cai, “High efficiency bridgeless PFC converter and method,” *US Patent*, No. US 8385032 B1, 26/02/2013.

[3.15] M. A. Liquicia, C. T. Liang, N. V. Tangonan, and W. R. Apuang, “Commutator for bridgeless PFC circuit,” *US Patent*, No. US8576597 B2, 05/11/2013.

[3.16] M. Soldano and B. Lu, “EMI noise reduction circuit and method for bridgeless PFC circuit,” *US Patent*, No. US7215560 B2, 08/05/2007.

[3.17] R. Yamada, “Power conversion apparatus,” *US Patent*, No. US8432710 B2, 30/04/2013.

[3.18] K. D. Wildash, “Bridgeless boost PFC circuits and systems with reduced common mode EMI,” *US Patent*, No. US8289737 B2, 16/10/2012.

[3.19] R. T. H. Li and C. N. M. Ho, “Active Virtual Ground: Single Phase Grid-Connected Voltage Source Inverter Topology,” in *Proc. IEEE APEC16*, pp. 2905-2911, Mar. 2016.

[3.20] N. M. Ho and T. H. Li, “Bridgeless power factor correction circuit,” *US Patent*, No. US9093917 B2, 07/28/2015.

[3.21] J. H. R. Enslin, M. S. Wolf, D. B. Snyman, and W. Swiegers, “Integrated photovoltaic maximum power point tracking converter,” *IEEE Trans. Industrial Electron.*, vol. 44, no. 6, pp. 769-773, Dec. 1997.

[3.22] G. Escobar, S. Pettersson, and C. N. M. Ho, “Control of single-phase inverter connected to the grid through an LCL filter,” in *Proc. IECON 2012*, pp. 3406-3411, Oct. 2012.

[3.23] W. Wu, Y. He, T. Tang, and F. Blaabjerg, “A New Design Method for the Passive Damped LCL and LLCL Filter-Based Single-Phase Grid-Tied Inverter,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 10, pp. 4339-4350, Oct. 2013.

[3.24] “Digitally Controlled Bridgeless Power Factor Correction (BL PFC) Converter Using C2000 Piccolo-A Microcontroller,” *Texas Instruments Application Report*, No. TIDU312, May 2014.

[3.25] “TI Designs: Bridgeless Power Factor Correction Converter,” *Texas Instruments Application Report*, No. TIDU672, Dec. 2011.

[3.26] B. Novak, “Implementing peak current mode control of a switch-mode power supply with a single microcontroller,” *Texas Instruments White Paper*, July 2012.

[3.27] *Safety of Power Converters for Use in Photovoltaic Power Systems—Part 1: General Requirement*, IEC Standard 62109-1-2007, 2007.

[3.28] *Effects of current on human beings and livestock – Part 1: General Aspects*, IEC Standard 60479-1-2005, 2005.

[3.29] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, “Leakage Current Reduction in a Single-Phase Bidirectional AC–DC Full-Bridge Inverter,” *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4281-4291, Oct. 2012.

[3.30] *Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤16 A per phase)*, IEC Standard 61000-3-2-2001, 2001.

[3.31] J. Dannehl, C. Wessels, and F. W. Fuchs, “Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers With LCL Filters,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 380-388, Feb. 2009.

[3.32] S. Y. Park, C. L. Chen, J. S. Lai, and S. R. Moon, “Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter,” *IEEE Trans. Power Electron.*, vol. 23, no. 4, pp. 1716-1723, July 2008.

[3.33] Y. He, H. S. H. Chung, C. N. M. Ho, and W. Wu, “Use of Boundary Control With Second-Order Switching Surface to Reduce the System Order for Deadbeat Controller in Grid-Connected Inverter,” *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2638-2653, Mar. 2016.

Chapter 4 Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC

The work described in this chapter was published in the following paper: K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, "Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3921-3936, April 2019. The work was also presented in part as a conference paper at the IEEE Applied Power Electronics Conference and Exposition 2017 [4.1].

4.1 Abstract

The chapter presents a new digital control scheme for Active Virtual Ground-Bridgeless PFC (AVG-BPFC) which is able to obtain an optimized solution between the system efficiency and Electromagnetic Interference (EMI) performance in the PFC stage. From the topology structure of AVG-BPFC, a resonant characteristic is generating from the input *LCL* filter structure of the converter. In addition, there is a phase difference between two inductor currents which also leads the controller design in the AVG-BPFC to become challenging, especially on the system stability and the current quality. Thus, a triple loop control's architecture together with an integrated state machine is proposed as the control methodology of the AVG-BPFC. Under the simple control structure in the digital platform, a stable system is achieved together with a precise grid current tracking function. Such control scheme was implemented digitally on a 1.5 kW prototype. In the chapter, theoretical models of the whole system were analysed and the system performance was

successfully verified in both steady state and transient state conditions. The experimental results showed a good agreement with the theoretical knowledge.

4.2 Introduction

Nowadays, a PFC converter is usually applied to the system front stage due to the power quality requirement. The wireless power transfer (WPT) system of Electric vehicle (EV) and hybrid electric vehicle (HEV) are the typical examples of the PFC stage applications [4.2] - [4.4]. In the EV system, battery power management is very crucial as it directly links with vehicle safety and battery lifetime. Therefore, many design requirements and industrial standards are needed to follow by the WPT system. Under the standard IEC 61980-1 [4.5] and the SAE J2954 [4.6], the efficiency requirements of the overall WPT system need to be higher than 85 %. In addition, the system is required to pass the CISPR 11 [4.7] in the EMI performance test. To fulfill efficiency standards, bridgeless PFC (BPFC) is widely preferred in the PFC stage. However, a large EMI filter is required to suppress the common-mode (CM) noise generated from the BPFC system in order to achieve the industry requirements on the EMI standard. Another alternative solution is to apply a CM noise mitigation topology to solve the CM noise issue [4.8].

The recently proposed Active Virtual Ground-Bridgeless PFC (AVG-BPFC) topology [4.9], [4.10], as shown in Figure 4-1, can achieve the above criteria by providing both low leakage current and high energy efficiency in the PFC stage. The AVG-BPFC takes the optimized point between the conventional PFC and the BPFC. The AVG-BPFC adopts the advantage of the BPFC, which is that there are only two semiconductors conducted in the main current path in each switching action. In addition, based on the operation structure, an *LCL* filter is formed at the input side. The filter capacitor clamps the high frequency (HF) voltage ripple in the circuit parasitic capacitor,

therefore, the leakage current flowing back into the earth is minimized [4.9].

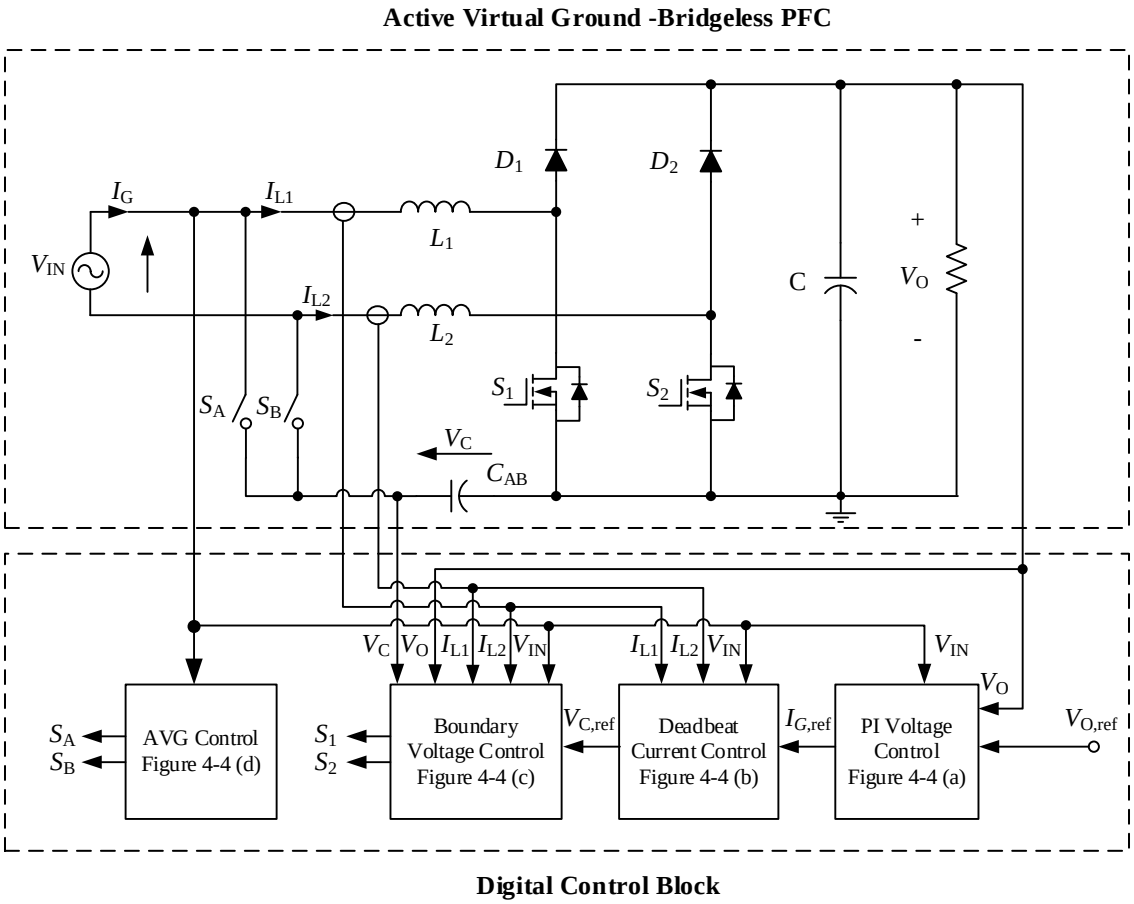


Figure 4-1. The proposed control scheme in AVG-BPFC.

In the AVG-BPFC, an *LCL* input filter structure is formed. There are two key main issues that should be considered in designing the controller. They are the phase shift properties and the resonant characteristics [4.9]. Firstly, there is a phase difference between the converter-side inductor and grid-side inductor. In AVG-BPFC, it is insufficient to use a single current detection control in ensuring system stability and performance characteristics. If only the converter-side inductor current is under control, the input power factor will be deteriorated due to the filter phase shift. If only the grid-side inductor current is under control, an unstable current may appear in the converter-side unless a further control block is added [4.11]. Thus, two current sensors for sensing

the two filter inductor currents are needed. Secondly, the high-order filter structure exhibits a resonant characteristic in the AVG-BPFC. Thus, the design of linear control over a wide operating range becomes a challenge. In the PFC stage, PI control is a well-known control methodology which is in simple structure and fewer sensor requirements. In order to alleviate the resonant characteristic of the *LCL* filter, an active damping method is generally adopted into the PI control [4.11] - [4.14]. However, in the digital implementation, the sampling-and-processing delay time in digital control would restrict the control bandwidth and thereby the input power factor and the current THD are deteriorated. On the other hand, non-linear control such as hysteresis and sliding mode control are also commonly applied to the PFC state which can offer stable performance over a wide range of operations. However, the system performance may still be distorted during the light load condition and some large signal transient conditions [4.15], [4.16]. Therefore, to maximize the system performance and to maintain the system stability under different operation conditions, a new system control scheme is required for the new operational characteristics.

An advanced control scheme is proposed in this chapter to fulfill the high quality grid current and the good system stability requirements on the AVG-BPFC. In contrast to [4.9], 1) an high power integrated AVG-BPFC system (1.5 kW) is built instead of using the add-on circuit (300 W) as shown in [4.9] in order to have a better circuit design and effective utilization of controller; 2) grid-side inductor current control associating with the proposed non-linear control methodology instead of the converter-side current control using a conventional linear controller to achieve the purpose of high quality grid current. A triple loop control architecture is built in the digital controller. In the inner loop control, a fast boundary controller with second-order switching surface [4.16] - [4.20] is implemented to eliminate the filter resonance in the transfer characteristic and to control the ac voltage. The second-order boundary control is applied to the input stage of the boost-

type rectifier under unipolar switching schemes with high sampling frequency. A state machine is integrated into the control loop to solve the zero crossing problem due to the discontinuous mode operation. Thus, both continuous conduction mode and discontinuous conduction mode operation are covered in the controller design and offer accuracy switching signals. The mid-loop is a deadbeat current controller [4.21] - [4.23] which offers high quality input current to enhance the input power factor and reduces the THD. In the outer loop, a PI controller aims to regulate the system output voltage. The approach can keep the advantages of the topology of AVG-BPFC in terms of low leakage current and small magnetic components, and furtherly improve the grid current quality and the system stability. The whole system stability was analyzed with the use of the small signal modelling which demonstrated how the resonant issue in the AVG input filter can be eliminated and the improvement of the power quality. A design guideline was provided for the proposed multi-control loop system. Such integrated control is applied digitally to deal with the complicated control scheme. A 1.5 kW AVG-BPFC prototype was implemented to verify the control scheme. Experimental results are in close agreement with theoretical predictions.

4.3 System Configuration

4.3.1 Review of AVG-BPFC Topology

Compared to the traditional BPFC, two additional low-frequency-bidirectional switches, S_A and S_B, and one additional filter capacitor, C_{AB}, are added in order to the form the AVG-BPFC. The circuit structure of the AVG-BPFC [4.9] is symmetrical in both positive and negative line cycles. The corresponding equivalent circuit in the positive half line cycle and the negative half line cycle are shown in Figure 4-2 (a) and (b) respectively. Under the unipolar switching method,

as shown in Figure 4-3 (a), only one switch is in high-frequency switching through the system operation. In the positive cycle, as shown in Figure 4-2 (a), the switches S_A and S_2 are kept ON and the switch S_1 is switched at HF. C_{AB} is linked to the Line of ac grid, the inductor L_1 becomes the converter inductor and the inductor L_2 acts as the grid-side inductor. An *LCL* filter structure is formed at the converter input. Likely, in the negative cycle, Figure 4-2 (b), the switches S_B and S_1 are kept ON and the switch S_2 is switched at HF. C_{AB} is connected to the Neutral of the ac grid and forms another *LCL* filter structure. L_1 becomes the grid inductor and L_2 acts as the converter-side inductor. The converter-side HF current is looped inside the converter through C_{AB}. Therefore, less ripple current appears in the grid-side inductor. The capacitor voltage and current waveform are shown in Figure 4-3 (b).

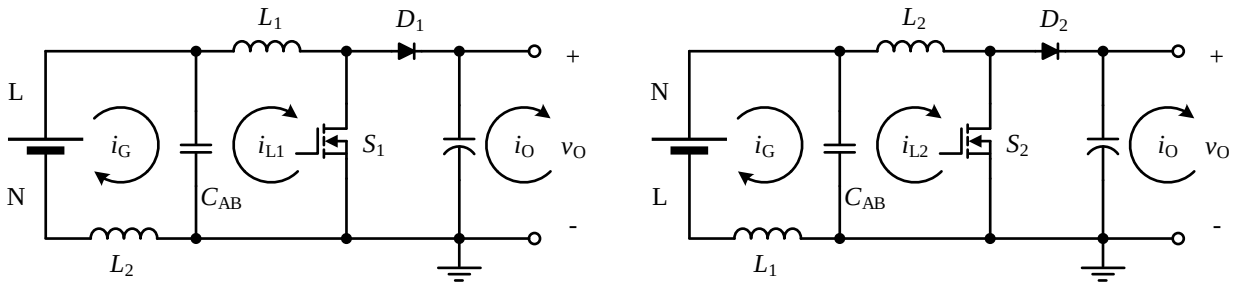
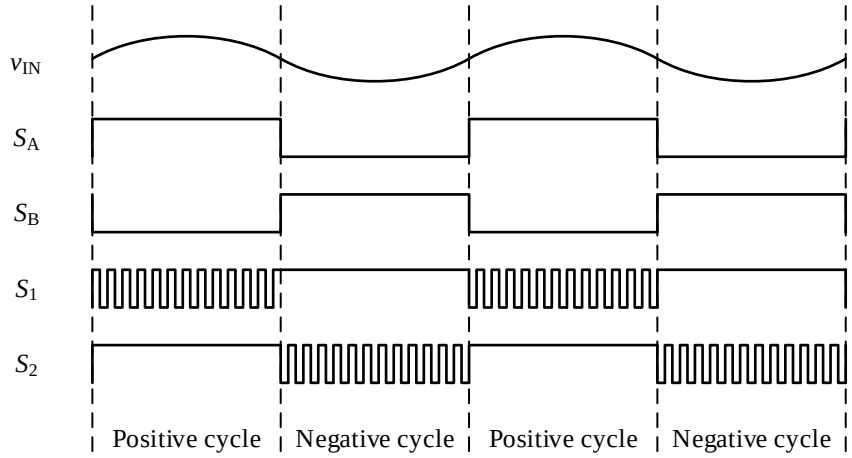
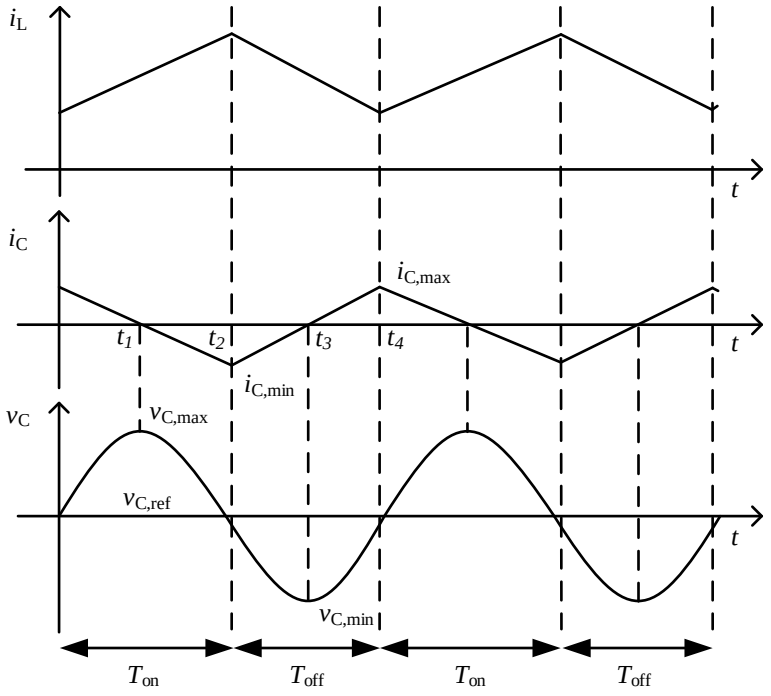


Figure 4-2. Equivalents circuit of AVG-BPFC in (a) positive line cycle and (b) negative line cycle.

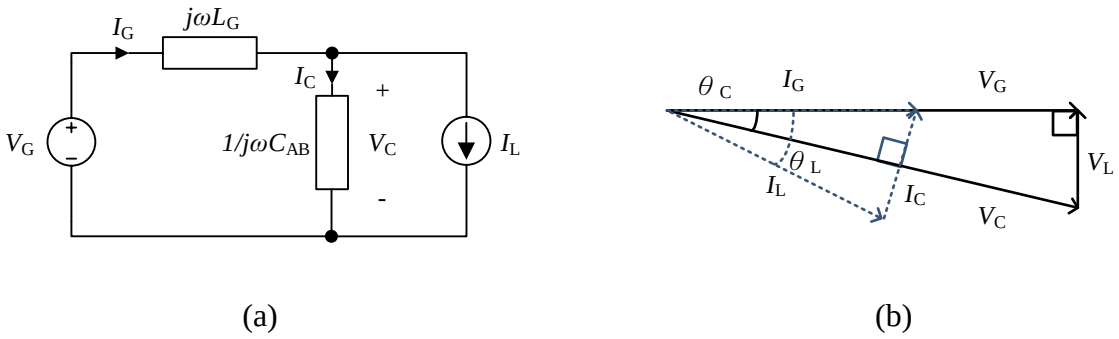


(a)



(b)

Figure 4-3. Key waveforms of AVG-BPFC's (a) switches operational sequence and (b) capacitor switching behaviors.



(a) (b)

Figure 4-4. AVG-BPFC's (a) phasor domain equivalent circuit and (b) the corresponding vector diagram.

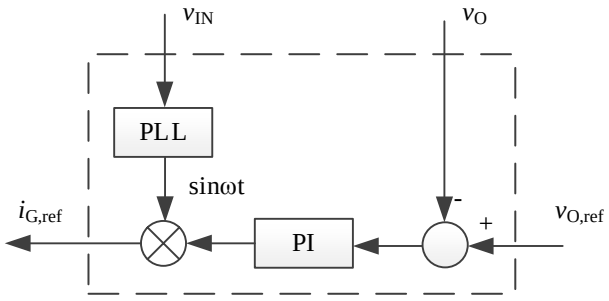
The reconfigurable *LCL* structure can help to filter out the switching frequency components in the grid current loop. Thus, both the grid-side current ripple and the corresponding DM noise are reduced. Due to the filter capacitor clamping the potential difference between the ac power source and the ground, CM noise is able to be minimized. Therefore, the large leakage current issue commonly appear in the traditional bridgeless PFC can be solved. Finally, the overall size of the EMI filter can be minimized in size and further optimized on the system CM and DM noises behavior.

It can be noticed from the *LCL* filter characteristic, there is a phase shift generated between the grid current and the inductor current at the input stage. A line frequency phasor domain equivalent circuit of the AVG-BPFC is formed in Figure 4-4 (a) to further elaborate the phase shift issue. Due to the symmetrical structure of the AVG-BPFC, the equivalent circuits of Figure 4-2 can be combined together and modified to Figure 4-4 (a). This can be done by changing the converter state into a continuous current source and transferring the system from the time domain into the phasor domain. In addition, a corresponding phasor diagram is shown in Figure 4-4 (b). The capacitor voltage is lagging behind the grid voltage in a relatively small angle, θ_C, due to the small impedance on between them. In addition, the inductor current is also lagging behind the grid

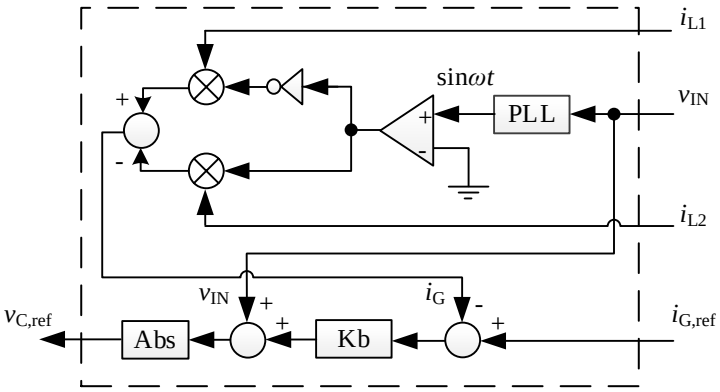
current with a phase angle, θ_L. Especially, at light load condition the phase angle between both inductor current is very significant. Therefore, it becomes one of the concern during the controller design of the AVG-BPFC.

4.3.2 Control Scheme

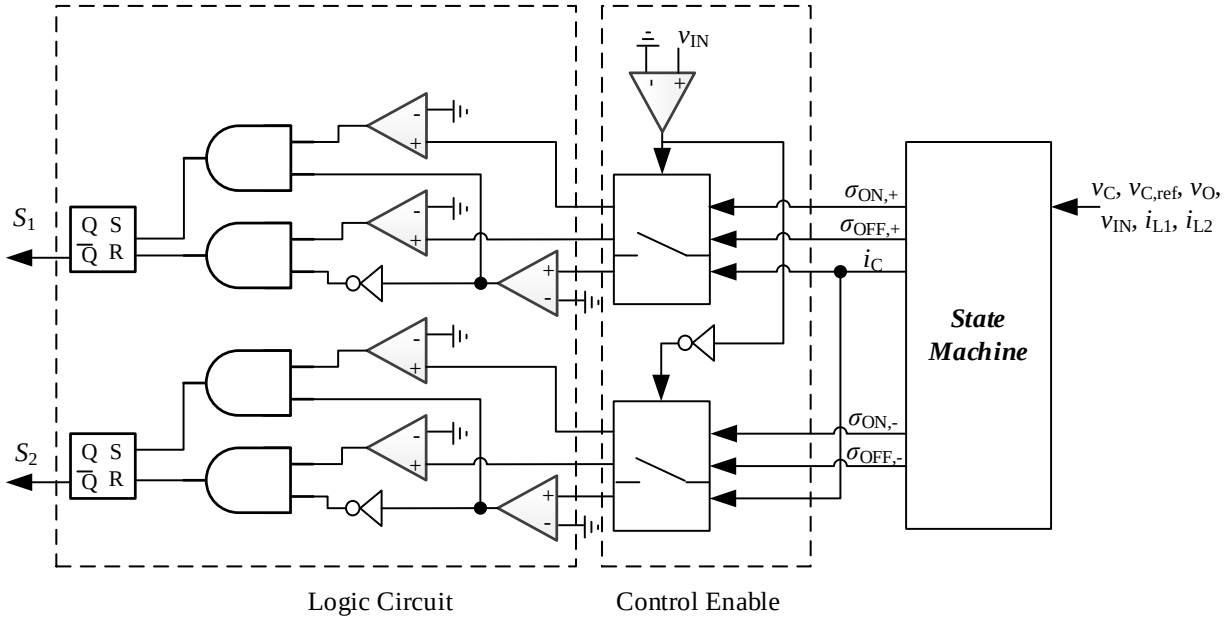
For the proposed control, three sets of voltage sensors are implemented on the system as shown in Figure 4-1. The voltage sensors sense for the input voltage, v_{IN}, filter capacitor voltage, v_C, and output voltage, v_O, respectively. In addition, two sets of current sensors are used to measure the currents of the inductor L_1 and L_2, as $i_{L1}$and i_{L2} separately. The detailed block diagrams of the proposed triple loop control architecture are shown in Figure 4-5. The outer loop is a PI controller, the middle loop is a deadbeat controller and the inner is a second-order boundary control loop. The logic flows of the proposed triple loop control architecture are shown in Section 4.4.3.



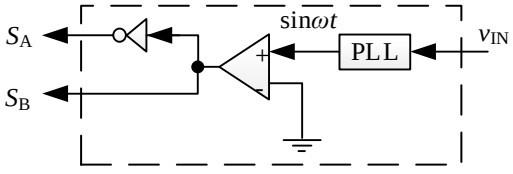
(a) PI Voltage Control



(b) Deadbeat Current Control



(c) Boundary Voltage Control



(d) S_A/S_B Control

Figure 4-5. Flow chart of the control diagram.

In the outer loop of the proposed control scheme, the PI controller is aimed to regulate the output voltage to the target output voltage, $v_{\mathrm{O,ref}}$, at a relatively slow speed. The corresponding control block diagram is shown in Figure 4-5 (a). During the dynamic change in the loading value, the rate change of the grid current is limited by the speed of the outer loop. Thus, the output voltage fluctuation level is well controlled within the targeting operation range. The output of the controller is a grid current reference, $i_{\mathrm{G,ref}}$.

A deadbeat controller is adopted as the middle loop to control the grid current, i_{G}. Under the deadbeat control, the phase shift issue which appears in [4.9] can be solved. The control block diagram is shown in Figure 4-1 and the corresponding logic flow is shown in Figure 4-5 (b). As the function of L_1 and L_2 is interchanged in each cycle, each of them only has half line cycle acting as grid inductor. The grid current information is formed with the positive cycle current in L_2 and negative cycle current in L_1. By using the simple control structure, both fast dynamic current tracking function and high quality input current are achieved. The output of the controller is a filter capacitor voltage reference, $v_{\mathrm{C,ref}}$. In order to linearize the relationship between the grid current and the filter capacitor voltage reference, forward Euler method is applied in the digital control platform to derive the deadbeat controller theory. The equation is found as,

$$v_{\mathrm{C,ref}}[\mathrm{n}] = v_{\mathrm{G}}[\mathrm{n}] + K_{\mathrm{c}}\big(i_{\mathrm{G,ref}}[\mathrm{n}] - i_{\mathrm{G}}[\mathrm{n}]\big), \tag{4.1}$$

where $K_{\mathrm{C}} = -\frac{L_{\mathrm{g}}}{T_{\mathrm{s}}}$, T_{s} is sampling time, [n] is value at nth sampling point and L_{g} is grid-side inductance. A detailed derivation of (4.1) is given in the Appendix.

The inner loop is implemented by a boundary controller with second-order switching surface to deal with the filter resonance issue and to regulate v_{C}. With the using of a boundary controller, it can eliminate the resonance issue generated from the *LCL* input filter by simplifying its order in

the transfer function. The detailed expression of the transfer function will be described in Section 4.4. As AVG-BPFC is a boost type rectifier, the boundary control method is applied to the input stage of the system. The corresponding switching surface is generated from the filter capacitor and the converter-side inductor information. Unipolar switching method is adopted in this proposed scheme and the converter switching actions are generating from the boundary controller. The corresponding block diagram is shown in Figure 4-1 and the corresponding logic flow is shown in Figure 4-5 (c). In the traditional control method, the PWM gate signals are generated by comparing the duty reference obtained from the PI controller with the system pre-set triangular wave. In the boundary control scheme, the switching actions are provided by estimating the state situation of the capacitor with the use of the system information, v_{C}, i_{C}, v_{IN}, and v_{O}. The capacitor current forms from i_{L1} and i_{L2} which is equal to $-i_{\mathrm{L1}} - i_{\mathrm{L2}}$. In every half line cycle, there are the corresponding switching criteria. To obtain the switching criteria, firstly the equation of the capacitor switching surface needs to be developed. In the development, the current boundary is applied to handle the fixed frequency operation. In the positive cycle, the on-state equation is developed from the filter capacitor voltage and converter inductor current information. The equation of the capacitor switching surface at the on-state is formulated as,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) + \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right], \tag{4.2}$$

where $i_{\mathrm{C,min}}(t)$ is the minimum capacitor current generated from prediction. A detailed derivation of (4.2) is given in the Appendix.

The equation of the capacitor switching surface at off-state is formulated as,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right], \tag{4.3}$$

where $i_{\mathrm{C,max}}(t)$ is the maximum capacitor current generated from prediction. A detailed derivation

of (4.3) is given in the Appendix.

Due to the symmetric structure of the converter, the capacitor switching surface equation at the negative half line cycle is similar to (4.2) and (4.3). The only variation in the formula is the inductor term. L_1 is applied to the positive cycle deviation and L_2 is applied to the negative cycle deviation. The equations for the negative half line cycle are shown as follows,

at on-state,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) + \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right], \tag{4.4}$$

and at off-state,

$$v_{\mathrm{C}}(t) = v_{\mathrm{C,ref}}(t) - \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right]. \tag{4.5}$$

At the on-state, the control will use the off-state behaviors of the converter to generate the turn-off requirement. Similarly, at the turn-off state, the on-state behaviors will be used to generate the turn-on requirement. From (4.2) to (4.5), the system switching criteria can be expressed as (4.6) to (4.9). Take (4.7) as an example, it will predict whether or not the energy in the capacitor is sufficient to support the coming on-state operation. During the positive cycle with positive capacitor current, (4.7) will be active. Once the system satisfies the defined boundary requirement, the control will give out a switch-on signal to the switch S_1 and respond immediately. Otherwise, the detection will be kept on until the conditions are met. The system program flow and the logic of the other three switching actions are shown in Figure 4-5 (b) with their corresponding switching criteria.

For the positive cycle switch ON criteria,

$$\sigma_{\mathrm{ON},+}(t) = v_{\mathrm{C}}(t) - v_{\mathrm{C,ref}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot v_{\mathrm{C}}(t)} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \tag{4.6}$$

For the positive cycle switch OFF criteria,

$$\sigma_{\mathrm{OFF},+}(t) = v_{\mathrm{C,ref}}(t) - v_{\mathrm{C}}(t) - \frac{L_1}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (4.7)$$

For the negative cycle switch ON criteria,

$$\sigma_{\mathrm{ON},-}(t) = v_{\mathrm{C}}(t) - v_{\mathrm{C,ref}}(t) - \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot \mathrm{v_C(t)}} \left[i_{\mathrm{C,min}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (4.8)$$

For the negative cycle switch ON criteria,

$$\sigma_{\mathrm{OFF},-}(t) = v_{\mathrm{C,ref}}(t) - v_{\mathrm{C}}(t) - \frac{L_2}{2 \cdot C_{\mathrm{AB}} \cdot [v_{\mathrm{O}}(t) - v_{\mathrm{C}}(t)]} \left[i_{\mathrm{C,max}}(t)^2 - i_{\mathrm{C}}(t)^2 \right] \geqq 0. \quad (4.9)$$

To generate the *LCL* input filter structure, the switch S_{A} and S_{B} are switched alternatively and synchronized with the line frequency. It is implemented by using a polarity detector on the v_{C} signal. In the positive line voltage cycle, S_{A} is on and S_{B} is off. And in the negative line voltage cycle, the switching action is opposite. The grid current ripple is minimized and clamped the CM noise all the time by the AVG circuit. Its control block diagram is shown in Figure 4-5 (d).

4.3.3 State Machine of the CCM and DCM Operation

By integrated the state machine into the second-order boundary control, it is possible to handle well in both continuous conduction mode (CCM) operation and discontinuous conduction mode (DCM) operation. In addition, by its fast dynamic response characteristics, it can offer a more precise current tracking function than the methodology with linear control. This is especially true during the zero crossing period [4.24] and the transition between CCM and DCM operation [4.25] where the weakness point normally finds in the traditional controller. High input power factor and low current THD can be obtained in the final.

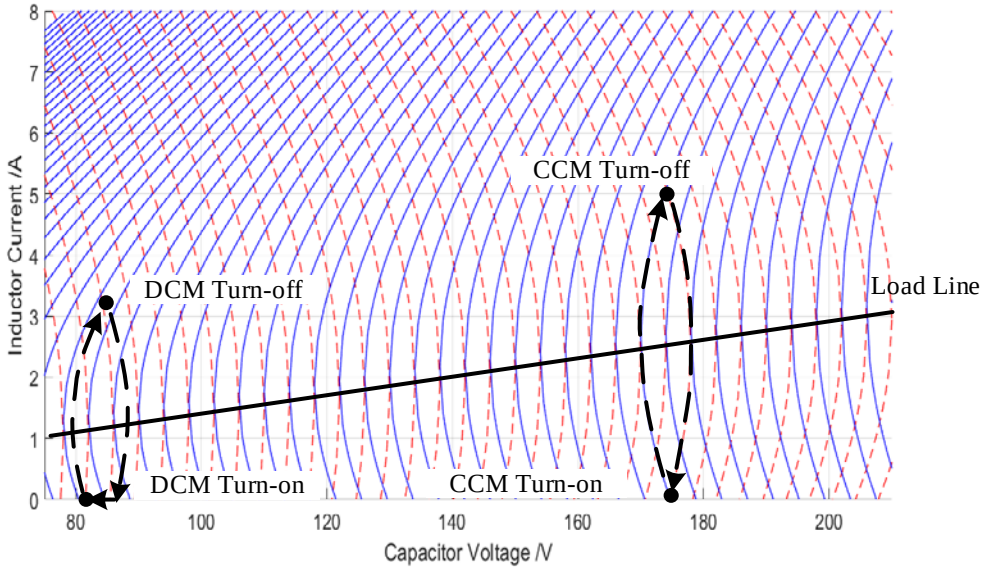


Figure 4-6. The switching surface of the boundary control.

From the state equation, the switching trajectories of the AVG-BPFC can be plotted out as Figure 4-6. The relationship between the inductor current and the capacitor voltage is demonstrated by the corresponding switching surface figure under the boundary operation. The red dotted line is drawn from the on-state operation and the blue one is drawn from the off-state operation. Based on the boundary condition, at all time there will be two operation points in the figure and the switching action of the system will be following the trajectory line between them.

During the CCM operation, there are two operation steps in the whole switching period, as shown in Figure 4-6. At the turn-on state, it starts from the CCM turn-on point and following the on-state trajectory line until it reaches the target CCM turn-off point. Afterward, the system will enter into the turn-off state and follow the off-state trajectory to return the CCM turn-off point to complete a period of switching. During the CCM operation, the capacitor current boundary can be defined as,

$$i_{\mathrm{C,min,CCM}}(t) = i_{\mathrm{C,max,CCM}}(t) = \Delta i_{\mathrm{C}}(t) = \frac{1}{2} \cdot \frac{v_{\mathrm{IN}}(t)}{v_{\mathrm{O}}(t)} \cdot \frac{v_{\mathrm{O}}(t) - v_{\mathrm{IN}}(t)}{L_{\mathrm{x}} \cdot f_{\mathrm{SW}}}, \tag{4.10}$$

where L_x can be either L_1 or L_2 as the value is the same and f_{SW} is the switching frequency.

During the low load condition or low input voltage condition, the system will enter into the DCM operation. As shown in Figure 4-6, one switching period is separated into three operation steps in the whole switching period. During the turn-on period, the on-state trajectory line is started from the DCM turn-on point and ended at the target DCM turn-off point. Then the system will enter into the turn-off state and follow the off-state trajectory before the inductor current becomes zero. Afterward, the converter diode will block the path and avoid the negative current in the inductor. Converter-side inductor current will be zero. It will wait until the capacitor voltage charges up to the target DCM turn-on operation point and completes a period of switching. During the DCM, the capacitor current boundary can be defined as,

$$i_{C,max,DCM}(t) = i_{G,ref}(t), \tag{4.11}$$

$$i_{C,min,DCM}(t) = 2 \cdot \sqrt{\Delta i_C(t) \cdot i_{G,ref}(t)} - i_{G,ref}(t). \tag{4.12}$$

The state machine diagram is shown in Figure 4-7 with the detailed logic flow. Due to the switching action, the voltage across C_{AB} is all the time in a positive sign and equals to a rectified sine waveform. In the circuit, L_1 and L_2 are set to the same inductance value. Therefore, the on-off state equations in the positive and the negative half line cycle, (4.6) – (4.9), will be totally the same. $\sigma_{ON,+}(t)$ and $\sigma_{ON,-}(t)$ are combined as $\sigma_{ON}(t)$ and $\sigma_{OFF,+}(t)$ and $\sigma_{OFF,-}(t)$ are combined as $\sigma_{OFF}(t)$. Based on the switching state equation, the controller will determine whether changing the switching action or keep staying by using the same state. Also, it will base on the value of $\Delta i_C(t)$ and $i_{G,ref}(t)$ to determine whether the DCM or CCM boundary should be applied. So that a precise control is achieved.

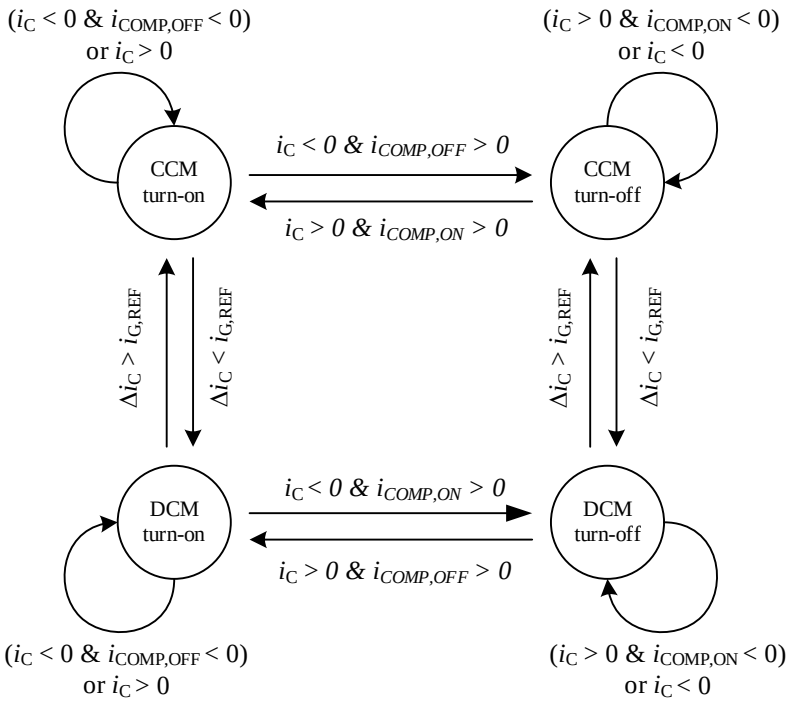
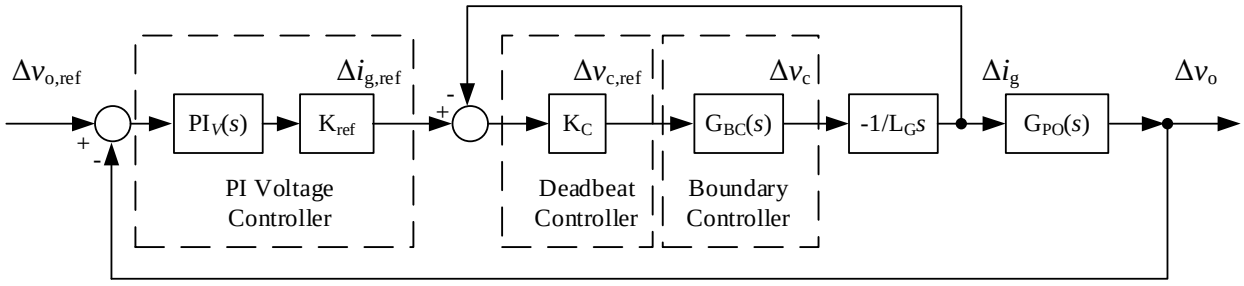


Figure 4-7. The logic flow of the mode operation.

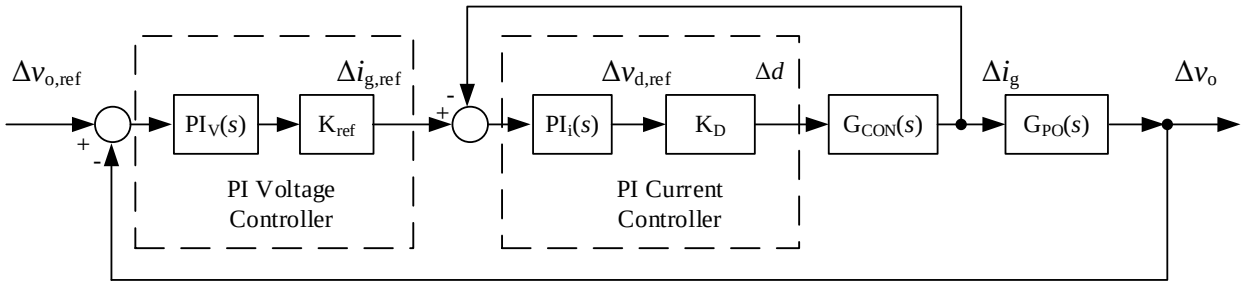
4.4 System Modelling and Implementation

To analyze the system stability, the small signal analysis method is applied. From the proposed control scheme as shown in Figure 4-1, the corresponding small signal model is determined and is shown in Figure 4-8 (a). At the same time, a small signal model of the traditional PI controller is generated as a reference and is shown in Figure 4-8 (b). In both cases, a PI controller is applied to implement in the outer loop to regulate the output voltage with the same set of controller parameter. The difference between the proposed control scheme and the traditional PI control scheme is in the inner loop which is the grid current loop. On the traditional control scheme, a linear PI controller aims to control the grid current. It generates the duty reference in the output and compares with a triangular wave in the PWM block to produce the switching signals. With the

proposed scheme, a deadbeat controller is implemented to control the grid current together with a boundary controller inside to regulate the ac voltage. The inner loop is a nonlinear block and the switching signals are provided from its boundary controller. The inner loop cut off frequency, 1.1 kHz, is used as a reference point for both of the proposed control scheme and the PI control scheme.



(a)



(b)

Figure 4-8. Block diagrams of (a) the proposed control scheme and (b) PI control scheme

4.4.1 Proposed Current Loop

In order to study the stability of the PI current loop, both of the system and controller transfer functions are required. Due to the symmetric structure of the AVG-BPFC, only the positive half line cycle information is used to generate the model for the following system analysis. In the positive cycle, the grid current, $i_{\mathrm{G}}(t)$, is equal to the current appearing on the inductor L_2, $i_{L2}(t)$.

L_1 acts as the converter-side inductor and uses for the converter energy transfer. The capacitor C_{AB} is connected to the Line and the negative bus.

In the proposed control scheme, there are two controllers inside the grid current loop. They are boundary controller and a deadbeat controller. Under the proposed control scheme, all of the filter components information are well under control. The grid-side current is controlled by the deadbeat controller, and the capacitor voltage and the converter-side inductor current are regulated by the boundary controller. By such method, the resonant issue appeared in the PI current control loop is eliminated. In order to analyze the system stability of the proposed control scheme, both of the system transfer function and the second-order boundary controller's transfer function are required.

Based on the method described in [4.16], the transfer function of the voltage boundary loop, $G_{\mathrm{BC}}(s)$, in the boost type rectifier can be developed and the boundary equation is found as,

$$G_{\mathrm{BC}}(s) = \frac{\Delta v_{\mathrm{c}}(s)}{\Delta v_{\mathrm{c,ref}}(s)} = \frac{1}{\frac{T}{4}s+1} \tag{4.13}$$

where T is switching period. A detailed derivation of (4.13) is given in the Appendix.

Based on the derived deadbeat controller theory, the corresponding transfer function of the deadbeat controller, $G_{\mathrm{DB}}(s)$, is found as,

$$G_{\mathrm{DB}}(s) = K_{\mathrm{C}} \tag{4.14}$$

where a detailed derivation of (4.14) is given in the Appendix.

From the expression of (4.14), it shows that only a single proportional gain, K_{C}, is shown on its transfer function. Thus, a simple and fast dynamic control is provided by the deadbeat controller. In addition, from the state equation of the filter capacitor, the transfer function between

$\Delta i_{\mathrm{g}}(s)$ and $\Delta v_{\mathrm{c}}(s)$ can be formed as,

$$\frac{\Delta i_{\mathrm{g}}(s)}{\Delta v_{\mathrm{c}}(s)} = -\frac{1}{L_{\mathrm{g}} \cdot s}. \tag{4.15}$$

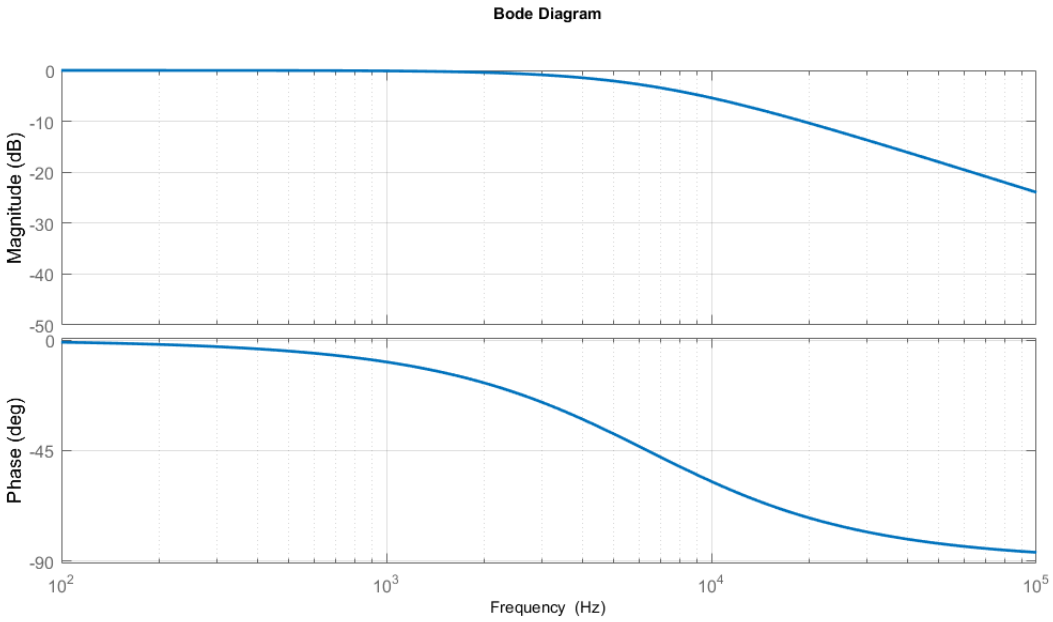
Therefore, by using (4.13) - (4.15), the overall closed-loop transfer function of the proposed current control scheme, $G_{\mathrm{CC,new}}(\mathrm{s})$, is derived as,

$$G_{\mathrm{CC,new}}(\mathrm{s}) = \frac{\Delta i_{\mathrm{g}}(s)}{\Delta i_{\mathrm{g,ref}}(s)} = \frac{K_{\mathrm{C}}}{\frac{T}{4} \cdot L_{\mathrm{g}} \cdot s^2 + L_{\mathrm{g}} \cdot s + K_{\mathrm{C}}}. \tag{4.16}$$

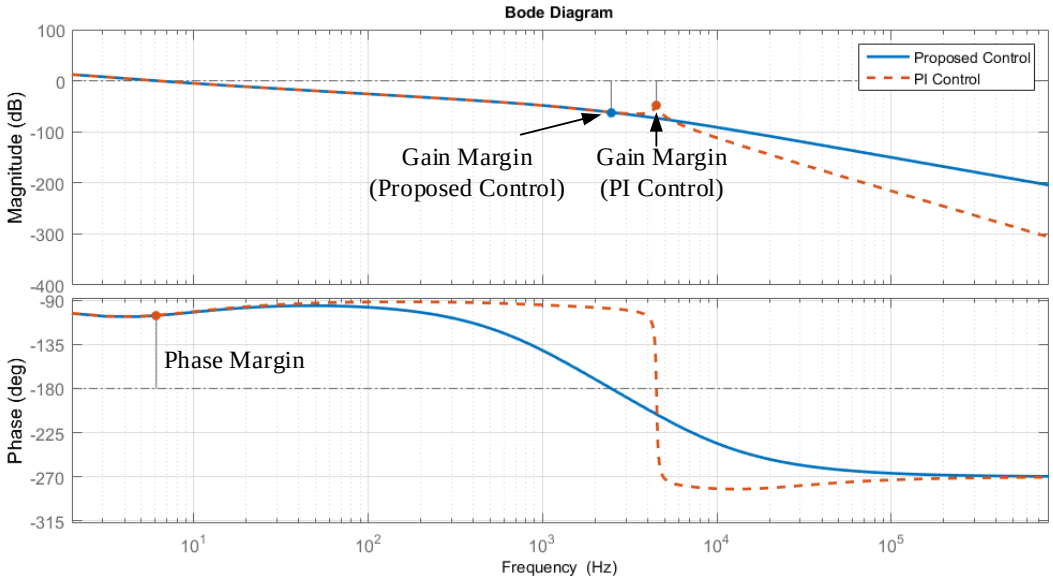
In the reference PI control method, due to the *LCL* input filter structure, the converter transfer function becomes complicated and with a lot of poles in the expression [4.11]. A third-order system will be generated in the inner loop of the PI control scheme together with a resonant pole. The current open-loop Bode diagram of Figure 4-8 (b) is shown in Figure 4-9 (b) with a red color dotted line. Based on the targeted cut off frequency, a set of PI parameter is generated for the system performance analysis where Kp and K_{i} in the inner loop are 0.0325 and 3250 respectively. Moreover, the detailed derivation of the converter block, $G_{\mathrm{CON}}(s)$, is given in the Appendix as a reference.

With the proposed system, the boundary control helps to simplify the system order and offers a first-order system in the inner loop as (13). Therefore, the current closed-loop transfer function becomes simple and the *LCL* resonant issue is also eliminated. A much simpler and more stable control loop is provided under the proposed control scheme. The corresponding frequency plots of $G_{\mathrm{BC}}(s)$ and $G_{CC,new}(s)$ are shown in Figure 4-9 (a) and the blue line in Figure 4-9 (b) respectively. It showed that the system is stable under the proposed control scheme, which eliminated the resonance issue from the converter stage. Therefore, the design of the system bandwidth no longer contradicts the *LCL* resonant frequency. A 4.3 kHz *LCL* resonant frequency will appear on the

system structure. However, under 1.1 kHz control bandwidth in the current loop, the system can still maintain stable operation as the resonance is eliminated by the boundary control method. The controller design is more fixable.



(a)



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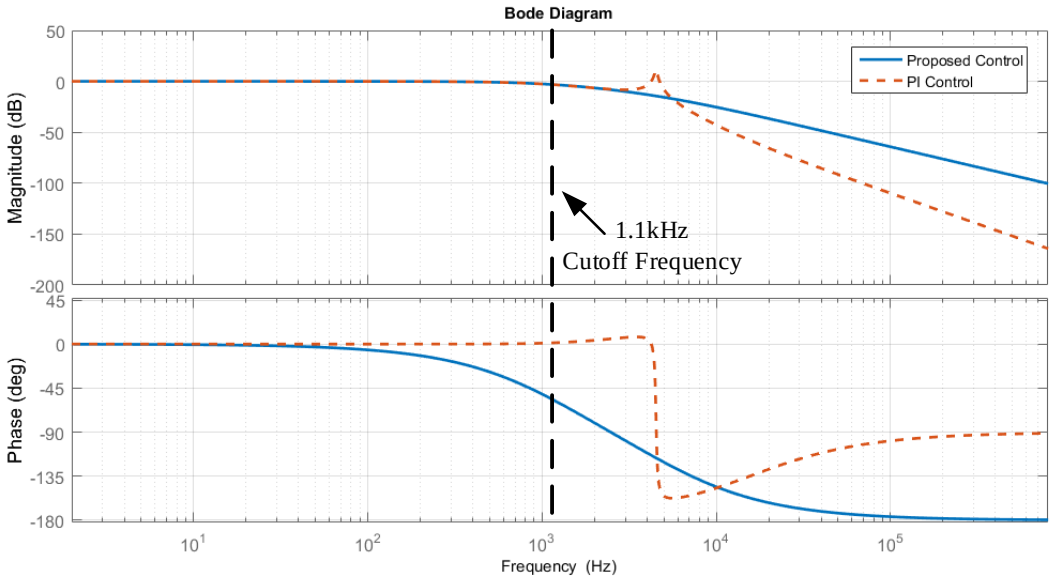


(c)

Figure 4-9. Frequency plots of (a) the boundary block, (b) the current closed-loop transfer function and (c) the overall open-loop system transfer function.

From the expression of (4.13) and (4.16), it shows that the current loop stability is available to support a wide range of operations including various loading conditions and the output voltage jumping. The inner loop transfer functions no longer depend on the system parameter but only relates to the switching frequency and the variation of the passive components. As a result, a stable phase margin is obtained all the time. Also under the proposed control methodology, more system parameters are available to control but in a simpler structure.

4.4.2 Overall System Stability of the Proposed Control Scheme

In order to analyze the overall system stability, a whole system open-loop Bode diagram is required. K_{ref}, as shown in the outer loop in Figure 4-8, is a proportional gain which correlates with the input voltage value.

The transfer function of the outer loop, $G_{\mathrm{PO}}(s)$, is expressed as:

$$G_{\mathrm{PO}}(s) = \frac{\Delta v_{\mathrm{o}}(s)}{\Delta i_{\mathrm{g}}(s)} = \frac{V_{\mathrm{IN}}}{V_{\mathrm{O}}} \cdot \left(\frac{R_{\mathrm{O}}}{2+R_{\mathrm{O}} \cdot C_{\mathrm{O}} \cdot s}\right), \tag{4.17}$$

where C_{O} is output capacitor, R_{O} is output resistance. A detailed derivation of (4.17) is given in the Appendix.

Lastly, the transfer function of the PI voltage controller, $G_{\mathrm{PIv}}(\mathrm{s})$, can be expressed as:

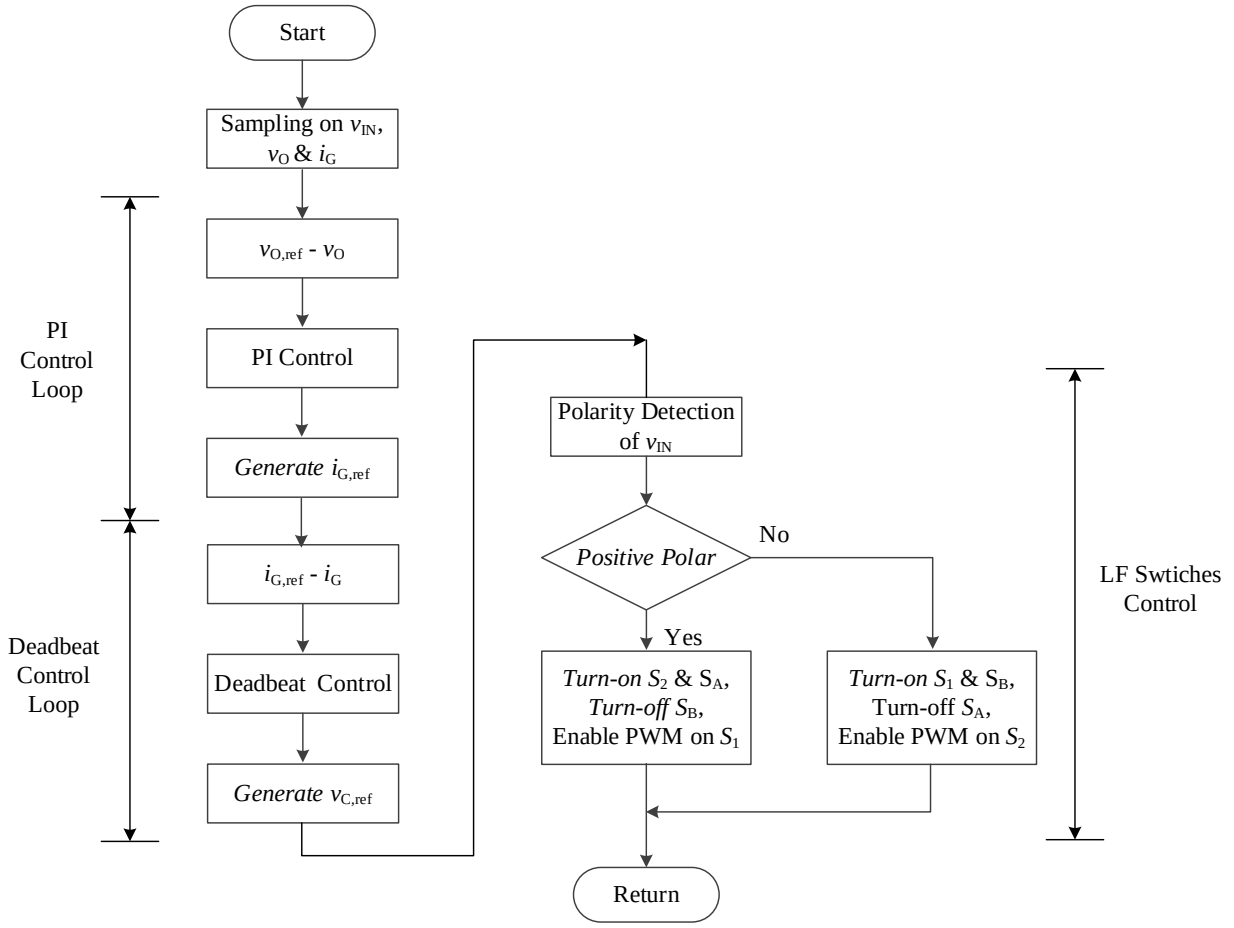
$$G_{\mathrm{PIv}}(\mathrm{s}) = \frac{K_{\mathrm{p}} \cdot \mathrm{s} + K_{\mathrm{i}}}{\mathrm{s}}. \tag{4.18}$$

By using K_{ref}, (4.16), (4.17) and (4.18), the overall open-loop characteristic of both control schemes are found. To achieve the phase margin in the system on the PI control scheme, an extra low pass filter is also implemented into the digital control. The system stability can be observed from the Bode diagram which is shown Figure 4-9 (c) where the Kp and K_{i} in the outer loop are 0.02352 and 0.000706 respectively. The proposed control scheme is in the blue straight line with 61.9 dB gain margin together with 74.6° phase margin. The PI control scheme is in red dotted line with 48.7 dB gain margin together with 74.6º phase margin. It showed that the output voltage can regulate well under both of the systems. In the proposed control scheme, the gain margin is more than the PI control scheme due to the elimination of the resonant characteristic. Also, no more resonance pole appeared in the voltage control loop. Therefore, with the use of the proposed control scheme, a stable operation system can be built.

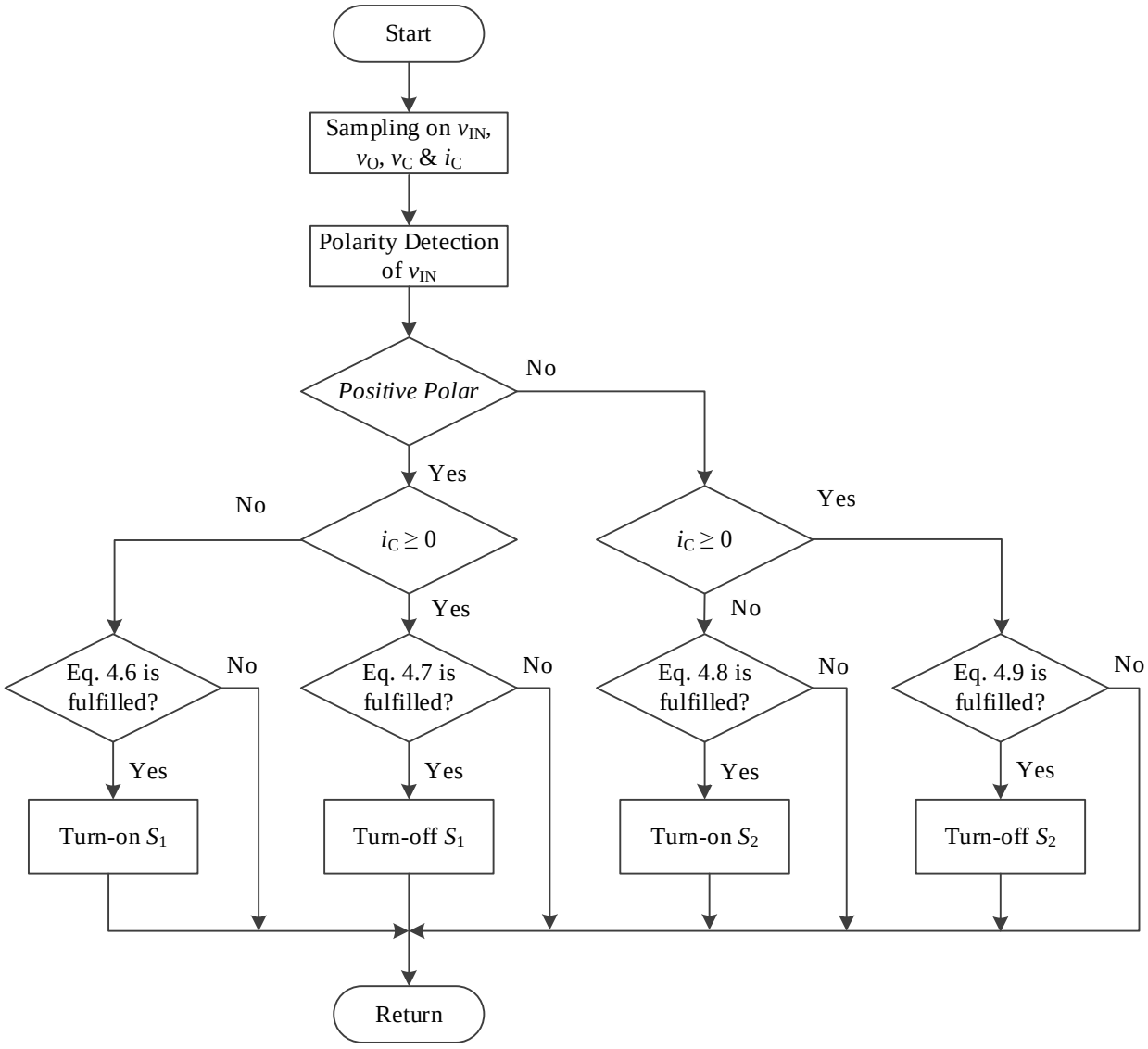
4.4.3 Implementation of the Digital Control

The whole controller system is built in the TI TMS320F28375S microcontroller. The detailed program flow of the digital control system is shown in Figure 4-10. The outer loop is

written in the CPU by converting (4.18), the transfer function of the PI controller, into z-domain to regulate the output voltage. In the middle loop, the relationship between the grid current error and the capacitor voltage is linearized by the deadbeat controller. Thus, a precise current tracking is able to be done in a simple way. Finally, in the inner loop, the switching criteria are generated from the CLA calculation and do comparison in the EPWM block to generate switching action. As a result, the whole system is implemented in the digital platform in a simple way.



(a)



(b)

Figure 4-10. Program flow diagrams of the proposed control scheme, (a) PI voltage control and deadbeat current control loop and (b) boundary voltage control loop.

As the switching action comes from prediction, one cycle delay usually exists in the digital platform. Therefore, the sensor updating rate in the digital control platform should be kept 80 to 100 times faster than the target switching speed. This can help to maintain the accuracy of the switching action and to generate a very precise $\boldsymbol{v_C}$ control in the inner loop. In the design, the inner loop frequency is targeted to 1 MHz and the target operation frequency is selected to 10 kHz under

the 100 times sampling criteria.

4.5 Experimental Verification

A 1.5 kW AVG-BPFC prototype is implemented as shown in Figure 4-11 with the specification shown in TABLE 4-I. An 120 Vac voltage source was applied to the system input and a group of resistive loads was connected to the system output as a power load. According to the system specification, the output voltage was regulated at 400 Vdc. The system code is written in the TI TMS320F28375S microcontroller. The AVG capacitor, C_{AB}, value is chosen as 3.3 µF which is based on the criteria of circuit resonance frequency and target leakage current requirements [4.9].

TABLE 4-I VALUE OF THE SYSTEM CONDITIONS USED IN THE DESIGN

Parameter	Value	Parameter	Value
Input Voltage	120 Vac	Output Voltage	380 Vdc
Input Frequency	60 Hz	Max. Output Power	1.5 kW
Switching Frequency	10 kHz	Output Capacitor	1.2 mF
Inductor (L_1 & L_2)	0.78 mH	Capacitor (C_{AB})	3.3 µF

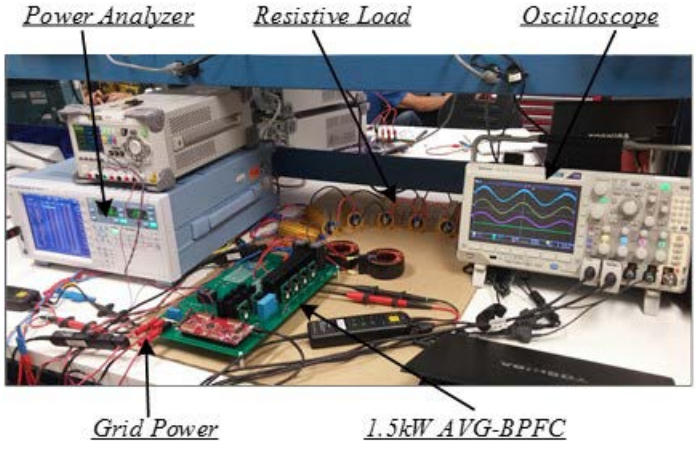
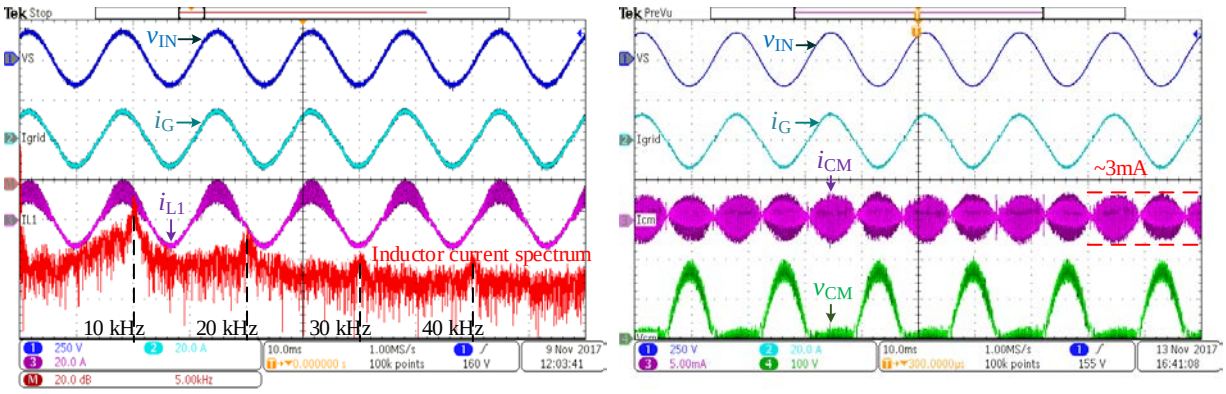


Figure 4-11. Experimental test setup.



(a) (b)

Figure 4-12. Experimental waveforms of the proposed control scheme with (a) the inductor current's FFT analysis and (b) the leakage current measurement at 1 kW output.

The steady state performance of the proposed AVG-BPFC control scheme is proofed under different power rating operations and the dynamic performance is proofed by the transient performance during an instantaneous load change and various input voltages. A FFT analysis is applied to the inductor current. From the resulted frequency spectrum, as shown in Figure 4-12 (a), it demonstrates that the proposed control scheme is able to fix the system switching frequency to the target value as 10 kHz which able to proof the control theory. If any tolerance appears in the converter-side inductance, the switching time period will be changed. In addition, referred to [4.26], a 470 pF capacitor is applied to the system as the parasitic capacitor between the system ground point and the Neutral point of the grid in order to demonstrate the low leakage current of the system. The HF common mode noise voltage generated by the system is limited to a low amplitude level and the leakage current is able to limit mA level which fulfills the theory mentioned in [4.9]. The measured result leakage current is shown in Figure 4-12. In addition, a conductive EMI test is done in order to demonstrate the advantage of the AVG-BPFC over the traditional BPFC. The result matched with the prediction in [9] which is very clear that the noise

level in the traditional BPFC is much higher than the AVG-BPFC in the range within 2 MHz. At the MHz frequency range, the noise level is varying as both topologies have different input filter components.

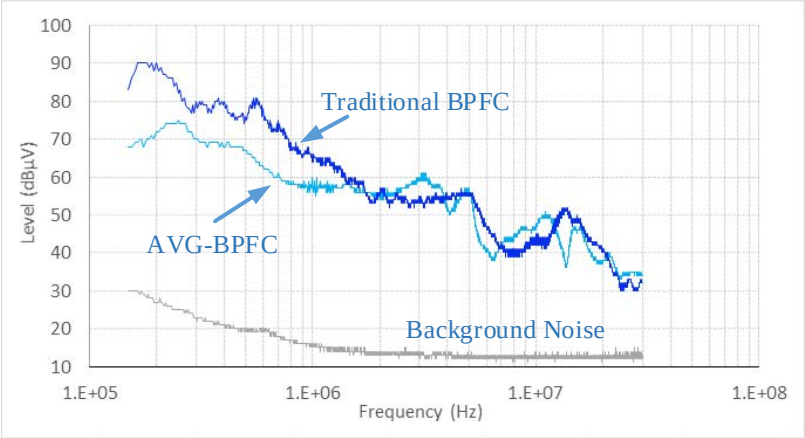
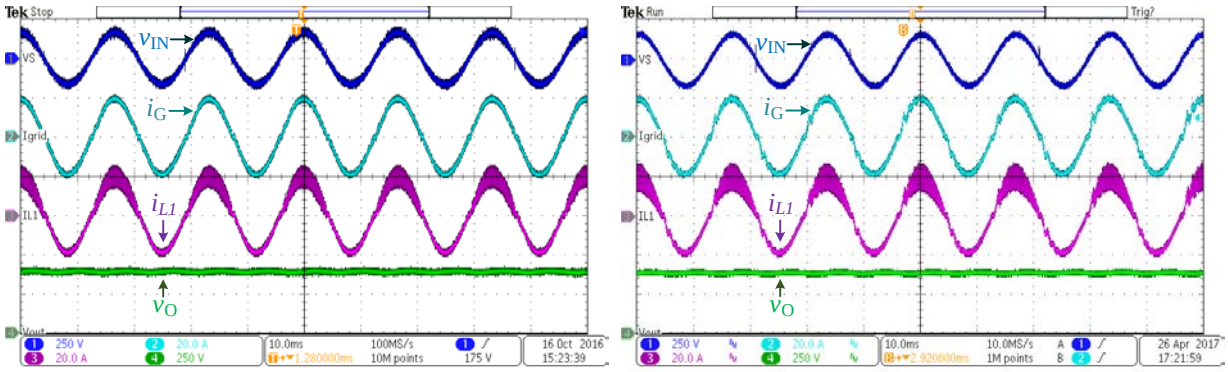


Figure 4-13. Conductive EMI measurement of the traditional BPFC and AVG-BPFC at 1kW output.



(a) (b)

Figure 4-14. Experimental waveforms of (a) the proposed control scheme and (b) the PI control scheme at 1.5 kW output.

The steady state waveforms of the AVG-BPFC with the proposed control scheme are shown in Figure 4-14 (a) and Figure 4-15. Figure 4-14 (a) was operated in the CCM mode with 100 %

loading condition and Figure 4-15 was operation in the DCM mode with 15 % loading condition. All of them showed that under the proposed control methodology, a stable waveform can be obtained together with a good system performance. From those steady state waveforms, it demonstrated the system can operate correctly. During the positive line cycle, L_1 carried a large HF current ripple as it was the converter-side inductor. While a relatively small HF current ripple appeared on the grid due to the generated input *LCL* structure. In the negative half line cycle, the function of L_1 and L_2 were interchanged, the inductor L_1 became the grid-side inductor. Thus, the current ripple that appeared in L_1 was the same as the grid current ripple. These waveforms were matched with the behaviours of input *LCL* filter and the converter characteristics.

Under the proposed control scheme, the input power factor was above 0.996 among the whole power range. From the waveforms, it demonstrated that the phase shift problems were solved. A good power and current qualities system was obtained as the resonant issue was eliminated by the proposed control scheme. At the full load condition, the system efficiency was 94.32 % and the voltage THD was 0.11 % together with 3.48 % current THD, where Figure 4-14 (a) was the corresponding operation waveform. At light load DCM mode, the system can still maintain good power quality and high efficiency. At 15 % power rating, 96.20 % efficiency was achieved and the system was stable as shown in Figure 4-14. The corresponding voltage THD and current THD were 0.022 % and 2.80 % respectively. The current harmonic spectrum of Figure 4-14 (a) and Figure 4-15 (b) are shown in Figure 4-16 and Figure 4-17 respectively. Under the proposed scheme, the AVG-BPFC could fulfill the IEEE 519 class A standard requirement and all harmonics are under the limitation line [4.27].

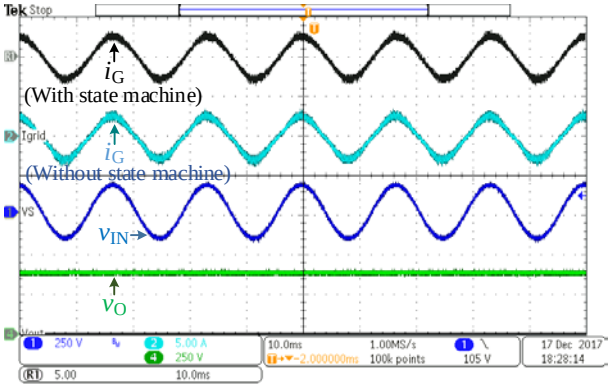


Figure 4-15. Experimental waveforms of the proposed control scheme at 230 W with and without state machine.

Comparing with the waveforms generated by the conventional PI method, as shown in Figure 4-14 (b), the waveforms from the proposed control system were more promising. As shown in Figure 4-14 (b), although the system output was able to regulate at a stable value, current distortion appeared in the grid current waveform, especially in the zero current point together with some small oscillation. Therefore, the input power factor and the THD were also affected. It degraded the system performance and generated stability concerns. In the 1.5 kW test case, the total voltage harmonic and the current harmonic of PI control method were 0.24 % and 5.77 % respectively. The current harmonic was at least 2.2 % more than the proposed scheme. The corresponding input current harmonic spectrum is shown in Figure 4-16. Due to the resonance issue in the PI control loop, the current harmonics of 13^{th} to 19^{th} in the PI control scheme were higher than the proposed control scheme. In the meantime, the values were over the limitation and not permitted by the industry standard. Moreover, the harmonics may influence the system stability causing abnormal operations under the resonant issue. To limit the harmonic contents, the control bandwidth needs to be decreased or an extra input filter is required. However, the dynamic performance will be influenced. With the proposed control scheme, it can successfully eliminate the resonant pole from

the *LCL* system input structure and offer a stable control system.

In Figure 4-15, it showed the performance difference between using and not using the state machine under the proposed method. During the light load operation, the system was operated in DCM condition. When the proposed control system didn't integrate with the state machine, once the inductor current reached zero and the switch would be immediately turned on. Therefore, the grid current waveform was distorted and the frequency was varying. The total voltage harmonic and the current harmonic were 0.024 % and 6.20 % respectively. Also, a higher 3^{rd} and 5^{th} order harmonics were resultant. Due to the current distortion issue, the current harmonics in the 15 % loading condition was at least 3.4 % lower when the state machine didn`t integrate on top of the proposed control scheme. The corresponding input current harmonic spectrum is shown in Figure 4-17. Under the implementation of the state machine, high grid current quality is able to achieve in both CCM and DCM conditions. The system was well controlled by the digital controller and the power quality was improved.

During the steady state operation, the system was performed well and this also happened in the transient operation. In Figure 4-18 (a) showed out the system performance during the load transient in which the load was jumping from 680 ohms to 97 ohms. Another transient test was the grid voltage jumping, as shown in Figure 4-18 (b), the input voltage was jumping from 137.5 V to 70 V. In both test cases, the system was also stable and was able to convert into the steady state in a short moment of time after the change appeared. For comparison, the same set of transient test is applied to the PI control scheme. The load transient waveform is shown in Figure 4-18 (c) and the grid voltage jumping waveform is shown in Figure 4-18 (d). In both situations, the system can still keep stable on the output voltage regulation.

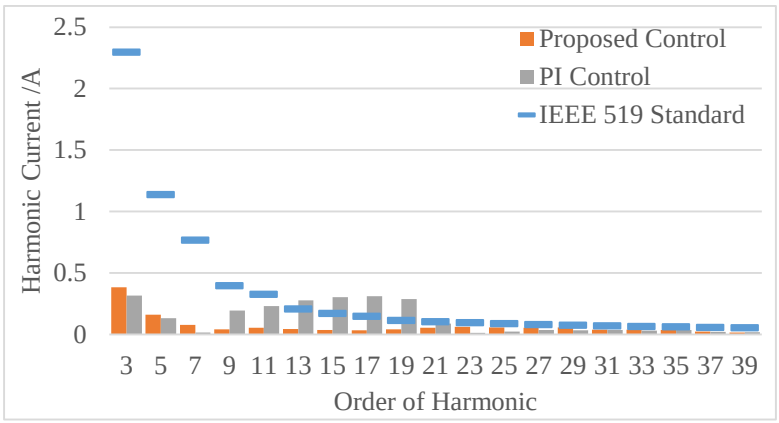


Figure 4-16. Input current harmonic comparison between the proposed control scheme and the PI control scheme at 1.5 kW

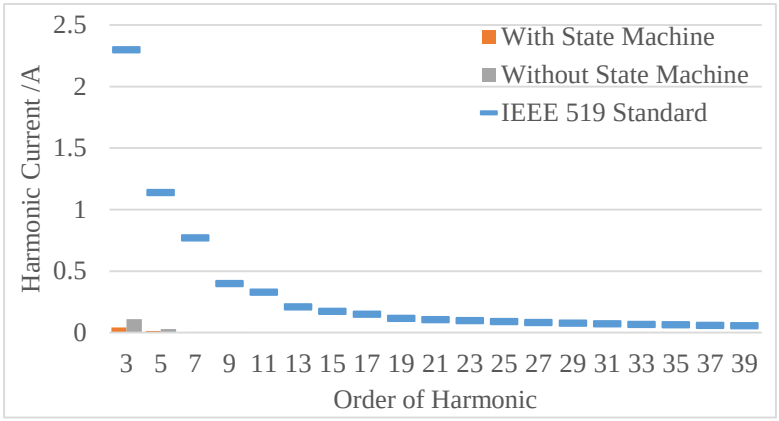
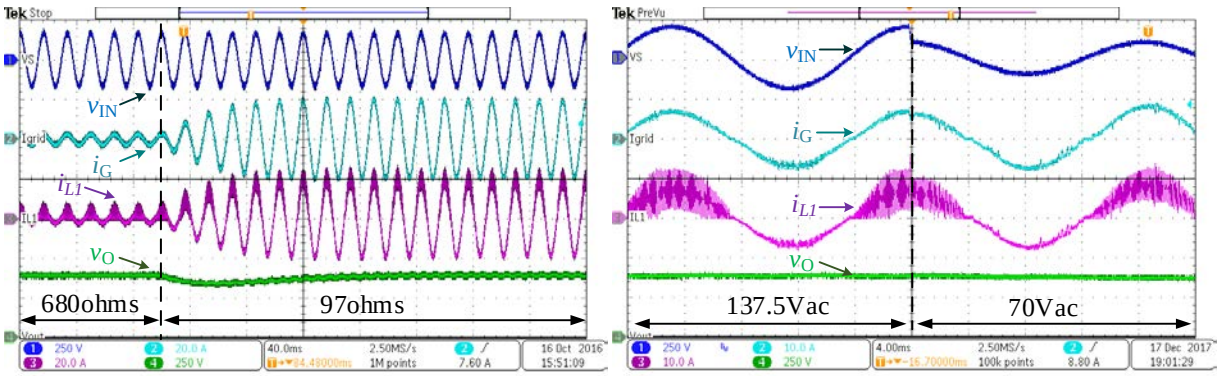
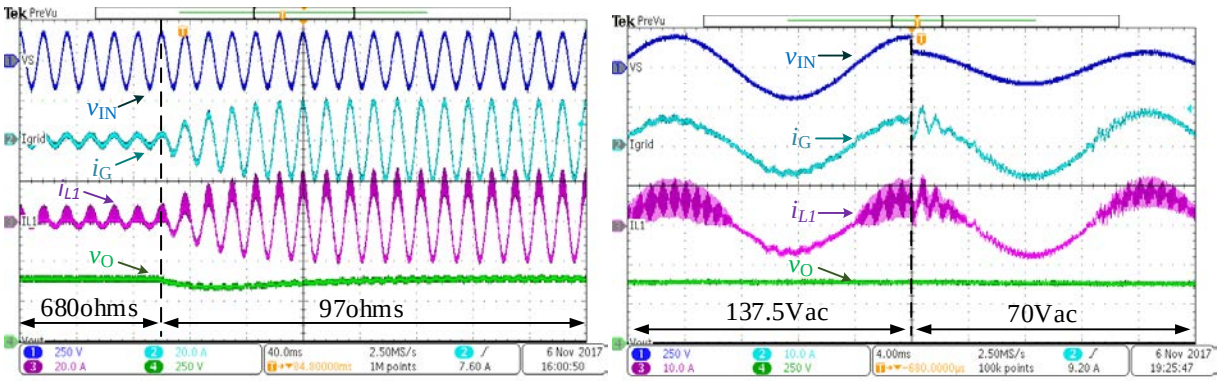


Figure 4-17. Input current harmonic comparison between the proposed control scheme with and without state machine at 230 W.



(a) (b)



(c) (d)

Figure 4-18. System transient response waveforms, the proposed control scheme at (a) load change and (b) input voltage sag, and the PI control scheme at (c) load change and (d) input voltage sag.

In the load transient test, the transient action influences the system power level and the main effect appears on the outer loop of the system. The same output voltage transient performance is observed in the proposed control scheme and the PI control scheme, as the same set PI controller is applied in both control scheme. In the grid voltage jumping test, the transient action influences the system grid current magnitude and the main effect appears on the inner loop of the system. In the proposed control scheme, the inner loop can provide a fast response to the system and smooth the action in the transient period. However, in the PI control scheme, the response was lower and a larger oscillation appeared on the grid current waveform. Also, low frequency harmonics were observed in the steady state.

All of the results of the proposed control scheme had a very good alignment with the theoretical control principle and fulfill the target design specification. Finally, a stable system was provided from such triple loop control architecture for an AVG-BPFC system.

4.6 Conclusion

The chapter has presented an advanced digital control scheme for the Active Virtual Ground-bridgeless PFC. The system implementation and detailed small signal model are given in this chapter. Such proposed control scheme improves the system stability and enhances grid current quality under various loading conditions. In addition, it performs well in the system transient response. As a result, under the proposed control structure, the advantages of the AVG-BPFC can be maximized in order to achieve high system efficiency, low leakage current, small magnetic components, and high current quality. The performance of the AVG-BPFC and the proposed control methodology was demonstrated with the experimental results. A 120 V, 60 Hz, 1.5 kW prototype has been implemented in order to verify the presented concept. There was a good agreement between the theoretical concept and the experimental results.

4.7 Discussion of the Design Limitation

In practice, there always has an upper limit on the maximum system control bandwidth and the available system operation frequency which are limited by program computation time and the ADC sampling rate. Different from PI control, more instruction codes are required in the proposed control method. Therefore, a longer computation time is needed. In order to minimize the computation time, CLA (control law accelerator) is used. The CLA is applied to handle the sensor data and to compute the boundary control criteria. It can work parallel with the main CPU which is used to handle the system program flow. Thus, by separating the work systematically, the overall computation time can be maintained in a minimized time and the loop frequency is within MHz range.

For the selected controller, TMS20F28377S, 2 ADC channels are offered and each of them has a maximum sampling rate of 3.5 MHz. However, in the proposed control architecture, 5 sensor signals are required which means that the actual maximum sampling rate is downscale to 1.19 MHz. Therefore, based on the program length and the ADC updating speed, 1 MHz is finally selected as the platform inner loop operation frequency. In addition, under the 100 sample point criteria, 10 kHz is selected at the target switching frequency. On the existing digital control platform, if the operating frequency is increased, the accuracy of the control will be reduced. Therefore, if higher frequency operation is required, a digital controller with a faster ADC is recommended.

Appendix

A. Derivation of (4.1)

From equivalent circuits on Figure 4-2, the state equation of the system input can be found as,

$$L_{\mathrm{G}} \frac{di_{\mathrm{G}}(t)}{dt} = v_{\mathrm{IN}}(t) - v_{\mathrm{C}}(t), \tag{A4.1}$$

where L_{G} is the grid inductor which is equal to L_1/L_2 as both are having the same value.

By applying forward Euler method on (A4.1) under discrete time domain, the equation is modified as,

$$L_{\mathrm{G}} \frac{i_G[n+1]-i_G[n]}{T_{\mathrm{S}}} = v_{\mathrm{IN}}[n+1] - v_{\mathrm{C}}[n+1]. \tag{A4.2}$$

Under the prediction of deadbeat control, $i_{\mathrm{G}}[n+1]$ is equal to $i_{\mathrm{G,ref}}[n]$ and $i_{\mathrm{G}}[n+1]$ is equal to $i_{\mathrm{G,ref}}[n]$. Also, the variation of v_{IN} is small between each sampling period, therefore, $v_{\mathrm{IN}}[n+1] \cong v_{\mathrm{IN}}[n]$. As a result, (4.1) can be obtained.

B. Derivation of (4.2)

From the on-state circuit in the positive line cycle, the equation of capacitor current and the voltage are defined as,

$$\frac{\mathrm{d}i_{\mathrm{C}}(t)}{\mathrm{d}t} = -\frac{\mathrm{d}i_{\mathrm{L1}}(t)}{\mathrm{d}t} = -\frac{v_{\mathrm{C}}(t)}{L_2} \Longrightarrow \mathrm{d}t = -\frac{L_1}{v_{\mathrm{C}}(t)} \cdot \mathrm{d}i_{\mathrm{C}}(t), \tag{A4.3}$$

and

$$C_{\mathrm{AB}} \frac{\mathrm{d}v_{\mathrm{C}}(t)}{\mathrm{d}t} = i_{\mathrm{C}}(t) \Longrightarrow C_{\mathrm{AB}} \cdot \mathrm{d}v_{\mathrm{C}}(t) = i_{\mathrm{C}}(t) \cdot \mathrm{d}t. \tag{A4.4}$$

By combining (A4.3) and (A4.4) together with the predicting values at t_2, (4.2) can be

obtained.

C. Derivation of (4.3)

The off-state equation in the positive line cycle is derived under the same method of deviation in the on-state. The same voltage equation (A4.4) is used and the corresponding current equation of the capacitor is renewed as,

$$\mathrm{d}t = -\frac{L_1}{v_{\mathrm{C}}(t)-v_{\mathrm{O}}(t)} \cdot \mathrm{d}i_{\mathrm{C}}(t). \tag{A4.5}$$

By combining (A4.4) and (A4.5) with predicting values at t_4, (4.3) can be obtained.

D. Derivation of (4.13)

In the boundary control, the capacitor voltage reference, $v_{\mathrm{C,ref}}$, is defined as,

$$v_{\mathrm{C,min}}(t_{\mathrm{OFF}}) + v_{\mathrm{C,max}}(t_{\mathrm{ON}}) = 2 \cdot v_{\mathrm{C,ref}}(t). \tag{A4.6}$$

Similar to (4.2) and (4.3), with the prediction value at t_1 and at t_3 respectively, another set of capacitor switching surface equations are formulated as,

at on-state,

$$v_{\mathrm{C}}(\mathrm{t}) = v_{\mathrm{C,max}}(\mathrm{t}) + \frac{L_1}{2\cdot[v_{\mathrm{C}}(t)-v_{\mathrm{O}}(t)]\cdot C_{\mathrm{AB}}} \cdot i_{\mathrm{C}}(\mathrm{t})^2, \tag{A4.7}$$

and off-state,

$$v_{\mathrm{C}}(\mathrm{t}) = v_{\mathrm{C,min}}(\mathrm{t}) + \frac{L_1}{2\cdot v_{\mathrm{C}}(t)\cdot C_{\mathrm{AB}}} \cdot i_{\mathrm{C}}(\mathrm{t})^2. \tag{A4.8}$$

By considering $\Delta v_{\mathrm{o}}(t)$, $\Delta i_{\mathrm{L1}}(t)$, $\Delta v_{\mathrm{c}}(t)$, $\Delta v_{\mathrm{c,ref}}(t)$, $\Delta i_{\mathrm{g}}(t)$ and $\Delta \mathrm{d}$ as the small-signal perturbations of v_{O}, i_{L1}, v_{C}, $v_{\mathrm{C,ref}}$, i_{G} and D respectively for the (A4.7) – (A4.8). In the AVG-BPC, the circuit is symmetric in each half line cycle. (4.13) can be formed with the same method

described in [4.16] for the boost state converter.

E. Derivation of (4.14)

By considering $\Delta v_{\mathrm{c,ref}}[n]$, $\Delta v_{\mathrm{g}}[n]$, $\Delta i_{\mathrm{g,ref}}[n]$ and $\Delta i_{\mathrm{g}}[n]$ as the small-signal perturbations of $v_{\mathrm{C,ref}}$, v_{G},$i_{\mathrm{G,ref}}$ and i_{G} respectively in the small signal analysis model, (4.1) can be rearranged into the small-signal perturbations equations in the frequency domain as,

$$\Delta v_{\mathrm{c,ref}}(s) = K_C\big(\Delta i_{\mathrm{g,ref}}(s) - \Delta i_{\mathrm{g}}(s)\big). \tag{A4.9}$$

By rearranging (A4.9), (4.14) can be obtained.

F. Derivation of $G_{CON}(s)$

The averaged state equations of the AVG-BPFC are listed in the following,

$$C_{\mathrm{O}}\frac{dv_{\mathrm{O}}(t)}{dt} = -\frac{v_{\mathrm{O}}(t)}{R_{\mathrm{O}}} + i_{L1}(t)\cdot(1-D), \tag{A4.10}$$

$$L_1\frac{di_{\mathrm{L1}}(t)}{dt} = v_{\mathrm{C}}(t) - v_{\mathrm{O}}(t)\cdot(1-D), \tag{A4.11}$$

$$C_{\mathrm{AB}}\frac{dv_{\mathrm{C}}(t)}{dt} = i_{\mathrm{G}}(t) - i_{L1}(t), \tag{A4.12}$$

$$L_2\frac{di_{\mathrm{G}}(t)}{dt} = v_{\mathrm{IN}}(t) - v_{\mathrm{C}}(t), \tag{A4.13}$$

where *D* is duty cycle.

By considering $\Delta v_{\mathrm{o}}(t)$, $\Delta v_{\mathrm{c}}(t)$, $\Delta i_{L1}(t)$, $\Delta i_{\mathrm{g}}(t)$ and Δd as the small-signal perturbations of v_{O}, v_{C},i_{L1}, i_{G} and *D* respectively in the small signal analysis model, (A4.10) – (A4.13) can be rearranged into the small-signal perturbations equations in frequency domain a,

$$C_{\mathrm{O}}\cdot s\cdot\Delta v_{\mathrm{o}}(s) = \frac{-1}{R_{\mathrm{O}}}\cdot\Delta v_{\mathrm{o}}(s) - I_{L1}(s)\cdot\Delta d + \overline{D}\cdot\Delta i_{L1}(s), \tag{A4.14}$$

$$L_1 \cdot \Delta i_{L1}(s) \cdot s = \Delta v_{\mathrm{c}}(s) + V_{\mathrm{O}} \cdot \Delta d - \overline{D} \cdot \Delta v_{\mathrm{o}}(s), \tag{A4.15}$$

$$C_{\mathrm{AB}} \cdot \Delta v_{\mathrm{c}}(s) \cdot s = \Delta i_g(s) - \Delta i_{L1}(s), \tag{A4.16}$$

$$\Delta i_{\mathrm{g}}(s) \cdot L_2 \cdot s = -\Delta v_{\mathrm{c}}(s), \tag{A4.17}$$

where $\overline{D}$ equals to 1-*D*.

By combining (A4.14) - (A4.17), the transfer function of the converter stage, $\mathrm{G_{CON}}(s)$, can be obtained as,

$$\mathrm{G_{CON}}(s) = \frac{\Delta i_{\mathrm{g}}(s)}{\Delta d(s)} = \frac{2 \cdot V_{\mathrm{O}} \cdot (C_{\mathrm{O}} \cdot s + \frac{1}{R_{\mathrm{O}}})}{C_{\mathrm{O}} \cdot Z_{\mathrm{T}} \cdot s^4 + \frac{Z_{\mathrm{T}}}{R_{\mathrm{O}}} s^3 + [C_{\mathrm{O}} \cdot (L_1 + L_2) + \overline{D}^2 \cdot C_{\mathrm{AB}} \cdot L_2] \cdot s^2 + \frac{L_1 + L_2}{R_{\mathrm{O}}} \cdot s + \overline{D}^2}. \tag{A4.18}$$

G. Derivation of (4.17)

The system power equations are listed as follows,

$$p_{\mathrm{IN}}(t) = p_{\mathrm{O}}(t) + p_{\mathrm{C}}(t), \tag{A4.19}$$

$$p_{\mathrm{IN}}(t) = v_{\mathrm{IN}}(t) \cdot i_{\mathrm{G}}(t), \tag{A4.20}$$

$$p_{\mathrm{O}}(t) = \frac{v_{\mathrm{O}}(t)^2}{R_{\mathrm{O}}}, \tag{A4.21}$$

$$p_{\mathrm{C}}(t) = \frac{1}{2} \cdot C_{\mathrm{O}} \frac{d v_{\mathrm{O}}(t)^2}{dt}, \tag{A4.22}$$

where $p_{\mathrm{IN}}(t)$ is input power, $p_{\mathrm{O}}(t)$ is output power and $p_{\mathrm{C}}(t)$ is capacitor power.

By considering $\Delta p_{\mathrm{in}}(t)$, $\Delta p_{\mathrm{o}}(t)$,$\Delta p_{\mathrm{c}}(t)$, $\Delta i_{\mathrm{g}}(t)$ and $\Delta v_{\mathrm{o}}(t)$ as the small-signal perturbations of $p_{\mathrm{IN}}(t)$, $p_{\mathrm{O}}(t)$, $p_{\mathrm{C}}(t)$, $i_{\mathrm{G}}(t)$ and $v_{\mathrm{O}}(t)$ respectively in the small signal analysis model, (A4.19) - (A4.22) can be updated into frequency domain small-signal perturbations equations as,

$$\Delta p_{\mathrm{in}}(s) = \Delta p_{\mathrm{o}}(s) + \Delta p_{\mathrm{c}}(s), \tag{A4.23}$$

$$\Delta p_{\mathrm{in}}(s) = V_{\mathrm{IN}} \cdot \Delta i_{\mathrm{g}}(s), \tag{A4.24}$$

$$\Delta p_{\mathrm{o}}(s) = \frac{2 \cdot V_{\mathrm{O}} \cdot \Delta v_{\mathrm{o}}(s)}{R_{\mathrm{O}}}, \tag{A4.25}$$

$$\Delta p_{\mathrm{c}}(s) = C_{\mathrm{O}} \cdot V_{\mathrm{O}} \cdot s \cdot \Delta v_{\mathrm{o}}(s). \tag{A4.26}$$

By putting (A4.24) – (A4.26) into (A4.23), (4.17) can be obtained.

Reference

[4.1] K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, "Design, Implementation and Analysis of an Advanced Digital Controller for Active Virtual Ground-Bridgeless PFC," in *Proc. IEEE APEC*, pp. 52-59, Mar. 2017.

[4.2] J. Huh, S. W. Lee, W. Y. Lee, G. H. Cho, and C. T. Rim, "Narrow-Width Inductive Power Transfer System for Online Electrical Vehicles," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3666-3679, Jun. 2011.

[4.3] B. Esteban, M. Sid-Ahmed, and N. C. Kar, "A Comparative Study of Power Supply Architectures in Wireless EV Charging Systems," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6048-6422, Jun. 2015.

[4.4] S. Li and C.C. Mi, "Wireless Power Transfer for Electric Vehicle Applications," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 3, no. 1, pp. 4-7, Mar 2015.

[4.5] *Electric vehicle wireless power transfer (WPT) systems - Part 1: General requirements*, IEC Standard IEC 61980-1:2015, 2015.

[4.6] *Wireless Power Transfer for Light-Duty Plug-In Electric Vehicles and Alignment Methodology*, SAE Standard J2954_201605, 2016.

[4.7] *Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement*, IEC Standard IEC CISPR 11:2015, 2015.

[4.8] K. K. M. Siu and C. N. M. Ho, "A Critical Review of Bridgeless Power Factor Correction (PFC) Boost Rectifiers with Common-mode Voltage Mitigation," in *Proc. IEEE IECON*, pp. 3654-3659, Nov. 2016.

[4.9] C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, "Active Virtual Ground - Bridgeless PFC Topology," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017.

[4.10] R. T. H. Li, C. N. M. Ho, and X. Chen, "Active Virtual Ground – Single Phase Transformerless Grid-Connected Voltage Source Inverter Topology," *IEEE Trans. on Power Electron.*, vol. 33, iss. 2, pp. 1335-1346, Feb. 2018.

[4.11] J. Dannehl, C. Wessels, and F.W. Fuchs, "Limitations of Voltage-Oriented PI Current Control of Grid-Connected PWM Rectifiers with LCL Filters," *IEEE Trans. Ind. Electron.*, vol.56, no. 2, pp. 380-388, Nov. 2008.

[4.12] V. Blasko and V. Kaura, "A novel control to actively damp resonance in input LC filter of a three-phase voltage source converter," in *Proc. IEEE APEC*, vol. 33, no. 2, pp. 542-550, Mar. 1996.

[4.13] M. Liserre, A. Dell'Aquila, and F. Blaabjerg, "Genetic Algorithm-Based Design of the Active Damping for an LCL-Filter Three-Phase Active Rectifier," *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 76-86, Jan. 2004.

[4.14] C. Bao, X. Ruan, X. Wang, W. Li, D. Pan, and K. Weng, "Step-by-Step Controller Design for LCL-Type Grid-Connected Inverter with Capacitor–Current-Feedback Active-Damping," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1239-1253, Mar. 2014.

[4.15] K. K. S. Leung and H. S. H. Chung, “A comparative study of the boundary control of buck converters using first- and second-order switching surfaces,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1196-1209, Jul. 2007.

[4.16] Y. He, H. S. H. Chung, C. N. M. Ho, and W. Wu, “Use of Boundary Control With Second-Order Switching Surface to Reduce the System Order for Deadbeat Controller in Grid-Connected Inverter,” *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2638-2653, Jun. 2015.

[4.17] C. N. M. Ho, H. S. H. Chung, and K. T. K. Au, “Design and implementation of a fast dynamic control scheme for capacitor-supported dynamic voltage restorers,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 237-251, Jan. 2008.

[4.18] W. T. Yan, C. Ho, H. S. H. Chung, and K. T. K. Au, “Fixed-frequency boundary control of buck converters with second-order switching surface,” IEEE Trans. Power Electron., vol. 24, no. 9, pp. 2193-2201, Sept. 2009.

[4.19] C. N. M. Ho and H. S. H Chung, “Implementation and performance evaluation of a fast dynamic control scheme for capacitor-supported interline DVR,” *IEEE Trans. Power Electron.*, vol. 25, no. 8, pp. 1975-1988, Aug. 2010.

[4.20] K. K. S. Leung and H. S. H. Chung, “Derivation of a Second-Order Switching Surface in the Boundary Control of Buck Converters,” *IEEE Power Electronics Letter*, vol. 2, no. 2, pp. 63-67, Jun. 2004.

[4.21] W. Jiang, W. Ma, J. Wang, L. Wang, and Y. Gao, “Deadbeat Control Based on Current Predictive Calibration for Grid-Connected Converter Under Unbalanced Grid Voltage,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 7, pp. 5479-5491, Jul. 2017.

[4.22] J. Lee and K. Lee, “A Dead-Beat Control for Bridgeless Inverter Systems to Reduce the Distortion of Grid Current,” *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 6, iss. 1, pp. 151-164, Mar. 2018.

[4.23] J. Hu, “Improved Dead-Beat Predictive DPC Strategy of Grid-Connected DC–AC Converters With Switching Loss Minimization and Delay Compensations,” *IEEE Trans. Ind. Electron.*, vol. 9, no. 2, pp. 728-738, May 2013.

[4.24] M. H. L. Chow and C. K. Tse, “Theoretical Study of Performance of Continuous-Mode Boost Converters for Power-Factor-Correction Applications,” in *Proc. IEEE PEDS*, pp. 590-595, May 1997.

[4.25] K. D. Gussemé, D. M. V. D. Sype, A. P. M. V. D. Bossche, and J. A. Melkebeek, “Digitally Controlled Boost Power-Factor-Correction Converters Operating in Both Continuous and Discontinuous Conduction Mode” *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 88-97, Feb. 2005.

[4.26] P. Kong, S. Wang, and F. C. Lee, “Common Mode EMI Noise Suppression for Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291-297, Jan. 2008.

[4.27] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE 519-2014, 2014.

Chapter 5 A Four-Quadrant Single-phase Grid-connected Converter with only Two High Frequency Switches

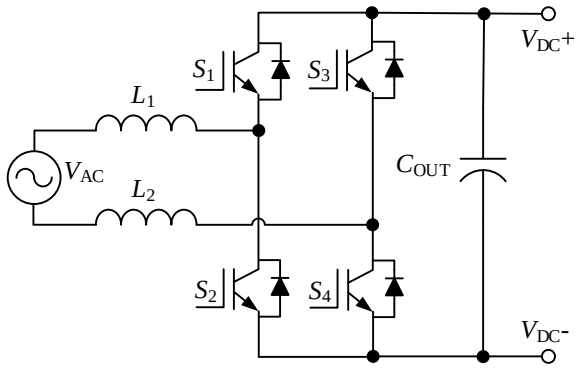
The work described in this chapter was published in the following paper: K. K. M. Siu, C. N. M. Ho, and R. T. H. Li, "A Four-Quadrant Single-Phase Grid-Connected Converter with only Two High Frequency Switches," *IEEE Trans. Ind. Electron.*, Early Access. The work was also presented in part as a conference paper at the 43rd Annual Conference of the IEEE Industrial Electronics Society 2017 [5.1].

5.1 Abstract

This chapter presents a new four-quadrant boost-type converter with the use of Active Virtual Ground (AVG) technology. The presented topology can step up the ac grid voltage to a regulated dc voltage under a stable bidirectional current flow and support the power transmission in either real power or reactive power delivery. With the use of the proposed modulation method, only two high frequency switches are required through the four-quadrant operation. Under a full-bridge converter structure, an efficient system can be guaranteed. Also, benefiting from the AVG technology, an *LCL* filter is formed at the system input over the four-quadrant operation. Both magnitudes of leakage current and grid current ripple are also minimized into a small value. Thus, a high efficiency and low noise four-quadrant converter is guaranteed. The presented topology is successfully implemented on a 750 VA prototype and the performance is experimentally verified on it which shows good agreement with the theoretical knowledge.

5.2 Introduction

Recently, controlling reactive power plays an important role in power applications for smart grids. Especially, in a Plug-In Electric Vehicle (PEV) system, by using a bidirectional rectifier charger, it is able to support both grid-to-vehicle and (G2V) and vehicle-to-grid (V2G) applications for both charging and discharging operations. The V2G function can help to optimize the energy distribution over a power transmission system. Thus, the cost of an energy distribution system is lower as the system offers more flexibility in energy delivery and more stability in available energy capacity [5.2], [5.3]. Meanwhile, in smart homes and smart grids, [5.4] - [5.6], sometimes a certain percentage of reactive power (Q) may be generated. They are caused by the connection of reactive electrical loads, such as motors or fluorescent lamps with inductive ballast. With the use of a four-quadrant (4Q) converter, these reactive powers can be compensated. A better grid power quality is achieved with a unity power factor through the overall system and a more efficient power transmission system is obtained.



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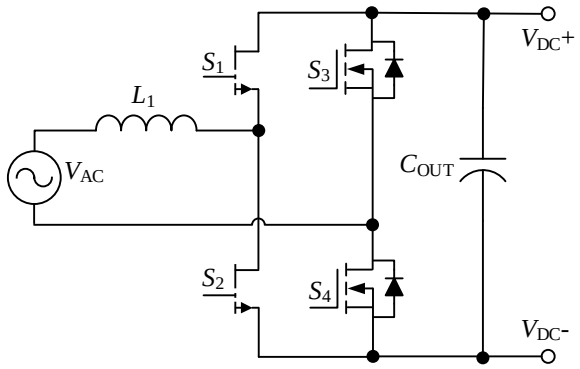

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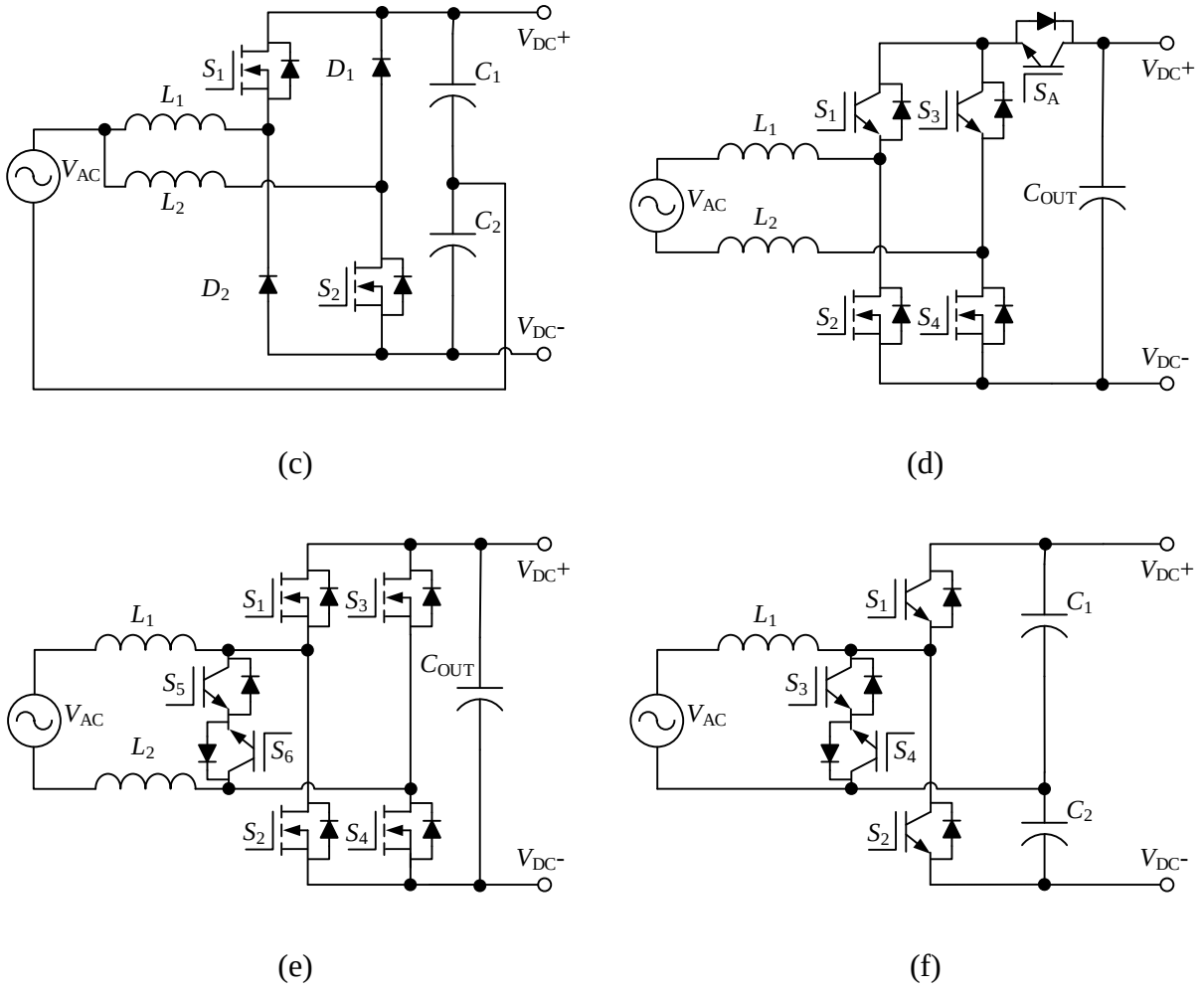


Figure 5-1. Different kinds of four-quadrant (4Q) converter, (a) full-bridge, (b) Totem-pole, (c) half-bridge dual-buck, (d) H5, (e) Heric and (f) Conergy-NPC.

In the past few years, many researchers and scientists have been working on the 4Q converter designs. Some soft switching isolated ac-dc converter solutions were presented in [5.7], [5.8] with the aim of high efficiency and low common mode (CM) noise. However, transformer and soft switching control are required which let the system design become more complicated. Generally, the non-isolation type 4Q converters are built by different kinds of full-bridge converter designs [5.9] - [5.22]. In order to generate a low leakage current system in the conventional full-bridge converter, as shown in Figure 5-1 (a), a 2-level switching scheme is usually applied on it [5.9] -

[5.11]. Under the bipolar switching scheme, reactive power injection is achieved and the system leakage current can be maintained in a small value. However, high switching losses appear in those devices which limit the increment of system efficiency. At the same time, a fast recovery diode is required for all the high frequency (HF) switches which will limit the selection of devices. IGBT is one of the options, but the tail current limits the maximum switching frequency of the converter. Totem-pole converter [5.12], [5.13], as shown in Figure 5-1 (b), is another possible solution on a 4Q converter design. The topology is in a simple structure and the resultant CM noise is minimized. Compared to other topologies, the switching pair of the totem-pole converter is always kept in the left leg. Therefore, the power dissipation per HF device is higher. Also, shoot-through issue and reverse recovery problem are required to be considered in the selection of devices. In this case, MOSFET is only suitable for discontinuous mode or critical mode operation. Thus, for a HF applications, the latest wide-bandgap semiconductor, GaN HEMT, would be required. Half-bridge dual buck system, [5.14], is another reactive power solution which is shown in Figure 5-1 (c). The working principle is similar to a half-bridge converter where each inductor is only responsible to handle the power conversion in half of the line cycle. Although only two active switches are required, however, a higher breakdown voltage is required. Meanwhile, the utilization of devices are lower than other topologies. H5, as shown in Figure 5-1 (d), is another topology that supports with reactive power injection. It provides effective power conversion and is electrically isolated the system from CM noise. Based on the foundation of [5.23] and [5.24], a reactive power modulation scheme was proposed in [5.15], [5.16]. However, one more switch is involved in the current conduction path which results in higher conduction loss than others. Similar to H5, there are another two types of converters which are called H6 [5.17], [5.18] and FB-DCB [5.19]. H6 has a similar operation principle as H5 but more device is required. In FB-DCB, extra switches and diodes are added to build the dc bypass circuit. However, higher semiconductor conduction losses

are generated. Heric, as shown in Figure 5-1 (e), is another type of electrically isolation topology which is available to support reactive power capability. Based on the foundation of [5.25] and [5.26], a reactive power modulation scheme was proposed by [5.16]. However, higher switching losses are resultant in the entire system. Also similar to Heric, there is another variant which is called HB-ZVR [5.20]. It replaces the bidirectional current switch by a single MOSFET and a diode bridge. Also, an extra diode is added to clamp the common mode noise. Conergy-NPC, [5.21], [5.22], is another type of topology that can support reactive power injection and with fewer semiconductor requirements. The topology diagram is shown in Figure 5-1 (f). One end of the grid is always connected to the middle point of the dc to eliminate the common mode noise of the system. However, the device breakdown voltage is double. Also similar to others, fast recovery diodes are required on the active switches, the usage of MOSFETs are limited. Therefore, either the device utilization is low or the requirement of fast recovery diode limits the selection of devices. A topology summary is given in TABLE 5-I.

TABLE 5-I SUMMARY OF NUMBERS OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topology	No. of Switches			No. of Diodes	No. of Components in the Main Current Path (Rectifier Mode)		I/P Filter	O/P Cap.
	HF and Need Freewheeling Diode	HF and Need not Freewheeling Diode	LF		Turn-on	Turn-off		
Figure 5-1 (a)	4	0	0	0	2	2	*L*	*C*
Figure 5-1 (b)	2	0	2	0	2	2	*L*	*C*
Figure 5-1 (c)	0	2	0	2	1	1	*L*	*2C*
Figure 5-1 (d)	5	0	0	0	2	3	*L*	*C*
Figure 5-1 (e)	6	0	0	0	2	2	*L*	*C*
Figure 5-1 (f)	4	0	0	0	2	1	*L*	*2C*
Figure 5-2	0	2	10	0	2	2	*LCL*	*C*

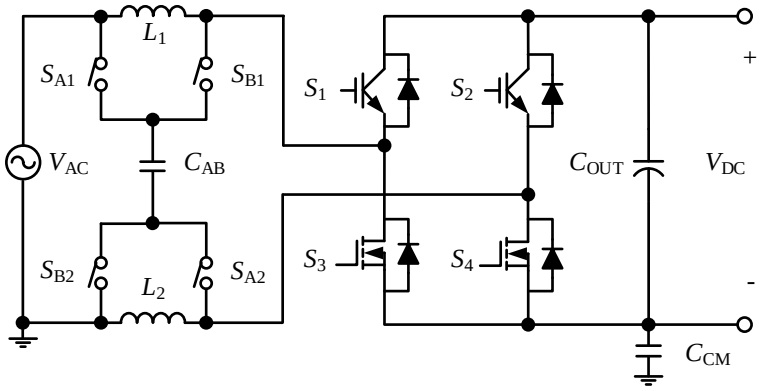


Figure 5-2. Circuit of the proposed 4Q AVG converter.

In this chapter, a new 4Q boost type converter is presented, as shown in Figure 5-2, under the Active Virtual Ground (AVG) converter family [5.27] - [5.29]. Different from [5.27] and [5.28], the proposed 4Q AVG converter is in another type of connection method. Based on the proposed modulation scheme, only two HF semiconductor switches are required. The circuit freewheeling path is not located in the HF switch, thus, MOSFET can be used in the circuit as the main switch. Without the tail current in the switching device, the switching frequency of the overall system can be increased and a reduction in power density is achieved. Also, all the time only two semiconductors are conducting in the main current path and only either one of them is in HF switching. A highly efficient system can be realized. Moreover, during the circuit operation, an *LCL* input filter is generated at the front state which helps to clamp CM noise generated by the system and to minimize HF ripple in the grid current. As a result, the overall HF noise is reduced [5.27]. The system operation can be divided into four different operation modes. Based on the phase requirement, it can be in either real power conversion (*P*) or reactive power injection. The proposed modulation scheme and the circuit operation are presented in detail. Also, the controller design is described in this chapter. A 750 VA prototype is successfully implemented to verify the proposed topology. Those experimental results are matched with theoretical findings.

5.3 Proposed Reactive Power Modulation Scheme in Active Virtual Ground Converter

5.3.1 Operation Principle of the Proposed System

In Figure 5-2, it shows that in the proposed topology, the main circuit is a traditional full-bridge converter circuit. On top of that, an AVG circuit is implemented at the front state and is combined together as a new topology. The AVG circuit is formed by four bidirectional switches (S_{A1}, S_{A2}, S_{B1} and S_{B2}) and one HF capacitor (C_{AB}). S_{A1} and S_{A2} are synchronized together and are grouped as S_A. S_{B1} and S_{B2} are synchronized together and are grouped as S_B. By changing the switching status of the AVG switches, different *LCL* filters are formed between the grid terminals and the switching legs. Under the proposed modulation method, only switches S_3 and S_4 are required to operate at high voltage (HV) and HF. The others are all line frequency (LF) switches. Switches S_1 and S_2 are with HV but in LF operation which can be implemented by IGBT. Likewise, the bidirectional switches are in LF operation which can be implemented by a pair of low voltage switches with a source-to-source connection. In Figure 5-2, a capacitor, C_{CM}, is applied to simulate the parasitic capacitor of the system. It is located between the dc bus terminal and the ac ground.

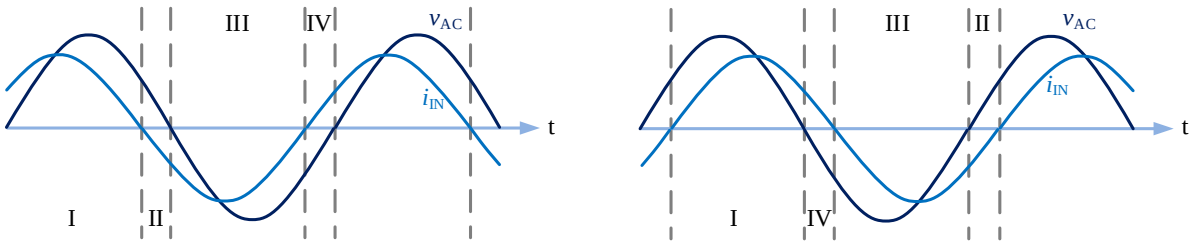


Figure 5-3. Grid current and voltage waveforms at (a) capacitive mode and (b) inductive mode.

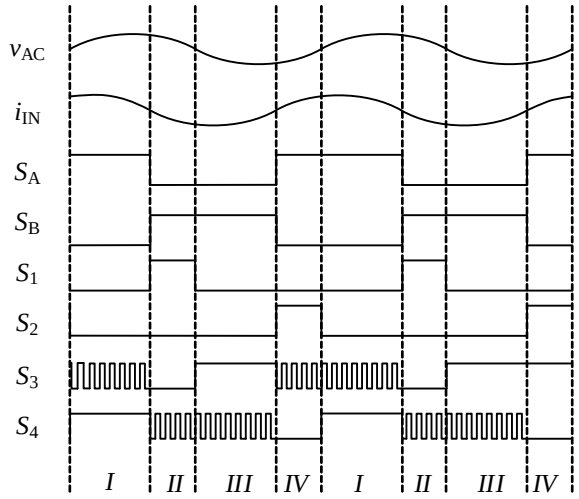


Figure 5-4. Detailed switching actions in capacitive mode operation.

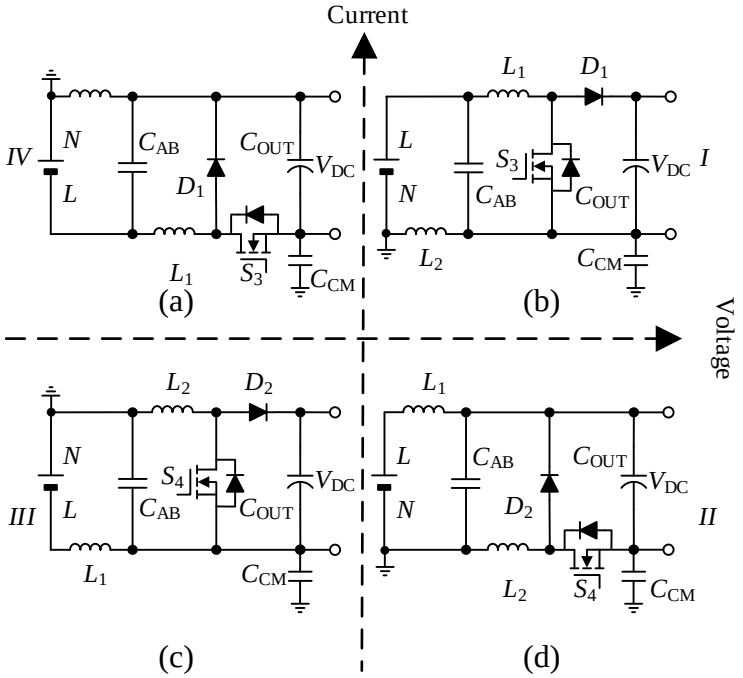


Figure 5-5. Equivalent circuits of the proposed 4Q system in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

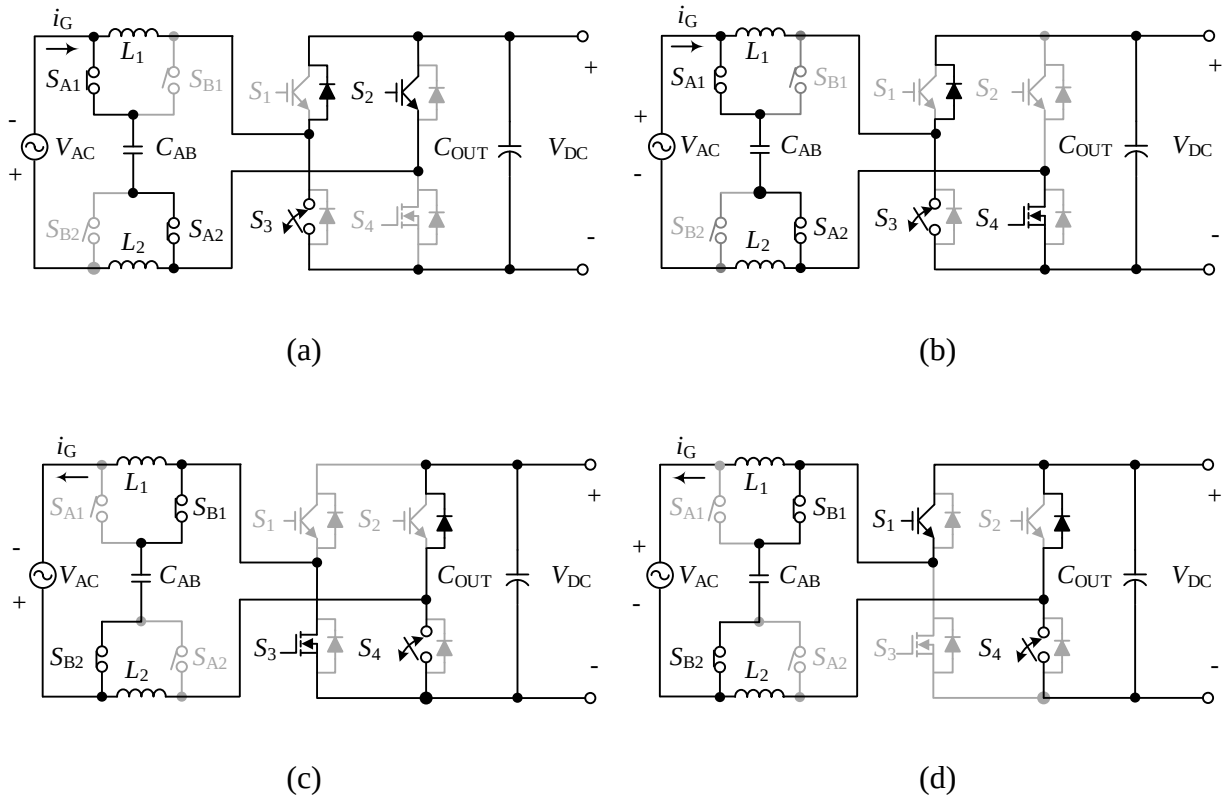


Figure 5-6. Switching diagrams in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

Based on different application requirements, the system operation mode can be changed from real power delivery to either capacitive or inductive modes easily by varying the phase inside the system controller. The detailed operations of capacitive mode are shown in Figure 5-3 (a) which is separated into four different operation sections and the detailed switching actions of the modulation are shown in Figure 5-4. Similarly, there are 4 sections as well in the inductive mode as shown in Figure 5-3 (b). By applying the proposed 3-level modulation scheme, there is only one HF switch, which is used to process the power conversion in each switching state. Based on the switching sequence in Figure 5-4, the corresponding switching diagram and the corresponding equivalent circuit of the proposed topology are able to be found and are shown in Figure 5-5 and Figure 5-6, respectively. The operation mode selections are determined by both of the current and

voltage directions. The amount of real power through the system is controlled by the phase angle. From the apparent power (S) equation, the rms value of grid current, $I_{G,rms}$, can be expressed as,

$$I_{\mathrm{G,rms}} \cdot V_{\mathrm{AC,rms}} \cdot \cos\theta = P_{\mathrm{O}} \rightarrow I_{\mathrm{G,rms}} = \frac{P_{\mathrm{O}}}{V_{\mathrm{AC,rms}} \cdot \cos\theta}, \tag{5.1}$$

where $V_{\mathrm{AC,rms}}$ is rms value of grid voltage , θ is phase angle between the grid voltage and current and P_{O} is dc output power.

In Mode I, according to Figure 5-4, both input voltage and grid current are also positive. S_3 works with HF ON-OFF as a converter switch and S_4 is always ON to provide a circuit current returning path, which is shown in Figure 5-5 (b). The operation is equivalent to a boost converter as Figure 5-6 (b). S_{A} is always ON at this operation mode and connects C_{AB} to the LINE (L) terminal and the drain of S_4. At the input, an *LCL* filter is formed in which inductor L_1 becomes a converter-side inductor and inductor L_2 becomes a grid-side inductor. C_{AB} help to clamp the HF voltage ripple coupling to the grid.

In Mode II, according to Figure 5-4, the input voltage is positive with a negative grid current. S_4 works with HF ON-OFF as a converter switch and S_2 is always ON to provide a circuit current returning path, which is shown in Figure 5-5 (d). The operation is equivalent to an inverted buck circuit as Figure 5-6 (d). Different from Mode I, the *LCL* filter is generated by connecting C_{AB} to the NEUTRAL (N) terminal and the drain of S_3 through conduction of S_{B}. L_1 acts as a grid inductor and L_2 acts as a converter inductor. The voltage of C_{AB} keeps following the ac voltage and clamps the HF voltage ripple in the grid.

In Mode III, according to Figure 5-4, both input voltage and grid current are also negative. S_4 works with HF ON-OFF as a converter switch and S_3 is always ON to provide a circuit current returning path, which is shown in Figure 5-5 (c). The operation is equivalent to a boost converter

as Figure 5-6 (c). S_B is always ON at this operation mode and C_{AB} has the same connection as Mode II. Therefore, comparing to Mode II, the same *LCL* filter is from in which L_2 becomes a converter-side inductor and L_1 becomes a grid-side inductor. And C_{AB} help to clamp the HF voltage ripple coupling to the grid.

In Mode IV, according to Figure 5-4, the input voltage is negative with a positive grid current. S_3 works with HF ON-OFF as a converter switch and S_1 is always ON to provide a circuit current returning path, which is shown in Figure 5-5 (a). The operation is also equivalent to an inverted buck circuit as Figure 5-6 (a). Same as Mode I, the same *LCL* filter is generated by conducting S_A where C_{AB} is used as filter capacitor to clamp the HF voltage ripple, L_2 becomes a grid inductor and L_1 act as a converter inductor.

The system duty is varying over the four-quadrant operation. At modes I and III, the circuit is operated as a boost converter where the corresponding duty cycle, $D_{\mathrm{I/III}}$, can be expressed as,

$$D_{\mathrm{I/III}} = 1 - \frac{V_{\mathrm{AC}} \cdot \sin\omega t}{V_{\mathrm{DC}}}, \tag{5.2}$$

where ω is angular line frequency, V_{AC} is peak input voltage and V_{DC} is output voltage.

At modes II and IV, the circuit is operated as a boost converter where the corresponding duty cycle, $D_{\mathrm{II/IV}}$, can be expressed as,

$$D_{\mathrm{II/IV}} = \frac{V_{\mathrm{AC}} \cdot \sin\omega t}{V_{\mathrm{DC}}}. \tag{5.3}$$

From (5.2) and (5.3), they show that the duty is different in each operation mode. When the operation mode exchanges between real power and reactive power operation, the duty cycle is totally inverted. So extra care is required when designing the system controller.

5.3.2 High Frequency Models

By applying HF analysis method to the equivalent circuits in Figure 5-5, the corresponding HF models are obtained as shown in Figure 5-7 [4.8]. In the analysis, ac source and dc load are considered as short-circuit, MOSFET is considered as the noise source of the system and the grid-side inductor is considered as open-circuit. Accordingly, regardless of the ground tapping point on the dc link, there is no change in the HF model. In all four modes of operation, the system results in the same set of HF equivalent models. The models are used to analyze the EMI performance of the system. On the EMI analysis, system noises can be classified into two types which are differential mode (DM) noise and CM noise. The DM noise is related to the magnitude of HF grid current ripple. The CM noise is related to the leakage current induced in C_{CM}.

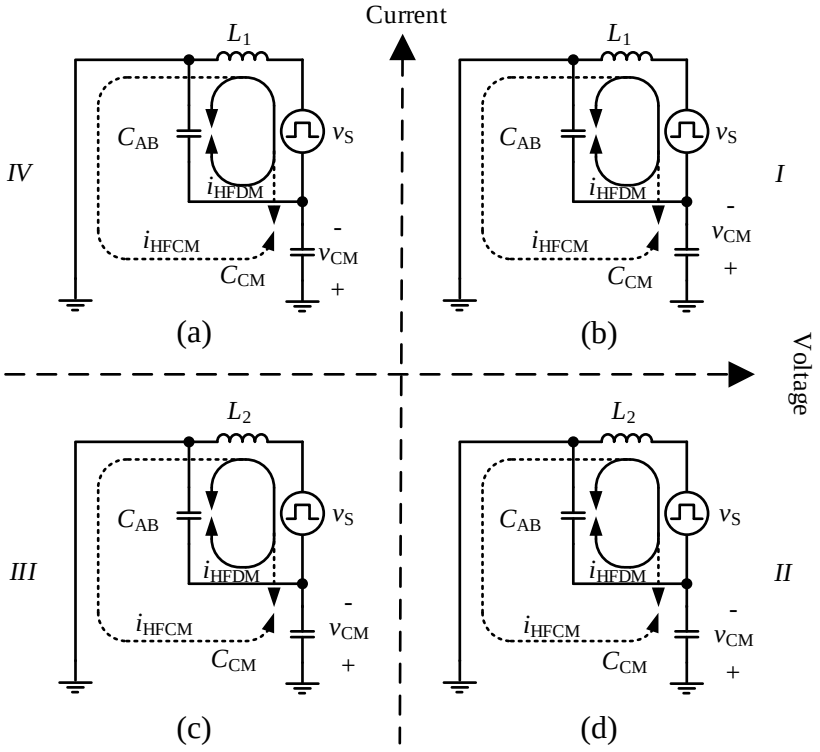


Figure 5-7. High frequency models of the proposed 4Q system in (a) Mode IV, (b) Mode I, (c) Mode III and (d) Mode II.

From the characteristic of the proposed 4Q AVG converter, at every operation modes, there is always an *LCL* filter structure generated in the circuit input. Those HF DM current information, i_{HFDM}, is passing through C_{AB} and circulate inside the converter. The grid-side inductor only carries the LF current. As a result, in the DM noise part, the influence from the HF inductor current ripple can be minimized.

In a general unipolar full-bridge converter, C_{CM} is parallel to a converter inductor in which a high leakage current has resulted from the HF and HV switching [4.8]. The HF leakage current is considered as CM noise current, i_{HFCM}. In the presented circuit, due to the input filter structure, C_{CM} is always paralleling to C_{AB}. The voltage waveform of C_{AB} is always synchronized with V_{AC} and the voltage ripple is always maintained in a small value, thus, the induced system leakage current can be controlled in a small value. Referred to [5.27], the magnitude of the HF leakage current can be calculated as,

$$\Delta i_{HFCM}(t) = \frac{C_{CM}}{C_{AB}+C_{CM}} \Delta i_L(t), \tag{5.4}$$

where Δi_L is magnitude of HF inductor current.

As a result, the CM noise issue in a converter is mitigated. The overall system noise can be maintained at a low magnitude level.

5.4 Controller Design and Implementation

5.4.1 Controller Design

In the control architecture, as shown in Figure 5-8, a double loop control methodology is applied to generate the proposed 3-level modulation switching signals. The outer loop is an output

dc voltage loop and the inner loop is an inductor current loop. The whole control is implemented digitally in a DSP. Two sets of voltage sensors are applied to sense the output voltage, V_O, and the grid voltage, V_G. Also, two sets of current sensors are applied to sense both of the inductor currents, I_{L1} and I_{L2} respectively.

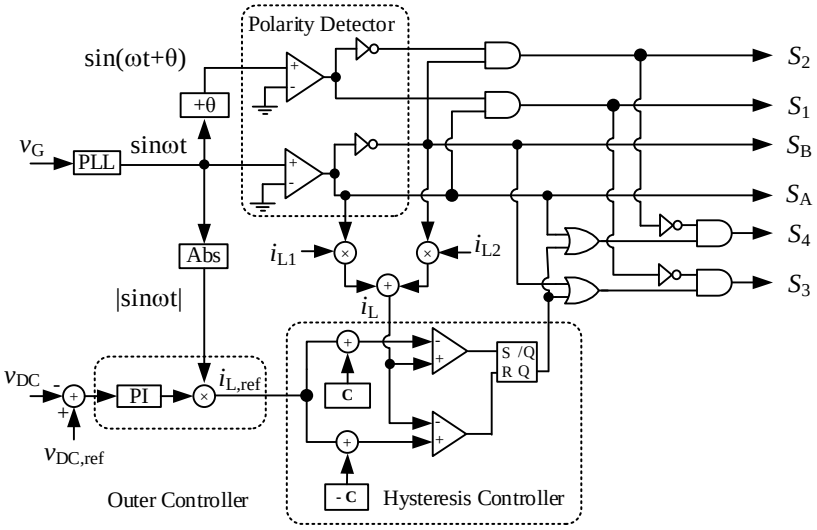


Figure 5-8. Control circuit of the proposed 4Q AVG converter.

In the design, a PLL is applied to the input voltage and is used to generate a synchronized sinusoidal reference for the controller. With the use of the sinusoidal reference and a predefined phase angle, an input current reference is generated and is applied to the inner loop control. Through the polarity detector, both voltage and current directions are identified. So that all four modes are distinguished. S_1 and S_2 are under LF operation. They are only assigned with a switching signal when reactive power operation is required. Both S_3 and S_4 are under HF operation individually. The corresponding control signals are generated from the selection of operating mode and the assigned duty reference. The control signals of S_A and S_B are LF operation and depend on the polarity of the grid current direction. By switching the AVG switches alternatively, various *LCL* filters are built at the system input and are constructed by different connection methods of

C_{AB}, L_1 and L_2 in every half line cycle. All the time only one switch is under HF operation and the others are in LF operation.

In the control scheme, the outer loop is an output voltage control where a PI controller is applied. Reference to [5.29], Kp and Ki are selected as 0.00051 and 0.047 respectively. Its major control objective is to maintain a stable dc bus voltage during power conversion and to avoid a large voltage fluctuation during any transient conditions. The output of the outer loop is an inductor current reference. The system inner loop is an inductor current control. During the mode exchange, there is a dramatic change in duty ratio between (5.3) and (5.4). However, obtaining a step change is a challenge for a linear control method. A certain time period is required to handle the transient process. As a result, the current shape is distorted before the time that the controller can lock back the reference. In order to provide a fast current response in the system inner loop, a hysteresis controller is applied to control inductor current, I_L, and to maximize the power quality of the system. I_L is combined from the current information of L_1 and L_2, I_{L1} and I_{L2}, by synchronizes with the target current polarity. Benefit from the non-linear characteristics of the controller, fast dynamic switching action is able to be guaranteed. It can provide a precise current tracking function which promises the high quality input current. Especially on the transition between real power and reactive power operations, the advantage of hysteresis control is more obvious. Therefore, the system power factor is enhanced and a better system THD is obtained.

In a digital platform, during the mode exchange between the power and reactive power operations, two possible current distortions are generated. The first one comes from digital sampling error, as shown in Figure 5-9. At the zero voltage point, the duty cycle of real power transfer is close to one and the corresponding duty cycle of reactive power transfer is close to zero. In the digital control, the ADC sampling point is fixed and the sampling frequency is limited.

During the fast changing of current magnitude, sampling error is generated. Also, it results that the inductor current is easier to exceed the current band. Especially at the voltage zero crossing position, an obvious current step is generated by the sampling error after the operation mode is exchanged and a grid current distortion is resulted due to a slightly mismatching on the average current magnitude. From the inductor off-state equation during real power operation and the inductor on-state equation during real power operation, the maximum current sampling error, Δi_{error}, can be found as,

$$\Delta i_{\text{error}} = \frac{2V_{\text{DC}}}{f_{sampling} \cdot L_{\text{X}}}, \tag{5.5}$$

where L_{X} is inductance of converter-side inductor and $f_{sampling}$ is sampling frequency of digital controller.

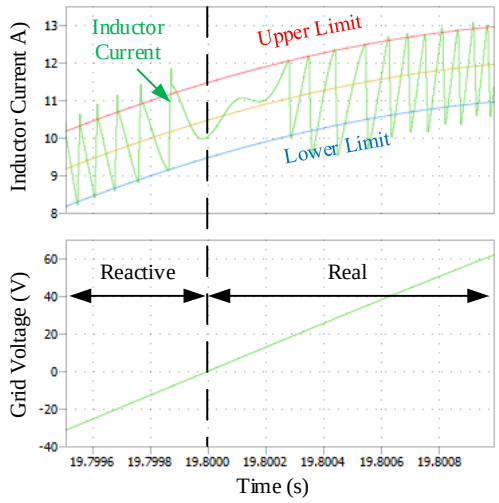


Figure 5-9. Simulation waveform of capacitor mode operation.

Another distortion is generated from the energy point of view. Similar to the current distortion as a general boost stage PFC [5.17] and [5.31]. During the voltage zero crossing region, the input voltage becomes zero but a large current magnitude is needed on the inductor to satisfy the energy

demand in power conversion. Therefore, it is not enough energy to magnetizing the converter inductor and leads that the current waveform is distorted for a certain period. The distortion period can be shorter by either reducing the inductance value to shorten the magnetizing time or limiting the boundary width in the hysteresis control in order to smooth the waveform. According to [5.31], the distortion period during zero crossing, β, is calculated as,

$$\beta = \frac{2}{\omega} \cdot \tan^{-1}\left(\frac{2 \cdot \omega \cdot L_X \cdot S \cos\alpha}{{V_{AC}}^2 + 2 \cdot \omega \cdot L_X \cdot S \sin\alpha}\right). \tag{5.6}$$

where α is angle that the applied in the current reference.

5.4.2 Selection of the Current Ripple Magnitude

In order to choose a suitable current ripple magnitude, ΔI, in the hysteresis control, the maximum available switching frequency, f_{SW}, is required to know. The expression of switching frequency can be found from the steady state characteristic of each mode. During real power operation, the corresponding on-state inductor voltage, $V_{L,ON,I/III}$, is,

$$V_{L,ON,I/III} = V_{AC} \cdot \sin\omega t = L_X \cdot \frac{\Delta I \cdot f_{SW}}{D_{I/III}}. \tag{5.7}$$

By combining (5.2) and (5.7), f_{SW} can be obtained as,

$$f_{SW} = \frac{V_{AC} \cdot \sin\omega t}{V_{DC}} \cdot \frac{V_{DC} - V_{AC} \cdot \sin\omega t}{L_X \cdot \Delta I}. \tag{5.8}$$

During reactive power operation, the corresponding on-state inductor voltage, $V_{L,ON,II/IV}$, is defined as,

$$V_{L,ON,II/IV} = V_{DC} - V_{AC} \cdot \sin\omega t = L_X \cdot \frac{\Delta I \cdot f_{SW}}{D_{II/IV}}. \tag{5.9}$$

By combining (5.3) and (5.9), the switching frequency has the same expression as (5.8). Therefore, under the same boundary value, the mode transition between real power and reactive power can have a smooth interaction. From (5.8), it shows that under a constant current band, the maximum switching frequency point is located at the maximum input voltage point. As a result, by putting in the system parameters and the maximum available switching frequency into (5.8), a suitable current band can be found. The hysteresis band is inversely proportional to the switching frequency, it means that increasing switching frequency could reduce current ripple but lower in system efficiency due to increased switching loss at each device. Thus, a device with low parasitic capacitance and fast transient behavior is recommended for S_3 and S_4 in HF applications. In our design, the inductor is selected to 1.2 mH. Therefore, 2 A is selected as the current band which helps to limit the switching frequency within a 30 kHz range.

5.4.3 Selection of Components

In each state, only one semiconductor switch is under HF switching. S_3 is in HF switching during positive current flow and S_4 is forced to be in HF switching during the negative current condition. MOSFETs, IPW60R070C6, are selected to implement as the HF and HV switches of S_3 and S_4. S_1 and S_2 are both LF switches which only operate at modes II and IV to provide a current returning path for the delivery of reactive power. In order to provide a fast reverse recovery performance during the freewheeling process, IGBTs with fast recovery anti-parallel diode, IKW20N60H3, are selected to implement as S_1 and S_2. All of AVG switches are implemented by LF MOSFETs, STB46NF30, in a source-to-source configuration as shown in Figure 5-10. The path of the AVG circuit is only required to handle the HF current ripple, therefore, losses on the AVG switches are not that significant. An estimated loss breakdown is shown in Figure 5-11,

which is done at the full power rating condition in rectifier mode operation. It shows that under 2A current band, the losses in the AVG switches are only contributed 1 % of the overall loss. Thus, losses on top are little and no extra heatsink is required. All the AVG switches can be mounted on a daughter board and do the cooling through the PCB.

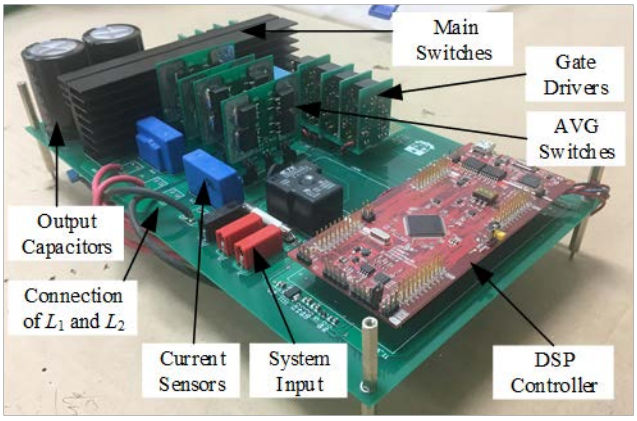


Figure 5-10. Experimental prototype.

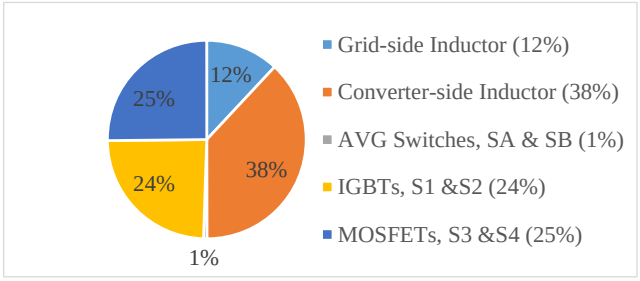


Figure 5-11. Loss breakdown in proposed converter under full power rating.

5.5 Experimental Verification

A 750 VA test platform, as shown in Figure 5-10, is built to verify the proposed 4Q AVG converter and the conditions of the system are shown in TABLE 5-II. In our design, 2 A is selected

as the inductor current band and the maximum switching frequency is 26 kHz. According to [5.27], a 3.3 µF film capacitor is selected as the circuit filter capacitor.

Figure 5-12 shows that the converter has a stable operation under different operation modes where all the testing points are with full rated power rating. When the power direction was positive, a 120 Vac voltage source, ac output mode of Keysight AC6803A, was applied to the system input and a group of resistive loads was connected to the system output as a power load. According to the system specification, the output voltage was regulated at 250 Vdc. In Figure 5-12 (a), it shows the steady state performance of the system during a 750 W real power test case. Under the same apparent power rating, a waveform that operating at capacitive shown in Figure 5-12 (c) where a positive 60˚ is applied to the reference grid current. In Figure 5-12 (d), it demonstrates the system operation at inductive mode operation with a negative 60˚ on the reference grid current. When the power direction was inverted, a 250 Vdc voltage source, dc output mode of Keysight AC6803A, was applied to C_{OUT} and the input side was directly connected to the 120 Vac grid with a pre-defined current magnitude. In Figure 5-12 (b), it shows the system steady state performance at inverter mode operation.

TABLE 5-II VALUE OF THE SYSTEM PARAMETERS THAT USED IN THE DESIGN

Parameter	Value	Parameter	Value
Input Voltage	120 Vac	Output Voltage	250 Vdc
Input Frequency	60 Hz	Output Power	750 W
Current Band	2 A	Output Capacitor	1.2 mF
Inductor (L_1 & L_2)	1.2 mH	Capacitor (C_{AB})	3.3 µF

As shown in Figure 5-12 (a) – (d), under the hysteresis control, a fast dynamic response is provided. The inductor current was all the time switching within the boundary. During the operation, an *LCL* was formed at the converter input. In the positive current cycle, the set of AVG

switch S_A was ON. Inductor L_1 acted as a converter-side inductor and took care of the HF ripple. Inductor L_2 acted as a grid-side inductor and carried the 60 Hz current information. Both inductors were connected with the filter capacitor C_{AB} to form an *LCL* input filter. During the negative current cycle, the inductor role was changed. With the connection of C_{AB} through S_B, another set of *LCL* was formed. Inductor L_1 became a grid-side inductor and carried the 60 Hz current information. Inductor L_2 became a converter-side inductor and took care of the HF ripple.

By switching the AVG switches alternatively, the filter capacitor voltage was following to the grid voltage. A set of experimental tests is done to verify the operation of the AVG switch. S_A is monitored during the test and the result is shown in Figure 5-13. As shown in Figure 5-13 (a), the control signal of S_A is under LF operation. S_A was ON when the current polarity is positive. The current passing through S_A was the filter capacitor current which was equal to the HF current ripple in the converter-side inductor. Under the hysteresis control, the ripple was kept within the current band. S_A was OFF when the current polarity was negative. As shown in Figure 5-13 (b) and (c), the voltage stress on S_{A1} and S_{A2} are different. The voltage applied on top of S_{A1} was equal to the voltage ripple on top of the grid-side inductor which was generated from the difference between grid voltage and filter capacitor voltage. The voltage applied on S_{A2} was the same as the voltage ripple appeared on the converter-side inductor. The voltage stress on S_{A2} was more significant than the voltage stress on S_{A1}, as the converter-side inductor was aimed for energy transfer. Similarly, the same performance was occurred in S_B.

During the operation, the HF voltage ripple was kept in a relatively small value. Thus, the resultant system CM noise would be small as well. Reference to [5.29], [5.32], a 330 pF capacitor was applied to the system to simulate the parasitic capacitance of the system. The resultant leakage current of the system during rectifier mode, inverter mode, capacitive mode and inductive mode

operation are measured and are shown in Figure 5-14 (a), (b), (c) and (d) respectively. In all the cases, the magnitudes of the leakage current were also maintained in 2 mA range. All the results have a very good alignment with the topology concept and meet the design target.

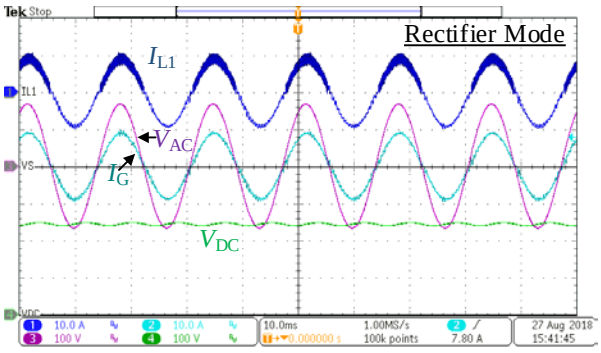
Under the steady state situation, the system was performance well. In both rectifier mode and inverter mode operations, the system power factor (PF) was always kept higher than 0.9. In rectifier mode, the PF was 0.997. Meanwhile, in inverter mode, the PF was 0.990. At the full power operation, the efficiency in rectifier mode was 96.98 % where the current THD was 3.632 %. Similarly, in inverter mode operation, the system efficiency was 96.83 % together with a 3.85 % current THD. In both cases, each THD magnitude was also within the requirement of IEEE 519 [5.33]. A summary of the test results is shown in TABLE 5-III.

In reactive power operation, the system performance was also maintained well. In Figure 5-12 (c), during capacitive mode testing, a positive 60˚ was applied to the reference grid current. In contrast, during inductive mode testing in Figure 5-12 (d), a negative 60˚ was applied to the reference grid current. In both cases, the apparent power was 750 VA and real power was half of it. The system efficiency in capacitive and inductive modes were 93.84 % and 93.48 % respectively. The system efficiency was slightly reduced when reactive power injection was required. Under the same apparent power level, the input current amplitude remained the same, which caused the device losses on these switches and inductors to keep at a similar level. However, during capacitive mode or inductive mode operation, the real power consumption was reduced. Therefore, the overall system efficiency was relatively low. An efficiency figure is shown in Figure 5-15, which demonstrates the relationship between system efficiency and system phase angle under the same apparent power condition. Meanwhile, in both test cases of Figure 5-12 (c) and (d), the current THD can also be kept in the 5 % range. The current THD in capacitive modes and

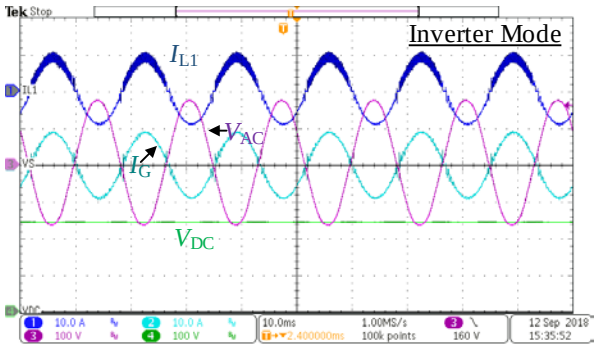
inductive were 4.81 % and 4.91 % respectively. Effective power conversion can be achieved in all four operation modes.

TABLE 5-III SUMMARY OF THE TEST RESULTS

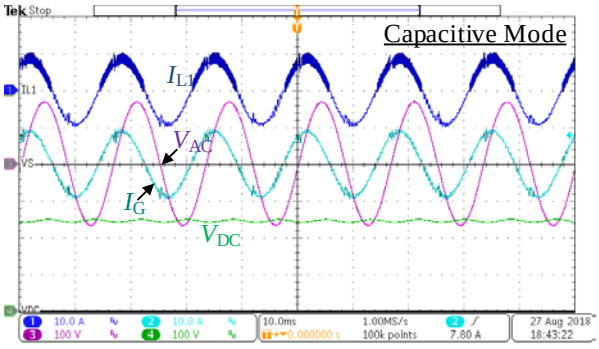
Operation Mode	Figure 5-12	I_{rms} /A	P /W	Q /VA	η /%	THD /%	PF
Rectifier	(a)	6.49	771	0	96.98	3.63	0.997
Inverter	(b)	6.48	-780	0	96.83	3.85	0.990
Capacitive	(c)	6.54	393	-676	93.84	4.81	0.503
Inductive	(d)	6.55	380	684	93.48	4.91	0.485



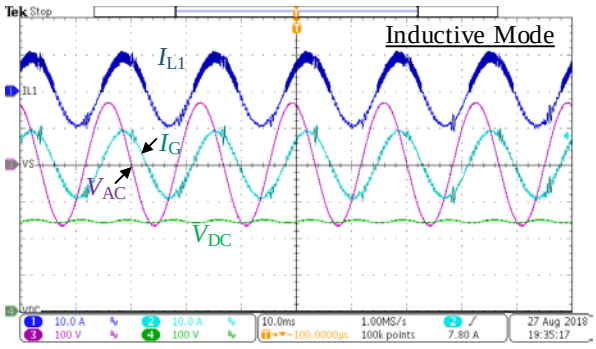
(a)



(b)

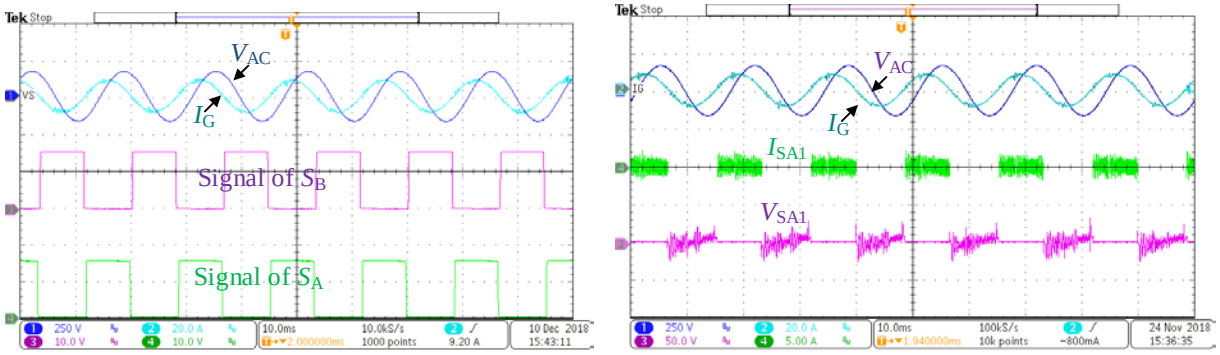


(c)

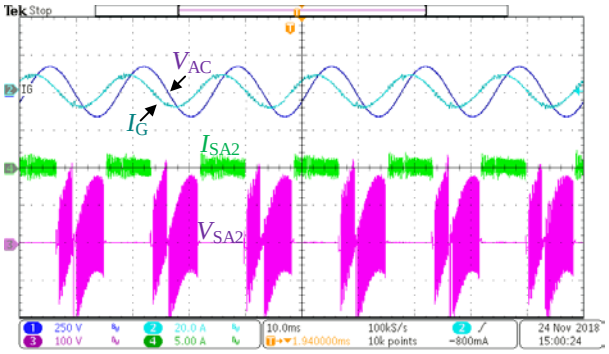


(d)

Figure 5-12. Experimental results of steady state performance: (a) rectifier mode, (b) inverter mode, (c) capacitive mode and (d) inductive mode.

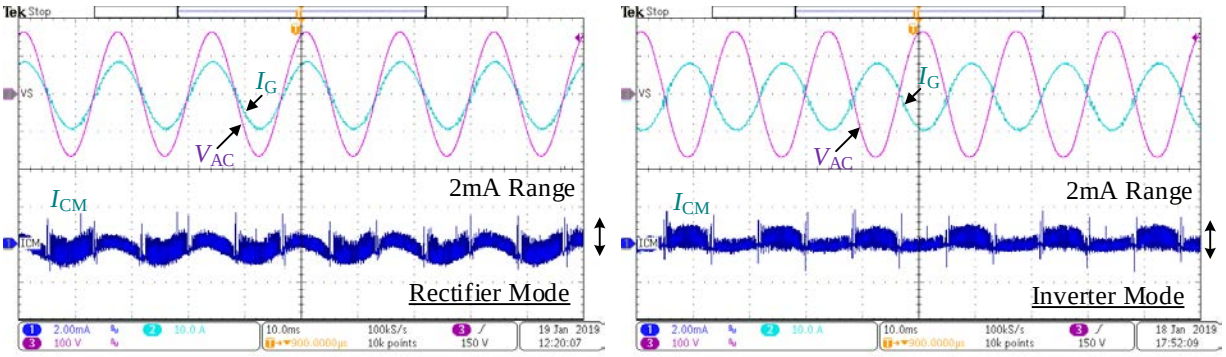


(a) (b)

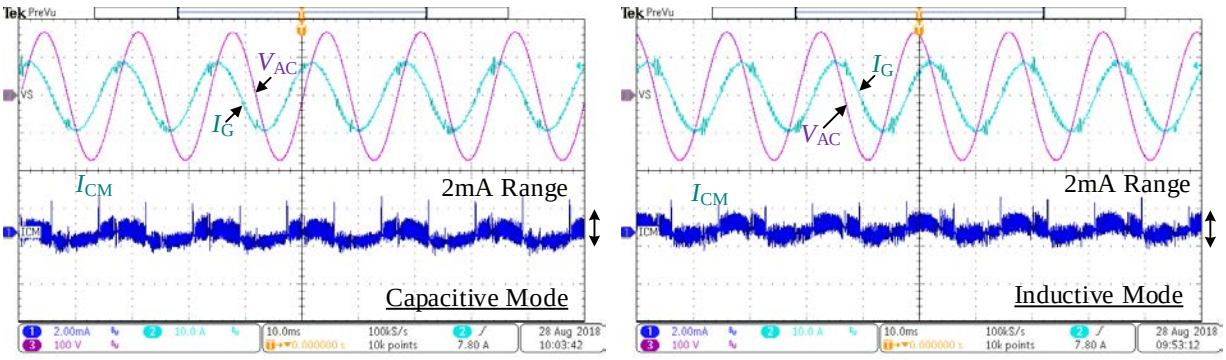


(c)

Figure 5-13. Experimental results of S_A: (a) control signal, (b) device stress in S_{A1} and (c) device stress in S_{A2}.



(a) (b)



(c) (d)

Figure 5-14. Experimental results of leakage current measurement: (a) rectifier mode, (b) inverter mode, (c) capacitive mode and (d) inductive mode.

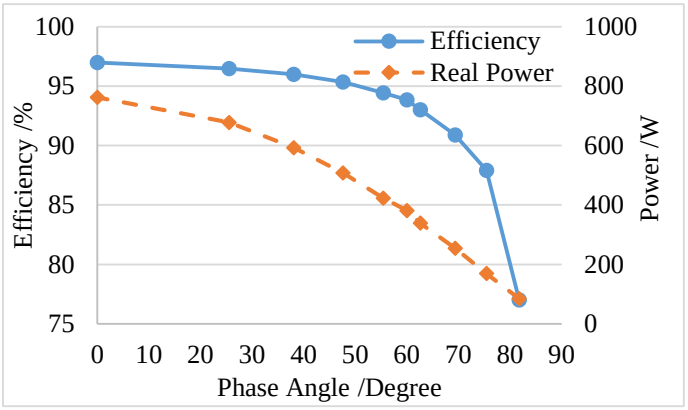


Figure 5-15. Efficiency plot of prototype under various phase conditions.

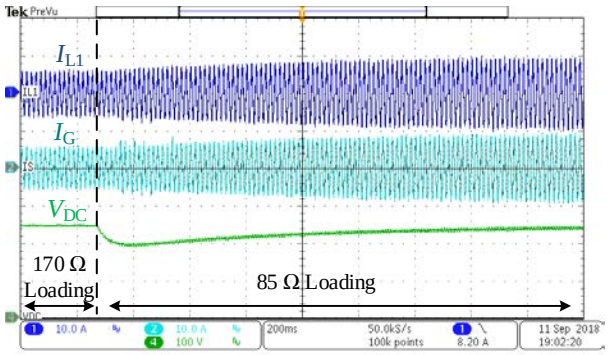


Figure 5-16. Experimental results of transient performance of load change.

Apart from the steady state, the system was also stable during transient operation. In Figure 5-16 shows out the system performance during load transient changing from 170 Ω to 85 Ω. The system was able to return to steady state within a short moment of time after the change appeared and the output voltage was always kept higher than 200 V. Therefore, a stable system was able to be guaranteed.

5.6 Conclusion

The chapter presented a new four-quadrant converter with the use of Active Virtual Ground technique. Under the proposed modulation scheme, it is able to support both real power and reactive power delivery with the use of two HF and HV switches only. The circuit freewheeling paths are located in the LF switches, so no extra device stresses are added onto the HF switches. During the system operation, a reconfigurable *LCL* filter is generated at the system input. The filter capacitor helps to build up a connection between the dc link and the grid, thus, the HF CM noise and generated leakage current of the system is always maintained at a low level. The operating principles and the steady state characteristics of the proposed topology are explained in detail. A 750 VA prototype has been built to verify the presented concept. The performance of the proposed 4Q AVG converter is demonstrated by experimental results which shows good agreement with the theoretical concept.

References

[5.1] K. K. M. Siu, C. N. M. Ho, D. Li, and R. T. H. Li, "A four-quadrant active virtual ground rectifier by using two high frequency switches," in *Proc. of IEEE IECON*, pp. 533-538, Nov. 2017.

[5.2] Y. Ma, T. Houghton, A. Cruden, and D. Infield, "Modeling the Benefits of Vehicle-to-Grid Technology to a Power System," *IEEE Trans. on Power Syst.*, vol. 27, iss. 2, pp. 1012-1020, Jan. 2012.

[5.3] H. Farzin, M. F. Firuzabad, and M. M. Aghtaie, "Reliability Studies of Modern Distribution Systems Integrated With Renewable Generation and Parking Lots," *IEEE Trans. Sustain. Energy*, vol. 8, iss. 1, pp. 431-440, Jan. 2017.

[5.4] G. Buja, M. Bertoluzzo, and C. Fontana, "Reactive Power Compensation Capabilities of V2G-Enabled Electric Vehicles," *IEEE Trans. Power Electron.*, vol. 32, no. 12, pp. 9447-9459, Dec. 2017.

[5.5] V. Monteiro, J. G. Pinto, and J. L. Afonso, "Operation Modes for the Electric Vehicle in Smart Grids and Smart Homes: Present and Proposed Modes," *IEEE Trans. Veh Commun.**, vol. 65, no. 3, pp. 1007-1020, Mar. 2016.

[5.6] S. M. R. Islam, S. Maxwell, M. K. Hossain, S. Y. Park, and S. Park, "Reactive Power Distribution Strategy using Power Factor Correction Converters for Smart Home Application," in *Proc. of IEEE ECCE*, pp. 1-6, Sept. 2016.

[5.7] F. Jauch and J. Biela, "Single-Phase Single-Stage Bidirectional Isolated ZVS AC-DC Converter with PFC," in *Proc. of EPE/PEMC*, LS5d. 1.1 - LS5d. 1.8, Sept. 2012.

[5.8] C. J. Shin and J. Y. Lee, “An Electrolytic Capacitor-less Bi-Directional EV On-Board Charger Using Harmonic Modulation Technique,” *IEEE Trans. Power Electron.*, vol. 29, iss. 10, pp. 5195-5203, Dec. 2013.

[5.9] M. C. Kisacikoglu, M. Kesler, and L. M. Tolbert, “Single-Phase On-Board Bidirectional PEV Charger for V2G Reactive Power Operation,” *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 767-775, Mar. 2015.

[5.10] M. C. Kisacikoglu, B. Ozpineci, and L. M. Tolbert, “EV/PHEV Bidirectional Charger Assessment for V2G Reactive Power Operation,” *IEEE Trans. Power Electron.*, vol. 28, no. 12, pp. 5717-5727, Dec. 2013.

[5.11] Y. S. Kim, G. C. Parkm, J. H. Ahn, and B. K. Lee, “Hybrid PFC-Inverter Topology for Bidirectional On Board Charger for Range Extended Electric Vehicle,” in *Proc. of ICEMS*, pp. 521-524, Oct. 2015.

[5.12] J. C. Salmon, “Circuit topologies for PWM boost rectifiers operated from I-phase and 3-phase ac supplies and using either single or split dc rail voltage outputs,” in *Proc. of IEEE APEC*, vol 1, pp. 473-479, Mar .1995.

[5.13] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, “Design of GaN-Based MHz Totem-Pole PFC Rectifier,” *IEEE J. Emerg. Sel. Topics in Power Electrons*, vol. 4, no. 3, pp. 799-807, Sept. 2016.

[5.14] H. Qian, J. Zhang, J. Lai, and W. Yu, “A high-efficiency grid-tie battery energy storage system,” *IEEE Trans. Power Electron.*, vol. 26, no. 3, pp. 886-896, Mar. 2011.

[5.15] T. Wu, C. Kuo, K. Sun, and H. Hsieh, “Combined Unipolar and Bipolar PWM for Current Distortion Improvement During Power Compensation,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1702-1709, April 2014.

[5.16] T. K. S. Freddy, J. Lee, H. Moon, K. Lee, and N. A. Rahim, “Modulation Technique for Single-Phase Transformerless Photovoltaic Inverters With Reactive Power Capability,” *IEEE Trans. Ind. Electron.*, vol. 64, no. 9, pp. 6989-6999, Sept. 2017.

[5.17] B. Liu, M. Su, J. Yang, D. Song, D. He, and S. Song, “Combined Reactive Power Injection Modulation and Grid Current Distortion Improvement Approach for H6 Transformer-Less Photovoltaic Inverter,” *IEEE Trans. Energy Convers.*, vol. 32, no. 4, pp. 1456-1467, Dec. 2017.

[5.18] J. Wang *et al*., “An Improved Hybrid Modulation Method for the Single-Phase H6 Inverter With Reactive Power Compensation,” *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7674-7683, Sept. 2018.

[5.19] E. Afshari, R. Rahimi, B. Farhangi, and S. Farhangi, “Analysis and modification of the single phase transformerless FB-DCB inverter modulation for injecting reactive power,” in Proc. of *IEEE CENCON*, pp. 413-418, Oct. 2015.

[5.20] T. Kerekes, R. Teodorescu, P. Rodriguez, G. Vazquez, and E. Aldabas, “A new high-efficiency single-phase transformerless PV inverter topology,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 1, pp. 184–191, Jan. 2011.

[5.21] C. Verdugo, S. Kouro, C. Rojas, and T. Meynard, “Comparison of single-phase T-type multilevel converters for grid-connected PV systems,” in *Proc. of IEEE ECCE*, pp. 3319-3325, Sept. 2015.

[5.22] G. R. Moradi, E. Afshari, R. Rahimi, B. Farhangi, and S. Farhangi, “Improvement of the modulation method for single-phase transformerless photovoltaic conergy inverter for reactive power injection capability,” in *Proc. of ICEE*, pp. 1312-1317, May 2016.

[5.23] M. Victor el at, “Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage,” *US Patent*, No. US7411802 B2, 12/08/2008.

[5.24] M. Xu and Q. L. Chen, “Ac-to-dc conversion apparatus and related control manner thereof,” *US Patent*, No. US 20130016545 A1, 12/07/2011.

[5.25] H. Schmidt *el at*, “DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current,” *US Patent*, No. US7046534 B2, 16/05/2006.

[5.26] D. Tollik and A. Pietkiewicz, “Comparative analysis of I-phase active power factor correction topologies,” in *Proc. of IEEE INTELEC*, pp.517- 523, Oct 1992.

[5.27] C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, “Active Virtual Ground-Bridgeless PFC Topology,” IEEE Trans. Power Electron., vol.32, iss.8, pp. 6206-6218, Aug. 2017.

[5.28] R. T. H. Li, C. N. M. Ho, and E. Chen, “Active Virtual Ground— Single-Phase Transformerless Grid-Connected Voltage Source Inverter Topology,” *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1335-1346, Feb. 2018.

[5.29] K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, “Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC,” *IEEE Trans. Power Electron*., vol. 34, iss. 4, pp. 3921-3936, Jul. 2018.

[5.30] K. K. M. Siu and C. N. M. Ho, “A Critical Review of Bridgeless Power Factor Correction (PFC) Boost Rectifiers with Common-mode Voltage Mitigation,” in *Proc. of IEEE IECON*, pp. 3654-3659, Nov. 2016.

[5.31] M. H. L. Chow and C. K. Tse, “Theoretical Study of Performance of Continuous-Mode Boost Converters for Power-Factor-Correction Applications,” in *Proc. of IEEE PEDS'97*, pp. 590-595, May 1997.

[5.32] P. Kong, S. Wang, and F. C. Lee, “Common Mode EMI Noise Suppression for Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291-297, Jan. 2008.

[5.33] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE 519-2014, 2014.

Chapter 6 Manitoba Rectifier – Bridgeless Buck-Boost PFC

The work described in this chapter was published in the following paper: K. K. M. Siu and C. N. M. Ho, “Manitoba Rectifier - Bridgeless Buck-Boost PFC,” *IEEE Trans. Power Electron.*, Early Access. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2017 [6.1].

6.1 Abstract

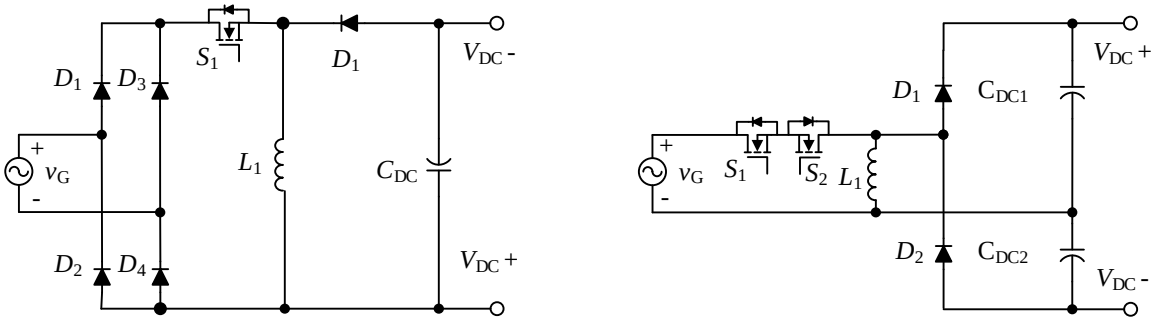
The chapter presents a new bridgeless buck-boost PFC with the use of the Active Virtual Ground technique which is named as Manitoba Rectifier. The proposed topology can convert the grid ac voltage into a wide range of voltage outputs within a single stage circuit. It is in bridgeless structure and simple in design. During the operation, an *LC* filter is generated at the system input where a continuous grid current is able to be guaranteed in a buck-boost characteristic topology. In addition, the filter capacitor helps to clamp the voltage ripple between the grid and the output bus terminal, both leakage current and common mode noise are also kept in a relatively small value. Thus, a single stage and low common-mode buck-boost converter system is built. The proposed topology is successfully implemented on an 800 W prototype and the performance is experimentally verified which shows good agreement with the theoretical findings.

6.2 Introduction

In most grid-connected power converter applications, a dual-stage system is usually adopted to support the power conversion between the ac grid and the low voltage dc. For example, a low dc output voltage is required in a battery charger system [6.2], [6.3], also a wide range of dc output voltages are required in brushless dc (BLDC) motor applications for the speed control [6.4] in lighting systems for the dimming control [6.5] and in induction heating cookers for the loading control [6.6]. The implementation of a dual-stage system is simple and straight-forward in the design. In a typical design, an ac-dc stage is adopted to correct the power factor and step up the input voltage to a higher level bus voltage. Meanwhile, it is followed by a dc-dc stage to step down the bus voltage to the required low output voltage. Several semiconductors are involved in the main current flowing path, therefore, the conduction loss in the system becomes critical. Also, a large number of components count are involved in a traditional dual-stage system. Hence, the system efficiency is restricted and the platform power density is also limited.

In order to simplify the dual-stage structure, some cascade solutions [6.7] - [6.11] and some single stage solutions [6.4], [6.12] - [6.14] were presented in the last two decades. In Figure 6-1 (a) [6.15], a traditional buck-boost rectifier is shown where the system structure is simple. However, the system efficiency is a drawback due to the high conduction loss is the diode bridge. Also, a discontinuous current results at the input which will induce harmonic issue in the grid and will also generate different mode (DM) noise from the system, thus an additional bulky input filter is required. In Figure 6-1 (b) [6.12], a simple bridgeless buck-boost system is presented where the output capacitor is split into two and is using a single inductor to handle the bidirectional current flow. The use of semiconductors is less, however, a higher buck-boost current is required when compared with other single stage solutions. This means that a higher conduction loss occurs.

Furthermore, the output capacitor voltages have to be balanced. Thus, more sensors are required and a balancing control is needed. Another single stage buck-boost rectifier solution is implemented from a tapped inductor concept, as shown in Figure 6-1 (c) [6.13], which can reduce the number of cores required. However, the discontinuous grid current will limit its usage and a special reverse blocking IGBT is required in those switches. In Figure 6-1 (d) [6.14], it combines two buck-boost switching cells into a single rectifier, where each cell handles half line cycle individually. The structure is straight forward, however, more components are required and a large input filter is still required to handle the discontinuous current in the grid. Also, more sensors are required to balance the two capacitor voltages. Similarly, In Figure 6-1 (e) [6.4], two clamping diodes and two branches of the buck-boost leg to form into a bridgeless buck-boost type rectifier. In each half line cycle, one of the clamping diodes is conducted which bypasses one of the inductors to create a current return path for the system. However, the utilization of devices becomes low and the grid-side current is always kept discontinuously. A summary is given in TABLE 1-I. Among those reviewed topology designs, either more semiconductor devices are required or larger power ratings are required in those devices. Also, a large input filter is required to handle the large scale of discontinuous current. Thus, the usages of these topologies are restricted.



(a) (b)

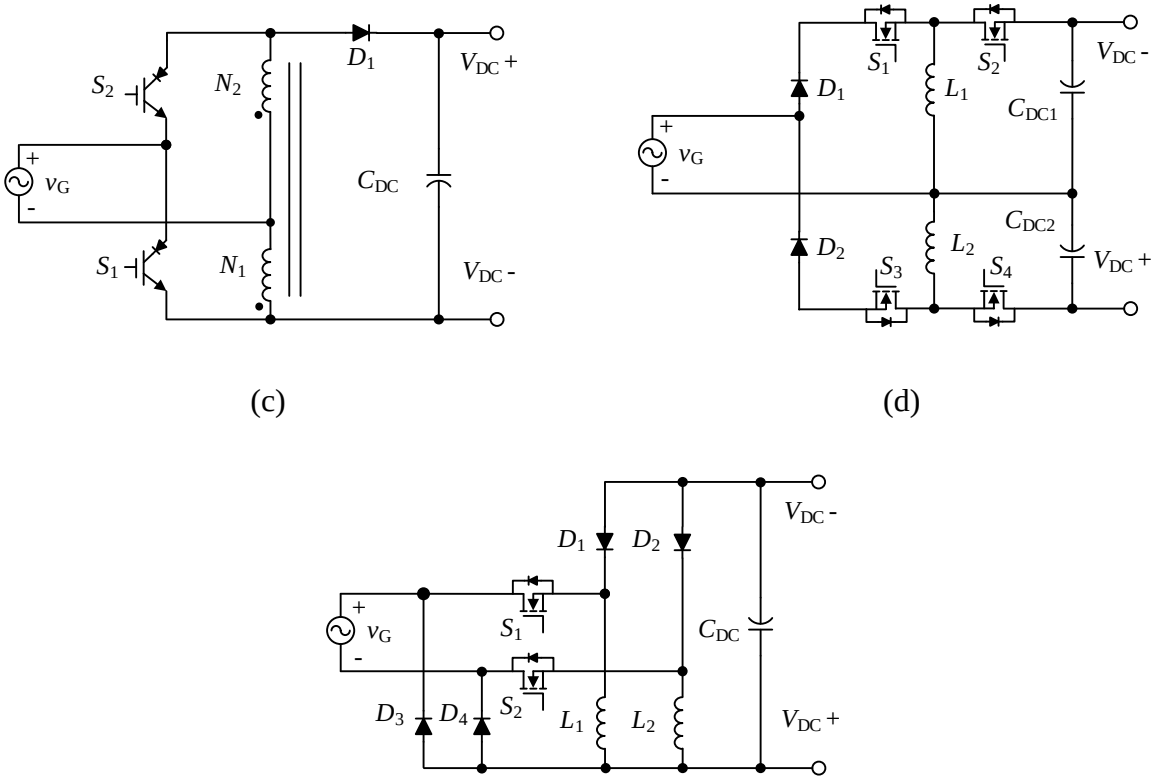


Figure 6-1. Types of buck-boost PFC topology, (a) [6.15], (b) [6.12], (c) [6.13], (d) [6.14] and (e) [6.4].

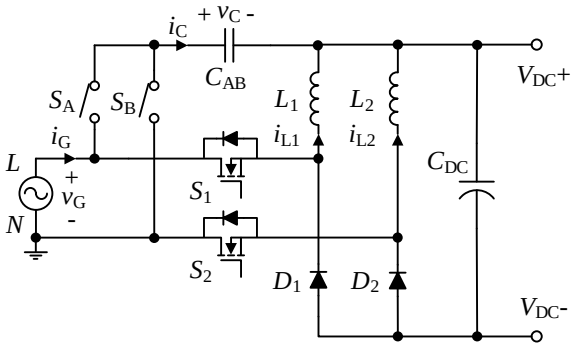
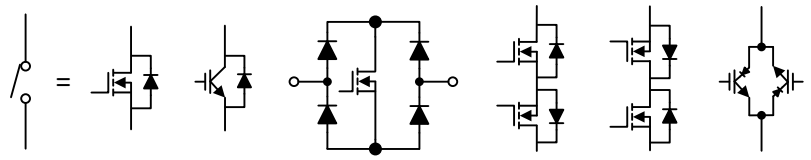


Figure 6-2. Proposed bridgeless buck-boost PFC.



(a) (b) (c) (d) (e) (f) (g)

Figure 6-3. Bidirectional current switch arrangements, (a) Ideal switch, (b) MOSFET, (c) IGBT, (d) Diode bridge, (e) Common emitter back-to-back, (f) Common drain back-to-back, and (g) anti-paralleled reverse blocking IGBTs.

TABLE 6-I SUMMARY OF NUMBERS OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topology	No. of switches		No. of Diodes	No. of Passive Components			No. of Components in the Main Current Path		Type of Input Filter
	LF	HF		Inductor	Dc Cap.	Filter Cap.	Turn-on	Turn-off	
Figure 6-1 (a)	0	1	5	1	1	0	3	3	No
Figure 6-1 (b)	0	2	2	1	2	0	2	1	No
Figure 6-1 (c)	0	2	1	2	1	0	1	1	No
Figure 6-1 (d)	0	2	4	2	2	0	2	1	No
Figure 6-1 (e)	0	2	4	2	1	0	2	2	No
Figure 6-2 (proposed)	2	2	2	2	1	1	2	2	*LC*

In this chapter, a new bridgeless buck-boost power factor corrector (PFC) topology is proposed, which is named as Manitoba Rectifier. The structure of the proposed topology is shown in Figure 6-2. It is a rectifier version of [6.16], however, they are different from each other. Compared to [6.16], two active switches are fewer in the rectifier approach, thus, a different modulation method is required. Also, due to the difference in applications, the control strategy is also different. The proposed rectifier system covers a wide input and output voltage ranges. In each half line cycle, a buck-boost converter is formed and an LC filter is generated at the system front

stage. In the main current path of the proposed system, the conduction loss of semiconductors is always less than the traditional dual-stage system. Only two semiconductors are conducting during the inductor charging period and only one semiconductor is involved for the power transfer during the inductor discharging period. Therefore, the system loss in the conduction path is minimized. The design of the reconfigurable *LC* filter is based on the recently proposed Active Virtual Ground (AVG) concept, [6.17], [6.18]. In each half line cycle operation, an LC filter is generated at the input to solve the discontinuous current problem that appeared at the grid inductor. Meanwhile, the common mode (CM) noise of the system is reduced due to the filter capacitor clamping the voltage between the grid and the bus terminals. As a result, low system noise and high system efficiency are guaranteed by the proposed topology. Both system operation principles and steady state characteristics of the proposed topology are described in detail in the chapter. Also, an 800 W prototype is successfully implemented to verify the performance of the proposed topology. All the experimental results show good agreement with the theoretical knowledge.

6.3 Principle of Operation

The bridgeless buck-boost circuit is formed by two identical switching cells together with two bidirectional current switches (S_A & S_B) and one filter capacitor (C_{AB}). The bidirectional current switches are synchronized with the input line frequency (LF) to form a reconfigurable *LC* filter at the PFC input. They can be realized by connecting two MOSFETs back-to-back in series or other configurations which are shown in Figure 6-3. The circuit structures of the proposed rectifier in the positive and negative half line cycles are different where the corresponding switching pattern is shown in Figure 6-4. Accordingly, a reconfigurable *LC* filter is always generated at the system input. It helps to filter out the discontinuous current of the buck-boost converter, so that the current

ripple in the grid side is reduced and the size of the additional input filter is reduced. In addition, due to the capacitor clamps the potential difference between the ac power source and the dc bus terminal, CM noise voltage on between is able to be minimized and the leakage current generated from the PFC circuit can also be reduced. Based on the system noise reduction, the overall noise filter can be maintained in small size and can be further optimized on the system performance.

6.3.1 States of System Operation

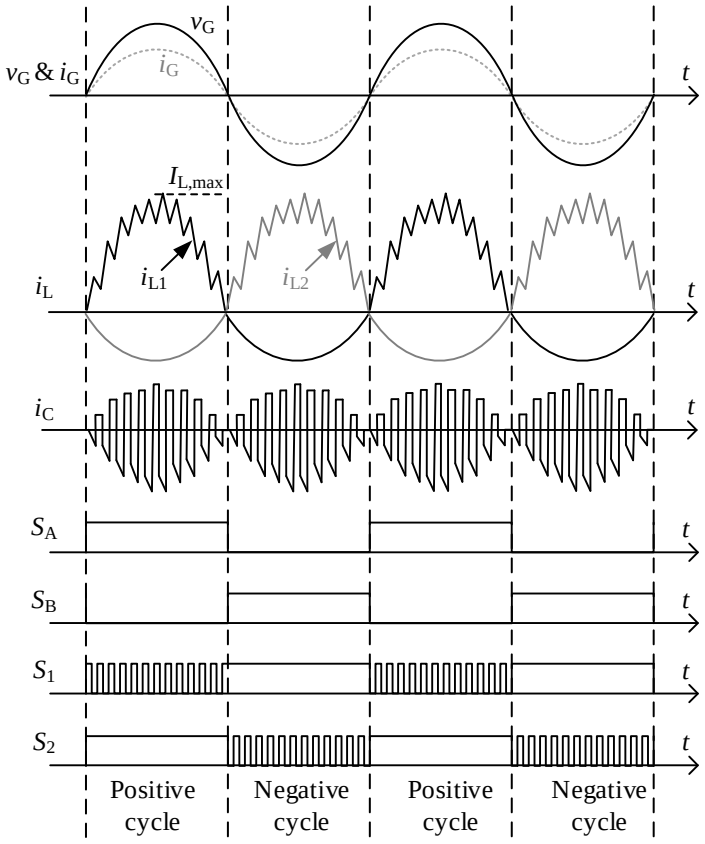


Figure 6-4. Switching pattern of the proposed topology.

The switching states of the proposed topology in the positive half line cycle are shown in Figure 6-5 (a) and the corresponding buck-boost equivalent circuits are shown in Figure 6-6 (a).

During the positive half line cycle, switch S_2 is continuously ON to provide a current return path to the circuit. Switch S_1 is with high frequency (HF) ON-OFF as a converter switch and forms a switching cell together with diode D_1. Inductor L_1 becomes a converter-side inductor to support the energy conversion in the buck-boost operation. During the turn-on state, two semiconductors are conducting in the main current path to charge up L_1. During the turn-off state, only one semiconductor is conducting in the power transformation. The corresponding current waveform is shown in Figure 6-4.

During the positive half line cycle, switch S_A is always ON and builds up the connection between C_{AB} and Line terminal (L) of the grid. Together with L_1, an LC filter is configured at the input. L_2 becomes the grid-side inductor in this half line cycle. Benefiting from the filter capacitor, the HF switching current is looping inside the converter through C_{AB} as shown in Figure 6-6 (a). The input LC filter helps to filter the discontinuous current generated from the buck-boost circuit. Thus, the grid current maintains in a continuous sinusoidal waveform and only a relatively small ripple appears on top of it. In addition, C_{AB} is coupling the voltage between Line and positive bus terminal. Only a small voltage ripple appears in C_{AB}, therefore, the CM noise that appears between the grid and the dc bus terminal will be smaller and the induced leakage current can be minimized to a small value.

The switching states of the proposed topology in the negative half line cycle are shown in Figure 6-5 (b) and the corresponding buck-boost equivalent circuits are shown in Figure 6-6 (b). During the negative half line cycle, switch S_1 is continuously ON to provide a current return path to the circuit. S_2 is with HF ON-OFF as the converter switch and forms a switching cell with diode D_2. L_2 acts as a converter-side inductor to support the energy conversion in the buck-boost operation. During the turn-on state, two semiconductors are conducting in the main current path to

charge up L_2. During the turn-off state, only one semiconductor is conducting in the power transformation path.

As switch S_B is always ON in the negative half line cycle, it helps to build up the connection between C_{AB} and Neutral terminal (N) of the grid. Together with L_1, another LC filter is configured at the input. L_1 becomes a grid-side inductor in this half line cycle. Benefiting from the filter capacitor, the HF switching current is looping inside the converter through C_{AB} as shown in Figure 6-6 (b), the HF switching current is looping inside the converter through C_{AB}. Also, the input LC filter helps to filter the discontinuous current generated from the buck-boost circuit. Thus, the grid current can maintain in a continuous sinusoidal waveform and only with a relatively small ripple appears on top of it. In addition, C_{AB} is coupling the voltage between Neutral and positive bus terminal. Thus, only small voltage ripple appears in C_{AB}, therefore, low CM noise and small leakage current are resultant from the system.

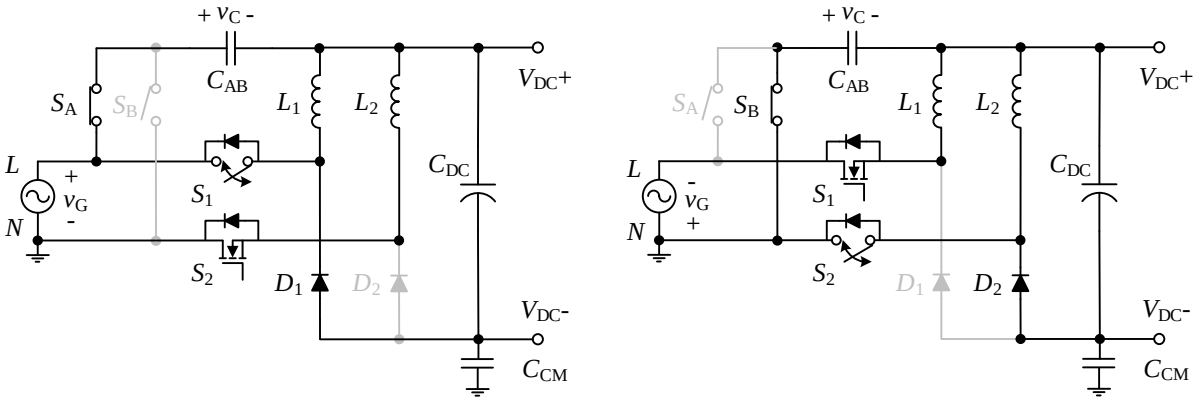


Figure 6-5. Switching actions in (a) positive and (b) negative half line cycles.

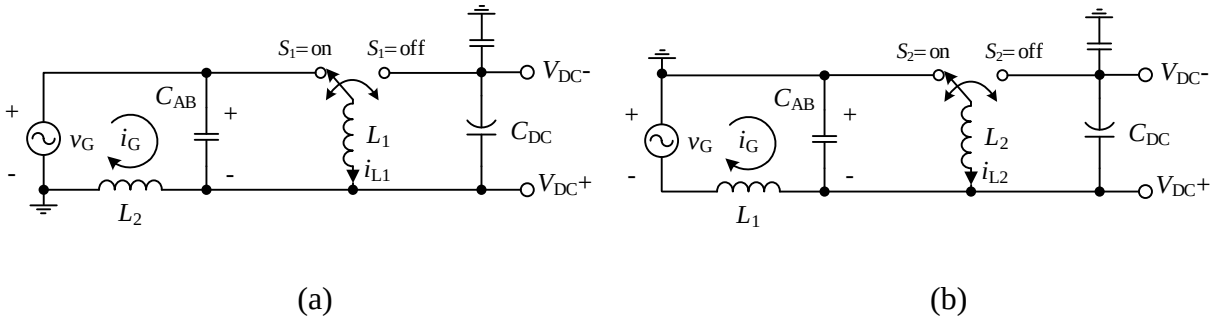


Figure 6-6. Equivalent circuits in (a) positive and (b) negative half line cycles.

6.3.2 Control Scheme

The control diagram of the proposed topology is shown in Figure 6-7. In the control architecture, a PI controller is implemented in the outer loop to regulate the rectifier output voltage, v_{DC}, and to limit the voltage fluctuation during any possible transient situations. The output of the outer loop is a grid current reference, $i_{G,REF}$. The inner loop is a grid current control loop which is implemented by another PI controller to maximize the system power factor by tracking the grid current, i_G, in sinusoidal. The output of the inner loop is a duty reference, u_{REF}, which is used to generate the PWM switching signals of the rectifier. An active damping circuit [6.19] is implemented into the controller with the use of HF capacitor ripple, Δv_C. It can help to stabilize the circuit operation and to damp any possible resonant harmonic current in the grid. By combining with the polarity signal, the switching signals of S_1 and S_2 are resultant.

As shown in Figure 6-4, switching signals of S_A and S_B are controlled by the polar of the grid voltage, v_G. Under the polarity detector, S_A stays ON at positive half line cycle and S_B is ON at negative half line cycle. Under unipolar switching method, only either one of the main switches, S_1 or S_2, is operated at HF ON-OFF in each half line cycle. S_1 is under HF switching during the positive half line cycle and keeps ON during the negative half line cycle. On contract, S_2 is kept as

HF switching during negative half line cycle and is kept ON at the positive half line cycle.

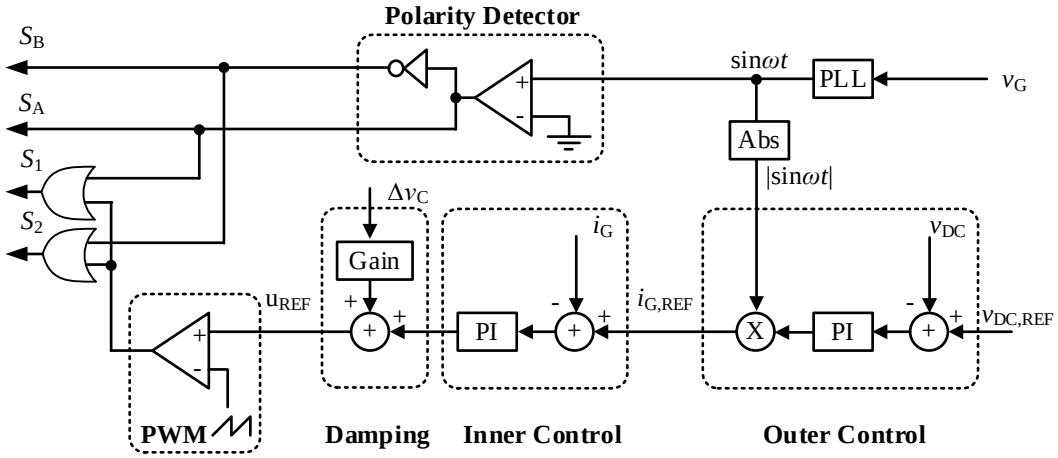


Figure 6-7. Control diagram of the proposed topology.

6.4 Steady State Characteristics

According to the operation diagram in Figure 6-6, system steady state characteristics are able to be found. Due to the symmetrical structure of the proposed topology, only the positive half line cycle is taken for the following analysis. In the design, the inductances of L_1 and L_2 are identical and with the same values. Thus, an equivalent inductance, L_X, is used represented all the inductances in the proposed circuit, i.e. $L_X = L_1 = L_2$.

A. Duty Cycle

In the positive half line cycle, L_1 acts a converter-side inductor and L_2 acts a grid-side inductor. With the use of the reconfigurable *LC* filter, all the time the filter capacitor voltage is always a positive sign. By neglecting the small voltage drop on the grid-side inductor, the capacitor voltage, v_C, is closed to the rectified grid voltage, $|v_G|$, as,

$$v_C(t) \approx |v_G(t)| = V_G|\sin \omega t|, \tag{6.1}$$

where V_{G} is peak amplitude of grid voltage and ω is angular line frequency.

Same as a general buck-boost converter, duty cycle of the proposed rectifier, *D*, is expressed as:

$$D(t) = \frac{V_{\mathrm{DC}}}{V_{\mathrm{DC}}+V_{\mathrm{G}}|\sin \omega t|}, \tag{6.2}$$

where V_{DC} is dc value of the system output voltage.

All the time, the duty cycle is time varying and is following the change of grid voltage as shown in (6.2).

B. Converter-side Inductor Fundamental Current and HF Current Ripple

In a buck-boost circuit, the converter-side inductor current is all the time larger than or equal to the grid-side inductor current. As a large amount of energy is required to support the buck-boost operation. The fundamental current value of the converter-side inductor, i_{L}, is depended on the input current value and the duty cycle information, where i_{L} is expressed as,

$$i_{\mathrm{L}}(t) = \frac{2 \cdot P_{\mathrm{O}} \cdot \sin \omega t \cdot (V_{\mathrm{DC}}+V_{\mathrm{G}}|\sin \omega t|)}{V_{\mathrm{G}} \cdot V_{\mathrm{DC}}}, \tag{6.3}$$

where P_{O} is output power.

The ripple current on the converter-side inductor, Δi_{L}, is related to the energy conversion process. Under fixed frequency switching and continuous-conduction mode (CCM) operation, Δi_{L} is able to be developed from the inductor on-state characteristic, as,

$$\Delta i_{\mathrm{L}}(t) = \frac{V_{\mathrm{DC}} \cdot V_{\mathrm{G}}|\sin \omega t|}{(V_{\mathrm{DC}}+V_{\mathrm{G}}|\sin \omega t|) \cdot L_{\mathrm{X}} \cdot f_{\mathrm{SW}}}, \tag{6.4}$$

where f_{SW} is switching frequency.

A detailed derivation of (6.3) and (6.4) are given in the Appendix.

C. Filter Capacitor HF Voltage Ripple

As shown in Figure 6-8, a discontinuous current appears on the filter capacitor which is generated from the buck-boost circuit operation. An *LC* filter is always configured at the grid side, thus, the converter-side HF current is expected to be filtered out and circulates in the converter-side through the C_{AB}. The HF current results a voltage ripple in the filter capacitor, Δv_{C}, which is calculated as,

$$\Delta v_{\mathrm{C}}(t) = \frac{2 \cdot P_{\mathrm{O}} \cdot |\sin \omega t|^2}{(V_{\mathrm{DC}} + V_{\mathrm{G}} |\sin \omega t|) \cdot C_{\mathrm{AB}} \cdot f_{\mathrm{SW}}}. \tag{6.5}$$

A detailed derivation of (6.5) is given in the Appendix.

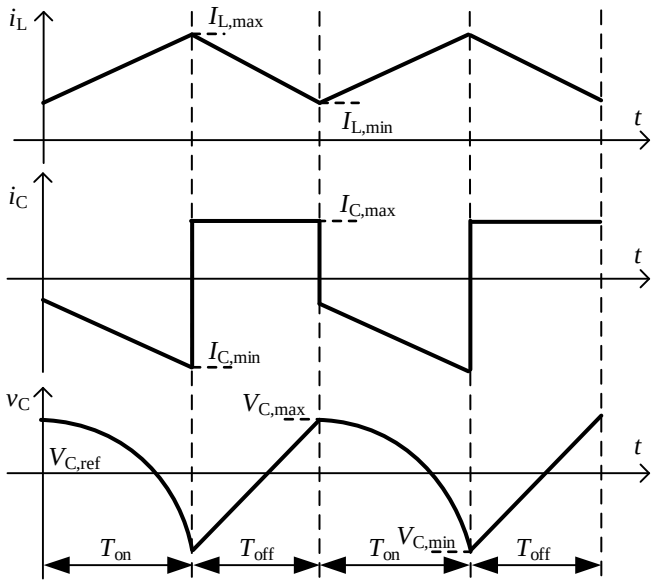


Figure 6-8. Switching waveforms of filter capacitor.

D. Grid-side Inductor HF Current Ripple

Due to the *LC* filter characteristic, the grid-side inductor current ripple is much smaller than the converter-side current ripple. From the circuit characteristic, the grid current ripple is mainly contributed from the capacitor voltage ripple. Under CCM operation, a continuous current is

present in the grid. The voltage ripple appeared in the filter capacitor is the same as the HF voltage ripple that appeared in the grid-side inductor. To simplify the calculation, a small approximation is taken. The inductor voltage ripple is approximating to the triangle waveform, therefore, the grid current ripple, Δi_{G}, is formed as,

$$\Delta i_{\mathrm{G}}(t) \approx \frac{P_{\mathrm{O}} \cdot |\sin \omega t|^2}{4 \cdot (V_{\mathrm{DC}} + V_{\mathrm{G}} |\sin \omega t|) \cdot L_{\mathrm{X}} \cdot C_{\mathrm{AB}} \cdot {f_{\mathrm{SW}}}^2}. \tag{6.6}$$

A detailed derivation of (6.6) is given in the Appendix.

E. Output Capacitor Voltage Ripple

The output capacitor is used to hold the dc link output voltage and to filter the HF current in the output. In the proposed topology, power decoupling function, [6.20], [6.21], is not included. Thus, in a single stage rectifier design, a double line frequency voltage ripple is always been found at the rectifier output. The magnitude of the output voltage ripple is depended on the size of the capacitor and the rated power of the system. The double line frequency voltage ripple of the output capacitor, ΔV_{DC}, is calculated as,

$$\Delta V_{\mathrm{DC}} = \frac{P_{\mathrm{O}}}{\omega \cdot C_{\mathrm{DC}} \cdot V_{\mathrm{DC}}}. \tag{6.7}$$

A detailed derivation of (6.7) is given in the Appendix.

From (6.7), it shows that when power increases, the output ripple is increased. In order to maintain the capacitor ripple voltage into a small value, generally, a larger scale dc link capacitor is needed for an application with higher power rating.

F. HF Common Mode Noise Voltage between Ac Grid and Dc Bus

As shown in Figure 6-5 and Figure 6-6, a parasitic capacitor, C_{CM}, is used to represent the

coupling between the grid and the dc bus terminal. In the positive cycle, the coupling voltage is equal to the sum of the output voltage, the filter capacitor voltage and the negative input voltage. In the negative cycle, the coupling voltage is equal to the sum of output voltage and filter capacitor voltage. In the HF analysis, the input voltage source and the dc output capacitor are always equivalent to short circuit. Thus, C_{CM} is virtually parallel to the filter capacitor in the Manitoba Rectifier circuit and has the same HF voltage ripple as the filter capacitor ripple. By modifying (6.5), the HF CM voltage ripple, Δv_{CM}, is obtained,

$$\Delta v_{\mathrm{CM}}(t) = \frac{2 \cdot P_{\mathrm{O}} \cdot |\sin \omega t|^2}{(V_{\mathrm{DC}} + V_{\mathrm{G}} |\sin \omega t|) \cdot (C_{\mathrm{AB}} + C_{\mathrm{CM}}) \cdot f_{\mathrm{SW}}}. \tag{6.8}$$

G. HF Leakage Current between Ac Grid and Dc Bus

In the system design, the HF current is circulating inside the rectifier through the filter capacitor. Thus, the magnitude of the filter capacitor ripple current is closed to or equal to the maximum inductor current during each switching period. A HF switching current is inducted in the coupling path and causes leakage current generated the system. Accordingly, the HF leakage current in the coupling path, $\Delta i_{\mathrm{CM}}(t)$, can be found as,

$$\Delta i_{\mathrm{CM}}(t) = \frac{C_{\mathrm{CM}}}{C_{\mathrm{AB}} + C_{\mathrm{CM}}} \cdot \left(i_{\mathrm{L}}(t) + \frac{\Delta i_{\mathrm{L}}(t)}{2}\right). \tag{6.9}$$

By combining (6.3) and (6.4) into (6.9), the expression of the HF leakage current is rearranged to,

$$\Delta i_{\mathrm{CM}}(t) = \frac{C_{\mathrm{CM}}}{(C_{\mathrm{AB}} + C_{\mathrm{CM}})} \cdot \left(\frac{2 \cdot \mathrm{P_O} \cdot \sin \omega t \cdot (V_{\mathrm{DC}} + V_{\mathrm{G}} |\sin \omega t|)}{V_{\mathrm{G}} \cdot V_{\mathrm{DC}}} + \frac{V_{\mathrm{DC}} \cdot V_{\mathrm{G}} |\sin \omega t|}{2 \cdot (V_{\mathrm{DC}} + V_{\mathrm{G}} |\sin \omega t|) \cdot L_{\mathrm{X}} \cdot f_{\mathrm{SW}}}\right). \tag{6.10}$$

According to (6.10), the magnitude of the leakage current is directly proportional to maximum converter-side inductor current and the capacitance ratio between C_{CM} and C_{AB}. It means the leakage current can be adjusted by turning the value of C_{AB}. The positive sign magnitude of i_{CM} is

following to inverse duty cycle, δ, which is calculated as,

$$\delta = \frac{V_G|\sin \omega t|}{V_{DC}+V_G|\sin \omega t|}. \quad (6.11)$$

6.5 Design and Implementation

6.5.1 Options in Implementation

The proposed circuit can have two types of circuit structure which are positive cell and negative cell structures. The positive cell structure is shown in Figure 6-9 (a) which is the same as Figure 6-2. The negative bus voltage is connected to the anodes of each diode and the positive bus voltage is connected to those inductors. The negative cell structure is shown in Figure 6-9 (b). Both switch and diode positions are in opposite directions when comparing to the positive cell structure. The polarity of the output voltage is also revised. The negative bus terminal is connected to both inductors and the positive bus terminal is connected to the cathodes of each diode. Switching signals of all the switches are exchanged, but the same switching pattern is kept as Figure 6-4. There is no change in the system performance.

There are two types of reconfigurable filter circuits which are shown in Figure 6-10. Based on the design requirements and needs of the application, different filter structures are selected and different connection methods are considered. In Figure 6-10 (a), a single capacitor circuit is demonstrated which is the one that appears in Figure 6-2. In Figure 6-10 (b), a spitted capacitor circuit is demonstrated which is used to avoid any short circuit possibility at the input. Each of them handles half line cycle. Even a failed signal appears in both switch S_A and S_B at the same time, there would not have any short circuit happened. The corresponding operation diagrams and

the equivalent circuits of the spitted capacitor method are the same as Figure 6-4 and Figure 6-6 respectively. Meanwhile, at the voltage zero crossing point, a relatively small dead time can be set. Thus, the power quality of the system can be further improved.

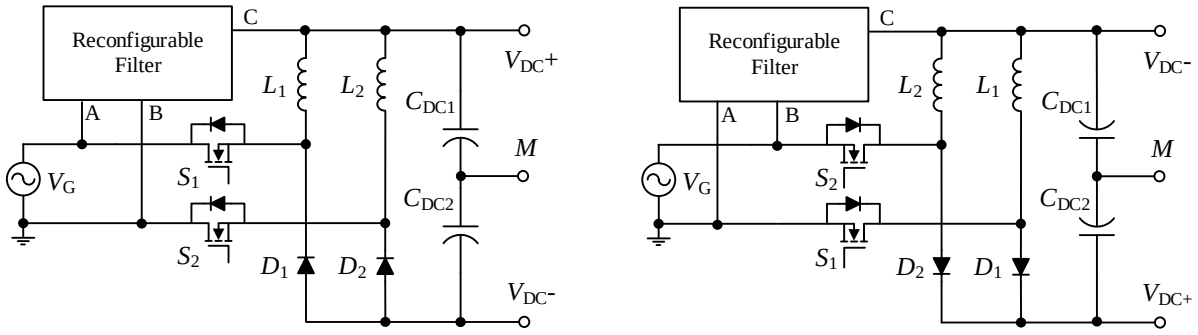


Figure 6-9. Implementations of the proposed topology with the use of (a) positive cell and (b) negative cell structures.

Figure 6-10. Implementations of the reconfigurable filter circuit, (a) single capacitor and (b) spitted capacitor methods.

Also, variants of connection methods are offered. The terminal C of the reconfigurable filtering circuit is possible to connect either the positive bus terminal, negative bus terminal or the middle point of the dc link capacitor, M. The advantage of middle point connection is when a large surge current appears in the input, the output capacitor can help to handle the large current flow.

The drawback is that there is a dc voltage offset in the filter capacitor, therefore, a higher voltage margin is required in the filter capacitor.

6.5.2 Selection of Filter Components

TABLE 6-II VALUE OF THE SYSTEM CONDITIONS USED IN THE DESIGN

Parameter	Value	Parameter	Value
V_{AC}	120~220 Vac	V_{DC}	50~200 Vdc
Input Frequency	60 Hz	P_O	800 W
f_{SW}	50 kHz	$I_{L.MAX}$	25 A

For the Manitoba Rectifier prototype, the maximum power is set to 800W and with a wide input and output voltage ranges. The target system specification is shown in TABLE 6-II. Universal input voltage is considered which covers from 120 to 220 Vac. The output voltage range is depended on the needs of the application. The maximum output voltage is related to the device breakdown voltage and the minimum output voltage is related to the maximum available inductor current. In the design, the output voltage range is set to 50 to 200 Vdc. Meanwhile, the specified inductance current ripple is set to 15 %. Based on (6.4) and all the testing conditions, the minimum required inductance is calculated as 0.7 mH. Finally, 0.78 mH is designed for both of the inductor L_1 and L_2. They are implemented by two 77.8 mm high flux cores, 58907, and are routed with 76 turns on top. The selection of C_{AB} is based on the following two criteria,

1. Maximum resonance frequency, to avoid the interaction between the *LC* filter resonance frequency and the switching frequency, there should be a big ratio different on between, such as 10 times different. The relationship is expressed as,

$$C_{AB} \geq \frac{1}{L_X}\left(\frac{10}{2\pi f_{sw}}\right)^2. \tag{6.12}$$

Based on the specification in TABLE 6-II, the minimum capacitance value is calculated 1.3μF.

2. Maximum leakage current, $\Delta I_{\mathrm{CM,MAX}}$, BLDC is taken as an example, the leakage current amplitude is limited to 3.5 A and 3.5 mA, as shown in [6.22] and [6.23] respectively. Refer to [6.24] and [6.25], 0.47 nF is selected as a reference of the system C_{CM} value to fulfill the requirement of 3.5 mA leakage current. From (8), the equation related to the maximum leakage current can be rearranged as,

$$C_{\mathrm{AB}} \geq C_{\mathrm{CM}}.\left(\frac{I_{\mathrm{L,MAX}}}{\delta.\Delta I_{\mathrm{CM,MAX}}} - 1\right). \tag{6.13}$$

Based on the specification in TABLE 6-II, the minimum capacitance value is calculated as 1.97 μF. Finally, a 3.3 μF capacitor is selected for C_{AB} of the designed prototype.

The value selection of C_{DC} is based on the following two criteria,

1. Hold-up time, t_{hold}, it is used to ensure the design circuit can maintain function properly when the input power is suddenly stopped for a short period of time. The corresponding equation is expressed as follows,

$$C_{\mathrm{DC}} \geq \frac{2P_{\mathrm{O}}.t_{\mathrm{hold}}}{{V_{\mathrm{DC}}}^2 - {V_{\mathrm{DC,MIN}}}^2}. \tag{6.14}$$

If a 5 ms is required for the hold-up time and the minimum output voltage, $V_{\mathrm{DC,MIN}}$, is set to 60 % of the maximum rated output, the minimum output capacitance is calculated as 0.87 mF.

2. Output voltage ripple, ΔV_{DC}, the maximum output ripple is set to 20 V of the target design. Based on (6.4) and all the targeted testing conditions, the minimum output capacitance is calculated as 0.88 mF.

Finally, a 0.94 mF capacitor is selected for C_{DC} in the prototype design.

6.5.3 Selection of Semiconductors

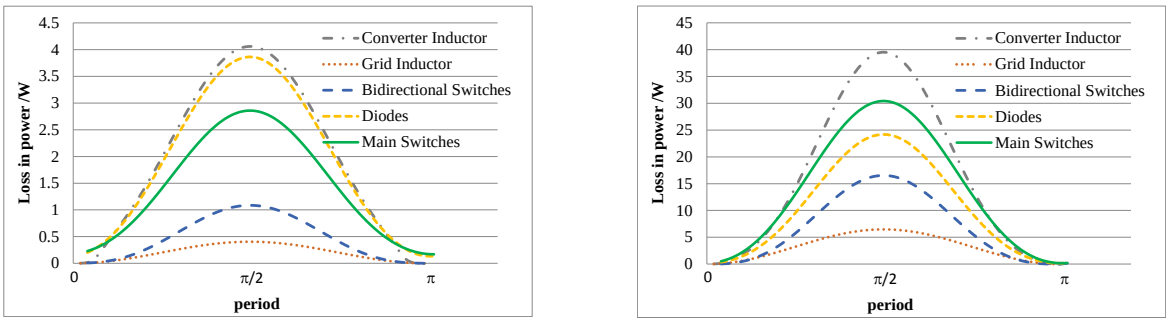
TABLE 6-III LIST OF SEMICONDUCTORS

Device	Type	Part Number	Voltage Stress
Switches S_A and S_B	Si MOSFET	IPW60R070C6	V_G
Switches S_1 and S_2	Si MOSFET	IPW60R080P7	$V_G + V_{DC}$
Diodes D_1 and D_2	SiC Diode	GP2D020A060B	$V_G + V_{DC}$

Semiconductors are required in the system to form the switching cells and to generate the reconfigurable *LC* input filter. S_1 and S_2 are the main switches of the circuit which handle the charging period of the buck-boost operation. They act as the converter switches and operate under HF switching. D_1 and D_2 are the converter diodes which handle the discharging period of the buck-boost operation. The voltage stress appears in the switching cell is equal to the sum of the input voltage and the output voltage. According to the voltage specifications shown in TABLE 6-II, 600V devices are required. Based on HF and high voltage (HV) requirement, Si MOSFETs are selected for the converter switches and SiC diodes are selected for the converter diodes. S_A and S_B are the LF bidirectional current switches which are used to configure different structural input *LC* filters during each half line cycle. Only HF ripple current passes through the LF switches and the voltage stress on top is from the grid only. Therefore, low on-state resistance MOSFETs are selected and are connected in a back-to-back configuration to support the required bidirectional blocking function. The selected semiconductors are summarized in TABLE 6-III.

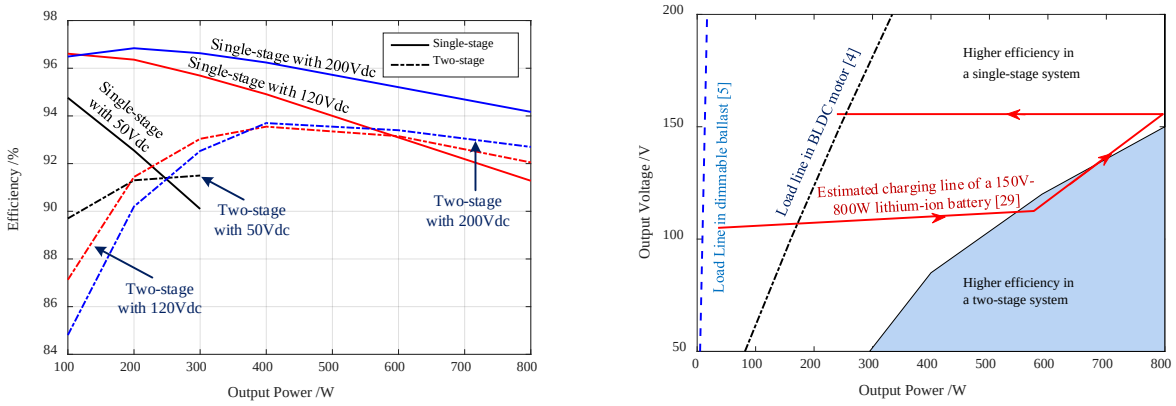
Refer to [6.26], [6.27], a loss breakdown of light load (200 W) and full load (800 W) under 120Vac-120Vdc test conditions are given in Figure 6-11(a) and (b) respectively. It can be seen that the highest converter loss is coming from the converter-side inductor where the HF current ripple induces the core loss and the high level buck-boost inductor current induces the conduction loss.

The lowest converter loss appears on the grid-side inductor where the core loss of itself is closed to zero and only LF current conduction loss remains. In the switching cells, the major losses appear on top are switching loss and conduction loss. For the LF switches, all the time only have the conduction loss on top. Also, they are only carrying the HF ripple, thus, the loss is far lower than the main switches. In the light load condition, the current value is low, therefore, the conduction loss generated from those devices are less and is closed to or less than the HF switching loss portion. In the full load condition, the conduction loss generated from those devices become more obvious as the current level is increased. The system conduction loss portion dominates the overall system loss. Based on the system loss estimation, a corresponding system efficiency figure is generated and is shown in Figure 6-12 (a). Significantly, in the middle to full load range, when the output voltage is lower, the system efficiency is lower. It is because the converter-side inductor current is higher when the output voltage is dropped. In the light load condition, the change of system efficiency depends on the balance between the switching loss and conduction loss.



(a) (b)

Figure 6-11. Loss breakdowns at 120 Vac– 120 Vdc with (a) 200 W power delivery and (b) 800 W power delivery.



(a) (b)

Figure 6-12. System estimations with (a) efficiency predication different power rating and (b) performance trade-off between the proposed rectifier and a two-stage system.

For efficiency evaluation, a two-stage solution is used as a reference for comparison, which is combined with a traditional boost-type converter and a buck-type converter. The corresponding system efficiency is estimated and is shown in Figure 6-12 (a). The applied system parameters and the types of considering devices remain the same as the proposed topology. In 200 Vdc test case, the proposed method is always more efficient than the two-stage system. In 50 Vdc and 120 Vdc test cases, in most of the power ranges, the proposed topology obtains better performance than the two-stage system. Only when the power is larger than 80 % of the loading, the two-stage system has a benefit on it. In the low output voltage but with high power rating situation, the inductor current produced in the buck-boost type rectifier is relatively higher than the current in the two-stage system. Thus, the benefit of a single-stage buck-boost rectifier will be reduced accordingly. The performance trade-off between the proposed rectifier and the two-stage system is shown in Figure 6-12 (b). However, in those systems that require a variable dc voltage, the output voltages are usually proportional to the output power, such as in BLDC motor system [6.5] and lighting dimming system [6.5]. Also in the battery charging system, [6.2] and [6.28], similar behavior can

be found in a constant current charging period of a lithium-ion battery pack [6.29]. Thus, the design of a single-stage buck-boost type rectifier can have the biggest advantage on it. Meanwhile, there is a method to enhance the benefits of the proposed rectifier at a higher power rating, which is to choose a lower on-state resistance device. However, the trade-off is that the light load efficiency will be reduced.

6.6 Experimental Verification

An 800W Manitoba Rectifier prototype is implemented which is based on the design guideline that provided in Section 6.5. In Figure 6-13 (a), it demonstrates the operating principle of the LF switches. By switching S_A and S_B alternatively, an *LC* filter was always formed in the front stage and the filter capacitor voltage was maintained close to the rectified grid voltage. The filter capacitor helped to maintain the ripple voltage between the grid and the bus terminal into a small value. Thus, low CM voltage and low leakage current were expected. In Figure 6-13 (b), a 470 pF capacitor is added into the system to simulate the effect of the parasitic capacitor. The voltage between the Neutral of the grid and the negative bus voltage was measured and used to represent the CM noise voltage of the system. The current that flowed through the capacitor was used to represent the leakage current. The result proofed that the HF noise voltage was in a relatively small value and closed to the ripple on the filter capacitor. Also, the resulted leakage current was able to be minimized into mA range which was accepted by the industrial standard.

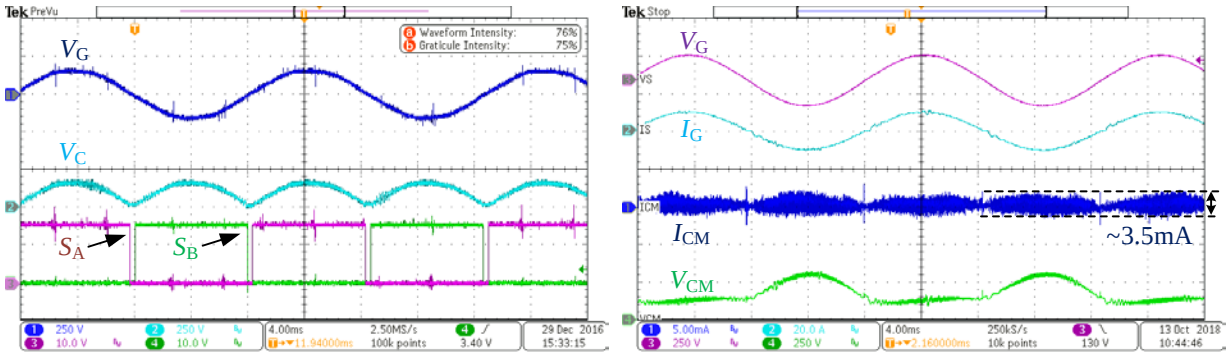
In Figure 6-14, it demonstrates the steady state performance of the system at various system conditions which including both step-up and step-down case situations. In Figure 6-14 (a)-(c), the platform is tested under 120 Vac input with 50 Vdc, 120 Vdc and 200 Vdc output respectively. In Figure 6-14 (d), the platform is tested under 220 Vac input and 120 Vdc output. All of them

demonstrated stable performance at the steady state conditions. During each half line cycle, the inductor role was interchanged. At the positive half line cycle, L_1 acted as a converter-side inductor to handle the power conversion. In the negative half line cycle acted as a grid-side inductor and had the same current magnitude as the grid current. The magnitude of the inductor current and the current ripple on top were matched with the theoretical concepts which calculated in (6.6) and (6.7). Under different output voltage conditions, the ratio between the converter-side inductor current and the grid-side current was varied. Smaller in the output voltage, higher in the inductor current magnitude was obtained. Due to an *LC* input filter was configured at the input, the discontinuous buck-boost input current was filtered out and a LF continuous current was given in the grid side. Under the same power rating, lower in the output voltage, higher output capacitor voltage ripple was obtained.

The power factor of the system was maintained higher than 0.99. In the 120 Vac input measurement, the best efficiency point was 96.8 % which was located at the 200 Vdc output and with 200 W loading. In detail, at full loading condition of 200 V output, voltage THD was 0.351 % and the current THD was 3.16 % where the system efficiency was 94.4 %. At full loading condition of 120 V output, the voltage THD was 0.34 % and the current THD was 2.91 % where the system efficiency was 91.6 %. Similar performance was obtained in the 120Vac-50Vdc and 220Vac-120Vdc testing conditions. All the time, the system THD in both voltage and current were also kept lower than 5 % [6.30]. Meanwhile, the detailed system efficiency is provided in Figure 6-15 and is summarized in TABLE 6-IV.

The performance of the proposed rectifier was competitive to other single stage buck-boost rectifiers. Referred to [6.8], under a similar Rdson device, STY60NM50, the simulation efficiency of the bridgeless Sepic rectifier was around 92.4 % at 120Vac-48Vdc-200 W. In a similar test case,

120Vac-50Vdc-200W, the achieved efficiency of the proposed rectifier 93.1 %. The result was closed with each other. Referred to Figure 6-1 (c) [6.13] and (d) [6.14], two different types of bridgeless buck-boost rectifier were proposed. One was operated at hard-switching and the other one was worked at soft-switching control. The given measured efficiencies were 87.7 % at 110 Vac-48Vdc-100W and 97.6 % at 240Vac-100Vdc-150W, respectively. Under similar testing conditions, 120Vac-50Vdc-100W and 220Vac-120Vdc-220W, the measured system efficiency was 94.76 % and 96.47 %, respectively. The performance of the proposed converter was better than [6.13] but lower than [6.14]. The difference mainly came from the different between soft-switching and hard-switching control. Better performance in soft-switching control, however, it more relies on the system parameters and a more precise control is required. Meanwhile, in those reference topologies, the input filter is not included in their design. It implies that the loss in the filter circuit is not included in their corresponding measurement. In proposed topology, a reconfigurable *LC* filter is always located at the input and helps to filter out the HF current ripple. In summary, the overall performance of the proposed topology was always comparable to others.



(a) (b)

Figure 6-13. Experimental waveforms at 120Vac–120Vdc–800W: (a) filter capacitor waveform and (b) parasitic capacitor waveform.

TABLE 6-IV SUMMARY OF THE TEST RESULTS

V_G / V	V_{DC} /V	Figure 6-14	P_O /W	η /%	V_G THD /%	I_G THD /%	PF
120	50	(a)	196	93.1	0.30	4.93	0.993
120	120	(b)	780	91.6	0.34	2.91	0.998
120	200	(c)	773	94.0	0.35	3.16	0.997
220	120	(d)	779	94.4	0.33	3.63	0.997

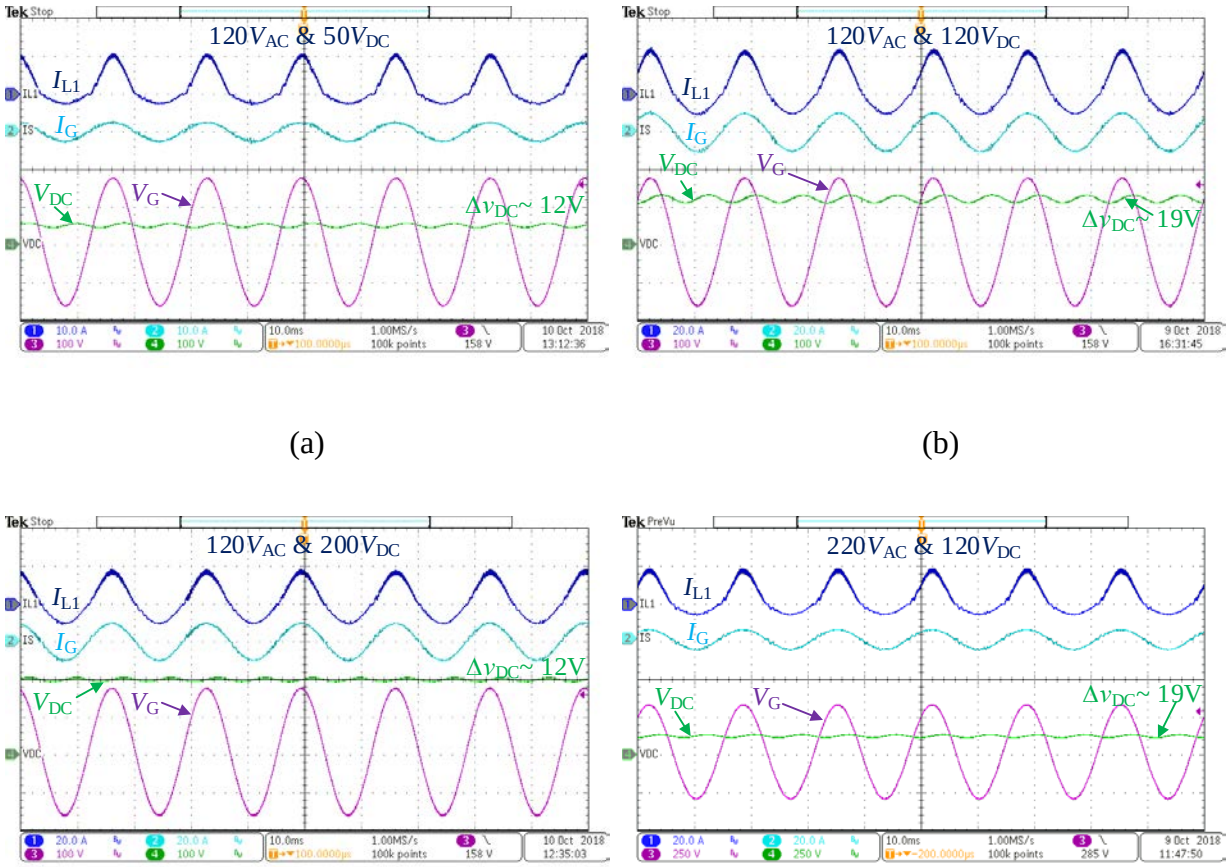
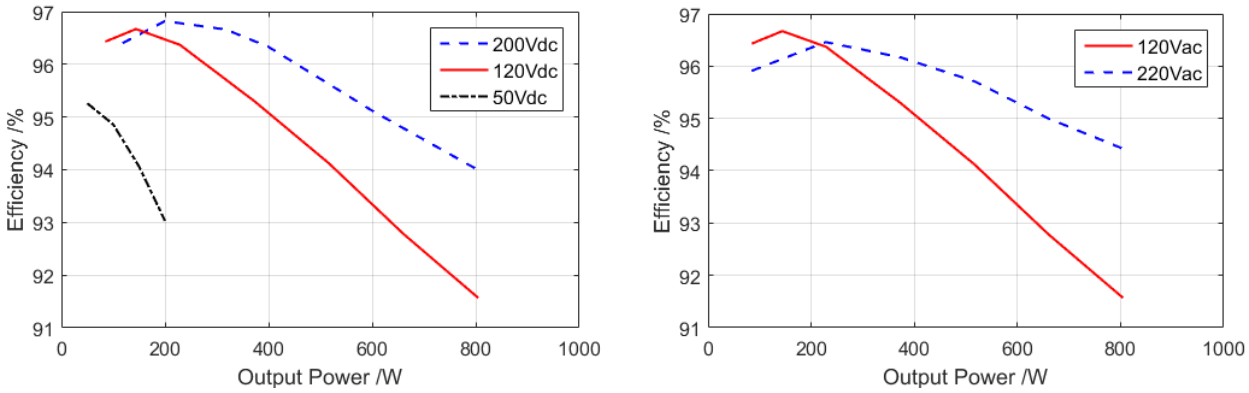
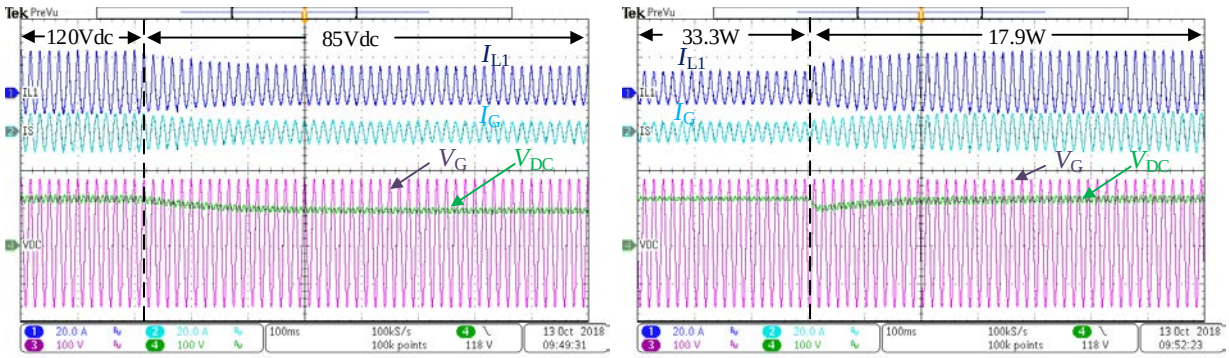


Figure 6-14. Experimental waveforms: (a) 120Vac–50Vdc–200W, (b) 120Vac–120Vdc–800W, (c) 120Vac–200Vdc–800W and (d) 220Vac–120Vdc–800W.



(a) (b)

Figure 6-15. Measured system efficiencies (a) under a fixed input voltage (120 Vac) and (b) under a fixed output voltage (120 Vdc).



(a) (b)

Figure 6-16. Transient waveforms during (a) an output voltage change and (b) a load change.

Apart from the steady state, the system also achieves stable performance under transient operations. Two transient tests were done. One is output voltage change as shown in (a) (b)

Figure 6-16 (a). In the test, the input voltage was kept at 120 Vac meanwhile the output voltage was dropped from 120 Vdc to 85 Vdc. The consuming power was half of the previous one. Another transient test case is load change, the performance is shown in (a) (b)

Figure 6-16 (b). At 120Vac-120Vdc test case, the output loading was changed from 33.3 Ω to 17.9 Ω. As the loading resistance dropped, the output power was rapidly increased at a short period of time. In both cases, the system was also maintained stable, the grid current kept sinusoidal and was able to convert into the steady state in a short moment of time after the change appeared. The performance of the designed prototype was always able to fulfill the industrial standard requirements and had a good alignment with the topology concept.

6.7 Conclusion

The chapter presented a new bridgeless buck-boost PFC rectifier. It can convert the grid voltage into a wide range of output voltages in both step-up and step-down conditions. Benefiting from the single stage structure, the proposed PFC is simpler than other dual-stage topologies with fewer components required and all the components are fully utilized. Moreover, since an *LC* filter is built in the front stage, a continuous grid current and low CM noise system is also able to be guaranteed. The operating principle and the steady state characteristics of the proposed topology were explained. An 800W prototype has been implemented in order to verify the presented concept. The performance of the proposed bridgeless buck-boost PFC was demonstrated on it with the experimental results. A good agreement is achieved between theoretical concepts and experimental results.

Appendix

A. Derivation of (6.3) and (6.4)

The fundamental current of the converter-side inductor can be found from the grid-side inductor current and system duty cycle. The grid-side inductor current and the relationship with the converter-inductor current are expressed as,

$$i_{\mathrm{G}}(t) = \frac{2 \cdot P_{\mathrm{O}} \cdot \sin \omega t}{V_{\mathrm{G}}}, \tag{A6.1}$$

$$i_{\mathrm{L}}(t) = \frac{i_{\mathrm{G}}(t)}{D(t)}. \tag{A6.2}$$

By putting (A6.1) and (6.2) into (A6.2), (6.3) can be calculated.

The ripple current of the converter-side inductor is related to the energy conversion process. It can be developed from the inductor on-state characteristic as,

$$v_{\mathrm{L,ON}} = V_{\mathrm{G}} |\sin \omega t| = L_{\mathrm{X}} \cdot \frac{\Delta i_{\mathrm{L}}(t)}{D(t) \cdot T}, \tag{A6.3}$$

where *T* is time period.

By putting (6.2) into (A6.3), (6.4) can be calculated.

B. Derivation of (6.5)

As shown in Figure 6-8, the capacitor current is equal to the grid current during the off-state. Therefore, the state equation can be formulated as,

$$i_{\mathrm{C,ON}}(t) = i_{\mathrm{G}}(t) = C_{\mathrm{AB}} \cdot \frac{\Delta v_{\mathrm{C}}(t)}{(1 - D(t)) \cdot T}. \tag{A6.4}$$

By putting (6.2) into (A6.4), (6.5) can be calculated.

C. Derivation of (6.6)

As an *LC* filter structure is formed at the front stage, the capacitor voltage ripple is equal to the grid-side inductor voltage ripple. By approximating the ripple to the triangle waveform, the grid current ripple expression can be formed as,

$$\Delta i_{\mathrm{G}}(t) = \frac{\Delta v_{\mathrm{C}}(t)}{8 \cdot L_{\mathrm{X}} \cdot f_{\mathrm{SW}}}. \tag{A6.5}$$

By putting (A6.4) into (A6.5), (6.6) can be calculated.

D. Derivation of (6.7)

The output capacitor voltage ripple can be determined from the system power equation. The input power and the output power equations are,

$$P_{\mathrm{IN}}(t) = V_{\mathrm{G}} \sin \omega t \cdot I_{\mathrm{G}} \sin \omega t, \tag{A6.6}$$

$$P_{\mathrm{O}}(t) = \frac{{V_{\mathrm{DC}}}^2}{R} + \frac{1}{2} \cdot C_{\mathrm{DC}} \cdot \frac{d}{dt} [V_{\mathrm{DC}} + \frac{\Delta V_{\mathrm{DC}}}{2} \sin(2\omega t)]^2, \tag{A6.7}$$

where *R* is output resistance.

During the steady state, power at the input and output must be equalized. By solving the double line frequency term in (A6.6) and (A6.7), (6.7) can be obtained.

Reference

[6.1] K. K. M. Siu and C. N. M. Ho, "Manitoba rectifier — Bridgeless buck-boost PFC," in *Proc. IEEE ECCE*, pp. 5287-5292, Oct. 2017.

[6.2] M. C. Kisacikoglu, M. Kesler, and L.M. Tolbert, "Single-Phase On-Board Bidirectional PEV Charger for V2G Reactive Power Operation," *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 767-775, Oct. 2014.

[6.3] V. Monteiro, J. G. Pinto, and J. L. Afonso, “Operation Modes for the Electric Vehicle in Smart Grids and Smart Homes: Present and Proposed Modes,” *IEEE Trans. Veh. Technol.*, vol. 65, no. 3, pp. 1007-1020, Mar. 2016.

[6.4] V. Bist and B. Singh, “An Adjustable-Speed PFC Bridgeless Buck–Boost Converter-Fed BLDC Motor Drive,” *IEEE Trans. Ind. Electron.*, vol. 61, no. 6, pp. 2665-2677, Dec. 2013.

[6.5] S. T. S. Lee, H. S. H. Chung, and S. Y. R. Hui, “A novel electrode power profiler for dimmable ballasts using DC link voltage and switching frequency controls,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 847-853, May 2004.

[6.6] E. Jang, S. M. Park, D. Joo, H. M. Ahn, and B. K. Lee, “Feasibility Study on All Metal Induction Cooker Systems Considering Topology and Control,” in *Proc. IEEE ECCE*, pp. 936 – 941, Sept. 2018.

[6.7] E. H. Ismail, “Bridgeless SEPIC Rectifier With Unity Power Factor and Reduced Conduction Losses,” *IEEE Trans. Ind. Electron.*, vol. 56, no. 4, pp. 1147–1157, Oct. 2008.

[6.8] A. J. Sabzali, E. H. Ismail, M. A. Al-Saffar, and A. A. Fardoun, “New Bridgeless DCM Sepic and Cuk PFC Rectifiers With Low Conduction and Switching Losses,” *IEEE Trans. Ind. Appl.*, vol. 67, no. 2, pp. 873–881, Jan. 2011.

[6.9] W. Wei, L. Hongpeng, J. Shigong, and X. Dianguo “A Novel Bridgeless Buck-Boost PFC Converter,” in *Proc. IEEE Power Electronics Specialists Conference*, pp. 1304 – 1308, Jun. 2008.

[6.10] W. Lin, “Boost and buck integrated bridge-free power factor correction (PFC) circuit,” *CN Patent*, No. CN102005915(B), April 2011.

[6.11] W. Lin and H. Lin, “Bridgeless power factor correction circuit with low voltage stress for wide voltage output,” *CN Patent*, No. CN102130576(B), Jan. 2013.

[6.12] C. Hsieh, M. Moallem, and F. Golnaraghi, “A Simple Bi-directional Bridgeless AC/DC Buck-Boost Converter for Automotive Energy Harvesting,” in *Proc. IEEE IECON*, pp. 1937-1943, Oct. 2014.

[6.13] B. Zhao, A. Abramovitz, and K. Smedley, “Family of Bridgeless Buck-Boost PFC Rectifiers,” *IEEE Trans. Ind. Electron.*, vol. 30, no. 12, pp. 6524–6527, Dec. 2015.

[6.14] K. Leong and A. Muetze, “An Analysis into Bridgeless Inverted Buck-Boost PFC with ZVS Capabilities,” in *Proc. EPE’14 ECCE Europe*, pp. 1-10, Aug. 2014.

[6.15] S. Singh, B. Singh, G. Bhuvaneswari, and V. Bist, “Improved Power Quality Switched-Mode Power Supply Using Buck–Boost Converter,” *IEEE Trans. Ind. Appl.*, vol. 52, no. 6, pp. 5194-5202, Nov.-Dec. 2016.

[6.16] C. N. M. Ho and K. K. M. Siu, “Manitoba Inverter – Single Phase Single-Stage Buck-Boost VSI Topology,” *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3445-3456, April 2019.

[6.17] C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, “Active Virtual Ground - Bridgeless PFC Topology,” *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017.

[6.18] K. K. M. Siu, Y. He, C. N. M. Ho, H. S. H. Chung, and R. T. H. Li, “Advanced Digital Controller for Improving Input Current Quality of Integrated Active Virtual Ground-Bridgeless PFC,” *IEEE Trans. Power Electron*., vol. 34, no. 4, pp. 3921-3936, April 2019.

[6.19] Y. He, K. W. Wang, and H. S. H. Chung, “Utilization of Proportional Filter Capacitor Voltage Feedforward to Realize Active Damping for Digitally Controlled Grid-Tied Inverter Operating Under Wide Grid Impedance Variation,” in *Proc. IEEE ECCE*, pp. 4450 – 4457, Sept. 2014.

[6.20] R. Wang et al., “A High Power Density Single-Phase PWM Rectifier With Active Ripple Energy Storage,” *IEEE Trans. Power Electron.*, vol. 26, no. 5, pp. 1430-1443, May 2011.

[6.21] H. Li, K. Zhang, H. Zhao, S. Fan, and J. Xiong, “Active Power Decoupling for High-Power Single-Phase PWM Rectifiers,” *IEEE Trans. Power Electron.*, vol. 28, no. 3, pp. 1308-1319, March 2013.

[6.22] *Effects of current on human beings and livestock – Part 1: General Aspects*, IEC Standard 60479-1-2005, 2005.

[6.23] *Household and similar electrical appliances - Safety - Part 1: General requirements*, IEC Standard 60335-1:2010, 2010.

[6.24] S. Wang, P. Kong, and F. C. Lee, “Common Mode Noise Reduction for Boost Converters Using General Balance Technique,” *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1-6, Jul. 2007.

[6.25] P. Kong, S. Wang, and F. C. Lee, “Common Mode EMI Noise Suppression for Bridgeless PFC Converters,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 291-297, Jan. 2008.

[6.26] C.N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. A. Serpa, and A. Coccia, “Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications, ” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2835-2845, June 2012.

[6.27] C. N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, and F. Canales, “A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 289-299, Jan. 2013.

[6.28] Z. Zhao, Q. Xu, Y. Dai, A. Luo, and Y. Chen, “Efficiency optimization design of LLC resonant converter for battery charging, ” in *Proc. IEEE ICIEA*, pp. 928-933, Jun. 2018.

[6.29] M. A. Hannan, M. M. Hoque, A. Hussain, Y. Yusof, and P. J. Ker, “State-of-the-Art and Energy Management System of Lithium-Ion Batteries in Electric Vehicle Applications: Issues and Recommendations,” *IEEE Access*, vol. 6, pp. 19362-19378, 2018.

[6.30] *IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*, IEEE 519-2014, 2014.

Chapter 7 Manitoba Inverter – Single-Stage Buck-Boost VSI Topology

The work described in this chapter was published in the following paper: C. N. M. Ho and K. K. M. Siu, "Manitoba Inverter—Single-Phase Single-Stage Buck-Boost VSI Topology," *IEEE Trans. Power Electron.*, vol. 34, no. 4, pp. 3445-3456, April 2019. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2017 [7.1].

7.1 Abstract

The chapter presents a new transformerless single-phase single-stage buck-boost grid-connected voltage source inverter (VSI) topology. The topology can achieve efficient power conversion with a wide input voltage range, the number of magnetic devices reduction and low leakage current. The proposed VSI topology consists of high frequency semiconductors for shaping inductor currents, and low frequency semiconductors to form grid *CL* filter structure for different conditions. This *CL* filter uses the same buck-boost inductor, thus no additional line frequency inductor is required. Besides, common mode (CM) voltage, the main problem of transformerless grid-connected VSI, is mitigated, since the capacitor in the *CL* filter clamps the voltage between the grid and the bus terminal. The performance of the proposed VSI is experimentally verified. The results show that the proposed VSI guarantees sinusoidal output current and wide input voltage range, and has a good agreement with the theoretical findings.

7.2 Introduction

Technology of single-phase (1-phase) grid-connected Voltage Source Inverter (VSI) has been rapidly developed in the last decade associates to the product development of uninterrupted power supply (UPS) [7.2], Photovoltaic (PV) inverter [7.3] and regenerative motor drive [7.4]. Advanced topology facilitates the increments of system efficiency and power density which leads researchers and engineers to propose and develop novel topologies. As well as efficiency and power density, material cost is another critical performance index to be minimized particularly in low power products. Thus, topology is the fundamental component of a VSI to achieve optimal performance. And it is also the key to satisfy industrial standards for Power Electronics products.

Particularly for 1-phase transformerless PV inverters technology, most of the low rated power (e.g. 1 kW, 120 V) PV inverters on the market are using two power stages, a dc-dc MPPT tracker and a VSI such as shown in the upper diagram of Figure 7-1. Since the output voltage of PV panel (e.g. 70 V – 200 V) in that low power range is sometimes not high enough to be over the peak value of grid voltage (e.g. 170 V) [7.5], [7.6]. It typically requires a boost converter to step up the voltage in a dc link (e.g. 250 V – 400 V) for a buck-type VSI to deliver power to the gird. Although the two-stage structure is straight forward for controller design and power processing, it is inefficient and bulky, as requiring two high frequency (HF) switching power stages to process the conversion. Besides, leakage current, which is led by HF Common Mode (CM) voltage, is generated if the topology or the modulation is not specifically designed for PV systems. Notice that leakage current is limited by industrial standards [7.7], [7.8] due to safety and reliability issues. Therefore, some VSI topologies as second power stage in a transformerless 1-phase PV inverter have been proposed based on a buck-type full-bridge inverter mainly for providing efficient switching and the leakage current reduction, such as H5 [7.9], Heric [7.10] and Active Virtual

Ground (AVG) [7.11]. However, the drawbacks are that they require more semiconductors in the circuit to disconnect or bypass the HF CM current path during the switching process. Although they solved the CM current problem, cost increases and the system efficiency are influenced, especially operating in a two-stage power processing. Thus, a single power stage topology becomes attractive for low power transformerless products.

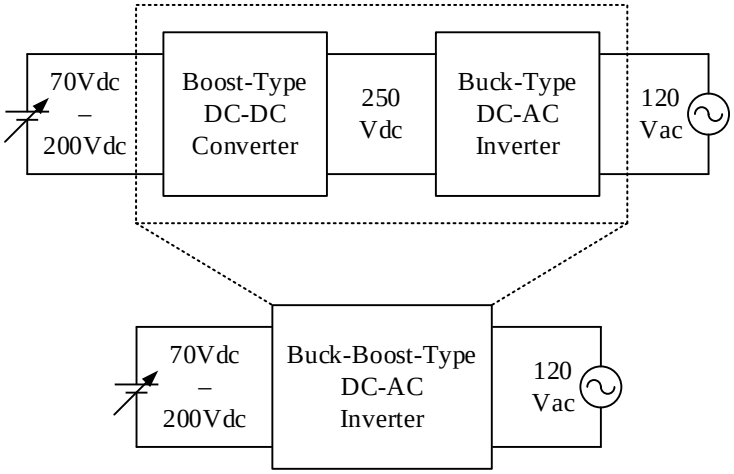


Figure 7-1. Typical power inverter structures with a variable and low input dc voltage.

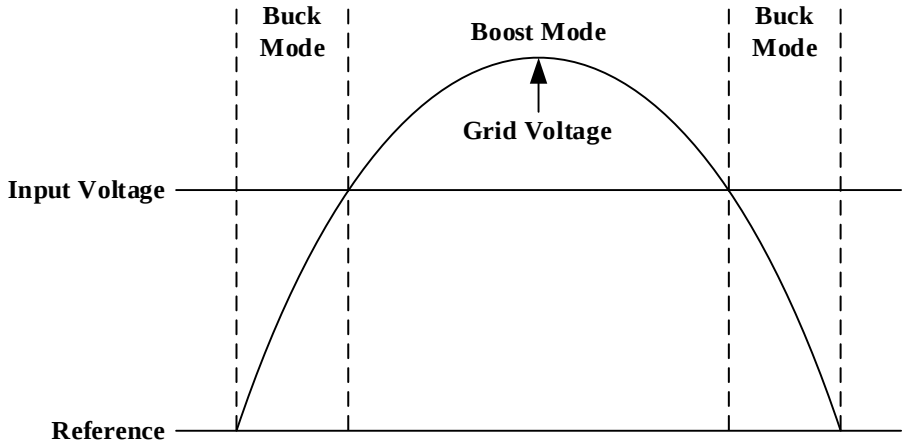


Figure 7-2. Input and output voltages of a inverter and its operating modes.

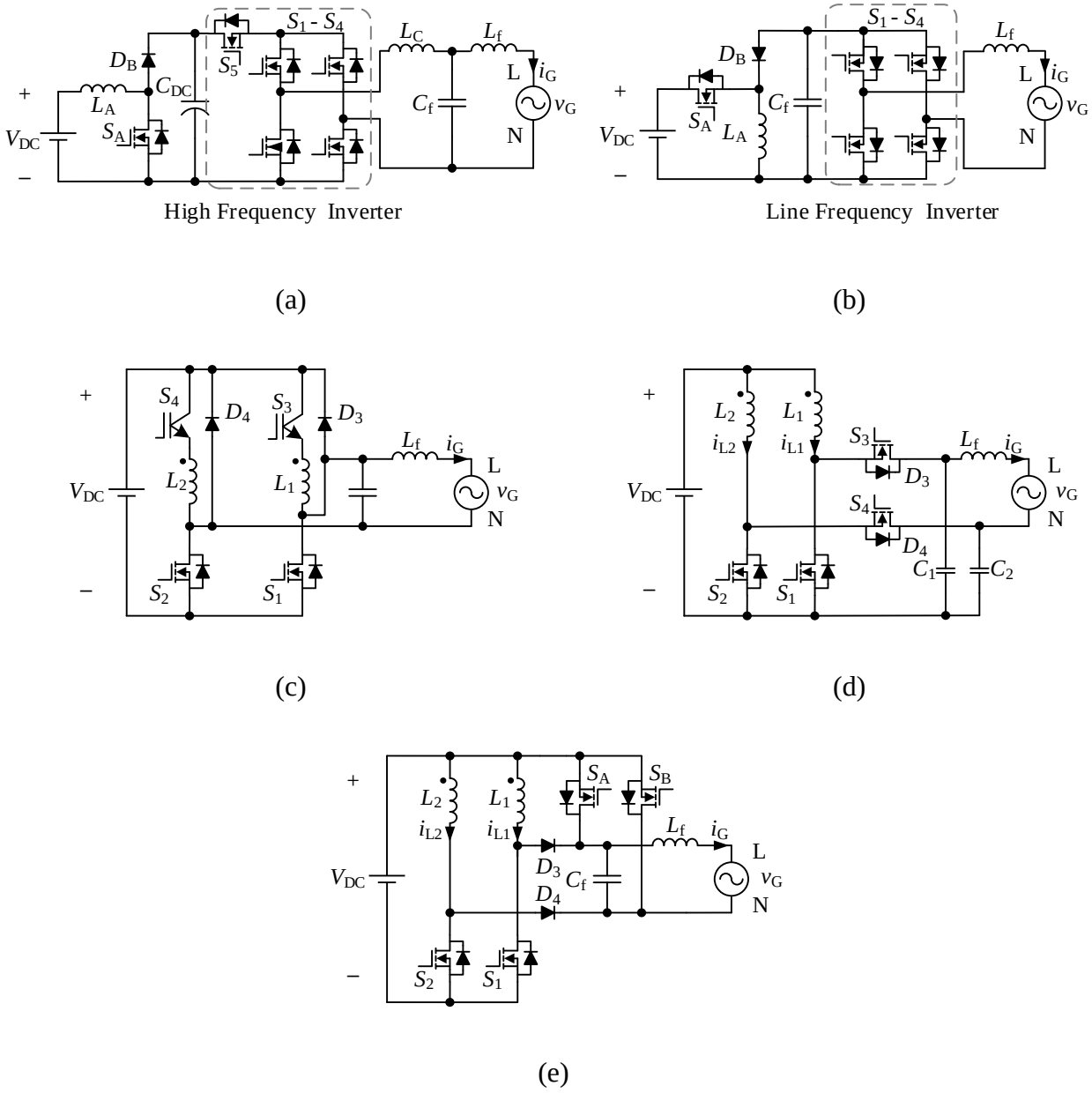


Figure 7-3. The prior-arts of transformerless buck-boost inverter, (a) [7.5], (b) [7.14], (c) [7.16], (d) [7.17] and (e) [7.18].

TABLE 7-I SUMMARY OF NUMBERS OF SEMICONDUCTOR DEVICES AND PASSIVE COMPONENTS INVOLVED IN THE TOPOLOGIES

Topologies	No. of components in the circuit					No. of components in the main current path	
	LF Semicond.	HF Semicond.	Inductor	DC Cap.	Filter Cap.	Turn-on	Turn-off
Figure 7-3 (a)	0	6	3	1	1	3	3
Figure 7-3 (b)	4	2	2	0	1	3	3
Figure 7-3 (c)	2	4	3	0	1	2	2
Figure 7-3 (d)	0	4	3	0	2	2	2
Figure 7-3 (e)	2	4	3	0	1	1	2
Figure 7-4 (proposed)	2	4	2	0	1	1	2

A single power stage PV inverter requires a buck-boost-type dc-ac inverter such as shown in the bottom diagram in Figure 7-1. A typical input and output voltage waveforms are shown in Figure 7-2. It shows that the inverter operates as buck mode when the input voltage is higher than the grid voltage and as boost mode when they are opposite. It creates challenges for designing a single stage inverter which can operate in the modes and satisfy the mentioned industrial standards at the same time. Figure 7-3 shows some prior-art solutions including dual-stage and single-stage power processing. A summary of components count is shown in TABLE 7-I which is used to indicate the major difference between those reviewed topologies. In Figure 7-3 (a), it is a typical dual-stage topology [7.7], it requires a boost converter to create a high voltage dc link and uses a HF buck-type inverter, such as H5, Heric, and AVG, to inject the power to the grid. There are two HF power stages in the system, high switching loss and high conduction loss are expected. There is another topology which is a time-sharing cascaded dual mode inverter [7.12], [7.13]. On top of [7.7], a bypass diode is adding into the circuit which links up the dc input and the dc bus together. Based on the output voltage level, either boost conversion or buck conversion is applied. With the

time-sharing technique, the numbers of HF switches are less in each half line cycle operation. The size of the dc link capacitor is reduced. However, the conduction loss is kept in a high magnitude as at least three semiconductors in the current path. Figure 7-3 (b) shows a buck-boost converter with an unfolding inverter [7.14], [7.15]. The buck-boost converter creates a rectified sinewave voltage across the filter capacitor and uses a line frequency inverter to convert it to a sinewave. Although only two HF components are required, high conduction loss is created as at least three semiconductors in the current path. In Figure 7-3 (c), it consists of two individual buck-boost cells [7.16]. When the grid is in the positive half line cycle, switch S_1 is at HF switching with freewheeling diode D_4. The disadvantage is that it has at least two power semiconductors, e.g. S_3 and S_1, in the current path which will increase the conduction losses of the converter. In Figure 7-3 (d), it uses two boost converters to create two capacitor voltages and the difference of the converters makes sinusoidal output voltage and current [7.17]. This requires two HF converters operating at the same time, thus overall switching loss is high. Figure 7-3 (e) shows a very interesting buck-boost inverter topology, it uses an additional switch to bypass an idle buck-boost switching cell for half line cycle [7.18]. It effectively steps up and down the voltage and clamps the CM voltage by the additional switches. However, the drawback is similar to other mentioned topologies, it is required a bulky filter inductor to filter out the HF components in the grid current, power density and cost are the issues. Other possible topologies have been well documented in the literature and they are based on the above five topologies with additional features [7.19].

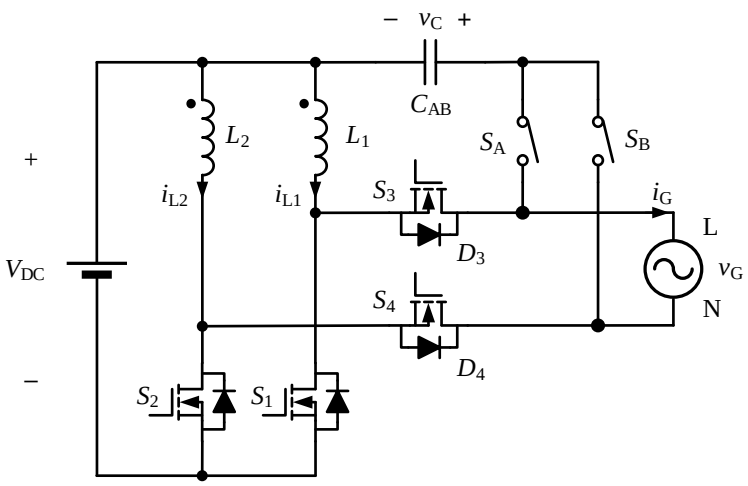


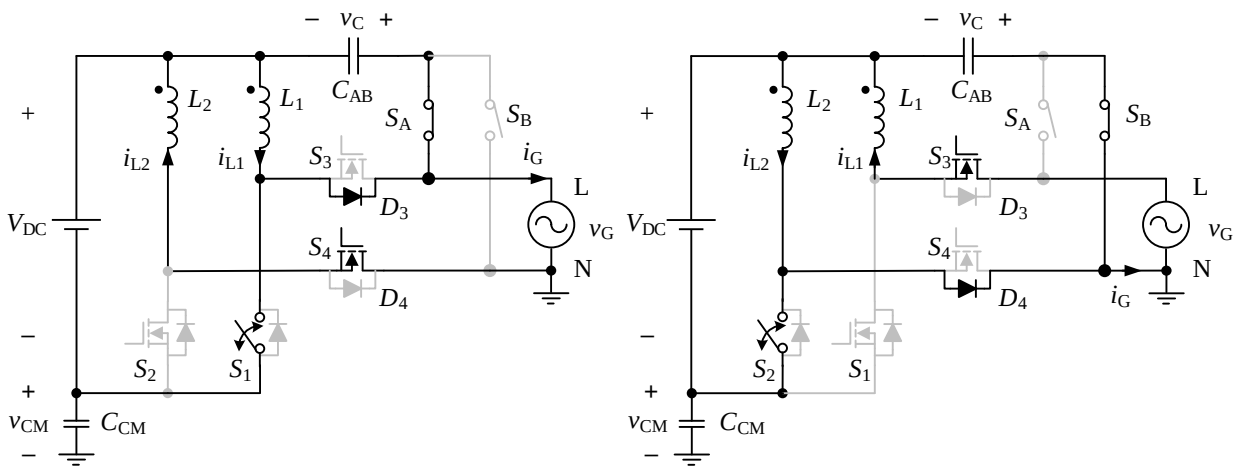
Figure 7-4. The proposed Manitoba Inverter topology.

This chapter proposes a new transformerless single-phase single-stage buck-boost grid-connected VSI circuit to transform dc voltage to ac voltage, namely Manitoba Inverter. The main advantages of the proposed topology are 1) wide input range with a single power stage, 2) sinusoidal continuous grid current and without additional grid inductor requirement, 3) low CM voltage with transformerless design, and 4) only one switch under HF operation in each half line cycle. Since Manitoba Inverter is able to support a very wide input dc voltage range, it is very promising for PV applications. In Figure 7-4, it shows the proposed circuit. The VSI consists of two buck-boost switching cells and a configurable *CL* filter circuit. The switches for configuring the *CL* filter is based on the recently proposed AVG concept [7.11], [7.20]. The configurable *CL* filter circuit can change the output filter to different *CL* structures depending on grid voltage polarities by using the built-in buck-boost inductors. This approach eliminates a bulky grid inductor in the system. In addition, since the VSI uses the AVG concept, it mitigates the CM voltage issue by using the capacitor in *CL* filter to clamp the voltage between the grid and the positive terminal of the dc bus. Thus, the leakage current is minimized, it is important for PV inverters due to industrial standards [7.7] - [7.8]. In each switching cycle, only one switch is operating under HF switching and the others are under line frequency operation. Therefore, the

overall switching loss is minimized. This chapter will define the problems, explain the operating principle of the proposed inverter, provide static characteristics, and use experimental results to verify the proposed concept. An 800 W, 120 V laboratory prototype has been implemented and is used to demonstrate the performance of the proposed topology.

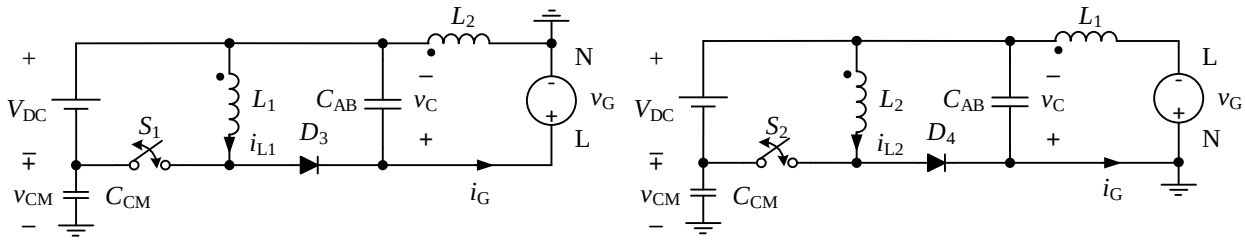
7.3 Principles of Operation

The proposed buck-boost VSI is shown in Figure 7-4, which is able to convert a dc bus voltage into an ac grid voltage either the dc bus voltage higher or lower than the peak value of ac grid and to deliver sinusoidal grid current to the grid. The circuit includes two buck-boost switching cells and a configurable *CL* filter circuit, namely AVG circuit. The configurable *CL* filter circuit filters out switching frequency components which are generated by the buck-boost cells, and issues a continuous sinusoidal current to the grid. The AVG circuit consists of two bidirectional switches (S_{A} and S_{B}), and they are connected to the Line (L) and Neutral (N) of the grid separately. The bidirectional switches, namely AVG switches, can be realized by connecting two back-to-back low cost MOSFETs in series or in other configurations to provide bidirectional blocking and conducting. The AVG switches operate at line frequency and their gating actions are synchronized with the zero-crossing points of the grid voltage. The switches switch alternatively which are depending on the polarity of the grid voltage. The circuit also includes a capacitor (C_{AB}), namely AVG capacitor, that is coupled between the junction point of two bidirectional switches and the positive terminal of dc bus (V_{DC}). It is used to clamp the potential difference between the dc bus and the ac ground in order to minimize the CM voltage and it is used to form a *CL* filter as an output grid filter.



(a) (b)

Figure 7-5. Current conducting paths of the proposed VSI in (a) positive line cycle, and (b) negative line cycle.



(a) (b)

Figure 7-6. Equivalent circuits of the proposed VSI in (a) positive line cycle, and (b) negative line cycle.

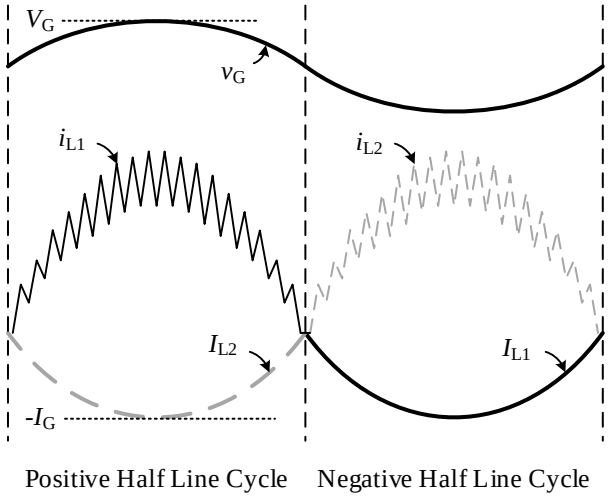


Figure 7-7. Ideal inductor current waveforms.

7.3.1 Operating Mode: Positive Half Line Cycle

In Figure 7-5 (a), the proposed buck-boost VSI works in positive half line cycle. In this half line cycle, C_{AB} is connected to the Line (L) of the grid voltage through the bidirectional switch (S_{A}), the main switch (S_2) is always open and the main switch (S_1) is switching at a HF for shaping the inductor current i_{L1}. Figure 7-6 (a) is the corresponding equivalent circuit of Figure 7-5 (a), note that S_{A} and S_4 are always conducting and S_2 is always open in this half line cycle thus they are not shown in the circuit. It can be seen that the inverter forms a buck-boost converter with L_1, and a *CL* filter is formed with C_{AB} and L_2 between the grid and the buck-boost converter. In this case, L_2 takes the role of grid inductor, then low grid differential mode (DM) current ripple is achieved. The corresponding inductor current waveform is shown in Figure 7-7. Specifically for PV applications, a parasitic capacitor presents in between PV cells and ac ground. In Figure 7-5 and Figure 7-6, a capacitor, C_{CM}, represents the parasitic capacitor of the system [7.11]. This capacitor is the main contributor of the HF leakage current when a HF potential difference changes across the capacitor. Thus, the voltage, v_{CM}, should be kept as stable and avoid to be affected by

the switching actions in the main converter circuit. In the proposed system, C_{AB} is coupled between Line (L) and the positive terminal of dc bus, the CM capacitor voltage can be determined by,

$$v_{\mathrm{CM}}(t) = v_{\mathrm{G}}(t) - v_{\mathrm{C}}(t) - V_{\mathrm{DC}}, \tag{7.1}$$

where v_{CM} is CM voltage, v_{C} is capacitor voltage of C_{AB}, and v_{G} is grid voltage with a positive value.

According to (7.1), there are no HF voltage changes in the terms, the potential difference of the parasitic capacitor C_{CM} is clamped. Therefore, low HF leakage current is achieved. Furthermore, from the HF signals point of view, the impedance of the voltage source in (7.1) is very low, it looks like the dc bus terminal is connecting to the ac ground, therefore, the technology is namely Active Virtual Ground (AVG) [7.11] - [7.20].

7.3.2 Operating Mode: Negative Half Line Cycle

In Figure 7-5 (b), the proposed buck-boost VSI works in negative half line cycle. In this half line cycle, the AVG capacitor (C_{AB}) is connected to the Neutral (N) of the grid voltage through the bidirectional switch (S_{B}), the main switch (S_1) is always open and the main switch (S_2) is switching at a HF for shaping the inductor current i_{L2}. Figure 7-6 (b) is the corresponding equivalent circuit of Figure 7-5 (b), note that S_{B} and S_3 are always conducting and S_1 is always open in this half line cycle thus they are not shown in the circuits. As well as the system in the positive half line cycle that the inverter forms a buck-boost converter with L_2, and a *CL* filter is formed with C_{AB} and L_1 between the grid and the buck-boost converter. In this case, L_1 takes the role of grid inductor, then low grid differential mode (DM) current ripple is achieved. The corresponding inductor current waveform is shown in Figure 7-7. C_{AB} is coupled between Neutral (N) and the positive terminal of dc bus, the CM capacitor voltage can be determined by,

$$v_{\mathrm{CM}}(t) = -V_{\mathrm{DC}} - v_{\mathrm{C}}(t). \tag{7.2}$$

According to (7.2), there are no HF voltage changes in the terms, the potential difference of the parasitic capacitor C_{CM} is clamped, therefore, low HF leakage current is achieved. However, $v_{\mathrm{C}}(t)$ presents in the equation and it is a line frequency varying component, thus line frequency component presents in the CM voltage.

7.4 Steady State Characteristics

The equivalent circuits in Figure 7-6 show that the system could be modelled as a simple buck-boost converter in each half line cycle, thus steady state characteristics can be determined by using buck-boost converter characteristics with time varying output voltage and current. The corresponding characteristic waveforms are shown in Figure 7-8.

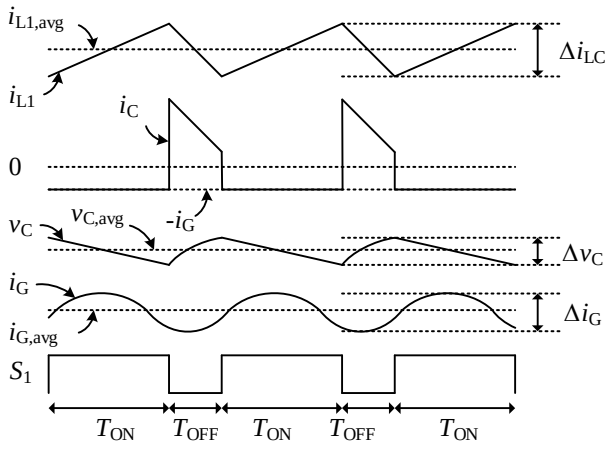


Figure 7-8. Steady-Stage waveforms.

In order to simplify the topology analysis, the inductors are assumed as identical, thus,

$$L_{\mathrm{X}} = L_1 = L_2, \tag{7.3}$$

where L_X is inductance of the inductors in the Manitoba Inverter topology.

By using the power flow transfer equation from v_{C} to v_{G} in Figure 7-6, the output power of the inverter can be obtained as,

$$P = \frac{V_{\mathrm{C}} V_{\mathrm{G}}}{\omega L_{\mathrm{X}}} \sin \delta, \tag{7.4}$$

where V_{C} and V_{G} are peak amplitude of capacitor (C_{AB}) voltage and grid voltage, respectively, ω is angular line frequency and δ is relative phase angle between the two voltage sources.

A. Grid Voltage and AVG Capacitor Voltage

It can be seen that from (7.4), δ is proportional to the inductance if the transferring power is constant. The inductor is half line cycle working as a grid inductor and half line cycle working as a buck-boost converter inductor, the value is typically in micro-Henry (μH) scale. Thus, the phase angle is small and the voltage drop on the grid inductor can be neglected in order to simplify the calculations. By assuming the AVG capacitor voltage v_C is almost the same as the rectified grid voltage. It can be expressed as,

$$v_{\mathrm{C}}(t) \approx |v_{\mathrm{G}}(t)| = V_{\mathrm{G}} |\sin \omega t|. \tag{7.5}$$

B. Grid Current

The control objective of the grid-connected inverter is to inject power to the grid and to keep the output current is in-phase with the grid voltage, thus the grid current can be expressed as,

$$i_{\mathrm{G}}(t) = I_{\mathrm{G}} \sin \omega t, \tag{7.6}$$

where I_{G} are peak amplitude of grid current.

C. Duty Ratio

Figure 7-6 shows the buck-boost converter transferring energy from the dc source to the AVG capacitor. The operation of the inverter is the same as a simple buck-boost converter. Thus, the duty ratio D can be expressed by,

$$D(t) = \frac{|v_{\mathrm{G}}(t)|}{|v_{\mathrm{G}}(t)|+V_{\mathrm{DC}}}. \tag{7.7}$$

It shows that the duty ratio is time varying in a line cycle following the change of grid voltage.

D. Low Frequency Buck-Boost Inductor Current

The inductor energy is transferring to the grid during the OFF-state operation as shown in Figure 7-9 (b). During the steady state situation, the OFF-state inductor current will equal to the average grid current over a completed duty cycle. Therefore, the low frequency buck-boost inductor current, $i_{\mathrm{LC}}(t)$, can be expressed as,

$$i_{LC}(t) = \frac{|i_{\mathrm{G}}(t)|(|v_{\mathrm{G}}(t)|+V_{\mathrm{DC}})}{V_{\mathrm{DC}}}. \tag{7.8}$$

E. Buck-Boost Inductor Current Ripple

By making assumptions that the inverter works with a constant switching frequency and continuous-conduction mode inductor current, the converter-side current ripple Δi_{LC} can be found from the inductor ON-state equation as follows,

$$v_{\mathrm{LC}} = L_{\mathrm{X}} \frac{\Delta i_{\mathrm{LC}}}{T_{\mathrm{ON}}}, \tag{7.9}$$

where v_{LC} is voltage across the switching inductor and T_{ON} is turn-on period in a switching cycle,

As shown in Figure 7-9 (a), v_{LC} is equal to V_{DC} during the ON-state operation. By using the relationships between the duty ratio D, the switching frequency f_{sw} and the time period and T_{ON}, the buck-boost inductor current ripple can be determined as,

$$\Delta i_{\mathrm{LC}}(t) = \frac{V_{\mathrm{DC}} D(t)}{L_{\mathrm{X}} f_{\mathrm{sw}}}. \tag{10}$$

And by putting (7.7) into (7.10), the instantaneous inductor ripple equation of Δi_{LC} can be obtained as,

$$\Delta i_{\mathrm{LC}}(t) = \frac{1}{L_{\mathrm{X}} f_{\mathrm{sw}}} \frac{|v_{\mathrm{G}}(t)| V_{\mathrm{DC}}}{|v_{\mathrm{G}}(t)| + V_{\mathrm{DC}}}. \tag{7.11}$$

It shows that the current ripple size is time varying in a line cycle.

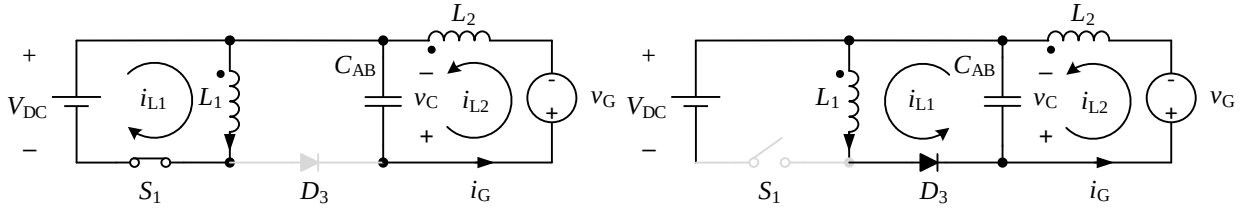


Figure 7-9. Operating modes of a buck-boost converter, (a) ON-state Mode and (b) OFF-state Mode.

F. AVG Capacitor Voltage Ripple

The voltage ripple of AVG capacitor is created by charging the capacitor with the discontinuous diode current. The buck-boost inductor releases the current to the capacitor during the OFF-state of the HF switching switch. During the ON-state, the capacitor current is the same as the grid inductor current which can be simplified as a constant current in a short switching period. Thus, the capacitor voltage ripple peak to peak value Δv_{C} is defined as,

$$i_{\mathrm{C}} = C_{\mathrm{AB}} \frac{\Delta v_{\mathrm{C}}}{T_{\mathrm{ON}}}, \tag{7.12}$$

where i_{C} is current of AVG capacitor.

(7.12) can be modified as,

$$\Delta v_{\mathrm{C}}(\mathrm{t}) = \frac{D(t)\cdot|i_{\mathrm{G}}(t)|}{C_{\mathrm{AB}} f_{\mathrm{sw}}}. \tag{7.13}$$

By putting (7.7) into (7.13), the following equation can be obtained.

$$\Delta v_{C}(\mathrm{t}) = \frac{|v_{\mathrm{G}}(t)||i_{\mathrm{G}}(t)|}{|v_{\mathrm{G}}(t)|+V_{\mathrm{DC}}} \frac{1}{C_{\mathrm{AB}} f_{\mathrm{sw}}}. \tag{7.14}$$

It shows that the voltage ripple size is time varying in a line cycle.

G. Grid Inductor Current Ripple

From the *CL* filter characteristic, the grid-side inductor will face the same HF voltage ripple as the one appeared on the AVG capacitor. As shown in Figure 7-8, the capacitor ripple voltage is much closer to a triangular wave. Therefore, under triangular wave approximation, the grid inductor current ripple, $\Delta i_{\mathrm{LG}}(t)$, can be expressed as,

$$\Delta i_{\mathrm{G}}(t) \approx \frac{\Delta v_{\mathrm{C}}(t)}{8\cdot L_{\mathrm{X}}\cdot f_{\mathrm{SW}}}. \tag{7.15}$$

By putting (7.14) into (7.15), the following equation can be obtained.

$$\Delta i_{\mathrm{G}}(t) \approx \frac{1}{8 C_{\mathrm{AB}} L_{\mathrm{X}} {f_{\mathrm{sw}}}^2} \frac{|v_{\mathrm{G}}(t)||i_{\mathrm{G}}(t)|}{|v_{\mathrm{G}}(t)|+V_{\mathrm{DC}}}. \tag{7.16}$$

It shows that the grid current ripple size is smaller than the buck-boost inductor current ripple and also time varying.

H. High Frequency CM Voltage Amplitude

By applying the HF analysis to Figure 7-6, the corresponding HF equivalent model is generated as shown in Figure 7-10. On the model, a capacitor, C_{CM}, is used to represent the parasitic capacitor between the Earth and the Negative bus terminal of the inverter. The voltage generated on the C_{CM} presents the CM voltage and the current passing through C_{CM} is defined as the leakage current. In the analysis model, C_{CM} is always paralleled to the filter capacitor C_{AB}, there CM voltage ripple is guaranteed as the filter capacitor helps to clamp the potential difference between the dc bus and the ac ground. By modifying (14), the CM voltage, $\Delta v_{CM}(t)$, can be expressed as,

$$\Delta v_{CM}(t) = \frac{|v_G(t)||i_G(t)|}{|v_G(t)|+V_{DC}} \frac{1}{(C_{AB}+C_{CM})f_{sw}}. \tag{7.17}$$

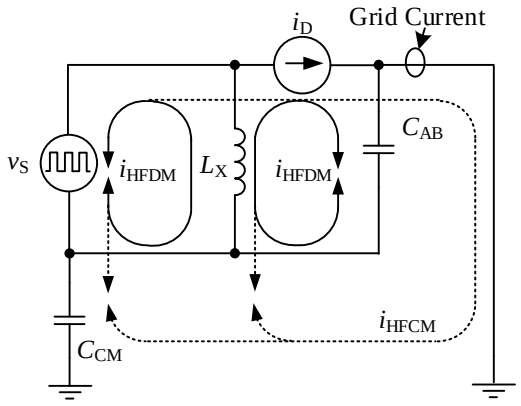


Figure 7-10. High frequency equivalent model.

I. Leakage Current Amplitude

From Figure 7-8, it shows that a discontinuous current is passing through the filter capacitor current in every completed switching cycle. As C_{CM} is paralleled to $C_{AB,}$ the leakage current amplitude, $\Delta i_{CM}(t)$, that appears in C_{CM} can be found under the current divider theory as,

$$\Delta i_{\mathrm{CM}}(t) = \frac{C_{\mathrm{CM}}}{C_{\mathrm{AB}}+C_{\mathrm{CM}}}\left(i_{\mathrm{LG}}(t) + \frac{\Delta i_{\mathrm{LG}}(t)}{2}\right). \tag{7.18}$$

By putting (7.11) and (7.16) into (7.18), the following equation can be obtained.

$$\Delta i_{\mathrm{CM}}(t) = |v_{\mathrm{G}}(t)||i_{\mathrm{G}}(t)|\frac{C_{\mathrm{CM}}}{C_{\mathrm{AB}}+C_{\mathrm{CM}}}\left(\frac{1}{V_{\mathrm{DC}}|v_{\mathrm{G}}(t)|} + \frac{1}{16C_{\mathrm{AB}}L_{\mathrm{X}}f_{\mathrm{sw}}{}^{2}(|v_{\mathrm{G}}(t)|+V_{\mathrm{DC}})}\right). \tag{7.19}$$

The capacitor value of C_{AB} is always much larger than the capacitor value of C_{CM}, therefore, the leakage current amplitude is able to minimize into a small level.

7.5 System Design and Implementation

7.5.1 Variants of Topology

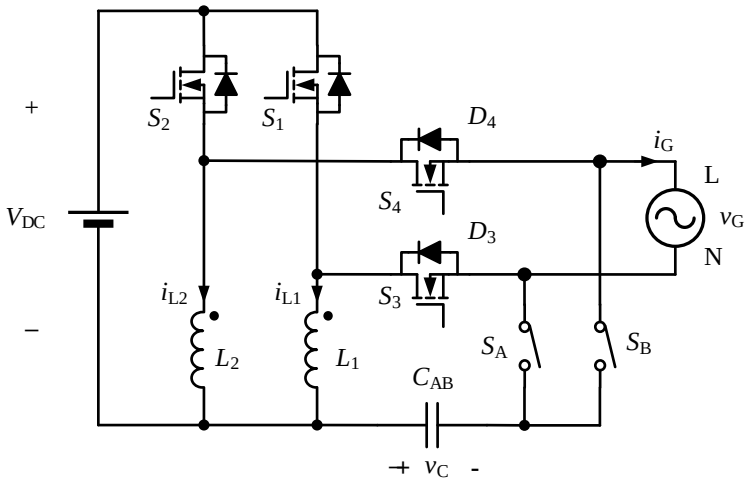


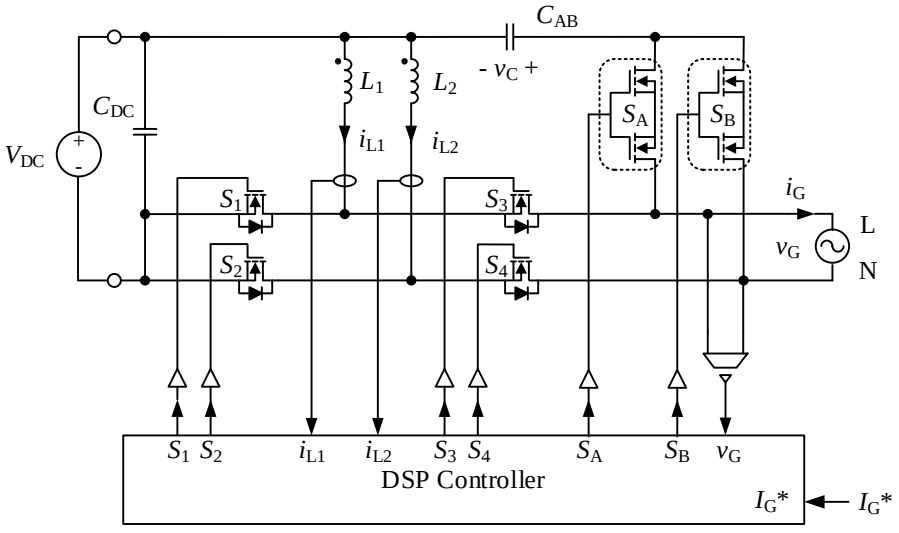
Figure 7-11. Mirrored topology of Figure 7-4.

Figure 7-4 is one of the topologies of the Manitoba Inverter topology family. The family is defined as a buck-boost inverter using the AVG circuit which can create the equivalent circuits as Figure 7-5. Another topology example is shown in Figure 7-11. The functionality of the circuit is the same as Figure 7-4. However, the circuit is mirrored, the inductors connect to the negative terminal of the dc input source. Other variants can be used two separated capacitors instead of one

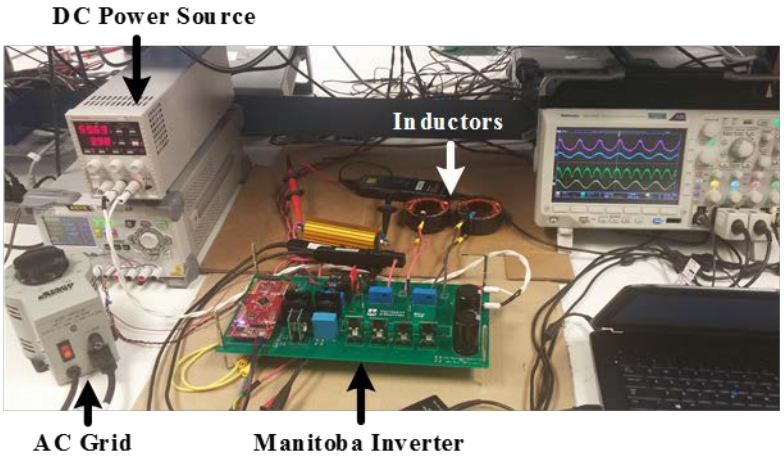
C_{AB}, each capacitor is in series with one AVG switch (S_A or S_B). Nevertheless, all the variants of the Manitoba Inverter would provide similar electrical performance.

7.5.2 System Implementation

An 800 W, 120 V ac output buck-boost grid-connected VSI prototype has been implemented to evaluate the proposed topology in Figure 7-4. TABLE 7-II shows the specification and key parameters of the prototype. The prototype is used to verify the operating principle and feasibility of the proposed topology. The prototype can manage a wide input dc voltage range from 60 V to 200 V, which covers the range of lower and higher of the output voltage peak value (170 V). Figure 7-12 (a) shows the connection block diagram of the prototype. There are six gate signals from the DSP, and two inductor currents and one grid voltage sensing signals to the DSP for control and protection purposes. Figure 7-12 (b) shows the single PCB Manitoba Inverter prototype and the experimental setup in the laboratory.



(a)



(b)

Figure 7-12. Testbed, (a) connection block diagram, and (b) laboratory setup.

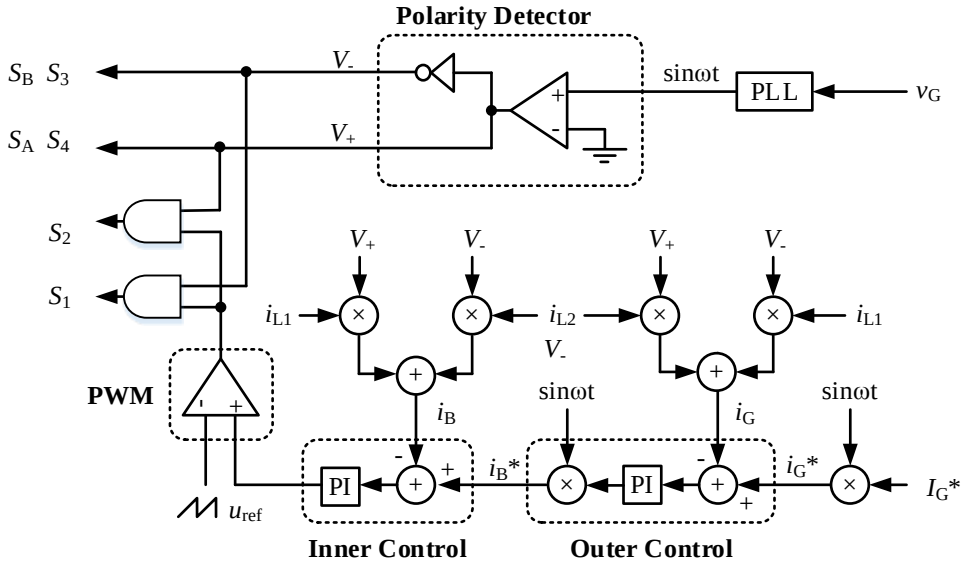
TABLE 7-II SPECIFICATION OF THE PROTOTYPE OF MANITOBA INVERTER

Parameter	Value	Parameter	Value
Input Dc Voltage	60 – 200 V	Grid Ac Voltage	120 V (60 Hz)
Max. Output Power	800 W	Switching Frequency	20 kHz
L_1 & L_2	780 µH	C_{AB}	6.8 µF

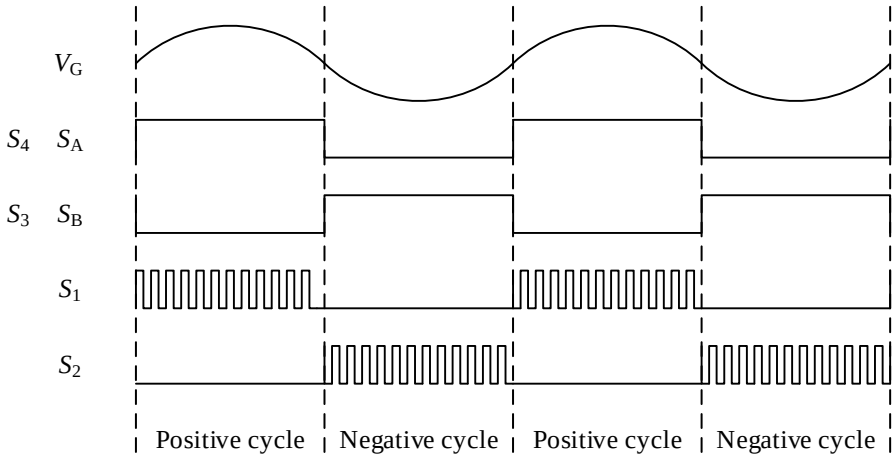
7.5.3 Controller Design

The roles of inductors L_1 and L_2 are interchanged in every half line cycle as a buck-boost inductor and grid inductor, thus additional line filter inductors are not required in the topology. Furthermore, only two current sensors are required for providing current signals to the controller. Figure 7-13 (a) shows the simplified control block diagram of the proposed Manitoba Inverter topology. There are two control loops in the system with Proportional Integral (PI) controllers. The outer loop is to regulate the grid inductor current to be sinusoidal and to synchronize with the grid voltage, and the inner loop is to control the buck-boost inductor current to balance the input and output powers in the inverter. The inner loop is running in high control bandwidth so that a

precise accurate switching action is resultant. The outer loop operates under a low frequency control which only requires to synchronize the grid current and grid voltage in the line frequency domain. To avoid the interaction in both current loops, the loop frequency is set with a 5 times difference between both loops. The parameter of the controller is set based on the target cut off frequency point.



(a)



(b)

Figure 7-13. Control and modulation, (a) Controller block diagram, and (b) Gate signals.

The gate signals of AVG switches are obtained by a simple polarity detector by sensing the grid voltage. Figure 7-13 (b) shows simplified gate signals for the switches in the proposed Manitoba Inverter topology. It can be seen that there is always only one switch working in HF switching, others operate at line frequency switching and change states at the zero crossing of the grid voltage. Therefore, the semiconductor switching losses can be minimized.

7.5.4 Selection of Filter Component

In every half line cycle, one of the inductors acts as the converter-side inductor for energy conversion. The other one acts as the grid-side inductor to form a *CL* filter with the capacitor C_{AB}. With the use of (7.11) and a predefined current ripple magnitude, the converter inductance is found. In the prototype, a 7.8 mH inductor is to limit the current ripple into 6 A. On the selection of the filter capacitor, there are two major concerns. One is the resonant frequency, f_{res}, which is defined as (7.20).

$$f_{\text{res}} = \frac{1}{2\pi\sqrt{L_{\text{x}} \cdot C_{\text{AB}}}}. \tag{7.20}$$

In order to avoid the interaction between resonant frequency and switching frequency, the resonant frequency is required 10 times lower than the switching frequency. Another criteria is the magnitude of leakage current which is defined in (7.11). In order to meet the standard requirement [7.7], the magnitude of leakage current needs to be within 300 mA. To fulfill both criteria, a 6.8 μF capacitor is selected in the prototype.

7.5.5 Selection of Semiconductor

The switches S_A and S_B for configuring the *CL* filter are implemented by two back-to-back connecting MOSFETs, the main switches S_1 and S_2 are Si MOSFETs, and S_3 and S_4 are IGBTs with antiparallel SiC Diodes. This combination of semiconductors can form fast switching cells to give efficient switching. In order to optimize the design, components losses in the converter are estimated. Reference to [7.7], semiconductor and inductor losses are the key components that require special attention. TABLE 7-III shows the selected semiconductors in the presented prototype. Also, a chart of loss estimation during 130Vdc-600W is given in Figure 7-14 as a design reference.

TABLE 7-III SEMICONDUCTORS IN THE PROTOTYPE

Switch	Type	Manufacturer	Part Number
S_1 ~ S_2	Si MOSFET	Infineon	IPW60R070P6
S_3 ~ S_4	IGBT + SiC Diode	STMicroelectronics	STGW30H60DFB
S_A & S_B	Si MOSFET	Infineon	IPW60R070C6

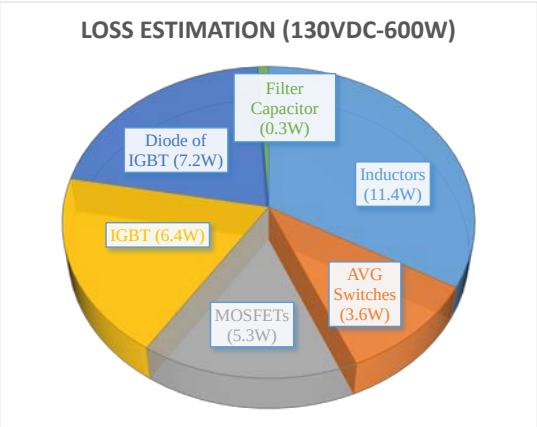
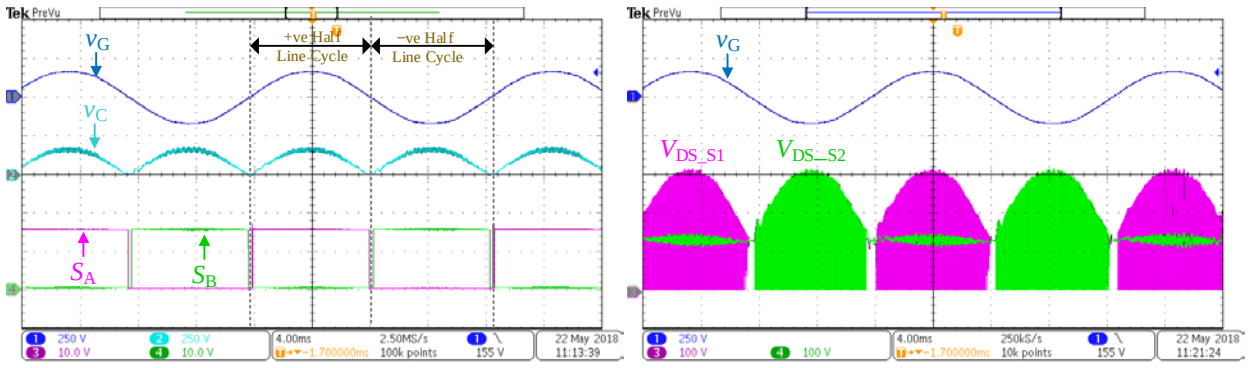


Figure 7-14. Loss estimation in 130Vdc-600W.

7.6 Experiential Verifications

An 800 W buck-boost type inverter prototype has been implemented for the system verification where the system specification is given in TABLE 7-II. The input of the inverter was connecting to a programmable dc source and the output of the inverter was directly connecting to a 120 Vac grid. Figure 7-15 and Figure 7-16 show the experimental results of the proposed buck-boost VSI. The waveforms show the gate signals of S_A and S_B are synchronized with the grid voltage and switching alternately as shown in Figure 7-15 (a). There is a short dead time at the grid voltage zero-crossing to avoid shoot-through issue between S_A and S_B. The capacitor, C_{AB}, voltage is a rectified sinewave, since the polarity of the capacitor is changed in every half line cycle. It can be seen in Figure 7-6 (a) and (b), the capacitor is always connecting to the "Positive Terminal" of the grid. According to the buck-boost characteristic, the voltage stress on S_1 and S_2 are equal to the sum of input and output voltage which is shown in Figure 7-15 (b).

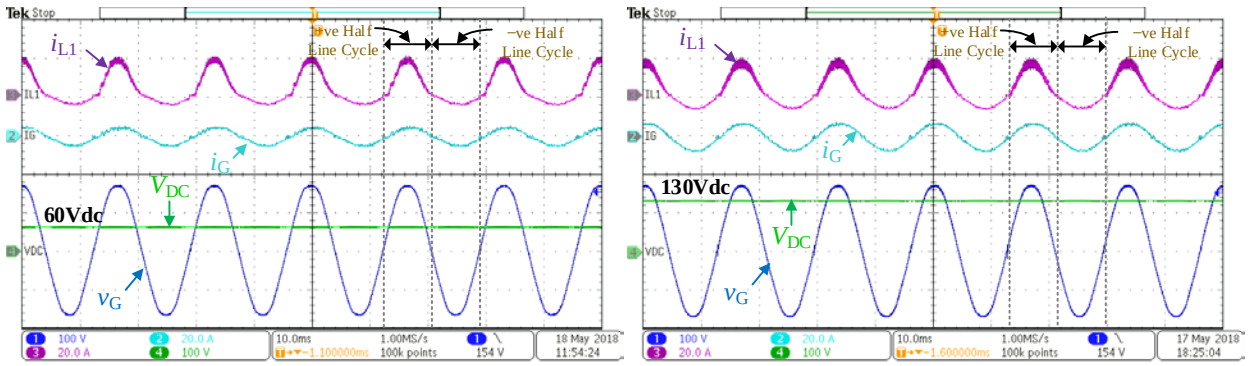


(a) (b)

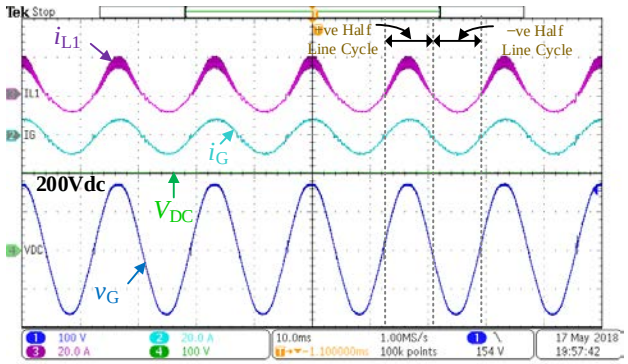
Figure 7-15. Experimental results, (a) gating signals of S_A and S_B and (b) drain to source voltage waveforms of S_1 and S_2 at 130 Vdc input.

Figure 7-16 (a), (b) and (c) show the experimental results of the prototype working with different input dc voltage levels and power levels, they are 60Vdc-400W, 130Vdc-600W, and 200Vdc-800W, respectively. The corresponding current reference of Figure 7-16 (a), (b) and (c)

are 3.3 A, 5 A and 6.6 A, respectively. The maximum inductor current is limited to 20 A. Figure 7-16 (a) shows the VSI prototype is in the buck-boost mode, the input dc voltage is lower than the peak value of grid voltage. The grid current, $i_{G,}$ is controlled as sinusoidal current with small current ripple. The inductor current is an asymmetrical waveform, it is because inductor are changing roles in the positive and negative line cycles which can be seen in Figure 7-6 (a) and (b). During the positive half line cycle, L_1 is the buck-boost inductor, it is charged up energy from the dc source and releases the energy to the capacitor, C_{AB}. Since it is a discontinuous process for the input source and the capacitor, the inductor current amplitude is higher than that of the grid current. During the negative half line cycle, L_1 becomes the grid inductor. Thus, the inductor current waveform of L_1 is identical to the grid current in the negative half line cycle. Figure 7-16 (b) shows similar experimental results, but with higher voltage and higher power values. The grid current can keep as a sinewave. Figure 7-16 (c) shows the VSI prototype is in the buck mode, the input dc voltage is higher than the peak value of grid voltage. The grid current, $i_{G,}$ keeps as sinusoidal current. The inductor current ripple in the positive half line cycle is larger than that in buck-boost mode. This is because the voltage across the inductor is larger, the di/dt of the inductor current is larger as well. Thus, the current ripple becomes larger with the same switching frequency. The experimental results show that the proposed system works well with wide input voltage and ensures high quality grid current output. The results also show the prototype can deliver energy from the dc source to the grid no matter what input voltage level. Moreover, sinusoidal output current is provided. In order to verify the accuracy of the proposed control loop, current references are also extracted from the controller to compare with the measured current waveforms, as shown in Figure 7-17. From the figure, it shows that the measured one and the reference one are synchronized in both frequency and magnitude which results in a stable control.



(a) (b)



(c)

Figure 7-16. Experimental results, (a) 60 Vdc input, (b) 130 Vdc input, and (c) 200 Vdc input.

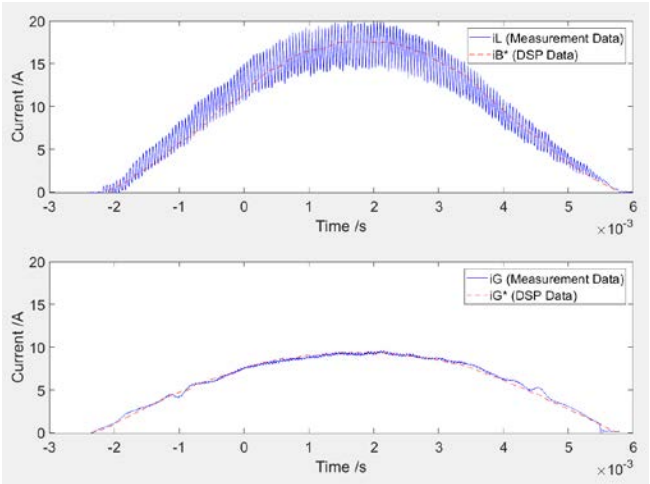


Figure 7-17. Comparison between measurement signals and controller reference signals.

An efficiency curve is provided in Figure 7-18 with various testing conditions. In the measurement, only the converter stage is taken into consideration. The auxiliary power is excluded in the measurement. It demonstrated that the system design is optimized from the medium voltage to high voltage scale, (130 Vdc to 200 Vdc). At the full loading condition of 130 Vdc, 93.7 % system efficiency was achieved. The power factor was kept higher than 0.98. The voltage harmonic was 1.31 % and the current harmonic was 4.71 %. During 20 % loading condition of 200 Vdc, the efficiency can be up to 95.7 %. In addition, at the full loading condition of 200 Vdc, 93.82 % system efficiency was able to achieve. The power factor was also kept higher than 0.98. The corresponding voltage harmonic was 1.34 % and the corresponding current harmonic was 4 %. The highest system efficiency for the prototype was 95.7 % which appeared in 20 % loading condition. A details current harmonic spectrum of the system operating in the buck-boost mode (130 Vdc) and the buck mode (200 Vdc) are shown in Figure 7-19 (a) and (b) respectively. In all cases, the current quality satisfies the IEEE 519 standard.

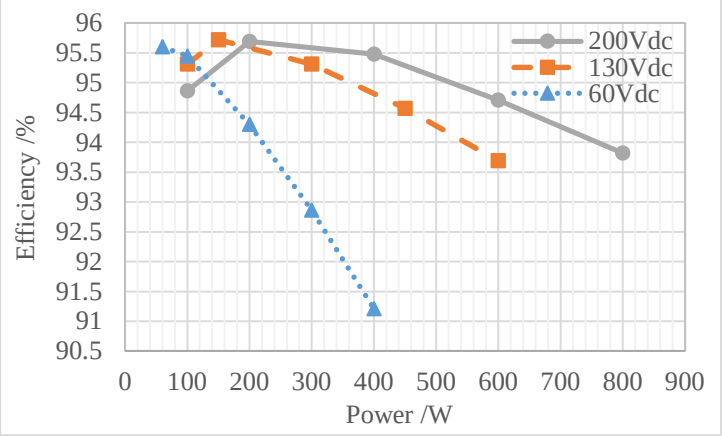
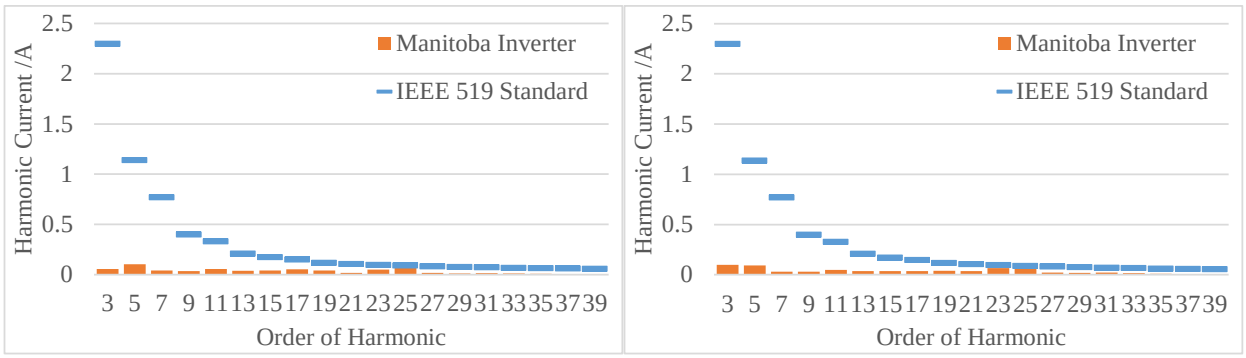


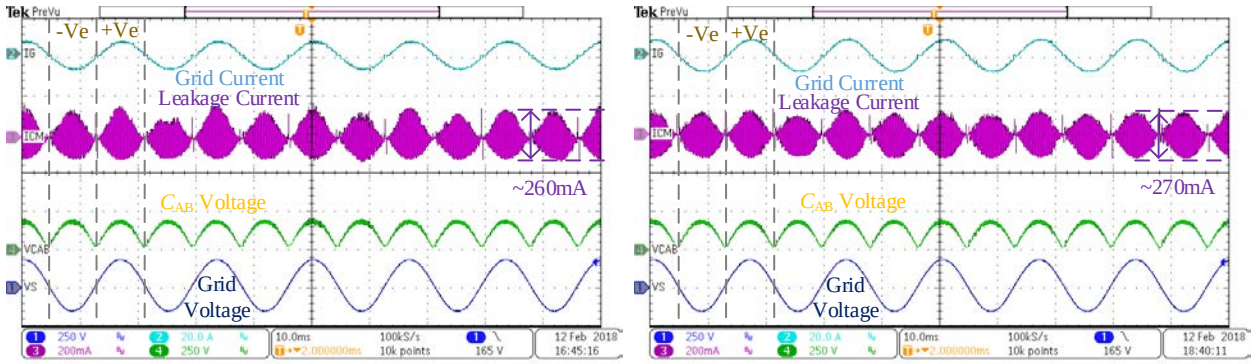
Figure 7-18. System efficiency graph.



(a) (b)

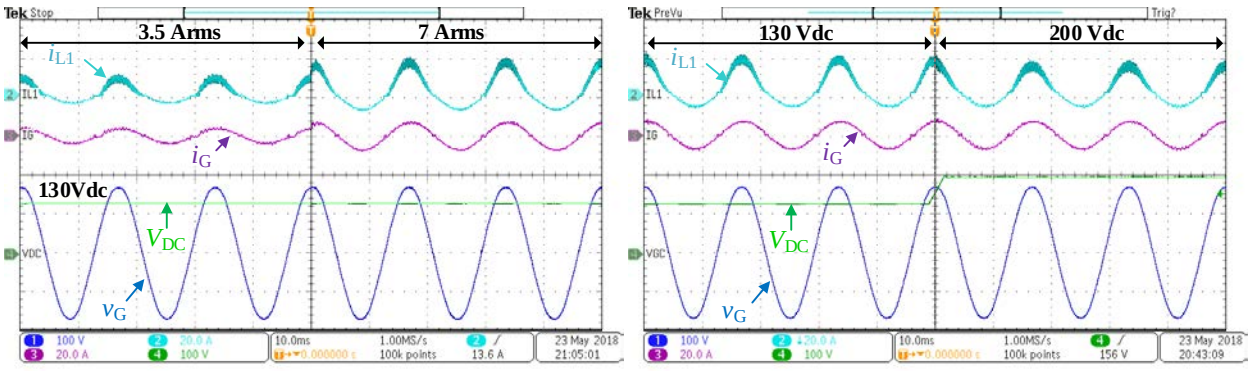
Figure 7-19. Current Harmonic spectrums, (a) 130 Vdc input and (2) 200 Vdc input.

Figure 7-20 (a) and (b) show the leakage current measurement of the inverter under the full loading condition in the 130 Vdc and 200 Vdc. A 100 nF capacitor is added to the testbed to simulate the parasitic capacitor C_{CM} of the inverter. In both cases, the leakage current levels were also close to the expected value and were within the standard requirement of 300 mA [7.7]. Low CM voltage and low leakage current are able to be guaranteed by the proposed topology.



(a) (b)

Figure 7-20. Leakage current measurements, (a) 130 Vdc input and (2) 200 Vdc input.



(a) (b)

Figure 7-21. Transient waveforms, (a) step change in grid current reference and (a) step change in input voltage.

Figure 7-21 (a) and (b) show the transient performance of the proposed inverter under different testing conditions. In Figure 7-21 (a), the reference of grid current was changed from 3.5 A to 7 A with a smooth transient action. Afterward, grid current was quickly settled into a new targeting value under the proposed control scheme. In Figure 7-21 (b), the input voltage was jumped from 130 Vdc to 200 Vdc. Grid current wasn't influenced during the transient action. The only variation was shown in inductor current as it related to input voltage magnitude. In both situations, the system can keep stable and provide a fast dynamic response during the transient period. A stable system is able to be guaranteed.

7.7 Conclusion

The chapter presented a new transformerless single-phase single-stage buck-boost grid-connected VSI topology. The VSI guaranteed the performance with small grid current ripple, low leakage current, a wide input voltage range, no additional grid inductor, and only one HF switch operates in the process. The concept is to use a low frequency switching circuit to reconfigure the

CL filter in positive and negative half line cycles. Since the filtering capacitor always connects between the dc link and one of the grid terminals, the HF common mode voltage is minimized. The switching states of the proposed topology were explained in detail. The performance of the VSI was demonstrated by experimental results. It showed that there is a good agreement between the concept and the experimental results.

Reference

[7.1] C. N. M. Ho and K. K. M. Siu, “Manitoba Inverter - Single Phase Single-Stage Buck-Boost VSI Topology,” in *Proc. IEEE ECCE17*, pp. 4576-4581, Oct. 2017.

[7.2] C. G. C. Branco, C. M. T. Cruz, R. P. Torrico-Bascope, and F. L. M. Antunes, “A Nonisolated Single-Phase UPS Topology With 110-V/220-V Input–Output Voltage Ratings,” *IEEE Trans. Ind. Electron.*, vol. 55, no. 8, pp. 2974-2983, Aug. 2008.

[7.3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292-1306, Sept.-Oct. 2005.

[7.4] D. Han, C. T. Morris, and B. Sarlioglu, “Common-Mode Voltage Cancellation in PWM Motor Drives With Balanced Inverter Topology,” *IEEE Trans. Ind Electron.*, vol. 64, no. 4, pp. 2683-2688, April 2017.

[7.5] C. N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, L. A. Serpa, and A. Coccia, “Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2835-2845, June 2012.

[7.6] C. N. M. Ho, H. Breuninger, S. Pettersson, G. Escobar, and F. Canales, “A Comparative Performance Study of an Interleaved Boost Converter Using Commercial Si and SiC Diodes for PV Applications,” *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 289-299, Jan. 2013.

[7.7] *Safety of Power Converters for Use in Photovoltaic Power Systems—Part 1*: General Requirement, IEC Standard 62109-1-2007, 2007.

[7.8] *Effects of current on human beings and livestock – Part 1*: General Aspects, IEC Standard 60479-1-2005, 2005.

[7.9] M. Victor el at, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage," *US Patent*, No. US7411802 B2, 12/08/2008.

[7.10] H. Schmidt *el at*, "DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current," *US Patent*, No. US7046534 B2, 16/05/2006.

[7.11] R. T. H, Li, C. N. M. Ho, and E. X. Chen, "Active Virtual Ground – Single Phase Transformerless Grid-Connected Voltage Source Inverter Topology," *IEEE Trans. Power Electron.*, vol. 33, no. 2, pp. 1335-1346, Feb. 2018.

[7.12] K. Ogura, T. Nishida, E. Hiraki, M. Nakaoka, and S. Nagai, "Time-sharing Boost Chopper Cascaded Dual Mode Single-phase Sinewave Inverter for Solar Photovoltaic Power Generation System," in *Proc. IEEE PESC2004*, pp. 4763-4767, Jun. 2004.

[7.13] W. Wu and T. Tang, "Dual-Mode Time-Sharing Cascaded Sinusoidal Inverter," *IEEE Trans. Energy Convers.*, vol. 22, pp. 795-797, Sept. 2007.

[7.14] F. Kang, C. Kim, S. Park, and H. Park, "Interface circuit for photovoltaic system based on buck-boost current-source PWM inverter," in *Proc. IEEE IECON2002*, pp. 3257-3261, Nov. 2002.

[7.15] Ahmed Mohamed Salamah, Stephen J. Finney, and Barry W. Williams, "Single-Phase Voltage Source Inverter With a Bidirectional Buck–Boost Stage for Harmonic Injection and Distributed Generation," *IEEE Trans. Power Electron.*, vol. 24, pp. 376-387, Feb. 2009.

[7.16] C.-M. Wang, “A novel single-stage full-bridge buck-boost inverter,” *IEEE Trans. Power Electron.*, vol. 19, no. 1, pp. 150-159, Jan. 2004.

[7.17] R. O. Caceres and I. Barbi, “A boost DC-AC converter: analysis, design, and experimentation,” *IEEE Trans. Power Electron.*, vol. 14, no. 1, pp. 134-141, Jan. 1999.

[7.18] S. Jain and V. Agarwal, “A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking,” *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928-1940, Sept. 2007.

[7.19] D. Meneses, F. Blaabjerg, Ó. García and J. A. Cobos, “Review and Comparison of Step-Up Transformerless Topologies for Photovoltaic AC-Module Application,” *IEEE Trans. Power Electron.*, vol. 28, no. 6, pp. 2649-2663, June 2013.

[7.20] C. N. M. Ho, R. T. H. Li, and K. K. M. Siu, “Active Virtual Ground—Bridgeless PFC Topology,” *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 6206-6218, Aug. 2017.

Chapter 8 System Model and Performance Evaluation of Single-Stage Buck-Boost Type Manitoba Inverter for PV Applications

The work described in this chapter was published in the following paper: K. K. M. Siu and C. N. M. Ho, "System Model and Performance Evaluation of Single-Stage Buck-Boost Type Manitoba Inverter for PV Applications" *IEEE J. Emerg. Sel. Topics Power Electron.*, submitted and under review. The work was also presented in part as a conference paper at the IEEE Energy Conversion Congress and Exposition 2018 [8.1].

8.1 Abstract

The chapter presents a control methodology for a recently proposed single-stage buck-boost type inverter in photovoltaic (PV) applications. A wide range of input voltage is covered and the dc power is effectively converted into the grid power within a single-stage system. However, from the topological characteristics, a *CL* filter is always formed at the system output which results in a resonance pole in the control system. In the PV system, the panel output voltage keeps varying. Under the traditional control method, stability issues may occur, which poses a challenge to controller design. Thus, targeting on PV applications, a comprehensive control methodology is presented in this chapter. Under such control scheme, a high quality ac grid power is guaranteed and the power conversion maintains in a stable manner. Meanwhile, the maximum power point (MPP) of PV panels is always tracked and no additional current sensor is required in the maximum power point tracking (MPPT) design. In this chapter, a detailed system analysis is presented which includes the system modelling and the stability evaluation. Performance of the presented control

methodology is experimentally verified in a 750 W PV inverter platform. Both steady state and dynamic characteristics are in good agreement with the theoretical knowledge.

8.2 Introduction

Recently, solar energy has become one of the important renewable energy sources in the world which is environmentally friendly and is replenished constantly in nature. With the use of photovoltaic (PV) inverters [8.2], [8.3], solar power is able to be effectively transferred from the PV panels to the power grid. The generated power is used to support the power demand in those localized areas, such as residential usages, solar farms and industrial applications. Generally, the basic requirements for PV inverters are to achieve highly efficient power conversion, low design cost, and low leakage current. Thus, in order to simplify the structure of the two-stage system and to achieve an efficient power transmission, many single-stage PV inverter solutions, [8.4] - [8.7], have recently been proposed.

A buck-boost type transformerless inverter is proposed in [8.7], in which the low voltage dc power is able to be converted into ac grid power within a single-stage system. The topology is named as Manitoba Inverter and is shown in Figure 8-1. Based on the topology characteristic, a *CL* filter is always formed at the inverter output which is similar to other buck-boost type inverters connected to an external *CL* filter. A continuous grid current is guaranteed and the system leakage current is minimized. However, a phase shift property and a resonance characteristic have been generated. In PV applications, the panel output remains varied under different environmental conditions and even transients step occurs. Therefore, the resonance characteristic has generated a great influence on system stability, which makes the design of the system control to become more challenging. To maintain stable performance of a PV inverter system, varying types of

methodologies were presented in the past. In [8.8], simple PI control is applied. In the control scheme, both input and output voltage information are always required to calibrate the difference between the buck-boost inductor current and the output current. Therefore, the accuracy of the control is highly dependent on the system parameters. In [8.9], the control method is based on an averaged continuous-time model and a feedforward compensation. In fact, the compensation circuit helps to eliminate the influence of both input and output voltages and allows the system to be more robust. However, when the system output filter is modified to a *CL* filter, a more complicated average model is resultant. In [8.10] and [11], one cycle control is adopted into the single-state buck-boost type inverter to offer a fast dynamic system response. The control structure is simple and no PLL is required, but the possible filter resonance issue cannot be compensated in the control and cause stability problem. In [8.12] and [8.13], sliding mode control is applied to PV inverter which is another type of non-linear control method. Stable performance and good dynamic response can be obtained. The determination of the sliding surface is based on the state equation of the inverter. Thus, when the output filter order is higher, the calculation of the switching criteria becomes more complicated.

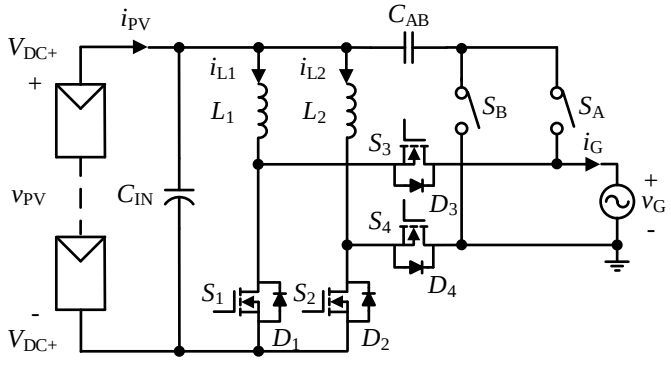


Figure 8-1. Single stage buck-boost inverter.

A comprehensive control scheme is proposed in this chapter to fulfill the high quality grid

current and the system stability requirements in a single-stage buck-boost type PV inverter. In contrast to [8.7], the proposed control scheme is focused on PV applications and is used to transfer the maximum PV power into the grid power within a single-stage buck-boost type transformerless converter. In the proposed control structure and modulation, a precise switching action and a high quality grid current waveform are guaranteed by the current control in the middle loop and the inner loop. Focusing on PV applications, an active damping circuit, [8.14], is integrated into the system inner loop with the use of the high frequency (HF) capacitor voltage ripple. The filter resonant pole is erased and the resultant system is able to adopt all the possible voltage inputs. The outer loop is targeted on input voltage which is applied to lock the maximum power point (MPP) voltage of the PV panel. A perturb and observe (P&O) method is adopted in the system outer loop and offers the maximum power point tracking (MPPT) [8.15], [8.16] function. In the implementation, the system output power is applied to the MPPT as a power reference, thus, no additional current sensor is required. Focusing on PV applications, both dynamic and steady state characteristics are determined and are applied to optimize the control system design. A 750 W inverter platform has been implemented to verify the control theory. All the time, the MPP was tracked and stable performance was guaranteed in both steady state and dynamic situations. All of the experimental results and the detailed findings were consistent with the theoretical analysis.

8.3 System Configuration

8.3.1 Review of Manitoba Inverter

Manitoba inverter is a single-stage buck-boost type inverter system which is in a simple circuit structure. Every half line cycle, the operation of the inverter is able to be converted back to a simple buck-boost type converter circuit. The corresponding modulation scheme of Manitoba Inverter is

documented in [8.7] and is shown in Figure 8-2. Accordingly, the equivalent circuits of the inverter connecting to a PV array in the positive and negative half line cycles are found and are shown in Figure 8-3 (a) and (b), respectively.

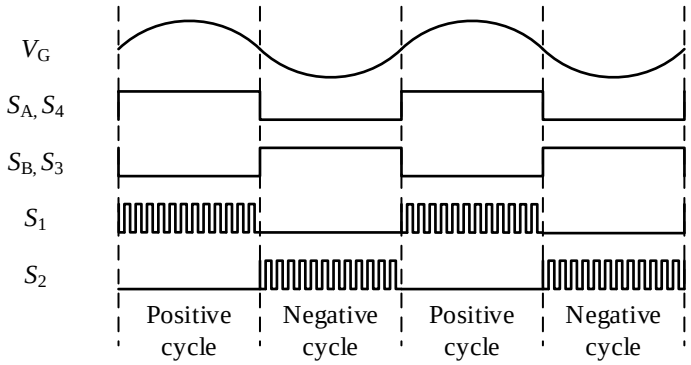
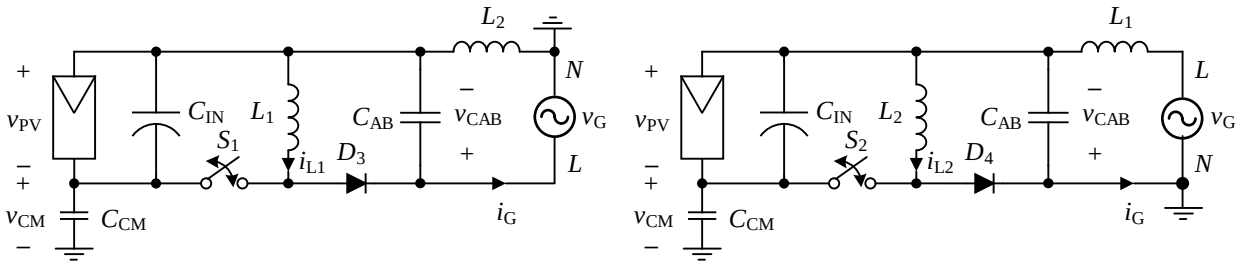


Figure 8-2. Gate signals sequence of the buck-boost inverter.



(a) (b)

Figure 8-3. Equivalent circuits of (a) positive and (b) negative half line cycles.

In each half line cycle, there is only one semiconductor is operated at HF switching and the others are in line frequency (LF) operation. During the power conversion, only two semiconductors are involved in the main current path. Thus, an efficient energy conversion is resultant. From the inverter topology, a reconfigurable *CL* filter is always located at the inverter output side. One of the inductors acts as the grid-side filter inductor and the other one acts as the converter-side power inductor. The roles of the inductor are interchanged in every half line cycle. The *CL* filter is formed by the grid-side inductor and a filter capacitor C_{AB}. Accordingly, in the buck-boost circuit, the

discontinuous output current is filtered out and a low noise continuous grid current, i_G, is guaranteed. Moreover, the filter capacitor helps to claim the voltage ripple between the positive PV terminal and one end of the grid terminal. Thus, the system common mode voltage noise is minimized. Consequently, a low noise system is guaranteed which has been reported in [8.7].

During the positive half line cycle, the buck-boost switching cell is formed by the switch S_1, the antiparallel diode D_3 and the inductor L_1. S_1 is the only HF switch at this cycle. Switches S_4 and S_A are in LF operation. Both of them are kept ON at this state. S_4 is used to generate a current return path for the circuit and S_A is used to link up the connection between the filter capacitor and the Line terminal of the grid. L_2 inductor acts as the grid-side filter inductor and L_1 acts as the converter-side power inductor. An output *CL* filter is formed by C_{AB} and L_2.

Similarly, during the negative half line cycle, the buck-boost switching cell is formed by the switch S_2, the antiparallel diode D_4 and the inductor L_2. S_2 is the only HF switch at this cycle. Switches S_3 and S_B are in LF operation. Both of them are kept ON at this state. S_3 is used to generate a current return path for the circuit and S_B is used to link up the connection between the filter capacitor and the Neutral terminal of the grid. L_1 inductor acts as the grid-side filter inductor and L_2 acts as the converter-side power inductor. An output *CL* filter is formed by C_{AB} and L_1.

8.3.2 Proposed Control Methodology

Targeted on a single-stage buck-boost type PV inverter system, a comprehensive control is proposed. A block diagram of the corresponding control method is shown in Figure 8-4. In the design, the outer loop is a PV voltage control loop that is integrated with an MPPT controller. So that the inverter input is always regulated to the MPP. The middle one is a grid-side current control which is applied to maintain the quality of the inverter output current. The inner one is an inductor-

side current control plus an active damping circuit. It is used to handle the power conversion on the system. On the controller implementation, a set of voltage sensors is applied to the system which is used to sense the PV output voltage, v_{PV}, the grid voltage, v_G, and the filter capacitor voltage, v_C. In addition, a set of current sensors is required which is used to sense the inductor currents, i_{L1} and i_{L2}.

In the outer loop, it is a PV output voltage control which is combined by a simple proportional integral (PI) control and an MPPT method. The control reference in the outer loop is generated from the MPPT function. A P&O method is adopted in the design where the inverter output power and PV voltage are used to track the MPP from the non-linear characteristic of the PV panel. A small voltage step is given in every tracking process. If the increment of the average power is in the same direction as the given voltage step, then another voltage step is given until the power level falls or remains stable. As the inverter output power is applied to the MPPT block, no extra current sensor is required on the system design. The corresponding program flow is shown in Fig. 5. Based on the reference voltage from the P&O, a simple PI control is applied to regulate the inverter input to the MPP. Thus, all the time, the maximum power is extracted from the PV panel and the inverter system is kept with a stable input. The output of the voltage control is a grid-side current reference, $i_{G,ref}$, which is the input of the middle loop of the system.

In the middle and the inner loops of the system, a double current control method is applied where both grid-side and converter-side inductor currents are under controlled. The grid-side inductor current is controlled through the middle loop and the converter-side inductor current is controlled by the inner loop. The grid-side and converter-side current information are able to be generated from the two inductor current sensors. The roles of both inductors are interchanged in every half line cycle. Therefore, by combining the positive cycle current information in i_{L2} and the negative cycle current information in i_{L1}, the grid-side current information is generated. Similarly,

through the current information in i_{L1} and the negative cycle current information in i_{L2}, the converter-side current information is generated. The middle loop is a grid-side current control which is implemented by a PI control. It is used to compensate the phase shift generated by the *CL* filter and to control the power factor of the system output close to one. Thus, a high quality output waveform is resultant. The output of the middle loop is a converter-side inductor current reference, $i_{L,ref}$, which is the input of the inner loop.

The inner loop is a converter-side inductor current control which is used to offer a precise switching action for the inverter and to avoid the filter resonance in the system. Based on the system operation, a resonant pole is generated by the *CL* filter. In a general fixed input voltage design, the stability issue that generated from the resonant pole can be avoided through a careful design in the system control bandwidth. However, in a PV system, the panel output is nonlinear and the system condition is always varying with time. Thus, system stability becomes challenging to ensure. In the design, an active damping circuit is integrated into the PI current control loop where the capacitor ripple voltage is applied as a damping factor [8.14]. Accordingly, its performance is similar to a resistor virtually series connecting to the converter-side inductor. The output of the converter-side inductor current control loop is a duty cycle reference, u_{ref}. Through the comparison with the sawtooth signal, the control signal of the HF switch is generated. Consistently, only one switch is under HF operation and the others are in LF operation. The whole controller design is maintained in a simple structure.

In the reconfigurable filter circuit, the switching action of S_A and S_B are controlled by a polarity detection circuit. By sensing the signal of v_G, S_A and S_B are switched alternatively and are synchronized with the LF operation. In the positive half line cycle, S_A is conducted and S_B is off. In contrast, on the negative half line cycle, the switching action is opposite. Thus, during the system operation, a *CL* filter is always formed at the inverter output. At the same time, the grid current

remains continuous and has a low current ripple on top.

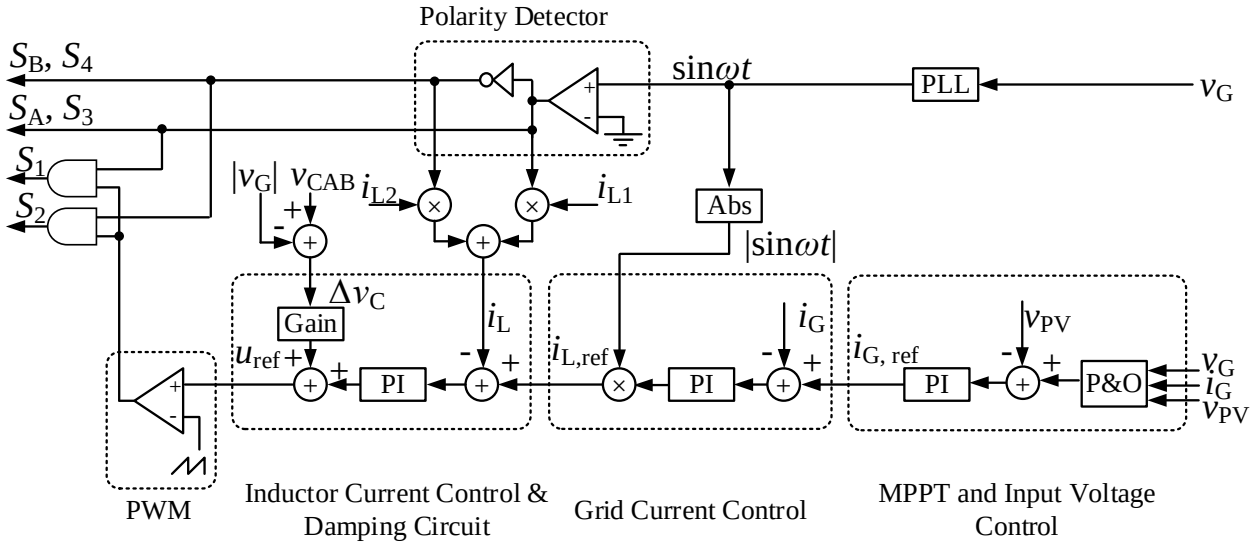


Figure 8-4. Block diagram of the presented control methodology.

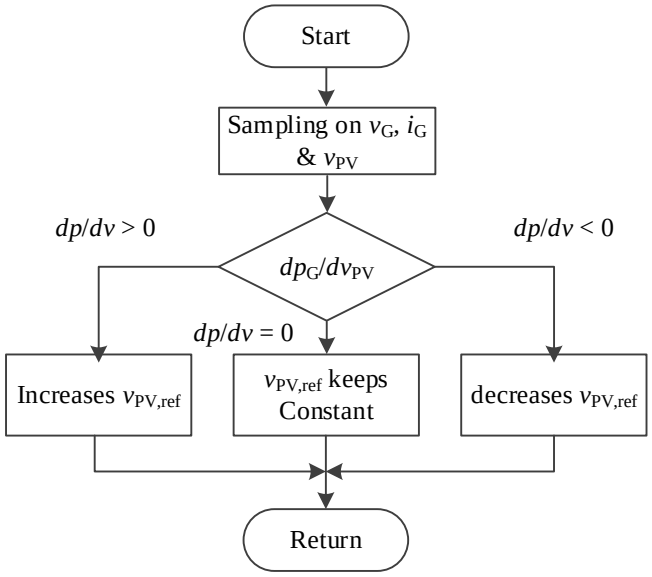


Figure 8-5. Logic flow of P&O control block.

8.4 System Modelling

8.4.1 Review of PV Panel Model

The overall system model can be separated into two parts, which are the modelling of the PV panel and the modelling of the inverter system. Referring to [8.17], a single diode equivalent circuit is applied to simulate the performance of a PV panel. The characteristic of PV panel is modelled as,

$$I_{\mathrm{PV}} = I_{\mathrm{ph}} - I_0 \cdot \left(e^{\frac{V_{\mathrm{PV}} + I_{\mathrm{PV}} \cdot R_{\mathrm{S}}}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}}} - 1 \right) - \frac{V_{\mathrm{PV}} + I_{\mathrm{PV}} \cdot R_{\mathrm{S}}}{R_{\mathrm{SH}}}, \tag{8.1}$$

where I_{PV} is current of panel output, I_{ph} is photogenerated current, I_0 is diode saturation current, N_{s} is number of series cell, R_{SH} is the shunt resistance in the PV model, R_{S} is the series resistance in the PV model and V_{T} is temperature coefficient.

From (1), it shows that the PV panel output characteristic is in a non-linear behavior where the I-V characteristic is varying under different conditions. The panel parameter is depended on sun radiation and environment temperature. Moreover, the system power is varying and the location of the MP is also located. In order to solve I_{PV} directly from (8.1), Lambert function is applied and (8.1) is reformulated to,

$$I_{\mathrm{PV}} = \frac{R_{\mathrm{TH}}}{R_{\mathrm{S}}} \cdot \left(I_{\mathrm{TH}} - \frac{V_{\mathrm{PV}}}{R_{\mathrm{SH}}} \right) - \frac{N_{\mathrm{S}} \cdot V_{\mathrm{T}}}{R_{\mathrm{S}}} \cdot W\left(\frac{I_0 \cdot R_{\mathrm{TH}}}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}} \cdot e^{\frac{1}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}} \left[V_{\mathrm{PV}} \cdot \left(1 - \frac{R_{\mathrm{TH}}}{R_{\mathrm{SH}}} \right) + I_{\mathrm{TH}} \cdot R_{\mathrm{TH}} \right]} \right), \tag{8.2}$$

where I_{TH} equals $I_{\mathrm{ph}} + I_0$ and R_{TH} equals $\frac{R_{\mathrm{SH}} \cdot R_{\mathrm{S}}}{R_{\mathrm{SH}} + R_{\mathrm{S}}}$.

Reference to the PV simulator characteristic, by using the open circuit, short circuit and the MPP condition, the required series and shunt resistances are available to be determined through Lambert function [8.18]. In the model, the equivalent series resistance is 0.81 ohms and the

equivalent shunt resistance is calculated as 410 ohms. By inputting all the model parameters and a PV voltage condition into (8.2), a corresponding PV current is obtained. The characteristic of the equivalent model is shown in Figure 8-6 with red color dotted line. The modelling characteristic is close to the simulator output.

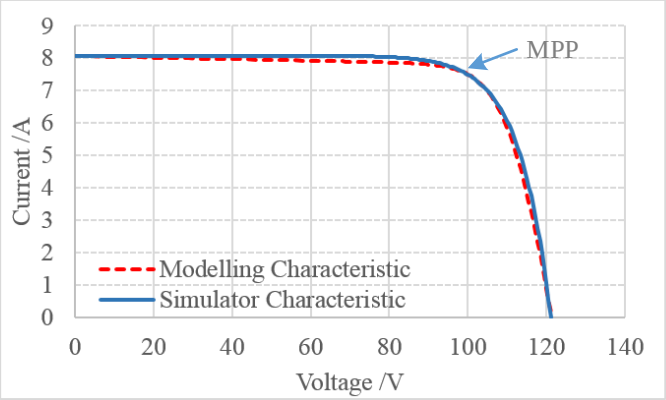


Figure 8-6. PV panel characteristic.

8.4.2 Inverter System Model

The applied inverter is a single stage system. It has a symmetrical system structure in the positive and the negative half line cycles. Thus, with the use of positive half line cycle information is sufficient to develop the whole converter system model. In the positive line cycle, L_2 acts as a grid-side inductor which handles the grid current, i_G. In addition, L_1 becomes the converter-side inductor and the current flowing on top is defined as i_L. In the design, all the inductors are set to the same value. Such that L_1 is equal to L_2 and is grouped as L_X.

As shown in Figure 8-3 (a), when S_1 is ON, the converter-side inductor is charging. When S_2 is OFF, the energy in the converter-side inductor is transferred to the grid. By combining the on-state and the off-state system conditions, a set of state-space averaging equations is formed and is shown as,

$$\frac{d}{dt}\begin{bmatrix} i_{\mathrm{L}} \\ i_{\mathrm{G}} \\ v_{\mathrm{pv}} \\ v_{\mathrm{CAB}} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \frac{D}{L_{\mathrm{X}}} & -\frac{1-D}{L_{\mathrm{X}}} \\ 0 & 0 & 0 & \frac{1}{L_{\mathrm{X}}} \\ -\frac{D}{C_{\mathrm{IN}}} & 0 & 0 & 0 \\ \frac{1-D}{C_{\mathrm{AB}}} & -\frac{1}{C_{\mathrm{AB}}} & 0 & 0 \end{bmatrix} \begin{bmatrix} i_{\mathrm{L}} \\ i_{\mathrm{G}} \\ v_{\mathrm{pv}} \\ v_{\mathrm{CAB}} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{v_{\mathrm{G}}}{L_{\mathrm{X}}} \\ \frac{i_{\mathrm{pv}}}{C_{\mathrm{IN}}} \\ 0 \end{bmatrix}, \tag{8.3}$$

where D is duty cycle of the system.

8.4.3 System Small Signal model

In the system stability evaluation, the small signal analysis method is applied. From Figure 8-4, a corresponding small signal model of the system is determined and is given in Figure 8-7.

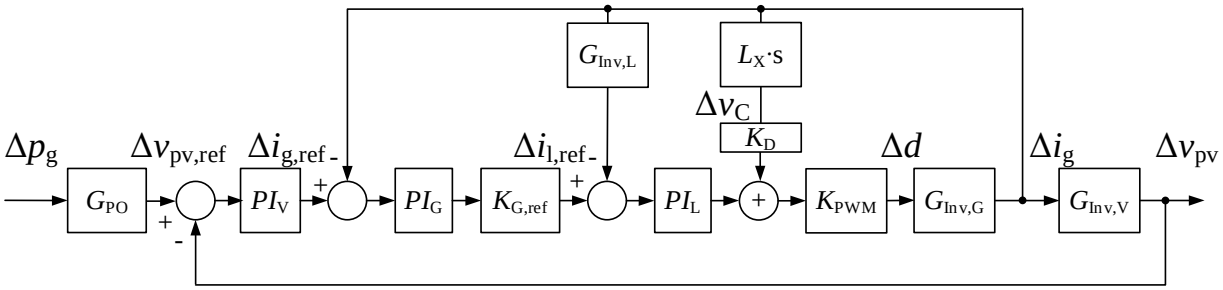


Figure 8-7. Controller small signal flow diagram.

From the PV panel portion, by considering $\Delta v_{\mathrm{pv}}(t)$ and $\Delta i_{\mathrm{pv}}(t)$ as the small-signal perturbations of v_{pv} and i_{pv} in the small signal analysis model, (8.1) is rearranged. Through small signal approximation method, [8.19], the small-signal perturbation equation of the PV characteristic is found as,

$$\Delta i_{\mathrm{pv}} = -\frac{\frac{I_0}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}} \cdot e^{\frac{V_{\mathrm{PV}} + I_{\mathrm{PV}} \cdot R_{\mathrm{S}}}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}}}}{1 + \frac{R_{\mathrm{S}}}{R_{\mathrm{SH}}} + \frac{I_0 \cdot R_{\mathrm{S}}}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}} \cdot e^{\frac{V_{\mathrm{PV}} + I_{\mathrm{PV}} \cdot R_{\mathrm{S}}}{N_{\mathrm{S}} \cdot V_{\mathrm{T}}}}} \cdot \Delta v_{\mathrm{pv}} = -X_{\mathrm{PV}} \cdot \Delta v_{\mathrm{pv}}, \tag{8.4}$$

where X_{PV} is defined as $\frac{\frac{I_0}{N_S \cdot V_T} \cdot e^{\frac{V_{\mathrm{PV}}+I_{\mathrm{PV}} \cdot R_S}{N_S \cdot V_T}}}{1+\frac{R_S}{R_{SH}}+\frac{I_0 \cdot R_S}{N_S \cdot V_T} \cdot e^{\frac{V_{\mathrm{PV}}+I_{\mathrm{PV}} \cdot R_S}{N_S \cdot V_T}}}$.

As shown in (8.2), Δv_{pv} is directly proportional to Δi_{pv} which is matched with the PV characteristic curve.

From the inverter system portion, by considering $\Delta v_{\mathrm{CAB}}(t)$, $\Delta v_{\mathrm{pv}}(t)$, $\Delta i_l(t)$, $\Delta i_{\mathrm{g}}(t)$ and Δd as the small-signal perturbations of v_{CAB}, v_{pv}, i_{L}, i_{G} and D respectively in the small signal analysis model, (3) is able to be rearranged into a set of small-signal perturbations equations, (8.5) – (8.8), as,

$$L_{\mathrm{X}} \cdot s \cdot \Delta i_l = (V_{\mathrm{PV}} + V_{\mathrm{CAB}}) \cdot \Delta d + D \cdot \Delta v_{\mathrm{pv}} - D' \cdot \Delta v_{\mathrm{CAB}}, \tag{8.5}$$

$$L_{\mathrm{X}} \cdot \mathrm{s} \cdot \Delta i_{\mathrm{g}} = \Delta v_{\mathrm{CAB}}, \tag{8.6}$$

$$C_{\mathrm{IN}} \cdot \mathrm{s} \cdot \Delta v_{\mathrm{pv}} = -X_{\mathrm{PV}} \cdot \Delta v_{\mathrm{pv}} - i_{\mathrm{L}} \cdot \Delta d - D \cdot \Delta i_{\mathrm{l}}, \tag{8.7}$$

$$C_{\mathrm{AB}} \cdot \mathrm{s} \cdot \Delta v_{\mathrm{CAB}} = D' \cdot \Delta i_l - i_{\mathrm{L}} \cdot \Delta d - \Delta i_{\mathrm{g}}, \tag{8.8}$$

where $D' = 1 - D$.

From (8.4), (8.5) – (8.8), the relationship of the inverter is able to found. In the derivation, the influence of Δi_{pv} can be eliminated as the scale of X_{PV} is relatively small compared to other parameters. The converter models are developed as,

$$G_{\mathrm{inv,L}}(s) = \frac{\Delta i_{\mathrm{l}}}{\Delta i_{\mathrm{g}}} = \frac{C_{\mathrm{AB}} \cdot C_{\mathrm{IN}} \cdot L_2 \cdot V_{\mathrm{X}} \cdot s^3 + L_{\mathrm{X}} \cdot (I_{\mathrm{G}} \cdot C_{\mathrm{IN}} - I_{\mathrm{PV}} \cdot C_{\mathrm{AB}}) s^2 + V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot s - I_{\mathrm{PV}}}{-C_{\mathrm{IN}} \cdot L_2 \cdot I_{\mathrm{PV}}/D \cdot s^2 + V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot D' \cdot s - I_{\mathrm{PV}}}, \tag{8.9}$$

$$G_{\mathrm{inv,G}}(s) = \frac{\Delta i_{\mathrm{g}}}{\Delta d} = \frac{-C_{\mathrm{IN}} \cdot L_2 \cdot I_{\mathrm{PV}}/D \cdot s^2 + V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot D' \cdot s - I_{\mathrm{PV}}}{C_{\mathrm{AB}} \cdot C_{\mathrm{IN}} \cdot {L_{\mathrm{x}}}^2 \cdot s^4 + L_{\mathrm{X}} \cdot (C_{\mathrm{IN}} + D^2 \cdot C_{\mathrm{AB}} + D'^2 \cdot C_{\mathrm{IN}}) s^2 + D^2}, \tag{8.10}$$

where V_{X} equals to the sum of dc and ac voltage.

As shown in (8.9) and (8.10), since the presence of a filter capacitor and a grid-side inductor,

more pole and zero are added into the system. A resonant point is induced and it makes the controller design to be challenging.

In the proposed control methodology, an active damping is inserted into the system inner loop. The capacitor ripple voltage is applied as the damping factor. In the inner loop, considering the effect of the damping system, the relationship between the duty ratio and the converter-side inductor current, $G_{\mathrm{inv,D}}$, is found as,

$$G_{\mathrm{inv,D}}(s) = \frac{\Delta i_{\mathrm{l}}}{\Delta d} = \frac{G_{\mathrm{inv,L}}(s) \cdot G_{\mathrm{inv,G}}(s)}{1 - K_{\mathrm{D}}.K_{\mathrm{PWM}}.L_{\mathrm{X}}.s.G_{\mathrm{inv,G}}(s)}, \tag{8.11}$$

which is rearranged to,

$$G_{\mathrm{inv,D}}(s) = \frac{C_{\mathrm{AB}} \cdot C_{\mathrm{IN}} \cdot L_{\mathrm{X}} \cdot V_{\mathrm{X}} \cdot s^3 + L_{\mathrm{X}} \cdot (I_{\mathrm{G}} \cdot C_{\mathrm{IN}} - I_{\mathrm{PV}} \cdot C_{\mathrm{AB}}) s^2 + V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot s - I_{\mathrm{PV}}}{\left(C_{\mathrm{AB}} \cdot C_{\mathrm{IN}} \cdot {L_{\mathrm{x}}}^2 \cdot s^4 + L_{\mathrm{X}} \cdot (C_{\mathrm{IN}} + D^2 \cdot C_{\mathrm{AB}} + D'^2 \cdot C_{\mathrm{IN}}) s^2 + D^2\right) + K_{\mathrm{D}}.K_{\mathrm{PWM}}.L_{\mathrm{X}}.s.(C_{\mathrm{IN}} \cdot L_2 \cdot \frac{I_{\mathrm{PV}}}{D} \cdot s^2 - V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot D' \cdot s + I_{\mathrm{PV}})}. \tag{8.12}$$

From (8.12), it shows that the effect of the active damping circuit is concentrated on the denominator of the transfer function. With the help of the active damping circuit, the influence from the resonance characteristic is eliminated. Through the Routh-Hurwitz stability criterion, the range of the damping ratio, K_{D}, is given as,

$$0 < K_{\mathrm{D}} < \frac{(1 + D'^2) \cdot C_{\mathrm{IN}} + D^2 \cdot C_{\mathrm{AB}}}{K_{\mathrm{PWM}}.V_{\mathrm{X}} \cdot C_{\mathrm{IN}} \cdot D'}. \tag{8.13}$$

For the overall transfer function of the system inner loop is calculated as,

$$G_{\mathrm{inner}}(s) = K_{\mathrm{PWM}}.\, G_{\mathrm{inv,D}}(s).\, PI_{\mathrm{L}}(s). \tag{8.14}$$

Accordingly, the overall transfer function of the system middle loop is formed as,

$$G_{\mathrm{middle}}(s) = \frac{G_{\mathrm{inner}}(s)}{G_{\mathrm{inv,L}}(s) \cdot (1 + G_{\mathrm{inner}}(s))} \cdot K_{\mathrm{G,ref}} \cdot PI_{\mathrm{G}}(s). \tag{8.15}$$

For the outer loop model, the system power equation is applied and is listed as,

$$p_{\mathrm{PV}} = v_{\mathrm{PV}} \cdot i_{\mathrm{PV}} = \frac{1}{2} \cdot C_{\mathrm{IN}} \frac{d{v_{\mathrm{PV}}}^2}{dt} + v_{\mathrm{G}} \cdot i_{\mathrm{G}}. \tag{8.16}$$

By considering $\Delta p_{\mathrm{PV}}(t)$, $\Delta v_{\mathrm{PV}}(t)$, $\Delta i_{\mathrm{PV}}(t)$ and $\Delta i_{\mathrm{G}}(t)$ as the small-signal perturbations of p_{pv}, v_{pv}, i_{pv} an i_{G} in the small signal analysis model, the relationship between the input and output sides can be found as,

$$G_{\mathrm{inv,V}}(s) = \frac{\Delta v_{\mathrm{pv}}}{\Delta i_{\mathrm{g}}} = \frac{V_{\mathrm{G}}}{I_{\mathrm{pv}} - X_{\mathrm{pv}} \cdot V_{\mathrm{pv}} - s \cdot C_{\mathrm{IN}} \cdot V_{\mathrm{pv}}}, \tag{8.17}$$

$$G_{\mathrm{PO}}(s) = \frac{\Delta v_{\mathrm{pv}}}{\Delta p_{\mathrm{g}}} = \frac{1}{I_{\mathrm{pv}} - X_{\mathrm{pv}} \cdot V_{\mathrm{pv}} - s \cdot C_{\mathrm{IN}} \cdot V_{\mathrm{pv}}}. \tag{8.18}$$

From (8.18), it shows that the input capacitor dominates the performance of the outer loop. If the capacitance is selected with a higher value, the control bandwidth will become lower.

8.5 System Performance Evaluation

8.5.1 Stability Analysis

From the determined system models, the relationship of each individual loops is found. Thus, the Bode plot is applied to evaluate the system stability. Due to the presence of the *CL* filter in the system, the system stability issue becomes a concern and it increases the difficulty in the controller design. The frequency response of (8.10) is given in Figure 8-8. As shown in the figure, a resonant point appears at 2.8 kHz together with a 180 degree phase change. At that point, a complex resonant pole occurs and the system gain margin point is located. Under traditional PI control, if only the grid current is controlled, the system would not meet the stability margin in the Bode plot. Therefore, a double current control method is applied to the system control in this chapter.

In the presented control strategy, the system inner loop is a converter-side inductor current

control and a capacitor voltage damping circuit. The effect of the damping circuit in the inner loop is shown in Figure 8-9. When the system doesn't have any damping factor, high resonance peak and large phase change occur at that frequency point. Therefore, at some transient or light load situations, the system may become unstable. Once the damping factor is added, the resonance peak is reduced and a smooth phase change appears. Large in K_D, the resonance peak amplitude becomes smaller. Thus, a stable system is achieved under the traditional PI control method.

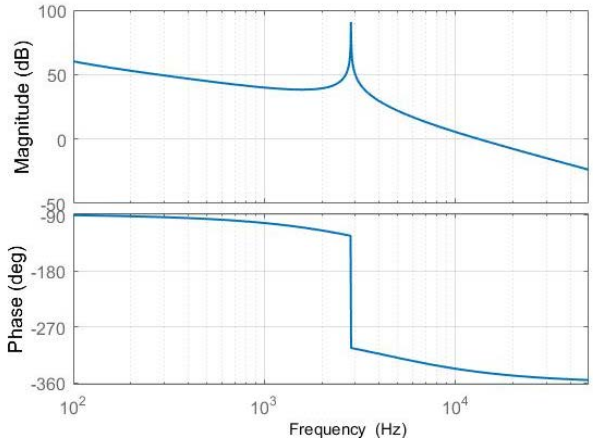


Figure 8-8. Bode plot of the relationship between duty cycle and grid current.

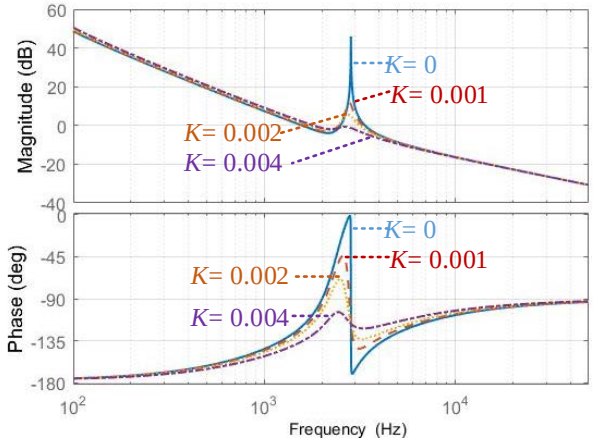
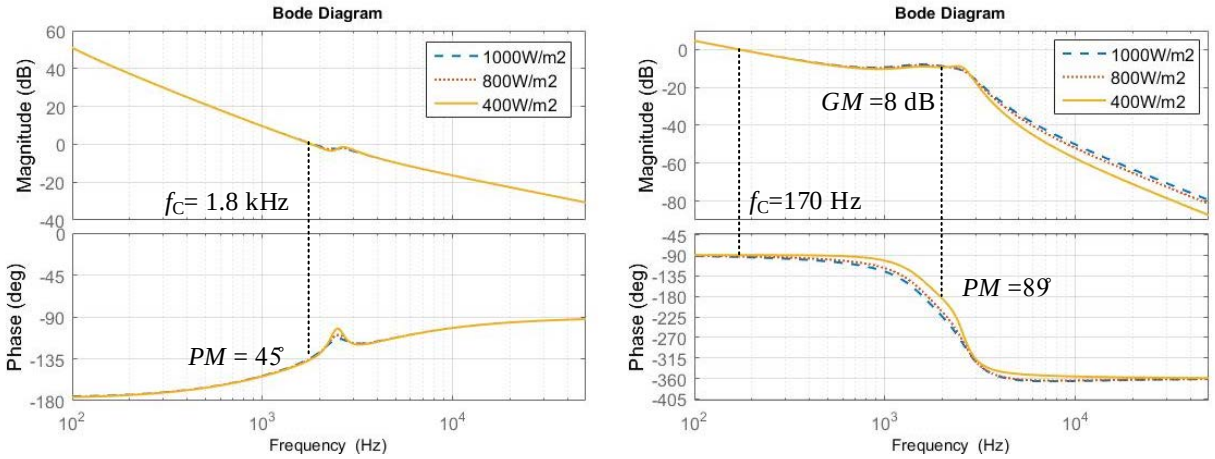
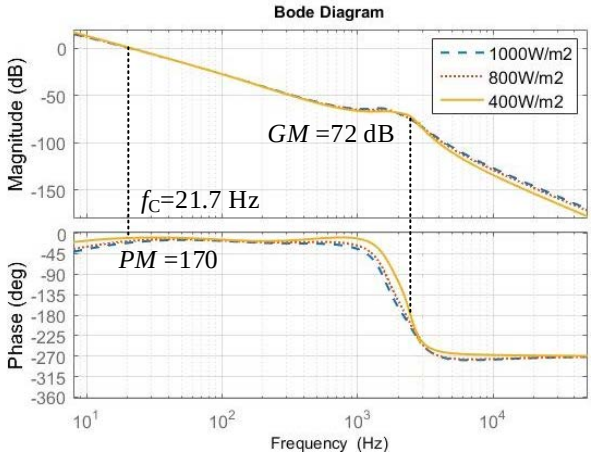


Figure 8-9. Bode plot of the inner loop with different damping ratios.



(a)

(b)



(c)

Figure 8-10. Bode plots of (a) converter-side inductor current loop, (b) grid-side inductor current loop and (c) input voltage loop.

The Bode plot of the presented control methodology is shown in Figure 8-10 where the converter-side inductor current loop, grid-side inductor current loop and input voltage loop are plotted in Figure 8-10 (a), (b) and (c) respectively. In the presented methodology, both converter-side inductor current and the grid-side inductor current are also under controlled separately. The converter-side inductor current loop is the fastest loop which controls the switching action of the

converter. The input voltage loop is the lowest in response. The inner loop bandwidth is set to 5 to 10 times lower than the targeted switching frequency. Meanwhile, each loop bandwidth is also set to 5 to 10 times different from each other to avoid the loop inference. Also, the system phase margin keeps higher than 45 degree and a positive phase margin is kept at all the test cases. As shown in Figure 8-10, all the loops are unaffected by the resonant issue and provide a stable inverter performance. Thus, a stable system operation can be always guaranteed.

8.5.2 System MPPT Efficiency

The MPP tracking efficiency is used to indicate the relationship between the panel output power and the maximum available power from the panel. The system tracking performance is mainly depended on the input capacitor value and the loop bandwidth of the outer loop. Two different types of tracking efficiency are involved, which are static and dynamic MPPT efficiencies. According to [8.20], the formula of the static MPPT efficiency can be determined as,

$$\eta_{\text{static}} = \frac{1}{n \cdot P_{\text{peak}}} \cdot \left[\sum_{k=1}^{n} i_{\text{PV}}\left(\frac{k \cdot 2T}{n}\right) \cdot v_{\text{PV}}\left(\frac{k \cdot 2T}{n}\right)\right], \tag{8.19}$$

where P_{peak} is maximum available power from PV panels under a fixed irradiation situation.

Meanwhile, the formula of the dynamic MPPT efficiency is,

$$\eta_{\text{dynamic}} = \frac{\int_0^{T_s} i_{\text{PV}}(t) \cdot v_{\text{PV}}(t) dt}{\int_0^{T_s} p_{\text{peak}}(t) dt}, \tag{8.20}$$

where T_s is a dynamic period defined in [8.20] and p_{peak} is the offered maximum available power from PV panels during dynamic period.

Different from [8.7], the input capacitor is located at the system input and is parallel to the PV panel. Generally, the design of C_{IN} is based on the double LF voltage ripple in the input side.

However, in a PV system, the value selection of the input capacitor becomes complicated, as it is highly related with the system tracking efficiency. Higher in capacitor value, the double LF voltage ripple will become lower and the static MPPT efficiency becomes higher. However, the outer loop bandwidth will be reduced. The loop bandwidth is highly related to the dynamic performance of the system. Lower in the system bandwidth, the dynamic MPPT efficiency of the system is lower. Thus, a trade-off appears between the static and dynamic MPPT efficiencies. In order to keep the overall system efficiency in a high value. A 1.9 mF capacitor is selected, so that the lowest inverter static MPPT efficiency can keep higher than 98 %. A capacitor trace-off figure is shown in Figure 8-11.

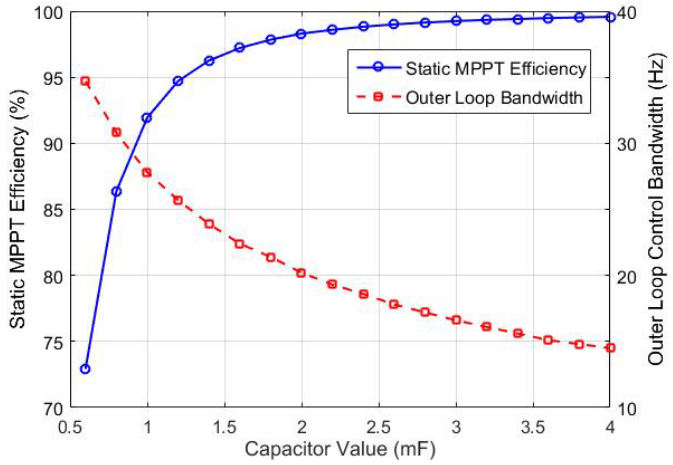


Figure 8-11. System performance under different input capacitor values.

8.6 Experimental Verification

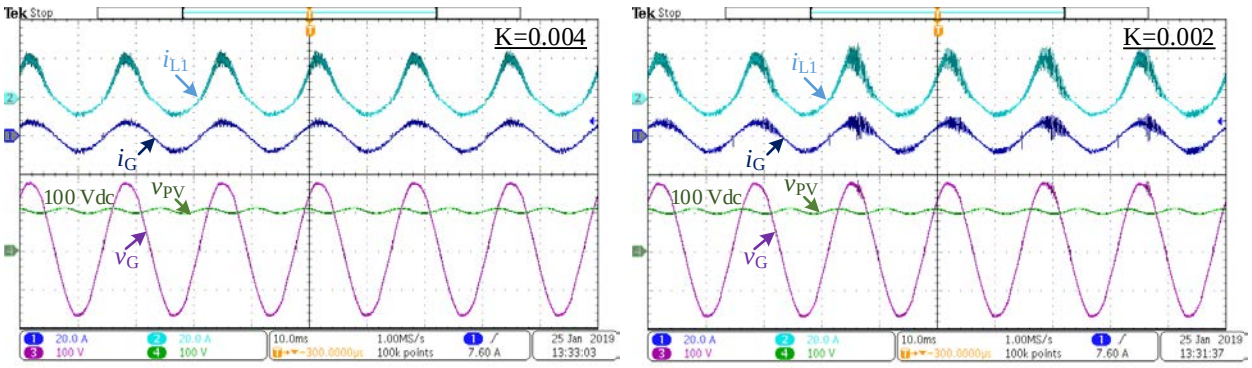
A 750 W grid-connected buck-boost type PV inverter (Manitoba Inverter) prototype has been implemented for the system verification. A set of experimental results are shown in Figure 8-12 and Figure 8-13. In the evaluation, a solar array simulator was applied as the inverter source. It used to simulate PV panels with series connection structures and voltages in the range of 200 Vdc.

The output of the inverter was directly connecting to a 120 Vac grid.

Specification of the prototype and the key parameters of the simulator setup are given in TABLE 8-I. Accordingly, the corresponding PV characteristic is shown in Figure 8-14 (a) with the use of a P-V curve where the MPP is located at 100 Vdc. The corresponding MPP current is 7.5 A. Similarly, when MPP point is shifted 200 Vdc, another P-V curve is generated which is shown in Figure 8-14 (b). The corresponding MPP current is 3.75 A. The output of the PV panel was in a non-linear characteristic. When the irradiation was 1000 W/m^2, the full rated power was expected to be 750 W.

TABLE 8-I SPECIFICATION OF THE PV SIMULATOR @ 100 VDC 1000 W/M^2 AND OF THE INVERTER PROTOTYPE

Simulator	Parameter	MPP Power	MPP Voltage	MPP Current	Open Circuit Voltage	Short Circuit Current
	Value	750 W	100 V	7.5 A	121.18 V	8.087 A
Prototype	Parameter	Grid Frequency	Grid Voltage	Switching Frequency	Inductors (L_1 & L_2)	Capacitor (C_{AB})
	Value	60 Hz	120 Vac	20 kHz	780 µH	5.6 µF



(a) (b)

Figure 8-12. Steady state waveforms at 1000 W/m^2 with a, (a) 0.004 and (b) 0.002 damping factors.

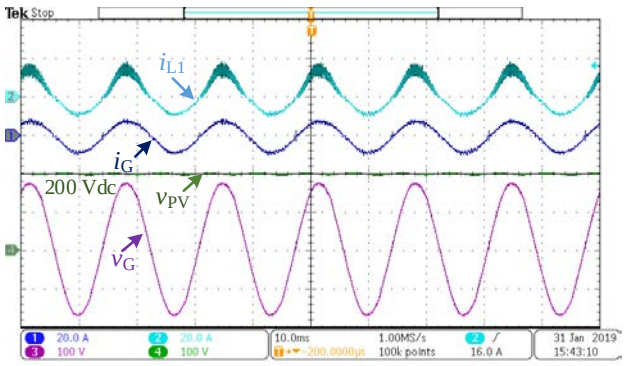
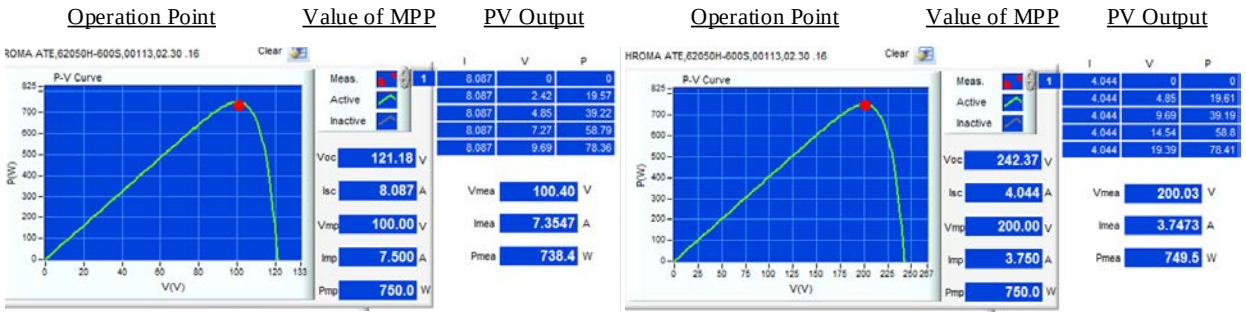


Figure 8-13. Steady state waveform at 1000 W/m^2 with 200 Vdc input.



(a) (b)

Figure 8-14. PV characteristics, (a) at 100 V input voltage, and (b) at 200 V input voltage.

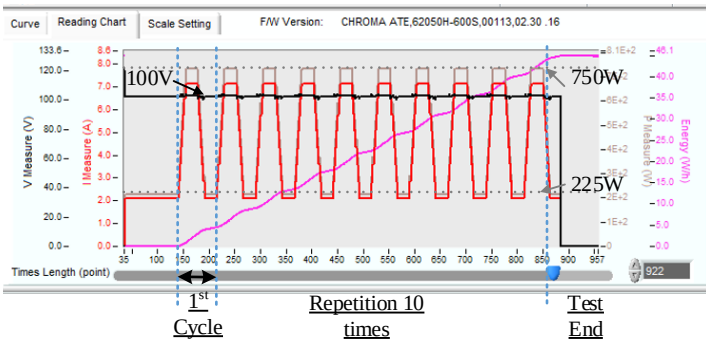
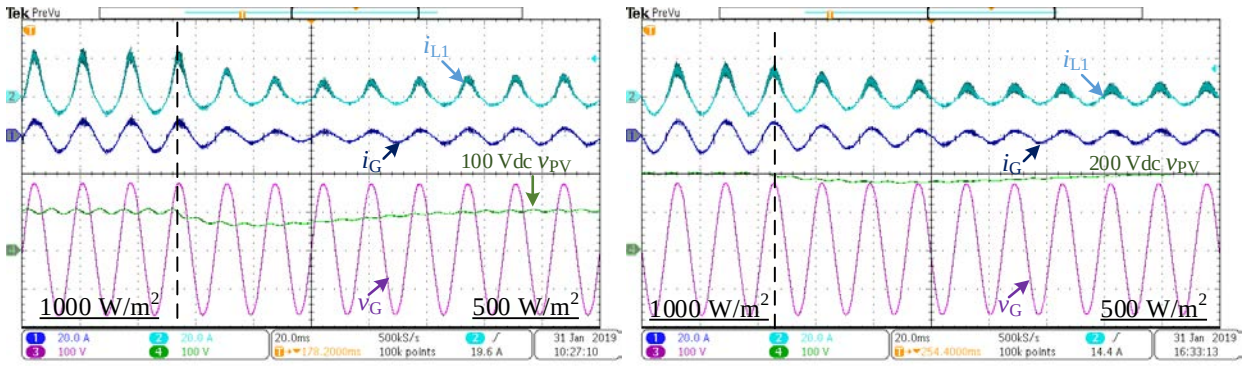


Figure 8-15. Dynamic MPPT test under EN50530.



(a) (b)

Figure 8-16. Waveforms of transient operation from 1000 W/m^2 to 500 W/m^2 at (a) 100 Vdc and (b) 200 Vdc.

TABLE 8-II SUMMARY TABLE OF THE SYSTEM MPPT EFFICIENCIES

MPP Voltage (Vdc)	Static MPPT Efficiency (%)	Dynamic MPPT Efficiency (%)
100	98.5	98.1
200	99.9	99.4

In Figure 8-12 (a), a steady state performance is demonstrated under 1000 W/m^2 irradiation and with 100 Vdc input. Under the presented control methodology, the system was stabilized at the MPP voltage point. In addition, a continuous and sinusoidal grid current was resultant. According to the inverter operation principle, both inductor currents were different in each half line cycle. In the positive half line cycle, L_1 acted as the converter-side inductor which was used for the power conversion. In the negative half line cycle, L_1 acted as the grid-side inductor which was used to filter those HF grid current ripple. As a result, the shape and the magnitude of i_{L1} were different in each half line cycle. Meanwhile, in Figure 8-12 (b), it shows the importance of the damping circuit. When the damping factor was dropped to 0.002, the inner loop stability was affected. As mentioned in Section 8.5, when the damping factor was not enough, the magnitude gain at the resonance point became positive. Thus, the system stability was affected. Other than

100 Vdc MPP voltage, the inverter also performed stable at different input voltage points. In Figure 8-13, the steady state waveform of the inverter is demonstrated at 200 Vdc input, respectively. Stable performance was also obtained and a high quality grid current was guaranteed.

The function of the MPPT is shown in Figure 8-14. During the steady state, the system was able to stabilize at the MPP voltage point and to collect the maximum available power from the PV panel. During the tracking, when the system voltage fell in the left part of the MPP voltage point, the reference voltage would be increased to track back the MPP. In contrast, the reference voltage would also be reduced when the system voltage fell in the right part of the MPP voltage point according to the implemented tracking function. As shown in Figure 8-14 (a), the system static MPPT efficiency at 100 Vdc MPP voltage is kept higher than 98.5 %. Also, according to EN50530 [8.20], the corresponding dynamic MPPT efficiency is 98.1 %. The dynamic MPPT test pattern and the test result are shown in Figure 8-15. Similarly, at 200 Vdc MPP voltage test case, both dynamic and static MPPT efficiencies are kept higher than 99.4 %. A summarized table of the system MPPT efficiencies is given in TABLE 8-II. As a result, an efficient PV inverter system is able to be guaranteed.

In Figure 8-16, a set of transient waveforms of the presented system is demonstrated. In Figure 8-16 (a), the MPP voltage was fixed at 100 Vdc, the irradiation was dropped from 1000 W/m^2 to 500 W/m^2. From the result, it showed that after a step change in irradiation, the system was able to recover back to the MPP in a short period of time and to maintain stable performance during the transient process. The response time was mainly depending on the size of the input capacitor and the tracking speed of the outer loop. Similarly, in Figure 8-16 (b), the irradiation was dropped from 1000 W/m^2 to 500 W/m^2 at 200 Vdc. From the result, it showed that after a step change irradiation, the system also maintained stable performance during the transient process. Moreover, the system was recovered to the MPP in a short period of time and the new MPP voltage was tracked correctly.

Under the proposed control scheme, it offered a high quality output current to the grid, kept tracking the MPP at the input and let the inverter to operate stably in any situations. Thus, the advantages of the inverter topology are maximized in PV applications.

8.7 Conclusion

The chapter has presented a comprehensive control strategy for a recently proposed single-phase single-stage transformerless buck-boost type PV inverter system. The system design and the detailed system modelling were given in this chapter. Under the proposed control scheme, the PV inverter was able to effectively transfer the maximum available solar power into the grid, maintained the system grid current in high quality. Also, such proposed control scheme improved the system stability and let the system able to adopt all the possible outputs from the PV panel. The performance of the PV inverter system and control methodology were demonstrated with the experimental results. A 750 W grid-connected PV prototype has been implemented. Stable performance was able to be obtained in both steady state and transient conditions. All the experimental results were consistent with the theoretical concepts.

Reference

[8.1] K. K. M. Siu and C. N. M. Ho, “Modelling and Stability Study of a Single Stage Buck-Boost Inverter for PV Application,” in *Proc. IEEE ECCE*, pp. 7088-7093, Sept. 2018.

[8.2] T. K. S. Freddy, N. A. Rahim, W.P. Hew, and H. S. Che, “Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters,” *IEEE Trans. Power Electron.,* vol. 29, no.10, pp.5358 – 5369, Oct. 2014.

[8.3] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules,” *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292-1306, Oct. 2005.

[8.4] S. Jain and V. Agarwal, “A Single-Stage Grid Connected Inverter Topology for Solar PV Systems With Maximum Power Point Tracking,” *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1928 – 1940, Sept. 2007.

[8.5] H. Patel and V. Agarwal, “A single-stage single-phase transformer-less doubly grounded grid-connected PV interface,” *IEEE Trans. Power Electron.,* vol. 24, no. 1, pp. 93-101, Mar. 2009.

[8.6] T. Sreekanth, N. Lakshminarasamma, and M. K. Mishra, “A Single-Stage Grid-Connected High Gain Buck–Boost Inverter With Maximum Power Point Tracking,” *IEEE Trans. Energy Convers.*, vol. 32, no. 1, pp. 330-339, Mar. 2017.

[8.7] C. N. M. Ho and K. K. M. Siu, “Manitoba Inverter - Single Phase Single-Stage Buck-Boost VSI Topology,” *IEEE Trans. Power Electron.,* vol. 34, no. 4, pp. 3445-3456, April 2019.

[8.8] M. Jang, M. Ciobotaru, and V. G. Agelidis, “A Single-Stage Fuel Cell Energy System Based on a Buck--Boost Inverter with a Backup Energy Storage Unit,” *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2825-2834, June 2012.

[8.9] P. Sanchis, A. Ursua, E. Gubia, and L. Marroyo, “Design and experimental operation of a control strategy for the buck-boost DC-AC Inverter,” *IEE Proceedings - Electric Power Applications*, vol. 152, no. 3, pp. 660-668, May 2005.

[8.10] X. Ji, T. Zhang, H. Su, Z. Xia, Z. Tang, and G. Zhu, “Single phase gird connected inverter based on one-cycle current control,” in *Proc. IEEE IPEMC-ECCE Asia*, pp. 2899-2903, May 2016.

[8.11] B. Zhao, R. Ma, B. Liang, and A. Abramovitz, “One-cycle-controlled high gain single stage Buck-Boost inverter for photovoltaic application,” in *Proc. IEEE IECON*, pp. 7813-7817, Nov. 2017.

[8.12] A. Darwish, A. Massoud, D. Holliday, S. Ahmed, and B. Williams, “Generation, performance evaluation and control design of single-phase differential-mode buck-boost current-source inverters,” *IET Renewable Power Generation*, vol. 10, no. 7, pp. 916-927, July 2016.

[8.13] Z. Yue, “Study of buck-boost photovoltaic inverter based on discrete sliding mode control strategy,” in *Proc. IEEE MACE*, pp. 1643-1647, July 2011.

[8.14] Y. He, K. W. Wang, and H. S. H. Chung, “Utilization of Proportional Filter Capacitor Voltage Feedforward to Realize Active Damping for Digitally Controlled Grid-Tied Inverter Operating Under Wide Grid Impedance Variation,” in *Proc. IEEE ECCE*, pp. 4450-4457, Sept. 2014.

[8.15] H. Patel and V. Agarwal, “MPPT Scheme for a PV-Fed Single-Phase Single-Stage Grid-Connected Inverter Operating in CCM With Only One Current Sensor,” *IEEE Trans. Energy Convers.*, vol.24, no.1, pp. 256-263, Mar. 2014.

[8.16] F.E. Aamri, H. Maker, D. Sera, S. Spataru, J.M. Guerrero, and A. Mouhsen, “A Direct Maximum Power Point Tracking Method for Single-Phase Grid Connected PV Inverters,” *IEEE Trans. Power Electron.*, vol. 33, iss. 10, pp. 8961-8971, Oct. 2018.

[8.17] A.Gow and C. D. Manning, “Development of a photovoltaic array model for use in power electronics simulation studies,” in *Proc. IEEE Elect. Power Appl.*, vol. 146, no. 2, pp. 193-200, Mar. 1999.

[8.18] J. Cubas, S. Pindado and C.D. Manuel, C. “Explicit Expressions for Solar Panel Equivalent Circuit Parameters Based on Analytical Formulation and the Lambert W-Function,” *Energies*, vol. 7, pp. 4098–4115, Jun. 2014.

[8.19] M. Fazeli, J.B. Ekanayake, P.M. Holland, and P. Igic, “Exploiting PV Inverters to Support Local Voltage—A Small-Signal Model,” *IEEE Trans. Energy Convers.*, vol. 29, no. 2, pp. 453-462, Jun. 2014.

[8.20] *Overall efficiency of grid connected photovoltaic inverters*, EN Standard 50530, 2010.

Chapter 9 Conclusion and Future Work

9.1 Conclusion

In this thesis, a comparative study was done on the various kinds of grid-connected topologies with CM voltage mitigation techniques. Through the analysis, according to noise voltage mitigation techniques, a topology classification method was presented. Different types of converter topology were evaluated and benchmarked based on the magnitude of common mode noise voltage and the high frequency ripple of the grid current. With the use of the high frequency virtually grounded concept, a series of new topologies was successfully developed that was with high efficiency and low leakage current performance. The design of boost-type rectifier, buck-boost type rectifier, buck-boost type inverter, and boost-type four-quadrant voltage source converter were all covered. All converters were all in single-phase and single-stage designs.

The operational principles of each topology were determined and the corresponding modulation methods were provided. By using the high frequency analysis method, the high frequency models of each converter topologies were found and were used to proof the low common mode noise characteristics of the proposed topologies. Meanwhile, the steady state characteristics of each proposed topologies were also derived. Accordingly, based on the needs of the application and the design requirements, guidelines for system design and components selections were provided. In addition, different kinds of stabilized control scheme were built to coordinate with the high frequency virtually grounded technique and to maximize the converter performance of new proposed topologies. A specific hardware prototype was built for each discussed topology and was used to verify the proposed topology performance experientially. All the time, stable performance was able to be obtained in both steady state and transient conditions. All the

performance metrics were met, and all the experimental results were consistent with the theoretical concepts.

9.2 Future Work

The work presented in this thesis can be extended. Several extensions and further studies based on this thesis can be explored as follows:

- On the single-stage grid-connected converter designs, double line frequency ripple is always present in the dc side. In PV applications, it rises out a performance trade-off between the static and dynamic MPPT efficiencies. One of the alternative solutions is to integrate the power decoupling method into the topology where a smaller dc capacitor can be used, but both static and dynamic MPPT efficiencies are improved.
- While this thesis focuses on single-phase systems, it is also possible to extend the idea of the high frequency virtually grounded technique into the three-phase converter topologies. Thus, units with higher power rating are able to be supported and more applications are benefited.
- In different applications, different design requirements are resulting. In order to extend the benefits of those proposed converters, efficiency and performance optimization methods should be developed. Both Si MOSFETs, IGBTs, SiC MOSFETs, and GaN transistors should be included under the optimization process.
- In the developed buck-boost converter topologies, a low-pass filter is always formed between the grid and the switching circuit. Apart from the proposed control method, the second-order boundary control is another control methodology to maintain the

system operating properly under the resonant characteristic. Focusing on the discontinuous filter capacitor current, a new set of control theory will be derived.