Design and Implementation of an Automated Testbed for Evaluating Switching Behavior of Power Semiconductors

by

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Abstract

A Double Pulse Tester (DPT) is a widely used setup for evaluating the switching behavior of power semiconductor devices. The results obtained from double pulse tests provide significant insight into the dynamic behavior of a device under test (DUT) such as its switching losses, switching speed (*di/dt*, *dv/dt*), turn-on and turn-off times etc. However, it is a tedious process to perform these tests under different permutations of test parameters and thereafter analyze the experimental data manually. This work presents a newly developed automated DPT prototype, which can run the tests one after another once the test conditions are entered in a Graphic User Interface (GUI). The test-control system also records the switching waveforms, test data, and systematically processes them to generate usable characterization results. The automatic, low cost, compact, modular and user-friendly design allows the proposed testing and measurement system to stand out from the conventional DPT setups. The design principles are experimentally verified by implementing a DPT prototype capable of testing power semiconductor devices up to 1000V, 60A, 250°C.

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Dedication

To my dear parents and beloved wife

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List of Abbreviations

AC	Alternating current
DC	Direct current
PE	Power Electronic
GTO	Gate turn-off thyristor
IEGT	Injection-enhanced gate transistor
IGBT	Insulated-gate bipolar transistor
FET	Field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
HEMT	High-electron-mobility transistor
WBG	Wide-bandgap
Si	Silicon
SiC	Silicon Carbide
GaN	Gallium Nitride
DPT	Double pulse tester
DUT	Device under test
FWD	Freewheeling diode
PCB	Printed circuit board
EMT	Electromagnetic transient
GUI	Graphic user interface
SMD	Surface mount device
PSU	Power supply unit

HV	High voltage
DPCU	Double pulse control unit
IC	Integrated circuit
IDE	Integrated development environment
VISA	Virtual Instrument Software Architecture
USB	Universal Serial Bus
PC	Personal computer
PWM	Pulse Width Modulation
CVR	Current viewing resistor
WAT	Waveform Analysis Tool
LUT	Lookup table

Chapter 1 Introduction

1.1 Background

Power Electronic (PE) converters play a significant role in efficient control, conversion and conditioning of electric power in today's energy systems. PE systems are primarily based on switching of power semiconductor devices by applying control signals in order to control the flow of current. The semiconductor devices being the heart of these converters, are one of the key components that determine the efficiency, size, and cost of these PE systems [1]-[7]. With the advent of wide bandgap power semiconductor devices that can be operated at higher switching frequencies, the filter sizes can be reduced leading to improved power density of the PE converters [8]. However, with increased switching frequency, the switching losses become a key contributor of the total converter losses [9],[10]. In the study of power converter optimization, accurate measurement of switching losses is therefore necessary for precise converter loss estimations. Possible techniques for measurement of conduction losses are discussed in [11]. In this thesis, the design and implementation techniques of an advanced device characterization tool for evaluating the switching performance of a semiconductor device has been explored.

The purpose of switching characterization is to study and evaluate the dynamic behavior of a device under various test conditions. The data obtained from the switching tests can greatly facilitate power converters' design regarding the selection of switching frequency, dead time setting, thermal management and efficiency estimation [12]-[14]. A study of the transient behavior of a power device also helps us to predict its dynamic performance in a target application. However, a fast, accurate and reliable testing & measurement system is necessary to capture the high-speed switching transients of a power device. In practice, a Double Pulse Tester (DPT) is

used for this purpose [15]. The DPT is also widely used to tune simulated semiconductor device models to improve possible accuracy so that the models can emulate real devices in terms of overall performance, loss behavior, voltage and current overshoots etc. [16],[17].

1.2 Review of Semiconductor technologies

Power semiconductor switches are the heart of any power electronic application. Silicon based power semiconductor devices i.e. diodes, thyristors, IGBTs, MOSFETs have dominated the power electronics and power systems market since the late 1950s. Si IGBTs and MOSFETs still represent the present standard for power switches in typical power applications such as AC/DC, DC/DC supplies, motor drives in low, medium and high power segments. Figure 1.1 depicts the power rating and frequency where the most common power semiconductor devices can operate [18],[19].

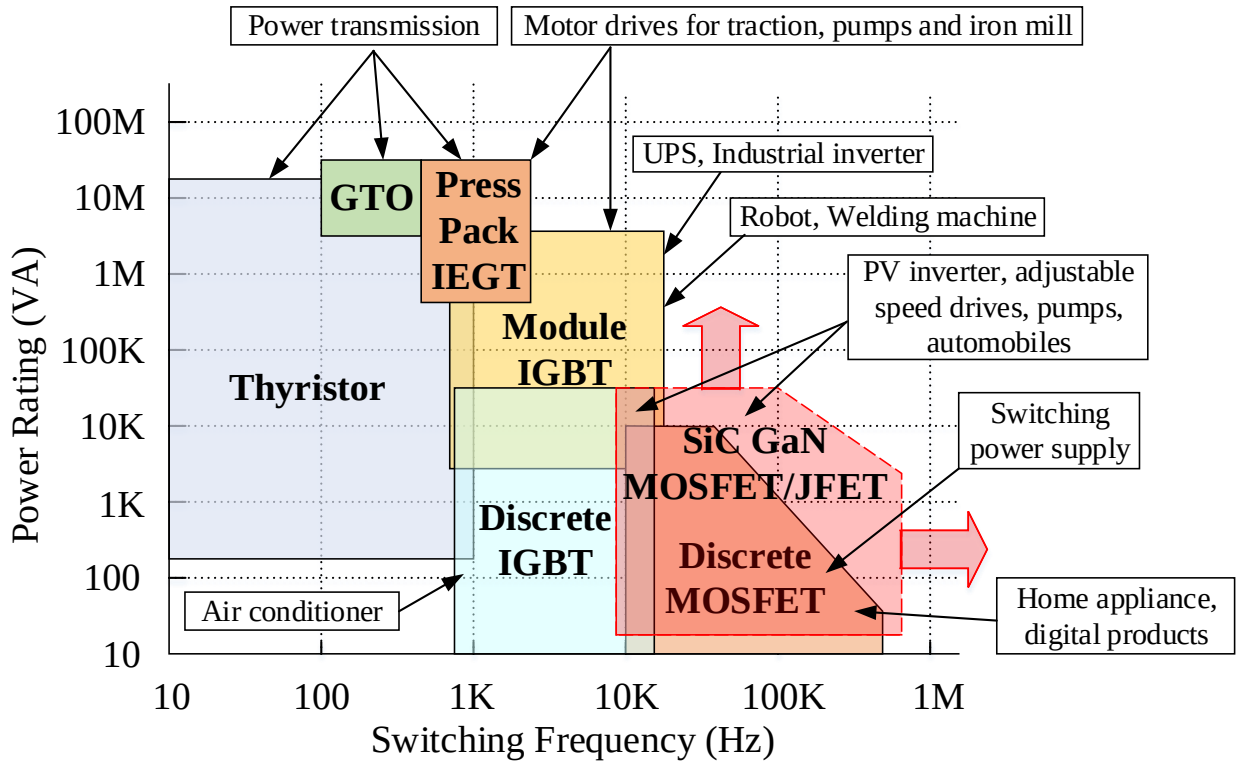


Figure 1.1 Typical operating regions of power semiconductor switches [18], [19].

The above plot presents an overall picture on the typical integration of power semiconductors in different industrial areas. The thyristors are used for low frequency, high power applications, IGBTs for medium frequency and power applications, and power MOSFETs for high frequency applications. These devices have undergone continual improvements in their key parameters such as on-state resistance, voltage and current ratings, switching speeds, packages as well as other attributes. However, due to continuous device optimization and improvements in production process, the performance of Si devices are approaching their theoretical limits imposed by its fundamental material properties. The next generation of power electronic systems has to achieve high power density, high efficiency and at the same time has to be cost-effective in terms of production and implementation.

The three major materials used for fabrication of power semiconductor devices are Silicon (Si), Silicon Carbide (SiC) and Gallium Nitride (GaN). The key properties of these materials are compared in Table 1.1 [7], [20]. SiC and GaN, which are categorized as Wide Bandgap (WBG) materials were introduced during the last decade as alternative materials for fabrication of power semiconductors. In recent years, WBG devices especially GaN high-electron-mobility transistor (HEMT) have emerged as promising technology for achieving high frequency, high-density power conversion [21]-[31]. Due to the superior material properties of GaN, it allows system operation at higher voltage, temperature and switching frequency in contrast with the state-of-the-art Si based counterparts [1], [7], [20], [32]. Figure 1.2 is a visual representation of the material property figures of these three popular semiconductor materials and it presents a clear picture of the superiority of WBG materials [33], [34].

Table 1.1 Material properties of Si, SiC and GaN [7], [20]

Properties	**Si**	**SiC**	**GaN**
Bandgap, E_g (eV)	1.12	3.26	3.39
Electric Breakdown/Critical field, E_{crit} (MV/cm)	0.3	2.0	3.3
Saturated electron drift velocity, V_s (10^7 cm/s)	1.0	2.0	2.5
Electron mobility, μ_n (cm^2/V.s)	1350	650	2000
Permittivity, ε_r	11.8	9.7	9

SiC and GaN are classified as WBG devices because the band gap energy E_g of these two materials is significantly higher than that of Si, as seen from Table 1.1. The band gap of a semiconductor material reveals the strength of the atomic bonds in its lattice [35]. High band gap in addition to other factors ensure greater lattice structure stability. This is why power semiconductor materials fabricated with these materials tend to have lower leakage current and have the ability to withstand higher operating temperature.

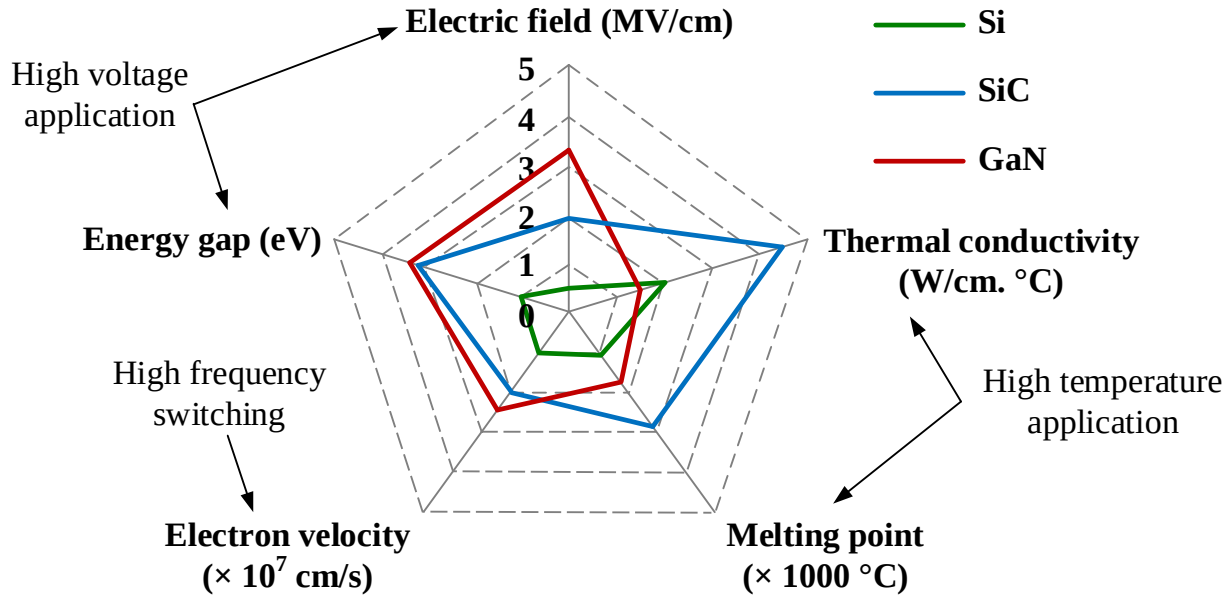


Figure 1.2 Visualization of material property comparison of Si, SiC and GaN [33], [34].

The robust chemical bonds responsible for the wider band gap in WBG devices and other material properties also cause higher critical electric field. The breakdown voltage of a device V_{BR} can be approximated by the following equation [35].

$$V_{BR} = \frac{1}{2} \cdot w_{drift} \cdot E_{crit} \tag{1.1}$$

Therefore, V_{BR} is proportional to the width of the drift region, w_{drift}. For the same breakdown voltage, the drift region in GaN and SiC can be 10 times smaller than Si [35].

The superiority of the material properties of WBG devices with respect to Si devices can be further explained with help of Poison's equation.

$$q \cdot N_D = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot E_{crit}}{w_{drift}} \tag{1.2}$$

In equation 1.2, q is the charge of the electron, N_D is the total number of electrons in the volume, ε_0 is the permittivity of vacuum, and ε_r is the relative permittivity of a GaN crystal to vacuum. From Table 1.1, it can be seen that the critical field E_{crit} of GaN is 10 times higher and from equation 1.1, the drift region w_{drift} is 10 times narrower than Si. By plugging in these two information in equation 1.2, it can be concluded that the number of electrons, N_D in the drift region can be 100 times greater for WBG devices. This is the reason a significantly better power conversion efficiency can be achieved by SiC and GaN with respect to Si semiconductor devices.

The theoretical on-state resistance R_{DS_ON} of a semiconductor device with electron mobility μ_n can be expressed as:

$$R_{DS\_ON} = \frac{w_{drift}}{q \cdot \mu_n \cdot N_D} \tag{1.3}$$

Further combining equations 1.1, 1.2 and 1.3, a relationship between device breakdown voltage and on-state resistance can be derived, which is expressed as:

$$R_{DS\_ON} = \frac{4 \cdot {V_{BR}}^2}{\varepsilon_0 \cdot \varepsilon_r \cdot \mu_n \cdot (E_{crit})^3} \tag{1.4}$$

This equation is a clear indication of the fact that devices with high critical field and electron mobility has considerably low on-state resistance. In Figure 1.3, which is a plot based on equation 1.4, the theoretical limits of material properties for Si, SiC and GaN are represented with solid lines. This is one of the popular ways of interpreting the inherent crystal parameters of these materials into a visual reference for comparison of device performance. According to experts, Si solutions have significantly matured and optimized over the last three decades and presently they are in the verge of theoretical limits of its material characteristics. However, a quick glance at Figure 1.3 implies the saturation limit for GaN is far beyond Si and SiC [36]-[38].

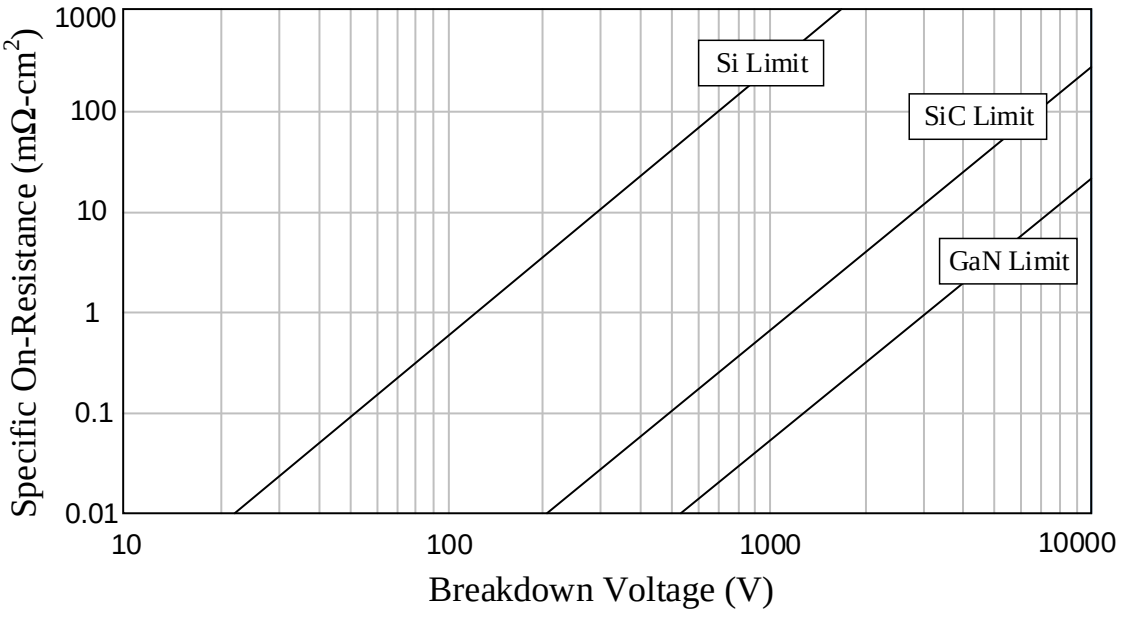


Figure 1.3 On-state resistance vs. breakdown voltage indicating theoretical limits for Si, SiC and GaN semiconductor materials.

As compared to Si devices, GaN devices have smaller gate charge and junction capacitors. A faster turn-on, turn-off speed is achieved due to smaller gate charge whereas due to a smaller junction capacitor, relatively less energy is stored during the turn-off period. The switching loss, which occurs due to the current and voltage overlap during the switching transition, is significantly reduced due to these properties. For the same efficiency, GaN devices allow converter operation in much higher frequencies with respect to Si devices. The switching frequency has been continually pushed up to several megahertz that allows reduction in the size of passive components and increase in power density of the system.

Extensive research has been done on performance comparisons between Si and GaN devices [39]. In the recent years, GaN high electron mobility transistor (HEMT) has been commercialized and used in some prototypes of power electronic systems, such as dc-dc converters, power factor correction converters and motor drives [21],[29],[39]-[41]. The performance, size, and cost improvement is significant with use of WBG semiconductors due to lower energy losses and smaller heat sink requirement. Hence, GaN HEMTs have emerged as a promising device for high power density applications [7],[26],[28],[31],[42]. It shows the importance of WBG semiconductor technology for future power electronic applications. However, GaN HEMT being a relatively new semiconductor technology, a lot of information regarding its performance in different application environments is still unknown. Hence, the characterization of switching behavior i.e. measurement of its turn-on and turn-off transients of GaN diodes and HEMTs is an ongoing study in both academia and industry.

The development of power semiconductor technology has led to great improvement in power handling capabilities and switching speed of power devices [43]. Despite its limitations, Si

technologies have proved adaptable and still used in a mass scale by industries around the globe due to their minimal cost, ease of implementation and relatively simpler control techniques.

1.3 Semiconductor characterization

The typical electrical characterization tests performed on a power semiconductor device can be broadly classified into static and dynamic tests. The purpose of static I-V (current-voltage) characterization is to understand the steady-state behavior of a device under certain operating parameters, such as gate voltage, device voltage and current. The junction temperature greatly affects the I-V characteristics of a device. If the device is continuously kept switched on to evaluate the static on-state behavior, the conduction losses may alter the junction temperature thereby affecting the test results. Hence, pulsed I-V test is performed to ensure the test conditions remain unchanged in the temporary on-state period. A curve tracer is typically used to perform pulsed static characterization tests in order to determine several device parameters such as on-state resistance, maximum current capability, leakage current, device breakdown voltage, saturation voltage, transconductance, capacitance etc. Curve tracers are available for purchase from test equipment manufacturers such as Tektronix and Keysight. Some popular models are 370 series curve tracers from Tektronix and B1500 series Semiconductor Device Analyzers from Keysight. The device setup and measurement techniques for static characterization are elaborately discussed in [44].

The dynamic switching characterization of power semiconductor devices gives us insight into the switching behavior of the device under various test conditions. The switching performance of a device changes with the operating voltage, current, junction temperature and the value of gate drive resistances. In a switching characterization test, these parameters are mainly regulated and the transient performance during switching of the device under test (DUT) is observed in an

oscilloscope. In this thesis, the terminologies of an IGBT is used in the text and figures however, the same concept applies for other semiconductor devices. One can gain useful information on several key parameters of the DUT such as Current rise/fall gradient (di/dt), Voltage rise/fall gradient (dv/dt), rise time (t_{rise}), fall time (t_{fall}), turn-on switching energy loss (E_{on}) and turn-off switching energy losses (E_{off}) etc. after analysing the collector-emitter voltage (V_{CE}), collector current (I_C) and gate voltage (V_{GE}) waveforms captured during the switching tests. The definition of the above-mentioned DUT switching parameters are discussed in the following sections and illustrated with Figure 1.4 and Figure 1.5.

1.3.1 Turn-on Characteristics

The key switching parameters of a device obtained from dynamic characterization tests are labelled in Figure 1.4 and Figure 1.5. In this section, the parameters are further defined and their implications on power electronic application, mainly converter design are discussed. These definitions are in accordance with JEDEC standard JESD24-1 which states the method for measurement of power device turn-off switching loss [45].

1) Current Rise Time (t_{rise}): It is the time taken by I_C to rise from 10% to 90% of the nominal current. This parameter is an indication of how quickly the collector current approaches the load current. It contributes to the total turn-on time and partially determines the maximum allowable switching frequency for the device.

2) Turn-on Delay Time (t_{d-on}): The time interval from V_{GE} rising to 10% of the nominal gate voltage to I_C rising to 10% of its nominal value is t_{d-on}. A measure of t_{d-on} indicates how fast the device can be turned on and its reaction time from the application of gate pulse. It

is part of the device's total turn-on time and determines the maximum switching frequency the device can handle safely.

3) Turn-on Switching Current Gradient ($di/dt_{(on)}$) and Voltage Gradient ($dv/dt_{(on)}$): The turn-on switching current gradient $di/dt_{(on)}$ is the slope of I_C during its rising edge, measured typically at 50% of the nominal current. Whereas, $dv/dt_{(on)}$ is the slope of the falling edge of V_{CE}, measured at 50% of the nominal voltage. The gradient values indicate the switching speed of the device and these parameters are key contributor of parasitic ringing and EMI in a device switching process.

4) Turn-on Switching Energy Loss (E_{on}): The Turn-on Energy loss is the integral of the instantaneous product of I_C and V_{CE} within the time interval of t_3 and t_4 in Figure 1.5. t_3 marks the time when the rising edge of V_{GE} hits 10% of its nominal value and t_4 is the time when the falling edge of V_{CE} reaches 3% of its nominal value. E_{on} can be mathematically expressed with equation 1.5. E_{on} partially contributes to the total switching losses of a device and is typically one of the largest source of losses in a high frequency converter application.

$$E_{on} = \int_{t_3}^{t_4} V_{CE} \times I_C \times dt \tag{1.5}$$

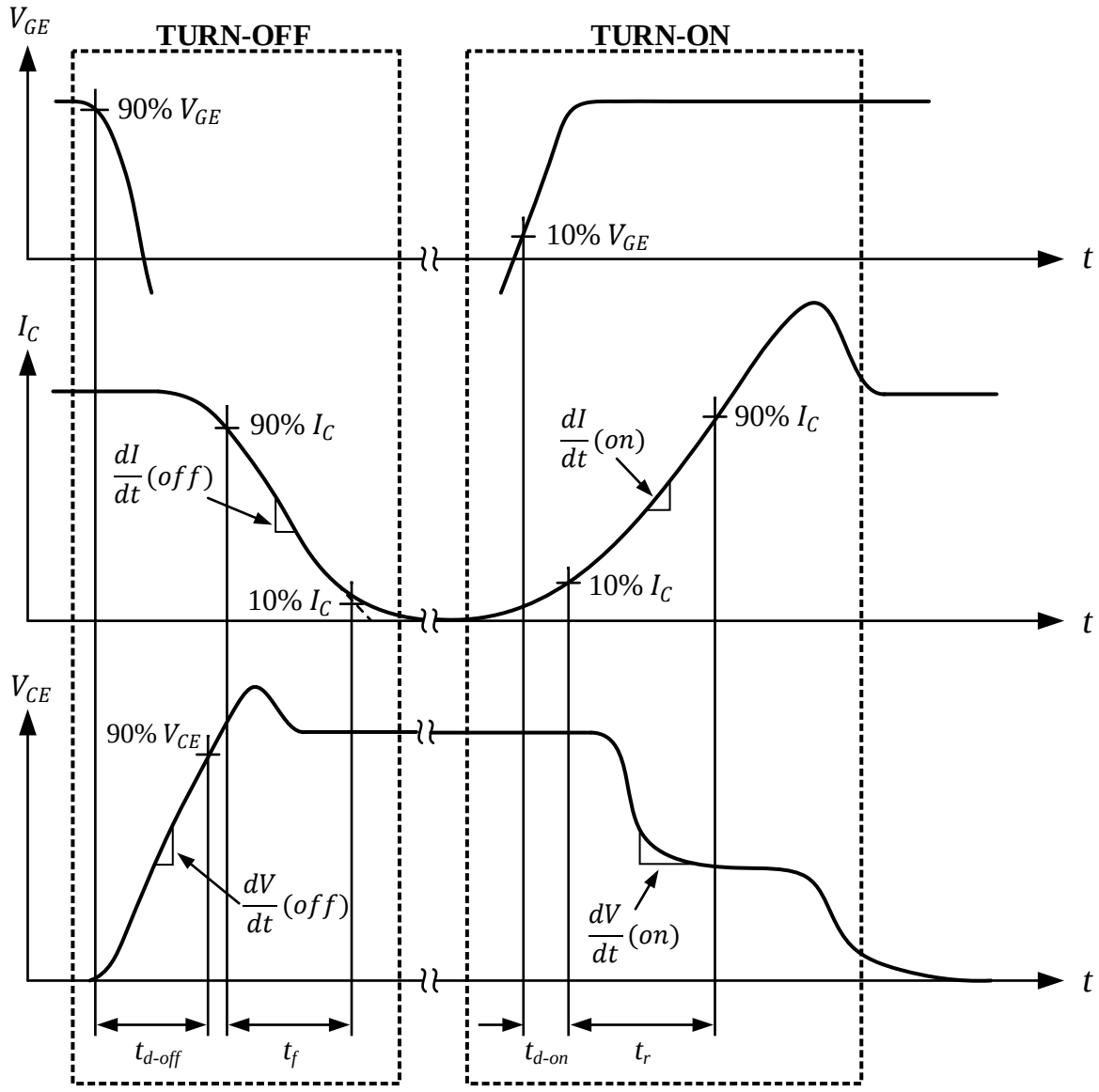


Figure 1.4 Definition of semiconductor switching time [45].

1.3.2 Turn-off Characteristics

In this section, the key switching parameters that represents a device's turn-off characteristics are discussed in details. These parameters are also labelled in Figure 1.4 and Figure 1.5.

1) Current Fall Time (t_{fall}): It is the time taken by I_C to fall from 90% to 10% of the nominal current. This parameter is an indication of how quickly the collector current can become

zero. It contributes to the total turn-off time and partially limits the maximum allowable switching frequency for the device.

2) Turn-off Delay Time (t_{d-off}): The time interval from V_{GE} dropping to 90% of the nominal gate voltage to V_{CE} rising to 90% of its nominal value is t_{d-off}. A measure of t_{d-off} specifies the response time of the device turning off with withdrawal of gate drive pulse. It is part of the device's total turn-off time and a key factor in determining the maximum allowable switching frequency.

3) Turn-off Switching Current Gradient ($di/dt_{(off)}$) and Voltage Gradient ($dv/dt_{(off)}$): The turn-off switching current gradient $di/dt_{(off)}$ is the slope of I_C during its falling edge, measured typically at 50% of the nominal current. Whereas, $dv/dt_{(off)}$ is the slope of the rising edge of V_{CE}, measurement at 50% of the nominal voltage. The gradient values indicate the switching speed of the device and these parameters are key contributor of parasitic ringing and EMI in a device switching process.

4) Turn-off Switching Energy Loss (E_{off}): The Turn-off Energy loss is the integral of the instantaneous product of V_{CE} and I_C within the time interval of t_1 and t_2 in Figure 1.5. t_1 marks the time when the falling edge of V_{GE} hits 90% of its nominal value and t_2 is the time when the falling edge of I_C reaches 1% of its nominal value. E_{off} can be mathematically expressed with equation 1.6. E_{off} in addition with E_{on} constitutes the total switching losses of a power semiconductor device and is typically one of the largest source of losses in a high frequency converter application.

$$E_{off} = \int_{t_1}^{t_2} V_{CE} \times I_C \times dt \tag{1.6}$$

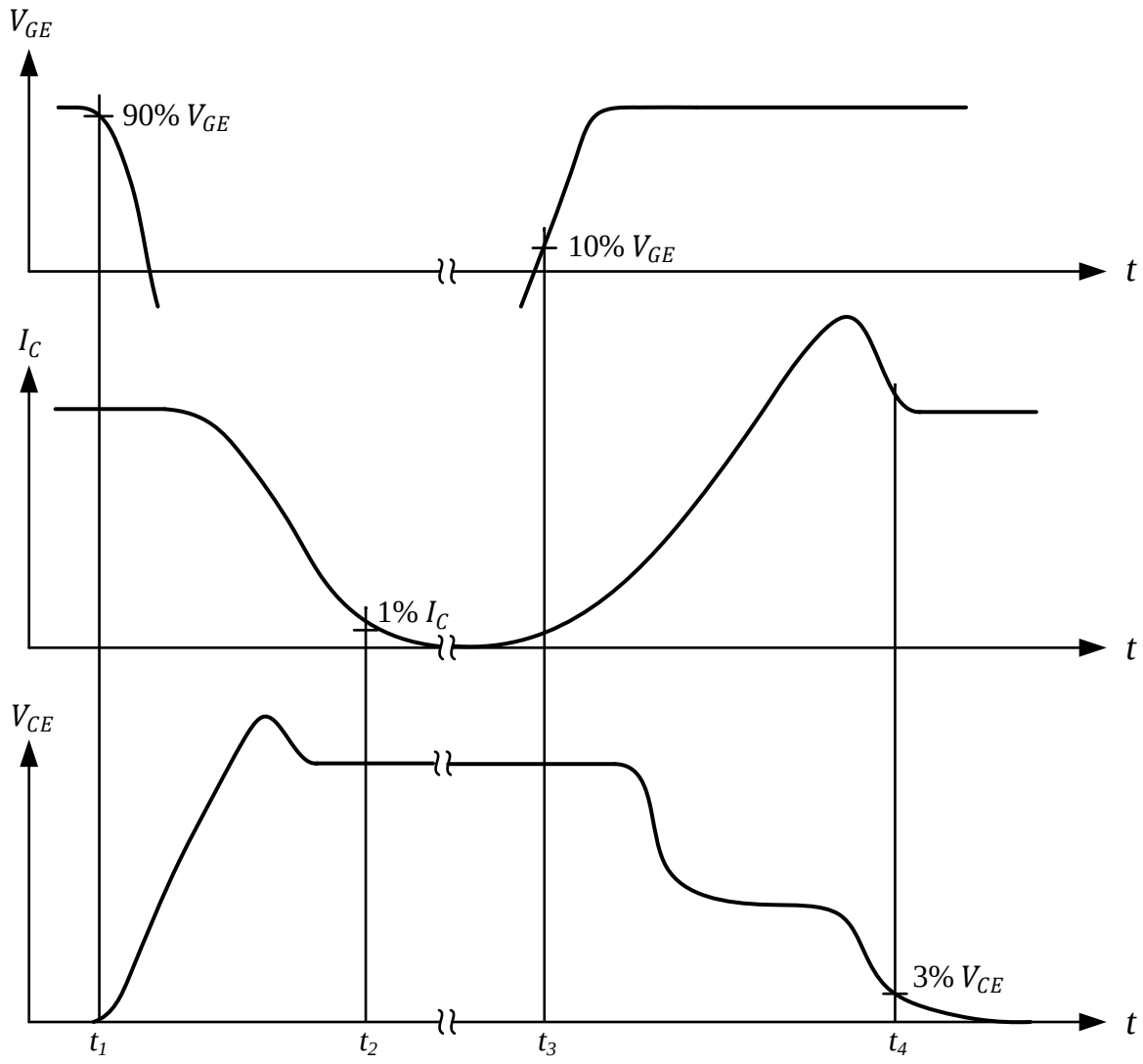


Figure 1.5 Definition of semiconductor switching energy [45].

With these data in hand, a power electronic designer can quantify the switching performance of power semiconductor devices and select a right device for a particular PE converter design. In a nutshell, the switching results act as a guideline for selection of switching frequency and dead time, choice of thermal management and efficiency estimation for PE applications.

1.4 Semiconductors in converters

The fundamental structure of modern power electronic converters is a Switching Block/Cell. As seen in Figure 1.6, a basic switching cell includes a diode (D), semiconductor switch (S), current source (I) and voltage source (V). In most cases, the current source is an inductor and the voltage source is a capacitor. The semiconductor switch, which can be a MOSFET, IGBT or any other switching device, is typically paired with a diode to provide current commutation during the switching process in hard switching conditions.

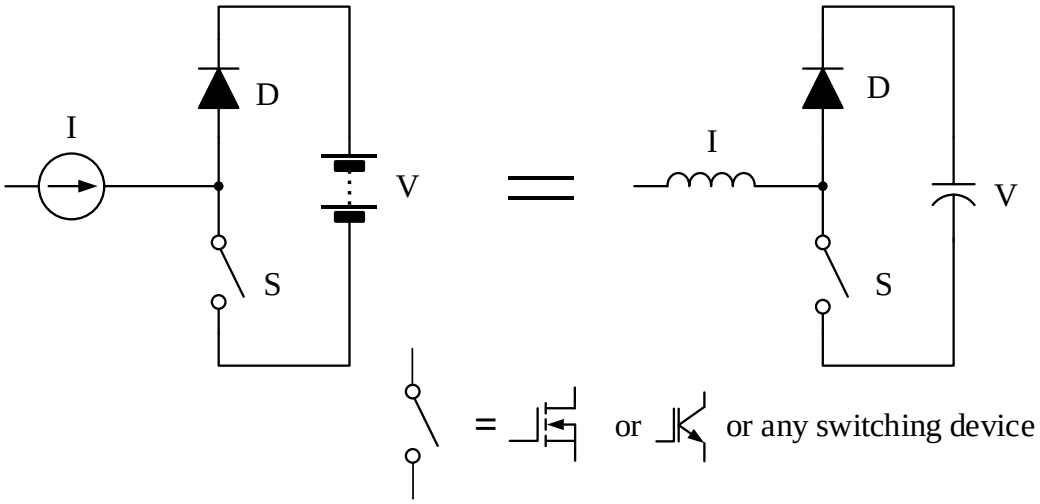


Figure 1.6 Basic switching cell topology.

Based on the position of the switching device in a typical switching cell, the cell can be configured as two basic structures, P-cell and N-cell. For a P-cell, the switching device is connected to the positive terminal of the voltage source whereas in an N-cell it is connected to the negative terminal of the voltage source or capacitor [46], [47]. In all modern power electronic converters, at least one switching cell can be found. The switching cells present in the classical dc-dc converters i.e. buck, boost and buck-boost as well as an inverter are identified in Figure 1.7. Each of these topologies can be represented with P-cell and N-cell circuits and discussed elaborately in [47].

However, for inverters it is not always straightforward to identify a switching cell because the diode is in parallel with another switch and the inductor is shared by multiple switching cells.

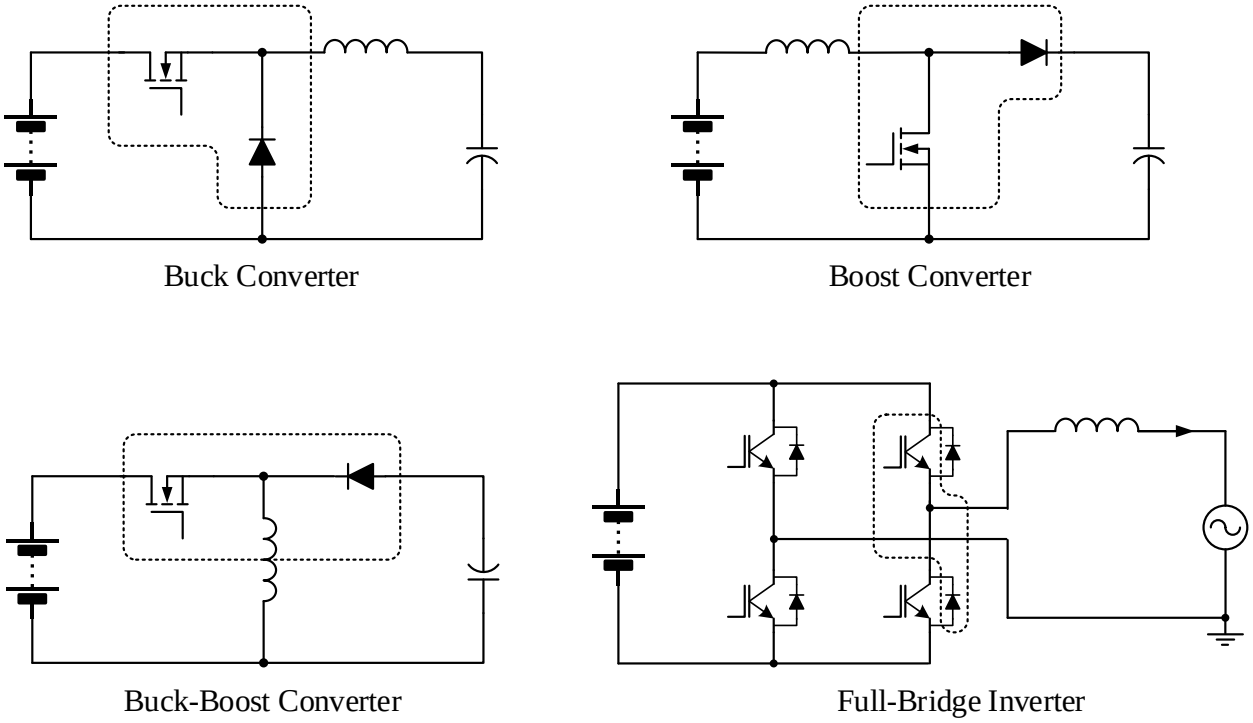


Figure 1.7 Basic switching cells in power electronic converters.

The behavior of the switching device affect the switching performance of the diode, and the operational behavior of the diode reflect back to the switching device. Since their dynamic behaviors are interrelated, it is useful to define a switching cell for estimating switching and conduction losses in a converter. The study of the switching cell reveals the comprehensive switching behavior of the devices concerned.

1.5 Overview of Double Pulse Tester

1.5.1 Basic Topology

A common application of a power semiconductor device is clamped inductive switching [15],[48],[49]. Since a Double pulse tester (DPT) emulates this typical application, it is a widely accepted test system to evaluate the dynamic performance of a switching cell. The DPT test circuit shown in Figure 1.8 closely represents a phase-leg of voltage source converter. The semiconductor device under test (DUT) is tested as a lower side device along with a freewheeling diode (FWD) as the upper (high) side device. Many a times, discrete IGBTs or MOSFETs with anti-parallel diode are used in both positions, where the anti-parallel/body diode of the upper side device plays the role of a FWD and the low side device is the DUT for the switching test.

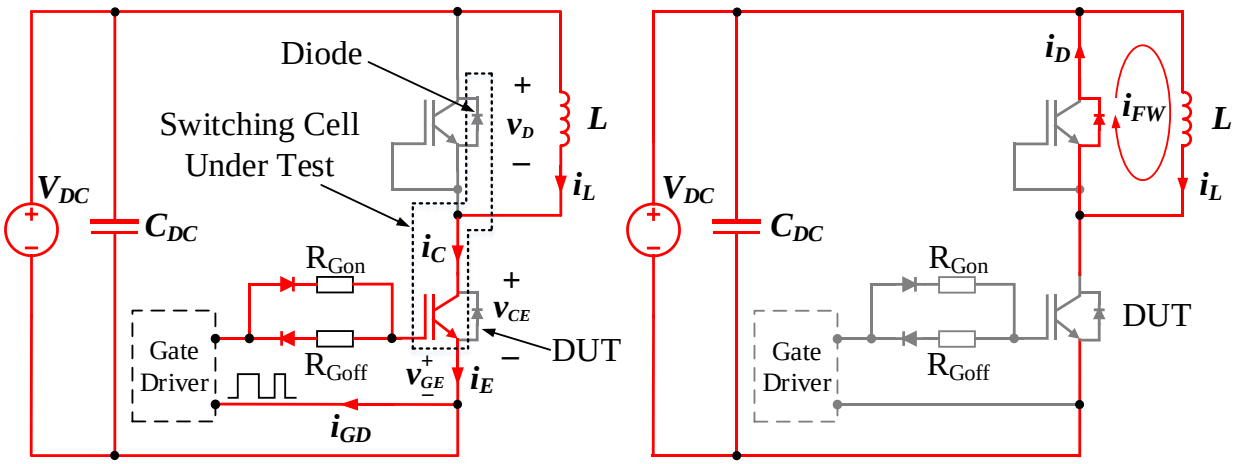


Figure 1.8 DPT dynamic test circuit with inductive load: (a) DUT ON and (b) DUT OFF.

An N-cell configuration is typically chosen for the test circuit because placing the DUT in the lower side simplifies the gate drive circuit due to ground referenced gate signal. The converter circuit is relatively immune to supply noise and gate drive noises in a ground referenced gate drive circuit.

Table 1.2 Definition of parameters used in Figure 1.8 and Figure 1.9

Parameter	Description	Parameter	Description
V_{DC}	High Voltage DC Supply	C_{DC}	DC link capacitor
v_D	Voltage across diode	L	Load inductor
v_{CE}	DUT collector–emitter voltage	R_{Gon}	DUT Turn-on gate resistance
v_{GE}	DUT gate–emitter voltage	R_{Goff}	DUT Turn-off gate resistance
i_C	DUT Collector current	i_L	Current through load inductor
i_E	DUT Emitter current	i_D	Current through diode
i_{GD}	Current through gate driver	i_{FW}	Freewheeling current
V_{TEST}	Test voltage	I_{TEST}	Test current

1.5.2 Principles of Operation

The operating principle of the DPT system in Figure 1.8 can be briefly described with the aid of characteristic switching waveforms in Figure 1.9. The figure shows the waveforms of interest i.e. the gate voltage, collector-emitter voltage, load current and collector current under double pulse operation. Two pulses with a delay time between them are sent to the gate of DUT through a suitable gate driver. At time t_0, the first pulse turns 'on' the DUT and it is held on until I_C reaches the desired test current level. At time t_1, the gate pulse is shut off and the turn-off switching characteristics of the DUT are captured. From time t_1 to t_2, the DUT is held off and this is when the inductor current I_L retreats from the DUT path and flows through the upper side diode creating a freewheeling current. The delay time between the two pulses i.e. the freewheeling time should be long enough to damp out the parasitic ringing in V_{CE} and I_C before the DUT is switched on again. However, it is short enough to keep the inductor current fairly constant in this period. The

choice of high load inductance also ensures I_C does not drop considerably. At time t_2, the second gate pulse turns the DUT on again and this time the turn-on characteristics of the DUT are recorded. The switching on of the DUT causes the FWD to undergo reverse recovery. At this time, both the reverse recovery current and the inductor current flow through the DUT. In practical testing scenarios, an overshoot is noticed in the device current I_C during this process. The time interval t_2 to t_3 is kept long enough for any possible switching ringing to subside and short enough to ensure I_C stays within the device's safe operating limits. At time t_3, the gate is forced low and the device is turned 'off'. This process is repeated under different test conditions, in this way the device does not heat up and the characterization can be performed under desired and controlled junction temperature condition.

The device voltage and current waveforms are measured using a high bandwidth high voltage probe and current monitor respectively. The specifications of the probes used for the testing as well as factors behind the choice of instrumentation for DPT is elaborately discussed in Chapter 4. The raw test data for all necessary channels that represent the switching waveforms are then extracted from the oscilloscope to a PC for further processing and analysis. Multiple tests are performed on a particular DUT with different gate resistances at different voltage, current and temperature levels to derive its typical switching curves. In order to control the *di/dt* and *dv/dt* of the DUT, the gate resistances (turn-on and turn-off) are kept adjustable for limiting the current responsible for charging up the input capacitance of the DUT.

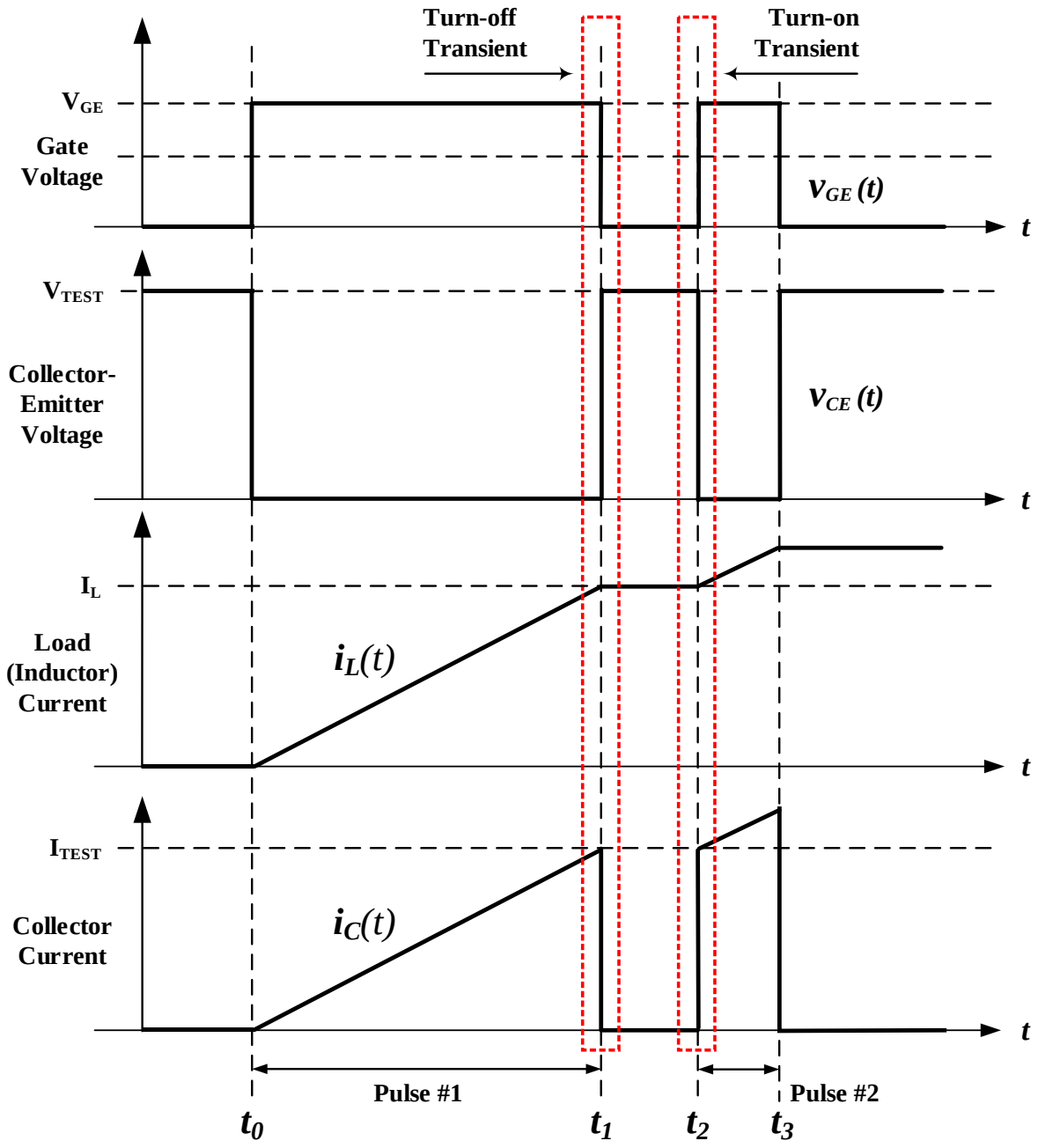


Figure 1.9 Ideal waveforms of double pulse switching test.

1.6 Literature Review

A double pulse test is a widely accepted method for switching performance evaluation of power semiconductor devices. Unlike static characterization, which is performed by industrial grade test equipments such as curve tracers/semiconductor device analyzers, there is no such commercially

available instrumentation from test equipment manufacturers for dynamic switching characterization. Industries and academia customize and design their own DPT setups based on the technical resources available to them and also considering the type of device to be tested. Some of the DPT setups mentioned in technical literatures are briefly discussed in this section.

In technical literature [50], the design principles and PCB design recommendations for implementing a double pulse test prototype to investigate the switching behavior of SiC MOSFET (Cree's C2M0080120D) in a TO-247 package are described. The literature highlights the different parasitic element associated with the DPT circuit and presents the effect of these parasitic components on the DUT switching characteristics through simulation results. For the hardware implementation stage, it discusses the circuit layout techniques adopted to minimise effect of parasitic elements on the switching characterization results.

A relatively broader picture of the dynamic characterization test process is presented in [51] and some of the key topics of a DPT, including components and layout design, instrumentation selection criteria, considerations during measurement, grounding effects as well as data processing are discussed. The authors provide an overview of the entire double pulse test process and the setup identifying the key components involved and their individual functions. The design criteria of main DPT components such as load inductor and DC capacitor bank are described. The power stage and gate driver circuitries are separated and modularized to allow DPT testing regardless of specific topologies. Like most of the literatures in this domain, this paper also highlights the importance of parasitic impedance minimization in PCB layouts to obtain test results that are genuine representation of the DUT's switching performance. Thereafter, the authors discuss the latest voltage and current measurement techniques for DPT as well as list the latest high bandwidth probes that can capture the high-speed switching transients during the test with adequate fidelity.

Experimental results are shown for double pulse tests conducted on a phase-leg module built with 1200V/500A SiC MOSFET and SiC Schottky diode. The authors also propose a method for switching loss evaluation of WBG devices in phase-leg configuration.

The switching characteristics of a WBG based 1200V, 35A SiC MOSFET in [15]. In this literature, the authors provide a brief description of the double pulse test process followed by presentation of simulation and experimental results. Simulation of double pulse circuit is performed in LT-Spice simulation platform and both turn-on and turn-off switching characteristics are presented in addition to a table of switching loss figures for different test conditions. The DPT hardware is realized with a six layer PCB consisting of SiC MOSFETS, DC filter capacitors, gate driver and an eight bit PIC microcontroller. Some key attributes of the gate driver design and component selection are presented. The authors also study the temperature dependent switching behavior by attaching the DUT to a hot plate. Finally, the DPT results are analysed to highlight the superiority of WBG devices.

A different approach is taken in [52] for designing a Multifunctional DPT for Cascode GaN Devices. The authors propose a tester that builds on a conventional DPT but is capable of carrying out the double pulse test and diode reverse recovery characterization on the same board without the need for moving the DUT from one setup to another. The tester is able to characterize device turn-on and turn-off transition like a conventional tester but in addition, it is also capable of measure the dynamic on-state resistance of the GaN devices in both hard and soft switching conditions (with use of additional zero-voltage transition circuitry for soft switching). Like other literatures, this work also specifies the importance of a compact PCB layout for DPT with a focus of keeping the parasitic inductance of the gate loop and high-frequency power loop to the lowest level possible. This will limit the chances of gate voltage ringing, unwanted triggering of the device

and overshoot on device voltage. The authors uses a finite-element analysis (FEA) tool, ANSYS Q3D package to extract and quantify the loop inductances and parasitic capacitances in the PCB layout. The functions of the proposed tester are validated with tests on a cascade GaN device.

A conventional DPT i.e. a clamped inductive switching circuit is implemented in [48] to test a 600V normally-off GaN-on-Si transistor. A test bench is constructed to house the DPT circuit, oscilloscope, high-voltage source, pulse generator and auxiliary unit with a computer controlling the entire setup. The test bench is made of plastic to avoid any parasitic capacitive coupling path. The device temperature is controlled with air flow around the device and monitored using an infrared thermometer. The paper also discusses techniques for measurement of gate charge and on-state resistance. The results obtained from the double pulse measurements is used as a basis to design a GaN based DC/DC converter.

Both static and switching characterization of a SiC JFET and SiC MOSFET device are covered in [53]. As a common practise, the author chooses the double pulse test circuit for the switching characterization because switching under clamped inductive load is the most common commutation mode for power devices in a pulse width modulated, hard-switching type converter. The ideal MOSFET switching behavior is studied along with a discussion on the effect of non-idealities on the high-speed switching waveforms. From the description of the DPT setup, it is noted that the double pulse signals are generated using an Agilent waveform generator and the test setup is powered by external power supply units. The test setup does not include any thermal system to conduct characterization tests under different temperatures. It requires manual configuration of the test equipments for each test condition. Finally, the characterization result is compared with simulation results in order to comment on the accuracy of the spice models.

There are some double pulse evaluation boards commercially available from semiconductor device manufacturers. EVAL-IGBT-650V-TO247-4 [54] from Infineon is an evaluation board for 1200V IGBTs in TO-247 packages, and with either three or four leads. It allows double pulse tests for switching voltages and currents upto 650V and 150A respectively. The board consists of the capacitor bank, load inductor and has connectors for external connection of signal generators, high voltage and auxiliary power supplies. The presence of probe tip adaptors facilitate easy connection of probes. A heat sink is connected to the DUT for temperature dependent dynamic testing. Moreover, this board can be configured as step-down or step-up DC/DC converter and used in continuous operation due to the basic phase-leg topology. This evaluation board is presently listed for sale in Mouser Electronics website for a unit price of $884.75.

GA100SBJT12-FR4 [55] from GeneSiC Semiconductor is a Double Pulse Switching board designed for performing switching tests on Si and SiC power transistors. The board is capable of testing devices upto 1200V and 100A. The board comes with a capacitor bank comprised of twenty 1µF, 630V capacitors and connection pads for external component connection. The DUT, freewheeling diode, external inductor and gate driver have to be soldered directly on to the board by an user. This evaluation board does not provide any provision for DUT case temperature adjustment. Like most of the conventional setups, the high voltage has to be supplied to the test board from an external power supply through a coaxial connection. This evaluation board is presently listed for sale in Mouser Electronics website for a unit price of $388.72 but for a minimum order quantity of 25 boards.

PGA26E07BA-SWEVB008 (~800W) and PGA26E19BA-SWEVB008 (~400W) [56] from Panasonic Semiconductor Solutions Co., Ltd. are half-bridge evaluation boards for evaluating the switching characteristics of Panasonic make X-GaN power transistors. The maximum DC input

voltage is 410V. The board consists of X-GaN Power Transistors in SMD package, Gate Driver IC and general purpose Half Bridge Isolator. This evaluation board offers a platform for testing and developing power circuits using only Panasonic make X-GaN devices. It has to be accompanied by external DC power supply units and Pulse generator for double pulse testing and does not come with any provision for adjusting DUT case temperature. The board supports continuous power supply test depending on the thermal design. This board can be used as a reference design for PCB layout and gate driver circuit. However, it cannot be considered as an universal setup for testing devices of different specification and packages. The evaluation board is listed in mouser electronics for an unit price of $585.12.

An application note available online from CREE [57] describes the design principles of a SiC MOSFET Double Pulse Fixture. The test fixture contains a test socket for the DUT, gate driver, capacitor bank, freewheeling diode and a tightly integrated two stage current transformer. This document is mainly focused on the design considerations of the double pulse test power circuit and gate driver. It shows the tester schematic, photos, PCB layout, bill of materials, test waveforms and provides recommendation for distortion-free measurement of switching waveforms for SiC devices. However, this test fixture is not commercially available from the manufacturer and not listed in any electronic component distributors' website.

GS66508T/GS66516T-EVBDB [58] evaluation board from GaN Systems Inc. includes 650V GaN Enhancement-mode HEMTs (E-HEMTs), half-bridge gate drivers, isolated power supplies and optional heatsink to form a continuously operated half bridge power stage. As other evaluation boards mentioned earlier, this serves as a reference design for the main DPT power board for the latest low-footprint, surface mount GaN devices. The two GaN devices along with their gate drive circuitries are implemented in a daughter board, which can be plugged into a universal mother

board GS665MB-EVB (sold separately). The mother board consist of connection pads for external load inductor connection, high voltage DC and auxiliary power supply units connection and a PWM control & dead time circuit. Provision is kept for attaching a heat sink with the switching devices in the daughter board but no such thermal arrangement is provided that allows temperature adjustment.

All the evaluation boards listed above consist the main half-bridge power stage, which represent the main DPT power circuit. These boards are designed by power semiconductor device manufacturers, hence can serve as a good reference while designing the power and gate drive circuit layout for testing the latest WBG semiconductors. However, the power board is only one of the key components amidst the several test elements involved in the overall double pulse testing process. These boards have to be accompanied with additional support equipments to conduct the double pulse testing. To the best of the author's knowledge, a complete DPT solution that can cover testing, recording and data processing aspects of switching characterization is not yet available from the test equipment manufacturing industry.

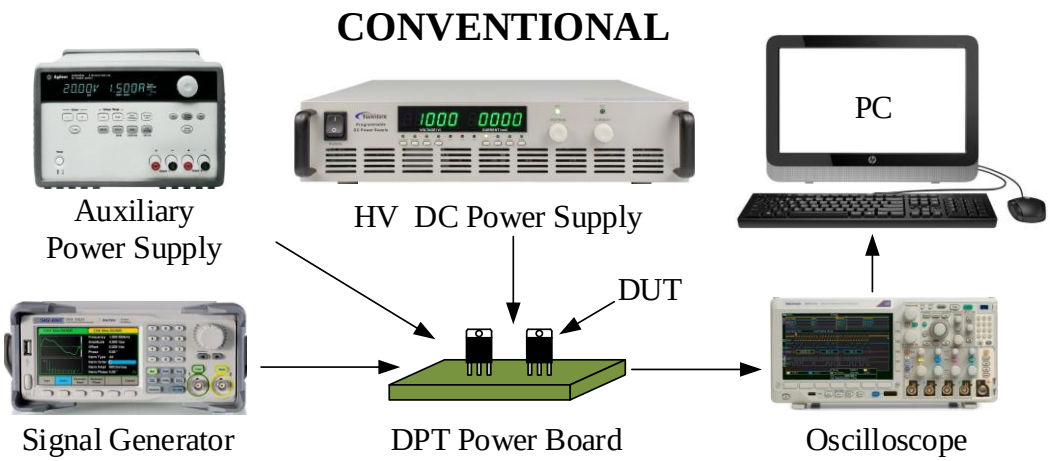
1.7 Motivation of the Thesis

A typical datasheet of a power semiconductor switch provides switching results for a particular test condition. However, the operating condition of a device in a real life target application may be different from the datasheet specified test condition. In this scenario, a designer requires a fully equipped dynamic test bench to conduct the switching test in a desired test condition. A DPT is a widely used setup for evaluating the switching behavior of power semiconductor devices. For conventional DPTs, the test control and data processing operations are done manually. However, it is a tedious, time-intensive process to perform these tests under different permutations of test parameters and thereafter analyze the experimental data manually. Although the switching event

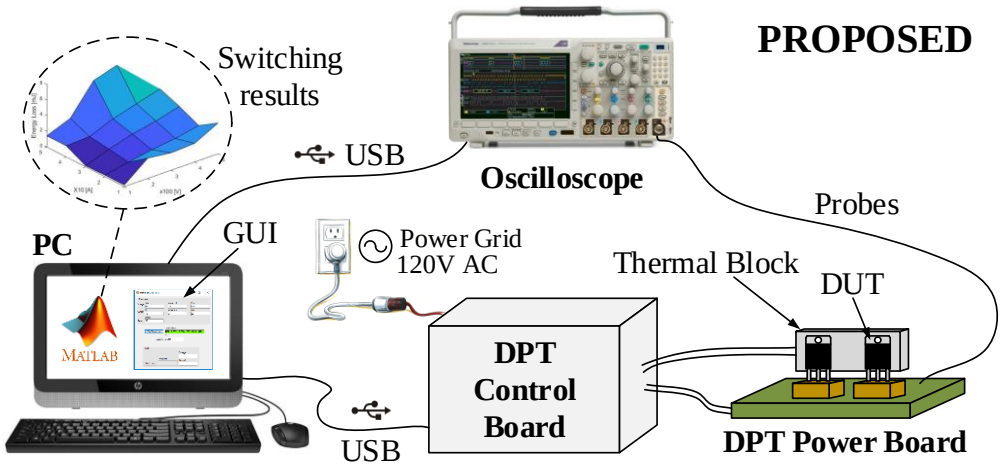
occurs in fraction of a second, manually setting up the test bed multiple times for each test conditions, extracting the post-test raw data and thereafter processing the raw data to obtain switching characteristics involve considerable amount of time and effort. An automatic test control and data processing system needs to be developed to minimize user interaction in the overall test process.

Moreover, conventional manually operated DPT systems, as discussed in Section 1.5, are expensive and consume substantial bench space due to involvement of several peripheral support equipments such as signal generators and bulky power supply units (PSU). To make the overall dynamic characterization setup compact and economic, the peripheral equipments need to be replaced with alternate solutions but to perform the same functions.

As mentioned in section 1.5, only DPT evaluation power boards are commercially available from semiconductor device manufacturers. A complete DPT solution is required that covers testing, recording and data processing aspects of switching characterization. However, to the best of the authors' knowledge, presently there is no such complete DPT system commercially available from any test equipment manufacturers. In view of the above discussion, an innovative DPT solution is proposed. Figure 1.10 shows a comparison between conventional and proposed DPT setup.



(a)



(b)

Figure 1.10 High-level comparison between (a) conventional and (b) proposed DPT setup.

To summarize, the motivation of this thesis is to develop a compact, cost-effective, fully automated, universal test platform for dynamic characterization of power semiconductor devices. It will also be a complete DPT solution for monitoring, measurement, recording and processing the switching data. The switching loss data obtained using this testing system can be used to generate switching time and loss databases for widely used semiconductor devices. These databases can be linked with simulation platforms to obtain more practical simulation results. It

will help engineers to create, optimize and validate power semiconductor devices models in power electronic simulation platforms such as PLECS and power system electromagnetic transient (EMT) simulation software like PSCAD etc. Due to availability of switching data with variation of operating temperature, thermal models can be developed. The thermal simulation results can provide information on converter loss and increase in device junction temperature. These results will greatly facilitate an user with heat sink design for a particular application since these information cannot be obtained easily from a typical datasheet.

Research Objective

The proposed research work is focused on integrating power electronics, control, communication and data processing techniques to develop a novel test bench that can characterize the dynamic performance of the existing as well as the latest power semiconductor technologies. This compact, automatic test setup will help engineers to quantify the switching behavior of power semiconductors effortlessly. In this phase of continually evolving semiconductor industry when new devices are regularly launched in the market from numerous manufacturers, this kind of test setup will be required in both academia and industry for understanding the potential of these devices in a lab environment before implementing them in real life applications. There is a considerable amount of human involvement in the power semiconductor conventional switching characterization methods. Hence, the critical research objective of this thesis is to explore ways of establishing automation in all the major test segments i.e. test control, double pulse testing, data acquisition and data processing in order to save labour and reduce the overall testing time.

Methodology to meet research objectives:

- Conduct a thorough literature review to learn about the recent work in the area of proposed research. Study about the existing dynamic characterization setups, any recent developments published in technical literatures or commercially available products from the semiconductor/test equipment manufacturing industry that can shape the trajectory of the proposed research work.

- Plan the hardware with an intention of scaling down the overall test setup footprint with respect to conventional setups, consider possible elimination of any heavy equipments involved in the test process and implement alternate solutions for carrying out same functions. Use voltage, current and temperature sensors to establish closed loop control of test bed, employ power electronic converters as power supply units and control pulses with help of logic circuitries.

- Design a control system to exercise necessary control on the hardware elements, prepare test bed, conduct test as well as co-ordinate the test process. Develop a GUI to allow interaction between an user and the control system. Establish communication between control system and other key units involved in the testing such as microcontroller and oscilloscope.

- Amalgamate the hardware and software elements systematically. Thereafter subject the prototype through series of open loop and closed loop tests to assess the performance of individual modules and finally ensure the system is capable of conducting high voltage double pulse tests.

- Characterize power semiconductor devices in a wide range of test conditions to demonstrate the stable operation of the proposed universal and automatic test setup.

- Develop a program to methodically process the raw test data, calculate values of different switching parameters as per relevant switching definitions in order to generate usable characterization results.

1.8 Organization of the Thesis

This thesis is organised in six chapters, a brief description of the chapters is provided below:

- **Chapter 1: Introduction** – This chapter presents background information related to the research work described in this thesis, review of literature and research objectives. Different semiconductor technologies are reviewed, the importance of dynamic characterization of semiconductor devices is discussed and key switching parameters are defined. Thereafter, the topology of a Double Pulse Tester (DPT) is introduced and its operating principles are explained. A comprehensive review of current literatures is presented to discuss pros and cons of existing conventional DPTs and research objective of the thesis is formulated accordingly. This chapter is concluded mentioning the thesis contribution.

- **Chapter 2: Hardware design** – This chapter focuses on the hardware implementation techniques of the Automatic DPT. The objective behind the segregated, modular design of the power and control modules is addressed. The detail design criteria of individual key units of both the control and power modules is presented and their contribution in achieving test automation is discussed. The PCB layout design considerations are discussed because the physical layout highly affects the switching test results.

- **Chapter 3: Controller design** – In this chapter, the control architecture of the Automatic DPT is introduced. The design principles of the PC based test control software and its Graphic User Interface (GUI) is elaborately discussed. Thereafter, the interaction between the control system, on-board microcontroller and other key elements of the DPT system is explored. Control flow chart and block diagrams are used to depict the systematic functioning of the control and power board units for seamless and automatic operation of the proposed DPT system.

- **Chapter 4: System Evaluation** – The specification and special technical requirements of the measurement tools such as probes, sensors, and oscilloscope for accurate recording of dynamic characterization results are discussed in detail in this chapter. The operation of the Waveform Analysis Tool (WAT), which is developed in MATLAB to process the vast amount of data captured during double pulse tests, is reviewed.

- **Chapter 5: Experimental Verifications** – The complete DPT experimental setup is described in this chapter along with presentation of various experimental results. The design principles of the automatic test bed are verified and validated by demonstrating its successful operation. The same switching cell is implemented in a boost converter and the switching results from the converter is compared with that obtained from DPT for similar test condition. Both Si and WBG devices are characterized by changing the DPT power interface board thereby illustrating the universal design of the setup. Oscilloscope waveforms, plots and figures generated from the processed data are presented and analysed to understand the dynamic behavior of the switching cell.

- **Chapter 6: Conclusion and Future Work** – This chapter summarizes the contribution of this thesis as well as key conclusions that are drawn from the studies conducted. It also discusses some of the potential future extensions.

1.9 Research contributions

This thesis proposed an innovative design of a power semiconductor dynamic characterization tool that is cost-effective, compact, automatic and user-friendly. The major contributions of this thesis is summarized below:

- A thorough literature review has been conducted to gather background information on the conventional and existing device characterization setups used in both the academic and industrial domain. Their pros and cons are discussed and the shortcomings of the conventional setups are narrowed down in order to conceive the original research idea and present the motivation behind this research work.

- An innovative test bench is designed and implemented that is capable of automatically conducting dynamic characterization tests on a device under test following an user-specified test routine. The prototype built to materialize the research idea is capable of testing devices up to 1000V, 60A and 250°C. The design principles have been validated by successfully characterizing a TO-247 style, 3 pin Si IGBT and TO-227 style GaN FET.

- Considering the vastness of raw data originating from tests conducted under numerous permutations of test parameters, a smart data processing program is developed in MATLAB to scan through the raw data and identify key points for calculating switching results. Raw data obtained from tests conducted on the proposed test bench is processed using this tool and results are presented and discussed.

- The results of this research work will provide a new understanding of the trade-offs involved in the design process of an universal test bench. The hardware designs produced out of this research work will serve as a good reference for physical layout design of PCB, gate drive circuitries in a power electronic converter. This work will also create a platform to attract discussion, criticism and learn the views of other experts in this domain.

- This research has fuelled other researches in this domain. The dynamic characterization results obtained from this test platform have been utilized by fellow researchers to develop thermal and transient models for switching cell loss estimation in Electromagnetic transient simulation software PSCAD [17]. As opposed to a lossless model, this new model closely emulates the performance of a real semiconductor in terms of its loss behavior. The research output has been transferred to local industry such HVDC research centre for enhancing the semiconductor models in the PSCAD library. The research output has been published in relevant literatures as well.

Chapter 2 Hardware Design of Automatic Tester

The objective of this chapter is to introduce the design considerations and methodologies adopted for the hardware realization of the proposed Double Pulse Tester. The entire design is fragmented into multiple units for ease of implementation, testing and debugging. The component selection for each these units are guided by the objective of designing a compact and automatic test bench. The impacts of the parasitic elements on the physical layout of the power stage are investigated and PCB design is optimized to obtain characterization results that reflect the true performance of the DUT.

2.1 System Architecture

The overall double pulse testing system is designed with a multiple module approach for ease of implementation, testing and debugging. These modules or support units by performing their individual tasks at pre-programmed time slots, build up an intricate network of routine actions through which automation is realized in the proposed DPT. A block diagram shown in Figure 2.1, categorizes and tags these support units with their respective functions. The specification and design principles of these individual support blocks are further explored in the sections below.

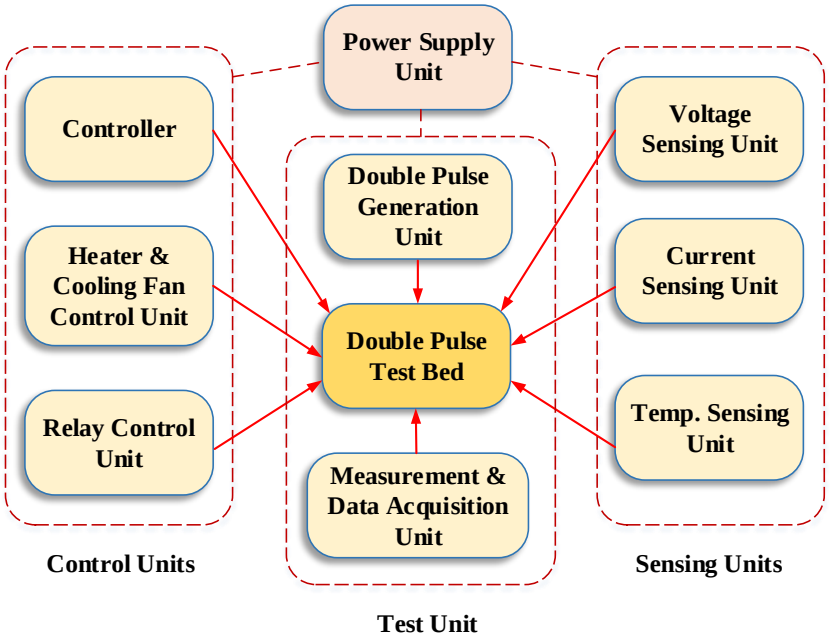


Figure 2.1 Block diagram of peripheral supporting units in double pulse test bed.

The process of obtaining the switching characteristics of a power semiconductor device can be broken down into discrete stages. The first stage involves preparation of the test bed at user-defined test voltage and temperature levels. Once the testing environment is ready, the main switching test is conducted in the next stage by feeding two controlled pulse trains into the gate of the device through a specialized gate driver. The post-test activities include extraction of the raw experimental data from the oscilloscope and thereafter processing the data to obtain facts and figures that describe switching performance of the DUT. The automation in each of these stages mentioned above is achieved through systematic interaction between the key elements associated with each of these stages.

Figure 2.2 shows a block diagram schematic of the proposed automated DPT indicating its key elements. The design considerations behind each of these hardware elements and support units are further discussed.

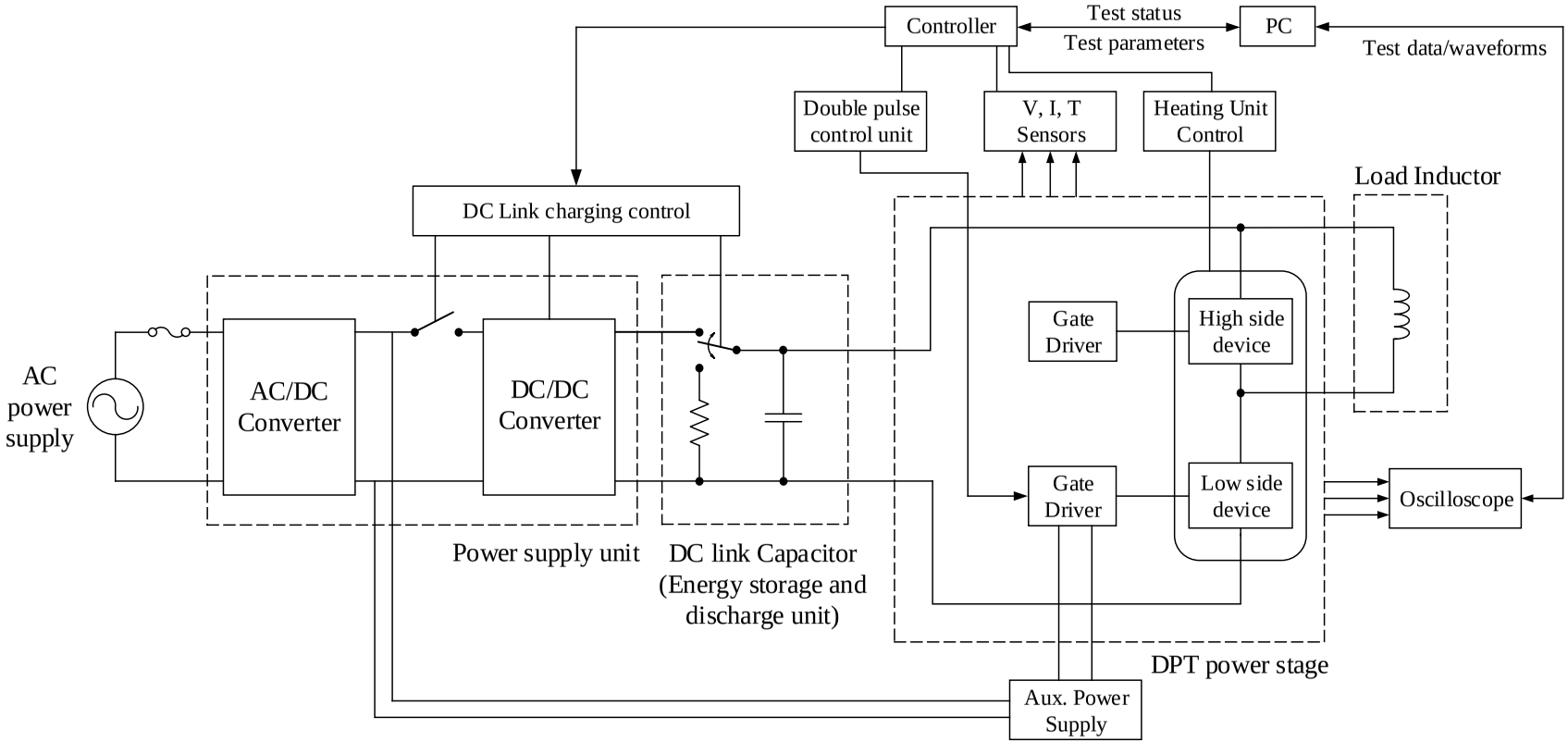


Figure 2.2 DPT test setup schematic.

2.2 Control Board Design

The overall DPT system has been implemented with a mother control board and replaceable DPT power boards. This modular approach facilitates easy debugging and allows freedom in independent designing of the two boards to meet their specific design requirements. The control board is a PCB that houses the power supply units, microcontroller, sensor, logic and relay circuitries. In the subsequent sections, the design of each of these units are explored.

2.2.1 Power Supply Unit (PSU)

One of the key focus in the design process is to make the testing system compact and stand-alone. Conventional setups use discrete DC power supply and Auxiliary power supply units, which consume a considerable amount of bench space and require manual control & configuration for every test condition [12],[15],[49]. In order to eliminate the need for such bulky units, a compact power supply system is designed to power up the main DPT board and its associated control and sensor circuitries. The overall design of the PSU and the units powered by it are shown in Figure 2.3. This compact PSU feeds the entire DPT setup i.e. the high voltage DC link voltage for the switching test, the gate driver, the DUT heating unit as well as the entire control circuitries on the control board including the controller. This makes the DPT system a stand-alone setup that can be installed and operated in any location that has access to a standard 120V AC power source.

An isolated dual output, PCB mount, 30W AC/DC converter (Model: ECL30UD03) is used to rectify the AC mains voltage to obtain 12V & 5V outputs. The 12V is used to power an ultra-small Volgen High Voltage DC/DC converter (Model: VHV12-1.0K2000P) to energize the High Voltage DC Bus up to 1000V for charging the capacitor banks. The availability of a voltage control pin in the High Voltage DC/DC converter facilitates automatic regulation of the converter's output voltage as per the set test voltage by isolated control signals from the microcontroller. The

converter's another useful pin, the ON/OFF pin is used as part of the protection system of the DPT. The microcontroller shuts off the high voltage output through this pin in the event of a fault. The 5V output from the AC/DC converter constitutes the Auxiliary power unit that feeds the microcontroller, sensor & gate drive circuitries, cooling fan and all the relays. The basic technical specifications as well as the key features of the DC/DC converters used in designing the PSU are encapsulated in Table 2.1.

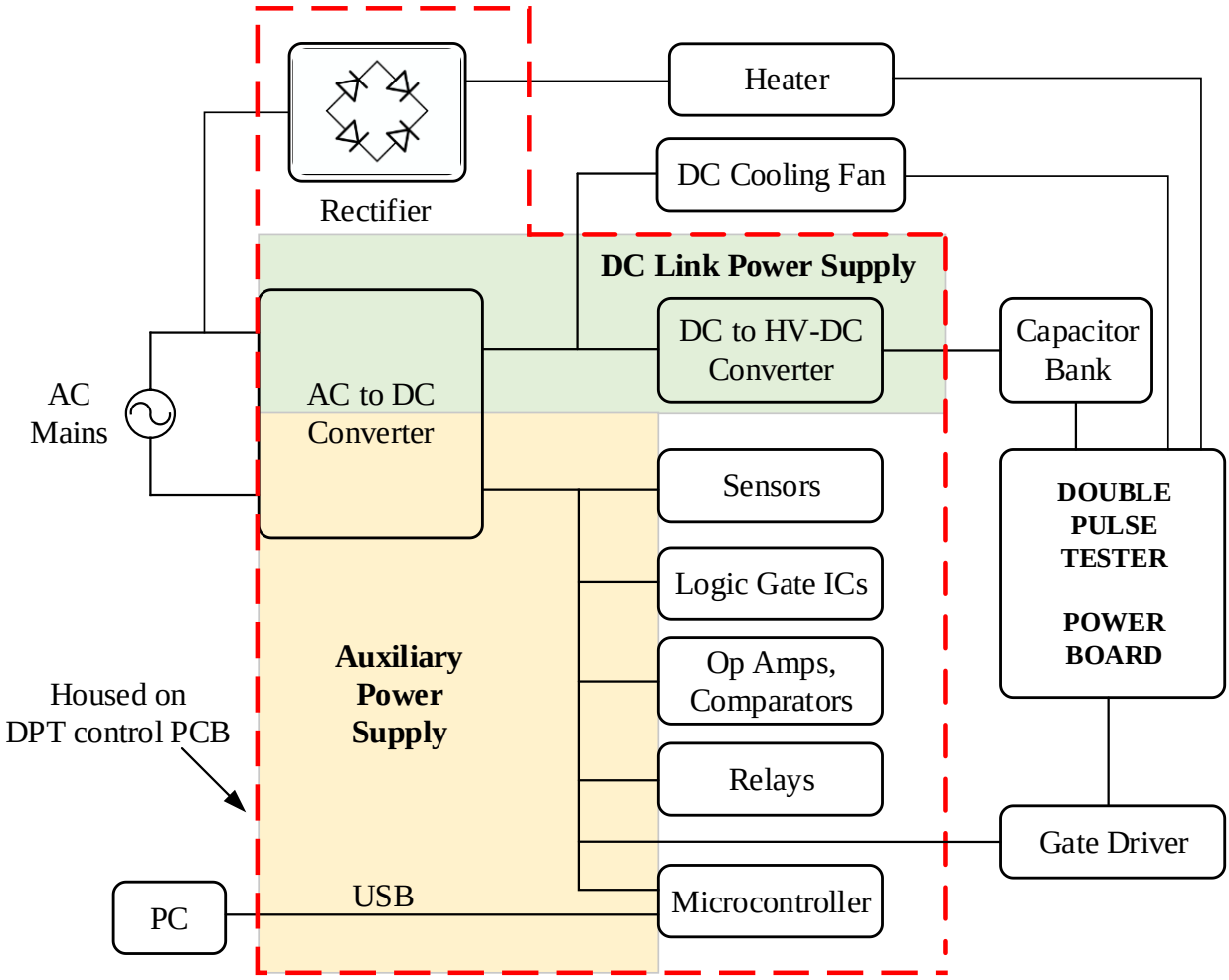


Figure 2.3 Overall design of PSU for proposed DPT.

Table 2.1 Technical specification of DPT PSU converters

Type	Model	Input Supply requirements	Output Power Specification	Salient features
AC/DC Converter	Make: XP Power Model: ECL30UD03	• 85-264 VAC • 0.8A rms at 230VAC • < 0.3W No load Input Power	Total: 30 W Output 1: 15 W (3 A, 5V) Output 2: 15 W (1.3A, 12V)	• Isolated Dual output • PCB mount • Encapsulated • Output power is sufficient to meet power requirements of all connected components
DC/DC Converter	Make: Volgen/ Kaga Electronics Model: VHV12-1.0K2000P	• 10.8 to 16.5 Vdc • 280 mA typ.	Power: 2 W Voltage: 0 to +1000 V Current: 2 mA	• PCB mount • Ultra compact HV supply unit • Output voltage can be regulated by application of external voltage • On/Off Pin allows remote switching on/off of output voltage

2.2.2 Sensor and Control Units

Voltage Control Unit: In conventional DPT setups, the DC link voltage switched by the DUT comes from a separate HV power supply unit. This unit is manually regulated to the desired test voltage before each test. Considering the fact that in a double pulse test a DUT is characterized in a wide range of test voltages, manual configuration of the PSU before every test seems is a crude and laborious approach. In order to implement an automatic voltage setup system, it is essential to read the real time voltage in the power leg of the DPT. The real time monitoring of the DC link voltage will allow the controller to regulate and maintain the voltage at user specified values at all times.

The ACPL-C87A from Avago technologies, which is a precision optically-isolated amplifier is the key component used in the voltage-sensing unit. A resistive voltage divider is used to scale down

the DC-link voltage to suit the 2V input range of the sensor. A differential output voltage proportional to the input voltage is then passed through an amplifier and fed to the analog input pin of the on-board microcontroller. The galvanic isolation of the sensor protect the control circuitries from any possible surges from the power stage.

When an operator inputs a test voltage in the GUI, it is serially communicated to the on-board microcontroller. The controller enables the output of the HV DC/DC converter through its ON/OFF pin. Thereafter, based on the value of the test voltage, it generates a reference and sends PWM signals to regulate the output of the converter through its dedicated output control pin. This initiates the charging of the DC link capacitor bank, the real time voltage read by the sensor is then fed back to the controller to control the charging process. The control signals are terminated from the converter's output control pin when the desired test voltage is established in the capacitor bank.

Current Sensing Unit: The gate pulses for the switching test originates from a signal generator in conventional DPT setups. In the proposed setup, a double pulse control unit (DPCU) is designed and deployed on the control board to replace the function generator. The DPCU automatically regulates the width of gate pulses based on the load current value. Although the pulse is initiated by the controller, analog circuitries are used in the DPCU to terminate the pulses when the desired test current is established in the load. This is why a current sensor is installed at the load leg to feed real time current measurements to the microcontroller. In the proposed DPT setup, the ACS758LCB-100B current sensor IC from Allegro Microsystems Inc. is used to monitor the load inductor current. The ACS758 outputs an analog voltage signal that varies linearly with the DC primary sampled current. The thick copper conductors allow testing at high current values upto 100A. Since the double pulse test involves pulsed switching and not continuous operation, there

is no concern of overheating of the sensor terminals. The terminals of the conductive path being electrically isolated from the signal leads, there is no need for an opto-isolator.

Temperature Control Unit: In the proposed setup, a heating block containing a cartridge heater is attached to the switching cell to allow easy adjustment of case temperature for characterization tests. The detail design of the heating unit is discussed in section 2.3.3 of this chapter. A K-type thermocouple wire is inserted into a compact cavity inside the block and placed in close proximity with the DUT. The real time temperature read by the thermocouple is converted into a proportional voltage output by using an AD595 IC, which is an instrumentation thermocouple amplifier from Analog Devices. The microcontroller reads this voltage output and controls the heating process by sending periodic switching signals to a MOSFET through hysteresis control. As seen from Figure 2.4, the implemented control system uses an upper band (T_{r1}) and a lower band (T_{r2}) to guide the actual heater temperature (T) to follow the reference temperature (T_r). The temperature reference is generated from the temperature value provided by the user in the test-control GUI.

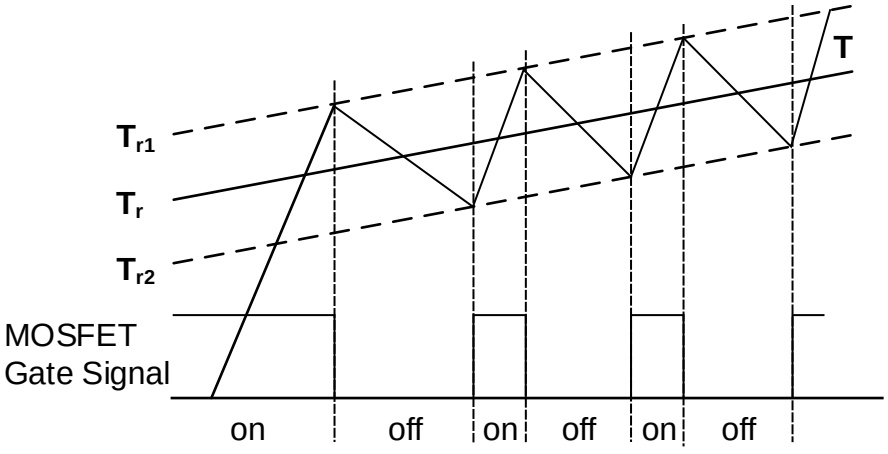


Figure 2.4 Generation of MOSFET switching signals based on temperature in hysteresis band.

2.2.3 Double Pulse Control Unit (DPCU)

In conventional DPT setups, the two pulses for the switching tests are generated from a function generator and fed into the gate of the DUT. This is an open loop system and requires human interaction in terms of pulse width calculation, configuration and overall control. In the proposed DPT, the two pulses are generated by a feedback system with an entry of test current value in the GUI. Figure 2.5 shows the circuitry responsible for generation of the pulses and the function of microcontroller pins involved in this process is summarized in Table 2.2. A hall-effect based current sensor IC, ACS758 placed in the load inductor leg, outputs an analog signal that varies linearly with the DC sampled current. The sensor output is fed to an analog input pin of the microcontroller as well as the inverting pin of both comparators U1 and U2. Comparators U1 and U2 are responsible for shutting off the 1^{st} and 2^{nd} pulse respectively. When the user starts the test, the microcontroller generates two different voltage references at the non-inverting pin of the comparators. The voltage reference is calculated with value of test-current specified in the GUI and the sensitivity or gain of the current sensor. The reference voltage at pin 1 of comparator U1 is set to allow the load current to rise up to 100% of the assigned test current whereas the reference voltage at pin 1 of comparator U2 is set to cut off the inductor current at 5% higher than assigned current. The difference between these two percentages represents the delay between the two pulses and both of these percentages can be modified as per requirements of a test. The output of comparators U1 and U2 are connected to pin A and B of the Multiplexer U3 respectively. The output pin of the mux Y is connected to R, the reset pin of a SR latch U4 while the input selection pin of the mux is connected to a digital output pin of the controller, D1. U5 is an AND gate which receives the output of U4 at pin 1 and D4, a digital output pin from the microcontroller at pin 2. D4 is set to high during the normal course of testing to allow the generation of double pulses. The controller turns it low only at the event of any fault to shut off pulses to the gate driver.

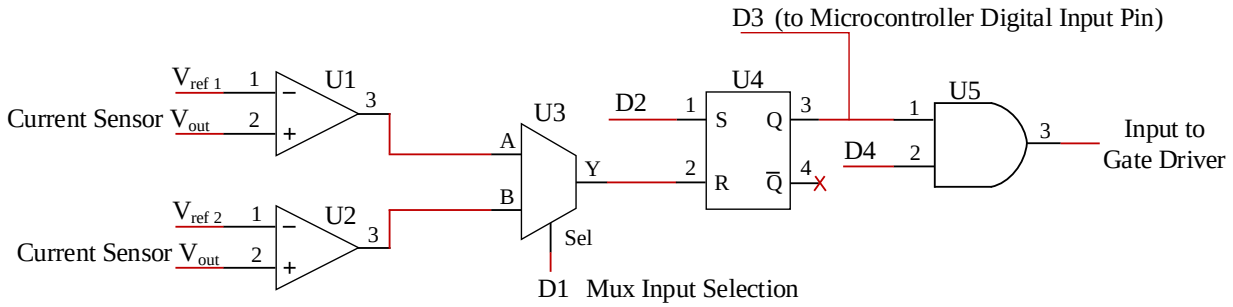


Figure 2.5 Circuitry for generation of automatic double pulses based on inductor current.

Table 2.2 Function of microcontroller pins in double pulse generation

Microcontroller Pins	**Pin configuration**	**Function**
D1	Digital output	Selects input pins of multiplexer U3
D2	Digital output	Initiates double pulse
D3	Digital input	Feedback from SR latch output to controller
D4	Digital output	Master control for double pulse generation system. In the event of any fault, pulse generation is stopped by setting this pin low
$V_{ref\ 1}$	PWM output	Sets voltage reference at 1st comparator input
$V_{ref\ 2}$	PWM output	Sets voltage reference at 2nd comparator input

At the beginning of the test, the controller keeps D1 low to select A as the active input pin of the multiplexer. During the test, as soon as the capacitor bank is charged to the desired test voltage and the heater is heated up to the desired test temperature, the controller initiates a digital pulse at pin 1 of U4 through D2. This sets the SR latch output Q high. D4 also being high during the normal course of testing, the output of U5 goes high and initiates the first gate pulse to the DUT through the gate driver. As the DUT switches on, the load inductor current starts rising. When the inductor current reaches the value of specified test current, the output of comparator U1 goes high and resets the SR latch through the mux. As Q of SR latch goes low, the output of U5 goes low as well and

this shuts off the gate signal to the DUT thereby ending the first pulse. The controller reads the status of SR latch output Q through D3. When Q goes low thereby marking the end of first pulse, the controller turns D1 high to select B as the active input pin of the mux. This enables the output of the comparator U2 to be routed to the output of the mux.

After the end of the first pulse, a delay is set in the program before the second pulse is generated. Once the delay time has passed, the controller initiates a digital pulse at pin 1 of U4 through D2. This begins the second pulse and switches on the DUT. When the load current rises to the assigned level, 5% higher than test current in this case, the comparator U2 shuts off the second pulse through the mux following the same mechanism as the first pulse. This marks the end of the second pulse i.e. the end of one dynamic test. After each test cycle, the controller is programed to return to its initial configuration for a new test to begin.

2.3 Power Board Design

The main test circuit shown in Figure 1.8 depicts a phase-leg of a voltage source converter. With all support circuitries placed on the control board, the layout of the main Power Board is carefully designed to minimize the parasitic loops associated with the test circuit. Kelvin contact sockets (Sullins make) are used at both upper and lower side device positions to allow testing of different devices. These sockets accept in-line semiconductor devices up to three leads including the most frequently used TO-247, TO-220 through-hole packages. The sockets increase the loop inductances a little bit however they protect the board from the thermal and mechanical stress during soldering and especially desoldering of the switches. Hence, during the design of the DPT power module, one has to decide a trade-off between best possible parasitic minimization and test convenience. The power board for the prototype DPT is designed considering pin 1, 2 and 3 of the DUT to follow the standard configuration of Gate, Collector and Emitter respectively for IGBTs

and Gate, Drain and Source respectively for MOSFETs. However, for testing devices with different pin configurations or packages, a new PCB can be designed to suit the concerned device and replaced with the standard PCB. This is another advantage of having the entire test setup split into control and power boards. The ability to interface a new power board for a DUT of different pin configuration or package with the existing control board makes it a universal test setup. The key elements housed on the main power board of the proposed tester are shown in Figure 2.6.

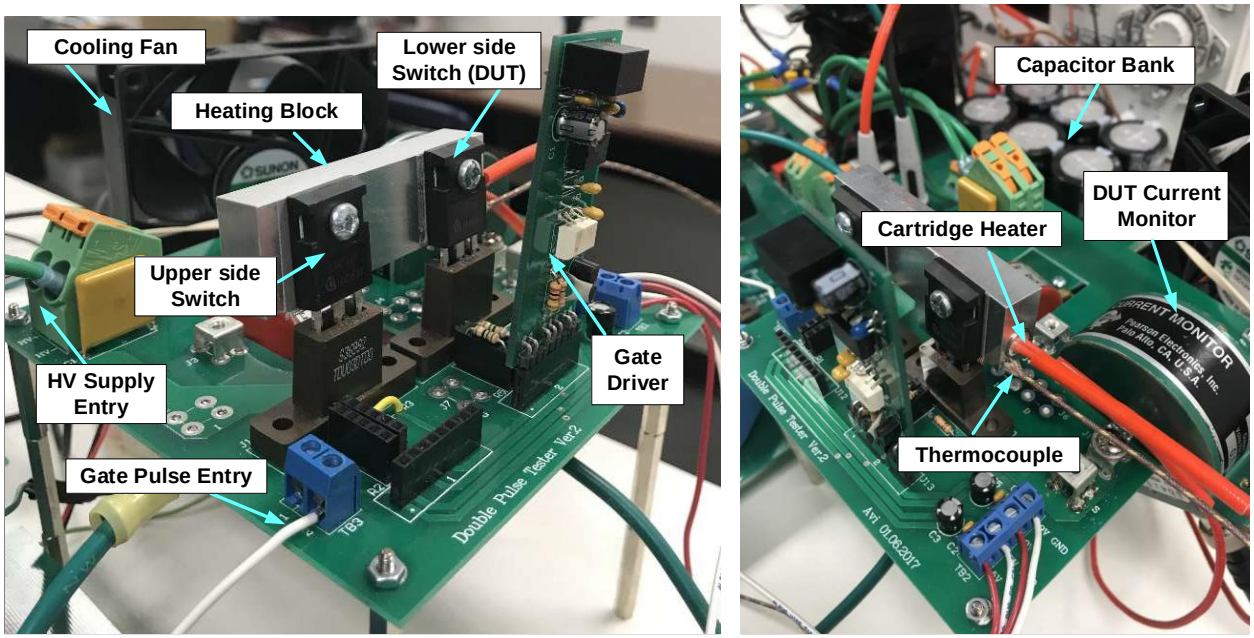


Figure 2.6 Photos of DPT power board prototype.

2.3.1 PCB Design criteria

Semiconductor devices especially the wideband gap devices are highly sensitive to circuit parasitics. The power circuit layout is carefully designed to minimize parasitics in order to obtain switching test results that describe the device properties as faithfully as possible. The main parasitic elements associated with the DPT power stage are shown in Figure 2.7.

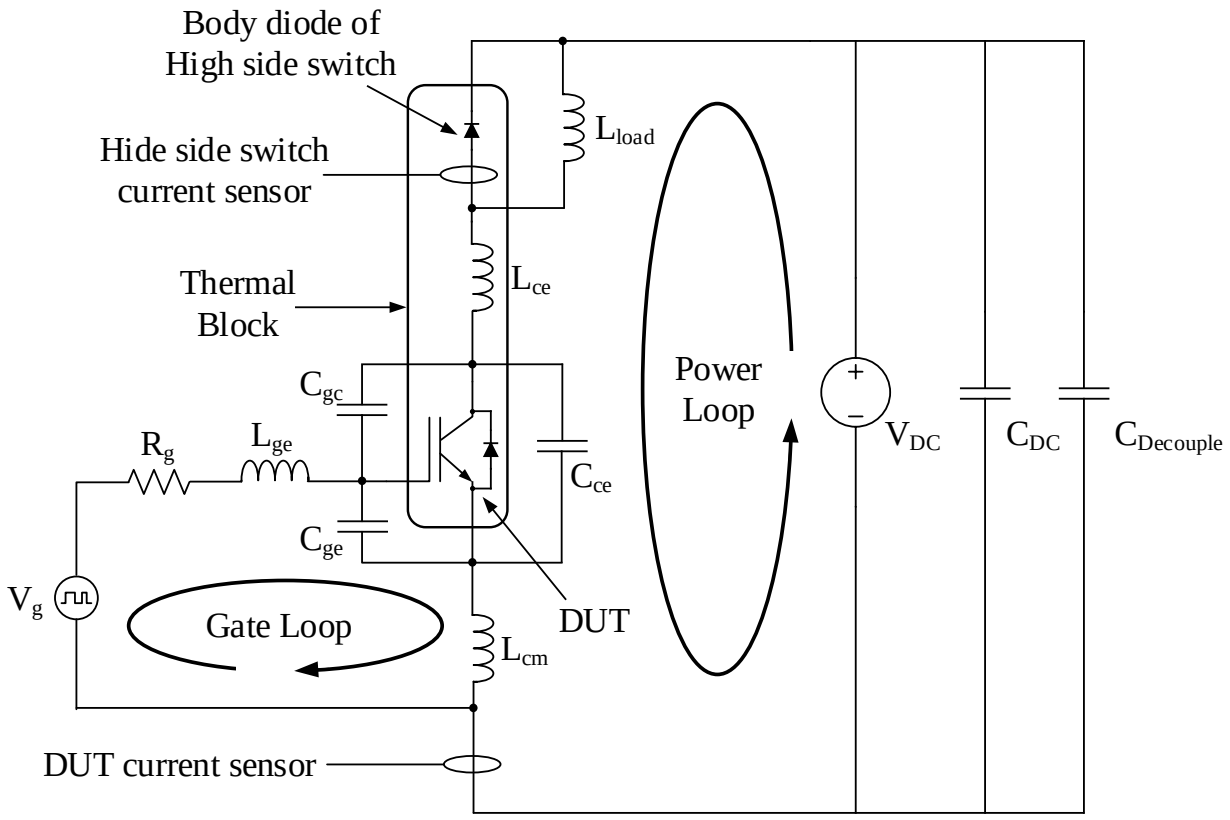


Figure 2.7 DPT test circuit schematic with parasitic elements.

L_{ce} and C_{ce} are the parasitic elements in the main power loop whereas L_{ge} and C_{ge} are parasitics associated with the gate loop. Common emitter inductance, L_{cm} and Miller capacitance, C_{gc} are the mutual parasitic elements shared by both the power and gate loops, these two act as negative feedback from the power loop to the gate loop leading to slower switching and thus increased switching losses [53]. The main switching loop stray inductance L_{ce} and gate loop inductance L_{ge} are the key contributors of the parasitic ringing but the ringing due to fast switching is more sensitive to L_{ce} [51],[53]. In this work, substantial consideration is given to reduce the critical power loop-inductance L_{ce} while designing the main power PCB. The PCB layout for the DPT power board is shown in Figure 2.8.

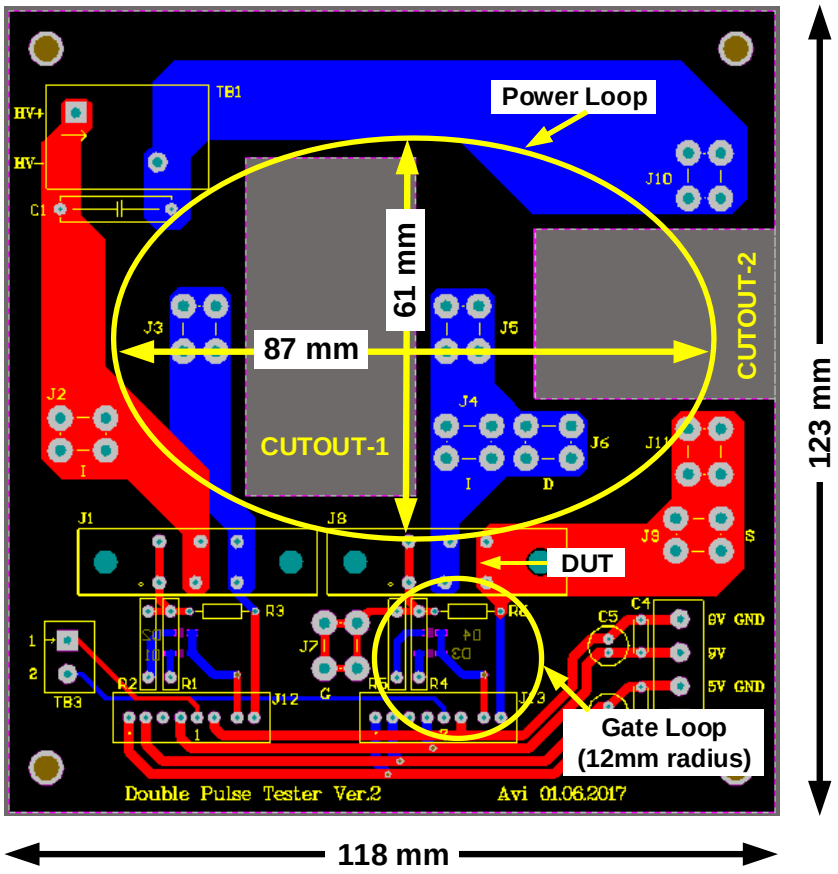


Figure 2.8 PCB layout of main test circuit – DPT power board.

As shown in Figure 2.8, cut-outs are implemented in the PCB to insert the Pearson make, current monitor or split core current probes in the main power loop. Cutout-1 and cutout-2 are for current measurements of high and low side device respectively. The gate driver has been placed as practically close to the DUT as possible in order to minimize the gate loop and limit the effects of L_{ge}. The PCB has been made compact to reduce the effects of both parasitic loops on the dynamic performance of the DUT. However, the necessary clearances and creepages are maintained as per relevant standards. The voltage drop in the device voltage V_{σ} observed in practical switching waveforms at DUT turn-on period is due to the cumulative stray inductance L_{σ} of the power loop. The mathematical expression for V_{σ} is shown in equation (2.1).

$$V_\sigma = L_\sigma \cdot \frac{di_c}{dt} \tag{2.1}$$

Where, $\frac{di_c}{dt}$ is the rate of change of device collector current or the current gradient.

2.3.2 Gate Driver Design

The gate driver is another important element of DPT that largely affects the switching behavior of the DUT. Unlike conventional setups where the gate driver is integrated with the main DPT board, the gate-driver for the proposed DPT has been designed as a discrete daughter card that can be plugged in & out of its designated socket on the mother DPT power board. This approach allows an operator to use different gate driver modules for different DUTs, replace a faulty gate driver or even replace a component on a gate driver board without the need of repeated desoldering and soldering. A typical gate driver used in the proposed DPT is shown in Figure 2.9.

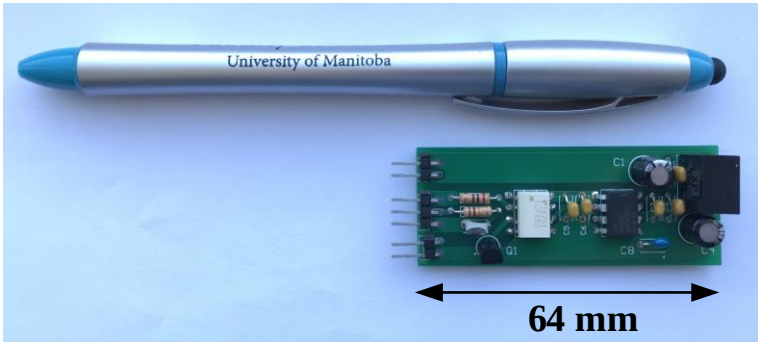


Figure 2.9 Gate driver for the automatic DPT.

The basic concept behind design of the Gate driver is explained with aid of Figure 2.10. The optocoupler provides galvanic isolation between the control and power loop while transmitting the control signals originating from the microcontroller to the gate driver IC. The selection of the gate driver IC is critical towards the switching performance of the DUT. While testing high power devices, a driver IC with high current drive capability is preferred because of its ability to switch

power semiconductor devices ‘ON’ and ‘OFF’ with short rise and fall time. This results in fast switching of the DUT and hence reduces the switching losses. A 9 A, non-inverting gate driver IC, IXDD609PI from IXYS has been used in the gate driver for testing high power MOSFETs and IGBTs. This IC has low output impedance and is able to sink and source large currents due to its totem pole configuration. The detailed design criteria of a gate driver has been extensively discussed in [59]. The DPT gate driver designed to characterize an IGBT has 0 to +15V gate drive.

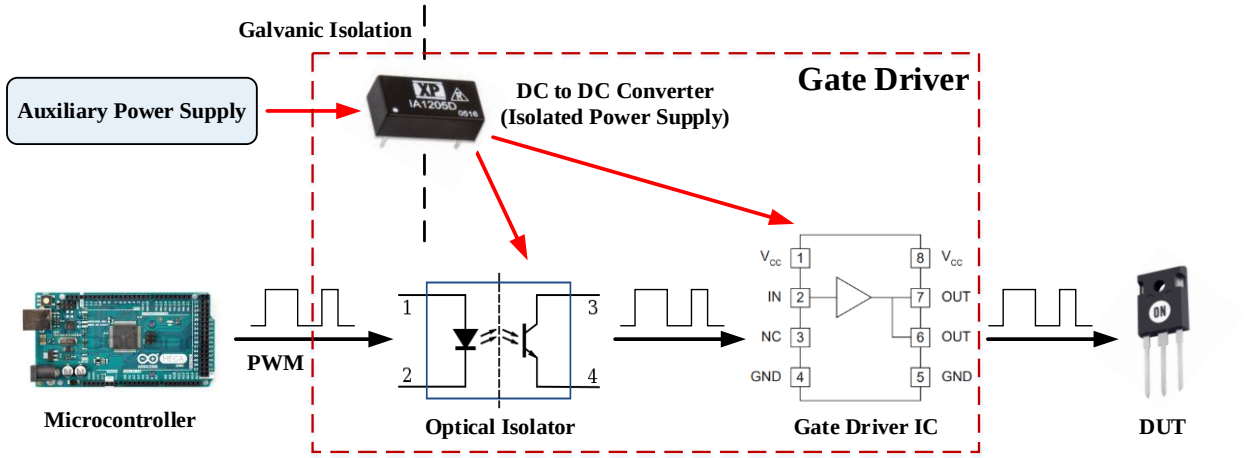


Figure 2.10 Block diagram showing overall design of DPT gate driver.

2.3.3 DUT Heating Unit Design

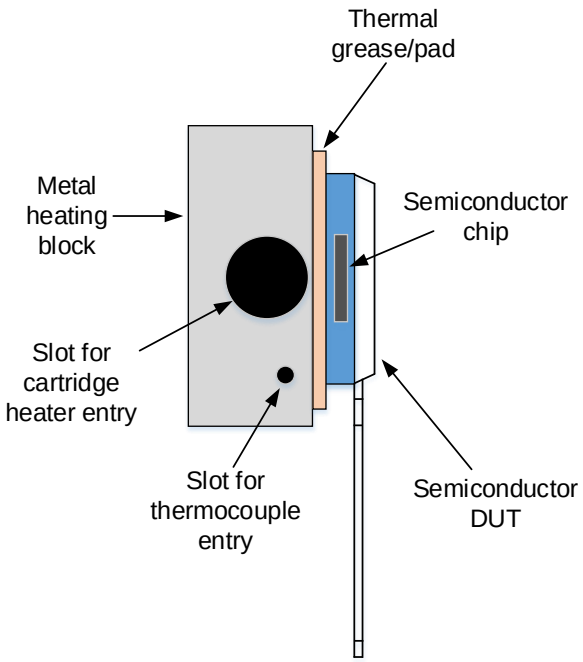
A proper thermal design is crucial for reliable operation of a power semiconductor device and the power electronics system where it is operated. It is therefore essential to study the performance of DUT under various temperature conditions to ensure its safe operation in a target application. In order to obtain the switching characteristics of a device as a function of variable case temperatures, a device heating arrangement is included in the proposed DPT. A schematic of the arrangement is shown in Figure 2.11. The DUT is mounted to a metal block containing a cylindrical cartridge heater inside it. The heater is strategically placed in a drilled cavity as close as possible to the surface of the metal block and at proper elevation in order to be in close proximity with the

semiconductor chip. A thermal pad provides insulation between the DUT and the metal block. In order to eliminate minute air gaps and maximize the heat transfer from the metal block to the chip, the heater is coated with a suitable thermal compound before inserting it in its designated slot. A K-type thermocouple wire is used to read the real-time temperature of the block and thereby control the heating action accordingly. In a fashion similar to the heater, the thermocouple is also placed inside its designated slot close to the DUT chip.

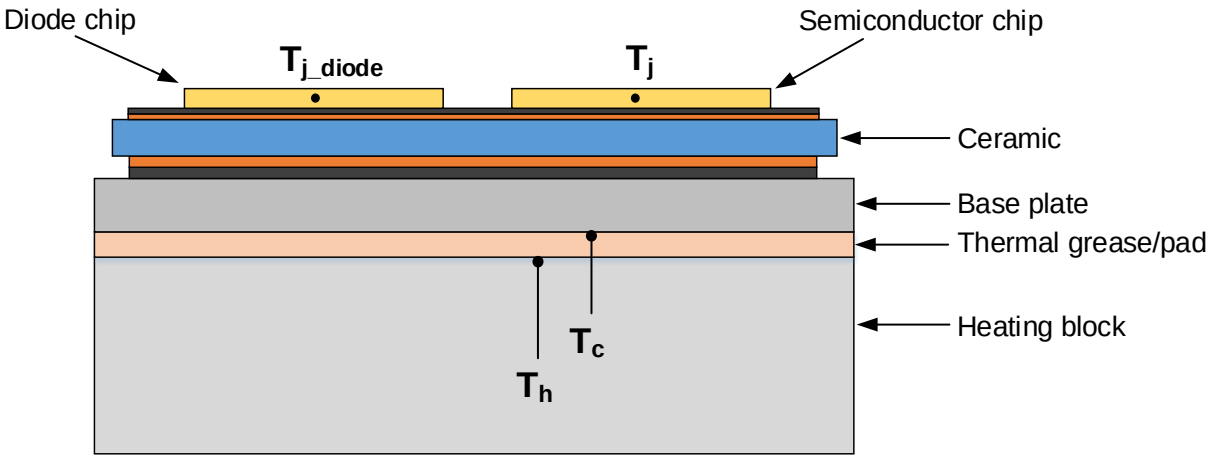
The cross sectional view of the metal block and the DUT is shown in Figure 2.11 (b). T_j and T_{j_diode} represents the case temperature of the semiconductor chip and the diode chip respectively. T_c is the surface temperature of the base plate in the semiconductor module, and T_h is the temperature measured on the surface of the metal block where the DUT is mounted. These temperatures will differ from each other because of their different positions. T_c and T_h can be measured by placing thermocouples at specific positions as shown in Figure 2.11 (b). However, T_j is measured indirectly and does not have a fixed value as the temperature inside the semiconductor chip is not uniform. The different methods used for measurement of T_j is described in the International Standard IEC 60747-9. For design simplification purpose, the values of these three temperatures are assumed to have negligible deviation in steady state. Hence, in the proposed Automatic DPT, the temperature measured through the thermocouple is assumed as the device chip temperature and used as the reference for device characterization.

In order to avoid any thermal stress on the switching cell due to prolonged heating from repetitive temperature varied DPT tests, the heating unit is cooled down to ambient temperature after completion of test cycle for a particular voltage and current range. The gate signal to the MOSFET controlling the heating action is withdrawn and a 12V DC axial fan (make: Sunon Fans) is used

for cooling the heating block. The fan is placed in close proximity with the heating block in order to expedite the cooling process. It is programmed to switch on after a complete test cycle.



(a)



(b)

Figure 2.11 DUT thermal unit arrangement, (a) side-view and (b) cross-sectional view.

2.4 Load Inductor Selection Criteria

The load inductor and DC capacitor bank are an integral part of the DPT. The design and physical placement of these components are critical as they significantly affect the switching behavior of the DUT. During the first pulse, the desired test current is established in the inductive load, which remains fairly constant at the end of the first pulse and beginning of the second pulse due to the short delay time applied between the pulses and high load inductance. The load inductance is selected to be high enough to limit the inductive current ripple ΔI_L during the switching transients [51]. By re-arranging the fundamental inductor equation, we can derive an expression for the load inductance L, as shown in equation 2.1.

$$L \geq \frac{V_{DC}}{\Delta I_L} \cdot t_{sw} = \frac{V_{DC}}{k_i \times I_L} \cdot t_{sw} \tag{2.1}$$

k_i is the current ripple coefficient which is practically considered to be 1% ~ 5%, V_{DC} and I_L are the maximum test voltage and current respectively and t_{sw} refers to the total switching time that can be obtained from device datasheet. Based on equation 2.1 an inductance value is calculated and a suitable inductor is chosen as a load which also acts as a current source for the switching cell under test. It can also be noted that fast switching wide bandgap devices are highly sensitive to circuit parasitics, therefore it is important to minimize the Equivalent parallel capacitance (EPC) of the load inductor by following certain design techniques as mentioned in [12],[53].

2.5 DC Capacitor Bank Design

During the first pulse of double pulse test, the energy from the capacitor bank is transferred to the load inductor to establish the desired test current. The bus voltage falls as the capacitor discharges during the test. The capacitance of the DC capacitor bank C_{bus} is thus chosen to limit the bus voltage ripple ΔV to 1% ~ 5% of the test voltage V_{DC} during the switching event. The energy

transfer between the capacitor bank and inductive load can be mathematically expressed with equation 2.2.

$$\frac{1}{2} \cdot C_{bus} \cdot (\Delta V)^2 = \frac{1}{2} \cdot L \cdot {I_L}^2 \tag{2.2}$$

By re-arranging equation 2.2 we can derive an expression to obtain the capacitance value of the DC capacitor bank and it is shown in equation 2.3.

$$C_{bus} = \frac{L \cdot {I_L}^2}{(\Delta V)^2} = \frac{L \cdot {I_L}^2}{(k_v \times V_{DC})^2} \tag{2.3}$$

where, k_v refers to the voltage ripple coefficient which is practically considered to be 1% ~ 5%. Based on the calculated capacitance value, suitable electrolytic capacitors are chosen for designing the DC capacitor bank. Generally, electrolytic and film capacitors are preferred for the DC capacitor bank. The technical parameters of these two types of capacitors are compared in [60] to facilitate the selection of the correct type for a particular application. The capacitor bank used for the proposed automatic DPT is built with 680µF Aluminium electrolytic capacitors rated for 350V dc from Nippon Chemi-con. An image of the capacitor bank is shown in Figure 2.12.

Figure 2.12 Image of DPT capacitor bank.

The designed capacitor bank is characterized to obtain a charging curve as a function of DC test voltages. The output current of the DC/DC converter used to charge the capacitor bank is around 2 mA (reference: Table 2.1), hence it takes considerable time to charge up the bank especially at higher voltages. A charging-time curve plotted from multiple experiments, as shown in Figure 2.13, suggests a linear relationship between the test voltage and the charging time.

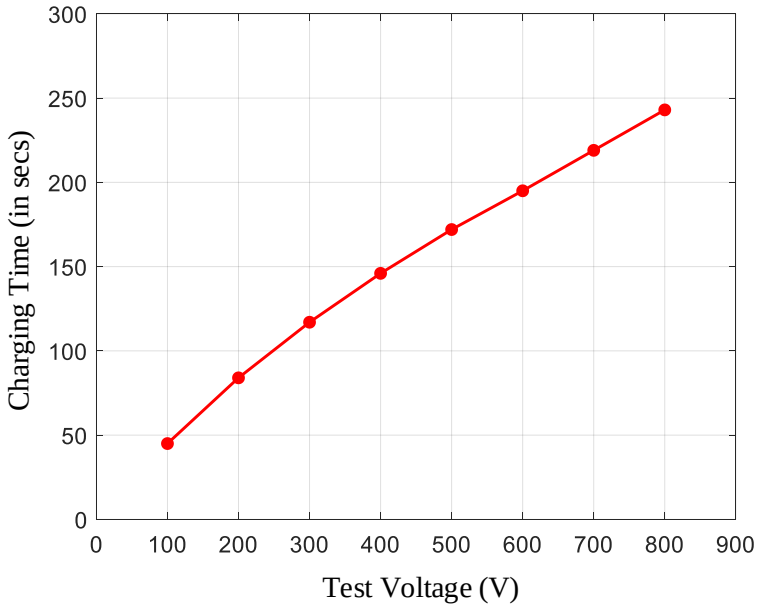


Figure 2.13 Charging time of capacitor bank as a function of test voltage.

2.6 Chapter Summary

In this chapter, design considerations of the hardware for the DPT is explored in detail. The methodical approach followed while designing the test bench is described. The setup is implemented through two modules namely, the Control board and the Power board. The Control board acts as an universal mother board whereas the Power board can be replaced to suit DUTs of different type, package, gate drive requirements etc. The design methodology, component selection criteria and primary objective of different control units onboard the Control board are

discussed. It is explained how the control units play an important role in achieving automation in the overall test process. The design of the Power board is equally important, its physical layout design being crucial in obtaining accurate switching results that truly describes the dynamic behavior of the DUT. The effects of different parasitic elements associated with the power circuit are discussed and circuit-layout optimization techniques are explored. However, it is discussed how a system designer has to choose a trade-off between test result accuracy and convenience behind the design of the Power board. The design of other key elements of the DPT such as the DC capacitor bank and load inductor is also discussed.

The entire design process is guided by the ultimate goal of building a compact, low-cost, universal, automatic DPT setup. This chapter presents the role of hardware elements in meeting each of these objectives mentioned above. The systematic control process through which the controller manages these hardware elements is explored in the next chapter.

Chapter 3 Controller Design of Automatic Tester

In the previous chapter, the multiple hardware units of the proposed DPT are introduced and their design approach and respective functions discussed in detail. In this chapter, we explore the control strategy adopted to establish an automatic, systematic functioning of the multiple hardware units as per instructions entered by an operator. In conventional DPT systems as described in Chapter 1, an user manually configures the supporting test equipments for every test condition, which makes double pulse testing a tedious process considering the numerous permutations of test conditions. This is the reason, in the proposed setup the conventional testing instruments are replaced, wherever possible, to do the same job with hardware elements that can be controlled by a microcontroller. A Graphic User Interface is designed to allow easy interaction between an operator and the control system to meet the desired objectives of the testing process. The interaction network between different key units in the testing system is described with illustrations.

3.1 Control Architecture

The control system plays a pivotal role in the stable operation of the proposed Automatic DPT. The overall test control and data acquisition activities are mainly performed by the PC based test-control software developed in Microsoft Visual Studio (IDE) and the Arduino microcontroller software (IDE). The controller is implemented with a low-cost Arduino Mega 2560, which is a microcontroller board based on the ATmega2560. It is mounted on the control board along with rest of the control circuitry. The role of these two software are further discussed in detail in the following sections.

The PC based test-control software is responsible for control and co-ordination of the overall testing process. It features a user-friendly Graphic User Interface (GUI) as shown in Figure 3.1.

The PC software also communicates with the Oscilloscope through VISA (Virtual Instrument Software Architecture), an industry-standard communication protocol. It is programmed to trigger the oscilloscope before each test to capture the switching transients, extract the raw test data and generate an excel file consisting the data captured by each channel of the oscilloscope.

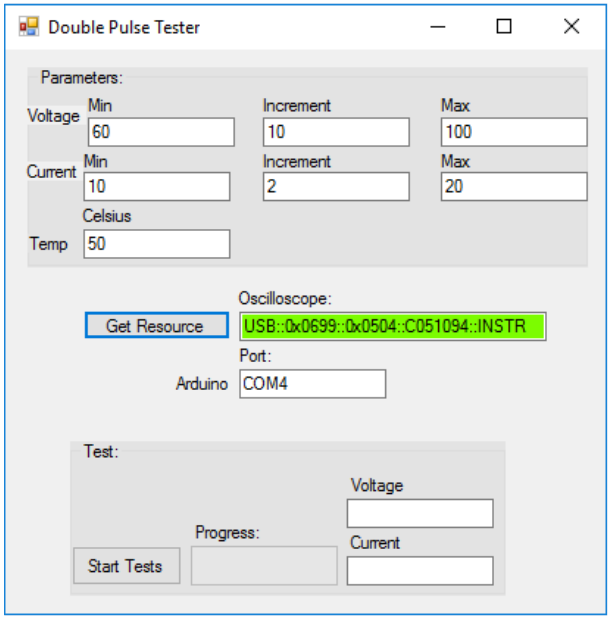


Figure 3.1 Graphic User Interface developed for the double pulse test control.

The GUI allows a user to:

- Input the test parameters i.e. voltage, current range and temperature
- Start or abort the test
- Track the progress of the test
- Monitor the real-time values of voltage and present test current
- Identify oscilloscope connected with the PC and the communication port of the controller

A serial communication is established between the PC software and the microcontroller via USB. The basic framework of the serial communication is indicated. The test-control software sends data & instructions to the controller based on the parameter entered in the GUI. Upon receiving communication from the PC software, the microcontroller sends control signals to the hardware elements on control board to prepare the test environment at the specified level and eventually execute the double pulse test. The major tasks performed by the Arduino can be outlined as below:

1. It executes a sequence of programmed instructions such as switching relays to charge up capacitor bank to a specified voltage level, heating up a cartridge heater to the test temperature and other necessary actions to prepare the test bed based on data/instructions received from the PC software.

2. Once the test bed is ready at appropriate voltage and temperature levels, it engages the load inductor into the main power circuit by switching respective relays and thereafter feeds digital and PWM signals to the logic ICs (Figure 2.5) to generate the gate pulses to perform the double pulse test.

3. It reads the real time voltage, current and temperature values from the respective sensors on the control board through its analog pins and forwards the read voltage data to the PC software to be displayed in the GUI.

4. It generates necessary digital signals to control respective relays for designated functions, PWM signals to regulate the High Voltage DC link voltage and for the fault protection-sensing circuitry.

3.2 Control Operation

The sequence of control operations programmed for conducting the double pulse test is described in this section and illustrated with Figure 3.2. Once an operator enters desired test voltage (V), current (I), temperature (T) in the GUI and initiates the test, the parameters are communicated to the Arduino. It sends control signals to the PSU to charge the DC capacitor bank to the desired test voltage and the thermal unit to set the test temperature. After the sensor feedbacks confirm that the test bed is ready, the controller sends the gate signal to the DPT power board through the DPCU (section 2.2.3). On completion of a test, the waveforms and raw data are extracted from the oscilloscope to the PC and stored in a designated location. Thereafter the next trigger setting is communicated to the oscilloscope. This process repeats until all set of tests are completed.

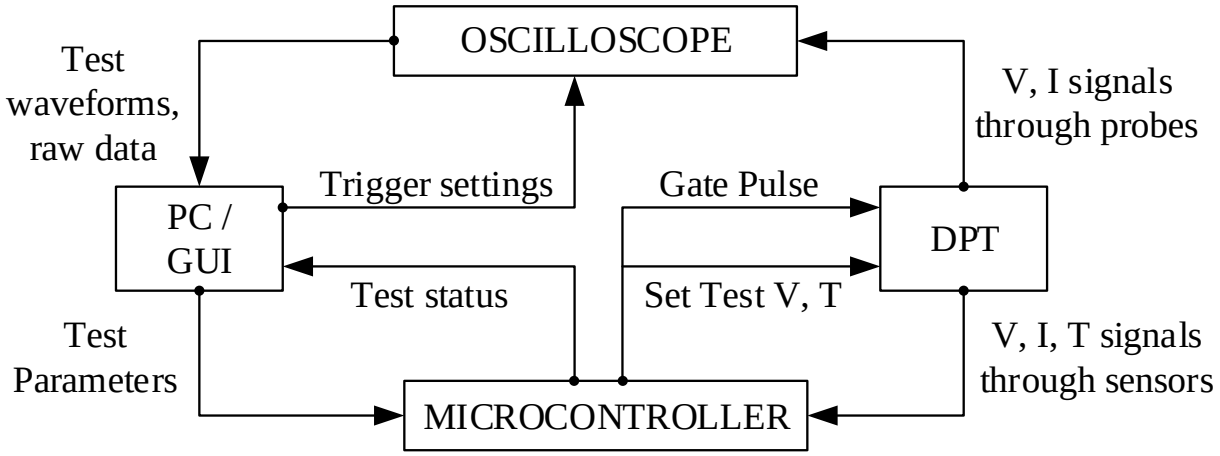


Figure 3.2 Control block diagram of DPT.

The flow chart in Figure 3.3 presents the sequence in which the test control system conducts the overall test in the Automatic DPT.

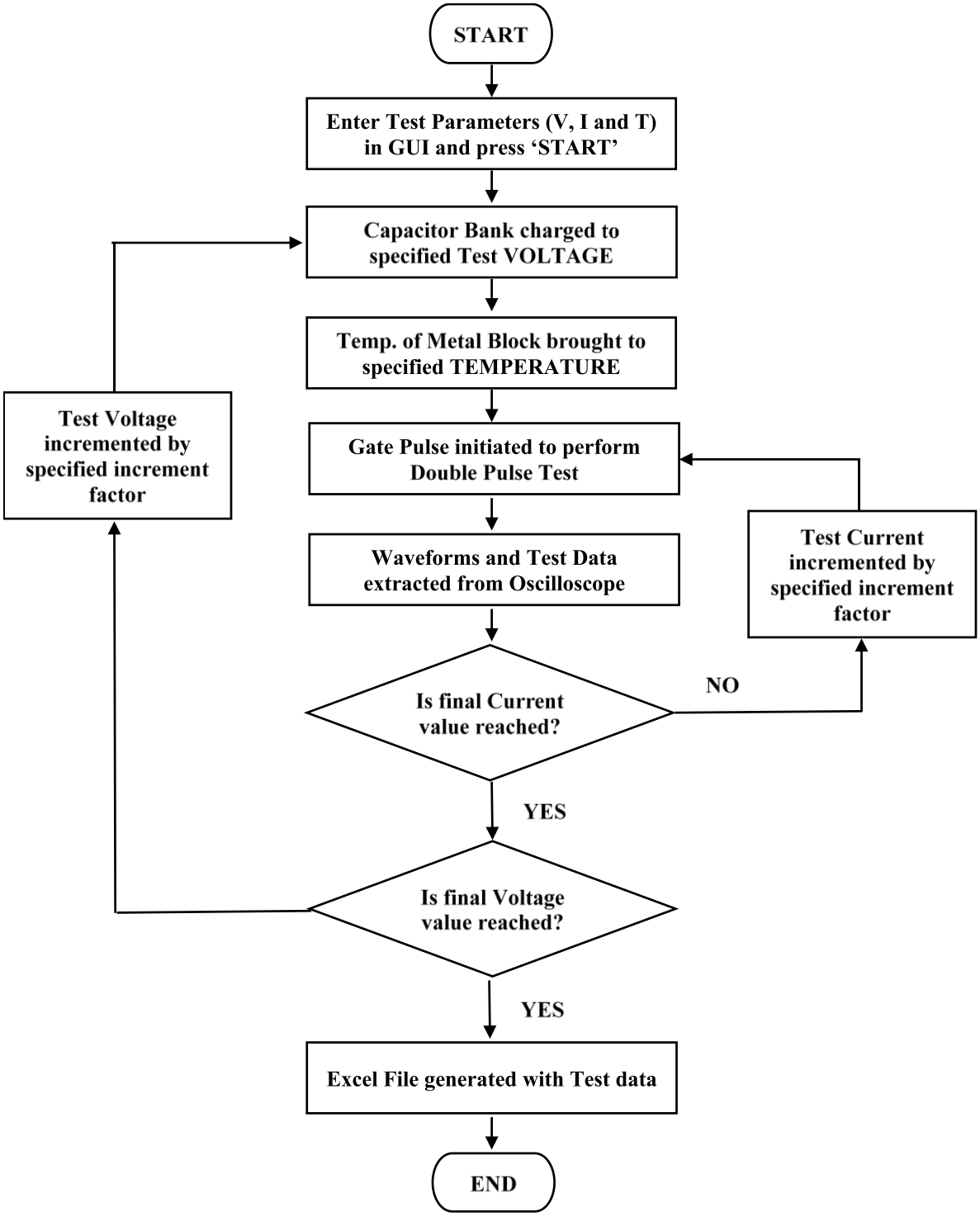


Figure 3.3 Control flow chart describing operation of DPT.

In every test cycle, the temperature is kept constant whereas the test voltage and current are gradually increased in incremental steps specified in the GUI. The primary intention behind

keeping the temperature constant unlike the continually increasing test voltage and current is to ensure safe operation of the DUT. The cumulative heating effect induced by cyclic stresses from repetitive temperature changes may cause thermal fatigue or damage to the DUT. In real life applications, heat sinks are attached to semiconductor switches for dissipation of the heat to allow safe device operation. In case of DPT, the idea is to artificially inject heat to the switching cell and evaluate its dynamic performance at a certain temperature. Since there is no scope of heat dissipation, prolonged operation especially at temperatures close to the absolute maximum rating of the device may cause device failure. Hence, after completion of the complete range of voltage and current tests for a particular temperature, the DUT is cooled down to ambient temperature.

Without any interruption in the test process, it may take up to 5 hours to characterize a DUT in a range of V_{CE} = 100V to 600V (with 100V incremental step), I_C =10A to 60A (with 10A incremental step), T_C = 25°C to 150°C (with 25°C incremental step) using the automatic DPT. Since the testing process is quiet long, the proposed DPT setup saves manpower by automatically performing the tests and capturing the test results. For the voltage, current and temperature range specified above, there are 360 tests in total considering separate tests for capturing turn-on and turn-off transient for each test condition. For each test value, only the turn-on and turn-off transients are captured rather than capturing the entire double pulse waveform. Although this approach increases the overall testing time, it offers multiple advantages from test-data management and accuracy point of view. Capturing the entire double pulse waveform in the oscilloscope window reduces the number of data points for the switching areas and results in very large file size. This makes the data handling process very challenging and slow considering the heavy data files generated from several tests. Since our area of interest is only the switching transients, the oscilloscope trigger is programmed to capture only the switching window. This approach gives us more data points for

the switching portion allowing better estimation of switching results. Moreover, the size of data file is also considerably reduced allowing convenient storage and processing of raw test data.

3.3 Chapter Summary

In this chapter, the control techniques adopted for the organized functioning of the proposed automatic DPT are studied. The control system is implemented mainly with two units, the 'test-control software' in the PC and the Arduino microcontroller software. The automation in the test process is achieved through the successful interaction between these two control units along with uninterrupted execution of their respective roles.

The PC based software through its GUI acts as an interface window thereby allowing the user to interact with the controller and operate the test system seamlessly. Based on the user inputs, it governs the testing process by communicating with the Arduino as well as the oscilloscope. However, on receiving the test parameters from the PC, the Arduino controller executes the main control operations by managing the on-board hardware elements introduced in Chapter 2 such as the PSU, DPCU, voltage, current, temperature sensor and control units. In this chapter, the sequence in which the control operations are performed is investigated with help of control block diagrams and necessary illustrations. The logic behind the chosen sequence of control operations is discussed in the final section.

The effective functioning of the control system enables the automatic DPT system to operate with minimal human involvement. Although the testing process takes its due time for completion, the proposed test bench allows the user to walk away from the setup after entering the test parameters, leaving the control system to take care of all the testing, recording and data acquisition operations.

Chapter 4 Data measurement and processing

The hardware and control elements of the proposed DPT are introduced and elaborately discussed in Chapter 2 and 3 respectively. The content of these two chapters allow a reader to gain an in-depth understanding of the test setup and test control mechanism. However, another important aspect of double pulse test is the measurement, recording and processing of the switching data gathered from multiple tests conducted at several different test conditions. This chapter focuses on special technical requirements of the measurement tools used in the testing process and the data processing techniques adopted in this thesis work.

The dynamic characterization of the latest power semiconductor devices require measurement tools of adequate bandwidth to accurately capture their fast dynamic switching waveforms. The latest state-of-the-art and widely used measurement tools i.e. voltage probes and current sensors are discussed in this chapter. The importance of voltage and current probe timing calibration is investigated and the calibration setup used during this work is described. Finally, a waveform analysis tool, developed during this thesis work to process the heavy amount of data captured during double pulse tests, is introduced.

4.1 Specification of Measurement tools

Switching characterization of power semiconductor devices involves accurate calculation of their switching energy losses and switching times i.e. rise time and fall time. As a standard practice, the three waveforms i.e. the gate emitter voltage V_{GE}, the collector-emitter voltage V_{CE} and the collector current I_C are measured for the loss calculations. In order to capture the rising and falling edges of the high-speed switching transients of the above parameters with adequate signal fidelity, high bandwidth measurement tools are required. According to signal theory, the effective

bandwidth f_{BW} of a slope signal with a rise time t_r or fall time t_f can be obtained using the expression below [12],[53],[61] :

$$f_{BW} \approx \frac{0.35}{\min(t_r, t_f)} \tag{4.1}$$

As a rule of thumb, for accurate pulse rise time measurements the rise time of a measuring equipment needs to be no more than one-fifth of the rise time of the signal to be measured [24]. We can use equation 4.1 to estimate the bandwidth/rise time of the measurement tools in our case since the typical rise/fall time figures of the DUT can be found from the manufacturer's datasheet.

The switching transients of an Infineon make 1200V 40A IGBT (IKW40T120) is measured using the proposed DPT. As per the manufacturer datasheet, the rise time of this IGBT is typically around 30ns. The corresponding bandwidth for a rise/fall time of 30 ns is calculated around 12 MHz using equation 4.1. This implies that the rise time of the oscilloscope and probes combined should be at least one fifth i.e. 6 ns or less (or an equivalent bandwidth of 60 MHz calculated using equation 4.1) for reasonable accuracy in measurement of switching transients of this IGBT. However, measuring equipments with higher bandwidths may be required for error-free and reliable switching transient measurement of WBG devices with very low rise/fall times.

The technical specifications of the latest voltage probes and current monitors used for dynamic characterization of power semiconductor devices have been discussed in the following sections. However, a detail comparison of their accuracy has been elaborately investigated in [51]. Along with the probes, the bandwidth of the Oscilloscope used to monitor and record the switching transients is also important for test result accuracy.

4.1.1 Device voltage measurement

The DUT switching voltage i.e. the collector-emitter voltage, V_{CE} for an IGBT or drain-source voltage, V_{DS} for MOSFET is one of the key waveforms captured during the double pulse test in order to monitor its dynamic behavior as well as derive the switching data. This waveform is also a key indicator of the design quality of the physical layout of the power circuit as the cumulative parasitic inductance of the power loop L_σ can be extracted from this waveform. The procedure for parasitic inductance extraction from the V_{CE} waveform is explained in the next chapter. Moreover, the turn-on and turn-off switching voltage gradient i.e. $dv/dt_{(on)}$ and $dv/dt_{(off)}$ which is one of the indicators of the switching speed of the DUT are also measured from this waveform.

Another important waveform for deriving the switching characteristics is the gate emitter voltage, V_{GE} or gate source voltage, V_{GS}. As mentioned in the definition of switching time and losses in Chapter 1, section 1.3, certain key points in the gate voltage waveform are used to calculate the switching data of a DUT. The V_{GE} waveform also serves as a reference while comparing the change in the device voltage and current switching with change of test parameters. For V_{GE} measurement, the dynamic range of the probe is not as critical as the bandwidth. A probe of high bandwidth may be used for low-side V_{GE} measurement in half-bridge configuration. However, several parameters such as probe bandwidth, galvanic isolation, common mode input voltage range, and CM rejection ratio need to be taken into account for the correct probe selection [51]. However, it is practically difficult to achieve an optimal trade-off between all the parameters mentioned above.

There are several probes in the market that can be used for device voltage measurement during double pulse tests. The two main types of voltage probes i.e. Differential and Passive probes both are used in switching characterization applications. However, passive probes are preferred due to

their high bandwidth and wide dynamic range. A comparison of the technical parameters for the latest and most commonly used voltage probes is summarized in Table 4.1.

Table 4.1 Technical comparison of latest voltage probes [51]

Models	**Manufacturer**	**Type**	**Max. input voltage**	**Bandwidth**	**Rise time**
P5100A/P5150	Tektronix	Passive	2.5 kV (peak), 1 kV (rms)	500 MHz	<700 ps
TPP0850	Tektronix	Passive	2.5 kV (peak), 1 kV (rms)	800 MHz	<525 ps
PPE4KV	LeCroy	Passive	4 kV	400 MHz	<875 ps
THDP0200	Tektronix	Differential	±1.5 kV	200 MHz	<1.8 ns
TMDP0200	Tektronix	Differential	±750 V	200 MHz	<1.8 ns
P5205A	Tektronix	Differential	±1300 V	100 MHz	<3.5 ns

From the figures in Table 4.1, it is evident that the bandwidth of differential probes are lower than that of the passive probes hence, not suitable for characterizing the latest fast switching WBG devices like GaN HEMTs, SiC MOSFETs etc. However, they can still be used to characterize Si devices depending on the switching speed of the device. However, from safety point of view, differential probes are a popular choice since they provide galvanic isolation. Adequate care has to be taken while using direct passive probes for DUT voltage measurement because the power ground is shared by all the channels grounds in the oscilloscope. Incorrect connection of certain components such current shunts, if used for device current measurement, may create a short and lead to potential damage to the probe, oscilloscope as well as the systems where it is attached. A

recommended probe connection while using passive probes for V_{CE} and V_{GE} measurement and current shunt for I_C measurement is shown in Figure 4.1.

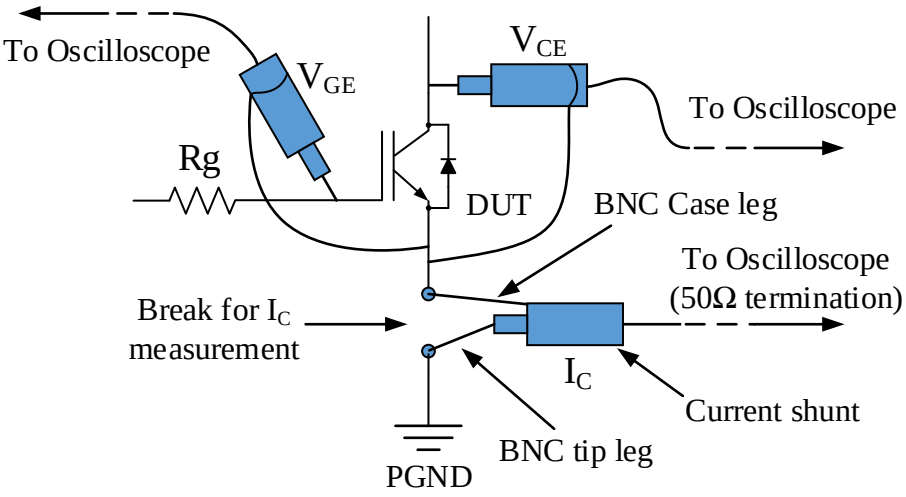


Figure 4.1 Recommended connection while using passive probes and coaxial current shunt.

4.1.2 Device current measurement

Besides the DUT switching voltage and gate voltage waveforms, the DUT current waveform is traditionally measured for switching loss and time calculations. Unlike voltage measurement techniques that can be applied by connecting the probes externally at the desired test point, the current measurement requires special consideration. The measurement of current requires a break in the power circuit to insert the measurement device. Although this approach increases the inductance of the power loop, it remains the only way to measure DUT current. Several current measurement devices are available from different test instrument manufacturers, a suitable option may be selected based on the type of device to be tested. The technical specifications of the most commonly used state-of-the-art models of current monitoring devices are summarized in Table 4.2.

Table 4.2 Technical comparison of the latest current measurement devices [51]

Models	Manufacturer	Type	Max. current	Bandwidth	Rise time
TCP0030A	Tektronix	Split core probe	50 A (peak), 30 A (rms)	120 MHz	<2.92 ns
Coaxial Shunt, SDN-414-10 (0.1Ω)	T&M Research Products	Current viewing resistor	–	2000 MHz	0.18 ns
Coaxial Shunt, SDN-414-025 (0.025Ω)	T&M Research Products	Current viewing resistor	–	1200 MHz	0.3 ns
Current monitor 2877	Pearson Electronics	Current transformer	100 A (peak), 2.5 A (rms)	200 MHz	2 ns
Current monitor 411	Pearson Electronics	Current transformer	5 kA (peak), 50 A (rms)	20 MHz	20 ns
CT-C0.1	Bergoz Instrumentation	Current transformer	10 kA (peak), 35 A (rms)	50 MHz	7 ns
CWT Mini 1	PEM	Rogowski Coil	300 A (peak)	15 MHz	25 ns

The split core current probe TCP0030A provides galvanic isolation and can sample both continuous and peak currents. However, due to its limited bandwidth, it may not be the best option for WBG device current measurements. The Pearson and Bergoz current transformers are also widely used for power semiconductor characterization applications. They can be introduced in the power loop by inserting the wire carrying DUT current through it. These monitors provide galvanic isolation and highly suitable for current measurements of conventional Si devices. Both the split core current probe and Pearson current monitors operate with a loop of wire running through it, this approach introduces additional parasitic inductance in the power loop thereby significantly affecting the switching performance of the latest high-speed WBG devices. Due to limited bandwidth and accuracy, the Rogowski coil is not suitable for switching current measurement of the latest WBG devices. Although the coaxial shunts/current viewing resistor (CVR) do not

provide galvanic isolation and only permit pulsed operation, they are the most popular choice for current measurement for WBG devices due to their higher bandwidth and accuracy. The CVR has a very low footprint connection to the power circuit, so the distance between the break points in current path can be short. Adequate care has to be taken while installing CVRs as they don't have galvanic isolation. While measuring the current of the low side device in phase leg configuration, the power ground is shared by the oscilloscope channel grounds when direct probes are used for voltage measurement. Hence, it has to be connected in proper configuration to avoid any electrical hazards and potential damages to the device as well as circuitry involved. A recommended probe connection while using CVRs has been discussed in the previous section and shown in Figure 4.1.

A test has been conducted in [51] to compare the measurement accuracy of the different current measurement devices mentioned above. The authors have presented accuracy evaluation results and concluded that the accuracy of the switching current measured by the coaxial shunt is the highest. In the above text, the pros and cons of the current measurement devices are investigated from an electrical point of view. Similarly, they have certain advantages and disadvantages when studied from convenience perspective. With suitable attachments, the Pearson current monitor, the split core current probe and Rogowski coil can be easily connected with the circuit. These devices offer high degree of flexibility in terms of handling as they can be conveniently connected and disconnected from the test circuit. However, a coaxial shunt/CVR has to be installed by soldering its legs on the PCB. If the device has to be disconnected from the setup for any reason, the only option is through desoldering. The soldering and desoldering process creates thermal and mechanical stress on the board as well as components surrounding the CVR. In this regard, it may be concluded that one has to decide an optimal trade-off between accuracy and convenience while designing an universal test platform.

4.1.3 Probe Calibration

The voltage and current probes have their individual characteristic propagation delay. When used in pair, the skew between the voltage and current probe can introduce a time delay between the voltage and current waveforms recorded in the oscilloscope. This will lead to inaccurate measurement of a DUT's switching behavior hence incorrect switching loss and time calculations. For an instance, double pulse tests conducted in [51] with uncompensated probes with a SiC MOSFET as a lower side switch indicates that 83% error in upper switch switching loss for 1 ns misalignment, 25% error per ns in the lower switching loss, and 31% error of total switching loss will be introduced for 1 ns skew. From these figures, it is evident that the Voltage (V) – Current (I) timing alignment is critical for true recording of double pulse test waveforms.

There are several methods for V-I alignment based on the type of voltage and current measurement device being used. The most commonly used methods for probe calibration are described in [51]. During this work, while using Tektronix make high voltage differential or passive probe and split core current probes as measurement devices, the power measurement deskew and calibration fixture (067-1686-00) from Tektronix [62],[61] is used to compensate for timing differences between the probes. The fixture has BNC inputs that can be connected to an external signal generator with a BNC cable to generate the reference signal. The probes are connected to the fixture in their respective test points. The fastest probe i.e. the probe with the highest bandwidth is chosen as a reference to deskew the slower channels. The deskew time in the oscilloscope is adjusted so that both the signals align with that of the fastest channel. The channels have to be deskewed to compensate probe timing every time the probes or oscilloscope are changed. A schematic showing the typical connections for probe calibration is shown in Figure 4.2.

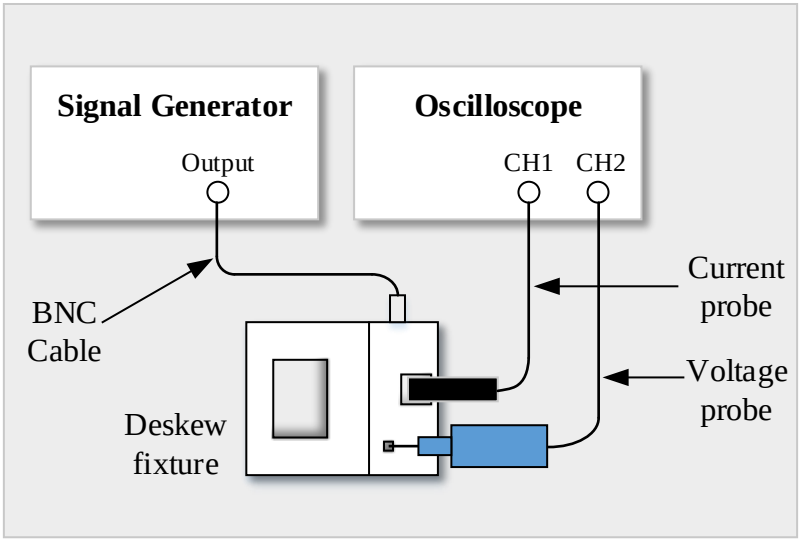


Figure 4.2 Typical connection for probe deskewing.

4.2 Waveform Analysis Tool

The switching transients are automatically captured and extracted from the oscilloscope by the PC based software and it becomes available to a user in form of excel files on completion of each test. Separate excel documents are generated for each oscilloscope channel containing raw data points of turn-on and turn-off switching period for each voltage and current value. Capturing only the switching window provides adequate data points for switching loss estimation and also results in data files of low file sizes. Once the entire test data is available to an user, an effective analysis tool is required to process the massive data and extract the useful information that can give us significant insight into the switching behavior of the DUT. In the proposed system, waveform analysis is performed by two MATLAB programs. On successful linking of the program and folder where the test results have been saved, the first program runs the data analysis on each of the waveforms recorded and plots the switching losses of each test on a 3-dimensional grid. The other program analyses a single test result and returns a series of information which includes the turn-on, turn-off energy loss figures, total switching loss, rise time, fall time and so on.

In order to test the newly designed Automatic DPT, an Infineon make 1200V 40A IGBT IKW40T120 was characterized. The Matlab script developed for automatic data processing scans through the raw data and identifies the key points in the switching waveforms, as shown in Figure 4.3, in order to obtain the switching time and loss figures. These points are selected based on the relevant switching definition followed by the manufacturer.

The waveform analysis tool has been programmed following the switching time and loss definitions discussed in Chapter 1, Section 1.3. However, if the switching results have to be analysed with different standards, the reference point in the programs can be easily changed to calculate switching data based on the new definitions.

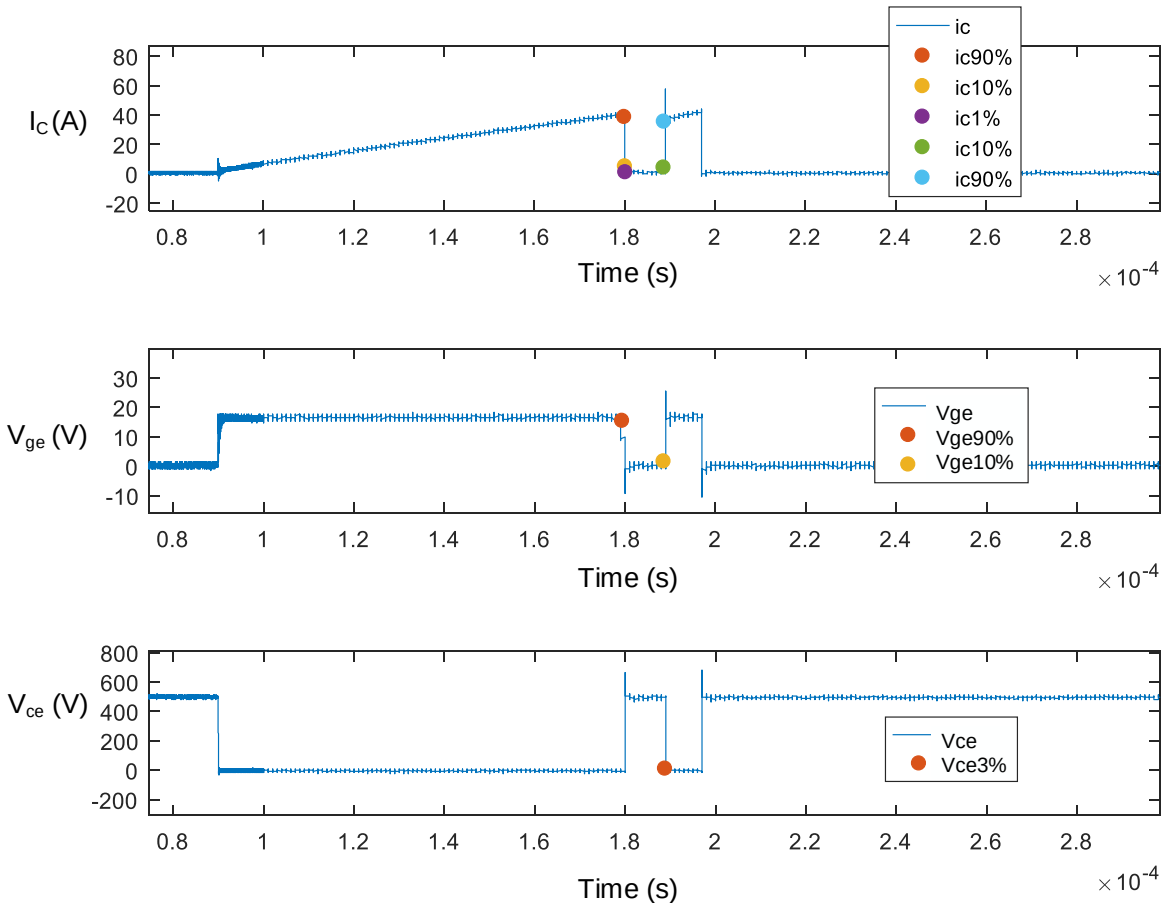


Figure 4.3 Key points identified on switching waveforms for switching data calculations.

4.3 Chapter Summary

The special technical requirements of the measurement devices used in capturing the switching transients during the double pulse test are discussed in this chapter. The latest state-of-the-art measurement tools and techniques available for device switching voltage and current measurements are presented. Their technical specification is summarized along with a discussion on pros and cons of each devices. It is concluded that measurement tools of high bandwidth and dynamic range are required for recording the high speed rising and falling edges of the switching waveforms of the latest WBG semiconductor devices. However, in context of the designing an universal test bed, it is also seen that an optimal trade-off has to be chosen between accuracy and convenience.

Following the discussion on appropriate measurement devices for switching characterization applications, the importance of voltage and current probe timing alignment is studied. Even a slight time delay between the voltage and current waveforms recorded during the test will introduce finite errors in the switching data calculation. The procedure followed for deskewing the probes prior to conducting double pulse tests during this research work is discussed.

Finally, the Waveform Analysis Tool (WAT) developed in MATLAB to process the vast amount of test data is introduced. In a double pulse test, a device is typically characterized in a wide range of test values by permutations of various test parameters. It is a tedious process to manually process the post-test raw data. The WAT scans through the waveforms, identifies the key points based on switching definitions and outputs the switching loss and time data.

Chapter 5 Experimental Results

In the previous chapters, the hardware and control elements for the proposed DPT are introduced; the selection of appropriate measurement tools and the post-test data processing technique developed during this research work are discussed. In this chapter, the theories and ideas are put into practise by subjecting the DPT prototype to various tests in order to verify and validate the design principles. The proposed DPT is designed to be a universal setup allowing switching characterization of all kinds of power semiconductor device by replacing the power module. However, to demonstrate the successful operation of the test bench, few devices are characterized and the switching results are presented. A detail analysis of the results is conducted in order to understand the dynamic behavior of the DUT concerned under different operating conditions.

5.1 Experimental Setup

The proposed DPT has been implemented with two modules, the control and power board. The power board can be changed based on the type of device being tested and then interfaced with the mother control board. To demonstrate the operation of the test bench, a power interface board suitable for testing devices in standard TO-247, 3-pin package is designed and implemented. The details of the power board design has been discussed in Chapter 2, Section 2.3. It has an optimized power loop layout and features sockets to allow easy replacement of DUTs. Although the legs of the sockets introduce some parasitic inductance to the power loop, it prevents the power board from thermal and mechanical stress during repeated soldering and desoldering of devices. The nominal and absolute maximum rating of the experimental setup is summarized in Table 5.1. However, these ratings are restricted to the demonstration prototype only and can be easily upgraded if required. In the event of testing DUTs of higher rating with respect to values indicated

in Table 5.1, possible ways of upgrading the operating ratings of the test setup is discussed in the following section.

Table 5.1 Technical Specifications of the Experimental Setup

Parameters	**Symbol**	**Value / Maximum Rating**	**Units**
DC Link test voltage	V_{DC}	1000[a]	V
Test Current – Peak	I_{C-pk}	100 [b]	A
Test temperature	T_C	400[c]	°C
Gate drive voltage	V_G	0/+15[d]	V
Auxiliary supply voltage	V_{AUX}	5	V
Stray Inductance	L_σ	123	nH

The discussion with reference to the superscript letters in the maximum rating numbers in Table 5.1 is presented below:

a. The maximum output voltage from the High Voltage DC/DC converter module i.e. VHV12-1.0K2000P used in the PSU design is 1000V. This restricts the maximum DC link test voltage of the experimental setup to 1000V. However, if necessary, this can be easily scaled up to higher voltages by using other models of DC/DC converters with higher voltage output. For instance, another model in the same series, the VHV12-2.0K1000P module has an output voltage of 2000V. However, the rating of the DC link capacitor banks, the decoupling capacitor as well as the clearances in the power circuit have to be revised to suit the higher voltage.

b. A current sensor IC, ACS758LCB-100B-PFF-T is used in the DPCU to control the gate pulse widths by sampling the load current in the power circuit. The peak test current rating of the

experimental setup indicated in Table 5.1 i.e. 100A is restricted by the maximum current that the current sensor can safely sample. If the test current needs to be increased in order to test DUTs above 100A, then other models of current sensors from this family may be used in the control board. For instance, the ACS758ECB-200B-PFF-T model is capable of sampling primary currents of 200A. However, the current rating of the load inductor, conductor sizes and PCB trace widths have to be increased in order to allow safe testing at higher currents.

c. The maximum operating temperature for the cartridge-heating element is approximately 650°C and the maximum temperature the K-type thermocouple wire can read is 482°C. This is the reason the maximum operating temperature of the setup has been selected as 400°C allowing some safety margin. However, absolute maximum ratings of the DUT has to be strictly followed in order to avoid any damages to the device.

d. The gate drive voltage of 0/+15V mentioned in Table 5.1 is for driving a Si IGBT which is the DUT selected for performance demonstration of the experimental setup. This can vary based on the type of device being tested. A suitable gate driver for the device being tested has to be installed in the power module for pulse testing.

The complete experimental setup is shown in Figure 5.1. Probes and oscilloscope of adequate bandwidth are necessary to accurately capture the high-speed switching transients. Tektronix High voltage differential probe THDP0200 (200 MHz) and current probe TCP0030A (120 MHz) are used for DUT voltage and current measurement respectively. The turn-on and turn-off switching transients of the DUT are monitored and captured by a 350 MHz high bandwidth digital oscilloscope MSO5034B from Tektronix.

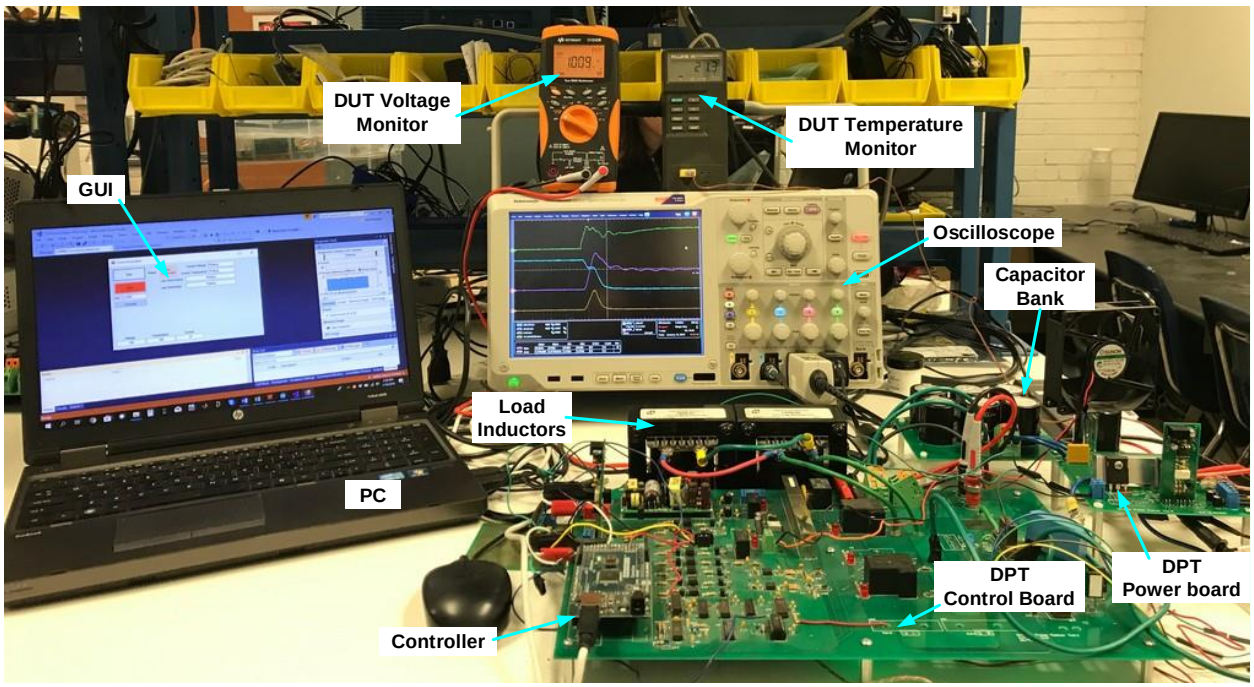


Figure 5.1 Complete DPT experimental setup.

5.2 Experimental Results

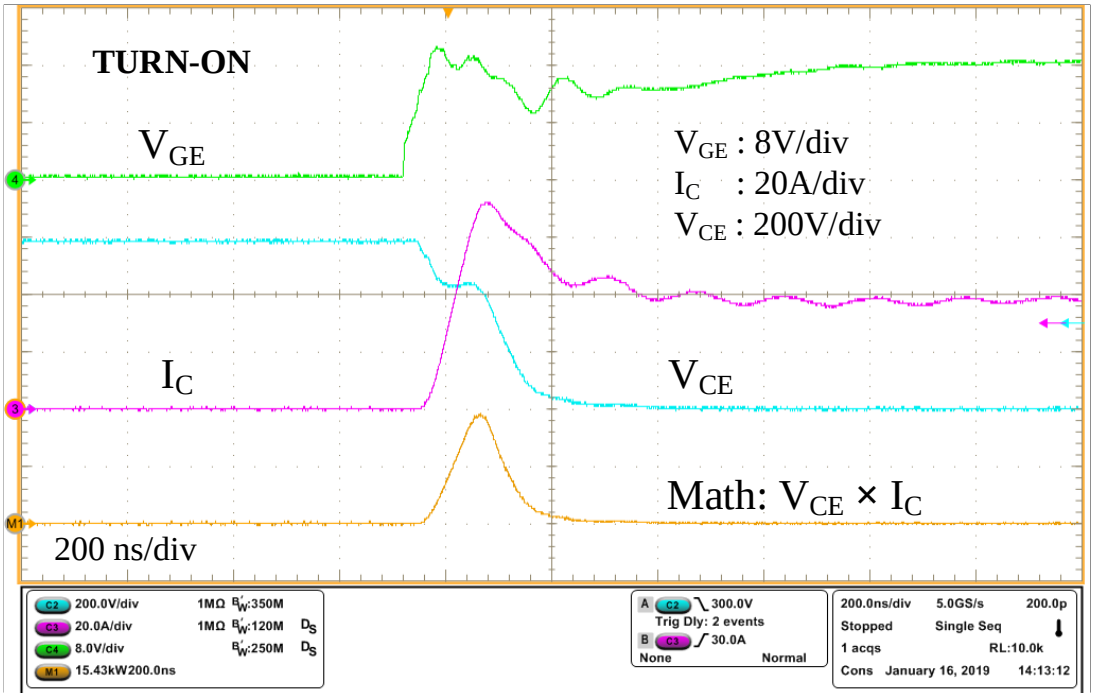
A Si IGBT is chosen within the maximum electrical ratings of the DPT demonstration board and characterized under different operating conditions. The raw data extracted from the DUT switching tests are processed by the WAT in order to generate the switching data. The final switching results are presented with different plots to allow an in-depth understanding of the dynamic behavior of the DUT under various test conditions. A GaN FET is also characterized and its switching performance is compared with that of the Si IGBT for a particular test condition.

The switching results obtained from the experiment are analysed and the dynamic behavior of the DUT is studied as a function of various key parameters in the subsequent sections. Although most of the turn-on and turn-off parameters are discursively defined in Chapter 1, section 1.3.1 and 1.3.2 respectively, the most commonly used terms in this analysis are summarized in Table 5.2.

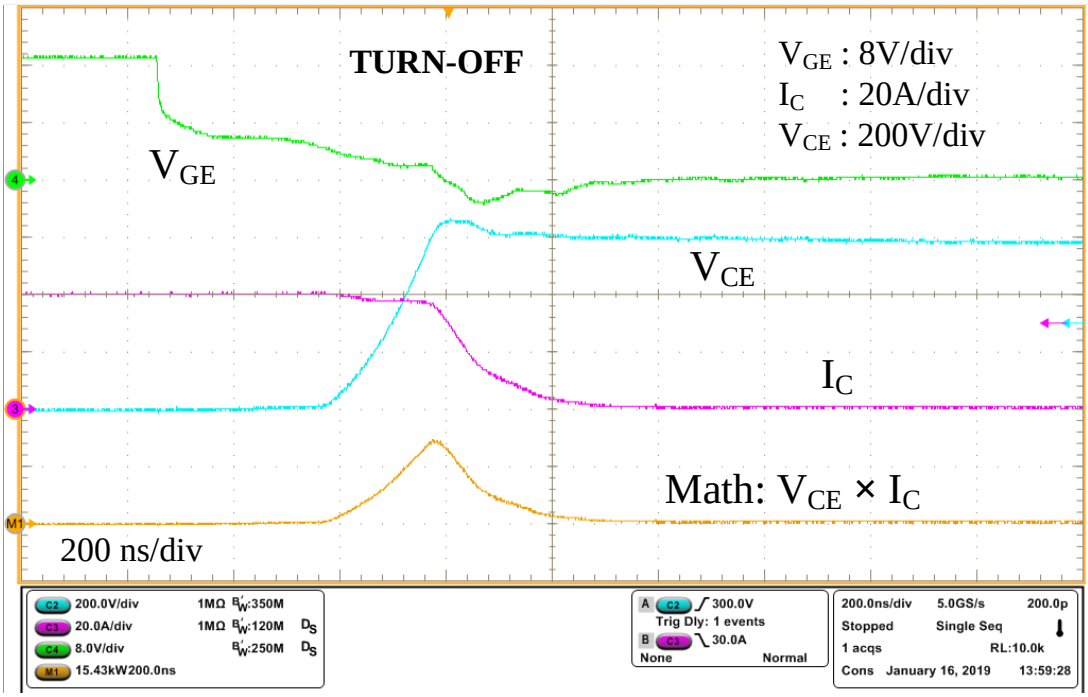
Table 5.2 Key parameters used in experimental result analysis

Parameters	**Symbol**	**Typical Units**
Collector-emitter voltage	V_{CE}	V (volts)
Gate voltage	V_{GE}	V
Collector current	I_C	A (ampere)
Gate resistance	R_g	Ω (ohm)
Case temperature	T_C	°C (degree Celsius)
Rise time	t_{rise}	ns (nano-seconds)
Fall time	t_{fall}	ns
Turn-on switching energy loss	E_{on}	mJ (milli-joule)
Turn-off switching energy loss	E_{off}	mJ
Total switching energy loss	E_{total}	mJ
Turn-on current slope/speed	$di/dt_{(on)}$	A/µs (amperes per micro-second)
Turn-on voltage slope/speed	$dv/dt_{(on)}$	V/ns (voltage per nano-second)
Turn-off current slope/speed	$di/dt_{(off)}$	A/µs
Turn-off voltage slope/speed	$dv/dt_{(off)}$	V/ns
Stray inductance voltage drop	V_σ	V

An Infineon 1200V 40A standard TO-247 style 3-pin IGBT, IKW40T120 is characterized with clamped inductive load under hard-switching conditions. The same IGBT is used as high side device. The typical turn-on and turn-off behavior of the IGBT for test conditions: V_{CE}=600V, I_C=40A, T_C=150°C, R_g=15Ω, V_{GE}=0/+15V, is shown in Figure 5.2 (a) and (b) respectively. The math channel represents the power loss i.e. the overlap of the current and voltage waveforms during the switching events. Area under the power loss curve represents the switching energy loss.



(a)



(b)

Figure 5.2 Typical switching performance of DUT with inductive load recorded during double pulse test: (a) Turn-on, (b) Turn-off transient.

5.2.1 Switching results Vs. Device current

The DUT is tested in a range of load currents i.e. from 10A to 60A to observe the variation in dynamic performance with respect to device current. The tests are conducted at 600V device voltage, 25°C case temperature with a gate resistance of 15Ω. The effect of load current on the switching time and energy losses of the device can be observed from Figure 5.3 below.

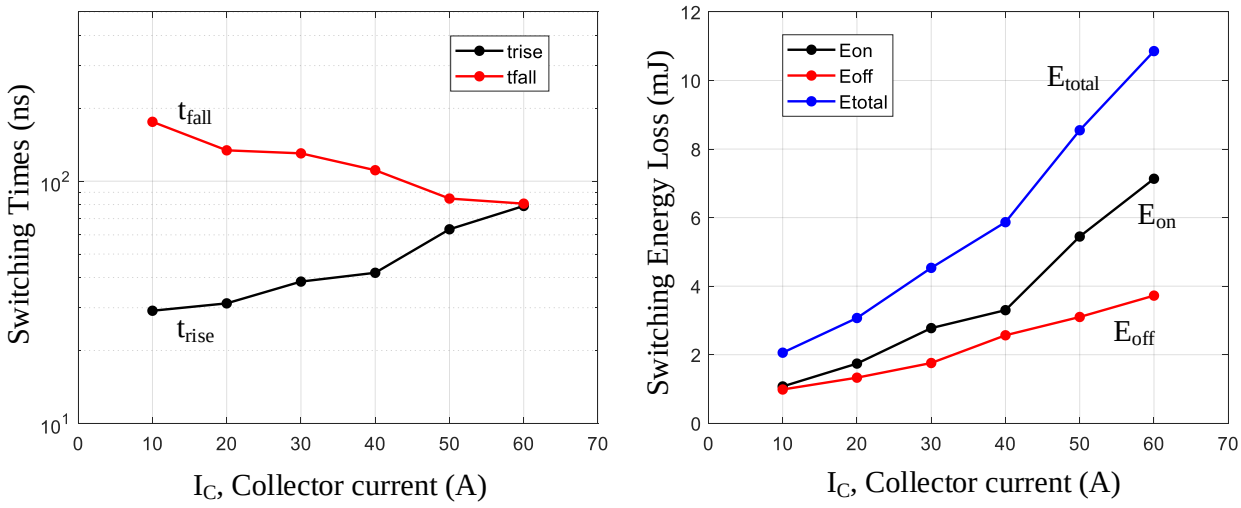


Figure 5.3 Switching data plotted against collector current: (a) Switching times, (b) Switching Energy Loss; test conditions: V_{CE}=600V, T_C=25°C, Rg=15Ω, V_{GE}=0/+15V.

Figure 5.3 (a) shows the rise time, t_{rise} and fall time, t_{fall} of the device i.e. the turn-on time and turn-off time respectively as a function of different load currents. As seen in the figure, both turn-on and turn-off times share almost a linear relationship with load current. t_{rise} increases with increase in load current whereas t_{fall} exhibit an opposite behavior by gradually decreasing with increase in load current. This behavior can be explained with the theory behind the charging and discharging of capacitances associated with gate terminal of an IGBT. With reference to Figure 2.7, the effective input capacitance of an IGBT, C_{ies} is the sum of the gate to collector capacitance,

C_{gc} and the gate to emitter capacitance, C_{ge}. The input capacitance must be charged to the threshold voltage for the device to turn-on, and discharged to the plateau voltage before the device begins to turn-off [63]. As the plateau voltage increases with load current, the gate discharge current increases thereby expediting the turn-off process. This is the reason the turn-off time reduces with increase in load current.

Figure 5.3 (b) presents the relationship between switching energy losses and collector current. The turn-on switching energy studied here i.e. E_{on} is the clamped inductive turn-on energy that includes the effects of the high-side device's commutating diode reverse recovery current on the DUT's turn-on switching loss. Again, both switching energy losses, E_{on} and E_{off} have more or less linear relationship with load current. Both the losses rise with increase in load current, which is in accord with the standard conception, however the rate of rise of E_{off} is lower than that of E_{on} due to reduction in t_{fall} for high load currents.

5.2.2 Switching results Vs. Case Temperature

The DUT is characterized in a wide span of operating temperature i.e. from 25°C to 150°C by adjusting its case temperature using the DUT heating unit. The switching results obtained are presented with multiple plots depending on the parameter being studied. The DUT case temperature is monitored using a Fluke 52 Thermometer as well as a Fluke TiS40 Infrared Camera/Thermal Imager. The thermocouple temperature sensor of the thermometer is inserted within the DUT heating block. The reading from the thermometer and the thermal imager has a close match and it is used to calibrate the temperature sensor on the DPT control broad. This approach improves the accuracy of the measurements fed to the controller and helps in precise

control of the DUT case temperature during the double pulse tests. A thermal image captured during dynamic characterization test at 150°C is shown in Figure 5.4.

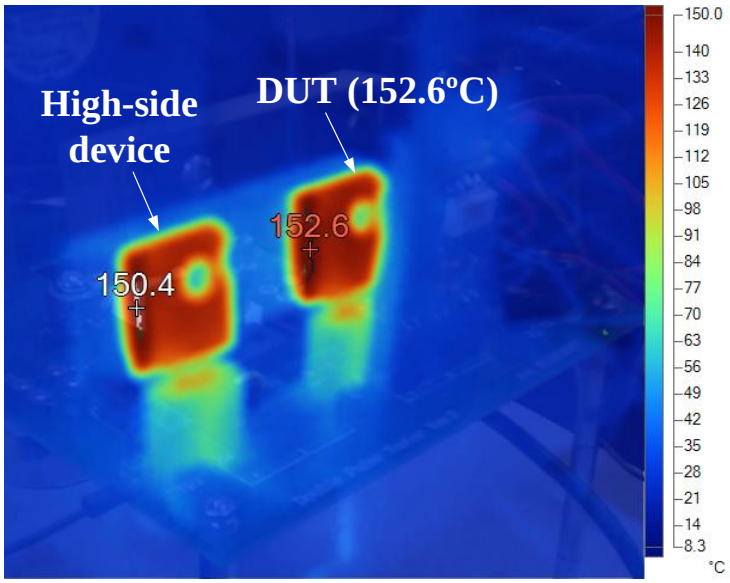
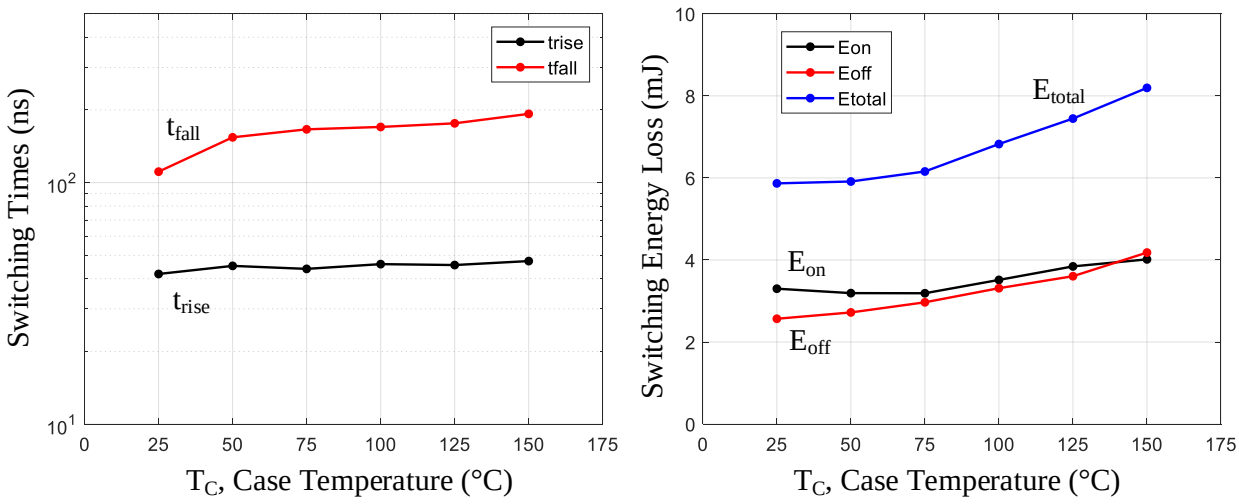


Figure 5.4 Thermal Image of DUT and high-side device captured during double pulse test, test condition: V_{CE} = 600V, I_C = 40A, R_g = 15Ω, T_C = 150°C, V_{GE} = 0/+15V.

The relationship between switching time and energies to case temperature can be visualised in Figure 5.5. In general, turn-on time is relatively independent of temperature [63], or actually increasing very slightly with increasing temperature. This theory is experimentally verified and can be observed from the trajectory of the t_{rise} line in Figure 5.5 (a). In this study, E_{on} includes the commuting diode reverse recovery current in the DUT turn-on switching loss. The diode reverse recovery current increases with temperature, which causes E_{on} to increase as well. The turn-off time, t_{fall} increases (decrease in speed) with increasing temperature, resulting in the increase of E_{off} with rise in temperature. E_{total} , being the cumulative switching energy from the turn-on and off switching events naturally increases as well with temperature. Both the phenomenon described above can be observed in Figure 5.5 (b).



(a) (b)

Figure 5.5 Switching data plotted against collector current: (a) Switching times, (b) Switching Energy Loss, test conditions: V_{CE} = 600V, I_C = 40A, R_g = 15Ω, V_{GE} = 0/+15V.

The behavior of turn-on and turn-off switching transients with respect to change in case temperature is explored in Figure 5.6 and Figure 5.7 respectively. The test voltage, collector current and gate resistance are kept constant during these temperature-varied tests. The gate voltage is taken as a reference to superimpose the waveforms for different temperature.

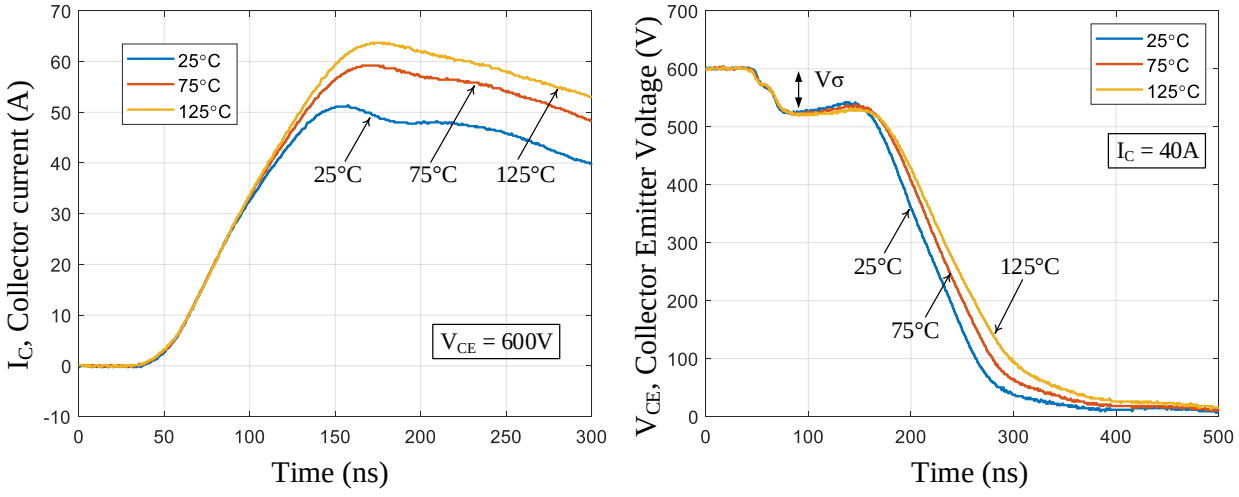


Figure 5.6 Switching transient behavior under different case temperatures during DUT turn-on; test conditions: V_{CE} = 600V, I_C = 40A, R_g = 15Ω, V_{GE} = 0/+15V.

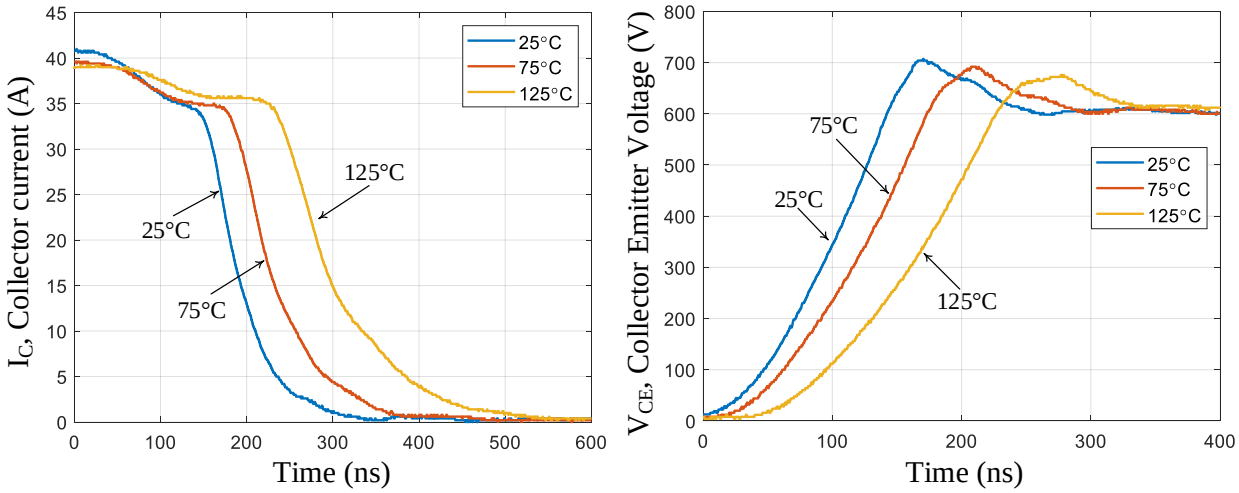


Figure 5.7 Switching transient behavior under different case temperatures during DUT turn-off; test conditions: V_{CE} = 600V, I_C = 40A, R_g = 15Ω, V_{GE} = 0/+15V.

The switching parameters from the turn-on and turn-off switching waveforms in Figure 5.6 and Figure 5.7 are summarized in Table 5.3 below.

Table 5.3 Switching parameters for change in case temperature

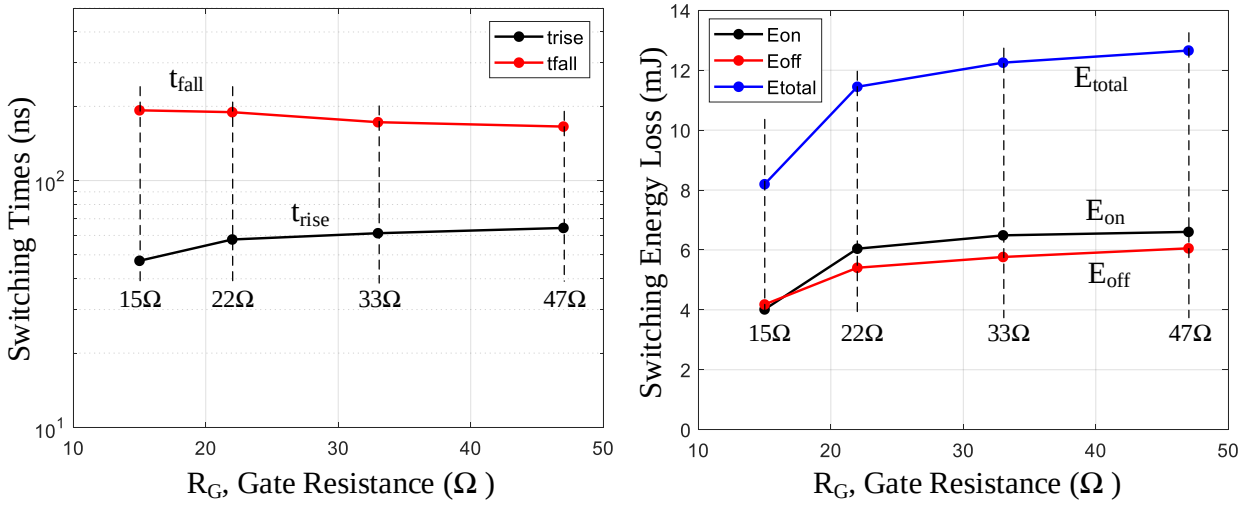
Parameters	**25°C**	**75°C**	**125°C**
$di/dt_{(on)}$	615 A/μs	618 A/μs	621 A/μs
$dv/dt_{(on)}$	– 4.03 V/ns	– 3.5 V/ns	– 2.8 V/ns
$di/dt_{(off)}$	– 343 A/μs	– 250 A/μs	– 187 A/μs
$dv/dt_{(off)}$	4.8 V/ns	4.1 V/ns	3.5 V/ns
E_{on}	3.3 mJ	3.2 mJ	3.8 mJ
E_{off}	2.6 mJ	3 mJ	3.6 mJ
V_σ	76 V	77 V	80 V

From the waveforms in Figure 5.6 and corresponding values in Table 5.3, we can see that the turn-on current speed $di/dt_{(on)}$ and energy E_{on} are relatively independent of temperature or actually increasing very slightly with increasing temperature. However, the DUT collector current

overshoot in Figure 5.6 is observed to increase with temperature, which is due to increase in diode reverse recovery current of high side device. To summarize the turn-off behavior, both current and voltage speed, $di/dt_{(off)}$ and $dv/dt_{(off)}$ clearly decreases with increasing temperature resulting in an increase in turn-off energy E_{off}.

5.2.3 Switching results Vs. Gate resistance

The switching speed of power semiconductor devices can be adjusted by changing the gate drive resistances. In order to investigate the change in the DUT's dynamic performance with gate resistance, a set of test is conducted with different gate resistances. The presence of gate resistor sockets in the DUT power board allow easy replacement of through-hole resistors. The switching time and energy data obtained from the characterization tests are presented in Figure 5.8.



(a) (b)

Figure 5.8 Switching data plotted against gate resistances: (a) Switching times, (b) Switching Energy Losses, test conditions: V_{CE} = 600V, I_C = 40A, T_C = 150°C, V_{GE} = 0/+15V.

The behavior of turn-on and turn-off switching transients with respect to change in gate resistance is explored in Figure 5.9 and Figure 5.10 respectively. The test voltage, collector current and case

temperature are kept constant during these tests. The gate voltage is taken as a reference to superimpose the waveforms for different gate resistances.

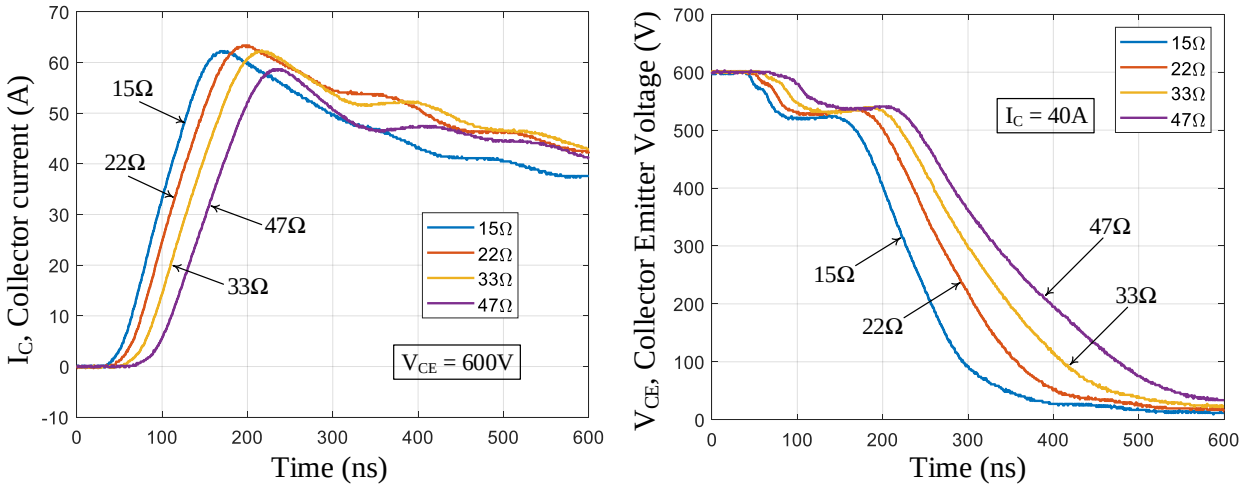


Figure 5.9 Switching transient behavior under different gate resistances during DUT turn-on; test conditions: V_{CE} = 600V, I_C = 40A, T_C = 150°C, V_{GE} = 0/+15V.

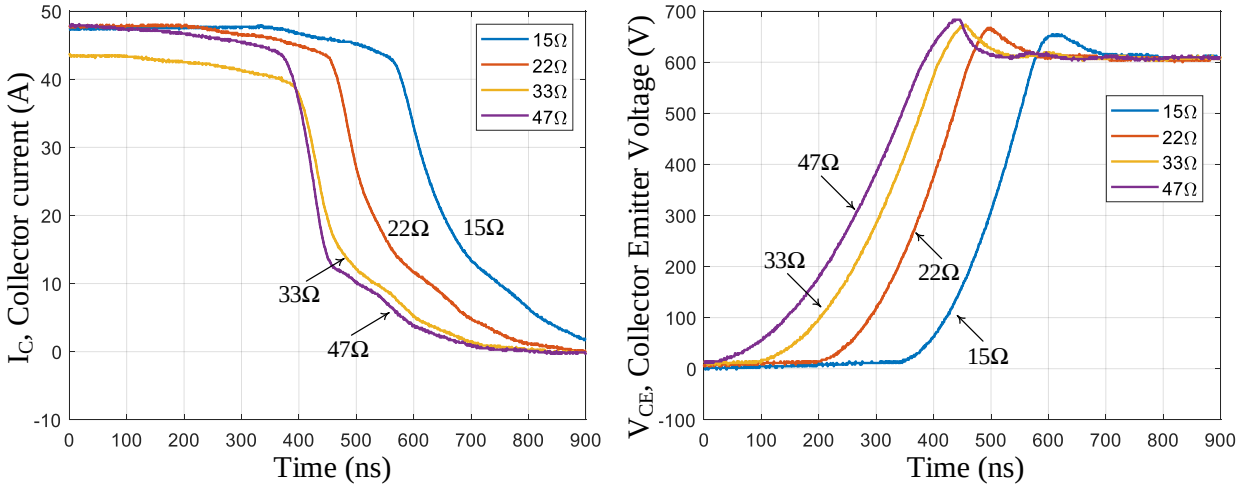


Figure 5.10 Switching transient behavior under different gate resistances during DUT turn-off; test conditions: V_{CE} = 600V, I_C = 47A, T_C = 150°C, V_{GE} = 0/+15V.

The switching parameters from the turn-on and turn-off switching waveforms in Figure 5.9 and Figure 5.10 are summarized in Table 5.4 below.

Table 5.4 Switching parameters for change in gate resistances

Parameters	15Ω	22Ω	33Ω	47Ω
$di/dt_{(on)}$	610 A/µs	554 A/µs	508 A/µs	460 A/µs
$dv/dt_{(on)}$	– 3 V/ns	– 2.5 V/ns	– 2.1 V/ns	– 1.7 V/ns
V_{σ}	78 V	71 V	67 V	58 V
$di/dt_{(off)}$	– 143 A/µs	– 156 A/µs	– 157 A/µs	– 180 A/µs
$dv/dt_{(off)}$	3 V/ns	2.6 V/ns	2.2 V/ns	1.9 V/ns
E_{ON}	4.02 mJ	6.04 mJ	6.49 mJ	6.6 mJ
E_{OFF}	4.18 mJ	5.4 mJ	5.8 mJ	6.1 mJ

When the gate resistance is increased, the current flowing into the gate of the DUT reduces. The reduced current takes more time to charge the gate capacitances. Hence, in Table 5.4 we see a decreasing trend in the switching speed, both turn-on and turn-off, with increase in gate resistance. This means the current and voltage slopes can be controlled by changing the gate resistance. To summarize, switching transient speeds are reduced as the gate resistance increases. Due to reduction in switching speed with rise in resistances, both the switching energies increase.

5.2.4 High-side device measurements

In the above tests, same IGBTs are used as DUT as well as high side device in the half-bridge configuration. The anti-parallel diode of the high side IGBT forms a switching cell with the low side IGBT i.e. the DUT. The dynamic behavior of the DUT affect the switching performance of the diode, and the switching behavior of the diode reflect back to the DUT. Thus their dynamic behaviors are interrelated. For an instance, in the above analysis, we have seen how the diode reverse recovery current affect the switching energy losses at DUT turn-on. A cut-out provision kept in the DPT power board, as seen in Figure 2.8, allow an user to insert a current sensor and

monitor the diode current. A zoomed out (500ns/div) oscilloscope capture is shown in Figure 5.11 to display the high side device behavior during DUT turn-on.

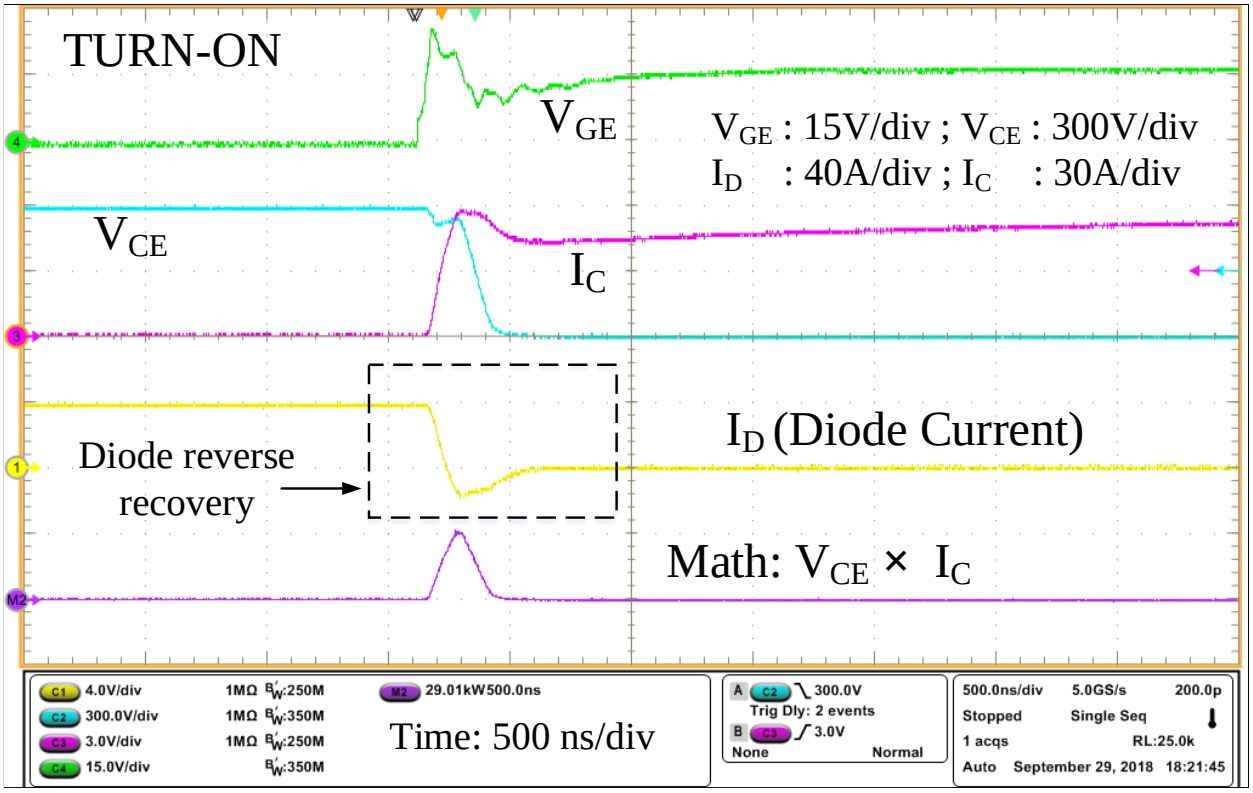


Figure 5.11 Switching transient behavior during DUT turn-on; test conditions: V_{CE} = 600V, I_C = 40A, T_C = 25°C, R_g = 15Ω, V_{GE} = 0/+15V.

The diode current switching transient window shown in Figure 5.11 is magnified and plotted in Figure 5.12 in order to investigate the switching characteristics of the anti-parallel diode in detail. When the low side DUT turns on, the freewheeling current retreats from the diode and starts to flow through the DUT. This is when the anti-parallel body diode of the high side IGBT undergoes reverse recovery. The parameters of interest from the reverse recovery period is showed in Figure 5.12.

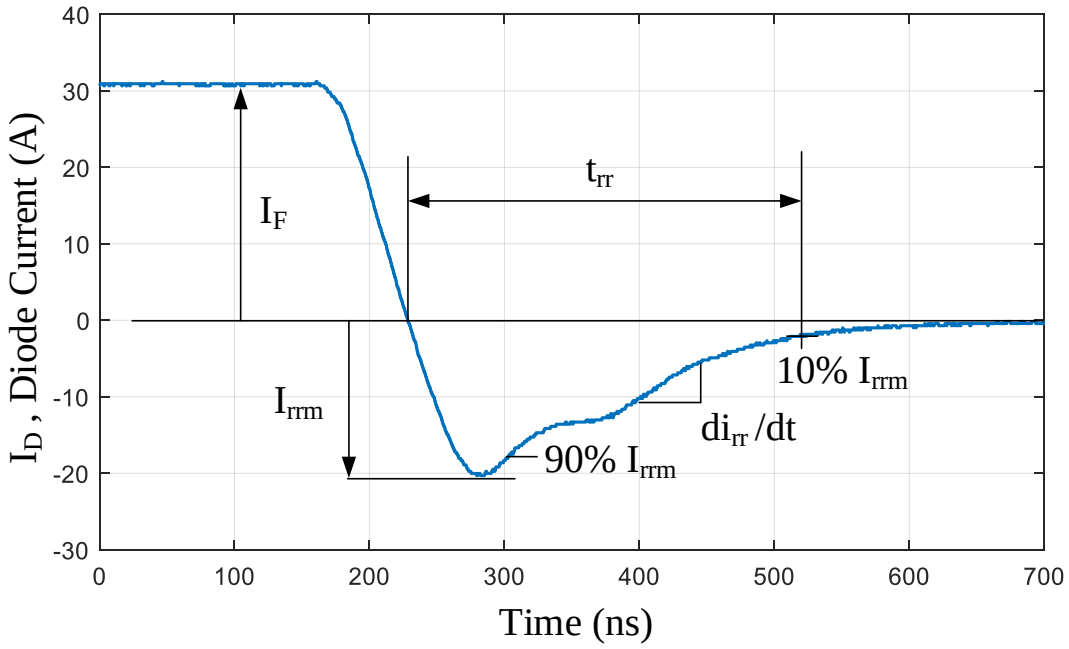


Figure 5.12 Switching transient characteristics of high side device anti-parallel diode; test conditions: V_{CE} = 600V, I_C = 35A, T_C = 25°C, R_g = 15Ω, V_{GE} = 0/+15V.

The values of diode switching parameters for test conditions in Figure 5.11 and Figure 5.12 are measured and presented in Table 5.5.

Table 5.5 Key parameters measured for Anti-parallel Diode

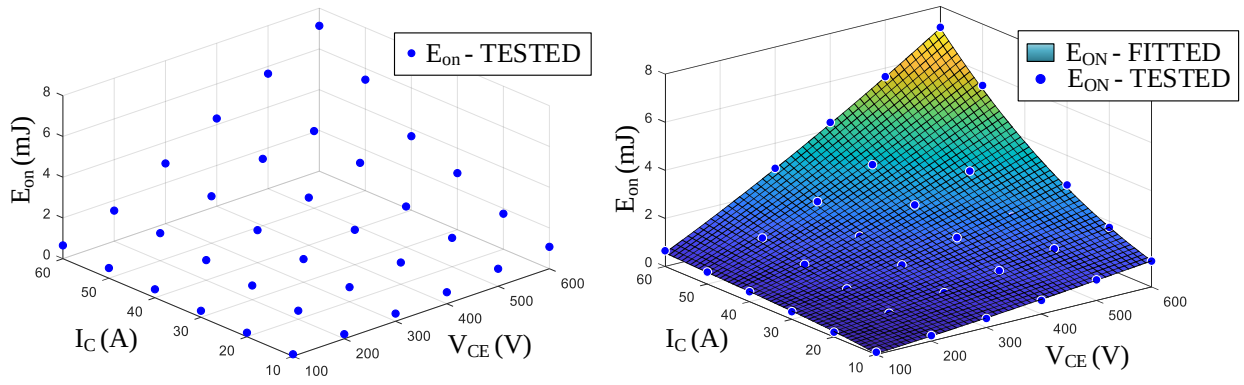
Parameters	**Symbol**	**Values**
Diode forward current	I_F	31 A
Diode peak reverse recovery current	I_{rrm}	20 A
Diode reverse recovery current slope	di_{rr}/dt	73 A/μs
Diode peak reverse recovery time	t_{rr}	291 ns

I_{rrm} increases with increase in DUT case temperature causing significant rise in switching energy losses. However, the continual drive for improving converter efficiency and the advent of WBG semiconductor materials have led to significant improvement in diode technologies. The latest SiC

Schottky barrier diodes have shorter t_{rr} and lower/almost negligible I_{rrm} because of which they are capable of reducing E_{on} by almost two-third compared to a Si fast recovery diode [64].

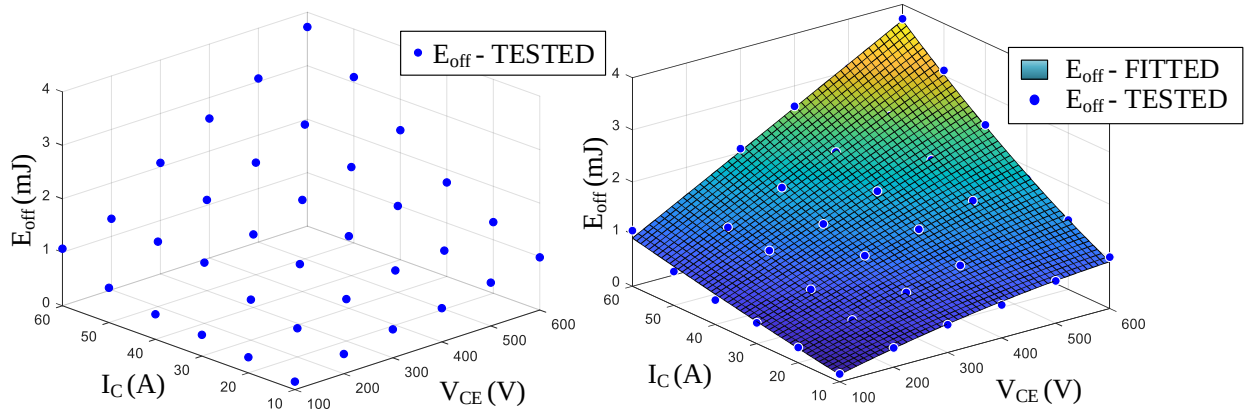
5.2.5 Additional Switching results

The dynamic data given in any device datasheet is restricted to certain test conditions such as fixed test current, voltage, gate resistances, case temperatures etc. However, for obvious reasons a real life application may be different from the datasheet test condition. In the absence of a dynamic characterization tool, the data switching data is usually scaled or extrapolated for variation between any application voltage and datasheet test condition [63]. This approach is purely an estimation method and the obtained values might differ from practical test values. However, the proposed DPT can be used to emulate the application conditions and evaluate the dynamic performance of the DUT accordingly. A chosen device can be characterized in a wide span of test conditions to obtain practical experimental data. The tested data points can be surface fitted to obtain 3D plot of switching energies against different test voltage and currents. This could serve as a loss data library for converter design calculations and such libraries may be linked with transient simulation softwares to obtain more practical simulation data. To demonstrate the described idea, the turn-on and turn-off switching energies obtained from the IGBT characterization tests are plotted against collector voltage and current and presented in Figure 5.13 and Figure 5.14 below.



(a) (b)

Figure 5.13 E_{on} plotted against V_{CE} and I_C, (a) Experimental data points, (b) Surface fitted values; test condition T_C = 25°C, R_g = 15Ω, V_{GE} = 0/+15V.



(a) (b)

Figure 5.14 E_{off} plotted against V_{CE} and I_C, (a) Experimental data points, (b) Surface fitted values; test condition T_C = 25°C, R_g = 15Ω, V_{GE} = 0/+15V.

5.3 Case Study – Switching cell in Boost converter

In order to verify the results obtained from the designed DPT, the author collaborated with a fellow research assistant to gather experimental data from a boost converter operated with the same switching cell (Infineon IGBT IKW40T120 as both high side and low side device). The switching cell in classical dc-dc converters including boost converter has already been introduced and shown

in Figure 1.7. The oscilloscope waveforms recorded during steady state operation of the boost-converter is shown in Figure 5.15. The turn-on and turn-off switching windows are highlighted. A closer magnified look on these windows reveals the dynamic behavior of the switching cell.

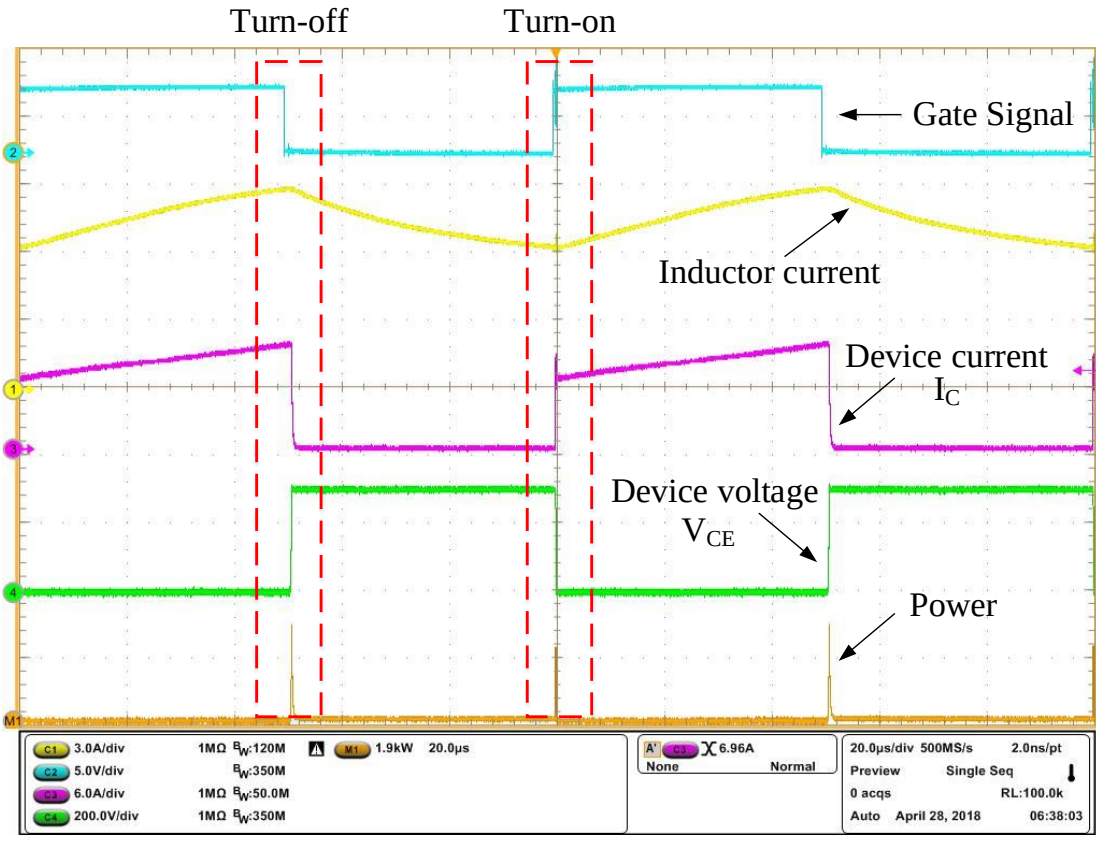
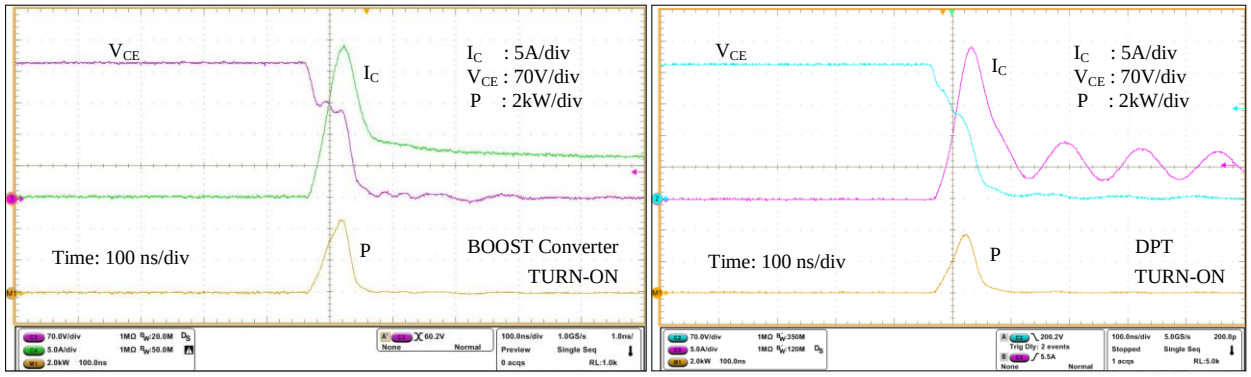


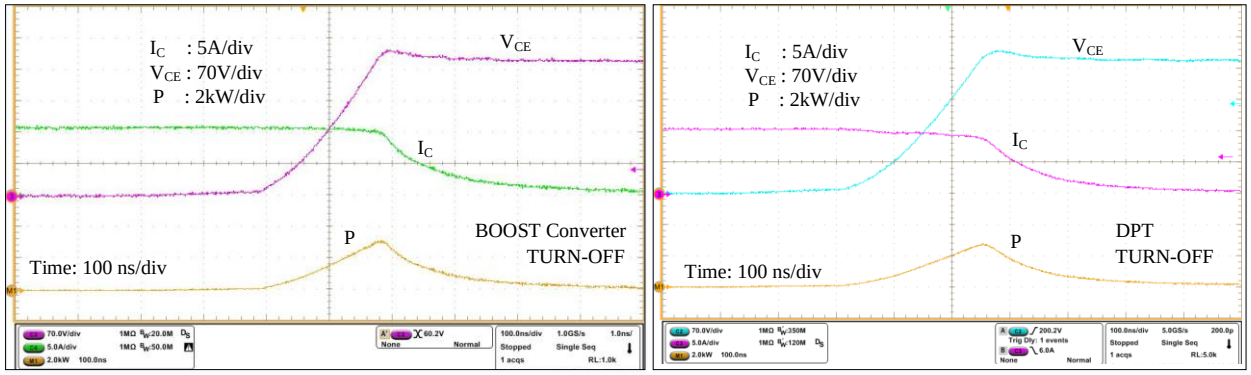
Figure 5.15 Turn-on and turn-off switching transients in boost converter steady state operation.

The test is conducted at the maximum output voltage of the boost converter i.e. 300V however due to the power rating of the DC input supply, the maximum test current is limited to 10 A. The DUT heats up during continuous operation in the boost converter hence the temperature of the DUT is monitored while recording the switching waveforms. While testing the switching cell in the DPT, it is subjected to same voltage, current and temperature conditions with that of the boost converter operation in order to compare the results. The results are presented in Figure 5.16 and Figure 5.17. The thermal images showing DUT operating at 80°C for both setups are shown in Figure 5.18.



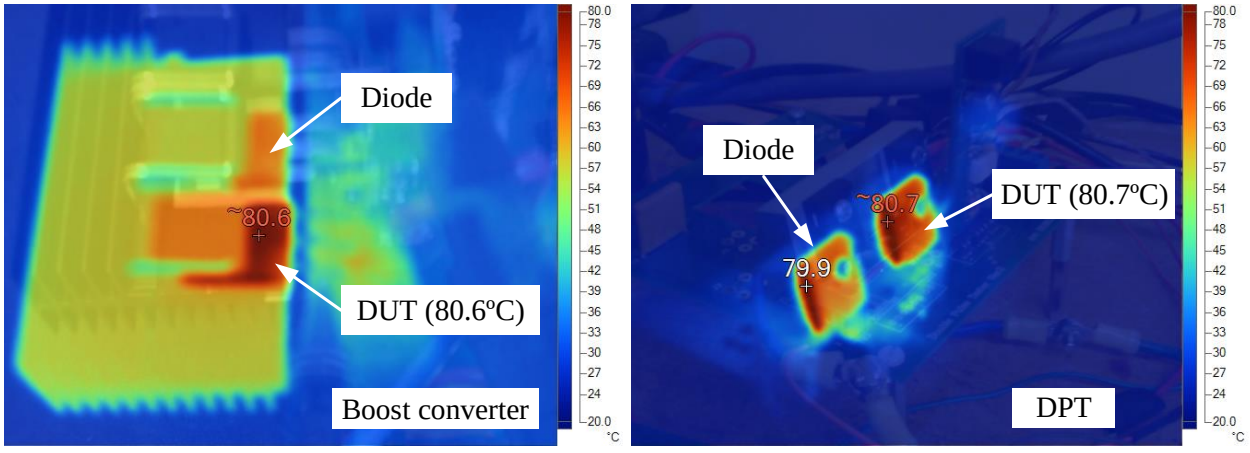
(a) (b)

Figure 5.16 Turn-on switching transient, (a) Boost converter, (b) DPT.



(a) (b)

Figure 5.17 Turn-off switching transient, (a) Boost converter, (b) DPT.



(a) (b)

Figure 5.18 Thermal image of switching cell, (a) Boost converter, (b) DPT.

From the above figures, the switching parameters for both turn-on and turn-off transients are extracted and summarized in Table 5.6. The test conditions for turn-on waveforms in Figure 5.16 is 300V, 6A, 80°C and for turn-off waveforms in Figure 5.17 is 300V, 10A, 80°C both with gate resistances of 15Ω and 0/+15V gate drive.

Table 5.6 Switching parameter comparison between Boost converter and DPT

Parameters	**Boost Converter**	**DPT**	**Difference**
Rise Time	13 ns	14 ns	1 ns
Fall Time	263 ns	260 ns	3 ns
Turn-on Energy Loss	0.203 mJ	0.196 mJ	0.007 mJ
Turn-off Energy Loss	0.578 mJ	0.568 mJ	0.010 mJ

From the figures as well as values of switching parameters in Table 5.6, it can be concluded that the DPT test results are in good agreement with that of the boost converter results for similar operating condition of the switching cell. There are multiple factors that can justify the difference noted in the switching values of DPT and boost converter. Primarily, devices of same model number from a manufacturer may slightly vary from one another in terms of material behavior due to process variation during device fabrication. The fabrication process variation can cause measurable variance in the output performance of the device. The IGBTs used in the boost converter and DPT have the same model number however they are not exactly the same device. Secondly, the physical layout of the DPT power board and the boost converter power-circuit is different. The variation in parasitic inductances in the power loop in both applications will affect the switching behavior of the DUT differently. However, it is demonstrated that the DPT can closely emulate the performance of a switching cell in a real converter and can estimate the switching time and losses with a low error margin.

5.4 WBG device characterization

The DPT power board shown in Figure 2.6 is used to characterize TPH3208PS, a 650V, 20A GaN FET of through-hole TO-220 package from Transphorm. IDH12G65C6 SiC Schottky Diode from Infineon is used as an upper side device to ensure zero reverse recovery. In order to compare the switching performance of Si device and GaN FET, the same Si IGBT IKW40T120 (Infineon) is used. Both the devices are characterized at similar test conditions i.e. at 100V, 10A, 27°C, Rg = 22Ω. The turn-on and turn-off performances of both these devices are presented in Figure 5.19 and Figure 5.20 respectively. The switching energy losses, rise and fall times from these tests are summarized in Table 5.7.

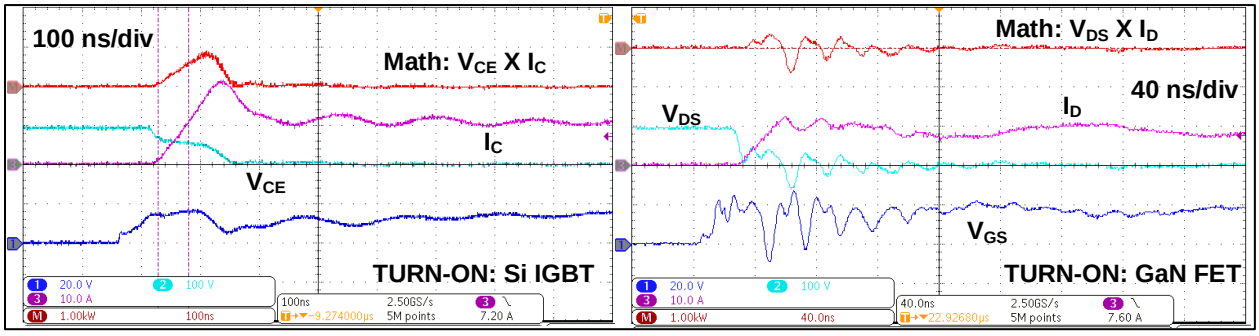


Figure 5.19 Turn-on performance of Si IGBT and GaN FET at 100V, 10A, 27°C, Rg = 22Ω.

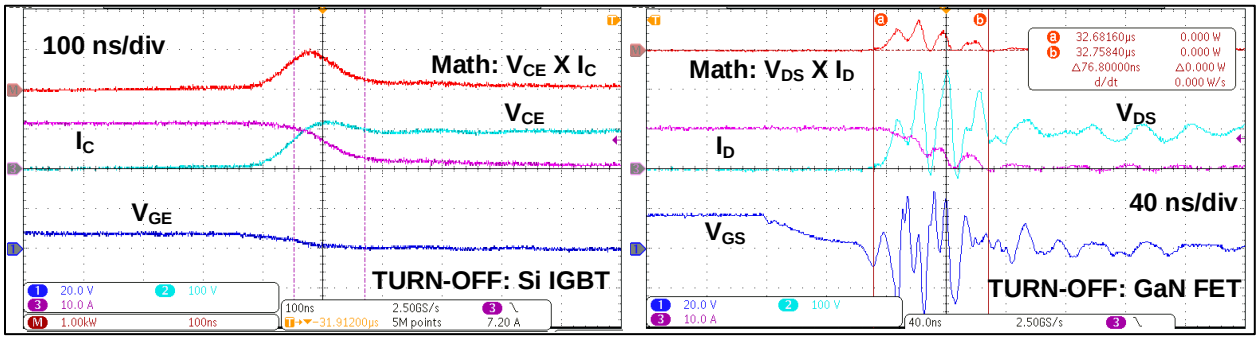


Figure 5.20 Turn-off performance of Si IGBT and GaN FET at 100V, 10A, 27°C, Rg = 22Ω.

Table 5.7 Switching performance comparison between Si IGBT and GaN FET

Parameters	**Si IGBT**	**GaN FET**
Rise Time	52.3 ns	4.9 ns
Fall Time	119.1 ns	9.34 ns
Turn-on Energy Loss	80.86 µJ	2.18 µJ
Turn-off Energy Loss	167.6 µJ	34.36 µJ

The significant difference in switching figures in the above table are clear indication of the superior performance of a GaN FET in comparison with a Si IGBT. However, for same test conditions, it is observed that the PCB layout that results in clean switching waveforms for a Si IGBT causes considerable gate ringing for a GaN FET. The cut-outs kept for current monitor insertion, the sockets for switching cell replacement, sockets for gate resistances and the leads of through-hole gate resistors introduce parasitic inductances that highly affect the high speed switching transients of the GaN device and causes considerable high frequency ringing in the gate voltage. This can be clearly observed from Figure 5.19 and Figure 5.20. This test implies that GaN devices require much more compact power and gate loops as compared to the dimensions shown in Figure 2.8. A possible future work may include designing a new DPT power board with compact power and gate drive loops using SMD components to test the latest WBG devices.

5.5 Chapter Summary

Switching times and energies can significantly vary with the stray inductances in the power and gate drive circuit. In particular, the parasitic inductance in series with the emitter/source of the device significantly affect the switching results. Therefore, the switching data obtained from a device datasheet are representative and reference only. It may vary from values obtained from a real life converter application. Moreover, the information in a typical datasheet is limited to certain test conditions, which may differ from the operating conditions of a desired application. The proposed DPT facilitates effortless characterization of devices in user specified test conditions, which results in more practical switching results rather than scaling or extrapolating the datasheet values. In this chapter, a switching cell in phase leg configuration is characterized which includes a Si IGBT as low side DUT and the anti-parallel diode of a same IGBT as high side device. The dynamic performance of the switching cell is studied under a wide range of operating conditions. The characterization tests are conducted with different values and permutation of all possible test parameters such as test voltage, current, case temperature, gate resistances in order to investigate the effect of these parameters on the switching performance of the device. The data recorded during the tests are processed and presented through multiple plots and figures that describe the dynamics of the DUT. The switching results are analysed and found in good agreement with typical behavior of an IGBT. It is also explained how switching databases can be built by gathering data over a wide range of test conditions. Likewise, any DUT can be tested using the proposed setup to obtain practical switching result that is specific to the application of the device. This successfully demonstrates the operation as well as the intent for developing the proposed DPT.

Chapter 6 Conclusions and Future Work

6.1 Conclusion

In this thesis, topics related to development of an automatic Dynamic Characterization Platform for evaluating the switching behavior of power semiconductor devices are addressed. An extensive investigation of the existing setups and technologies in both industry and academia is conducted through review of technical recent literatures such as scientific publications and application notes from device manufacturers. The shortcomings of the conventional characterization setups identified during the literature review served as a basis for conceiving the original research idea as well as the motivation for this research work.

The main conclusions and contributions of this thesis are summarized as follows:

- Semiconductor device characteristics directly influence the performance of power electronics converters. For an optimized converter design, we need to know the dynamic characteristics of semiconductors precisely, e.g. switching losses can be estimated by the information, and it can used to design a high sink for the system. Considering the fact that a typical device datasheet provides switching results for only specific operating conditions, an advanced semiconductor characterization tool is required that allows an user to evaluate switching performance at any desired test condition. There is no standard equipment available for such testing. Typically, a dynamic characteristic test setup, namely double pulse tester (DPT), is the way to extract this information from semiconductor devices. The setup is tailor-made for a newly developed semiconductor. This thesis summarizes the pros and cons of the conventional setups and presents an optimized, cost-effective and automatic test solution.

- As opposed to conventional DPT setups that are expensive and consume considerable bench space due to presence of several peripheral equipments, the proposed setup uses a newly designed central control unit that scales down the overall test setup footprint substantially by replacing bulky support instruments, however to perform the same tasks in a much efficient manner. The idea of designing a compact and automatic test setup has been materialized with the implementation of the control board. Moreover, to facilitate dynamic characterization of different kinds of switching devices, the power stage is implemented as a separate module. A power board suitable for the device being tested can be interfaced with the mother control board for conducting the test. The detail design of the control and power boards are explored in Chapter 2.

- The switching behavior of the DUT can be greatly affected by the parasitic inductances of the DPT power loop. Hence, the physical layout of the power PCB needs to be carefully designed in order to reduce the effects of the parasitic elements and to harness the full advantage of the latest fast switching devices. The PCB layout optimization techniques are discursively investigated in Chapter 2.

- The significant role played by the control system in achieving automation in the double pulse testing process is explained in Chapter 3. The test control software developed in Microsoft Visual Studio features a user-friendly GUI and co-ordinates the overall test process by communicating with the microcontroller on-board the DPT control board as well the oscilloscope. The GUI serves as an excellent communication window between the operator and the DPT control system allowing full human control and monitoring of the testing process. The systematic control operations performed by the control board

microcontroller starting from preparation of test bed until conducting of tests are individually discussed.

- A smart data processing program is developed in MATLAB to process the vast test data recorded during double pulse tests. The program scans through the test waveforms and identify key points for calculating switching results as per relevant switching definitions. This approach saves time and effort and enables accurate estimation of switching losses. This program has been used to process the test results from DPT demonstration tests and results presented and discussed in Chapter 5.

- The research work has successfully met one of the research objectives i.e. to establish automation in all the major test segments of the switching characterization process i.e. test control, double pulse testing, data acquisition and data processing. Unlike the conventional test setups which involves human involvement in every stage of the testing process, the proposed setup can prepare the test bed, calculate the pulse widths, run the test, capture the waveforms and process it automatically once an operator has entered the test parameters in a GUI. This approach saves significant amount of labour and has reduced the testing time to a great extent. An example of typical testing time taken by the proposed setup to characterize a power semiconductor for a given set of test conditions is discussed Chapter 3 , Section 3.2

- This thesis has provided an understanding of the trade-offs involved in the design process of an universal test bench. In certain instances, a choice has to be made between absolute test accuracy and convenience. However, it is discussed how the choice can be made based on the device being tested. The hardware designs produced out of this research work will

serve as a good reference for physical layout design of PCB, gate drive circuitries in a power electronic converter.

- This thesis has enabled other researches in device modelling domain. The practical test results obtained from the proposed DPT platform have been used to develop thermal and transient models of semiconductor switching devices for Electromagnetic transient simulation software PSCAD. As opposed to a lossless model, this new model closely emulates the performance of a real semiconductor in terms of its loss behavior and produces practical simulation results. The research output has been transferred to local industry i.e. HVDC research centre for enhancing the semiconductor models in the PSCAD library. The research output has been published in relevant literatures as well [17].

- This test platform allows the testing of the latest Wide Bandgap devices. As the application of these semiconductors is still in its infancy, this presents a great opportunity to establish a leadership position in this area. The research project has provided practical training experience to the author as well as undergraduate summer students, which will allow them to excel in hardware implementation techniques in their future research pursuits.

6.2 Future Work

As with any study, the work presented in this thesis can be extended. Several extensions of this thesis can be suggested in the following ways:

- So far, a semiconductor interface board suitable for testing TO-247/TO-220 style devices have been built and tested in order to demonstrate the operation of the proposed DPT setup. In future, new power interface boards unique for different semiconductor devices including

the latest wide bandgap devices can be built. These new interface boards can be connected with the universal mother control board and more devices can be tested.

- During this thesis work, the DPT control board has been implemented with mostly through-hole components for ease of testing and debugging at the development stage. Now that the design principles are verified, the control board can be redesigned with surface mount components, which will result in considerable reduction of board size. To give the setup a more professional outlook, the control board can be covered with a metal case with dedicated connectors for input-output connections.

- The widely used, popular switching devices can be dynamically characterized over a wide span of operating conditions using the proposed DPT setup to create a database of switching data. These devices can be of various semiconductor technologies such as Si, SiC, GaN etc., different packages i.e. through-hole or surface mount and of different ratings.

- The switching data/database obtained from this DPT setup can be used to create Look Up Tables (LUT) which can then be transferred to power electronic and power systems electro-magnetic transient (EMT) simulation environments. As opposed to the results obtained from conventional switch models currently available in the simulation software libraries, this approach will allow an user to get more practical simulation data.

References

[1] J. Millán, "A review of WBG power semiconductor devices," *CAS 2012 (International Semiconductor Conference)*, Sinaia, 2012, pp. 57-66.

[2] B. K. Bose, "Power Electronics, Smart Grid, and Renewable Energy Systems," in *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2011-2018, Nov. 2017.

[3] S. Mao, R. Ramabhadran, J. Popovic and J. A. Ferreira, "Investigation of CCM boost PFC converter efficiency improvement with 600V wide band-gap power semiconductor devices," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 388-395.

[4] S. Mao, T. Wu, X. Lu, J. Popovic and J. A. Ferreira, "Three-phase active front-end rectifier efficiency improvement with silicon carbide power semiconductor devices," 2*016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Milwaukee, WI, 2016, pp. 1-8.

[5] R. A. Barrera-Cardenas, T. Isobe and M. Molinas, "Meta-parameterisation of power semiconductor devices for studies of efficiency and power density in high power converters," *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, 2016, pp. 1-10.

[6] J. C. Balda and A. Mantooth, "Power-Semiconductor Devices and Components for New Power Converter Developments: A key enabler for ultrahigh efficiency power electronics," in *IEEE Power Electronics Magazine*, vol. 3, no. 2, pp. 53-56, June 2016.

[7] T. P. Chow, "Wide bandgap semiconductor power devices for energy efficient systems," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 402-405.

[8] Sei-Hyung Ryu et al., "2 kV 4H-SiC DMOSFETs for low loss, high frequency switching applications," *Proceedings. IEEE Lester Eastman Conference on High Performance Devices*, 2004., Troy, NY, 2004, pp. 255-259.

[9] Z. J. Shen, Y. Xiong, X. Cheng, Y. Fu and P. Kumar, "Power MOSFET Switching Loss Analysis: A New Insight," *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*, Tampa, FL, 2006, pp. 1438-1442.

[10] Y. Xiong, S. Sun, H. Jia, P. Shea and Z. John Shen, "New Physical Insights on Power MOSFET Switching Losses," in *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 525-531, Feb. 2009.

[11] P. Ghimire, S. Bęczkowski, S. Munk-Nielsen, B. Rannestad and P. B. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-10.

[12] N. Galanos, "Investigation of the inductor's parasitic capacitance in the high frequency switching of the high voltage cascode GaN HEMT," M.S. thesis, Dept. Elect. Sust. Eng., Delft Univ. of Tech., Delft, Netherlands, 2015.

[13] Z. Liu, "Characterization and Failure Mode Analysis of Cascode GaN HEMT," M.S. thesis, Dept. Elect. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2014.

[14] Z. Guo, G. Cao and Y. Wang, "A novel semiconductor switch test platform for power converter optimization," *2017 20th International Conference on Electrical Machines and Systems (ICEMS)*, Sydney, NSW, 2017, pp. 1-4.

[15] Ganesan P, Manju R, Razila K R and R. J. Vijayan, "Characterisation of 1200V, 35A SiC Mosfet using double pulse circuit," *2016 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, 2016, pp. 1-6.

[16] T. Musikka et al., "Improvement of IGBT model characterization with experimental tests," *2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, 2013, pp. 1-10.

[17] Y. Xu, C. N. M. Ho, A. Ghosh and D. Muthumuni, "A behavioral transient model of IGBT for switching cell power loss estimation in electromagnetic transient simulation," *2018 IEEE*

Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 270-275.

[18] N. Sintamarean, F. Blaabjerg, H. Wang and Y. Yang, "Real Field Mission Profile Oriented Design of a SiC-Based PV-Inverter Application," in *IEEE Transactions on Industry Applications*, vol. 50, no. 6, pp. 4082-4089, Nov.-Dec. 2014.

[19] Tiago Davi C. Busarello, Marcelo G. Simões, José A. Pomilio, "Semiconductor Diodes and Transistors," in *Power Electronics Handbook (fourth edition)*, M.H. Rashid, Eds., Oxford: Butterworth-Heinemann (Elsevier), 2018, pp-15-48.

[20] T. P. Chow, "Progress in high voltage SiC and GaN power switching devices," in *Proc. Materials Science Forum*, 2014, pp. 1077-1082.

[21] Y. Wu, M. Jacob-Mitos, M. L. Moore and S. Heikman, "A 97.8% Efficient GaN HEMT Boost Converter With 300-W Output Power at 1 MHz," in *IEEE Electron Device Letters*, vol. 29, no. 8, pp. 824-826, Aug. 2008.

[22] W. Saito et al., "A 120-W Boost Converter Operation Using a High-Voltage GaN-HEMT," in *IEEE Electron Device Letters*, vol. 29, no. 1, pp. 8-10, Jan. 2008.

[23] W. Saito et al., "Demonstration of resonant inverter circuit for electrodeless fluorescent lamps using high voltage GaN-HEMT," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 3324-3329.

[24] W. Chen, K. Wong and K. J. Chen, "Single-Chip Boost Converter Using Monolithically Integrated AlGaN/GaN Lateral Field-Effect Rectifier and Normally Off HEMT," in *IEEE Electron Device Letters*, vol. 30, no. 5, pp. 430-432, May 2009.

[25] D. Costinett, H. Nguyen, R. Zane and D. Maksimovic, "GaN-FET based dual active bridge DC-DC converter," *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Fort Worth, TX, 2011, pp. 1425-1432.

[26] M. J. Scott, K. Zou, J. Wang, C. Chen, M. Su and L. Chen, "A Gallium Nitride Switched-Capacitor Circuit Using Synchronous Rectification," in *IEEE Transactions on Industry Applications*, vol. 49, no. 3, pp. 1383-1391, May-June 2013.

[27] B. Hughes, Y. Y. Yoon, D. M. Zehnder and K. S. Boutros, "A 95% Efficient Normally-Off GaN-on-Si HEMT Hybrid-IC Boost-Converter with 425-W Output Power at 1 MHz," *2011 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, Waikoloa, HI, 2011, pp. 1-3.

[28] B. Hughes, J. Lazar, S. Hulsey, D. Zehnder, D. Matic and K. Boutros, "GaN HFET switching characteristics at 350V/20A and synchronous boost converter performance at 1MHz," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, 2012, pp. 2506-2508.

[29] J. Delaine, P. Jeannin, D. Frey and K. Guepratte, "High frequency DC-DC converter using GaN device," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Orlando, FL, 2012, pp. 1754-1761.

[30] D. Reusch, D. Gilham, Y. Su and F. C. Lee, "Gallium Nitride based 3D integrated non-isolated point of load module," *2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando*, FL, 2012, pp. 38-45.

[31] F. C. Lee and Q. Li, "High-Frequency Integrated Point-of-Load Converters: Overview," in *IEEE Transactions on Power Electronics*, vol. 28, no. 9, pp. 4127-4136, Sept. 2013.

[32] B. Ozpineci, L.M. Tolbert, “Comparison of Wide-Bandgap Semiconductors for Power Electronics Application,” U.S. Dept. of Energy Report, no. ORNL/TM-2003/257, December 2003.

[33] Emrani, A. and Spadoni, S., "Improving Multi-Voltage Electrical System Performance with smart Step-Down Converters," *SAE Technical Paper* 2017-01-1668, 2017.

[34] Bigorra, J., Borrego, C., Fontanilles, J., and Giró, J., "Innovative Electrical and Electronic Architecture for Vehicles With Dual Voltage Power Networks. In-Vehicle Application," *SAE Technical Paper* 2000-01-0452, 2000.

[35] A. Lidow, J. Strydom, M. D. Rooij, and D. Reusch, GaN transistors for efficient power conversion. Chichester, West Sussex: Wiley, 2015.

[36] N. Ikeda et al., "GaN Power Transistors on Si Substrates for Switching Applications," in *Proceedings of the IEEE*, vol. 98, no. 7, pp. 1151-1161, July 2010.

[37] N. Ikeda, S. Kaya, J. Li, Y. Sato, S. Kato, and S. Yoshida, "High power AlGaN/GaN HFET with a high breakdown voltage of over 1.8 kV on 4 inch Si substrates and the suppression of current collapse," in *20th International Symposium on Power Semiconductor Devices and IC's*, 2008, pp.287-290.

[38] International Rectifier "The Status of GaN Power Device Development at International Rectifier," May 2012, PCIM 2012, available online: www.IRF.com.

[39] M. Ishida, T. Ueda, T. Tanaka and D. Ueda, "GaN on Si Technologies for Power Switching Devices," in *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3053-3059, Oct. 2013.

[40] S. Dusmez and Z. Ye, "Designing a 1kW GaN PFC stage with over 99% efficiency and 155W/in3 power density," *2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, 2017, pp. 225-232.

[41] H. Nakao et al., "2.5-kW power supply unit with semi-bridgeless PFC designed for GaN-HEMT," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, 2013, pp. 3232-3235.

[42] D. Costinett, H. Nguyen, R. Zane and D. Maksimovic, "GaN-FET based dual active bridge DC-DC converter," *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Fort Worth, TX, 2011, pp. 1425-1432.

[43] M. H. Rashid, *Power electronics: devices, circuits, and applications*, 4th ed., Upper Saddle River, New Jersey: Pearson, 2014.

[44] F. Wang, Z. Zhang, and E. A. Jones, *Characterization of Wide Bandgap Power Semiconductor Devices*, London, UK: The Institution of Engineering and Technology, 2018.

[45] *Method for Measurement of Power Device Turn-off Switching Loss*, JEDEC Standard JESD24-1, 2002

[46] F. Z. Peng, L. M. Tolbert and F. Khan, "Power electronics' circuit topology - the basic switching cells," *IEEE Workshop Power Electronics Education, 2005.*, Recife, Brazil, 2005, pp. 52-57.

[47] F. H. Khan, L. M. Tolbert and F. Z. Peng, "Deriving New Topologies of DC-DC Converters Featuring Basic Switching Cells," *2006 IEEE Workshops on Computers in Power Electronics*, Troy, NY, 2006, pp. 328-332.

[48] T. Heckel, L. Frey and S. Zeltner, "Characterization and application of 600 V normally-off GaN transistors in hard switching DC/DC converters," *2014 IEEE 26th International Symposium on Power Semiconductor Devices & IC's (ISPSD)*, Waikoloa, HI, 2014, pp. 63-66.

[49] Z. Zhang et al., "Methodology for switching characterization evaluation of wide band-gap devices in a phase-leg configuration," *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, Fort Worth, TX, 2014, pp. 2534-2541.

[50] A. Anthon, J. C. Hernandez, Z. Zhang and M. A. E. Andersen, "Switching investigations on a SiC MOSFET in a TO-247 package," *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Dallas, TX, 2014, pp. 1854-1860.

[51] Z. Zhang, B. Guo, F. F. Wang, E. A. Jones, L. M. Tolbert and B. J. Blalock, "Methodology for Wide Band-Gap Device Dynamic Characterization," in *IEEE Transactions on Power Electronics*, vol. 32, no. 12, pp. 9307-9318, Dec. 2017.

[52] T. Yao and R. Ayyanar, "A Multifunctional Double Pulse Tester for Cascode GaN Devices," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9023-9031, Nov. 2017.

[53] C. Zhen, “Characterization and modeling of high-switching-speed behavior of SiC active devices,” M.S. thesis, Dept. Elect. Eng., Virginia Polytech. Inst. State Univ., Blacksburg, VA, USA, 2009

[54] V. Scarpa, K. Sobe, “SiC MOSFET Double Pulse Fixture TRENCHTOP ™ 5 in TO-247 4pin Evaluation Board,” 2015. [Online] Available: http://www.infineon.com

[55] GeneSiC Semiconductor Inc., “GA100SBJT12-FR4 – Double Pulse Switching Board,” 2015. [Online] Available: http://www.genesicsemi.com

[56] Panasonic Semiconductor Solutions Co., Ltd., “PGA26E19BA-SWEVB008 Half Bridge Evaluation Board,” 2017. [Online] Available: https://na.industrial.panasonic.com

[57] B. Callanan, “SiC MOSFET Double Pulse Fixture,” 2011. [Online] Available: http://www.cree.com

[58] GaN Systems Inc., “GS66508T/GS66516T-EVBDB GaN EHEMT Daughter Board and GS665MB-EVB Evaluation Platform – User’s Guide” 2018. [Online] Available: http://www.gansystems.com

[59] Z. Zhang and F. Wang, "Driving and Characterization of wide bandgap semiconductors for voltage source converter applications," *2014 IEEE Workshop on Wide Bandgap Power Devices and Applications*, Knoxville, TN, 2014, pp. 1-84.

[60] K. Zou, L. Qi, X. Cui, G. Zhao and B. Zong, "The design and measurement of test system for dynamic characteristics of IGBT," *2014 International Conference on Power System Technology*, Chengdu, 2014, pp. 2209-2216.

[61] Tektronix Inc.: ABCs of probes-primer., Applicat. Note. 2005. [Online] Available: http://www.tektronix.com.

[62] Tektronix, “Power measurement deskew & calibration fixture instructions”, 2008. [Online] Available: http://www.tek.com

[63] J. Dodge and J. Hess, “IGBT Tutorial,” Advanced Power Technologies, Application Note. APT0201 Rev. Bpp. 1–15, 2002. [Online] Available: https://www.microsemi.com

[64] ROHM Semiconductor, “Silicon Carbide Schottky Barrier Diodes,”, 2011. [Online] Available: https://www.rohm.com