A Chemical Sensor Design Using a Standard CMOS Process

by

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Abstract

By integrating an electrochemical deposition process and a silicon chip manufacturing process, a chemical sensor based on a floating gate field-effect transistor was developed. The sensor was fabricated using the standard 0.35μm CMOS process with minimal post-processing. A pH-sensitive organic polymer was electrochemically deposited on the "pseudo" floating gate extension.   This "pseudo" floating gate extension was an external area connected to the floating gate of the testing device.   By monitoring the change of the current-voltage characteristics during exposure to the gas phase of the chemical aqueous solution, the sensor was shown to be feasible with a reasonable sensitivity.

Acknowledgements

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I would like to thank all of my friends and colleagues, especially Pommy Patel, Nishant Dhruve and Kwanyu Lai. Without these fellows, my graduate study would not be so colorful. ☺

Last but not least, I would especially thank my parents, who have strongly supported me for my whole life.

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Symbol	Description	Unit
α	Capacitance coupling factor	None
ε_{si}	Permittivity of silicon	$CV^{-1}m^{-1}$
ε_1	Permittivity of ILD	$CV^{-1}m^{-1}$
ε_{ox}	Permittivity of the gate dielectric (SiO_2)	$CV^{-1}m^{-1}$
ν	Optical frequency	Hz
φ_B	Difference between Fermi level and intrinsic level	V
ϕ_s	Work function of the solid	V
μ	Mobility of charge carriers	$cm^2/V\text{-}s$
BE	Binding energy	eV
C_0	Capacitance per unit area	F/cm^2
C_1	Capacitance between the two gates	F
C_{dm}	Maximum depletion-layer capacitance (per unit area)	$F\ (F/cm^2)$
C_g	Gate capacitance	F
C_2	Capacitance between the floating gate and the substrate	F
C_p	Capacitance associated with the polymer	F/cm^2

d_1	Thickness of the I_1 layer	μm
d_2	Thickness of the I_2 layer	μm
ΔV_{th}^{FG}	Difference of the threshold voltage	V
ΔQ_{FG}	Difference of the net charge	C
E	Electric field	V/cm
E_0	Constants dependent on the electron effect	None
g	Resist thickness	nm
h	Plank's constant ($=6.626\times10^{-34}$Js)	Js
I_{ds}	Drain/source current	A
I_{max}	Maximum drain/source current	A
I_{min}	Minimum drain/source current	A
j	Current density	A/cm^2
KE	Kinetic energy	eV
k	Constant related to the photoresist process	None
N_a	Acceptor impurity density	cm^{-3}
L	Gate length	μm
Q(t)	Charge density on the floating gate	C/cm^2
Q_{FG}	Net charge on the floating gate	C

t_1	ILD thickness between floating gate and control gate	μm
t_{ox}	Thickness of the gate dioxide	μm
V	Voltage	V
V_{cg}	Potential applied to the control gate	V
V_d	Potential applied to the drain electrode	V
V_{fb}	Flat-band voltage	V
V_{fg}	Potential applied to the floating gate	V
V_g	Potential applied to the gate electrode	V
V_s	Potential applied to the source	V
V_{sub}	Potential applied to the substrate	V
V_{th}	Threshold voltage	V
V_{th}^{FG}	Threshold voltage of a floating-gate FET	V
V_{th}^{SG}	Threshold voltage of a single-gate FET	V
W_{min}	Minimum feature size	nm
W	Gate width	μm

List of Abbreviations and Acronyms

CHEMFET   Chemical field effect transistor

CMP   Chemical mechanical polishing

DC   Direct current

DLD   Delay-line detector

DUT   Device under test

FET   Field-effect transistor

MOSFET   Metal-oxide field-effect transistor

EnFET   Enzyme field-effect transistor

ICP   Inductively coupled plasma

ILD   Inter-layer dielectric

ISFET   Ion sensitive field-effect transistor

I-V   Current-voltage

GPIB   General purpose interface bus (the IEEE 488 standard)

RIE   Reactive ion etching

SAW   Surface acoustic wave

UV   Ultraviolet

WF-FET   Work function field-effect transistor

XPS   X-ray photoelectron spectroscopy

Chapter 1 Introduction

1.1 Motivation

In traditional food, beverage, cosmetic, and tobacco industries, trained people are used to detect individual smells and/or flavors of various products. Although the human nose is a very good "sensing system", the special training process required is expensive and greatly increases production cost.[1] In the past several decades, researchers have tried to develop less expensive and more accurate chemical sensing systems which can mimic the function of the human nose. These chemical sensing systems are called "electronics noses". In "electronic noses", chemical sensors are used to react with the detected environment and give off electric signals. The electric signals are further analyzed with the application of pattern recognition techniques.

Among the variety of concepts and the different types of chemical sensors proposed in literature, one of the most attractive approaches is to combine the chemical recognition processes with the silicon chip manufacturing.[2] As such, chemical sensors were developed based on field-effect transistors. This type of chemical sensor is attractive because it has many potential advantages, such as the small size, high sensitivity, inexpensive fabrication, and the possible integration into large sensor arrays. Especially,

with the rapid development of semiconductor micro- and nano-technologies, these micro-sensors and "system on a chip" devices have become realizable.[2]

In this thesis, the development of a FET based micro-sensor is described. The sensor was composed of a floating gate field-effect transistor with a large extension area connected to the floating gate. The basic sensor structure was fabricated using a standard CMOS process, while the "sensing" polymer was deposited in post-processing. Using the field-effect transistor's non-linear nature of the sub-threshold current, the sensor was found to be highly sensitive to the chemical reactions processed on the "pseudo" floating gate extension. In the future, this designed sensor will be used to create a sensor array system that will emulate the capabilities of mammalian olfaction.

1.2   Organization of Thesis

In Chapter 2, several types of chemical sensors are introduced. In particular, the advantages and disadvantages of the floating-gate field-effect transistor structure are discussed to show why it was used in the new chemical sensors.

Two iterations of the chemical sensors, reference transistors and other structures were developed and their designs are introduced in Chapter 3. Issues found in the post-processing or the device characterizations are discussed. An improved sensor design

in the second iteration is then presented.

In Chapter 4, the post-processing procedures developed to expose the "sensing" area of the device are introduced.   Difficulties met in etching and the XPS techniques used to differentiate between two dielectrics are discussed.

The current-voltage characteristics of the different devices are presented in Chapter 5. From the I-V curves before and after the exposure to the gas phase of the chemical aqueous solution, the feasibility of the sensor was demonstrated.

In Chapter 6, the project work is summarized and conclusions are presented. Improvements to the sensors are described while discussing the future work that can be undertaken.

Chapter 2 Introduction of Chemical Sensors

Chemical sensors can detect certain molecules in both chemical solutions and gases. However, the operation mechanism used in various chemical sensors is quite different. For example, with resistive sensors, the chemical gas changes the conductivity of the sensing material while with the chemical transistors (or CHEMFETs), the chemical reaction changes the charge stored on the gate and shifts the threshold voltage of the transistor. With the surface acoustic wave (SAW) chemical sensors, the gas adsorption changes the wave impedance of the device.[3] In quartz-resonator arrays, the mass of molecules adsorbed is utilized in changing the resonance frequency.[3] Although many different types of chemical sensors exist, the discussion in this chapter will be restricted to resistive sensors and CHEMFETs since these devices work in a similar manner by assessing the change of the current in the respective devices.

2.1 Chemiresistors

As its operation depends on the resistance change, resistive sensors that are used for chemical sensing are referred to as chemiresistors.[1] Various materials have been used as the sensing films including metal oxides, conducting and non-conducting polymers.

Specific material application as well as the general operation of chemiresistors will be discussed in this section.

2.1.1 Tin Oxide Chemiresistors

The tin oxide detector (see Figure 2-1) is a type of sensor developed by Figaro Inc. (Japan).[3]   It can be used in olfactory sensing system.   Its sensing part consists of a thin tin oxide (SnO) film doped with a metal behaving as an n-type semiconductor.   When molecules react with the chemisorbed lattice oxygen in the SnO film, electrons are injected from the valence band of the semiconductor to the conduction band, and the electron mobility, through a lowering of intergranular barriers, is increased, which results in the change of the conductivity in semiconductor.[3]
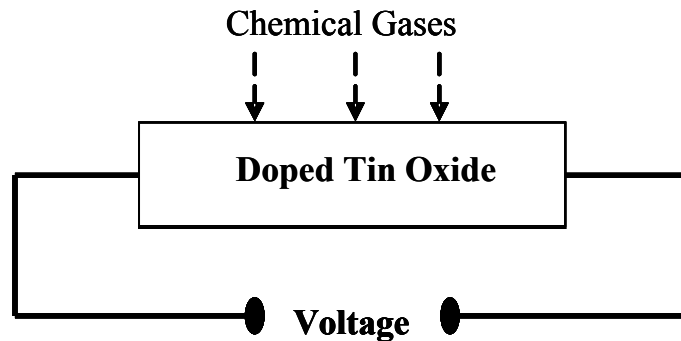
Figure 2-1:   *Tin oxide doped with a precious metal. [3]*

Tin oxide detectors are a commercial product and are sensitive to several combustible gases with the sensitivities in the range of ~1 part per million (ppm).

Typically, prior to the actual operation, detectors are warmed up to approximately 300~400°C to reduce its response time. However, the sensitivity of the Figaro SnO gas sensors varies with the temperature as well as the doping concentration and the exposure environment.[3] The ultimate sensitivity is also very dependent upon the detailed manufacturing process.

2.1.2 Conducting Polymeric Chemiresistors

Compared to the metal oxide used in the aforementioned chemiresistor, conducting polymers used in conducting polymeric chemiresistors can be more easily deposited electrochemically.[3] The device can operate at the room temperature. A general view of a sensing device of this type is shown in Figure 2-2. The sensor is built on a substrate which is typically a ceramic tile. Two electrodes are formed which are separated by an insulator. The conducting polymer is deposited in the space between these two electrodes.

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Figure 2-2: *Configuration of a conducting polymeric chemiresistor. [3]*

When a small voltage is applied across the electrodes, a current is generated which passes through the conducting polymer. The current varies when the sensor is exposed to different gases due to the change of the polymer resistance. Therefore, this type of sensors can distinguish various chemical gases.

2.1.3 Non-conducting Polymeric Chemiresistors

Non-conductive, chemically sensitive polymers can also be used to make chemiresistors. For example, conductive particles of carbon black [4, 5] are embedded into a non-conductive polymer to create a conducting path. When the sensor is exposed to the particular chemical environment, chemicals diffuse into the polymer and cause it to swell. Due to the swelled polymer, the length of conducting paths and therefore the resistance of the sensor increases. This phenomenon is illustrated in Figure 2-3. Since the base value of the resistance can still be recovered by removing the adsorbed chemicals through healing and out-gassing, this type of sensors is reusable.

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Figure 2-3: *a) Particles of carbon black are embedded in the non-conducting polymer; b) after the chemiresistor is exposed to the chemical gases. [4]*

2.2   CHEMFETs

Chemresistors typically have a sensitivity that is linear: i.e. a change in resistance that is to some degree linearly proportional to a change in chemical concentration.   However, the drain/source current of a field-effect transistor (FET) can have a logarithmic relationship with the applied gate voltage in the sub-threshold regime. Therefore, a linear change in the gate bias can produce an exponential change in the drain/source current, which makes this type of device extremely sensitive.   If transistors are used for chemical sensing, they are often referred to as CHEMFETs.   In this section, three types of CHEMFETs will be introduced: ion sensitive field-effect transistors, enzymatically selective field-effect transistors and work function field-effect transistors.

2.2.1 Ion Sensitive Field-Effect Transistors

An ion sensitive field-effect transistor (ISFET) is an electronic device very similar to a standard metal-oxide-semiconductor field-effect transistor (MOSFET). Schematic diagrams of these two devices are shown in Figure 2-4.   Unlike a standard MOSFET, the gate of the ISFET is separated from the device and is formed by a reference electrode inserted in the test solution that is in contact with the gate oxides.   By depositing an ion sensitive material on top of the traditional gate oxide (e.g. SiO_2), an ISFET is formed.
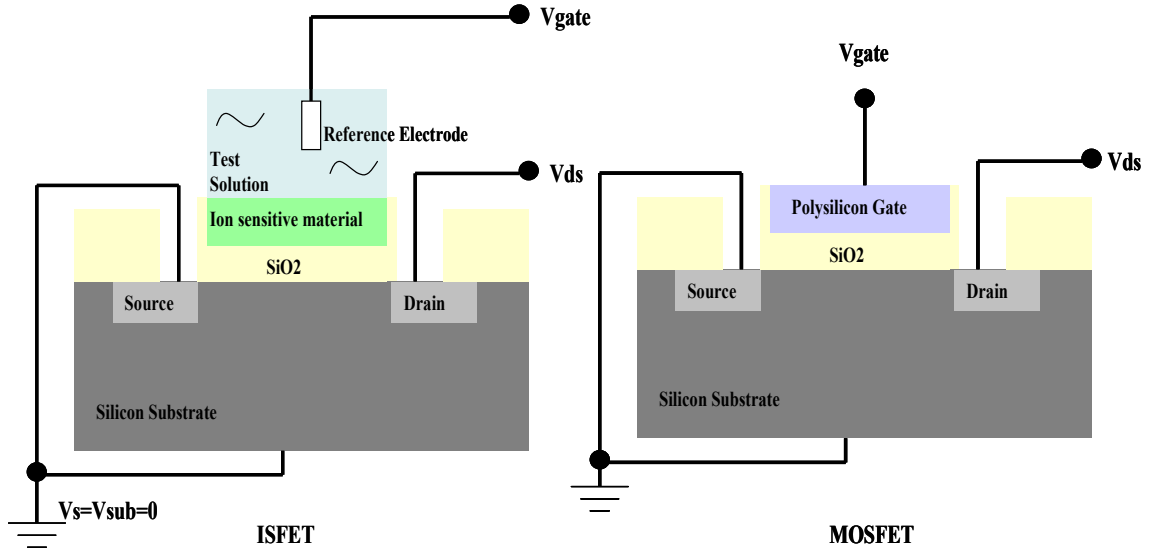
Figure 2-4: *Schematic representation of a) an ISFET and b) a MOSFET.*

This material can react with chemicals and change the ion concentration in the test solution.

The change in the charge state of the ion sensitive material, due to different ion

concentrations, then generates the charge at the oxide/solution interface in the form of

protonized (OH_2^+) or deprotonized (O^-) OH groups [6]. Subsequently a change in the

surface potential of the ISFET is observed, leading to a change in the threshold voltage of

the ISFET. The threshold voltage, V_{th}, is the gate voltage required to turn on an FET. In

the linear regime, its relationship with the drain/source current of an ISFET can be

expressed using

$$I_{ds} = C_{ox} \mu \frac{W}{L} \left[\left(V_g - V_{th} \right) V_{ds} - \frac{1}{2} V_{ds}^{\ 2} \right] \tag{2.1}$$

where C_{ox} is the gate capacitance per unit area, μ is the mobility of charge carriers in the

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channel, W and L are the width and length of the gate, respectively, V_g is the gate voltage, and V_{ds} is the applied drain voltage. The drain/source current is measurable, and the shift of the threshold voltage can then be calculated using this equation. Since its threshold voltage can be chemically modified via the potential generated at the electrolyte/oxide interface, ISFETs are often used in sensors to measure the ion concentration (or pH) of the test solution. Typically, Si_3N_4, Al_2O_3, SiO_2 and Ta_2O_5 are used as the gate oxides in ISFETs.

The operation of the ISFET is highly dependent upon the use of a reference electrode as the gate. A conventional reference electrode is made by placing a reference metal (e.g., Ag) in a compartment filled with the aqueous solution (e.g., the saturated KCl) as shown in Figure 2-5. The bottom of the compartment is sealed by a thick frit, which is a porous glass that allows for ions to pass though, but larger molecules and solvent flow more slowly through the frit. When there is no bias applied on the reference metal, a liquid junction exists between the test solution and the aqueous solution. Since no ions can be easily transferred, the content of the aqueous solution remains the constant and a stable reference potential is formed. However, over time, the KCl in the aqueous solution has a tendency to diffuse out of the compartment into the test solution, likewise, ions in the test solution may diffuse into the compartment. If the diffusion in either direction occurs,

ion current will exist and as such can make the reference potential not entirely stable.

Therefore, the period over which the reference potential remains constant is defined as the

stable lifetime of the reference electrode. The operation range of an ISFET is limited by

the stable lifetime.
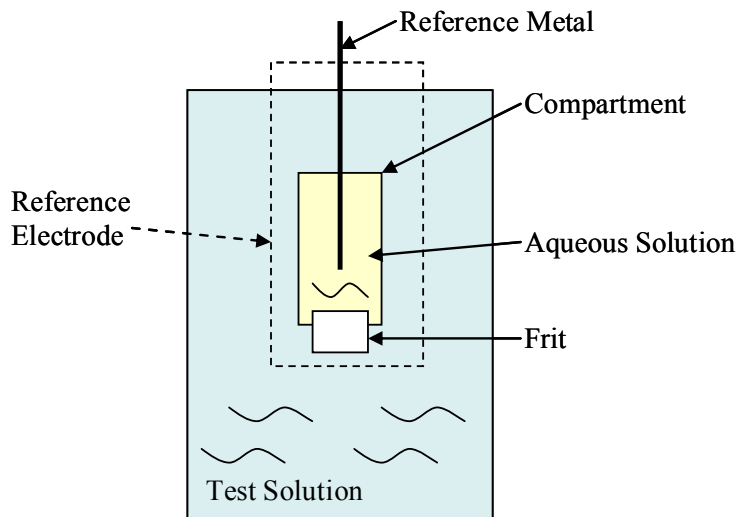
Figure 2-5: *A conventional reference electrode.*

Since the measurement apparatus for an ISFET is comprised of an ISFET and a

reference electrode submersed in the test solution, the application of ISFETs as a sensor

can be limited by the size of the reference electrode. Several methods have been tried to

solve this issue. One of them is to make the micro-reference electrodes by reducing the

size of the compartment. However, due to the lesser amount of aqueous solution that can

be filled in the compartment, the contents of the aqueous solution are more quickly

changed by diffusion. In other words, the stable lifetime of micro-reference electrodes will

be shortened.   The fabrication of a stable micro-reference electrode for ISFETs used in the

micro biosensor is still one of the challenges.

Depending on the type of ion sensitive oxides used in an ISFET, some

post-processing might be required.   For example, Al_2O_3, Ta_2O_5 may need to be thermal

evaporated or sputtered on the device, [7] while organic polymers may have to be

deposited electro-chemically.

2.2.2 Enzyme Field-Effect Transistors

A second type of CHEMFET is the enzyme field-effect transistor (EnFET)

whose structure is very similar to an ISFET.   However, EnFETs are capable of sensing

electrically neutral species due to a layer of enzyme adsorbed on the surface of the ion

sensitive oxide (see Figure 2-6).   Enzyme molecules catalytically hydrolyze the test

solution and change its ion concentration.   The ion sensitive oxides (i.e., outer gate

insulator and SiO_2) detect the change and induce a surface charge at the interface.   The

surface potential and thus the threshold voltage of the device is changed, which in turn

changes the drain/source current of the FET.[8]   As a consequence, Enzyme FETs

translate the change in the ion concentrations of a test solution into the change in the

drain/source current of an FET.
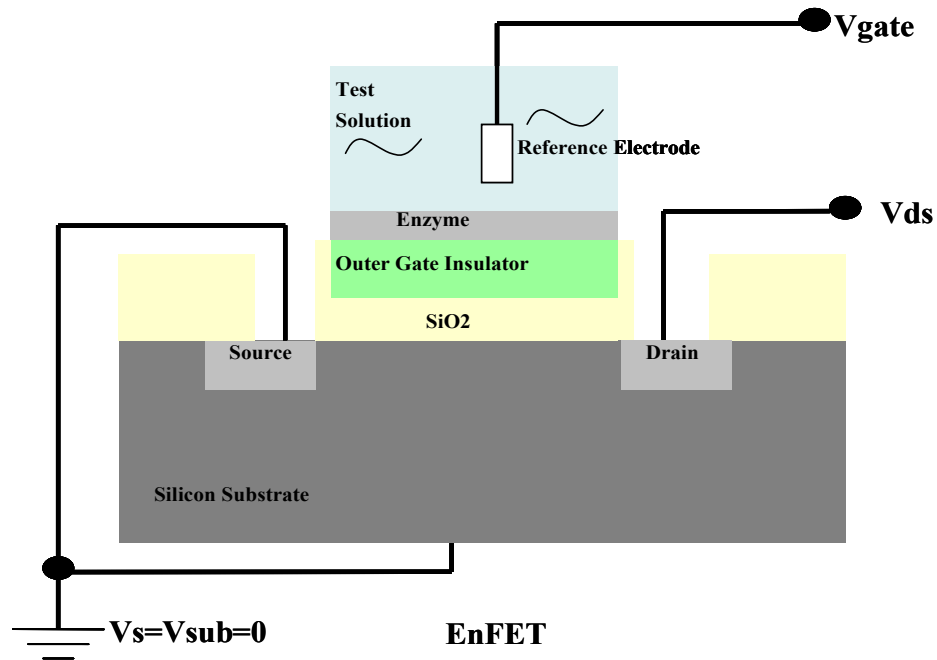
Figure 2-6: *Schematic Diagram of an enzyme field-effect transistor.*

Two methods can be used to operate an EnFET. Firstly, the EnFET can be set up

similarly to a standard ISFET with the same type of reference electrodes. However, as

stated previously, due to the difficulties in making micro-reference electrodes, the

measurement apparatus of EnFETs is usually large. Therefore, a differential measurement

system is often employed. In this method, the operation of the EnFET is controlled by

measuring the potential difference between the EnFET and a reference FET, which is

identical to the EnFET but insensitive to the ion concentration of the test solution. These

EnFETs with a differential measurement system are more applicable for the construction of

sensor arrays.

2.2.3 Work Function Field-Effect Transistors

Work function field-effect transistor (WF-FET) is another type of CHEMFET. It can be used to detect electrically neutral species in non-conducting environments such as gases and dielectric liquids.[9]   An example of such a WF-FET is shown in Figure 2-7 where a conducting polymer is deposited as the gate electrode.   The conducting polymer is stable in air and water.   Its conductivity can vary over a certain range depending on its oxidation state and doping level.[8]   When this WF-FET is exposed to the particular gaseous analyte, a chemical or electrochemical modification of the conducting polymer occurs.[8, 10, 11]   Gas molecules penetrate the polymer up to the interface between the conducting polymer and the gate dielectric, where they are adsorbed and form an electrical dipole with an associated electric field.   The work function of the conducting polymer and therefore, the threshold voltage of the WF-FET, are shifted.

The conducting polymer used in a WF-FET is usually deposited by a spinning process.   For example, when the conducting polymer polyaniline is used as the gate, it can be dissolved in aqueous formic acid first and then spun onto the gate dielectric.   The device is heated to approximately 60ºC for 30 minutes to evaporate the formic acid. [8] The remaining polyaniline is then patterned with a photolithography process which will be discussed more in Chapter 4.   This operation procedure could be repeatedly used in the

deposition of the different conducting polymers. However, the baking temperatures and time should be adjusted.
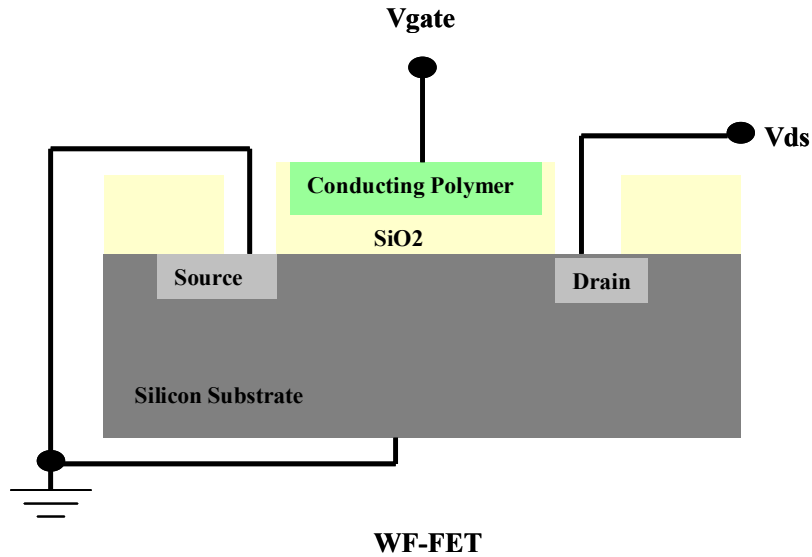
Figure 2-7: *Schematic diagram of a work function field-effect transistor (WF-FET).*

The biggest advantage of using the WF-FET chemical sensors is that no reference electrodes or reference FETs are required to operate the device. The gate bias can be directly applied to the conducting polymer. The silicon substrate, which is covered by a gate dielectric consisting of silicon dioxide or silicon nitride, can work as a stable internal reference electrode. The chemical reaction induced change in a WF-FET can thus be easily obtained by comparing the gate voltage before and after exposing the device to the chemical analyte. Since the measurement system is very simple, WF-FETs are more suitable for the miniaturization and construction of sensor arrays. [9]

Even though WF-FETs are much simpler to operate than ISFETs and ENFETs, they still have several limitations.   Firstly, polymers that have been deposited on the gate and used as the electrode need to be conductive.   Secondly, the fabricated WF-FETs can only be scaled down to several microns since the gates are not self-aligned.[13]   The gate-to-source and gate-to-drain overlap capacitance can be a serious issue if the gate dimension is very small.   Thirdly, only a single conducting polymer can be deposited and patterned on a chip as all of devices on the same chip are heated up at the same time with the same temperature.

2.2.4 Floating Gate Field-Effect Transistors

So far, the introduced chemresistors have been shown to be easy to fabricate but limited in sensitivity.   Chemtransistors do have the high sensitivity, however, they cannot be easily fabricated using standard CMOS processes due to the conducting polymers or ion sensitive polymers which are used as the gate making the integration difficult.   Due to the desire to be able to integrate the sensors with a standard CMOS process, another form of sensor was thus investigated: the floating-gate field-effect transistor.

The floating-gate field-effect transistor structure was firstly introduced by D. Kahng and S.M. Sze in 1967.[12]   As shown in Figure 2-8, two metal layers (M2 and M3)

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Figure 2-8: *Schematic diagram of a floating gate field-effect transistor.[12]*

were used as separate gates and were isolated by a thick insulating layer (I2). The M2 layer was separated from the substrate by a thin insulating layer (I1). During the device operation, a high voltage was applied to the M3 gate with respect to the substrate and a negative voltage was applied on the drain with respect to the source. Since the potential M2 layer was not tied (i.e., floating), it was named as the floating gate. Hence, FETs with this structure were named as floating gate field-effect transistors.

In this floating gate field-effect transistor, charge can be held on the floating gate for a long period of time even after the bias was removed. This phenomenon can be explained using the energy band diagram shown in Figure 2-9.

Figure 2-9: *Energy band diagram of a floating gate structure in the floating gate FETs. a) when a positive bias was applied on the M3 layer; b) when this bias was removed, the stored charge Q causes an inversion of the silicon substrate. [12]*

When a positive bias is applied to the M3 layer, electrons can tunnel through the thin I1 layer and accumulate on the floating gate (M2). Since the I2 layer is designed to be much thicker, most of electrons cannot be transported across the I2 layer, but remain on the floating gate surrounded by insulators. This charge storage nature thus enables floating gate FETs to work as a bistable memory with a nondestructive read-out capability.[12]

Currently, floating gate field-effect transistors are one of components that have been widely used in the electronically erasable programmable read only memory (EEPROM) or flash memory industry.

For a given current density j, the charge density stored on the floating gate, Q, is given by [12]

$$Q(t) = \int_0^t j\,dt \qquad \text{C/cm}^2 \tag{2.2}$$

To the thin I1 layer made of SiO_2, the charge was transported by the Fowler-Nordheim tunneling.[13]   Therefore, the current density j, can be given by

$$j = C_0 E^2 \exp(-E_0 / E) \tag{2.3}$$

where C_0 and E_0 are constants dependent upon the electron effective mass and interfacial barrier height, and E is the electrical field across the I1 layer.[12]   The electrical field (E) is a function of the applied voltage V and $Q(t)$, and is expressed as

$$E = \frac{V}{d_1 + d_2(\varepsilon_1 / \varepsilon_2)} - \frac{Q}{\varepsilon_1 + \varepsilon_2(d_1 / d_2)} \tag{2.4}$$

where d_1 and d_2 are the thickness, and ε_1 and ε_2 are the permittivity of I1 and I2, respectively.[12]   For a given applied gate voltage, the charge stored on the floating gate can be estimated using equations 2.2, 2.3 and 2.4.   However, parasitic capacitances were neglected in these equations.

As shown in equation 2.4, if a chemical reaction can change the charge density of

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the floating gate, the surface potential of silicon and therefore the threshold voltage will be changed. By comparing the threshold voltages before and after the sensor is exposed to the chemical analytes, the floating gate field-effect transistor can transform chemical reactions into easier measurable electronic signals.

However, a sensitive polymer has to be deposited onto the floating gate to be able to affect the charge storage on the floating gate. With a standard CMOS process, this is not easily possible. Therefore, a "revised" CMOS process was required to fabricate the sensor. As well, the floating gate structure in a device was "revised" to make the integration of sensors easier. As such, the floating gate in the field-effect transistor (FET) was attached with a large extension area as shown in Figure 2-10. The extension area could only be exposed in the post-processing and followed by the deposition of a sensitive polymer. However, with the application of the floating gate extensions, the size of the field-effect transistor in a sensor was greatly scaled down. A smaller sensor should be more sensitive as a larger percentage of the sensor area could be affected by the chemical molecules.
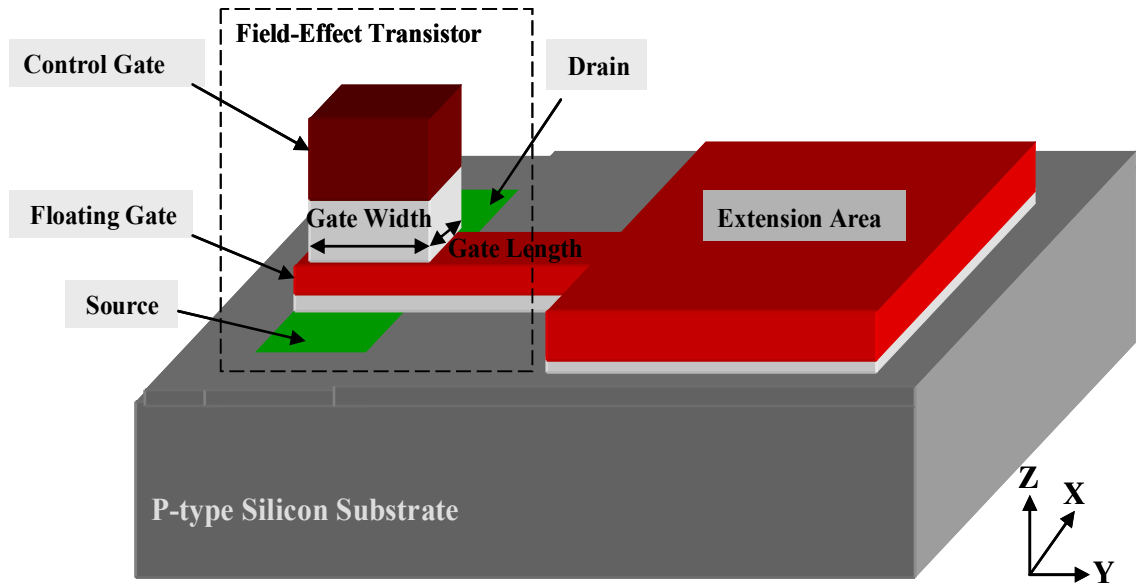
Figure 2-10: *The chemical sensor built on top of the floating gate field-effect transistor structure.*

In this project, a commercialized tool (Cadence) was used for the design of the sensor chips. The Cadence system was supplied by Canadian Microelectronics Corporation (CMC) Microsystems. Among various CMOS processes, the 0.35 μm CMOS process supplied by Taiwan Semiconductor Microelectronic Company (TSMC) was selected to fabricate the sensor chips since this is a process providing two polysilicon layers which could be used to form the floating gate and the control gate of the sensor. The sensor chip was designed following a set of material and dimensional restrictions known as "design rules", which are the basic layout guide as defined by TSMC for this 0.35 μm process.

Chapter 3 Chemical Sensor Design

For the first iteration of the chemical sensor development, twenty four different sensors were designed and then grouped on the final chip into devices. However, only one group of sensors exhibited the reasonable operating characteristics. This working sensor structure will be presented and discussed in section 3.1. Due to the design issues found after the initial device characterization, improvements were made to the sensor structure for the second iteration of the chemical sensor development. Forty eight different types of sensors were designed based on the improved structure and integrated into the second chip which will be presented in section 3.3.2.

3.1   First Iteration of the Chemical sensor Design

3.1.1 Sensors with a Floating Gate Extension

In Figure 3-1, a schematic diagram of a sensor structure is presented. This structure was used for all the sensors of the first iteration. As shown in the figure, the sensor has five different terminals: source, drain, floating gate, control gate and substrate. The floating gate field-effect transistor portion of the sensor is shown on the left side of Figure 3-1. The "sensing" part of the device was achieved by attaching a large extension

area to the floating gate as shown on the right hand side of Figure 3-1. It is on this floating gate extension that a chemically sensitive polymer layer was deposited. This was performed using a selective electrochemical deposition technique, with a bias applied on the floating gate.
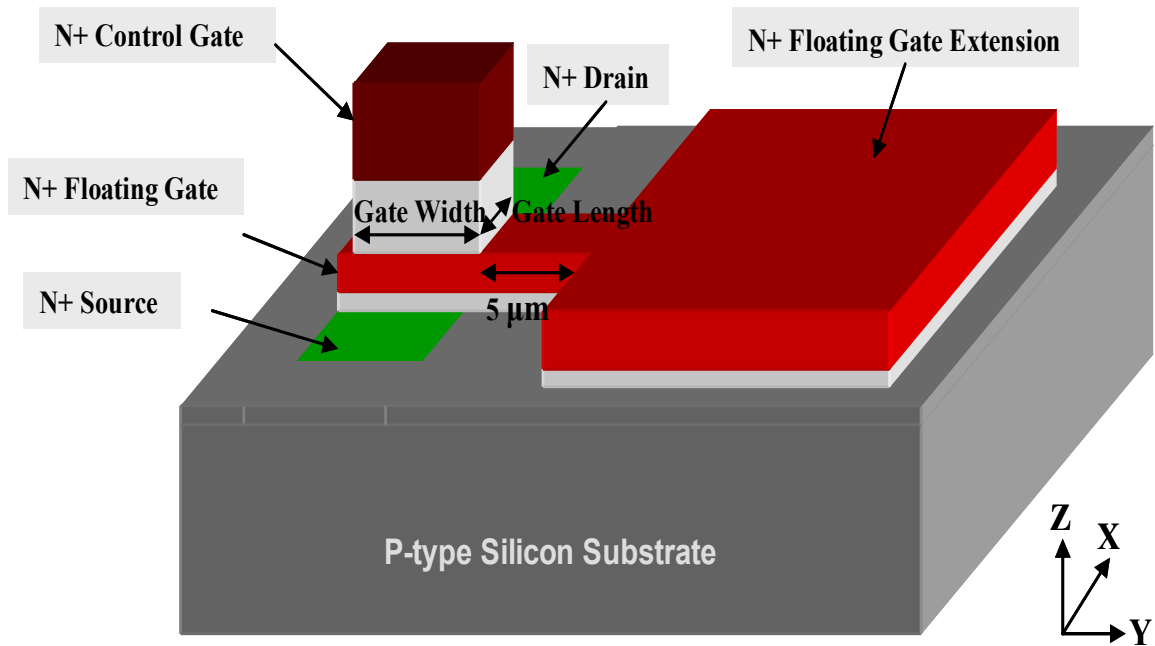
Figure 3-1: *A 3D schematic diagram of an n-type sensor with a floating gate extension.*

In this sensor, the floating gate extension was 10×10 μm and was placed 5 μm away from the floating gate of the field-effect transistor. It was formed using the same polysilicon layer as the floating gate. However, the gate width and length of the field-effect transistor were varied in the different sensors and are listed below in Table 3-1.

Table 3-1: *Sensor gate lengths and widths*

Gate Width-to-Length (W/L) Ratio	Gate Length (μm)	Gate Width (μm)
6.25	0.8	5
3	1.2	3.6
2.50	1.5	3.75

Different gate widths and lengths were used to improve the sensitivity of devices. The sensitivity depends on the operating characteristics of the floating gate field-effect transistor, particularly the drain/source current where a larger current range leads to a more sensitive device. As shown in equation 3.1, the drain/source current (I_{ds}) of this transistor can be affected by the mobility of charge carriers, the gate width-to-length ratio (W/L), the applied drain voltage, the oxide capacitance and the potential difference between the gate voltage and the threshold voltage. However, with a standard CMOS process, only the gate width-to-length ratio (W/L) is adjustable in the sensor design. Therefore, the drain/source current was changed by the factor of 1.2 or 2.5 when the W/L ratios were varied from 2.5 to 3 or 6.25.

$$I_{ds} \sim \mu C_{ox} \frac{W}{L}(V_g - V_{th})V_{ds} \tag{3.1}$$

The large 10×10 μm floating gate extension was also designed to increase the sensitivity of devices. A polymer deposited on the floating gate extension reacts chemically with the gas analyte and induces the change in the charge density on the

floating gate, which in turn shifts the threshold voltage of the field-effect transistor. A larger floating gate extension produces a larger area of reactive polymers, which induces a larger shift of the threshold voltage. Therefore, the extension area was designed to be significantly larger than the gate area of the field-effect transistor.

The floating gate extension was separated from the floating gate to allow for post-processing (see Figure 3.1). Since the entire sensor area, including the floating gate extension, was covered by a series of dielectrics, a number of post-processing steps were required to expose the extension area using either wet etching or reactive ion etching techniques. Initially it was assumed that wet etching would be used.

Wet etching is an isotropic etching process and generates an "undercutting" around the exposed floating gate extension as illustrated in Figure 3-2. The undercutting could damage the field-effect transistor if the extension was not at least 5 μm away as this was approximately the depth of dielectrics that was to be etched and the etch rates in the vertical and lateral directions were assumed to be the same. This 5 μm separation should protect the field-effect transistor structure from being attacked during wet etching.

Anisotropic Etching
(Etching in one direction)

Isotropic Etching
(Etching in all directions)
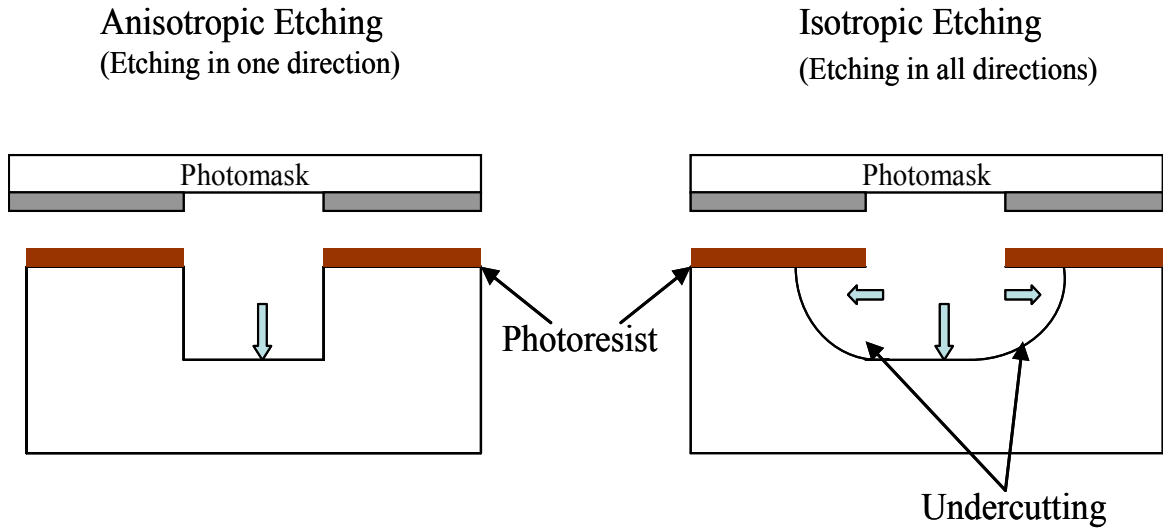
Figure 3-2:   *The difference between the anisotropic etching and isotropic etching.*

Although the schematic diagram shown in Figure 3-1 includes all the important sections of the sensor structure, it is not an exact representation of the final design that was manufactured.   A plan view of the actual sensor layout that was designed is presented in Figure 3-3.   In this design, the contact holes were placed over each electrode region to generate a conducting path from the isolated layer to the top chip surface.   The cross-section (A-A') shown in Figure 3-4 reveals the layers that must be etched to access the floating gate extension.

1. p type Substrate
2. n+ type Source
3. n+ type Floating Gate
4. n+ type Control Gate
5. n+ type Drain
6. n+ type Floating Gate Extension
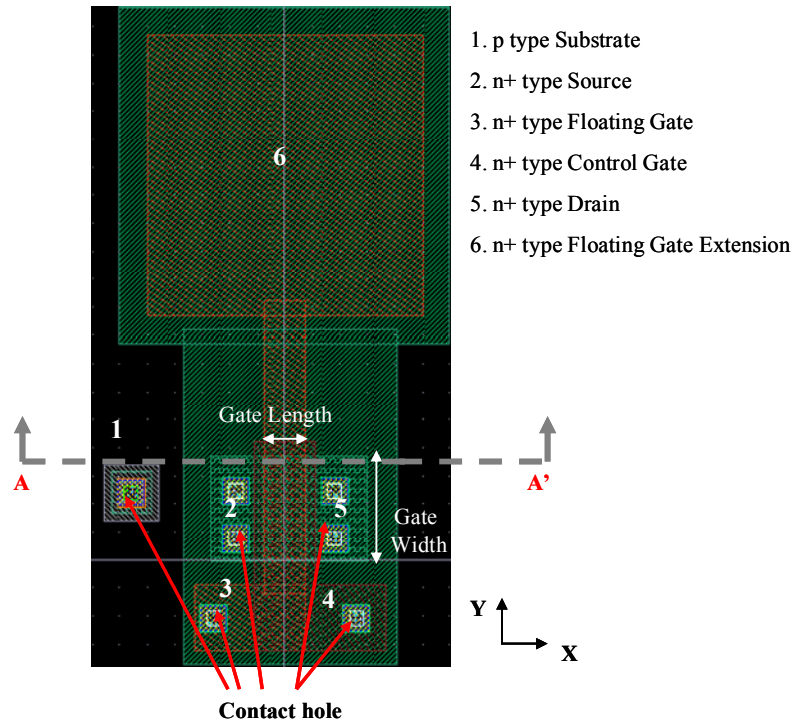
Figure 3-3: *Layout of an n-type sensor with a floating gate extension.*
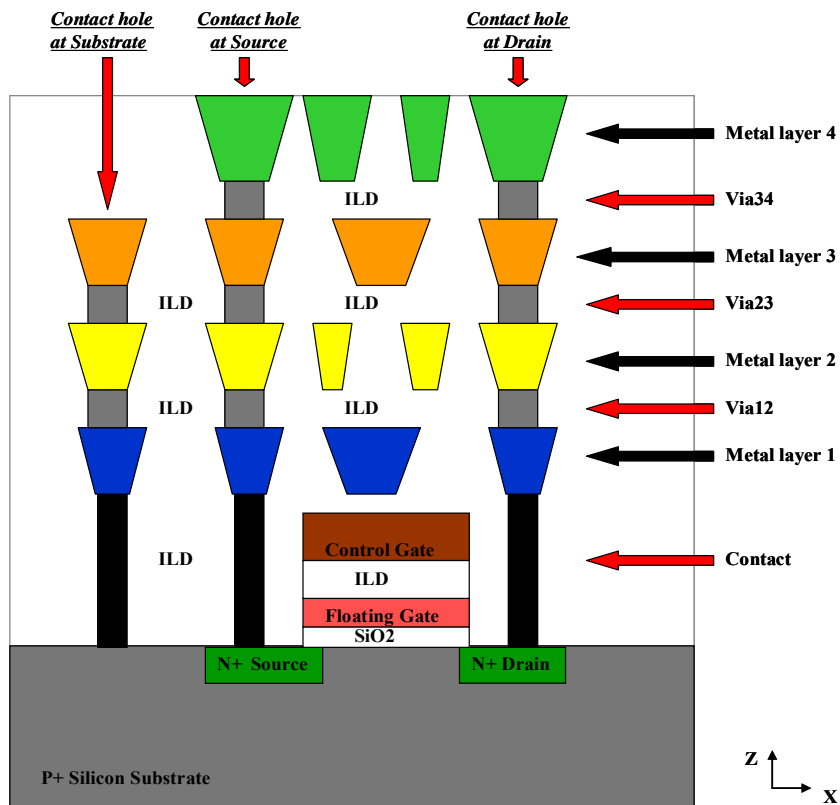
Figure 3-4: *The cross section (A-A') of the device.*

3.1.2 Reference Transistors

Reference transistors are simply standard transistors without the floating gate extension. To extract the basic device parameters, two types of reference transistors were introduced: the single-gate field-effect transistor and the floating-gate field-effect transistor.

Figure 3-5 shows a schematic diagram of a single-gate field-effect transistor and a plan view of the actual layout. The single-gate field-effect transistor was only composed of four terminals: gate, source, drain and substrate. The bottom polysilicon, used for the gate, was on the same layer used for the floating gate extension. Since the design of these terminals or electrode regions was identical for both the single-gate field-effect transistors and the actual sensors, the single-gate field-effect transistors were able to extract the basic device parameters in the FET of each sensor.

a)   b)
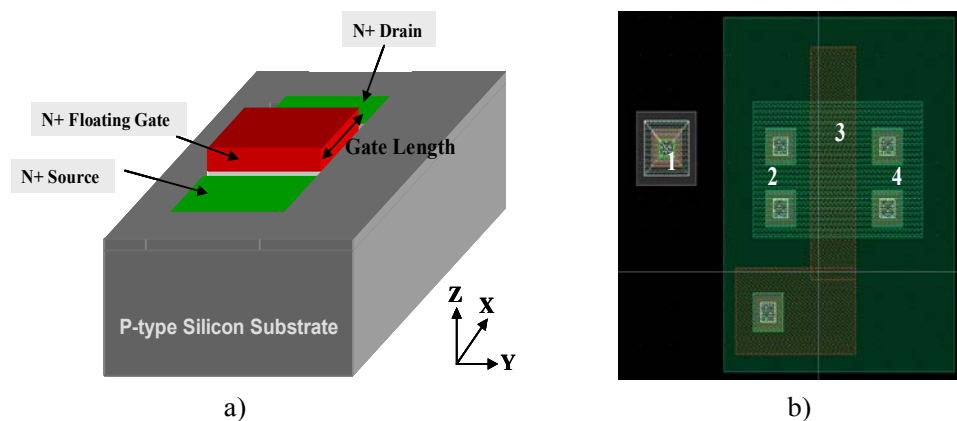
Figure 3-5: *Reference Transistors - single-gate field-effect transistor. a) 3-D schematic diagram and b) layout of an n-type single gate field-effect transistor: 1-Substrate; 2-N$^+$Source; 3-N$^+$Gate; 4-N$^+$Drain.*

Figure 3-6 a) shows a floating gate field-effect transistor design. This reference transistor was a five terminal device, the same as the designed sensor. However, this device did not have the floating gate extension structure. The operating characteristics of the floating gate field-effect transistor could be compared to the operating characteristics of the sensor. The difference in the current-voltage characteristics would be a result of the floating gate extension. The characterization results of these FETs will be presented in Chapter 5.

a)   b)
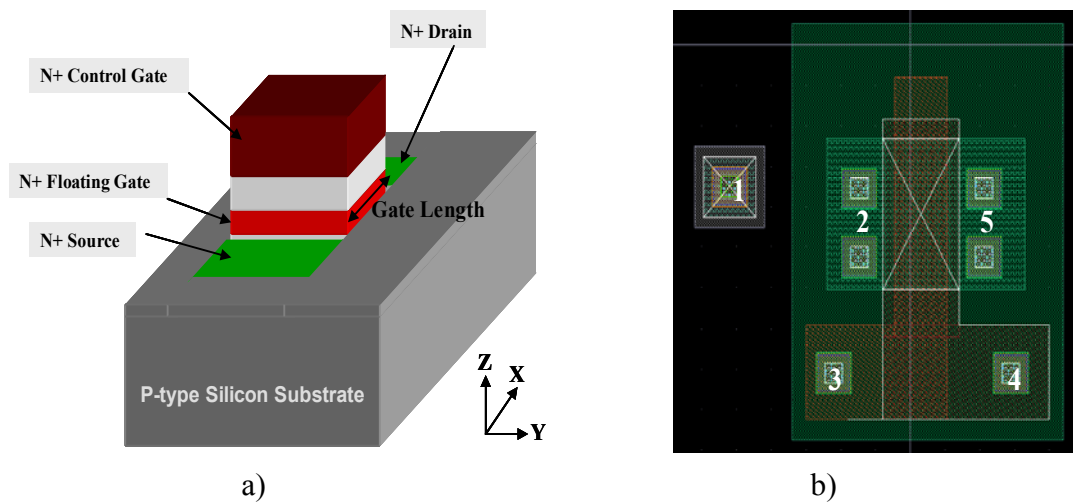
Figure 3-6: *Reference Transistors - floating-gate field-effect transistor. a) 3-D schematic diagram and b) layout of an n-type floating-gate field-effect transistor: 1-Substrate; 2-N^+ Source; 3-N^+ Floating Gate; 4-N^+ Control Gate; 5-N^+ Drain.*

3.1.3 Bonding Pads

The plan view of the bonding pad layout for the external chip access and its cross-section schematic is shown in Figure 3-7 a) and b), respectively. The $80 \times 80 \ \mu m$

bonding pads consist of a heavily-doped bottom polysilicon layer and four metal layers.

These five conducting layers are connected by contacts or vias through the different ILDs.

A contact window was defined to open the top metal (Metal4) contacts at the end of the

CMOS process.
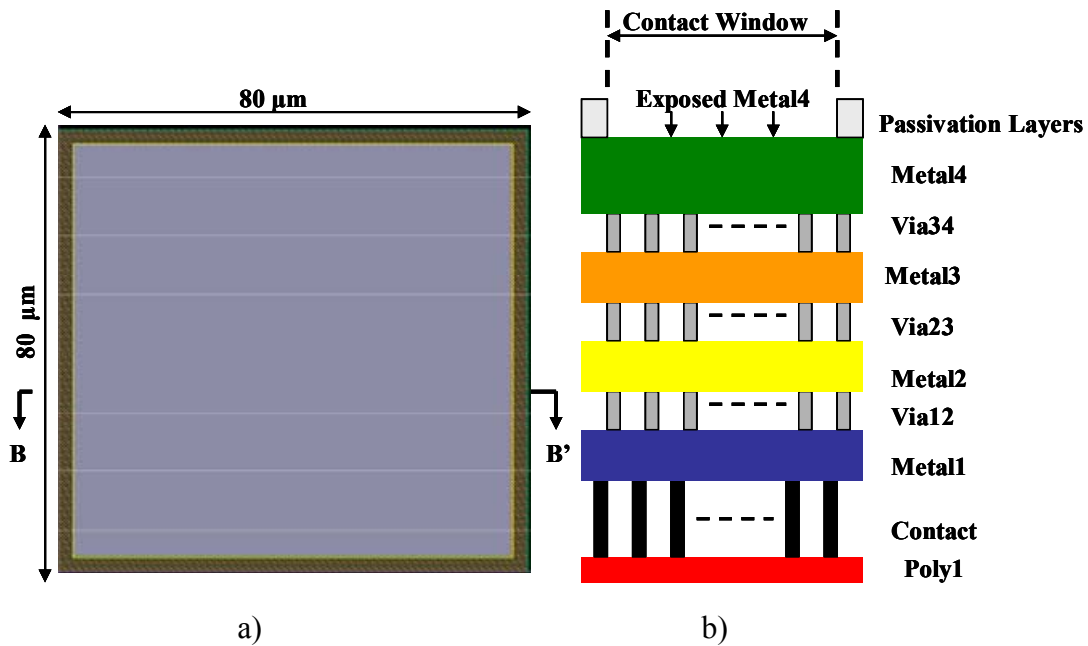
Figure 3-7: *Bonding Pad (80 × 80 μm²); a) The plan view of the bonding pad layout; b) The cross-section(B-B') of the bonding pad.*

As shown in Figure 3-8, every sensor and reference transistor was covered by a

series of passivation layers after the CMOS process. Bonding pads were required when

generating the conducting paths from the test equipment supplying the electrical signals to

the electrode regions in the sensor.
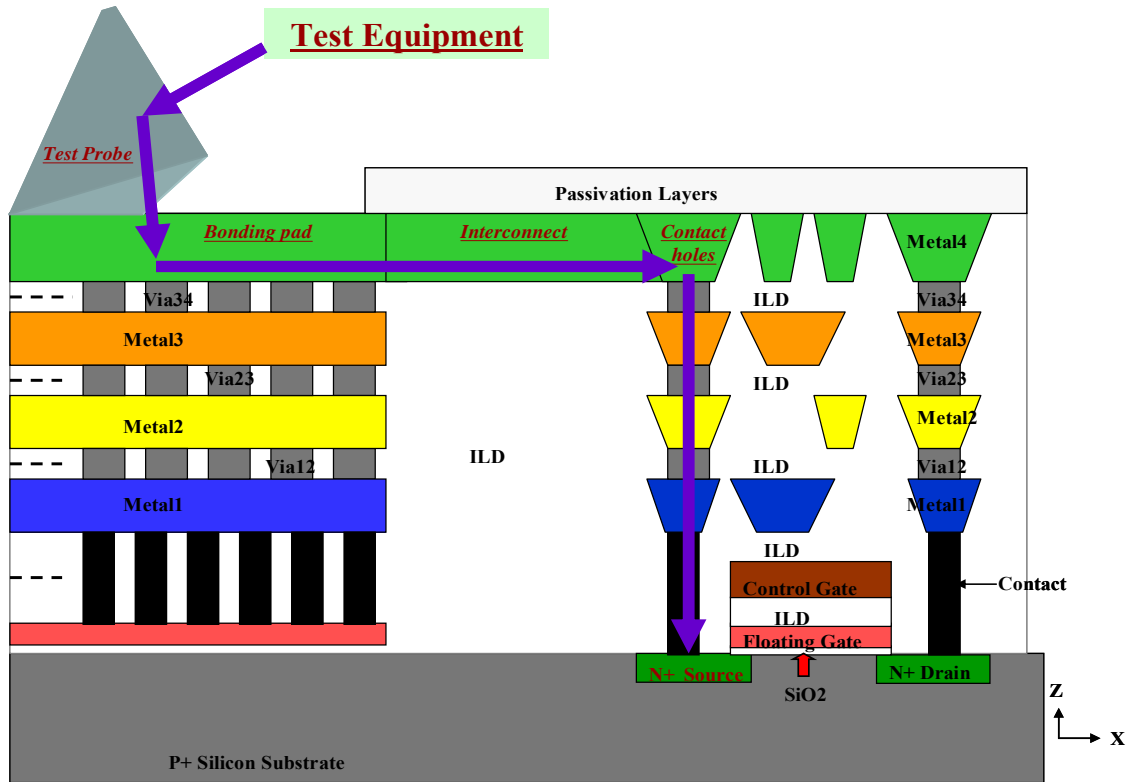
Figure 3-8: *A conducting path generated from the test equipment to the electrode region.*

Initially, each bonding pad was connected to one terminal of the device (ie, source, drain or gate etc.). Therefore, five individual bonding pads were required for each sensor (see Figure 3-9). However, due to the limited chip space, the total number of bonding pads that could be placed on the chip was limited to a maximum of 232. Even though the separation between the bonding pads was decreased from 65 μm to 25 μm, the total number of bonding pads required for all of the devices was still much higher than was possible. Therefore, certain bonding pads were shared between several different devices.

For example, the substrate or n-well of certain devices with the same gate width and length were connected to the same bonding pad. However, when a bonding pad is connected to more than one electrode region, the parasitic capacitance among the different electrode regions can interact and hence affect the threshold voltage of the devices. These parasitic effects were not found to be significant.
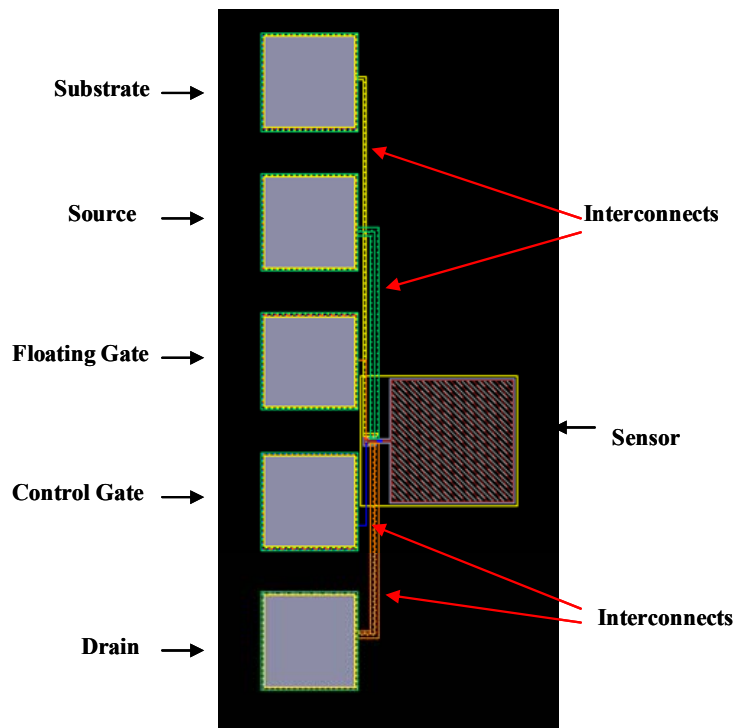
Figure 3-9:   *Sensor connected with the bonding pads and interconnects*

3.1.4 The First Chip Layout

The dimension of the first chip was 1.865 × 1.76 mm. A plan view of this chip layout is shown in Figure 3-10. The capacitors and the three multi-finger sensors were

placed on the right bottom quadrant.   Other sensors and reference transistors were placed on the remaining three quadrants and were grouped by the gate widths and lengths. Even though the devices introduced in the previous sections were all n-type, some p-type devices were also included for each type of sensor and reference transistor.
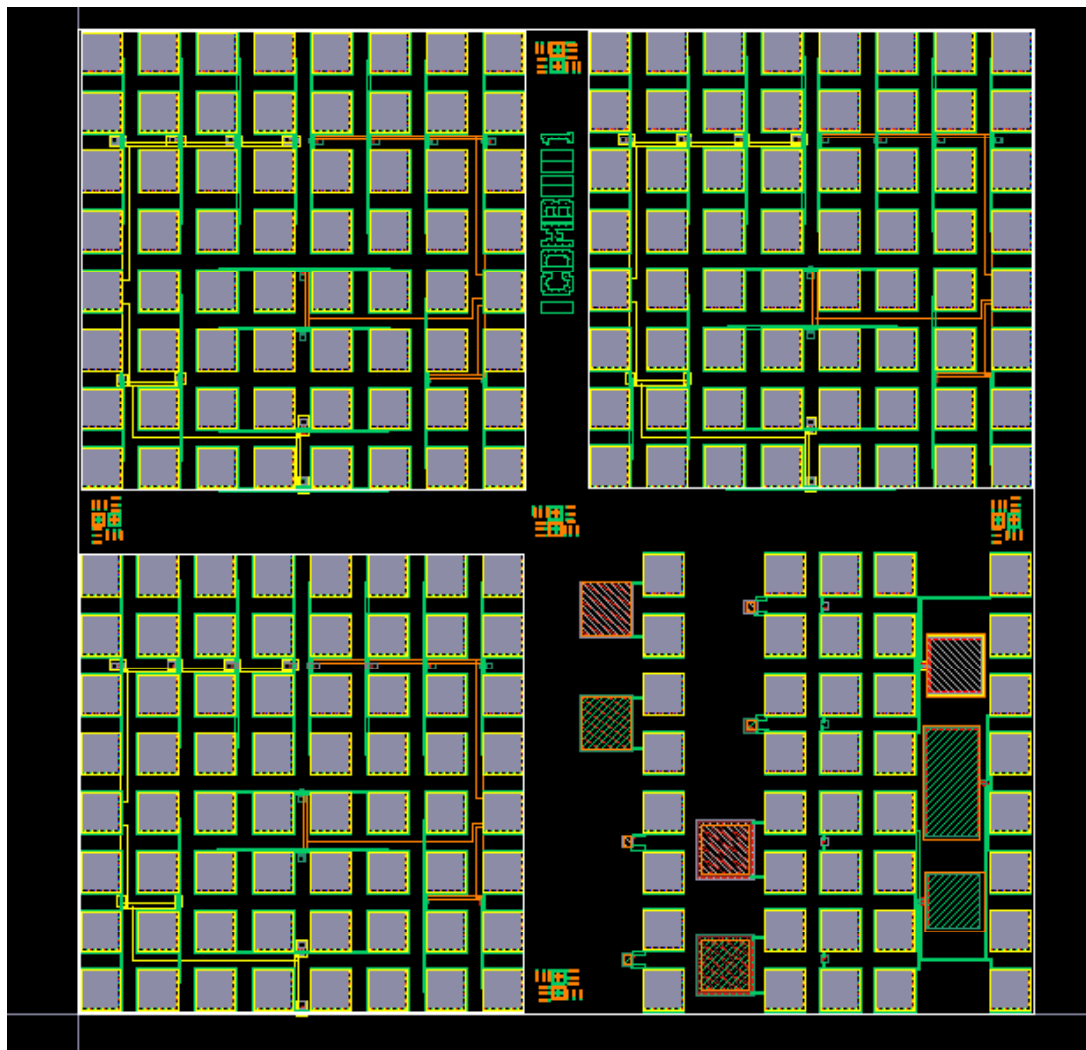
Top Left Quadrant	Top Right Quadrant
(W =5 μm, L =0.8 μm)	(W =3.6 μm, L =1.2 μm)
Bottom Left Quadrant	**Bottom Right Quadrant**
(W =3.75 μm, L =1.5 μm)	(W =3.75 μm, L =1.5 μm)

Figure 3-10:   *Top layout of the first iteration of sensor system design.*

The chip design also included the design of alignment marks that were used in post-processing. As mentioned previously, it was required to post-process the chip in order to expose the floating gate extensions. Photolithography, which was one of the post-processes and will be discussed in detail in Chapter 4, was used to transfer the image pattern printed on the photomask to the chip surface. To be able to align the chip with the photomask, alignment marks were required. These marks were a series of crosses and bands and are shown in Figure 3.11. Blue marks were formed by the top metal layer (Metal4) and were placed on the chip. Pink marks were made of chrome and were printed on the photomask. When two sets of alignment marks line up as shown, it represents that the chip is perfectly aligned with the photomask.
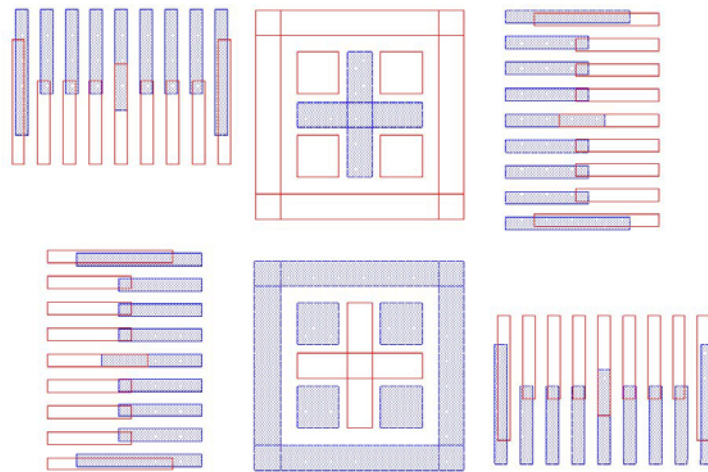
Figure 3-11: *Alignment Marks.*

The floating gate field-effect transistor is a device not generally fabricated with the 0.35 μm standard CMOS process. Therefore, several design rules had to be broken in

order to produce the floating gate structure.   These are discussed in some detail below.

In the 0.35 µm CMOS process, the bottom polysilicon layer (PO1) is usually used to form the gates of MOSFETs, while the top polysilicon layer (PO2) is used to build up resistors or capacitors.   Therefore, the PO2 layer is not allowed to pass over the gate dielectric as shown in Figure 3-12 a).[14]   However, a floating gate field-effect transistor is a two-gate device.   Both polysilicon layers (PO1 and PO2) should be used to form the two gates: the floating gate and the control gate.   Since the control gate was directly built up on top of the floating gate, these two polysilicon layers would have to be stacked vertically passing over the gate dielectric.   The aforementioned design rule was thus broken.   Figure 3-12 b) shows how this was implemented in the current work.

a)   b)
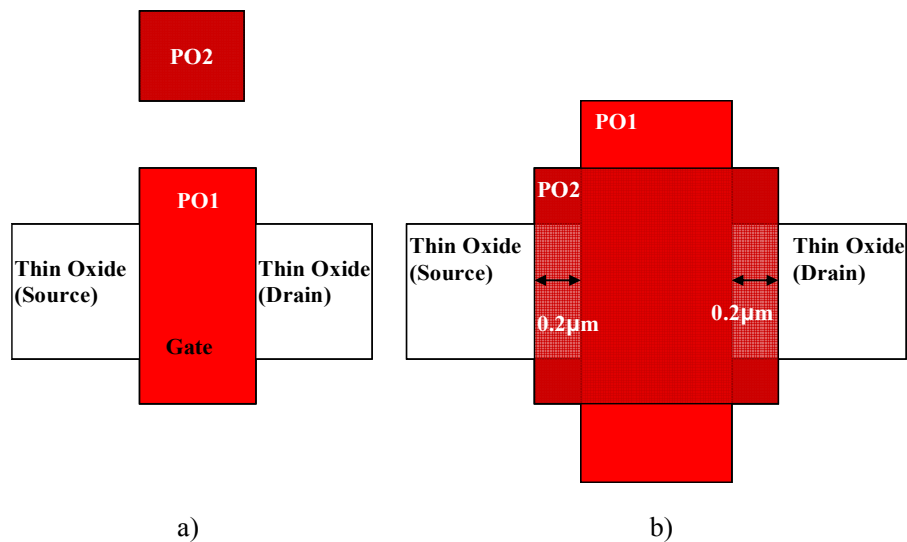
Figure 3-12: *a) Design rule: PO2 cannot pass over the thin oxide layer.   b) Design in the sensor system: Both polysilicon layers have to put on top of thin oxide layer.*

In the sensor design (see Figure 3-13 a)), the length of the control gate was designed to be 0.4 μm wider than the length of the floating gate in order to prevent the control gate to be over-etched during the formation of the floating gate. This broke the design rule schematically shown in Figure 3-13 b) which dictates that the minimum extension of the PO1 layer beyond the PO2 layer should be at least 1 μm.[14]
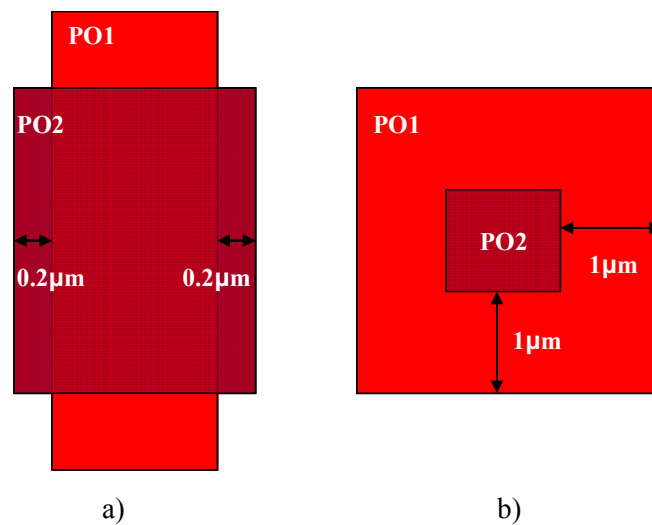
Figure 3-13: *a) Design in the sensor; b) Design Rule in 0.35 μm CMOS process.*

Another design rule that had to be broken related to the spacing of bonding pads. During the chip layout design, the clearance between the bonding pads was set as 105 μm to save "real estate" on the chip, which was less than the minimum clearance (150 μm) defined by the design rules (Figure 3-14) [14]. However, this clearance was still tolerable to the 0.35 μm CMOS process.
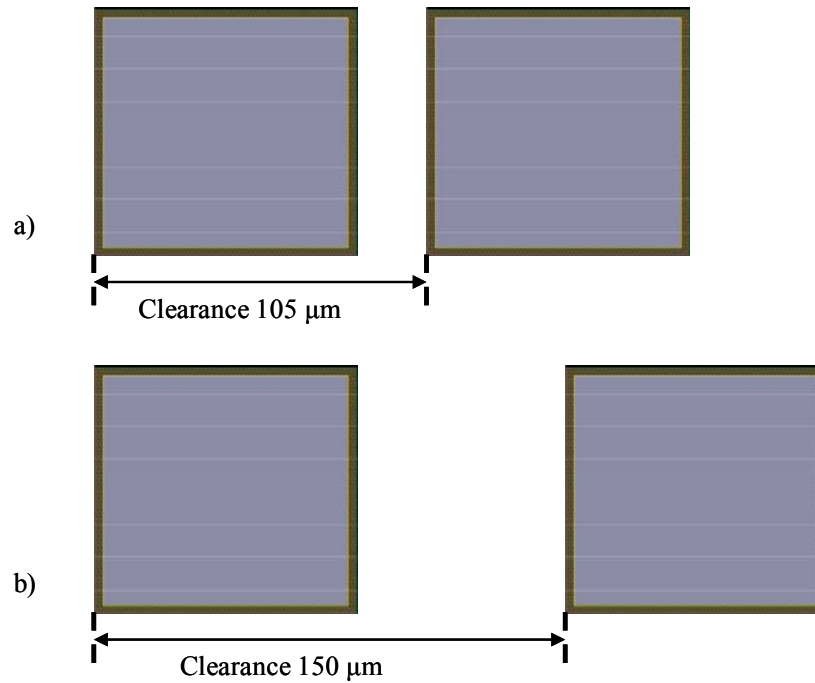
Figure 3-14: *The clearance between the bonding pads. a) The clearance used on the first chip; b) The clearance defined by the design rules.*

3.2 Results from the First Chip

Sensors designed in the first iteration were characterized and post-processed. In this section, the effects of the gate leakage current, undercutting, and bonding pad dimensions on the performance of the manufactured devices will be addressed.

3.2.1 Gate Leakage Current

When characterizing the designed sensors, it was found that devices could only be turned on after some charge was tunneled onto the floating gate. This charge only remained for a short period of time, indicating that there was a leakage current channel in

the device, particularly between the floating gate and the substrate.   Therefore, the sensor

structure was analyzed (see Figure 3-15).   In the sensor, the floating gate and the substrate

was isolated by a 7.5 nm gate dielectric, while the floating gate extension and the substrate

were isolated by a 270 nm field oxide.[14]   Due to the large difference in dielectric

thickness, the leakage current channel was more possibly formed in the gate dielectric,

especially if the gate dielectric was partly damaged by the charge that could have

accumulated during some of the plasma based CMOS processes.   This plasma processes

induced gate dielectric damage will be illustrated more in Section 3.3.1.
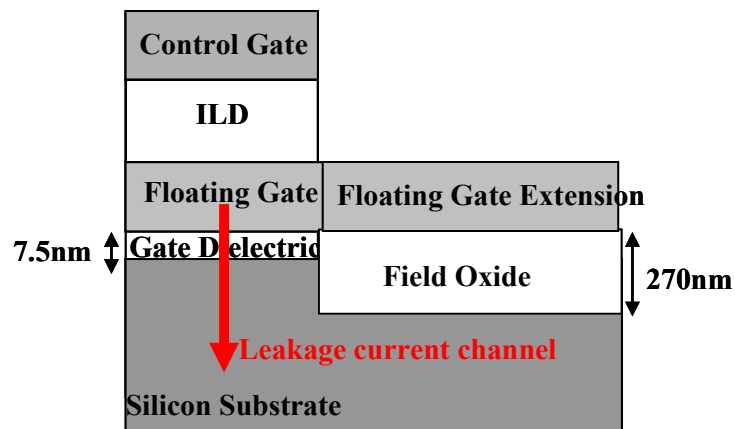
Figure 3-15:   *The gate dielectric and dielectrics used in the sensor.*

This large gate leakage current highlighted two issues.   First, the leakage current

degraded the gate dielectric leading to a poor performance of the field-effect transistor.

This will be discussed more in Chapter 5.   Second, the gate leakage current would affect

the charge stored on the floating gate.   It thus would be difficult to determine the effect

induced by the chemical reaction on the floating gate extension.

For these two reasons, the gate leakage current had to be reduced. One simple method is to temporarily isolate the floating gate extension from the field-effect transistor structure by using a metal jumper as was introduced in the second design.

3.2.2 Undercutting

Even though the floating gate extension was placed 5 μm away from the field-effect transistor to prevent the transistor from being damaged by the undercutting generated during wet etching, this distance was found to be inadequate. After a series of post-processing experiments, the transistor structures were found to be attacked or sometimes completely destroyed by the undercutting. In the second iteration (Section 3.3), the minimum separation between the floating gate extension and the FET was increased to at least 10 μm.

3.2.3 Bonding Pads

Bonding pads were used both for device characterization and for electrochemical deposition of the polymer. During the electrochemical deposition, a chip carrier (Figure 3-16) was used onto which the chip was bonded with the conducting silver epoxy. The bonding pads of the floating gates were wire bonded to the selected pads on the chip carrier and the test equipment was connected to the corresponding pin at the backside of the chip

carrier. The gold wires used in the wire bonding process were 25.4 μm in diameter. The bonds formed using these wires were found to be bigger than the designed bonding pads. In some cases, they were able to short the neighboring bonding pads on the chip. This issue was solved by increasing the space between adjacent bonding pads as well as by increasing the dimension of the bonding pads in the second design.
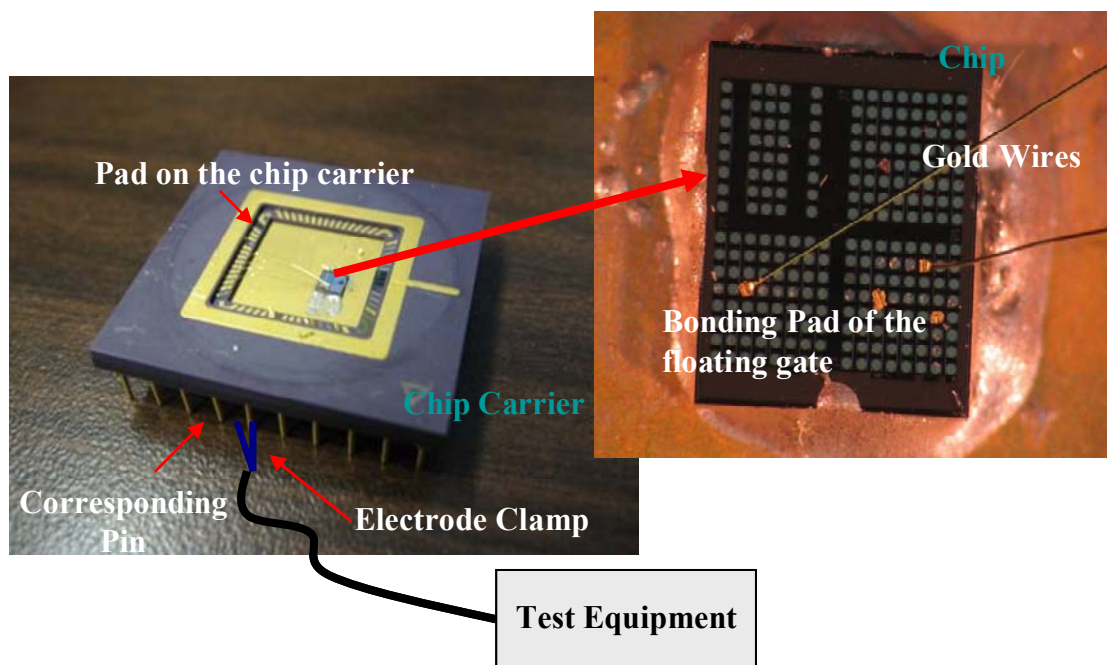
Figure 3-16: *Setup for electrochemical deposition of the sensitive polymer.*

3.3 Second Iteration of the Chemical Sensor Design

A second iteration of the sensor design was implemented to resolve the aforementioned issues that arose from the first chip (Section 3.2). Once again, sensors were fabricated using the same 0.35 μm CMOS process.

3.3.1 Sensor with the Improved Floating Gate Extension

The schematic diagram of the improved sensor structure is shown in Figure 3-17.

The floating gate extension was formed by the same polysilicon used for the control gate.

From the design rules of the 0.35 μm CMOS process, the dielectric thickness between the

floating gate extension and the substrate was increased to ~3070 Å[14] and the parasitic

capacitance between the floating gate extension and the substrate was reduced.   The

devices could therefore have a lower threshold voltage and a better I-V characteristic.

This will be discussed in detail in Chapter 5.
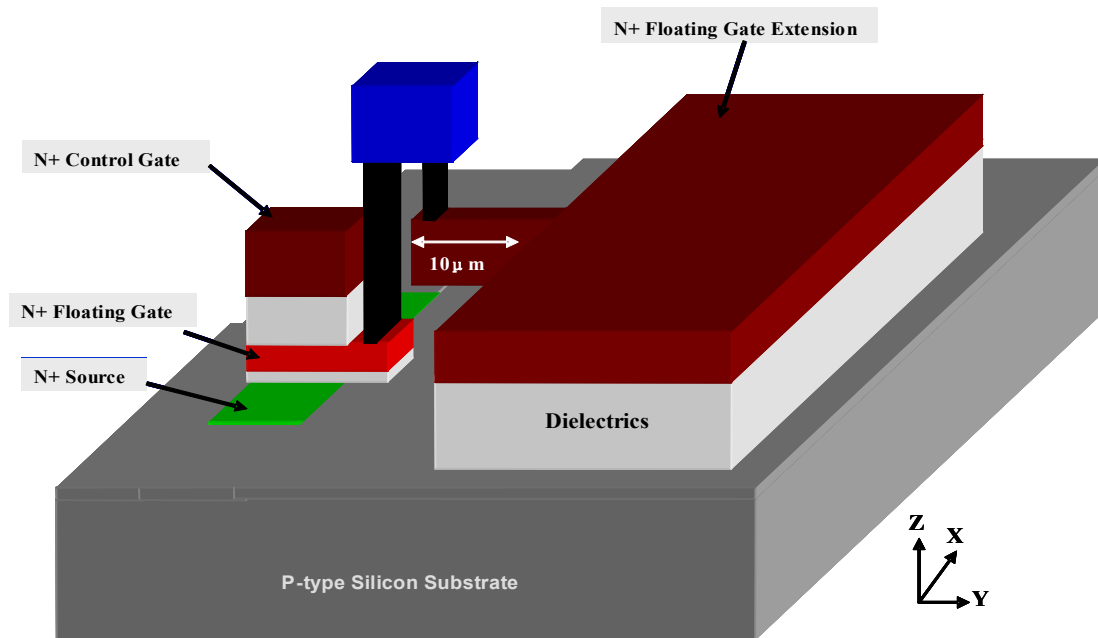
Figure 3-17: *3-D drawing of the improved sensor structure by using an N-type floating gate field-effect transistor.*

Since the doped polysilicon can behave as an n-type conductor or a p-type

conductor, the floating gate extension formed by the polysilicon layer could be put either in

an n-type sensor or in a p-type sensor.   As a result, the top polysilicon layer was selected as the substitute of the bottom polysilicon layer.

The floating gate extension was placed 10 μm away from the field-effect transistor to keep the undercutting from affecting the transistor structure.   Since the dimension of the gate extension was large, a metal jumper formed of the Metal1 layer was used to connect the floating gate extension and the floating gate of the field-effect transistor. During the sensor fabrication, the floating gate extension was not connected to the field-effect transistor until the metal jumper was formed.   This temporary isolation kept the gate dielectric from being damaged by the charge that could have accumulated during some of the plasma based CMOS processes.

This plasma processes induced gate dielectric damage is referred to as the antenna effect [15, 16, 17, 18].   It is produced in the aluminum or polysilicon processing when the plasma etching is used.   These metal layers are always covered by a non-conducting photoresist and built on top of an ILD layer, like a floating "island". During the plasma etching process, the charge can be stored on the sidewalls of these layers and induce a potential which may discharge through the oxide.   This creates the defects in the dielectrics and reduces the insulating nature of the gate dielectric or ILDs.   For MOSFETs, the gate damage during etching is an issue.   The discharging channel through

the gate dielectric must be temporarily broken in order to protect the transistor.

Two common methods to reduce the antenna effect include inserting additional diodes to shunt charge away and adding metal jumpers.[19] However, when a diode is placed into an antenna net, its parasitic effects also need to be considered and a different antenna model needs to be applied. These reasons make the insertion of the diodes problematic for this iteration design. Therefore, metal jumpers were used as shown by the plan view of the layout in Figure 3-18. Sensors of varying sizes were designed and are listed in Table 3-3. Six different gate width-to-length ratios were used. The floating gate extensions were 10×10, 20×20, 50×50 or 100×100 μm.
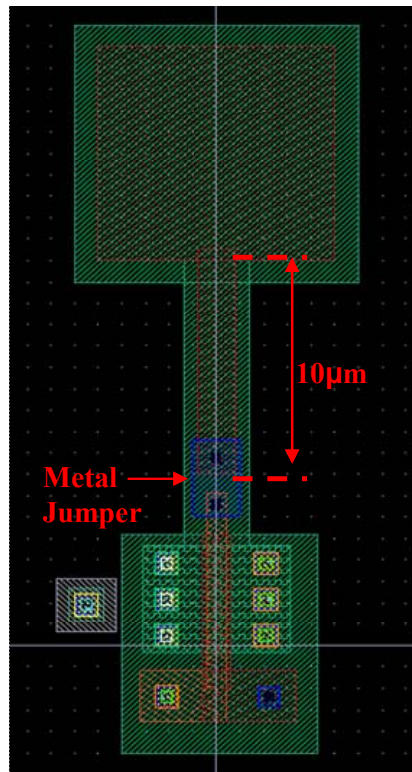
Figure 3-18: *The layout of an n-type sensor designed in the second iteration.*

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Table 3-2: *List of N/P type sensors designed in the second iteration with a floating Gate extension*

No.	Gate Length (μm)	Gate Width (μm)	Dimensions of the Floating Gate extension (μm x μm)	No.	Gate Length (μm)	Gate Width (μm)	Dimensions of the Floating Gate extension (μm x μm)
1	0.8	5	10 X10	13	0.8	40	10 X10
2	0.8	5	20 X 20	14	0.8	40	20 X 20
3	0.8	5	50 X 50	15	0.8	40	50 X 50
4	0.8	5	100 X 100	16	0.8	40	100 X 100
5	0.8	8	10 X10	17	1.2	6	10 X10
6	0.8	8	20 X 20	18	1.2	6	20 X 20
7	0.8	8	50 X 50	19	1.2	6	50 X 50
8	0.8	8	100 X 100	20	1.2	6	100 X 100
9	0.8	16	10 X10	21	1.2	12	10 X10
10	0.8	16	20 X 20	22	1.2	12	20 X 20
11	0.8	16	50 X 50	23	1.2	12	50 X 50
12	0.8	16	100 X 100	24	1.2	12	100 X 100

3.3.2 The Second Chip Layout

Devices designed in the second iteration were connected with interconnects and bonding pads and then placed on a 2.5 × 2.5 mm chip (see Figure 3-19). Interconnects to the source, drain, floating gate and control gate were formed using the different metal layers (Metal1 - Metal4). The dimensions of bonding pads were increased to 85 × 85 μm and the separation between the bonding pads was increased to 35 μm to allow for the easier wire bonding. Due to a larger chip area, fifteen sets of alignment marks were used on this chip as opposed to only five sets on the first chip.

Dummy Pads
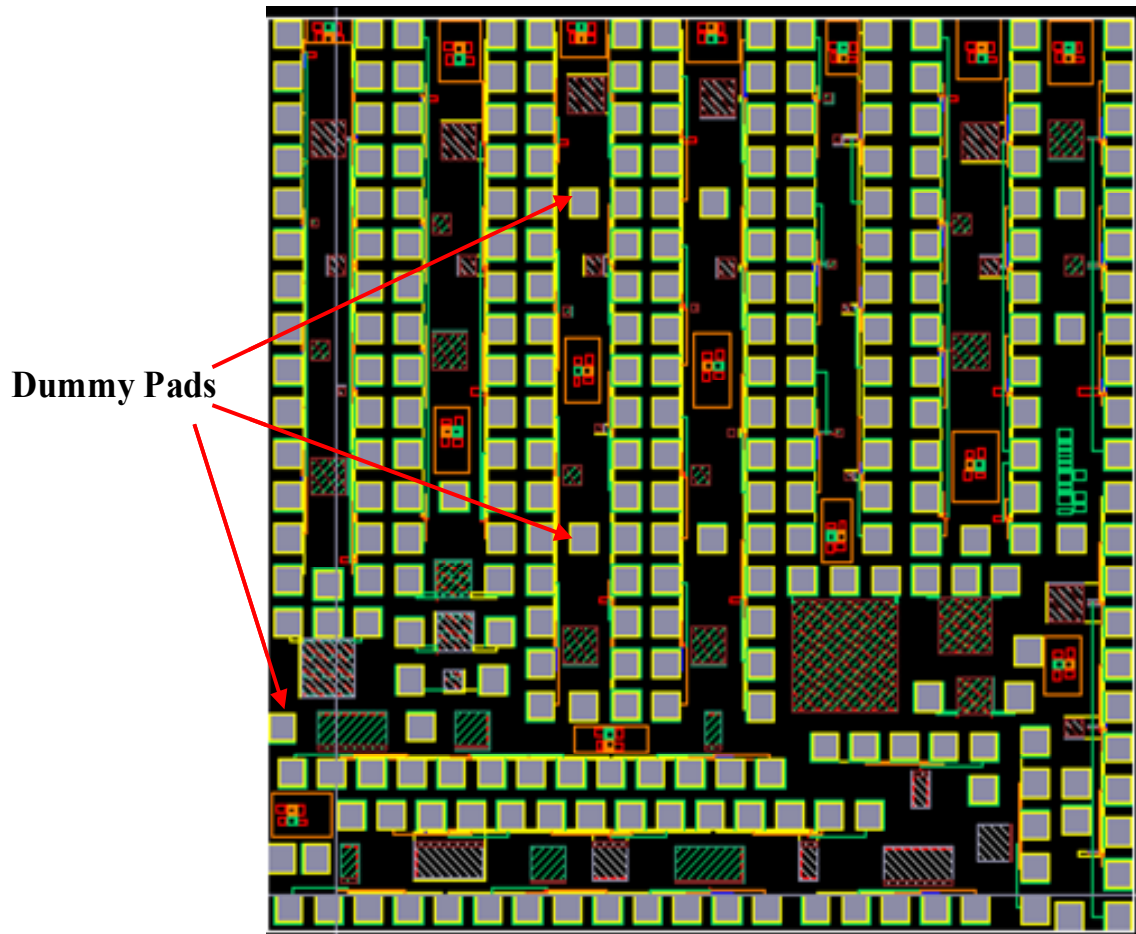
Figure 3-19: *Second iteration of the chip design.*

After the chip layout was complete, the metal density was found to be less than 30% of the overall area - the minimum metal density dictated by the design rules of the 0.35 μm CMOS process. The low metal density could induce the dishing issue [20] after the chemical mechanical polishing (CMP) process. As illustrated in Figure 3-20, the surface of ILDs would display a cylindrical shape (dishing) after polishing. This "dishing" could affect the adjacent metal patterns and thus negatively affect the

interconnect performance. Since it could be reduced by increasing the metal density, many 80 × 80 μm dummy pads were placed on the chip. These dummy pads were smaller than the normal bonding pads so that more space could be left between the dummy pads and the bonding pads or interconnects connecting to the devices.

| Metal | ILD | Metal | After Metal Patterning |

Dishing

| Metal | ILD | Metal | After CMP |

Dishing

| Metal | ILD | Metal | After CMP with the increased metal density |
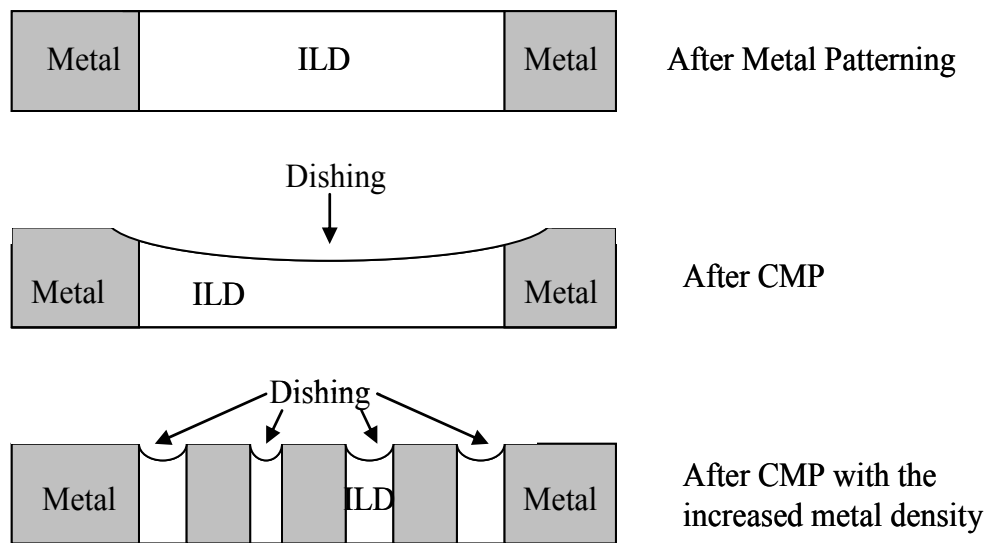
Figure 3-20: *The dishing could be reduced by increasing the metal density.*

Chapter 4 The Minimum Post-processing to Expose the Floating Gate Extension

After the chips were fabricated using TSMC's 0.35 μm CMOS process, the floating gate extension of each sensor was covered by the dielectrics approximately 7 μm thick. The procedure for exposing these floating gate extensions is described in Figure 4-1. These dielectrics were anisotropically etched away using a reactive ion etching (RIE) technique. To allow etching only in the extension areas, the bonding pads, interconnects and the field-effect transistors of sensors were protected by the patterned mask layer. As shown in Figure 4-1 b), aluminum was used as the "hard mask" since it has a much lower etch rate in the RIE processes used, especially when a high DC bias voltage was applied. In Figure 4-1 c) the cross-section of an exposed device after the removal of the two metal layers are shown.

Therefore, twelve post-processing steps were implemented in the Nano Systems Fabrication Laboratory (NSFL) at the University of Manitoba. As demonstrated in the Figure 4-2, these steps were grouped into five major processes: 1) the metal deposition process, 2) the photolithography process, 3) the wet etching process, 4) the plasma etching process and 5) the wet etching process. In this chapter each process will be illustrated,

processing problems will be discussed and the results will be presented.
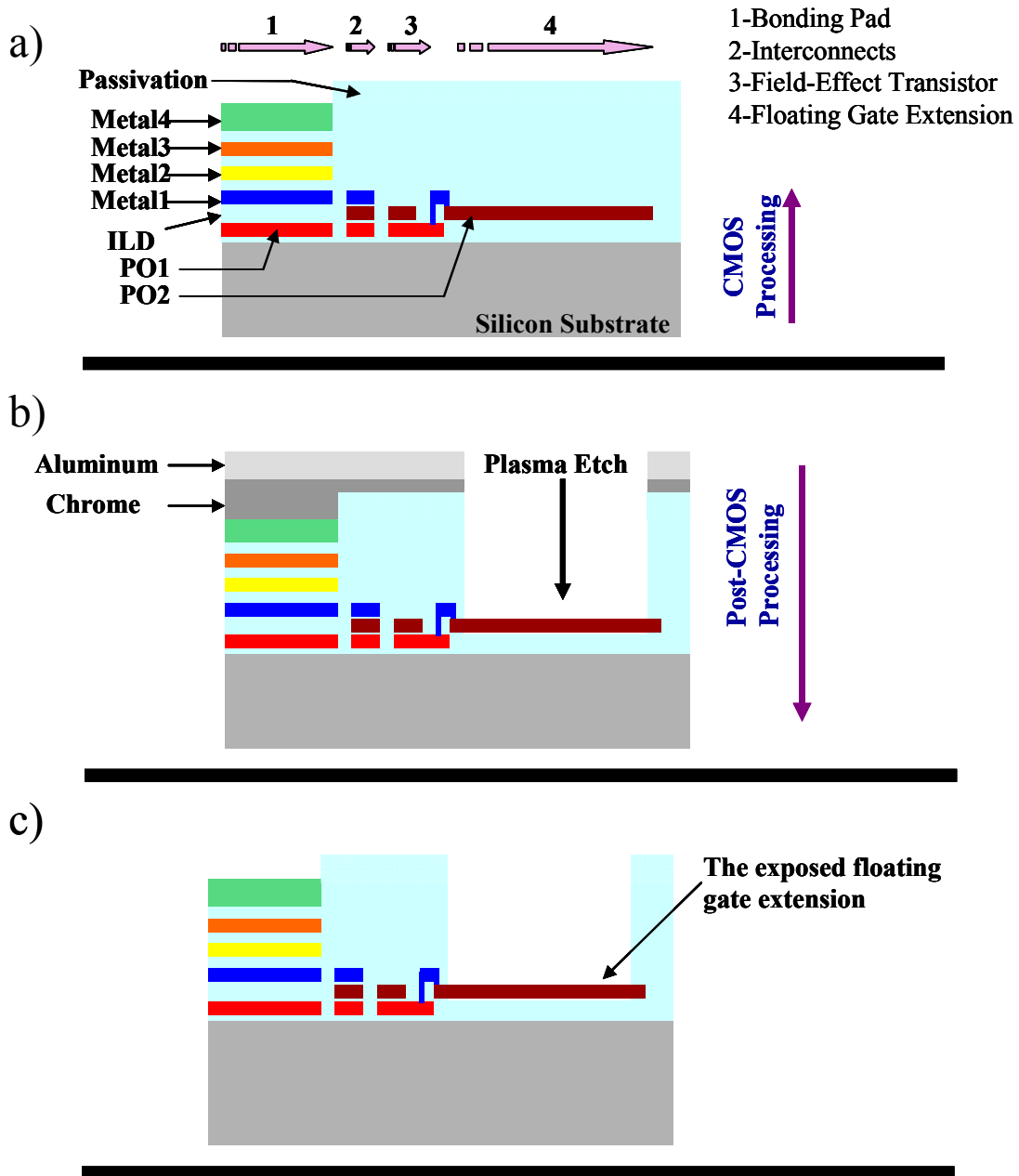
Figure 4-1: *Process flow. a) The structure after the CMOS processing; b) use Al metal "hard" mask to etch the dielectrics and expose the floating gate extension; c) structure after metal mask removal.*

```
┌─────────────────────────────┐
│ Step 1: Sputtering the      │
│ Chrome Layer                │
│           ↓                 │          ➤ 1.Metal Deposition
│ Step 2: Sputtering the      │             Process
│ Aluminum mask               │
└─────────────────────────────┘
              ↓
┌─────────────────────────────┐
│ Step 3: Photoresist Coating │
│           ↓                 │
│ Step 4: Soft baking         │
│           ↓                 │
│ Step 5: Hard Contact Lithography ➤ 2.Photolithography
│           ↓                 │             Process
│ Step 6: Developing          │
│           ↓                 │
│ Step 7: Hard baking         │
└─────────────────────────────┘
              ↓
┌─────────────────────────────┐
│ Step 8: Patterning  the     │
│ Aluminum  Mask              │
│           ↓                 │          ➤ 3.Wet Etching
│ Step 9: Patterning the      │             Process
│ Chrome Layer                │
└─────────────────────────────┘
              ↓
┌─────────────────────────────┐
│ Step 10: Reactive Ion Etching│
│ (the Passivation Layer and  │          ➤ 4.Plasma Etching
│ the ILD)                    │             Process
│           ↓                 │
└─────────────────────────────┘
              ↓
┌─────────────────────────────┐
│ Step 11: Stripping Off the  │
│ Aluminum Mask               │          ➤ 5.Wet Etching
│           ↓                 │             Process
│ Step 12: Stripping Off the  │
│ Chrome Layer                │
└─────────────────────────────┘
```

Figure 4-2:   *Twelve steps to expose the floating gate extensions.*

4.1 Metal Deposition Process

In this work, the application of the "hard mask" was necessary since several issues were found when using a photoresist "soft mask" in the RIE process. First, it was found that during etching the photoresist could be sputtered and re-deposited on the exposed areas, and thus caused the contamination as shown in Figure 4-3 a). Second, with the applied RIE power, the photoresist was found to be etched away faster than the dielectrics. Therefore, two metal layers were deposited on the chip surface and patterned (see Figure 4-3 b)). A thick aluminum layer was used as the "hard mask" in the RIE process. The thin chrome layer was used to separate the aluminum bonding pads from the aluminum mask so that the bonding pads were protected during the chemically stripping of the aluminum mask.
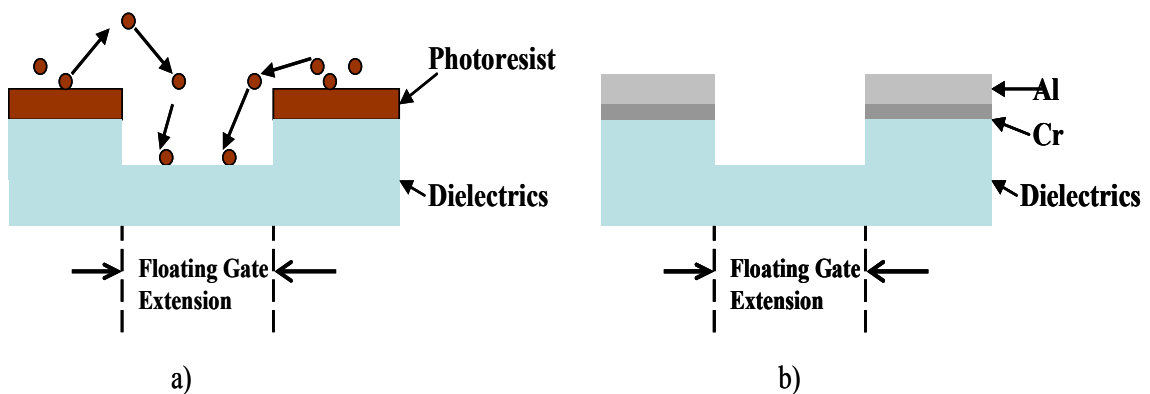
Figure 4-3: *"Soft mask"-photoresist and "hard mask"-metal layers. a) photoresist was found to be sputtered and re-deposited on the floating gate extensions to be exposed; b) Al and Cr were deposited on the chip surface and patterned.*

Sputtering and evaporation are two technologies widely used for metal deposition. Since metals deposited by sputtering have a better step coverage than metals deposited by thermal evaporation [21], aluminum (Al) and chrome (Cr) layers used in this project were deposited by sputtering.
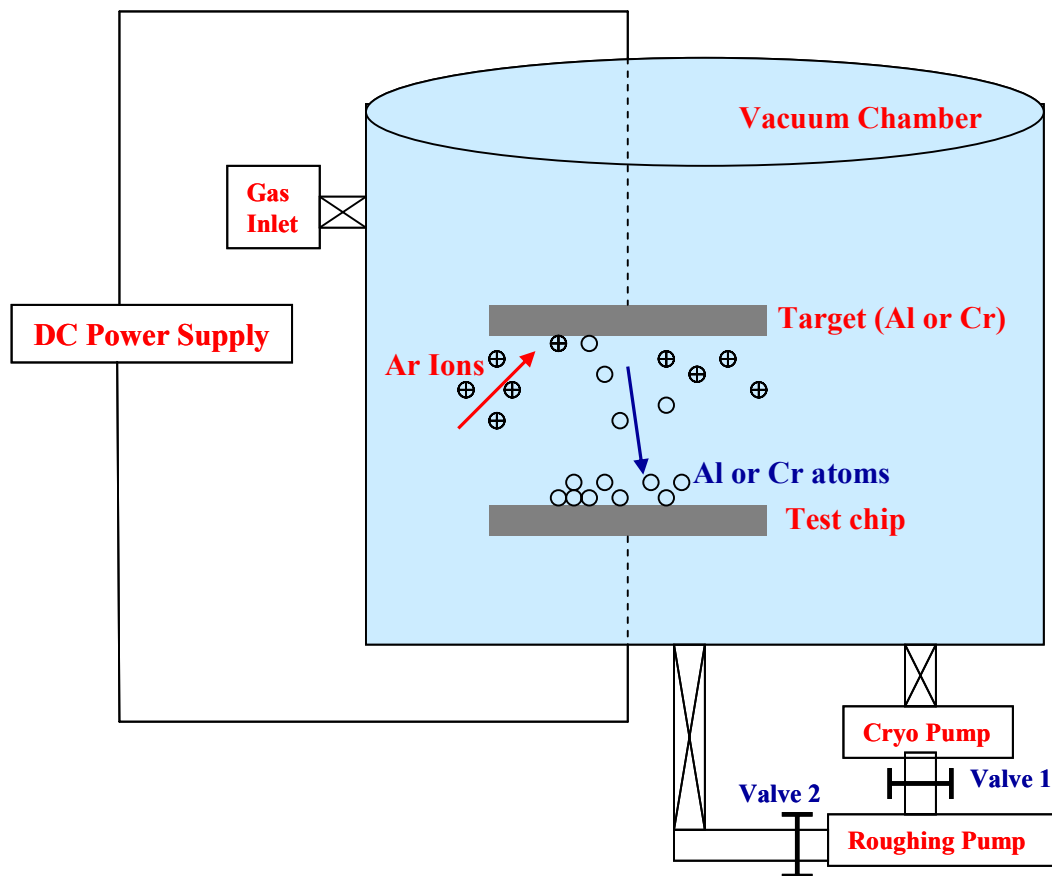
Figure 4-4: *The metal deposition process in a parallel-plate sputtering system. [21]*

The deposition process using a parallel-plate sputtering system is illustrated in Figure 4-4. A DC power is applied across the target and the test chip. In the sputtering process, positive argon ions were generated in the vacuum chamber. These high energy

ions were driven towards the cathode and hit the Al or Cr target. Metal atoms were ejected from the target and deposited on the test chip placed below.

The chrome layer was deposited first on the chip. For the deposition of the chrome, the chamber pressure was 10 mTorr (set with an Argon flow rate 41 sccm). The applied DC power was 200 Watts. With a deposition rate of ~66 nm/min, a chrome layer of ~165 nm was deposited in 2.5 minutes.

The aluminum layer was sputtered following the chrome deposition. Although little aluminum would be etched away during the RIE process, the surface roughness of Al after etching was found to be increased to more than 200 nm. It was measured using the Tencor Alpha Step 500 Surface profiler. Therefore, a thick aluminum layer was deposited. For the aluminum sputtering, the applied DC power was 200 Watts, and the pressure was approximately 10^{-2} torr. The Al thickness was ~300 nm deposited in 5.5 minutes yield a deposition rate of ~54.5 nm/min.

4.2 Photolithography Process

Photolithography is a process used to transfer the pattern from the photomask to the photoresist. It includes five basic steps: photoresist coating, soft baking, hard contact lithography [21], developing and hard baking.

4.2.1 Photoresist Coating

4.2.1.1 Photoresist

Photoresist is a photosensitive material used to transfer an image pattern onto the chip surface. Photoresist is a polymer compound typically composed of three components: a resin or base material, a photoactive compound and a solvent. [21] When the photoresist is exposed to the ultraviolet (UV) light, the photoactive compound enables the absorbed UV photons to react with the bonds to change the chemical structure of the photoresist. Both positive and negative resists exist such that the UV light either breaks or cross-links bonds to make the photoresist softer or harder when developed. Therefore, a pattern which is the same as the one printed on the photomask can be transferred onto the chip surface by a positive photoresist and a reversed image pattern can be transferred using a negative photoresist. Positive resists tend to have the better resolution.[21] Olin Hunt HPR 504 was the positive photoresist used in this project.

4.2.1.2 Spin Coating Process

The photoresist was uniformly coated onto the test chip using a Machine World positive photoresist spinner which is shown in Figure 4-5. During the spin coating process, the test chip was held in place by a vacuum chuck. The chuck and the test chip were rotated at approximately 3000rpm, while the photoresist was poured onto the surface

of the chip ensuring a uniform film on the chip.
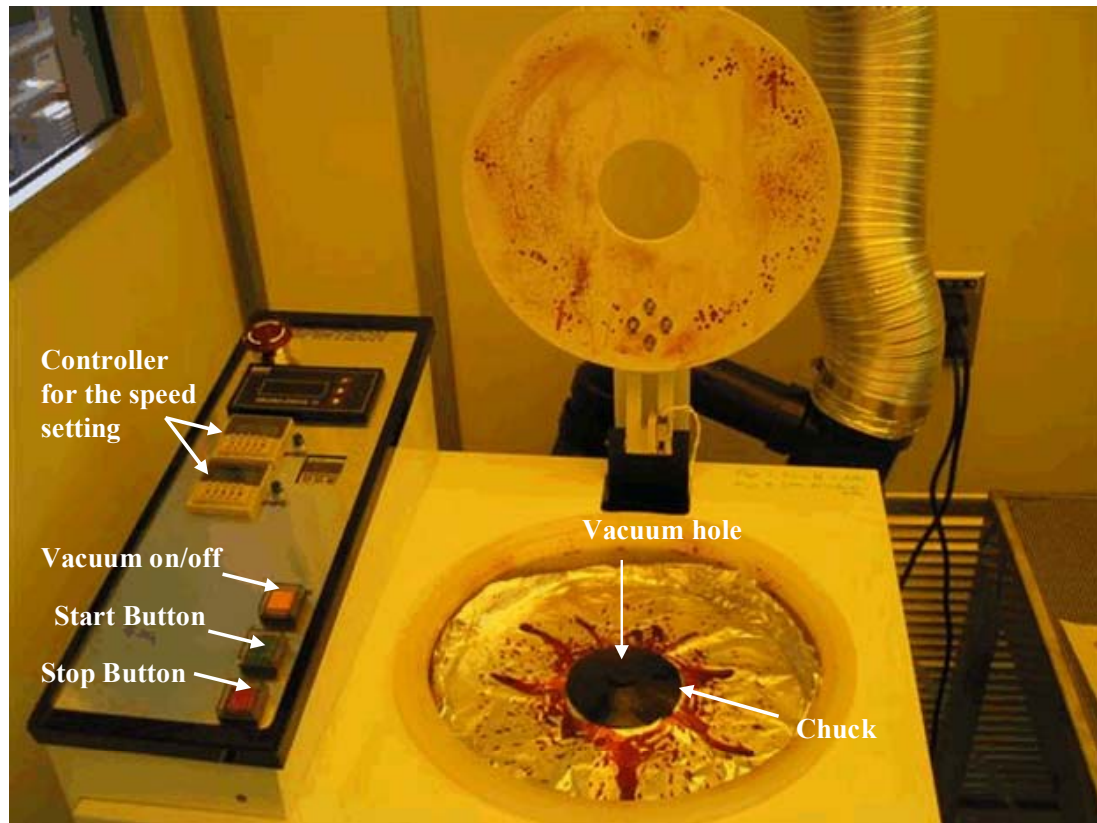
Figure 4-5:   *Photoresist Spinner.*

Due to the small size of the chip deigned, the chip needed to be fixed to a larger

three inch silicon wafer, which was then held in place on the chuck for the photoresist

coating. However, resist bumps or "edge beads" were found to form at the corners or along

the edges of the test chip as shown in Figure 4-6.   With rotation of 3000 rpm, a photoresist

layer of approximately 1.5 μm was formed on the chip surface with the edge beads forming

over approximately 15%-25% of the area.   The edge beads were approximately 4.5 to 5.5

μm thick.

Chip areas are exposed after the contact lithography

Edge Beads
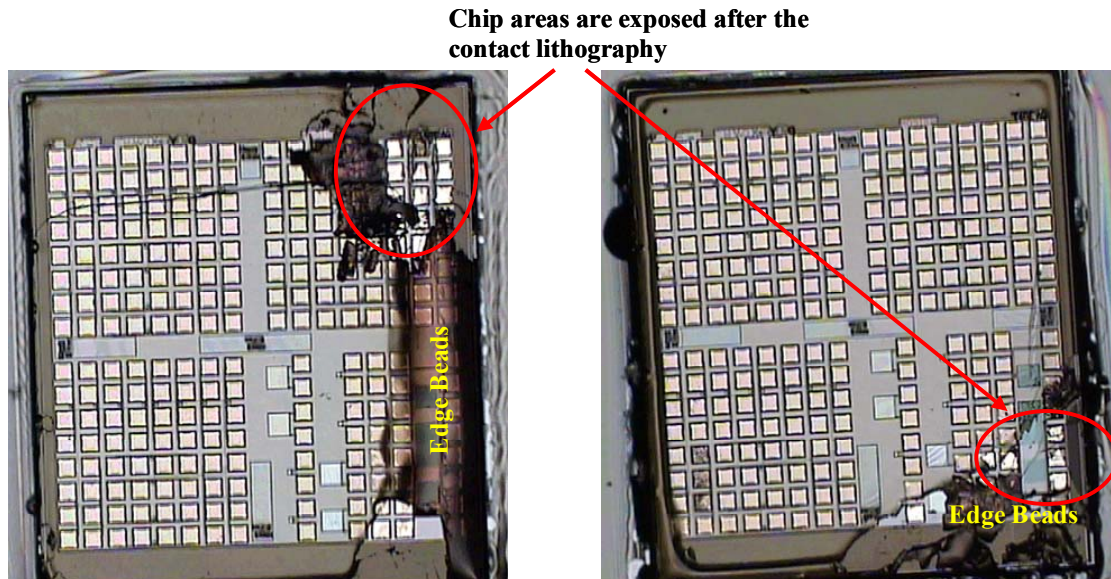
Edge Beads

Figure 4-6: *Edge beads on the chip.*

As a result of edge beads, two main issues were discovered. First, the resolution was decreased, and the minimum feature size that could be exposed was increased. This issue can be illustrated using the Fresnel diffraction theory [21] for contact lithography. The minimum feature size within the Fresnel range is given by

$$W_{min} \approx \sqrt{k\lambda g} \qquad (4.1)$$

where W_{min} is the minimum feature size, k is a constant which depends on the photoresist process and g is the resist thickness.[21] As the photoresist thickness increases, the minimum feature size also increases. Therefore, edge beads increase the minimum feature size. To maintain the required resolution, edge beads had to be reduced to be used with contact lithography. Second, photoresist in some areas (see Figure 4-6) was removed

manually. This photoresist was found to be deposited onto the photomask during alignment. Even though the photomask could be cleaned using the acetone, the edge beads affected such a large portion of the chip that they needed to be removed or at least reduced in size and thickness. As a result, two methods discussed below were used to obtain a uniform photoresist layer and eliminate this edge bead problem.

The first method attempted was to use the chip socket shown in Figure 4-7 a) during spin coating process. This chip socket was made of aluminum and contained a recessed area where the chip was to be placed. The depth of the recess is the same as the thickness of the test chip. A hole was drilled through the bottom of the socket for a vacuum connection to hold the chip during high speed spinning. The chip socket was set on the chuck as shown in Figure 4-7 c).
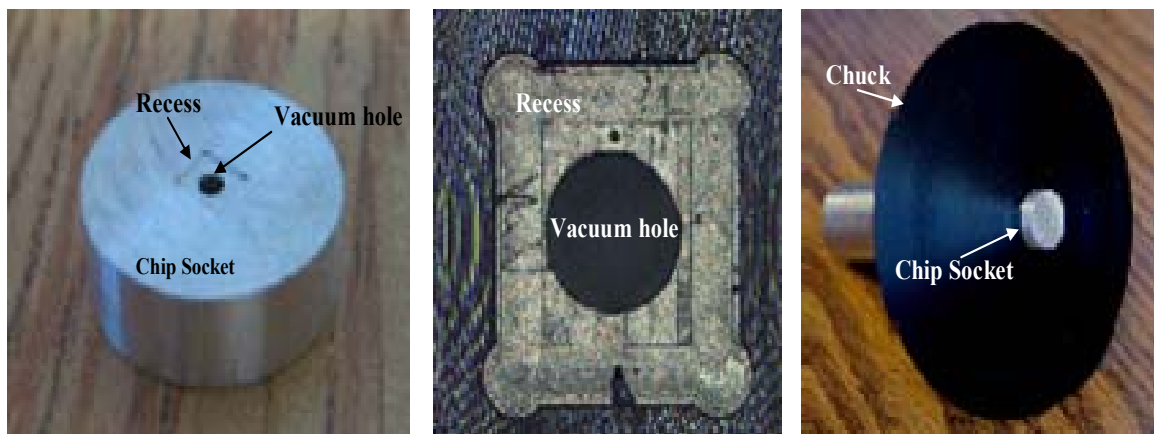
Figure 4-7: *a) The chip socket; b) The hole in the center of the chip socket to pass the vacuum; c) The chip socket is put on the chuck used in the spin coating process.*

The extended chip socket surface area was intended to reduce the edge beads generated on the chip. However, the recess was not a perfect fit to the test chip such that there were spaces at the corners of the recess and between the edges of the chip and the sidewalls of the recess as shown by arrows in the Figure 4-8. It was also found that the depth of the recess was not a perfect fit such that the top of the chip lay above the socket's surface. This was due to a combination of limitations of the machining of the socket and a lack of knowledge regarding the precise silicon wafer thickness. This is illustrated schematically in Figure 4-8 b). Unfortunately, this meant that the edge beads were not eliminated or even reduced.
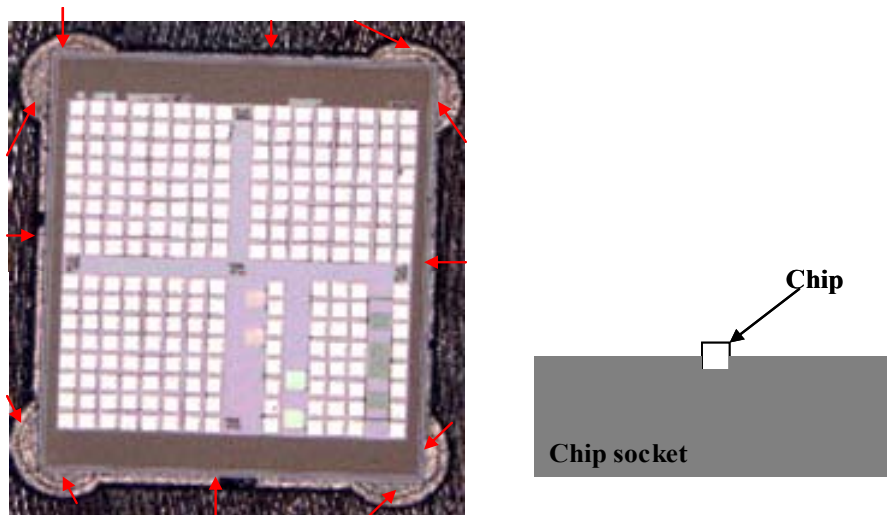
Figure 4-8: *Illustration of the chip and the chip socket showing a) the space between the chip and the notch edge(red arrows); b) the chip surface residing above the socket.*

The second method attempted was using the photoresist to attach the chip onto a three inch silicon wafer. To be able to obtain the repeatable experimental results, the test

chips were always placed at the center of the wafer with one side parallel to the flat cut of

the wafer as shown in Figure 4-9.
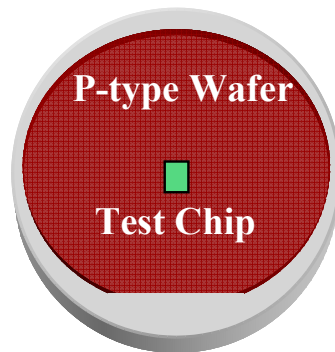
Figure 4-9:   *Chip position relative to the silicon wafer before the spin coating.*

During the spin coating experiments, the edge beads were expected to be found

in the same regions if the test chips were started spinning from the same position.   For

example, when the test chips were started spinning from the position (90 degrees in the

counterclockwise direction) shown in Figure 4-10 a), the edge beads were only found

along the side A and side B.   These results suggested that if two dummy chips could be

connected in series with the test chip (see Figure 4-10 b)), the edge beads would be

generated along the side C and the side D while the test chip, in the middle, would remain

uniformly coated.   In Figure 4-11 a test chip is shown, which was uniformly coated with

photoresist using this method.   As shown, the edge beading problem was almost

eliminated on this chip.
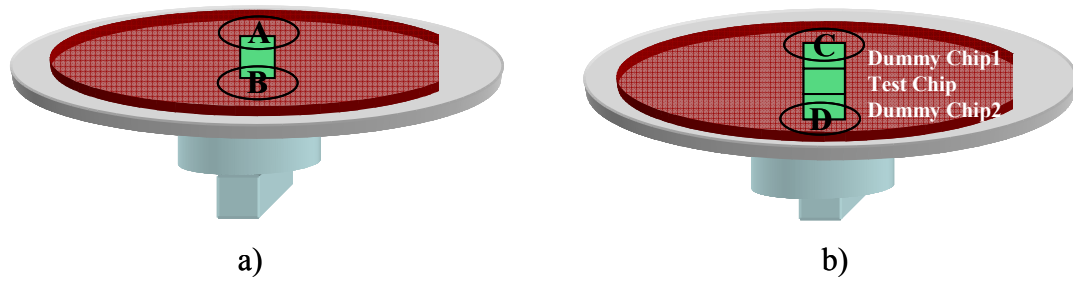
Figure 4-10:   *Two positions that will have edge beads after the spin coating process.*
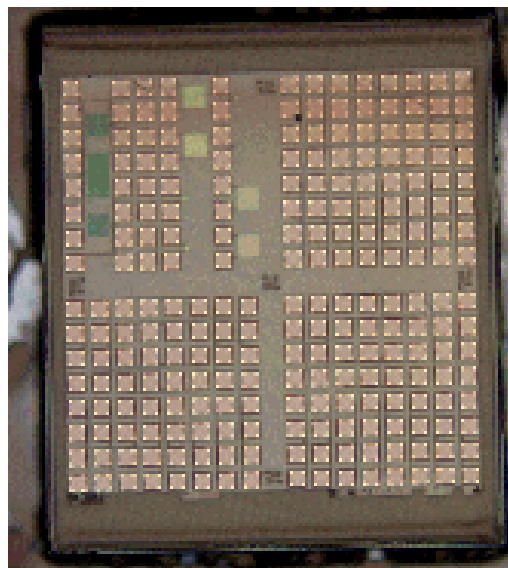
Figure 4-11:   *A test chip coated with a layer of the uniform photoresists.*

The biggest advantage of this method was that it could be operated using a standard procedure demonstrated in Figure 4-12.   To start the process for patterning the chip, the silicon wafer was rotated at a low speed (1000 rpm) to coat a layer of thick photoresist onto which the test chip would be placed.   Before the photoresist dried, the test chip and two dummy chips were immediately placed in the center of the wafer.   They were

then put on a hot plate for the soft baking to harden the photoresist at 110ºC for 60 seconds.

After the sample was cooled down, another spin coating process was initiated. A higher

speed (3000 rpm) was used to coat a photoresist layer to approximately 1.5 μm. The two

dummy chips were then removed from the silicon wafer right after the photoresist was

coated. Only the wafer with the test chip was exposed to a second soft bake. The test

chip was now ready for the next post-process: Hard Contact Lithography.

Step 1: Put the wafer on the chuck

Step 2: Spin the photoresist on the wafer at 1000 rpm for 35 seconds

Step 3: Stick three chips on the wafer & soft-bake at 110ºC for 60 seconds

Step 4: Put the wafer on the chuck

Step 5: Spin the photoresist on the chip at 3000 rpm for 35 seconds

Step 6: Remove two dummy chips and soft-bake the wafer at 110ºC for 60 seconds
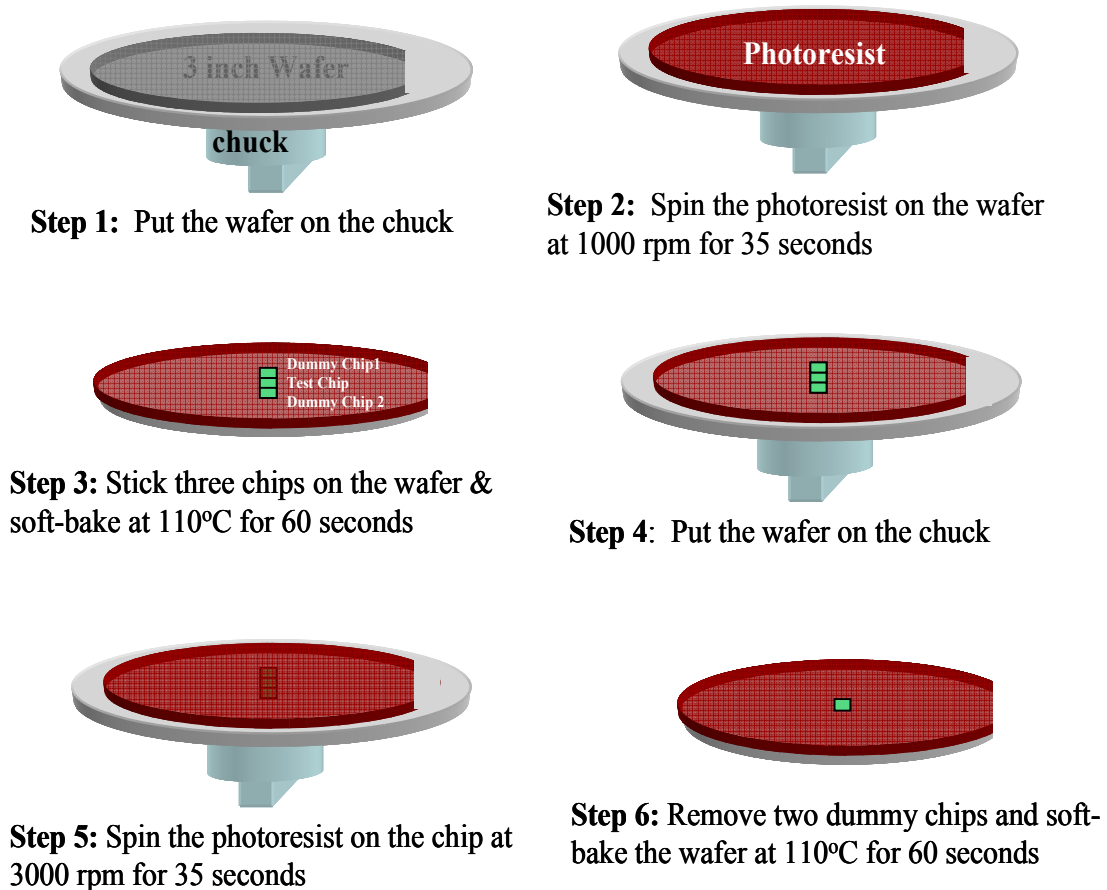
Figure 4-12:   *The standard procedure for the chip spin coating process (2nd method).*

4.2.2 Hard Contact Lithography

The ABM 6 inch Two-Sided Mask Aligner was used for all post-processing lithography (see Figure 4-13).
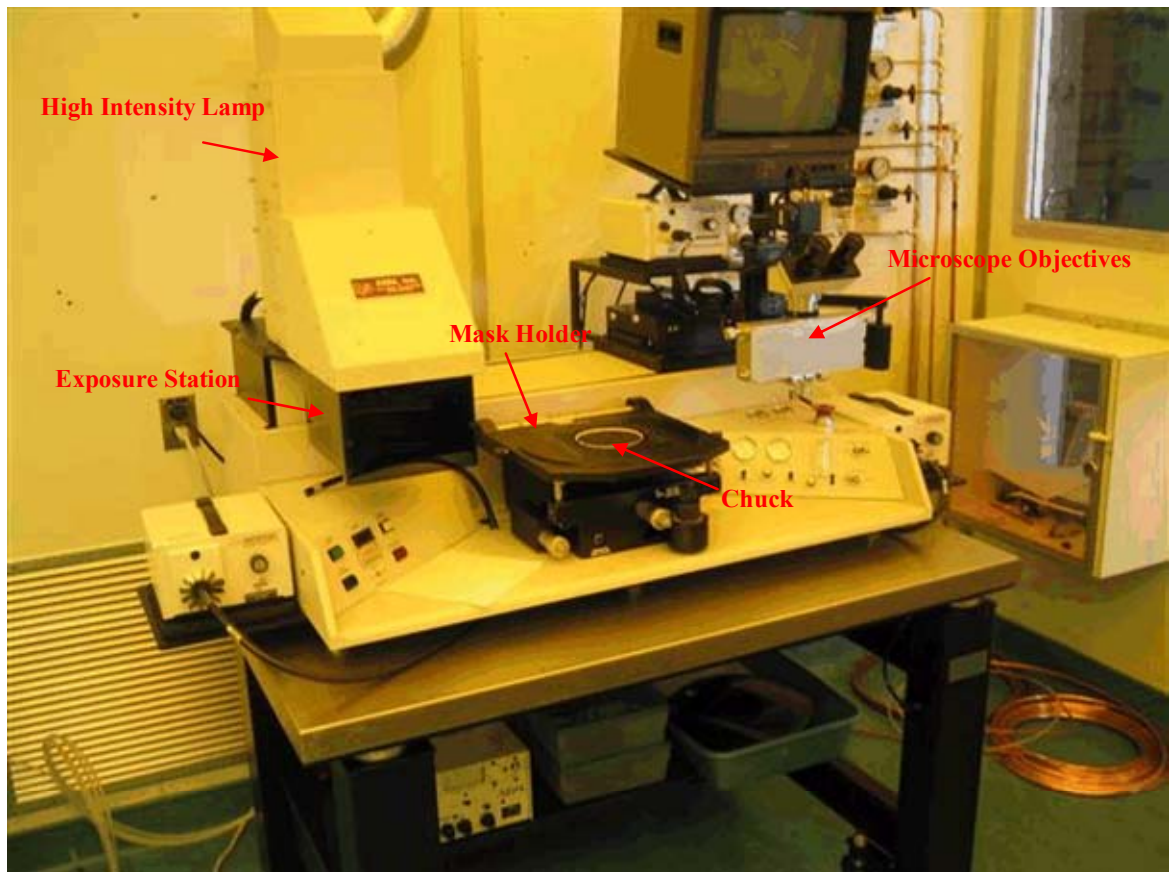
Figure 4-13: *ABM 6 inch Two-Sided Mask Aligner (a contact mode printer).*

The procedure used to perform the lithography is described as follows. The chip was put on the chuck and the photomask was placed on the mask holder with the chrome side down. During alignment, the microscope objectives were moved above the photomask and the X, Y and angle differential micrometers were used to align the chip to

the photomask.   When the alignment is finished, the microscope objectives were retracted, the photomask and the chip were brought into contact and the exposure station was then moved above the photomask/chip.   The UV light from the high intensity Hg-arc lamp was used to expose the wafer for 10 seconds for the 1.5 μm photoresist.   The exposure station was then retracted and the chip was unloaded.   Due to the 0.05 atm pressure used to bring the photomask in contact with the photoresist coated chip, this exposure process is referred to as hard contact lithography.[21]

4.2.3 Developing

Developing is a process to form the photoresist image on the chip surface.   The photoresist exposed to the UV light was etched away in the chemical solutions and the photoresist unexposed remained on the chip.   In this project, the test chip was immersed in the Microposit^{TM} 352 developer for 25 seconds to pattern the photoresist.

4.2.4 Hard Baking

To improve film adhesion and to make the photoresist more resistant to the exposure to the subsequent chemical solution used in the wet etching process, the chip with the patterned photoresist was "hard baked" at a temperature of 120ºC for 20 minutes.

4.2.5 Photomask Design

As mentioned previously, a photomask was used in the lithography process.

The photomask is fabricated on a highly polished fused silica with a high degree of optical transparency at the exposure wavelength.[21]   On one side of this silica is coated with a patterned opaque layer usually made with chrome.   Since the UV light can pass through the transparent silica but be absorbed or reflected by the opaque chrome, the photoresist coated on the chip surface was patterned.

In this work, two photomasks (5" × 5") were designed and fabricated in the NanoFab at the University of Alberta.   A plan view of the photomask layout design for the first and second iterations of this chip design are shown in Figures 4-14 and 4-15 respectively.   On each photomask, the chip design (1.865 × 1.76 mm or 2.5 × 2.5 mm) was replicated one hundred times in a 10 × 10 array.   However, only one of the hundred would be used during the lithography process.   The layout designs of two single masks are shown in Figure 4-14 b) and 4-15 b).   The pink square covered areas were left open and the black areas were covered by chrome.   In the single mask designed for the second chip, the substrate windows were used to make it easier to perform a gross alignment of the relatively small chip underneath the photomask which is mostly opaque.
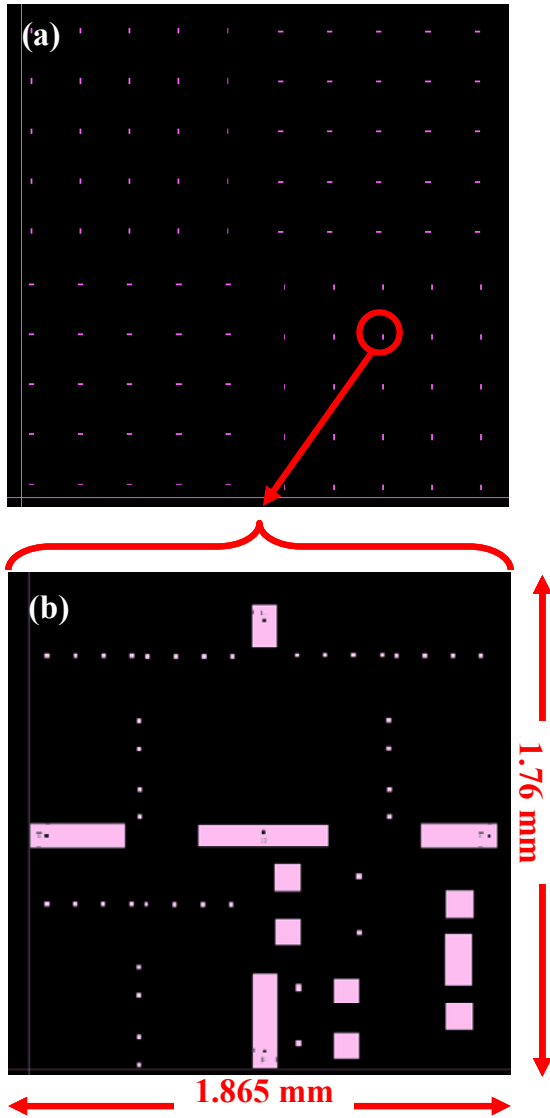
Figure 4-14: *a) Photomask of the first chip; b) single mask of the first chip.*
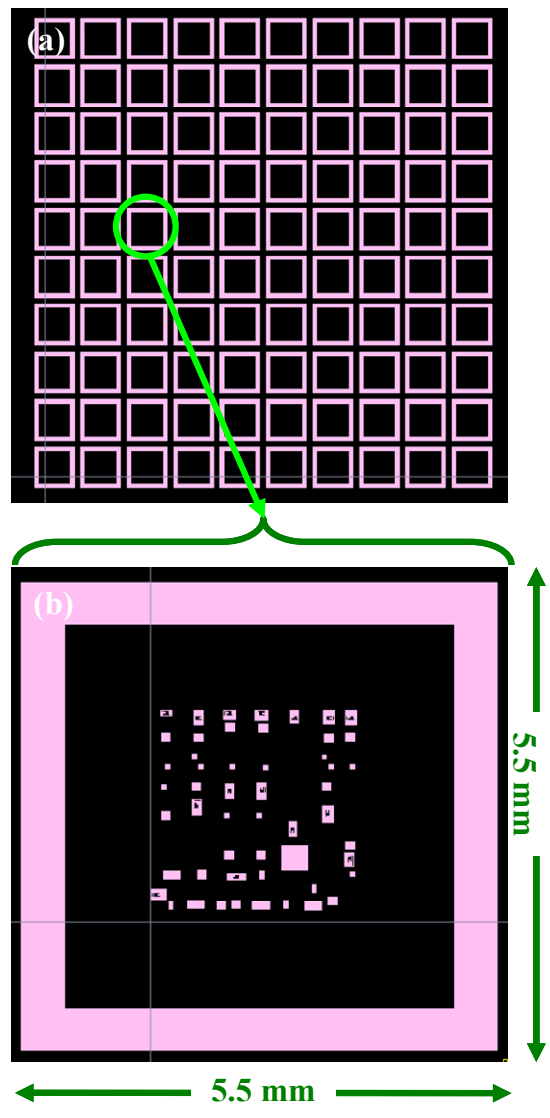
Figure 4-15: *a) Photomask of the second chip; b) single mask of the second chip.*

4.3 Wet Etching Process

The image was transferred to the metal layers under the photoresist using a wet etching technique. In general, wet etching involves only three basic steps: 1) the chip

surface is exposed to the etchant species, 2) the etchant reacts with the exposed film (the

metal in this case) and produces the soluble by-products and 3) the reaction by-products are

removed from the chip surface. Since the etchants have the different etch rates for

different materials, wet etching can be highly selective.[21] As well, the undercutting

generated in the wet etching was tolerable to the sensor structure since the aluminum and

chrome layers were relatively thin. Due to these reasons, the wet etching was selected to

pattern two metal layers.

During the aluminum patterning, the chip was immersed in a beaker filled with

the H_3PO_4 phosphoric solution (70% phosphoric acid, 15% acetic acid, <5% nitric acid).

The solution was heated up to 50ºC to increase the etch rate. Under these conditions, the

~300 nm aluminum was etched away within 1.5 minutes with an etch rate of ~200 nm/min.

The chrome layer was patterned using HNO_3 nitric acid (15% ceric ammonium

nitrate, <7% nitric acid). With an etch rate of ~165 nm/min, it took about one minute to

etch away the deposited 165 nm chrome layer. However, this etch rate could only be used

as a reference. It was found that the etching time could vary greatly even for the chrome

layer with the same thickness. It made the chrome etching very difficult to control. This

was one disadvantage of using the chrome in this work.

The wet etching was not only used to pattern these two metal layers but also used

to strip them off after the floating gate extensions were exposed. The same chemical solutions and etching conditions were used.

4.4   Plasma Etching Process

The series of dielectrics on top of the floating gate extensions were removed by plasma etching. Since this was an anisotropic etching process, the undercutting was small enough to not affect the other parts of a sensor. The photoresist was removed using the acetone before the plasma etching process started to prevent the contamination of the floating gate extensions caused by patterning and re-deposition as stated previously.

4.4.1 Why Plasma Etching?

For the patterning of the different materials used in microelectronics fabrication, three techniques are commonly used: wet etching, plasma etching and ion milling. Wet etching can be undesirable in this work due to the large undercuts that may be produced during long etch periods. Undercutting could seriously damage these sensors due to the close proximity of the extension area, to be etched, to the transistor. Ion milling can be a difficult process to use as it is purely a physical attack process where high energy ions are generated and accelerated towards the chip. Any exposed materials on the chip surface will be removed at the same time with a similar etch rate resulting in very little selectivity.

Therefore, in order to etch away the ~7 μm dielectrics stack above the floating gate extension, the Al mask would need ~7 μm thick to protect the bonding pads, interconnects and other sensors on the chip. The application of the thick metal mask can bring about issues such as a longer deposition time and the larger undercutting in the wet etching, which would make the post-processing even more difficult. These issues are to some extent reduced when plasma etching is used. Plasma assisted etching (or reactive ion etching) includes both the chemical and physical etching and usually has a reasonably high selectivity (the ratio of etch rates of various materials) and etch rate. Furthermore, it is an anisotropic etching process enabling the generation of the fine features with a high aspect ratio. All of these advantages led to the use of plasma etching to remove the dielectrics above the extension areas.

4.4.2 Plasma Etching Technique

The general plasma etching involves many processes. This is illustrated in Figure 4-16. When the reactive gas flow passes through a plasma environment, the reactive species (or free radicals / ions) are generated. Reactive radicals diffuse to the substrate surface and are absorbed. Depending upon their energy, radicals reside on the surface or slightly penetrate the surface. Upon exposure to the film to be etched, a chemical reaction occurs. The gaseous reaction by-products are desorbed from the

surface, diffusing into the plasma, and are pumped out of the reactor.[22] Different

reactive gases are used for various substrate materials. For example, the gas mixtures of

CF_4 and O_2 are commonly used to etch away the silicon nitride layer, while the SF_6 and O_2

plasma are typically for etching silicon.
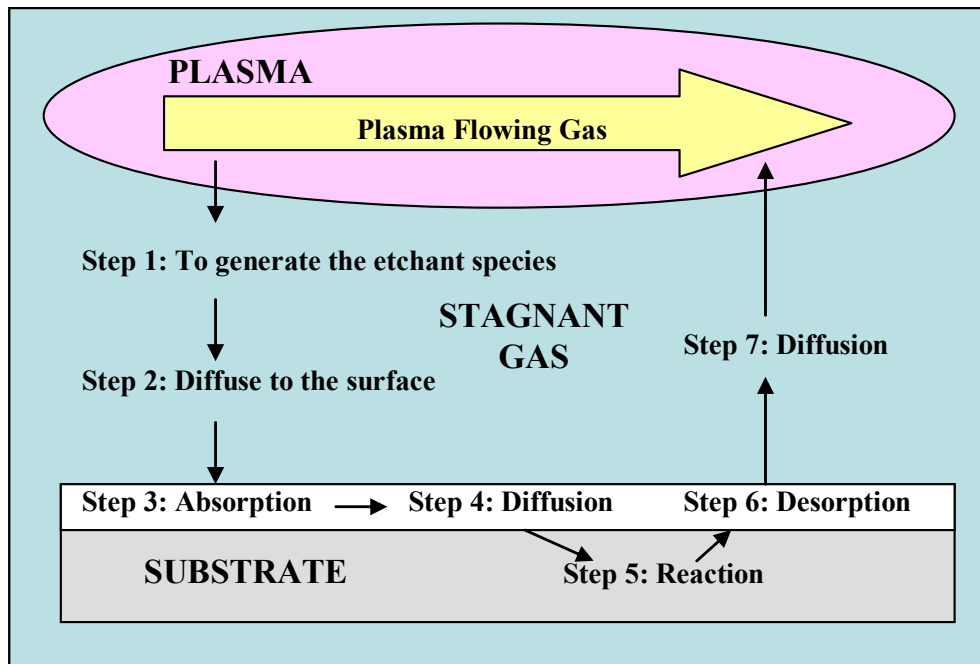
Figure 4-16: *A schematic of a plasma etching system.[21] [22]*

4.4.3 Trion ICP Plasma Etcher

The plasma etching system used was a RIE/ICP plasma etcher produced by Trion

Technology. It is a system used to etch nitrides, oxides and any films requiring

fluorine-based chemistries. This etching system (see Figure 4-17) includes an inductively

coupled plasma (ICP) source, which reduces the radiation damage and contamination from

the RIE sputtering and allows for higher plasma densities as power is transferred into the bulk plasma via a magnetic field resultant from the inductive coupling.[21]   It thus allows the etching process to be implemented at a lower pressure so that the tight anisotropy in high aspect ratio structures can be achieved.
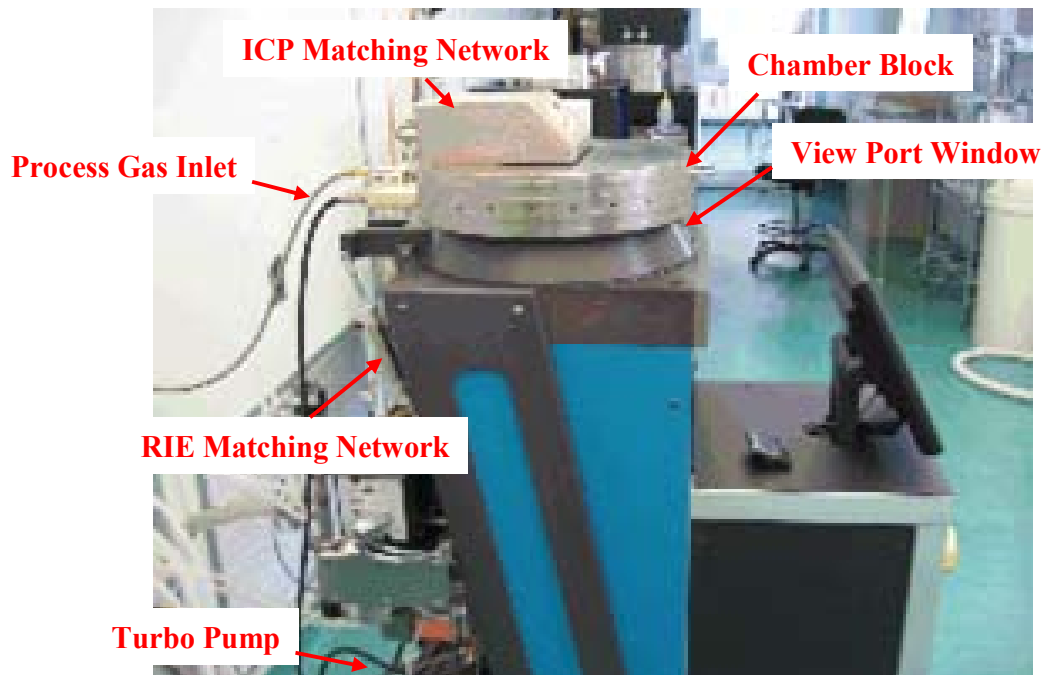
Figure 4-17:   *A photo of the Trion ICP Plasma Etcher.*

4.4.4 Plasma Etching of Dielectrics

The dielectric stack to be etched consists of a silicon nitride layer, the silicon-oxy-nitride layer and four "inter-layer dielectric" (ILD) layers.   According to the specifications of TSMC's 0.35 μm CMOS process, the silicon nitride layer is approximately 1.2 μm, the silicon-oxy-nitride layer is approximately 0.3 μm and the total

thickness of all ILD layers is approximately 4.8 μm.[14]   In this section, etching recipes

for the different dielectrics will be presented.

4.4.4.1 Etching the Silicon Nitride Layer

The first general gas mixture attempted to etch the silicon nitride layer consisted

of CF_4 (45 sccm) and O_2 (5 sccm).[21]   However, carbon-fluorine based polymer residue

was found in the extension regions.   These consisted of cylinder shaped materials with the

axis-oriented normal to the surface.   To reduce or eliminate this residue, the O_2

concentration in the gas mixture was increased.   The extra O_2 reacted with the carbon

atoms and increased the fluorine atomic concentration in the plasma.   Due to the reduction

of carbon atoms in the plasma, the amount of the polymer generated was greatly

reduced.[21]   Through a series of experiments, the CF_4 to O_2 ratio was decreased to a final

value of 8.3.   With this gas ratio, the silicon nitride layer was etched in 5 minutes without

the generation of any observable polymers.   The RIE recipe for the silicon nitride layer is

summarized in Table 4-1.

Table 4-1:   *RIE Recipe for the silicon nitride layer*

CF_4 (sccm)	50	Processing Time (min)	5
O_2 (sccm)	6	Etch Rate (nm/min)	~240
ICP Power (W)	300		
RIE (W)	100		
Pressure (mTorr)	100		

4.4.4.2 Etching the Silicon-Oxy-Nitride Layer

At the end of the Si_3N_4 etching process, the etch rate suddenly dropped, which

indicated that the silicon nitride was etched away and a new underlying layer (i.e.,

silicon-oxy-nitride) was exposed.   Since the etch recipe for silicon nitride was found not to

significantly etch the silicon-oxy-nitride, a new etch recipe was required. In this new recipe,

the reactive gas mixtures were changed to CHF_3 and O_2.[23]   The different parameter

settings are listed in Table 4-2.

Table 4-2: *RIE Recipe for the silicon-oxy-nitride layer*

CHF_3 (sccm)	22	Processing Time (min)	~3.5
O_2 (sccm)	32	Etch Rate (nm/min)	~90
ICP Power (W)	400		
RIE (W)	75		
Pressure (mTorr)	50		

4.4.4.3 Etching the ILD Layer

One of the most difficult parts in RIE was to find a good recipe that could quickly

etch away the thick ILD layer, achieve a reasonable surface roughness and have a high

selectivity of SiO_2 to Si.   Two batches of recipes were developed.   Although neither

recipe could reach a sufficiently high selectivity, a second batch of recipes was found to be

able to quickly etch away the thick ILD layer with a reasonable surface roughness.

However, to be able to successfully expose the floating gate extensions, these recipes still needed to be improved.

The first developed recipe had a low O_2 concentration in the gas mixture so that both C and F atoms could react with the O atoms in the ILD and a high etch rate was achieved. Initially, the CHF_3 to O_2 ratio was set as 4.[23]

In order to test how the etch rate and surface roughness could be affected by the different parameters, such as the ICP power, RIE power and pressure, a series of RIE experiments were implemented by using wafers with a layer of ~2 μm SiO_2. By only changing one parameter at a time, five different recipes were created and tested. Samples were etched for 10 minutes. By calculating the SiO_2 thickness difference before and after RIE etching, the etch rates of the different recipes were obtained. The SiO_2 thickness was measured using the Nanometrics Nanospec 210 resist and dielectric thickness measurement system. The surface roughness after RIE was measured using Veeco EnviroScope Atomic Force Microscope. The average surface roughness within the measured area is symbolized by R_a. The comparison results are shown in Tables 4-3, 4-4 and 4-5.

Table 4-3:   *Recipes with the variable RIE power*

	Recipe1	Recipe2	Recipe3
RIE Power (W)	**100**	**75**	**50**
ICP Power (W)	350	350	350
Pressure (mTorr)	25	25	25
CHF_3 (sccm)	20	20	20
O_2 (sccm)	5	5	5
Etching Time (mins)	10	10	10
Thickness of the etched SiO_2 (nm)	1586.2	1068.3	522.4
Etch Rate (nm/min)	158.62	106.83	52.24
Surface Roughness R_a (Å)	11.3	13	9.4

Table 4-4:   *Recipes with the variable ICP power*

	Recipe2	Recipe4
RIE Power (W)	50	50
ICP Power (W)	**350**	**200**
Pressure (mTorr)	25	25
CHF_3 (sccm)	20	20
O_2 (sccm)	5	5
Etching Time (mins)	10	10
Thickness of the etched SiO_2 (nm)	522.4	414
Etch Rate (nm/min)	52.24	41.4
Surface Roughness R_a (Å)	9.4	6.97

Table 4-5: *Recipes with the variable pressure*

	Recipe4	Recipe5
RIE Power (W)	50	50
ICP Power (W)	200	200
Pressure (mTorr)	**25**	**100**
CHF_3 (sccm)	20	20
O_2 (sccm)	5	5
Etching Time (mins)	10	10
Thickness of the etched SiO_2 (nm)	414	171.2
Etch Rate (nm/min)	41.4	17.12
Surface Roughness R_a (Å)	6.97	2.37

From these experimental results, the etch rate decreases with the decreasing RIE power, and increasing ICP power and pressure.   At most of times, the surface roughness decreased with increasing etch rate.   To be able to maintain a good etch rate and a reasonable surface roughness, the RIE power was set as 100 W, the ICP power was set as 200 W and the pressure was set as 25 mTorr.

The next experiment was to vary the O_2 concentration in the gas mixtures.   It was found that the etch rate was increased with the reduced O_2 concentration. The surface roughness was also improved.   This was ascertained using the results shown in Table 4-6.

Table 4-6: *Recipes with the variable O_2 concentration in the gas mixture*

	Recipe6	Recipe7
RIE Power (W)	100	100
ICP Power (W)	200	200
Pressure (mTorr)	25	25
CHF$_3$ (sccm)	20	20
O$_2$ (sccm)	**5**	**0~1**
Etching Time (mins)	10	10
Thickness of the etched SiO$_2$ (nm)	799.9	977.6
Etch Rate (nm/min)	79.99	97.76
Surface Roughness R$_a$ (Å)	6.31	0.284

To make the etching even faster, the amount of reactive gases were doubled resulting in a new recipe shown in Table 4-7.

Table 4-7: *The first RIE Recipe for ILD that has been tested on the designed chip*

CHF$_3$ (sccm)	40	Etch Rate (nm/min)	>50
O$_2$ (sccm)	2		
ICP Power (W)	200		
RIE (W)	100		
Pressure (mTorr)	25		

This recipe was tested on the designed chip. However, three main issues were found. First, the actual etch rate could not be easily obtained since the Al mask was also etched at the RIE power used. Second, a thick Al mask (>0.7 μm) was required to be able to protect the chip from the long etching (~80 minutes). Third, some unknown material with the green color (see Figure 4-18) was deposited on the exposed areas. This material stayed at

the surface and blocked the further etching. Therefore, the first recipe was found

inappropriate.
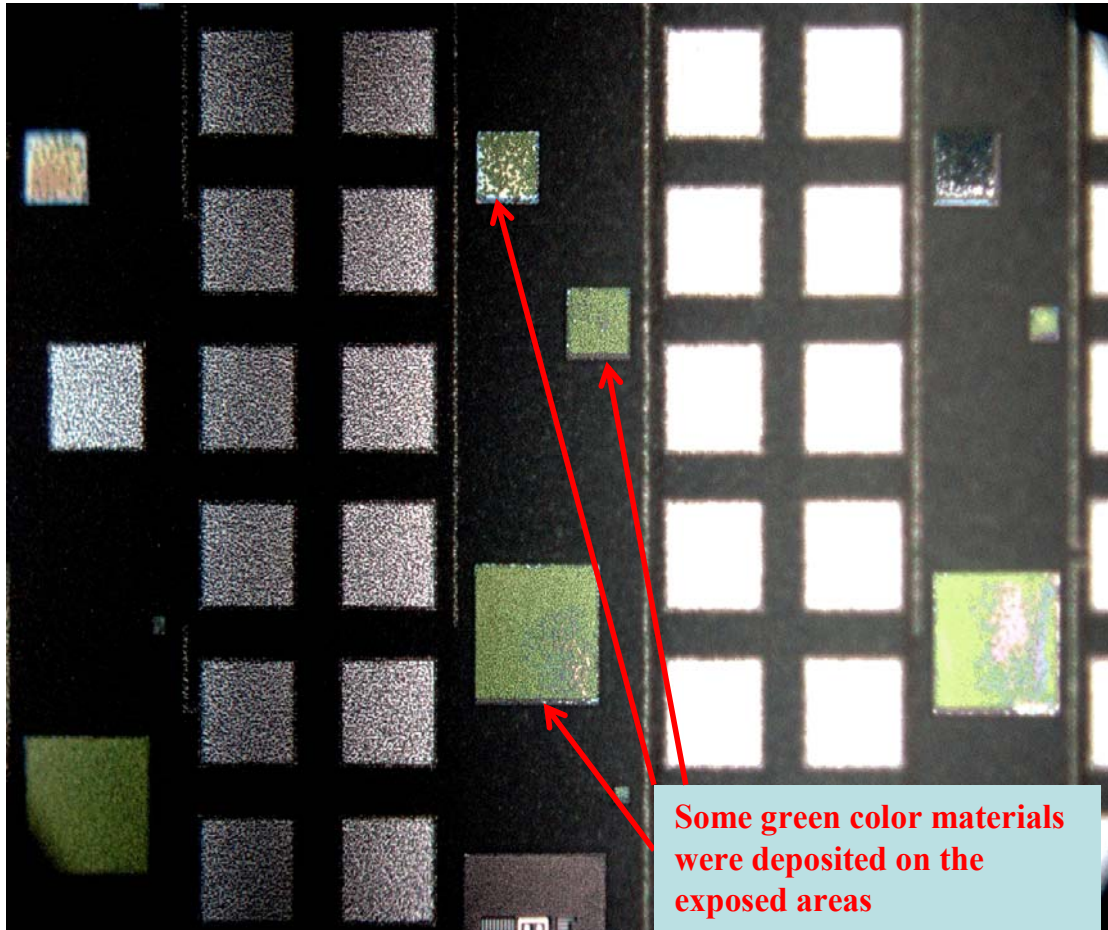
Figure 4-18: *The green color materials were deposited on the exposed chip areas and blocked the further etching.*

In the second batch of recipes, the applied gas ratio of CHF_3 of O_2 was decreased

to approximately 0.69.[24, 25]   The RIE power was reduced to 75 W to decrease the etch

rate of Al.   However, the etch rate of ILD was also decreased.   To maintain a reasonable

etch rate, a high ICP power and a low pressure were applied, which increased the plasma

density and thus the etch rate.   Four recipes with the different ICP power, pressure or the

reactive gas ratio were tested on the designed chips.   The parameters of each recipe and

the obtained etch rates are summarized in Table 4-8.

Table 4-8:   *Four different RIE recipes for ILD*

	Recipe1	Recipe2	Recipe3	Recipe4
RIE Power (W)	75	75	75	75
ICP Power (W)	400	400	300	300
Pressure (mTorr)	50	50	50	50
CHF_3 (sccm)	22	18	22	22
O_2 (sccm)	32	32	32	22
Etch Rate (nm/min)	~90	~50	~78	~80

There are two advantages to using these recipes.   First, the generation of the

green material was eliminated.   Second, very little Al mask was etched during the process.

The thickness of the Al mask was decreased from ~700 nm to 300~400 nm.

These recipes also have some disadvantages.   After a long etching, the

carbon-fluorine based polymer residue shown in Figure 4-19 was observed on the exposed

extension areas and increased the surface roughness up to ~200 nm.   This roughness was

too high to expose the floating gate extension (i.e., polysilicon) which was only ~180 nm

thick.   The problem was solved by reducing the RIE power to 50 W, especially when the

etching was close to the polysilicon layer.

Another disadvantage of these recipes was that the selectivity of SiO_2 to Si was too low. The experimental results showed that the selectivity was only ~0.27 (etch rate of ILD ≈ 80nm/min, etch rate of Si ≈ 300nm/min), which means that Si was etched 4~5 times faster than ILD making it very difficult to stop the etching at the polysilicon interface. To increase the selectivity, either H_2 should be added into these recipes or CH_2F_2 should be used instead of CHF_3. With extra H atoms in the reactive gases, more HF can be formed which only reacts with SiO_2 and therefore the selectivity can be increased.

The black polymer was still generated on the exposed surface areas
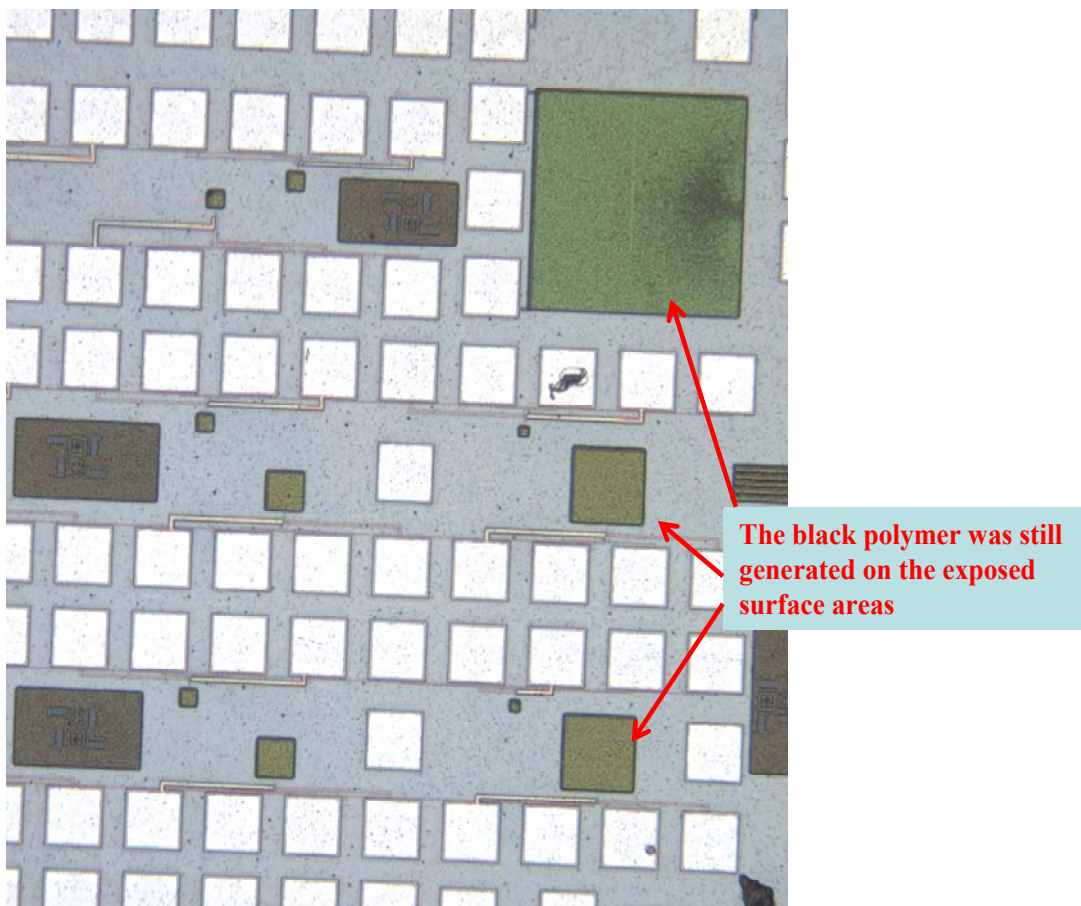
Figure 4-19: *After RIE, the black polymer was observed on the exposed areas. The floating gate extension was green color due to the thick ILD remained on top of the polysilicon.*

4.4.5 Establish the Appropriate Etch Time

Due to the issues mentioned with selectivity, it was very difficult to ascertain an appropriate etch time. When the etching approached the polysilicon interface, it was difficult to simply differentiate between the ILD and Si even under the microscope. To establish whether the etching proceeded to the silicon, an x-ray photoelectron spectroscopy (XPS) was used.

The XPS is a technique based on the photoelectric effect. Its basic principle of operation is shown in Figure 4-20. In this process, a photon with a defined energy hv strikes the sample and is absorbed by a surface atom, which is then ionized and emits a core (inner shell) electron. If the photon energy is high enough, this photoelectron can escape from the surface and its kinetic energy may be approximated using

$$KE = hv - BE - \phi_s \qquad (4.2)$$

where BE is the binding energy of the escaping electron and ϕ_s is the work function of the solid. The work function is defined as the energy required to remove an electron from the Fermi level to the vacuum level. The Fermi level is defined as the energy state where the probability of occupation of this state by an electron is one-half.[13] Since the kinetic energy of the photoelectrons depends strongly on the type of the surface atoms, the XPS technique can be used to analyze the elemental and chemical information. However, due

to the short range of the photoelectrons that can be excited from the solid, the XPS typically can only analyze the elemental information 7 nm ~ 11 nm deep into the sample.[26]
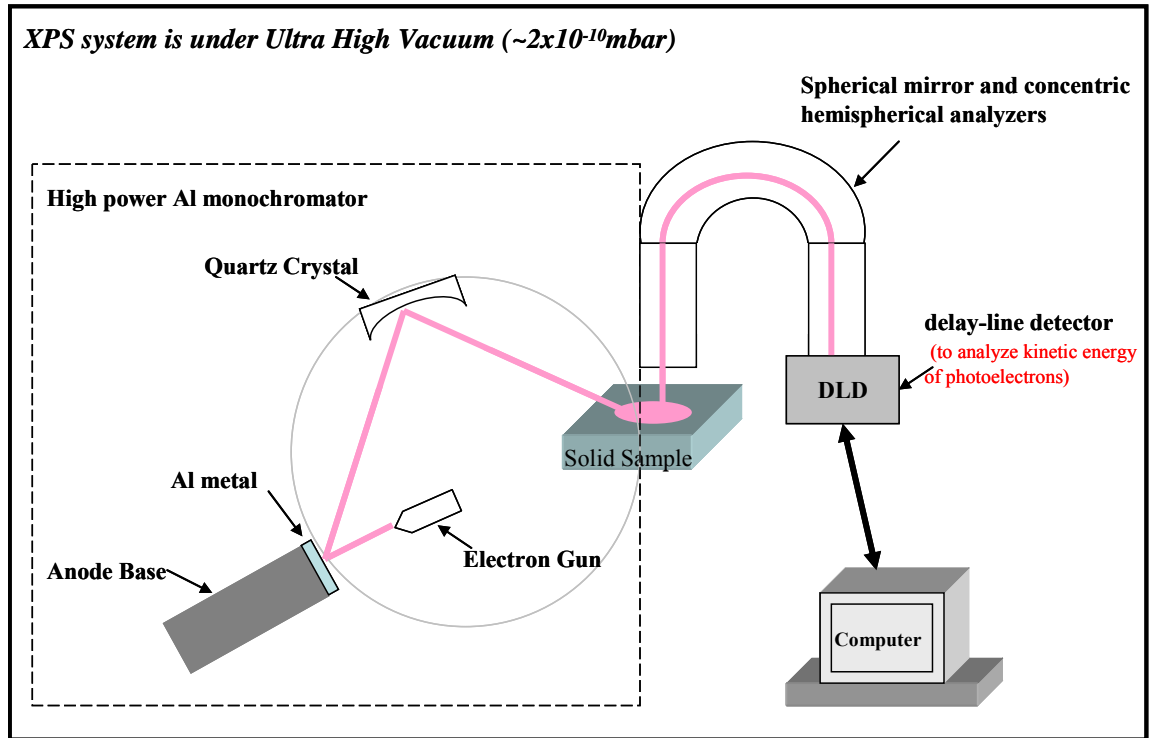
Figure 4-20: *The operation principle of an x-ray photoelectron spectroscopy (XPS).[26] The applied XPS was AXIS Ultra DLD supplied by Kratos Analytical Ltd..*

As mentioned previously, the floating gate extension was formed of polysilicon, the ILD layer deposited on top of it was formed of materials similar to silicon dioxide and the top passivation layer was mainly formed of silicon nitride. All three of these materials contain silicon. However, as listed in Table 4-9, the binding energy of silicon in each material is different as the BE depends on the bonding of the elements. Therefore, XPS can be used to differentiate between SiO_2 and Si.

Table 4-9: *Binding energy of silicon in the different materials*

Materials	Binding Energy of Silicon (eV)
Polysilicon	99
Silicon Nitride	101
Silicon Dioxide	103

In XPS the energy of escaped photoelectrons is analyzed using the spherical mirror and concentric hemispherical analyzers and a spectrum can be generated with a series of photoelectron peaks as shown in Figure 4-21. The peaks represent the binding energy of the detected element and the area under each peak can be used to determine the relative composition of each material.
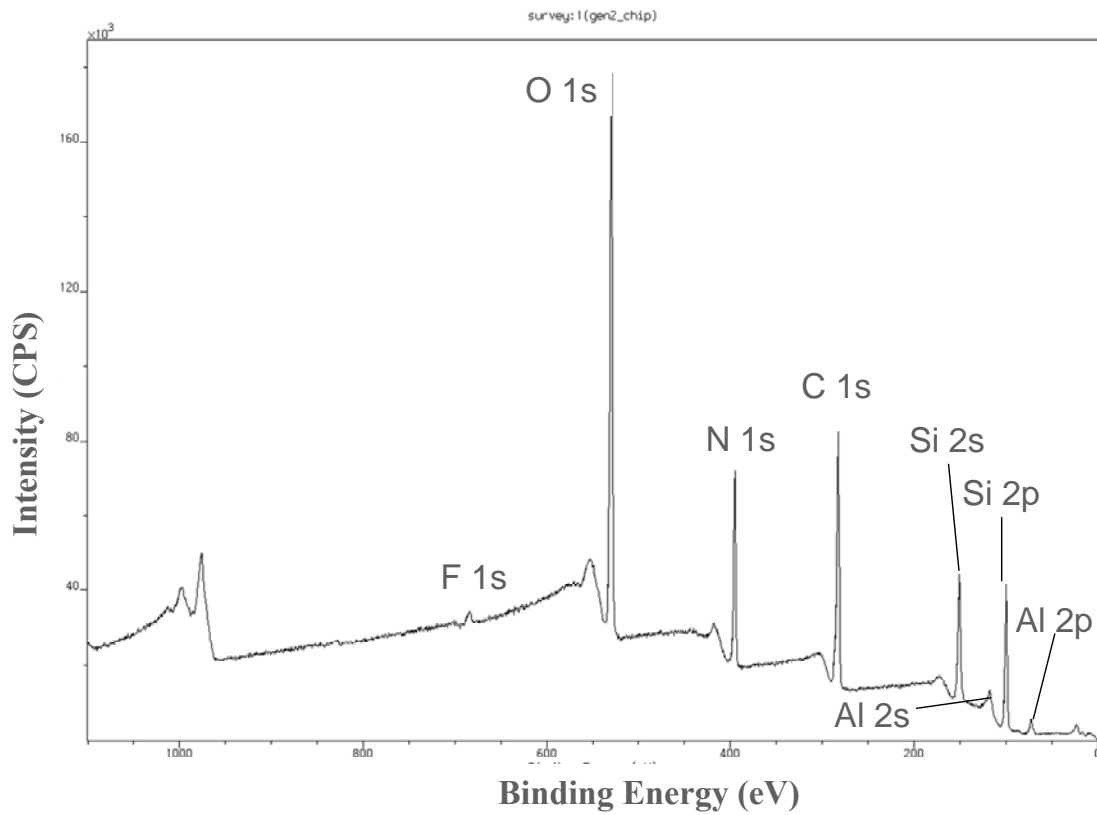
Figure 4-21: *A spectrum with a series of photoelectron peaks. The spectrum was obtained after running a survey scan [26] on the designed chip surface.*

Therefore, if a floating gate extension is analyzed using the XPS, spectra before and after the post-processing should be different. The spectrum taken before the post-processing should include a silicon peak with the binding energy of ~101eV as the extension area is covered by the silicon nitride layer. The spectrum after the post-processing should only include the silicon peak with the binding energy of 99eV indicating the exposure of the polysilicon. However, if the chip is over etched and the substrate was exposed, the same spectrum can also be obtained, such as the spectra shown in Figure 4-22 b). These results were obtained from a chip that had a 10 μm step height after the RIE. Since this value was much larger than the expected 7 μm, the chip was said to be over exposed. However, in the spectrum after the post-processing, a silicon peak with the binding energy of ~99 eV was observable.

Both the step height measurement and the XPS technique were used to ascertain an appropriate etch time. The step height can roughly estimate if the etching is close to the ILD and polysilicon interface, while the XPS data can accurately determine if the polysilicon is truly exposed.
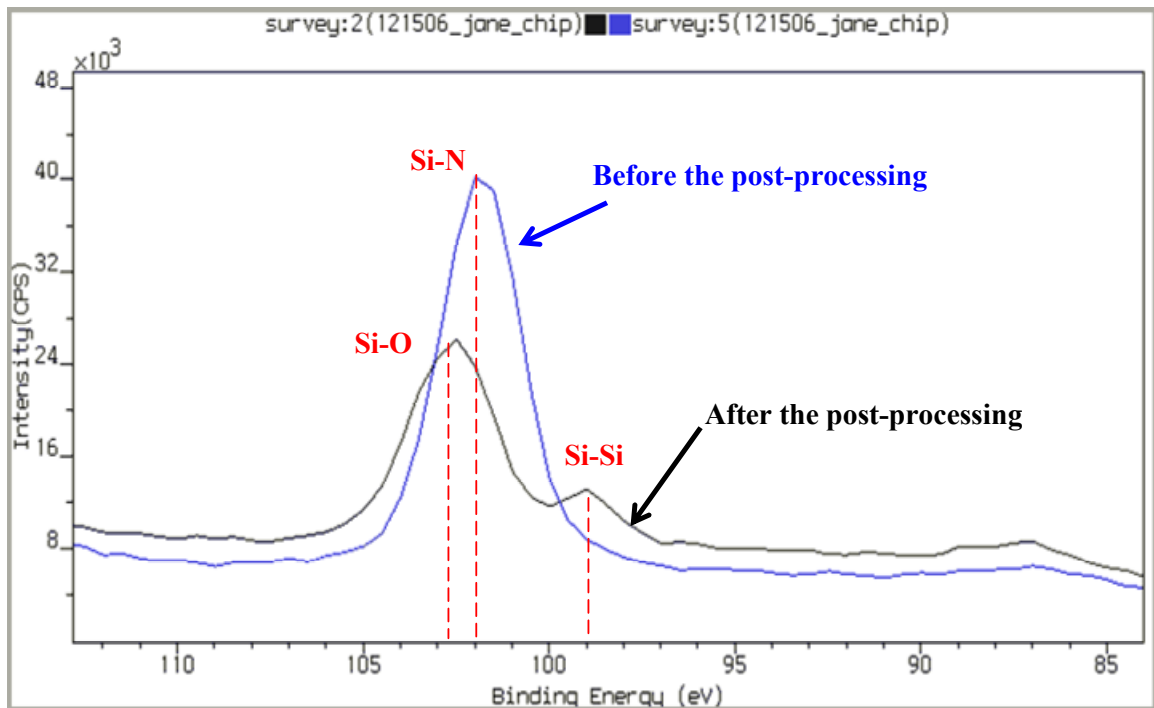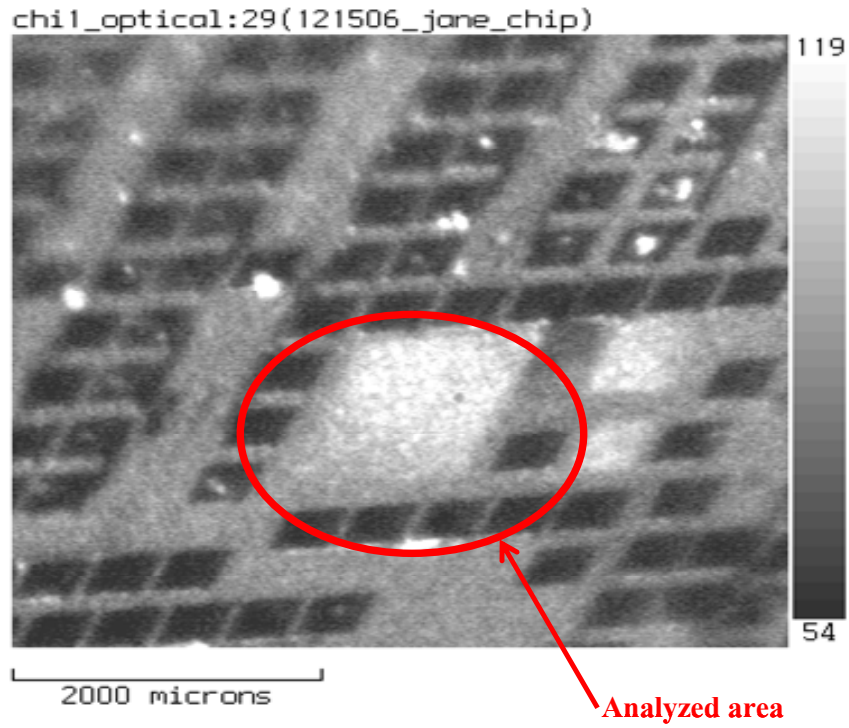
Figure 4-22: *a) The image of the area to be analyzed by XPS; b) Spectra of silicon binding energy before and after the post-processing*

Due to the difficulties met in the RIE process, no floating gate extensions were exposed in this work. To be able to test the feasibility of the designed sensors, an external "pseudo" floating gate extension deposited with the "sensing" polymer was used as the substitute, which will be discussed in Chapter 5. In collaboration with Dr. Freund's research group in the Chemistry Department of the University of Manitoba, the testing polymers were deposited electrochemically on the "pseudo" floating gate extensions. The device characterization was then completed in the Electrical and Computer Engineering Department.

Chapter 5 Device Characterization

In this chapter, the electrical characterization of the designed sensors will be discussed. The basic current-voltage (I-V) relationships for standard MOSFETs are introduced first. The effect of the "floating gate" on these standard characteristics is then introduced specifically relating to the manner in which charge on the floating gate shifts the I-V characteristics. After introducing the measurement set-up, the I-V characteristics of fabricated sensors are presented. The discussion of the sensors includes measured data before and after exposure to the chemical solution.

5.1   Theory

5.1.1   I-V Characteristics of a Standard MOSFET

A standard n-type enhancement mode [13] MOSFET is used to illustrate the device characterization and is shown schematically in Figure 5-1. A MOSFET consists of a p-type substrate and an n-type source, drain and gate. The gate is separated from the substrate by a thin gate dielectric, typically SiO_2. The channel is formed at the surface of the silicon substrate between the source and the drain.
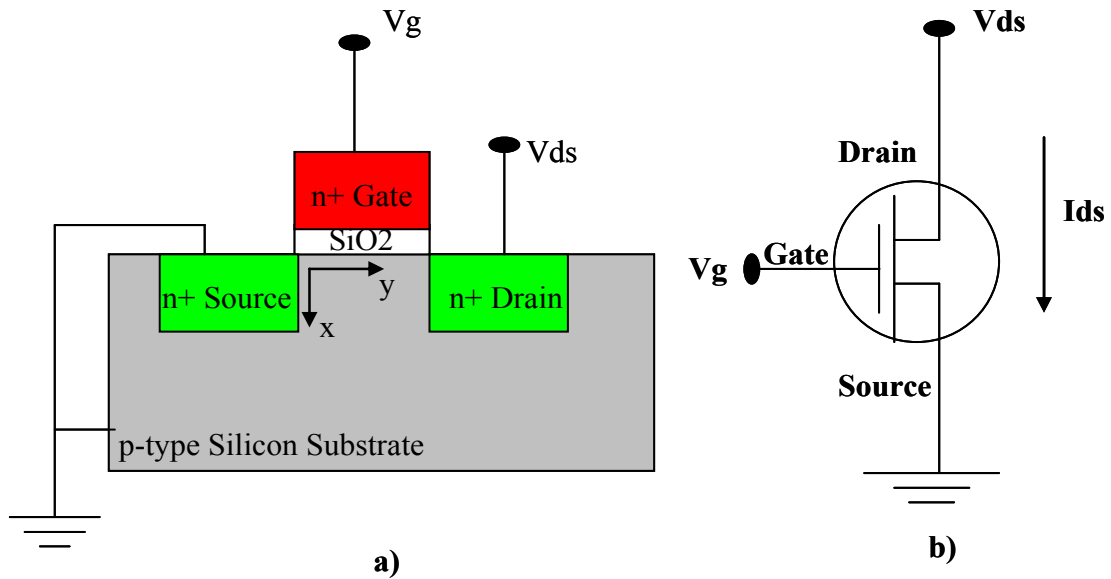
Figure 5-1: *The operation mode of an n-type MOSFET.*

Typically, the operation characteristics of a MOSFET can be divided into three regions: the subthreshold region, the linear region and the saturation region. With a zero gate bias ($V_g = 0V$), the source, silicon substrate and drain form two back to back p-n junction diodes. There is only limited conduction in this channel between the source and the drain. When a positive bias is applied to the gate (V_g), electrons in the substrate are driven to the silicon surface. However, if the gate voltage is smaller than the threshold voltage ($V_g < V_{th}$) of the device, the electron density at the surface is not high enough to form a conduction channel and the MOSFET is said to be in the "subthreshold" region. In this region, the drain/source current increases exponentially with the applied gate voltage. From a plot of the I_{ds}-V_g on the logarithmic scale (see Figure 5-2), the inverse slope is

approximately 70-100 mV/decade, which is typical of the standard MOSFETs. Therefore,

a 0.5 V shift in the gate voltage would result in a current change of approximately five

decades, which demonstrates that MOSFETs I-V characteristics in the subthreshold region

can be extremely sensitive to the small changes in the gate potential.
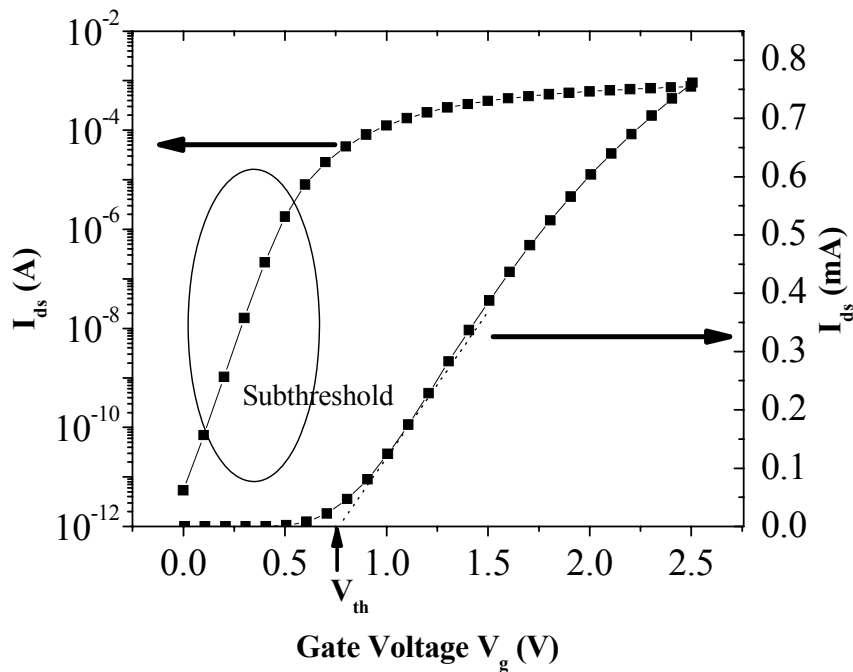
Figure 5-2: *The I_{ds}-V_g characteristic of an n-type MOSFET (W=5μm and L=0.8μm) with a small drain voltage (V_{ds}=0.5V). The drain/source current is plotted on both LINEAR and LOGARITHMIC scales. The threshold voltage V_{th} is the intersection of the voltage scale and the tangential line along the linear I-V curve.*

The device operates in the subthreshold region until the gate voltage is larger

than the threshold voltage (V_{th}). Depending on the applied voltage across the drain and

source, the MOSFET can either operate in the "linear" region or in the "saturation" region.

In the linear region, the drain voltage (V_{ds}) is smaller than the potential difference between the gate voltage and the threshold voltage (i.e., $V_{ds} < V_g - V_{th}$). The MOSFET acts like a resistor and the drain/source current changes linearly with the applied drain voltage as shown in Figure 5-3. In the saturation region, the drain voltage is larger than the potential difference between the gate voltage and the threshold voltage (i.e., $V_{ds} \geq V_g - V_{th}$). The drain/source current increases following a parabolic curve until a maximum value is reached (see Figure 5-3).
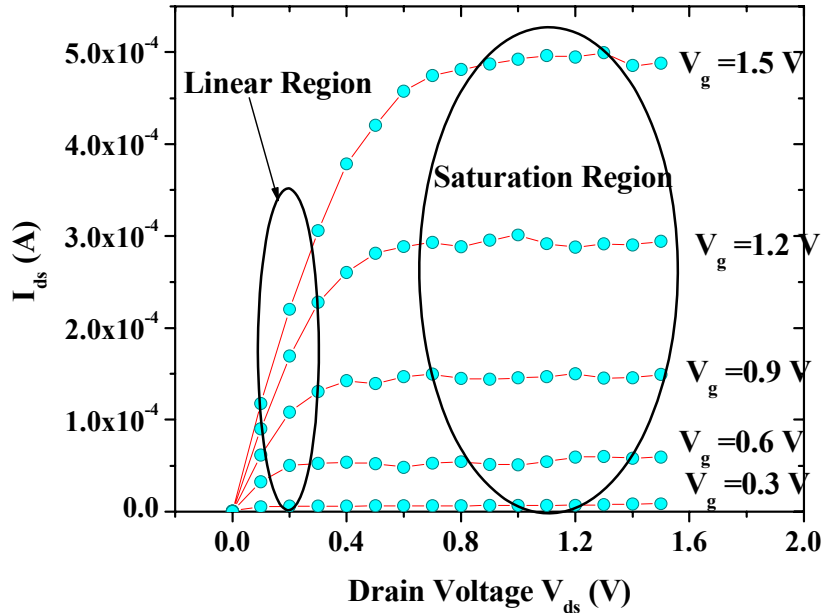
Figure 5-3: *The I_{ds}-V_{ds} characteristic of an n-type MOSFET with a variable gate voltage. In the saturation region, the drain/source current is saturated and reaches a maximum value.*

The threshold voltage is an important point on the current-voltage plot. It can

be expressed as

$$V_{th} = V_{fb} + 2\varphi_B + \frac{\sqrt{4\varepsilon_{si}qN_a\varphi_B}}{C_{ox}}$$ (5.1)

where V_{fb} is the flat-band voltage, φ_B is the difference between silicon Fermi level and

intrinsic level, ε_{Si} is the permittivity of silicon, and N_a is the acceptor impurity density in

the substrate.[13]   From this equation, the threshold voltage of the MOSFET is

determined by the work function of the polysilicon and silicon, material properties and the

interfacial characteristics of the gate dielectric. However, it can also be affected by the

substrate bias and the temperature.   The details of the substrate effect will be discussed in

section 5.4.1.3.   Since all of devices were tested at the room temperature.   The

temperature effect was neglected during the measurements.

5.1.2 I-V Characteristics of Floating-Gate Field-Effect Transistors

As mentioned in the previous chapters, the chemical sensors were designed

based on the floating gate field-effect transistor structure. It is not a standard MOSFET,

but a FET with two gates: the floating gate and the control gate. The application of the

unique floating gate enables the device to operate with a high electric field where electron

tunneling from the substrate is possible. However, during the normal operation, the

current-voltage characteristics of this type of device should still be similar to that of the standard MOSFET as shown in Figure 5-2 and 5-3.

The schematic diagram of the gate stack of a floating gate field-effect transistor is shown in Figure 5-4. By neglecting the parasitic capacitors from the floating gate to the source, drain and the substrate, the floating-gate field-effect transistor has a capacitance equivalent circuit (see Figure 5-4) consisting of two capacitors: the capacitor between the two gates, and gate capacitor between the floating gate and the silicon substrate. [27, 28, 29, 30, 31]
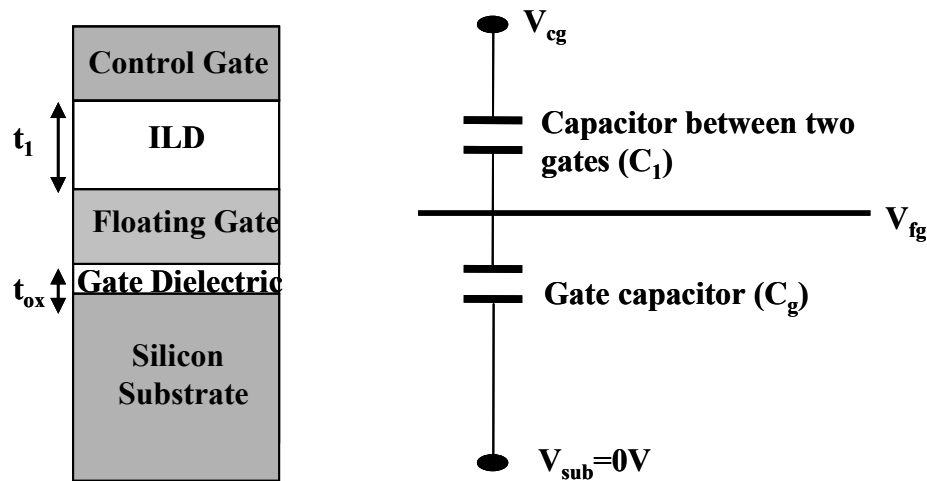
Figure 5-4: *Schematic Diagram of the gate stack in a floating-gate field-effect transistor and the relative capacitor equivalent circuit.*

If the floating gate is left floating and the transistor is operated using the control gate, the net charge on the floating gate (Q_{FG}) is the sum of the charge in each capacitor and

is given by

$$Q_{FG} = C_1(V_{fg} - V_{cg}) + C_g(V_{fg} - V_{sub}) \tag{5.2}$$

where V_{fg} is the floating gate potential, V_{cg} is the voltage applied to the control gate, V_{sub} is the substrate bias, C_1 is the capacitance between two gates and C_g is the gate capacitance. Since V_{sub} was usually zero, equation 5.2 can be expressed as

$$V_{cg} = \frac{C_1 + C_g}{C_1} V_{fg} - \frac{Q_{FG}}{C_1} \tag{5.3}$$

The threshold voltage of the floating gate field-effect transistor (V_{th}^{FG}) can thus be given by [32]

$$V_{th}^{FG} = \frac{C_g + C_1}{C_1} V_{th}^{SG} - \frac{Q_{FG}}{C_1} \tag{5.4}$$

where V_{th}^{SG} is the threshold voltage of the single-gate field-effect transistor. From this equation, the net charge stored on the floating gate is the main factor that can affect the threshold voltage of the transistor V_{th}^{FG} because the C_1, C_g, and V_{th}^{SG} are constant and are parameters relating to the device design and the particular CMOS process used. Therefore, the threshold voltage shift (ΔV_{th}^{FG}) as a function of the charge change on the floating gate (ΔQ_{FG}) can be expressed as [31]

$$\Delta V_{th}^{FG} = \frac{\Delta Q_{FG}}{C_1} \tag{5.5}$$

5.1.3 I-V Characteristics of Sensors

The sensor was composed of the floating-gate field-effect transistor and a floating gate extension. Due to this extra extension area connected to the floating gate, sensors included more parasitic capacitors than floating gate field-effect transistors. Aside from C_g and C_1, the capacitance between the floating gate extension and the substrate (C_2) also existed in the capacitance equivalent circuit shown in Figure 5-5. The effect of C_2 was discussed using the first iteration of sensors.
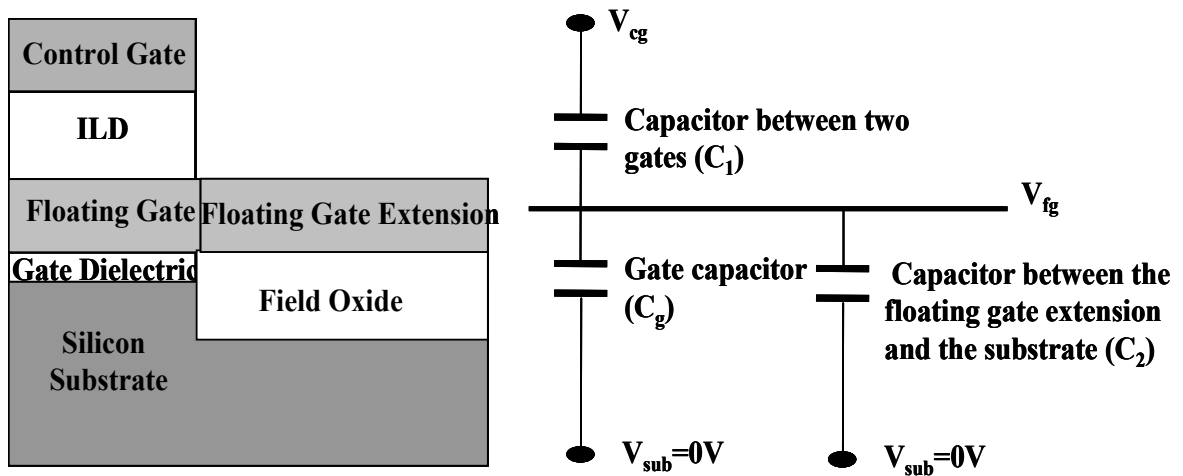
Figure 5-5:   *Capacitance equivalent circuits of the sensor.*

From the design rules, the dielectric thickness from the floating gate extensions to the field regions in the substrate was found to be approximately 270 nm with a capacitance per unit area of approximately 4.8×10^{-8} F/cm^2.[14]   The gate dielectric thickness was only 7.5 nm yielding gate capacitance per unit area approximately 4.6×10^{-7}

F/cm^2.[14]   Since the floating gate extensions were much larger than the gate areas in the

field-effect transistor, the capacitance C_2 became comparable or even larger than the gate

capacitance C_g.   It could not be neglected in the capacitance equivalent circuit.   As a

result, the net charge stored on the floating gate of the sensor should be expressed as

$$Q_{FG} = C_1(V_{fg} - V_{cg}) + C_g(V_{fg} - V_{sub}) + C_2(V_{fg} - V_{sub}) \qquad (5.6)$$

When V_{sub} is zero, the threshold voltage of the sensor is given by

$$V_{th}{}^{FG} = \frac{C_g + C_1 + C_2}{C_1} V_{th}{}^{SG} - \frac{Q_{FG}}{C_1} \qquad (5.7)$$

Comparing with equation 5.4, the sensor would require a larger threshold voltage than a

floating gate field-effect transistor with the same gate dimension.   However, the threshold

voltage shift ($\Delta V_{th}{}^{FG}$) of the sensor could still be expressed as a function of the charge

change on the floating gate (ΔQ_{FG}) and equation 5.5 could still be used in sensors.

Using equations 5.5 and the schematic diagram shown in Figure 5-6, the operation

mechanism of sensors can be demonstrated.   In the sensor, an ion-sensitive polymer was

deposited on the floating gate extension of the sensor.   When the sensor was exposed to

the particular chemical environment, the polymer should react with the chemical analyte

and change the charge density (Q_{FG}) on the floating gate.   According to equations 5.5, it

would change the threshold voltage of the sensor.   When the threshold voltage was

changed, the current-voltage characteristics of the device would be shifted as an example shown in the Figure 5-6. Therefore, by measuring the I_{ds}-V_{cg} characteristics before and after the exposure, ΔV_{th}^{FG} could be obtained on the plot and the charge generated during the chemical reaction could then be calculated using the equation.
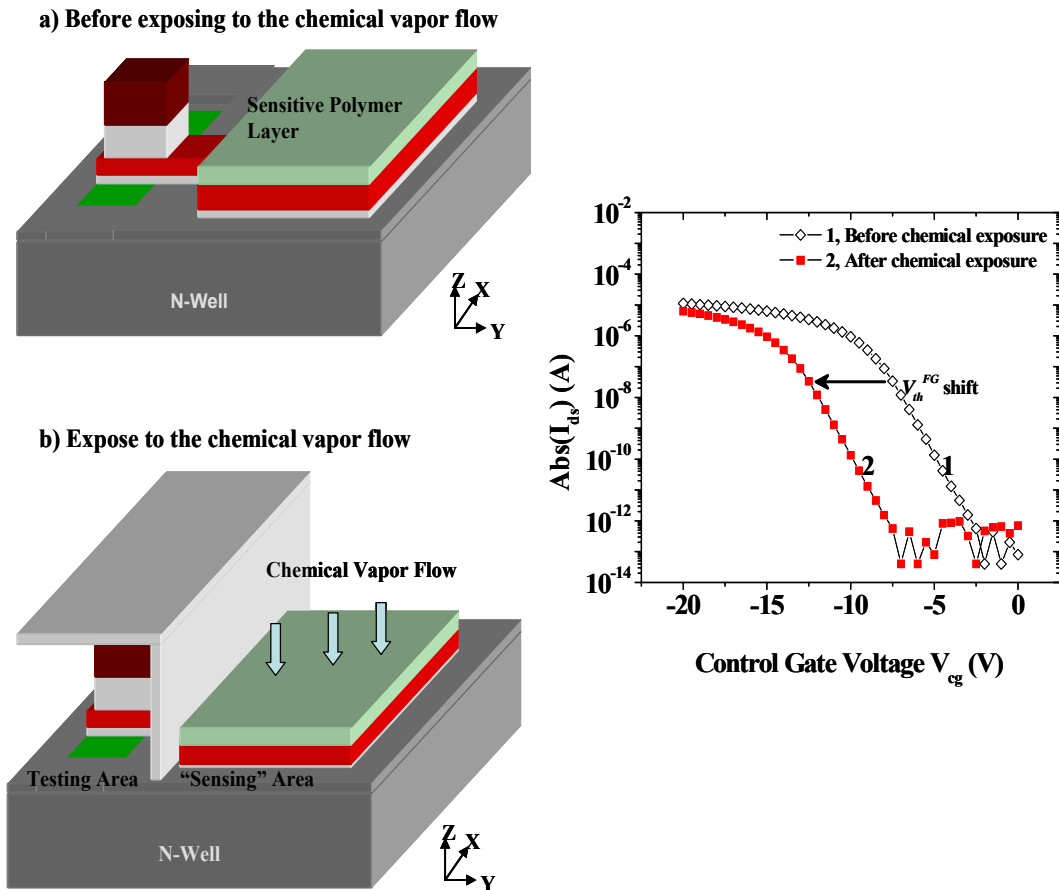
Figure 5-6: *The expected I-V shift of the p-type sensors before and after exposure to the chemical vapor flow.*

Three I-V characteristics could be obtained for each sensor: 1) the I-V characteristic of the sensor without the "sensing" polymer; 2) the I-V characteristic of the

sensor with the "sensing" polymer but before exposure to the chemical vapor; 3) the I-V

characteristic of the sensor with the "sensing" polymer and after exposure to the chemical

vapor.   These three I-V characteristics should look similar, albeit perhaps shifted, as the

shape of these curves should not be changed by the electrochemical deposition process nor

the chemical exposure process.   Since the I-V characteristics of the devices without the

"sensing" polymers could be easily measured, this type of I-V characteristic was used to

test the sensors.

5.2 $I_{ds} - V_g$ Measurement Set-up

The apparatus used for the I-V measurement is shown in Figure 5-7.   The

system consists of a probe station, a switch matrix and the test equipment.   The test chip

was placed on the Alessi REL 6100 from Cascade Microtech.   This probe station has four

probes to individually probe the source, drain, gate and substrate of the device under test

(DUT).   The station and the device are put inside a shielded box to reduce electrical noise

and the I-V test is performed in the dark to reduce optical noise.   The output of the probe

station is connected to a switch matrix (Keithley 7001) which enables the use of various

test equipment for the different types of measurements.   For example, Agilent 4156C

Precision Semiconductor Parameter Analyzer was used for the I-V measurement and

Agilent 4284A Precision LCR Meter was used for the capacitance-voltage (C-V) measurement. The probe station, switch matrix and the test equipment are all controlled by the computer via GPIB (IEEE 488) bus. [33]
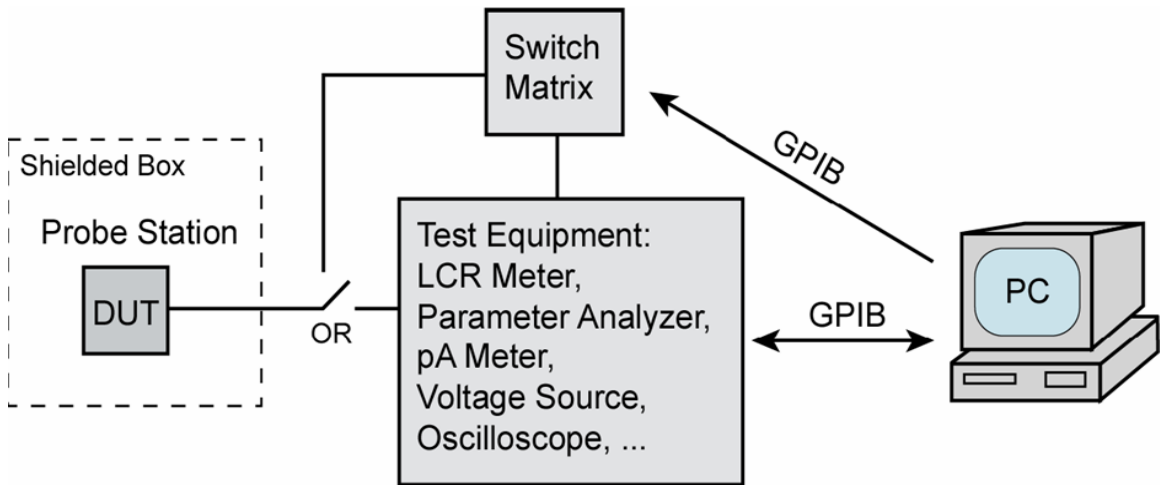
Figure 5-7:   *Measurement set-up for the device characterization. [33].*

5.3   Voltage Limits for the I-V Measurement

Before measuring the sensors' operating characteristics, the voltage limits of the FETs have to be ascertained first. To make field-effect transistors work in the normal operation region, the electric field across the gate dielectric should not be larger than 5 MV/cm as this is when tunneling becomes significant. This phenomenon thus limits the voltage that can be applied to the gates.

In the 0.35 μm CMOS process, the gate dielectric thickness is approximately 7.5 nm. For a maximum electric field of 5 MV/cm, the applied floating gate voltage should be

less than 3.75 V assuming that there was no initial net charge on the floating gate. The control gate voltage required to produce the same electric field can be deduced using the capacitance coupling factor (α) in equation 5.8. The coupling factor is the ratio of the total capacitances above the floating gate to the total capacitances below the floating gate. By neglecting the C_2 effect on the field-effect transistor, the capacitance equivalent circuit shown in Figure 5-4 is used. Therefore, α is expressed as

$$\alpha = \frac{C_1}{C_g} = \frac{\varepsilon_1 t_{ox} A}{\varepsilon_{ox} t_1 A} \tag{5.8}$$

where ε_1 is the permittivity of the inter layer dielectric (ILD) between two gates, ε_{ox} is the permittivity of the gate dielectric, t_1 is the thickness of the ILD later between the two gates, t_{ox} is the gate dielectric thickness and A is the gate area. For the field-effect transistors in sensors, both the $\varepsilon_1 / \varepsilon_{ox}$ ratio and the capacitance coupling factor were unknown. However, this ratio could be derived from the published data of a device fabricated using the exact same CMOS process.[34] In the literature, a value of $\alpha \sim 0.45$ was found for $t_{ox} \sim 7.5$ nm and $t_1 \sim 14$ nm.[34] Using equation 5.8, the dielectric constant ratio of the published device was calculated to be $\varepsilon_1 / \varepsilon_{ox} \sim 0.84$. The sensors in the current work had the same $\varepsilon_1 / \varepsilon_{ox}$ ratio and t_{ox} as the published data, but a different ILD thickness; $t_1 \sim 37$ nm. As a result, the capacitance coupling factor of the current sensors was calculated to be $\alpha \sim 0.17$. The values for the published data and current sensor data are summarized in Table 5-1.

Table 5-1: *Data used to calculate the capacitance coupling factor of the sensors.*

	t_{ox} (nm)	t_1 (nm)	$\varepsilon_1 / \varepsilon_{ox}$	α
Device in paper [34]	7.5	~14	0.84	0.45
Sensors in this project	7.5	~37	0.84	0.17

The control gate voltage (V_{cg}) can be expressed as a function of the floating gate voltage (V_{fg}) and the capacitance coupling factor, and is given by

$$\frac{V_{cg}}{V_{fg}} = \frac{C_{ox} + C_1}{C_1} = \frac{1}{\alpha} + 1 \tag{5.9}$$

From this equation, a maximum 25.81 volts can be applied to the control gate in order to stay below a 5 MV/cm electric field across the gate dielectric.

5.4   Typical $I_{ds} - V_g$ Characteristics of Sensors

The current-voltage (I-V) characteristics of sensors and reference transistors were measured using Agilent 4155C/4156C parameter analyzer. The characterization results are presented and analyzed in the following sections. All of these presented I-V characteristics were obtained from the sensors prior to the deposition of the "sensing" polymer.

5.4.1 I-V Characteristics of Devices on the First Chip

On the first chip, the reference transistors and sensors were characterized. It

was found that these sensors could not be directly turned on. Three different methods were applied to drive the devices into the operational mode. These methods will be introduced and the obtained I-V characteristics will be discussed below.

5.4.1.1 $I_{ds} - V_g$ Characteristics of Single-Gate Reference Transistors

When measuring the single-gate reference transistors, a voltage sweep was applied to the gate (e.g. $0 \sim 2.5$ V), a constant voltage (e.g. 0.5 V) was applied to the drain, the source and the silicon substrate (or n-well for a p-type device) were grounded. The I_{ds}–V_g characteristics of a single-gate reference transistor are shown in Figure 5-8 for both n-type, 5-8 a) and p-type, 5-8 b) transistors. Each graph consists of three I-V curves measured at the different drain voltages.

From these figures, the I-V characteristics seem to be very stable to the change of the drain voltage. However, it can be seen that the three I-V curves overlap in the subthreshold region but slightly split in the linear region. The reason for the overlapping is because the drain/source current in the subthreshold region is independent of the drain voltage once V_{ds} is larger than a few kT/q. In the linear region, the drain/source current increases with the applied drain voltage and thus the separate I-V curves were measured.
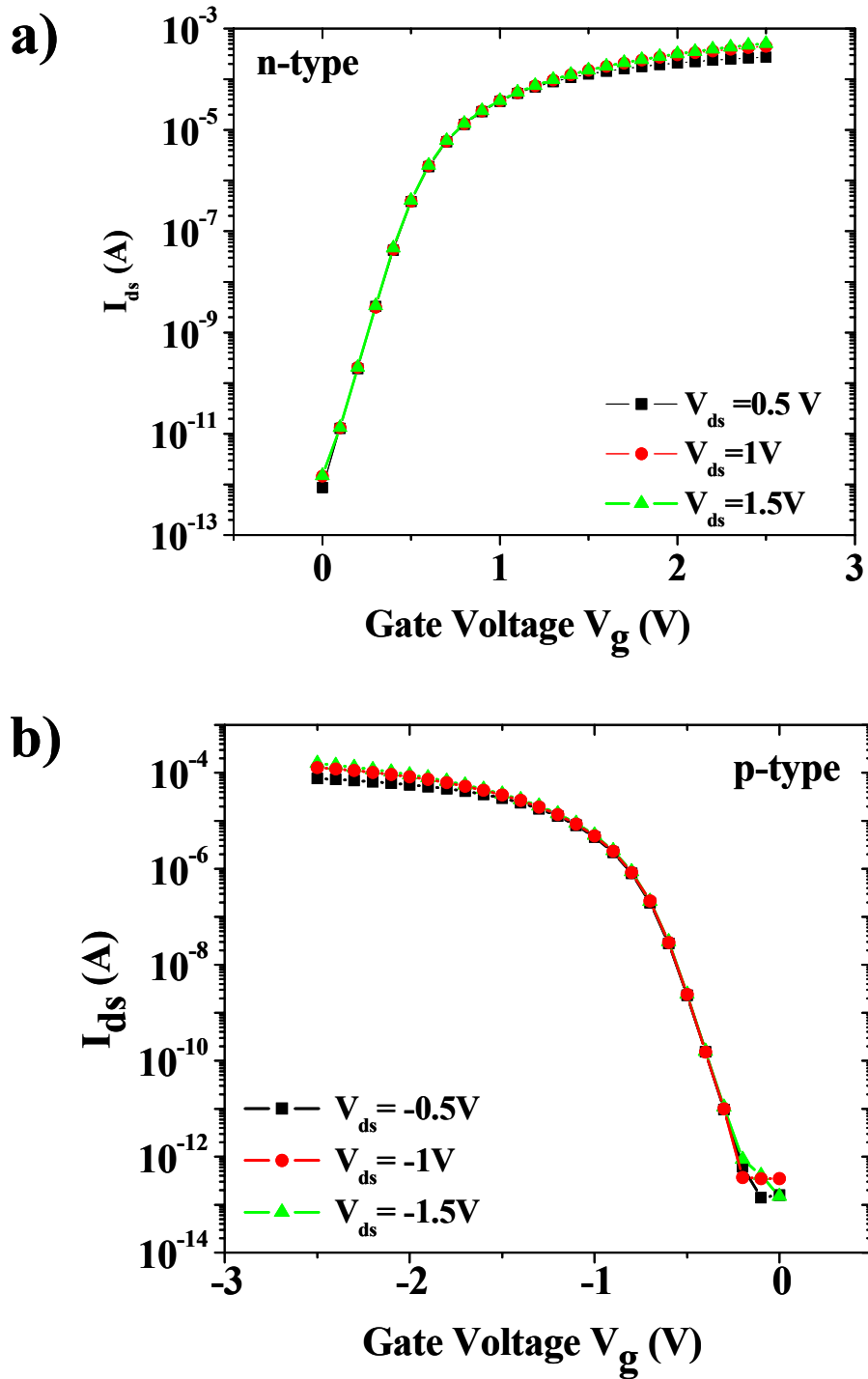
Figure 5-8: *Typical I_{ds}-V_g characteristics of single-gate reference transistors with a gate width to length ratio of W/L=3. Both n-type a) and p-type b) devices are shown.*

The threshold voltage of single-gate reference transistors can be estimated from the I-V plot in the linear scale. For the n-type transistor, the threshold voltage was found to be ~0.7 V. For the p-type transistor, the threshold voltage was ~ -0.6 V. In equation 5-1, the threshold voltage was shown to be independent of the gate width to length (W/L) ratio. Therefore, the same V_{th} should also be applicable to all sensors independent of their dimensions.

5.4.1.2 I – V Characteristics of Floating-Gate Reference Transistors

The floating-gate reference transistor is a five terminal device: source, drain, floating gate, control gate and substrate. Although two gates were available, only one (either the floating gate or the control gate) was used during the device characterization, while the other gate was left floating. Two types of I-V characteristics were obtained: the I_{ds}-V_{fg} characteristic when the gate bias was applied to the floating gate and the I_{ds}-V_{cg} characteristic when the gate bias was applied to the control gate.

The current-voltage characteristics of an n-type floating-gate reference transistor are shown in Figure 5-9. The device was measured under the conventional test conditions, where the source and the substrate were grounded, a voltage sweep was applied to the gate and a constant bias was applied to the drain. From the figure, the I_{ds}-V_{fg} characteristic was found to be similar to that of a single-gate reference transistor. However, the I_{ds}-V_{cg}
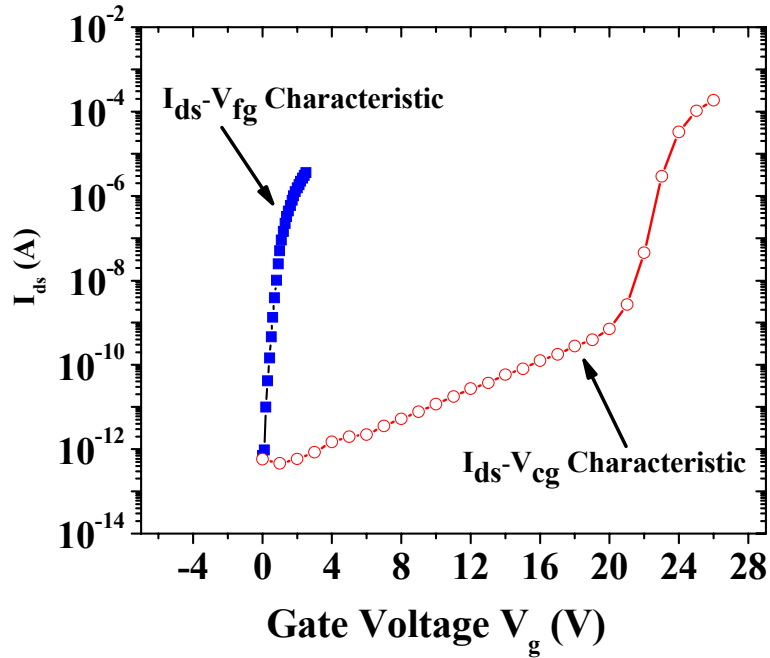
Figure 5-9: *I-V Characteristics of an **n-type** floating-gate reference transistor with a W/L of 3, including the I_{ds}-V_{fg} and I_{ds}-V_{cg} characteristics. $V_s=V_{sub}=0$; $V_{ds}=0.5V$.*

characteristic was found to be significantly different.   The drain/source current (I_{ds}) was

greatly increased after the control gate voltage was extended beyond 22 V.   Similar results

was observed for the I_{ds}-V_{cg} characteristic of a p-type floating-gate reference transistor..

5.4.1.3   I – V Characteristics of Sensors

The sensors in this work have similar I-V characteristics as the floating-gate

reference transistors discussed previously.   The current-voltage characteristics of a typical

sensor are shown in Figure 5-10, including both I_{ds}-V_{fg} and I_{ds}-V_{cg} characteristics.   As

shown previously, the drain/source current of the device slowly increased within the

applied control gate voltage sweep (0~22V), suggesting that the device was not turned on.
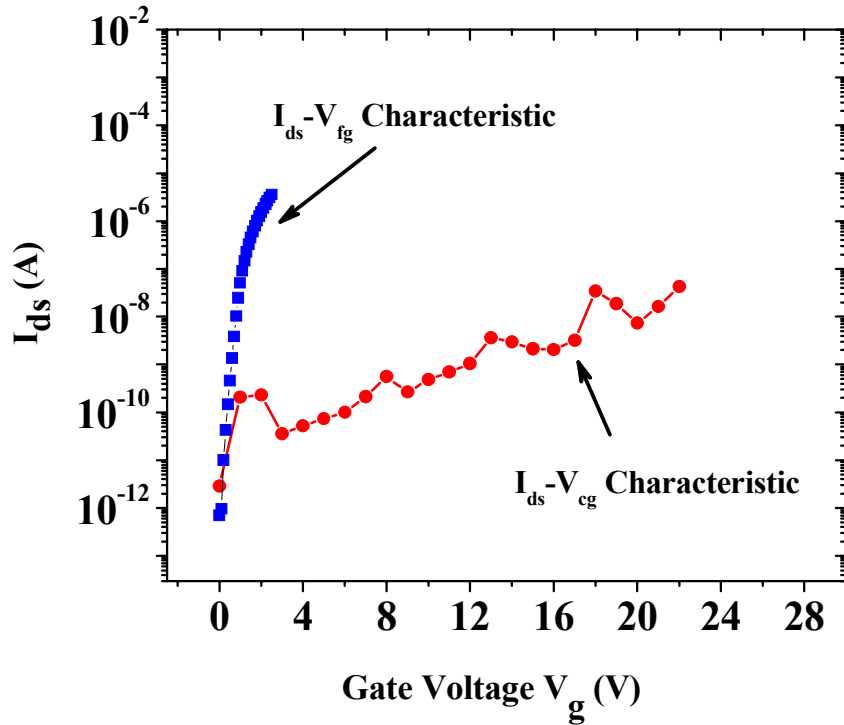
Figure 5-10: *Two I-V characteristics of an n-type sensor with a W/L of 3 and a 10um x 10um extension area. During the characterization, $V_s = V_{sub} = 0$; $V_{ds} = 0.5V$.*

Three methods were attempted to produce a working device. In the first method,

Fowler-Nordheim (F-N) tunneling was used during which a high electric field was applied

across the gate dielectric. Some charge from the channel tunneled through the thin gate

dielectric and was stored on the floating gate. The net charge increase on the floating gate

allowed the device to be easily turned on. Based on these hypotheses, an n-type sensor

was measured five times following the sequence listed in Table 5-2.   The obtained I_{ds}-V_{cg}

characteristics are shown in Figure 5-11.

Table 5-2:   *The measurement sequence and test conditions of an n-type sensor*

Sequence	V_{cg} Sweep (V)	V_s (V)	V_{sub} (V)	V_d (V)	Remarks
1	0 ~22	0	0	0.5	Curve 1: Operate with no tunneling
2	0~23	0	0	0.5	Curve 2: Operate with little tunneling
3	0~26	0	0	0.5	Curve 3: The first time to operate in the relatively high electric field region with more charge tunneling
4	0~26	0	0	0.5	Curve 4: The second time to operate in the relatively high electric field region with more charge tunneling
5	-5~15	0	0	0.5	Curve 5: Operate in the small electric field with no tunneling
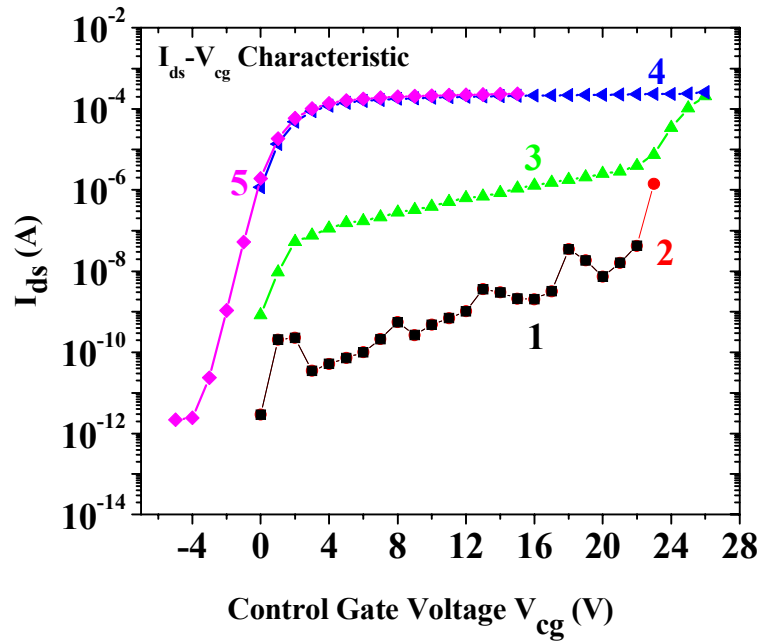
Figure 5-11: *The I_{ds}-V_{cg} characteristics of an n-type sensor with a W/L of 3 and a 10x 10um extension area. The sequence of measurements is listed in Table 5-2.*

During the first I-V measurement, a relatively small electric field was applied to the device. The drain/source current (I_{ds}) of the device was increased slowly, but no obvious subthreshold region could be observed. In the second I-V measurement, the control gate voltage was increased to 23 volts and the charge tunneling occurred. In the third I-V measurement, the gate voltage sweep was continued in order to generate a relatively high electric field across the gate dielectric. As a result of the charge tunneling, I_{ds} was increased substantially from ~10^{-9} A to ~10^{-4} A. Since the charge could be stored on the floating gate, the device was turned on at a low gate bias during the fourth

measurement. The V_{th} change resulted from the charge stored on the floating gate. The device was operated again without the charge tunneling. This fifth and final I-V characteristic could then be used for chemical sensing.

In these experiments, it was found that the charge could only be stored on the floating gate for a short period of time. Fowler-Nordheim tunneling was used frequently to turn on the device. However, the F-N tunneling is a process that can also generate the defects in the gate dielectric and degrade the quality of the insulator, finally leading to the gate dielectric breakdown.[13] As such, the sensors could have been permanently destroyed after a few I-V measurements.

This measurement technique was therefore improved and the sensor was operated in two modes: the programming mode and the normal operation mode. The parameter settings of each mode are listed in Table 5-3. In the programming mode, a high voltage sweep was applied to the control gate. The same bias was applied to the source and the drain to diminish any lateral electric field. Since the largest potential difference was between the gate and the substrate, the charge tunneled from the substrate bulk to the floating gate. The net charge generated on the floating gate reduced V_{th} and the device was able to be turned on at a reasonable gate bias.

Table 5-3:   *Voltages applied to the terminals in the second method*

Mode	V_{cg} Sweep (V)	V_s (V)	V_d (V)	V_{sub} (V)
Programming	15~23	-2	-2	-4
Normal Operation	-5~8	0	0.5	0

In Figure 5-12, the I_{ds}-V_{cg} characteristic was obtained using the aforementioned

programming technique.   Two I-V curves were measured under the conditions given in

Table 5-3 where curve 1 and curve 2 were the measurement results before and after the

sensor was programmed.
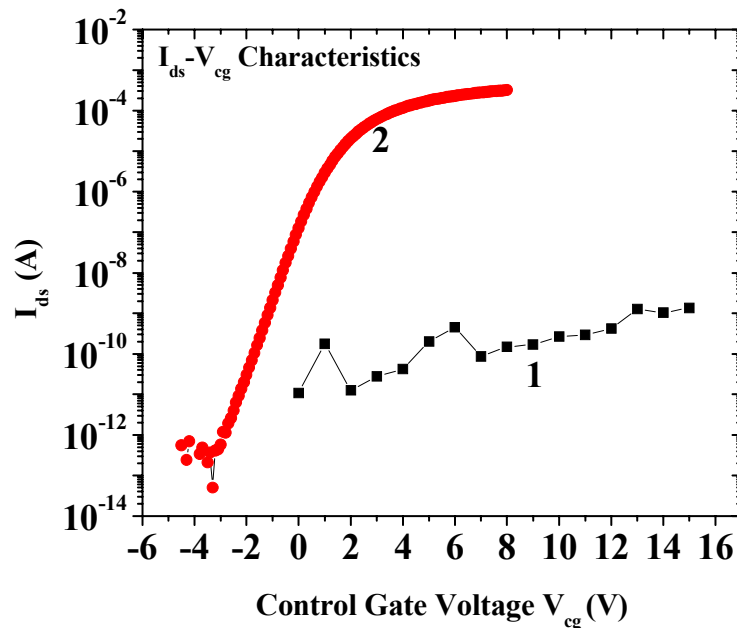

Figure 5-12:   *The I_{ds}-V_{cg} characteristics of an n-type sensor with a W/L of 3 and a 10x 10um extension area.   1)-Measured before the sensor was programmed; 2)-The device was turned on after running in the programming mode.*

However, since tunneling under high fields was still used in the second method, defects could still be generated in the gate dielectric and damage could result. As such, a third method was developed which included the use of a small substrate bias during the device measurement.

As mentioned previously, the threshold voltage can be changed with the application of a substrate bias (V_{sub}). This relationship can be expressed as [13]

$$V_{th} = V_{fb} + 2\varphi_B + \frac{\sqrt{2\varepsilon_{si}qN_a(2\varphi_B - V_{sub})}}{C_{ox}} \tag{5.10}$$

For an nFET, if a positive substrate bias is applied, the threshold voltage is decreased as the depletion region in the substrate bulk is narrowed and the maximum depletion-layer capacitance (C_{dm}) is increased. The decrease of the threshold voltage enables the device to be more easily turned on.

An n-type sensor was measured with the different substrate biases. From the characterization results shown in Figure 5-13, the sensor was found to be turned on with a relatively small positive substrate bias. However, the drain/source current was found to vary only within a small range with an I_{max}/I_{min} ratio of ~10^4. When the substrate bias was increased slightly, the drain/source leakage current in the "OFF" state was found to be greatly increased. This suggested that these particular devices although usable, would not

make the best sensors due to the smaller current change in the subthreshold region.
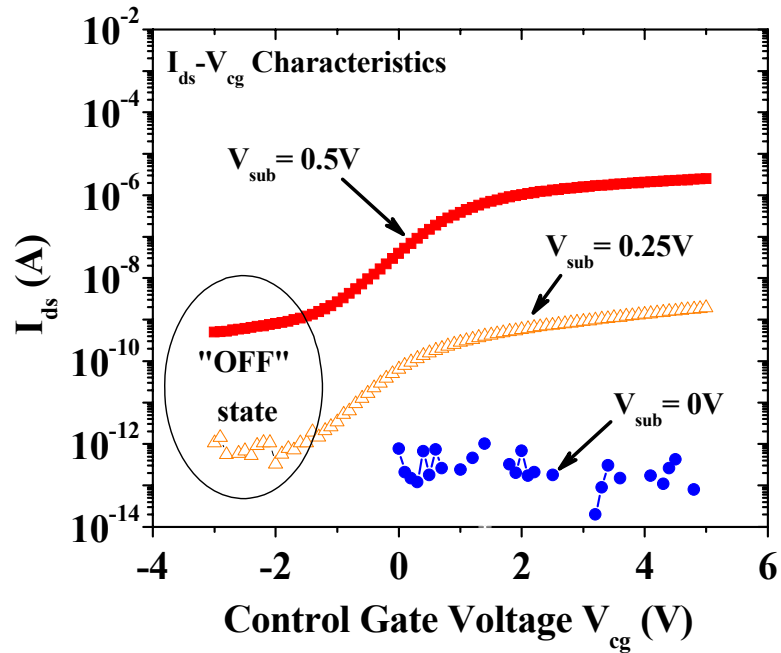
Figure 5-13: *The I_{ds}-V_{cg} characteristics of an n-type sensor with a W/L of 3 and a 10×10um extension area. The different I-V characteristics were obtained at the different substrate biases. During the measurement, V_s is 0V and V_{ds} is 0.5V.*

Sensors designed on the first chip could be used for chemical sensing. However, the devices operated with less than desirable characteristics and had to be turned on either using the tunneling techniques, which could induce some permanent damage, or using the small substrate bias which had a very small drain/source current range. Sensors with the better I-V characteristics were required. Therefore, the second iteration of sensors was designed.

5.4.2 I-V Characteristics of Sensors on the Second Chip

As introduced in Chapter 3, the floating gate extensions of the sensors designed on the second chip were made of the top polysilicon layer rather than the bottom polysilicon layer.   Due to the increased ILD thickness, the parasitic capacitance C_2 was even smaller leading to much improved I-V characteristics.   These sensors were measured and their current-voltage characteristics will be discussed in the following section.

5.4.2.1   Typical I-V characteristics of Sensors

Many different sensors were included in the second iteration of the chemical sensor development.   Although these devices had the different W/L ratios and/or the extension areas, the I-V characteristics of sensors were found to be quite similar.   Typical I-V characteristics of n-type and p-type sensors are shown in Figure 5-14.   During these measurements conventional test conditions were applied, where the source and the substrate/ n-well were grounded, the drain was applied with a certain voltage (e.g., 1V) and a voltage sweep was applied to the gate.
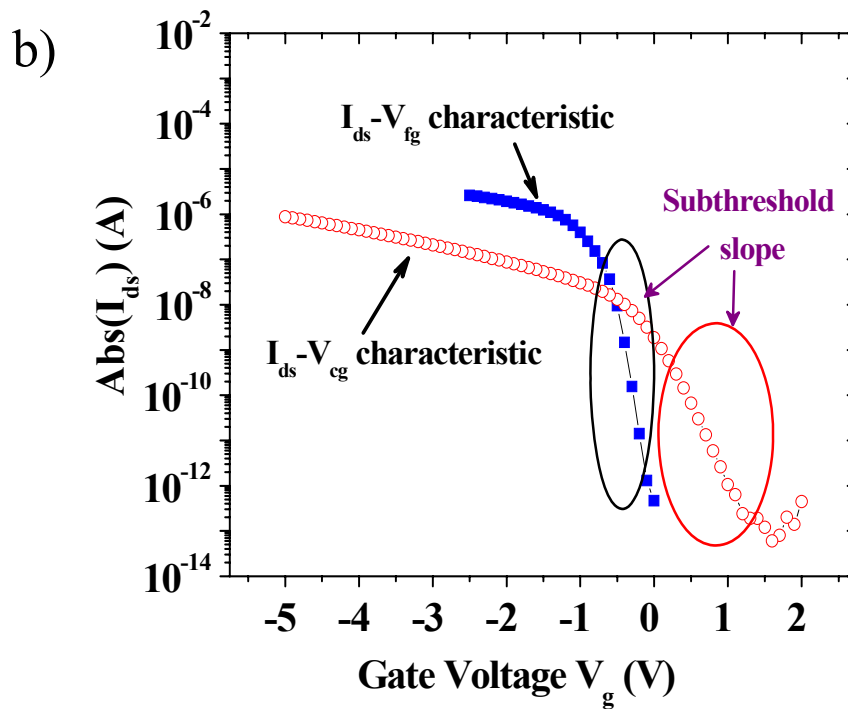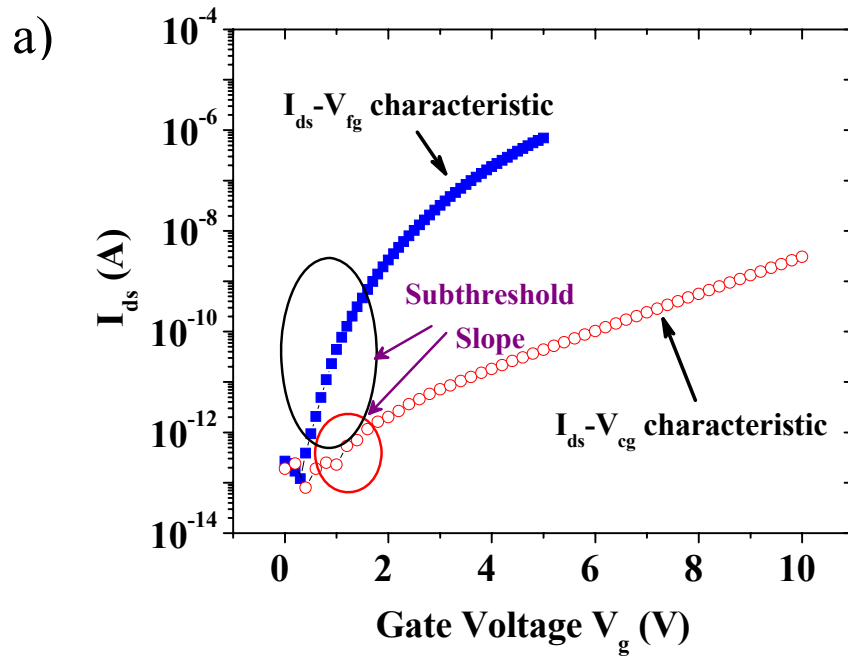
Figure 5-14: *Typical I-V characteristics of sensors designed on the second chip. The characterized sensor (W=16um, L=0.8um, and the extension area is 100x100um. a) n-type device: V_s=V_{sub}=0V, V_{ds}=1V; b) p-type device: V_s= V_{n-well} =0V, V_{ds}= -1V.*

Different from the sensors designed on the first chip, these devices were found to be turned on easily by the control gate and the required voltage sweep was much smaller; 0~5V as opposed to 0~26V for the first group. Comparing these two I_{ds}-V_{cg} characteristics (see Figure 5-14), the subthreshold slope of p-type sensors was found to be steeper than that of n-type sensors and the drain/source current of p-type sensors varied over a larger range than for n-type sensors. These characteristics indicated that the p-type sensor would be more sensitive for chemical sensing as a larger current change would be observed for a given V_{th} shift.

5.4.2.2 Effect of the Gate Width/ Length Ratios

The eight sensors listed in Table 5-4 were used to demonstrate the effect of the *W/L* ratio on the drain/source current. All of these sensors had the same gate length (L=0.8 μm) and floating gate extension areas (20×20 μm), but different *W/L* ratios. The current-voltage (I-V) characteristics of n-type and p-type sensors are shown in Figures 5-15 and 5-16 respectively. As expected, the largest drain/source current was obtained when the *W/L* ratio was largest (W/L=50), while the smallest drain/source current was obtained when the *W/L* ratio was smallest (W/L=6.25). Sensors with other extension areas, such as 50×50 μm, showed similar results.

Table 5-4: *List of sensors (L=0.8 µm) used to test the effect of the gate width to length ratio*

Dopant	No.	Gate Width (µm)	Gate Width to Length Ratio
n-type	1	5	6.25
	2	8	10
	3	16	20
	4	40	50
p-type	1	5	6.25
	2	8	10
	3	16	20
	4	40	50

Figure 5-15: *The I-V characteristics of four **n-type** sensors with the same 20× 20µm extension area but with a different W/L ratio; a) I_{ds}-V_{fg} characteristics; b) I_{ds}-V_{cg} characteristics. During the measurement, V_s=V_{sub}=0V, V_{ds}=1V.*

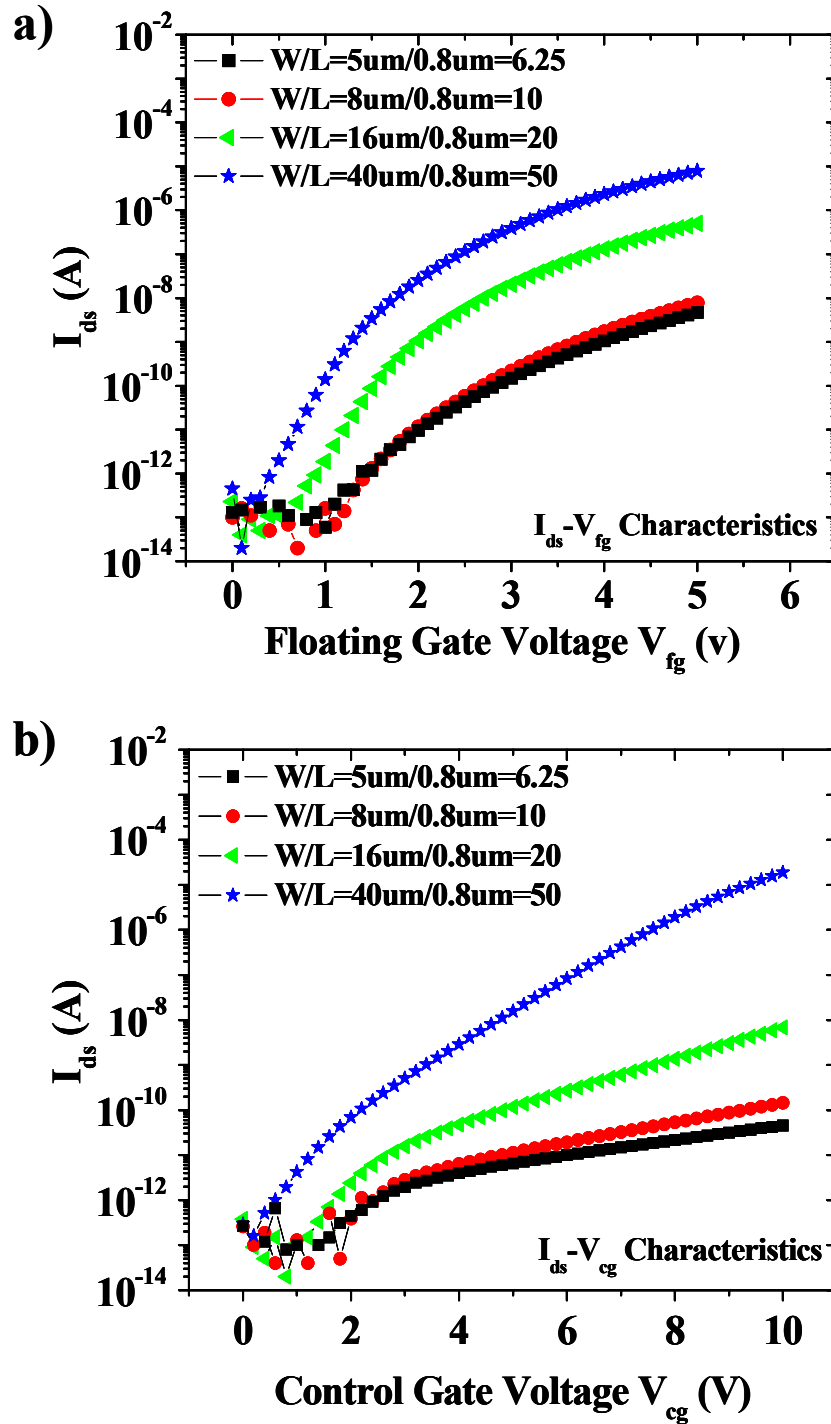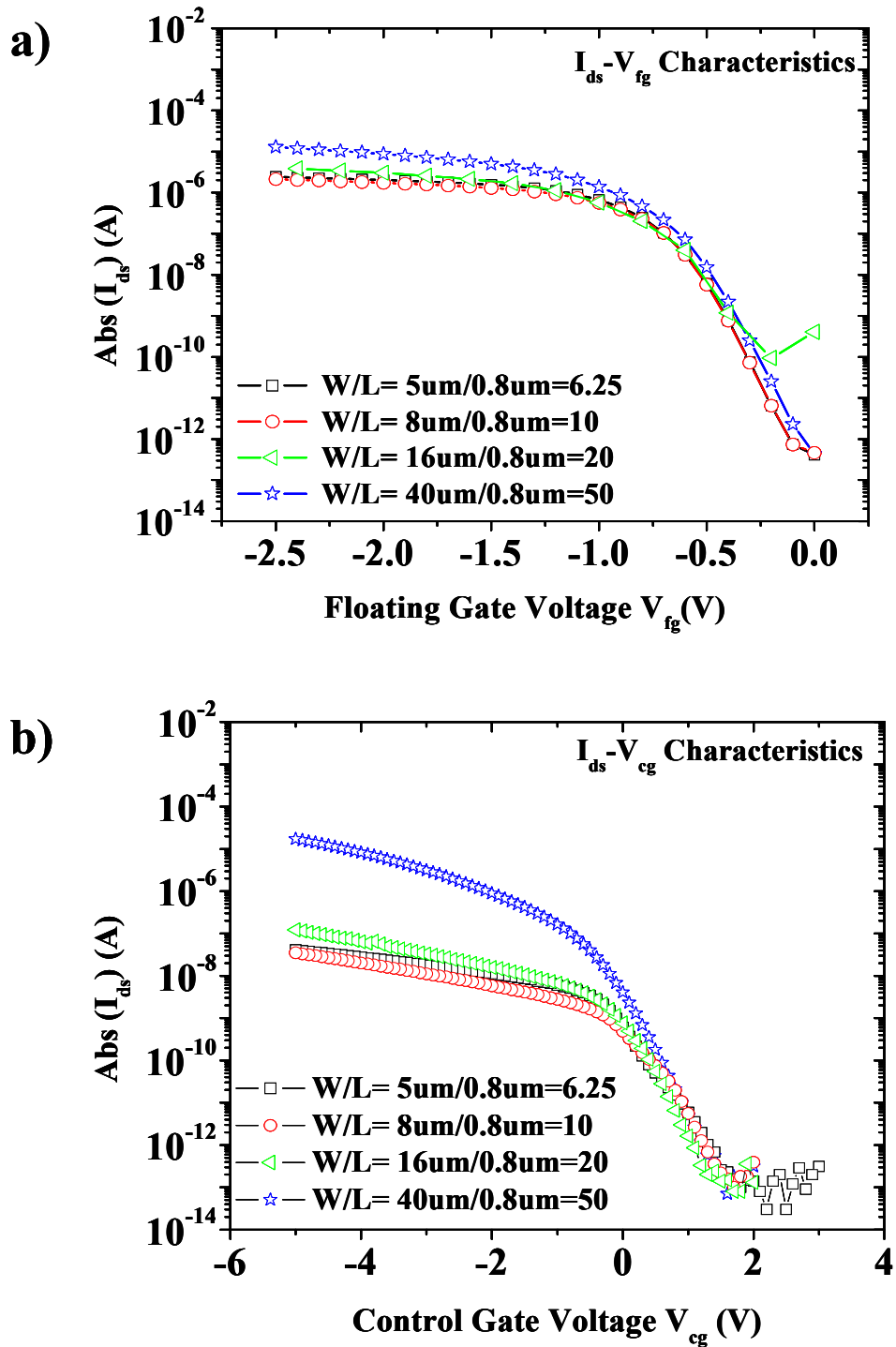**Figure 5-16**: *The I-V characteristics of four **p-type** sensors with the same 20 x 20μm extension area but with a different W/L ratio; a) I_{ds}-V_{fg} characteristics; b) I_{ds}-V_{cg} characteristics. During the measurement, V_s=$V_{n\text{-}well}$=0V, V_{ds}=-1V.*

5.4.2.3 Effect of the Extension Area

The floating gate extensions designed in sensors had four different sizes: 10×10, 20×20, 50×50 and 100×100 μm.   To establish how the I-V characteristics of the sensors would be affected by the floating gate extensions with the different sizes, various p-type sensors were measured.   The gate dimensions of these sensors are listed in Table 5-5. The data from these devices is presented in Figures 5-17 to 5-20, and the I-V characteristics were shown to be not strongly affected by the extension areas, especially for sensors with a large gate area.   Some shifts of the I-V plots shown in Figure 5-19 were not typical and could have been a result of the damage in the CMOS fabrication.

The p-type sensors were selected for further investigation due to more desirable I-V characteristics shown.   However, n-type sensors could still be used but likely with less sensitivity.

Table 5-5:   *List of p-type sensors used in this experiments*

No.	Gate Length (μm)	Gate Width (μm)	Gate Width to Length Ratio
1	0.8	5	6.25
2	0.8	8	10
3	0.8	16	20
4	0.8	40	50

1st Group of Devices: W/L = 5µm / 0.8µm = 6.25

a)

b)

Figure 5-17: *The I-V characteristics of p-type sensors with the same W/L ratio (W/L=5µm/0.8µm=6.25), but a different extension area. During the measurements, Vs=V$_{sub}$=0V, V$_{ds}$= -1V. Both the I$_{ds}$-V$_{fg}$ a) and the I$_{ds}$-V$_{cg}$ b) characteristics are shown.*

2nd Group of Devices: W/L = 8μm / 0.8μm = 10

a)

I_{ds}-V_{fg} Characteristics

- extension area 10x10um
- extension area 20x20um
- extension area 50x50um
- extension area 100x100um

Abs(I_{ds}) (A)

Floating Gate Voltage V_{fg} (v)

b)

- extension area 10x10um
- extension area 20x20um
- extension area 50x50um
- extension area 100x100um

Abs(I_{ds}) (A)

I_{ds}-V_{cg} Characteristics

Control Gate Voltage V_{cg} (V)

Figure 5-18: *The I-V characteristics of p-type sensors with the same W/L ratio (W/L=8μm/0.8μm=10), but a different extension area. During the measurements, Vs=V$_{sub}$=0V, V$_{ds}$= -1V. Both the I$_{ds}$-V$_{fg}$ a) and the I$_{ds}$-V$_{cg}$ b) characteristics are shown.*

3rd Group of Devices: W/L = 16µm / 0.8µm = 20

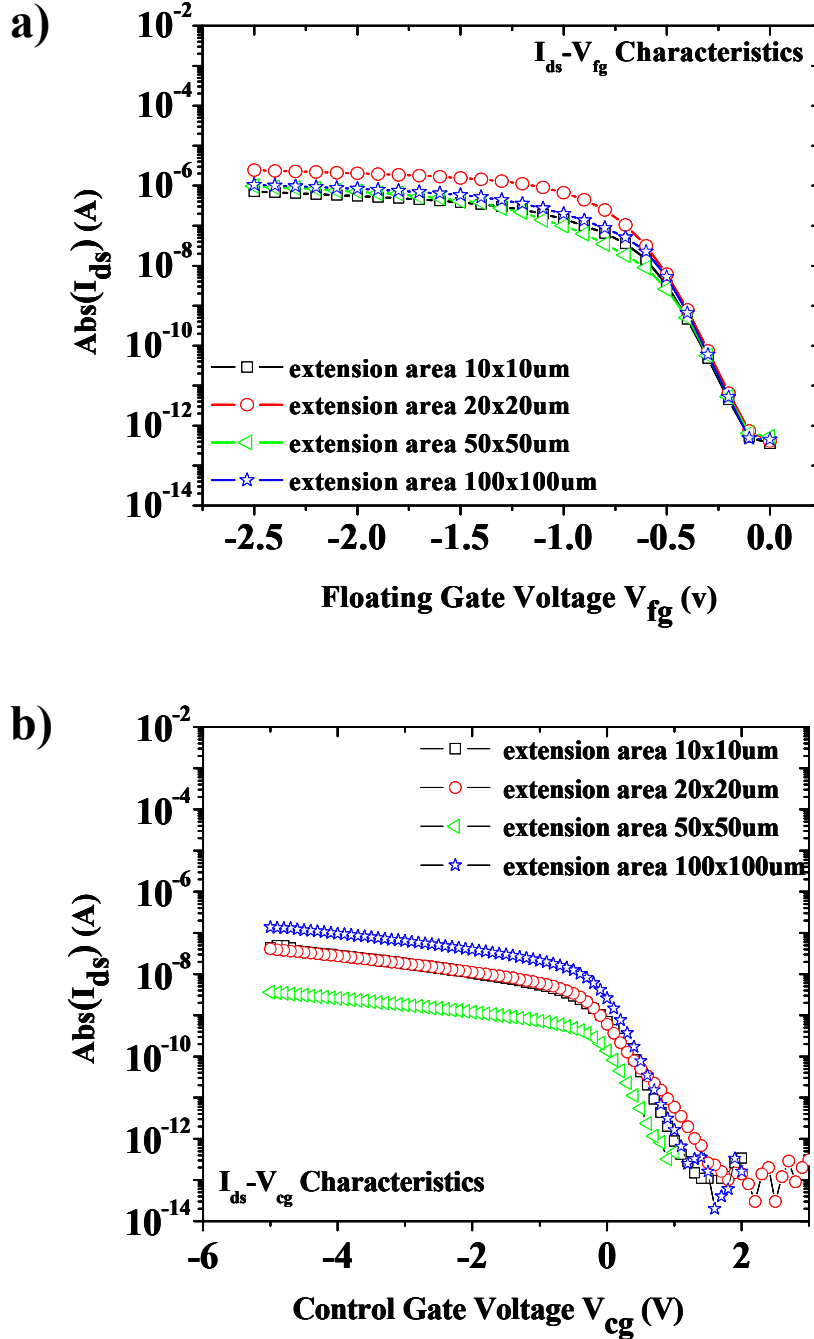**Figure 5-19**: *The I-V characteristics of p-type sensors with the same W/L ratio (W/L=16µm/0.8µm=20), but a different extension area. During the measurements, $V_s=V_{sub}=0V$, $V_{ds}= -1V$. Both the I_{ds}-V_{fg} a) and the I_{ds}-V_{cg} b) characteristics are shown.*
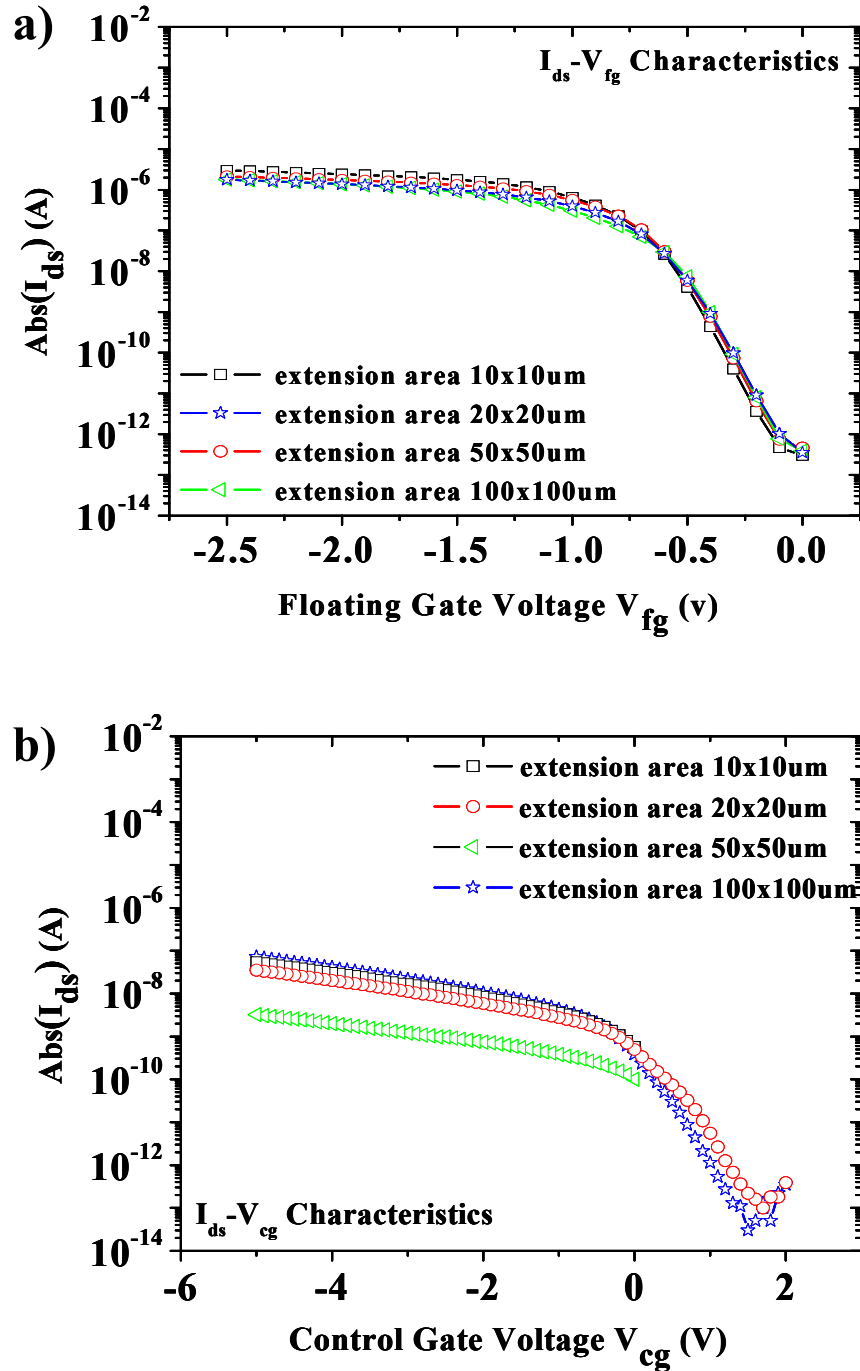
4th Group of Devices: W/L = 40μm / 0.8μm = 50

a)

b)

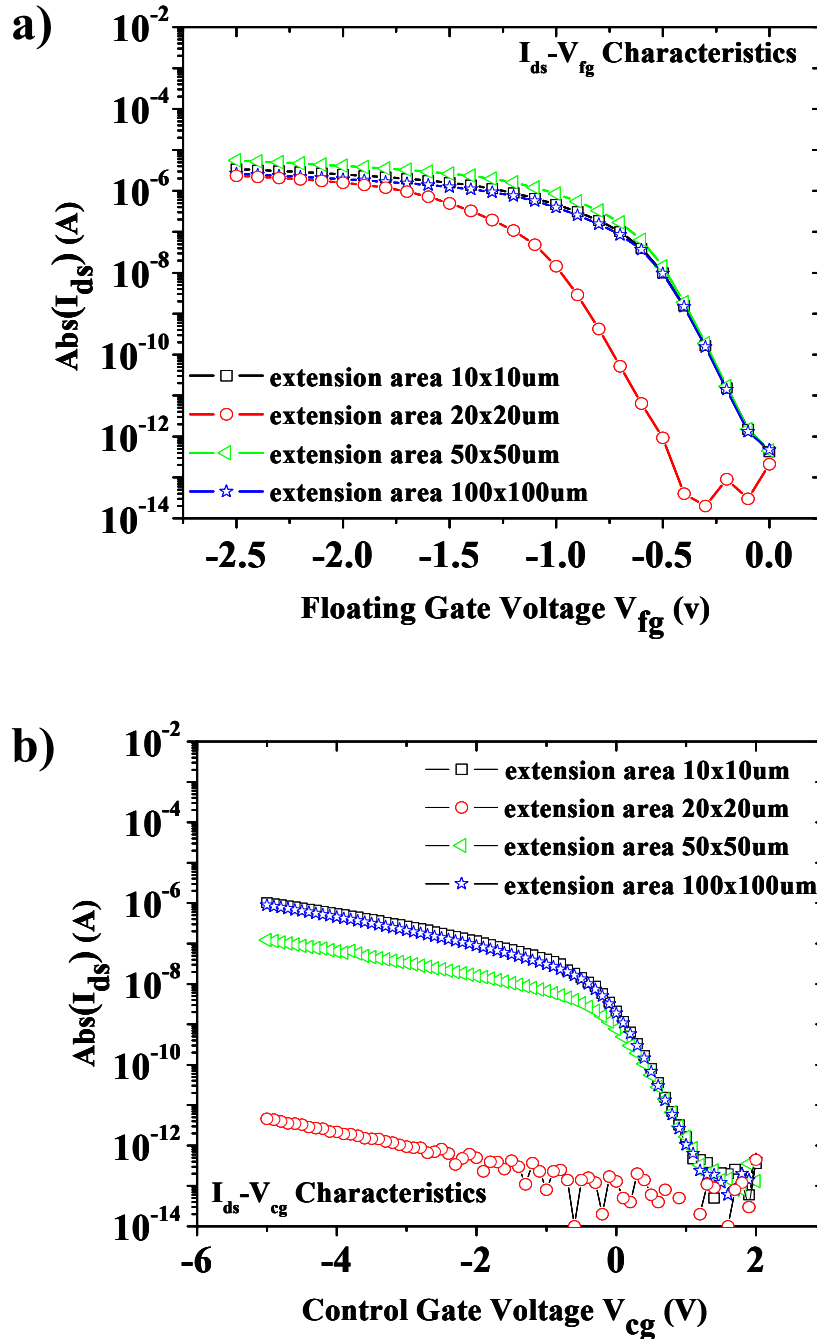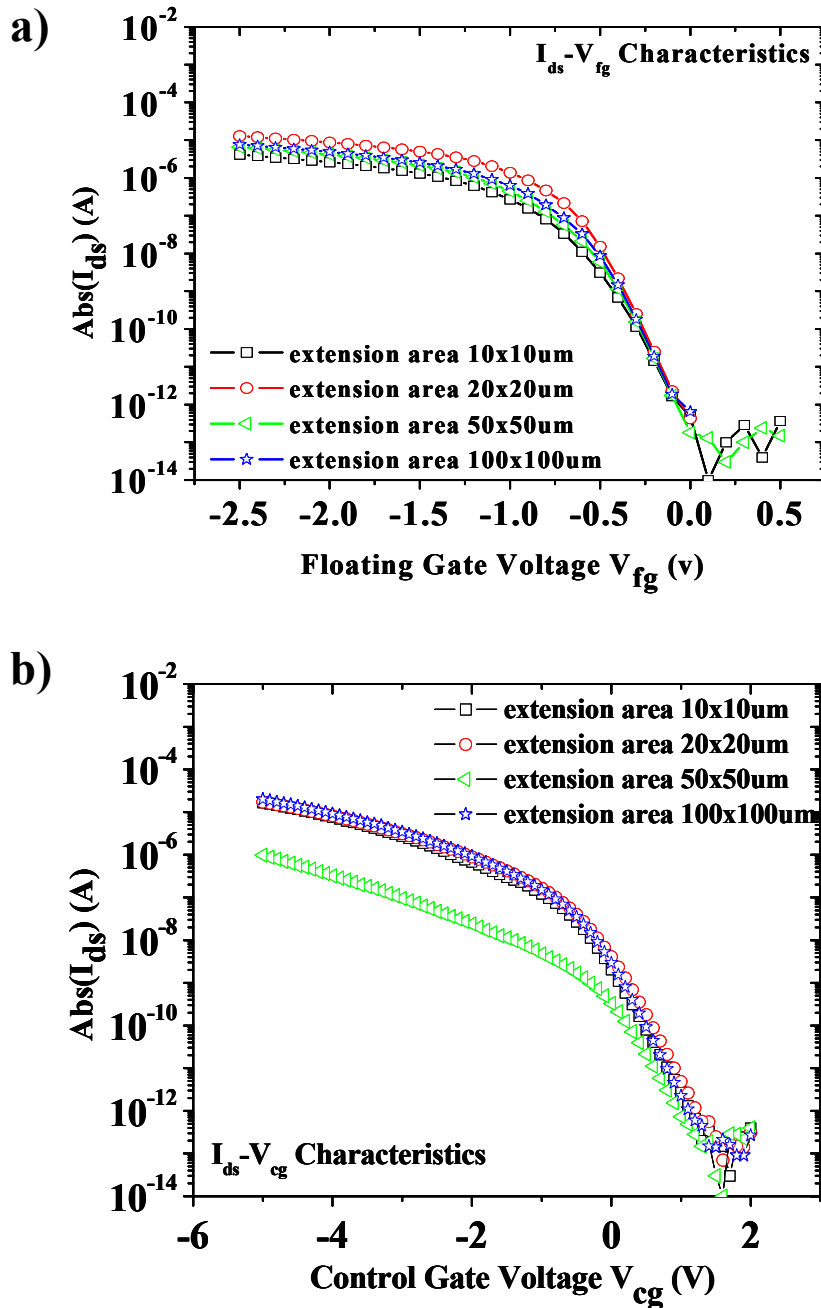**Figure 5-20**: *The I-V characteristics of p-type sensors with the same W/L ratio (W/L=40μm/0.8μm=50), but a different extension area. During the measurements, $V_s=V_{sub}=0V$, $V_{ds}=-1V$. Both the I_{ds}-V_{fg} a) and the I_{ds}-V_{cg} b) characteristics are shown.*

All of sensors designed in the second iteration demonstrated electrical characteristics (I_{ds}-V_{cg}) that would enable them to be used for chemical sensing. The p-type sensors were found to be more sensitive than the n-type devices.

5.5   I – V Characteristics during the Chemical Sensing

Due to the difficulties met with the RIE processing (see Chapter 4), no device was produced with a useable floating gate extension. However, to still demonstrate the feasibility of this type of sensor, an "external area" was used to replace the standard floating gate extension. This "external area" was connected to the floating gate of the testing sensor and therefore worked as a "pseudo" floating gate extension.

In order to connect the "external area" with the testing device, the chip was glued on a chip carrier as shown in Figure 5-21. A gold pad on the edge of the chip carrier was used as the "external area". This pad was wire bonded to the floating gate of the testing device and the "pseudo" floating gate extension was thus formed.

A pH-sensitive polymer was then deposited electrochemically on the "pseudo" floating gate extension. The dodecylbenzenesulfonic acid-doped polyaniline film was the "sensing" polymer (see Figure 5-21) that was deposited and tested. The device was then exposed to an 8 parts per thousand (ppt) sulfuric acid (H_2SO_4) gaseous mixture as obtained

from the vapour immediately above an appropriate sulfuric acid aqueous solution.
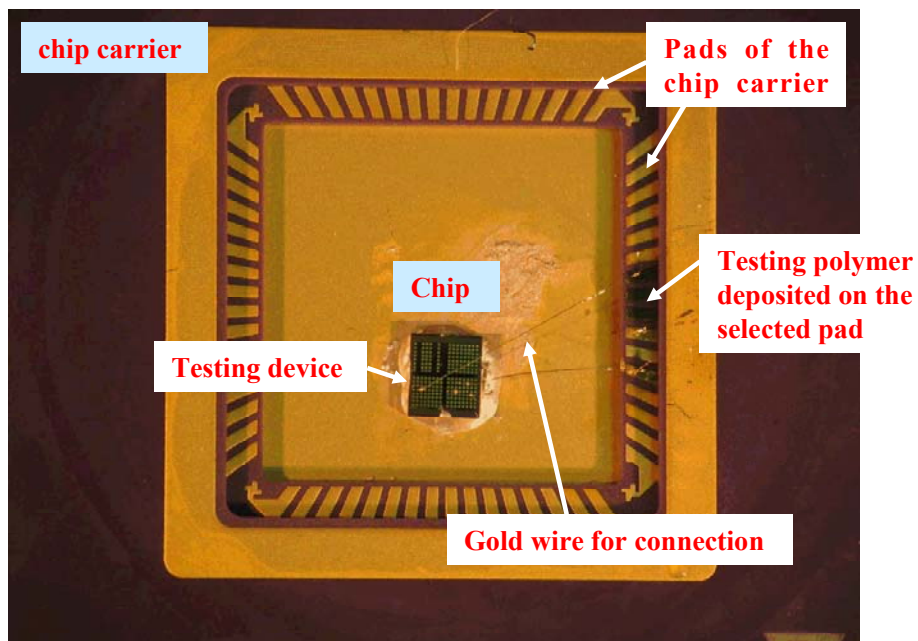
Figure 5-21: *The set-up of the pseudo floating gate extension that was used in chemical sensing.*

During the chemical exposure, the polymer accepted the protons from the acid and increased the total amount of the charge in the material. The polymer, then positively charged (see Figure 5-22), generated an interface potential between the polymer and the floating gate. This interface potential could move the electrons away from the floating gate and reduce the net charge density on the floating gate. Therefore, the device required a higher gate voltage to be turned on. Depending on the density of the reactive molecules in the polymer and the H_2SO_4 solution, a different interface potential would be induced and the threshold voltage change would be different. As a result, the I-V characteristic would

be shifted differently.
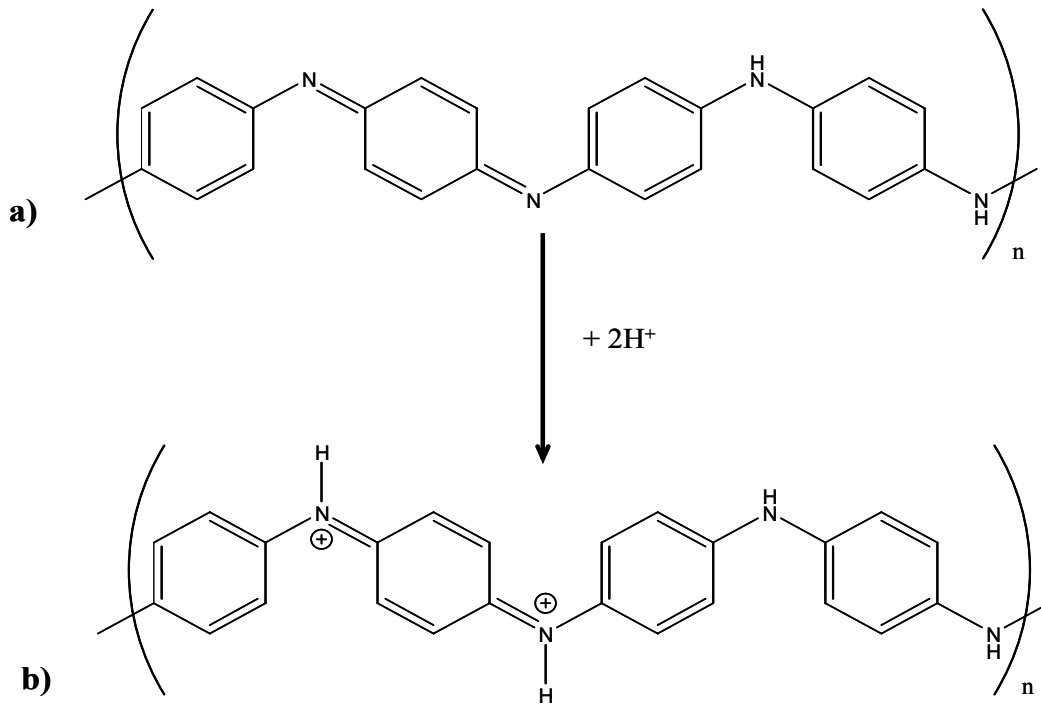
Figure 5-22: *Sites within the polymer chain of polyaniline that have become positively charged upon exposure to some acid analyte in the test environment. Illustrated are a) sites before the chemical exposure and b) sites after the chemical exposure.*

A p-type sensor on the chip was measured and the obtained current-voltage characteristics (I_{ds}-V_{cg}) before (curve 1) and after (curve 2) the chemical exposure are shown in Figure 5-23 and 5-24. By plotting the drain/source current on the linear scale (see Figure 5-23), the threshold voltage of the sensor was found to be changed from ~ -4.8 V to ~ -8.5V with a shift of ~3.7 V. Using equation 5.5, together with C_1 per unit area (~6.8×10^{-8} F/cm^2) derived from the data in the design rules, the charge change due to the chemical reaction was ~2.45×10^{-7} C/cm^2.

Figure 5-23: *The current-voltage (I-V) characteristics of a p-type sensor (W=5μm, L=0.8μm) before and after the chemical exposure. The obtained drain/source current was plotted on the LINEAR scale.*

The current-voltage (I-V) characteristics was then plotted on the logarithmic scale (see Figure 5-24) to observe the sensitivity of the device. It was found that the inverse subthreshold slope of the device was ~60 mV/decade, suggesting that the drain/source current of the sensor could change approximately 5~6 decades in the subthreshold region. For a decade change in current, the threshold voltage shift should be ~0.6 V, which was induced by a charge change of ~3.97×10^{-8} C/cm^2 stored on the floating gate. Using these data, this p-type sensor would be able to detect a 0.1 ppt sulfuric acid

(H$_2$SO$_4$) gaseous mixture.   The expected change in the threshold voltage, net charge on

the floating gate and the drain/source current is listed in Table 5-6.

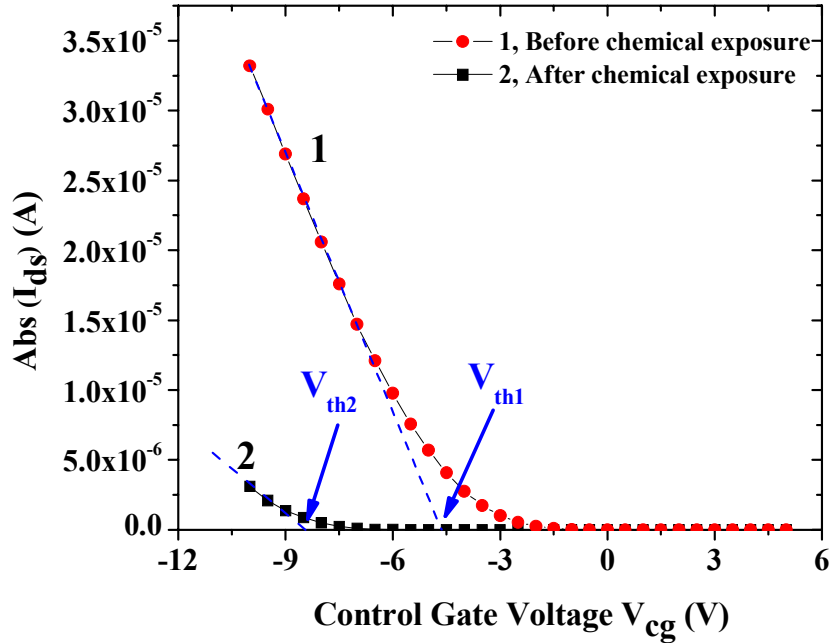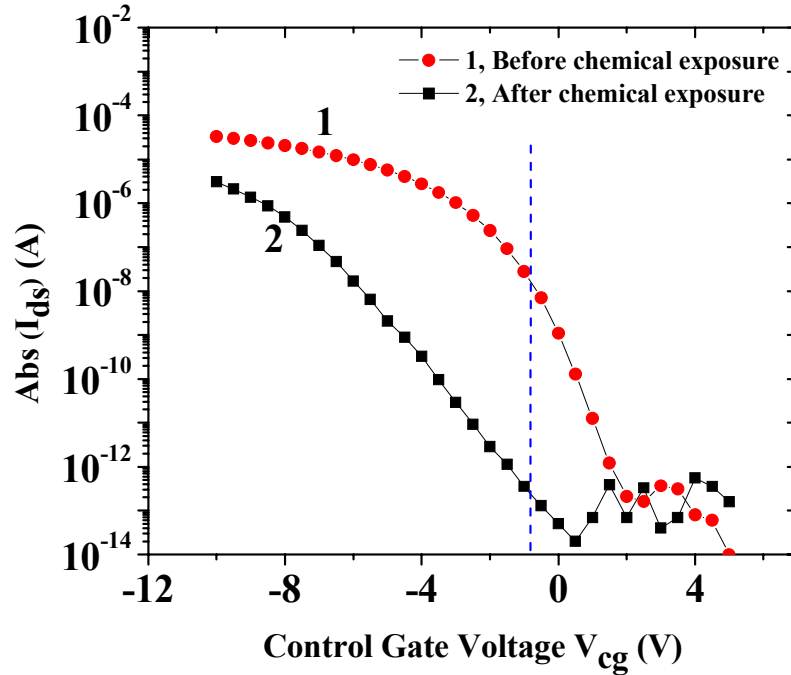**Figure 5-24**: *The current-voltage (I-V) characteristics of a p-type sensor (W=5μm, L=0.8μm) before and after the chemical exposure. The obtained drain/source current was plotted on the LOGARITHMIC scale.*

Table 5-6:   *The predicted sensitivity of the p-type sensor*

Concentration of H$_2$SO$_4$ gaseous mixture	ΔV_{th}	ΔQ (C/cm^2)	ΔI (decades)	Current Multiplier	Remarks
8ppt	3.7 V	2.45×10^{-7}	~6.2	~ ×10^6	Observable
1ppt	0.46 V	3.1×10^{-8}	~0.77	~ ×5.89	Observable
0.1ppt	**46 mV**	**3.1×10^{-9}**	**~0.08**	**~ ×1.2**	**Observable**
0.01ppt	4.6 mV	3.1×10^{-10}	~0.01	~ ×1.02	Too small

In this chapter, the I-V characteristics of the designed sensors and devices were measured and analyzed. Even though it was difficult to turn on the sensors from the first chip, three methods were developed to enable their operation. Sensors designed on the second chip showed much better I-V characteristics. The p-type sensors were found to be more sensitive for chemical sensing than n-type devices. Even with the processing difficulties, the feasibility of the sensors was still demonstrated using a "pseudo" floating gate extension.

Chapter 6 Conclusions

A chemical sensor that can be used to create a sensor array system to emulate the capabilities of mammalian olfaction was developed in this research. The sensor was designed based on the floating gate field-effect transistor structure. Two iterations of the sensor chips and more than seventy five n-type and p-type sensors were designed and fabricated. The operating characteristics of sensors were found to be improved by increasing the ILD thickness between the floating gate extension and the substrate.

Twelve post processes were developed to expose the floating gate extensions of the sensors. Most of the difficulties were met in the reactive ion etching process. Even though the developed etch recipe could quickly etch away the ILD layer, its selectivity to the polysilicon was very low making it difficult to stop the etching at the polysilicon interface.

These chemical sensors had the similar operating characteristics as that of the standard MOSFETs. From the characterization results, the p-type devices were found to be more sensitive than n-type devices. Therefore, a p-type device with a "pseudo" floating gate extension was used to demonstrate the feasibility of the sensor. From the measured current-voltage (I_{ds}-V_{cg}) characteristics, this p-type sensor should be able to

detect the charge change induced by the 0.1 ppt sulfuric acid (H_2SO_4) gaseous mixture. The designed chemical sensors could be highly sensitive.

However, future work in two areas can still be undertaken on this project. The first area relates to the post-processing. The different reactive gases, such as H_2 and CH_2F_2 should be used in the recipe in order to improve the etch selectivity of ILD to Si. The RIE, ICP power or the pressure set in the reactive chamber may also be adjusted. The second area relates to the sensor design. It would be more reasonable to use an aluminum metal layer to form the floating gate extension of the sensor due to four reasons. 1) the metal layers (e.g., 0.64 μm) are much thicker than the top polysilicon layer (i.e., 0.18 μm); 2) the etch selectivity of ILD to Al can be much higher; 3) the difference between Al and ILD can be easily observed under the microscope; 4) the dielectric thickness above the floating gate extension can be decreased and thus shorten the etching time. All of these will simplify the post-processing and make the floating gate extensions to be more easily exposed.

The schematic diagram of a potential sensor design is shown in Figure 6-1. In this structure, the top metal layer is used for the floating gate extension. Since the top metal layer could be left open in the standard CMOS process, no post-processing would be required and would make the integration of the sensors much easier. This sensor will be

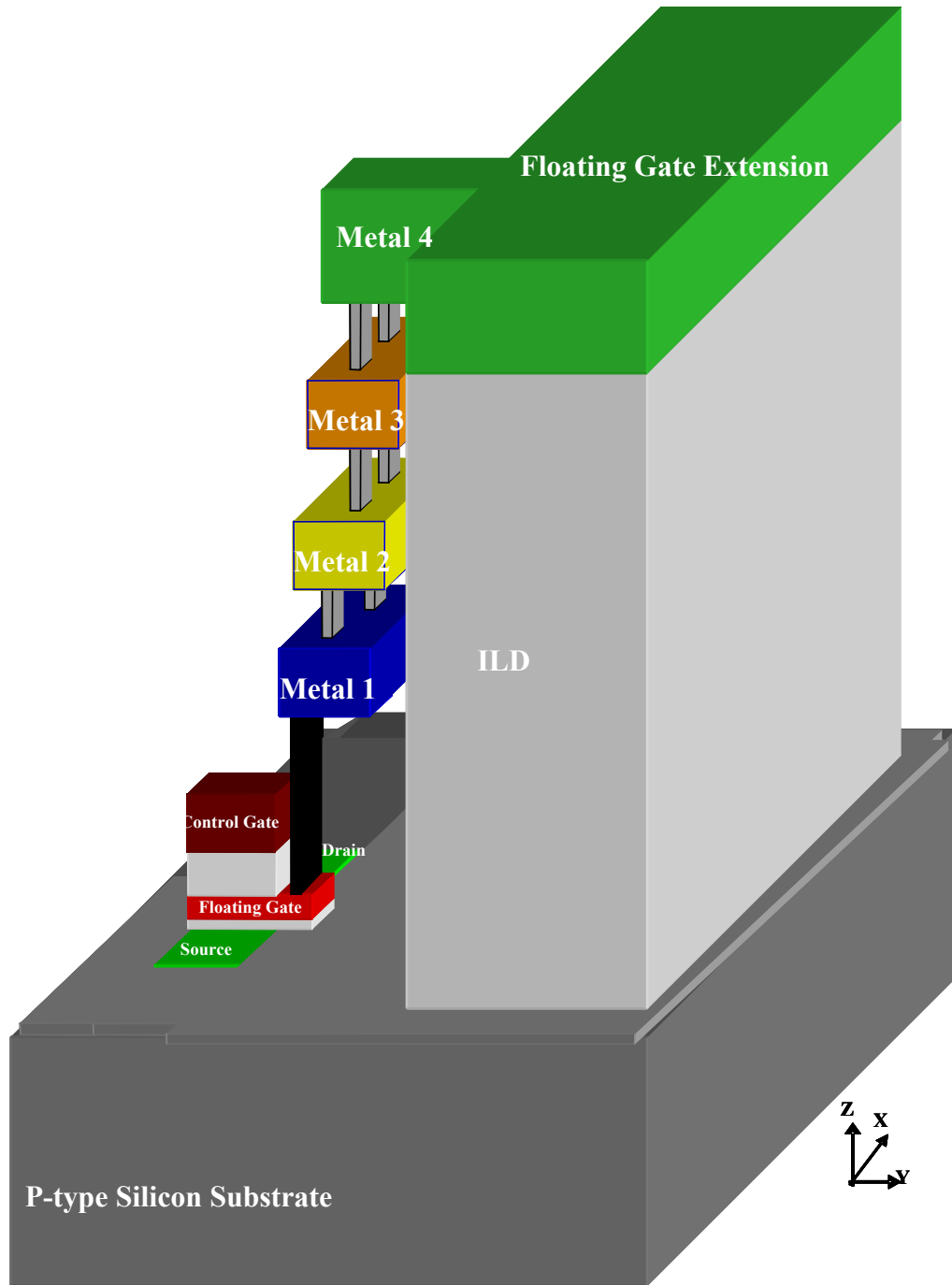fabricated and tested in the near future.

Figure 6-1: *The potential sensor with the floating gate extension exposed after the standard CMOS process. No post-processing is required.*

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