Adaptive Phase Locked Loops for VSC connected to weak ac systems

By

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Abstract

The performance of the High voltage dc systems is dependent on the stiffness of the ac bus, it is connected to. With the traditional synchronous reference frame-phase locked loops (SRF-PLL), voltage source converters (VSC) systems with large PLL gains, connected to weak ac networks are shown to be prone to instabilities, when subject to disturbances. Thus, for weak ac systems the plausible operating range for the traditional SRF-PLL is limited.

In this thesis a new Adaptive PLL is designed. This PLL has a frequency adaptive 'pre-filter' architecture, designed to extract the fundamental positive sequence component of the input voltage, to be fed into the traditional SRF-PLL for tracking of its phase angle. The pre-filter comprises of frequency adaptive proportional resonant (PR) filters and all-pass filters, to extract only the fundamental positive sequence component. Compared with other traditional PLL topologies, this Adaptive PLL shows superior immunity to voltage distortions and negative sequence, and also has a faster dynamic performance.

To include the Adaptive PLL into the VSC control system, the control system parameters are optimized. Non-linear Simplex Nelder-Mead algorithm is used for optimization of the control parameters. A modified approach for the objective function formulation, which allows for finer control and improved dynamic performance, has been presented.

The thesis presents a comparative analysis of the performance of the traditional SRF-PLL with the Adaptive PLL in a VSC control system, and its impact on stability for VSCs connected to weak ac systems. In a VSC system, the reduced sensitivity of the system stability, to the PLL gain variation of the Adaptive PLL, is demonstrated.

Further, several tests were devised to compare the stability with the inclusion of the above mentioned PLL designs. Using Electromagnetic Transient Simulation, it is shown that the VSC equipped with the Adaptive PLL can operate into very weak ac systems (i.e. SCR≈1.3) more stably in comparison with widely used SRF-PLL.

Acknowledgements

I would like to express my deep sense of gratitude to Prof. Aniruddha Gole, for his continued guidance during the course of this research. To work under you and experience your enthusiasm for research, first hand, has been a privilege.

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Dedication

To my beloved Mother.

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List of Abbreviations:

HVdc	High Voltage Direct Current
VSC	Voltage Source Converters
LCC	Line Commutated Converters
CCC	Capacitor Commutated Converters
SCR	Short Circuit Ratio
ESCR	Effective Short Circuit Ratio
PLL	Phase Locked Loop
SRF	Synchronous Reference Frame
PWM	Pulse Width Modulation
SPWM	Sinusoidal PMW
pu	Per Unit
ITSE	Integral of time multiplied by square of error
ISE	Integral of square of error
THD	Total harmonic distortion
PR	Proportional Resonant
PI	Proportional Integral
EMT	Electromagnetic Transients
OE-EMTS	Optimization Enabled EMT Simulation

Chapter 1
Introduction

1.1 Background

The Power System broadly comprises of three components, namely, generation, transmission and finally, the distribution network [1]. The generation largely comprises of synchronous generators in the grid, which are typically located in remote areas. Lately, with the advent of distributed generation, relatively smaller sources are now connected into the grid, allowing for the integration of cleaner sources of energy. In Canada, the main source of generation is hydro power [2] and hence, eco-friendly. Other popular traditional sources of power generation include thermal, gas and nuclear power plants, to list a few. Around the world, among the distributed generation sources, wind [3] [4] and solar farms [5] are fast becoming viable options.

The transmission system forms the conduit between the distribution network and the generators. High voltage ac systems are commonly used for transmission distances less than 500km [6], owing to their cheap cost. But, the integration of the renewable energy sources into the network has posed several challenges for network engineers, owing to the wide range of

frequency variations in these networks [4]. And thus, High Voltage DC (HVdc) systems are imperative for the inclusion of these sources into the network.

At present, HVdc transmission systems are the preferred choice for bulk transmission of power. The increased efficiency and improved voltage profile over long distance power transmission, are just some of the major advantages that this technology offers. Moreover, to cross large water bodies, DC cables [7] are the only solution. In Chapter 2, a comparison between HVac and HVdc systems has been provided.

The traditional line commutated converters (LCC) HVdc systems based on thyristors have served well for about six decades now [8]. There are several large projects currently in operation, based on the traditional LCC systems, including the collector system in Manitoba, (Bipole I and Bipole II), popularly known as the Nelson River System [9]. By controlling the firing angle of the LCC converters at either ends, it is possible to control the active power flow in the DC lines. At present, there are well established control systems for the LCC converters, even for contingency conditions. But, the requirement of additional reactive power support at the converter and also, the need for considerable filtering at the ac side (Chapter 2), are just some of the limitations of the LCC system.

Despite the increased installation costs, with the ability to independently control both the active and reactive power supply, voltage source converters (VSC) are fast becoming viable alternatives to the LCC systems. In contrast to the LCC, the VSC has several performance advantages, such as its reduced susceptibility to ac system disturbances and its ability to generate reactive power[6]. For reasons ranging from increased flexibility, in terms of the control system design (including DC grids), to easier integration of the renewable sources of generation into the power network, the future of VSC HVdc looks promising.

Based on self-commutated switches, the voltage source converter (VSC) HVdc allows for very high switching frequencies, ranging up to several *kHz*, thus eliminating the need for large ac filters. Especially, with the Modular Multilevel Converter (MMC) topology [10], the VSC can generate an almost perfect sinusoidal waveform, with no additional filtering required on the ac side. Alternatively, with the two-level converters the technique of pulse width modulation (PWM) is popularly used in VSCs to generate the firing pulses for the switching valves.

One of the main reasons for the large interest in the VSC technology is its ability to connect into weaker ac systems, compared to the LCC. The strength of the ac network connected to the converter is quantized by the Short Circuit Ratio (SCR) [8], which is defined as the ratio of the Short Circuit MVA (SCMVA) at the ac bus to rated power,P_{dc}, of the converter as shown in equation (1-1).

$$SCR = \frac{SCMVA}{P_{dc}} \tag{1-1}$$

For LCC systems it widely accepted that for SCR<2.5, (implying an ESCR≈2.0) the system is considered weak. In contrast, [11] defines this limit for networks connected to VSC systems to be SCR=1.6. Further, [11] also reported the results of the small signal studies on the VSC system, upon performing sensitivity studies on the impact of the control gains of the VSC on the overall system stability. Considering the nature of small signal studies, these results are optimistic in nature. The conclusions from [11], pointed to the significant impact that the PLL gains have on the stability when SCR of the ac system is greater than 1.6. These results formed the motivation for this research. In this thesis, a new Adaptive PLL design is developed, which works well under conditions where the VSC is connected to very weak ac

systems. It is also important to note, that the studies in this thesis are done on EMT software, PSCAD/EMTDC, which allows for detailed modeling of the non-linear VSC HVdc system.

1.2 Project objective and outline of this thesis

Phase Locked Loop (PLL) tracks the phase angle and frequency of the fundamental positive sequence component of the input ac voltage. The PLL provides the reference phase angle for the VSC control system. Typically, the Synchronous reference frame PLL (SRF-PLL) is used. However, this has posed some stability issues when operating in weak ac systems. The emphasis of this thesis is to address the issue of the sensitivity of the VSC to the PLL, when it is connected to weak ac systems. This research aims to provide a solution in the form of a new PLL design, which shows good performance when providing the reference angle to VSC systems, even when they are connected to very weak ac system, up to SCR=1.31.

The broad outline of this thesis is as follows:

Chapter 1: Introduction

This chapter provides a brief introduction to HVdc systems and touches upon the organization of this thesis.

Chapter 2: VSC HVdc systems: Transmission and Control

In this Chapter, a comparison between the ac and dc systems is conducted, for bulk power transmission. The advantages of HVdc systems over the ac systems are categorized. The traditional LCC systems are contrasted with the VSC systems. The four quadrant operation of the VSC is explained, with in depth analysis of the *dq*-decoupled control system.

Chapter 3: Design and Analysis of the Adaptive Phase Locked Loop

Owing to the tracking errors with the SRF-PLL design, in the presence of voltage distortions in the input, it is essential to design a PLL architecture which can extract true phase angle output i.e., the fundamental positive component of the input voltage. In Chapter 3, a new Adaptive PLL design is introduced, which is designed to extract this component. The methodology and design for this PLL is presented. The criterion for the selection of PLL gain parameters is established. Further, the gains of the Adaptive PLL and that of the SRF-PLL and SRF-PLL+filter designs are optimized for good dynamic performance. Using these optimized gains, the comparison between them is done with distorted input voltages, including unbalance, harmonics and interharmonics.

Chapter 4: Optimization of the VSC Controls

Using the non-linear Simplex algorithm, the VSC control parameters are tuned using objective functions that quantify the dynamic performance of the VSC. This chapter explains the criterion for the formulation of the objective Function for the VSC terminal.

Chapter 5: Adaptive PLL for the VSC

Using the optimized controls from chapter 4, studies are done using the electromagnetic transient simulation program, EMTDC/PSCAD, to study the performance of the Adaptive PLL providing angle reference to the VSC control system, when connected into a weak ac system. The performance of the VSC is compared with the traditionally used SRF-PLL. Several large disturbance tests are formulated and studied, thereof, to establish the impact of the Adaptive PLL on the stability. It is proved that with the inclusion of the Adaptive PLL, the stability of the VSC system improves considerably for small as well as large disturbances, even when connected to very weak ac systems (SCR≈1.31).

Chapter 6: Conclusions and Future Work

This chapter lists the conclusions from this research. Also, possible future works are suggested.

1.3 Scientific contributions of this thesis

- Development of a new Adaptive PLL design which can operate well under distorted voltage conditions, causing minimal errors in the phase and frequency output of the Phase Locked Loop
- Optimization enabled- electromagnetic transient simulation (OE-EMTS) based optimization of the VSC controller parameters enabling greater control over the final optimized parameters
- Study of the operating range for the standard SRF-PLL and the Adaptive PLL for VSCs connected to weak ac systems
- Demonstration of the improved immunity of the VSC to large disturbances when the Adaptive PLL design is used, with very weak ac systems

Chapter 2

VSC HVdc Systems: Transmission and Control

This Chapter begins with explaining the need for HVdc systems and certain distinct advantages it offers over its ac counterparts. The types of HVdc systems are introduced and the traditional LCC converters are contrasted with the VSC. Further, the components of typical VSC HVdc system are introduced. The various control systems employed typically in a VSC system are also explored. In addition, the Phase Locked Loops and their significance in the VSC control system is studied. Thereafter, the impact that the ac system parameters can have on the VSC performance is also discussed in brief.

2.1 Introduction and background of HVdc

The contest between ac systems and DC systems is an old one. Back in the 1880s, what is now known as, the 'War of currents' [12] commenced between Tesla, who championed the idea of ac networks, and Thomas Edison, of DC networks. Edison later went on to pioneer the first electrical network, with DC transmission at low voltages, in the year 1882. Soon after, there was a proliferation of ac systems, with the main advantage being the ease of voltage transformation to different levels, which proved beneficial long distance transmission. At

present, although most of the electrical network is ac, there is still a huge interest in High Voltage DC (HVdc) Transmission.

Commissioned in 1954, the first fully commercial HVdc scheme was installed in Gotland [13]. With a rating of 100 *kV*, 20 *MW* the monopolar HVdc cable links the Sweden Mainland with the Gotland Island. The first Canadian HVdc link, however, went into service in 1969, a 312 *MW*, ±130 *kV* [14] scheme stretching 41km. At present, the longest HVdc link, still under construction is the 2071km long, ±800 *kV*, 6400 *MW* line connecting the Xiangjiaba Dam to Shanghai [15], in the People's Republic of China.

Despite the large installation costs of converters, HVdc Transmission systems find prominence due to certain distinct features that the ac systems cannot adequately measure up to or in some cases cannot offer. The salient points are discussed below [8]:

- Interconnecting asynchronous networks: Interconnecting two ac networks using an ac interconnection can result in undesired oscillations in voltage and power, following a disturbance [1]. HVdc systems provide a solution to this, since for interconnecting two networks through HVdc, the frequency and phase angle considerations, are not critical [8]. The back to back converter topologies allow for power transfer between asynchronous grids.

- Integration of renewable energy sources: Power generated from renewable energy sources such as solar and wind farms [16] [5], can have undesirable harmonics, voltage and frequency fluctuations. Connecting them directly into the ac network would have devastating effects on the loads connected in close proximity. HVdc provides the necessary interface to connect these sources into the network, without affecting the nearby loads.

- Undersea cables: Due to large charging currents in ac cables (for lengths greater than 50 *km*), it is not a practical solution to use them, for long distance transmission, such as undersea links. The HVdc cables form the only plausible solution in such cases.

- Reduced right of way (ROW) for transmission corridors: For places where land acquisition can be difficult, HVdc proves to be beneficial, considering the reduced ROW it requires, compared to ac transmission lines, for the same power level.

- Absence of reactive power consumption in transmission lines: One of the primary advantages of DC transmission is that there are only resistive losses in the DC lines. In contrast, for ac lines in long distance transmission, large reactive power compensation would be needed at regular intervals, so as to maintain an acceptable voltage profile.

- Improved stability: Unlike ac systems, with HVdc transmission, the phase angles of the ac system at either ends, are not critical. Therefore, forming interconnections are simpler. In [17], studies have shown that upon the inclusion of an HVdc link between two ac systems, the overall stability of the network improves. For instance, connecting an HVdc line between two ac networks, would reduce the impact that a fault in one network would have on the other ac network in the absence of an HVdc link.

- Lower insulation levels needed: For a given insulation level, the DC lines can transmit more power compared to the ac lines [18], primarily due to the sinusoidal nature of ac voltage.

2.1.1 Types of HVdc systems:

Depending on the converter topology and design, the following are the widely used types of HVdc systems [19]:

1. Current source converters /Line commutated converters (CSC/LCC)

2. Voltage source converters (VSC)

3. Capacitor commutated converters (CCC)

In the traditional CSC/LCC systems, the flow of the DC current is unidirectional and the power reversal takes place through the reversal of the voltage polarity. Based on line commutated devices, such as thyristors (in older systems with mercury arc valves), making high frequency switching infeasible in such systems. Therefore, they introduce significant lower order voltage harmonics into the ac side and hence, large filters are needed at the PCC (point of common coupling) in order to remove these harmonics. In addition, these converters are highly inductive in nature, and thus require additional reactive power support to maintain the ac voltage at the filter bus (typically 0.6 *pu* of the converter rating). Further, in LCC systems, during low ac voltages at the inverter side (possibly due to a nearby fault) or for operation with high DC currents, commutation failure [20] of the valves can occur. commutation failures occur due to improper turn-off of thyristor valves, resulting in the failure to transfer current from one valve to the next. Recovery from successive commutation failures require temporary cessation of power transfer which can lead to other major power system problems. Through control mechanisms (such as Voltage dependent current limiter (VDCL) [21]), commutation failure issues can be addressed partially, to prevent successive commutation failures. The DC side faults are also dealt with using the control mechanisms, such as Force Retard [21], where the rectifier is forced to act as an inverter, allowing for clearing of the dc fault. In [22], the Multi In-feed HVdc (MIHVdc) topology has been studied, where multiple LCC converters are connected in close proximity, which in certain situations have improved immunity to commutation failures in contrast to the single in-feed systems. However, due to the large reactive support requirement of the LCC, it is prone to transient

over-voltages (TOV) upon sudden tripping of loads. Further, since the direct current is unidirectional and power reversal requires a voltage reversal, the implementation of a large interconnected DC grid is not feasible with the traditional LCC.

On the other hand, for VSCs, the power reversal entails current reversal[23] [24] [7], with constant voltage polarity and hence the implementation of DC grids is feasible. Based on fast-switching devices, with precise control mechanisms such as pulse width modulation (PWM) [25] (or advanced topologies such as the Modular Multilevel Converter), the VSCs require only marginal high pass filtering at the PCC bus. These converters are capable of operating in all four power quadrants and hence, in principle, do not require any external reactive power compensation at the converter terminals, as the converter itself can absorb or deliver reactive power to maintain the ac voltage. Nevertheless, recent studies in [11] have shown, that with additional capacitive compensation at the PCC, the maximum transmissible power of the VSC increases, because the MVA rating of the VSC is now available for active power transfer and not wasted in providing reactive power. In addition, in theory, they have the black start capability [6], i.e. the ability to provide power to an ac system with no voltage source. VSCs, based on IGBTs, do not have problems such as commutation failure or that of transient over-voltage, which plague the LCC systems. Further, due to the reduced harmonic content, specialized transformers on the ac side which are needed for the LCC systems, are not required for the VSC, which can use typical commercial transformers. Currently, a major problem with the VSC system, is its performance during DC faults, considering the reverse diodes provide an uninterruptible path for the fault currents to feed the fault. Also, even though VSC systems have a smaller footprint [24], the installation costs of the converter are higher than that of the LCC.

Combining the LCC and the VSC, in [26], the dual in-feed topology has been studied, and is shown to have a higher MAP(Maximum Available Power) for the LCC converter when the VSC provides ac voltage support (reactive power) at the bus with minimal active power supply.

MTDC [27] or DC grids are HVdc systems, where 3 or more VSC converters are interconnected which allow for multi-directional flow of power. Just as in the case of an ac network, where the frequency is constant throughout [1], in a DC grid (assuming zero losses in interconnecting lines) the DC voltage is constant [27]. In [28] and [29], various control mechanisms such as the master slave, voltage margin and even autonomous control mechanisms are presented to control power flow in the DC grids.

As noted previously, upon the occurrence of a DC fault, the diodes in the typical two-level VSC converter would continually feed the fault. In the absence of commercial DC breakers, the lack of control on the DC side would mean that ac breakers would be the only possible mechanism to break the path of the fault current. However, using ac breakers would take longer and also, result in loss of power. It is in this scenario, that alternative topologies were introduced. The Modular Multilevel Converters (MMC) [10] topology, where each module (consisting of individual capacitors and valves) is independently switched in and out, is gaining momentum. The full bridge MMC topology, is popular due to their ability to block DC faults. In [10] the control system of the MMC is also explored. Depending on the number of modules, the sinusoidal wave thus generated, is near ideal, and does not require any filtering.

Capacitor commutated converters (CCC) [30], are a modification of the traditional LCC converters, with added capacitors in each phase, each connected in series between the

converter transformer and the valves. Primarily, this allows for reactive power generation [10] (i.e. four quadrant operation), and also reduces the minimum extinction angle [10] for valves, thus reducing the probability of commutation failures. Recently, there is some renewed interest in the CCC owing to the high installation costs of the VSC and also lack of a DC breaker model, as of yet. But, the over-voltage and protection remains a challenge [10].

In this thesis, the 2-level VSC topology is of primary interest. Thus, the following sections are devoted to elucidating the various components of the VSC HVdc and the common control systems employed.

2.2 VSC: Operation and control

The voltage source converter, generates a controlled sinusoidal ac voltage at the VSC ac terminals, from a DC source [6] [24]. The ac voltage thus generated, is by the controlled switching of self-commutated devices (such as IGBTs, GTO etc.) in the converter. The VSC allows for four-quadrant power operation [24], which means it allows for control of active and reactive power supplied to, or absorbed from the connected ac network.

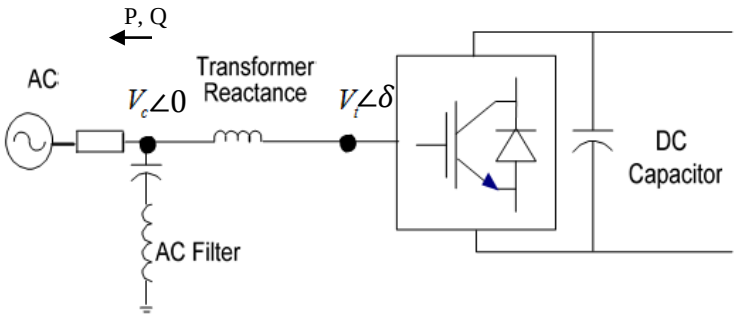

Figure 2- 1 VSC terminal connected to an ac system

Figure 2-1 represents the typical configuration of a VSC connected to an ac system, represented by its Thevenin equivalent. By modulating the magnitude and phase angle of the generated ac voltage at the VSC terminals, V_c, the active (P) and reactive power (Q) output of the VSC are controlled [24] [31], based on equation (2-1) and (2-2).

$$P = \frac{V_t V_c}{X} Sin(\delta) \tag{2-1}$$

$$Q = \frac{V_c^2 - V_t V_c}{X} Cos(\delta) \tag{2-2}$$

Where δ is the phase angle between the fundamental voltages of V_t and V_c,

V_t is the fundamental component of the converter's internal voltage,

V_c is the fundamental component of voltage at the ac filter bus,

X is the combined reactance of the transformer and the phase reactor.

The line resistance is ignored in these power equations. If the generated ac voltage is greater than the VSC terminal voltage, then reactive power is fed to the ac system (and vice versa). Further, if the phase angle of the generated voltage leads that of the VSC terminals, active power is then supplied to the ac system (and vice versa).

Power reversal in VSC systems is accomplished by reversing the DC current, while keeping the voltage polarity constant. Self-commutating switches such as IGBTs, are capable of high-frequency switching, and hence can generate precise, high quality ac waveforms, of the desired magnitude, phase & frequency. Figure 2-2 shows the schematic depicting the basic anatomy of a two terminal VSC HVdc system. In the following section, the various components in a VSC HVdc system are explained, in some detail.

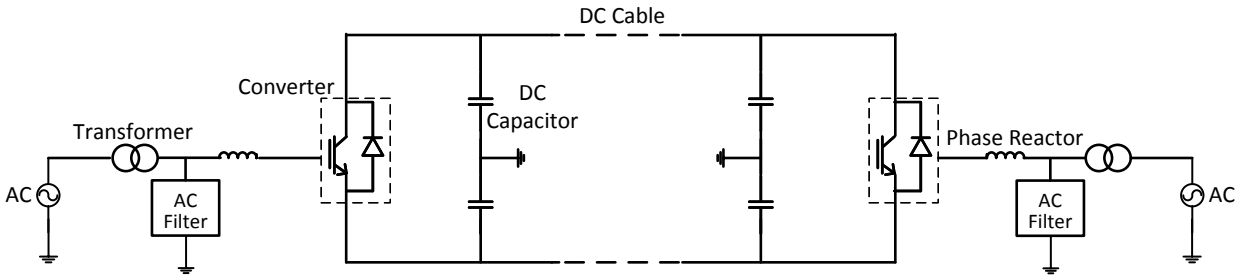

Figure 2- 2 Schematic of a two-terminal VSC system

2.2.1 Components of the VSC HVdc system:

Referring to Figure 2-2, the main components of a VSC HVdc system are as follows:

- DC Capacitor
- Converter Bridges
- Phase Reactor
- Converter Transformer
- ac filters
- DC Cables/OH lines

DC Capacitor:

The main purpose of the DC capacitor is to store energy to reduce the ripple in the DC voltage. Additionally, the capacitor forms the low inductive path for the turn-off current [24]. The size of the DC capacitor (C_{dc}) is dependent on the DC voltage rating and would in turn determine its immunity to voltage transients due to disturbances in the ac system.

The response of the DC capacitor in general, is characterized by its "time constant". The time constant (typically $\approx 5ms$) is proportional to the size of the capacitor, implying that a

larger capacitance would result in slower dynamics, and vice versa. The time constant (τ) of the capacitor (C_{dc}) is defined in equation (2-3) [17].

$$\tau = \frac{0.5 C_{dc} V_{dc}^2}{S_N} \tag{2-3}$$

Where, V_{dc} : Rated DC voltage

S_N : Nominal Apparent Power of the converter.

Converter Bridge:

Each valve of the VSC consists of an IGBT connected with the freewheeling diode in anti-parallel. Depending on the rating, many individual switches are connected in series so as to withstand higher voltages, thereby, also reducing the reverse blocking voltage of each IGBT [24]. The anti-parallel freewheeling diode forms the path for the current in the reverse direction. The switching frequency of the IGBTs are typically in the order of a few kHz. The topology of the basic 2-level converter is shown in Figure 2-3. As the number of voltage levels in the converter is increased, the generated ac voltage approaches the pure sine wave. Thus, with the increase in the levels of the converter, the filtering required at the ac bus reduces. The 2-level converter topology is the most basic module, with two voltage levels: $+V_{dc}/2 \ and - V_{dc}/2$ [10]. The 3-level converter with the clamped neutral [32], has three voltage levels: $+V_{dc}/2\,, 0 \ and \ -V_{dc}/2$, and so on. Generating voltage levels greater than three, result in very complex converter topologies, and are hence not recommended [10].

The Modular Multilevel converter (MMC) topology [10] uses the concept of dividing the converter into smaller modules (of full bridge or half bridge topology), each consisting of its own capacitor. Depending on the control signals generated, in order to track the reference sinusoidal waveforms, the modules are switched in and out, thus creating incremental steps,

which connected in series form the resultant ac output waveform [10]. With the MMCs, it is possible to generate near perfect sinusoidal ac waveforms, with no need for filtering. The external controls that develop the voltage orders for the MMC and the two level VSC are identical. However, the internal control system for the VSC with the MMC topology are very different from the traditional two- or three-level VSC, since factors such as the voltage balancing of the capacitors in each phase ought to be taken into consideration.

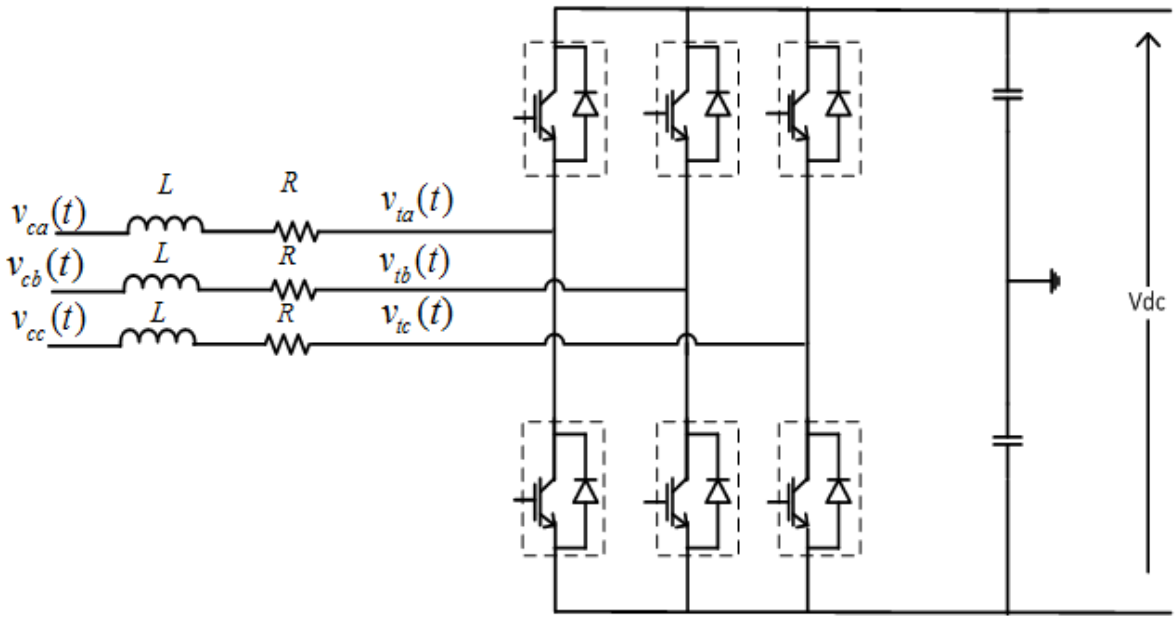

Figure 2- 3 Two-level converter topology

Phase Reactor:

The phase reactor (component of '*X*') is crucial in the control of the active and reactive power control, as seen in equation (2-1) and (2-2). Additionally, this reactance provides a large impedance path for the high-frequency current harmonic components introduced due to PWM (explained in Section 2.2.2).

Converter Transformer:

The transformer is useful in transforming the ac side system voltage to a suitable value for the converter. The type of transformer winding connections would determine the dynamics of the transformer [17]. The combined reactance of the transformer and the phase reactor is typically about *0.3 pu*.

ac Filters:

The ac filters which act as high pass filters (or tuned filters), remove the higher order voltage harmonics in the waveforms generated by the PWM [25]. Considering that the PWM switching frequencies are selected to be an integral multiple of the fundamental frequency, the cut-off frequency (or the tuned frequency) of the filters are quite high. The analysis of the harmonic content of the PWM generated waveforms is explained in detail in Section 2.2.2.

HVdc Transmission Lines/Cables:

For long distance bulk transmission of power, transmission lines or cables are used. Since ground return is possible for HVdc, installation costs can be further reduced [24]. Further, the undersea cables form the backbone to connect two networks separated by large water bodies. HVdc cables thus facilitate the power exchange between such networks.

2.2.2 Pulse width modulation

Pulse width modulation (PWM) is the controlled switching of the IGBT valves to generate a switched (pulse) waveform, to reproduce the reference voltages at the terminals of the VSC [25]. The most commonly employed method is the Sinusoidal PWM (SPWM). Other approaches include the CRPWM [33], OPWM [34] etc. Using the modulation index (m), phase angle (δ) and the frequency (f_s) as in equation (2-4) and (2-5), the three phase *reference* signal is generated. In each phase, this reference signal is compared against the *carrier*

waveform, which is typically a triangular waveform (with frequency: f_c). The output, from this modulation, provides the switching pulses for the valves in each converter leg.

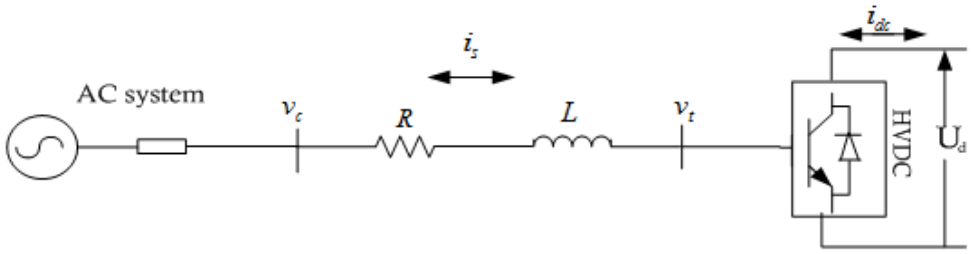

Figure 2- 4 Equivalent circuit of the single terminal system, neglecting the ac filter

The ratio of the frequency of the carrier wave with that of the reference wave is termed as the frequency modulation ratio (m_f):

$$m_f = \frac{f_c}{f_s} \tag{2-4}$$

The Figure 2-4 shows the equivalent circuit for the single terminal system. The generated voltage waveform (V_t) has the fundamental component as defined in equation (2-5). The Figure 2-5, is the block diagram of the generation of the ac voltage waveform the *dq*-components of the voltage.

$$V_t = m * Sin(\omega t + \delta) \tag{2-5}$$

Where *m*: Modulation index

δ: Phase angle of voltage

ω: Frequency of the sinusoidal waveform.

By controlling the modulation index & the phase angle of voltage, as explained in Section 2.2, it is possible to control the reactive power & the active power supplied to/from the VSC terminals, respectively.

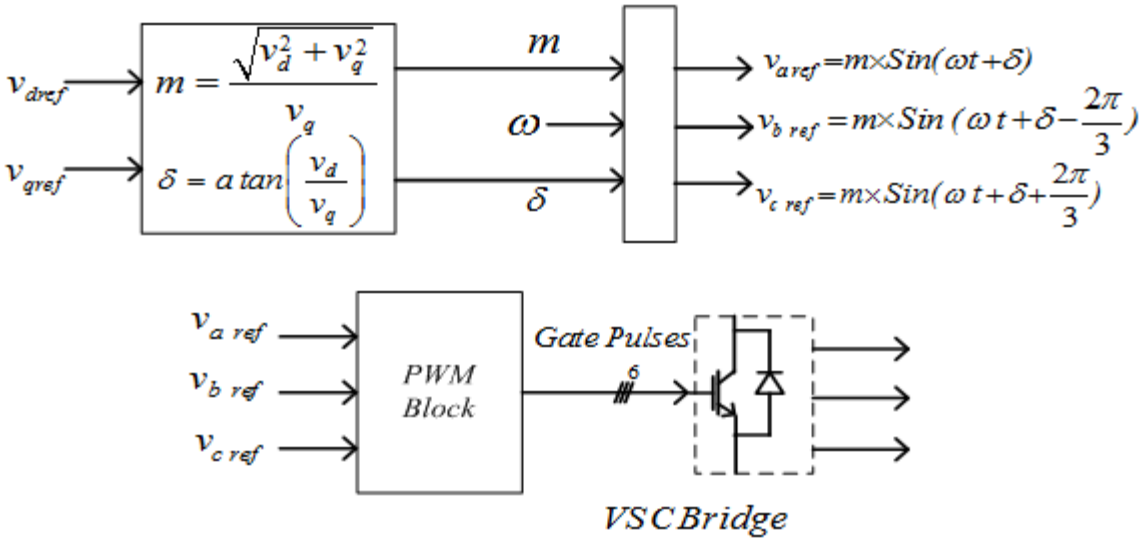

Figure 2- 5 Generation of reference waveforms

Generally, the converter control system generates orders for the direct and quadrature component (v_{dref} and v_{qref}) of the ac voltage which can be considered as the magnitudes of the VSC voltage component in phase and in quadrature with the ac bus bar.

With SPWM, when the modulation index (m), is less than unity, the frequency spectrum of the generated voltage at the VSC terminals, contains harmonics at: ($k * f_c \pm p * f_s$) [25]. Where, *k* and *p* are integers, such that, if *k* is even, *p* is odd and vice versa. Figure 2-6 shows the frequency spectrum of the pulse width modulated waveforms.

Although, at higher switching frequencies, the harmonic content in the voltage is reduced, the switching losses are high. Therefore, a suitable value of m_f, which forms as a tradeoff between these two is selected. In addition, it is recommended to select a frequency which is $3n$ times the fundamental to eliminate the zero sequence harmonics, if any [25]. Also, the due to symmetry considerations, the m_f is recommended to be an odd number.

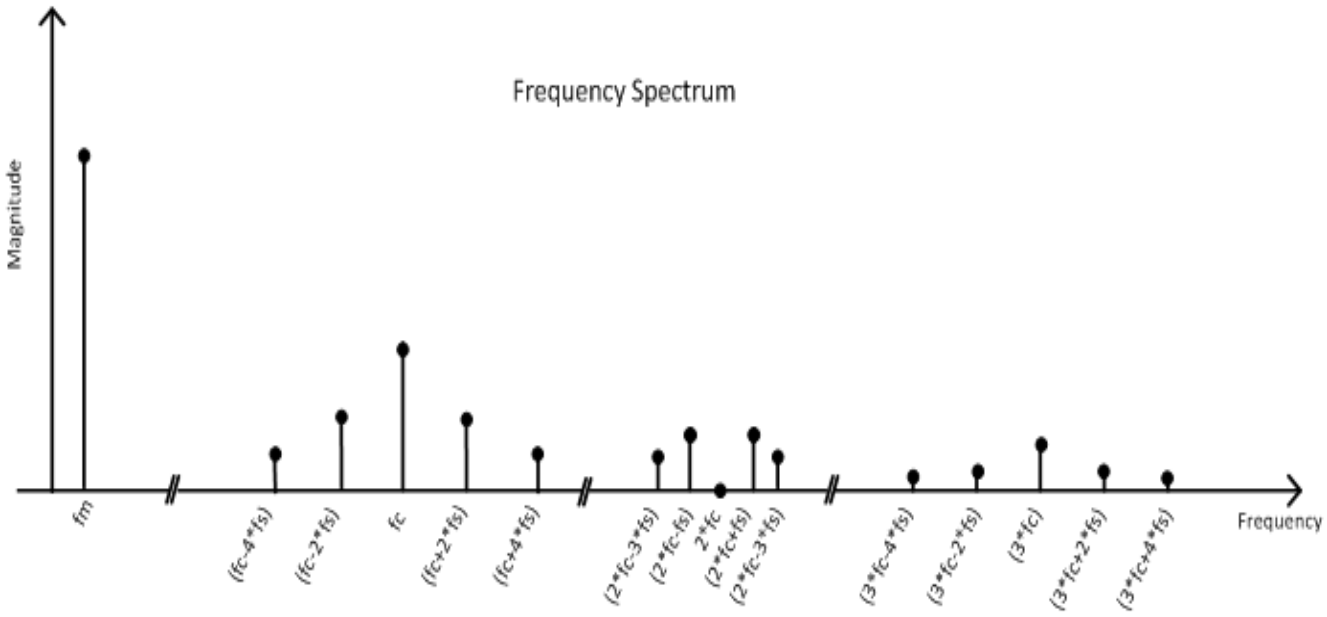

Figure 2- 6 Frequency spectrum of the pulse width modulated waveform [25]

The output of the VSC control system, are the *dq*-components of the reference voltage, i.e. v_d and v_q.

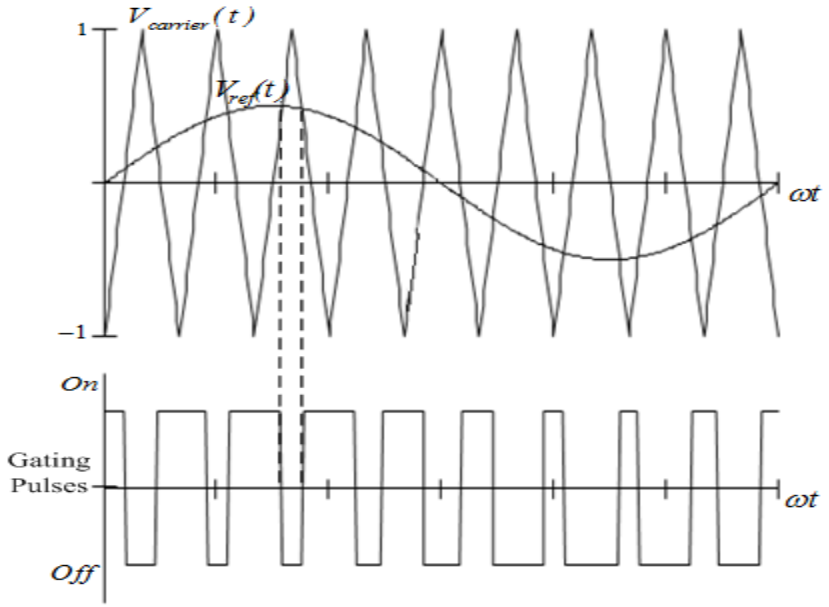

Figure 2- 7 Generation of gating pulses for IGBT valves [taken by permission from HVdc course notes of Dr. A. M. Gole]

The gating pulses for each leg of the converter are generated, as shown in the above figure (Figure 2-7), are provided to the IGBT valves in each phase. In Section 2.3, the commonly used approaches for the VSC control system are explained.

2.2.3 Capability curves for VSC:

The VSC can operate in all four power quadrants, allowing for the supply/absorption of the active and reactive power to/from the ac system it is connected to. As with any practical device, there are limitations to the operating range of the VSC. These constraints are essentially depicted by the Capability Curves of the VSC. The capability curves (Figure 2-8), therefore, show the confines within which the VSC operates.

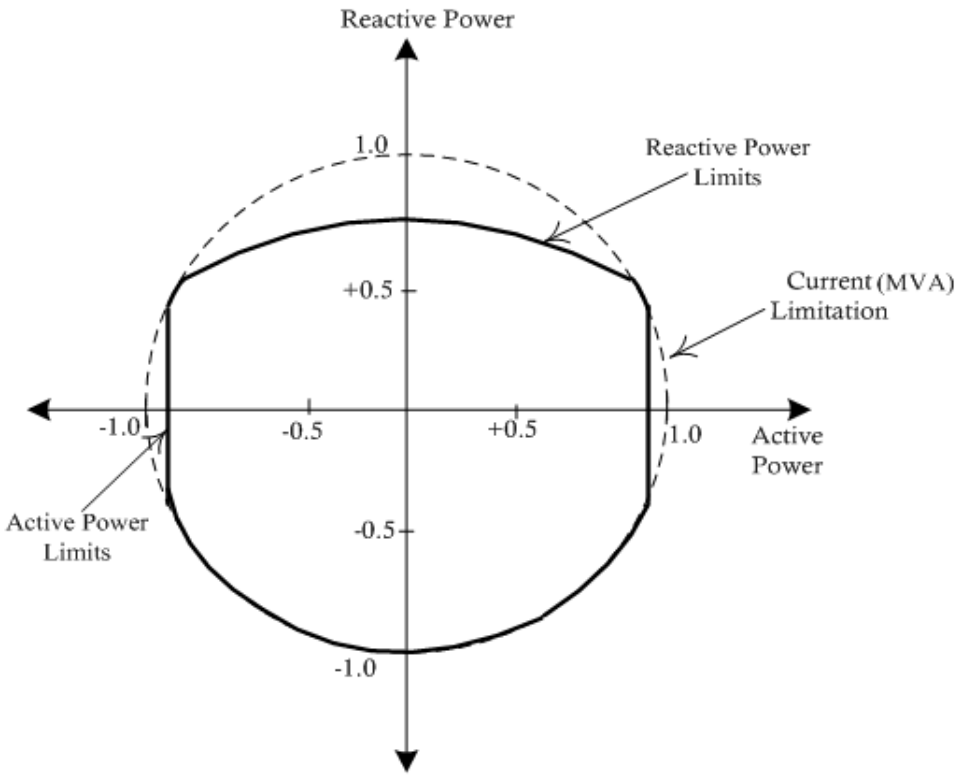

Figure 2- 8 Capability curve for the VSC [35]

The following are the limits imposed on the VSC operation based on the ratings of the converter and the ac system it is connected to [35]:

1. MVA limitation: The limitation in terms of the maximum permissible current through the IGBT valves, determines the maximum MVA the VSC can supply to the ac system. The resultant circle, as shown in Figure 2-8, is the product of the maximum permissible current and the actual ac voltage.

2. Maximum DC current: The active power limits of the converter are limited by the maximum permissible DC current. This limit of the maximum active power that can be supplied by the VSC, manifests itself as a vertical line in the PQ plane, as shown in Figure 2-8. Depending on the magnitude of the DC voltage, these limits may or may not intersect the maximum MVA circle.

3. Reactive Power Limits: The maximum permissible reactive power that can be supplied by the VSC, is dictated by the limits of the maximum voltage that the VSC can generate at the terminals. The reactive power limit is obtained by solving the expression for Q as defined in Section 2.2. The resultant solution is a circle centered at $(0, -V^2/X)$ in the PQ plane, Figure 2-8. The variation of the ac voltage with respect to the constant DC voltage would result in a change in the radius of the circle.

2.3 Control system for the VSC

Selecting an optimal structure as well as the parameters for the VSC control system is very important. In simple terms, the VSC control system is a non-linear, coupled, double input double output system [36]. The accuracy with which the actual system dynamics are modeled in the control system, would largely determine its efficacy.

The following sections are devoted to the two existing control methodologies, namely:

1. Power Angle control

2. Vector Current control

In Power Angle control approach [37], the non-linear, analytical equations for active and reactive power with the power orders, are used to directly compute the modulation index (m) and the phase angle (δ) of the reference voltage. The active power & reactive power are the *controlled* variables, and the modulation index and the phase angle of voltage are the *controlling* variables. The non-linear equations relating the controlled and the controlling variables form the basis of this approach (as explained in Section 2.3.2). Although the method is simple & efficient, the main shortcoming is that, in this approach, the valve currents are not limited [36]. Therefore, under faulted conditions, for instance, limiting the over-currents would prove to be a challenge.

In contrast, the vector current control or *dq*-decoupled control [24] [38], is a current control method. In this approach, the power control loops (P and Q) are independently controlled by the d and q-components of current, respectively. The control system is designed so as to allow for the independent control of the power control loops.

In literature, alternative methods of control can be found, such as the Power Synchronization Loop (PSL) [39] and predictive methods, as in [40], but are not discussed here. In this thesis, the vector current control approach has been used, which is the most common.

2.3.1 Vector current control:

The vector control method, allows for the independent control of the active (P) and reactive power (Q), by controlling the d and q-components of current, respectively. These controlled currents, are thereafter used to determine the magnitude and phase angle (using m and δ) of the converter's internal voltage. Based in the SRF (synchronous reference frame) domain, the

vector control approach depends substantially on the continuous synchronization of the reference *d*-axis with the filter ac bus voltage. In order to do so, Phase Locked Loops are used.

Consider the simplified network as shown in Figure 2-9.

Using the same notation as in equation (2-1) and (2-2), assuming the line resistance (R) and line inductance (L), to be equal for all phases, equation (2-6) is obtained.

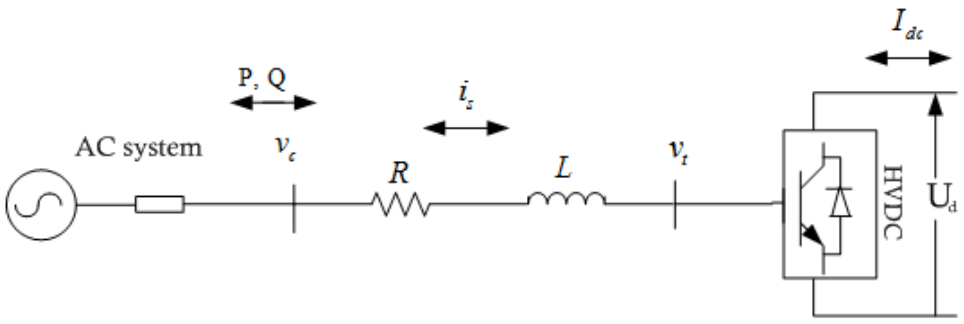

Figure 2- 9 Simplified single line diagram of the HVdc system

$$L\frac{di_{sn}}{dt} + Ri_{sn} = v_{tn} - v_{cn} \tag{2-6}$$

For n=a,b,c, corresponding to each phase.

Upon using the Park's transformation (equation (2-8)), the above voltage equations are transformed to the synchronous domain, using the transformation angle (θ) at the ac filter bus.

$$\begin{bmatrix} f_d(t) \\ f_q(t) \end{bmatrix} = \frac{2}{3}T(\theta)\begin{bmatrix} f_a(t) \\ f_b(t) \\ f_c(t) \end{bmatrix} \tag{2-7}$$

$$T(\theta) = \begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ sin(\theta) & sin(\theta - \frac{2\pi}{3}) & sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \tag{2-8}$$

The *dq*-transformed voltage equations, thus obtained are as follows:

$$L\frac{d}{dt}i_q = \omega L i_d - Ri_q + v_{tq} - v_{cq}$$
$$L\frac{d}{dt}i_d = \omega L i_q - Ri_d + v_{td} - v_{cd} \quad (2\text{-}9)$$

The overall control system can be divided into the *outer control* and *inner current control loops*, connected in cascade. The outer control loops provide the desired reference currents as inputs to the inner current control loops. Depending on the control objective at the concerned VSC terminal, the outer loop controls are selected. The output of the inner current control loop is the VSC's internal voltage in the *dq*-domain, which would further, provide the *m* and δ, for the PWM.

2.3.1.1 Inner Current Control Loop:

Primarily, the inner current control constitutes the control system design, which takes into account the network equations, to determine the desired terminal voltage, which would exist, when the desired "*reference*" currents flow through the phase reactor. Therefore, reiterating the point that the efficacy of the control system indeed depends on the accuracy of the network model.

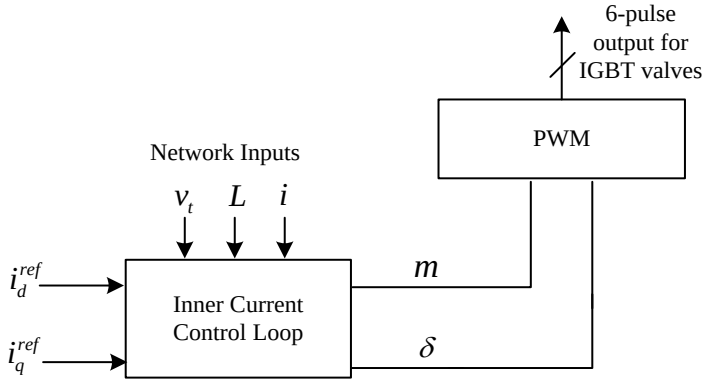

Figure 2- 10 Conceptual Block diagram of the Inner current control loop

With the reference currents (i_d^{ref} & i_q^{ref}) as the input, the *inner current control loop* provides the mechanism to determine the reference voltage, as shown in Figure 2-10. In order to facilitate the decoupling of i_q & i_d control loops, Schauder et al. in [40], proposed the 'Inverter type 1' control system, which has been described above as the Vector Current control method.

In the following section, the inner loop control system of the VSC is developed. From the equation (2-9), the cross coupling between *dq*-equations is evident, due to the presence of the terms, "$\omega L i_d$" & "$\omega L i_q$" in the equations for i_q & i_d, respectively.

The equation (2-9) is rewritten in the matrix form as follows:

$$L\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} R & -\omega L \\ \omega L & R \end{bmatrix}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} v_{td} - v_{cd} \\ v_{tq} - v_{cq} \end{bmatrix} \tag{2-10}$$

From equation (2-10), the converter's internal voltages v_{td} & v_{tq} can be controlled as per equation (2-11).

$$\begin{aligned} v_{td} &= x_1 + v_{cd} - \omega L i_{sq} \\ v_{tq} &= x_2 + v_{cq} + \omega L i_{sd} \end{aligned} \tag{2-11}$$

Upon substituting for the controlled voltages, into equation (2-10), the decoupled control for i_d & i_q, are obtained as shown in equation (2-12).

$$L\frac{d}{dt}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} + \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix}\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{2-12}$$

It is evident from this equation, that a change in control input x_1, would result in a change in only i_d, and to the same effect, a change in $x_2$would cause a change in i_q alone. Subsequently, the control system design can be concluded by defining x_1 and x_2 as follows:

$$x_1 = \left(K_P + \frac{K_i}{s}\right)\left(i_d^* - i_d\right)$$
$$x_2 = \left(K_P + \frac{K_i}{s}\right)\left(i_q^* - i_q\right) \quad (2\text{-}13)$$

The resultant control system, based on these equations, is shown in Figure 2-11. The VSC terminal reference voltages, thus obtained, i.e. v_{td} & v_{tq}, are used to calculate the modulation index and phase angle, which form the input for the PWM block, computed using equation (2-14).

$$m = \frac{\sqrt{v_{td}^2 + v_{tq}^2}}{v_{tq}}$$
$$\delta = \tan^{-1}\left(\frac{v_{tq}}{v_{td}}\right) \quad (2\text{-}14)$$

Here v_{cd} and v_{cq}, are *dq*-components of the voltage measured at the ac filter bus. The delay due to this measurement is represented by the transfer function $H_{LPF}(s) = 1/(1+s\tau)$; where τ tis a measurement related delay. The combined control system, within the inner current control loop is shown in Figure 2-11.

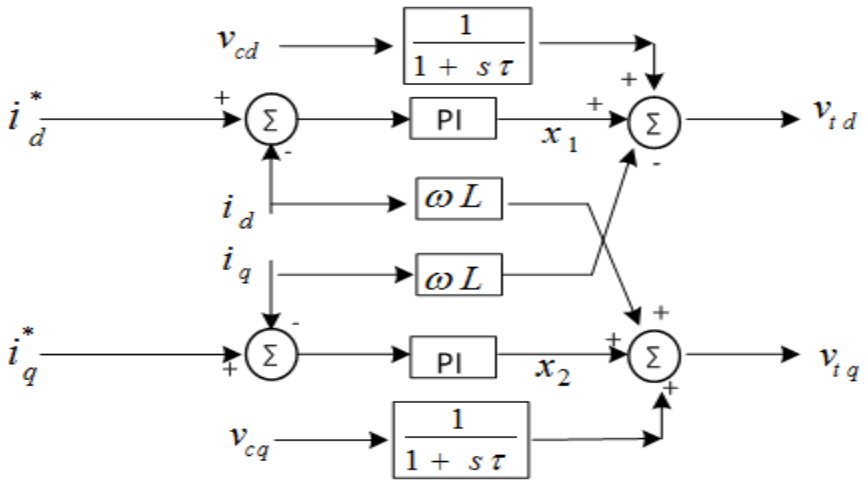

Figure 2- 11 Inner current control of the Vector current control method

The current references, i_d^* and i_q^*, are the output of the outer control loops. The gains of the PI controllers are usually high, since the inner current controller is expected to provide, near instantaneous tracking of the reference currents.

2.3.1.2 Outer Control Loops:

Depending on the ac system parameters and the network operating conditions, typically, the functionality is assigned to the outer control loops. In multi terminal DC (MTDC) systems, for instance, a unique converter (preferably with the highest SCR) is assigned with the task of DC voltage control [11], while the dc voltage at the other converters would be relative to this bus voltage, minus the losses. In this section, a brief analysis of the possible types of outer loop controllers is presented.

In order to better understand the dynamics of the outer loop controls, the equations for *P* and *Q* are linearized [38]. The instantaneous active (P) and reactive power (Q) output at the ac filter bus (Figure 2-9), are defined as follows:

$$\begin{aligned} P &= Re(\, v_t i_s^* \,) \\ Q &= Im(\, v_t i_s^* \,) \end{aligned} \tag{2-15}$$

The following equations are obtained upon transforming the voltages and currents in the *dq*-domain and linearizing equation (2-15) [38].

$$\begin{aligned} \Delta P &= \begin{bmatrix} i_{sd0} \\ i_{sq0} \end{bmatrix}^T \begin{bmatrix} \Delta v_{td} \\ \Delta v_{tq} \end{bmatrix} + \begin{bmatrix} u_{td0} \\ u_{tq0} \end{bmatrix}^T \begin{bmatrix} \Delta i_{sd} \\ \Delta i_{sq} \end{bmatrix} \\ \Delta Q &= \begin{bmatrix} i_{sd0} \\ -i_{sq0} \end{bmatrix}^T \begin{bmatrix} \Delta v_{tq} \\ \Delta v_{td} \end{bmatrix} + \begin{bmatrix} u_{td0} \\ u_{tq0} \end{bmatrix}^T \begin{bmatrix} -\Delta i_{sq} \\ \Delta i_{sd} \end{bmatrix} \end{aligned} \tag{2-16}$$

For a network with stiff ac bus voltage, the change in the bus voltage magnitude is negligible, therefore, it can be assumed that Δv_{tq} and Δv_{td} are both, zero. Hence, equation (2-16) can be rewritten as follows:

$$\Delta P = \begin{bmatrix} u_{td0} \\ u_{tq0} \end{bmatrix}^T \begin{bmatrix} \Delta i_{sd} \\ \Delta i_{sq} \end{bmatrix}$$
$$\Delta Q = \begin{bmatrix} u_{td0} \\ u_{tq0} \end{bmatrix}^T \begin{bmatrix} -\Delta i_{sq} \\ \Delta i_{sd} \end{bmatrix} \quad (2\text{-}17)$$

Also, at steady state, with rated conditions, the *dq*-transformed values of the voltage are: $u_{td0} = 1 \& u_{tq0} = 0$. As a result, the above equation further simplifies to, equation (2-18).

$$\Delta P = \Delta i_{sd}$$
$$\Delta Q = \Delta i_{sq} \quad (2\text{-}18)$$

Accordingly, a change in ΔP would cause a proportional change in Δi_{sd}. And correspondingly, a change in ΔQ would result in a change in Δi_{sq}. These equations form the essence of the design of the outer loop controls.

In this thesis, a single terminal converter system is considered, with active power and ac voltage control. As mentioned previously, only one of the converters should control the dc voltage in the HVdc system. In the system under consideration, the dc voltage control terminal is modeled by a simple DC source, representing an ideal dc voltage controlled converter. In the following sections, though, for the sake of completeness, all possible combinations (including those for dc voltage control) for the outer loop controls of the VSC have been explained.

Active Power Control:

Equation (2-18) depicts the strong coupling between i_{sd} and *P*. To control the active power supplied by the VSC to the ac system, based on the demand (P_{ref}), a simple PI controller structure as shown in Figure 2-12, is used. The output of the PI controller forms the reference current, i_d^*. The instantaneous power is typically filtered (P_s), prior to providing it to the controls.

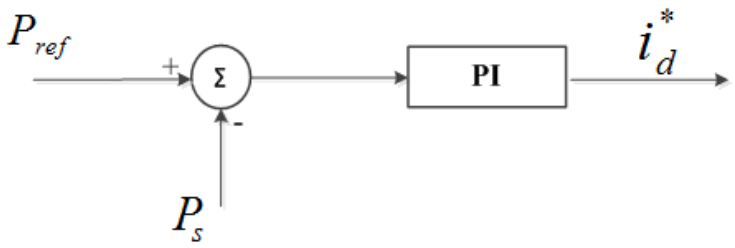

Figure 2- 12 Active power control loop

DC Voltage Control:

In a two-terminal network, one of the converters must have the DC voltage control ability, while the other terminal is made to control the power. In a DC grid, the DC voltage control can only be assigned to one converter. Typically, this converter is chosen to be the one connected to the strongest ac system (i.e. highest SCR), as shown in [11]. The other converters would have a DC voltage which is derived from this terminal, minus the transmission line losses. Thus, to maintain a stable DC voltage across the grid, it is imperative to have a strong ac system connected to the DC controlling converter. Figure 2-13 shows the typical control system to regulate the DC voltage.

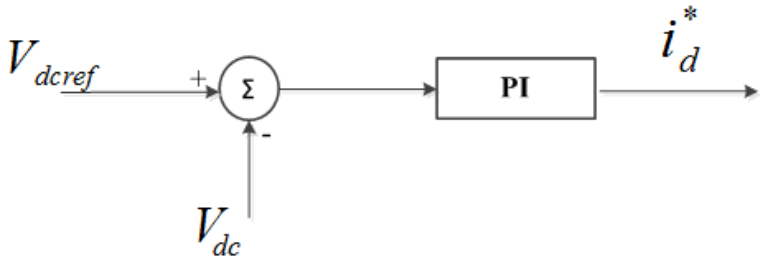

Figure 2- 13 DC voltage control loop

Frequency Control:

Typically used in isolated networks, the frequency control loop provides a mechanism to control the frequency of isolated networks [24] which can be, further, integrated into a larger

network. The control architecture is similar to that of the active power control loop (PI controller), the output of which is the reference current i_d^*.

ac voltage Control:

Controlling the magnitude of the ac voltage at the VSC terminals directly, is essentially a form of the reactive power control. The anatomy of the ac voltage control is as shown in Figure 2-14.

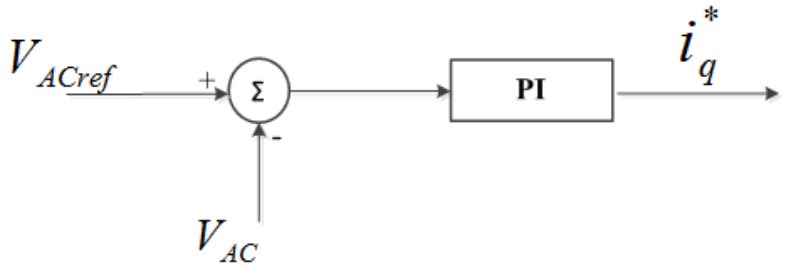

Figure 2- 14 AC voltage control loop

Reactive Power Control:

Controlling the reactive power fed into/out of the ac system is analogous to controlling the ac voltage at the bus terminals. The control architecture for the reactive power control is identical to that of the active power control loop i.e. using PI controllers.

Outer loop control selection for Multi Terminal DC systems:

Some broad paradigms for the design of MTDC systems are listed below:

1. There can only be one converter with DC voltage control [27]. Else, multiple converters would compete with one another, which is not desirable. Although, there can be multiple converters with the dc droop characteristics [5].

2. The DC voltage control terminal cannot regulate power flow and therefore, another converter should be assigned this task. In a two terminal system, both converters cannot have DC voltage control or active power control.

3. In an MTDC system, in case of loss of the DC voltage control converter, a backup converter can be assigned to take over. Which is, in essence, a combination of the Master-Slave approach with the voltage margin method [28] [27] . Borrowing the terminology from communications, typically, the one main converter is referred to as the Master converter and the other converters (slaves), which take over if the Master converter fails to operate for some reason.

4. Intuitively, it makes sense to assign the task of active power control to be assigned to the converter which acts mostly as the inverter. Additionally, if the rectifier end does not have DC voltage control, the risk of DC overvoltage emerges [27]. This might occur in cases when there is load tripping at the inverter end, causing sudden drop in power demand.

Currently, the determination of optimal power flow in MTDC grids [41], [42] remains a topic of interest. Considering the enormous challenges in the solving the non-linearities involved in optimal power flow, there is still a lot of ground to cover. But, new topologies including the Current Flow Controllers [43] are a step in that direction.

2.3.1.3 Phase Locked Loop (PLL):

Phase locked loops provide the phase angle and frequency input of the filter bus voltage to the control system of the VSC. Since with the Vector current control approach, the control systems are largely based in the synchronous (*dq*) domain, the performance of the PLL plays a very crucial role in its operation [44] [11]. In addition, it also provides the reference to the

PWM block, in generating precise gating pulses for the IGBT valves. PLLs are discussed in detail in Chapter 3.

2.3.1.4 Strength of the ac system: Short Circuit Ratio (SCR)

As mentioned previously, the performance of the Vector current control method is dependent on the strength of the system [44] [38], quantized by the SCR.

For a VSC system with rated power of P_{dc} , and rated line to line voltage V_l (Figure 2-15) connected to an ac network with the impedance of Z_s, the Short Circuit ratio (SCR) is defined as the ratio of the SCMVA to P_{dc}, as shown in equation (2-19).

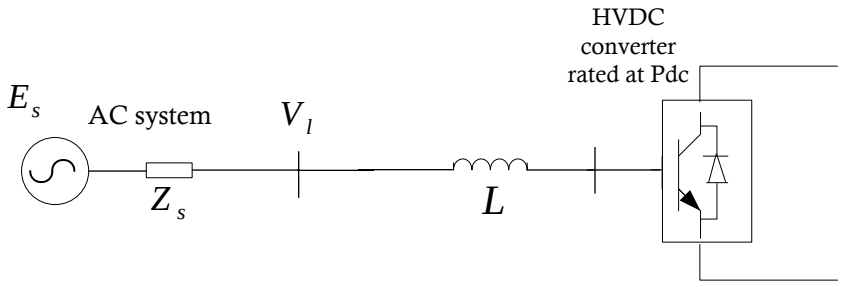

Figure 2- 15 Equivalent representation of the HVdc system

$$SCR = \frac{SCMVA}{P_{dc}} = \frac{\left(V_l^2 \Big/ |Z_s| \right)}{P_{dc}} \tag{2-19}$$

In [11], the limit of SCR=1.6, has been prescribed to be the boundary between *strong* and *weak* systems. The angle of the Thévenin impedance of the equivalent ac system also has a significant impact on the power transmission ability of the VSC, as explained in the later sections. Therefore, the SCR is also represented with this angle.

2.3.2 Power angle control:

The power angle control approach is an alternative approach for VSC controls. Based on the non-linear analytical equations for the active and reactive power [36] derived from equation (2-1) and (2-2), the method is not preferred due to its lack of current controlling ability.

The strong coupling between the δ & P, and, voltage magnitude (m) & Q, form the basic premise of this method. The *controlled* variables (modulation index and phase angle) are computed, using analytical equations, involving the reference values of the *controlling* variables (P and Q). These (computed) controlled variables from the power references, m & δ, and their respective corrective terms Δm & $\Delta\delta$, obtained from the measured (actual) power supplied by the VSC, in combination, result in the final m & δ output [37] [36]. The modulation index and phase angle thus obtained, is provided to the PWM control system.

In addition to the lack of current control, the method is also incapable of damping resonance in the ac system, which can permeate into the DC network [38]. Hence, this method is not commonly used.

2.4 Summary

In this chapter, a comparison between the traditional LCC technology and the VSC is presented. The inner control system of the VSC HVdc and the components in a VSC HVdc system are explained in detail. Two possible control mechanisms for the VSC, namely the power angle control and the vector current control are explored. Further, the crucial concept of the SCR of an ac system has been established. The impact of the SCR on the working of the vector current control method, will be explained in the following chapters.

Chapter 3

Design and Analysis of the Adaptive PLL

With standard Phase Locked Loop (PLL) designs, distortions (such as harmonics, interharmonics, unbalance etc.) in the input voltage, permeate into the phase and frequency outputs of the PLL causing errors. In this Chapter, a new PLL design is developed and introduced to address this problem. The proposed design includes a frequency adaptive 'pre-filter' structure, which extracts the fundamental positive sequence component of the input voltage and hence, mitigates possible distortion errors in the PLL outputs. This adaptive filter changes its parameters according to the measured frequency to always give the designed performance. This is expected to make the dynamic response of the PLL faster than would be possible with a wider band passive filter. Further, the dynamic performance of the PLL is studied and the effect of voltage distortions on the Adaptive PLL is compared with that of the other traditional PLL designs.

3.1 Phase Locked Loops: Background and architecture

In FACTS [6] [45] and HVdc systems [8] [46] [24], Phase Locked Loops (PLLs) provide the reference phase angle and frequency of the ac bus voltage input. In conventional LCC HVdc systems, the PLL provides precise zero crossings for the firing controls of the thyristor

valves [8]. Likewise in FACTS devices, be it the IGBT-based STATCOM [6], or thyristor based SVC [6], they depend on PLLs for accurate tracking of the phase angle of the ac bus voltage at the PCC. These high frequency switching devices can be used for the purpose of providing reactive power support [6] in transmission systems or for end-user power quality conditioning applications such as active filtering [47], load balancing [48] etc.

For a VSC HVdc system with the vector current control approach (Chapter 2), the control system is largely based in the Synchronous reference frame (SRF) domain. Therefore, intuitively, the PLL performance should have a significant impact on the VSC. Also, in networks with high distortion, such as islanded systems or upon the integration of renewable sources such as wind [16], the inclusion of the frequency adaptive characteristic in the PLL design is important. In literature, there are prominent PLL designs such as, the EPLL(Enhanced PLL) in [16] and the DSOGI (Double second order generalized integrator) PLL in [49] which are designed to operate in such networks.

3.1.1 Significance of the PLL in a VSC control system

The vector control method is based on decoupling the control equations in the *dq*-domain, to independently regulate the outer control loops. In essence, provided that the ac bus voltage is stiff, a change in the current reference of i_d cannot introduce a change in i_q, and vice versa [38]. However, in weak ac systems, the ac voltage is prone to disturbances. Consequently, the PLL itself has a hard time following the ac voltage phase in non-stiff systems. Therefore, the performance of the vector control method is in turn dependent on the strength of the system, which is quantized by the SCR (Section 2.3.1).

For a VSC connected into an ac system with high impedance, the voltage at the PCC is prone to disturbances, and no longer stiff. In this scenario, the PLL performance is crucial.

This has been studied in [38] and [11]. In [38], the anatomy of the vector current control method has been explained. In [11], the small signal model of the VSC system, with the inclusion of the PLL, has been developed and stability studies are done thereof. These studies show the significant impact of the PLL parameters on the small signal and transient stability, especially for low SCR systems. In fact, in weak systems the PLL gains are shown to have a higher impact on stability, in comparison with the gains of the inner and outer control loops [11]. It is shown that the traditional PLL designs are not well suited for weak ac systems, considering that for SCR<1.6, they can have a detrimental impact on stability.

The primary objective of this research, therefore, is to design and implement a new PLL design for the VSC control system, to study its impact on stability, especially, when the VSC is connected into very weak ac systems.

3.1.2 Anatomy of typical PLL:

The primary objective of the PLL is to track the frequency and the phase angle of the fundamental positive sequence component of the input voltage. There are several ways to realize this, the most basic design being the d-q-z PLL(or SRF-PLL), which was first proposed by Ainsworth in [46] and further analyzed and EMT validated in [50]. In this section the broad PLL architecture is explored.

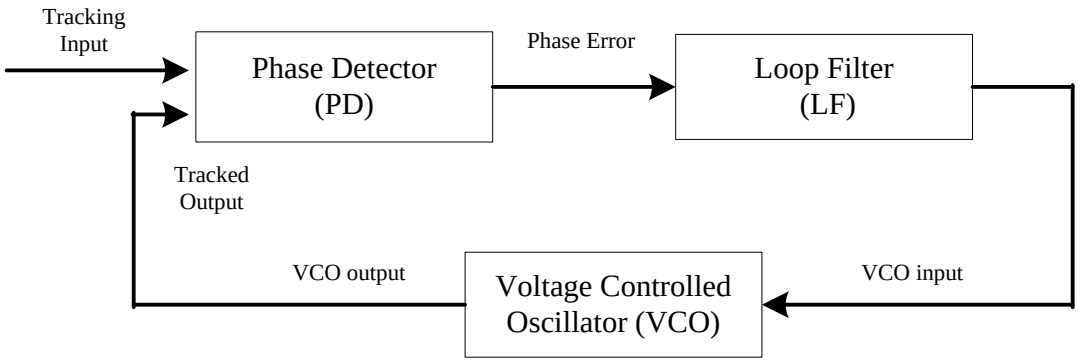

Figure 3- 1 Schematic of a typical Phase Locked Loop [51]

Based on functionality, the PLL architecture can be divided into 3 sections [52] [51] (Figure 3-1):

1. Phase detector (PD)
2. Loop filter (LF)
3. Voltage controlled oscillator (VCO)

The *phase detector* [51] , determines the phase angle error between the voltage input and the PLL output. The implementation of the PD may vary with the design, but essentially, it performs the operation akin to multiplication.

This phase error is passed onto the *loop filter*, which may be a simple PI controller, or alternatively PI controller in conjunction with a LPF, or even higher-order lead lag filters etc. The selection of the Loop filter is based on the desired complexity (in terms of its order) and of course the operating conditions in the network. A higher-order filter design, offers improved accuracy, but affects the dynamic performance adversely. Therefore, the selection of the Loop filter is important.

The output of the loop filter is provided to the *voltage controlled oscillator* (VCO), which generates a periodic signal with a frequency dependent on the VCO input voltage. In a properly working PLL, the output of the loop filter will change so as to eliminate the phase error between the PLL output and that of the input voltage.

In general, every PLL has a *base frequency* which provides the initial output for the PLL. Depending on the "*lock in range*"[52] of the PLL, the output of the PLL eventually locks onto the frequency of the input signal i.e. matches it in frequency and is in phase with it. In power systems, since the range of frequency does not vary significantly, it is presumed that the frequency always falls within this range. If the PLL phase angle is not locked onto that of the

input ac voltage, the phase error is non-zero. In its most basic form, this phase error is passed through a simple PI controller.

3.2 Traditional d-q-z PLL

3.2.1 Architecture:

The architecture of the SRF-PLL is best explained, when correlated with the anatomy of the PLL, as explained in Section 3.1.1 (depicted by the demarcation in Figure 3-2).

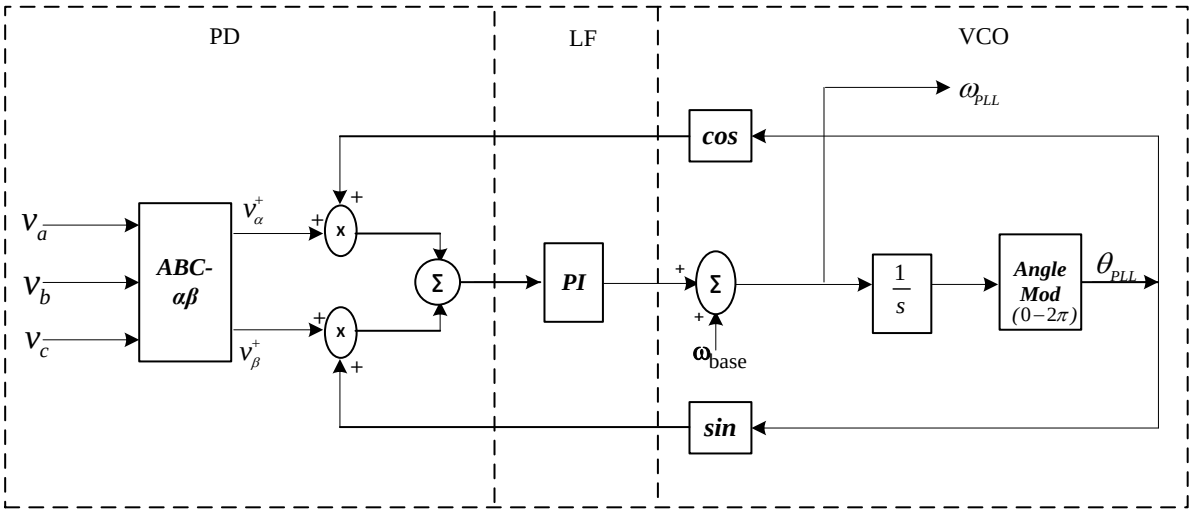

Figure 3- 2 Synchronous Reference Frame PLL (d-q-z PLL) [51]

In the SRF-PLL, the PD transforms the *abc*-components of the input voltage into the Clarkes' components [53] of the voltage (stationary reference frame) (i.e. v_α and v_β). These *αβ*-components are further transformed into the rotating (synchronous) reference frame, *dq*-components. This transformation is based on the angle θ_{PLL}, provided as feedback from the PLL output (in essence, the VCO output). The *d*-component of the voltage is the Phase Error which forms the input to the PI controller (loop filter stage).

The output of this PI controller forms the corrective term for the VCO stage, which is added to the base frequency, ω_{base}. Further, the phase angle is calculated from this corrected

frequency and again provided as feedback to the PD stage. The PLL is perfectly locked, if the *d*-component of the voltage is zero.

3.2.2 Problems with the d-q-z PLL

Under circumstances where there are voltage distortions in the input, the frequency response of the LF block determines the extent of error that propagates into the PLL output [51]. In such a case, the PI controller has a limitation in the range of frequencies it can provide a filtering action for. A filter with lower cut-off frequency (i.e. higher bandwidth) and higher-order, would result in reduced errors in the PLL output. Simultaneously, due to the reduced bandwidth, the overall dynamic response would deteriorate. Therefore, depending on the input voltage distortion, the selection of the LF is a tradeoff between the accuracy and the response time of the PLL.

To understand the extent to which distortions in the input voltage propagate into the PLL output, it is useful to perform an analytical study of the same. This can provide useful insight into the design criterion of the pre-filter structure in the Adaptive PLL. For a given transfer function ($F(s)$) of the Loop Filter block, the error can be calculated analytically, for all distorted voltage conditions, as shown in [51]. Theoretically, the phase error can be calculated as follows [51]:

$$G_f(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{K_d * F(s)}{s + K_d * F(s)} \tag{3-1}$$

Where, $\theta(s)$: Actual phase angle of the input signal

$\hat{\theta}(s)$: Estimated phase angle PLL output

K_d is a constant gain.

This equation is indicative of the relationship between the filtering properties of the *F(s)* block and the errors in the phase and frequency output. Essentially, depending on the type of

voltage distortion, the frequency response i.e. the transfer function of *F(s)* is designed, so as to reduce the errors permeating into the output phase angle. With quantifiable errors, this analysis was used to design the loop filter block in the Adaptive PLL.

3.3 Methodology

In order to mitigate the effect of the input voltage distortions on the PLL output, in this work, a "*pre-filter*" architecture is developed. The inclusion of this pre-filter structure (preceding the SRF-PLL), facilitates the extraction of the fundamental positive sequence of the input voltage, thus providing precise tracking of the phase angle and frequency.

Since the negative sequence component is to be removed, as a first step, the Fortescue's transformation [54] was modified to obtain only the positive sequence component of each individual phase from its fundamental components. Subsequently, this is combined with the Clarke's transformation equations to obtain the final set of equations for the design of the pre-filter.

In the Adaptive PLL, filtering is performed in the stationary reference frame (on the $\alpha\beta$-components). To extract the fundamental component of the $\alpha\beta$-voltage components, which are sinusoidal in nature, an adaptive resonant filter, tuned to the fundamental frequency is used. The analytical derivation of the PLL structure is explained below.

Consider a three-phase input voltage vector: v_{abc}.

For this set of calculations, it is assumed that the input voltage is already filtered and distortion free. The objective, was to extract the positive sequence components from the filtered αβ-components of the voltage. Using the Clarke's transformation, the three phase components are transformed into the $\alpha\beta$-domain, while retaining the original frequency profile of the voltage (excluding the zero sequence).

$$v_{\alpha\beta} = \left[A_{\alpha\beta}\right] * v_{abc}$$
$$\left[A_{\alpha\beta}\right] = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \quad (3\text{-}2)$$

Further, the Fortescue's transformation is modified as follows, to extract the positive sequence component of each individual phase:

$$v^{+}_{abc} = [A] * v_{abc}$$
$$\text{Where } [A] = \frac{1}{3}\begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \quad (3\text{-}3)$$
$$\text{and } a = 1e^{-j120}$$

Upon combining the equations (3-2) and (3-3) , the resultant equation [49] can be obtained in the form of a single transformation (equation 3-4), to extract the positive sequence fundamental *αβ*-components from the fundamental *abc*-components (v_{abcf}).

$$v^{+}_{\alpha\beta} = \left[A_{\alpha\beta}\right] v^{+}_{abc} = \left[A_{\alpha\beta}\right][A] v_{abcf}$$
$$v^{+}_{\alpha\beta} = \left[A_{\alpha\beta}\right][A]\left[A_{\alpha\beta}\right]^{-1} v_{\alpha\beta f} \quad (3\text{-}4)$$
$$= \frac{1}{2}\begin{bmatrix} 1 & -j \\ j & 1 \end{bmatrix} v_{\alpha\beta f}$$

Writing equation (3-4) as separate scalar equations:

$$v^{+}_{\alpha} = 0.5 * \left(v_{\alpha f} - j \cdot v_{\beta f}\right)$$
$$v^{+}_{\beta} = 0.5 * \left(j \cdot v_{\alpha f} + v_{\beta f}\right) \quad (3\text{-}5)$$

From this equation, it is evident that upon linearly combining the fundamental *αβ*-components and their 90^0 phase-shifted counterparts, the fundamental positive sequence component (v^{+}_{α} *and* v^{+}_{β}) of the input voltage is obtained. The combination of the adaptive resonant filter with the equation (3-5), together, form the pre-filter block.

The fundamental positive sequence $\alpha\beta$-components are then transformed to the dq-domain to provide the input to the SRF-PLL block. The following section is devoted to the design of the Adaptive PLL.

3.4 Design of the Adaptive PLL

The Adaptive PLL can be divided into 3 sections based on functionality, namely:

a) Fundamental component filter

b) Positive sequence filter

c) SRF-PLL

Figure 3-3 shows the block diagram representation of the Adaptive PLL. As shown in the figure, essentially, the Fundamental component filter in conjunction with the positive sequence filter block (together comprising the Pre-filter), produce the fundamental positive sequence components to be provided as the input to the SRF-PLL block. The feedback term (ω_{PLL}) depicts the frequency adaptive nature of the PLL.

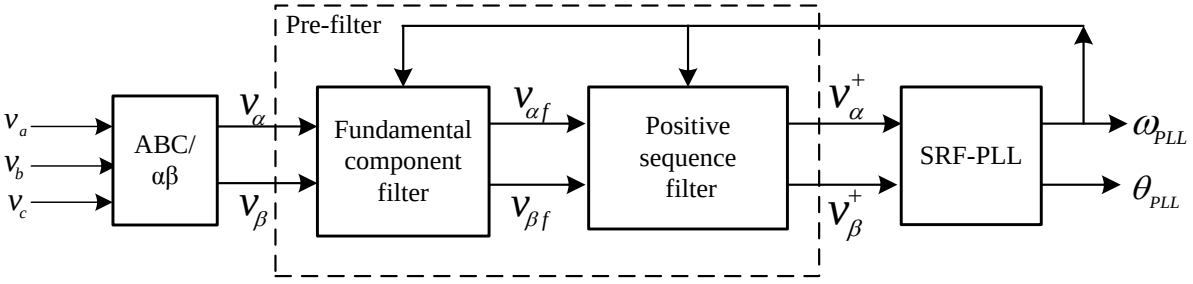

Figure 3- 3 Block diagram of the Adaptive PLL

3.4.1 Fundamental component filter:

The stationary reference frame signals, v_α and v_β, form the input to this block. The objective of the fundamental component filter block is to extract the fundamental component of

v_α and v_β, independently. In this work, it is proposed that the Proportional + Resonant (PR) filter [55] be used. PR filters have complex poles at the resonant frequency and hence, are apt for tracking sinusoidal signals. Also, the frequency adaptive nature for the resonant poles of the PR-filter, are easy to implement. The PR-filters are designed so as to preserve the exact magnitude and phase information of the fundamental component (Figure 3-4).

The transfer function of an ideal PR filter is as follows:

$$H_{AC}(s) = K_p + \frac{2K_i s}{s^2 + \omega_0^2} \tag{3-6}$$

Where $K_P$and K_i are the Proportional and Resonant gains respectively. And ω_0: is the resonant frequency, such that, $\omega_0 = \omega_{PLL}$.

Usually some damping is introduced to improve settling time resulting in a damped filter as in equation (3-7).

$$H_{AC}(s) = K_P + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{3-7}$$

An increase in the cut off frequency (ω_c) would increase the bandwidth of the controller and an increase in the Integral gain (K_i) would improve its harmonic rejection ability (i.e. greater attenuation for frequencies other than the resonant) and vice versa. The selection of the ω_c, however, is a trade-off between the accuracy and the speed of the PLL. Figure 3-4 shows the variation in the frequency response of the PR-filter with changes in the cut-off frequency, and fixed PI gains of $K_P = 1$ and $K_i = 10$.

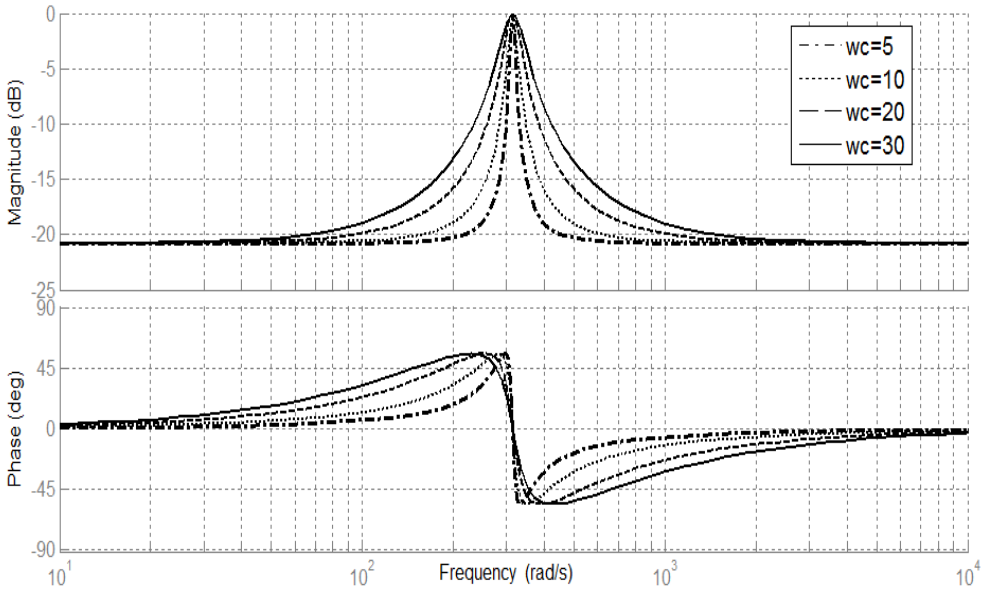

Figure 3- 4 Frequency Response of the Proportional-Resonant (PR) filter with varying cut off frequencies

For the performance analysis of the Adaptive PLL in the further sections, the controller parameters are chosen based on the optimization, explained in Section 3.5.1.

3.4.2 Positive sequence filter:

The output of the positive sequence filter is the fundamental positive sequence component of v_α and v_β signals. In order to obtain the positive sequence component from the fundamental, as shown in equation (3-5), the filtered outputs have to be delayed by a quarter cycle (i.e. 90^0 in the phase domain). This delay can be accomplished in several ways such as using the Hilbert transform [56], integrator [49] etc. The all-pass filter, has a unity gain, but allows for a phase shift of 90^0 at a specific frequency. In this case, this frequency is feedback from the SRF-PLL stage, as shown in Figure 3-5. The all-pass filters [57] are easy to implement with the frequency adaptive nature. In order to make it frequency adaptive, the following transfer function is used:

$$H_j(s) = \frac{-s + w_{PLL}}{s + w_{PLL}} \tag{3-8}$$

Where ω_{PLL}: frequency output from the SRF-PLL stage.

The block diagram of the positive sequence filter is as shown in Figure 3-5.

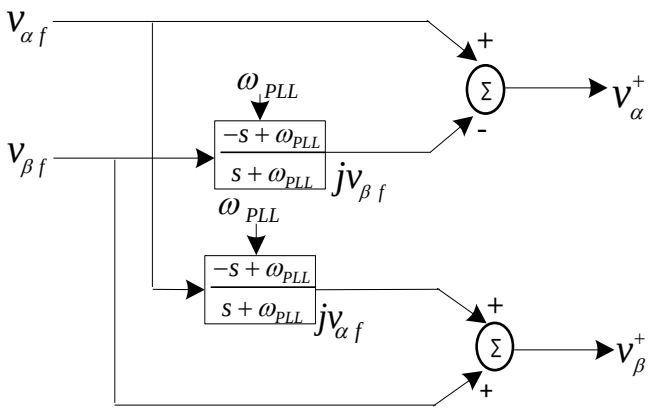

Figure 3- 5 Control system of the positive sequence filter

3.4.3 Synchronous reference frame–PLL (SRF-PLL):

The SRF-PLL structure is as shown in Figure 3-6 and is structurally identical to that of Section 3.2.1. Using the feedback phase angle output of the PLL, the v_{α}^{+} and v_{β}^{+} signals are transformed to the synchronous reference frame. The base frequency of 50Hz is provided for the PLL, and the sum of this base frequency with the output of the PI controller, together, result in the frequency output of the PLL.

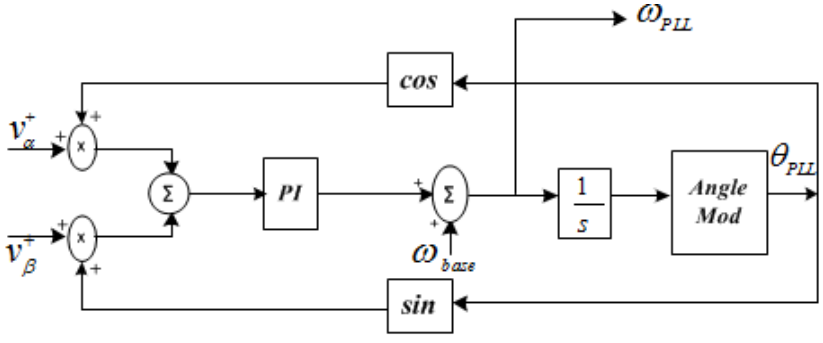

Figure 3- 6 Synchronous reference frame PLL

3.5 Dynamic performance analysis of the Adaptive PLL

3.5.1 Optimization of the PLL parameters:

Prior to studying the dynamic performance of the Adaptive PLL, it is imperative that the PLL parameters be optimized. For this sake, the PLL is modeled in the electromagnetic transient simulation software, PSCAD/EMTDC. The performance of the PLL is compared against that of the standard SRF-PLL, and the SRF-PLL with a basic LPF (SRF-PLL+filter) [51]. The gain values for all the PLLs are optimized using the inbuilt non-linear optimization tool in PSCAD [58] to obtain the best possible dynamic response for a step change in frequency of 1% on the base frequency of 50*Hz* (i.e. 0.5*Hz*). The integral square error (ISE) is used as the error index for optimization and the objective function is formulated as follows.

$$OF_{freq} = \int_{t_1}^{t_2} \left(f_{reference} - f_{actual} \right)^2 dt \tag{3-9}$$

3.5.2 Dynamic response studies and performance analysis under distorted voltage conditions:

3.5.2.1 Frequency Tracking Ability

A disturbance in the form of a 1% step change in frequency is used as the base case for optimization. For the Adaptive PLL, all the variable PLL parameters, including the PR filter and the PI controller parameters are tuned.

Table 3.1 shows the settling times of the respective PLL designs prior to and after optimization. It is evident that with the optimized gains, the settling times reduce significantly.

Table 3. 1 Dynamic Response for 1% step change in frequency

Frequency change:0.5Hz	SRF-PLL	Filter+SRF-PLL	Adaptive PLL
Initial Settling time	300ms	1787ms	1590ms
Optimized Settling time (5%)	33.62ms	54.1ms	36.68ms

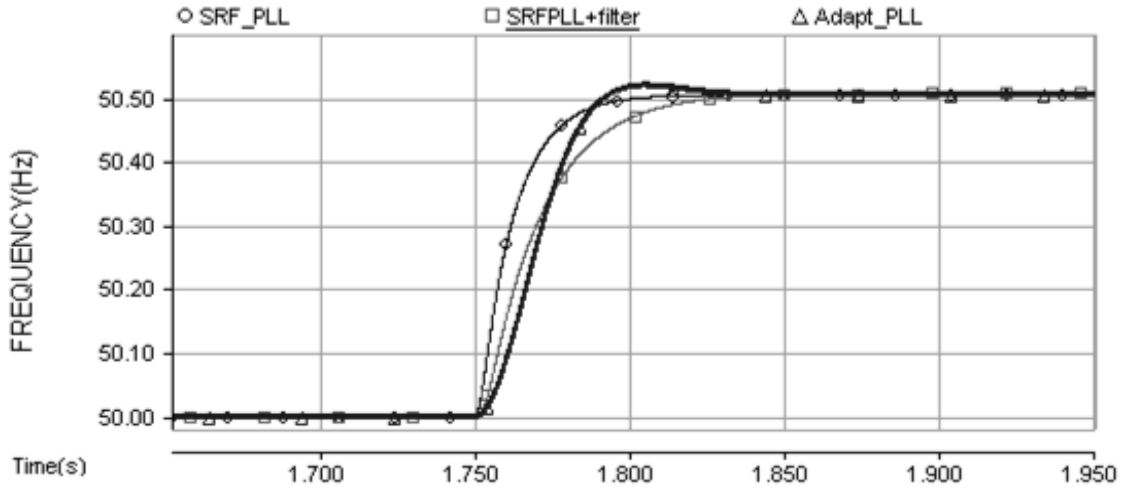

Figure 3- 7 Step change in frequency of 1%

Upon using the optimized gains, for a step change in frequency of 1%, i.e. 0.5Hz, the Adaptive PLL shows a (5%) settling time of approximately 37*ms*, which is comparable to that of the SRF-PLL design. Also, the test satisfactorily demonstrates the frequency adaptive nature of the PR filter and all-pass filter. In contrast, the performance of the SRF-PLL with the filter, is seen to be somewhat sluggish, with settling times up to 54*ms* (Figure 3-7).

The initial and final optimized parameters are given in Table 3.2.

Table 3. 2 Optimized gains for the PLL

SRF-PLL	Initial parameters	Optimized parameters
K_{PSRF}	10	88.9149
K_{iSRF}	20	63.56

SRF-PLL+Filter with ω_{cLPF}=15rad/s	Initial parameters	Optimized parameters
K_{PSRF}	10	88.9149
K_{iSRF}	20	63.56

Adaptive PLL	Initial parameters	Optimized parameters
K_{PSRF}	10	100
K_{iSRF}	20	51.2486
ω_c (rad/s)	25	150
K_{iPR}	2.7991	0.93
K_{pPR}	0.069978	0.069978

3.5.2.2 Phase Tracking Ability

The phase tracking ability of the PLL designs are studied upon using the optimized gains. A sudden step change of 50° is made to the phase angle of the input voltage, and from the Figure 3-8, the settling times are compared in Table 3.3.

Table 3. 3 Dynamic Response for 50° step change in phase angle

Phase change : 50^0	SRF-PLL	Filter+SRF-PLL	Adaptive PLL
Settling time (5%)	33.1ms	43ms	31.4ms

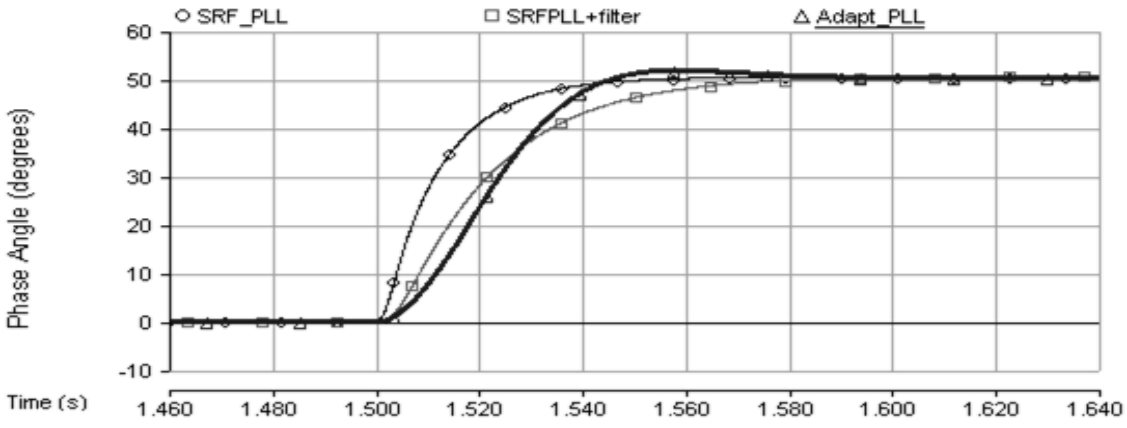

Figure 3- 8 Step change in Phase angle of 50°

The settling times for the SRF-PLL and the Adaptive PLL are somewhat similar, with negligible overshoots. The SRF-PLL with filter on the other hand, has an overdamped response with comparatively slower performance with a settling time of 43*ms*.

3.5.2.3 PLL Performance with Unbalanced Voltages

Unbalance in the input voltage appears in the form of a second harmonic component in the synchronous reference frame and therefore, very small bandwidth filter would be needed to prevent it from being transmitted into the frequency output.

With the gains unchanged, a voltage unbalance of 50% is supplied as the input to the PLL to study its immunity to unbalance. Figure 3-9 and Table 3.4 show the response of the PLL in response to this input. Evidently, from Figure 3-9, the voltage unbalance has negligible effect on the Adaptive PLL output. Whereas with the other PLL designs, the 2^{nd} harmonic component permeates through the system, causing a 100*Hz* oscillating component to appear in the frequency output, with errors as shown in Table 3.4. Although the percentage of unbalance is large and can be deemed impractical, the idea is to show the improved performance with the Adaptive PLL even with very high values of voltage unbalance. The peak amplitude of the ripple in frequency measurement around the fundamental (50*Hz*) is taken as a measure of performance for the PLL. The percentage error so calculated is shown in the Table 3.4.

Table 3. 4 Frequency Output for Input with 50% Unbalance

Unbalance :50%	**SRF-PLL**	**Filter+SRF-PLL**	**Adaptive PLL**
Frequency Fluctuations (*Hz*)	57.83-42.97	52.7-47.21	50.0
Per Unitized Frequency	1.156-0.8594	1.054-0.9442	1.0
Errors	15.6%	5.4%	0%
Error oscillations Frequency	100Hz	100Hz	-

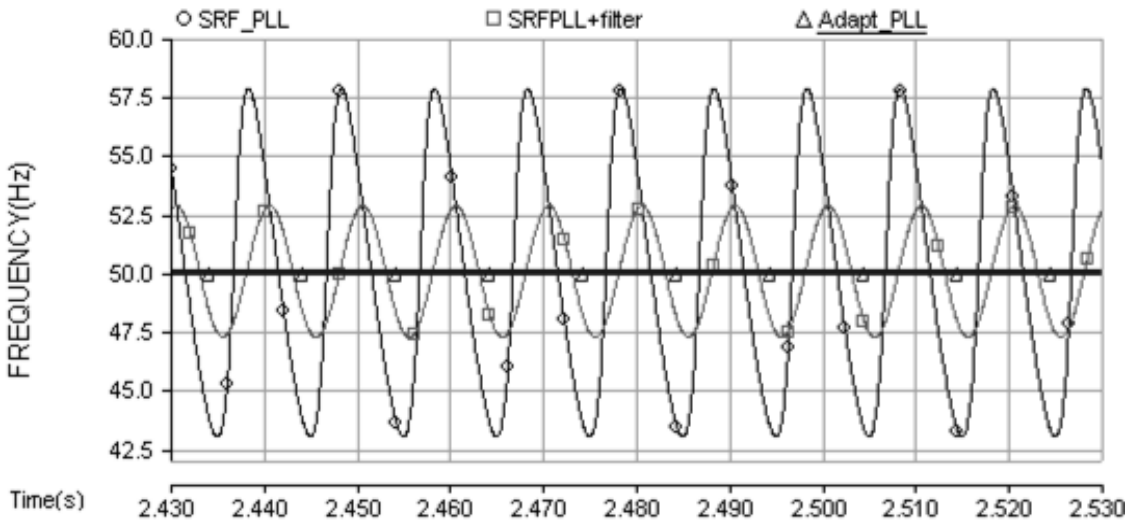

Figure 3- 9 Frequency output of the PLL with 50% Voltage Unbalance in the input

In order to study the effect of voltage unbalance over an entire range, the Figure 3-10 is useful. It is clear that, as the percentage unbalance in the voltage increases, the error percentage also increases, in proportion. The slope of this curve is dependent on the filtering ability of the loop filter block in the PLL structure.

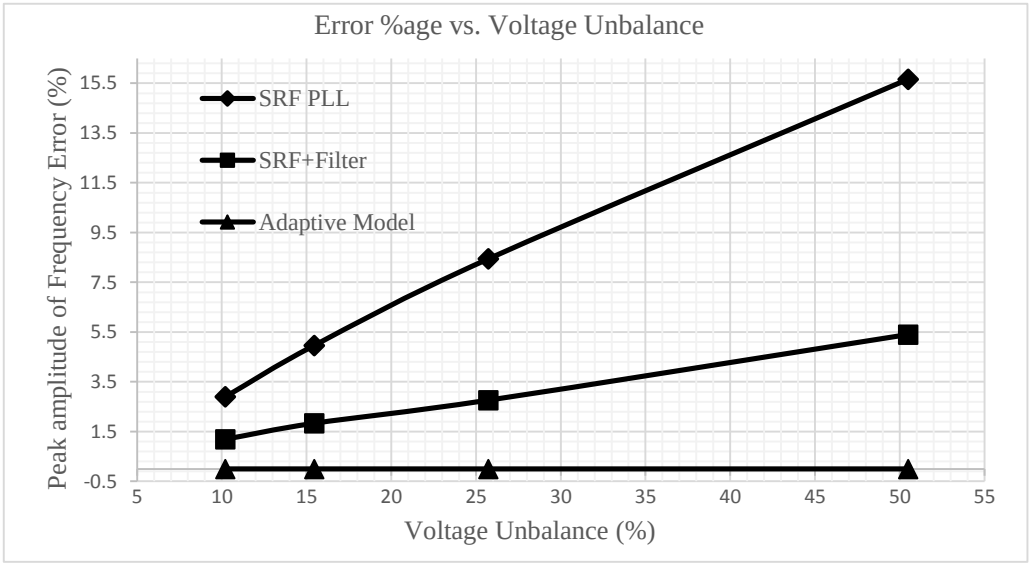

Figure 3- 10 Error Percentage in frequency vs. Percentage unbalance in voltage input

3.5.2.4 PLL performance with Harmonics in input voltage

A n[th]-harmonic frequency component, $n * f_0$, will appear in the SRF domain as $(n-1) * f_0$ or $(n+1) * f_0$ depending on whether it is positive sequence or negative sequence, respectively. In addition, the zero sequence components will have no impact on the output of the PLL. As mentioned in the design section, for the Adaptive PLL, a larger K_i (in the PR filter) would increase the harmonic rejection ability of the PR filter and in turn, in this case, reduce the frequency errors. For the sake of uniformity, though, in this test the optimized gains are used. The PLLs were tested with 5th and 7th harmonic injected into the voltage, as shown in Table 3.5, with a THD of 13.25%.

Table 3. 5 Input Voltage with Harmonic content

Harmonic Order	PU value
1 (50*Hz*)	1 *pu*
5 (250*Hz*)	0.08695 *pu*
7 (350*Hz*)	0.1 *pu*

Theoretically, for the SRF based PLLs, from equation (3-1), the errors seen in the output frequency, are a superposition of the errors due to each of the input harmonics subject to the attenuation due to the filter frequency response [51]. This is validated by the Figure 3-11.

Table 3. 6 Frequency Output for Voltage input with THD=13.25%

Input with harmonics	SRF-PLL	Filter+SRF-PLL	Adaptive PLL
Frequency Fluctuations (*Hz*)	52.6-47.38	50.72-49.27	50.22-49.77
Per Unitized Frequency	1.05-0.95	1.014-0.98	1.004-0.995
Errors	5.2%	1.44%	0.44%
Error oscillations Frequency	300*Hz*	300*Hz*	300*Hz*

For the given set of input harmonics in the test case, the FFT of the frequency outputs show a 300*Hz* component, corresponding to the 6th harmonic, which is on expected lines considering the 5th harmonic is of the negative sequence and the 7th harmonic of the positive sequence.

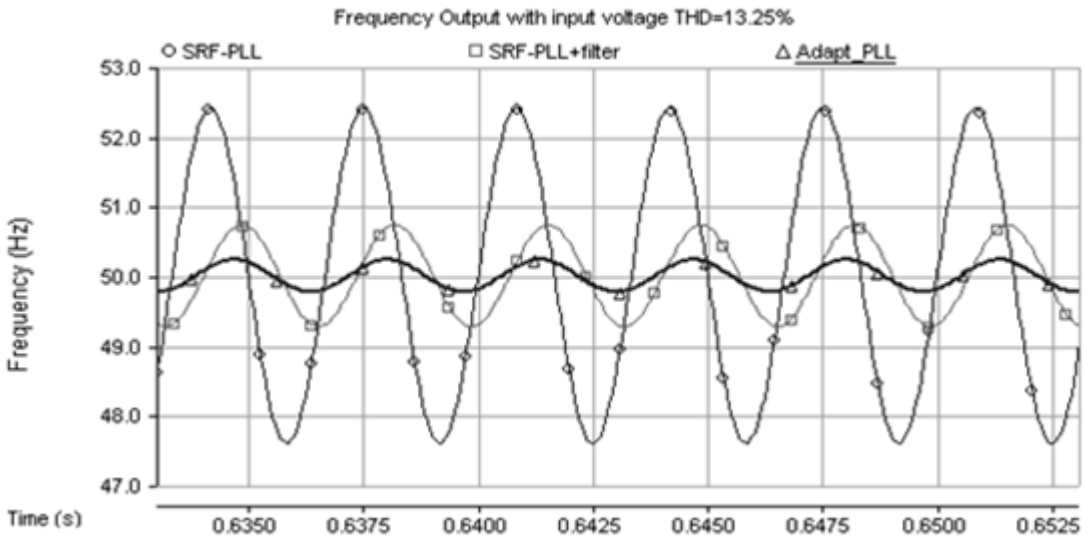

Figure 3- 11 Frequency output of the PLL with input voltage THD=13.25%

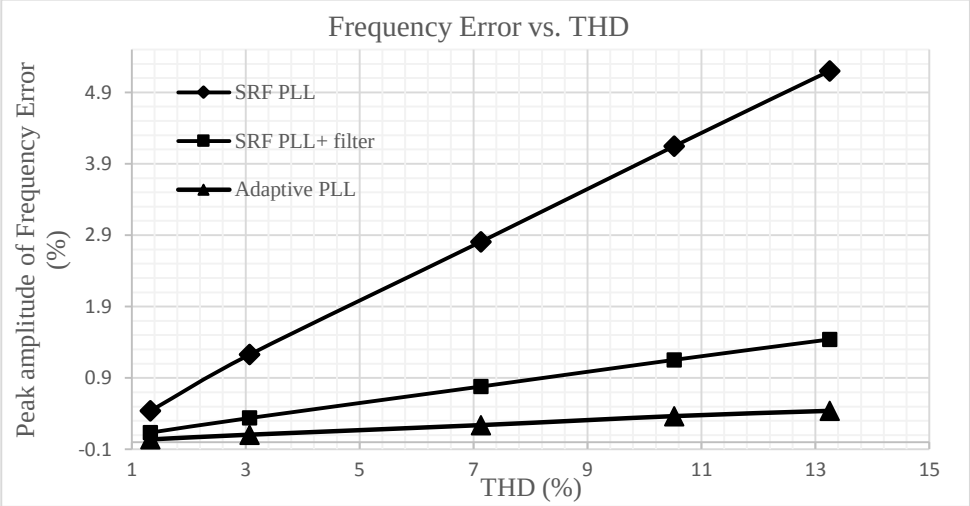

Figure 3- 12 Error percentage in frequency vs. THD of the input voltage

It is evident from the Figure 3-11, that the percentage errors are minimal for the Adaptive PLL compared to the other PLLs. This trend continues for inputs with higher THD, as shown in Figure 3-12.

3.5.2.5 PLL performance with Interharmonics

Although interharmonics are not encountered very often, it is nevertheless important to study their impact on the since some of the PLL designs such as in [45], work poorly in the presence of interharmonics. Mostly because of their dependence on the voltage distortions being an integral multiple of the fundamental. Therefore, it becomes imperative to test the performance of the Adaptive PLL design in the presence of interharmonics.

For the test case, a 120Hz positive sequence interharmonic of magnitude 1% of fundamental is used (results in Figure 3-13). The results for the various designs of PLL are as shown in the Table 3.7.

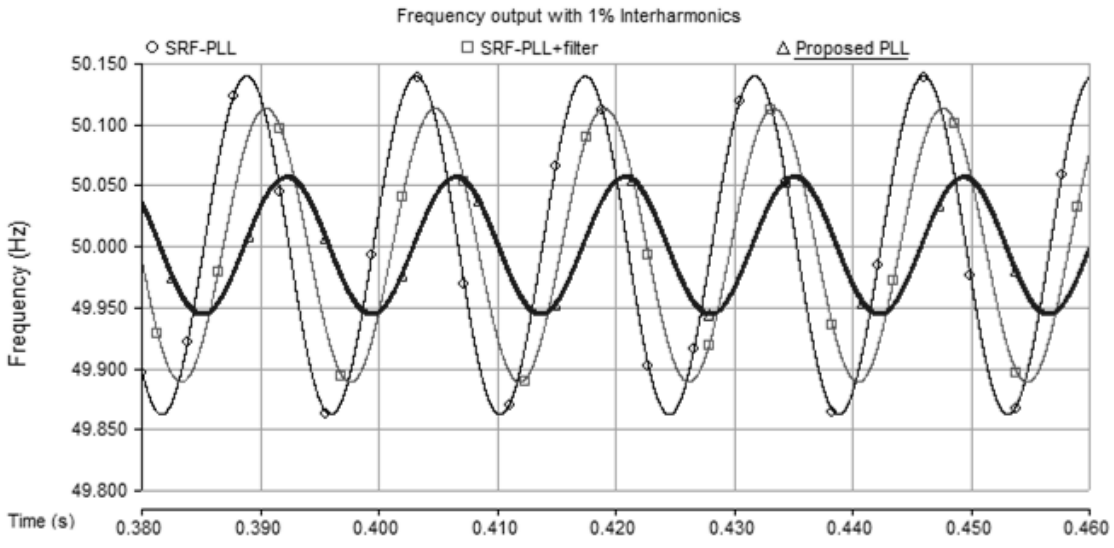

Figure 3- 13 Output frequency with 1% interharmonics of 120Hz in the input voltage

Table 3. 7 Frequency Output for Voltage input with 1% interharmonics

Input with interharmonics	SRF-PLL	Filter+SRF-PLL	Adaptive PLL
Frequency Fluctuations (*Hz*)	50.12-49.8791	50.097-49.9	50.049-49.95
Per Unitized Frequency	1.0024-0.9975	1.00194-0.998	1.0009-0.999
Errors	0.24%	0.194%	0.098%
Error oscillations Frequency	70*Hz*	70*Hz*	70*Hz*

The results are on expected lines, considering the frequency response characteristics of each the designs. It can be inferred that the Adaptive PLL has the least frequency errors.

3.6 Summary

In this Chapter, a novel Adaptive PLL design is introduced. The methodology and design of this PLL is explained. Thereafter, the dynamic performance of this PLL is tested and proven to be satisfactory. Further, the performance of the PLL in the presence of the input voltage distortions, is compared with other existing topologies. It is concluded that the Adaptive PLL shows good immunity to these distortions, hence resulting in significantly reduced errors in the PLL output. Therefore, the overall performance of the PLL in presence of voltage distortions can be deemed satisfactory. In the next few chapters, the effect that this Adaptive PLL design has on the VSC performance is studied.

The main difference between the traditional approach of using a filter in the SRF-PLL and using the proposed pre-filter is as follows:

- SRF PLL with filter uses a higher order low pass filter does improve harmonic and unbalance behavior but slows down the dynamic response. Upon trying to improve

filtering capability, the dynamic response slows down even further. Hence there is a tradeoff.

- The adaptive filter is designed to filter out precisely the tuned frequency. Rather than make it wide band to cater for frequency variations, it is continuously tuned using the measured PLL frequency. This makes it fast, as its behavior is optimized to the tuned frequency. The frequency feedback is used to continuously tune the filter so that it adapts to frequency changes.

Chapter 4

Optimization of the VSC Controls

The natural corollary of Chapter 3, would be to implement this newly developed PLL structure into the VSC control system and study the implications on the system stability, thereof. Prior to this, in Chapter 4, the controller parameters of the VSC control system have been optimized, so as to provide good dynamic performance. A modified approach for single-converter optimization of the VSC control system is presented, which allows for finer control.

4.1 Introduction and background

Prior to testing the effect of the Adaptive PLL on the stability of the VSC system, it is imperative to compute suitable gains for the VSC control system. The object of the optimization is to obtain gain values for the VSC control system which:

1. Provide stable operation at least up to rated conditions
2. Provide good dynamic response for the given stimulus

In order to obtain the initial set of gains for optimization of the controller gains, at first, the use of the Ziegler-Nichols (ZN) method [57] was examined. The empirical formulae of the ZN method would have formed a good starting point for optimization. Unfortunately, the magnitude of disturbances considered in this case, are not within the prescribed tolerance for

the ZN method, which is typically about 10% [57]. Also, with this approach, for each converter, the controllers would need to be tuned one at a time. This process can be very tedious and time consuming and hence is not recommended. Further, for MTDC systems or DC grids, it would be impossible to do so manually.

In this scenario, the multiple-run feature in PSCAD/EMTDC forms a viable alternative to determine the initial gain values. The multiple-run tool is useful when a simulation is to be repeated several times, with a variation in some of the control parameters. Therefore, this tool is used to obtain the initial set of gains so that the system at least reaches a stable operating point with the initial set points. Once the initial set of gains are obtained, from this point on, the optimization is devised.

In [58], the concept of Optimization Enabled Electromagnetic Transient Simulation (OE-EMTS) was introduced. Previous works, such as in [36], have used the non-linear optimization algorithms to obtain the controller parameters for the VSC. Further, in [11], the concept of single converter relaxation approach is proposed for a multi-terminal VSC HVdc system, where each terminal of the system is optimized one at a time. The ambit of this research is restricted to the optimization of a single converter VSC system.

Broadly, the optimization algorithms to solve a global optimization problem, can be classified into two categories [59]:

a. Deterministic

b. Stochastic

Stochastic optimization methods provide a high quality approximation of the global optima. Possessed with inherent randomness in their vast search area, these methods are ideally suited for black-box formulations and poorly behaving functions.

In contrast, with Deterministic methods, the search area is limited to a localized area in the n-dimensional space. Therefore, the solution obtained may or may not be the global minima, rather a local minimum. In essence, these methods can provide the global minimum for a convex problem, but for non-convex type problems, a deterministic method does not guarantee the best solution (i.e. the global optimum). Additionally, for optimization problems with more than 10 variables, Deterministic methods are not preferred. An alternative approach to finding the global minima with deterministic methods can be, to divide the search area into many sections and employ the deterministic optimization methods in each area [60]. In this way, a solution which is comparable to that of the stochastic methods can be found.

In this thesis, the deterministic, Non-linear Simplex algorithm is used. The Optimization Enabled Electromagnetic Transients Simulation (OE-EMTS) is used to optimize the VSC parameters.

4.2 Optimization enabled EMTS

The concept of OE-EMTS was first introduced in [58]. In contrast to the multiple-run tool, which lacks any intelligence, OE-EMTS allows for determining the minima for a defined objective function. Therefore, the formulation of the objective function (OF) forms a crucial aspect of this exercise.

In OE-EMTS, the OF acts as the interface between the network solution and the optimization algorithm. The input to the optimization algorithm is the OF, and therefore should be indicative of the controller performance. Since, the optimization algorithm primarily aims to reduce the OF, once the gradient of the OF during consecutive runs, is less than that of the tolerance, the algorithm terminates.

The gain parameters from each optimization output are plugged into the VSC control system to find the network solution and recalculate the OF for the next run. Although somewhat erratic initially, eventually the algorithm ensures that the magnitude of the OF reduces continually. Upon satisfying the convergence criterion, the optimization terminates and the optimized controller parameters are obtained. Figure 4-1 shows the schematic which depicts the interface between the optimization algorithm and the network solver in EMTDC.

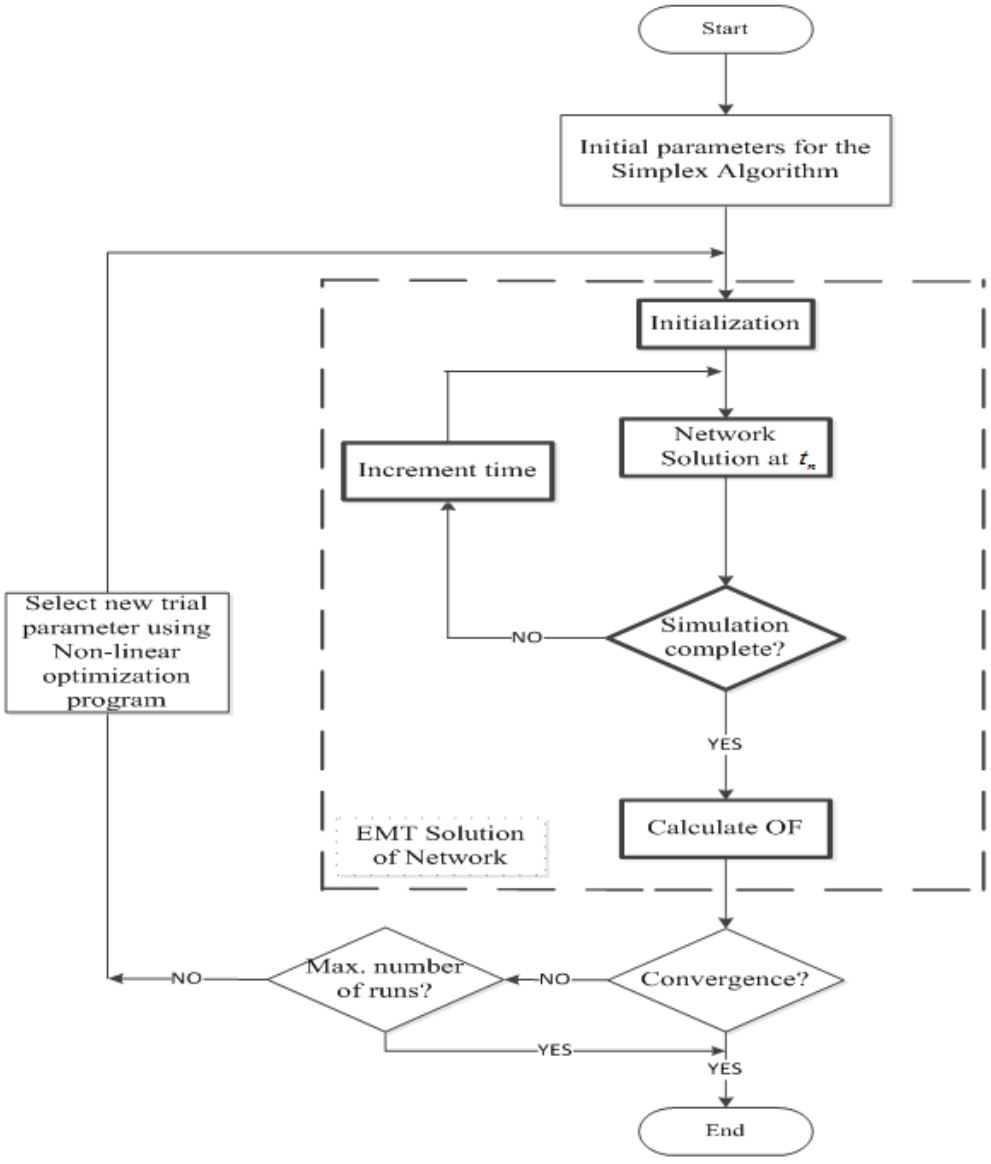

Figure 4 - 1 Flowchart for optimization enabled EMT simulation

The direction in which the algorithm looks for the next set of gain parameters, is dependent on the algorithm selected. Therefore, for non-convex type problem, it is useful to note that the results of the optimization from different optimization algorithms are not necessarily identical. For reasons mentioned in the earlier section, in this research, the Nelder-Mead Simplex [61] algorithm in PSCAD/EMTDC is used.

The test network in Figure 4-2 is used for optimization and all further analysis. The ratings for the system are mentioned in Appendix A.

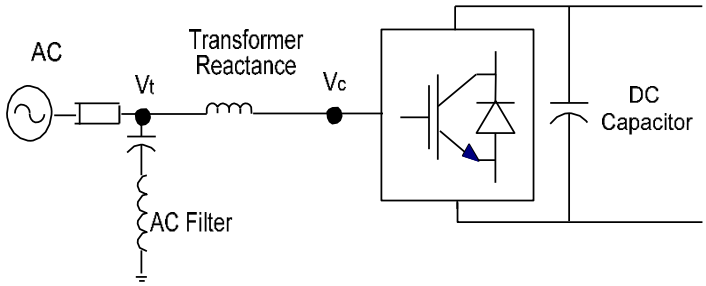

Figure 4 - 2 Test network for the Single converter system

In the test system the single converter is connected to an ideal DC source, which acts as an ideal DC voltage controlled converter terminal.

Therefore, for the single converter, the following VSC control parameters were optimized:

1. Controller parameters for the outer control loops:
   a. Proportional + Integral gains for the active power control loop (P)
   b. Proportional + Integral gains for the ac voltage control loop(V_{AC})
2. Controller parameters for the inner control loops:
   a. Proportional + Integral gains for the i_d control loop
   b. Proportional + Integral gains for the i_q control loop

For this research, it was assumed that the dynamics of the inner loop control for i_d & i_q are identical. Therefore, in total, 6 parameters were optimized.

4.2.1 Optimization algorithm: Non-linear Simplex Nelder-Mead method

The Non-Linear Simplex algorithm is a deterministic method, based on the formation of a geometric figure referred to as the "*Simplex*". For an *N*-variable optimization problem, the simplex has *(N+1)* vertices. At the outset, the algorithm chooses a simplex (i.e. *(N+1)* initial points) in space and computes the value of the OF at each of these vertices. After comparison, the vertex with the highest value of OF is discarded and replaced with another one. The selection of the new vertex for this algorithm employs one of the following operations [61] [62]:

(i) Reflection (ii) Expansion (iii) Contraction (iv) Shrinkage

After each iteration, a new point in (for operation (iii) or (iv)) or near (for operation (i) or (ii)) the current simplex is generated in search of the minima. The algorithm terminates when the diameter of the simplex is less than the specified tolerance. With repeated operations of (i), (ii), (iii) or (iv) providing new vertices, the algorithm determines a point in the *N*-dimensional where the OF is minimum. Since this method is deterministic in nature, the minima obtained may or may not be the global minima. The results are of course dependent on the initial search area of the simplex. This is one of the drawbacks of this method. This problem can be addressed by using different sets of initial operating points, or alternatively, by sectioning the search area into multiple regions. But, the main advantage of this method compared to the other methods is that for each iteration, the value of function needs to be calculated only once (at the new vertex). Therefore, the computational effort required for this method is very low [61].

4.3 Formulation of the objective function (OF)

The suitability of a given set of controller parameters, is measured by the OF. It is a scalar quantity. Therefore, the objective function so formulated, ought to be a combination of all the relevant error indices of the VSC control system, quantifying the deviations from the desired performance. The commonly used error indices [63] are *ISE* (integral of square of error), *ITSE* (integral of time multiplied by square of error) and *ITAE* (integral of time multiplied by absolute multiplied by absolute of error), to list a few. Each error index would result in its own characteristic OF, distinct from the others. For instance, the ISE depends purely on the magnitude of the error, therefore, providing more emphasis to the beginning of the transient. Whereas the ITSE and ITAE terms, lay more emphasis on the steady state error, since they include the time variable in their definitions.

In this research, the ITSE [63] was chosen as the error index. The definition for the ITSE is as follows:

$$ITSE_n = \int_{t_1}^{t_2} t\left(err_n\right)^2 dt \tag{4-1}$$

Where, $ITSE_n$ is the ITSE for the nth error, e.g.

$err_1 = (\mathrm{P}_{actual} - \mathrm{P}_{ref})$ i.e., the active power mismatch;

$err_2 = (V_{ac\_actual} - V_{ac\_ref})$ i.e., the ac voltage regulation;

$err_3 = (i_{d\_actual} - i_{d\_ref})$ i.e., tracking i_d in the inner current control;

$err_4 = (i_{q\_actual} - i_{q\_ref})$ i.e., tracking i_q in the inner current control

Each ITSE term contributes to a corresponding sub-objective function. The total OF, is a linear combination of the weighted sub-objective function, associated with each of the four

control loops. The selection of weights is explained in Section 4.3.1. In case of the VSC control system, since in theory, equal precedence is given to each of the tracked variables, the weights (w_n) are chosen taking this into consideration.

During optimization, to study the dynamic response with the controller parameters, the following disturbances were considered:

a. Startup transient (*Disturbance 1*)

b. Full power reversal (100 *MW*/30 *ms* ramp at 0.7*sec*) (*Disturbance 2*)

c. Voltage step change (from 0.9 *pu* to 1.2 *pu* at 1.25*sec*) (*Disturbance 3*)

Together, these disturbances cover most of the nominal operating range of the VSC. With three disturbances and weights assigned to the error indices from each control loop, it proved challenging to attain finer control during optimization. For instance, a preliminary analysis will show that since, typically, the startup times are large in the practical system, the startup transient need not be given the same weightage as the power reversal or the voltage change transient.

To overcome this, in this research it is proposed, that the time variables are assigned different weights(w_t) during the course of the run. Upon doing this, there were three more degrees of freedom attained, allowing for finer control. Of course this complicates the OF formulation, but this modification showed a marked improvement in the final optimized results. Therefore, upon substituting the errors from equation (4-1), the final OF, which is a linear combination of each of the sub-objective functions, is obtained as follows:

$$OF = \sum_{n=1}^{4} OF_n \tag{4-2}$$

$$\text{Where, } OF_n = w_n \int_{t_{1n}}^{t_{2n}} t_w \left(err_n\right)^2 dt$$

and $t_w = w_t * t$, for n=1,2, 3 and 4.

Choosing the SCR of the ac system connected to the VSC during optimization, was also crucial. For instance, using an ac system with very high SCR, would result in faster controller parameters which are likely to be detrimental for a low SCR systems. Similarly, with very low SCR, the optimized controller parameters might be too conservative, which would result in a slower system, which is not desirable either. Hence, the middle range was chosen, in this case, an SCR=2.0. After optimization, it was confirmed that operation was possible (though not necessarily optimal) for conditions where the ac system impedance was at its lowest expected value.

4.3.1 Selection of weights for optimization

The weights assigned to each error index, are essentially dependent on the magnitude of that error index from each variable, to avoid skewed emphasis completely in favor of one variable. For the sake of optimization, all of the values for the power, voltage and the currents were converted from their per-unitized values into their actual values. Initially all the weights for the transients(w_t) and the error indices(w_n) were set to unity. Thereafter, individual contributions for the total OF from each of the variables (P, V_{AC}, i_d, i_q) was studied. The contribution of $ITSE_{i_{d,q}}$ was seen to negligible, since the actual values (after conversion from *pu* to *kA*) were very small compared to the other errors. Therefore, it was imperative to provide a higher weightage for the $ITSE_{i_{d,q}}$ term, to give it comparable importance with

respect to the other ITSE terms. Thus, a very high weight of 5000 was chosen. This seemed to provide adequate weightage to the inner current control gains.

In addition, it was also noticed that the startup transients were satisfactory, but the response to the *Disturbance 2* and *Disturbance 3* were undesirable. Thereafter, the w_t provided to *Disturbance* 1 was reduced significantly and that of *Disturbance 2* and *3* were increased, equally. Thereafter, various combinations were tried using trial and error, for the component from power and voltage OFs and among them the most suitable ones were selected.

After several trials, the chosen values for the w_t and w_n are as listed in Table 4.1 and 4.2, respectively.

Table 4. 1 Weights chosen for each individual disturbance

Startup	Power Reversal	Voltage Step change
0.9	3.0	1.75

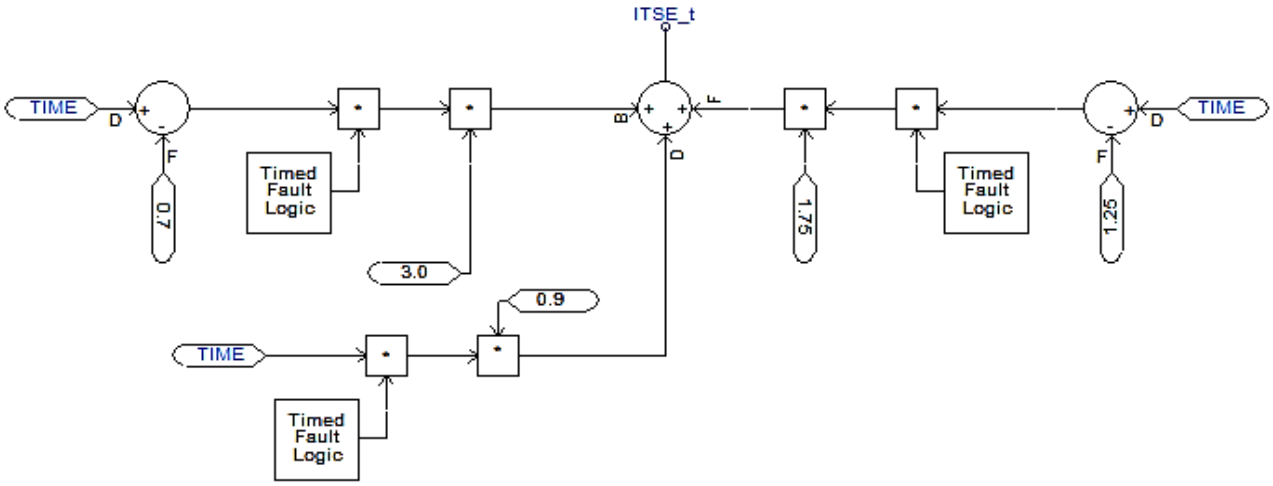

Figure 4 - 3 Block diagram to calculate the weighted time for the ITSE terms

Figure 4-3 shows the individual weights allotted to each disturbance, to obtain a weighted time variable.

Table 4. 2 Weights chosen for each individual VSC control loop

Power	AC Voltage	I_d, I_q
0.9	1.6	5000

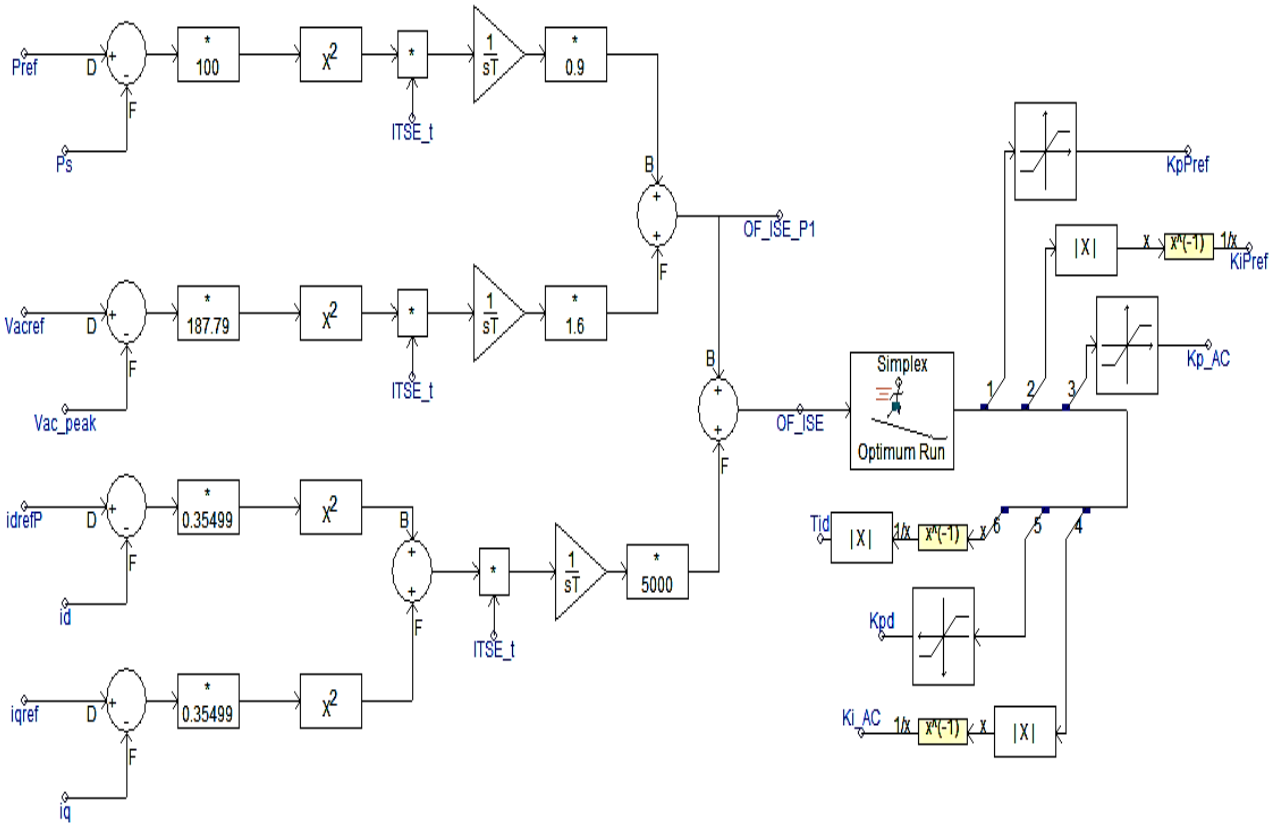

Figure 4 - 4 Block diagram for the OF calculation in OE-EMTS, showing each of the sub-objective functions

The implemented block diagram for the formulation of the OF is as shown in Figure 4-4.

4.3.2 Initial parameters and tolerance setting for the Simplex algorithm

The initial parameters for optimization as mentioned in Table 4.4 (a), are from the multiple run tool in PSCAD/EMTDC. Since this is a 6-parameter optimization problem, the simplex would be a heptahedron. As recommended in [61], the tolerance for the optimization algorithm was provided as 3% of the initial OF, resulting in a value of 6.76 [61].

Table 4. 3 Initial and optimized PI gains for the VSC control loops

(a) Initial gains

OF	K_{p_Ps}	$1/T_{i\_Ps}$	K_{p_Vac}	$1/T_{i\_Vac}$	$K_{p\_id,q}$	$1/T_{i\_id,q}$
225.44	0.45	106.2	10.2	86.2	12.9	88.5

(b) Optimized gains

OF	K_{p_Ps}	$1/T_{i\_Ps}$	K_{p_Vac}	$1/T_{i\_Vac}$	$K_{p\_id,q}$	$1/T_{i\_id,q}$
29.46	1.88	114.01	6.055	373.46	30.0	116.50

4.4 Results and analysis

The total number of runs for the optimization to terminate was 108. The Figure 4-5 shows the results from the first and the last run, allowing for a comparison between the VSC controller parameters prior to and after optimization.

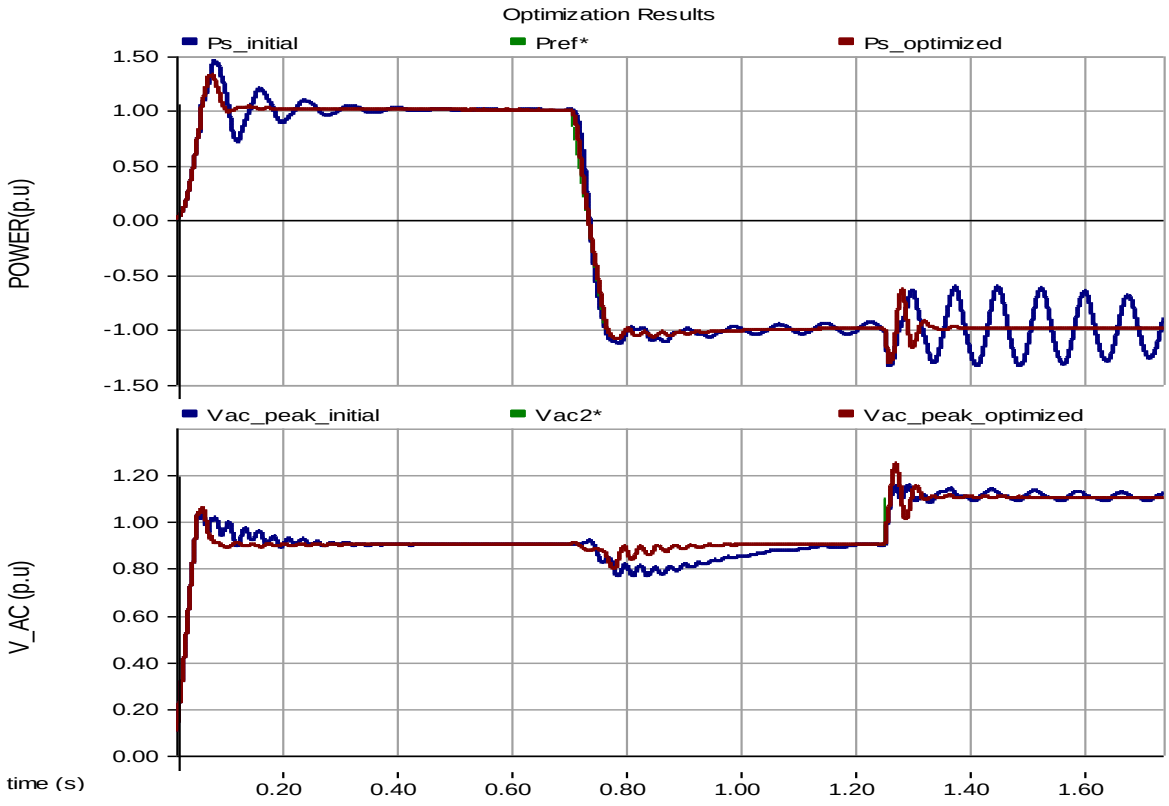

Figure 4 - 5 Power and Voltage at the VSC terminals, prior to and after optimization

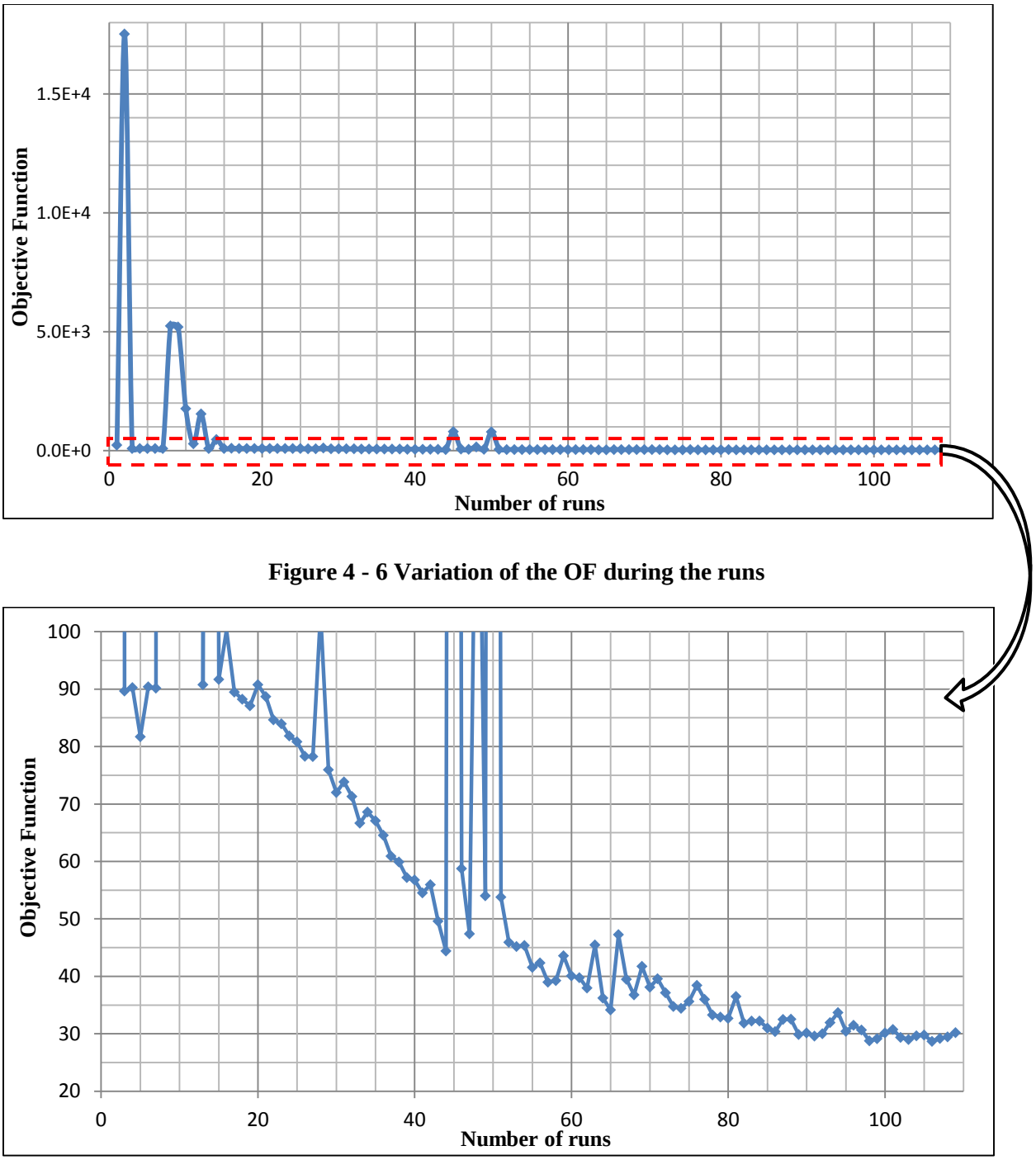

Figure 4 - 6 Variation of the OF during the runs

Figure 4 - 7 Zoomed in version of the OF variation using the Simplex method

The variation of the OF is as shown in Figure 4-6, and indicates how the OF reduces as it approaches the final tolerance value (as shown in Figure 4-7). The Table 4.4(b), lists the

output of the optimization algorithm i.e. the optimized gains for the VSC control loops. The results in Figure 4-5 show the marked improvement in the dynamic performance of the VSC.

4.5 Summary

The optimization of the Proportional and Integral gains of the VSC control system was done successfully. OE-EMTS employing the Non-Linear Simplex (Nelder-Mead) method was used to accomplish the same. After several trials, the weights for the ITSE terms (error index) corresponding to each VSC control loop were chosen. In addition, a novel approach is used, in which weighted time variables were used to attain finer control over the final optimized operating point.

By extrapolation, the elucidated approach for optimization of the VSC parameters can be extended to a two terminal system, with some modifications, and is left for future researchers. In case of multiple converters, considering the sheer number of parameters to be optimized, it is recommended that the relaxation approach be used, where each converter is tuned at a time, as demonstrated in [11].

Chapter 5
Adaptive PLL for the VSC

In this Chapter, the impact of the Adaptive PLL, introduced in this thesis, is investigated for controlling a VSC converter connected to an ac network of varying Short Circuit Ratio (SCR). It presents a comparison in system stability between the VSC with classical SRF-PLL and the Adaptive PLL, when subjected to large disturbances. Essentially, the main aim of this Chapter is to investigate the impact of the PLL architecture as well as its parameters, on the overall system performance, when connected to a weak ac system. Thereafter, possible reasoning for the improved performance of the Adaptive PLL with the VSC is presented.

5.1 Introduction and background

VSC converters with vector current control, connected into weak ac systems are prone to instabilities, due to disturbances. In [38], the anatomy of the vector current control approach is explained. The vector control method is based on decoupling the network equations in the *dq*-domain, to independently regulate the outer control loops (P and V_{ac} in this case). In a weak system, this decoupling between loops is weakened, owing to the reduced stiffness of the ac voltage bus [38]. Under these circumstances, the PLL performance would play a significant impact on the performance of the control system.

5.1.1 Stability of VSC

There can be two approaches adopted to analyze the overall stability of the system. For a small disturbance from the steady state, the system can be linearized about the operating point and the small signal analysis of the same, would provide significant insight into behavior of the system. Using this approach, it is possible to use the movement of the Eigenvalues to study the state variables and quantify precisely, the point at which the system would become unstable. In [11] a complete small signal model of the VSC connected to an ac system is developed. Further, using this model, a thorough analysis of the effect of each of the control system parameters on the overall stability has been presented.

Unfortunately, the range within which the linearized approach can accurately represent the system is limited, as the VSC and ac system form a nonlinear system whose operating point constantly changes. When subject to a large disturbance, using the TNA or EMT tools form the only mechanism to study the stability. In this thesis, PSCAD/EMTDC is used to study the effect of sudden large disturbances on the system stability, and how the inclusion of the Adaptive PLL can impact the performance, especially in weaker systems.

5.1.2 PLL and VSC

In [11], the linearized model of the VSC provides insight into the impact of controller parameters on the system stability. According to [11], a limit of SCR less than 1.6 is considered to be *weak* for a VSC converter. One of the major contributions from the small signal analysis, in [11] and [44], was the impact of the PLL gains (SRF-PLL) on the system stability especially at low SCRs. In fact, it was shown that for SCR less than 1.6, large PLL gains are detrimental to the system stability, especially under the rectifier mode of operation.

Therefore, smaller gains (resulting in slower dynamics) are recommended, thus limiting the operating range considerably.

In this thesis, it is proposed that the, both, PLL architecture and the gain parameters play a significant role in the stability of the system. The following sections are devoted to demonstrating the improved performance of the Adaptive PLL with the VSC connected in weak ac systems.

Test system:

In order to test the effect of the PLL on system stability in weak systems, several large disturbance tests were formulated in Electromagnetic Transient simulation software, PSCAD/EMTDC.

One of the main limitations of the SRF-PLL when operating in weak systems, is the plausible range of operating gains for stable operations. Therefore, the first endeavor was to find the stable operating range for the Adaptive PLL, and contrast it with that of the SRF-PLL. This would aid in determining the possible gain values for any further analysis.

The test system is a single VSC HVdc converter (Figure 5-1), connected to an ac system, represented by its Thévenin equivalent. The converter ratings, controller parameters for the VSC and ac system ratings are maintained same as in Table 4.1 and Table 4.4 (b). The other end of the dc line has been modeled as a stiff DC source, which represents an ideal voltage controlling converter on the other end, connected via a coaxial cable (100*km* long). The specifications for the DC cable are in Appendix A.

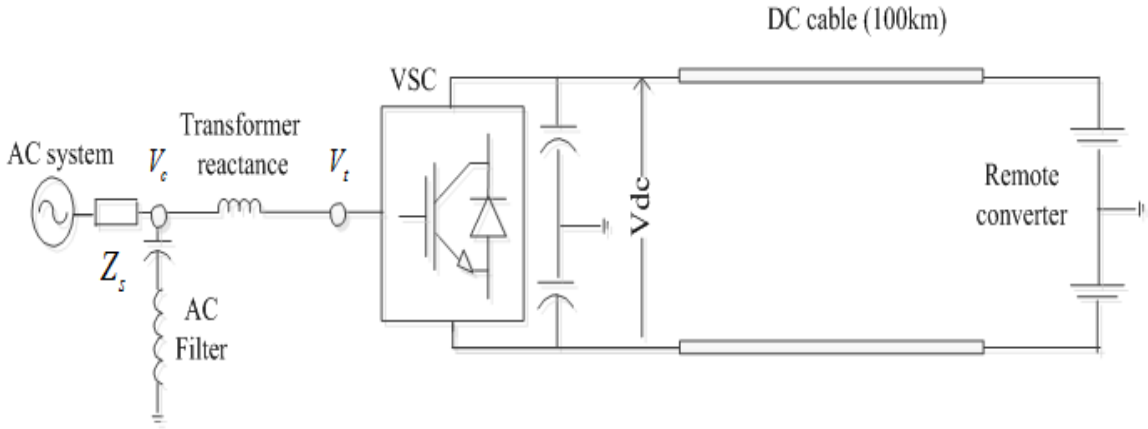

Figure 5 - 1 Single converter test system

The tests for analyzing the system stability, were framed on the basis of typical disturbances which can occur in a network. The sudden sharp changes in the ac system parameters were formulated with the deliberate intent of being pessimistic when testing the PLL.

The large disturbances designed to test the performance of the Adaptive PLL are as follows:

1. Change in Power Reference for the VSC
2. Sudden Change in the SCR of the ac system
3. Fault recovery ability, for symmetrical and asymmetrical faults at the VSC terminals

5.2 Operating range for PLL

Theoretically, the maximum power that can be transmitted by the VSC, for a given SCR, with the inverter or rectifier mode of operation can be calculated as follows [11]:

$$P_{max}(\,pu\,) \approx SCR * \left(1 \pm \frac{|R_s|}{|Z_s|}\right) \qquad (5\text{-}1)$$

Where +: Inverter Operation; - : Rectifier Operation;

P_{max}: Maximum power that can be transmitted to the system

R_s: Resistance of the equivalent ac system impedance

Z_s: Thévenin system impedance of the ac system

and SCR: Short Circuit Ratio of the ac system.

From equation (5-1), it is evident that for a given SCR, the rectifier operation is more difficult than inverter operation. The above equation is also indicative of the significant impact that the ac system impedance angle has on the system performance, especially in the rectifier mode of operation. In fact, it can be inferred that, during the rectifier operation of the VSC, P_{max} reduces as the ac system impedance becomes more resistive (i.e. angle deviates from 90°). For low SCR ac systems, this is further aggravated.

In order to study the impact of the PLL parameters, in terms of both, their plausible operating range and their sensitivity to slight variations in these parameters, the multiple-run tool is used. The objective formulated to analyze this, is to ramp up the VSC to full rated power in the rectifier mode of operation. It is useful to note that, although stability studies with the small signal analysis can determine stable operation at individual operating points, only EMT simulations can give an idea whether that point can be reached in practice, when power would be ramped i.e. with changing operating points. This is explored further, later on in this section.

The results from these multiple run simulations provide an understanding of the effect of a the variation in the PLL gain parameters (ΔKp or ΔKi), on the system stability. For a given SCR, the PLL gains (for the Adaptive and SRF-PLL) are varied, ranging from *1* to *200*, for the PI gains, K_{pPLL} & K_{iPLL}. For the sake of uniformity, in all cases, the system impedance angle is fixed at 80^0. In this analysis, the SCR of the ac system is set to 1.65, considered to be close to the boundary of SCR=1.6, between *strong* & *weak* systems [11].

The ramp-up time for the power reference to reach its rated rectifier operation (1 pu) is 10 s, which is sufficiently large. Figure 5-2 and 5-3 are the contour plots for the PI gains of the SRF-PLL and the Adaptive PLL, respectively. The colour scale of the Contour plots in Figure 5-2 and 5-3 are based on the ability of the VSC to track the reference power. An error index is used to quantify the deviations from the reference power, P_{ref}. Accordingly, the PLL gains corresponding to the highlighted (darker) region in the numerical scale, depict satisfactory performance. The higher error values on the scale are discarded, as they indicate of instability.

Operating range for the SRF-PLL:

A preliminary conclusion from the contour plots is that the permissible operating range for the Adaptive PLL is much larger than that of the SRF-PLL. Further, for the SRF-PLL, the best operating range is (area A) around K_p=60, largely independent of K_i. There is a small stable operating area, (B) in Figure 5-2, around K_p=10, K_i=20.

Operating range for the Adaptive PLL:

In contrast to the SRF-PLL, the Adaptive PLL shows a larger range of operation (Figure 5-3) for the rectifier startup operation with an SCR of $1.65\angle 80°$. The least error (implying improved P_{ref} tracking ability) is observed in the region around K_{pPLL}=5 and K_{iPLL}=10. However this point is very close to the unstable region and is thus not recommended as an operating point. These values are discarded, also to their poor dynamic performance.

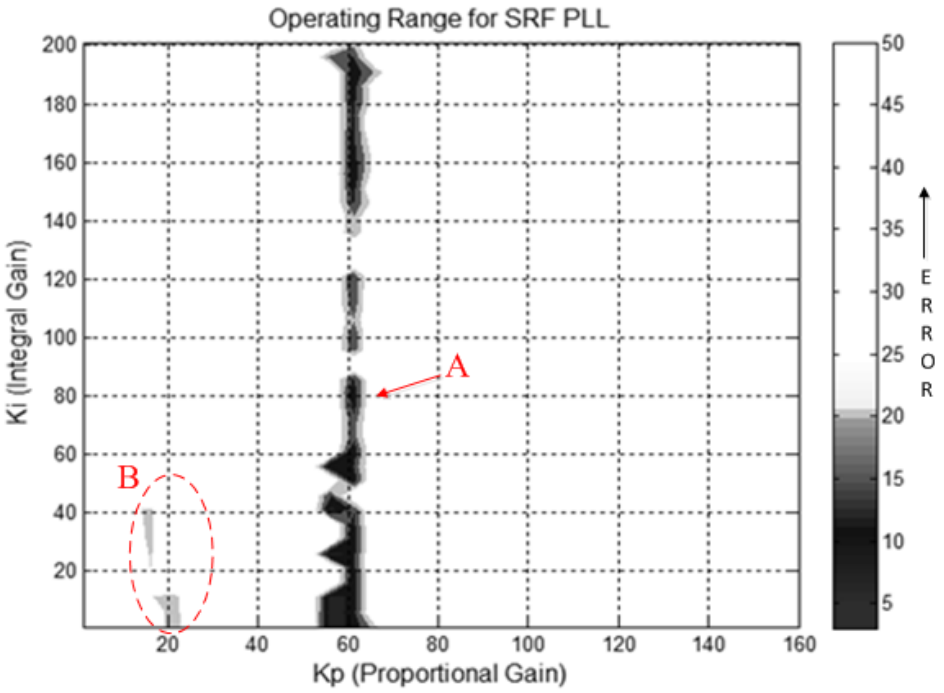

Figure 5 - 2 Operating Range for SRF-PLL

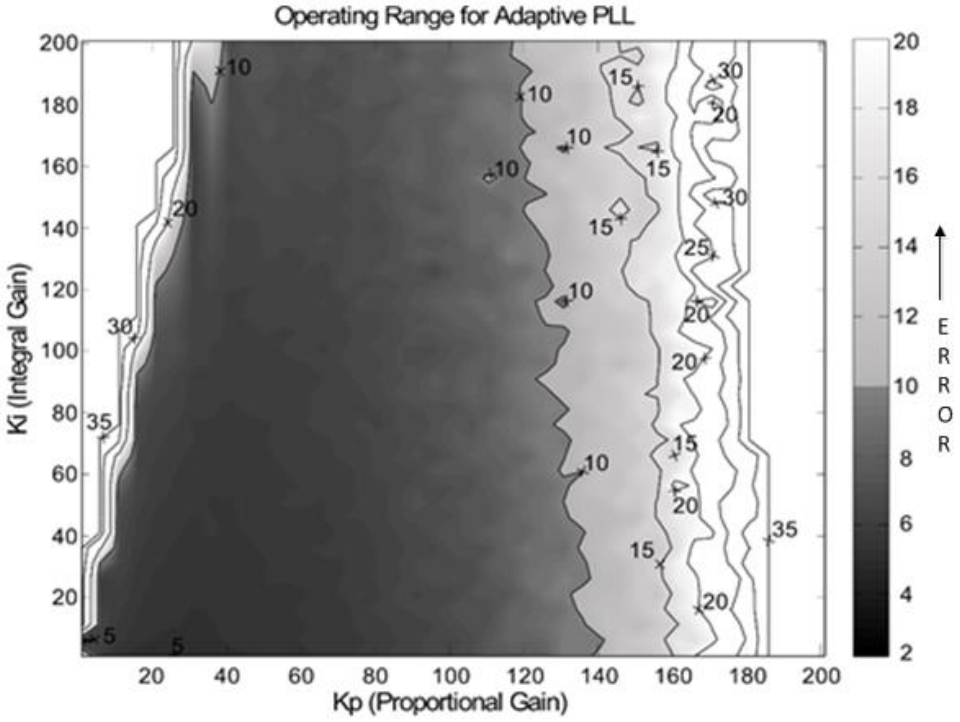

Figure 5 - 3 Operating Range for Adaptive PLL

In [11] it is proposed that for SCR>1.6, the system is always stable for rated power, irrespective of the PLL gains. The results in this section, evidently, contest the same. Typically, the small signal analysis provides results on the optimistic side, in comparison with that from the large disturbances studies [11].Therefore, although, each individual operating point might be stable (as shown by the small signal analysis), but the collective operation in the form of a ramp up, does not necessarily have to be stable, as indicated by the EMT results. This can be attributed to be the reason for the deviation from the limit of SCR=1.6.

5.3 EMT Tests to study impact of the PLL architecture on the system stability

5.3.1 Variation of active power reference:

In the first test case, the power reference for the VSC is varied to compare the effect on the system stability, with the SRF-PLL and Adaptive PLL. The PLL gains are set to $K_p = 60$ and $K_i = 120$. Numerous simulations were done over a wide range of ac system SCRs, connected to the VSC, ranging from strong system (SCR=4.0) to a very weak system (SCR=1.3). The ability of the VSC to provide the reference active power and maintain the ac voltage (i.e. response of outer loop controls) is analyzed for all cases. Additionally, the frequency output of the PLL in response to these disturbances is studied. The reference power variation, encompassing most of the nominal operating range of the active power for the VSC, is as shown in Figure 5-4.

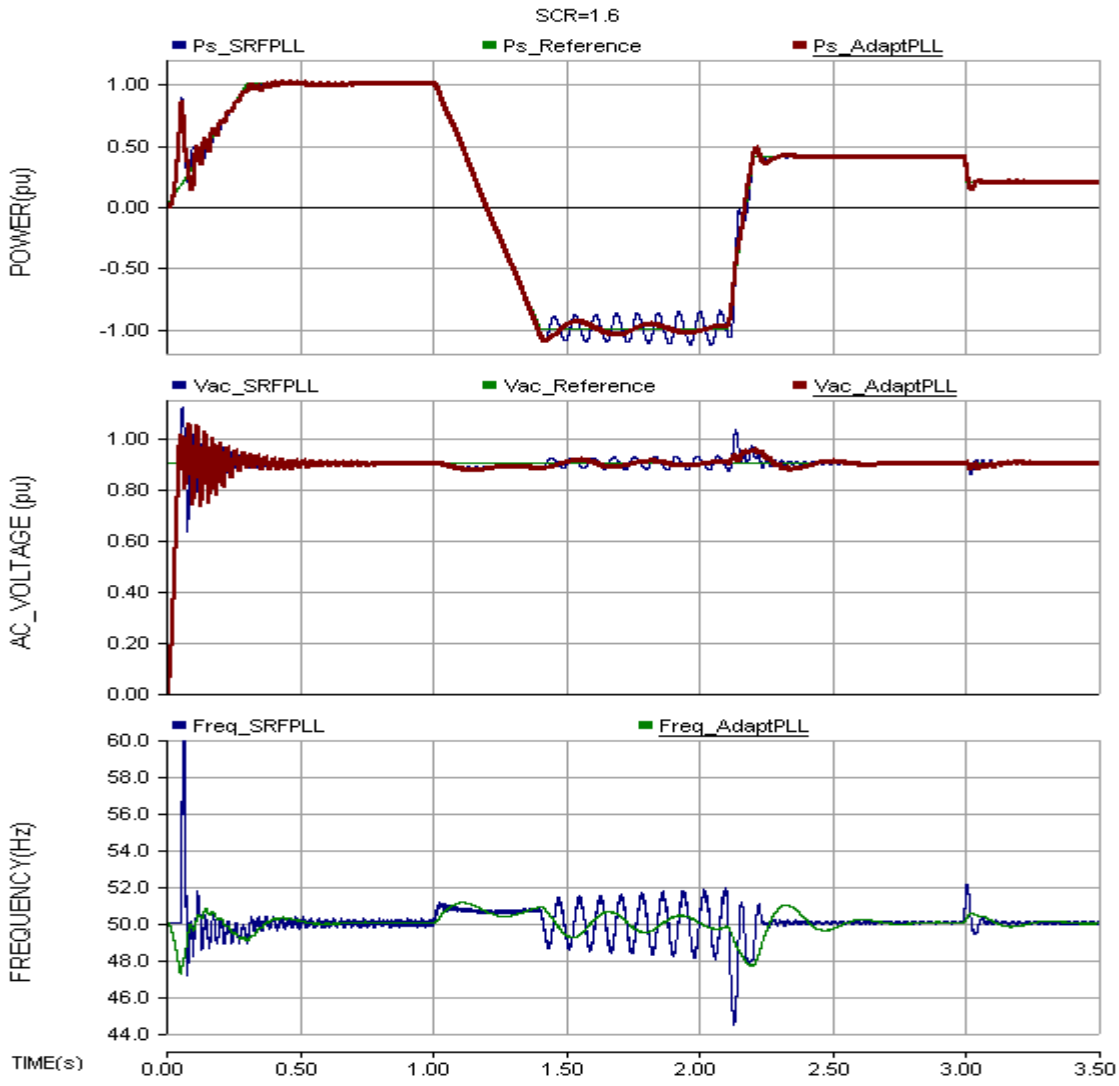

Figure 5 - 4 Response to change in Power Reference to the VSC for SCR=1.6, with the SRF-PLL and Adaptive PLL

The results shown in Figure 5-4, demonstrate the response of the VSC system for an SCR=1.6, with the SRF-PLL and Adaptive PLL, allowing for a comparative analysis. A study of the response shows that with the SRF-PLL, the oscillations in power and voltage (after t=1.4sec) continually increases. In comparison, the Adaptive PLL response is significantly better damped.

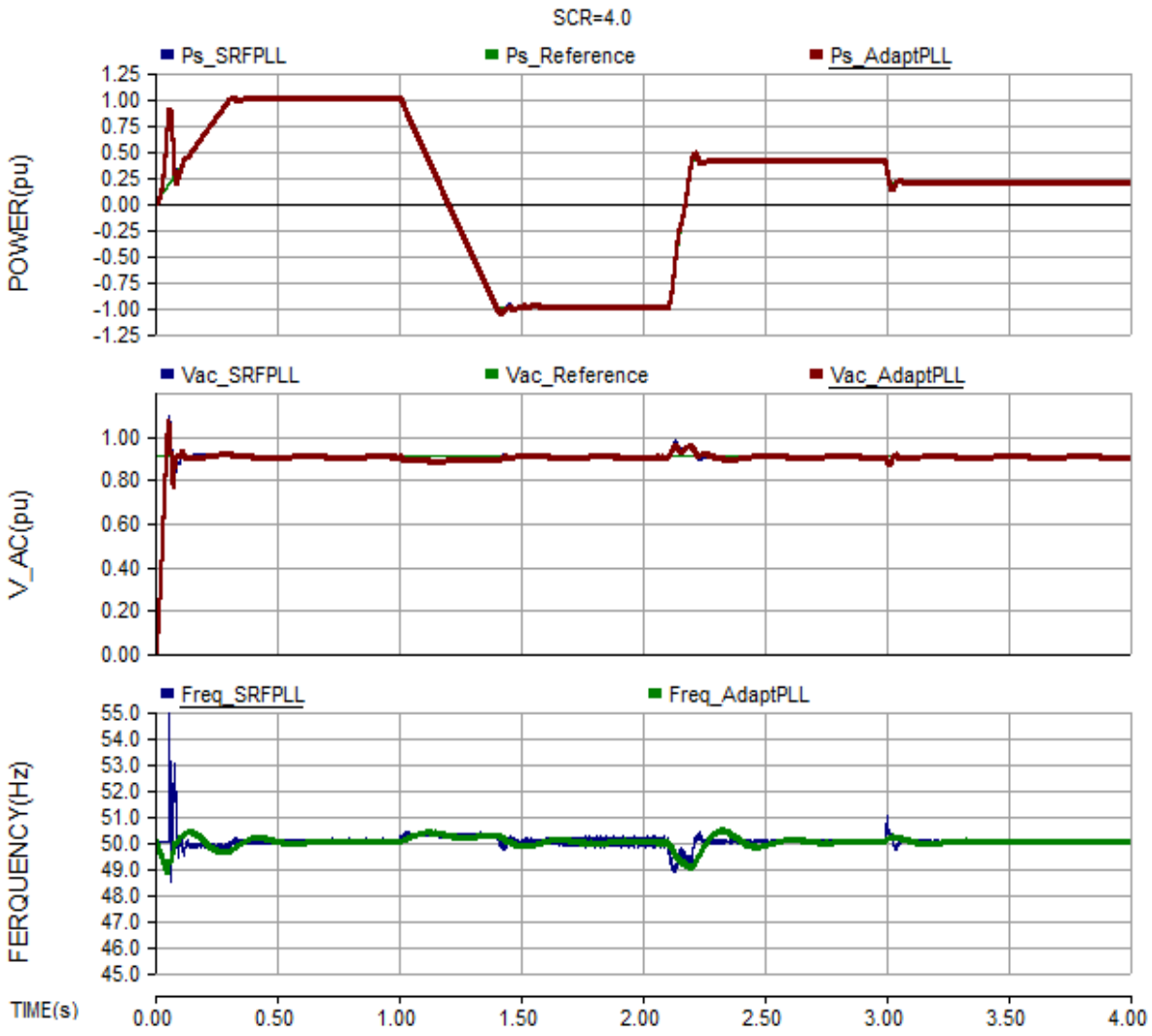

Figure 5 - 5 Response to change in Power Reference to the VSC for SCR=4.0, with the SRF-PLL and Adaptive PLL

The results can be summed up as follows. For strong systems (from SCR around 4.0), Figure 5-5, the VSC response with both the PLL designs can be seen to be essentially identical. As the SCR is reduced (less than 1.9), the VSC with the SRF-PLL showed poor dynamic response. Further, below the limit of SCR=1.6, with the SRF-PLL, the oscillations in the power and ac voltage increase continually, with negative damping. This shift in performance for the SRF-PLL is seen at SCR=1.6. Whereas, as evidenced from Figure 5-6,

with the same power reference, the Adaptive PLL is able to operate in very weak ac systems (SCR=1.31).

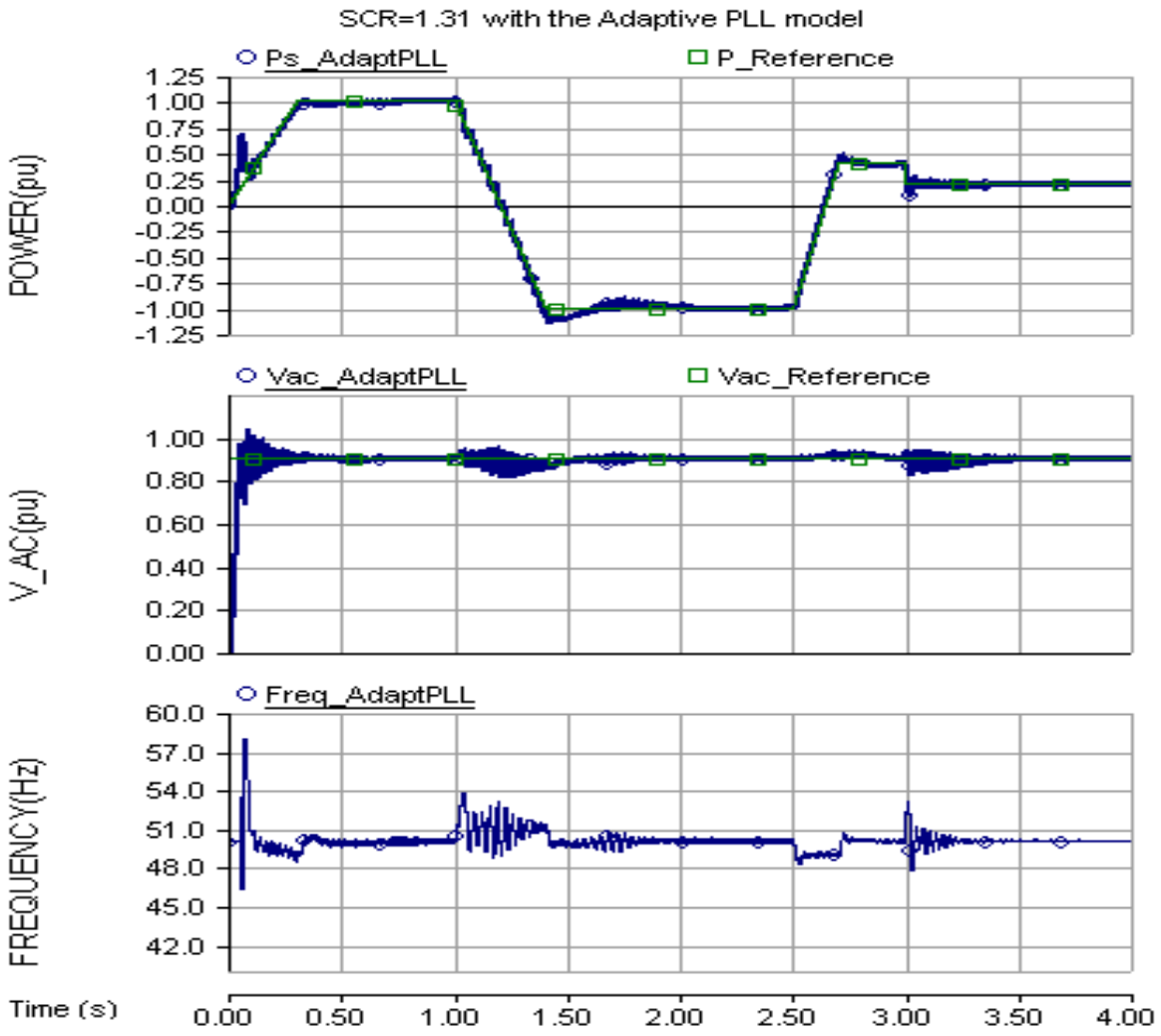

Figure 5 - 6 Change in Power Reference to the VSC for SCR=1.31, with the Adaptive PLL

Further, the deviation of the ac bus voltage magnitude from its reference value of 0.9pu is marginal. Also, the improved frequency tracking ability of the ac bus voltage by the Adaptive PLL, during & after large disturbances, is demonstrated in Figures 5-4 to 5-6.

5.3.2 Maximum transmissible Power:

The theoretical limit for the maximum transmissible power in the rectifier mode of operation is [11]:

$$P_{max}(\,pu\,) \approx SCR * \left(1 - \frac{|R_s|}{|Z_s|}\right) \tag{5-2}$$

In a practical scenario, though, the maximum transmissible power (P_{max}) is also dependent on the controller gains and the PLL architecture. Simulations were done to ascertain the maximum power that can be transmitted by the VSC with the SRF-PLL & Adaptive PLL, and to compare this with the theoretical limits. For the sake of uniformity, the ac system impedance angle is maintained at 80°, throughout. Further, the PI controller gains of both the PLLs was maintained at K_{pPLL}=60 & K_{iPLL}=120. The Figure 5-7 shows the plot of the P_{max} vs. SCR of the ac system, in the rectifier mode of operation, for all the three scenarios.

Evidently, the Adaptive PLL, shows a characteristic which is closer to the theoretical limits, in contrast with the SRF-PLL, which shows a significant deviation, especially for low SCRs. It would be useful to note that, with the increase in SCR values, corresponding to P_{max}> (2*P_{rated}), other limits such as that of the maximum currents through IGBT valves would also need to be considered.

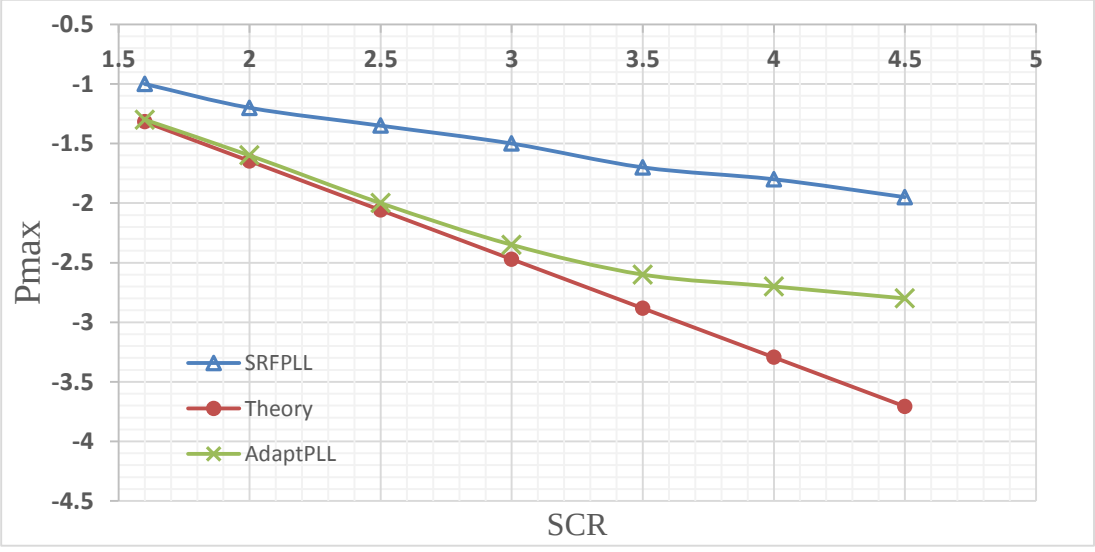

Figure 5 - 7 Pmax vs. SCR of the ac system in the rectifier mode of operation

5.3.3 Sudden change in the SCR of the ac system:

In the second set of tests, the impact of a sudden change in the ac system impedance on the VSC stability is explored. In particular, the impact that the structure of the PLL would have in this scenario is of interest. Considering the increased sensitivity with low SCRs, the VSC is operated with the rectifier mode of operation, supplying rated power (1 *pu*) is chosen. The PI gains for the SRF-PLL and the Adaptive PLL are maintained the same as before, at K_p=60 and K_i=120. The Figure 5-8 shows the response for both, SRF-PLL and Adaptive PLL.

The SCR of the ac system is stepped from 4.0 to 1.21 and then raised back to 4.0 as shown in the Figure 5-8. With the SRF-PLL, at the instance of the first change in SCR (at t=1*sec*), limit cycles are generated and the system never recovers. It can be seen that for the sudden reduction of the SCR from 4.0 to 1.21, the new operating point is unstable as evidenced by the oscillating limit cycles for power and voltage. Also the PLLs, frequency tracking mechanism goes awry and the frequency saturates at its controller limit of 60 Hz (Figure 5-8).

This performance is impressive for several reasons. Firstly, the SRF-PLL cannot even operate at this low SCR. For rated rectifier operation, with an ac impedance angle of 80°, reference [11] shows that the theoretical limit of the SCR, is 1.21, based on the voltage stability analysis. The Adaptive PLL can allow for full power reversal for SCRs approaching these theoretical limits (of SCR=1.21∠80°).

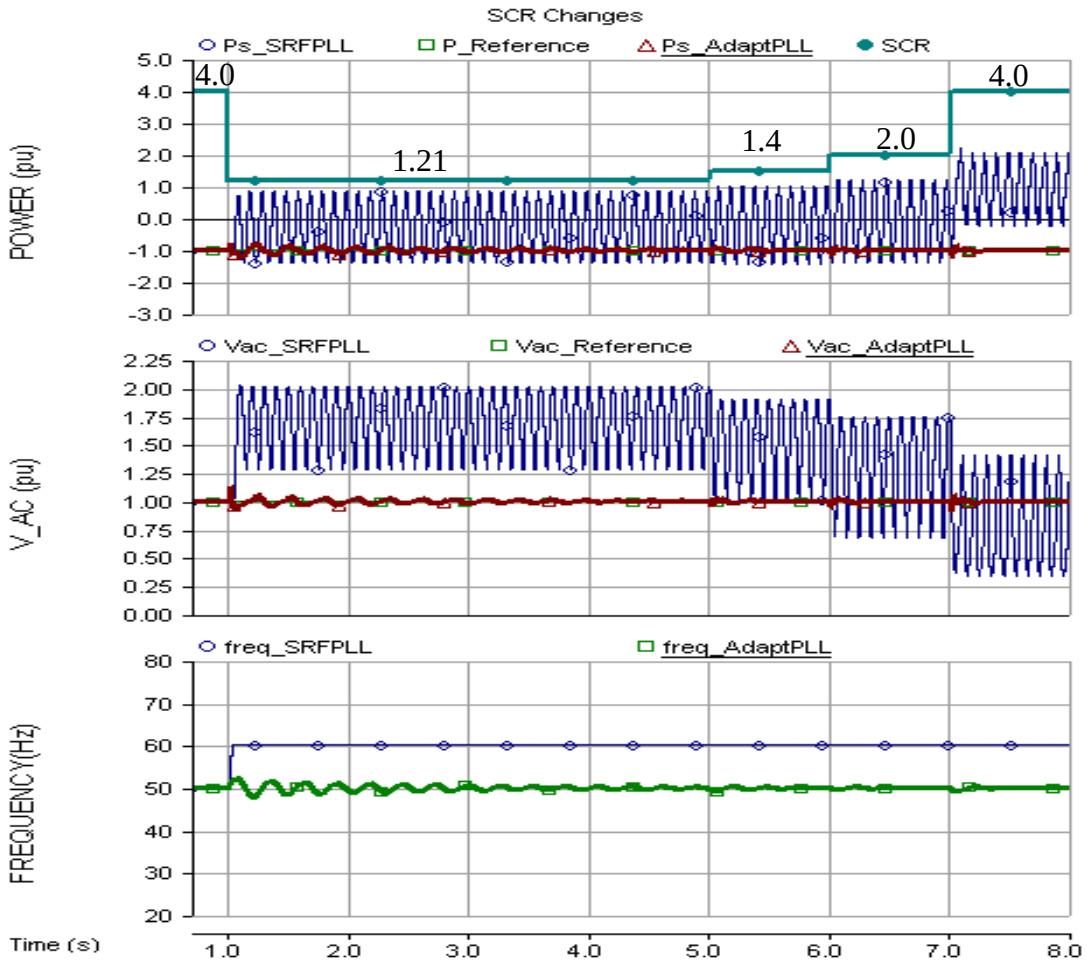

Figure 5 - 8 Response to sudden change in the SCR of the ac system with the SRF-PLL and Adaptive PLL

In contrast, with the Adaptive PLL, after the occurrence of the disturbance, the resultant frequency settles to the nominal value, eventually when the oscillations damp out. In each case, the VSC continues to supply the rated power, with minor transients at the time of the disturbance. This test, therefore, is indicative of the improved stability exhibited by the VSC system with the inclusion of the Adaptive PLL.

5.3.4 Fault recovery ability, for symmetrical and asymmetrical faults at the VSC terminals

The following tests were done to study the performance of the PLL, in terms of the impact the PLL architecture would have on the fault recovery ability of the VSC system, especially when connected to low SCR ac systems.

5.3.4.1 Three phase to ground Fault

With the test system, a 5-cycle (20*ms*) solid three phase to ground fault is applied at the terminals of the VSC, and the fault recovery is studied for the SCR of the connected ac system ranging from 4.0 to 1.25. The fault is applied at 4.00*s* and lasts for 200*ms*. During the fault, (starting at 4.02 s, allowing 20*ms* for fault detection logic to operate), the power order is set to zero. On fault clearing, the active power order is ramped to -100 *MW* (the negative denoting rectifier operation) at the rate of 100 *MW*/500*ms.*

During this analysis, it is duly noted that the fault dynamics of the system are dependent on several ac system parameters such as the insulation and grounding etc. But, by focusing on the performance of the PLL during the fault, it is possible to perform a comparative analysis between the traditional SRF-PLL and the Adaptive PLL. The added dimension of the weak ac system, will further provide useful insight into the PLL performance.

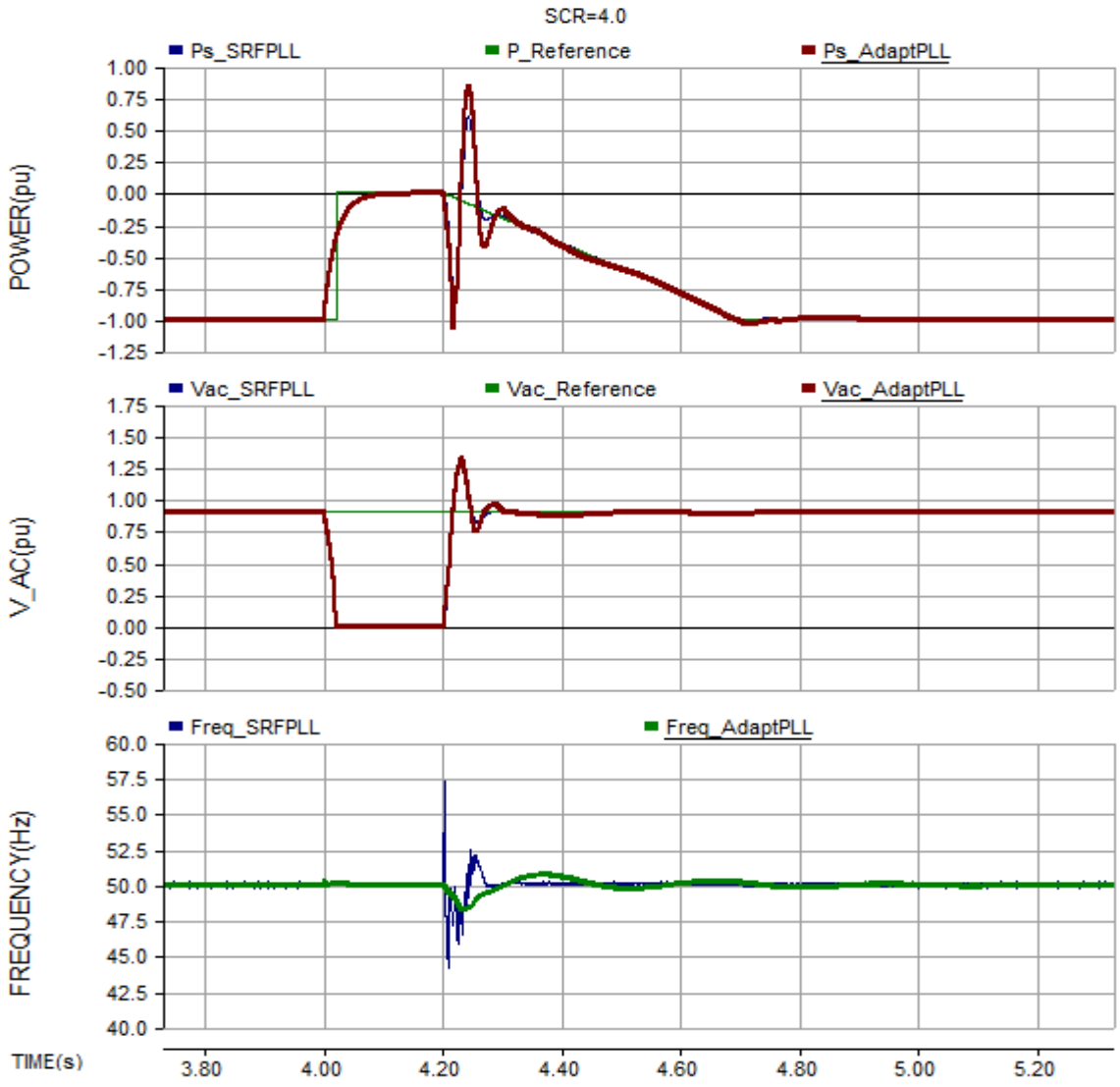

Figure 5 - 9 Three Phase to ground at the VSC terminals, for SCR=4.0, with the SRF-PLL and Adaptive PLL

Figure 5-9 demonstrates the response of the VSC system, with SRF-PLL and Adaptive PLL for SCR=4.0. Clearly, the power and ac voltage responses for both options are essentially identical, although there the detected frequency shows a larger variation with the SRF-PLL. This trend remains for SCR greater than 2.0.

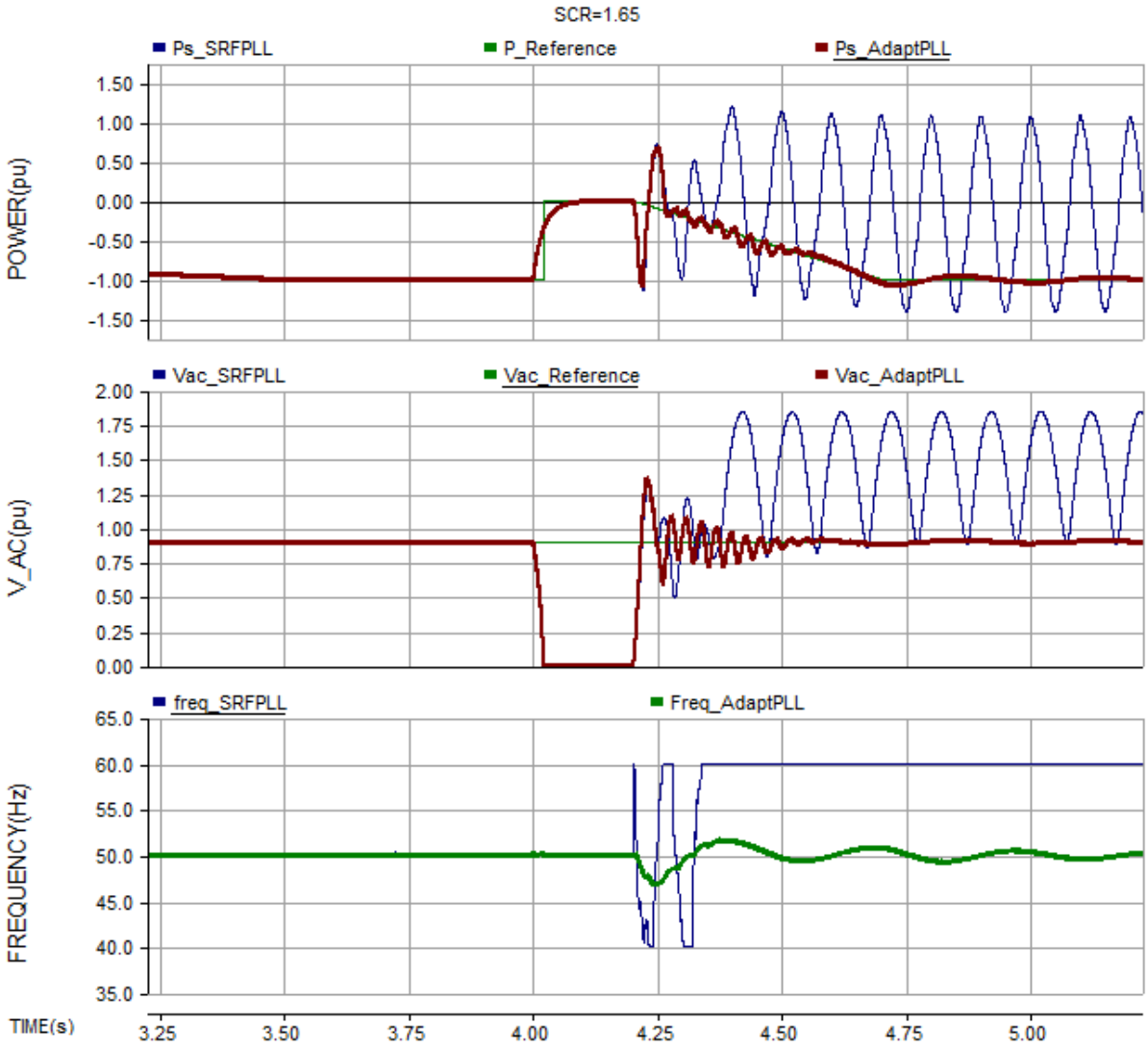

Figure 5 - 10 Three Phase to ground at the VSC terminals, for SCR=1.65, with the SRF-PLL and Adaptive PLL

As the SCR is reduced further, with the SRF-PLL, the minimum SCR for which the system is able to recover successfully from the fault, is SCR=1.65. For example, Figure 5-10 shows the corresponding fault recovery response of the SRF-PLL and Adaptive PLL for SCR = 1.65. Clearly, the system with the SRF-PLL goes unstable, whereas that with thee adaptive PLL

recovers. Whereas, with the inclusion of the Adaptive PLL, even for very low SCRs, such as SCR= 1.33, the system is able to recover successfully, as shown in Figure 5-11.

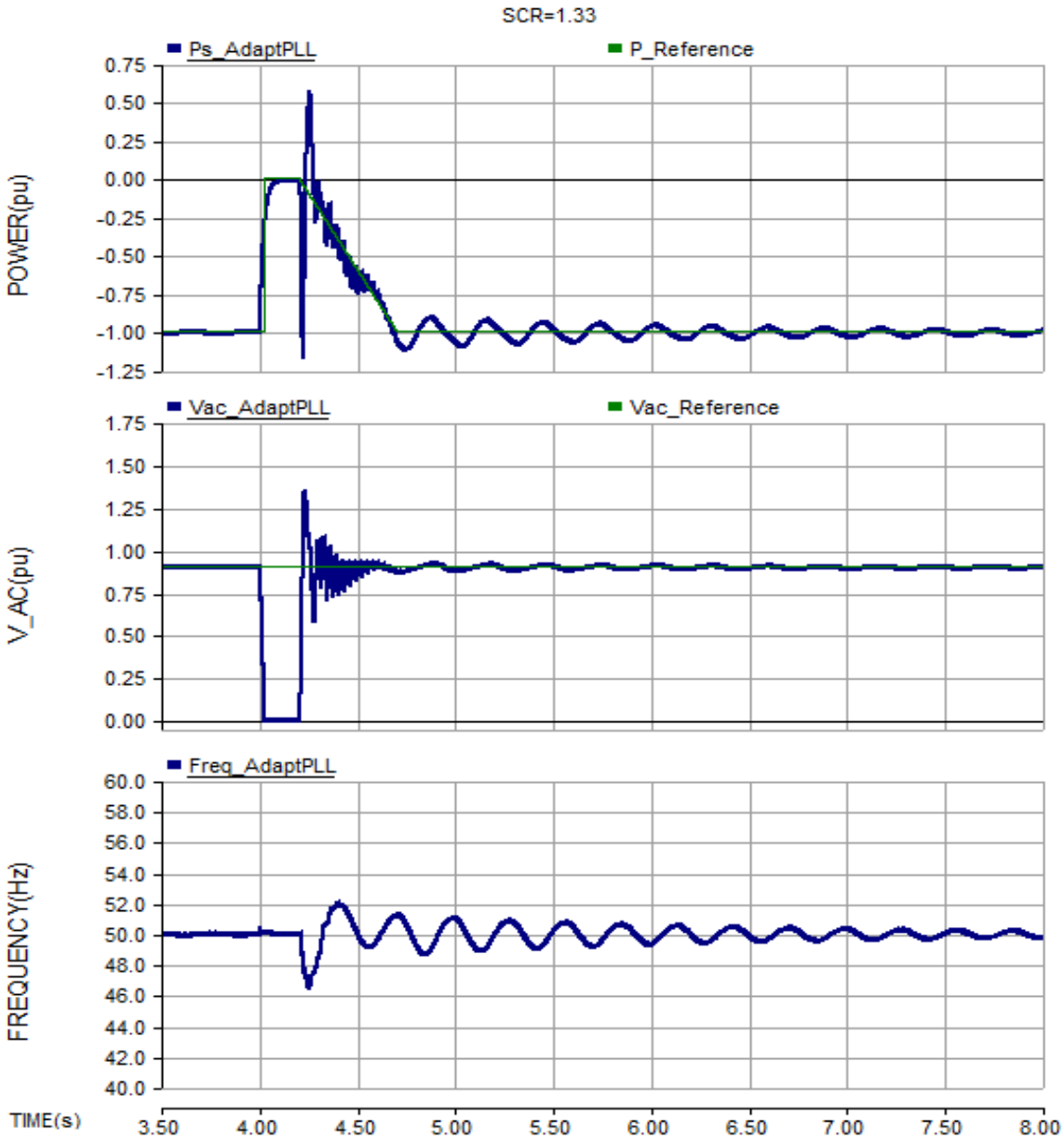

Figure 5 - 11 Three phase to Ground fault at the VSC terminals, for SCR=1.33 with the Adaptive PLL

Additionally, it is can be noted that with the Adaptive PLL, the deviation of the output frequency after the disturbance is marginal.

5.3.4.2 Single phase to ground fault (SLG)

The same sets of test cases, as above, were emulated for the SLG fault at the VSC terminals. It was seen with the Adaptive PLL, the minimum SCR was 1.42, whereas the limit for the SRF-PLL remained at 1.65. In the interest of brevity only macroscopic conclusion is being reported.

5.3.5 Summary of the Simulation tests:

The results in Section 5.3 are emblematic of the performance which the Adaptive PLL offers, particularly, when the VSC is connected to very weak ac systems. In most cases, the minimum SCR is approximately 1.3, which is very close to the theoretical limits for these systems.

5.4 Probable Reason for improved performance of Adaptive PLL

From the EMT simulations, it is evident that the inclusion of the Adaptive PLL causes an improvement in stability of the VSC system. This section provides the likely reason for this.

With the vector current control approach, for ideal conditions with very stiff voltage at the ac bus (infinite bus), there is perfect decoupling between the control loops (between (P,i_d) and (V_{AC},i_q)). Reduction in the stiffness of the ac voltage means that it is subject to change when a disturbance occurs. This causes a transient in the tracked phase generated by the PLL. In such a case, some coupling of the control loops will occur, irrespective of the PLL design, resulting in poorer performance. The main difference between the adaptive PLL and the SRF-PLL is the presence of the pre-filter block (Figure 3-4 and 3-5) which includes the fundamental component filter and the positive sequence filter block which extract the positive sequence

fundamental frequency component and then feeds it to a conventional SRF-PLL. This provides a cleaner signal with less distortion and interference by any negative sequence to the SRF-PLL within the Adaptive filter as compared to the standalone SRF-PLL. Hence the transients in the ac voltage are pre-filtered and allow the Adaptive PLL to track the phase and frequency more accurately, and consequently result in maintaining the decoupling between the control loops more tightly.

5.5 Summary

In [44], the significant impact of the PLL gains on the system stability was first alluded to. In this thesis, this concept has been taken further to note that in addition to the controller parameter gains, the PLL architecture also can have significant impact on the stability of weak systems. Two possible PLL architectures have been compared: the classical SRF-PLL and the Adaptive PLL. With the aid of EMT simulations, for rectifier operation, a wide range of stable operation has been established for the Adaptive PLL, which is in contrast with the SRF-PLL, even for systems which are at the boundary of strong and weak systems (at SCR =1.65).

Further, several tests were devised to compare the stability with the inclusion of the above mentioned PLL designs. Based on the tests, results can be classified as follows:

1. Variation of reference active power: With the SRF-PLL, the VSC system can remain stable only up to SCR=1.6 considering step changes in power. Adaptive PLL is better in comparison. It accommodates a change in power from +100 *MW* to -100 *MW* for ac systems with SCR greater than 1.31.

2. Sudden change in ac system impedance: A change in the ac system impedance, would significantly impact the VSC performance. With the Adaptive PLL, the stability of the system was intact even for a sharp change in the SCR from 4.0 to 1.21.

3. Fault Recovery ability: Basic tests were done over a wide range of SCRs for the ac system, when a fault of three phase to ground and single line to ground fault were applied at the VSC terminals. Here again, the Adaptive PLL, showed good recovery for very weak systems, where the SRF-PLL clearly failed.

With the above results, it can be concluded that the Adaptive PLL is very well-suited to perform under situations where the ac system is very weak.

Chapter 6

Conclusions and Future Work

6.1 Contributions and conclusions

The main contributions and major conclusions from this thesis are listed below:

Design of an improved Adaptive PLL:

A new PLL was designed which can extract and track the fundamental positive sequence component of the input voltage. The Adaptive PLL consists of a frequency adaptive pre-filter structure, which is designed to extract this component, so as to provide error-free tracking with input voltage distortions. The Proportional-Resonant (PR) filter and all-pass filter are designed for this pre-filter architecture.

Optimization of the proposed Adaptive PLL is for good dynamic performance:

The parameters of the proposed PLL were selected using optimization-enabled EMT simulation. The Adaptive PLL showed dynamic performance which is comparable with the SRF-PLL when the applied voltages are harmonic free. However, in actual applications the SRP PLL would require additional harmonic filters. In that case, the Adaptive PLL is significantly faster (i.e. reduced settling time) than the SRF-PLL with filter.

Investigation of performance under ac voltage unbalance and harmonic conditions:

The performance of the Adaptive PLL with unbalance in the input voltage is tested over a wide range, ranging from an unbalance of 10% up to 50%. The SRF-PLL and the SRF-PLL with filter showed considerable errors, increasing in proportion with the percentage unbalance in the input. In contrast, the Adaptive PLL shows no errors.

Further, the PLL performance upon being subject to harmonic distortions is studied. The voltage THD is varied over a whole range of values, ranging from small THD of 1%, up to very high values such as 13%. The SRF-PLL shows the highest errors in frequency tracking. The SRF-PLL with filter, has improved performance, subject to the relation between the cut off frequency of the filter, the order of the filter and the order of the input harmonics. For the Adaptive PLL, the effect of the harmonics for higher THD is far reduced compared to the other two designs. The disparity is more pronounced as the THD increases, making a stronger case for the Adaptive PLL. This trend continued even for inputs with interharmonics.

Optimization of the VSC control system:

The control system of the VSC with vector current control was optimized. Using OE-EMTS, the Non-linear Nelder-Mead Simplex method is used for controller parameters optimization. In this thesis, a modified optimization approach is demonstrated, which allows for finer control and improved dynamic response, for a single converter system.

Evaluation of System Operation with the PLL with the VSC connected to an ac network:

The impact of the Adaptive PLL is investigated for a VSC converter system connected in to ac systems of different SCR. As reported in [11], the inner and outer loop gains have a smaller impact on system stability compared to the PLL gains. In furtherance to this, during

the course of this thesis, it has been established that, the Adaptive PLL has improved dynamic response. In particular:

- Sensitivity to Parameters:

  In the controller parameter space (i.e. proportional and integral gains), the Adaptive PLL showed a larger stable operating range, for rated rectifier operation as PLL parameters were changed. In contrast for the SRF-PLL, the operation was limited to narrow specific regions. These results in turn implied the reduced sensitivity of the system stability, to the PLL gain variation for the Adaptive PLL, a key highlight of the newly developed PLL design. Even with very slow ramp up, the VSC rectifier with SRF-PLL, showed very small plausible region of operation to attain rated power (1*pu*).
- The Adaptive PLL was able to operate stably when large steps in power order are made (e.g. from +1pu to -1pu) at much smaller SCRs for the ac system. The limit was SCR = 1.3 as opposed to 1.6 with the SRF-PLL.
- The adaptive PLL was able to operate stably even with sudden changes in system SCR. In contrast for large SCR changes (e.g. 4.0 to 1.21), the SRF-PLL did not.
- The adaptive PLL showed faster recovery from ac faults.

6.2 Future work

With the results from this research, the significant impact that the Adaptive PLL has on the overall system with the VSC, has been established.

The following is a list of possible future work:

- A natural extension of this work would be the implementation of the Adaptive PLL in a two converter system and further, in MTDC systems. The performance of the PLL in weak ac systems when connected in a larger DC grid would be interesting.
- To develop the small signal model of the entire system, including the Adaptive PLL, and perform sensitivity analysis on the Eigenvalues corresponding to the PLL gain parameters.
- In this work, the Adaptive PLL has been shown to have good immunity to distorted voltage conditions, showing minimal errors in phase and frequency outputs. Thus, the application of the Adaptive PLL, in FACTS devices such as STATCOM in networks prone to such voltage distortions or prone to unbalanced faults, would be interesting.
- Optimization of the VSC control system parameters, with the inclusion of the PLL parameters.

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Appendix

1. AC system parameters

Table A- 1 AC system parameters of the test network

Ac system parameters	Values
Rated ac system voltage (base)	230 *kV*, 50*Hz*
Rated dc power rating	100 *MW*
DC voltage	375.58 *kV*
Transformer reactance + Phase reactor	0.3 *pu*
Tuned filter	33rd Harmonic
PWM switching frequency	1650 *Hz*
Converter type	2-level

2. DC cable model parameters

Bergeron model

Table A- 2 Bergeron model parameters

Line parameters	Values
Series resistance	0.13379E-04 Ω*/m*
Series inductance	3.0506 *μH/m*
Shunt capacitance	0.27224 *nF/m*

Additional cable data:

Table A- 3 Coaxial cable parameters

Cable parameters	Values
Conductor resistivity	1.68e-8 Ω*m*
Conductor relative permeability	1
Insulation relative permittivity	2.3
Insulation relative permeability	1

Cross section of the coaxial cable model:

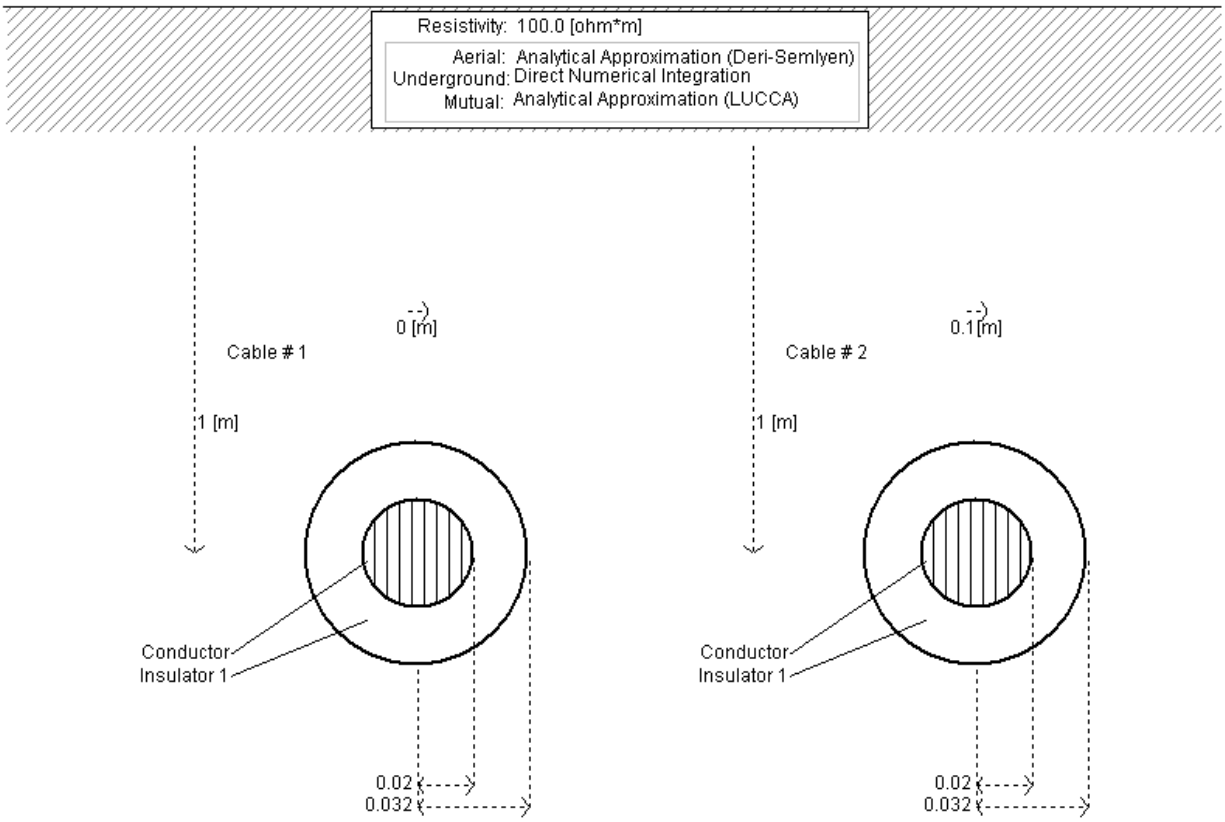

Figure A- 1 Cross section of the DC cable model