Determination of Impulse Generator Setup for Transient Testing of Power Transformers Using Optimization-Enabled Electromagnetic Transient Simulation

by

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Abstract

Natural lightning strikes induce impulsive overvoltages on transmission lines and its terminal equipment. These overvoltages may cause failures in insulation mechanisms of electrical devices in the power system. It is important to test the insulation strength of a device against these impulsive overvoltages. Usually, Marx generators are used to generate impulse waveforms for testing purposes. A novel approach is proposed to obtain resistor settings of a Marx generator for impulse testing of power transformers. This approach enables us to overcome most of the major challenges in the commonly used trial-and-error method, including excessive time consumption and potential damage to the transformer. The proposed approach uses the frequency response of the transformer to synthesize a circuit model. Then, a genetic algorithm based optimization-enabled electromagnetic transient simulation approach is used to obtain the resistor settings. The difference between the desired waveform and the simulated waveform is set as the objective function. Maximum feasible resistor values define boundary conditions for unknowns to be optimized. The optimized resistors are implemented in a real impulse generator and tested on a three phase power transformer. Different cases of impulse generator resistor arrangements are studied that confirm the accuracy of the proposed method.

Acknowledgements

This thesis is an outcome of two years of hard work. I may not have made it through without the support of some wonderful people throughout this period. It's an honor for me to extend my warm acknowledgments to all of them at this point.

First, I would like to express my sincere gratitude to my advisor, Dr. Behzad Kordi for suggesting me this topic and for his invaluable guidance, support and encouragement throughout this work. It has been a great privilege to work with him. I am also grateful to my co-advisor Dr. Aniruddha M. Gole for his valuable suggestions and encouragement. I would like to thank the examining committee for accepting my thesis to review. Conducting this work wouldn't have been possible without the financial support from the Faculty of Graduate Studies of the University of Manitoba and Natural Sciences and Engineering Research Council of Canada. I would also like to convey my gratitude to Mr. Nathan Jacob at Manitoba Hydro High Voltage Test Facility for sharing his valuable knowledge and for making necessary arrangement to use test facilities.

I am forever indebted to my family for all their love and guidance throughout my life. Without them, I won't be the person who I am today. Finally, all my friends deserve a thank for their support and encouragements whenever I needed them most.

Dedication

To my loving parents.

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Chapter 1

Introduction

1.1 Background

The occurrence of a natural electrical discharge within very short time between a cloud and the ground or within a cloud, accompanied by a bright flash is called lightning. Lightning strikes induce impulsive overvoltages on transmission lines and its terminal equipment. Some overvoltages are transfered from the lightning strokes by hitting the transmission line directly. Typically, an average lightning waveform on a transmission line would have a crest value in order of 1000 kV and every stroke may inject lightning current up to about 100 kA [1, 2]. These impulsive overvoltages can cause insulation failures in most of the electrical devices in the power system. The insulation mechanism of an electrical device needs to be strong enough to withstand impulsive overvoltages to avoid any unnecessary breakdowns. There are number of tests perform on electrical devices to ensure their insulation strength. In general, the tests performed on electrical devices can be divided into three main categories [2]:

- Type tests (also known as design tests) are conducted on the first prototype of product to confirm the design specifications. This test is not repeated on other products of same type, *e.g.* temperature-rise test, zero sequence impedance voltage test, etc.

- Routine tests are performed on each product manufactured to confirm proper manufacturing of each and every unit. This test is essential to be performed on each unit before dispatching the product to the site, *e.g.* measurement of winding resistance, partial-discharge measurement, dielectric tests, etc.

- Special tests (also known as other tests) are conducted as per customer requirement to obtain information useful to the user during operation or maintenance of the device, *e.g.* measurement of harmonics of the no-load current, determination of sound level, measurement of insulation resistance, etc.

Some tests can fit into more than one category, based on the operating voltage of the Device Under Test (DUT). The tests which check the strength of an insulation mechanism are called dielectric tests. Usually, dielectric tests are a sub category of routine tests, which includes lightning impulse test, switching impulse test, induced AC voltage test. The main purpose of in-factory dielectric tests is to ensure the overall insulation strength of a given apparatus. Typically these tests are conducted by the manufacturer at the end of the production line or sometimes by the end user.

The lightning impulse test is one of the key and well known tests in the dielectric test category. The purpose of this test is to check the insulation strength of a device under a lightning strike. There are a number of lightning impulse tests to be performed

on a sample as per the standards [3], [4]. These tests include full lightning impulse test, tail chopped lightning impulse test, and front chopped lightning impulse test. Usually the test voltage is selected based on the basic insulation level (BIL) of the DUT. This value can reach a few times of the DUT's operating voltage. Further details of lightning impulse tests and impulse waveforms are explained in Chapter 2.

1.2 Problem Definition and Existing Solution

The most challenging task in the lighting impulse test is generating lightning impulse waveforms in the laboratory. From the data acquired by natural lightning, the standard lightning impulse waveform has been defined as a double exponential waveform (see Fig. 1.1) with a risetime (T_1) of 1.2 μs and a falltime (T_2) of 50 μs. Impulse generator is the device which is used to generate these waveforms. It is typically a Marx generator [1] which consist of multiple stages. Each stage has two resistors which control the risetime and falltime dominantly. These resistors should be set to their optimum values to obtain the desired waveform [5].

In the existing method, these resistor values were calculated using a set of analytic equations that have been developed for a simplified model of the impulse generator [1]. In the initial calculation, the DUT is assumed to be a capacitive load and the multi-stage impulse generator is simplified to a single stage generator. The DUT's capacitance is an essential parameter in this calculation since it is a part of the generator circuit as well. The usual practice involves conducting a bridge measurement to record this capacitance. In addition, there are some other methods which use fre-

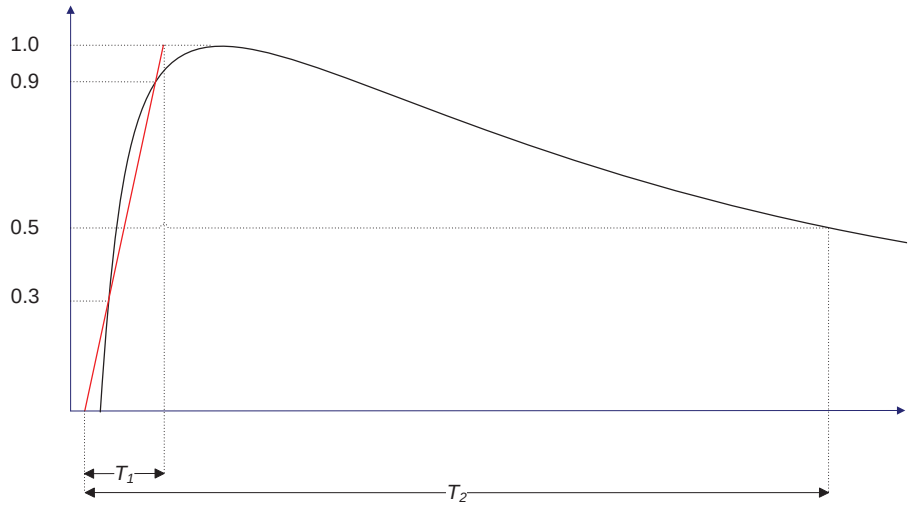


Figure 1.1: The general shape of double exponential impulse waveform with risetime of T_1 and falltime of T_2 [1].

quency response analysis (FRA) [6], finite element analysis (FEA) [7], or analytical approaches based on the physical construction [8] to calculate the capacitance of the DUT. When the capacitance is measured or calculated, the resistor values were calculated based on the desired waveform. In most cases, a close match to the desired waveform is not guaranteed in the first try. This is a result of the approximation of the DUT as a capacitive load which is not valid for the frequency range of interest, and due to the approximation of the multi-stage impulse generator as a single stage generator. The above calculated resistor values will be employed to start as an initial point. The fine tuning of resistor values is done by trying different resistor combinations starting with the above calculated values based on the test engineer's experience [9].

This trial-and-error approach has caused several drawbacks in the existing method. Since each resistor combination should set up manually in the impulse generator, the

process is very time consuming. In some cases, it takes one full working day to set up the impulse generator (Nathan D. Jacob, High Voltage Test Facility - Manitoba Hydro, personal communication, April 10, 2014). Further, excessive number of trial tests on the DUT is not recommended, since it affects the lifetime of the insulation mechanism and may cause unwanted damages too. In some cases, typical impulse test arrangement is not sufficient enough to generate the desired waveshape. It may require additional circuit elements or arrangements like overshoot compensator, Glaninger circuit, paralleling stages or introducing a grounding resistor [10]. In the existing method, these requirements cannot be identified at the beginning of the testing process. Usually, it takes number of trail tests to sense such requirements and sometimes it is impossible. All these disadvantages, result in long test times, ultimately causing higher operating cost. Therefore a fast and accurate method to obtain impulse generator resistor values is highly desirable.

1.3 Objective of the Thesis

The primary objective of this thesis is to find the optimum resistor settings of the impulse generator to obtain the standard lightning impulse waveform for testing of the power transformer. The total time consumption for the entire optimization process is expected to be significantly lower than that of the existing method.

The selected DUT for this thesis is a power transformer (hereafter referred to as the transformer). The development of a detailed circuit model for the transformer, to be used in an electromagnetic transient simulation program (EMTP-type program)

is considered as another objective. Identification of the requirement of additional test apparatus for the impulse test setup is also noted as an objective of this thesis.

1.4 Contributions

The contributions of this thesis are presented as follows.

- Development of a detail circuit model for the transformer. The circuit elements are synthesized by a rational function which is fitted from the transformer frequency response.

- Validation of the frequency response measuring procedure and the circuit synthesis procedure. A test circuit with known elements is used to conduct the validation experiments. The comparison of measured data with simulation results confirmed the accuracy.

- Determination of the optimum resistor settings for the impulse generator using a Genetic Algorithm (GA) based Optimization-Enabled Electromagnetic Transient Simulation (OE-EMTS) approach. The circuit model of entire test setup is simulated in PSCAD/EMTDC which includes the impulse generator, multiple chopping gap, voltage divider and the derived model of the transformer. The simulated impulse waveforms are compared with the desired waveforms and the difference is used to calculate the objective function. The objective function is minimized and the optimum settings are obtained.

- Implementation of the obtained optimum settings on a real impulse generator and

conducting an impulse test on a three phase, 138/13.8 kV, Y-Δ, 60 Hz, 80 MVA transformer to confirm the accuracy of the approach.

- Introduction of a new impulse generator setup, which was not possible with the conventional trail-and-error method. This new setup gave the closest match to the desired waveform.

1.5 Thesis Outline

This thesis is organized as follows. In Chapter 2, a brief review of impulse waveforms and how to generate those waveforms are explained. The circuit models of test apparatus and their importances and operations are highlighted in this chapter. In Chapter 3, a methodology for the development of the transformer circuit model is described, consisting of frequency response measurements, rational function approximation and circuit synthesis. Additionally, the accuracy of both measurement procedure and method of circuit synthesis is validated using a test circuit. Chapter 4 is the core of this thesis which contains the GA based OE-EMTS approach. A step-by-step description of the genetic algorithm is presented. The accuracy of the optimization procedure is validated using two example circuits in this chapter. In Chapter 5, the results of three different case studies performed on a three phase, 138/13.8 kV, Y-Δ, 60 Hz, 80 MVA transformer have been summarized. Finally, Chapter 6 consists of the conclusion and future work of this research.

Chapter 2

Characterization and Generation of Impulse Waveforms

2.1 Characterization of Impulse Waveforms

Impulse waveforms in the high voltage context are usually unidirectional waveforms. These waveforms are rises quickly to a peak value and then falls less rapidly to zero. There are two major types of impulse waveforms based on the waveshape. They are the full impulse waveform and the chopped impulse waveform (see Fig. 2.1 and 2.2). Full impulse waveforms develop its complete waveshape without flashover, while chopped waveforms are a result of an occurrence of a flashover. This flashover can happen during the risetime or the falltime causing extremely rapid voltage fall. If it is during the risetime it is considered as a front chopped waveform and if it is during the falltime, it is considered as a tail chopped waveform. The rapid fall may have a very severe effect on power system equipment compared to the full waveform [2].

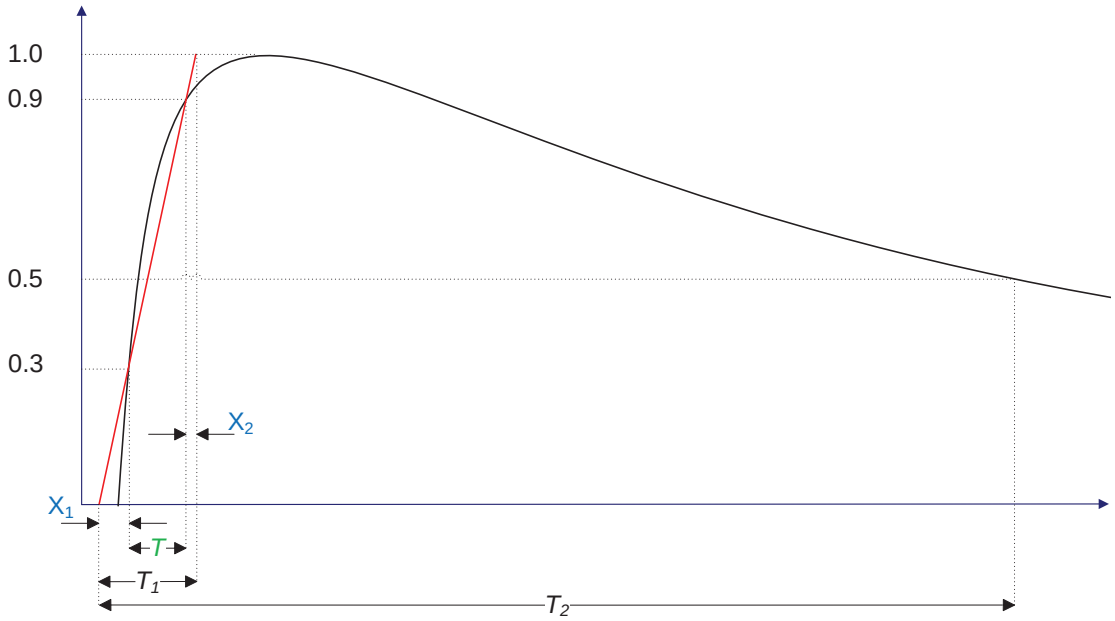


Figure 2.1: General shape and definitions of full impulse waveform. T_1: risetime and T_2: falltime [1].

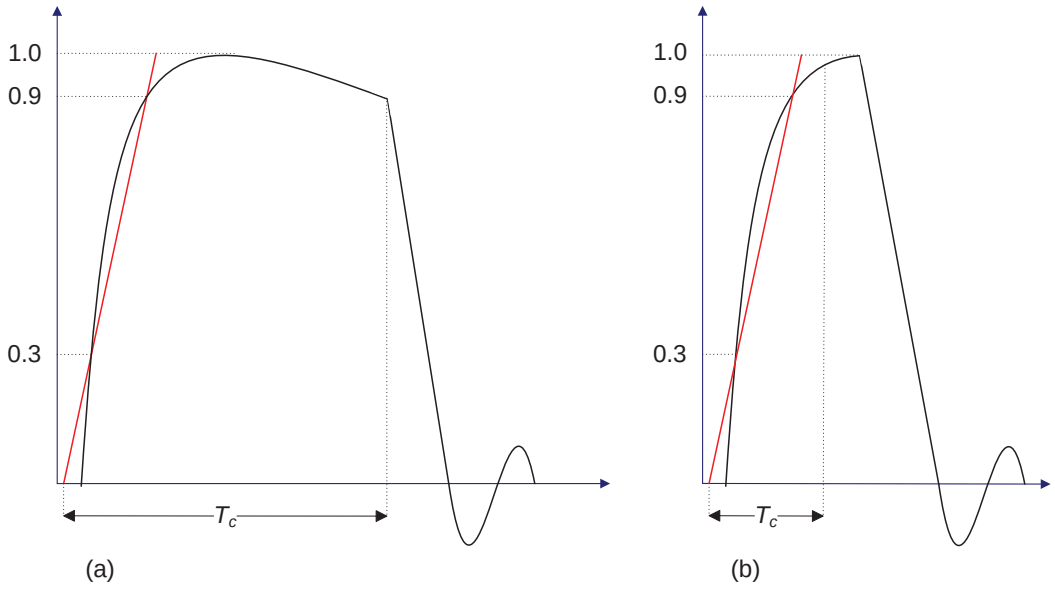


Figure 2.2: General shape and definitions of chopped impulse waveforms: (a) chopped on the tail, (b) chopped on the front, T_c: time to chopping [1].

It is important to know the risetime and the falltime of an impulse waveform, as they directly affect the severity of the damage that can be caused on equipments in the power system. In the Fig. 2.1, the time T_1 refers to the risetime of the waveform and time T_2 refers to the falltime of the waveform. The calculation of time T_1 can be done as follows.

$$K = \frac{0.9V_p - 0.3V_p}{T} = \frac{0.6V_p}{T} \tag{2.1}$$

$$X_1 = \frac{1}{K} \times 0.3V_p = \frac{T}{2} \quad ; \quad X_2 = \frac{1}{K} \times 0.1V_p = \frac{T}{6} \tag{2.2}$$

Therefore,

$$T_1 = \frac{T}{2} + T + \frac{T}{6} = 1.67T \tag{2.3}$$

In (2.1), K refers to the slope of the red line which connects the two points with 30% and 90% of peak magnitude. V_p refers to the peak of the impulse waveform.

Generally, an impulse waveform is denoted by their risetime and falltime. International standard organizations have defined some standard impulse waveforms (risetime/falltime : 1.2/5 μs, 1.2/50 μs, 1.2/200 μs, 250/2500 μs) for regular testing [3, 4]. These values have been derived from the data extracted from natural phenomenons like lightning, switching, etc. Among those waveforms 1.2/50 μs and 250/2500 μs waveforms are considered as standard lightning and switching impulses respectively.

2.1.1 Lightning Impulse

As described earlier, the standard lighting waveform is defined as 1.2/50μs waveform. Even though natural lightning waveforms may not have exactly these time values, definition of 1.2/50μs waveform helps to set up a standard waveform for testing purposes.

If a lighting induced overvoltage waveform travels for a relatively long distance (more than the distance travel within 50μs) along a transmission line before it reaches a terminal equipment, the waveshape may approach the full wave. If during the travel a flashover occurs after the peak of the wave, the wave may become a tail chopped wave. If the lightning stroke directly hits the transformer or any electrical equipment terminals, the impulse voltage rises rapidly and occurs a flashover on or before the peak of the waveform. These incidents may form the front chopped waveshape. The effect of these waveforms on a device's insulation mechanism may be different from each other. All of them can cause insulation failures in power system equipments.

2.1.2 Switching Impulse

The research studies and observations have shown that a typical switching over voltage may have a risetime of 250 μs and a falltime of 2500 μs. Although the switching surges have different forms and sources, they all are low frequency events usually within a spectrum of under kHz range. The amplitude of an average switching surge is about 2.5 per unit (p.u.). Most of the time they are associated with a change in the operating state of the system caused by a switching event. Unlike the lightning surge,

the switching surge is generally self induced by the operation of a breaker, switch or disconnect switch [11].

The reason for existence of switching surges is due to the inductance and capacitance of the power systems. Whenever the status of a reactive component is changed (added or removed), the system finds a new stable point. This change of operating point is the cause for creation of switching impulses. Since the switching surges are generally low in magnitude and slow in frequency, they act differently on the system compared to lightning. Due to the traveling wave phenomena, a switching surge generated in one location can affect an equipment located at hundreds of km away.

Therefore, terminal equipments should posses a good insulation mechanism to avoid impulse flashovers. To check the insulation strength of an electrical device, it is essential to conduct an impulse test.

2.2 Generation of Impulse Waveforms

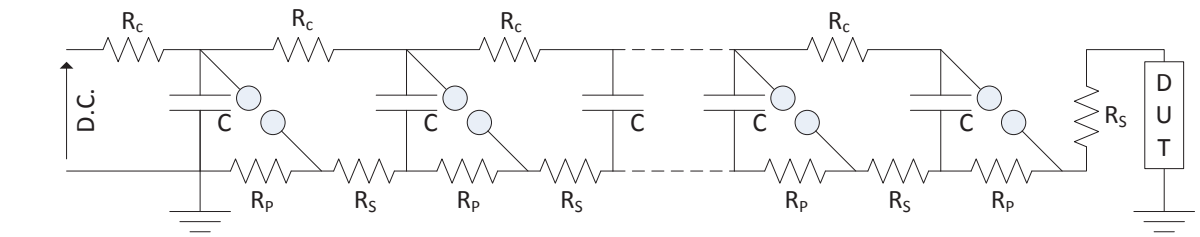
The apparatus which generate impulse waveforms in the laboratory are called impulse generators or Marx generators. The Marx generator is an electrical circuit first introduced by Erwin Otto Marx in 1924 (see Fig. 2.3 a). It generates high-voltage impulses from a low-voltage DC supply. First, Marx generator charges number of capacitors (C) in parallel through resistors R_C (see Fig. 2.3 b) and then discharge them in series by triggering set of sphere gaps (see Fig. 2.3 c). This discharge process charge the DUT (Device Under Test) by making the front portion of the impulse waveform (up to the the peak of the waveform). The resistors whose in the path of

discharge current are called "front resistors" (R_S) and determine the risetime of the waveform. Subsequently, the charged DUT discharges to the ground via resistors (R_S and R_P) by making the tail portion of the impulse waveform (see Fig. 2.3 d). Since the front resistors R_S are already set as per the desired risetime, the resistors R_P which are called as "tail resistors" determine the falltime of the waveform.

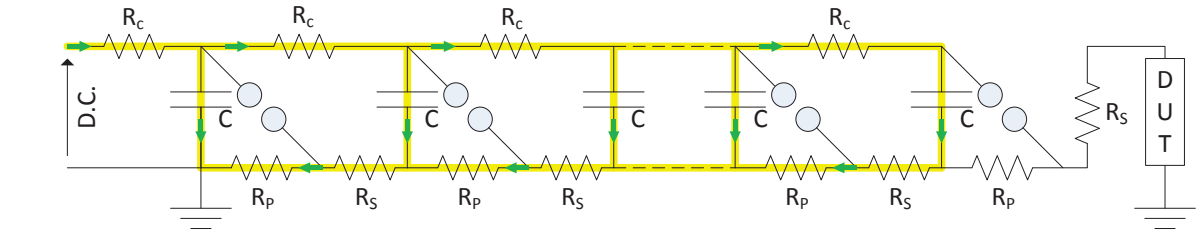
The combination of impulse generator, DUT and other necessary equipment is called an impulse test setup. It is very important to make the impulse test setup cautiously and accurately to generate those standard waveforms in the laboratory. The correct test setup ensures a stable and an accurate output. The key factors of consideration are grounding connections, terminal connections and external clearances [3,4]. The main idea of this physical setup is to minimize the unwanted noise and the error in the recorded impulse waveform which can be caused from high voltages and high frequency currents.

In a typical impulse test setup, there are four key components. Namely, an impulse generator, a multiple chopping gap, a DUT (a transformer in this work) and a voltage divider. Fig. 2.4 illustrates a schematic of a test setup with these components. All these components contributes to the parameters of the generated impulse waveform. Therefore, settings of the impulse generator need to be adjusted while connected to the entire test setup, not only based on the DUT.

In this thesis, this actual test setup is simulated by their circuit models as a part of the impulse generator setting optimization procedure. The circuit models of all components, except for the transformer, are modeled as per the circuit diagrams given in their manuals [10]. The circuit model of the transformer is developed as described



(a)



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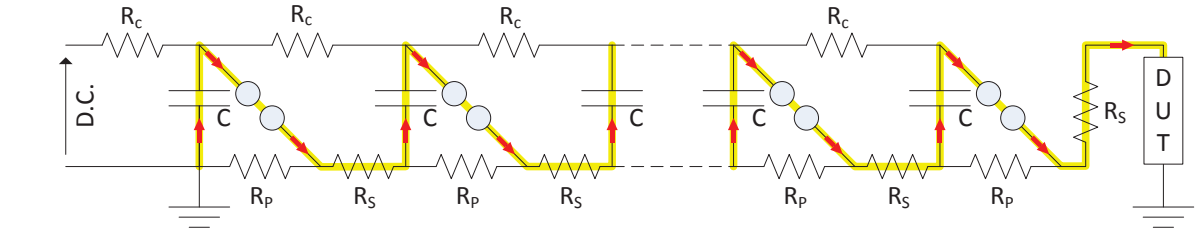

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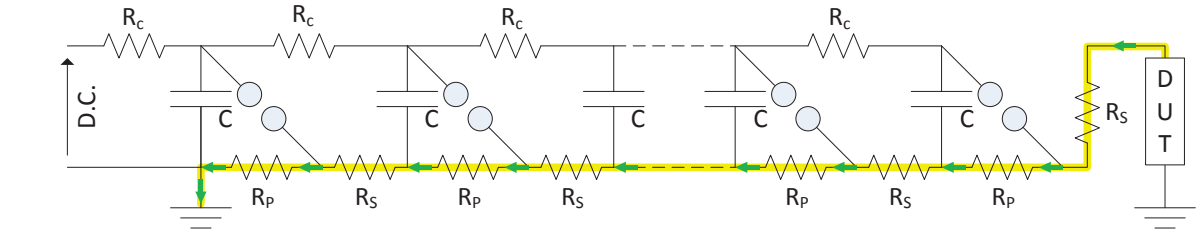


(d)

Figure 2.3: (a) A circuit diagram of a typical Marx Generator, (b) Parallel charging of impulse capacitors, (c) Series discharging of impulse capacitors, (d) Discharging of charged DUT to the ground

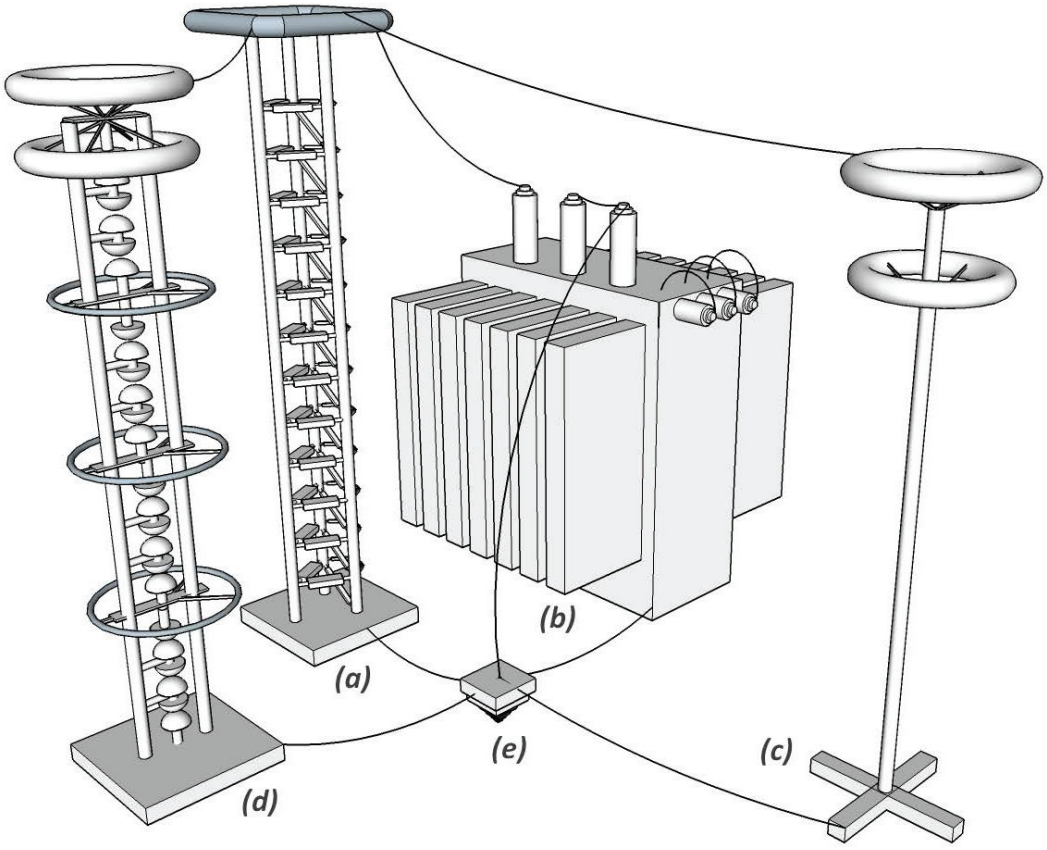
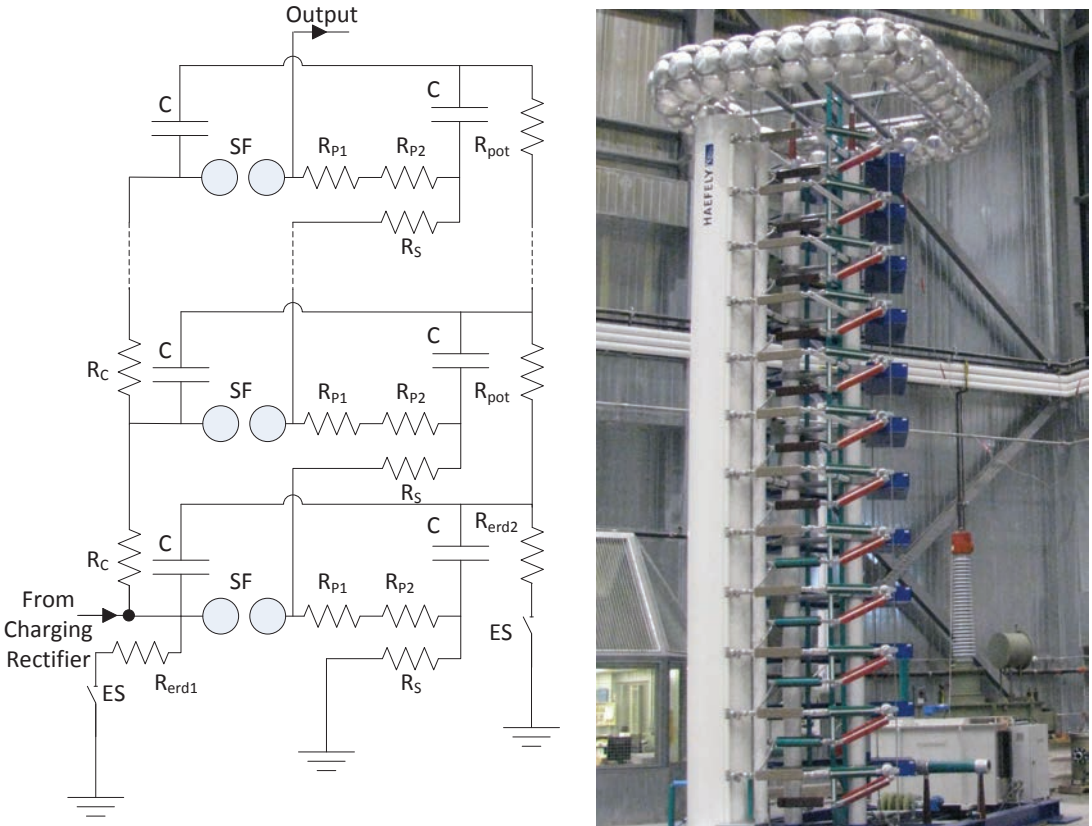


Figure 2.4: Overall impulse test setup: (a) Impulse Generator, (b) Power Transformer, (c) Voltage Divider, (d) Multiple Chopping Gap, (e) Grounding Grid of the Test Laboratory.



(a) (b)

Figure 2.5: a) Circuit diagram and b) a snapshot of the multi stage impulse generator. Courtesy of Manitoba Hydro High Voltage Test Facility.

in the chapter 3. A detail description of each item with their circuit models are presented below.

2.2.1 Impulse Generator

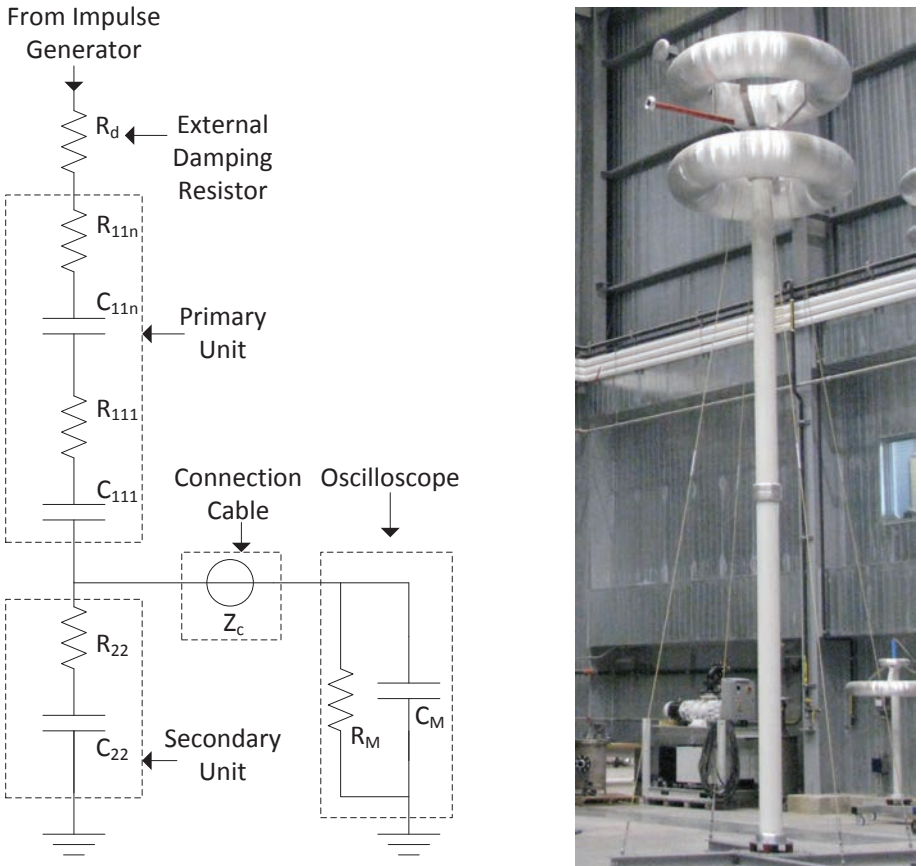
The circuit model and a snapshot of the real impulse generator used in this thesis are shown in Fig. 2.5. The operation of the impulse generator is presented as follows. The impulse capacitors (C) are charged in parallel through the charging resistors (R_C). When the charging voltage has reached the required value, breakdown of the first

stage's sparkgap (SF) is initiated by an external triggering pulse. When it breaks down, the potential of the following stage rises and breaks down the second stage spark gap. Thus, the sparkgaps are caused to break down in sequence. Consequently, the capacitors are discharged in series-connection via front resistors (R_S) by generating the front portion of the impulse waveform. This discharge process charges the load capacitance till the peak of the impulse waveform. This load capacitance includes the capacitances of the transformer, voltage divider, multiple chopping gap and the parasitic capacitances. After that, the load capacitance is discharged to the ground via tail resistors ($R_P = R_{P1} + R_{P2}$) by making the tail portion of the waveform. The earth switches (ES) along with damping resistors or discharge resistors (R_{erd1} and R_{erd2}) are used to make the ground connections to neutralize the remaining charge after a complete operation.

The required peak voltage is obtained by selecting a suitable number of serially connected stages and by adjusted the charging voltage. In order to obtain the necessary discharge energy, parallel or series-parallel connections of the generator can be used. The required waveshape is obtained by suitable selection of the front and tail resistors of the generator. A detailed technical specification of the impulse generator can be found in Appendix A.1.

2.2.2 Voltage Divider

The voltage divider steps down the impulse voltage to a measurable value. Apart from stepping down the voltage, the divider act as a capacitive load for the impulse generator. The circuit model and a snapshot of the damped capacitive voltage divider



(a) (b)

Figure 2.6: a) Circuit diagram and b) a snapshot of the damped capacitive voltage divider (Type CR). Courtesy of Manitoba Hydro High Voltage Test Facility.

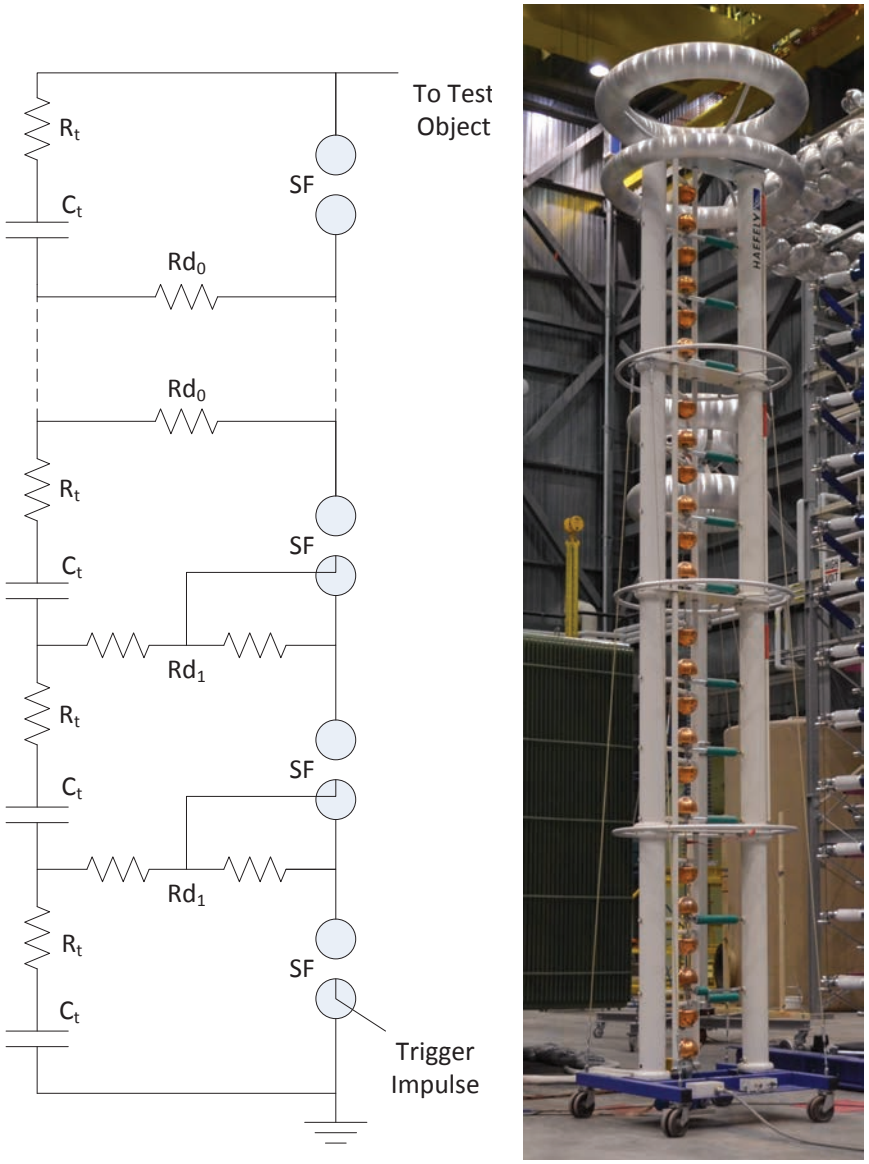
(type CR) used in this thesis is shown in Fig. 2.6. The feature of this model is that both the primary and the secondary units consist of a serially connected capacitor, resistor segments which support better readings for full lightning impulse voltages, tail chopped impulse voltages, switching impulses and AC voltages.

Based on the voltage rating, the high voltage part of the divider consists of one or several oil-filled capacitors (C_{11n} and C_{111}). The damping resistors (R_{11n} and R_{111}) are inserted between the capacitor units to act as distributed internal resistive elements. An external damping resistor (R_d) is also used for voltages above 1600 kV. The high voltage electrode is made in the shape of a toroid to guarantee a discharge-free operation. The secondary unit consists of a capacitor (C_{22}) and a damping resistor (R_{22}), both arranged in a coaxial design. This unit is fixed at the bottom of the divider and can easily be exchanged. The divider and the oscilloscope is connected via a coaxial cable with a characteristic impedance of 50 Ω. The oscilloscope's input resistance (R_M) and capacitance (C_M) are 1 MΩ and 20 pF respectively. A detailed technical specification of the voltage divider can be found in Appendix A.2.

2.2.3 Multiple Chopping Gap

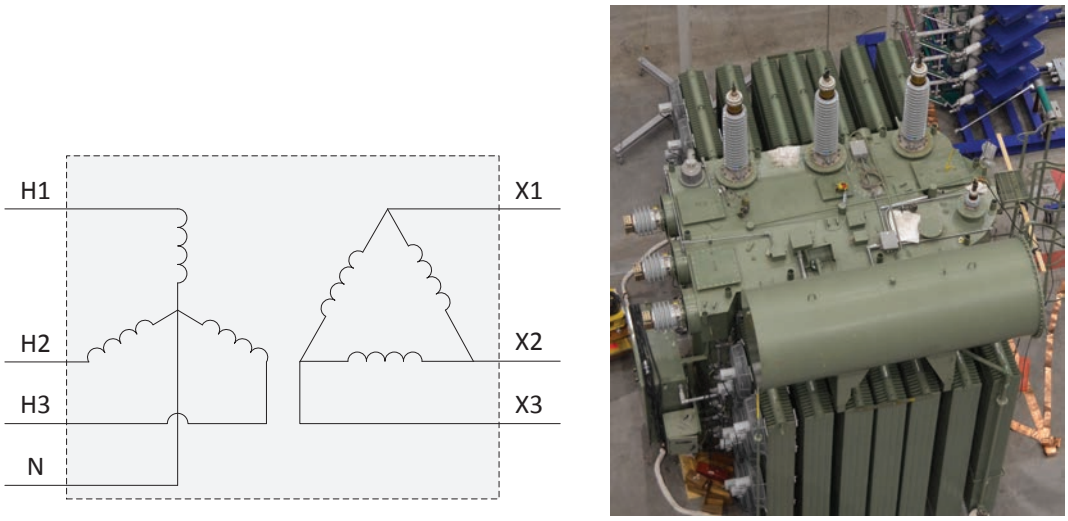
The multiple chopping gap is a device used to chop the impulse waveforms. Since the impulse generator setting optimization is limited to the full waveform in this thesis, the chopping gap is served only as a load capacitance in the test setup. This capacitance is considerably large and supports to reduce the overshoot of the waveform.

The chopping gap (see Fig. 2.7) consists of two columns, one is the support for sphere gaps (SF) and other one is a damped capacitance (sum of all C_t and R_t) to



(a) (b)

Figure 2.7: a) Circuit diagram and b) a snapshot of the multiple chopping gap. Courtesy of Manitoba Hydro High Voltage Test Facility.



(a) (b)

Figure 2.8: a) Power frequency circuit diagram and b) a snapshot of the transformer. Courtesy of Manitoba Hydro High Voltage Test Facility.

control the voltage distribution along the device. The lower sphere of each gap is assembled on a fix structure, whereas the upper spheres are assembled on a movable structure, which can move up or down to adjust the gap distance. Usually, the gap distance is set automatically according to the charging voltage. The upper sphere of one gap is connected to the lower sphere of the next gap via a damping resistor (Rd_0 or Rd_1) to a tap of the damped capacitor. The three bottom most spheres are equipped with a trigger pin for fast firing and to delay the chopping time reference to the beginning of the impulse. For the upper stages the natural over-voltages are sufficient to ensure a fast firing. A detail technical specification of the chopping gap can be found in Appendix A.3.

2.2.4 The Device Under Test - A Power Transformer

The device under test is the object whose insulation strength is checked by the impulse test. The DUT used in this thesis is a three phase, 138/13.8 kV, Y-Δ, 80 MVA power transformer. A detailed technical specification of the transformer can be found in Appendix A.4. The power frequency circuit diagram and a snapshot of the transformer is shown in Fig. 2.8. The derivation of the circuit model for the impulse test (the one which should build in the electromagnetic transient simulation) is explained in Chapter 3.

Generally, the DUT is the main contributor for the capacitive load in an impulse test. Since the circuit model of the DUT (in this thesis the transformer) is unique for each terminal, the capacitance contribution is different in each situation. Therefor settings for the impulse generator should be optimized based on the test terminal.

Chapter 3

Circuit Model Derivation of the Transformer

3.1 Literature Survey

It is essential to have a detailed circuit model or representation of the transformer to implement it in an EMTP-type program. In many papers, a model has been developed using the physical structure (geometric parameters) of the transformer. Usually, the aim of these models is to identify the deformation of transformer's geometry using the frequency response, *e.g.*, [12, 13]. A number of researchers have developed detailed models using frequency response analysis (FRA). In that approach, the parameter modeling was done by finite element analysis (FEA) or analytic methods [13,14]. The accuracy of these methods depends heavily on the transformer's internal dimensions and material properties which are typically unavailable [13,14]. Further, some models are confined only to a single phase transformer which hinders modeling of most large

power transformers [15–17]. In [18], a three phase circuit model is developed directly from the FRA data, however, the main focus of the model is on core parameter identification and is not valid for the entire impulse frequency spectrum.

In the method proposed in this thesis, the modeling of the transformer has been carried out by means of rational function approximation of FRA data and circuit synthesis [19]. FRA is one of the most popular methods to diagnose the mechanical integrity of power equipments. *e.g.*, [20, 21]. Typically, it is used to identify any dislocation or deformation of transformer windings. The frequency response is highly sensitive to the configuration of the transformer winding, because even minor changes in the winding geometry would affect the winding inductance and capacitance. Generally, the transformer manufacturer (or sometimes the end user) records the frequency response of the transformer before it undergoes a change. This change can be an electrical fault or a mechanical fault. After the fault, again the frequency response is recorded and compared with the original one. The differences between them indicate that mechanical and electrical changes occurred inside the transformer [22–24]. Currently this is popular in identifying the winding deformations occurred during transportation. In this thesis, FRA data has been used to obtain a circuit model for the transformer. The accuracy of the model is tested by comparing it with the measured data and simulation results.

There are three major steps in the transformer modeling process. Namely, measurement of frequency response, rational function approximation and circuit synthesis which are discussed in detail in the following.

3.2 Measurement of Frequency Response

In this section, two major topics are discussed as follows. First, a comprehensive procedure to measure the frequency response of the transformer is presented. Then, the accuracy of the developed procedure is validated using a test circuit. A detailed descriptions of each topic are presented in section 3.2.1 and section 3.2.2 as follows.

3.2.1 Frequency Response Measurement Procedure

The frequency response of the transformer under test is recorded using a Sweep Frequency Response Analyzer (SFRA). According to the standards for impulse test of power transformers ([3], [4]), all the terminals except the test terminal should be grounded during an impulse test. The same connection configuration is used to record the frequency response of the transformer. Fig. 3.1 shows the connection diagram used to record the frequency response of terminal H1. This ensures the circuit model to be developed gives the same response as the real transformer under considered connections to the given input signal.

The frequency response of the transformer is recorded over a wide range of frequencies which covers the spectrum of the (lightning) impulse waveform. The SFRA records both the magnitude and the phase of Vm/Vr. It has the ability to record 20,000 logarithmically spaced samples within its bandwidth. A commercial SFRA[1] with a bandwidth of 1 Hz to 2 MHz is used for this application [25]. Snap shots of SFRA and its accessories are shown in the Fig. 3.2. In Fig. 3.1, the 50 Ω re-

[1]FRAX 101 by Megger Sweden AB (A detailed technical specification of the device can be found in Appendix A.5)

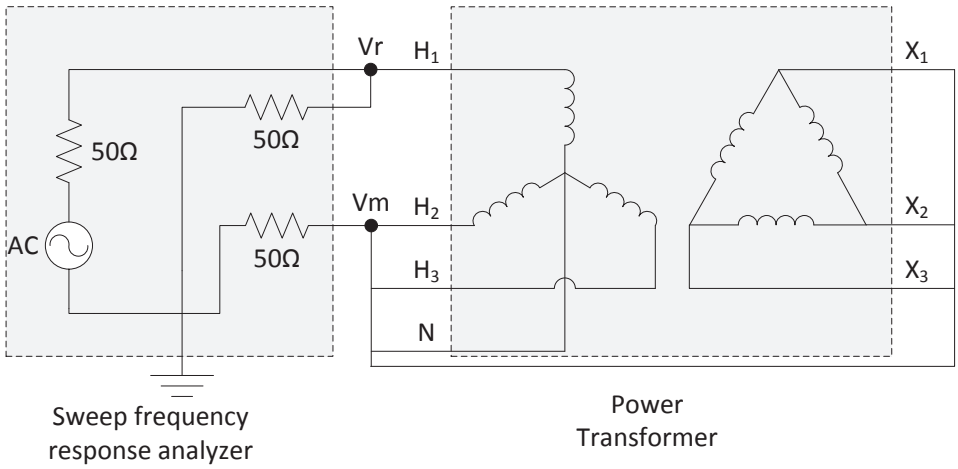


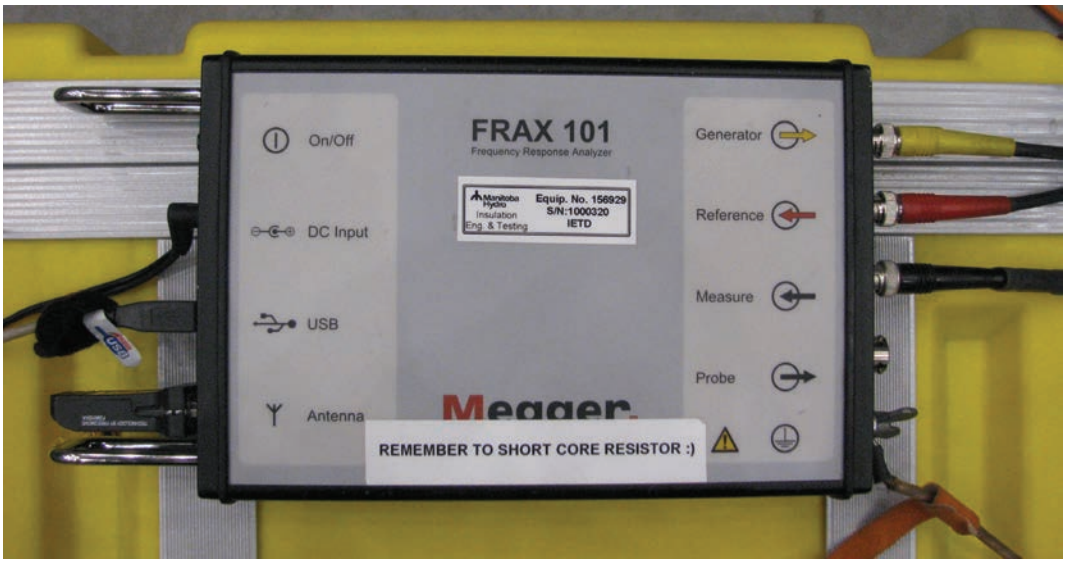
Figure 3.1: Connection schematic for frequency response measurement of the high voltage winding H1 of a three phase transformer.

sistors represent the internal resistor and terminations of the SFRA. Calibration of the SFRA is done prior to the test and the errors that are caused by the admittance of connection cables and clamps are compensated by the calibration results. In the calibration test, all three outputs (generator, reference and measure. see Fig. 3.2 (a)) are connected together and voltage ratios are recorded as usual. Fig. 3.3 shows the connection diagram of SFRA which is made for calibration test. The total admittance of connection cables and clamps is calculated as follows.

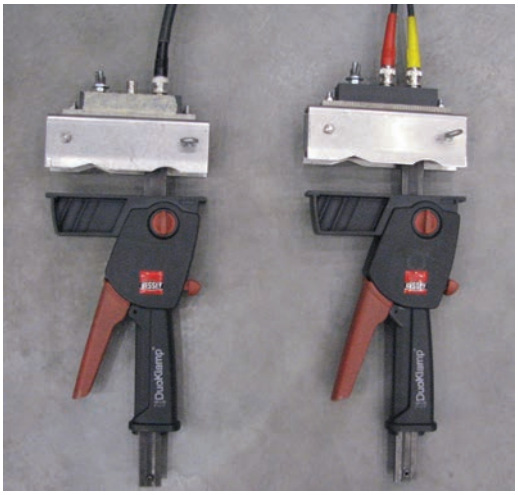
$$\frac{Vm}{Vr}_{cal} = 10^{(|Vre_c|/20)} \times e^{j\angle Vre_c} \tag{3.1a}$$

$$\frac{1}{Y_{cal}} = \frac{50\left(1 - \frac{Vm}{Vr}_{cal}\right)}{\frac{Vm}{Vr}_{cal}} \tag{3.1b}$$

Therefore, the input admittance of the transformer can be calculated as follows.



(a)



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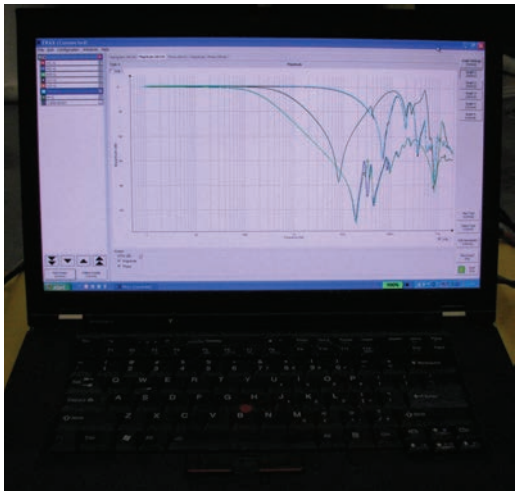


(c)

Figure 3.2: a) Sweep Frequency Response Analyzer (SFRA), b) connection clamps that are used to connect the SFRA cables to the transformer terminals and c) Frax-101 software interface. Courtesy of Manitoba Hydro High Voltage Test Facility.

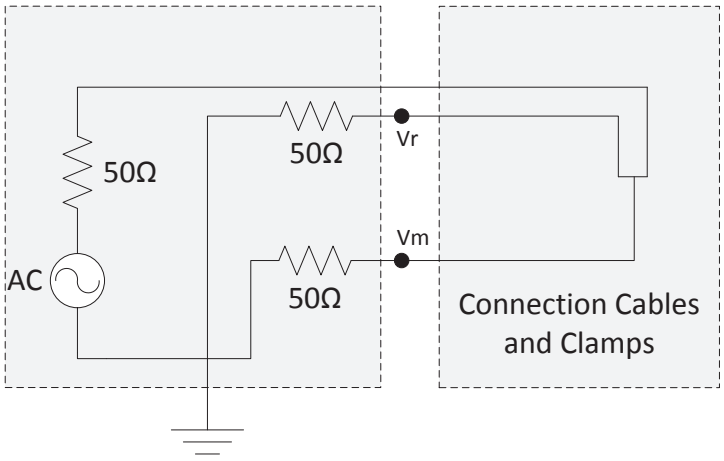


Figure 3.3: Connection schematic for calibration of SFRA.

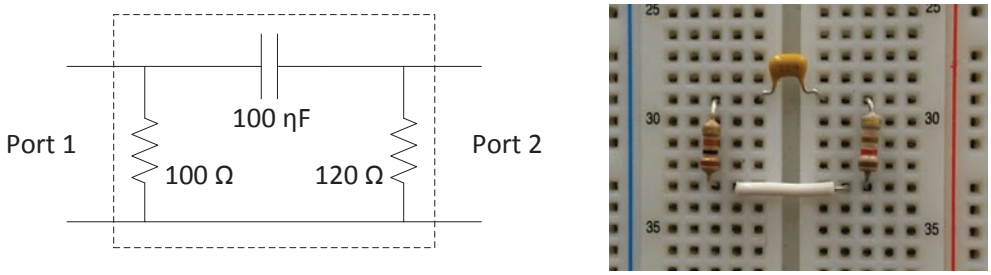
$$\frac{Vm}{Vr}_t = 10^{(|Vre_t|/20)} \times e^{j\angle Vre_t} \tag{3.2a}$$

$$\frac{1}{Y}_t = \frac{50\left(1 - \frac{Vm}{Vr}_t\right)}{\frac{Vm}{Vr}_t} - \frac{1}{Y_{cal}} \tag{3.2b}$$

where, Y_{cal} and Y_t are represented the admittance of connection cables and input admittance of the transformer, respectively. Vre_c and Vre_t are the corresponding recorded voltage ratios of the calibration test and the actual sweep frequency response test of the transformer. The above measurement procedure is repeated for all frequency samples and the calculated admittance is stored in an array with its corresponding frequency.

3.2.2 Validation of Measurement Procedure

It is important to check the accuracy of the measuring procedure before it is applied to a real transformer. For this purpose, a two port test network with two resistors



(a) (b)

Figure 3.4: a) Circuit diagram and b) a snapshot of the test circuit which used to validate the frequency response measurement procedure.

and a capacitor is constructed in a breadboard as shown in Fig. 3.4. The admittance matrix is derived as explained below and results are compared with the analytical solution.

Calculation of Input Admittance of the Test Circuit

Three different connection arrangements are introduced to calculate the admittance matrix elements (Y_{11}, Y_{22} and Y_{12}) of the test circuit. All connection arrangements are made carefully such a way that those do not violate the two port network theory [26]. As shown in the Fig. 3.5, an SFRA is connected to the test circuit and the magnitude and the angle of Vm/Vr for each frequency are recorded. Then the admittances are calculated using the two port network theory as follows.

- Y_{11} *Calculation*

  From the two port network theory (see Fig. 3.5 (a)),

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3.3}$$

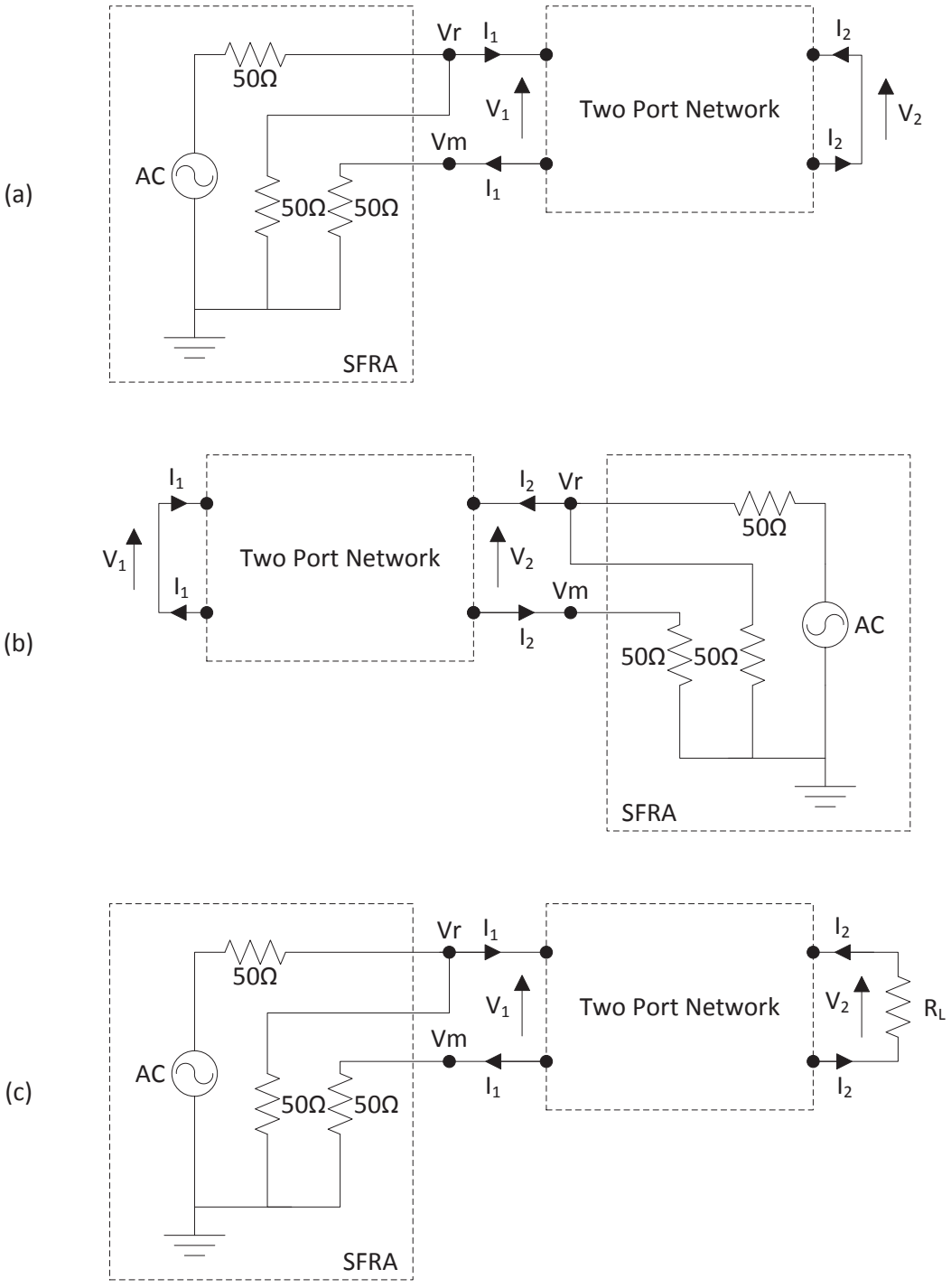


Figure 3.5: SFRA connection diagram of test circuit for the calculation of a) Y_{11}, b) Y_{22} and c) Y_{12}.

Since $V_2 = 0$ we have that,

$$Y_{11} = \frac{I_1}{V_1} = \frac{Vm/50}{Vr - Vm} \tag{3.4}$$

$$Y_{11} = \frac{Vm/Vr}{50\,(1 - Vm/Vr)} \tag{3.5}$$

Where,

$$\frac{Vm}{Vr} = 10^{(|V_{y11}|/20)} \times e^{j\angle V_{y11}} \tag{3.6}$$

In (3.6), V_{y11} refers to the recorded voltage ratio of Fig. 3.5 (a).

- *Y_{22} Calculation*

Calculation of Y_{22} is almost same as Y_{11} calculation as explained in the previous section. The only change made in the SFRA connection diagram is to switch ports 1 and 2.

- *Y_{12} Calculation*

From the two port network theory (see Fig. 3.5 (c)),

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{3.7}$$

$$I_1 = Y_{11} \cdot V_1 + Y_{12} \cdot V_2 \tag{3.8}$$

$$I_2 = Y_{21} \cdot V_1 + Y_{22} \cdot V_2 \tag{3.9}$$

$$\frac{I_1}{V_1} = Y_{11} + Y_{12} \cdot \frac{V_2}{V_1} \tag{3.10}$$

$$\frac{I_2}{V_1} = Y_{21} + Y_{22} \cdot \frac{V_2}{V_1} \tag{3.11}$$

Writing $V = IR$ to the resistor which is connected in the port 2, gives

$$Y_L = \frac{1}{R_L} \tag{3.12}$$

$$I_2 = -Y_L \cdot V_2 \tag{3.13}$$

Substituting (3.13) in (3.11), yields

$$\frac{-Y_L \cdot V_2}{V_1} = Y_{21} + Y_{22} \cdot \frac{V_2}{V_1} \tag{3.14}$$

$$\frac{V_2}{V_1} = \frac{-Y_{21}}{Y_{22} + Y_L} \tag{3.15}$$

Substituting (3.15) in (3.10), we have that

$$\frac{I_1}{V_1} = Y_{11} + Y_{12} \cdot \left(\frac{-Y_{21}}{Y_{22} + Y_L} \right) \tag{3.16}$$

$$Y_{12} = \sqrt{\left(\frac{I_1}{V_1} - Y_{11} \right) (-Y_L - Y_{22})} \tag{3.17}$$

Calculation of I_1/V_1 is done similar to the "Y_{11} *Calculation*". Therefore, substituting I_1/V_1 from (3.5) in (3.17), yields

$$Y_{12} = \sqrt{\left(\frac{Vm/Vr}{50\,(1 - Vm/Vr)} - Y_{11} \right) (-Y_L - Y_{22})} \tag{3.18}$$

Where,

$$\frac{Vm}{Vr} = 10^{(|V_{y12}|/20)} \times e^{j\angle V_{y12}} \tag{3.19}$$

In (3.19), V_{y12} refers to the recorded voltage ratio of Fig. 3.5 (c). The calculation of Y_{12} is done after the calculations of Y_{11} and Y_{22}, since those values are needed in this calculation.

- *Analytical Calculation*

From the definition of nodal admittance matrix, we have

$$Y_{ij} = \begin{cases} y_{ii} + \sum_{i \neq j} y_{ij}, & \text{if } i = j \\ -y_{ij}, & \text{if } i \neq j \end{cases} \tag{3.20}$$

Therefore,

$$Y_{11} = \frac{1}{100} + j\omega 10^{-7} \tag{3.21}$$

$$Y_{22} = \frac{1}{120} + j\omega 10^{-7} \tag{3.22}$$

$$Y_{12} = -j\omega 10^{-7} \tag{3.23}$$

Where, ω being the angular frequency.

- *Simulation Results*

The same test circuit (Fig 3.4) is simulated in PSCAD/EMTDC and the magnitude and the angle of Vm/Vr for each frequency are recorded. Then, the same

method, that is explained in the section 3.2.2 is used to calculate the admittance matrices.

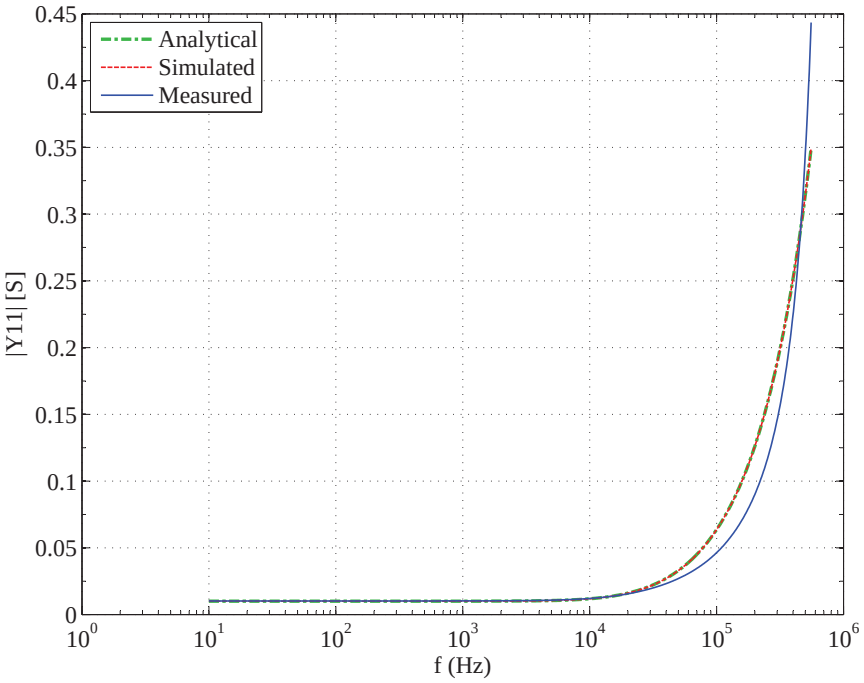
Comparison of Measured Admittances with Analytical and Simulated Results

Fig. 3.6, 3.7 and 3.8 shows a comparison of the magnitudes (a) and the angles (b) of Y_{11}, Y_{22} and Y_{12} for the analytical, simulated and measured results. As shown, all these graphs have a close response, in analytical and simulated results, confirming the accuracy of the frequency response measurement procedure.

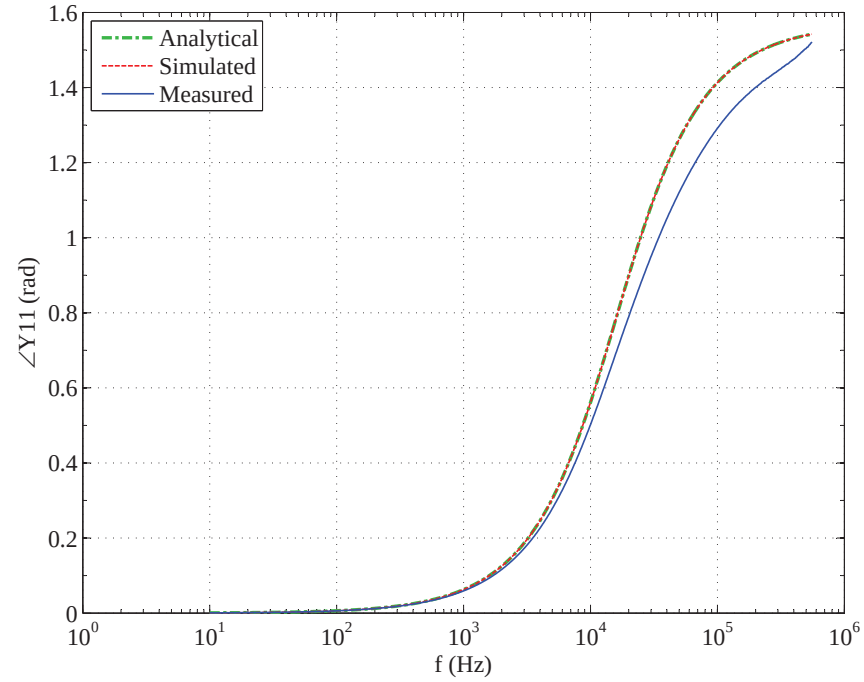
In all three cases, the measured admittance has been deviated from other two graphs in high frequencies. The reason for this deviation might be a parasitic effect which is neglected in the analytical and simulated solutions. Further, the increase of the deviation with the increasing frequency, confirms that this effect is from a capacitive element. Capacitance of the breadboard's conductive mesh can be considered as one of the main contributors for this deviation.

3.3 Rational Function Approximation of FRA Measurements

Many methods are available for rational function approximation of FRA measurements. Such as, Inverse Fourier Transform (IFT) [27], Inverse Fast Fourier Transform (IFFT) [27], rational interpolation technique [28] and Vector Fitting [29]. Compared to other methods, the vector fitting method offers acceptable convergence and better

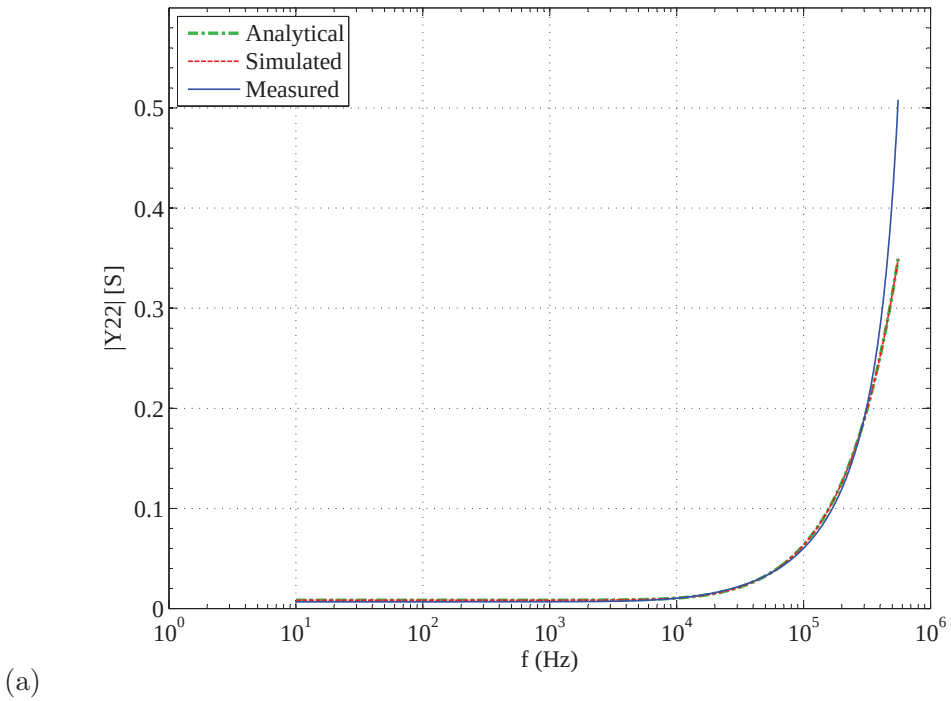


(a)

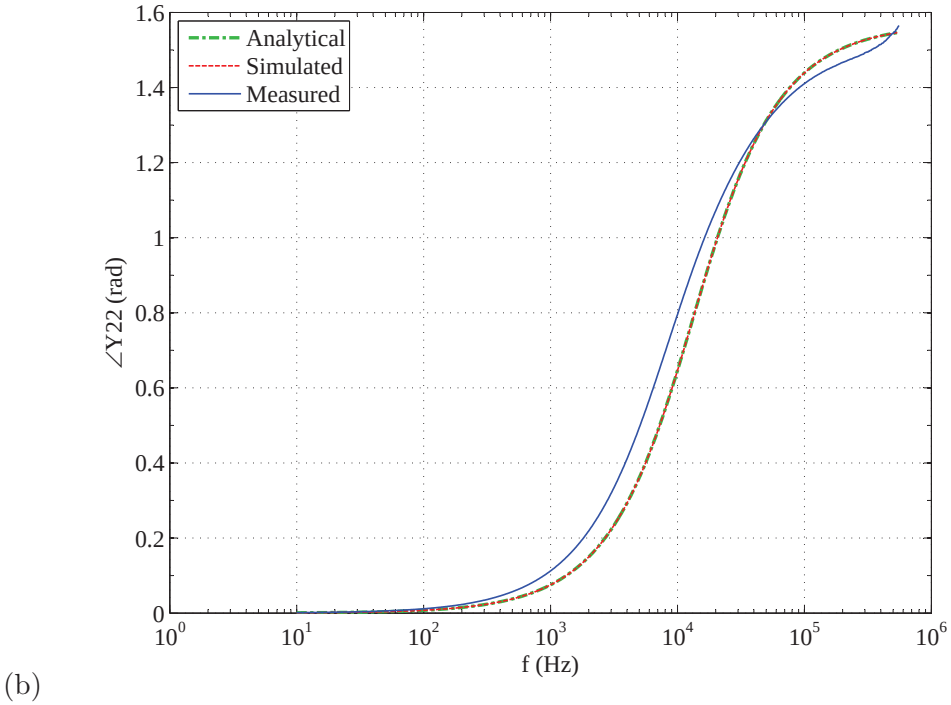


(b)

Figure 3.6: Variation of the a) magnitude and the b) angle of Y_{11} of the test circuit shown in Fig. 3.4.

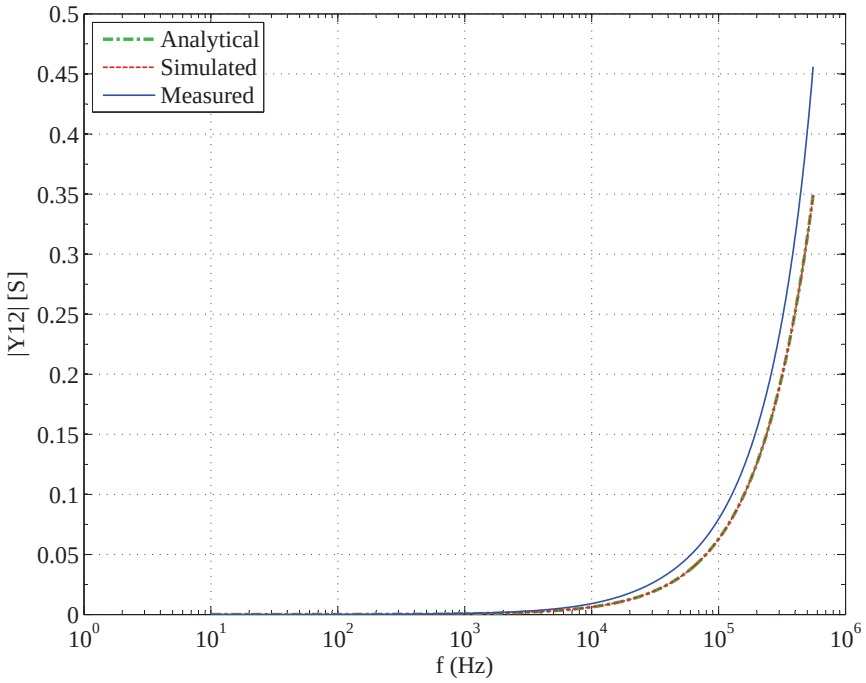


(a)

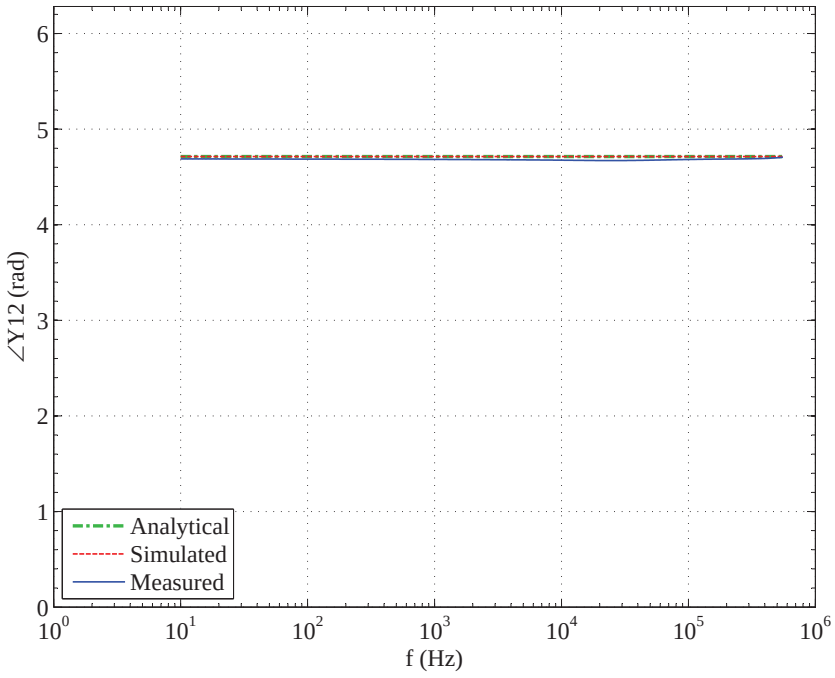


(b)

Figure 3.7: Variation of the a) magnitude and the b) angle of Y_{22} of the test circuit shown in Fig. 3.4.



(a)



(b)

Figure 3.8: Variation of the a) magnitude and the b) angle of Y_{12} of the test circuit shown in Fig. 3.4.

accuracy. Also, it can be used for systems with a large number of inputs and outputs.

Assume a rational function approximation for $Y(j\omega)$ as follows.

$$Y(j\omega) \cong \sum_{n=1}^{N} \frac{c_n}{j\omega - a_n} + d + j\omega e \tag{3.24}$$

where c_n and a_n represent the residues and poles, respectively. N is the order of the approximation and d and e are constants. Using Vector Fitting, all these coefficients (c_n, a_n, d and e) are determined in such a way that the error between fitted function and the measured frequency response is minimized. Normally, a higher number of poles gives a good fit to the measured data. One of the disadvantages in defining a large number of poles is that it increases the number of branches in the synthesized circuit. Further, sometimes large number of poles reduces the accuracy by trying to fit each and every point to a higher precision. Therefore, selecting the optimum number of poles is quite important.

After employing Vector Fitting, one of the concerns of the fitted vector is passivity. Since a power transformer is a passive element in reality, the fitted admittance also needs to be a passive. Therefore, a passivity check needs to be performed prior to the circuit synthesis to avoid unstable simulations.

3.3.1 Passivity Assessment

A system or network is considered as passive, only if the initial stored energy and energy delivered to the system is greater than or equal to zero. In other words, a passive system cannot generate any energy. There are several approaches based on

Hamiltonian matrix [30] to check the passivity of a system. The half-size singularity test matrix method [31] is one of the popular approaches, and is used in this thesis. It uses a matrix whose dimension is half that of the conventional Hamiltonian matrix. This significantly increases the computational speed due to reduction of the algorithmic complexity.

3.3.2 Passivity Enforcement

Non-passive models may be generated for passive circuits and systems due to various reasons, such as errors in the vector fitting program, reduced number of order in the rational function, etc [32]. Therefore, a post-processing passivity enforcement algorithm is desired. Passivity enforcement techniques are introduced as a solution to this problem. Some techniques are performed during the construction of state-space model. These methods require more computational time to recompute the residues and constant matrices till it obtains a passive model. In some techniques, the passive model is achieved either by perturbing eigenvalues of residues matrices, or eigenvalues of Hamiltonian matrices. These methods are fast in operation due to perturbing the eigenvalues of the residue matrices instead of perturbing matrix elements. The method used in this thesis is called "fast passivity enforcement by perturbation of residue matrix eigenvalues" introduced by Gustavsen [33].

In this thesis, for the rational function approximation, passivity assessment and for the passivity enforcement functions, the computer code developed by Gustavsen is used [34].

3.4 Circuit Synthesis

The objective of circuit synthesis is to obtain a network of RLC elements such that it has an admittance given by (3.24). Since it is derived from the frequency response of the system, the solution might not be unique, i.e. several networks can give the same frequency response with different circuit elements [19]. In this case, the circuit model for transformer is derived from the state-space model of the fitted vector. The used procedure of circuit element derivation is explained below. Further, the accuracy of the procedure is validated by two experiments conducted on the test circuit used in Section 3.2.2.

3.4.1 Derivation of the Circuit Elements

The coefficients of the approximated rational function is used here to calculate the circuit elements. The solution consists of a real constant, a complex constant, real poles and complex conjugate pole pairs. A schematic of a circuit with an admittance in the form of (3.24) is shown in the Fig. 3.9. The real constant and the complex constant give the element values of parallel resistor and capacitor (first two elements of the figure) respectively. The real poles represents the series RL branches while RLGC branches were results of complex conjugate pole pairs.

As explained in the section 3.3, the frequency response of the transformer can be approximated by a rational function as given in (3.24). Where, N is the total number of poles which consists of i number of real poles and k number of complex conjugate pole pairs as shown in the Fig. 3.9. The summation of three admittances is equal to

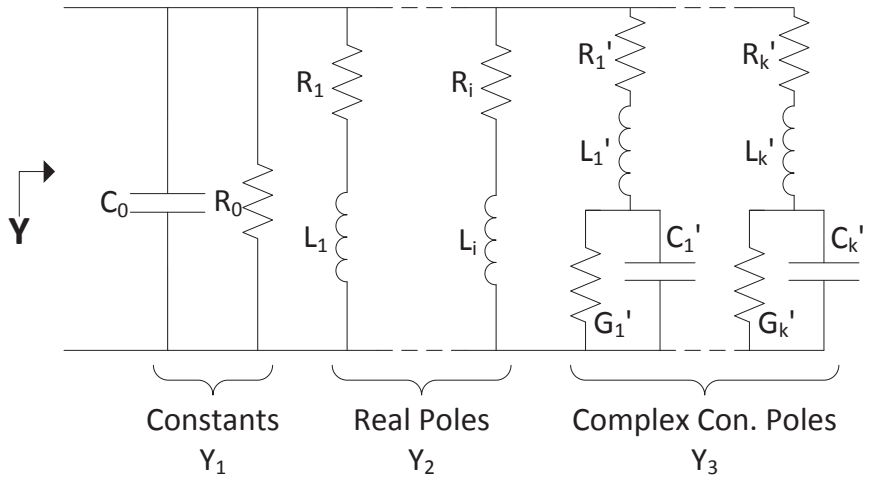


Figure 3.9: Circuit element arrangement of synthesized circuit for the transformer.

the total admittance which is represented by the rational function $Y_1 + Y_2 + Y_3 = Y$. The derivation of circuit elements are shown below.

Circuit Element Derivation From Constants (Y_1)

From circuit elements arrangement (see Fig. 3.9),

$$Y_1(j\omega) = \frac{1}{R_0} + j\omega C_0 \tag{3.25}$$

From rational function,

$$Y_1(j\omega) \cong d + j\omega e \tag{3.26}$$

By comparing (3.26) and (3.25), we get

$$C_0 = e \tag{3.27}$$

$$R_0 = \frac{1}{d} \tag{3.28}$$

Circuit Element Derivation From Real Poles (Y_2)

From circuit elements arrangement (see Fig. 3.9),

$$Y_2(j\omega) = \frac{1}{R_1 + j\omega L_1} \tag{3.29}$$

$$Y_2(j\omega) = \frac{\frac{1}{L_1}}{\frac{R_1}{L_1} + j\omega} \tag{3.30}$$

From rational function,

$$Y_2(j\omega) \cong \sum_{n=1}^{i} \frac{c_n}{j\omega - a_n} \tag{3.31}$$

By comparing (3.31) and (3.30), we get

$$a_n = -\frac{R_1}{L_1} \tag{3.32}$$

$$c_n = \frac{1}{L_1} \tag{3.33}$$

Therefore,

$$L_1 = \frac{1}{c_n} \tag{3.34}$$

$$R_1 = -\frac{a_n}{c_n} \tag{3.35}$$

Circuit Element Derivation From Complex Conjugate Pole Pairs (Series RLGC Branches)

From circuit elements arrangement (see Fig. 3.9),

$$Y_3(j\omega) = \frac{1}{(R'_1 + j\omega L'_1) + \frac{1}{G'_1 + j\omega C'_1}} \tag{3.36}$$

$$Y_3(j\omega) = \frac{G'_1 + j\omega C'_1}{L'_1 C'_1 (j\omega)^2 + (R'_1 C'_1 + G'_1 L'_1) j\omega + R'_1 G'_1 + 1} \tag{3.37}$$

$$Y_3(j\omega) = \frac{\frac{G'_1}{L'_1 C'_1} + j\omega \frac{1}{L'_1}}{(j\omega)^2 + \frac{(R'_1 C'_1 + G'_1 L'_1)}{L'_1 C'_1} j\omega + \frac{R'_1 G'_1 + 1}{L'_1 C'_1}} \tag{3.38}$$

From rational function (assumed $c_{n2} = c_{n1}^*$ and $a_{n2} = a_{n1}^*$),

$$Y_3(j\omega) \cong \sum_{n=1}^{k} \frac{c_{n1}}{j\omega - a_{n1}} + \frac{c_{n2}}{j\omega - a_{n2}} \tag{3.39}$$

$$Y_3(j\omega) \cong \frac{c_{n1}(j\omega - a_{n2}) + c_{n2}(j\omega - a_{n1})}{(j\omega - a_{n1})(j\omega - a_{n2})} \tag{3.40}$$

$$Y_3(j\omega) \cong \frac{-(c_{n1}a_{n2} + c_{n2}a_{n1}) + j\omega(c_{n1} + c_{n2})}{(j\omega)^2 - (a_{n1} + a_{n2}) j\omega + a_{n1}a_{n2}} \tag{3.41}$$

By comparing (3.41) and (3.38), we get

$$(c_{n1} + c_{n2}) = \frac{1}{L'_1} \tag{3.42}$$

$$-(c_{n1}a_{n2} + c_{n2}a_{n1}) = \frac{G'_1}{L'_1 C'_1} \tag{3.43}$$

$$-(a_{n1} + a_{n2}) = \frac{(R'_1 C'_1 + G'_1 L'_1)}{L'_1 C'_1} \tag{3.44}$$

$$a_{n1}a_{n2} = \frac{R'_1 G'_1 + 1}{L'_1 C'_1} \tag{3.45}$$

Solving (3.42), (3.43), (3.44) and (3.45) simultaneously, we get

$$R'_1 = -\frac{a_{n1}c_{n1} + a_{n2}c_{n2}}{(c_{n1} + c_{n2})^2} \tag{3.46}$$

$$L'_1 = \frac{1}{c_{n1} + c_{n2}} \tag{3.47}$$

$$G'_1 = \frac{(a_{n1}c_{n2} + a_{n2}c_{n1})(c_{n1} + c_{n2})^2}{c_{n1}c_{n2}(a_{n1} - a_{n2})^2} \tag{3.48}$$

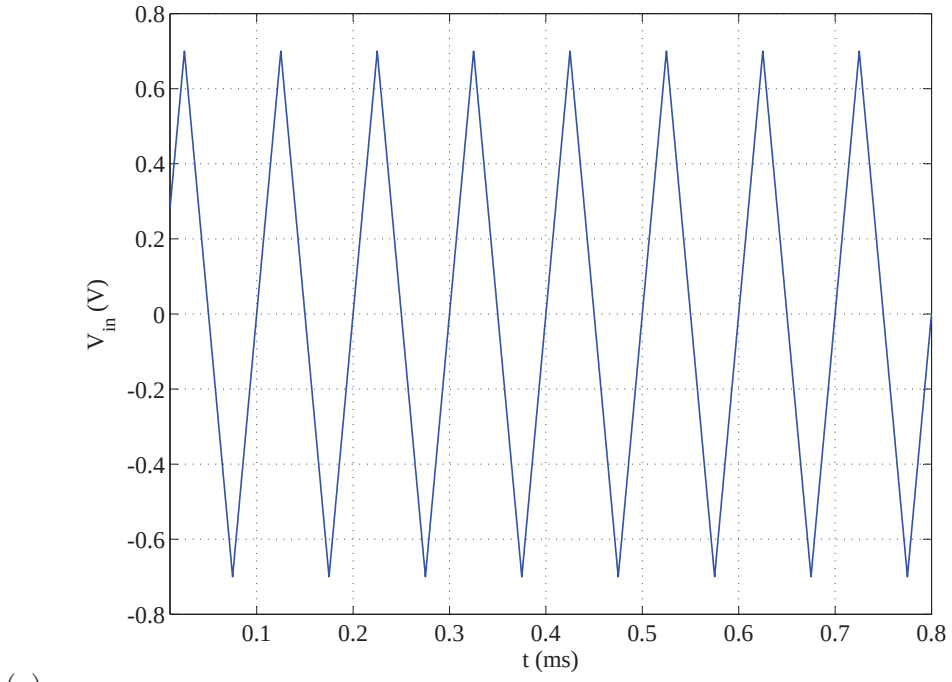
$$C'_1 = \frac{(c_{n1} + c_{n2})^3}{c_{n1}c_{n2}(a_{n1} - a_{n2})^2} \tag{3.49}$$

3.4.2 Validation of the Circuit Elements Derivation Procedure

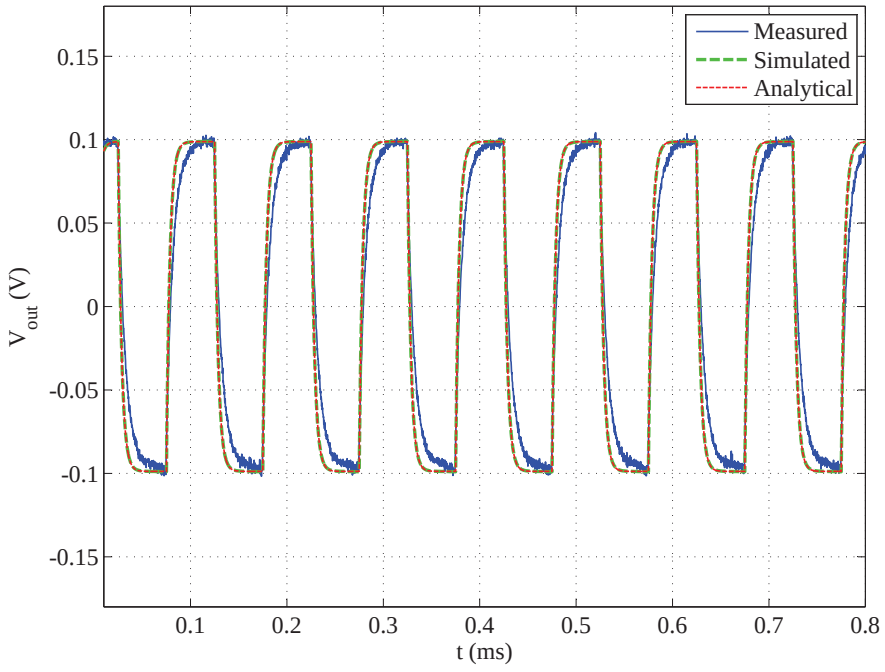
The test circuit (Fig. 3.4) which is used in Section 3.2.2 is also used here to validate the procedure for circuit elements derivation. Since the measurement procedure is already validated, the same admittance matrices (Calculated in Section 3.2.2) are deployed to synthesize the circuit elements. The approximation of rational function is done as described in Section 3.3 by assuming 20 number of poles (12 real poles and 4 complex conjugate pole pairs). The circuit synthesis is conducted according to the method which is described in Section 3.4.1 and results are tabulated in Appendix B.1.1.

The accuracy of the synthesized circuit is tested with two different case studies as follows. In the first case, port 1 of the test circuit is connected to an external signal generator/oscilloscope [2] [35] and a 10 kHz sawtooth waveform is applied. The output waveform is recorded from port 2. Similarly, the synthesized model of the test circuit is simulated in PSCAD/EMTDC with the same input waveform. In addition, the test circuit is simulated with their real element values instead of synthesized model. Fig. 3.10 shows the given input signal and the recorded output signals for all three situations. In the second case, the synthesized model of the test circuit is simulated with a Gaussian waveform (whose magnitude drops to 10% at 2 MHz) as the input. Similarly, the test circuit is simulated with real element values. Fig. 3.11 shows the given input signal and output signals for both situations.

[2] Agilent InfiniiVision 3024A (A detailed technical specification of the device can be found in Appendix A.6)

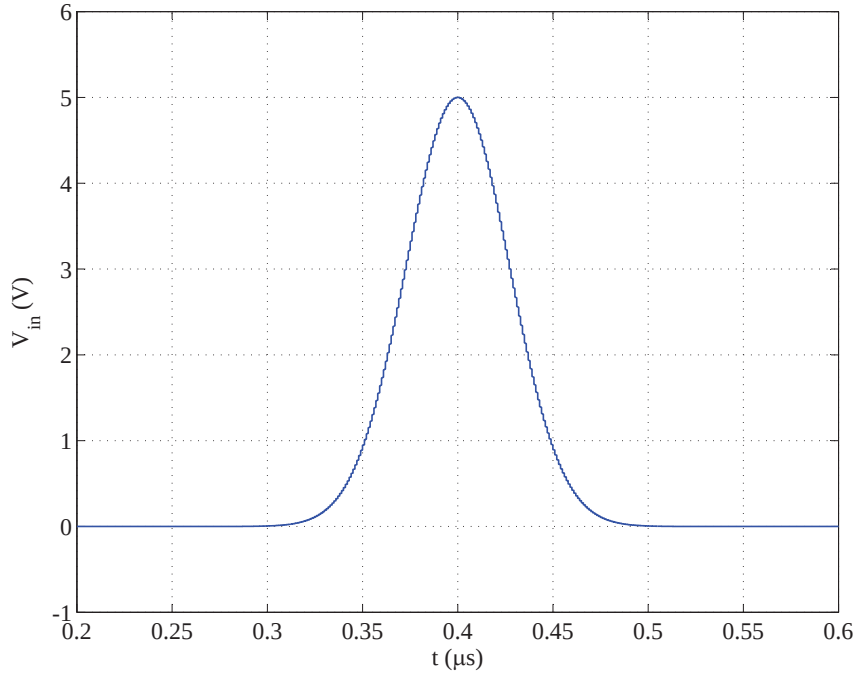


(a)

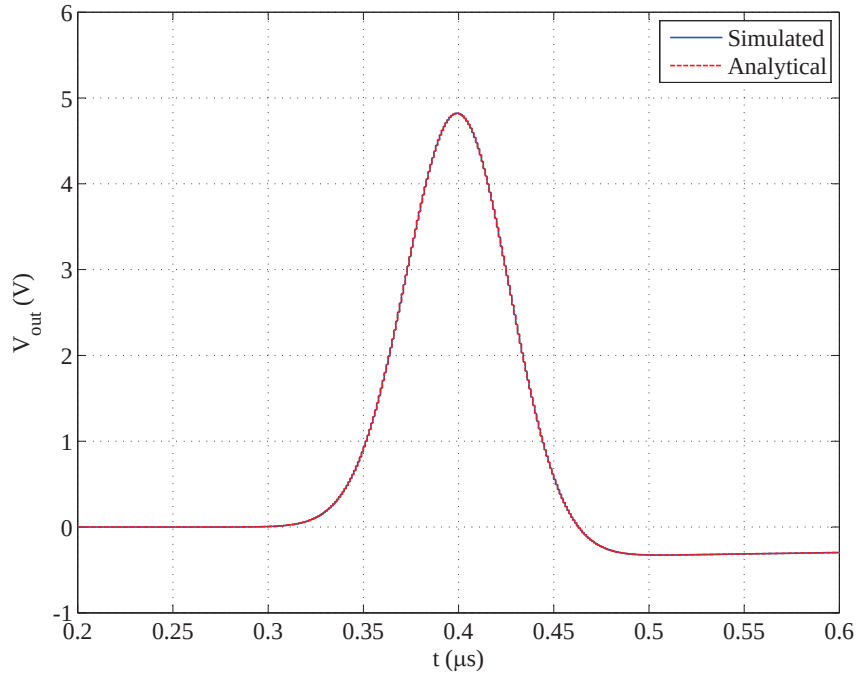


(b)

Figure 3.10: a) The 10 *kHz* sawtooth input signal given to port 1 and b) The recorded output signals of real, synthesized and analytical circuits at port 2 of the test circuit shown in Fig. 3.4.



(a)



(b)

Figure 3.11: a) The input Gaussian waveform (which magnitude drops to 10% at 2 *MHz*) at port 1 and b) The recorded output signals of synthesized and analytical circuits at port 2 of the test circuit shown in Fig. 3.4.

In both cases, the output of the synthesized circuit matches the analytical results. Further, in the first case, the recorded results from simulations are compared with a real measurement obtained from a laboratory experiment. As you can see from Fig. 3.11, those measurements also have given a good match to the simulation results by confirming the accuracy of the circuit synthesis procedure.

Validation of both measurement and circuit synthesis procedures (presented in Section 3.2.2 and Section 3.4.2, respectively) are used the same test circuit with two ports as shown in the Fig. 3.4. Even though the transformer which is used in this thesis is a three phase transformer, under the impulse test connection configuration, it acts as a single port network. Since the two port network is a combination of two single port networks, the validated procedures can be applied to a single port network as well. Therefore, the developed method is used to derive a circuit model for the transformer in case studies in Chapter 5.

Chapter 4

Optimization of Impulse Generator Settings

4.1 Literature Survey

As mentioned in Section 1.3, the main objective of this research is optimizing impulse generator settings to obtain desired impulse waveforms. The proposed approach for setting optimization is a Genetic Algorithm (GA) based Optimization Enabled Electromagnetic Transient Simulation (OE-EMTS) [36, 37]. The OE-EMTS can be divided into two main parts: an electromagnetic transient simulation program (EMTP-type program) and an optimization algorithm.

EMTP-type programs are useful tools for the analysis of transients in power networks. They allow the user to model various components that are part of a power system and test the entire power system for a range of transient conditions. Most of those programs are written to solve power system problems in the time domain. A few

programs, however, solve in the frequency domain, using Fourier Transform [38]. It is essential to have a time-domain solution to model nonlinear elements such as electronic switches, surge arresters, etc. In the proposed method, PSCAD/EMTDC [39] is used as the EMTP-type program which is operating in the time domain.

The other part of OE-EMTS is the optimization algorithm. There are several optimization algorithms which can be used to minimize an objective function. Among them, evolutionary algorithms (EA) are popular subcategory which is inspired by the biological mechanisms of evolution. There are several algorithms under EA, such as Genetic Algorithm (GA), Evolutionary Programming (EP), Evolution Strategies (ES), Genetic Programming (GP) [40, 41]. In this thesis, the genetic algorithm (GA) [42] is used as the optimization technique to obtain impulse generator settings. The GA mimics the process of natural selection. It simulate the survival of the fittest among families over consecutive generations for solving a problem. In the GA employed in this thesis, each generation consists of a population of binary bit strings that are analogous to the chromosome that we see in our DNA. Each family represents a point in a search space and a possible solution. The families in the population are then made to go through a process of evolution. The GA always deal with a set (population) of solutions at a time. These solutions are spread throughout the solution space, so the chance of reaching the global optimum is increased significantly. Further, each solution can consists any number of unknowns which are needed to be optimized. The GA uses objective function or fitness information only, compared with the more traditional methods that rely on existence and continuity of derivatives or other auxiliary information. In addition, GA does not necessarily guarantee that

the global optimum solution will be reached, although experience indicates that they will give near-optimal solutions after a reasonable number of evaluations.

In the proposed method, the GA which is running in a numerical environment[1] employs the PSCAD/EMTDC[2] as the engine of the optimization process. The GA is interfaced with the PSCAD/EMTDC to exchange data in each run. The input for the simulation is set as the resistor values and the output is configured as the simulated waveform. The difference between simulated and desired waveforms is set as the objective function and minimized through an iterative manner.

4.2 Evolution of Genetic Algorithm

The GA used in this thesis is written especially for the specific task of optimization of resistor values in MATLAB. In that, the unknown resistor values are presented as family members. A population consists of families which include members. The number of family members is equal to the number of unknowns (i.e., resistor values to be optimized). The number of families in the population is arbitrary fixed as the population size. The value of a family member (which is the value of a resistor) is coded to a string of binary bits, whose length is set as per the number of resistor values in the impulse generator. This changes the granularity of resistor values in the GA. At the beginning of GA process, an initial population is created randomly and then evolves through set of genetic operators as shown in Fig. 4.1. "Crossover" and "mutation" operators introduce changes to the initial population. Then fitness

[1]MATLAB R2013b (8.2.0.701) by The MathWorks, Inc.
[2]PSCAD/EMTDC version 4.5.3.0 by Manitoba HVDC Research Centre

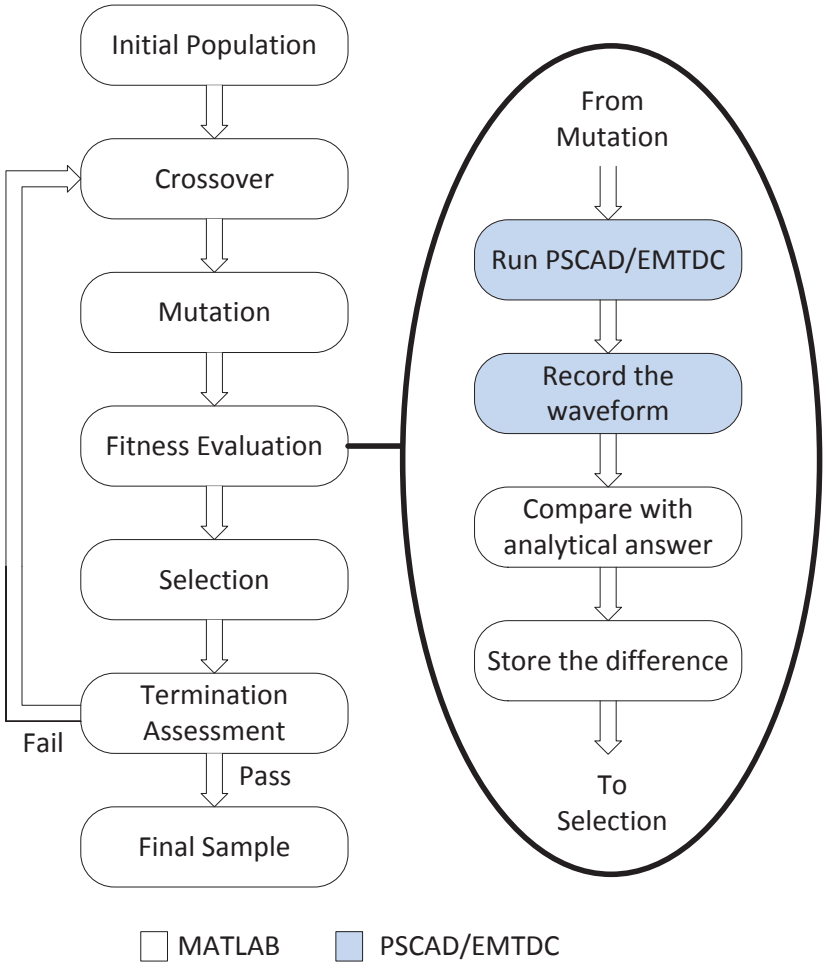


Figure 4.1: Flowchart of the genetic algorithm employed in this thesis.

value for each family is calculated by the "fitness evaluation" operator. The objective function is a measure of the difference between the simulated waveform and the desired impulse waveform. "Selection" operator selects the best families in the population and pass them into the next generation unless terminal conditions are met. When the termination assessment is passed, the final sample gives the optimized results of unknowns. A detailed description of each genetic operator is presented in the following.

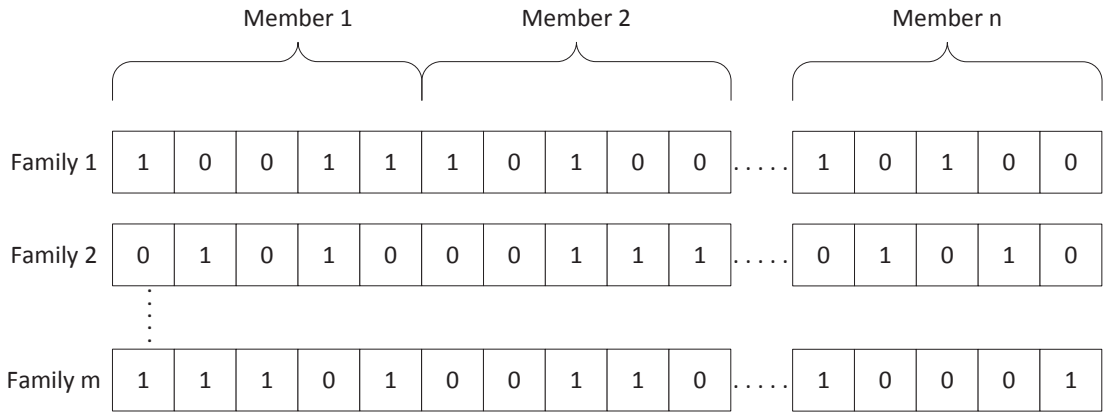


Figure 4.2: An example initial population of size m and n number of unknowns. In this example each member is coded as a 5-bit binary number.

4.2.1 Genetic Operators and Their Tasks

Initial Population

The initial population is created by a random set of binary bits. Since the number of unknowns (resistor values) can be differed from case to case, the number of members in a family is adjusted accordingly. An example of an initial population of size m with n number of unknowns is shown in Fig. 4.2.

Crossover

The function of crossover is explained as follows. The first family (first row of bit strings) and another random family is selected from the same population (this can be initial or previous population). Then the binary bit patterns (bit rows) of both families is divided into two parts at an arbitrarily selected point. This point is the same for both families. Subsequently, the corresponding bit segments are exchanged, resulting in two new families as shown in Fig. 4.3. The same procedure is followed

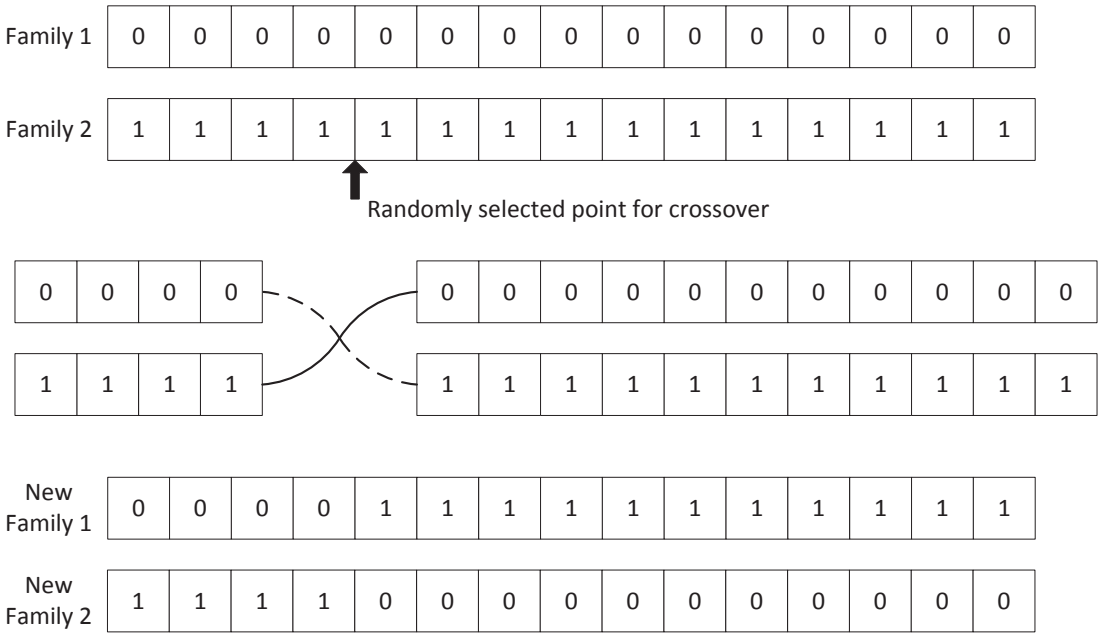


Figure 4.3: A demonstration of crossover operator.

for all the families in the population and to make a new population with a size of double the original population size.

Mutation

In the mutation operator, a family is randomly selected with a predefined probability. This probability is known as thee probability of mutation (pm), which determines the degree of exploration (searching the solution space as much as possible) in the solution. Generally it is a fix value, but in the proposed method, a dynamic approach is used to find the optimum family. i.e., a comparatively large pm is used in initial generations for a better exploration and a lower pm at later generations for a fast convergence. A new family is created by mutating a randomly selected bit of the selected family as shown in Fig. 4.4.

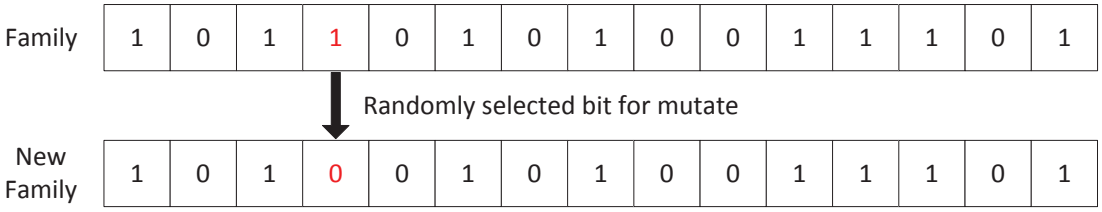


Figure 4.4: A demonstration of mutation operator.

Fitness Evaluation

This is the operator which calculates the fitness value of the objective function. First, it decodes the binary values and obtain the actual values of unknowns. Then, those values are normalized by applying boundary conditions. Boundary conditions are the practical limits of unknowns. In this application, the minimum and the maximum values of impulse generator resistors define the boundary conditions. These values can be different from generator to generator. The normalized values are stored in a file in such a way that PSCAD/EMTDC can read it. For example:

Bit string of the selected unknown: 10011

Upper boundary (in this thesis, maximum available resistor value): x_2

Lower boundary (in this thesis, minimum available resistor value) : x_1

The normalized actual value (R) of unknown can be calculated as,

$$R = \frac{(10011)_2}{2^5 - 1} \times (x_2 - x_1) + x_1 \tag{4.1}$$

In each run, the GA instructs PSCAD/EMTDC to run the simulation by using those stored unknowns as the input and to record the simulated impulse waveform.

This output waveform is sent back to the GA and compared with the desired waveform. The difference between two waveforms gives the error (or the fitness value). In this thesis the error has been calculated in two ways given by,

$$E_p = \sqrt{\frac{1}{K}\sum_{n=1}^{K} |Vs_n - Va_n|^2} \tag{4.2a}$$

or

$$E_t = k_1.\,|T_{1s} - T_{1a}| + k_2.\,|T_{2s} - T_{2a}| \tag{4.2b}$$

where, E_p and E_t are two fitness values which are calculated from the point to point comparison of waveforms, and the time (rise and fall) comparison of waveforms, respectively. K is the number of points in the waveform while Vs_n and Va_n are the n^{th} point voltage of simulated and desired waveforms, respectively. T_1 and T_2 stands for the rise time and the fall time, respectively. k_1 and k_2 denotes the weight factors for the rise time and the fall time in order. Subscripts "s" and "a" refer to simulated and desired.

In initial generations, the point to point comparison given by (4.2a) is used due to the incapability of time comparison to calculate rise time and fall time without having a proper waveshape. Later, (4.2b) is employed which is more important since the rise time and fall time are the parameters which should be achieved as per the standards. The rise time is weighted higher compared to fall time due to the higher sensitivity.

Selection

The fitness-evaluated population is sorted in descending order by its fitness value. The upper half (least error half) of the generation is selected and passed on to the next operator. Since the population size is doubled in the crossover operator, this operator resizes it to its original population size by selecting the best half of the population.

Termination Condition

This operator checks whether the newly created population is good enough or should continue for another generation. The fitness value of the best family of five generations prior to the current generation is kept and is checked for the difference of the fitness value between adjacent generations. If all the five differences are lower than the defined tolerance,the development of new generations is terminated.

Optimized settings

When the development of generations is stopped by meeting the termination condition, the last created generation is selected and the population is sorted in descending order by its fitness value. The top family after sorting has the least error which is the best family or the optimized setting.This family is selected and decoded for the actual values. This normalized resistor values are optimized settings for the impulse generator.

Selecting closest available resistors to the optimized resistors within the GA is not efficient in terms of convergence since the changes make to the resistors with

respect to practical values may result the solution to deviate from the global optimum. Therefore, a separate program is written to obtain practical resistor values to be implemented in the real impulse generator.

4.3 Validation of Optimization Procedure

It is important to validate the accuracy of the proposed method before it is used in a real impulse test. For this purpose, two different tests are conducted. In the first test, some known resistor values were obtained using above method by comparing the step response of a series RLC circuit. In the second test, the known impulse generator settings were obtained by comparing the impulse waveforms generated by a single stage impulse generator.

4.3.1 Step Response Test

In this test, a step signal is applied to a series RLC circuit as shown in Fig. 4.5. First we determine the response of the circuit using some known values for R, L and C. Then the circuit element values are obtained using the proposed method, such that the response of the circuit matches the previously calculated response. The simulated voltage output (at the terminal shown in the figure) is compared with the desired waveform for fitness evaluation. The number of unknowns in the GA is set as three since a resistor, an inductor and a capacitor are the unknowns in the circuit. The boundary conditions are defined as follows; zero for the all lower boundaries and five times of known values as the upper boundaries. The Length of the bit string

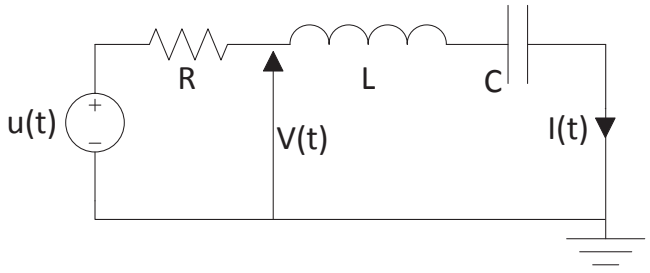


Figure 4.5: The series RLC test circuit which is used to validate the accuracy of the optimization procedure.

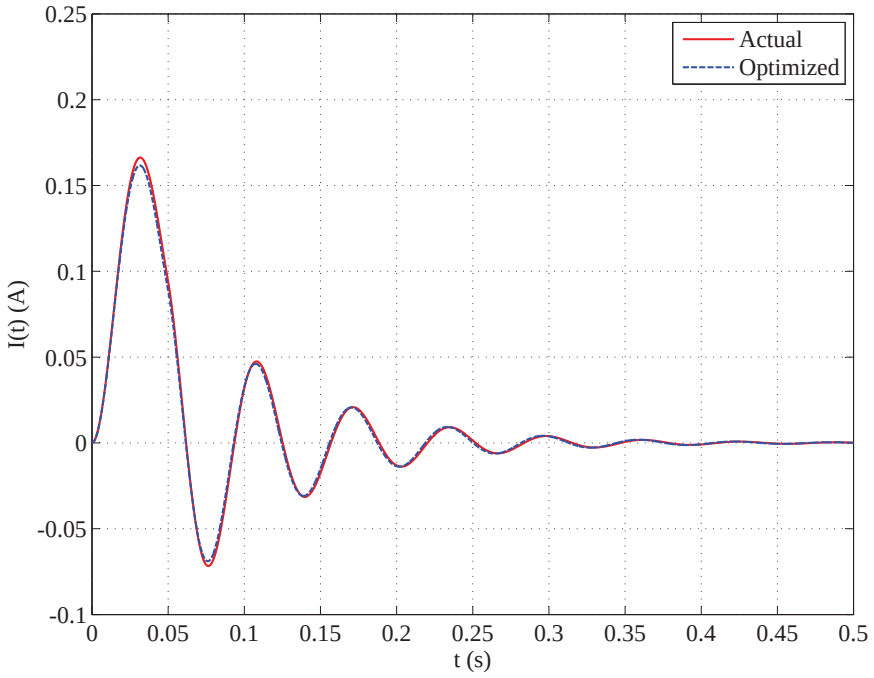
Table 4.1: Optimized circuit elements of the test circuit (Fig. 4.5) with its desired values.

Parameter	**R** (Ω)	**L** (H)	**C** (μ**F**)
Original	50.00	02.00	50.00
Optimized	52.24	02.08	47.13
Error	04.48 (%)	04.00 (%)	05.74 (%)

is defined as per the maximum upper boundary condition. The optimized values for circuit elements with its known values are shown in the table 4.1. The obtained waveforms are compared in the Fig. 4.6.

4.3.2 Impulse Response Test

In this test, a circuit model of a single stage impulse generator with a purely capacitive load is simulated in PSCAD/EMTDC as shown in Fig. 4.7. The impulse generator settings are obtained using the proposed method. The output of the impulse generator is compared with the desired waveform for the fitness evaluation. The number of unknowns in the GA is set as two since only the values of R_1 and R_2 are needed to be optimized (C_1 (0.5 μF) and C_2 (20 nF) are fixed). The boundary conditions and



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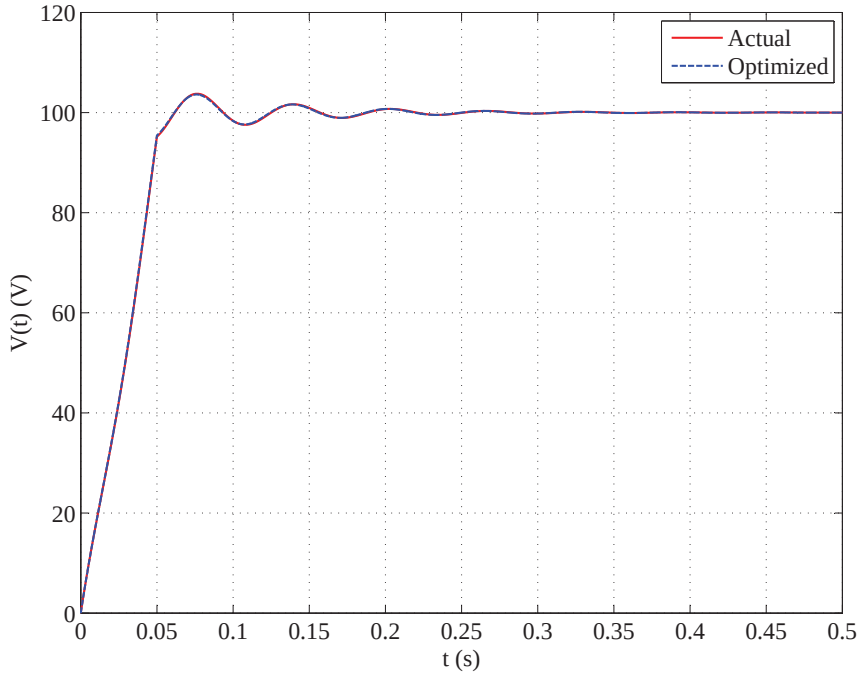


(b)

Figure 4.6: Optimized and desired a) current and b) voltage waveforms of the test circuit shown in Fig. 4.5.

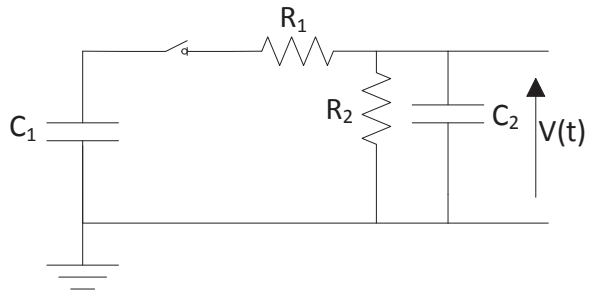


Figure 4.7: The single stage impulse generator circuit which is used to validate the accuracy of the optimization procedure. C_1 is assumed to be fully charged before the operation of the switch.

Table 4.2: Optimized circuit elements of the impulse generator circuit (Fig. 4.7) with its desired values.

Parameter	**R1** (Ω)	**R2** (Ω)
Analytical	25.779	107.145
Optimized	23.543	108.031
Error	08.674 (%)	0.827 (%)

the bit string length are defined similar to the previous test. The optimized resistor values and the original values (which deliver the 1.2/50 μs waveshape) are shown in Table 4.2. The obtained waveforms are compared in Fig. 4.8.

The maximum element error is recorded as 8.67 % in the R_1 of impulse response test. This is an acceptable error, since rise time and fall time of the simulated waveform are within the standard tolerance [3, 4]. Further, the recored waveforms (Fig. 4.6 and Fig. 4.8) have shown a fine match in both cases. Therefore, theses tests confirm that the proposed method is very accurate for the calculation of the impulse generator settings in a real impulse test.

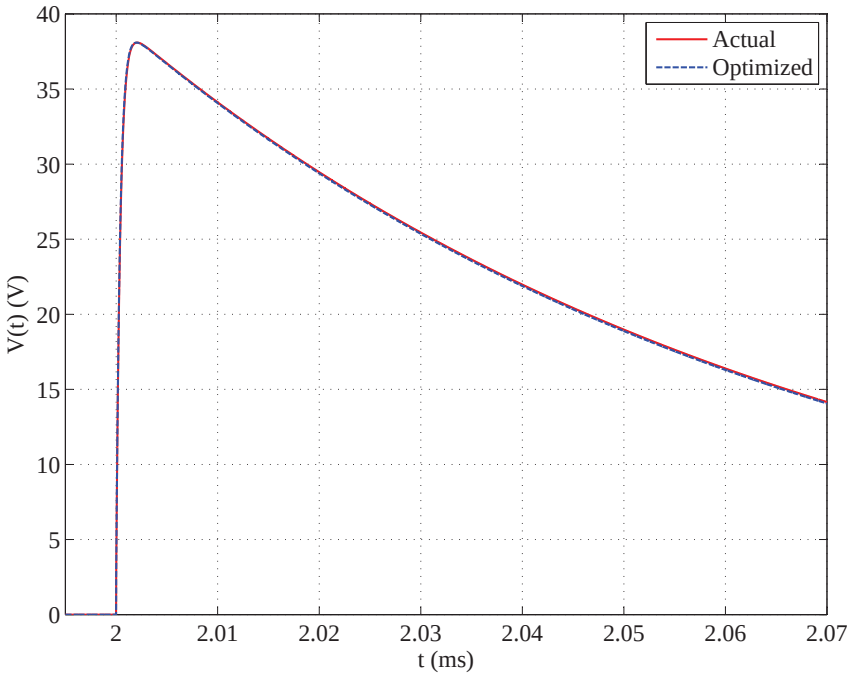


Figure 4.8: Optimized and desired voltage waveforms of the test circuit shown in Fig. 4.7.

Chapter 5

Case Study Results

5.1 Introduction

In Chapters 2-4, a comprehensive method was introduced to optimize the impulse generator settings. Further, the accuracy of the method is also validated with two test circuits. In this chapter, this validated method is implemented on a real impulse test setup. The setup is tested at High Voltage Test Facility (HVTF) at Manitoba Hydro for experimental validation of the proposed technique, where a three phase test transformer (138/13.8 kV, Y-Δ, 80 MVA) is tested with three different arrangements of impulse generator. These arrangements are first optimized using the proposed technique. Then, these settings are implemented in the real test setup. The three cases in this thesis are studied as follows.

- Case I : Three stages of the impulse generator are connected in series with the same resistor setting in each stage.

- Case II : Six stages of the impulse generator are connected in series with the same resistor setting in each stage.

- Case III : Six stages of the impulse generator are connected in series with different resistor setting in each stage

In all three cases, the tests are performed on the terminal H_1 of the test transformer. Fig. 5.1 shows the real test setup at Manitoba Hydro HVTF. The automatically generated impulse test reports from the impulse recording system is shown in Appendix B.2. A brief technical description of the test apparatus and the DUT used in the experiment is presented in Tables 5.1 and 5.2, respectively. Further technical details can be found in Appendix A.1-A.5 . In Section 5.2, the developed circuit model for the test transformer is presented and Section 5.3 contains the generated impulse waveform with used resistor settings.

5.2 Circuit Model of the Test Transformer

The entire circuit model derivation is done as described in Chapter 3. Fig. 5.2 shows some snapshots that are taken during the FRA measurement process.

In the vector fitting program, the optimum number of poles for the rational function approximation is obtained by trying different cases using a trial-and-error method. The accuracy of the derived circuit model is tested by comparing the frequency responses. Fig. 5.3 shows the frequency response of measured, fitted and passivity enforced vectors. The element values of the derived circuit model is shown in Appendix B.1.2.

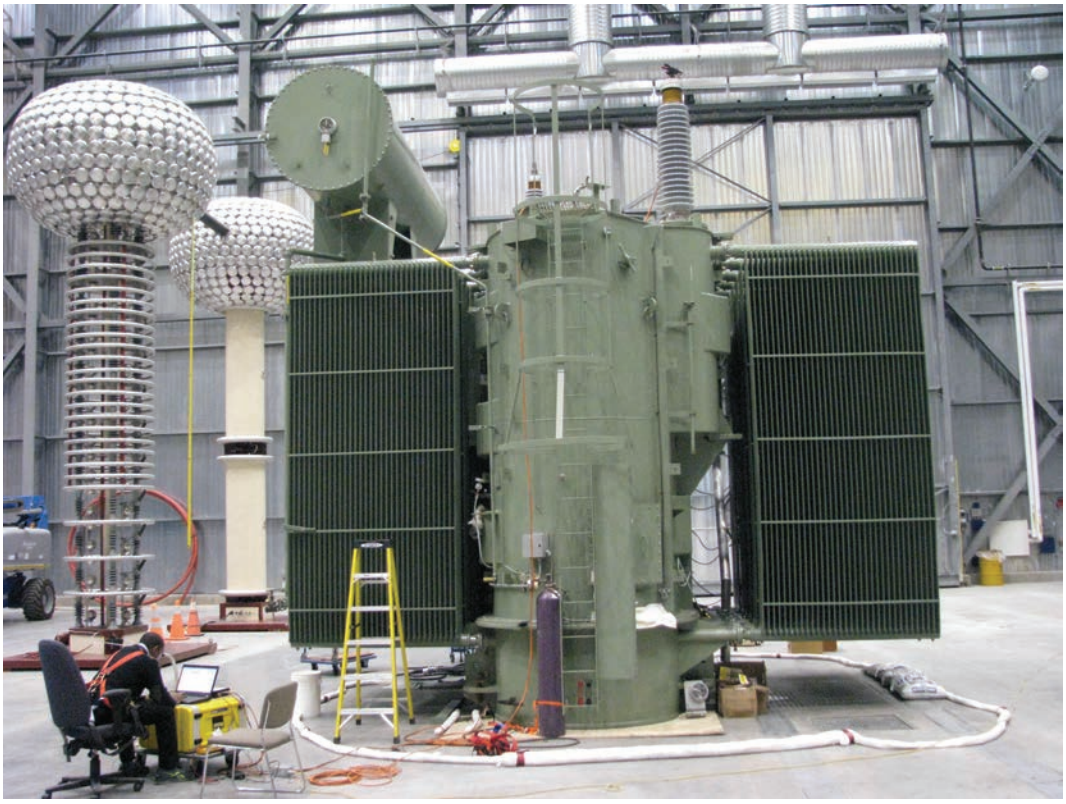
Figure 5.1: Actual impulse test setup at Manitoba Hydro HVTF. a) Impulse Generator, b) Power Transformer, c) Voltage Divider, and d) Multiple Chopping Gap.

Table 5.1: Details of test equipment used in the experiment.

Item	**Model**	**Specification**
Impulse Generator	Haefely SGVA 360 kJ	Number of stages: 12, Maximum lightning impulse voltage: 2400 kV, Maximum switching impulse voltage: 2160 kV, Impulse capacitance per stage: 1.5 μF.
Voltage Divider	Haefely CR 2400-350	Maximum lightning impulse voltage: 2400 kV, Maximum switching impulse voltage: 1300 kV, Primary unit: 0.7 ηF and 180 Ω, Secondary unit: 0.23 ηF and 540 Ω.
Multiple chopping gap	Haefely MAFS 2400	Maximum lightning impulse voltage: 2400 kV, Number of primary unit: 4, Capacitance per unit: 2.4 ηF.
Sweep Frequency Response Analyzer	Frax 101	Frequency range: 1 Hz - 2 MHz, Maximum number of samples: 32000, Output channel voltage: 0.2 - 20 V peak-to-peak, Measurement channel voltage at 50 Ω: 0.1 - 10 V peak-to-peak.

Table 5.2: Details of the DUT (high voltage power transformer.

Item	**Make**	**Specification**
Power Transformer	GE Energy	138/13.8 kV, wye-delta, 80 MVA, Number of phases: 3, Class: ONAN/ONAF /ONAF, Frequency: 60 Hz, Vector group: YNd 1.



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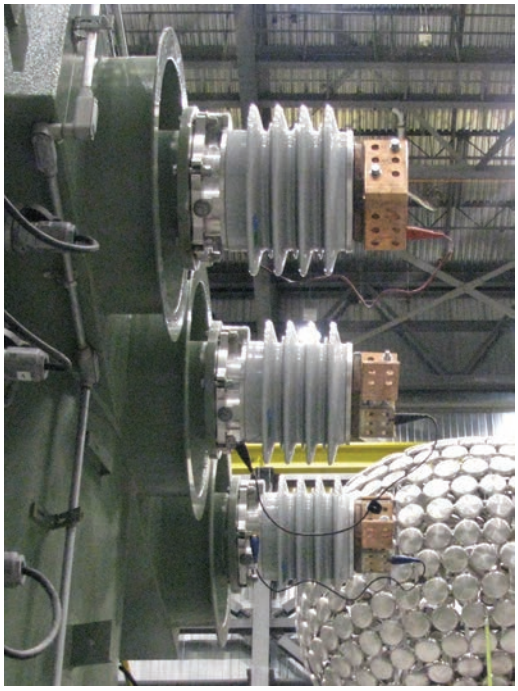
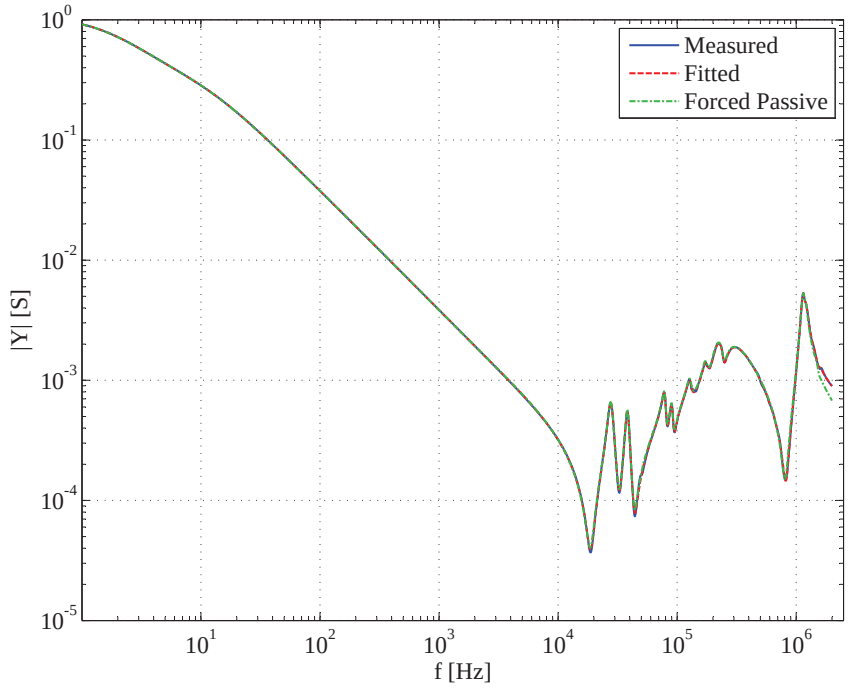


(c)

Figure 5.2: a) Recording the frequency response of the transformer b) The SFRA connection at $H1$ terminal of the transformer c) Short circuited low voltage windings. Courtesy of Manitoba Hydro High Voltage Test Facility.



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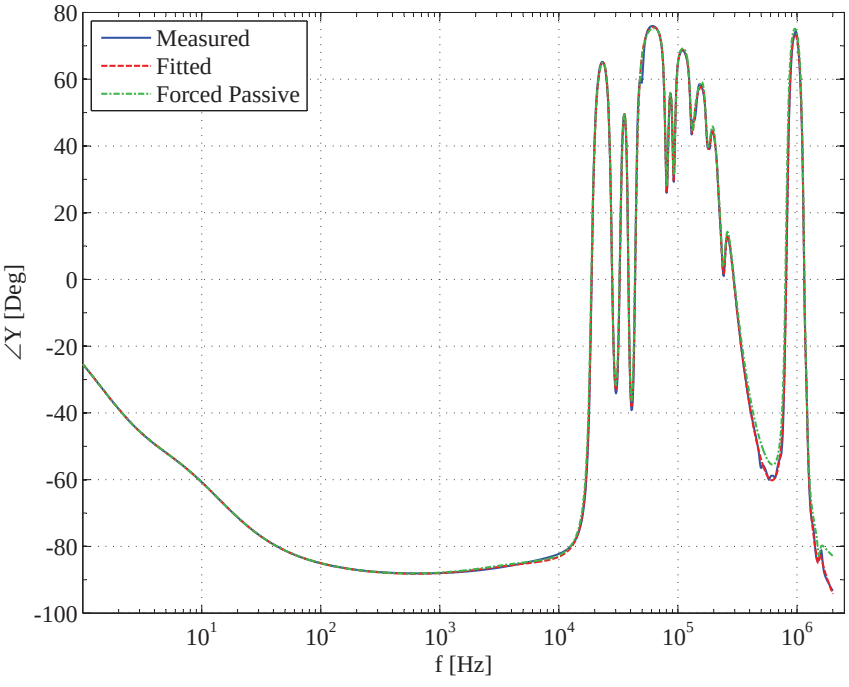


(b)

Figure 5.3: a) The magnitude and b) the angle of the admittance calculated for $H1$ terminal of the test transformer.

As seen in Fig. 5.3, the derived circuit has given a fine match to the measured admittance.

5.3 Lightning Impulse Test Results

The complete test setup including the above developed transformer circuit model is simulated in PSCAD/EMTDC. The time step and the run time of the EMT simulation is fixed as 1 ns and 80 μs, respectively. As described in Chapter 4, the final resistor settings are obtained by a GA based OE-EMTS procedure. Some of the parameters used in the GA are highlighted as follows.

- Population size : 10
- Length of a bit string : 13
- Maximum number of generations : 100
- Initial mutation probability (pm) : 0.05

On the above list, the maximum generation number is selected by the convergence rate of all three cases. The mutation probability (pm) is selected as 0.05 initially and changed dynamically with the generation number. The results obtained for each case with the generated impulse waveforms are explained in Sections 5.3.1, 5.3.2 and 5.3.3.

5.3.1 Case I : Three stages with same resistor setting

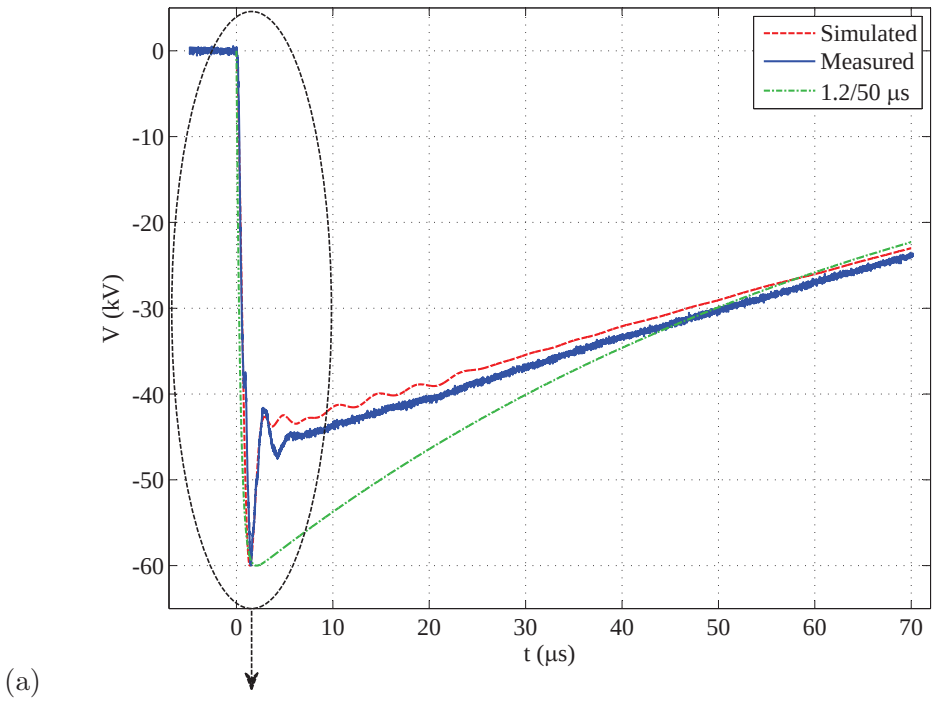
In the first case, the impulse generator is configured in such a way that, three stages are connected in series with the same resistor setting for all stages. Since all the stages

Table 5.3: Optimum resistor setting for the impulse generator - Case I : Three stages with same resistor setting.

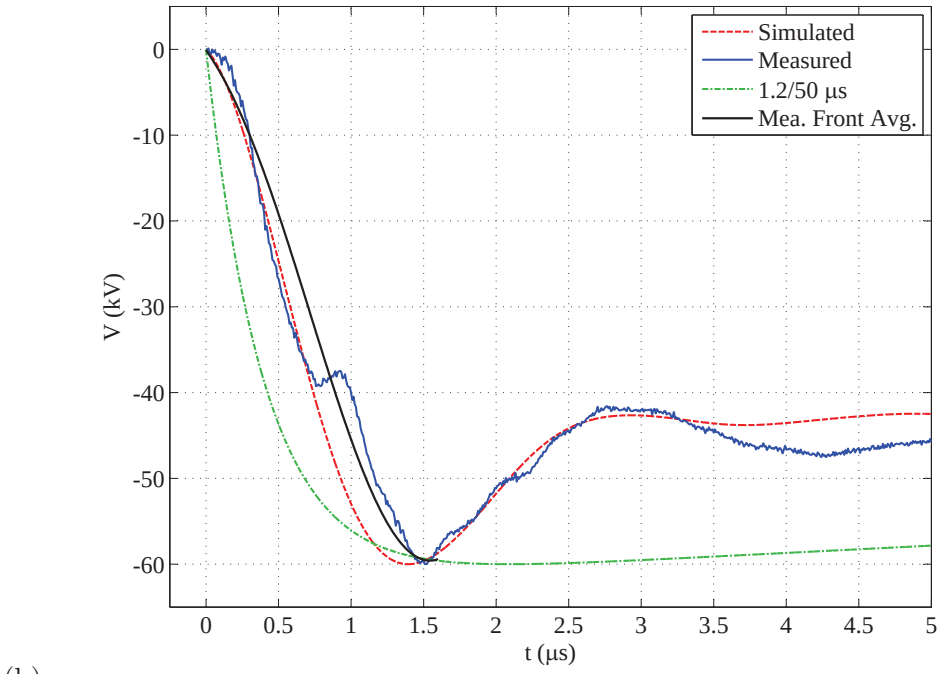
Parameter	**Series Resistor (Rs) in Ω**	**Parallel Resistor (Rp) in Ω**
Calculated Optimum	16.13	113.60
Practical Optimum	15.00	110.00
Resistor Combination	30 ‖ 30	220 ‖ 220

use the same setting, the number of unknowns is set as two (Rs and $Rp_1 + Rp_2$). Even though there are two serially connected resistors for tail resistor in the impulse generator schematic diagram (see Fig. 2.5), in the GA they are considered as one resistor. Later, two resistors equivalent to the optimized resistance are calculated by a separate program. This makes the length of the bit pattern in a GA family shorter and resulting in faster calculation. The final resistor values converged by the end of 43^{rd} generation are shown in Table 5.3.

In practice, since a limited number of resistor values are available, the closest value to the calculated value was selected for the experiment. Using the values calculated for the impulse generator, a lightning impulse test was performed on the transformer. The measured impulse waveform is compared with the simulated and desired (1.2/50 μs) waveforms in Fig. 5.4. Since there are considerably large fluctuations in the front portion of the measured waveform, as per the standards, an average line has to be drawn to calculate the proper risetime of the waveform. The black color line named as "Mea. Front Avg." represents this average line which used to calculate the risetime.



(a)



(b)

Figure 5.4: Comparison of lightning impulse waveforms - Case I : Three stages with same resistor setting.

Table 5.4: Optimum resistor setting for the impulse generator - Case II : Six stages with same resistor setting.

Parameter	**Series Resistor (Rs) in Ω**	**Parallel Resistor (Rp) in Ω**
Calculated Optimum	20.61	80.23
Practical Optimum	19.82	76.10
Resistor Combination	22 ‖ 400 ‖ 400	92 ‖ 440

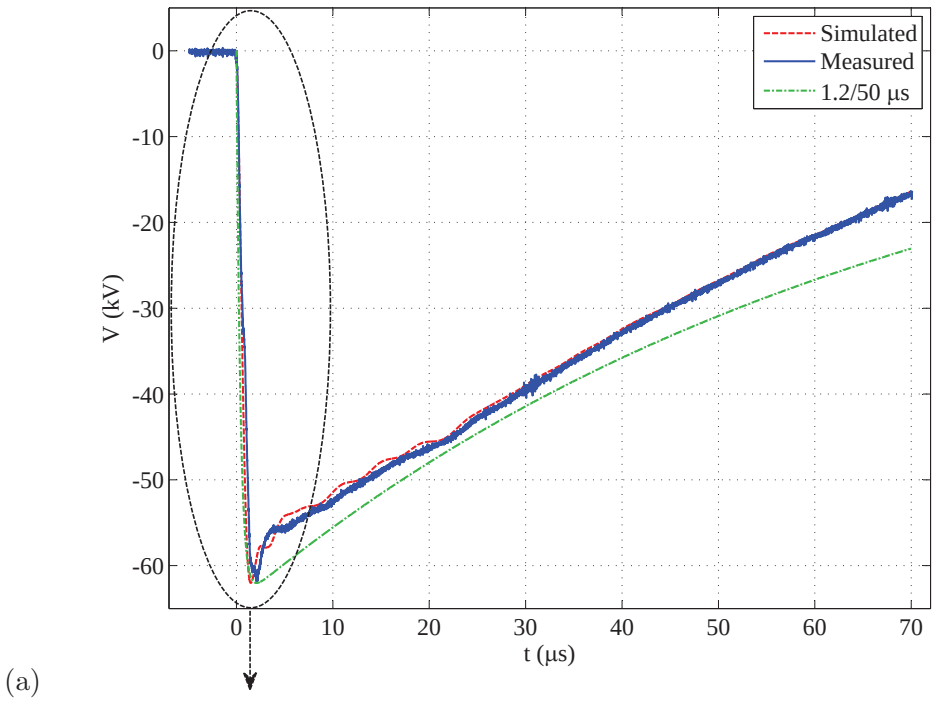
5.3.2 Case II : Six stages with same resistor setting

In this case, the impulse generator is configured as six stages in series with the same setting for each level. Similar to the first case, same setting in each level limits the number of variables to two. By end of the 68^{th} generation, convergence is achieved and the two resistor values are given in Table 5.4.

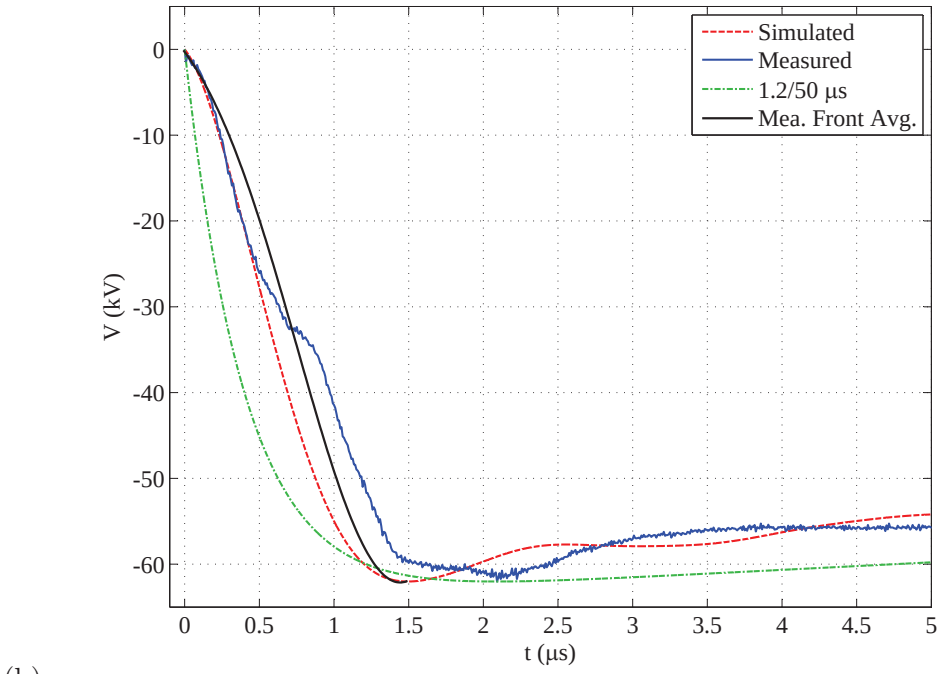
The simulated, measured, and desired waveforms are plotted in Fig. 5.5. The resulted waveform has improved in waveshape compared to the first case (less overshoot voltage) as shown in Fig. 5.5. This confirms that higher number of stages offers a better shape in the waveform. This is one of the key advantage in the proposed method. Because it offers an opportunity to find the optimum stage arrangement for the impulse generator apart from optimizing resistor values.

5.3.3 Case III : Six stages with different resistor setting

This study is different compared to the other two cases because the condition of same resistor values for all stages is not imposed any more. The impulse generator is configured as six stages in series with different settings for each stage. Since it has used different settings in each level, the number of unknowns increases to twelve. This



(a)



(b)

Figure 5.5: Comparison of lightning impulse waveforms - Case II : Six stages with same resistor setting.

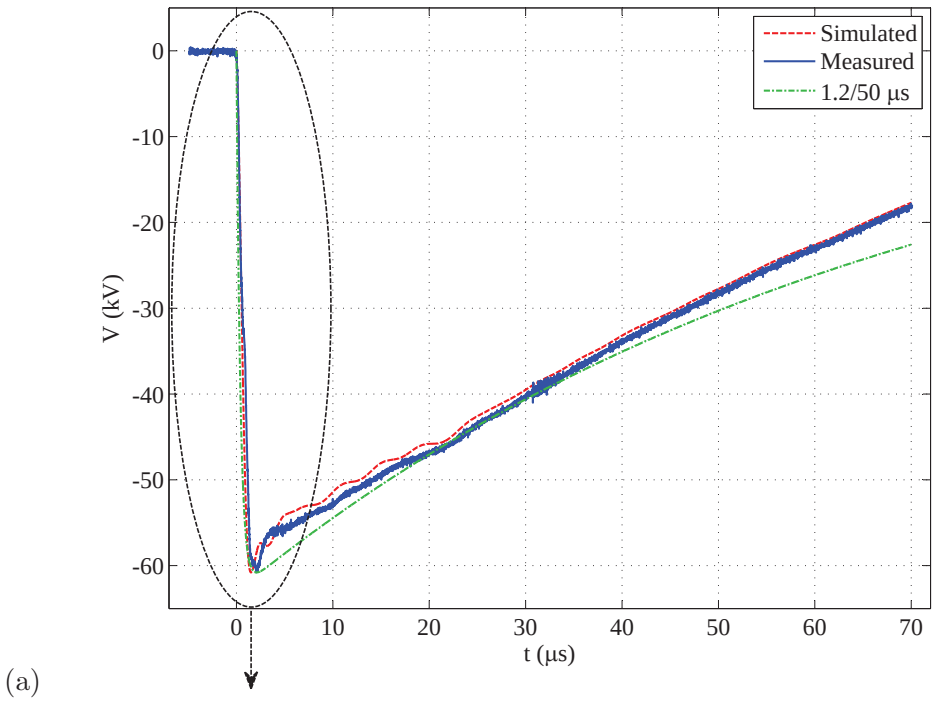
increases the number of members in the GA family and makes bit patterns longer. This hardly affects calculation time because the full solution time mainly depends on the number of generations to converge. The final optimized setting is shown in Table 5.5 which is obtained at the end of the 37^{th} generation. The obtained waveforms are compared with the simulated and analytical results in Fig. 5.6. Compared to the two previous cases, this case has given the closest to the ideal waveform in shape. As seen in Fig. 5.6, the overshoot has significantly reduced in this case.

5.4 Analysis of Lightning Impulse Test Results

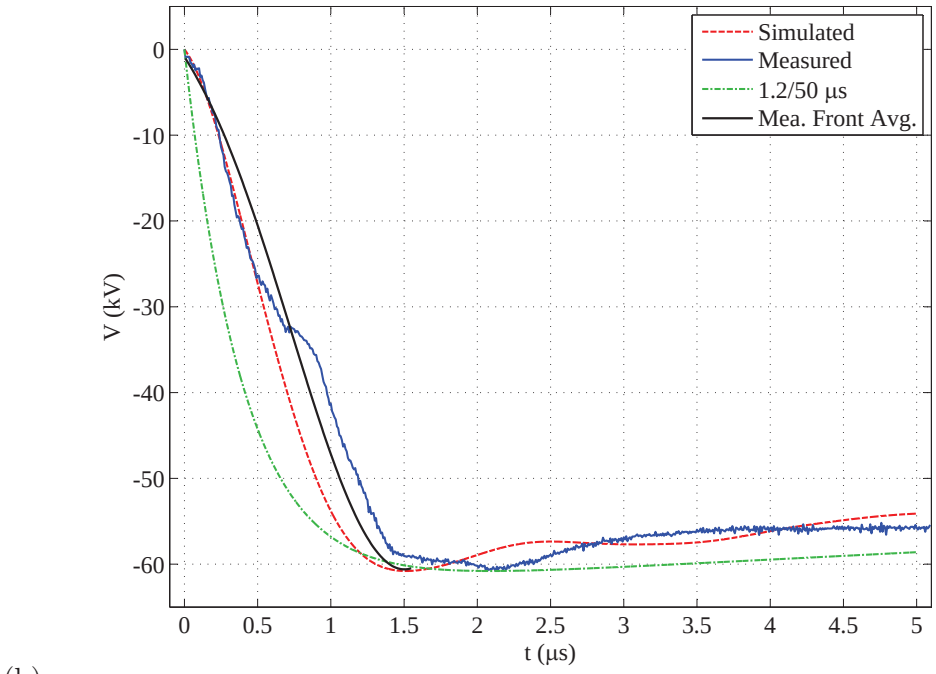
The main parameters that describe an impulse waveform have been identified as the rise and fall times which for the case of a lightning impulse are 1.2 and 50 μs, with an acceptable tolerance of 30% and 20%, respectively [3,4]. However there are additional factors that must be considered before the waveform is accepted. Overshoot is one of these factors for which a value of less than 10% is accepted [3, 4]. The rise and fall times of the measured and simulated impulse waveforms and their relative error when compared with a 1.2/50 μs waveform is shown in Table 5.6. The rise and fall times of the measured and simulated waveforms have directly been calculated from those shown in Figs. 5.4 - 5.6. One can observe oscillations on both the measured and simulated waveforms, the risetimes of measured waveforms were calculated based on the average line. However, no averaging was performed on the simulation results as the frequency of the oscillations is not high enough [3]. A study of Table 5.6 shows that all cases were able to reproduce the 1.2/50 μs waveform with the allowed tolerance,

Table 5.5: Optimum resistor setting for the impulse generator - Case III : Six stages with different resistor setting.

Stage	**Parameter**	**Series Resistor (Rs) in Ω**	**Parallel Resistor (Rp) in Ω**
1	Optimum	14.85	90.02
	Available	15.00	92.00
	Combination	30 ‖ 30	92
2	Optimum	18.61	80.23
	Available	15.00	80.00
	Combination	30 ‖ 30	160 ‖ 160
3	Optimum	22.43	66.54
	Available	22.00	64.87
	Combination	22	92 ‖ 220
4	Optimum	29.06	144.94
	Available	30.00	149.15
	Combination	30	160 ‖ 2200
5	Optimum	29.53	152.21
	Available	30.00	149.15
	Combination	30	160 ‖ 2200
6	Optimum	10.80	20.45
	Available	11.00	46.00
	Combination	22 ‖ 22	92 ‖ 92



(a)



(b)

Figure 5.6: Comparison of lightning impulse waveforms - Case III : Six stages with different resistor setting.

Table 5.6: Comparison of rise and fall times calculated for the waveforms in each case. The error is with respect to the desired 1.2/50 μs Waveform.

Parameter	**Source**	**Case**	**Time** (μs)	**Error (%)**
Risetime	Simulation	I	1.06	12.05
		II	1.10	8.29
		III	1.11	7.59
	Measurement	I	1.21	0.90
		II	1.24	03.22
		III	1.20	00.26
Falltime	Simulation	I	46.72	6.56
		II	42.38	15.25
		III	45.18	9.63
	Measurement	I	49.55	0.91
		II	42.71	14.57
		III	45.74	8.51

however, in case I, where three identical stages were employed the overshoot is more than the preferred and may not be considered as a valid solution. For cases II and III, the simulated and measured waveforms demonstrate a satisfactory consistency with the desired waveform. The measured rise time is higher than the simulation. This is due to the oscillation that exists on the rising portion of the measured waveform and effective front resistors being larger than actually implemented (due to the neglected connection impedances).

Overall, case III shows a better performance. Such arrangement of resistors (i.e. different resistors in each stage) is only possible through the proposed approach. In the conventional trial-and-error method, due to the very large number of resistor combinations possible, it is virtually impossible to find this solution. In addition,

the waveform match is not as close as it could be due to the practical availability of resistors. In all cases, the difference between the simulated and measured waveform has been caused by the neglected parameters, such as parasitic inductances and capacitances. This can be treated with a careful insertion of those parameters in the simulation case. The dynamics of the impulse generator gaps and their firing/operation time may have some influence for wave shape. Breakdown time of each sphere gap after the first (triggered) stage could have some variation. Perhaps this influence is minimal but there can be some slight differences in wave shape between successive impulses even when all parameters remain constant.

Chapter 6

Conclusion

6.1 Contribution

In this thesis, a new Genetic Algorithm (GA) based Optimization Enabled-Electromagnetic Transient Simulation (OE-EMTS) approach is proposed to calculate the settings of the impulse generator. A complete replica of the test setup was simulated in an electromagnetic transient simulation program (EMTP)-type program (in this thesis it is PSCAD/EMTDC) to mimic the real impulse test. The following principal contributions were made during this thesis.

- A detailed circuit model for the device under test (transformer) was obtained from a frequency response analysis (FRA). First, a procedure to measure the frequency response of the transformer was introduced. Then the accuracy of the introduced measuring procedure was validated using an experiment performed on a test circuit. Subsequently, The circuit elements were synthesized by a rational function which was fitted from the frequency response. The accuracy of the circuit synthesis procedure

was validated using two laboratory experiments which were performed on the same test circuit as above.

- The optimization of impulse generator settings was done via a GA based OE-EMTS process. A specifically written GA in MATLAB interfaced with PSCAD/EMTDC was used to optimize the impulse generator settings. Before applying the optimization process to the full problem which involves a model of the test setup including the device under test, the process was validated with simpler examples of finding the best fit R,L, C parameters for a small circuit that would match its actual circuit parameters.

- Finally, the proposed approach was validated by a real lightning impulse test performed on a 138/13.8 kV, Y-Δ, 60 Hz, 80 MVA transformer. Three different arrangements of the impulse generator were studied and the resulted waveforms were confirmed the accuracy and the viability of the proposed approach. All cases were able to reproduce the 1.2/50 μs waveform with the allowed tolerance.

  - In case I, where three identical stages were employed, the maximum error in the measured waveforms is less than 1 % which has a tolerance of 30 %. Even though the risetime and falltime were within the standard tolerance, the overshoot in the peak may led to not to consider as a valid solution.

  - In cases II, where six identical stages were employed, the simulated and measured waveforms demonstrate a satisfactory consistency with the desired waveform.

  - Overall, case III shows the best performance. Such arrangement of resistors (i.e. different resistors in each stage) is only possible through the proposed approach.

- A new impulse generator setup (different resistor setting in each stage) was introduced which was not possible with the conventional trail-and-error method. With the new setup, many more resistor values can be optimized than in the conventional method. With twelve resistors, the waveform was able to more closely fit the desired test waveform.

- Sometimes additional equipment such as Glaninger circuit, overshoot compensator, paralleling stages or introducing a grounding resistor is used to shape the waveform if the basic waveform generated by the test setup is unsuitable, e.g., the overshoot may be too high. In the conventional approach, this is realized only after physical testing. In the proposed approach, the external equipment can be modeled in the EMT simulation and be part of the design process.

6.2 Future Work

In this thesis, the settings of the impulse generator were optimized only to generate the lightning impulse waveform. This could be extended to switching impulse too.

The configuration of the impulse generator circuit can be changed based on the nature of the test object. Apart from the already tested stage arrangements, some other configurations are available for testing, such as all parallel stages, mix of series and parallel stages, etc. This also will help to identify the requirement of additional test equipment. These arrangements might give better results compared to the results obtained in this thesis. Therefore further researches may find the optimum stage arrangement before optimizing the resistor settings.

Correct representation of the test setup parameters, such as parasitic capacitance, mutual inductances, lead impedances and ground resistances incorporated in the impulse test setup will improve the results. Specially, the calculations of rise time could further be improved if correct connection lead impedances are known, which is neglected in this study. Therefore, further improvement of the simulation parameters should ensure better match of rise and fall time as well as produce a better match in waveshape.

In addition to changes in the physical structure, there are few more areas which further can optimize within the GA program. Mutation and crossover functions can be optimized further by customizing them according to the nature of the case. One of the drawbacks in the developed approach is the time consumed by the GA to converge. This dominates by the time needed for the electromagnetic transient (EMT) simulation, but still it was very small compared to the time taken for conventional method. A further research can be performed to develop a circuit model which can operate in the same numerical environment as the optimization algorithm which directs for smaller simulation time.

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Appendix A

Technical Specifications

A.1 Impulse Generator (Manufacturer: Haefely)

General
Model: SGVA 2400 kV 360 kJ
Max. charging voltage - LI: 2400 kV
Max. charging voltage - SI: 2160 kV
Energy at max. charging voltage: 360 kJ
Total Impulse Capacitance: 125 nF
Time between Impulses: 60 s
Waveform acc. IEC 60060-1: 1.2/50 μs
Waveform acc. IEC 60060-1: 250/2500 μs
Waveform acc. IEC 60076-3: 20/200/500 μs
Waveform acc. IEC 600230: 1-5/50 μs
Max. charging voltage per stage - LI: 200 kV
Max. charging voltage per stage - SI: 180 kV
Energy per stage at max. charging voltage: 30 kJ
Impulse capacitance per stage: 1.5 μF
Number of stages: 12
Max. Height: 9 m
Top electrode type: T6
Top electrode dimensions: 3750 x 3750 x 700 mm
Top electrode weight: 210 kg

Other
Air cushions: type B70N
Sphere gap: 250 mm
Potentiometer for gap: Type TEX 150, 6 kΩ
Motor drive voltage: DC 24 V
Fan supply voltage: AC 230 V
Discharge switch supply voltage: DC 24 V
Security grounding system supply voltage: AC 230 V
Warning lamp supply voltage: AC 230 V

Environmental Conditions
Altitude above sea level: 1000 m
For each add. 100 m, the voltage rating must be decreased by: 1%
Operation temperature range of HV components: $+3 to + 45\,°C$
Relative humidity for HV components: $\leq$ 90 %
Operation temperature range of electronics: $+10 to + 45\,°C$
Relative humidity for electronics: $\leq$ 80 %
Storage and shipment temperature range of all components: $-20 to + 60\,°C$

A.2 Voltage Divider (Manufacturer: Haefely)

General
Max. - LI: 2400 kV
Max. - SI (Positive Polarity): 1300 kV
Max. - SI (Negative Polarity): 1525 kV
Primary Unit Resistance: 180 Ω
Primary Unit Capacitance: 0.7 nF
Secondary Unit Resistance: 180 Ω
Secondary Unit Capacitance: 0.7 nF
Number of secondary units: 3
External damping resistor: 400 Ω
Max. height: 7.9 m
Top electrode diameter: 1900 mm
Bottom electrode diameter: 1900 mm
Top electrode cross section diameter: 450 mm
Bottom electrode cross section diameter: 450 mm

A.3 Multiple Chopping Gap (Manufacturer: Haefely)

General
Max. - LI: 2400 kV
Max. - SI (Positive Polarity): N/A
Max. - SI (Negative Polarity): N/A
Number of secondary units: 4
Maximum voltage per gap: 200 kV
Primary Unit Capacitance: 2.4 nF
Secondary Unit Resistance: 180 Ω
Sphere gap diameter: 200 mm
Max. height: 8.3 m
Top electrode diameter: 1900 mm
Bottom electrode diameter: 1800 mm

Top electrode cross section diameter: 300 mm
Bottom electrode cross section diameter: 300 mm

A.4 Power Transformer (Manufacturer: GE Energy)

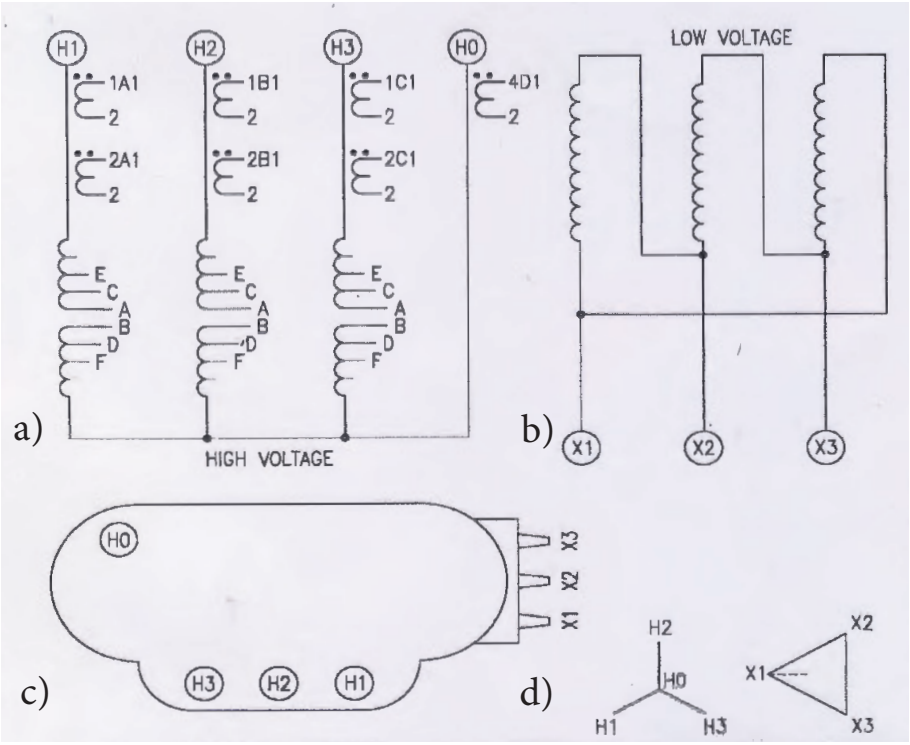


Figure A.1: A snapshot of the nameplate of the power transformer which is used in this thesis. Courtesy of Manitoba Hydro HVTF. a) High voltage winding diagram with CT connections and tap changer positions, b) Low voltage winding diagram, c) Plan view of the high voltage, low voltage and neutral terminals arrangement and, d) Phasor diagram of the vector group.

General
Base Rating: 80 *MVA*
HV rated: 138 *kV*
LV rated: 13.8 *kV*
Class: ONAN/ONAF/ONAF
Number of Phases: 3 (Three)
Frequency: 60 *Hz*
Vector Group: YNd1

Load Capacities

Full load continuous 65° *C rise* 30° *C Ambient*
80 MVA Oil Natural and Air Natural (ONAN)
107 MVA Oil Natural and Air Forced (ONAF)
134 MVA Oil Natural and Air Forced (ONAF)

Full load continuous 65° *C rise* 0° *C Ambient*
100 MVA Oil Natural and Air Natural (ONAN)
127 MVA Oil Natural and Air Forced (ONAF)
159 MVA Oil Natural and Air Forced (ONAF)

Approximate Weights
Core and Coils: 55769 kg
Tank and Fittings: 25401 kg
Mineral Oil - Main tank: 30044 kg (35274 L)
Mineral Oil - Conservator: 1709 kg (2006 L)
Mineral Oil - Coolers: 606 kg (712 L)
Total Weight: 113529 kg
Tank will withstand full vacuum: Yes

Table A.1: Current transformer details (Fig. A.1 - (a)).

C.T.	**Class**	**Ratio**	**Conn.**
1	10L400	600:5	1-2
2	10L800	1200:5	1-2
4	2.5L200	300:5	1-2

Table A.2: Voltage and current output of high voltage winding with different tap positions (Fig. A.1 - (a)).

Tap Changer		**Amps**	**Amps**	**Amps**	**Voltage**
Pos.	**Conn.**	**ONAN**	**ONAF**	**ONAF**	**(V)**
1	A-B	311	416	522	148350
2	B-C	319	426	534	144900
3	C-D	327	437	547	141450
4	D-E	335	448	561	138000
5	E-F	343	459	575	134550

Table A.3: Voltage and current output of low voltage winding (Fig. A.1 - (b)).

Amps	**Amps**	**Amps**	**Voltage**
ONAN	**ONAF**	**ONAF**	**(V)**
3347	4477	5606	13800

Table A.4: Basic Insulation Levels (BIL).

Type	**H.V.**	**L.V.**	**Neutral**
Impulse Level Full Wave (kV)	550	110	110

A.5 Sweep Frequency Response Analyzer (SFRA) (Manufacturer: Megger)

General
FRA Method: Sweep frequency (SFRA)
Frequency Range: 1 *Hz* - 10 *MHz*, user selectable
Extended Frequency Range: 0.1 *Hz* - 25 *MHz*, user selectable
Number of Points: User selectable, maximum 32,000
Points Spacing: Logarithmic, linear or combination of both
Dynamic Range/Noise Floor: >125dB (FRAX-99>115dB). Extended range: >110dB
Accuracy: ± 0.5 dB (FRAX-99 ±1 dB) down to -100 dB
IF Bandwidth/Integration Time: User selectable
Software: FRAX for Windows 2000/XP/Vista
PC Communication: Bluetooth (FRAX-101) and galvanic isolated USB
Calibration Interval: Maximum 3 years
Standards: Fulfill requirements in CIGRE Brochure 342, Mechanical Condition Assessment of Transformer Windings using FRA and Chinese standard DL/T 911-2004, FRA on Winding Deformation of Power Transformers

Analog Output
Channels: 1
Compliance Voltage: 0.2 - 20 V peak-to-peak
Measurement Voltage: at 50 Ω 0.1 - 10 V peak-to-peak
Output Impedance: 50 Ω
Protection: Short-circuit protected

Analog Inputs
Channels: 2
Sampling: Simultaneously, 100MS/s
Input Impedance: 50 Ω

Physical
Instrument Weight: 1.4 kg/3.1 lsb, 1.9 kg (FRAX-101 with Battery)
Dimensions: 250 x 169 x 52 mm (9.84 x 6.65 x 2.05 in.)
Input Voltage: 90-135 VAC and 170-264 VAC, 47-63 Hz

Environmental
Operating Ambient Temperature: -20°C to 50°C (-4°F to 122°F), Bluetooth 0°C to

50°C
Operating Relative Humidity: < 90% non-condensing
Storage Ambient Temperature: -20°C to 70°C
Storage Relative Humidity: < 90% non-condensing
CE Standards: IEC61010 (LVD) EN61326 (EMC)

PC requirements
Operating System: Windows 2000, Windows XP or Windows Vista
Processor: Pentium 500 MHz or higher
Memory/Hard Drive: 256 MByte / 30 MByte free or more
Interface: Bluetooth (FRAX-101 only) and USB

A.6 Oscilloscope and Signal Generator (Manufacturer: Agilent Technologies)

General
Model: InfiniiVision 3024A
Bandwidth (3 dB): 200 MHz
Calculated rise time (10 - 90%): 1.75 ns
Input channels: 4 (DSOX) and 4 + 16 (MSOX)
Maximum sample rate: 4 GSa/s half channel, 2 GSa/s all channel
Maximum memory depth: 2 Mpts, optional 4 Mpts and optional segment memory
Display size and type: 8.5-inch WVGA display
Waveform update rate: > 1 million waveforms per second
Number of active probes supported: 2

Vertical system analog channels
Hardware bandwidth limits: Approximately 20 MHz (selectable)
Input coupling: AC, DC
Input impedance: Selectable: 1 MΩ ± 1% (14 pF), 50 Ω ± 1.5%
Input sensitivity range: 1 mV/div to 5 V/div (1 MΩ and 50 Ω)
Vertical resolution: 8 bits (measurement resolution is 12 bits with averaging)
Maximum input voltage: 300 Vrms, 400 Vpk; transient overvoltage 1.6 kVpk
DC vertical accuracy: ± [DC vertical gain accuracy + DC vertical offset accuracy + 0.25% full scale]
DC vertical gain accuracy: ± 2.0% full scale
DC vertical offset accuracy: ± 0.1 div 2 mV ± 1% of offset setting
Channel-to-channel isolation: > 100:1 from DC to maximum specified bandwidth of each model
Offset range: ± 2 V (1 mV/div to 200 mV/div) and ± 50 V (> 200 mV/div to 5 V/div)

Vertical system digital channels
Digital input channels: 16 digital (D0 to D15. pod 1: D7 ∼ D0, Pod 2: D15 ∼ D8)

Thresholds: Threshold per pod
Threshold selections: TTL (+1.4 V), 5V CMOS (+2.5 V), ECL (1.3 V), user-defined (selectable by pod)
User-defined threshold range: ± 8.0 V in 10 mV steps
Maximum input voltage: ± 40 V peak CAT I; transient overvoltage 800 Vpk
Threshold accuracy: ± (100 mV + 3% of threshold setting)
Maximum input dynamic range: ± 10 V about threshold
Minimum voltage swing: 500 mVpp
Input impedance: 100 kΩ ± 2% at probe tip
Input capacitance: ∼ 8 pF

Horizontal system analog channels
Time base range: 2 ns/div to 50 s/div
Time base accuracy: 25 ppm ± 5 ppm per year (aging)
Time base delay time range: Greater of 1 screen width or 250 μs (Pre-trigger), 1 s to 500 s (Post-trigger)
Channel-to-channel deskew range: ± 100 ns
Δ Time accuracy (using cursors): ± (time base acc. x reading) ± (0.0016 x screen width) ± 100 ps
Modes: Main, zoom, roll, XY
XY: On channels 1 and 2 only. Z Blanking on ext trigger input, 1.4 V threshold.
Bandwidth: Maximum bandwidth. Phase error at 1 MHz: < 0.5 degree.

Horizontal system digital channels
Minimum detectable pulse width: 5 ns
Channel-to-channel skew: 2 ns (typical); 3 ns (maximum)

Environmental and other characteristics
Power line consumption: 100 watts
Power voltage range: 100-120V, 50/60/400 Hz; 100-240V, 50/60 Hz ± 10% auto ranging
Temperature Operating: 0 to +55°C
Non-operating: 30 to +71°C
Humidity Operating: Up to 80% RH at or below +40°C; up to 45% RH up to +50°C
Non-operating: Up to 95% RH up to 40°C; up to 45% RH up to 50°C
Altitude Operating: up to 4,000 m, Non-operating 15,300 m
Dimensions: 381 mm (15 in) W x 204 mm (8 in) H x 142 mm (5.6 in) D
Weight Net: 3.9 kg (8.5 lbs), shipping: 4.1 kg (9.0 lbs)

Appendix B

Results

B.1 Results of Synthesized Circuit Elements

This section contains the circuit element values derived for the test circuit (see Fig. 3.4) and for the transformer (see Fig. 2.8).

B.1.1 Synthesized Circuit Elements of The Test Circuit

The derivation of circuit elements is done as explained in Chapter 3. Three separate circuit segments related to Y_{11}, Y_{12} and Y_{22} were obtained as shown in the Fig. B.1. The numerical values of circuit elements is shown in Tables B.1, B.2 and B.3.

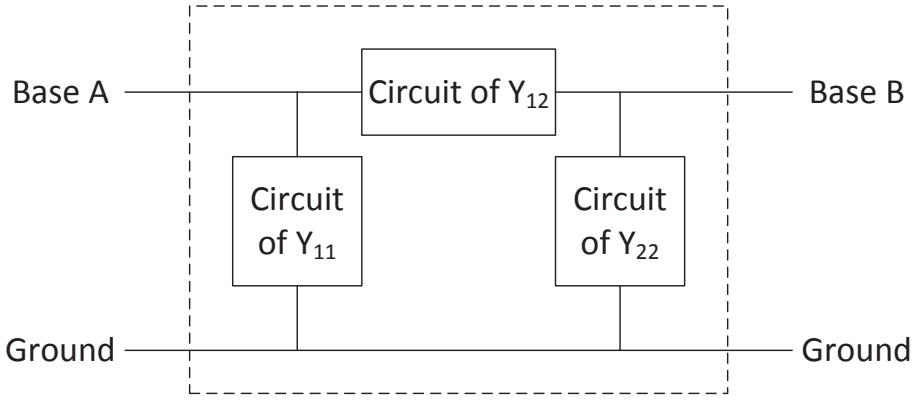


Figure B.1: Connection block diagram of circuit segments derived for test circuit of Fig. 3.4.

Table B.1: Numerical values of circuit elements obtained for circuit of Y_{11} of the test circuit.

Coefficient	**Start**	**End**	**R (Ω)**	**L (H)**	**C (μF)**
Constants	Base A	Ground	9.97E+01	0	0
	Base A	Ground	0	0	3.00E-10
Real Poles	Base A	Ground	-1.43E+16	-9.10E+10	0
	Base A	Ground	1.08E+13	1.96E+06	0
	Base A	Ground	-8.61E+03	-3.89E-05	0
	Base A	Ground	1.06E+24	3.33E+15	0
	Base A	Ground	1.36E+24	3.33E+15	0
	Base A	Ground	2.20E+24	3.33E+15	0
	Base A	Ground	2.38E+24	3.33E+15	0
	Base A	Ground	3.00E+24	3.33E+15	0
	Base A	Ground	3.05E+24	3.33E+15	0
	Base A	Ground	3.79E+24	3.33E+15	0
	Base A	Ground	4.18E+24	3.33E+15	0
	Base A	Ground	4.88E+25	3.33E+15	0
Complex Conjugate Pole Pairs	Base A	Base 3	1.54E+16	6.30E+11	0
	Base 3	Ground	1.78E+16	0	0
	Base 3	Ground	0	0	8.57E-15
	Base A	Base 4	1.46E+08	1.55E+00	0
	Base 4	Ground	-1.90E+08	0	0
	Base 4	Ground	0	0	1.10E-10
	Base A	Base 5	-1.19E+04	-2.49E-04	0
	Base 5	Ground	-2.08E+04	0	0
	Base 5	Ground	0	0	-4.38E-07
	Base A	Base 6	-5.08E+04	1.44E-04	0
	Base 6	Ground	5.97E+04	0	0
	Base 6	Ground	0	0	2.78E-08

Table B.2: Numerical values of circuit elements obtained for circuit of Y_{12} of the test circuit.

Coefficient	**Start**	**End**	**R (Ω)**	**L (H)**	**C (μF)**
Constants	Base A	Base B	1.47E-02	0	0
	Base A	Base B	0	0	-1.00E-10
Real Poles	Base A	Base B	-1.58E+14	-1.01E+09	0
	Base A	Base B	7.99E+08	1.44E+02	0
	Base A	Base B	-1.31E-02	-5.91E-11	0
	Base A	Base B	-3.18E+24	-1.00E+16	0
	Base A	Base B	-4.09E+24	-1.00E+16	0
	Base A	Base B	-6.60E+24	-1.00E+16	0
	Base A	Base B	-7.14E+24	-1.00E+16	0
	Base A	Base B	-9.01E+24	-1.00E+16	0
	Base A	Base B	-9.16E+24	-1.00E+16	0
	Base A	Base B	-1.14E+25	-1.00E+16	0
	Base A	Base B	-1.25E+25	-1.00E+16	0
	Base A	Base B	-1.46E+26	-1.00E+16	0
Complex Conjugate Pole Pairs	Base A	Base 7	1.79E+14	6.72E+09	0
	Base 7	Base B	3.47E+14	0	0
	Base 7	Base B	0	0	6.52E-13
	Base A	Base 8	1.75E+02	5.63E-06	0
	Base 8	Base B	3.17E+02	0	0
	Base 8	Base B	0	0	2.04E-04
	Base A	Base 9	2.73E-01	-1.81E-09	0
	Base 9	Base B	-3.58E-01	0	0
	Base 9	Base B	0	0	-9.06E-03
	Base A	Base 10	-4.77E-02	-1.36E-10	0
	Base 10	Base B	9.73E-02	0	0
	Base 10	Base B	0	0	-1.02E-01

Table B.3: Numerical values of circuit elements obtained for circuit of Y_{22} of the test circuit.

Coefficient	**Start**	**End**	**R (Ω)**	**L (H)**	**C (μF)**
Constants	Base B	Ground	1.20E+02	0	0
	Base B	Ground	0	0	3.00E-10
Real Poles	Base B	Ground	-3.02E+15	-1.93E+10	0
	Base B	Ground	1.42E+13	2.56E+06	0
	Base B	Ground	-1.15E+04	-5.18E-05	0
	Base B	Ground	1.06E+24	3.33E+15	0
	Base B	Ground	1.36E+24	3.33E+15	0
	Base B	Ground	2.20E+24	3.33E+15	0
	Base B	Ground	2.38E+24	3.33E+15	0
	Base B	Ground	3.00E+24	3.33E+15	0
	Base B	Ground	3.05E+24	3.33E+15	0
	Base B	Ground	3.79E+24	3.33E+15	0
	Base B	Ground	4.18E+24	3.33E+15	0
	Base B	Ground	4.88E+25	3.33E+15	0
Complex Conjugate Pole Pairs	Base B	Base 11	4.91E+15	2.83E+11	0
	Base 11	Ground	2.22E+15	0	0
	Base 11	Ground	0	0	3.27E-14
	Base B	Base 12	1.97E+08	2.08E+00	0
	Base 12	Ground	-2.56E+08	0	0
	Base 12	Ground	0	0	8.10E-11
	Base B	Base 13	-1.59E+04	-3.32E-04	0
	Base 13	Ground	-2.77E+04	0	0
	Base 13	Ground	0	0	-3.30E-07
	Base B	Base 14	-6.73E+04	1.91E-04	0
	Base 14	Ground	7.91E+04	0	0
	Base 14	Ground	0	0	2.10E-08

B.1.2 Synthesized Circuit Elements of the Transformer

Table B.4: Numerical values of circuit elements obtained for circuit of H_1 of the transformer.

Coefficient	**Start**	**End**	**R (Ω)**	**L (H)**	**C (μF)**
Constants	Base A	Ground	1.00E+06	0	0
	Base A	Ground	0	0	1.99E-06
Real Poles	Base A	Ground	-4.58E+00	1.09E+01	0
	Base A	Ground	1.25E+00	1.18E-01	0
	Base A	Ground	1.77E+01	4.75E-01	0
	Base A	Ground	5.47E+00	7.83E-02	0
	Base A	Ground	9.23E+02	1.54E+00	0
	Base A	Ground	1.08E+04	3.23E-01	0
	Base A	Ground	5.08E+03	6.11E-03	0
	Base A	Ground	-2.38E+04	-1.21E-03	0
Complex Conjugate Pole Pairs	Base A	Base 3	1.68E+04	-2.23E+04	0
	Base 3	Ground	-1.44E+06	0	0
	Base 3	Ground	0	0	-9.08E-01
	Base A	Base 4	9.81E+03	-5.60E+03	0
	Base 4	Ground	-2.08E+05	0	0
	Base 4	Ground	0	0	-2.41E+00
	Base A	Base 5	-8.82E+07	-2.71E+05	0
	Base 5	Ground	8.83E+07	0	0
	Base 5	Ground	0	0	-3.48E-05
	Base A	Base 6	1.03E+06	1.72E+04	0
	Base 6	Ground	-1.05E+06	0	0
	Base 6	Ground	0	0	1.61E-02
	Base A	Base 7	8.76E+03	-7.22E+02	0
	Base 7	Ground	-1.60E+04	0	0
	Base 7	Ground	0	0	-4.49E+00

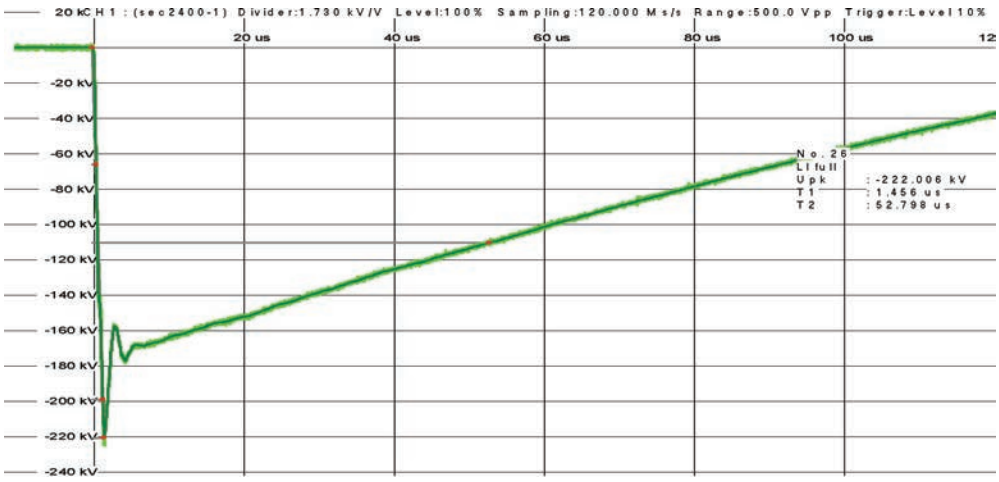
Coefficient	Start	End	R (Ω)	L (H)	C (μF)
Complex Conjugate Pole Pairs	Base A	Base 8	-1.56E+06	-1.83E+04	0
	Base 8	Ground	1.60E+06	0	0
	Base 8	Ground	0	0	-7.37E-03
	Base A	Base 9	-4.50E+07	-1.31E+05	0
	Base 9	Ground	4.51E+07	0	0
	Base 9	Ground	0	0	-6.45E-05
	Base A	Base 10	-1.60E+05	-4.47E+03	0
	Base 10	Ground	2.45E+05	0	0
	Base 10	Ground	0	0	-1.19E-01
	Base A	Base 11	1.53E+03	8.74E-02	0
	Base 11	Ground	2.36E+06	0	0
	Base 11	Ground	0	0	3.75E-04
	Base A	Base 12	1.22E+03	1.08E-01	0
	Base 12	Ground	9.38E+05	0	0
	Base 12	Ground	0	0	1.60E-04
	Base A	Base 13	-1.35E+03	5.46E-02	0
	Base 13	Ground	2.19E+05	0	0
	Base 13	Ground	0	0	7.35E-05
	Base A	Base 14	-2.37E+03	7.90E-02	0
	Base 14	Ground	3.86E+05	0	0
	Base 14	Ground	0	0	3.85E-05
	Base A	Base 15	8.18E+03	3.34E-02	0
	Base 15	Ground	-1.45E+05	0	0
	Base 15	Ground	0	0	4.31E-05
	Base A	Base 16	2.03E+04	2.07E-02	0
	Base 16	Ground	-4.88E+04	0	0
	Base 16	Ground	0	0	2.40E-05
	Base A	Base 17	1.57E+03	-4.31E-03	0
	Base 17	Ground	-1.13E+04	0	0
	Base 17	Ground	0	0	-1.28E-04

Coefficient	Start	End	R (Ω)	L (H)	C (μF)
Complex Conjugate Pole Pairs	Base A	Base 18	-8.13E+04	-1.53E-02	0
	Base 18	Ground	8.83E+04	0	0
	Base 18	Ground	0	0	-2.23E-06
	Base A	Base 19	4.52E+02	2.77E-04	0
	Base 19	Ground	-2.02E+04	0	0
	Base 19	Ground	0	0	1.13E-03
	Base A	Base 20	3.67E+06	-1.28E-01	0
	Base 20	Ground	-3.76E+06	0	0
	Base 20	Ground	0	0	-8.37E-09
	Base A	Base 21	3.96E+02	3.10E-04	0
	Base 21	Ground	-2.53E+04	0	0
	Base 21	Ground	0	0	6.12E-05
	Base A	Base 22	9.88E+03	1.93E-03	0
	Base 22	Ground	-3.34E+04	0	0
	Base 22	Ground	0	0	6.44E-06
	Base A	Base 23	-1.41E+04	-1.29E-02	0
	Base 23	Ground	2.25E+06	0	0
	Base 23	Ground	0	0	-8.40E-07

B.2 Results of Lightning Impulse Test

This section contains the automatically generated impulse test reports from the impulse recording system at Manitoba Hydro HVTF.

B.2.1 Case I - Impulse Test Report



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<Title2>+<Field2>	Test Technicians NP, JW, A		
<Title3>+<Field3>	Inspector	<MemoIndex1>	
<Title4>+<Field4>	Standards		
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<Title7>+<Field7>	Air temperature 22 C		
<Title8>+<Field8>			
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<TerminalNa>	sec2400-1	<NotesTXT>	Switching impulse counter No. 1 DTC on tap 5, H1-H0 front resistors (series) - 15 ohms Tail resistors (parallel) 110 ohms
<TerminalDi>	1730		
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<SamplinhRa>	120.000 Ms		
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<TestAmplit>	500.000 kV		
<CurveTypeT>	Full lightning impulse		
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<MinPeak>	0.000 V		
<Standards>			
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<ErrorText>			
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<FullInfo_T>	26 LI full -222.006 kV 1.456 us 52.798 us		
<FullInfo_C>	No. 26 LI full Upk: -222.006 kV T1: 1.456 us T2: 52.798 us		
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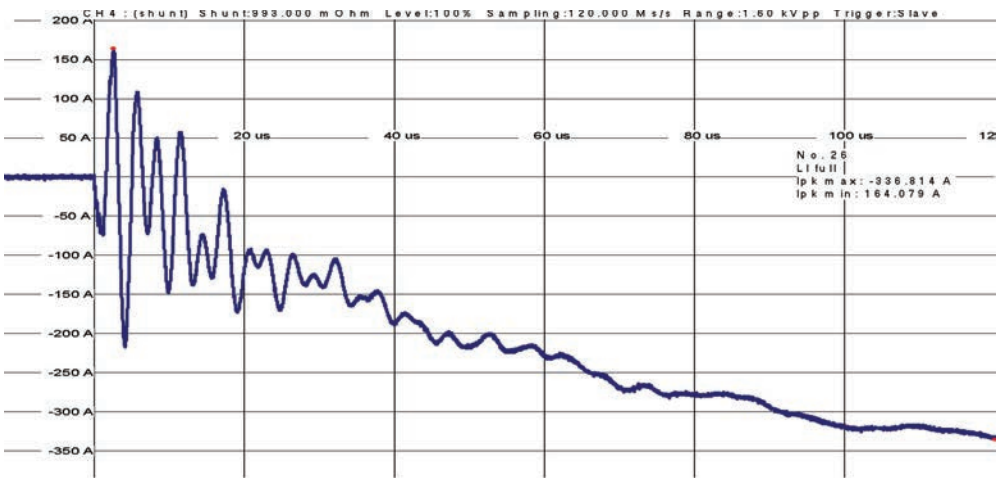
<ChannelCal>	12/13/2010		

Figure B.2: Case I - Impulse Test Report :Voltage Waveform.



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<FullInfo_T>	26 LI full -336.814 A 164.079 A		
<FullInfo_C>	No. 26 LI full Ipk max: -336.814 A Ipk min: 164.079 A		
<ChannelNum>	4		
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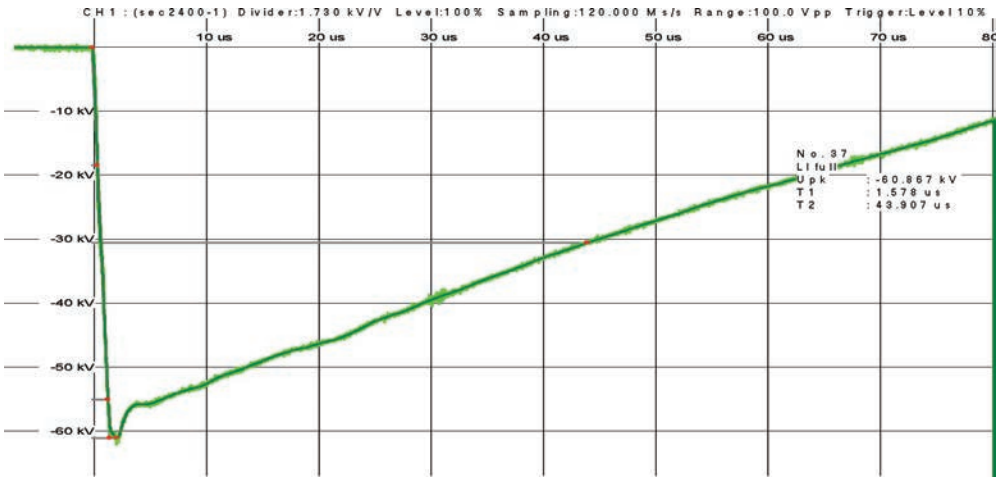
Figure B.3: Case I - Impulse Test Report :Current Waveform.

B.2.2 Case II - Impulse Test Report



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<FullInfo_T>	37 LI full -60.867 kV 1.578 us 43.907 us		
<FullInfo_C>	No. 37 LI full Upk: -60.867 kV T1: 1.578 us T2: 43.907 us		
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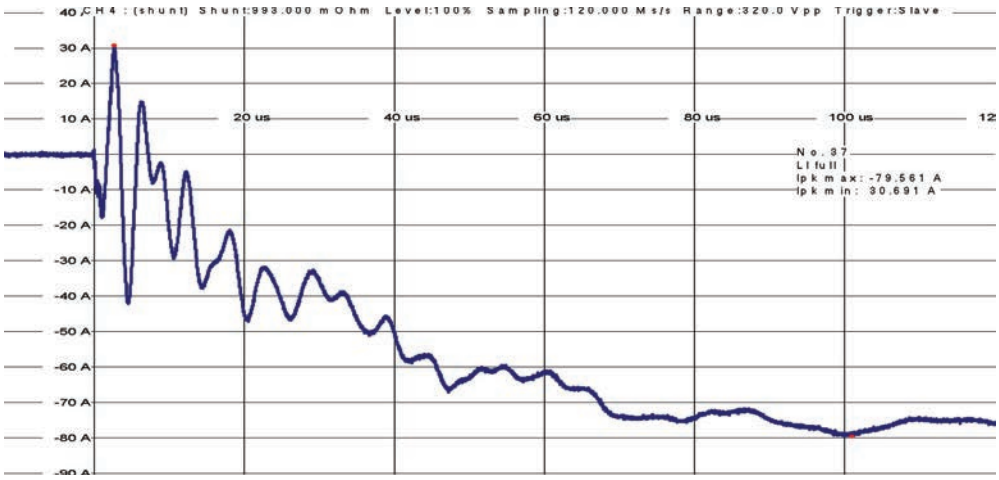
Figure B.4: Case II - Impulse Test Report : Voltage Waveform.



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<Title7>+<Field7>	Air temperature 22 C		
<Title8>+<Field8>			
<SoftwareVe>	5.11		
<TerminalNa>	shunt	<NotesTXT>	DTC on tap 5, H2-H0 6 Stages front resistors (series) - 19.5 ohms Tail resistors (parallel) - 76 ohms
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<Standards>			
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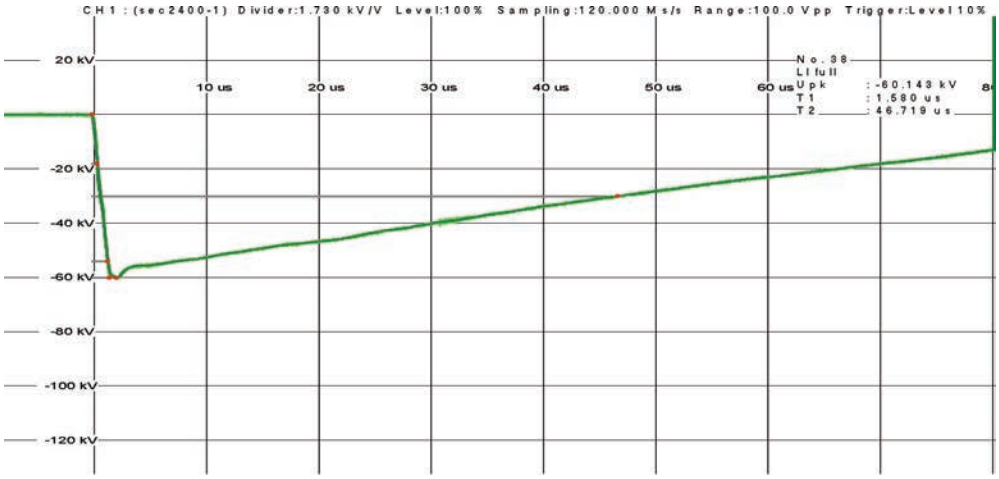
Figure B.5: Case II - Impulse Test Report : Current Waveform.

B.2.3 Case III - Impulse Test Report



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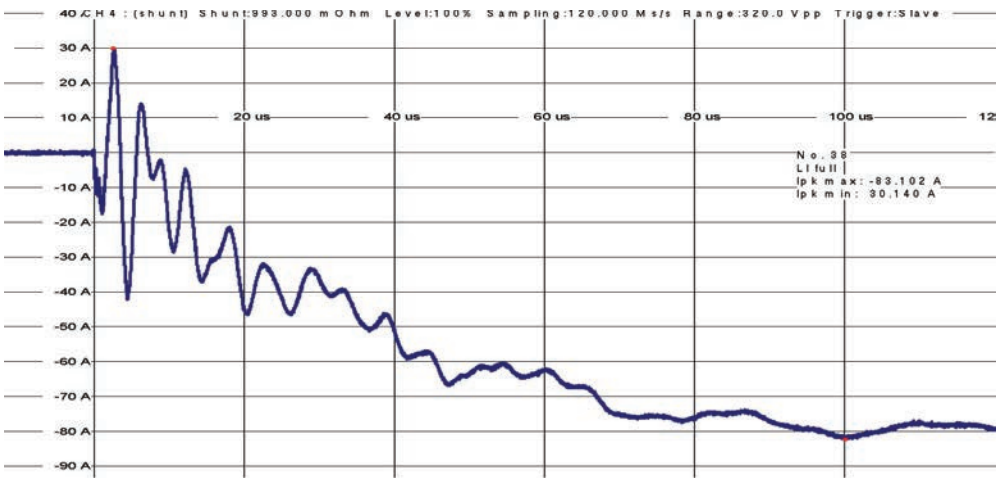
<ErrorText>			
<HWInfo_TAB>	CH1 : (sec2400-1) Divider:1.730 kV/V Level:100% Sampling:120.000 Ms/s Range:100.0 Vpp T		
<FullInfo_T>	38 LI full -60.143 kV 1.580 us 46.719 us		
<FullInfo_C>	No. 38 LI full Upk: -60.143 kV T1: 1.580 us T2: 46.719 us		
<ChannelNum>	1		
<ChannelCal>	12/13/2010		

Figure B.6: Case III - Impulse Test Report : Voltage Waveform.



<Table field name>	Table field value		
<Datanmuber>	3988	<CharData>	No. 38 LI full Ipk max: -83.102 A Ipk min: 30.140 A
<Index1>	KETTLE TRANSFORMER		
<Index2>	LIGHTNING IMPULSE H2 KA		
<Timestamp>	4/10/2014 9:49:38 AM		
<Counter>	38		
<Title1>+<Field1>	Test manager Nathan Jacob		
<Title2>+<Field2>	Test Technicians NP, JW, A		
<Title3>+<Field3>	Inspector	<MemoIndex1>	
<Title4>+<Field4>	Standards		
<Title5>+<Field5>	Air pressure		
<Title6>+<Field6>	Air humidity 45 %		
<Title7>+<Field7>	Air temperature 22 C		
<Title8>+<Field8>			
<SoftwareVe>	5.11		
<TerminalNa>	shunt	<NotesTXT>	DTC on tap 4, H2-H0 6 Stages Series and Parallel resistors mixed - each stage different Counter 38
<TerminalDi>	0.993		
<TerminalRa>	322.256 A		
<MeasuringU>	A		
<MeasuringT>	120.000 us		
<SamplinhRa>	120.000 Ms		
<FullAmplit>	150.000 A		
<TestAmplit>	150.000 A		
<CurveTypeT>	Full lightning impulse		
<MaxPeak>	-83.102 A		
<MinPeak>	30.140 A		
<Standards>			
<ManualEval>	False		
<ErrorText>			
<HWInfo_TAB>	CH4 : (shunt) Shunt:993.000 mOhm Level:100% Sampling:120.000 Ms/s Range:320.0 Vpp Tri		
<FullInfo_T>	38 LI full -83.102 A 30.140 A		
<FullInfo_C>	No. 38 LI full Ipk max: -83.102 A Ipk min: 30.140 A		
<ChannelNum>	4		
<ChannelCal>	12/7/2010		

Figure B.7: Case III - Impulse Test Report : Current Waveform.