

THE UNIVERSITY OF MANITOBA

WAVE DIGITAL ADAPTORS FOR BRUNE,
DARLINGTON C AND D, AND TWIN-T SECTIONS

BY

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A dissertation submitted to the Faculty of Graduate Studies of
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ABSTRACT

This thesis is concerned with the derivation of new wave adaptors for the Brune section, the Darlington C and D sections, and an adaptor for the Twin-T structure.

These wave adaptors have been derived by applying Martens' and Meerkötter's n-port voltage scattering matrix representation to the corresponding reference network interconnections.

The following results have been obtained:

- a) The Brune, C and D adaptors are realized without any unit elements.
- b) The adaptors in a) are canonical in the number of delays.
- c) All the adaptors considered may have a reflection-free port which makes cascade synthesis possible.
- d) The Brune and C adaptors require six multipliers, four of which are independent and two of which are identical.
- e) The D adaptor requires a total number of eleven multipliers, seven of which are independent and two pairs of which are identical.
- f) The Twin-T adaptor requires ten multipliers of which seven are independent.
- g) In a hardware realization, all the adaptors considered are made to have zero output after a finite time for zero input by means of a simple arithmetic procedure.

Illustrative examples of filters using these structures have

been designed, and simulated on a minicomputer. Their respective impulse responses are obtained and show no granularity and/or overflow oscillations, as expected.

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CHAPTER I

INTRODUCTION

It is well known [1] that real-time digital filters have several advantages over continuous-time filters. A greater degree of accuracy can be attained in the digital filter realization. A greater variety of digital filters can be built, since certain realization problems do not arise, for example negative circuit elements. No aging process can affect the parameters of the digital filter. In addition, they can operate down to extremely low frequencies where the size of analog components becomes appreciable.

There are at least three techniques for designing infinite impulse response recursive digital filters which are derived from a transformation of the transfer function of continuous-time filters. They are, namely, the impulse invariance, the bilinear transformation and the matched z-transform techniques [2]. The resulting realization will have either a direct form or a canonic form as mentioned by Oppenheim and Schaffer [3]. The structure to be used must be chosen according to the computational complexity and mainly to its sensitivity to finite-register-length effects. It is to be expected that some of these structures will be less sensitive than others to quantization of the parameters; i.e., the system function of the realization will be a closer approximation of the desired system function. Unfortuna-

tely, no systematic method has yet been developed for determining the best realization given constraints on the number of multipliers, word length, and the number of delays. In place of a detailed mathematical analysis of the parameter-sensitivity problem, a common practical approach is the use of simulation for determining acceptable quantization of the parameters of a given network. Due to the finite word length, zero input limit cycles and overflow oscillations can occur in recursive digital filters [4], [5]. Meerkötter and Wegener [6] and Verkroost and Butterweck [7] have derived structures for a second-order digital filter section which are free of limit cycles when magnitude truncation is used for quantization, and which do not have overflow oscillations. However, for higher order conventional digital filters, no general theory has yet been developed to eliminate those undesirable oscillations [8].

In order to obtain a solution to these sensitivity and stability problems of digital filters, Fettweis [9] has derived a class of digital filter which has the stopband insensitivity of ladder structures combined with the passband insensitivity of resistance-terminated LC filters. These so called Wave Digital Filters [9] have been essentially derived from the continuous-time filters by applying the bilinear transformation (defined as follows) directly to the circuit elements of the linear continuous-time filter. In the continuous-time filter, the frequency s is replaced by the frequency variable Ψ defined by

$$\Psi = \frac{1 - e^{-sT}}{1 + e^{-sT}} = \frac{1 - z^{-1}}{1 + z^{-1}} = \tanh \left(\frac{sT}{2} \right) \quad (1.1)$$

and for $s = j\omega$, (1.1) can be written as

$$\Psi = j\phi, \quad \phi = \tan \frac{\omega T}{2} = \tan \frac{\pi f}{f_s} \quad (1.2)$$

where $T = \frac{1}{f_s}$ = the sampling interval; and voltage waves are used

as the signal variables so that the reactance elements are characterized by a delay.

A list of some circuit elements together with their corresponding wave flow diagrams as derived by Fettweis [10] is given in Appendix I.

By means of the wave adaptors [11] such as the two-port adaptor, the n-port parallel adaptor and the n-port series adaptor, Fettweis and Sedlmeyer [12] have obtained a true ladder wave digital structure from a resistance-terminated LC ladder network.

Such a wave digital realization has the following advantages over the conventional digital realization of a transfer function. First, due to the insensitivity in the stopband as well as in the passband, a drastic reduction in the coefficient word length is possible [13,14,15]. Secondly, it has been shown by Fettweis and Meerkötter [16], and by Claasen et al. [5] that it is much easier to eliminate parasitic oscillations, both granularity and overflow, in such a wave structure. Thirdly, though there are handbooks of digital filter synthesis, it is still convenient to translate directly any well-known classical ladder filter into a wave digital form.

It is known that resistance-terminated LC filters can be

realized by using Darlington's cascade synthesis as interpreted by Guillemin [17] and Youla [18], or as in Fettweis' cascade synthesis by transfer matrix factorization [19]. The LC filter is realized in both methods by cascading zeroth, first, second and fourth order sections. Fettweis' and Sedlmeyer's ladder wave structure is only capable of realizing transmission zeros on the imaginary axis of the complex s -plane. Using the ladder structure, a digital Brune section can be realized with five multipliers and four delays. However, one of the port resistances is negative and the resulting wave structure is not guaranteed to be free of limit cycles [20].

Also, the wave digital lattice [21] or Jauman structure [22] is restricted because it realizes only symmetric reference filters. Thus, other adaptors must be introduced if we want to have a wave cascade synthesis translated directly from a cascade synthesis realization in the continuous-time domain. That such a wave cascade synthesis is possible has been shown by Nouta [23] by the introduction of wave adaptors for the reciprocal and non-reciprocal zeroth, first, second-order sections. In particular, Nouta's wave digital realization of the reciprocal second-order section requires six multipliers and three delays. A direct realization of the transfer function of the second-order section would require a minimum number of four multipliers and a minimum number of two delays. For the reciprocal Darlington D section, Nouta has referred to Scanlan and Rhodes [24] where the cascading of a fourth-order reciprocal section and a unit element, if translated into the wave digital form, would require ten multipliers and seven delays, while the canonic numbers of multipliers and delays are, respectively, seven

and four. However, Nouta has "passified", the introduced structures in a strictly linear sense only and the given cascade synthesis procedure suffers from the disadvantage that each section can only be realized with a cascaded unit element.

Fahmy's digital realization of the Darlington C section from a microwave structure using two-wire coupled line [25] is canonic in the number of delays but requires a total number of ten multipliers. Also, his digital realization of the Darlington D section is canonic in the number of delays but the number of multipliers would certainly exceed eleven. Scanlan's and Fagan's [26] wave digital realization of the C section requires five multipliers and three delays. As in the case of Fahmy's paper, Scanlan's and Fagan's paper does not offer any realization scheme by which the hardware realization of the section will be guaranteed to be free of zero input oscillations.

The purpose of this thesis is to derive new wave adaptors for the reciprocal sections mentioned above, namely, the Brune section, the Darlington C and D sections with the following properties : Firstly, wave digital realizations with the canonic number of delays; secondly, without any unit elements ; thirdly, with the possibility of having reflection-free ports, and finally, with a truncation scheme to guarantee zero input asymptotic stability.

These new wave adaptors have been derived by applying an extended version of Martens' and Meerkötter's [27] n-port voltage scattering matrix representation to the considered sections. Also, by following Martens' and Meerkötter's scheme for deriving a Bridge-Tee adaptor, we present an adaptor for the Twin-T structure which is used

in classical cascade synthesis.

In Chapter II, a brief review of Martens' and Meerkötter's method and its extension to the Brune section, the Darlington C and D sections are presented. A general formulation is derived for the case of an adaptor with a reflection-free port and for the "dependent-multiplier equations" which relate the dependent multipliers to the independent multipliers. Problems in the hardware realization of the adaptors are discussed and a theorem on the stability of the investigated structures is given. In order to implement magnitude truncation, a few simple rules to calculate the output error of the actual nonlinear filter output with respect to the output of the non-realizable associated linear filter are given.

In Chapters III, IV and V, respectively, the necessary formulas and wave flow diagrams for the design of the wave digital realization of the Brune and Darlington C section, the Darlington D section and the Twin-T structure are presented.

Chapter VI provides a magnitude truncation method which guarantees the asymptotic stability of the investigated adaptors under zero input. Details of the design of these adaptors are given step by step. Three illustrative examples of filters which have been designed and simulated on a PDP 11/40 computer system are described.

CHAPTER II

GENERAL FORMULATION FOR THE WAVE DIGITAL REALIZATION OF THE TWIN-T, BRUNE, C AND D SECTIONS

2.1 REVIEW OF MARTENS' AND MEERKÖTTER'S METHOD

In this thesis, we extend Martens' and Meerkötter's method to the case of a reciprocal n-port which may include ideal transformers. Upon partitioning the ports of the reference network interconnections into two sets : "link" ports and "tree" ports, Martens' and Meerkötter's method is applicable if we are able to write the "cutset matrix" Q and the "circuit matrix" B to express the vectors i and v of port currents and voltages as a function of the link currents and tree voltages, respectively,

$$i = B^T i_\ell \quad (2.1)$$

$$v = Q^T v_t \quad (2.2)$$

The subscripts t and ℓ identify the "tree" and "link" ports, respectively; the superscript T denotes transpose. We note that B and Q must satisfy the orthogonality condition; i.e., $BQ^T = 0$.

In particular, this is possible with the Brune section, the

Darlington C and D sections; and the following results will hold.

Let the incident and reflected voltage wave vectors be defined as

$$a = v + Ri \quad (2.3)$$

$$b = v - Ri \quad (2.4)$$

respectively, where R is a diagonal matrix of the port resistances, then we have

$$b = Sa \quad (2.5)$$

where S is the scattering matrix.

Partitioning $Q = [Q_\ell \ U]$, $B = [U \ B_t]$ where U denotes the unit matrix, and $G = R^{-1} = \begin{bmatrix} G_\ell & 0 \\ 0 & G_t \end{bmatrix}$ according to "link" and "tree" ports, and defining

$$K = [QQ^T]^{-1}Q_\ell G_\ell = [G_t + Q_\ell G_\ell Q_\ell^T]^{-1}Q_\ell G_\ell \quad (2.6)$$

yields the following equivalent representations [27] :

$$S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \quad (2.7)$$

$$= \begin{bmatrix} 2Q_\ell^T K - U & 2Q_\ell^T - 2Q_\ell^T K Q_\ell^T \\ 2K & U - 2K Q_\ell^T \end{bmatrix} \quad (2.8)$$

$$= \begin{bmatrix} -U & Q_\ell^T \\ 0 & U \end{bmatrix} \begin{bmatrix} -U & 0 \\ -2K & U \end{bmatrix} \begin{bmatrix} -U & Q_\ell^T \\ 0 & U \end{bmatrix} \quad (2.9)$$

$$= \begin{bmatrix} -U & 0 \\ 0 & U \end{bmatrix} \begin{bmatrix} U & B_t \\ 0 & U \end{bmatrix} \begin{bmatrix} U & 0 \\ 2K & U \end{bmatrix} \begin{bmatrix} U & B_t \\ 0 & U \end{bmatrix} \quad (2.10)$$

We note that U is a unit matrix of appropriate dimensions in each case and all three matrices in (2.9) are self-inverse, hence

$$S = S^{-1} \quad (2.11)$$

i.e., S is also self-inverse.

From the definition of K (2.6), it can be shown that

$$S^T G = G S \quad (2.12)$$

and (2.11) and (2.12) yield

$$S^T G S = G \quad (2.13)$$

Equations (2.12) and (2.13), respectively, correspond to the reciprocity and the losslessness of the given reference network.

According to Martens and Meerkötter, the matrix K has a simple network interpretation obtained as follows: Terminate all the "link" ports in their port resistances in series with a voltage source and all the "tree" ports in their port resistances. Let e_ℓ denote the vector of "link" voltage sources, then we have

$$v_t = K e_\ell \quad (2.14)$$

where v_t is the vector of response voltages across the "tree" port resistances.

2.2 ADAPTOR WITH A REFLECTION - FREE PORT

In cascade synthesis, it is useful to have a reflection -free

port to avoid any delay-free loops which lead to an unrealizable wave flow diagram when we connect different sections together as shown in Fig. 2.1.

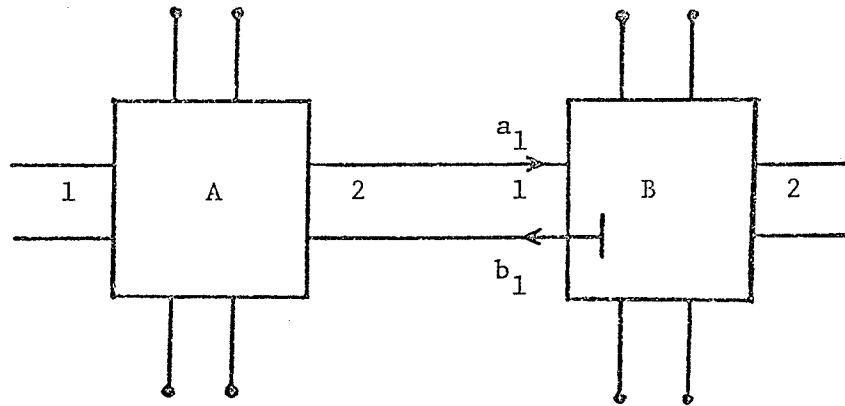


Fig. 2.1 Direct connection of adaptors with reflection-free ports.

From Fig. 2.1, port 1 of the adaptor B has been made reflection-free; i.e., the reflected wave b_1 is no longer dependent on the incident wave a_1 .

Let port 1 be a link port of the n -port network shown in Fig. 2.2. If we want to make it a reflection-free port then we must have the port resistance R_1 equal to the input resistance R_{in} of the reference network interconnections with all the remaining ports terminated in their respective port resistances R_2, R_3, \dots, R_n .

With $R_1 = R_{in}$, the entry s_{11} of the S matrix is equal to zero; i.e., no delay-free loop will occur. According to (2.8), s_{11}

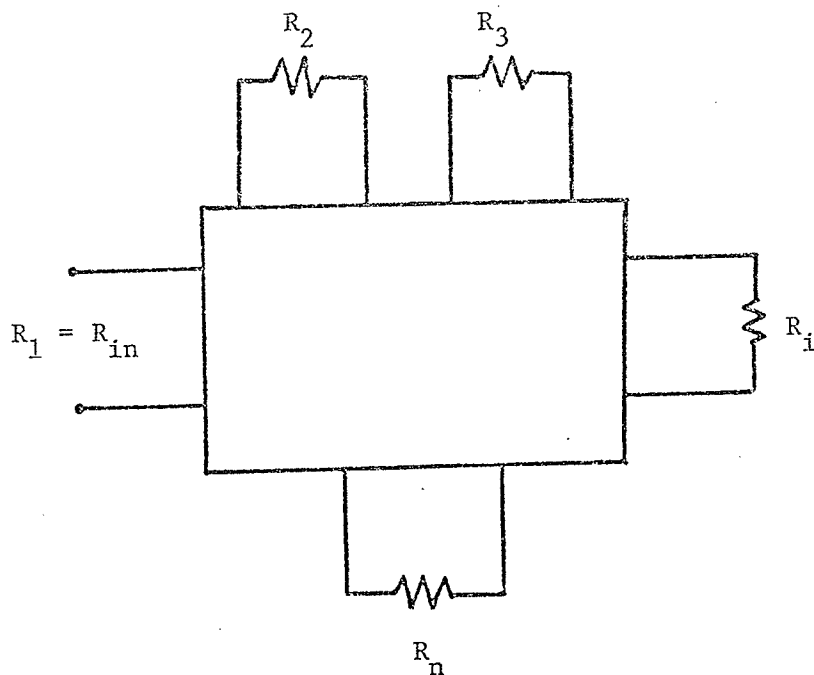


Fig. 2.2 Network used to determine R_{in} .

equal to zero also means that the (1,1) entry of the matrix

$[2Q_{\ell}^T K - U]$ is equal to zero. In other word, if we let

$$q_{ij} = [Q_{\ell}]_{ij} \quad \text{and} \quad k_{ij} = [K]_{ij}$$

then

$$s_{11} = [2Q_{\ell}^T K - U]_{11} = 0$$

yields

$$\sum_{j=1}^t q_{j1} (2k_{j1}) - 1 = 0 \quad (2.15)$$

or

$$q_{11} \cdot 2k_{11} = 1 - \sum_{j=2}^t q_{j1} \cdot 2k_{j1} \quad (2.16)$$

where t is the total number of "tree" branches.

Expression (2.16) shows that the existence of a reflection-free port reduces the number of independent multipliers by one.

2.3 DEPENDENT - MULTIPLIER EQUATIONS

The number of multipliers required to realize (2.10) is equal to the number of elements of the matrix K plus twice the number of multipliers which may be contained in the matrix B_t .

Given a reciprocal n -port together with a set R of n port resistances r_i

$$R = \{ r_i, i = 1 \text{ to } n \} \quad (2.17)$$

and a set N of p transformer ratios

$$N = \{ n_i, i = 1 \text{ to } p \} \quad (2.18)$$

we obtain a set of multipliers

$$T = \{ t_i, i = 1 \text{ to } s \} \quad (2.19)$$

upon writing the matrices $2K$ and B_t .

The set T may contain some or all the transformer ratios of the set N . In general, the number of elements of T exceeds the number of independent parameters of the network which determine the transfer function. Therefore, there are independent multipliers as well as dependent multipliers. The number of independent multipliers can be determined by inspection : It is equal to the total number of ports and

transformer ratios minus one; i.e., $n + p - 1$.

Among the elements of T , one can choose arbitrarily $n+p-1$ elements to form the subset M defined as the set of independent multipliers

$$M = \{ m_i, i = 1 \text{ to } n+p-1 \} \quad (2.20)$$

The remaining elements of T form the subset of dependent multipliers

$$H = \{ h_i, i = 1 \text{ to } s-n-p+1 \} \quad (2.21)$$

We note that $T = M + H$, where $+$ denotes set union.

For the structures investigated in this thesis, each element of H can be expressed explicitly as a function of the elements of M

$$h_i = f_i(M) = f_i(m_1, m_2, \dots, m_{n+p-1}) \quad (2.22)$$

for $i = 1$ to $s-n-p+1$.

These equations expressing the dependence among the multipliers can be determined by solving for the port conductance ratios of the network from the set of multipliers T and then checking for consistency among these solutions, as follows :

From (2.12), it is easy to derive the following equations

$$\frac{[G_\ell]_j}{[G_\ell]_i} = \frac{[Q_\ell^T K]_{ij}}{[K^T Q_\ell]_{ij}} = \frac{[Q_\ell^T K]_{ij}}{[Q_\ell^T K]_{ji}} \quad (2.23)$$

$$\frac{[G_t]_j}{[G_\ell]_i} = \frac{[Q_\ell^T - Q_\ell^T K Q_\ell^T]_{ij}}{[K]_{ji}} \quad (2.24)$$

$$\frac{[G_t]_j}{[G_t]_i} = \frac{[KQ_\ell^T]_{ij}}{[Q_\ell K^T]_{ij}} = \frac{[KQ_\ell^T]_{ij}}{[KQ_\ell^T]_{ji}} \quad (2.25)$$

The desired "dependent-multiplier equations" of the investigated structures, except for the Twin-T structure for which we have another approach, which will be presented in Chapter V, are easily obtained upon checking the consistency of the equations (2.23) to (2.25). For example, we must have

$$\frac{[G_\ell]_j}{[G_\ell]_i} = \frac{[G_t]_k}{[G_t]_i} \quad \text{for } k = 1, 2, \dots, t \quad (2.26)$$

2.4 HARDWARE REALIZATION

In a hardware realization, all the multipliers of the set T must be quantized to some finite number of bits due to the available finite word length. Thus, quantizing the set M of independent multipliers produces the set

$$\hat{M} = \left\{ \hat{m}_i = \frac{a_i}{2^{b_i}} = m_i - \sigma_i ; \quad i = 1 \text{ to } n+p-1 \right\} \quad (2.27)$$

where a_i and b_i are integers and σ_i is the coefficient quantization

error of the independent multipliers.

Corresponding to the set \hat{M} , we can calculate the set \hat{H} defined as

$$\hat{H} = \{ \hat{h}_i = f_i(\hat{M}) = h_i - \zeta_i ; i = 1 \text{ to } s-n-p+1 \} \quad (2.28)$$

where ζ_i is the coefficient deviation.

In general, the elements \hat{h}_i cannot be realized with a finite number of bits. These dependent multipliers \hat{h}_i must also be quantized in a hardware realization, and are denoted by the set

$$\tilde{H} = \{ \tilde{h}_i = \hat{h}_i - \delta_i = \frac{c_i}{2^i} ; i = 1 \text{ to } s-n-p+1 \} \quad (2.29)$$

where c_i and d_i are integers and δ_i is the coefficient quantization error of the dependent multipliers.

Since the coefficient quantization errors cause error in the digital filter's response (e.g., impulse response, frequency response, etc.) [2], the choice of σ_i and δ_i is not arbitrary but is determined by certain criteria given in the following.

We note at this point that the choice of δ_i is determined by the magnitude truncation technique which will be presented in Chapter VI. As will be seen from Chapter VI, the δ_i 's are in general smaller than the σ_i 's; in the following development, we assume that the dependent multipliers are realized exactly (i.e., with infinite precision).

From the new set \hat{M} , we can calculate the new sets \hat{R} and \hat{N} , which determine a set \mathcal{B} of deviations from the original values defined as

$$B = \{ \beta_i \mid \beta_i \geq 0 \text{ for } i = 1 \text{ to } n+p \} \quad (2.30)$$

where

$$\beta_i = | r_i - \hat{r}_i | \quad \text{for } i = 1 \text{ to } n$$

$$\beta_{j+n} = | n_j - \hat{n}_j | \quad \text{for } j = 1 \text{ to } p$$

For any particular analog filter design, there is always a certain tolerance imposed upon the component values determined either by various sensitivity analysis methods or just by experience from practical design. In other words, given a maximum tolerance set

$$B_{\max} = \{ \beta_{i \max} \mid \beta_{i \max} \geq 0 \text{ for } i = 1 \text{ to } n+p \} \quad (2.31a)$$

we must have

$$\beta_i \leq \beta_{i \max} \quad \text{for } i = 1 \text{ to } n+p \quad (2.31b)$$

as the condition that the variation of the element values must satisfy to meet the required specifications.

The optimization problem can now be formulated : Given an acceptable deviation set B_{\max} of the original sets R and N , we must calculate a suitable deviation set E_{\max} defined as

$$E_{\max} = \{ \sigma_{i \max} \mid \sigma_{i \max} \geq 0 \text{ for } i = 1 \text{ to } n+p-1 \} \quad (2.32a)$$

in such a way that

$$| m_i - \hat{m}_i | \leq \sigma_{i \max} \Rightarrow \beta_j \leq \beta_{j \max} \quad (2.32b)$$

for $i = 1$ to $n+p-1$

and $j = 1$ to $n+p$

In this thesis, the n_j 's are given by dependent - multiplier

equations; i.e., the n_j 's are chosen as dependent multipliers

$$n_j = f_j(M) \quad \text{for } j = n+1 \text{ to } n+p \quad (2.33)$$

and from Equations (2.23) to (2.25), it can be seen that the r_i 's are explicit functions of the n_j 's and M or simply functions of M . In other word, we can write

$$r_i = g_i(M) \quad \text{for } i = 1 \text{ to } n \quad (2.34)$$

If the functions f_j and g_i are continuous within an $(n+p)$ -dimensional neighborhood

$$\beta_k \max \geq 0, \quad k = 1 \text{ to } n+p \quad (2.35)$$

of M , then the optimization problem stated in (2.32) always has a solution set E_{\max} .

So far, we have assumed that the system is linear. However, in actual implementation, signal truncation and dependent multiplier quantization will affect the performance of the filter. Thus, it is necessary to simulate the hardware realization of the filter on the computer if we want to know its actual performance. The simulation procedure will be discussed in Chapter VI. In the next section, we will investigate the stability of the structures under investigation.

2.5 STABILITY OF THE WAVE STRUCTURES UNDER INVESTIGATION

Besides the coefficient quantization error of \hat{M} and \tilde{H} mentioned in the last section, the result of processing will naturally

lead to values requiring additional bits for their representation. For example, an m -bit data input multiplied by an m -bit multiplier results in a product which is $2m$ bits long. If in a wave digital filter we do not quantize the result of arithmetic operations, the number of bits required will increase indefinitely. Two common methods are used to eliminate the lower order bits resulting from arithmetic operations in such a recursive digital filter : truncation and rounding. Truncation is accomplished by discarding all bits less significant than the least significant bit which is retained and rounding of a number to m bits, when the number is initially specified to more than m bits, is accomplished by choosing the rounded result as the m -bit number closest to the original unrounded quantity.

It is well known that the resulting truncation error or rounding error causes a deadband effect or limit cycle in the filter output [4,5]. A common type of limit cycle is a zero input limit cycle where the output of a digital filter remains periodic and nonzero, after the input has been set to zero.

Another source of error due to the finite word length representation is the overflow error which occurs when a digital filter computes a number that is too large to be represented in the arithmetic used in that filter. This kind of error has also been known to produce overflow oscillations [8,28] .

As we have mentioned in the introduction, it has been pointed out by Claasen et al. [5] that it is possible to design a wave digital filter of arbitrary order, without limit cycles and overflow oscilla-

tions. Using simple arithmetic operation, Fettweis and Meerkötter [16] have been able to guarantee the absence of zero input limit cycles in the wave digital ladder structures for which all port resistances are positive and moreover are pseudopassive (lossless) according to the pseudopower function as originally defined by Fettweis [29].

In the following, we derive a theorem which guarantees the zero input asymptotic stability of the wave structures under investigation.

$$\text{Partitioning } b = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}, a = \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}, S = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$

$$\text{and } G = \begin{bmatrix} G_{11} & 0 \\ 0 & G_{22} \end{bmatrix} \quad \text{according to ports with delay and ports}$$

without delay yields the following from the pseudolosslessness already shown in (2.13) :

$$S_{11}^T G_{11} S_{11} + S_{21}^T G_{22} S_{21} = G_{11} \quad (2.36)$$

From (2.5) we can write the system equations

$$b_1(n) = S_{11} a_1(n) + S_{12} a_2(n) \quad (2.37a)$$

$$b_2(n) = S_{21} a_1(n) + S_{22} a_2(n) \quad (2.37b)$$

The next input $a_1(n+1)$ is given by

$$a_1(n+1) = \Sigma b_1(n) \quad (2.37c)$$

where Σ is a diagonal matrix the elements of which are either 1 or -1 depending on whether the reactive element connected at each port is a capacitance or an inductance, respectively.

Due to the necessary quantization error of the dependent mul-

multipliers and the rounding or truncation error mentioned above, the linear, pseudolossless discrete wave system S (2.37) which contains the multiplier sets M and H cannot be physically realized. A model of the actual, finite-state, nonlinear wave digital filter with the input $a_2(n)$ set to zero is shown in Fig. 2.3, where S represents the nonrealizable (i.e., with finite precision) linear system (2.37) and Q represents the signal quantization nonlinearities.

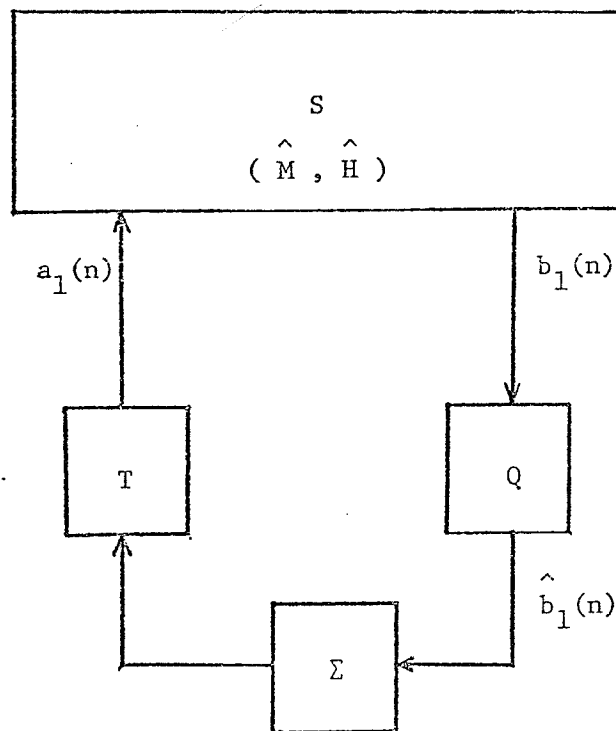


Fig. 2.3 Model of actual nonlinear wave digital filter.

Upon defining the Lyapunov energy function

$$V[a_1(n)] = a_1^T(n) G_{11} a_1(n) \quad (2.38)$$

which is positive definite since G_{11} is positive definite, we can

state the following theorem :

THEOREM : The actual finite-state nonlinear realizable wave digital system of Fig. 2.3 is asymptotically stable under zero input if the output signals are modified in such a way that the Lyapunov function defined in (2.38) is strictly decreasing.

Proof : With the input $a_2(n)$ set to zero, we have from (2.37a) and (2.37b)

$$b_1(n) = S_{11}a_1(n) \quad (2.39a)$$

$$b_2(n) = S_{21}a_1(n) \quad (2.39b)$$

From the definition of the Lyapunov energy function, (2.38) and (2.39a), we can write

$$\begin{aligned} V[b_1(n)] &= b_1^T(n) G_{11} b_1(n) \\ &= a_1^T(n) S_{11}^T G_{11} S_{11} a_1(n) \end{aligned} \quad (2.40)$$

Let us consider the difference

$$V[a_1(n)] - V[b_1(n)] = a_1^T(n) [G_{11} - S_{11}^T G_{11} S_{11}] a_1(n)$$

which can be rewritten by using (2.36) and (2.39b) as

$$V[a_1(n)] - V[b_1(n)] = a_1^T(n) S_{21}^T G_{22} S_{21} a_1(n) \quad (2.41)$$

$$= b_2^T(n) G_{22} b_2(n) \geq 0 \quad (2.42)$$

which is positive semi-definite since G_{22} is positive definite (semi-definite since $b_2(n)$ could be zero even though $a_1(n) \neq 0$).

Thus for the linear part of the system shown in Fig. 2.3

$$V[a_1(n)] \geq V[b_1(n)] \quad (2.43)$$

and for the overall nonlinear system, if the output $b_1(n)$ is modified by Q into an output $\hat{b}_1(n)$ in such a way that

$$|\hat{b}_1(n)| < |b_1(n)| \quad \text{when } b_1(n) \neq 0 \quad (2.44)$$

i.e., if the vectors $b_1(n)$ and $\hat{b}_1(n)$ are given as

$$\begin{aligned} b_1(n) &= [b_{11}(n), b_{12}(n), \dots, b_{1m}(n)] \\ \hat{b}_1(n) &= [\hat{b}_{11}(n), \hat{b}_{12}(n), \dots, \hat{b}_{1m}(n)] \end{aligned}$$

for a wave structure with m delays, then we have

$$|\hat{b}_{1i}(n)| < |b_{1i}(n)| \quad \text{for } i = 1 \text{ to } m, \quad (2.45)$$

then we obtain for the nonlinear system

$$V[a_1(n)] \geq V[b_1(n)] > V[\hat{b}_1(n)] = V[a_1(n+1)] \quad (2.46)$$

That is, the forward difference

$$\Delta V = V[a_1(n+1)] - V[a_1(n)] < 0 \quad (2.47)$$

is negative definite.

Thus given any input $a_1(n)$, (2.38) and (2.47) always hold whenever (2.44) is satisfied. Then, according to Lyapunov's asymptotic stability theorem [30], the nonlinear system is asymptotically stable under zero input. In other words, once the input $a_2(n)$ is set to zero, the output $b_2(n)$ will be zero after a certain finite time interval since the number of states of the system is finite.

2.6 CALCULATION OF ERROR

Let us redraw the model of the k -port wave digital filter shown in Fig. 2.3 without including the delays and without partitioning the ports into ports with delay and ports without delay. We obtain Fig. 2.4

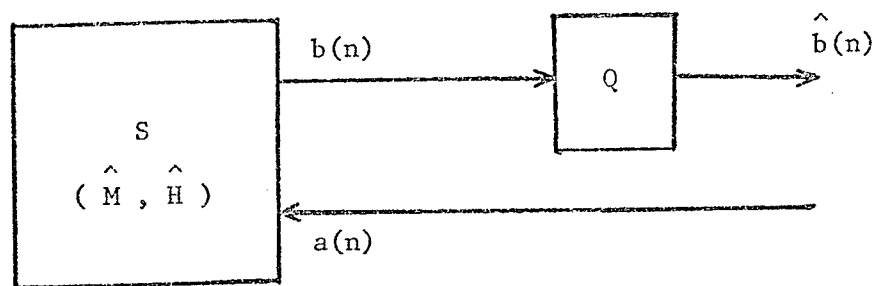


Fig. 2.4 Model of the k -port wave digital filter.

where

$$a(n) = [a_1(n), a_2(n), \dots, a_k(n)]$$

and

$$b(n) = [b_1(n), b_2(n), \dots, b_k(n)]$$

are, respectively, the inputs and outputs of the linear system S .

Due to the quantizer Q , we have the modified outputs

$$\hat{b}(n) = [\hat{b}_1(n), \hat{b}_2(n), \dots, \hat{b}_k(n)]$$

such that the stability condition

$$|\hat{b}_i(n)| < |b_i(n)| \quad (2.48)$$

is satisfied for $i = 1$ to k .

Since the system S is not realizable, the actual implementation of Fig. 2.4 is given by Fig. 2.5

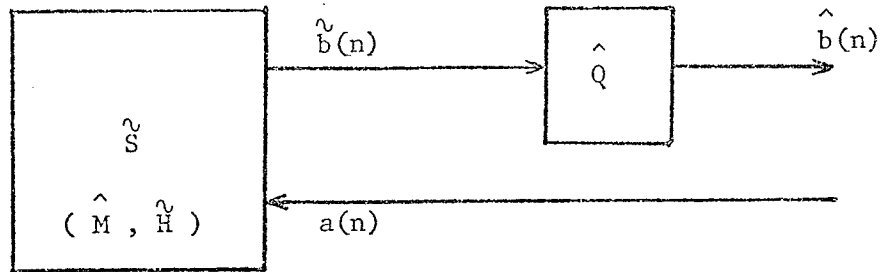


Fig. 2.5 Actual implementation of the wave digital filter of Fig. 2.4.

where \tilde{S} is nonlinear due to signal truncation and not pseudolossless due to the quantization of the dependent multipliers.

Given an input $a(n)$, the output of \tilde{S} is $\tilde{b}(n)$. To implement \hat{Q} which modifies the signal $\tilde{b}(n)$ into $\hat{b}(n)$, we have to calculate the output errors $\epsilon_{b_i}(n)$ defined by

$$\epsilon_{b_i}(n) = b_i(n) - \tilde{b}_i(n) \quad \text{for } i = 1 \text{ to } k \quad (2.49)$$

Once the output errors $\epsilon_{b_i}(n)$ are known, \hat{Q} is implemented as follows:

Corresponding to the input $\tilde{b}_i(n)$, the output

$$\hat{b}_i(n) = \tilde{b}_i(n) + \gamma_i = b_i(n) - \epsilon_{b_i}(n) + \gamma_i \quad (2.50)$$

is obtained by adding to the input $\tilde{b}_i(n)$ a corrective term γ_i which compensates for the output error $\epsilon_{b_i}(n)$ in such a way that

$$|\hat{b}_i(n)| < |b_i(n)| \quad (2.51)$$

In the following section, we assume that the hardware realization uses fixed-point arithmetic with two's complement representation for the signals between building blocks. We will present a few simple rules to calculate the output error $\varepsilon(n)$ resulting from two sources : the first from the signal truncation after a multiplication and the second from the quantization of the dependent multipliers.

RULE II.1 : Signal truncation results in a positive error.

$$x_* = x - \varepsilon_x \quad ; \quad \varepsilon_x > 0 \quad (2.52)$$

where x_* denotes the truncated value of x .

Proof : The proof of Rule II.1 is given by Oppenheim and Schaffer [3].

RULE II.2 : The error of a sum of truncated terms is the sum of the individual truncation errors of each term.

Proof : For the flow diagram shown in Fig. 2.6 we have

$$\begin{aligned} S_* &= x_{1*} + x_{2*} + \dots + x_{n*} \\ &= (x_1 - \varepsilon_{x_1}) + (x_2 - \varepsilon_{x_2}) + \dots + (x_n - \varepsilon_{x_n}) \\ &= (x_1 + x_2 + \dots + x_n) - (\varepsilon_{x_1} + \varepsilon_{x_2} + \dots + \varepsilon_{x_n}) \\ &= S - \varepsilon_S \end{aligned} \quad (2.53)$$

RULE II.3 : The error of a truncated product of a truncated input by an exact multiplier is equal to the sum of two terms : the

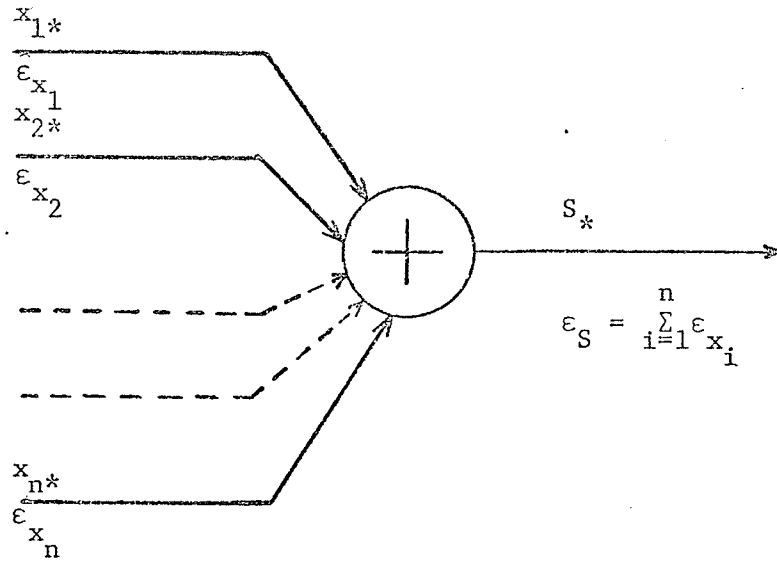


Fig. 2.6 Error of a sum.

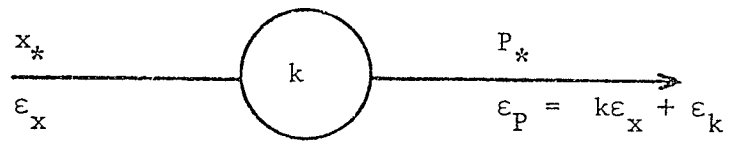


Fig. 2.7 Error of a product.

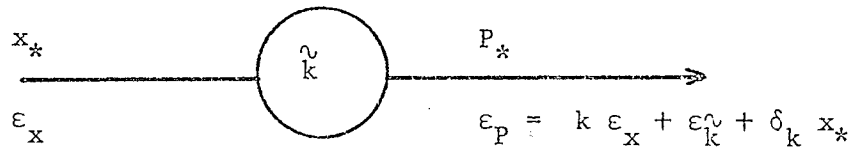


Fig. 2.8 Error of a product by a quantized dependent multiplier.

first one is the product of the truncation error of the input by the multiplier and the second is the truncation error of the product.

Proof : From the flow diagram shown in Fig. 2.7 we have

$$\begin{aligned}
 P_* &= (kx_*)_* = kx_* - \epsilon_k = k(x - \epsilon_x) - \epsilon_k \\
 &= kx - (k\epsilon_x + \epsilon_k) \\
 &= P - \epsilon_P
 \end{aligned} \tag{2.54}$$

where ϵ_k denotes the truncation error of the product.

RULE II.4 : If the multiplier in Rule II.3 has a quantization error

$\delta_k = k - \tilde{k}$, then the error in Rule II.3 is augmented by the product δ_k times the truncated input.

Proof : From the flow diagram shown in Fig. 2.8 we have

$$\begin{aligned}
 P_* &= (\tilde{k}x_*)_* = \tilde{k}x_* - \epsilon_{\tilde{k}} = (k - \delta_k)x_* - \epsilon_{\tilde{k}} \\
 &= kx_* - \delta_k x_* - \epsilon_{\tilde{k}} = k(x - \epsilon_x) - \delta_k x_* - \epsilon_{\tilde{k}} \\
 &= kx - (k\epsilon_x + \epsilon_{\tilde{k}} + \delta_k x_*) \\
 &= P - \epsilon_P
 \end{aligned} \tag{2.55}$$

By applying these simple rules to any wave flow diagram, it is always possible to calculate the output error because any realizable wave flow diagram would consist only of adders and multipliers which are already investigated by these rules. We have seen from (2.50) that the corrective term γ_i must compensate for the output error $\epsilon_{b_i}(n)$.

Consequently, it is necessary to have an explicit expression for the output error. Thus, the appropriate modification scheme of the output is deferred to Chapter VI after we have derived the output error of the structures under investigation. In the following Chapters III, IV and V, we present the necessary formulas for the design of the adaptors for the Brune section, the Darlington C and D sections, and the Twin-T structure.

CHAPTER III

WAVE ADAPTOR FOR THE BRUNE SECTION AND THE DARLINGTON C SECTION

In this chapter, we present the wave adaptor for the Brune section and the Darlington C section. We follow closely the general formulation already given in Chapter II to derive the wave flow diagram, the dependent-multiplier equation and the calculation of output error of the Brune section and the Darlington C section and of their equivalent form.

3.1 WAVE FLOW DIAGRAM OF THE BRUNE SECTION

The Brune section and its reference network interconnections are shown, respectively, in Fig. 3.1 and Fig. 3.2.

The transformer equations are

$$v_5 = n v_3 \quad (3.1)$$

$$i_1 + i_3 = - n i_2 \quad (3.2)$$

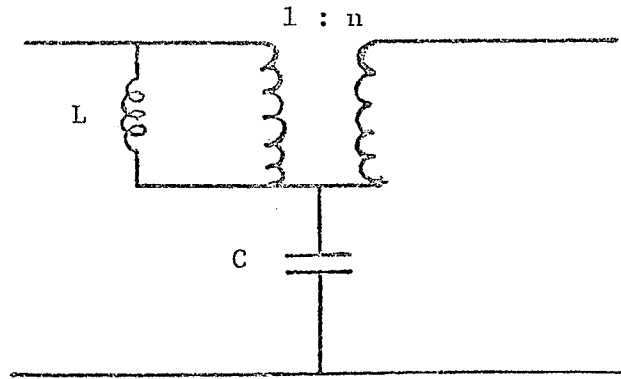


Fig. 3.1 The Brune section.

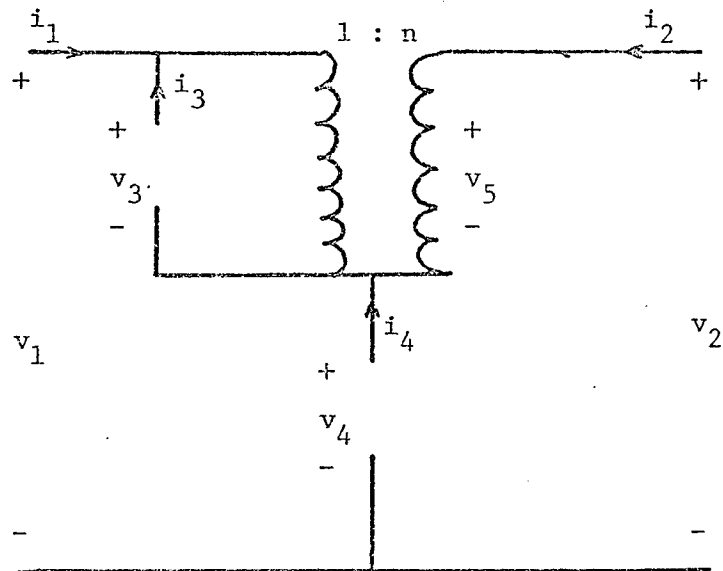


Fig. 3.2 The reference network of the Brune section.

By choosing port 1 and port 2 as "link" ports and by letting the vectors i and v of port currents and voltages be defined as

$$i = [i_1 \ i_2 \ i_3 \ i_4]^T \quad (3.3)$$

$$v = [v_1 \ v_2 \ v_3 \ v_4]^T \quad (3.4)$$

then (2.1) and (2.2) can be written as

$$i = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & -n \\ -1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = B^T i_\ell \quad (3.5)$$

$$v = \begin{bmatrix} 1 & 1 \\ n & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} = Q^T v_t \quad (3.6)$$

From (3.5) and (3.6) we get

$$B_t = \begin{bmatrix} -1 & -1 \\ -n & -1 \end{bmatrix} \quad (3.7)$$

and

$$Q_\ell = \begin{bmatrix} 1 & n \\ 1 & 1 \end{bmatrix} \quad (3.8)$$

Letting

$$G = \left[\begin{array}{cc|cc} G_1 & 0 & 0 & 0 \\ 0 & G_2 & 0 & 0 \\ \hline 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & G_4 \end{array} \right] = \left[\begin{array}{c|c} G_\ell & 0 \\ \hline 0 & G_t \end{array} \right] \quad (3.9)$$

enables us to write

$$QGQ^T = \begin{bmatrix} G_1 + n^2G_2 + G_3 & G_1 + nG_2 \\ G_1 + nG_2 & G_1 + G_2 + G_4 \end{bmatrix} \quad (3.10)$$

hence

$$[QGQ^T]^{-1} = \frac{1}{\Delta} \begin{bmatrix} G_1 + G_2 + G_4 & -G_1 - nG_2 \\ -G_1 - nG_2 & G_1 + n^2G_2 + G_3 \end{bmatrix} \quad (3.11)$$

where

$$\Delta = G_3(G_1 + G_2 + G_4) + G_4(G_1 + n^2G_2) + (1-n)^2G_1G_2 \quad (3.12)$$

and finally

$$\begin{aligned} K &= [QGQ^T]^{-1} Q_\ell G_\ell \\ &= [QGQ^T]^{-1} \begin{bmatrix} 1 & n \\ 1 & 1 \end{bmatrix} \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \\ &= \frac{1}{\Delta} \begin{bmatrix} [(1-n)G_2 + G_4]G_1 & [nG_4 - (1-n)G_1]G_2 \\ [G_3 - n(1-n)G_2]G_1 & [G_3 + (1-n)G_1]G_2 \end{bmatrix} \\ &= \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \end{bmatrix} \end{aligned} \quad (3.13)$$

Upon defining

$$\begin{aligned} \ell_1 &= 2 k_{11} \quad , \quad \ell_2 = 2 k_{12} \\ \ell_3 &= 2 k_{21} \quad , \quad \ell_4 = 2 k_{22} \end{aligned} \tag{3.14}$$

Equation (2.5) can be written explicitly as

$$[b_1 \ b_2 \ b_3 \ b_4]^T = S \cdot [a_1 \ a_2 \ a_3 \ a_4]^T \tag{3.15}$$

where

$$S = \begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & -1 & -1 \\ 0 & 1 & -n & -1 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ \ell_1 \ell_2 & 1 & 0 & 0 \\ \ell_3 \ell_4 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 & -1 & -1 \\ 0 & 1 & -n & -1 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \tag{3.16}$$

and the resulting wave flow diagram is shown in Fig. 3.3.

3.2 DEPENDENT - MULTIPLIER EQUATION

From (3.8) , we can write

$$Q_\ell^T = \begin{bmatrix} 1 & 1 \\ n & 1 \end{bmatrix} \tag{3.17}$$

$$Q_\ell^T K = \begin{bmatrix} k_{11}^+ k_{21} & k_{12}^+ k_{22} \\ nk_{11}^+ k_{21} & nk_{12}^+ k_{22} \end{bmatrix} \tag{3.18}$$

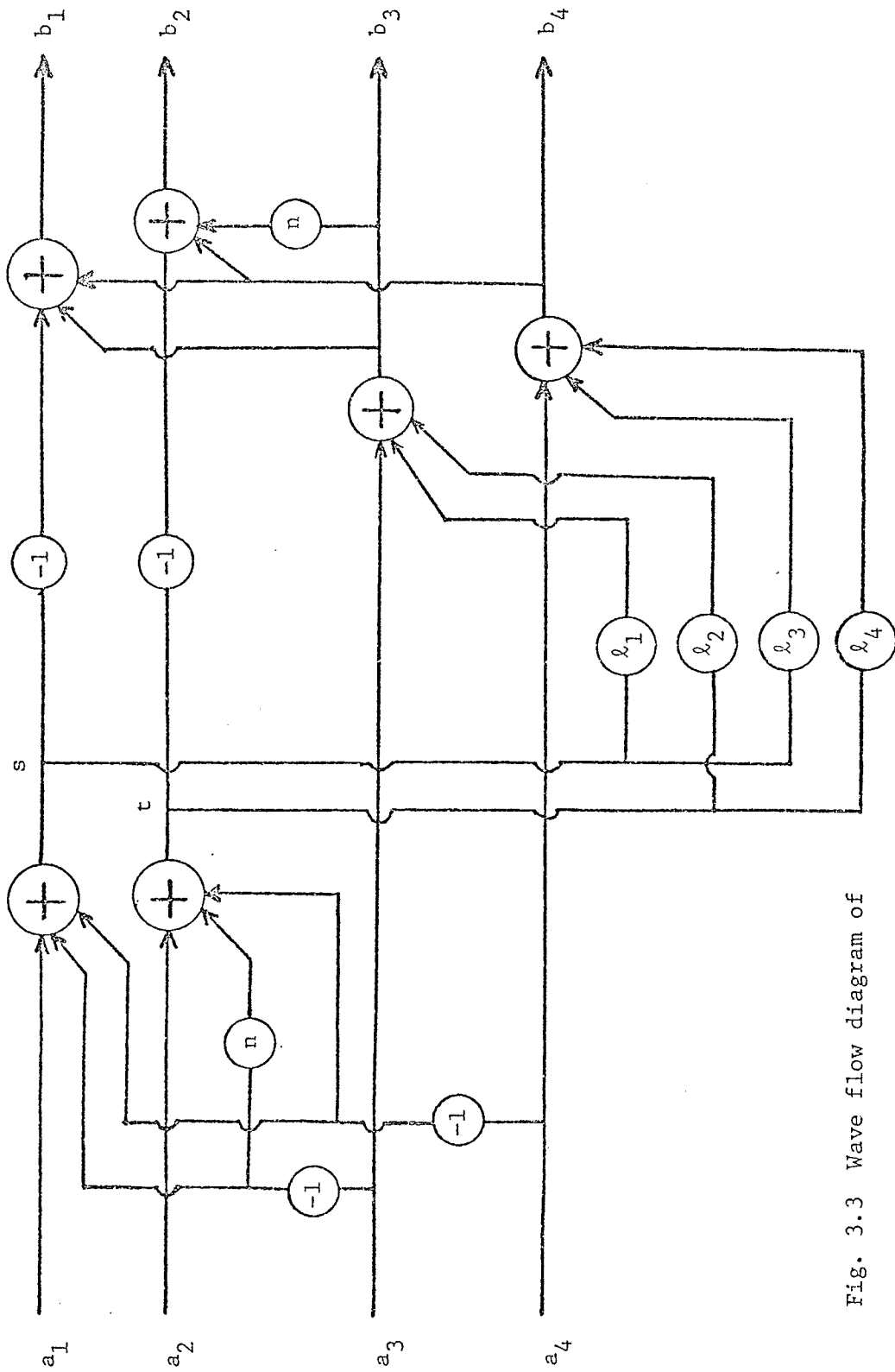


Fig. 3.3 Wave flow diagram of the Brune adaptor.

$$Q_{\ell}^T K Q_{\ell}^T = \begin{bmatrix} k_{11} + nk_{12} + k_{21} + nk_{22} & k_{11} + k_{21} + k_{12} + k_{22} \\ nk_{11} + n^2 k_{12} + k_{21} + nk_{22} & nk_{11} + k_{21} + nk_{12} + k_{22} \end{bmatrix} \quad (3.19)$$

Using (2.23) and (2.24) yields the following

$$\frac{G_2}{G_1} = \frac{k_{12} + k_{22}}{nk_{11} + k_{21}} \quad (3.20)$$

$$\frac{G_3}{G_1} = \frac{1 - k_{11} - k_{21} - nk_{12} - nk_{22}}{k_{11}} \quad (3.21)$$

$$\frac{G_3}{G_2} = \frac{n - nk_{11} - k_{21} - n^2 k_{12} - nk_{22}}{k_{12}} \quad (3.22)$$

$$\frac{G_4}{G_1} = \frac{1 - k_{11} - k_{21} - k_{12} - k_{22}}{k_{21}} \quad (3.23)$$

$$\frac{G_4}{G_2} = \frac{1 - nk_{11} - k_{21} - nk_{12} - k_{22}}{k_{22}} \quad (3.24)$$

Equations (3.20) to (3.24) must be consistent; i.e., we must have

$$\frac{G_2}{G_1} = \frac{\frac{G_4}{G_1}}{\frac{G_4}{G_2}} = \frac{k_{22}}{k_{21}} \frac{1 - (k_{11} + k_{21}) - (k_{12} + k_{22})}{(1 - nk_{12} - k_{22}) - (nk_{11} + k_{21})} \quad (3.25)$$

and

$$\frac{G_2}{G_1} = \frac{\frac{G_3}{G_1}}{\frac{G_3}{G_2}} = \frac{k_{12}}{k_{11}} \frac{1 - (k_{11} + k_{21}) - n(k_{12} + k_{22})}{n(1 - nk_{12} - k_{22}) - (nk_{11} + k_{21})} \quad (3.26)$$

By letting

$$u = k_{11} + k_{21}$$

$$v = k_{12} + k_{22}$$

$$H_1 = \frac{k_{22}}{k_{21}}$$

$$H_2 = \frac{k_{12}}{k_{11}}$$

$$X = nk_{11} + k_{21}$$

$$Y = 1 - nk_{12} - k_{22}$$

Equation (3.25) can be rewritten as

$$\frac{v}{X} = \frac{H_1 (1 - u - v)}{Y - X} \quad (3.27)$$

or

$$vY = X [H_1 (1 - u - v) + v] \quad (3.28)$$

and (3.26) can be rewritten as

$$\frac{v}{X} = \frac{H_2 (1 - u - ny)}{nY - X} \quad (3.29)$$

or

$$nvY = X [H_2 (1 - u - nv) + v] \quad (3.30)$$

Multiplying (3.28) by n gives

$$nvY = nX [H_1 (1 - u - v) + v] \quad (3.31)$$

Subtracting (3.30) from (3.31) yields

$$X [nH_1 (1-u-v) + nv - v - H_2 (1-u) + nH_2 v] = 0 \quad (3.32)$$

Since X is not zero in general, the expression inside the brackets must be equal to zero; i.e.,

$$n [H_1 (1-u-v) + v(1+H_2)] - v - H_2 (1-u) = 0 \quad (3.33)$$

Solving (3.33) for n yields the dependent-multiplier relation

$$n = \frac{H_2 (1 - u) + v}{H_1 (1-u-v) + v(1+H_2)} \quad (3.34)$$

$$= \frac{\frac{k_{12}}{k_{11}} (1 - k_{11} - k_{21}) + (k_{12} + k_{22})}{\frac{k_{22}}{k_{21}} (1 - k_{11} - k_{21} - k_{12} - k_{22}) + (k_{12} + k_{22}) (1 + \frac{k_{12}}{k_{11}})} \quad (3.35)$$

3.3 BRUNE ADAPTOR WITH REFLECTION-FREE PORT

If we choose to make port 1 reflection-free, then according to (2.16) we have

$$q_{11} \cdot 2k_{11} = 1 - q_{21} \cdot 2k_{21} \quad (3.36)$$

Since $q_{11} = q_{21} = 1$, (3.36) can be written as

$$2k_{11} = \ell_1 = 1 - 2k_{21} = 1 - \ell_3 \quad (3.37)$$

Equation (3.37) allows us to eliminate one multiplier in the realization of S . The resulting modified wave flow diagram is shown in Fig. 3.4. We note that b_1 is independent of a_1 from the wave flow diagram as expected.

Making port 1 reflection-free is equivalent to setting the port resistance R_1 equal to the input resistance R_{in} when the other ports are terminated in their respective resistances R_2 , R_3 and R_4 as shown in Fig. 3.5. Hence for practical purpose of design, we calculate R_{in} of the network shown in Fig.3.5 by using simple network analysis

$$R_{in} = \frac{v_1}{i_1} = \frac{R_2 R_3 + R_2 R_4 + R_3 R_4 (1 - n)^2}{R_2 + n^2 R_3 + R_4} \quad (3.38)$$

3.4 CALCULATION OF OUTPUT ERROR

In the following, we calculate the error of each output in the general case where all the multipliers have been approximated; i.e., we have

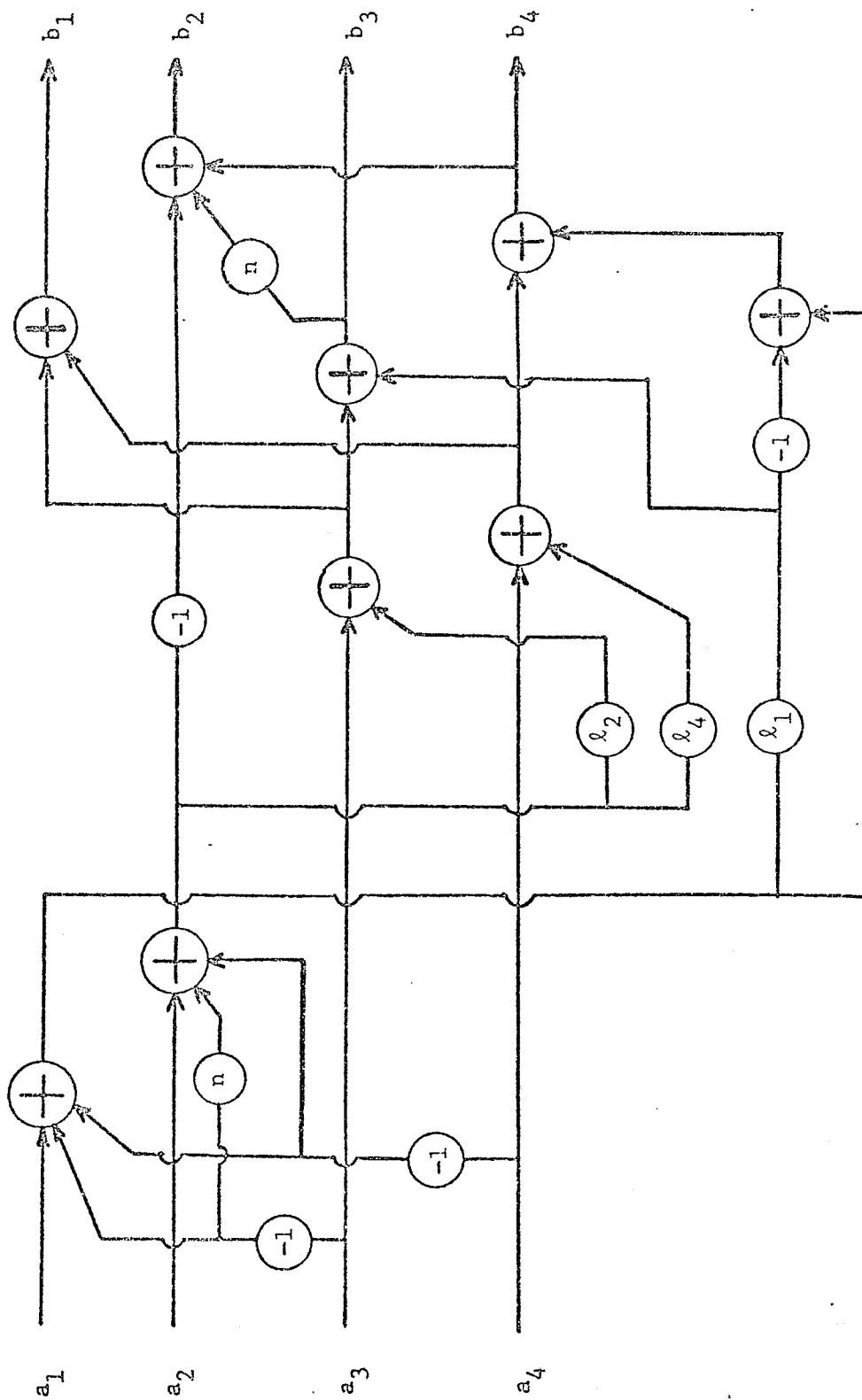


Fig. 3.4 Brune adaptor with port 1 reflection-free.

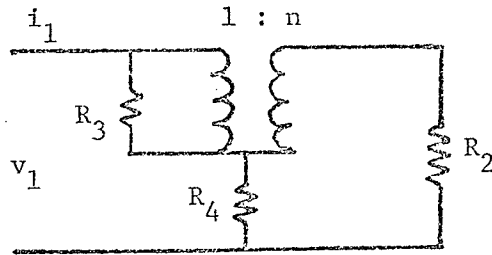


Fig. 3.5 Circuit used to calculate R_{in} .

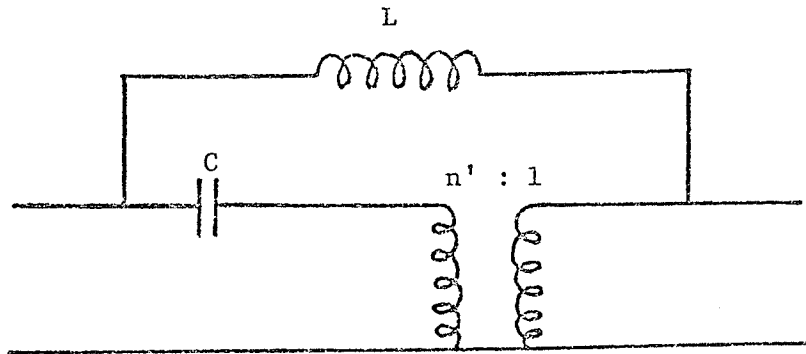


Fig. 3.6 Equivalent form of the Brune section.

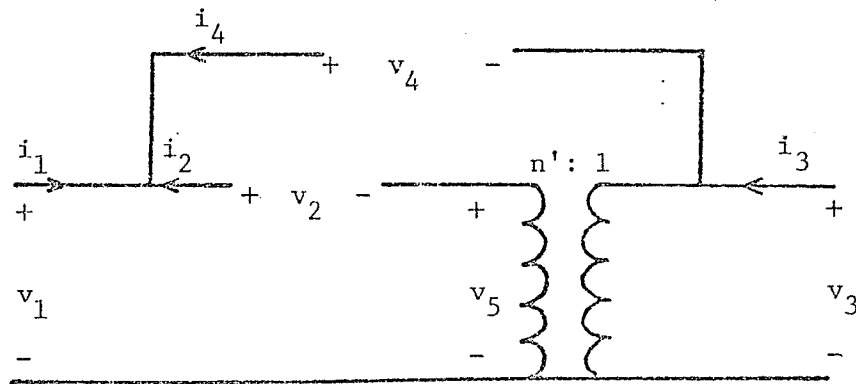


Fig. 3.7 Reference network interconnections of Fig. 3.6.

$$\tilde{n} = n - \delta_n \quad (3.39)$$

$$\tilde{\lambda}_i = \lambda_i - \delta_i \quad \text{for } i = 1 \text{ to } 4 \quad (3.40)$$

(the superscript $\tilde{}$ denotes the actual value realized by hardware)

By defining

$$s = a_1^- a_3^- a_4 \quad (3.41)$$

and

$$t = a_2^- a_4^+ n(- a_3) \quad (3.42)$$

as shown in Fig.3.3 , we have from Rules II.2 and II.4

$$\varepsilon_s = 0 \quad (3.43)$$

$$\varepsilon_t = \delta_n(- a_3) + \varepsilon_n \quad (3.44)$$

since $a_{1*} = a_1$, $a_{2*} = a_2$, $a_{3*} = a_3$, and $a_{4*} = a_4$.

Again by inspection and by using Rules II.2 and II.4

$$\begin{aligned} \varepsilon_{b_3} &= \lambda_1 \varepsilon_s + \delta_1 s_* + \varepsilon_{\lambda_1} + \lambda_2 \varepsilon_t + \delta_2 t_* + \varepsilon_{\lambda_2} \\ &= \varepsilon_{\lambda_1} + \varepsilon_{\lambda_2} + \lambda_2 \varepsilon_t + \delta_1 s_* + \delta_2 t_* \end{aligned} \quad (3.45)$$

$$\begin{aligned} \varepsilon_{b_4} &= \lambda_3 \varepsilon_s + \delta_3 s_* + \varepsilon_{\lambda_3} + \lambda_4 \varepsilon_t + \delta_4 t_* + \varepsilon_{\lambda_4} \\ &= \varepsilon_{\lambda_3} + \varepsilon_{\lambda_4} + \lambda_4 \varepsilon_t + \delta_3 s_* + \delta_4 t_* \end{aligned} \quad (3.46)$$

$$\begin{aligned} \varepsilon_{b_1} &= \varepsilon_{b_3} + \varepsilon_{b_4} \\ &= \varepsilon_{\lambda_1} + \varepsilon_{\lambda_2} + \varepsilon_{\lambda_3} + \varepsilon_{\lambda_4} + (\lambda_2 + \lambda_4) \varepsilon_t + (\delta_1 + \delta_3) s_* + (\delta_2 + \delta_4) t_* \end{aligned} \quad (3.47)$$

$$\begin{aligned}
\varepsilon_{b_2} &= -\varepsilon_t + \varepsilon_{b_4} + n\varepsilon_{b_3} + \delta_n b_{3*} + \varepsilon_n^{\sim} \\
&= \varepsilon_{\lambda_3}^{\gamma} + \varepsilon_{\lambda_4}^{\gamma} + n(\varepsilon_{\lambda_1}^{\gamma} + \varepsilon_{\lambda_2}^{\gamma}) + (\lambda_4 + n\lambda_2 - 1)\varepsilon_t + \varepsilon_n^{\sim} \\
&\quad + (\delta_3 + n\delta_1)s_* + (\delta_4 + n\delta_2)t_* + \delta_n b_{3*} \\
&= \varepsilon_{\lambda_3}^{\gamma} + \varepsilon_{\lambda_4}^{\gamma} + n(\varepsilon_{\lambda_1}^{\gamma} + \varepsilon_{\lambda_2}^{\gamma}) + \varepsilon_n^{\sim} + (\lambda_4 + n\lambda_2 - 1)\varepsilon_n^{\sim} \\
&\quad + (1 - \lambda_4 - n\lambda_2)\delta_n a_3 + (\delta_3 + n\delta_1)s_* + (\delta_4 + n\delta_2)t_* + \delta_n b_{3*}
\end{aligned}
\tag{3.48}$$

In the following section, we will derive the wave digital realization of the equivalent form of the Brune section. It will be seen that all the previous results are still applicable upon making some simple modifications.

3.5 ADAPTOR FOR EQUIVALENT FORM OF THE BRUNE SECTION

An equivalent form of the Brune section and its reference network interconnections are shown, respectively, in Fig.3.6 and Fig.

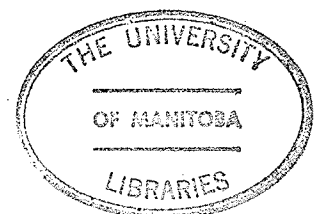
3.7.

The transformer equations are

$$v_5 = n'v_3 \tag{3.49}$$

$$i_3 - i_4 = -n'(-i_2) \tag{3.50}$$

By choosing port 1 and port 2 as "link" ports and by letting the



vectors i and v of port currents and voltages be defined as

$$i = [i_1 \ i_2 \ i_3 \ i_4]^T \quad (3.51)$$

$$v = [v_1 \ v_2 \ v_3 \ v_4]^T \quad (3.52)$$

then (2.1) and (2.2) can be written as

$$i = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & n'-1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = B^T i_\ell \quad (3.53)$$

$$v = \begin{bmatrix} 1 & 1 \\ 1-n' & 1 \\ 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_3 \\ v_4 \end{bmatrix} = Q^T v_t \quad (3.54)$$

By letting $m = 1 - n'$, then (3.53) and (3.54) are similar to Equations (3.5) and (3.6). Thus, all the results obtained so far are applicable to the equivalent form of the Brune section.

3.6 ADAPTOR FOR THE DARLINGTON C - SECTION

The reference network interconnections of the Darlington C section is exactly the one shown in Fig.3.2 or in its equivalent form shown in Fig.3.7. All the results obtained so far are applicable to the

adaptor of the Darlington C-section. The only difference is that the transformer ratio n is negative.

CHAPTER IV

WAVE ADAPTOR FOR THE DARLINGTON D-SECTION

In this chapter, the wave adaptor for the Darlington D-section is derived using all the formulae and results already given in Chapter II. First, the wave flow diagram is presented, then the dependent-multiplier equations and the calculation of the output error are given.

4.1 WAVE FLOW DIAGRAM OF THE DARLINGTON D-SECTION

The Darlington D-section and its reference network interconnections are shown, respectively, in Fig.4.1 and Fig.4.2.

The transformer equations are

$$v_6 = n_4 v_4 \quad (4.1)$$

$$i_1 + i_4 = -n_4 i_2 \quad (4.2)$$

$$v_7 = n_5 v_5 \quad (4.3)$$

$$i_1 + i_5 = -n_5 i_2 \quad (4.4)$$

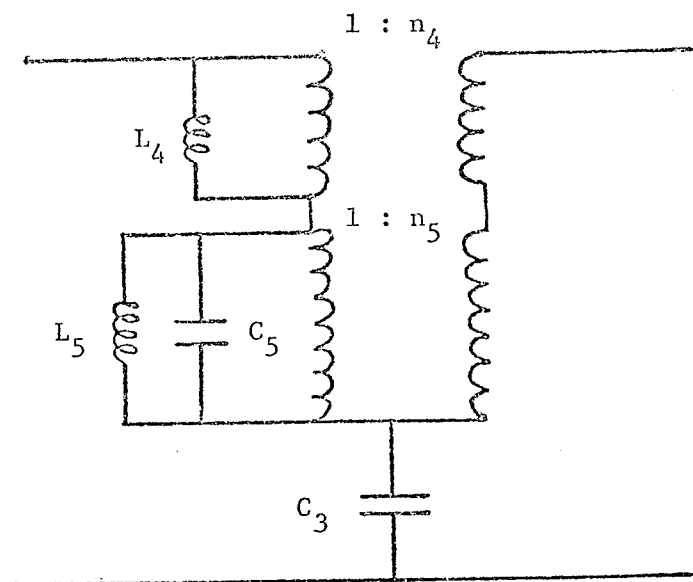


Fig. 4.1 The Darlington D-section.

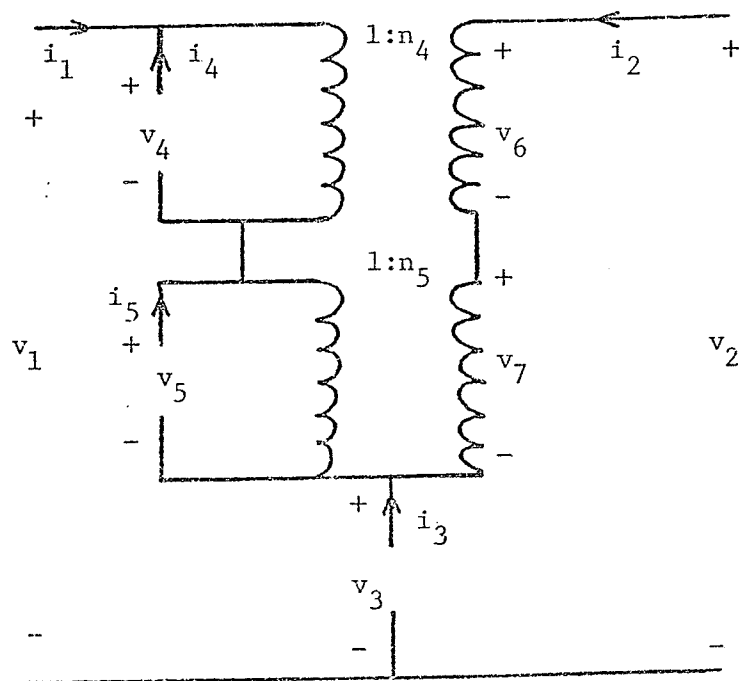


Fig. 4.2 The reference network of Fig. 4.1.

By choosing port 1 and port 2 as "link" ports and by letting the vectors i and v of port currents and voltages be defined as

$$i = [i_1 \ i_2 \ i_3 \ i_4 \ i_5]^T \quad (4.5)$$

$$v = [v_1 \ v_2 \ v_3 \ v_4 \ v_5]^T \quad (4.6)$$

then (2.1) and (2.2) can be written as

$$i = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ -1 & -1 \\ -1 & -n_4 \\ -1 & -n_5 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = B^T i_\ell \quad (4.7)$$

$$v = \begin{bmatrix} 1 & 1 & 1 \\ 1 & n_4 & n_5 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_3 \\ v_4 \\ v_5 \end{bmatrix} = Q^T v_t \quad (4.8)$$

From (4.7) and (4.8) we get

$$B_t = \begin{bmatrix} -1 & -1 & -1 \\ -1 & -n_4 & -n_5 \end{bmatrix} \quad (4.9)$$

and

$$Q_\ell = \begin{bmatrix} 1 & 1 \\ 1 & n_4 \\ 1 & n_5 \end{bmatrix} \quad (4.10)$$

Letting

$$G = \begin{bmatrix} G_1 & 0 & 0 & 0 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_3 & 0 & 0 \\ 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & G_5 \end{bmatrix} = \begin{bmatrix} G_\ell & 0 \\ 0 & G_t \end{bmatrix} \quad (4.11)$$

enables us to write

$$QGQ^T = \begin{bmatrix} G_1+G_2+G_3 & G_1+n_4G_2 & G_1+n_5G_2 \\ G_1+n_4G_2 & G_1+n_4^2G_2+G_4 & G_1+n_4n_5G_2 \\ G_1+n_5G_2 & G_1+n_4n_5G_2 & G_1+n_5^2G_2+G_5 \end{bmatrix} \quad (4.12)$$

hence

$$[QGQ^T]^{-1} = \frac{1}{\Delta} \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix} \quad (4.13)$$

where

$$A_{11} = G_1G_5 + G_1G_4 + G_4G_5 + n_4^2G_2G_5 + n_5^2G_2G_4 + (n_5 - n_4)^2G_1G_2$$

$$A_{12} = (n_5 - n_4)(1 - n_5)G_1G_2 - G_1G_5 - n_4G_2G_5$$

$$A_{13} = (n_4 - n_5)(1 - n_4)G_1G_2 - G_1G_4 - n_5G_2G_4$$

$$A_{21} = A_{12}$$

$$A_{22} = (1 - n_5)^2G_1G_2 + G_1G_5 + G_2G_5 + G_1G_3 + G_3G_5 + n_5^2G_2G_3$$

$$A_{23} = (n_5 - 1)(1 - n_4)G_1G_2 - G_1G_3 - n_4n_5G_2G_3$$

$$A_{31} = A_{13}$$

$$A_{32} = A_{23}$$

$$A_{33} = (1 - n_4)^2G_1G_2 + G_1G_4 + G_2G_4 + G_1G_3 + G_3G_4 + n_4^2G_2G_3$$

$$\Delta = G_1G_4G_5 + G_2G_4G_5 + G_1G_3G_5 + G_1G_3G_4 + G_3G_4G_5 + n_4^2G_2G_3G_5 \\ + n_5^2G_2G_3G_4 + (1 - n_4)^2G_1G_2G_5 + (1 - n_5)^2G_1G_2G_4 + (n_5 - n_4)^2G_1G_2G_3$$

and finally

$$K = [QQQ^T]^{-1}Q_\ell G_\ell \\ = [QQQ^T]^{-1} \begin{bmatrix} 1 & 1 \\ 1 & n_4 \\ 1 & n_5 \end{bmatrix} \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \\ = \frac{1}{\Delta} \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \\ g_{31} & g_{32} \end{bmatrix} = \begin{bmatrix} k_{11} & k_{12} \\ k_{21} & k_{22} \\ k_{31} & k_{32} \end{bmatrix} \quad (4.14)$$

where

$$g_{11} = G_1[G_4G_5 + n_4(n_4 - 1)G_2G_5 + n_5(n_5 - 1)G_2G_4]$$

$$\begin{aligned}
g_{12} &= G_2 [(1-n_4)G_1G_5 + (1-n_5)G_1G_4 + G_4G_5] \\
g_{21} &= G_1 [(1-n_4)G_2G_5 + G_3G_5 + n_5(n_5-n_4)G_2G_3] \\
g_{22} &= G_2 [(n_4-1)G_1G_5 + n_4G_3G_5 + (n_4-n_5)G_1G_3] \\
g_{31} &= G_1 [(1-n_5)G_2G_4 + G_3G_4 + n_4(n_4-n_5)G_2G_3] \\
g_{32} &= G_2 [(n_5-1)G_1G_4 + n_5G_3G_4 + (n_5-n_4)G_1G_3]
\end{aligned}$$

Upon defining

$$\begin{aligned}
l_1 &= 2k_{11} & , & & l_2 &= 2k_{12} \\
l_3 &= 2k_{21} & , & & l_4 &= 2k_{22} \\
l_5 &= 2k_{31} & , & & l_6 &= 2k_{32}
\end{aligned} \tag{4.15}$$

Equation (2.5) can be written explicitly as

$$[b_1 \ b_2 \ b_3 \ b_4 \ b_5]^T = S [a_1 \ a_2 \ a_3 \ a_4 \ a_5]^T \tag{4.16}$$

where

$$S = \begin{bmatrix} -1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & -1 & -1 & -1 \\ 0 & 1 & -1 & -n_4 & -n_5 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ l_1 l_2 & 1 & 0 & 0 & 0 \\ l_3 l_4 & 0 & 1 & 0 & 0 \\ l_5 l_6 & 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 & -1 & -1 & -1 \\ 0 & 1 & -1 & -n_4 & -n_5 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{4.17}$$

and the resulting wave flow diagram is shown in Fig.4.3.

This wave flow diagram requires ten multipliers. Since port 5

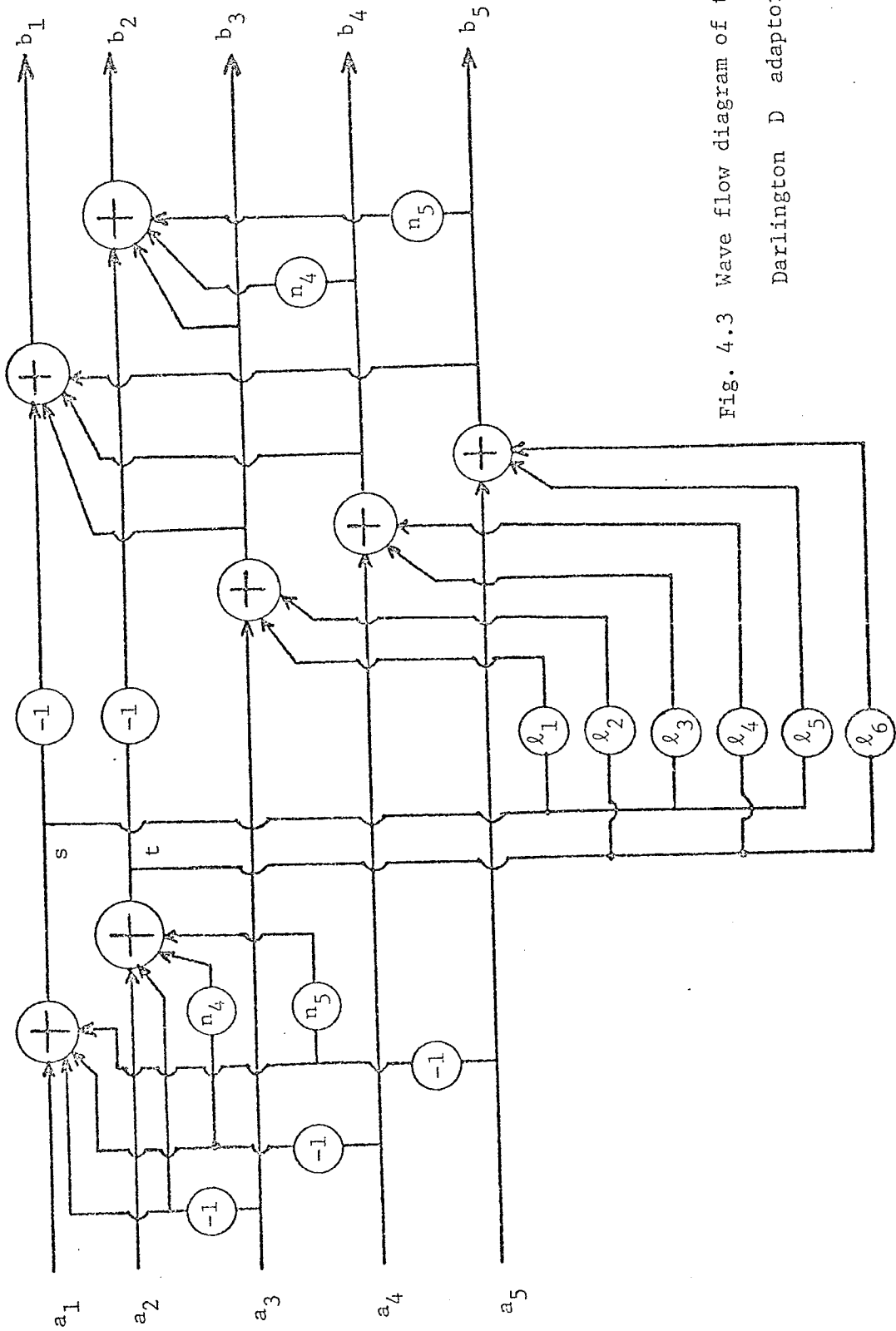


Fig. 4.3 Wave flow diagram of the Darlington D adaptor.

must accommodate an inductance and a capacitance in parallel, a three-port parallel adaptor of Fettweis and Sedlmeyer with a reflection-free port can be directly connected to the wave flow diagram shown in Fig.4.3 to form the complete wave adaptor for the Darlington D-section. This complete wave flow diagram then requires a total number of eleven multipliers, seven of which are independent multipliers by inspection of Fig.4.1.

4.2 DEPENDENT-MULTIPLIER EQUATIONS

From (4.10) , we can write

$$Q_{\ell}^T = \begin{bmatrix} 1 & 1 & 1 \\ 1 & n_4 & n_5 \end{bmatrix} \quad (4.18)$$

$$Q_{\ell}^T K = \begin{bmatrix} k_{11} + k_{21} + k_{31} & k_{12} + k_{22} + k_{32} \\ k_{11} + n_4 k_{21} + n_5 k_{31} & k_{12} + n_4 k_{22} + n_5 k_{32} \end{bmatrix} \quad (4.19)$$

$$Q_{\ell}^T K Q_{\ell}^T = \begin{bmatrix} d_{11} & d_{12} & d_{13} \\ d_{21} & d_{22} & d_{23} \end{bmatrix} \quad (4.20)$$

where

$$d_{11} = k_{11} + k_{21} + k_{31} + k_{12} + k_{22} + k_{32}$$

$$d_{12} = k_{11} + k_{21} + k_{31} + n_4 (k_{12} + k_{22} + k_{32})$$

$$d_{13} = k_{11} + k_{21} + k_{31} + n_5 (k_{12} + k_{22} + k_{32})$$

$$d_{21} = k_{11} + n_4 k_{21} + n_5 k_{31} + k_{12} + n_4 k_{22} + n_5 k_{32}$$

$$d_{22} = k_{11} + n_4 k_{21} + n_5 k_{31} + n_4 (k_{12} + n_4 k_{22} + n_5 k_{32})$$

$$d_{23} = k_{11} + n_4 k_{21} + n_5 k_{31} + n_5 (k_{12} + n_4 k_{22} + n_5 k_{32})$$

Using (2.23) and (2.24) yields the following

$$\frac{G_2}{G_1} = \frac{k_{12} + k_{22} + k_{32}}{k_{11} + n_4 k_{21} + n_5 k_{31}} \quad (4.21)$$

$$\frac{G_3}{G_1} = \frac{1}{k_{11}} [1 - (k_{11} + k_{21} + k_{31}) - (k_{12} + k_{22} + k_{32})] \quad (4.22)$$

$$\frac{G_3}{G_2} = \frac{1}{k_{12}} [1 - k_{12} - n_4 k_{22} - n_5 k_{32} - (k_{11} + n_4 k_{21} + n_5 k_{31})] \quad (4.23)$$

$$\frac{G_4}{G_1} = \frac{1}{k_{21}} [1 - (k_{11} + k_{21} + k_{31}) - n_4 (k_{12} + k_{22} + k_{32})] \quad (4.24)$$

$$\frac{G_4}{G_2} = \frac{1}{k_{22}} [n_4 (1 - k_{12} - n_4 k_{22} - n_5 k_{32}) - (k_{11} + n_4 k_{21} + n_5 k_{31})] \quad (4.25)$$

$$\frac{G_5}{G_1} = \frac{1}{k_{31}} [1 - (k_{11} + k_{21} + k_{31}) - n_5 (k_{12} + k_{22} + k_{32})] \quad (4.26)$$

$$\frac{G_5}{G_2} = \frac{1}{k_{32}} [n_5 (1 - k_{12} - n_4 k_{22} - n_5 k_{32}) - (k_{11} + n_4 k_{21} + n_5 k_{31})] \quad (4.27)$$

By letting

$$u = k_{11} + k_{21} + k_{31}$$

$$v = k_{12} + k_{22} + k_{32}$$

$$X = k_{11} + n_4 k_{21} + n_5 k_{31}$$

$$Y = 1 - k_{12} - n_4 k_{22} - n_5 k_{32}$$

Equations (4.21) to (4.27) can be rewritten as

$$\frac{G_2}{G_1} = \frac{v}{X} \quad (4.28)$$

$$\frac{G_3}{G_1} = \frac{1 - u - v}{k_{11}} \quad (4.29)$$

$$\frac{G_3}{G_2} = \frac{Y - X}{k_{12}} \quad (4.30)$$

$$\frac{G_4}{G_1} = \frac{1 - u - n_4 v}{k_{21}} \quad (4.31)$$

$$\frac{G_4}{G_2} = \frac{n_4 Y - X}{k_{22}} \quad (4.32)$$

$$\frac{G_5}{G_1} = \frac{1 - u - n_5 v}{k_{31}} \quad (4.33)$$

$$\frac{G_5}{G_2} = \frac{n_5 Y - X}{k_{32}} \quad (4.34)$$

Equations (4.28) to (4.34) must be consistent; i.e., we must have

$$\frac{G_2}{G_1} = \frac{\frac{G_3}{G_1}}{\frac{G_3}{G_2}} = \frac{k_{12}}{k_{11}} = \frac{1 - u - v}{Y - X} \quad (4.35)$$

$$\frac{G_2}{G_1} = \frac{\frac{G_4}{G_1}}{\frac{G_4}{G_2}} = \frac{k_{22}}{k_{21}} \frac{1 - u - n_4 v}{n_4 Y - X} \quad (4.36)$$

$$\frac{G_2}{G_1} = \frac{\frac{G_5}{G_1}}{\frac{G_5}{G_2}} = \frac{k_{32}}{k_{31}} \frac{1 - u - n_5 v}{n_5 Y - X} \quad (4.37)$$

Upon letting

$$H_1 = \frac{k_{12}}{k_{11}}$$

$$H_2 = \frac{k_{22}}{k_{21}}$$

$$H_3 = \frac{k_{32}}{k_{31}}$$

we recognize immediately that Equations (4.35) to (4.37) are similar to Equations (3.27) and (3.29).

Thus (4.35) and (4.36) give

$$n_4 = \frac{H_2 (1 - u) + v}{H_1 (1 - u - v) + v(1 + H_2)} \quad (4.38)$$

$$= \frac{\frac{k_{22}}{k_{21}} (1 - k_{11} - k_{21} - k_{31}) + (k_{12} + k_{22} + k_{32})}{\frac{k_{12}}{k_{11}} (1 - k_{11} - k_{21} - k_{31} - k_{12} - k_{22} - k_{32}) + (1 + \frac{k_{22}}{k_{21}}) (k_{12} + k_{22} + k_{32})}$$

and (4.35) and (4.37) yield

$$\begin{aligned}
 n_5 &= \frac{H_3 (1 - u) + v}{H_1 (1 - u - v) + v(1 + H_3)} & (4.39) \\
 &= \frac{\frac{k_{32}}{k_{31}} (1 - k_{11} - k_{21} - k_{31}) + (k_{12} + k_{22} + k_{32})}{\frac{k_{12}}{k_{11}} (1 - k_{11} - k_{21} - k_{31} - k_{12} - k_{22} - k_{32}) + (1 + \frac{k_{32}}{k_{31}}) (k_{12} + k_{22} + k_{32})}
 \end{aligned}$$

4.3 ADAPTOR WITH REFLECTION-FREE PORT

If we choose to make port 1 reflection-free, then according to (2.16) we have

$$q_{11} \cdot 2k_{11} = 1 - q_{21} \cdot 2k_{21} - q_{31} \cdot 2k_{31} \quad (4.40)$$

Since $q_{11} = q_{21} = q_{31} = 1$, (4.40) can be written as

$$2k_{11} = \rho_1 = 1 - 2(k_{21} + k_{31}) = 1 - \rho_3 - \rho_5 \quad (4.41)$$

Equation (4.41) allows us to eliminate one multiplier in the realization of S . The resulting modified wave flow diagram is shown in Fig. 4.4.

Again, for the practical purpose of design, we calculate the input resistance R_{in} of the network shown in Fig. 4.5. The input resistance R_{in} is given by simple network analysis as

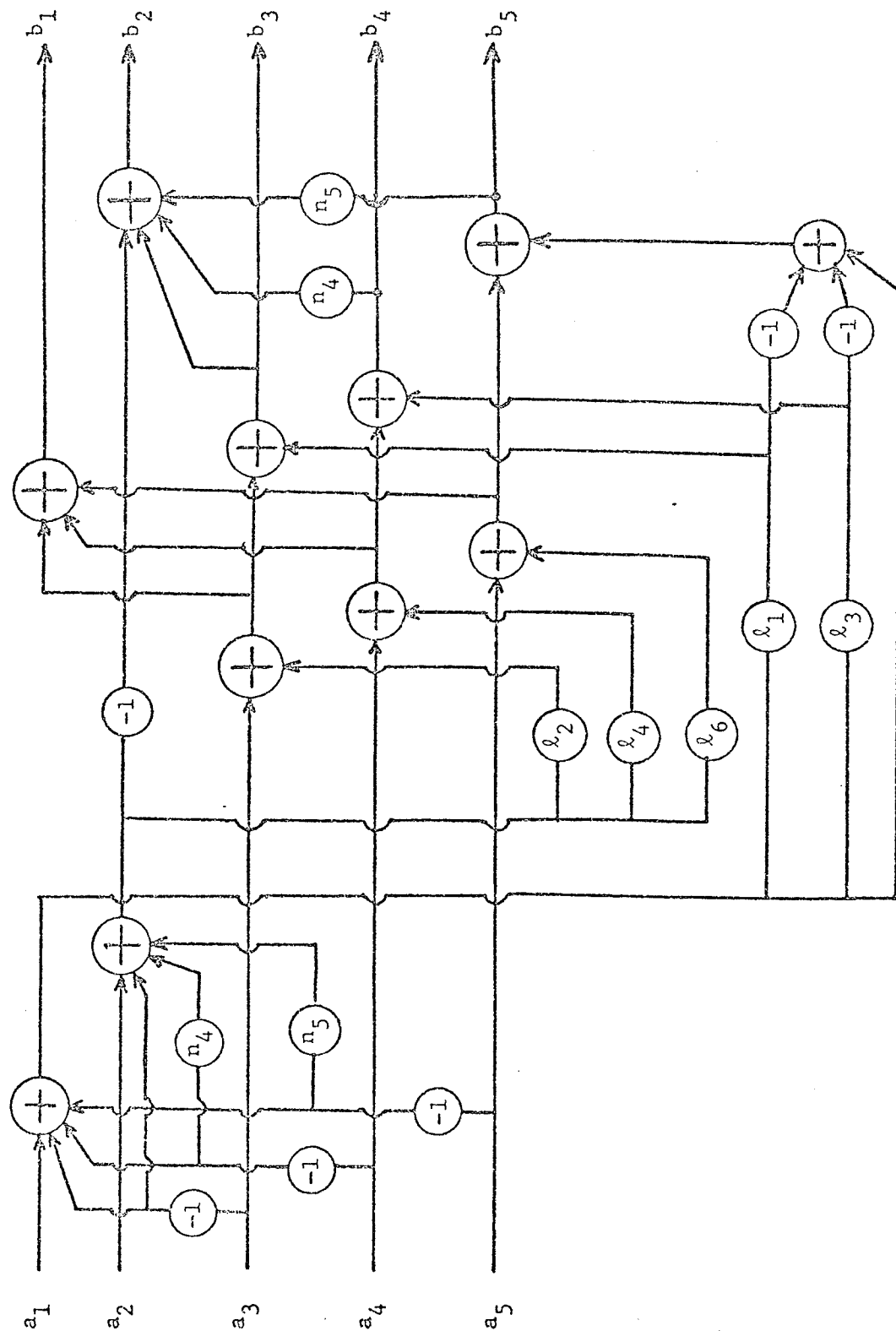


Fig. 4.4 Darlington D adaptor with port 1 reflection-free.

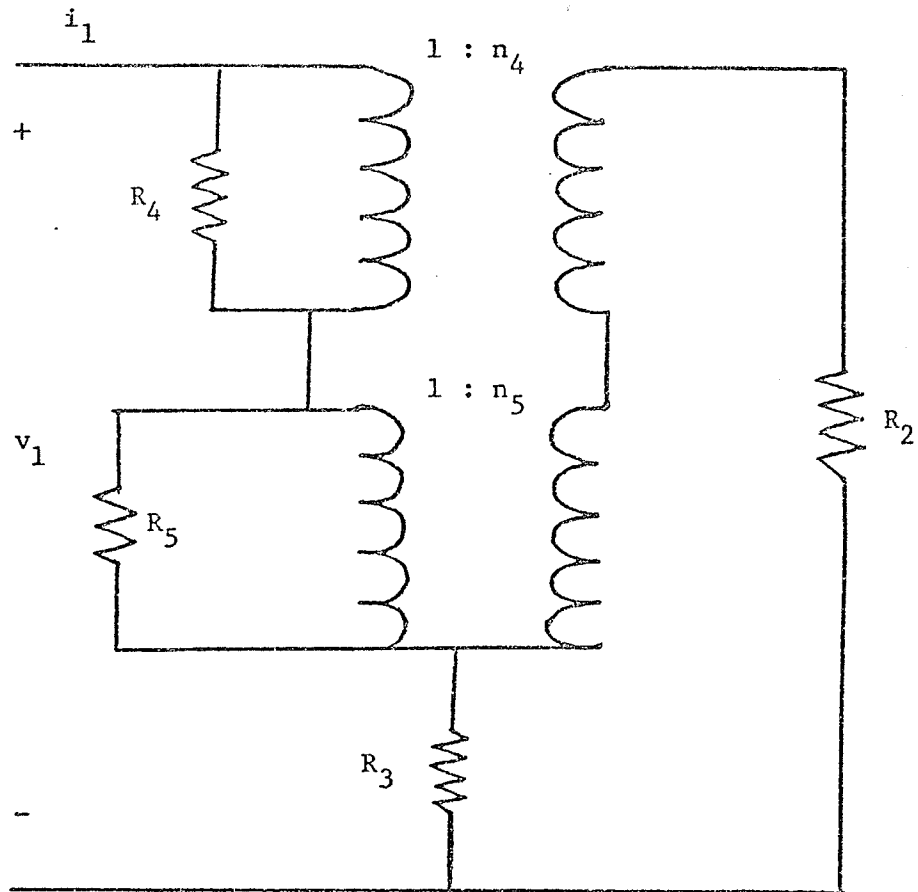


Fig. 4.5 Circuit used to calculate R_{in} .

$$R_{in} = \frac{v_1}{i_1} = \frac{R_2(R_3+R_4+R_5)+R_3R_4(1-n_4)^2+R_3R_5(1-n_5)^2+R_4R_5(n_4-n_5)^2}{R_2+R_3+n_4^2R_4+n_5^2R_5} \quad (4.42)$$

4.4 CALCULATION OF OUTPUT ERROR

In this section, we calculate the error of each output in the general case where all the multipliers have been approximated; i.e.,

$$\tilde{n}_4 = n_4 - \delta_4 \quad (4.43a)$$

$$\tilde{n}_5 = n_5 - \delta_5 \quad (4.43b)$$

$$\tilde{\lambda}_i = \lambda_i - \lambda_i \quad , \quad \text{for } i = 1 \text{ to } 6 \quad (4.43c)$$

By defining

$$s = a_1 - a_3 - a_4 - a_5 \quad (4.44)$$

$$t = a_2 - a_3 + n_4(-a_4) + n_5(-a_5) \quad (4.45)$$

as shown in Fig.4.3 , we have from Rules II.2 and II.4

$$\varepsilon_s = 0 \quad (4.46)$$

$$\varepsilon_t = \delta_4(-a_4) + \delta_5(-a_5) + \varepsilon_{n_4} + \varepsilon_{n_5} \quad (4.47)$$

since $a_{1*} = a_1$, $a_{2*} = a_2$, $a_{3*} = a_3$, $a_{4*} = a_4$ and $a_{5*} = a_5$.

By inspection of the wave flow diagram shown in Fig.4.3 and by using

Rules II.2 and II.4 , we can write

$$\begin{aligned}
 \epsilon_{b_3} &= \ell_1 \epsilon_s + \lambda_1 s_* + \epsilon_{\lambda_1} + \ell_2 \epsilon_t + \lambda_2 t_* + \epsilon_{\lambda_2} \\
 &= \epsilon_{\lambda_1} + \epsilon_{\lambda_2} + \ell_2 \epsilon_t + \lambda_1 s_* + \lambda_2 t_* \quad (4.48)
 \end{aligned}$$

$$\begin{aligned}
 \epsilon_{b_4} &= \ell_3 \epsilon_s + \lambda_3 s_* + \epsilon_{\lambda_3} + \ell_4 \epsilon_t + \lambda_4 t_* + \epsilon_{\lambda_4} \\
 &= \epsilon_{\lambda_3} + \epsilon_{\lambda_4} + \ell_4 \epsilon_t + \lambda_3 s_* + \lambda_4 t_* \quad (4.49)
 \end{aligned}$$

$$\begin{aligned}
 \epsilon_{b_5} &= \ell_5 \epsilon_s + \lambda_5 s_* + \epsilon_{\lambda_5} + \ell_6 \epsilon_t + \lambda_6 t_* + \epsilon_{\lambda_6} \\
 &= \epsilon_{\lambda_5} + \epsilon_{\lambda_6} + \ell_6 \epsilon_t + \lambda_5 s_* + \lambda_6 t_* \quad (4.50)
 \end{aligned}$$

$$\begin{aligned}
 \epsilon_{b_1} &= \epsilon_{b_3} + \epsilon_{b_4} + \epsilon_{b_5} \\
 &= \epsilon_{\lambda_1} + \epsilon_{\lambda_3} + \epsilon_{\lambda_5} + \epsilon_{\lambda_2} + \epsilon_{\lambda_4} + \epsilon_{\lambda_6} + (\ell_2 + \ell_4 + \ell_6) \epsilon_t \\
 &\quad + (\lambda_1 + \lambda_3 + \lambda_5) s_* + (\lambda_2 + \lambda_4 + \lambda_6) t_* \quad (4.51)
 \end{aligned}$$

$$\begin{aligned}
 \epsilon_{b_2} &= -\epsilon_t + \epsilon_{b_3} + n_4 \epsilon_{b_4} + \delta_4 b_{4*} + \epsilon_{n_4} + n_5 \epsilon_{b_5} + \delta_5 b_{5*} + \epsilon_{n_5} \\
 &= \epsilon_{\lambda_1} + \epsilon_{\lambda_2} + n_4 (\epsilon_{\lambda_3} + \epsilon_{\lambda_4}) + n_5 (\epsilon_{\lambda_5} + \epsilon_{\lambda_6}) - \epsilon_t + \epsilon_{n_4} \\
 &\quad + (\ell_2 + n_4 \ell_4 + n_5 \ell_6) \epsilon_t + (\lambda_1 + n_4 \lambda_3 + n_5 \lambda_5) s_* + \epsilon_{n_5} \\
 &\quad + (\lambda_2 + n_4 \lambda_4 + n_5 \lambda_6) t_* + \delta_4 b_{4*} + \delta_5 b_{5*} \quad (4.52)
 \end{aligned}$$

This concludes the derivation of the wave adaptor for the Darlington D-section. In the next chapter, we will derive an adaptor for the Twin-T structure.

CHAPTER V

THE TWIN - T ADAPTOR

In this chapter, the derivation of the wave adaptor of the Twin-T structure does not follow the approach given in Chapters III and IV but it rather follows closely Martens' and Meerkötter's derivation of the Bridge-Tee adaptor [27].

5.1 WAVE FLOW DIAGRAM OF K

The 8-port of interconnections of the Twin-T structure together with the chosen reference directions for the port variables is shown in Fig.5.1.

By inspection, the number of "tree" ports is four. Therefore, if we derive K directly from (2.6), the wave flow diagram of the Twin-T structure would require sixteen multipliers, nine of which are dependent multipliers. It would be cumbersome to determine the necessary dependent-multiplier equations. To avoid this difficulty, we will deri-

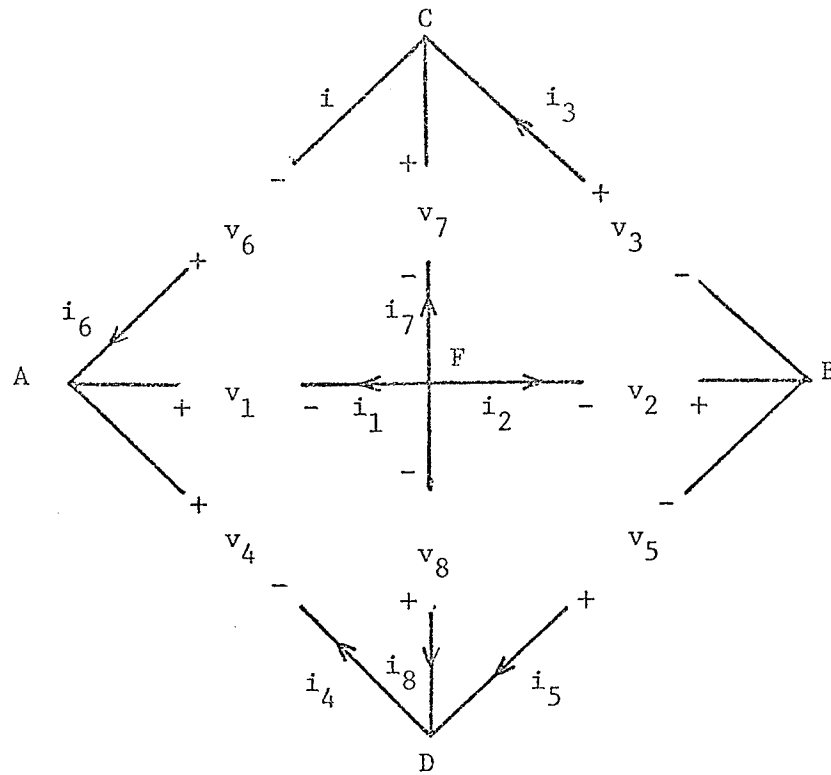


Fig. 5.1 Reference network interconnections of the Twin-T.

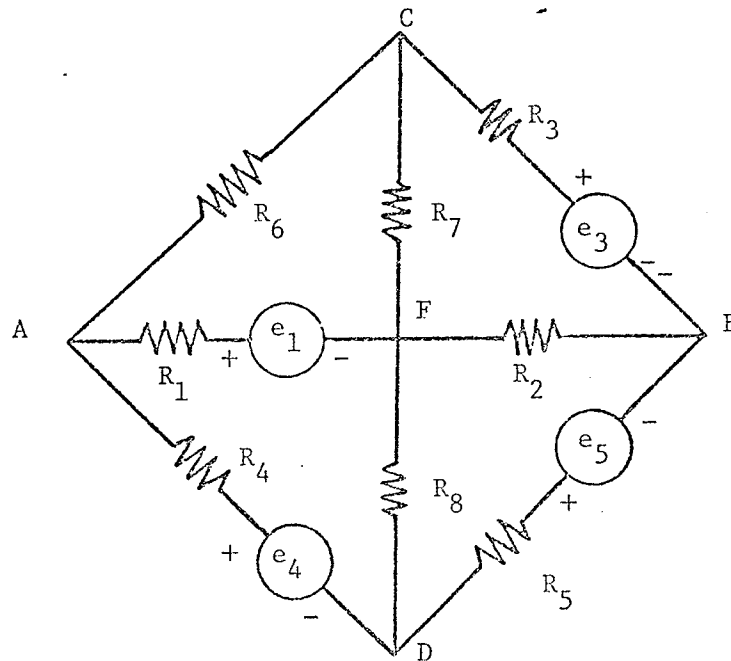


Fig. 5.2 Network used to calculate K.

ve K from its network interpretation as mentioned in Chapter II.

Thus, port resistances are connected to the "tree" ports 2, 6, 7, 8 and port resistances in series with voltage sources are connected to the "link" ports 1, 3, 4, 5 as shown in Fig.5.2.

To obtain a wave flow diagram for K, this network is now analyzed in successive steps to relate the "tree" voltages v_2, v_6, v_7, v_8 to the "link" source voltages e_1, e_3, e_4 and e_5 . Multiplier coefficients are defined as required in the analysis.

The first step is to apply Thevenin's theorem to Fig.5.2 to obtain Fig.5.3.

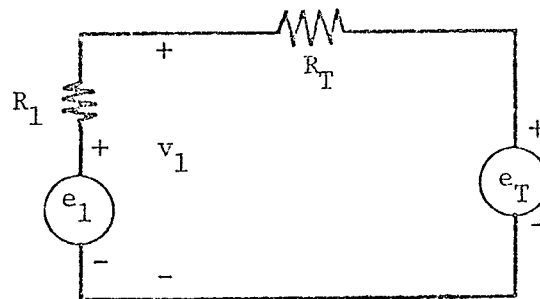


Fig. 5.3 Network obtained from Fig. 5.2 upon applying Thevenin's Theorem.

where R_T is the input impedance and e_T is the open circuit voltage of the network shown in Fig.5.4.

Analysis of this network by superposition gives

$$R_T = \frac{\Delta}{\Delta^*} \quad (5.1)$$

where

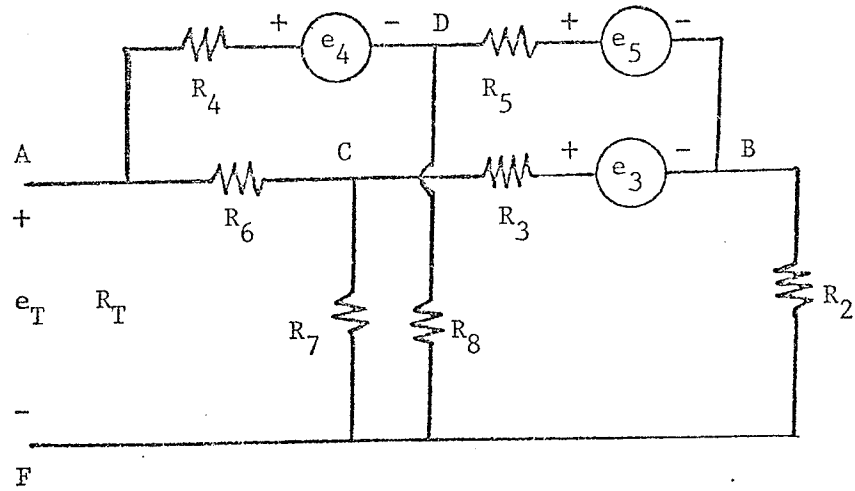


Fig. 5.4 - Network used to calculate R_T .

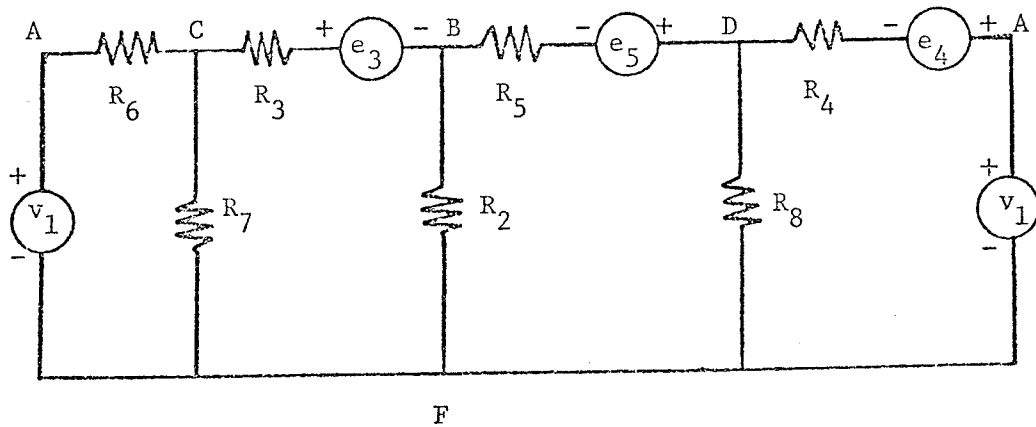


Fig. 5.5 Equivalent network of the network shown in Fig. 5.2.

$$\Delta = R_2(R_6+R_7)[R_5(R_4+R_8)+R_4(R_3+R_8)]+R_4R_7(R_2R_6+R_3R_5) \\ +R_4R_5R_6(R_3+R_7)+R_8(R_2+R_4+R_5)[R_3R_7+R_6(R_3+R_7)] \quad (5.2)$$

$$\Delta^* = R_2[(R_3+R_5)(R_4+R_8)+R_4(R_7+R_8)] + (R_3+R_7)[R_4R_5+R_8(R_4+R_5)] \\ +R_2[(R_3+R_5)(R_6+R_7)+R_6(R_7+R_8)] + (R_5+R_8)[R_6R_7+R_3(R_6+R_7)] \quad (5.3)$$

and

$$e_T = A_3e_3 + A_4e_4 + A_5e_5 \quad (5.4)$$

where

$$A_3 = \frac{1}{\Delta^*} [R_4R_7(R_2+R_5+R_8) + R_8(R_5R_7 - R_2R_6)] \quad (5.5)$$

$$A_4 = \frac{1}{\Delta^*} \{R_2[(R_3+R_5)(R_6+R_7)+R_6(R_7+R_8)] + (R_5+R_8)[R_3(R_6+R_7)+R_6R_7]\} \quad (5.6)$$

$$A_5 = \frac{1}{\Delta^*} [R_6R_8(R_2+R_3+R_7) + R_7(R_3R_8 - R_2R_4)] \quad (5.7)$$

By defining

$$A_1 = \frac{R_1}{R_1 + R_T} \quad (5.8)$$

we can write

$$v_1 = (1 - A_1)e_1 + A_1e_T \\ = (1 - A_1)e_1 + A_1(A_3e_3 + A_4e_4 + A_5e_5) \quad (5.9)$$

and Fig.5.2 can be redrawn as shown in Fig.5.5.

The following step consists of applying Thevenin's theorem to Fig.5.5 to obtain Fig.5.6.

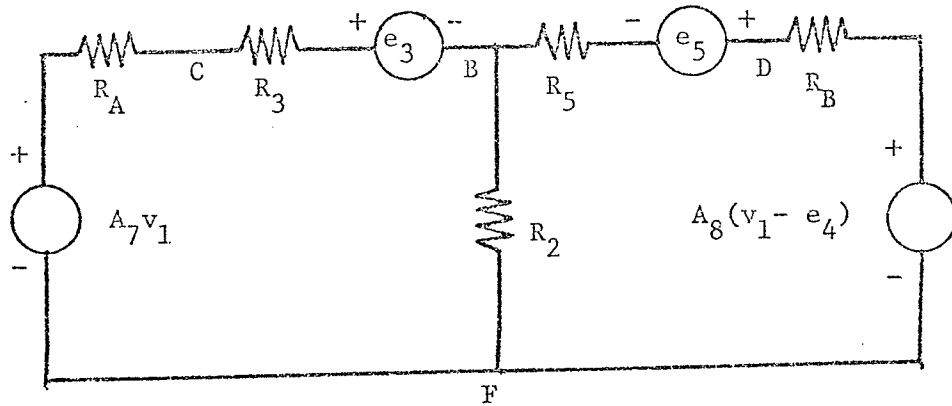


Fig. 5.6 Network obtained from Fig. 5.5 upon applying Thevenin's Theorem.

where

$$R_A = R_6 || R_7 \quad (5.10)$$

$$R_B = R_4 || R_8 \quad (5.11)$$

$$A_7 = \frac{R_7}{R_6 + R_7} \quad (5.12)$$

$$A_8 = \frac{R_8}{R_4 + R_8} \quad (5.13)$$

The notation $R_x || R_y$ denotes the parallel equivalent of R_x and R_y .

Applying Thevenin's Theorem once more to Fig.5.6 yields the following Fig.5.7, from which we have

$$A_2 = \frac{R_2}{R_2 + R_5 + R_B} \quad (5.14)$$

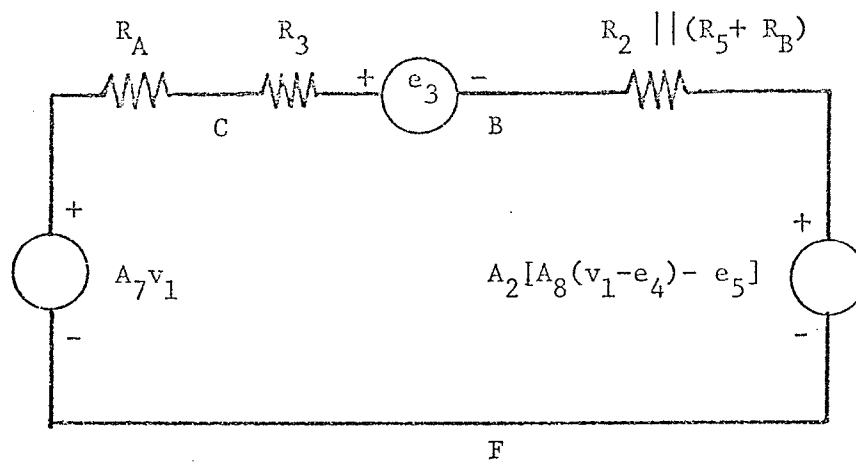


Fig. 5.7 Network obtained from Fig. 5.6 upon applying Thevenin's Theorem.

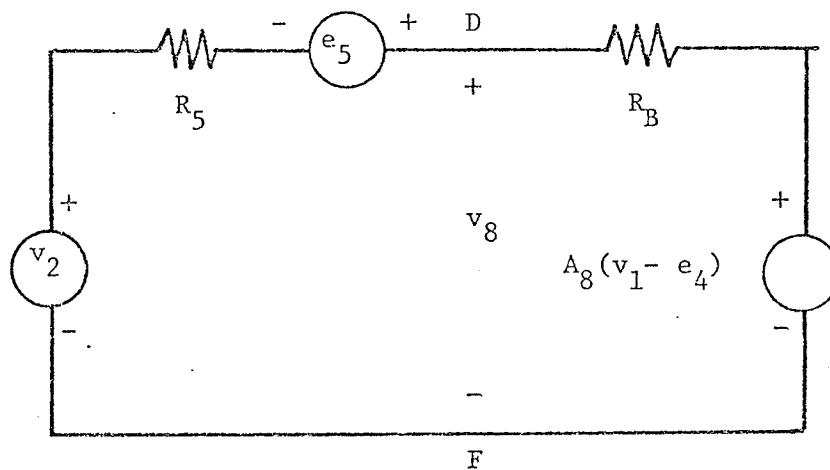


Fig. 5.8 Network used to determine v_8 .

By defining

$$A_6 = \frac{R_A + R_3}{R_A + R_3 + [R_2 \parallel (R_5 + R_B)]} \quad (5.15)$$

$$A_9 = \frac{R_3}{R_A + R_3 + [R_2 \parallel (R_5 + R_B)]} \quad (5.16)$$

we obtain from Fig.5.6 and Fig.5.7

$$v_{CB} = e_3 + A_9 \{ (A_7 v_1 - e_3) - A_2 [A_8 (v_1 - e_4) - e_5] \} \quad (5.17)$$

$$v_2 = (A_7 v_1 - e_3) - A_6 \{ (A_7 v_1 - e_3) - A_2 [A_8 (v_1 - e_4) - e_5] \} \quad (5.18)$$

$$v_7 = v_{CB} + v_2 \quad (5.19)$$

and from Fig.5.5

$$v_6 = v_1 - v_7 \quad (5.20)$$

The remaining v_8 can be determined by examining Fig.5.8. By letting

$$A_{10} = \frac{R_5}{R_5 + R_B} \quad (5.21)$$

we can write

$$v_8 = (v_2 + e_5) - A_{10} [(v_2 + e_5) - A_8 (v_1 - e_4)] \quad (5.22)$$

The equations (5.9), (5.17), (5.18), (5.19), (5.20), and (5.22) determine the sought wave flow diagram for the matrix K which is shown in Fig.5.9.

5.2 WAVE FLOW DIAGRAM OF TWIN-T STRUCTURE

From Fig.5.1, we can write

$$\begin{bmatrix} i_1 \\ i_3 \\ i_4 \\ i_5 \\ i_2 \\ i_6 \\ i_7 \\ i_8 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & 1 \\ -1 & 0 & -1 & 0 \\ -1 & -1 & -1 & 0 \\ 0 & 0 & 1 & -1 \end{bmatrix} \begin{bmatrix} i_1 \\ i_3 \\ i_4 \\ i_5 \end{bmatrix} = B^T i_\ell \quad (5.23)$$

Hence

$$B_t = \begin{bmatrix} 0 & -1 & -1 & 0 \\ 1 & 0 & -1 & 0 \\ 0 & -1 & -1 & 1 \\ 1 & 0 & 0 & -1 \end{bmatrix} \quad (5.24)$$

and the S matrix of the Twin-T structure can be written as

$$S = \begin{bmatrix} U & 0 \\ 0 & U \end{bmatrix} \begin{bmatrix} U & B_t \\ 0 & U \end{bmatrix} \begin{bmatrix} U & 0 \\ 2K & U \end{bmatrix} \begin{bmatrix} U & B_t \\ 0 & U \end{bmatrix} \quad (5.25)$$

The resulting wave flow diagram of the Twin-T adaptor is thus shown in Fig.5.10. The realization requires a total number of ten multipliers.

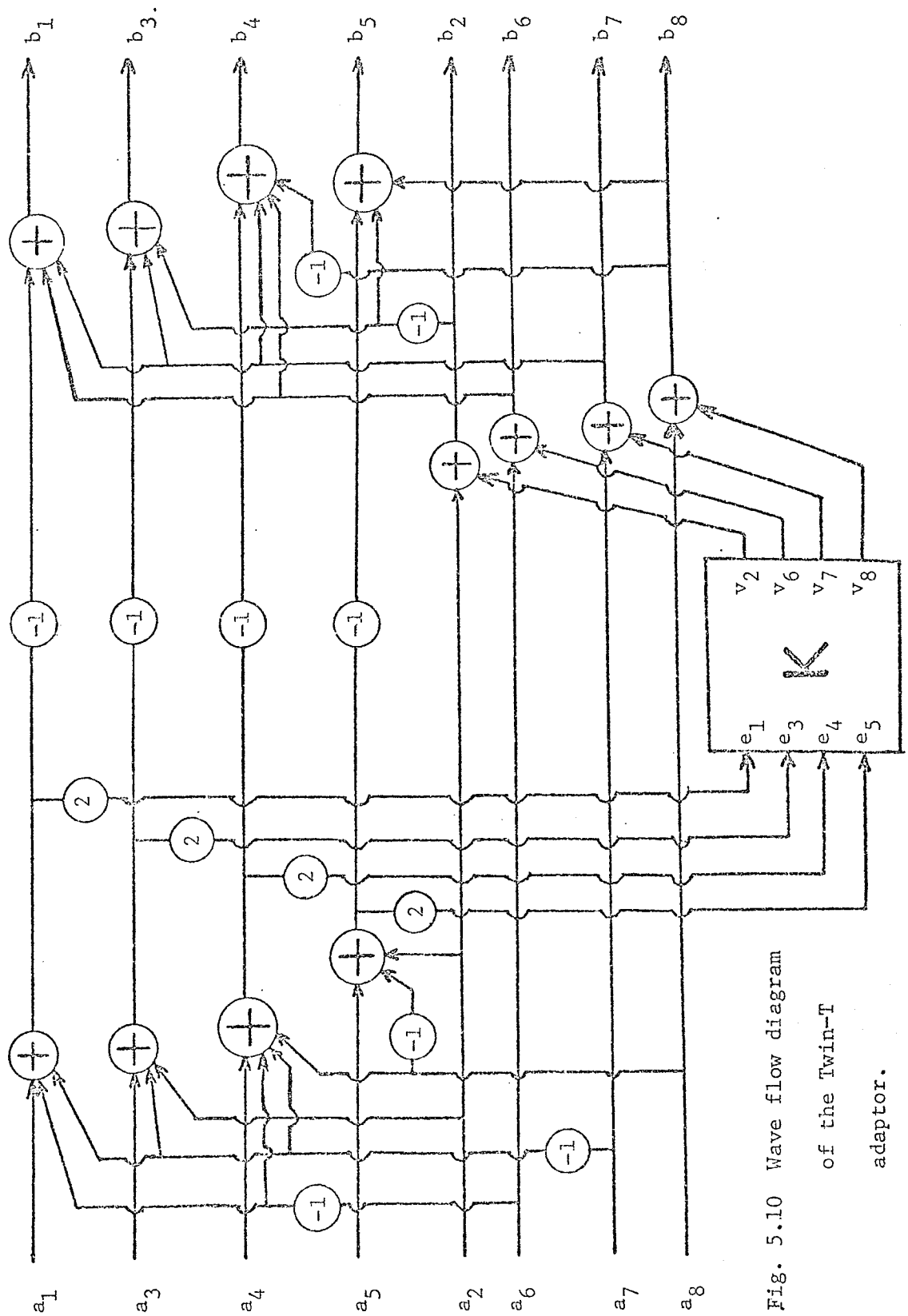


Fig. 5.10 Wave flow diagram of the Twin-T adaptor.

5.3 DEPENDENT-MULTIPLIER EQUATIONS

Since the Twin-T structure has 8 ports, the number of independent multipliers is seven. We can choose arbitrarily $A_1, A_2, A_6, A_7, A_8, A_9, A_{10}$ to be independent multipliers and we will write the dependent-multiplier equations for $A_3, A_4,$ and A_5 by seeking first to determine the port resistances from the independent multipliers.

From (5.12) and (5.13), we can write immediately

$$\frac{R_7}{R_6} = \frac{A_7}{1 - A_7} \quad (5.26)$$

$$\frac{R_8}{R_4} = \frac{A_8}{1 - A_8} \quad (5.27)$$

From (5.14) and (5.21), we can write

$$\frac{1 - A_2}{A_2} = \frac{R_5 + R_B}{R_2} \quad (5.28)$$

$$1 - A_{10} = \frac{R_B}{R_5 + R_B} \quad (5.29)$$

Multiplying (5.28) by (5.29) gives

$$\frac{R_B}{R_2} = \frac{R_4 \parallel R_8}{R_2} = \frac{R_4}{R_2} \frac{R_8}{R_4 + R_8} = \frac{(1 - A_{10})(1 - A_2)}{A_2} \quad (5.30)$$

Since $A_8 = \frac{R_8}{R_4 + R_8}$, we have from (5.30)

$$\frac{R_4}{R_2} = \frac{(1 - A_{10})(1 - A_2)}{A_2 A_8} \quad (5.31)$$

Dividing (5.29) by A_{10} gives

$$\frac{1 - A_{10}}{A_{10}} = \frac{R_B}{R_5} = \frac{R_4}{R_5} \frac{R_8}{R_4 + R_8} = \frac{R_4}{R_5} A_8 \quad (5.32)$$

from which we have

$$\frac{R_5}{R_4} = \frac{A_8 A_{10}}{1 - A_{10}} \quad (5.33)$$

Subtracting (5.16) from (5.15) then dividing the difference by (5.16) yields

$$\frac{A_6 - A_9}{A_9} = \frac{R_A}{R_3} = \frac{R_6 || R_7}{R_3} = \frac{R_6}{R_3} \frac{R_7}{R_6 + R_7} \quad (5.34)$$

Since $A_7 = \frac{R_7}{R_6 + R_7}$, we have

$$\frac{R_6}{R_3} = \frac{A_6 - A_9}{A_7 A_9} \quad (5.35)$$

From (5.15) and (5.16), we can write

$$\frac{1 - A_6}{A_9} = \frac{R_2 || (R_5 + R_B)}{R_3} \quad (5.36)$$

Since

$$R_2 || (R_5 + R_B) = \frac{R_2}{R_2 + R_5 + R_B} \frac{R_5 + R_B}{R_5} R_5 = A_2 \frac{1}{A_{10}} R_5 \quad (5.37)$$

we have from (5.36)

$$\frac{R_5}{R_3} = \frac{A_{10} (1 - A_6)}{A_9 A_2} \quad (5.38)$$

Upon introducing the notation

$$\bar{A}_x = 1 - A_x \quad (5.39)$$

and using Equations (5.26), (5.27), (5.31), (5.33), (5.35) and (5.38),

we can write the following

$$\frac{R_6}{R_3} = \frac{A_6 - A_9}{A_7 A_9} \quad (5.40)$$

$$\frac{R_5}{R_3} = \frac{A_{10} \bar{A}_6}{A_2 A_9} \quad (5.41)$$

$$\frac{R_4}{R_3} = \frac{R_4}{R_5} \frac{R_5}{R_3} = \frac{\bar{A}_6 \bar{A}_{10}}{A_2 A_8 A_9} \quad (5.42)$$

$$\frac{R_7}{R_3} = \frac{R_7}{R_6} \frac{R_6}{R_3} = \frac{A_6 - A_9}{\bar{A}_7 A_9} \quad (5.43)$$

$$\frac{R_2}{R_3} = \frac{R_2}{R_4} \frac{R_4}{R_3} = \frac{\bar{A}_6}{\bar{A}_2 A_9} \quad (5.44)$$

$$\frac{R_8}{R_3} = \frac{R_8}{R_4} \frac{R_4}{R_3} = \frac{\bar{A}_6 \bar{A}_{10}}{A_2 \bar{A}_8 A_9} \quad (5.45)$$

Inspection of (5.3) and (5.6) allows us to write

$$A_4 = \frac{B_1}{\Delta^*} = \frac{B_1}{B_1 + B_2} = \frac{1}{1 + \frac{B_2}{B_1}} \quad (5.46)$$

where

$$B_1 = R_2 [(R_3 + R_5)(R_6 + R_7) + R_6(R_7 + R_8)] + (R_5 + R_8) [R_3(R_6 + R_7) + R_6 R_7] \quad (5.47)$$

$$B_2 = R_2 [(R_3 + R_5)(R_4 + R_8) + R_4(R_7 + R_8)] + (R_3 + R_7) [R_8(R_4 + R_5) + R_4 R_5] \quad (5.48)$$

Instead of using (5.47) and (5.48) to evaluate A_4 , let us define

$$X = \frac{B_1}{R_3^3} \quad (5.49)$$

and

$$Y = \frac{B_2}{R_3^3} \quad (5.50)$$

then by using Equations (5.40) to (5.45), we can write

$$X = \frac{\bar{A}_6(A_6 - A_9) [\bar{A}_2 A_6 (\bar{A}_8 A_{10} + \bar{A}_{10}) + \bar{A}_6 (\bar{A}_8 A_{10} + \bar{A}_7 \bar{A}_{10}) + A_2 A_6 \bar{A}_8]}{\bar{A}_2 A_2 A_9^3 A_7 \bar{A}_7 \bar{A}_8} \quad (5.51)$$

$$Y = \frac{\bar{A}_6^2 \bar{A}_{10} [\bar{A}_7 (A_9 + \bar{A}_6) + (A_6 - A_9) (\bar{A}_2 + A_2 \bar{A}_8)]}{\bar{A}_2 A_2^2 A_9^3 \bar{A}_7 \bar{A}_8 \bar{A}_8} \quad (5.52)$$

and our first dependent-multiplier equation

$$A_4 = \frac{1}{1 + \frac{Y}{X}} \quad (5.53)$$

From (5.46), (5.49), (5.50) we have

$$\Delta^* = B_1 + B_2 = R_3^3 (X + Y) \quad (5.54)$$

From (5.5) and (5.54) we can write

$$A_3 = \frac{\frac{R_4 R_7 (R_2 + R_5 + R_8) + R_8 (R_5 R_7 - R_2 R_6)}{R_3^3}}{X + Y} = \frac{W}{X + Y} \quad (5.55)$$

if we define W as the numerator of A_3 .

Also, from (5.7) and (5.54), we can write

$$A_5 = \frac{\frac{R_6 R_8 (R_2 + R_3 + R_7) + R_7 (R_3 R_8 - R_2 R_4)}{R_3^3}}{X + Y} = \frac{Z}{X + Y} \quad (5.56)$$

if we define Z as the numerator of A_5 .

Again, using Equations (5.40) to (5.45) allows us to write

$$W = \frac{(A_6 - A_9) \bar{A}_6^2 \bar{A}_{10} [A_7 \bar{A}_2 + A_2 (A_7 \bar{A}_8 - \bar{A}_7 A_8)]}{A_9^3 A_2^2 \bar{A}_7 \bar{A}_2 \bar{A}_8 A_7 A_8} \quad (5.57)$$

$$Z = \frac{(A_6 - A_9) \bar{A}_{10} \bar{A}_6 \{A_8 [\bar{A}_6 \bar{A}_7 + A_9 \bar{A}_2 \bar{A}_7 + (A_6 - A_9) \bar{A}_2] + A_7 [A_9 \bar{A}_2 A_8 - \bar{A}_6 \bar{A}_8]\}}{A_2 \bar{A}_2 A_9^3 \bar{A}_7 \bar{A}_8 A_7 A_8} \quad (5.58)$$

Equations (5.55) to (5.58) determine completely the last two dependent-multiplier equations.

From (5.8) , we can write

$$\frac{R_1}{R_T} = \frac{A_1}{1 - A_1} \quad (5.59)$$

Using (5.54) , (5.1) can be rewritten as

$$R_T = \frac{\Delta}{R_3^3 (X+Y)} \quad (5.60)$$

from which we derive

$$\frac{R_T}{R_3} = \frac{\frac{\Delta}{R_3^4}}{X + Y} \quad (5.61)$$

We note that the numerator of (5.61) can be evaluated using Equations (5.40) to (5.45).

Multiplying (5.59) by (5.61) yields finally

$$\frac{R_1}{R_3} = \frac{R_1}{R_T} \frac{R_T}{R_3} = \frac{A_1}{\bar{A}_1} \frac{\frac{\Delta}{R_3^4}}{X + Y} \quad (5.62)$$

5.4 TWIN-T ADAPTOR WITH REFLECTION-FREE PORT

By choosing port 1 as a reflection-free port, we have

$R_1 = R_T$ and from (5.8), we can write

$$A_1 = \frac{R_1}{R_1 + R_T} = \frac{1}{2} \quad (5.63)$$

Absorbing the factors 2 in $2K$ inside the wave flow diagram of K shown in Fig.5.10 would enable us to delete the multiplier A_1 in the wave flow diagram of the Twin-T adaptor. Thus the number of multipliers is reduced to nine.

5.5 CALCULATION OF OUTPUT ERROR

For the Twin-T adaptor, the calculation of output error is more complicated due to the complexity of the wave flow diagram of the matrix K . Let us assume that the dependent multipliers A_3 , A_4 and A_5 are quantized values used in hardware; i.e., we have

$$\hat{A}_i = \tilde{A}_i - \delta_i, \quad \text{for } i = 3, 4, 5$$

From the wave flow diagram of K as shown in Fig.5.9, let us define

$$F = \tilde{A}_3 e_3 + \tilde{A}_4 e_4 + \tilde{A}_5 e_5 \quad (5.64)$$

$$G = e_1 + A_1 F \quad (5.65)$$

$$M = G - e_4 \quad (5.66)$$

$$N = A_8 M - e_5 \quad (5.67)$$

$$H = A_7 G - e_3 \quad (5.68)$$

$$W = H + (-A_2)N = H + A_2' N \quad (5.69)$$

$$P = e_5 + v_2 \quad (5.70)$$

$$Q = P - A_8 M \quad (5.71)$$

We note that all the independent multipliers have no quantization error and that the notation A' denotes $-A$.

These newly defined expressions allow us to write

$$v_2 = H + A_6' W \quad (5.72)$$

$$v_7 = v_2 + e_3 + A_9 W \quad (5.73)$$

$$v_6 = G - v_7 \quad (5.74)$$

$$v_8 = P + A_{10}' Q \quad (5.75)$$

Noting that the inputs $e_1, e_3, e_4,$ and e_5 have no truncation error and applying Rules II.1 to II.4 to Expressions (5.64) to (5.71) yield successively

$$\epsilon_F = \delta_3 e_3 + \delta_4 e_4 + \delta_5 e_5 + \epsilon_{A_3}^\nu + \epsilon_{A_4}^\nu + \epsilon_{A_5}^\nu \quad (5.76)$$

$$\begin{aligned} \epsilon_G &= A_1 \epsilon_F + \epsilon_{A_1} \\ &= A_1 (\delta_3 e_3 + \delta_4 e_4 + \delta_5 e_5) + A_1 (\epsilon_{A_3}^\nu + \epsilon_{A_4}^\nu + \epsilon_{A_5}^\nu) + \epsilon_{A_1} \end{aligned} \quad (5.77)$$

$$\epsilon_M = \epsilon_G \quad (5.78)$$

$$\epsilon_N = A_8 \epsilon_G + \epsilon_{A_8} \quad (5.79)$$

$$\epsilon_H = A_7 \epsilon_G + \epsilon_{A_7} \quad (5.80)$$

$$\epsilon_W = \epsilon_H + A_2' \epsilon_N + \epsilon_{A_2}'$$

$$= (A_7 + A_2' A_8) \epsilon_G + A_2' \epsilon_{A_8} + \epsilon_{A_7} + \epsilon_{A_2'} \quad (5.81)$$

$$\epsilon_P = \epsilon_{V_2} \quad (5.82)$$

$$\epsilon_Q = \epsilon_P - \epsilon_N = \epsilon_P - A_8 \epsilon_G - \epsilon_{A_8} \quad (5.83)$$

Applying the same rules to Expressions (5.72) to (5.75) gives

$$\epsilon_{V_2} = \epsilon_H + A_6' \epsilon_W + \epsilon_{A_6'} \quad (5.84)$$

$$\begin{aligned} \epsilon_{V_7} &= \epsilon_{V_2} + A_9 \epsilon_W + \epsilon_{A_9} \\ &= \epsilon_H + (A_6' + A_9) \epsilon_W + \epsilon_{A_6'} + \epsilon_{A_9} \end{aligned} \quad (5.85)$$

$$\epsilon_{V_6} = \epsilon_G - \epsilon_{V_7} \quad (5.86)$$

$$\begin{aligned} \epsilon_{V_8} &= \epsilon_P + A_{10}' \epsilon_Q + \epsilon_{A_{10}'} \\ &= (1 + A_{10}') (\epsilon_H + A_6' \epsilon_W + \epsilon_{A_6'}) - A_{10}' A_8 \epsilon_G - A_{10}' \epsilon_{A_8} + \epsilon_{A_{10}'} \end{aligned} \quad (5.87)$$

To simplify the expressions of the output errors, we choose to express each output error as a function of ϵ_G . The exact expression of each output error can then be obtained by replacing ϵ_G by its value given by (5.77).

Inspection of the wave flow diagram of the Twin-T adaptor shown in Fig.5.10 yields

$$\begin{aligned} \epsilon_{b_2} &= \epsilon_{V_2} \\ &= [A_7 + A_6' (A_7 + A_2' A_8)] \epsilon_G + A_6' (A_2' \epsilon_{A_8} + \epsilon_{A_2'} + \epsilon_{A_7}) + \epsilon_{A_6'} + \epsilon_{A_7} \end{aligned} \quad (5.88)$$

$$\begin{aligned}
\varepsilon_{b_7} &= \varepsilon_{v_7} \\
&= [A_7 + (A'_6 + A_9)(A_7 + A'_2 A_8)] \varepsilon_G + (A'_6 + A_9)(A'_2 \varepsilon_{A_8} + \varepsilon_{A'_2} + \varepsilon_{A_7}) \\
&\quad + (\varepsilon_{A'_6} + \varepsilon_{A_7} + \varepsilon_{A_9})
\end{aligned} \tag{5.89}$$

$$\begin{aligned}
\varepsilon_{b_6} &= \varepsilon_{v_6} = \varepsilon_G - \varepsilon_{b_7} \\
&= [1 - A_7 - (A'_6 + A_9)(A_7 + A'_2 A_8)] \varepsilon_G - (A'_6 + A_9)(A'_2 \varepsilon_{A_8} + \varepsilon_{A'_2} + \varepsilon_{A_7}) \\
&\quad - (\varepsilon_{A'_6} + \varepsilon_{A_7} + \varepsilon_{A_9})
\end{aligned} \tag{5.90}$$

$$\begin{aligned}
\varepsilon_{b_8} &= \varepsilon_{v_8} \\
&= [(1 + A'_{10})(A_7 + A'_6 A_7 + A'_2 A'_6 A_8) - A'_{10} A_8] \varepsilon_G - A'_{10} \varepsilon_{A_8} + \varepsilon_{A'_{10}} \\
&\quad + (1 + A'_{10}) [A'_6 (A'_2 \varepsilon_{A_8} + \varepsilon_{A'_2} + \varepsilon_{A_7}) + (\varepsilon_{A'_6} + \varepsilon_{A_7})]
\end{aligned} \tag{5.91}$$

$$\varepsilon_{b_1} = \varepsilon_{b_6} + \varepsilon_{b_7} = \varepsilon_G \tag{5.92}$$

$$\begin{aligned}
\varepsilon_{b_3} &= \varepsilon_{v_7} - \varepsilon_{v_2} = A_9 \varepsilon_W + \varepsilon_{A_9} \\
&= A_9 (A_7 + A'_2 A_8) \varepsilon_G + A_9 (\varepsilon_{A_7} + A'_2 \varepsilon_{A_8} + \varepsilon_{A'_2}) + \varepsilon_{A_9}
\end{aligned} \tag{5.93}$$

$$\begin{aligned}
\varepsilon_{b_4} &= \varepsilon_{v_6} + \varepsilon_{v_7} - \varepsilon_{v_8} = \varepsilon_G - \varepsilon_{b_8} \\
&= [1 - (1 + A'_{10})(A_7 + A'_6 A_7 + A'_2 A'_6 A_8) + A'_{10} A_8] \varepsilon_G + A'_{10} \varepsilon_{A_8} - \varepsilon_{A'_{10}} \\
&\quad - (1 + A'_{10}) [A'_6 (\varepsilon_{A_7} + A'_2 \varepsilon_{A_8} + \varepsilon_{A'_2}) + (\varepsilon_{A'_6} + \varepsilon_{A_7})]
\end{aligned} \tag{5.94}$$

and finally

$$\begin{aligned}
\epsilon_{b_5} &= \epsilon_{b_8} - \epsilon_{b_2} \\
&= A_{10}' (A_7 + A_6' A_7 + A_2' A_6' A_8 - A_8) \epsilon_G + \epsilon_{A_{10}'} \\
&\quad + A_{10}' [A_6' (\epsilon_{A_7} + A_2' \epsilon_{A_8} + \epsilon_{A_2}') + (\epsilon_{A_6}' + \epsilon_{A_7} - \epsilon_{A_8})]
\end{aligned}
\tag{5.95}$$

Having calculated the output error of each adaptor and having obtained the necessary wave flow diagrams, we are now able to present in the following chapter a design procedure using the investigated adaptors and a magnitude truncation scheme which guarantees the zero input asymptotic stability of the wave structure.

CHAPTER VI

DESIGN PROCEDURE AND SIGNAL TRUNCATION SCHEME

In this chapter, a general wave cascade design procedure from a reciprocal analog filter is outlined. Then a signal truncation scheme to eliminate granularity and/or overflow oscillations is given. Methods and means of simulation of the hardware realization are presented. Finally, three illustrative examples of wave digital filter using the investigated structures are described.

6.1 DESIGN PROCEDURE

It is well known that any linear, lossless, reciprocal, continuous-time reference filter derived from Darlington cascade synthesis or from Fettweis' transfer matrix factorization method requires for its realization the following reciprocal zero-producing sections :

- 1) the zeroth-order section such as the two-port transformer which can be realized digitally by Fettweis [10] or Nouta [23].

- 2) the first-order section which consists of a reactive element in series or in shunt and which can be realized digitally by Fettweis' n-port adaptors [11].
- 3) the second-order sections such as the Brune section and the Darlington C-section which can be realized digitally by the adaptors given in Chapter III.
- 4) the fourth-order section such as the Darlington D-section which can be realized digitally by the adaptor investigated in Chapter IV.

Since these basic adaptors all have a reflection-free port, a wave cascade synthesis which translates any linear, lossless, continuous-time reference filter derived from Darlington cascade synthesis or from Fettweis' transfer matrix factorization method into a wave digital form is thus possible. Such a general design can be outlined as follows :

- A) From the reference filter, we can identify the cascaded zero-producing sections and draw the equivalent wave cascade realization using the reciprocal zeroth, first, second and fourth-order wave adaptors.
- B) We choose the reflection-free ports for the directly connected adaptors of the equivalent wave cascade realization. This usually leaves one adaptor with no reflection-free port.
- C) For every adaptor
 - c.1) We attribute to each port resistance its corresponding

parameter r_i imposed by the element or source to which the port belongs.

c.2) In case of a reflection-free port, the port resistance must be set equal to the input resistance R_{in} .

c.3) From the sets R and N , we calculate the set of multipliers $T = M + H$.

($+$ denotes set union and R, N, T, M and H are already defined in Chapter II)

c.4) Given a certain tolerance on the sets R and N , we quantize the set M to get a suitable set \hat{M} .

c.5) From the set \hat{M} , we calculate the set \hat{H} using the dependent-multiplier equations.

c.6) From the calculation of the output error and from the choice of the implementation of the magnitude truncation which is necessary to suppress zero input oscillations, and which will be described in the next section, we can decide on the quantization of \hat{H} to get the set \hat{H} .

c.7) Using the sets \hat{M} and \hat{H} , we calculate the new set of port resistances \hat{R} which is to be used in the corresponding adaptors.

c.8) We repeat step c.1 to step c.8 for the next adaptor.

6.2 MAGNITUDE TRUNCATION METHOD

The calculation of the output error of the investigated struc-

tures has produced the following result. If b is the exact output of the associated linear filter of which all the dependent multipliers are realized exactly and all the multiplications are carried out exactly (without any rounding or truncation error), then the actual truncated output b_* of the actual nonlinear filter with its dependent multipliers quantized is

$$b_* = b - \epsilon_b \quad (6.1)$$

where ϵ_b is the calculated total error of the output b .

If N is the total number of multipliers of the realized wave flow diagram of an m -port network, then we can write for each ϵ_b using for example Expression (3.48)

$$\epsilon_b = \sum_{i=1}^N x_i \epsilon_i - \sum_{i=1}^N y_i \epsilon_i + Z_A \quad (6.2)$$

where

x_i and y_i are positive constants determined from the calculation of error in a particular adaptor.

ϵ_i is the truncation error after multiplier i .

Z_A is an amplitude-dependent expression which can be written explicitly as

$$Z_A = \sum_{i=1}^K z_i (\pm A_{i*}) \quad (6.3)$$

where

z_i are positive constants determined from the calculation of error; z_i are functions of the quantization errors of the

dependent multipliers; i.e., $z_i = f_i(\delta_1, \delta_2, \dots, \delta_L)$; (L is the total number of dependent multipliers)

A_{i^*} can be any input a_i , or any output b_i , or any intermediate truncated result inside the filter.

The + or - sign inside the brackets is determined by the numerical calculation of output error.

The Theorem in Chapter II has given a sufficient condition that guarantees the wave adaptor to be asymptotically stable for zero input. Let \hat{b}_i be the modified outputs, then they must satisfy

$$|\hat{b}_i| < |b_i| \quad (6.4)$$

Let us assume that the hardware realization uses fixed-point arithmetic with two's complement representation for the signals between building blocks. If there are m bits d_0, d_1, \dots, d_{m-1} in a number, its value is given by

$$d_0 \Delta d_1 d_2 d_3 \dots d_{m-1} = -d_0 + \sum_{\mu=1}^{m-1} d_{\mu} 2^{-\mu} \quad (6.5)$$

The highest value which this number can take is $1 - 2^{-m+1}$, and the lowest is -1 .

We note that we must provide enough additional front bits inside the filter to avoid discarding any possible overflow which may occur before the output stage. This can be done by inspection of the wave flow diagram. A rule of thumb is to provide n additional bits for an adder of up to 2^n inputs. Thus, we have to provide four additional front bits for the Brune, the Darlington C and D adaptor if

all the multipliers are less than 1, and four additional front bits for the Twin-T adaptor.

Against possible overflow oscillations when the output is either greater than 1 or lower than -1, any number b_0 of the form (6.5) satisfies (6.4) in either case and is thus acceptable. Hence, we can reduce the output b either by a saturation characteristic or by a "modulo 2" characteristic as mentioned by Fettweis and Meerkötter [16], and by Claasen et al. [5].

Against granularity oscillations, we can use the following scheme. Let us define

$$S_p = \text{an upper bound of } \sum_{i=1}^N x_i \epsilon_i = \left(\sum_{i=1}^N x_i \epsilon_i \right)_{\max} \quad (6.6)$$

$$S_n = \text{an upper bound of } \sum_{i=1}^N y_i \epsilon_i = \left(\sum_{i=1}^N y_i \epsilon_i \right)_{\max} \quad (6.7)$$

These bounds are easily found by letting, for example, $\epsilon_i = 2^{-m+1}$. For each z_i of (6.3), we can find an upper bound \bar{z}_i which is given by the quantization characteristic shown in Fig. 6.1 where $q = 2^{-m+1}$.

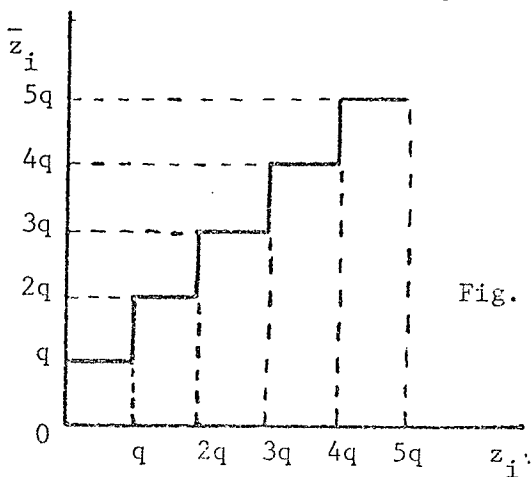


Fig. 6.1 Quantization characteristic for z_i .

To obtain the corrected outputs \hat{b}_i from the actual output b_{i*} , the following logic flow diagram is given in Fig.6.2.

Care should be taken when the magnitude of b_{i*} is less than one of the upper bounds. To avoid error in that case, the output is simply set to zero whenever there is a change of sign after each correction as shown in Fig.6.2.

Since the \bar{z}_i 's are equal to a power of 2, the product $\bar{z}_i (\pm A_{i*})$ is simply obtained by retaining some of the most significant bits of A_{i*} . Therefore, no extra multiplier is required in the realization of the logic flow diagram of Fig.6.2. For example, a possible hardware realization of the logic flow diagram of Fig.6.2 with $K = 2$ is shown in Fig.6.3. We note that there are K iterative cells. Each iterative cell contains two exclusive-or gates and one adder. The "add enable" input of the adder (1) is controlled by the 0th bit of the output b_{i*} which adds the preset ($-S_n$) or (S_p) to b_{i*} . The exclusive-or gate (1) detects the change of sign and clears the output register. The quantities $\pm \bar{z}_i A_{i*}$ need not be stored since they can be wired directly from the A_{i*} . The output of the exclusive-or gate (2) will enable the adder (2) to add $\pm \bar{z}_i A_{i*}$ or 0 to the input of the adder (2). Again, the output of the exclusive-or gate (3) will detect the change of sign and will set the output register to zero. The operation of the next iterative cell is identical to the first one.

Since the available range of the hardware is $[-1, 1]$, we have $|A_{i*}| < 1$ for $i = 1$ to K . Thus, it is possible to find

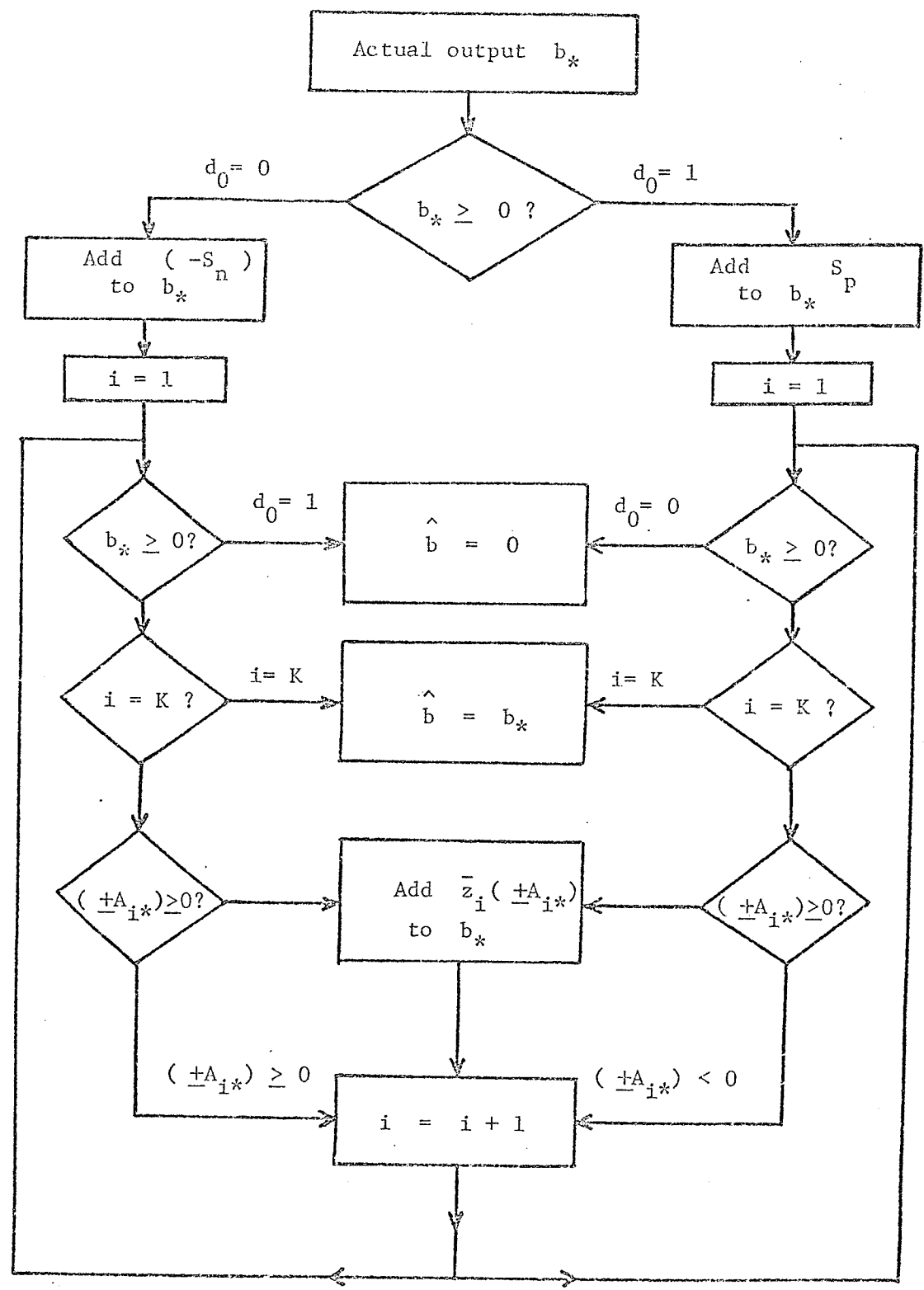


Fig. 6.2 Logic flow diagram used to modify any output b_* to satisfy the asymptotic stability condition.

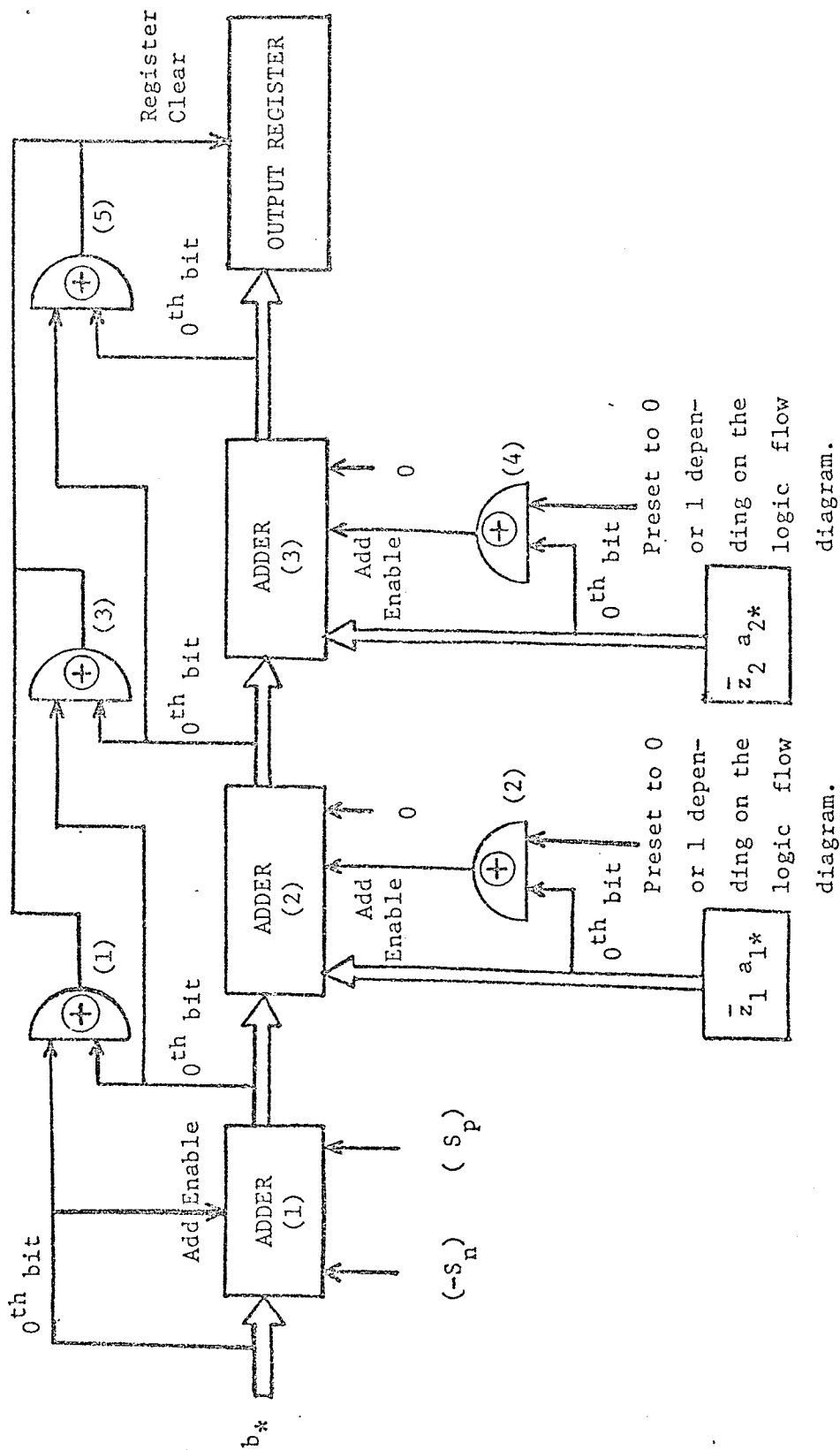


Fig. 6.3 Possible hardware realization of the logic flow diagram shown in Fig. 6.2 with $K = 2$.

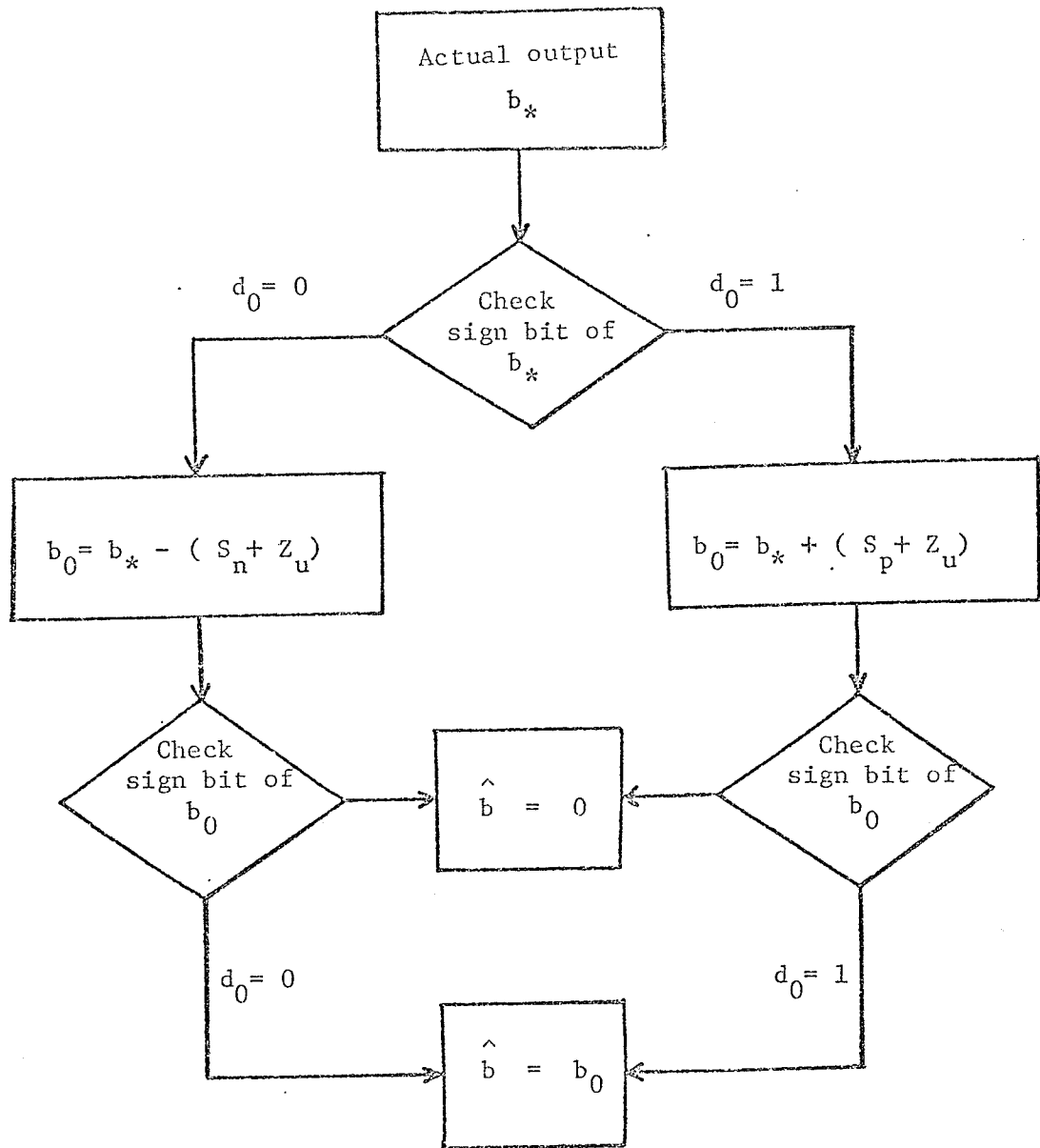


Fig. 6.4 Alternate logic flow diagram for magnitude truncation.

an upper bound of Z_A as

$$Z_u = \left(\sum_{i=1}^K z_i |A_{i*}| \right)_{\max} = \sum_{i=1}^K z_i \quad (6.8)$$

An alternate way to modify the outputs b_* to satisfy (6.4) is now given by the logic flow diagram shown in Fig.6.4.

A possible hardware realization of this logic flow diagram is shown in Fig.6.5

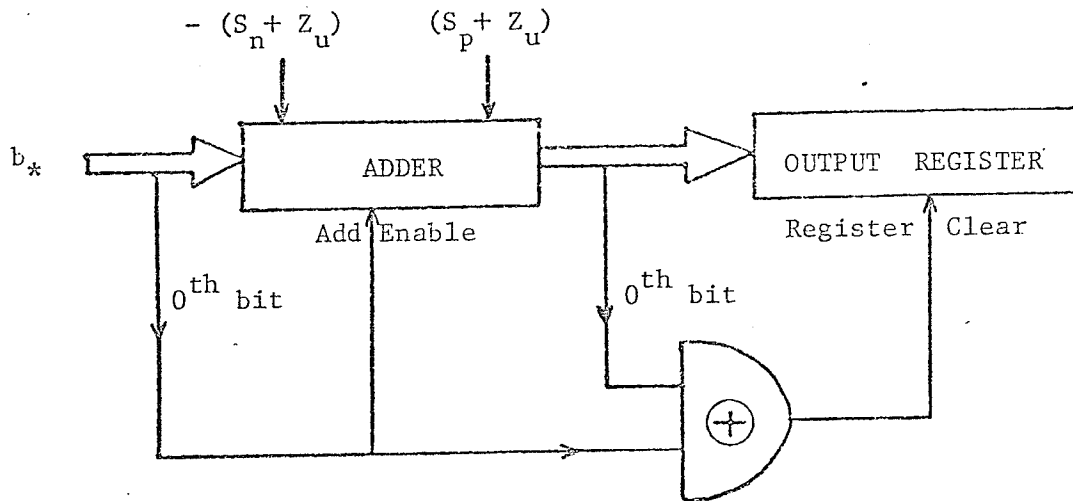


Fig. 6.5 Possible hardware realization of the logic flow diagram shown in Fig. 6.4.

where the 0th bit (the sign bit d_0) of b_* will enable the adder to add $-(S_n + Z_u)$ or $(S_p + Z_u)$ to b_* and the output register is cleared if the output of the exclusive-or gate is 1; i.e., if there is a change of sign.

The hardware realization of such a logic diagram is much sim-

pler than the previous one since there are no iterative cells. However, to avoid large error, Z_u must be comparable in magnitude to S_p and S_n , hence a longer word length representation for the dependent multipliers is necessary since the z_i 's depend on the quantization error δ_i 's. Thus, the choice of δ_i is determined by the magnitude truncation method used to eliminate parasitic oscillations.

6.3 SIMULATION

Having calculated the sets of multipliers \hat{M} and \hat{H} , we simulate the filter and obtain the impulse response of the wave digital filter. A PDP 11/40 mini-computer has been used for the task. It is a 16-bit general purpose computer using two's complement arithmetic with 8K of core memory. The programming languages used are

- a) BASIC : By using BASIC, all arithmetic operations are performed in floating-point with great accuracy thus there is almost no truncation error.
- b) ASSEMBLER : By using ASSEMBLER, all the arithmetic operations of the hardware which uses fixed-point arithmetic with two's complement representation are simulated in software. Magnitude truncation of every output signal according to (6.4) is implemented.

From the calculated impulse response using either BASIC or ASSEMBLER, it is possible to determine the frequency response of the simulated filter by using an available subroutine language called SPARTA which computes the FFT of the impulse response and yields both the magnitude and phase response of the filter. A graphics terminal which is part of the PDP 11/40 system is used to display those responses.

In the following section, we present three illustrative examples of filters using the Brune section, the Darlington D-section and the Twin-T section.

6.4 ILLUSTRATIVE EXAMPLES

6.4.1 First Example : Fifth-order elliptic low-pass filter.

The data of a fifth order elliptic low-pass filter designated as CC 05 20 36 is given by Zverev [31]. Its frequency response is given by Fig.6.6 and its circuit is given by Fig.6.7, where

$$\begin{aligned} R_1 &= 1 \Omega & , C_1 &= 1.21244 \text{ F} & , C_2 &= 0.11019 \text{ F} \\ L_2 &= 1.23669 \text{ H} & , C_3 &= 1.85307 \text{ F} & , C_4 &= 0.30614 \text{ F} \\ L_4 &= 1.04011 \text{ H} & , C_5 &= 1.05244 \text{ F} & , R_5 &= 1 \Omega \end{aligned}$$

Let us consider the circuit shown in Fig.6.8 . First, we de-

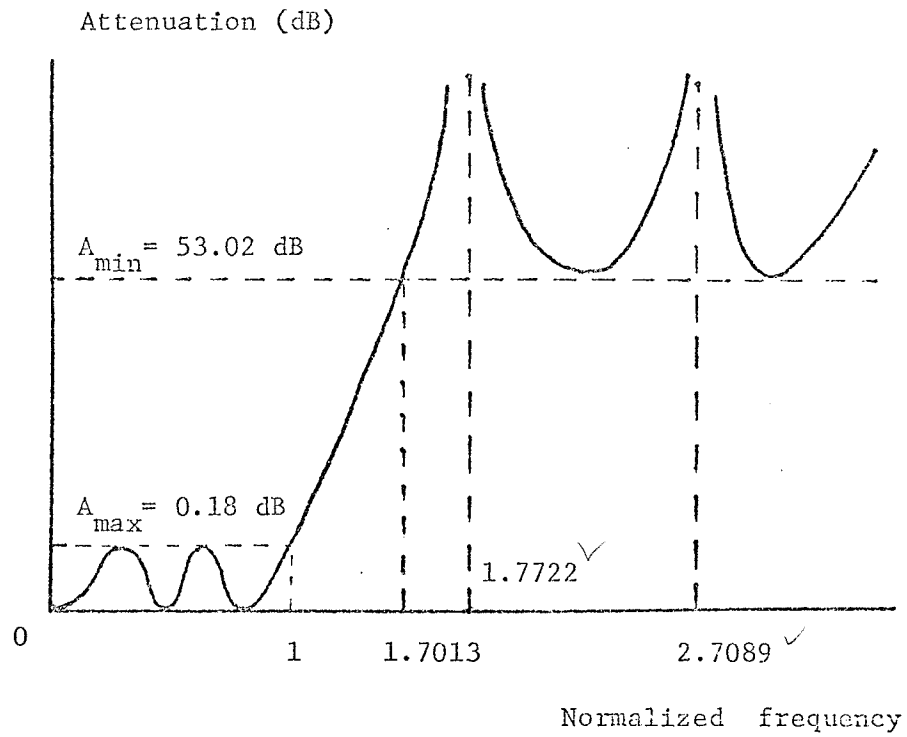


Fig. 6.6 Attenuation characteristic of the reference filter.

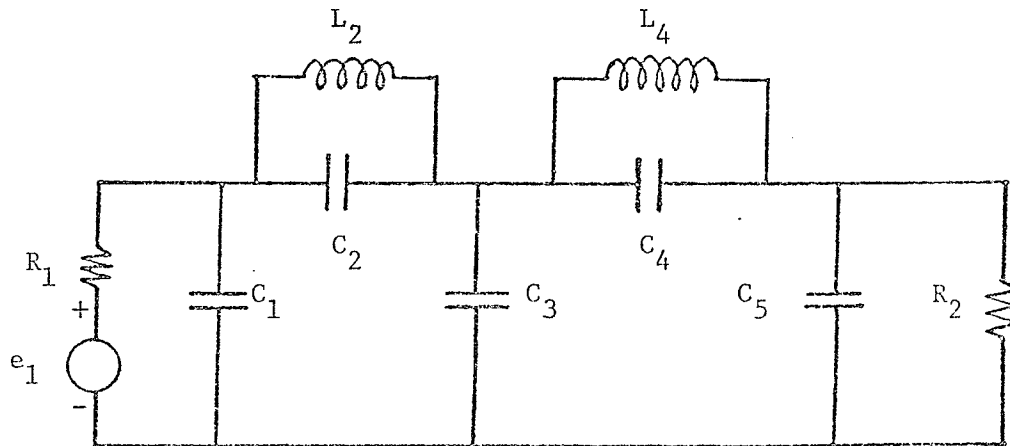


Fig. 6.7 The reference filter of the first example.

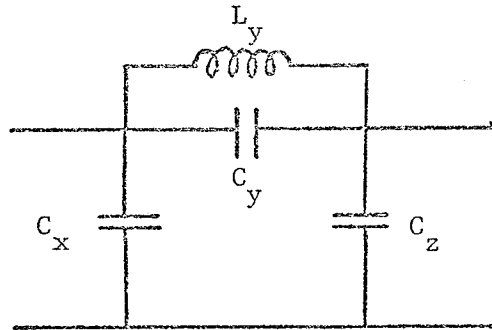


Fig. 6.8 Circuit with loop of capacitances (C_x , C_y , C_z).

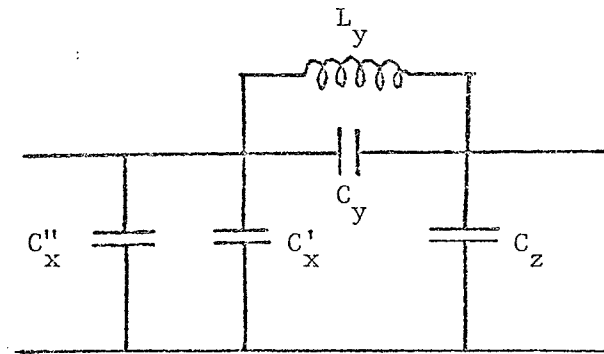


Fig. 6.9 Equivalent circuit of Fig. 6.8.

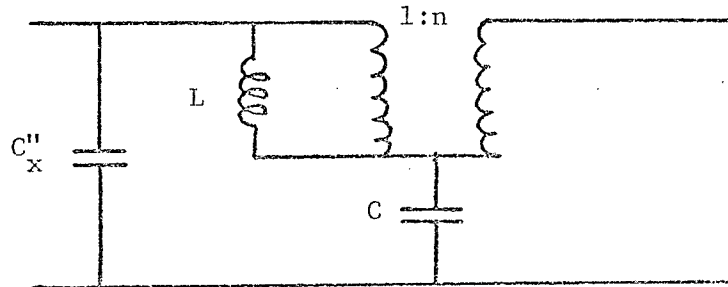


Fig. 6.10 Equivalent circuit of Fig. 6.9.

compose the capacitance C_x into two capacitances C'_x and C''_x such that

$$C'_x + C''_x = C_x \quad (6.9)$$

$$C'_x C_y + C'_x C_z + C_y C_z = 0 \quad (6.10)$$

to obtain an equivalent circuit of Fig.6.8 as shown in Fig.6.9.

Solving Equations (6.9) and (6.10) yields

$$C''_x = C_x + \frac{C_y}{k} \quad (6.11)$$

where

$$k = 1 + \frac{C_y}{C_z} = \frac{C_z + C_y}{C_z} > 1 \quad (6.12)$$

From Guillemin [17], an equivalent circuit of Fig.6.9 is given by Fig.6.10, where

$$L = L_y k^2 \quad (6.13)$$

$$C = \frac{C_z}{k} \quad (6.14)$$

$$n = 1 - \frac{1}{k} = \frac{C_y}{C_z + C_y} < 1 \quad (6.15)$$

Applying the above transformation to the loop of capacitances (C_3, C_4, C_5) of Fig.6.7 yields the circuit of Fig.6.11.

Applying again the transformation to the loop of capacitances (C_1, C_2, C_3) yields the final equivalent circuit of the reference filter as shown in Fig.6.12., where

$$L_A = 1.733225 \text{ H} , C_A = 0.815285 \text{ F}$$

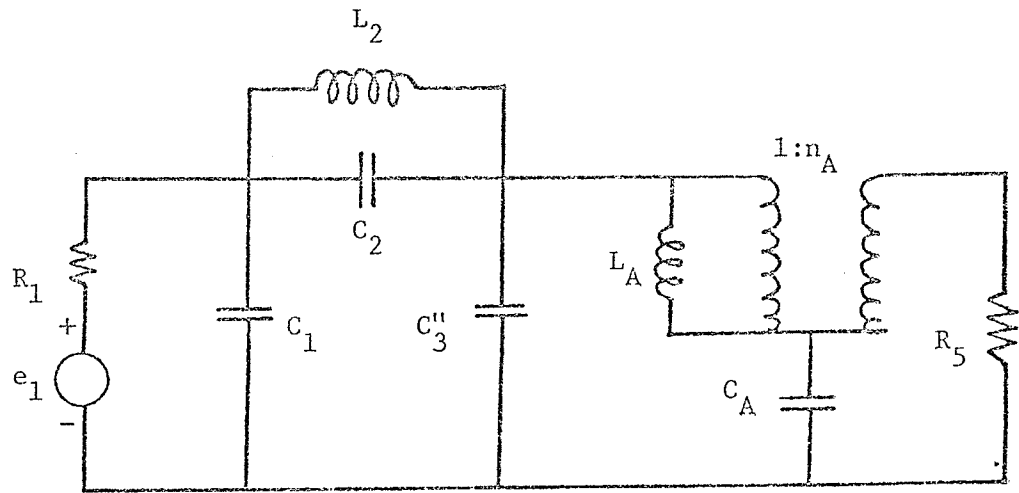


Fig. 6.11 Equivalent circuit of Fig. 6.7.

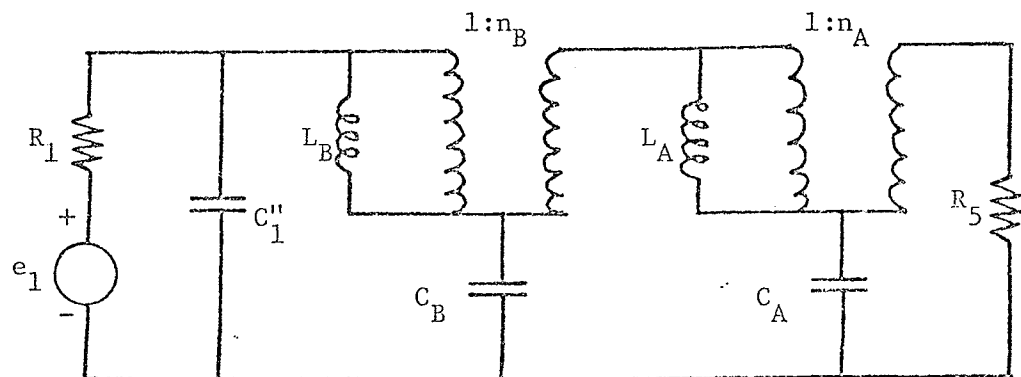


Fig. 6.12 Equivalent circuit of the reference filter.

$$\begin{aligned}
 L_B &= 1.370243 \text{ H} , & C_B &= 1.989698 \text{ F} \\
 n_A &= 0.225338 , & n_B &= 0.0499825 \\
 C_1'' &= 1.304183 \text{ F} , & R_1 &= 0.985839 \Omega
 \end{aligned}$$

and which uses two Brune sections and a total number of five reactive elements. We can draw by inspection an equivalent wave cascade realization as shown in Fig.6.13

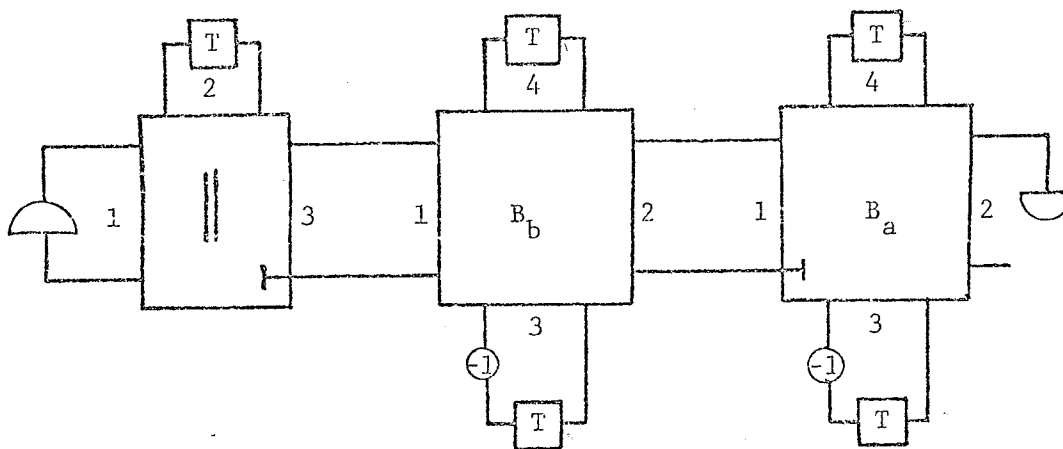


Fig. 6.13 Wave cascade realization of the reference filter.

which uses one three-port parallel adaptor of Fettweis and Sedlmeyer and two Brune adaptors labelled B_a and B_b . Port 3 of the parallel adaptor and port 1 of B_a are chosen as reflection-free ports. The structure is canonic in the number of delays since the order of the filter is five.

Upon imposing a 5% relative error on the set of dependent multipliers and applying the steps of design outlined in Section 6.1, we have the following set of multipliers for the wave filter

a) For B_a :

$$\hat{l}_{1a} = 1 - \hat{l}_{3a} = \frac{51}{64}$$

$$\hat{l}_{2a} = -\frac{7}{32} = -2^{-2} + 2^{-5}$$

$$\hat{l}_{3a} = \frac{13}{64} = 2^{-3} + 2^{-4} + 2^{-6}$$

$$\hat{l}_{4a} = \frac{59}{64} = 1 - 2^{-4} - 2^{-6}$$

$$\hat{n}_A = \frac{13 \times 1399}{78816} = 0.23075264$$

b) For B_b :

$$\hat{l}_{1b} = \frac{5}{8} = 2^{-1} + 2^{-3}$$

$$\hat{l}_{2b} = -\frac{1}{8} = -2^{-3}$$

$$\hat{l}_{3b} = \frac{45}{256} = 2^{-2} - 2^{-4} - 2^{-7} - 2^{-8}$$

$$\hat{l}_{4b} = \frac{89}{512} = 2^{-3} + 2^{-4} - 2^{-6} + 2^{-9}$$

$$\hat{n}_B = \frac{18 \times 23}{8653} = 0.047844678$$

c) For the parallel adaptor :

$$\hat{\alpha} = \frac{7}{16} = 2^{-1} - 2^{-4}$$

Upon using the transformation shown in Fig.6.14 , where

$$C_a = -\frac{n C}{1 - n} \quad (6.16)$$

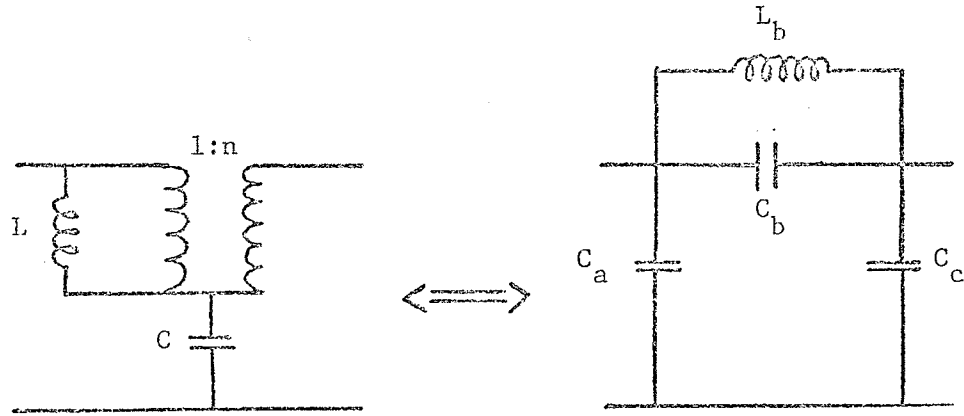


Fig. 6.14 Transformation of the Brune section into a ladder structure.

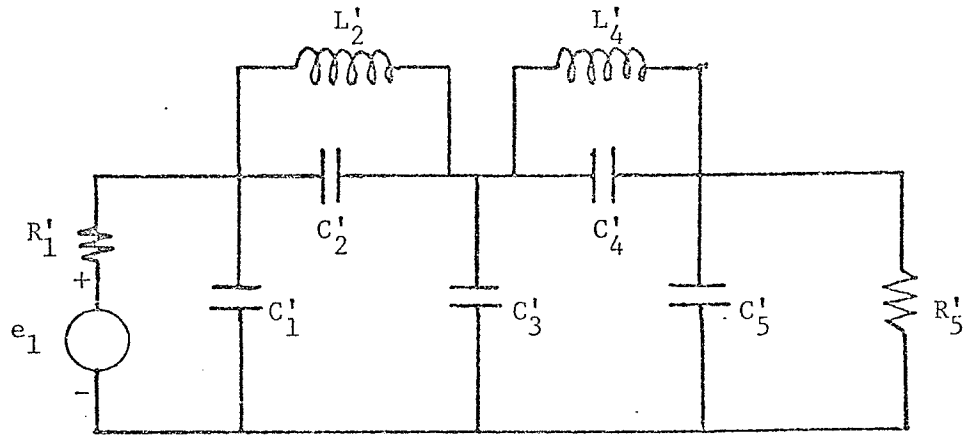


Fig. 6.15 Modified reference filter resulting from the quantization of the independent multipliers.

$$C_b = \frac{n C}{(1 - n)^2} \quad (6.17)$$

$$C_c = \frac{C}{1 - n} \quad (6.18)$$

$$L_b = L (1 - n)^2 \quad (6.19)$$

and the above multipliers, we can draw the corresponding modified ladder filter shown in Fig. 6.15, where

$$R'_1 = 0.985839 \Omega, \quad C'_1 = 1.20450 \text{ F}, \quad C'_2 = 0.10468 \text{ F}$$

$$L'_2 = 1.24128 \text{ H}, \quad C'_3 = 1.84201 \text{ F}, \quad C'_4 = 0.31369 \text{ F}$$

$$L'_4 = 1.02263 \text{ H}, \quad C'_5 = 1.04575 \text{ F}, \quad R'_5 = 1 \Omega$$

By comparing these new values with the original values, we have at most a 5% relative error in C_2 . If we were able to realize linearly the wave adaptor, then its performance would be similar to the continuous structure shown in Fig. 6.15. Instead, due to the finite word length available in the hardware realization, the quantized multipliers \tilde{n}_A and \tilde{n}_B are used. Upon choosing

$$\tilde{n}_A = 2^{-2} - 2^{-6} - 2^{-8} + 2^{-12}$$

$$\tilde{n}_B = 2^{-4} - 2^{-6} + 2^{-10}$$

and the simplified magnitude truncation scheme shown in Fig. 6.4, it can be shown that up to 3 bits are used to modify the outputs to suppress granularity oscillations. In other words, if the signals at the delays are represented by n bits of the format $d_0 \Delta d_1 d_2 \dots d_{n-1}$,

then the magnitude-truncated outputs are obtained from the actual outputs by adding or subtracting at most a numerical value equal to $7 \times 2^{1-n}$ according to the sign of the actual outputs; i.e., we add if the output is negative and subtract if the output is positive.

Simulation of the hardware realization is then carried out by a program written in Assembler language. Photograph I shows the impulse response which is finite due to the magnitude truncation of the output. Photograph II shows the attenuation characteristic vs the fractional bandwidth f/f_s where f_s is the sampling frequency or operating frequency of the filter. Photograph III shows the passband characteristic vs the fractional bandwidth. To compare these characteristics with the original attenuation characteristic shown in Fig. 6.6, these graphs have to be plotted again vs the frequency $\phi = \tan \frac{\pi f}{f_s}$.

Thus, the computer printout for Photograph IV gives the location of zeros of transmission

$$\phi_1 = 1.7907$$

$$\phi_2 = 2.822$$

and the minimum attenuation A_{\min} in the stopband

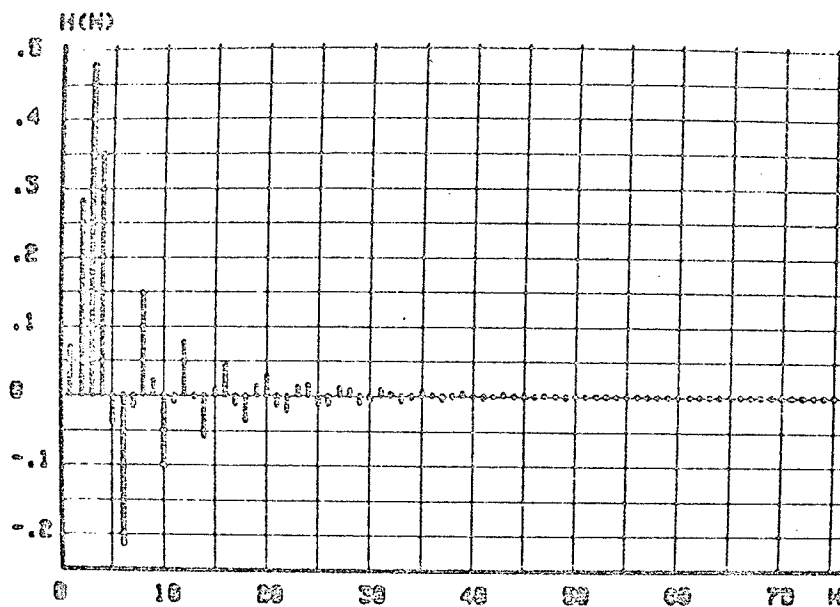
$$A_{\min} = 51.82 \text{ dB}, \text{ for } 1.7158 \leq \phi \leq \infty$$

We note that $\phi = \infty$ when $f/f_s = 0.5$.

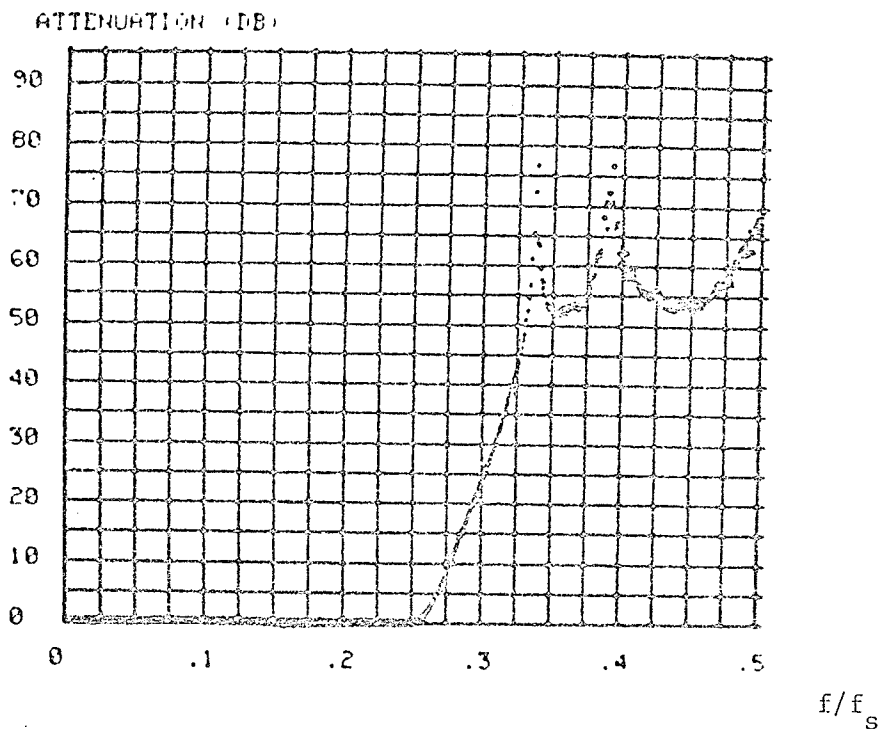
The computer printout for Photograph V gives the maximum ripple A_{\max} in the passband

$$A_{\max} = 0.192 \text{ dB}, \text{ for } 0 \leq \phi \leq 1$$

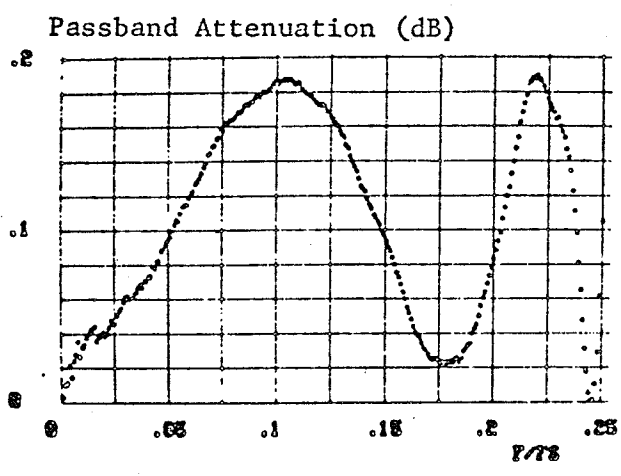
These values which have been obtained without using any iteration in



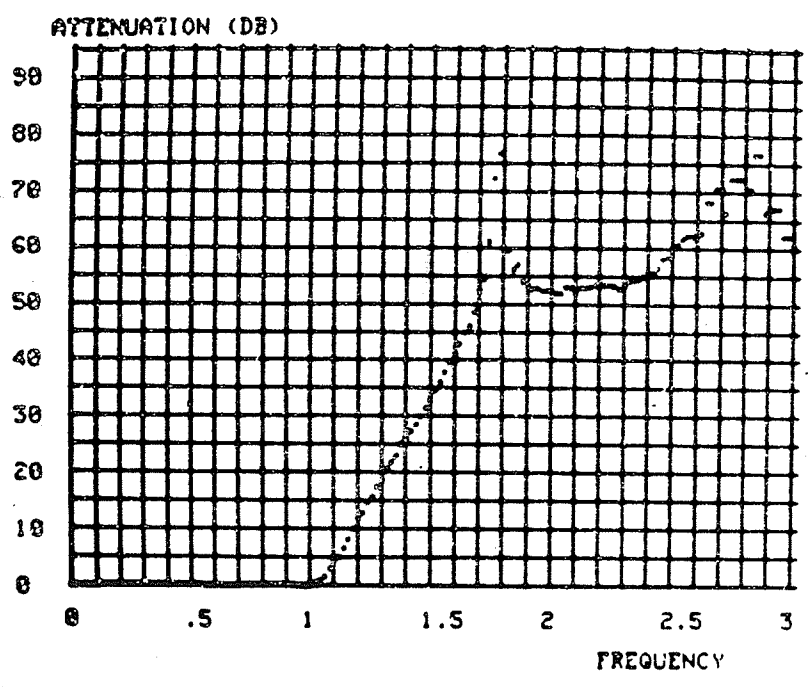
PHOTOGRAPH I Impulse response of fifth-order wave digital low-pass filter.



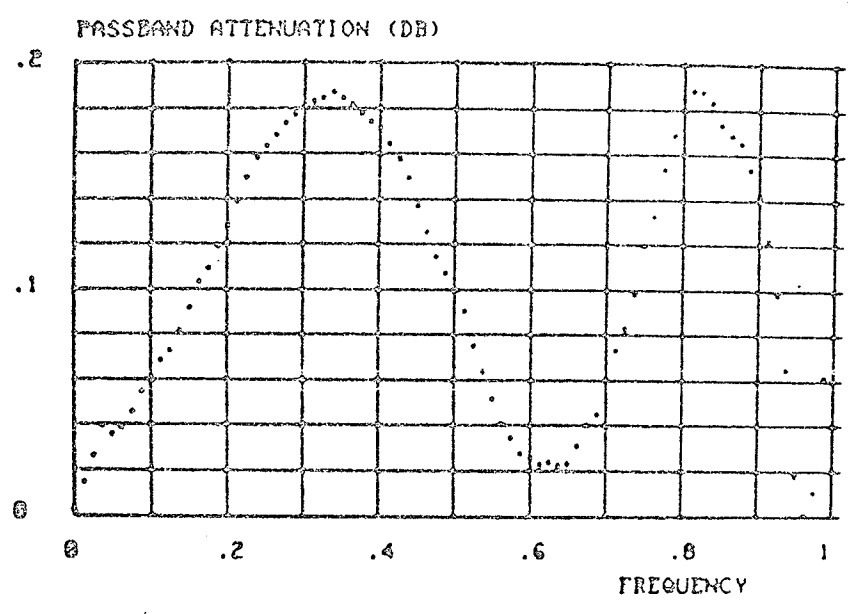
PHOTOGRAPH II Attenuation characteristic vs f/f_s .



PHOTOGRAPH III Passband characteristic vs f/f_s .



PHOTOGRAPH IV Attenuation characteristic vs ϕ



PHOTOGRAPH V Passband characteristic vs ϕ

the optimization procedure are close to the original specifications. If they are to satisfy the specifications, one could always go back to optimize the multiplier values or to start the design with another set of network parameters which exceed the original specifications.

As a possible application, such a fifth order elliptic wave digital filter could be used in PCM codecs that convert voice to digital signals as mentioned by Falk [32].

6.4.2 Second Example : Tenth order equiripple delay and attenuation low-pass filter.

The reference filter of the second example has been taken from Kwan and Bach [33]. It is shown in Fig.6.16.

The finite zeros of transmission of this filter are given as

$$\begin{aligned} f_1 &= 1.0390514 j & , & & f_2 &= -1.0390514 j \\ f_3 &= 1.3472503 j & , & & f_4 &= -1.3472503 j \\ f_5 &= -.31959 + .20921 j & , & & f_6 &= -.31959 - .20921 j \\ f_7 &= .31959 + .20921 j & , & & f_8 &= .31959 - .20921 j \end{aligned}$$

It is a tenth-order equiripple delay and attenuation low-pass filter, the specifications of which are given by the following :

- a) Minimum stopband attenuation $A_{\min} = 63 \text{ dB}$, for $1.013 < \omega \leq \infty$
- b) Maximum passband attenuation ripple $A_{\max} = 0.164 \text{ dB}$, for $0 \leq \omega \leq 0.4 \text{ rad/s}$
- c) A linear phase over $0 \leq \omega \leq 0.7 \text{ rad/s}$ with a mean time delay $\tau = 15.355 \text{ s}$.

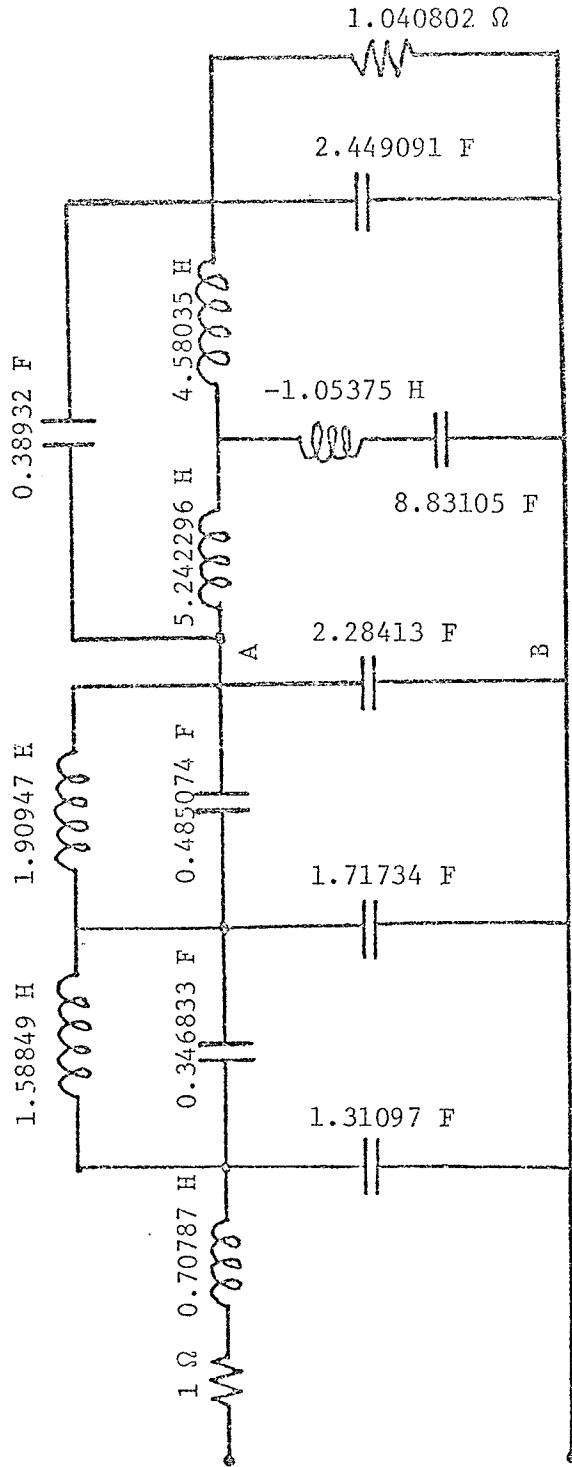


Fig. 6.16 Reference filter of the second example.

We note first that Martens' and Meerkötter's Bridge-Tee adaptor [27] might have been used together with Fettweis' and Sedlmeyer's adaptors [12] to realize the filter in wave digital form if the inductance L_6 were positive. Since L_6 is negative, we might not be able to guarantee the asymptotic stability of the wave filter under zero input. The two loops of capacitances (C_1, C_2, C_3) and (C_3, C_4, C_5) can be transformed into two Brune sections using the transformation given in the first example. For the remaining Bridge-Tee structure, we proceed in the following manner.

First, let us consider the Bridge-Tee structure shown in Fig. 6.17. Analysis of the structure yields the input impedance Z_{in} as

$$Z_{in} = \frac{Z_1 Z_2 (Z_4 + Z_5) + Z_3 Z_4 (Z_1 + Z_2) + Z_4 Z_5 (Z_1 + Z_3) + Z_3 Z_5 (Z_1 + Z_2)}{Z_1 (Z_2 + Z_3 + Z_5) + Z_2 (Z_3 + Z_4 + Z_5) + Z_4 (Z_3 + Z_5)} \quad (6.20)$$

Upon letting

$$Z_1 = L_5 s = 5.242296 s$$

$$Z_2 = L_7 s = 4.58035 s$$

$$Z_3 = \frac{1 - L_6 C_6 s^2}{C_6 s} = \frac{1 + 1.05375 \times 8.83105 s^2}{8.83105 s}$$

$$Z_4 = \frac{1}{C_8 s} = \frac{1}{0.38932 s}$$

$$Z_5 = \frac{1}{C_7 s + \frac{1}{R_7}} = \frac{1}{2.449091 s + \frac{1}{1.040802}}$$

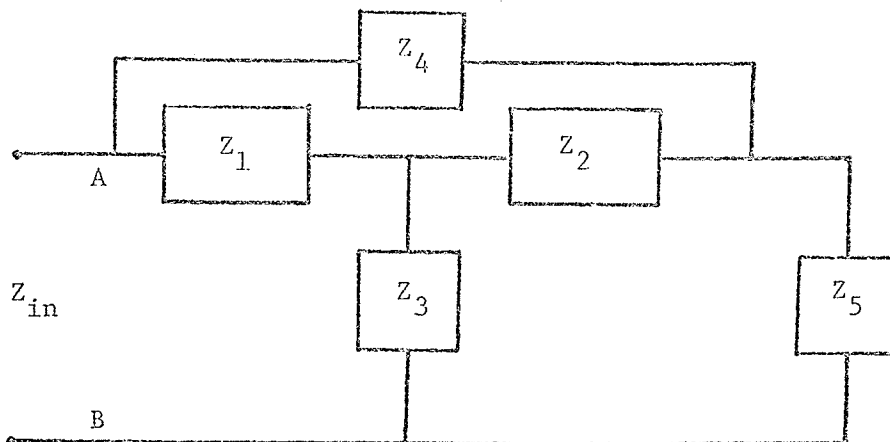


Fig. 6.17 Bridge-Tee structure.

$$n_4 = 0.1371493371 \quad , \quad n_5 = -1.12001474$$

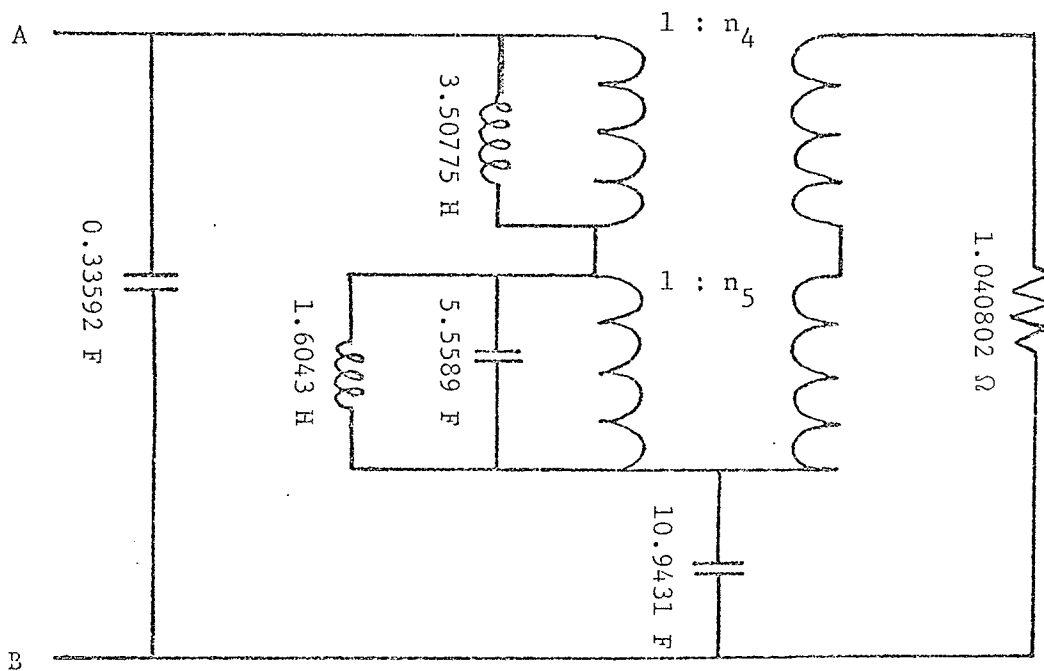


Fig. 6.18 Realization of Z_{in} .

the input impedance $Z_{in}(s)$ can be written as

$$Z_{in}(s) = \frac{342.4271s^4 + 115.911s^3 + 64.87s^2 + 9.4376s + 1}{115.028s^5 + 45.1265s^4 + 119.4105s^3 + 33.597s^2 + 11.28s + 0.960798} \quad (6.21)$$

Upon removal of a parallel capacitance $C = \frac{115.028}{342.4271} \text{ F} = 0.3359204 \text{ F}$,

the remaining driving-point impedance $Z_R(s)$ is

$$\begin{aligned} Z_R(s) &= Z_{in}(s) - \frac{1}{Cs} \\ &= \frac{(342.4271s^4 + 64.87s^2 + 1) + (115.911s^3 + 9.4376s)}{(6.1896s^4 + 30.42664s^2 + 0.960798) + (97.6193s^3 + 10.9442s)} \end{aligned} \quad (6.22)$$

If $Z_R(s)$ is to be realized as a resistively terminated lossless network, then the zeros of transmission are the roots of the following polynomial

$$\begin{aligned} P(s) &= (342.4271s^4 + 64.87s^2 + 1)(6.1896s^4 + 30.42664s^2 + 0.960798) \\ &\quad - (115.911s^3 + 9.4376s)(97.6193s^3 + 10.9442s) \\ &= 2119.48815s^8 - 494.72756s^6 + 119.122588s^4 - 10.53335s^2 + 0.960798 \end{aligned} \quad (6.23)$$

Solving $P(s) = 0$ yields the quadruplet of zeros of transmission

$$s_0 = \pm 0.319613 \pm 0.209261j \quad (6.24)$$

which corresponds to the given frequencies f_5, f_6, f_7, f_8 .

Knowing s_0 , we can realize $Z_R(s)$ using a Darlington D-section. According to Scanlan and Rhodes [34], the element values of the

Darlington D-section can be found to be the one given by Fig.6.18 which shows the realization of $Z_{in}(s)$.

Combining the capacitance $C = 0.33592$ F of Fig.6.18 with C_5 and then using the transformation given in the first example yield the realization of the given filter which features two Brune sections and one Darlington D-section as shown in Fig.6.19. We note that the realization contains ten reactive elements. From Fig.6.19, we can draw the equivalent wave cascade realization with the chosen reflection-free ports as shown in Fig.6.20. The wave realization has two Brune adaptors labelled B_a and B_b , one Darlington D adaptor labelled D , two 3-port parallel adaptors of Fettweis labelled P_a and P_b , and one 3-port series adaptor of Fettweis labelled S . It is canonic in the number of delays since the number of delays is equal to the order of the filter which is ten .

Upon imposing a 3% relative error bound on the set of dependent multipliers and applying the design steps outlined in Section 6.1, we have the following set of multipliers for the wave digital filter

a) For D :

$$\hat{\ell}_{1d} = \frac{9}{512} = 2^{-6} + 2^{-9}$$

$$\hat{\ell}_{2d} = \frac{1}{8} = 2^{-3}$$

$$\hat{\ell}_{3d} = 1 - \hat{\ell}_{1d} - \hat{\ell}_{5d} = \frac{473}{512}$$

$$\hat{\ell}_{4d} = \frac{7}{16} = 2^{-1} - 2^{-4}$$

$$\hat{\ell}_{5d} = \frac{15}{256} = 2^{-4} - 2^{-8}$$

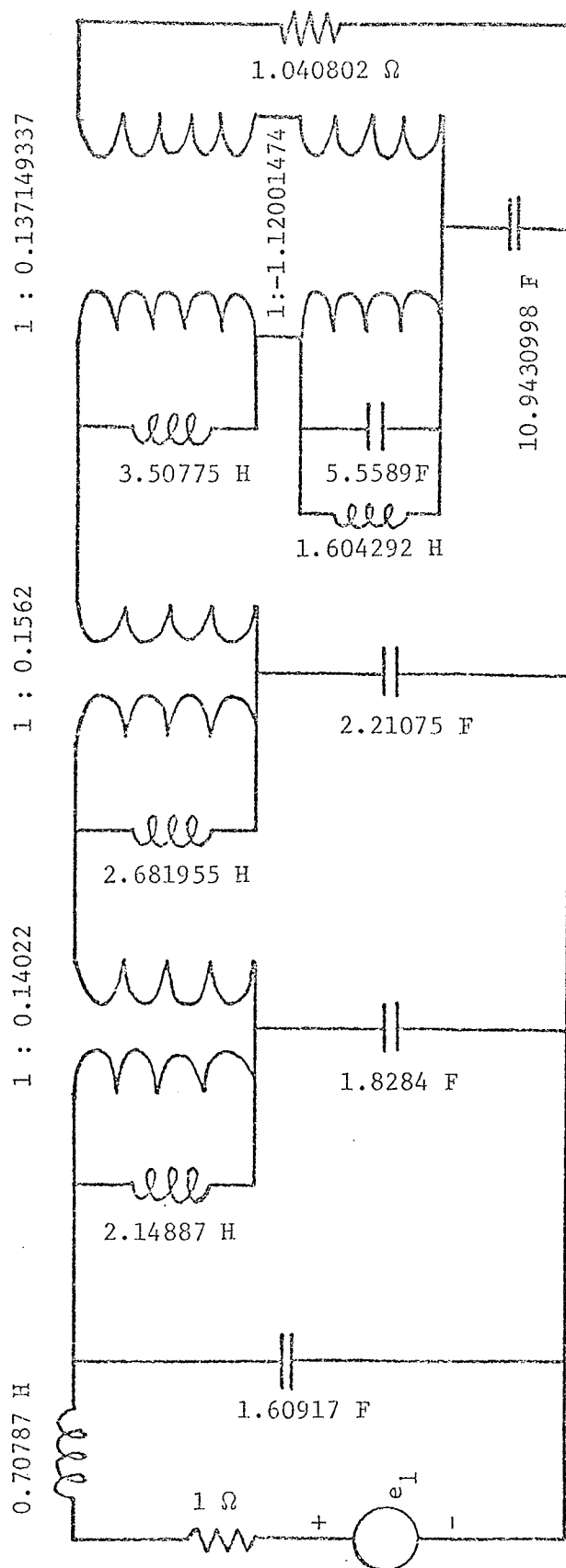


Fig. 6.19 Equivalent circuit of the reference filter.

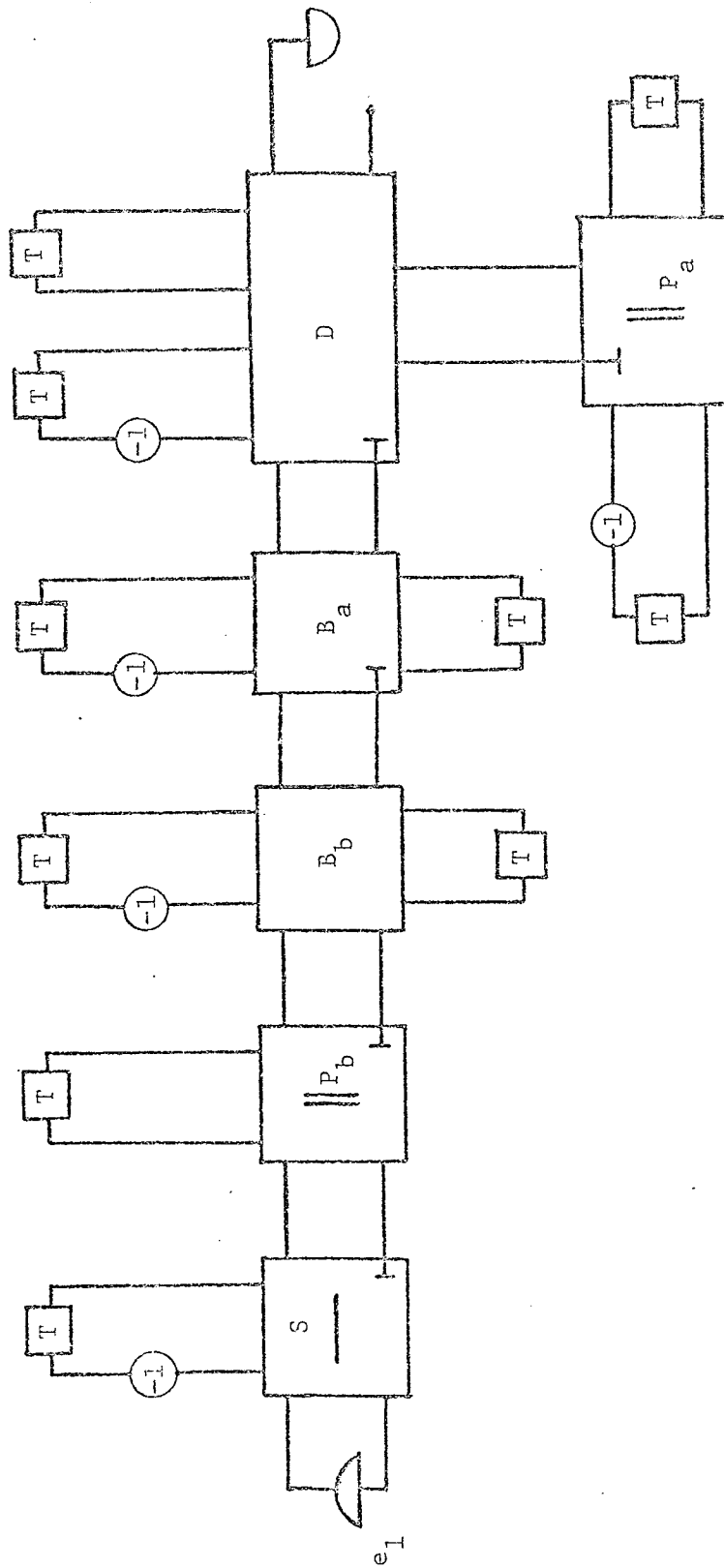


Fig. 6.20 Wave cascade realization of the given filter.

$$\hat{\ell}_{6d} = -\frac{9}{32} = -2^{-2} - 2^{-5}$$

$$\hat{n}_4 = 0.1366058511$$

$$\hat{n}_5 = -1.117849167$$

b) For B_a :

$$\hat{\ell}_{1a} = 1 - \hat{\ell}_{3a} = \frac{7}{8} = 1 - 2^{-3}$$

$$\hat{\ell}_{2a} = \frac{9}{512} = 2^{-6} + 2^{-9}$$

$$\hat{\ell}_{3a} = \frac{1}{8} = 2^{-3}$$

$$\hat{\ell}_{4a} = \frac{3}{16} = 2^{-2} - 2^{-4}$$

$$\hat{n}_a = 0.1606524636$$

c) For B_b :

$$\hat{\ell}_{1b} = \frac{45}{32} = 1 + 2^{-1} - 2^{-3} + 2^{-5}$$

$$\hat{\ell}_{2b} = -\frac{11}{64} = -2^{-3} - 2^{-4} + 2^{-6}$$

$$\hat{\ell}_{3b} = \frac{9}{32} = 2^{-2} + 2^{-5}$$

$$\hat{\ell}_{4b} = \frac{1}{4} = 2^{-2}$$

$$\hat{n}_b = 0.1442006$$

d) For P_a :

$$\hat{c}_a = \frac{13}{128} = 2^{-4} + 2^{-5} + 2^{-7}$$

e) For P_b :

$$\hat{\alpha}_b = \frac{17}{64} = 2^{-2} + 2^{-6}$$

f) For S :

$$\hat{\alpha}_s = \frac{19}{32} = 2^{-1} + 2^{-3} - 2^{-5}$$

Corresponding to the above multipliers, we would have a modified reference filter as shown in Fig.6.21. By comparing the new element values with the original values, it can be seen that the highest relative error is 4.86% for the inductance of the Brune section which is adjacent to the Darlington D-section. All the other relative errors are less than 3%.

Upon choosing

$$\tilde{n}_4 = 2^{-3} + 2^{-6} - 2^{-8} - 2^{-13}$$

$$\tilde{n}_5 = -1 - 2^{-3} + 2^{-7} - 2^{-11} - 2^{-12} + 2^{-14}$$

$$\tilde{n}_a = 2^{-3} + 2^{-5} + 2^{-8} + 2^{-11}$$

$$\tilde{n}_b = 2^{-3} + 2^{-6} + 2^{-8} - 2^{-12} - 2^{-14}$$

and the simplified magnitude truncation scheme as shown in Fig.6.4, it can be shown that up to 3 bits are used to modify the outputs to suppress granularity oscillations.

Simulation of the hardware realization is carried out by two programs, one written in BASIC and one written in ASSEMBLER, with both using the quantized dependent multipliers \tilde{n}_a , \tilde{n}_b , \tilde{n}_4 and \tilde{n}_5 .

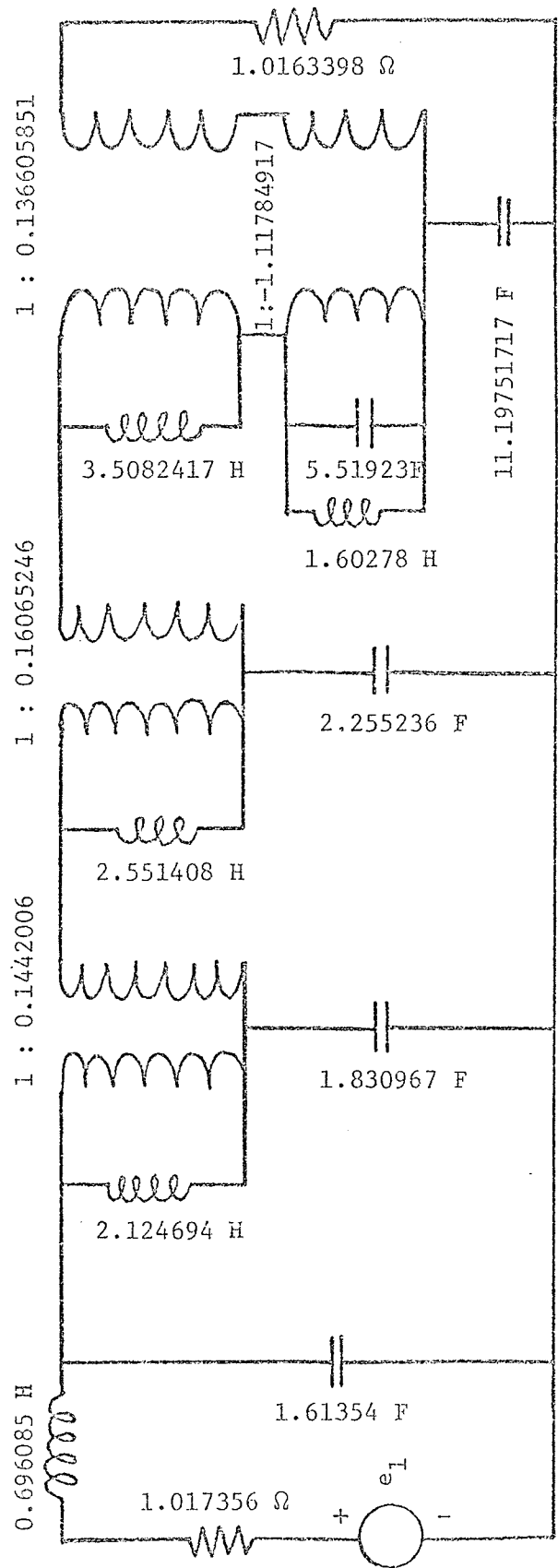


Fig. 6.21 Modified equivalent circuit of the reference filter.

Running the program under BASIC introduces practically no truncation error because all arithmetic operations produce results in floating-point numbers which have a wider range than fixed-point arithmetic. Photograph VI shows the impulse response of the filter which is decreasing rapidly towards zero. Photographs VII and VIII show, respectively, the stopband and the passband attenuation characteristics vs the fractional bandwidth f/f_s . Photographs IX and X show again the same curves in Photographs VII and VIII which are plotted vs the frequency $\phi = \tan \frac{\pi f}{f_s}$ to permit a direct comparison with the original specifications of the continuous-time filter. From the computer printout for these photographs we have

$$\text{a) zeros of transmission at } \phi_1 = 1.0503, \phi_2 = 1.2895$$

$$\text{b) } A_{\min} = 58.8 \text{ dB, for } 1.0062 < \phi \leq \infty$$

$$\text{c) } A_{\max} = 0.15535 \text{ dB, for } 0 \leq \phi \leq 0.4$$

Photograph XI shows the phase of the filter plotted vs ϕ which is linear over $0 \leq \phi \leq 0.7$ with a mean time delay

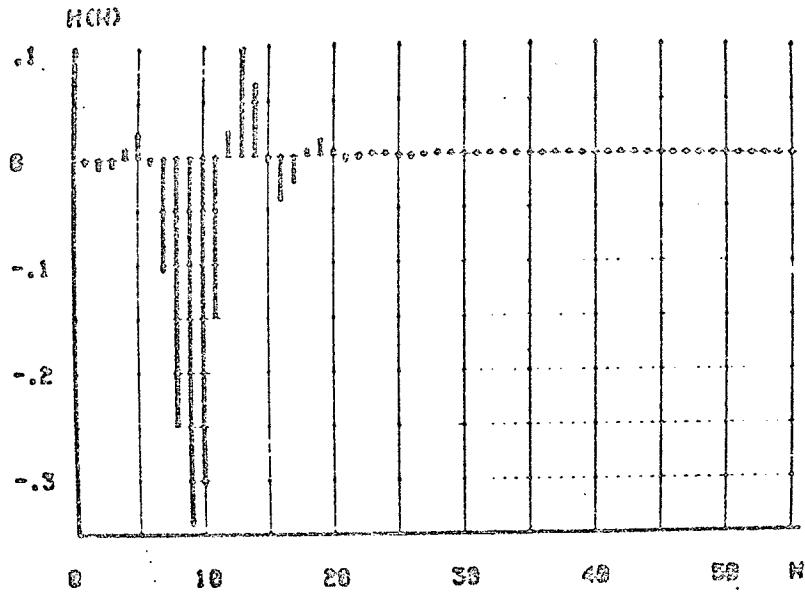
$$\tau = \frac{13}{0.85} = 15.2941 \text{ s}$$

These values have been obtained if there is almost no truncation error.

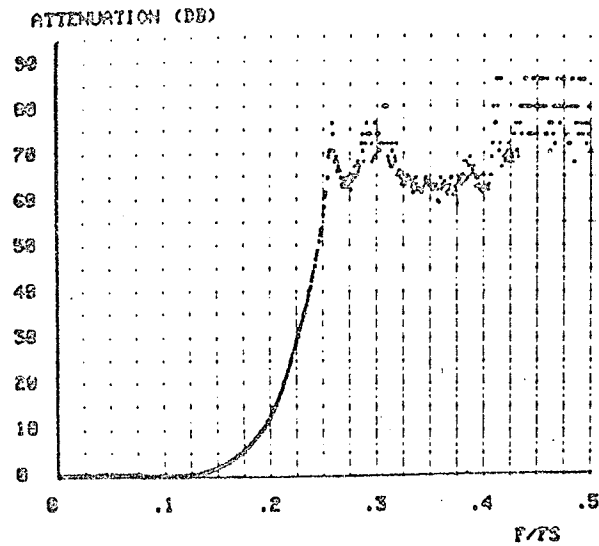
Running the simulation under ASSEMBLER gives the following results.

Photograph XII shows the finite impulse response and Photograph XIII shows the stopband attenuation characteristic vs f/f_s . From the computer printout for these photographs we have a

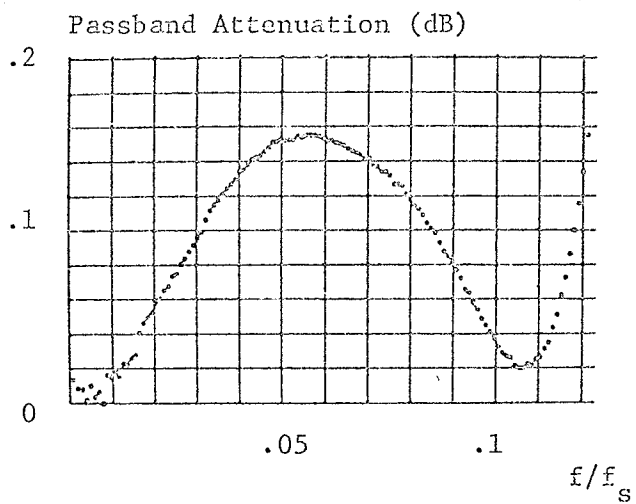
$$A_{\min} = 59 \text{ dB, for } 1 < \phi \leq \infty$$



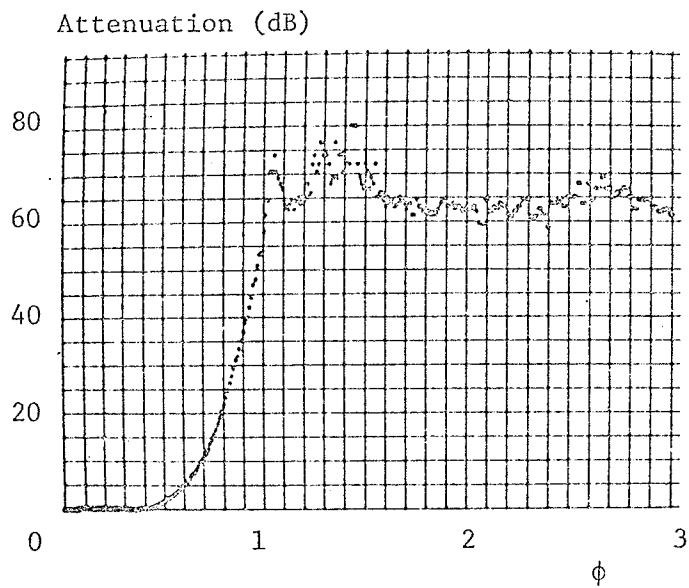
PHOTOGRAPH VI Impulse response of tenth-order wave digital low-pass filter.



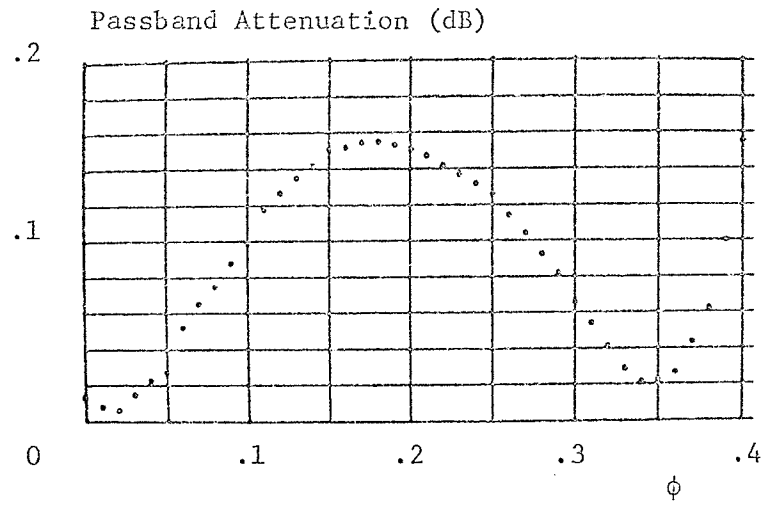
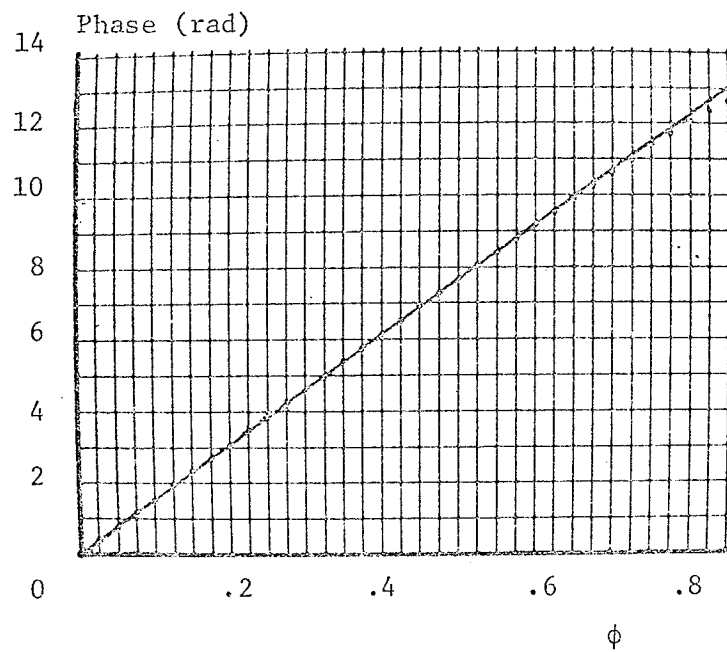
PHOTOGRAPH VII Attenuation characteristic vs f/f_s .

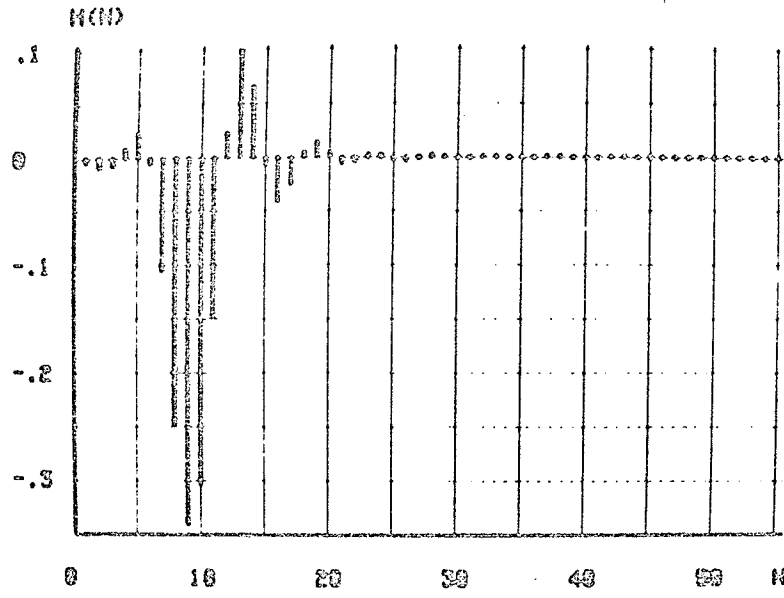


PHOTOGRAPH VIII Passband characteristic vs f/f_s .

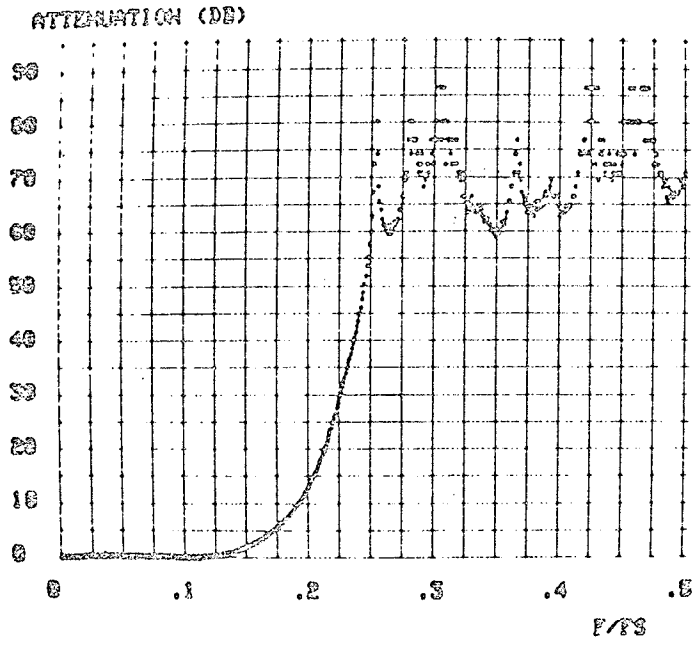


PHOTOGRAPH IX Attenuation characteristic vs ϕ

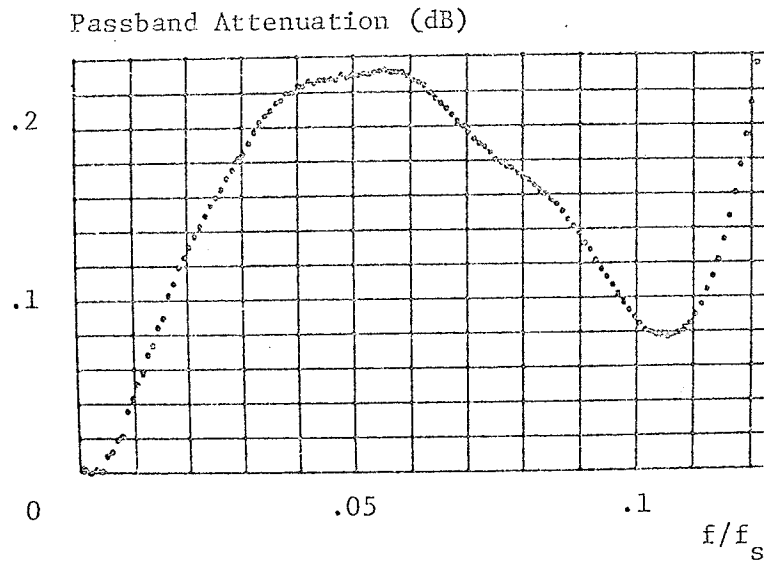
PHOTOGRAPH X Passband characteristic vs ϕ PHOTOGRAPH XI Phase of the filter vs ϕ



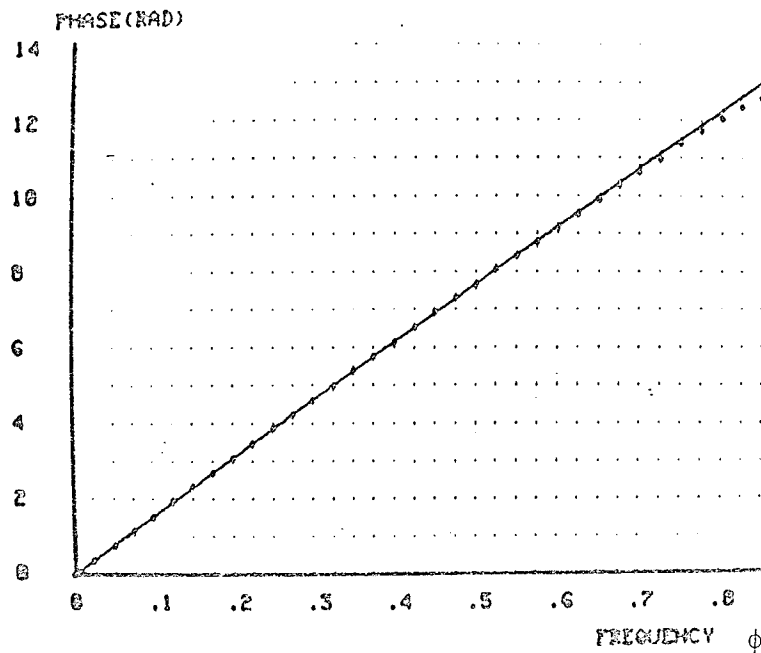
PHOTOGRAPH XII Finite impulse response of tenth-order wave digital low-pass filter.



PHOTOGRAPH XIII Attenuation characteristic vs f/f_s .



PHOTOGRAPH XIV Passband characteristic vs f/f_s .



PHOTOGRAPH XV Phase of the filter vs ϕ

and two zeros of transmission at

$$\phi_1 = 1.0248$$

$$\phi_2 = 1.2895$$

The computer printout for Photograph XIV gives a maximum ripple

$$A_{\max} = 0.2323 \text{ dB} , \text{ for } 0 \leq \phi \leq 0.4$$

Photograph XV shows the phase plotted vs ϕ which is still linear over $0 \leq \phi \leq 0.7$ with a slope $\tau = 15.2941 \text{ s}$. The curve seems to be the same as the one already shown in Photograph XI.

We note that truncation error in this case has degraded the performance of the filter in the passband. In the stopband, the zeros are displaced but the stopband attenuation is still as good as the one shown in Photograph VII.

6.4.3 Third Example : Twin-T filter.

As reference filter for the third example, we have the following Twin-T filter shown in Fig.6.22.

According to Appendix II, if we let

$$R_1 = R_2 = 1 \ \Omega$$

$$C_3 = C_6 = 1.5 \text{ F}$$

$$L_4 = L_5 = \frac{2}{3} \text{ H}$$

$$L_7 = 1 \text{ H}$$

$$C_8 = 1 \text{ F}$$

then we have the transfer voltage function

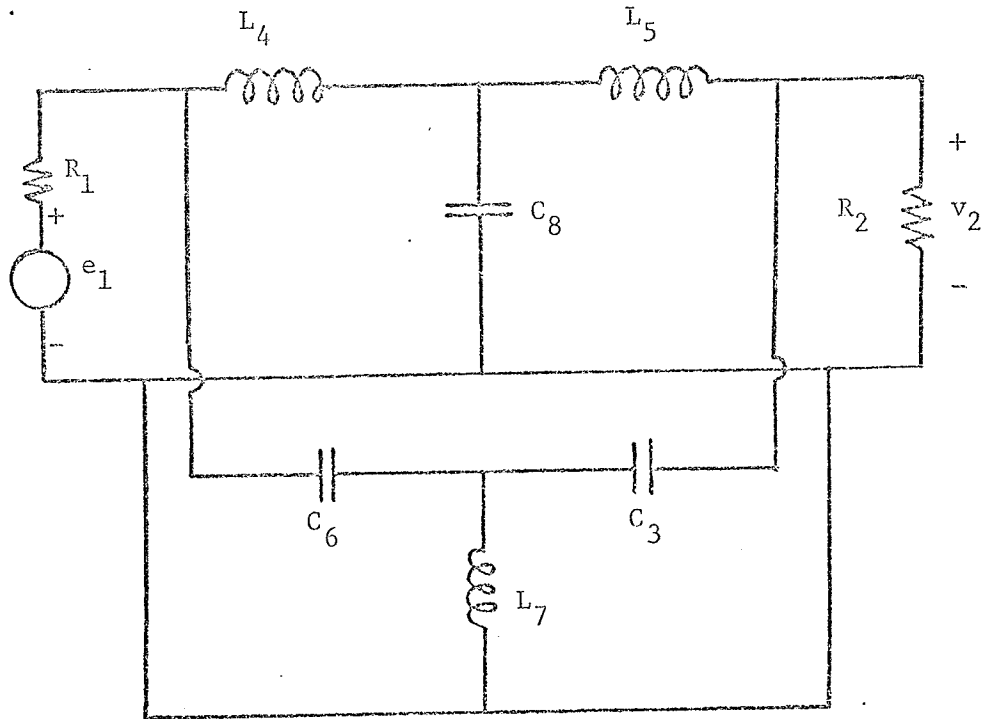


Fig. 6.22 Reference filter of the third example.

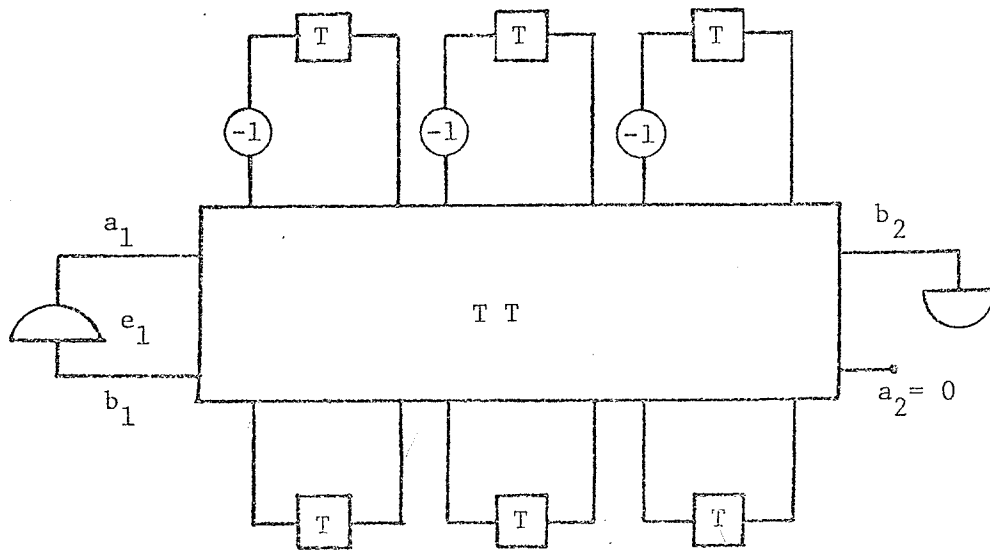


Fig. 6.23 Wave realization of the Twin-T filter.

$$t_v(s) = \frac{v_2}{e_1} = \frac{(s^2 + 1)^3}{2s^6 + 5.333s^5 + 11.333s^4 + 12.444s^3 + 10.333s^2 + 5.333s + 2} \quad (6.25)$$

From (6.25), it is seen that the transfer function has third-order zeros of transmission at $\omega = \pm 1$. The Twin-T filter behaves as a notch filter at the frequency $\omega = \pm 1$ with a 3 dB rejection bandwidth over the range $0.465 \text{ rad/s} \leq \omega \leq 2.125 \text{ rad/s}$.

We immediately can draw the equivalent wave realization upon labelling the Twin-T adaptor as the block TT in Fig.6.23.

We note again that the realization is canonic in the number of delays since the order of the filter is six.

Using the given numerical element values then following closely the design steps detailed in Section 6.1, we have the following set of multipliers upon imposing a tolerance of 0.5% on the dependent multipliers A_3, A_4, A_5 which are, respectively, 0.136364, 0.5, and 0.136364.

$$\hat{A}_1 = \frac{151}{256} = 2^{-1} + 2^{-3} - 2^{-5} - 2^{-8}$$

$$\hat{A}_2 = \frac{31}{64} = 2^{-1} - 2^{-6}$$

$$\hat{A}_3 = 0.135931$$

$$\hat{A}_4 = 0.499556$$

$$\hat{A}_5 = 0.13602$$

$$\hat{A}_6 = \frac{345}{512} = 2^{-1} + 2^{-3} + 2^{-4} - 2^{-6} + 2^{-9}$$

$$\hat{A}_7 = \frac{307}{512} = 2^{-1} + 2^{-4} + 2^{-5} + 2^{-7} - 2^{-9}$$

$$\hat{A}_8 = \frac{307}{512} = 2^{-1} + 2^{-4} + 2^{-5} + 2^{-7} - 2^{-9}$$

$$\hat{A}_9 = \frac{27}{64} = 2^{-1} - 2^{-4} - 2^{-6}$$

$$\hat{A}_{10} = \frac{5}{8} = 2^{-1} + 2^{-3}$$

The modified reference filter corresponding to the above set of multipliers is shown in Fig.6.24.

It can be seen from Fig.6.24 that the highest relative error is 0.56% for the inductance L_7 .

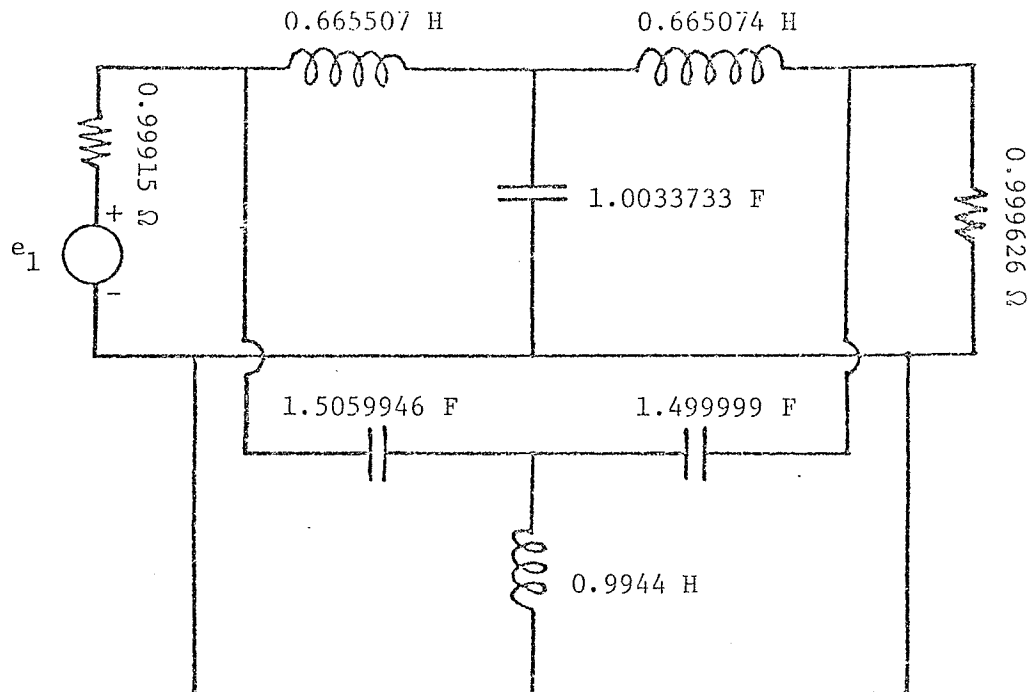


Fig. 6.24 Modified reference filter.

Upon choosing

$$\tilde{\Lambda}_3 = 2^{-3} + 2^{-7} + 2^{-8} - 2^{-10} + 2^{-13}$$

$$\tilde{\Lambda}_4 = 2^{-1} - 2^{-11}$$

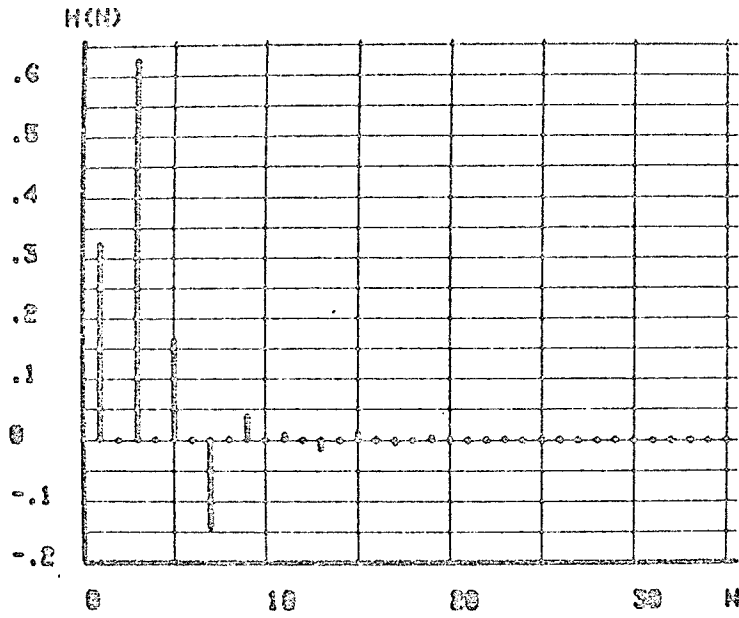
$$\tilde{\Lambda}_5 = 2^{-3} + 2^{-7} + 2^{-8} - 2^{-10} + 2^{-12}$$

and the simplified magnitude truncation scheme as shown in Fig.6.4, it can be shown that up to 3 bits are used to modify the outputs to suppress granularity oscillations.

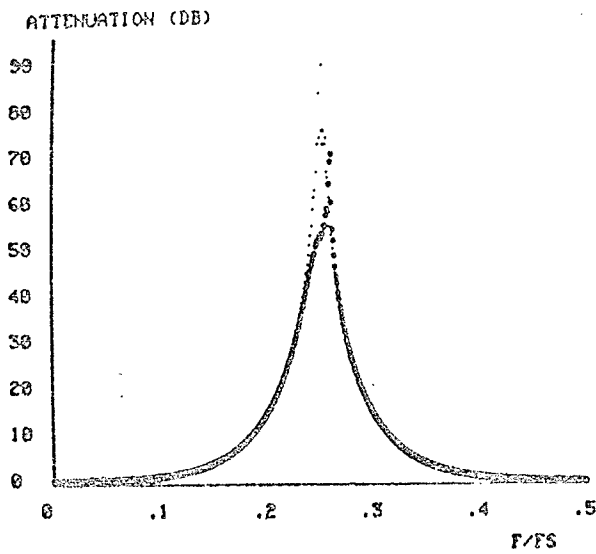
We note that the low tolerance 0.5% imposed upon the dependent multipliers requires a longer word length representation of the quantized independent multipliers such as $\hat{\Lambda}_6$, $\hat{\Lambda}_7$ and $\hat{\Lambda}_8$.

Simulation of the hardware realization has been again carried out by two programs, one written in BASIC and one written in ASSEMBLER. Photograph XVI shows the impulse response of the filter obtained from the BASIC program. Photograph XVII shows two frequency response curves : the fainter one is the frequency response of the ideal linear filter vs f/f_s and the brighter one is the frequency response of the simulated filter without truncation error vs f/f_s . The computer printout for these curves shows a displacement of the zeros of transmission from the original $\phi = 1.0$ to the frequency $\phi = \tan \pi(0.2588) = 1.057$, and a lower minimum attenuation in the neighborhood of this zero of transmission probably due to the resolution of the FFT subroutine SPARTA.

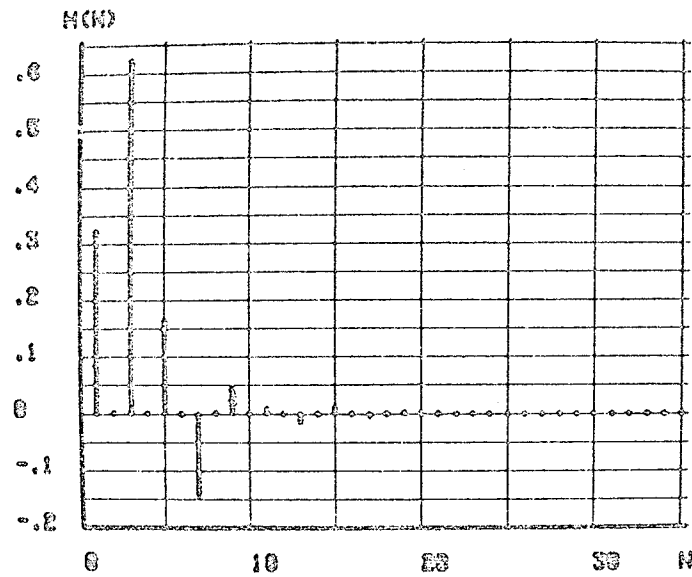
The impulse response obtained from the ASSEMBLER program is



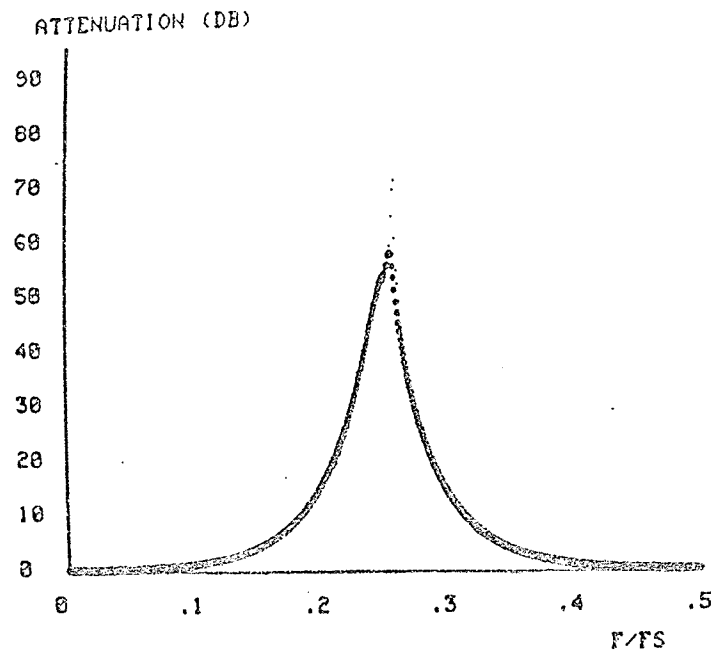
PHOTOGRAPH XVI Impulse response of the Twin-T wave digital filter.



PHOTOGRAPH XVII Attenuation characteristics vs f/f_s .



PHOTOGRAPH XVIII Finite impulse response of the Twin-T wave digital filter.



PHOTOGRAPH XIX Attenuation characteristics vs f/f_s .

shown to be finite in Photograph XVIII. Photograph XIX shows the degradation in performance of the hardware realization of the filter when there is truncation error : the fainter curve corresponds to the frequency response of the filter when there is no truncation error and is a duplication of the brighter curve of Photograph XVII while the brighter curve corresponds to the frequency response of the actual hardware realization of the given filter. Photograph XIX shows no change in the passband but it does show a smaller attenuation in the neighborhood of the zero of transmission. This degradation of performance is expected since the filter has been "passified" and thus has lost its good insensitivity property in the stopband.

CHAPTER VII

CONCLUSIONS

In this thesis, wave adaptors for the Brune section, the Darlington C and D sections, and the Twin-T structure have been derived together with the necessary formulas and wave flow diagrams for their realization .

The wave adaptors for the Brune section, the Darlington C and D sections have been realized without any unit elements and since they all may have a reflection-free port, these sections together with Fettweis' parallel, series, and lattice adaptors as well as Fettweis' or Nouta's wave realization of a transformer are sufficient to translate any reciprocal cascade realization resulting from Darlington's cascade synthesis or from Fettweis' factorization of the transfer matrix into a true and direct wave digital cascade synthesis.

The investigated adaptors mentioned above are canonical in the number of delays. The wave adaptors for the Brune section and the

Darlington C-section each require a total number of six multipliers of which two are identical multipliers. The wave realization of the Darlington D-section requires a total number of eleven multipliers of which there are two pairs of identical multipliers.

The Twin-T adaptor requires a total number of ten multipliers of which seven are independent multipliers. It may have a reflection-free port. For the structures investigated in this thesis, the presence of a reflection-free port always reduces the total number of multipliers by one.

For the hardware realization of the investigated adaptors, the optimization problem for the quantization of the independent multipliers has been formulated and proven to always have a solution if the dependent-multiplier functions are continuous. Although the thesis does not offer an optimization technique, such a technique can be chosen among the already available programming techniques.

A sufficient condition which guarantees the zero input asymptotic stability of the investigated structures together with some rules to calculate the output errors of the hardware implementation using fixed-point arithmetic and two's complement arithmetic representation from the wave flow diagrams has enabled us to present a magnitude truncation scheme which determines the quantization of the dependent multipliers and which guarantees the zero input asymptotic stability of the hardware realization by means of a simple arithmetic procedure. Though the performance of these adaptors is expected to be degraded due to this magnitude truncation procedure, the effect of such an error

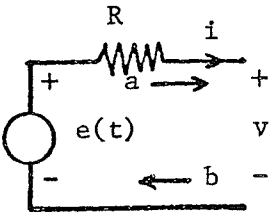
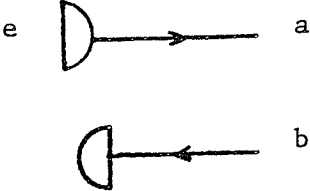
on their performance still is subject to further investigation.

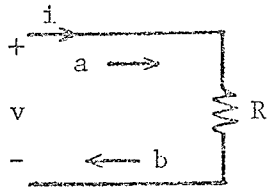
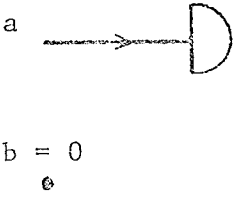
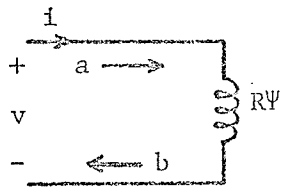
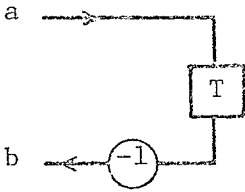
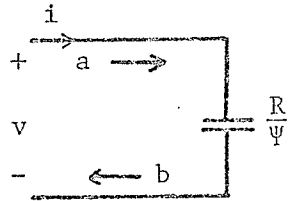
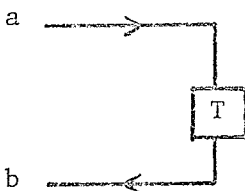
Illustrative examples of filters using the investigated adaptors have been designed and implemented on a small PDP 11/40 computer. Their respective impulse responses are obtained and show no granularity and/or overflow oscillations, as expected.

APPENDIX I

WAVE FLOW DIAGRAMS OF SOME BASIC CIRCUIT ELEMENTS

In this appendix, we present the wave flow diagrams of some basic circuit elements as derived by Fettweis [10] upon applying directly the bilinear transformation to these elements. The instantaneous incident wave $a(t)$ and reflected wave $b(t)$ are defined by means of a port resistance equal to the resistance constant R occurring in the definition of the element under consideration. The following table will give the wave flow diagrams of some basic circuit elements such as a resistive source, a resistance R , an inductance and a capacitance together with the difference equations which result from the wave digital realization.

ELEMENT	WAVE FLOW DIAGRAM	DIFFERENCE EQUATION
 <p>Resistive source.</p>		$a(t) = e(t)$

ELEMENT	WAVE FLOW DIAGRAM	DIFFERENCE EQUATION
 <p>Resistance R.</p>	 <p>$b = 0$</p>	<p>$b(t) = 0$</p>
 <p>Inductance of impedance $R\Psi$</p>		<p>$b(t) = -a(t-T)$</p>
 <p>Capacitance of impedance R/Ψ</p>		<p>$b(t) = a(t-T)$</p>

APPENDIX II

VOLTAGE TRANSFER FUNCTION OF THE TWIN-T STRUCTURE

Let us consider the Twin-T filter as shown in Fig.II.A, where (1) , (2) , (3) , (4) and (5) are the vertices of the network.

Upon transforming the voltage source e_1 into the Thevenin's current source $I_1 = G_1 e_1$, we have the equivalent network shown in Fig.II.B.

According to Seshu and Reed [35] , we can write

$$\frac{v_2}{I_1} = \frac{\sum T_{2,3}}{V(Y)} \quad (\text{II.1})$$

where

$$V(Y) = \sum (\text{tree-admittance products})$$

and

$\sum T_{2,3}$ is the sum of 2-tree products in which the vertices (1) and (2) are in one connected part and the vertex (3) is in the other connected part.

The voltage transfer function can be written from (II.1) as

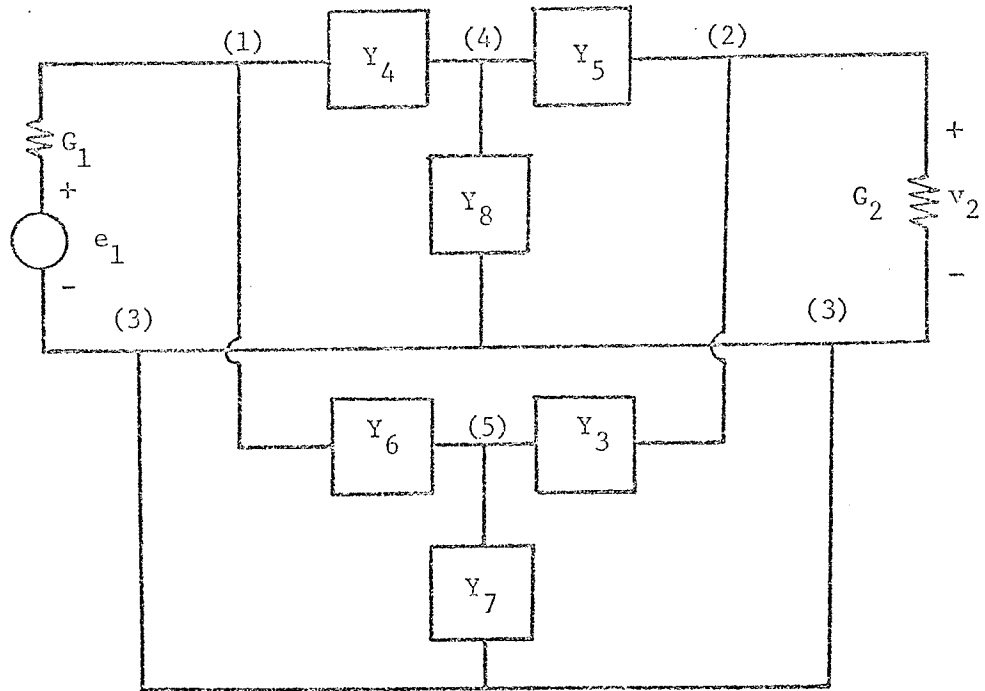


Fig. II.A Twin-T filter.

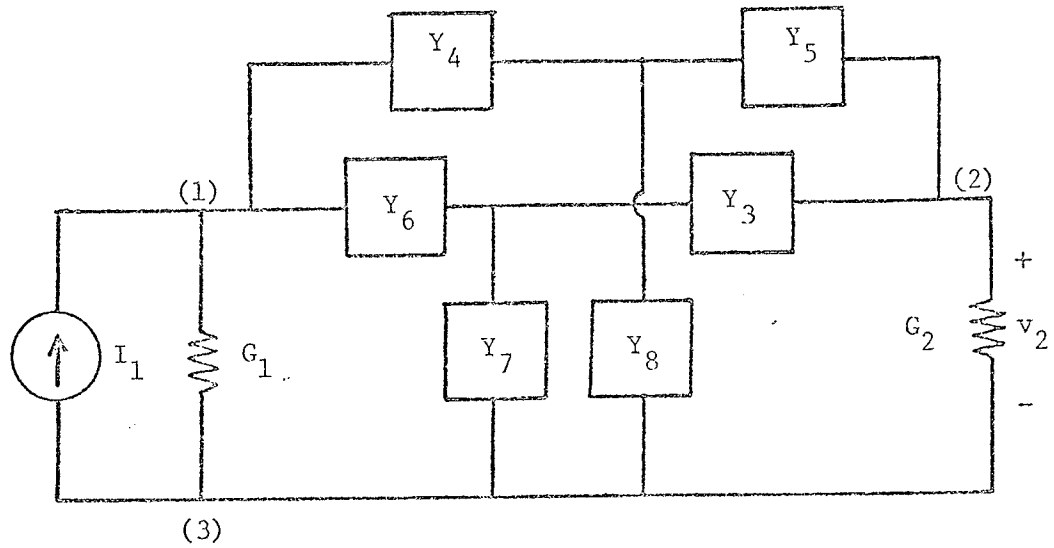


Fig. II.B Twin-T filter with current source $I_1 = G_1 e_1$.

$$t_v = \frac{v_2}{e_1} = \frac{G_1 \Sigma T_2}{V(Y)} \quad (II.2)$$

where

$$\Sigma T_2 \quad 12,3 = Y_3 Y_6 Y_8 + Y_4 Y_5 Y_7 + Y_3 Y_5 Y_6 + Y_3 Y_4 Y_5 + Y_4 Y_5 Y_6 + Y_3 Y_4 Y_6$$

and

$$\begin{aligned} V(Y) = & G_1 G_2 (Y_7 Y_8 + Y_5 Y_6 + Y_3 Y_4 + Y_4 Y_6 + Y_3 Y_5 + Y_3 Y_8 + Y_4 Y_7 \\ & + Y_6 Y_8 + Y_5 Y_7) + G_1 Y_3 (Y_7 Y_8 + Y_5 Y_6 + Y_4 Y_5 + Y_5 Y_7 + Y_6 Y_8 \\ & + Y_5 Y_8 + Y_4 Y_6) + G_1 Y_5 (Y_6 + Y_7) (Y_4 + Y_8) + Y_7 Y_8 (Y_3 Y_4 \\ & + Y_5 Y_6 + Y_3 Y_6 + Y_4 Y_5 + Y_2 Y_6 + Y_2 Y_4) + G_2 Y_4 (Y_5 Y_6 + Y_3 Y_6 \\ & + Y_5 Y_7 + Y_6 Y_8 + Y_6 Y_7 + Y_3 Y_5 + Y_3 Y_8) + Y_6 Y_8 (Y_3 Y_4 + Y_3 Y_5 \\ & + Y_2 Y_3 + Y_4 Y_5) + Y_6 Y_7 (Y_3 Y_4 + Y_4 Y_5 + Y_3 Y_5 + Y_2 Y_5) \\ & + Y_3 Y_5 (Y_4 Y_7 + Y_2 Y_6 + Y_4 Y_8) \end{aligned}$$

Upon letting

$$Y_3 = C_3 s$$

$$Y_4 = \frac{1}{L_4 s}$$

$$Y_5 = \frac{1}{L_5 s}$$

$$Y_6 = C_6 s$$

$$Y_7 = \frac{1}{L_7 s}$$

$$Y_8 = C_8 s$$

we have

$$t_v(s) = \frac{v_2}{e_1} = \frac{N}{D} \quad (\text{II.3})$$

where

$$N = G_1 [C_3 C_6 C_8 L_4 L_5 L_7 s^6 + C_3 C_6 L_7 (L_4 + L_5) s^4 + L_7 (C_3 + C_6) s^{2+1}]$$

and

$$\begin{aligned} D = & C_3 C_6 C_8 L_4 L_5 L_7 (G_1 + G_2) s^6 + [G_1 G_2 L_4 L_5 L_7 C_8 (C_3 + C_6) \\ & + C_3 C_6 C_8 (L_4 L_5 + L_4 L_7 + L_5 L_7)] s^5 + [G_1 (C_3 C_8 L_4 L_5 \\ & + C_3 C_6 L_4 L_7 + C_3 C_8 L_4 L_7 + C_3 C_6 L_5 L_7 + C_6 C_8 L_4 L_7) + G_2 (C_6 C_8 L_4 L_5 \\ & + C_3 C_6 L_5 L_7 + C_6 C_8 L_5 L_7 + C_3 C_6 L_4 L_7 + C_3 C_8 L_5 L_7)] s^4 \\ & + [G_1 G_2 (C_8 L_4 L_5 + C_6 L_4 L_7 + C_3 L_5 L_7 + C_6 L_5 L_7 + C_3 L_4 L_7) \\ & + C_6 C_8 (L_4 + L_7) + C_3 (C_8 L_5 + C_6 L_5 + C_8 L_7 + C_6 L_4)] s^3 \\ & + [L_7 (G_1 + G_2) (C_3 + C_6) + L_4 (G_1 C_8 + G_1 C_3 + G_2 C_6) \\ & + G_2 L_5 (C_6 + C_8)] s^2 + [C_3 + C_6 + C_8 + G_1 G_2 (L_4 + L_5)] s \\ & + (G_1 + G_2) \end{aligned}$$

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