MODELING OF

INSTRUMENT TRANSFORMERS

FOR TRANSIENT SIMULATION

BY : FARAMARZ AMJADI

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A thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

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Faramarz Amjadi

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ABSTRACT

The Electromagnetic Transient DC program, EMTDC, is the software simulator of power networks in the real time domain. Over the years models for most power system elements have been developed as the FORTRAN subroutines of this package.

Among the power system instruments are transducers. The scaled-down duplicate of the current and the voltage of transmission lines measured by the instrument transformers is of great importance for both relaying and metering purposes. An accurate model should be able to simulate the different types of distortion associated with transducers. The distortion in current transformers is mostly due to nonlinear core characteristic. To represent the highly nonlinear magnetizing curve of a ferromagnetic core by a global linearized model, different approaches are implemented and three models are developed in this thesis. In all three cases there are two zones of operation, namely, the unsaturated portion and the saturated one which causes harmonic distortion in core current. The departure point from linear operation zone to saturation is known as the knee point. The user is able to specify the coordinates of this point as well as the slope of each portion.

The study of typical runs of the core saturation models indicates that there is close consistency between the outputs of the three models. There is also agreement between these outputs and the experimentally recorded core current waveforms.

It is shown that core saturation is not the sole distorting factor of measured waveforms. With capacitive voltage devices ferroresonance is a known phenomenon which causes undesirable voltage oscillation. Parameters like instant of fault, turns ratio of intermediate potential transformer and load configuration are separately tested and contribution of each factor to the maximum magnitude and time constant of the resonating waveform is investigated. The results are in agreement with the data recorded in literature.

Potential transformers are known as devices with the least output distortion. A properly designed potential transformer should not cause noticeable magnitude and phase distortion even when its core is saturated. This fact is checked by the model of a potential transformer and the obtained voltage fidelity is quite satisfactory.

In general the developed subroutines of a current transformer, a potential transformer and a capacitive voltage transformer are accurate enough to be used for power system simulation purposes. However, there is still room for further refinement of the models in many aspects including core saturation.

CHAPTER 1

INTRODUCTION

INTRODUCTION

The objective of this thesis is to develop software to study the transient response of three types of instrument transformers in the time domain. The investigated devices are current transformers (CT s), potential transformers (PT s) and capacitive voltage transformers (CVT s).

The results of a transient simulation may be used by power system engineers in design and placement of protective devices. These results also ensure that the system components have the proper ratings to tolerate the effects of overvoltages and overcurrents caused by a system disturbance.

The developed software will be used as subroutines in the EMTDC (Electromagnetic Transient Direct Current) package. EMTDC is the software tool used for the simulation of power system transients in the real time domain by the digital simulator at the Manitoba HVDC Research Centre. Fig. 1.1 illustrates the algorithm of EMTDC and the location of each subroutine or file within the program .

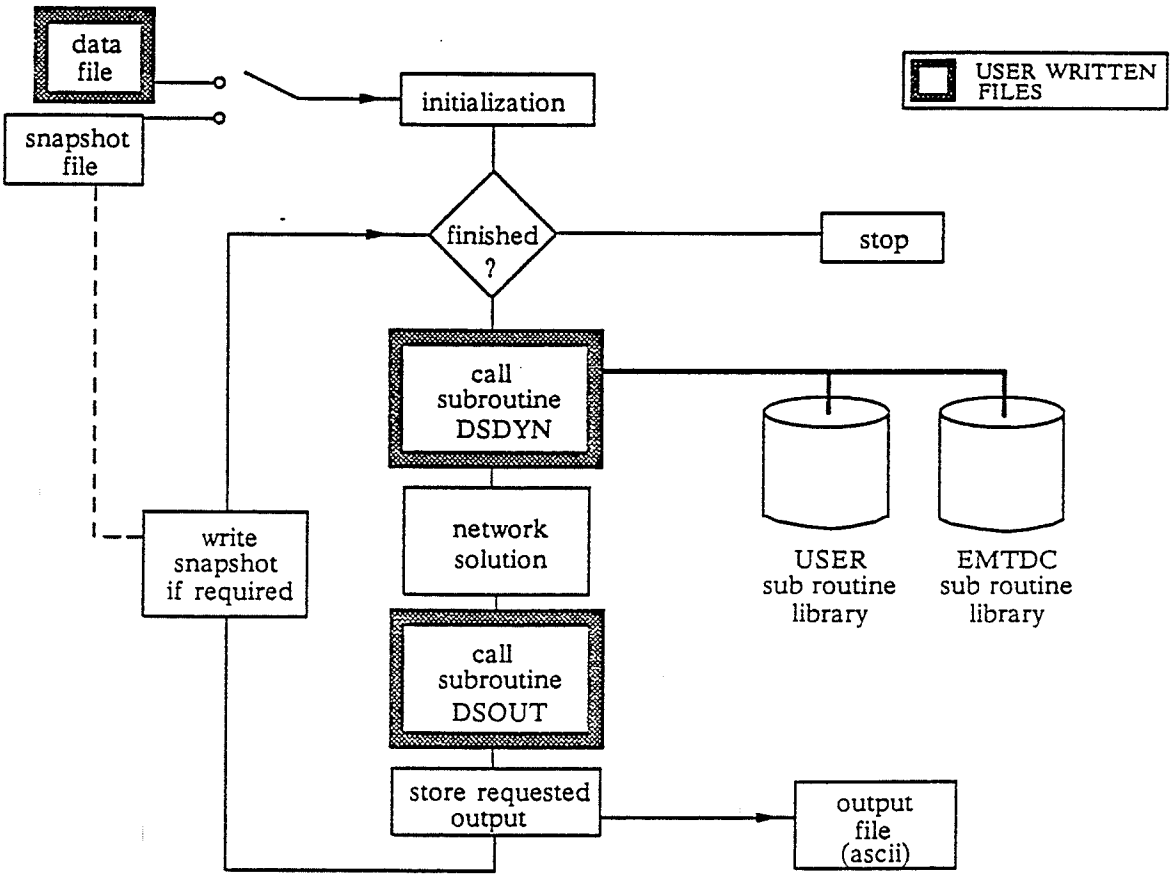

Fig. 1.1 Simplified EMTDC Algorithm Flow Chart [1]

A few words regarding the real time domain and digital simulators will asist the reader to gain a better understanding of the capabilities of EMTDC. An electrical power system can be mathematically represented by a set of equations in time domain. The exact number of these equations differs from one system to another. To determine the power system response to a disturbance, a typical digital simulator has to solve all these equations within a discrete time step. In order to achieve real time operation, all calculations must be performed in a time less than or equal to the time step which is used by the software-based simulator.

The computer network that is used at the Manitoba HVDC Research Centre to perform the calculations is based on the parallel processing concept. The general architecture of the machine is shown in Fig. 1.2 :

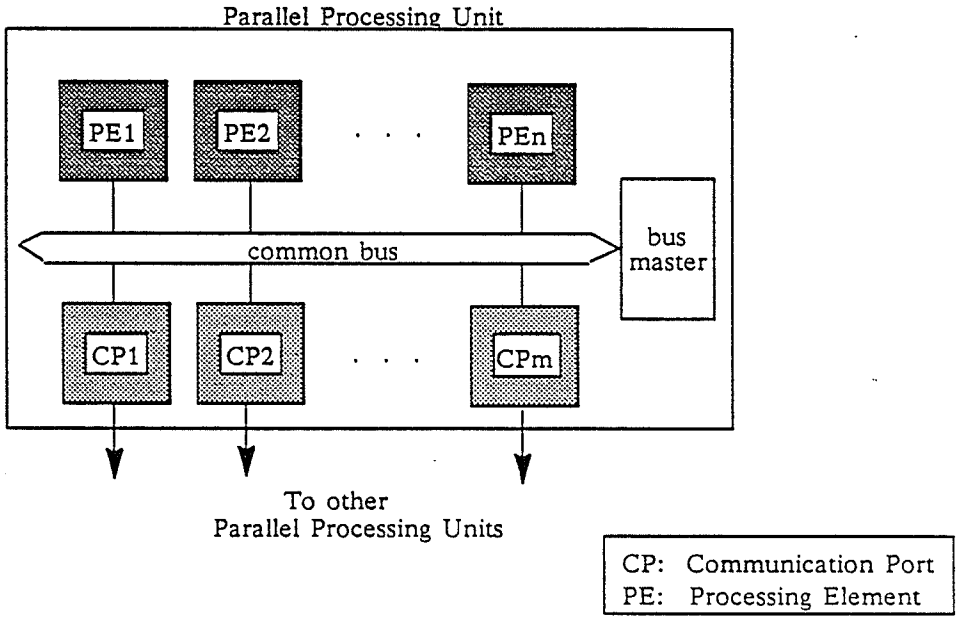

Fig. 1.2 Digital Simulator - Parallel Processing Unit [1]

Each one of the developed subroutines for the instrument transformers can be regarded as a PE module.

Although the introduction of the EMTDC program is not within the scope of this thesis, the following two paragraphs taken from the Manitoba Research Centre introductory booklet [1] can be beneficial for those with no background in EMTDC.

Simulation of electric power networks by digital computer was made possible by the pioneering work of Herman Dommel with the development of EMTP. The elegance and simplicity of Dommel's algorithm has been incorporated into a software transients package initially developed at Manitoba Hydro. The software simulator known as EMTDC was designed especially to allow the time domain simulation of power system networks which include HVDC converters and their controls.

Manitoba Hydro required very large electromagnetic transients system simulations of their power system including several DC links with controls and protection represented in detail. EMTDC was developed independently from published algorithm descriptions [2] without reference to any existing software code. Emphasis was placed on accommodating multiple converter representations with controls and protections in modular form for easy assembly and running on computer.

The next six chapters deal with the development and completion of subroutines which will be used in EMTDC for the simulation of instrument transformers. Chapter two starts with a review of fundamental electromagnetic concepts. Basic parameters governing core saturation such as magnetic field intensity and flux density are briefly skimmed to pave the way for introduction to magnetizing curves and hysteresis loops. Later in this chapter, hysteresis loops under steady state and transient conditions are discussed. Transient phenomena such as inrush current, remanence and minor loops are reviewed and different types of core losses are explained.

In chapter three, general electromagnetic principles applicable to all types of instrument transformers are reviewed. Equivalent circuits are discussed and the nature of saturated core current is investigated. Figures from reference 3 are used in chapters two and three to illustrate certain electromagnetic concepts.

Modeling of current transformers is the subject of chapter four. Here a thorough explanation of the model from the generation circuit up to the numerical stabilizing techniques is included. The mathematical background, as well as the practical aspects of circuit element modeling, are discussed. Two different core saturation models are developed. These two models are referred to as case 1 and case 2 throughout the thesis.

Most often transformer saturation is modeled using a piecewise linear representation of the magnetization characteristic. The characteristic can be fairly accurately represented in a piecewise linear manner using as few as two linear segments. This approach results in simple and fast models with sufficient accuracy [4].

In case 1, magnetizing core current is modeled by a two segment piecewise linear inductor. A linear resistor in parallel with the inductor models core resistive losses. Similar models have already been developed and discussed in literature [5]. The advantage of the present core model is that when an unsaturated core goes to saturation, the system admittance matrix does not change. This feature saves computer processing time in executing transient programs like EMTDC which use the method of admittance matrix inversion.

The core model of case 2 is based on a linearized flux - current loop. A similar method of modeling known as "square loop approximation" is discussed in reference [6] and its shortcomings are shown. The model of case 2 overcomes some of those deficiencies. The other feature of the core model of case 2 is that it does not contribute to the expansion of the system admittance matrix. In other words, no linear or nonlinear inductors would be placed in the admittance matrix. Therefore some computer processing time will be saved.

Finally the minor loops are linearized as parallelograms inside the parent flux - current loop. This is a unique feature in modeling of core transients and provides linear approximation of highly nonlinear minor loops.

Potential transformers are discussed in chapter five. The equivalent circuit model and a different method of representing core saturation are explained. To be able to evaluate the performance of the core models of case 1 and case 2, this third saturation model was developed. A similar core model is suggested in reference 7. The model is based on representing magnetizing inductance as a linear inductor. When a core goes to saturation, the difference between its linear magnetizing current and saturated magnetizing current is added to the current drawn by the linear inductor.

This model is implemented in the subroutines of potential transformers and capacitive voltage transformers. In many aspects this model is similar to the model of case 1. However, in the model of potential transformers both the linear magnetizing inductor and the core resistor appear in system admittance matrix, which is a drawback compared to the case 1.

Conclusions of the last two chapters are extended to chapter six. The content of this chapter includes a review of the development of the equivalent circuit of capacitive voltage transformers and ferroresonance. The main factors contributing to ferroresonance in capacitive voltage transformers are introduced and the effect of each parameter in this regard is investigated. The developed model of capacitive voltage transformers is subjected to a set of transient excitations, and the simulation responses are in close agreement with the recorded field data.

The results of the study are documented in chapter seven. The practical problems which were discovered during the development of the software are mentioned and the methods of overcoming them are explained. Chapter seven concludes with suggestions for the future improvement of models.

Typical computer plots of the developed models are included in the three appendices. One appendix has been devoted for each device. Appendix one deals with the response of a current transformer to a variety of different excitations. Appendices two and three consider the response of potential transformers and capacitive voltage transformers respectively. The content of each appendix is outlined prior to the computer plots.

The FORTRAN codes of the models are available upon request from:

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Winnipeg , Manitoba
Canada

CHAPTER 2

BASIC ELECTROMAGNETIC CONCEPTS

BASIC ELECTROMAGNETIC CONCEPTS

The nonlinear relation between the exciting current and the induced flux in the transformer core has been the subject of much study. In order to explain core saturation in instrument transformers, the nature of this nonlinear phenomenon has to be understood. In this chapter a number of basic and essential electromagnetic principles are briefly reviewed. More emphasis is put on those fundamental concepts which are closely related to the modeling of instrument transformers.

2.1 - Magnetic Field Intensity ($\vec{H}$) and Magnetic Flux Density($\vec{B}$)

Ampere's Circuital Law can be explained by employing the circuit of Fig. 2.1.

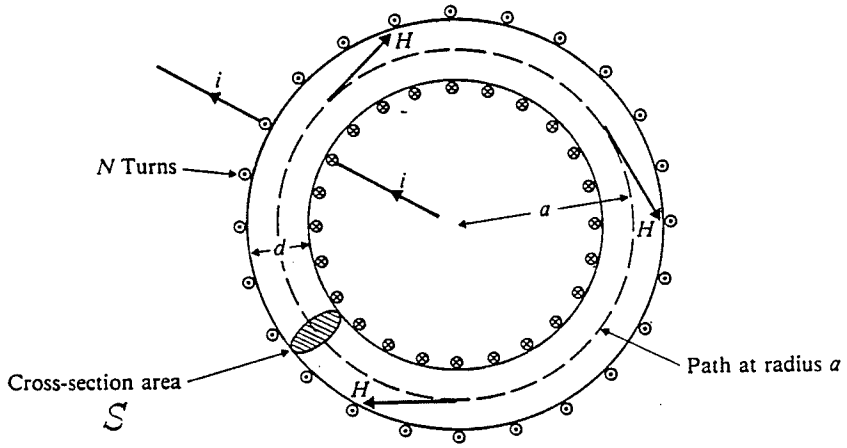


Fig. 2.1 - Coil Wound on a Ferromagnetic Torus [3]

The average length of the toroidal core is l. A circular cross section is chosen for convenience and s is the area of the surface bounded by the closed path. The core is made of a ferromagnetic material and a coil of N turns carrying a current i produces a magnetic field in the core. The intensity of this field can be calculated by Ampere's law :

$$\oint H \,.\, dl \;=\; \int_S J \;.\, dS \qquad 2.1.1$$

Here $\vec{J}$ is the current density over the bounded surface of the toroidal core. The flow of current i causes a magnetic flux within the core. The flux density ($\vec{B}$) is zero at points inside the hollow central portion and decreases inside the torus from the inner periphery to the outer periphery.

Although $\vec{B}$ changes with the variation of $\vec{H}$, the two parameters are not always linearly related. More specifically, if the magnetic flux density produced by a suitable range of the coil current is measured and is plotted versus the corresponding $\vec{H}$, a magnetizing curve similar to Fig. 2.2 will be obtained. Such a nonlinear curve can be considered as the basis of the core saturation of transformers and therefore has to be clearly understood before other important modeling factors are investigated.

In the following section the phenomenon of ferromagnetism will be discussed in more detail. This in turn will help the better understanding of the nonlinear nature of the magnetizing curves of ferromagnetic materials.

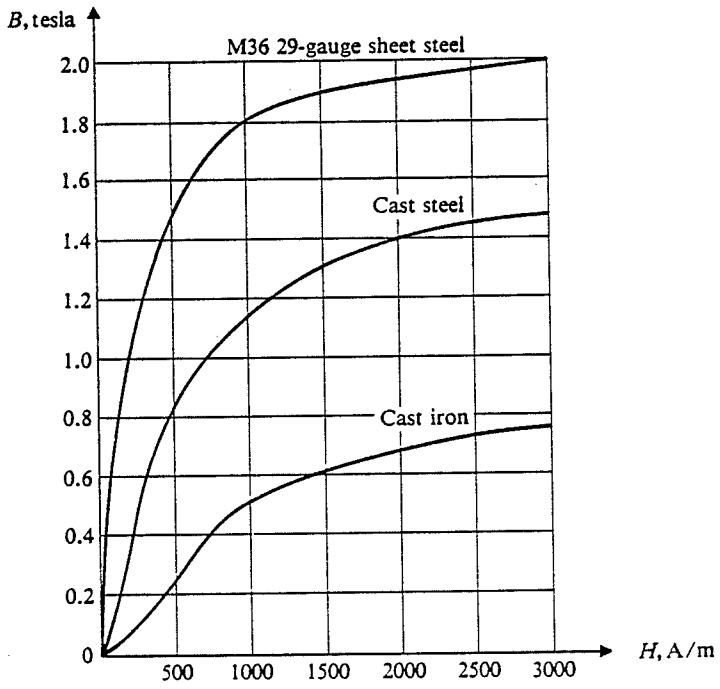


Fig. 2.2 - Magnetization Curves [3]

2.2 - Ferromagnetism and Saturation

Fig. 2.3 shows the spin and the motion of an electron around its atomic nucleus. The spherical model of the electron orbit is substituted with the simple circular path to

illustrate the atomic movements. For an electron with 1.6 x 10^{-19} Coulomb electric charge rotating clockwise around the nucleus, the direction of the equivalent positive current on the closed orbit is shown in Fig. 2.3.

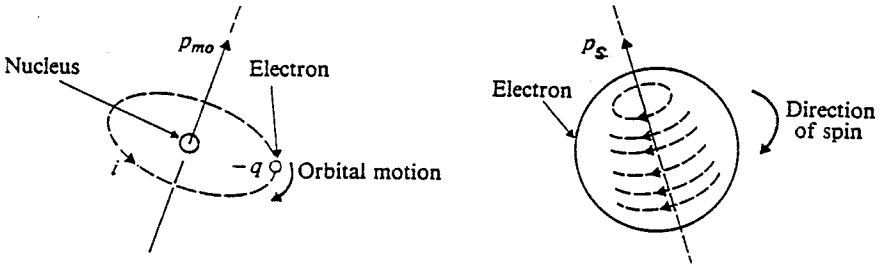


Fig. 2.3 Orbital Motion and Spin of an Electron [3]

This current causes a magnetic field whose direction can be determined by the Right Hand Rule. The generated magnetic field can be represented as the magnetic moment of the electron (ρ_{mo}) along the axis of the orbit. The other magnetic moment of the electron is the one caused by its spin (ρ_s) and is independent of the orbital motion of the electron. The net magnetic moment of an atom is the vectorial sum of these two components and is known as ρ_m. In many nonferromagnetic materials the two components cancel each other out leaving the atom with a zero resultant magnetic moment. In some other nonferromagnetic materials, although individual atoms have a net magnetic moment, the symmetry of the arrangement of atoms is such that the moment of one atom is cancelled out by the moment of an oppositely directed neighbor atom. However, in ferromagnetic materials the natural arrangement of atoms is such that the resultant moments are in parallel and supplement rather than cancel out each other. Therefore within some microscopic region of ferromagnetic elements the magnetic moment of the domain exists and is usually along one of the crystal axes.

If a sample of the ferromagnetic moment is exposed to a magnetic field, the magnetic moment of the different domains will rotate in alignment with the applied field. In other words, the area of the region with the same field direction as the applied field increases . This is known as "domain wall motion". The net magnetic moment of the sample is an indicator of the degree of the atomic moments' alignment.

The nonlinearity of the $\vec{B}$ - $\vec{H}$ curves can now be investigated once more. The rapid rise of magnetic flux density (when $\vec{H}$ is increasing from zero) indicates that atomic moments of nonaligned domains do not need a strong applied field to come into partial alignment with $\vec{H}$. However, further increase of $\vec{H}$ reduces the slope of the curve, which means that fewer magnetic moments still exist to adjust themselves in the field direction. In other words, the domain wall motion is decreased (Fig. 2.2).

The upper portion of the curve indicates that a further increase of the field realigns almost all of the crystal moments and since not many unaligned moments remain, the increase in magnetic flux density is not noticeable and the upper portion of the curve becomes flattened. This flattening of the $\vec{B}$ - $\vec{H}$ curve, which is due to the alignment of the magnetic moments of the ferromagnetic material in $\vec{H}$ direction, is known as "saturation". Saturation is a critical phenomenon that has to be taken care of in the design and modeling of instrument transformers. Although here the $\vec{B}$ - $\vec{H}$ curves of the ferromagnetic elements are being discussed, conclusions can be extended to the flux - exciting current curves. This can be done by linear rescaling of the flux - exciting current curves.

2.3 - Hysteresis Loop in the Steady State

The plot of core flux versus exciting current with ac excitation is called hysteresis loop. In the study of core saturation, hysteresis loop provides information required for understanding core behavior under transient and steady state conditions. In order to deduce a few basic facts which can be used in analyzing transient behavior, steady state excitation will be considered first.

Fig. 2.4 is a typical hysteresis loop which results after a few cycles of sinosoidal excitation.

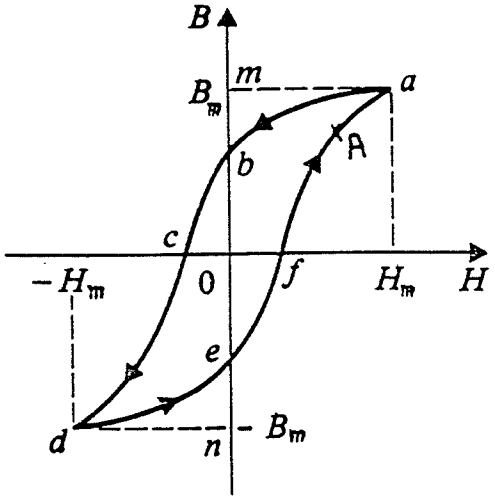


Fig. 2.4 The Steady State Hysteresis Loop [3]

Clearly when $\vec{H}$ increases in segment fa, B also increases. However after reaching the peak excitation at H_m, the magnetizing curve does not return on path fa. Instead, it shapes the path ad which intersects the $\vec{B}$ axis at point b. Portion ob represents the flux density which is reserved in the core due to the alignment of the magnetic moments of the core material. What can be observed here is that application of an exciting current in the reverse direction does not realign all the magnetic moment vectors which are already aligned by an equal excitation of the forward direction. Some of the domains keep their arrangement and these are the ones which produce a magnetic flux ob when $\vec{H}$ is zero. The residual flux is also known as "remanence". To overcome this memory flux density, a negative field of intensity oc has to be applied. In fact the real hysteresis loop lags $\vec{B}$ behind the value of $\vec{H}$ which would be expected if $\vec{B}$ and $\vec{H}$ had a single valued relation. The lagging is called hysteresis.

Under steady state conditions, excitation current (or $\vec{H}$) can be represented by a phasor of constant amplitude. In this case the hysteresis loop repeats itself at each cycle. It will be shown later that the area enclosed by the loop represents the magnetic energy dissipated in the core as heat per cycle per unit of core volume.

2.4 - Transient Behavior of Hysteresis Loop

If a ferromagnetic core is not initially magnetized, then during the first few cycles of oscillation of its exciting current a pattern similar to the one in Fig. 2.5 will result.

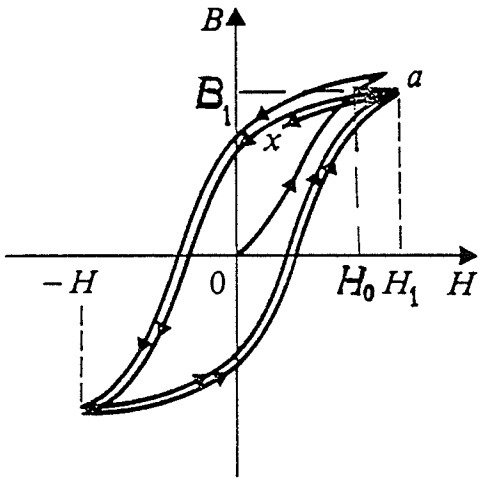


Fig. 2.5 $\vec{B}$ - $\vec{H}$ Curve for $0 \leq t \leq \tau$ [3]

It can be seen that in the beginning a smaller excitation can cause the same flux density that a larger excitation will cause after one cycle. The reason for this difference is that at the beginning of the first cycle magnetic moments which were not aligned before the start of the process become aligned under the field. In the beginning of the second cycle, flux density is zero but $\vec{H}$ has a positive value which represents the corrective force that has to be applied to compensate the negative portion. If the field intensity is increased such that flux reaches the point B_1, H_1 (which generates B_1 in this cycle) can be compared with H_0 (which produced B_1 in the first cycle). From Fig. 2.5 it can be seen that H_1 is bigger than H_0. Based on what was discussed in the previous paragraphs, this is an expected result. During the first quarter of the first cycle, magnetic moments are not aligned in the $\vec{H}$ direction and the applied H_0 arranges them and causes B_1. During the first quarter of the second cycle, some of the core domains which have already kept their $\vec{H}$ alignment are sources of no extra flux density. Therefore to achieve the same B_1, the field intensity has to be increased. That is why H_1 appears to be bigger than H_0.

In steady state the hysteresis loop approaches the closed loop (Fig. 2.4) which is also referred to as the parent loop.

2.5 - Inrush Current

In analyzing the transient behavior of a transformer core sometimes it can be observed that at the instant of energizing the transformer, a large current known as "inrush current" is drawn from the line. On some occasions this current is large enough to cause tripping of the protective relays. The magnitude of the inrush current depends on several factors, among them the energizing instant (closing instant of circuit breakers) , the magnetic alignment of the core and the shape of the hysteresis loop. To calculate the amplitude of inrush current, one can ignore the ohmic resistance of the primary circuit of current transformers. If the primary voltage is a sinosoid, then :

$$V_m \sin \omega t = N \frac{d\varphi}{dt} \qquad 2.5.1$$

where N is the number of coil turns in the primary side , V_m is the maximum primary voltage at fundamental frequency and φ is the core flux.From 2.5.1 φ can be derived as:

$$\varphi(t) = - \frac{V_m}{N \omega} \cos \omega t + \varphi_0 \qquad 2.5.2$$

where φ_0 is the maximum transient magnetic flux and decays with time. However, it will be shown that the magnitude of φ_0 depends on the energizing instant. Assume that a core

is energized at $\omega t = \alpha$ and further assume that at this instant magnetic flux of the core is zero. Then :

$$- \frac{V_m}{N\omega} \cos\alpha + \varphi_0 = 0$$

or :

$$\frac{V_m}{N\omega} \cos\alpha = \varphi_0 \qquad 2.5.3$$

Substituting equation 2.5.3 into equation 2.5.2 leads to :

$$\varphi(t) = \varphi_m (\cos\alpha - \cos\omega t) \qquad 2.5.4$$

where $\varphi_m = \frac{V_m}{N\omega}$ is the maximum amplitude of core flux in steady state. Notice that φ_0 depends on the energizing instant. If the transformer is switched on at $\alpha = \frac{\pi}{2}$, there will be no transient term and only steady state flux appears. This is the best desired condition. However, if the transformer is energized at $\alpha = 0$ then equation 2.5.4 becomes :

$$\varphi(t) = \varphi_m (1 - \cos\omega t) \qquad 2.5.5$$

The maximum core flux occurs at $\omega t = \pi$ and will be :

$$\varphi(t = \frac{\pi}{\omega}) = 2\,\varphi_m \qquad 2.5.6$$

It can be seen that the maximum transient value of flux can be twice as large as its steady state value. This in turn can lead to the saturation of the transformer core. In some cases the transient exciting current is a few hundred times larger than the steady state one. It can be concluded that the inrush current may potentially be up to ten times the nominal transformer current. However, such a situation rarely happens because energization switching is usually done by electric spark when voltage is high $(\alpha \approx \pi/2)$. Therefore magnetic flux does not become doubled. The other reason is that during the time $t = \pi/\omega$ magnetic flux reduces. This reduction is due to the magnetic resistance of the ferromagnetic core and is not taken into account in the above calculation [8].

2.6 - Minor Loops

Up to now steady state excitation current with constant amplitude has been discussed. For this waveform, H_m in Fig. 2.4 represents the maximum field amplitude.

Now, if because of a system distorbance the field intensity does not increase to H_m and starts decreasing at point A on the portion f a of Fig. 2.4, then the resulting loop (which is not a parent loop anymore) will be called the minor loop. A minor loop does not have a defined pattern. Instead, different ferromagnetic elements have different minor loops. The shapes of minor loops are subject to many factors. Among these factors is the magnetic alignment of magnetic moments in a ferromagnetic core at the instant of decreasing of field intensity. Some experimentally recorded minor loops are shown in Fig. 2.6.

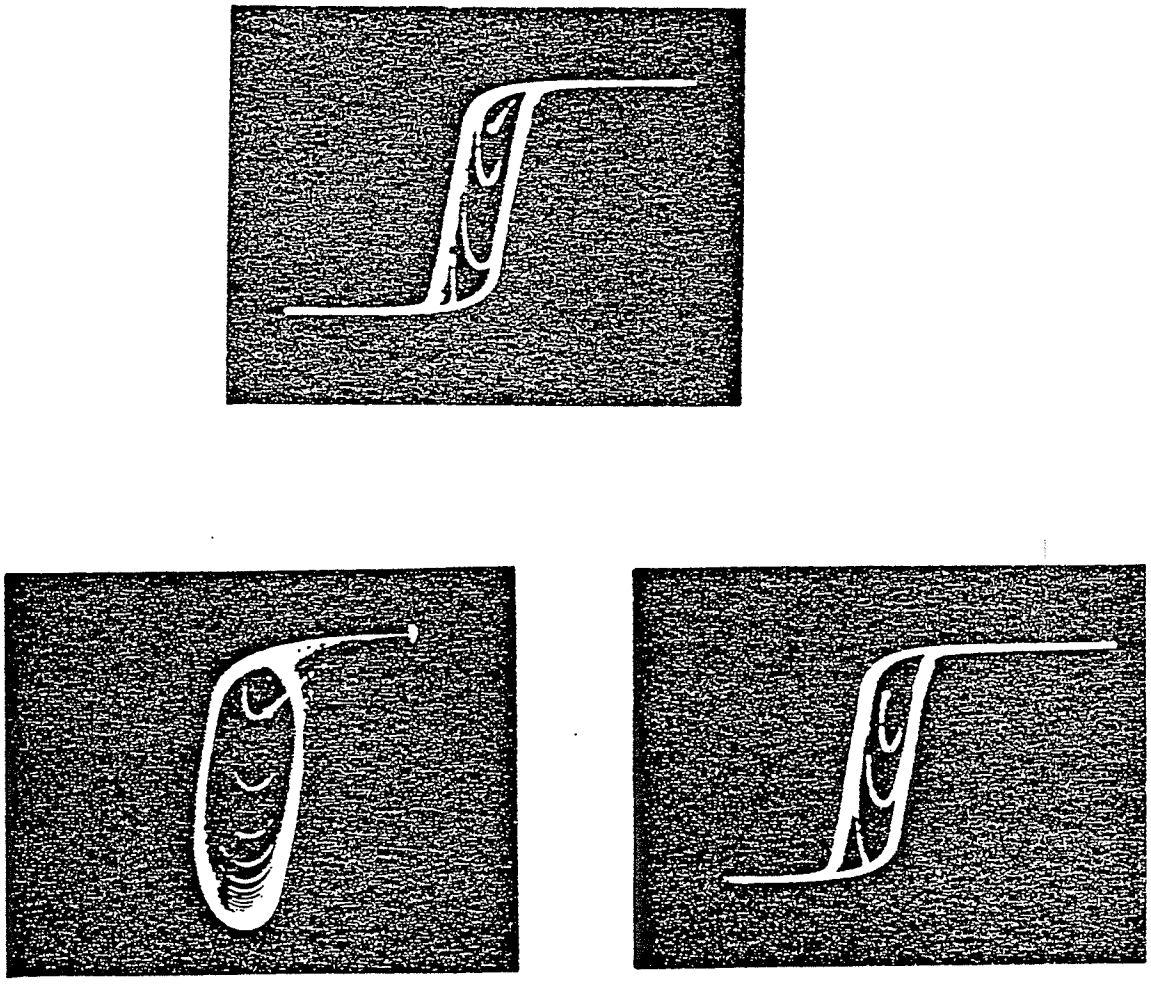


Fig. 2.6 Experimental Minor Loops [9]

2.7 - Hysteresis Loss

Once more, the circuit of Fig. 2.1 will be referred to. This time the coil resistance is modeled as a lumped resistor. If a time varying voltage is applied to the coil terminals, then the total coil linkage flux will be :

$$\lambda = N \times B \times S \qquad 2.7.1$$

where B is the magnitude of flux density, S is the circular cross section of the core and N is the number of coil turns. The induced *emf* in the coil will be :

$$e = \frac{d\lambda}{dt} = N \times S \times \frac{dB}{dt} \qquad 2.7.2$$

Taking coil loss into account, the terminal voltage can be expressed as :

$$v = R \times i + N \times S \times \frac{dB}{dt} \qquad 2.7.3$$

Therefore the instantaneous power due to the exciting current and terminal voltage is :

$$P = v \times i = R \times i^2 + N \times S \times i \times \frac{dB}{dt} = P_{coil} + P_m \qquad 2.7.4$$

P_{coil} is the power loss due to coil resistance. However, P_m is the coil magnetic power loss. Ampere's law for the circuit of Fig. 2.1 indicates that :

$$N \times i = H \times l \qquad 2.7.5$$

Therefore the core magnetic loss becomes :

$$P_m = S \times l \times H \times \frac{dB}{dt} \qquad 2.7.6$$

or in terms of field energy :

$$W_m = \int_0^B S \,.\, l \,.\, H(B') \,.\, dB' \qquad 2.7.7$$

Here H is expressed as a function of B to include the nonlinear hysteresis relation.

Since S . l is the core volume, equation 2.7.7 can be simplified to :

$$w_m = \int_{B1}^{B2} H(B') \,.\, dB' \qquad 2.7.8$$

Equation 2.7.8 shows that magnetic energy per unit volume of core material is the area enclosed by hysteresis loop on the $\vec{B}$ - $\vec{H}$ plane. Fig. 2.4 makes this phenomenon more clear. In this figure, when $\vec{H}$ increases on portion $f\,a$, the positive magnetic energy transferred into the unit volume of the core is the area $f\,a\,B_m\,0$. When $\vec{H}$ decreases to zero on portion $a\,b$, the negative magnetic energy released by the unit volume of the core material is the area $a\,B_m\,b$ .Therefore the net transferred energy is :

$$f\,a\,b\,0 = f\,a\,B_m\,0 - a\,B_m\,b \qquad 2.7.9$$

By the same reasoning it can be shown that the net magnetic energy transferred in one cycle of the oscillation of the exciting current per unit volume of the core material is the area $a\,b\,c\,d\,e\,f$ enclosed by the hysteresis loop. This energy dissipates as heat in the magnetic material and represents the work done per unit volume in reorienting the magnetic moments of the material as it is carried through a cycle of magnetization. The power dissipated in this manner is called the hysteresis loss.

2.8 - Eddy Current Loss

In the previous section it was concluded that the area enclosed by a hysteresis loop represents the hysteresis loss per unit volume of ferromagnetic element per cycle. By increasing the frequency of exciting current it will be observed that the hysteresis loop becomes broader. Fig . 2.7 shows this change .

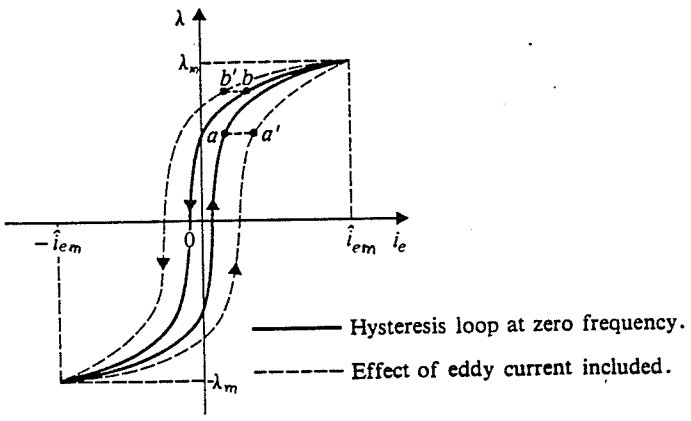


Fig. 2.7 The Eddy Current Effect [3]

The loop shown in full line is obtained by low frequency exciting current and the dashed loop is for the same core when frequency is increased. This effect is due to the induced core current known as "eddy current". When magnetizing current flows through the coil, it induces flux (φ) in the core (Fig. 2.1). Flux is normal to the cross section of the core and in turn induces a *mmf* in any cross section of the core. By Lenz Law this *mmf* tends to generate a current whose direction is such that it opposes the linkage flux. This is called eddy current. For an alternating exciting current, the eddy current is also alternating; and due to a phenomenon known as "magnetic skin effect", as frequency of the applied exciting current increases, the eddy current tends to circulate toward the outer surface of the core . When flux density in the core changes slowly, the induced *mmf* and the eddy current are negligible. However, as Fig. 2.7 indicates, even for the operating 60 Hz frequency they are not very small any more.

To produce a given core flux at each instance, i_e must be increased by an amount necessary to overcome the *mmf* induced by eddy current. That is why a typical point on the increasing portion of the solid loop of Fig. 2.7 (point a) has shifted to point a'. Again, when i_e is decreasing, the induced *mmf* opposes the reduction of core flux. Therefore to produce a desired flux level, i_e has to be reduced by an amount corresponding to the eddy current *mmf*. This is illustrated in Fig. 2.7 by the shift of the typical point b to the point b'.

The eddy current loss together with the hysteresis loss comprise the core losses of transformer. There are approximate formulations describing the variation of each power loss component with respect to the core dimensions. However, the separate evaluation of each loss component is neither possible nor necessary. Instead, manufacturers provide curves which indicate the power loss per kilogram of core material for various values of S, f and B.

CHAPTER 3

MODELING OF INSTRUMENT TRANSFORMERS

MODELING OF INSTRUMENT TRANSFORMERS

In chapter two fundamental electromagnetic principles of operation of instrument transformers were briefly reviewed. For engineering purposes these basics have to be represented by a fairly accurate mathematical model. There is no doubt that a physical device has complexities which are not always very easy to calculate and model. However, by implementing some permissible approximations and assumptions, one can develop a mathematical model whose response to a set of different excitations in the desired range is relatively close to the actual response of the physical device. It has to be noticed that the accuracy of an instrument transformer is somehow related to the specific application of the device. For instance, a current transformer used in conjunction with a meter does not necessarily have to have the same accuracy as a current transformer which feeds a microprocessor controlled relay.

In this chapter modeling of instrument transformers will be reviewed by defining each element in the primary side, the core and the secondary side of the models. The approximations (if any) along with their effect on circuit accuracy will also be explained at each stage.

3.1 - Primary and Secondary Windings

When a coil wound around a ferromagnetic core is excited by a sinosoidal voltage source, an exciting current flows through the coil and induces an *emf* across the winding. This current provides the magnetic field which is required for alignment of the core magnetic moments (Chapter 2). Here the electric fields between the turns of each winding have practically no effect for a wide range of frequencies and can be omitted. The other factor which is sometimes neglected is the distributed ohmic resistance of the primary winding. For some devices like current transformers (CT s) where the primary side has just one or sometimes a few turns and therefore the primary winding is not long, this resistance can be neglected without any sensible effect. However, in other devices like potential transformers (PT s) and capacitive voltage transformers (CVT s) it is advisable to include primary side resistance as a lumped resistor. In a loaded transformer the voltage drop across this resistor is taken into account by the following equation between the terminal voltage and the induced *emf* :

$$V_t = (r_p \times i_p) + e_p \qquad 3.1.1$$

where V_t is the terminal voltage, r_p is primary winding resistance, i_p is primary current and e_p is the induced *emf* in the primary side.

The induced *emf* is caused by the total flux linking the primary winding. However, not all the flux generated by the circuit links the primary winding. Fig. 3.1 shows that a small portion of the flux which is known as leakage flux (φ_l) does not pass through the core. Therefore :

$$\varphi = \varphi_l + \varphi_m \qquad 3.1.2$$

where φ_m is the core flux and φ is the total flux. The leakage flux is modeled as a lumped inductor. Although the leakage circuit includes part of the core ferromagnetic material, it also includes a relatively large air portion. Therefore the magnetic resistance of the circuit is almost constant and saturation of the core portion of the device has no significant effect on the magnetic resistance of the circuit. Therefore the leakage flux in the primary side is proportional to the primary current i_p and can be modeled by a linear inductor L_p, which is known as primary leakage inductance.

The same conclusion can be extended to the secondary side. Again, the core flux induces an *emf* (e_s) across the secondary winding. This *emf* is larger than the voltage drop across the load. The difference is due to the secondary flux leakage and the secondary resistive voltage drop (Fig 3.2).

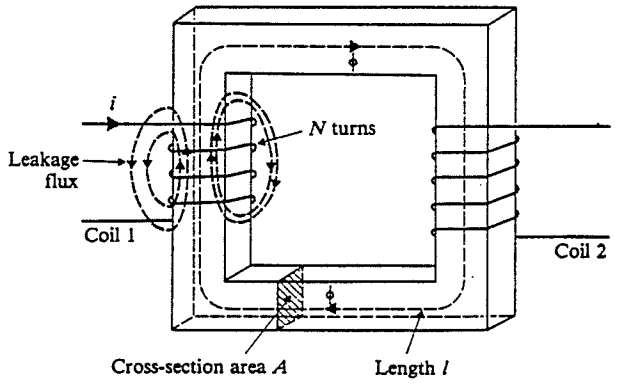


Fig. 3.1 The Leakage Reactance [3]

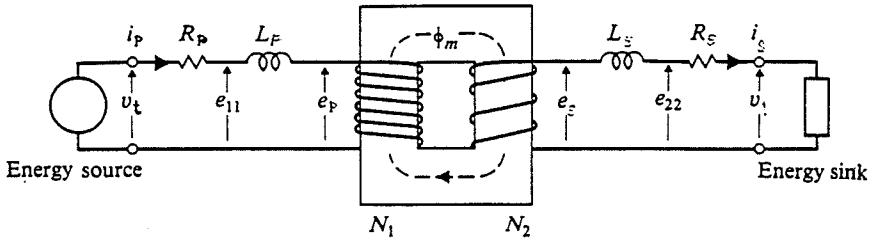


Fig. 3.2 The Transformer Circuit Representation [3]

The circuit equation of Fig. 3.2 is :

$$e_s = r_s i_s + L_s \frac{di_s}{dt} + v_l \qquad 3.1.3$$

Here r_s is the lumped resistor representing the resistance of the secondary winding, i_s is the secondary current, L_s models the small linear inductor standing for the secondary leakage and v_l is the load voltage .

3.2 - Exciting Current in an Unloaded Transformer

The shape of exciting current depends on the variation of core flux $\varphi(t)$ and the electromagnetic properties of the core. Assuming that the magnetizing curve is linear and that $\varphi(t)$ has a sinosoidal waveform defined by :

$$\varphi(t) = \varphi_m \sin \omega t \qquad 3.2.1$$

and also assuming that the core and wire resistive losses are ignored, then the exciting current will be in phase with the flux as follow :

$$i_e(t) = i_{em} \sin \omega t \qquad 3.2.2$$

The core flux induces the *emf* e_p across the primary winding. e_p is defined by Lenz Law to be :

$$e_p = - N \frac{d\varphi}{dt}$$

$$e_p = N \cdot \omega \cdot \varphi_m \sin(\omega t - 90) \qquad 3.2.3$$

Comparing equations 3.2.2 and 3.2.3, it can be observed that because of the 90° phase shift between the voltage and current no real power is drawn from the source and the transformer behaves like a pure inductor. However, the core materials do not have linear magnetizing curves. Instead, factors like saturation and hysteresis losses shape the appearance of magnetizing curves. Under these conditions, a plot of the variation of the exciting current versus time can be drawn point by point using the hysteresis loop and the graph of flux versus time.This method is illustrated in Fig. 3.3.

The resulting steady state magnetizing current is symmetrical with respect to the time axis. Due to the double - valued relation between total flux and exciting current, the former lags the latter. The exciting current is not a pure sinosoid and can be decomposed into a fundamental frequency and its odd harmonics.

Fig. 3.4 shows the fundamental frequency, its third harmonic and the summation of the fundamental and the third harmonic. The last one is closely similar to the waveshape of the steady state exciting current. The fundamental component lags the terminal voltage (and leads the core flux) by less than 90°. Therefore, in the steady state the fundamental component of the exciting current can be decomposed into two components. The one which is in phase with the terminal voltage will be called i_r and the one which is in phase with the total flux will be i_m.

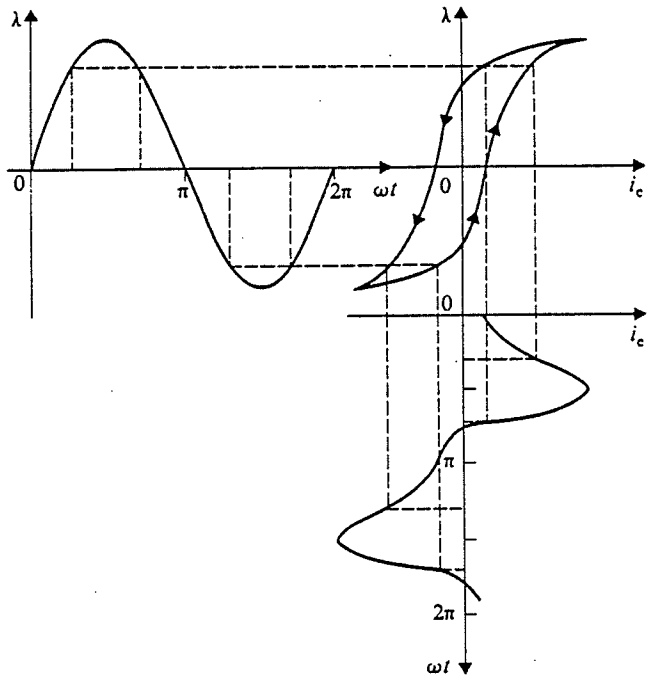


Fig. 3.3 Exciting Current Waveform [3]

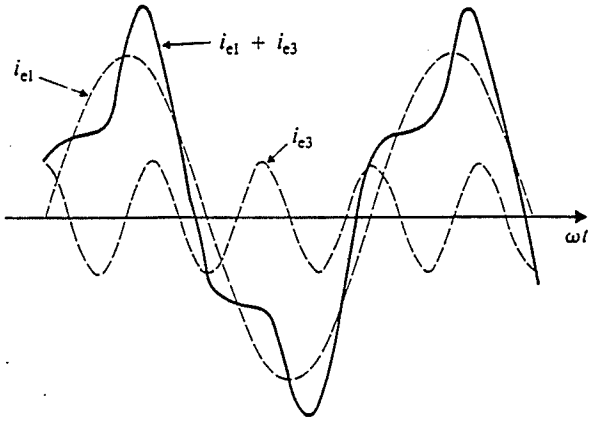


Fig. 3.4 Fundamental and Third Harmonic Components of Exciting Current [3]

The current i_m , which is 90° out of phase with the terminal voltage, does not draw any real power from the source. However, i_r is in phase with the source voltage and for alternating excitation it represents both the hysteresis and eddy current losses. In Fig. 3.4, the exciting current is shown to be approximately the sum of the fundamental frequency and the third harmonic. In general the exciting current can be expressed in terms of its odd frequency components as :

$$i_e = \sum_{n=0}^{\infty} i_{e(2n+1)} = i_{e1} + i_{e3} + i_{e5} + \ldots\ldots \qquad 3.2.4$$

In the steady state when the hysteresis loop does not go into the saturation region, the *rms* values of the higher harmonics are negligible and the exciting current can be approximated by its fundamental frequency component. In this case, a lumped linear resistor models the core losses and a linear inductor in parallel with the loss element simulates magnetizing current. Fig. 3.5 shows that the same argument cannot be extended to the saturation region. When saturation occurs, the *rms* values of the higher harmonics are not negligible any more; on the contrary they become an essential factor in determining the waveshape of the exciting current. Nonlinear resistive and inductive elements have to be implemented in order to model the circuit behavior under this condition. However, in the real devices, the core dimensions and the material are chosen to keep the resistive core loss as low as possible. This means that using the same linear core loss resistor model which was used under steady state conditions will not cause a noticeable error.

The exact characteristic of the nonlinear magnetizing inductor depends on the magnetic behavior of the core material and may differ from one alloy to another. For digital simulation of this nonlinear phenomenon, three different techniques are developed in this thesis. The first one models the nonlinear inductor as a piecewise linear element with two slopes. The second approach simulates the hysteresis loop as piecewise linear parallelograms surrounded by the parent parallelogram. Models of the first and second cases are used in the programming of the CT and will be discussed in more detail in chapter four. The third method is implemented in the programing of the potential devices (PT and CVT) and will be reviewed in chapter five. There the extra current drawn by the saturated core adds to the steady state unsaturated core current.

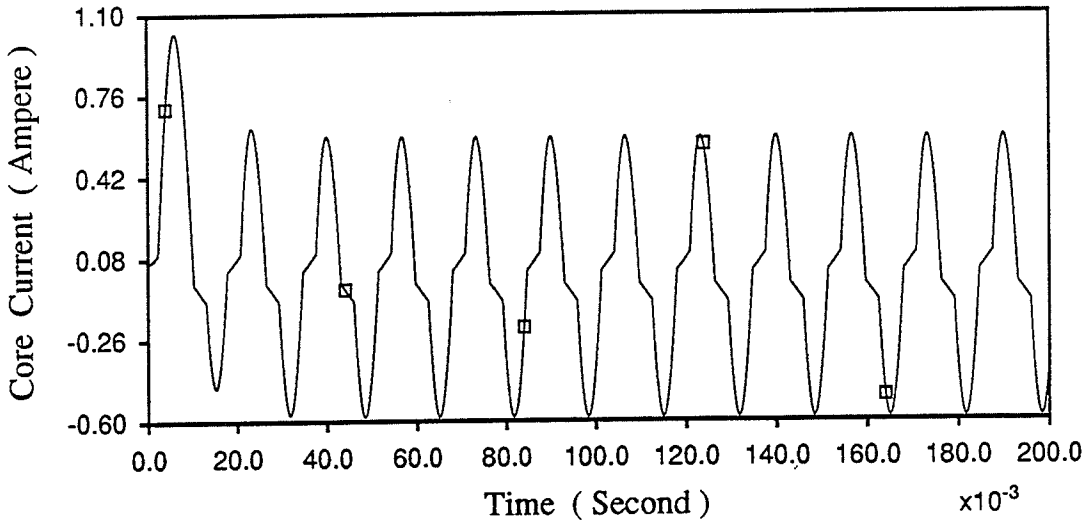


Fig. 3.5 a - Saturated Core Current of the Linearized Model of the Current Transformer

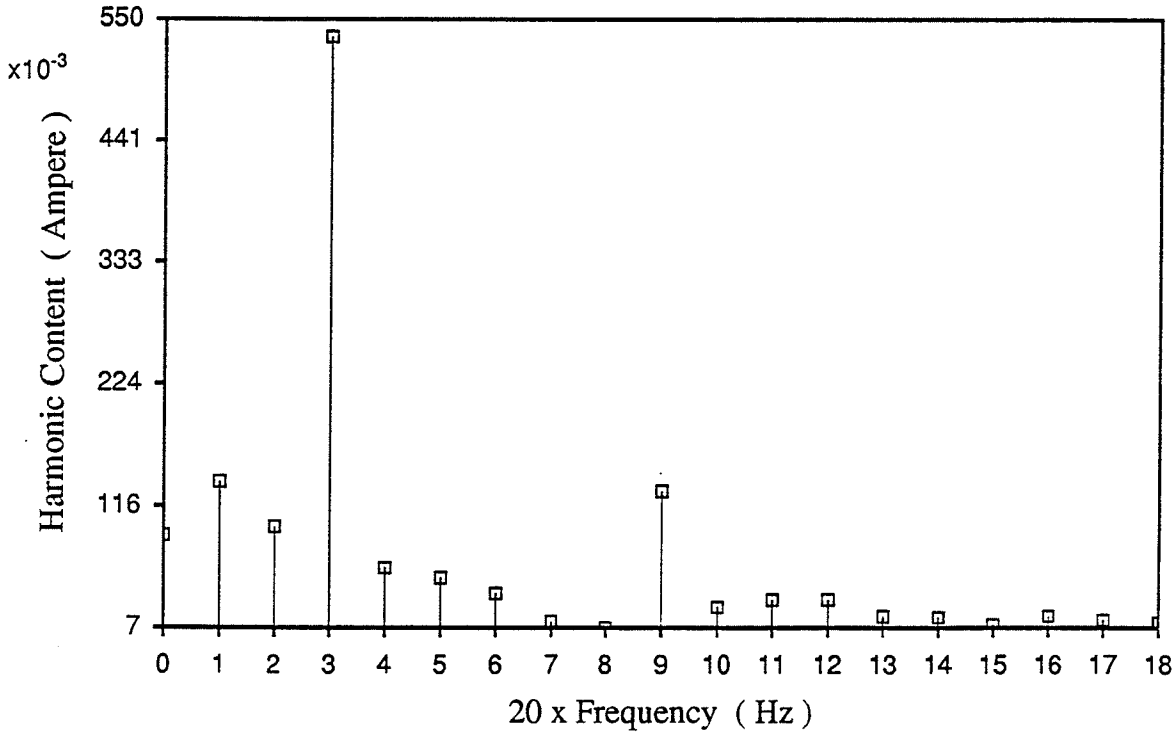


Fig. 3.5 b - Fourier analysis of the first cycle of the core current waveform indicating the presence and relative amplitudes of DC, 20 Hz, 40 Hz and 180 Hz frequency components in the inrush current.

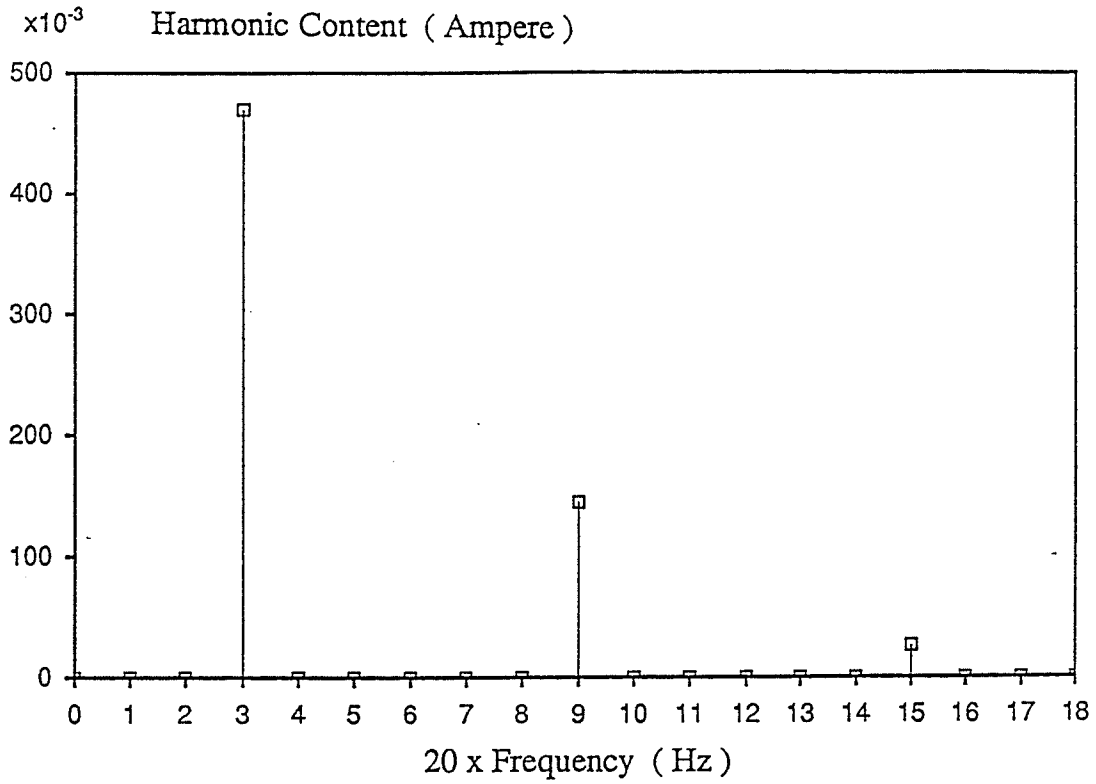


Fig. 3.5 c - Fourier analysis of the tenth cycle of the core current waveform indicating the presence and relative amplitudes of third and fifth harmonics at steady state saturation. DC, 20 Hz and 40 Hz frequency components become negligible as steady state conditions are approached.

CHAPTER 4

MODELING OF CURRENT TRANSFORMERS

MODELING OF CURRENT TRANSFORMERS

The effect of core saturation in the modeling of instrument transformers was discussed in chapter three and it was concluded that in order to model the nonlinear behavior of a core, certain approximations have to be used. In chapter three it was also mentioned that proper core design minimizes the resistive core losses and therefore the error caused by the approximations is negligible. These facts are essential in the modeling of current transformer characteristics within the EMTDC software package. In order to provide the user with a wider range of options and to enrich the saturation library of EMTDC, two different algorithms of simulating current transformers are developed. These two approaches will be referred to throughout the thesis as *case 1* and *case 2* . In *case 1* a piecewise linear inductor in parallel with a constant linear resistor models core saturation. The inductor represents the core magnetizing branch and the resistor simulates the core resistive losses. Other electromagnetic transient programs have used a similar approach to model core saturation of transformers :

" Saturation and magnetizing - current effects are confined to a single nonlinear reactor in the winding 1 circuit . This is internally modeled as a type - 98 pseudo nonlinear reactor (EMTP terminology for nonlinear reactors - Author) , should the saturation characteristic have two or more segments ; for a single segment a simple constant linear inductance element is used in which case the transformer is completely linear . Core losses are confined to the constant linear resistance R_{mag} *which is in parallel with the saturation branch ."* [10]

In *case 2* the linearized model of the flux - current loop simulates core saturation. The area enclosed by the loop represents the core loss per cycle per unit volume of core material. The user can change the resistive core loss by changing the coordinates of the knee point of the hysteresis loop in the data file. Both cases are explained in more detail in this chapter .

Apart from the core parameters, other circuit elements of both cases are identical, and the same Thevenin equivalent circuit supplies primary current for both cases.

4.1 - The Generation Circuit

To be able to observe the response of the CT model, the primary side has to be fed by a transmission line current. The circuit of Fig. 4.1 provides the primary current for both cases. The main idea of using this circuit is to generate and control the current flow in the primary winding of a CT. In order to test the performance of current transformers under different steady state and transient conditions the primary generation circuit has to meet the following conditions :

a) It should be able to reproduce any arbitrary waveshape desired by the user (for instance, superimposed DC on a sinosoid or a decaying sinosoid).

b) It has to be able to generate current waveforms with *rms* values similar to *rms* currents of a typical high voltage transmission line.

c) It has to meet the circuital and monitoring rules governing the EMTDC program. The simple circuit of Fig. 4.1 basically satisfies all the above conditions.

For the benefit of readers who have little experience with EMTDC, the EMTDC terminology which is used in Fig. 4.1 will be explained here. Reference 11 may be consulted for more information in this regard.

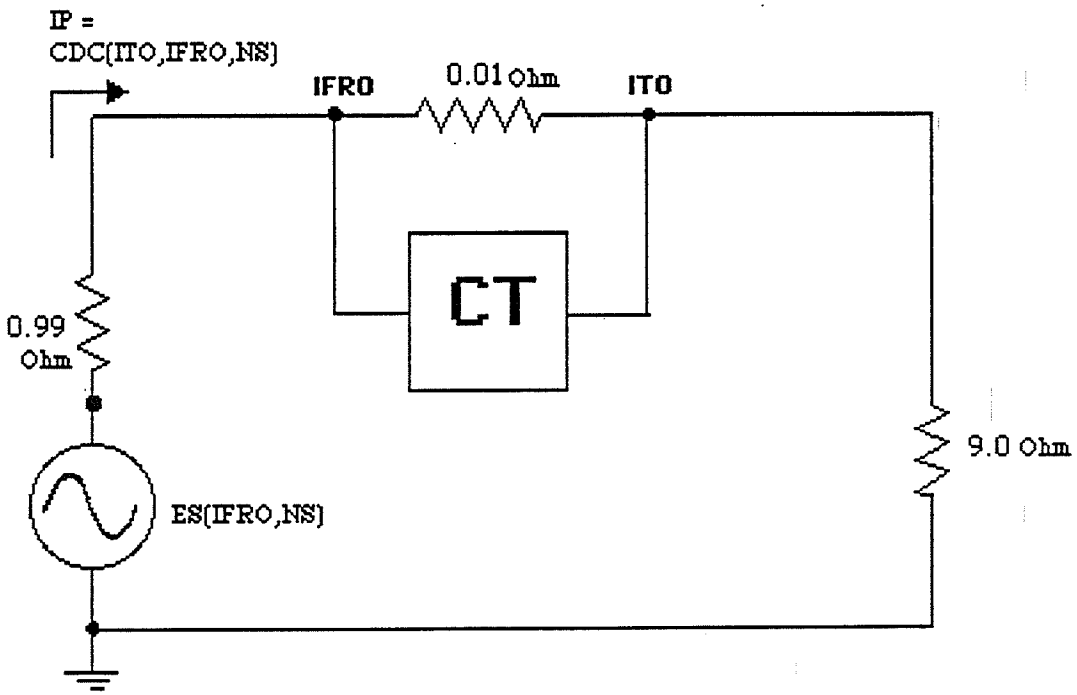


Fig. 4.1 Generating Circuit of Primary Side

ES (IFRO , NS); this pattern is used throughout the EMTDC for a Thevenin voltage source. The source must be connected to node *IFRO* through a Thevenin resistor. *NS* is the number of the subsystem in which *ES* is located. If the circuit consists of only one independent subsystem, then *NS* will be "1" . The waveshape of the voltage *ES(IFRO,NS)* has to be defined by the user in the user - written subroutine DSDYN [11] . The small resistance between the nodes *IFRO* and *ITO* is essential. Theoretically this has to be the resistance of the primary side winding. But practically the primary winding of a physical CT only consists of one (or sometimes a few) turn (s) of the transmission line. Therefore the resistance (and the leakage inductance) of the primary winding is almost zero. However, to be able to monitor the transmission line current, which is named *CDC (ITO,IFRO,NS)*, a small resistor has to be placed between the nodes *IFRO* and *ITO*. This resistor enables the EMTDC main program to keep track of the instantaneous current leaving *IFRO* and entering *ITO*. For these reasons the resistor between the connection nodes has a very small nonzero value of the order of miliohms. Finally, the load resistor between the node *ITO* and ground is chosen to provide a path for the *CDC (ITO,IFRO,NS)* in phase with *ES (IFRO, NS)* . The values of the Thevenin resistor and the load resistor are chosen to make :

$$\text{CDC (ITO,IFRO,NS)} = \frac{\text{ES(IFRO, NS)}}{0.99 + 0.01 + 9.00} = 0.1 \text{ ES(IFRO, NS)} \qquad 4.1.1$$

4.2 - Basic " CT " Model

The circuit of Fig. 4.2 is the basic model of a current transformer with core saturation.The nonlinear core characteristic is shown by the box labelled CORE. The circuit parameters are named in the same order that they are named within the subroutines. For example, variable *VOLT* stands for the induced *emf* across the secondary winding, and *IB* represents the burden current.

Where the primary and the secondary windings have N_1 (usually one) and N_2 turns respectively, the ratio of the former to the latter one is the turns ratio and is defined as :

$$\text{RATIO} = \frac{N_2}{N_1} \qquad 4.2.1$$

Since for all CT s the secondary side has always more turns than the primary side, *RATIO* is a real number greater than one and has to be specified in the data file. The primary current is *CDC(ITO , IFRO, NS)* which is defined in the previous section. The ideal secondary current *ISEC* is defined as :

$$\text{ISEC} = \frac{\text{primary current}}{\text{turns ratio}} = \frac{\text{CDC (ITO,IFRO,NS)}}{\text{RATIO}} \qquad 4.2.2$$

For an ideal transformer whose core draws no current, *ISEC* will be the current that flows into the burden. However, in a real CT the core draws some current. The secondary side refelected core current, which is called *ICORE* , is a nonlinear function of the core-flux (*FLUX*).

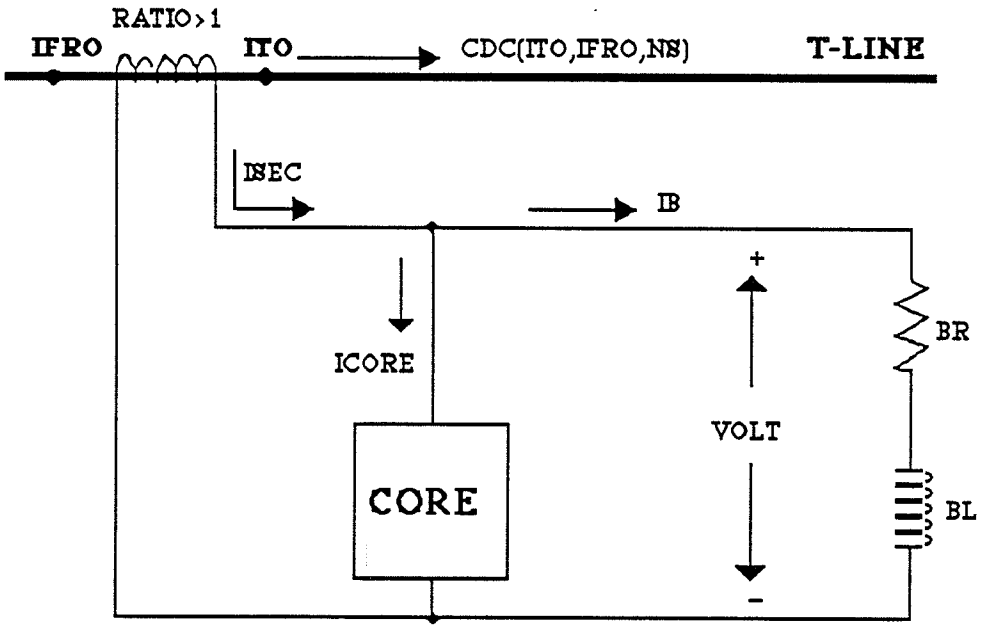


Fig. 4.2 Basic CT Model

If the *emf* of the secondary side is referred to as *VOLT* , then *FLUX* can be expressed as :

$$\text{FLUX}(t) = \int_{t_1}^{t} \text{VOLT}(\tau)\, d\tau + \text{FLUX}(t_1) \qquad 4.2.3$$

If the integration is evaluated over one small time step Δt , then equation 4.2.3 changes to :

$$FLUX(t) = \int_{t-\Delta t}^{t} VOLT(\tau)\, d\tau + FLUX(t - \Delta t) \qquad 4.2.4$$

The variable *DELT* represents the time step increment within the EMTDC program. If DELT is small enough then the trapezoidal rule can be implemented with acceptable accuracy to perform the integration. This method and its effect on modeling of inductors and capacitors is discussed in the next section.

Once the flux is known, the core current can be derived by substituting the flux into the nonlinear relation between *FLUX* and *ICORE* . The user can differentiate between case 1 and case 2 by the algorithm which is used in each case to model the *FLUX* - *ICORE* relation. The flow chart of Fig. 4.3 illustrates the calculation of the core current components for a piecewise linear inductor core model (*case 1*). The core saturation model of *case 2* is explained in the flow chart of Fig. 4.4.

In both cases the burden current *IB* at each instant of time is :

$$IB = ISEC - ICORE \qquad 4.2.5$$

The burden current flows into the secondary winding and through the burden. The secondary resistance and leakage inductance are taken to be lumped elements in series with the resistance and inductance of the burden. It will be an acceptable approach to model the secondary and the burden resistances as a single resistor *BR* and the secondary and the burden inductances as a single inductor *BL*. This assumption leads to the definition of the secondary *emf* (*VOLT*) as :

$$VOLT = IB \times BR + BL \times \frac{dIB}{dt} \qquad 4.2.6$$

4.3 - Modeling of Lumped Inductors and Capacitors

The method of representing lumped inductors and capacitors in EMTDC is illustrated in Fig. 4.5.

Here the active circuit element is replaced by a passive resistor in parallel with a current source [11]. The method will be explained for an inductor, and conclusions can be extended for modeling of capacitors.

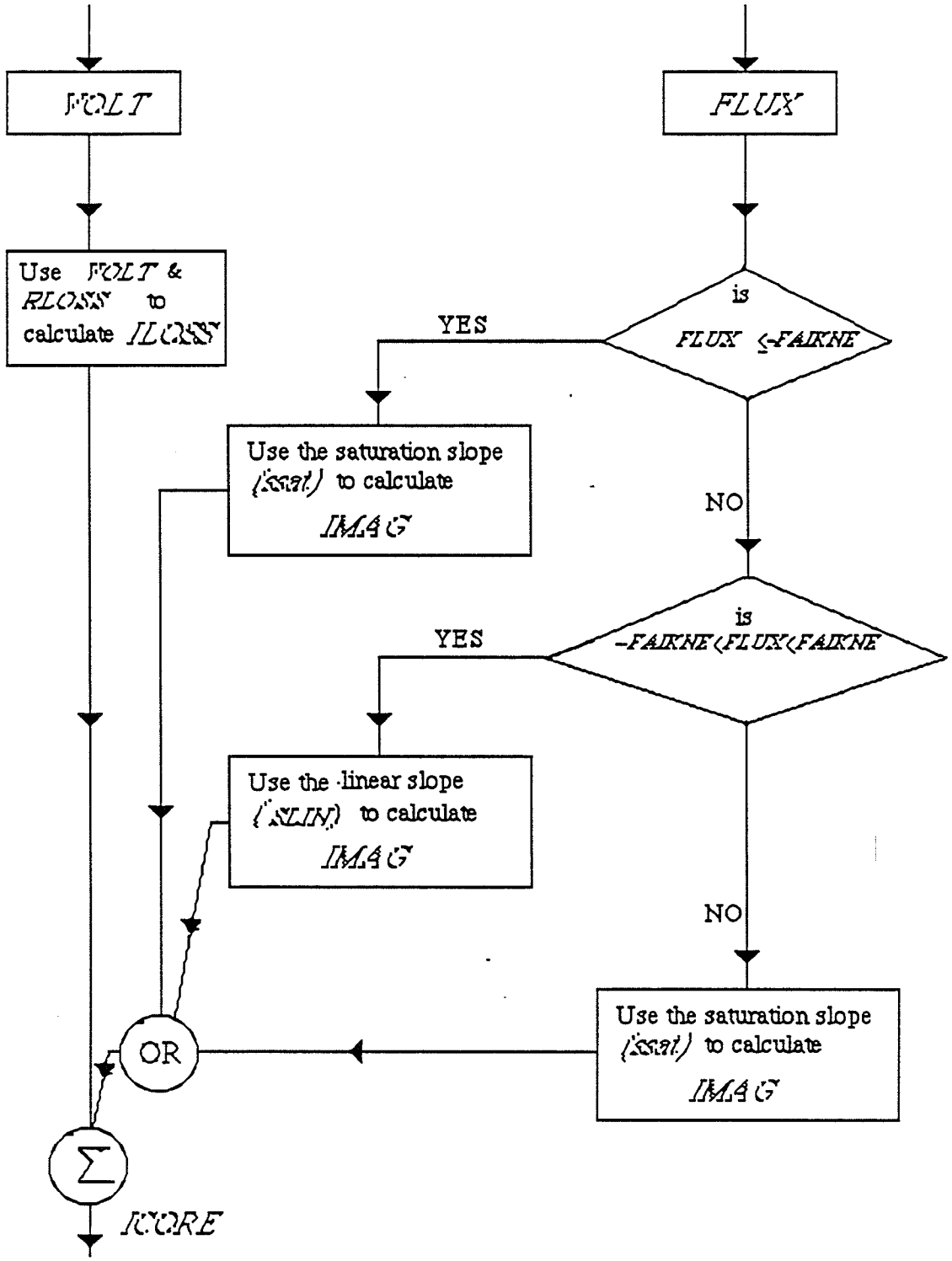


Fig. 4.3 Components of Core Current in the Model of Case 1
(Piecewise Linear Inductor)

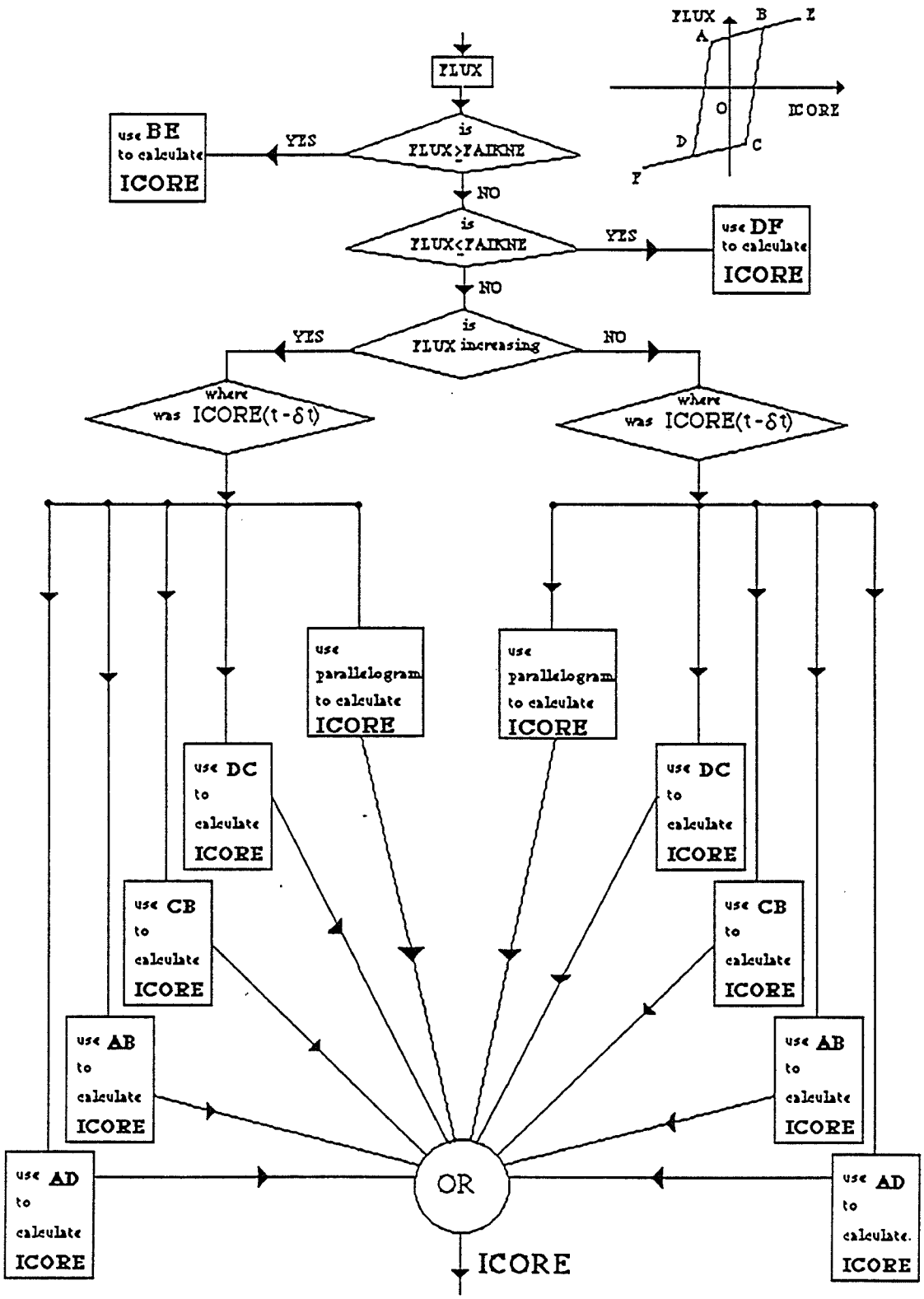


Fig. 4.4 Components of Core Current in the Model of Case 2
(Linearized Flux - Current Loop)

Inductor L of Fig. 4.5 is excited by the current $IB(t)$ and has the following circuit equation :

$$VC(t) = e_k(t) - e_m(t) = L\frac{d[IB(t)]}{dt} \qquad 4.3.1$$

where $VC(t)$ is the voltage drop across the terminals of the inductor. The integral form of equation 4.3.1 is :

$$IB(t) = \frac{1}{L}\int_{t_1}^{t} VC(\tau)\, d\tau + IB(t_1) \qquad 4.3.2$$

The digital computer is not able to produce a continuous history of a transient waveform but rather a sequence of snapshot pictures at discrete intervals Δt. Such discretization causes truncation errors which can lead to numerical instability. Because of this, the trapezoidal rule was chosen for integrating the ordinary differential equations of lumped inductors and capacitors. It is simple, numerically stable and accurate enough for practical proposes [2].

If the integral is evaluated over one time step, then IB(t) will be :

$$IB(t) = \frac{1}{L}\int_{t-\Delta t}^{t} VC(\tau)\, d\tau + IB(t-\Delta t) \qquad 4.3.3$$

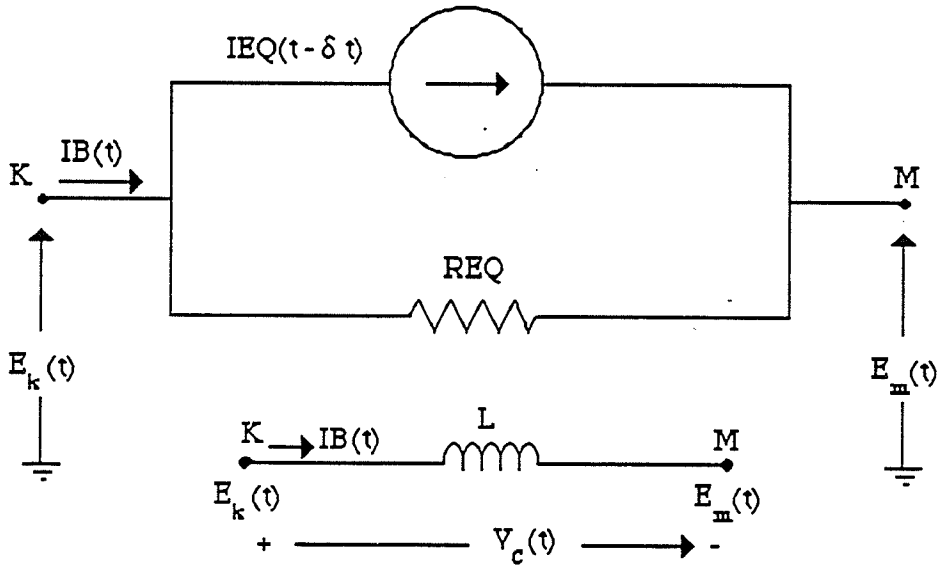


Fig. 4.5 The Equivalent Circuit of an Inductor

For a small time interval Δt, the integral of equation 4.3.3 can be evaluated by the trapezoidal rule :

$$\int_{t-\Delta t}^{t} VC(\tau)\, d\tau = \left[\frac{VC(t) + VC(t-\Delta t)}{2}\right]\Delta t \qquad 4.3.4$$

Substituting 4.3.4 into 4.3.3 leads to :

$$IB(t) = \frac{\Delta t}{2L} VC(t) + \left[\frac{\Delta t}{2L} VC(t-\Delta t) + IB(t-\Delta t)\right] \qquad 4.3.5$$

At this point the equivalent resistance of an inductor is defined to be :

$$REQ = \frac{2L}{\Delta t} \qquad 4.3.6$$

In equation 4.3.5, the terms inside the bracket belong to the previous time step. Therefore they can be replaced by a history term defined as :

$$IEQ(t-\Delta t) = \frac{VC(t-\Delta t)}{REQ} + IB(t-\Delta t) \qquad 4.3.7$$

The right hand side of the equation 4.3.7 has the dimensions of current. Therefore the inductor current of equation 4.3.5 can be formulated as the sum of two current components. The first component is the sum of all current elements of the previous time step, and the second one is based on the present time data.

$$IB(t) = \frac{VC(t)}{REQ} + IEQ(t-\Delta t) \qquad 4.3.8$$

The same approach can be used to define current flow through a capacitor. The only difference is that here the capacitor current will be :

$$IB(t) = C\frac{d[VC(t)]}{dt}$$

Therefore the equivalent resistance of capacitor becomes :

$$REQ = \frac{\Delta t}{2C} \qquad 4.3.9$$

and the history term becomes :

$$IEQ(t-\Delta t) = \frac{VC(t-\Delta t)}{REQ} - IB(t-\Delta t) \qquad 4.3.10$$

Equation 4.3.8, which defines the two components of the burden current, is valid for both capacitors and inductors.

In summary , equations 4.3.6 , 4.3.7 and 4.3.8 define the inductor parameters, and equations 4.3.8 , 4.3.9 and 4.3.10 are used to model capacitors.

The theoretical basis of this modeling method was first described in 1969 by Dommel [2]. Having substituted the inductors and capacitors of each subsystem by their equivalent resistive branches, Dommel developed a simple algorithm for computer solution of the circuit nodal equations in their matrix form. The resultant conductance matrix is a system of algebraic equations that describes the state of the system at time t :

$$[G] \times [V] = [I]$$

and from this the node voltage matrix is calculated as :

$$[V] = [G]^{-1} \times [I] \qquad 4.3.11$$

Each element of the column matrix [I] is the sum of all the current sources connected to a node. This includes the history current source of inductors and capacitors (if any) defined by equations 4.3.7 and 4.3.10.

The conductance matrix [G] is a square matrix whose size depends on the number of the nodes in the subsystem. Since the time step is fixed during a computer run, the elements of the [G] matrix do not change unless switching takes place. In this case the new [G] matrix will be inverted and the state variable, which is the column matrix [V], can be calculated.

The modeling criterion proposed by Dommel is used in the EMTDC program . This approach enables the user to start from any nonzero initial conditions (snapshots), it is flexible toward any voltage or current excitation waveform, and it may include nonlinearities and switchings during the transient state.

4.4 - The Modified CT Model

In section 4.3, the theoretical basis of the equivalent resistive model of inductors and capacitors was discussed. It was observed that the proposed models facilitate the solution of the state variable column matrix by arranging the conductance matrix.

In the circuit of Fig. 4.6, which represents the current transformer of either case,

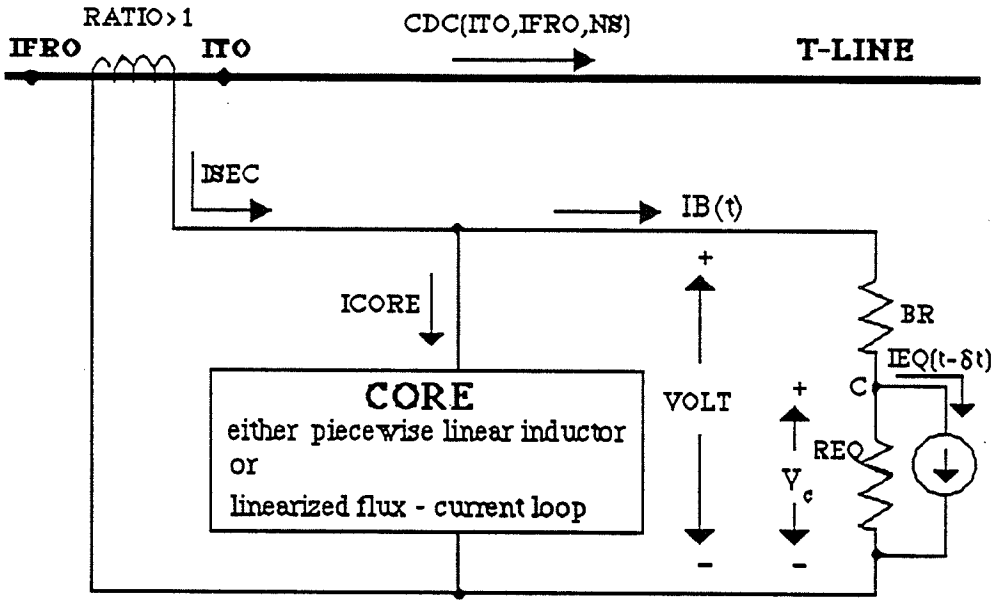


Fig. 4.6 Equivalent Inductor in the Basic CT Model

the inductor *BL* is replaced by its equivalent resistor :

$$REQ = \frac{2\,BL}{DELT} \qquad 4.4.1$$

and the current source which represents the history term is defined at the previous time step as :

$$IEQ = \frac{VC}{REQ} + IB \qquad 4.4.2$$

where the inductor voltage *VC* is :

$$VC = VOLT - (IB \times BR) \qquad 4.4.3$$

The circuit of Fig. 4.6 which represents both cases 1 and 2 (linearized hysteresis loop & piecewise linear inductor) was run on digital computer. It was observed that for very small values of *BL* (in the range of microhenrys) or for *BL* equal to zero, the program works properly. However, when *BL* is in the milihenry range, numerical instability occurs. In EMTDC this type of instability is usually observed when in a specific subsystem there is only an inductor between a node and ground.

One known technique to stabilize the circuit is paralleling a stabilizing resistor *R* with the equivalent resistor of *BL* . A properly selected *R* improves the circuit response

and prevents numerical overflows. But this fictitious resistor draws a certain amount of current which is equal to :

$$\frac{VC}{R}$$

Unless this current is somehow compensated, the current through *REQ* is not the same current that used to flow in *REQ* before the addition of *R*. Therefore a compensating current of magnitude VC / R should be inserted into the connection node to provide *R* with its desired current without violating the Kirchhoff's Current Law. In this way, the stabilizing resistor prevents numerical instability without modifying the current through *REQ*. The circuit of Fig. 4.7 shows the new configuration.

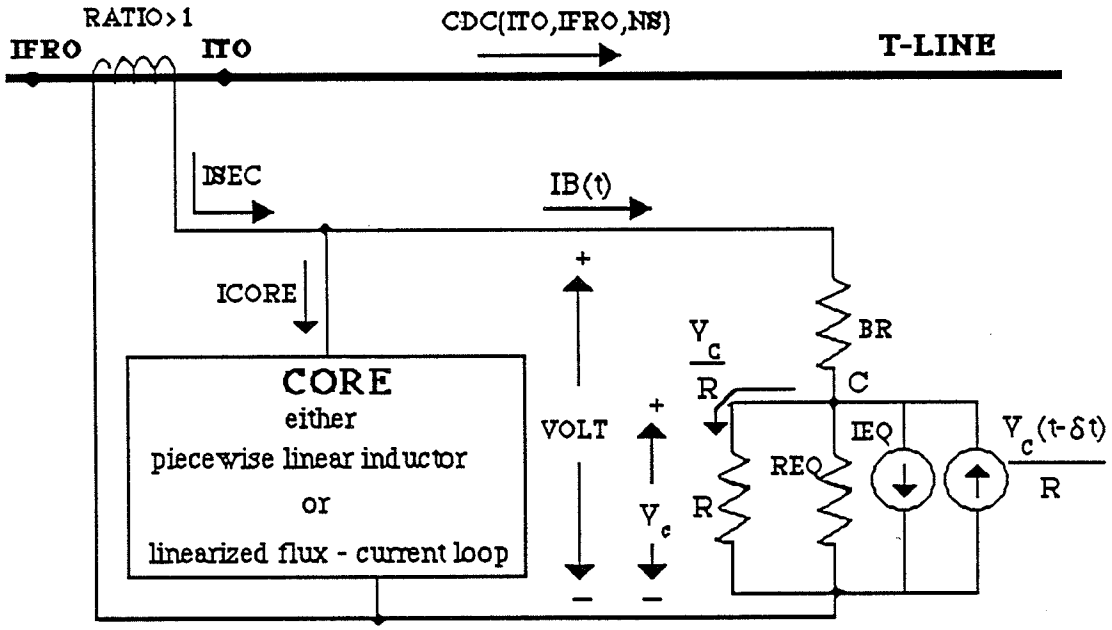


Fig. 4.7 Compensating Current and Stabilizing Resistor

The induced *emf* across the secondary winding for this circuit will be :

$$VOLT(t) = IB(t) \times BR + \frac{R \times REQ}{R+REQ} \times \left[IB(t) + \frac{VC(t-\Delta t)}{R} - IEQ(t-\Delta t) \right] \qquad 4.4.4$$

Fig. 4.8 illustrates the electrical equivalent circuit for *case 1*.

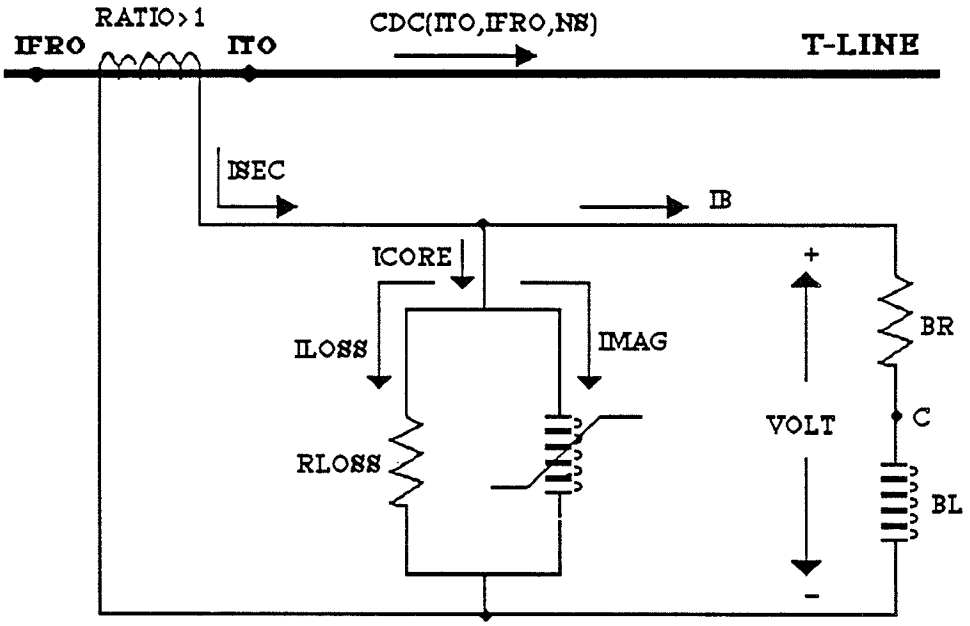


Fig. 4.8 Basic CT Model of Case 1

The stabilizing resistor and compensating current source are not shown here. Fig. 4.9 shows the similar circuit for *case 2* , which is based on the flux - current loop approach. The flow chart of Fig. 4.10 lays out the basic algorithm used in the programming of*case 2*.

The computer printouts for different excitations of both cases are included in appendix 1.

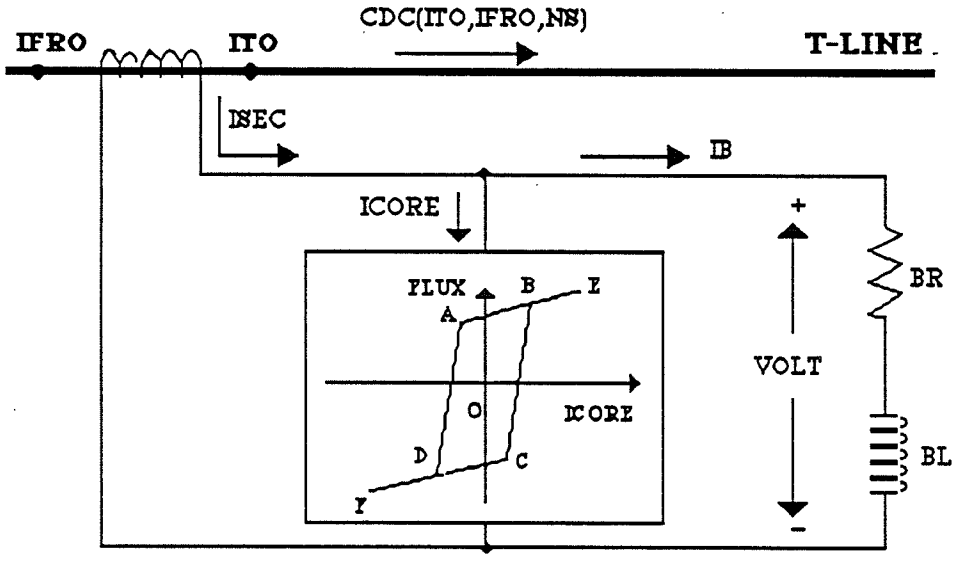


Fig. 4.9 Basic CT Model of Case 2

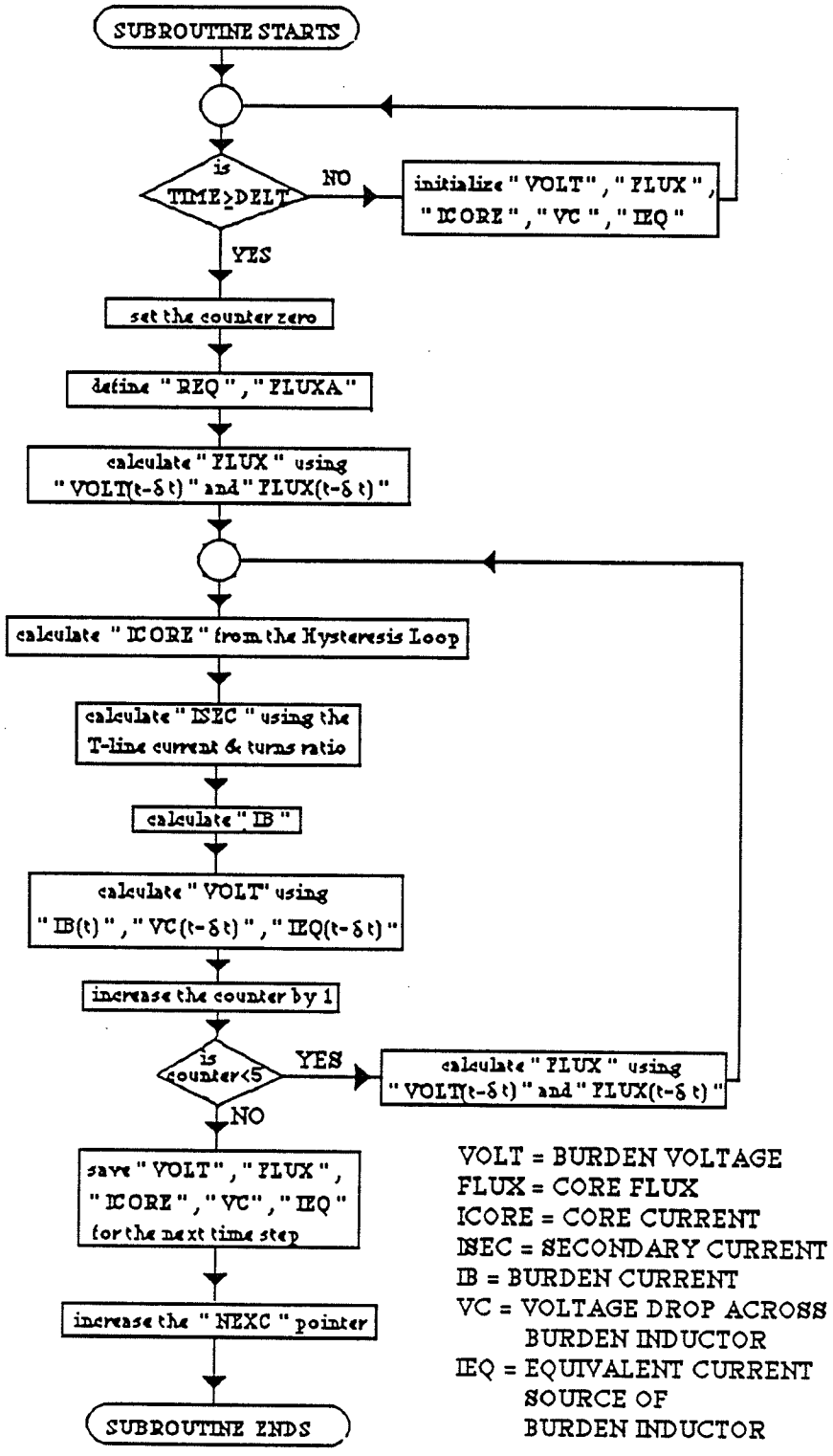


Fig. 4.10 Flow Chart of the Subroutine CT9 (Case 2)

4.5 - Conclusions

In this chapter, core saturation of current transformers is modeled in two different ways and the responses of both models are compared to those obtained from the similar models in literature [6]. The comparison indicates that both models are capable of reproducing the transient and steady state responses of current transformers. The simulation printouts are accurate enough to be compared to the experimental cases [9].

Figs. 4.11 a and b are the steady state simulation of the flux - current loop by the model of case 1 (piecewise linear inductor) and the model of case 2 (linearized flux - current loop) respectively. Figs. 4.11 c and d [6] represent the work already done in this area. Although Figs. 4.11 a and c are very similar, one has to notice that the developed model of case 1 does not cause any change of system admittance matrix. This means that the inductance of the magnetizing branch does not appear in the matrix, and therefore when the core goes to saturation, the system admittance matrix remains intact. As a result no matrix inversion would be required and computer processing time would be saved.

Fig. 4.11 d shows the deficiencies of the existing linearized model [6]. It can be seen that moving from the saturation slope to the linear one is delayed by one time step. This appears as overshoots in the flux - current loop. The developed model of case 2 overcomes this problem and as Fig. 4.11 b shows the overshoots do not exist here.

The other feature of case 2 is the way that it simulates minor loops. As Fig. 4.12 a indicates, minor loops are represented by interior parallelograms. Fig. 4.12 b illustrates minor loops simulated by the model of case 1 for the same excitation. The excitation current, core current and burden current of case 2 are shown in Fig. 4.13. The effect of the core current on the burden current especially during the first cycle is noticeable. Neither of the two models contributes to the expansion of the system admittance matrix.

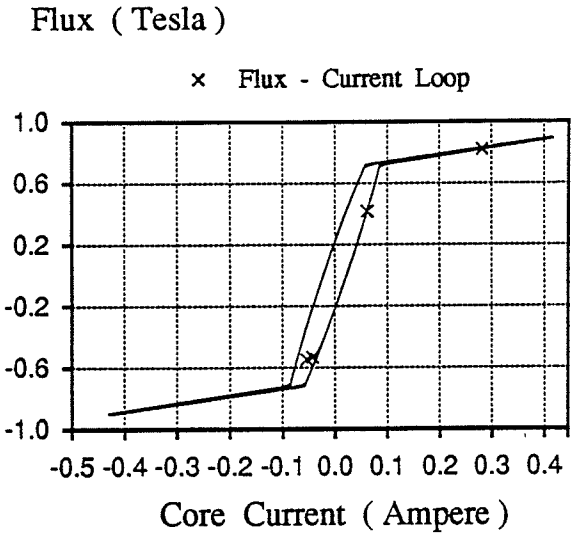


Fig. 4.11 a
Piecewise Linear Model - Case 1

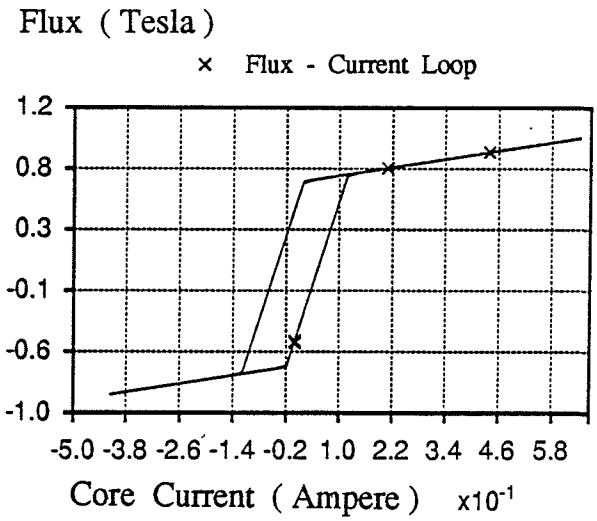


Fig. 4.11 b
Linearized Model - Case 2

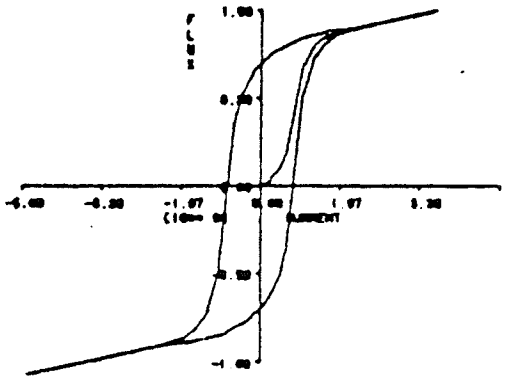


Fig. 4.11 c

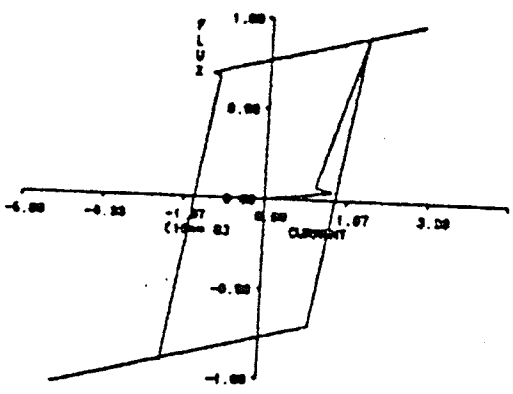


Fig. 4.11 d

Figs. 4.11 c and 4.11 d - Existing Core Models [6]

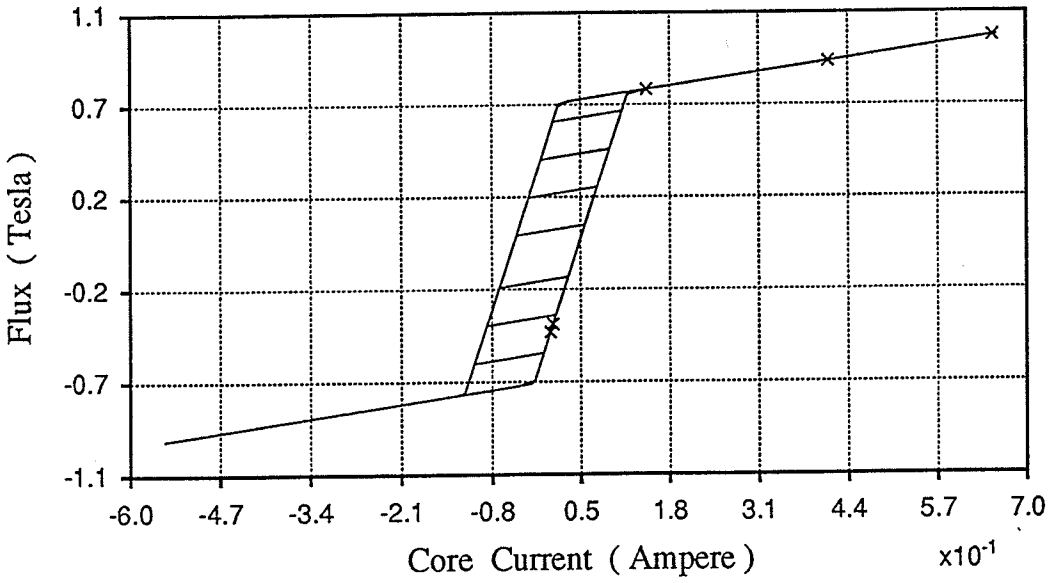


Fig. 4.12 a Flux - Current Loop Modeled by Case 2

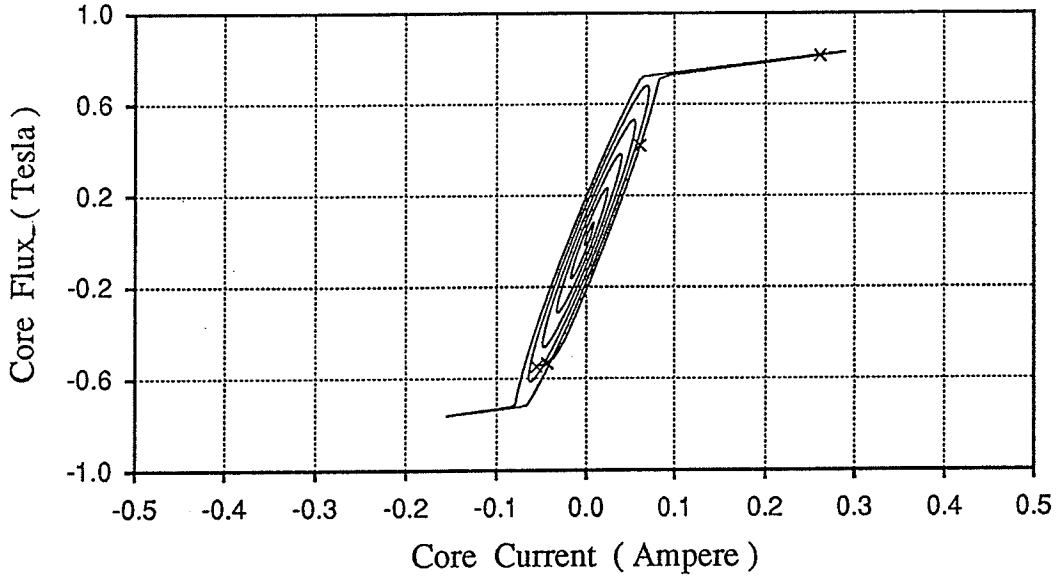


Fig. 4.12 b Flux - Current Loop Modeled by Case 1

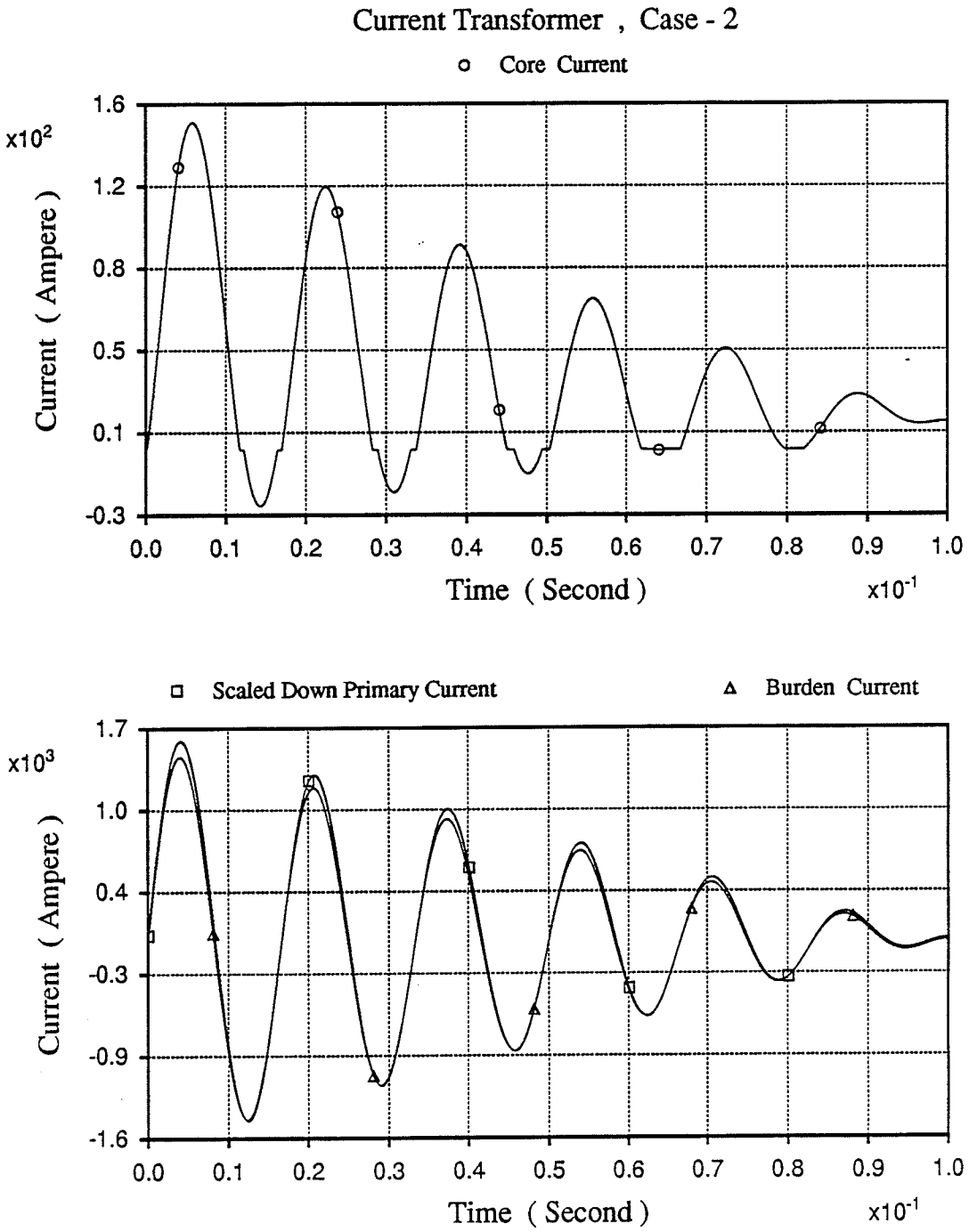


Fig. 4.13 - CT Currents

The linearized core model of case 2 is compared to a nonlinear core model created by Dr. Rohan J. Lucas from the University of Maratova , Sri - Lanka [16]. Dr. Lucas was working on a similar project at the University of Manitoba from September 1989 till September 1990. Figs. 4.14 a, b and c show the steady state results of the nonlinear model developed by Dr. Lucas. Figs. 4.15 a, b and c illustrate the response of the linearized model to the same excitation. The scaling of these two sets are arbitrarily choosen and are not based on the real core saturation data.

The flux - current loops of Figs. 4.14 c and 4.15 c are very similar in the linear and saturation portions. However, the two loops are slightly different in the knee portion. The difference is caused by the linearization of knee portion in the model of case 2.

The linearization effect can be observed by comparing the core current waveforms. In Fig. 4.14 b, the transfer from the unsaturated core current to the saturated one occursin a smoth manner. The core current of the linearized model (Fig. 4.15 b) does not show the same smothness. However, the difference is such small that it does not affect the burden current. Figs. 4.14 b and 4.15b show that the two models develop similar burden currents for the same core flux.

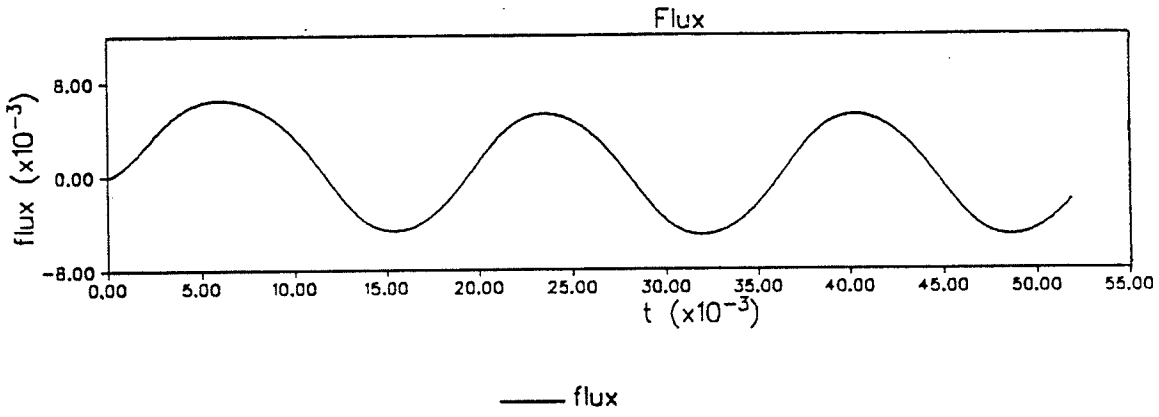


Fig. 4.14 a

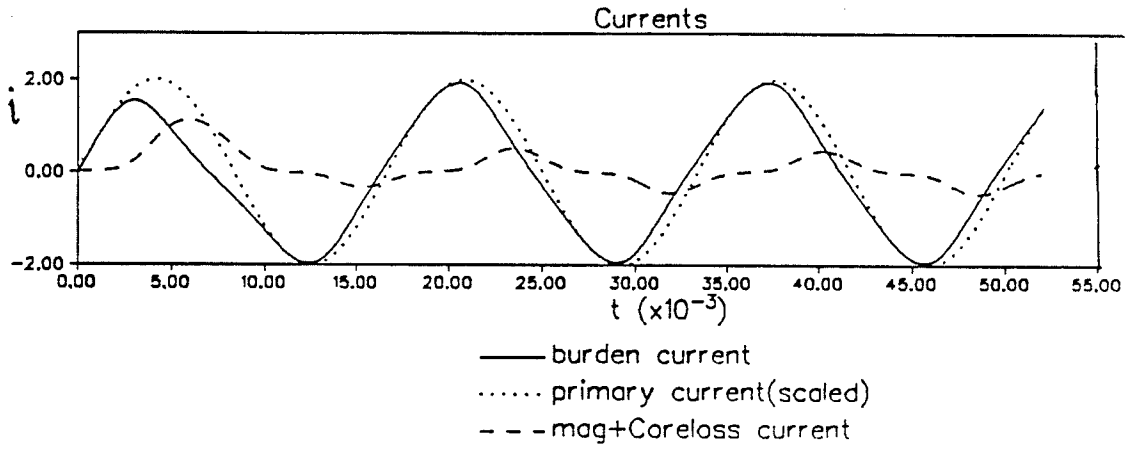


Fig. 4.14 b

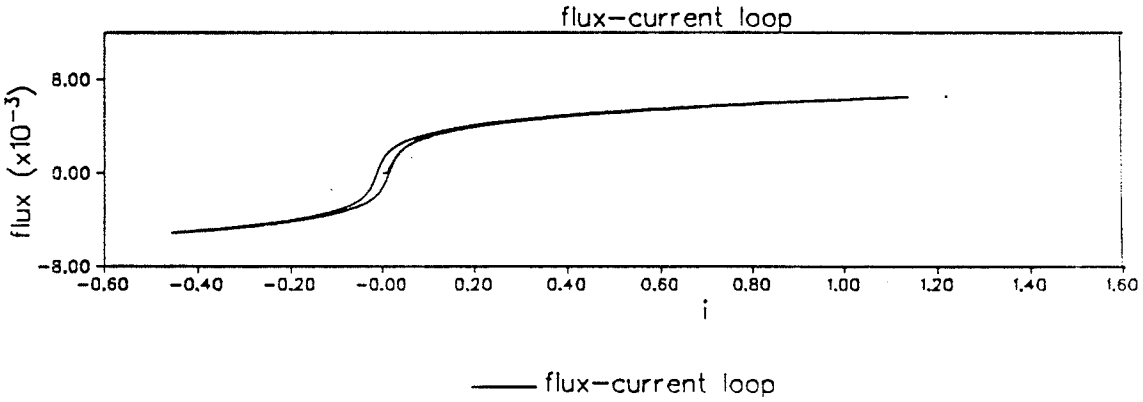


Fig. 4.14 c

Fig. 4. 14 - The steady state simulation of the saturated core of a current transformer. The nonlinear core model.

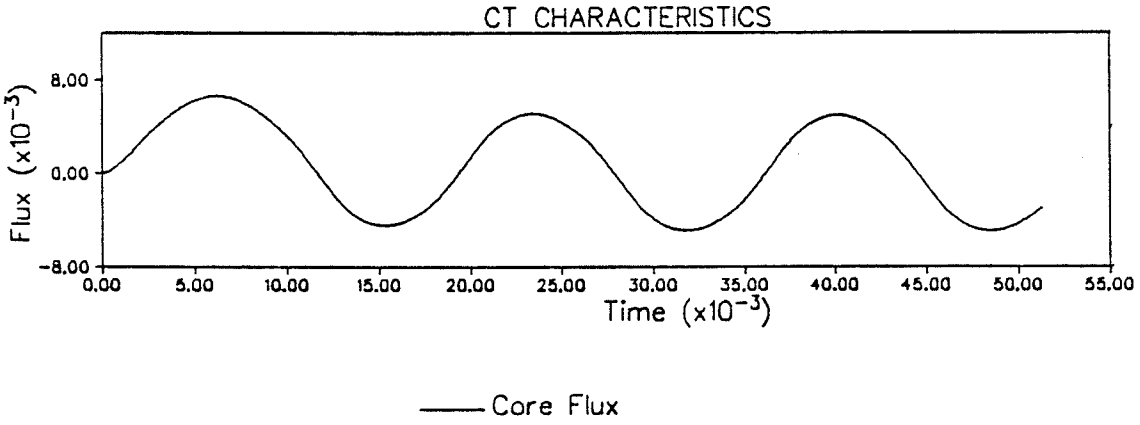


Fig. 4.15 a

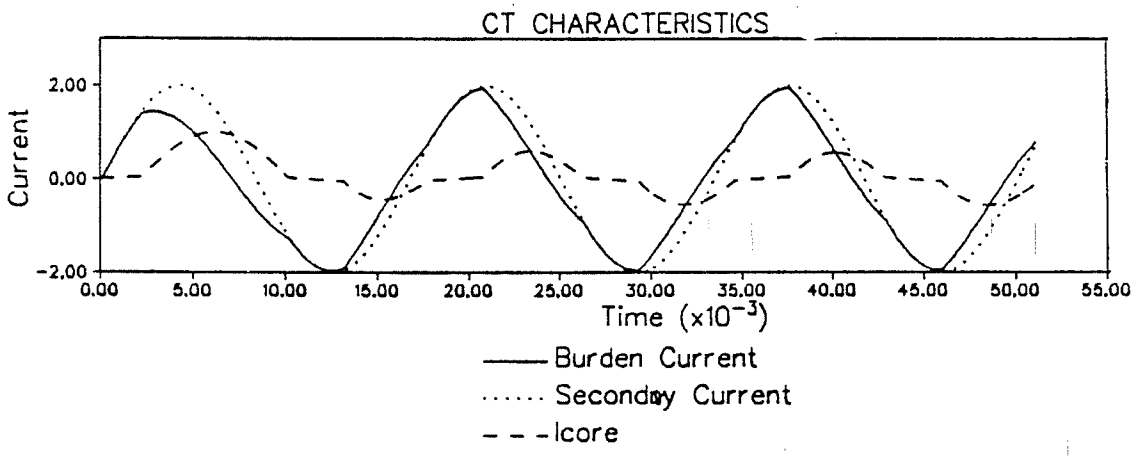


Fig. 4.15 b

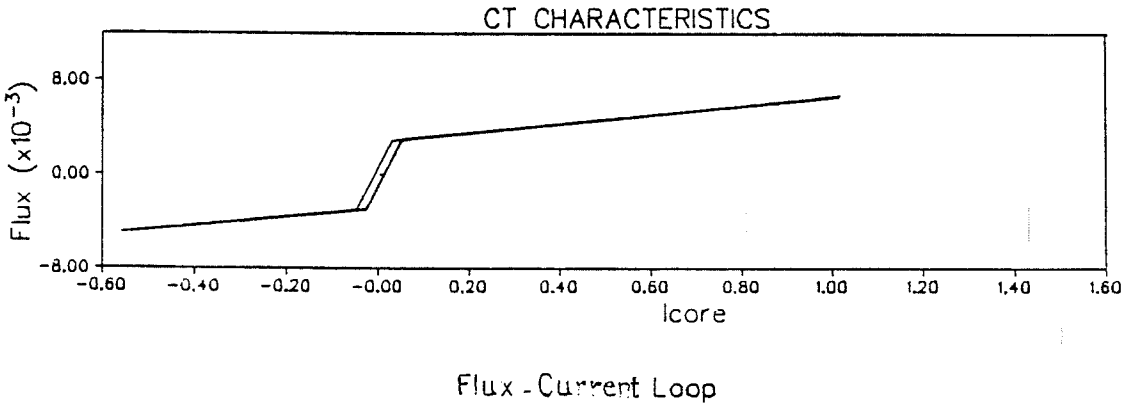
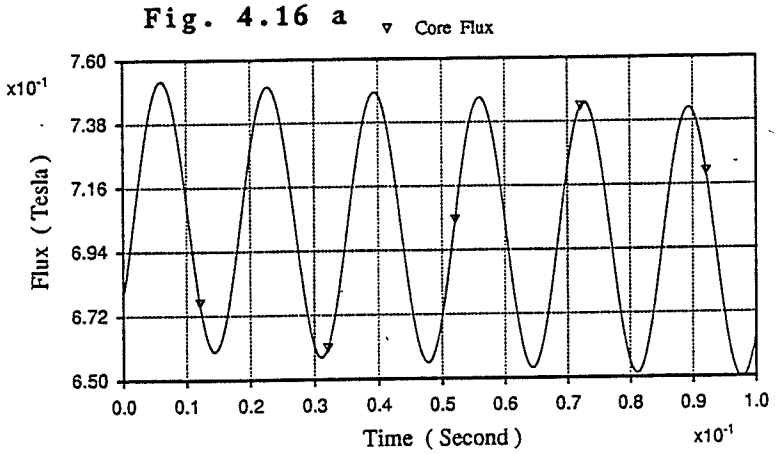
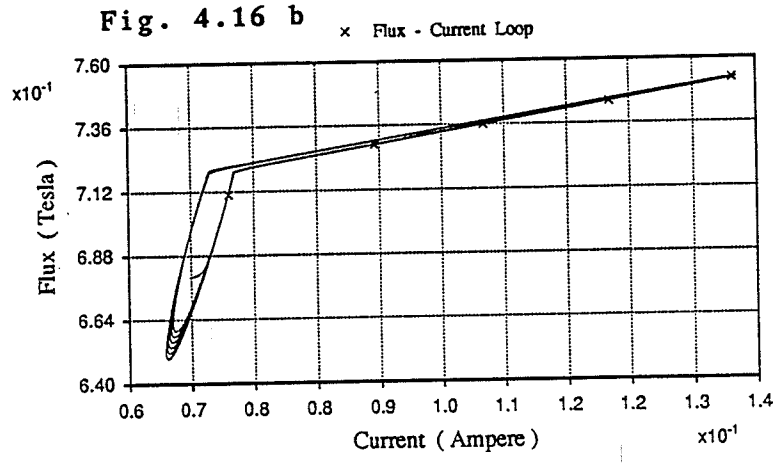


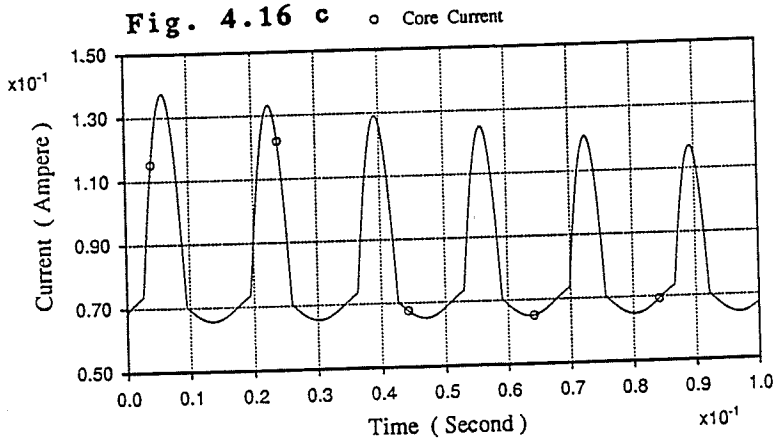
Fig. 4.15 c

Fig. 4. 15 - The steady state simulation of the saturated core of a current transformer. The linearized core model ofcase 2.

In Fig. 4. 16 model of case 1 simulates remanence by starting from a nonzero initial core flux.The distortion of core current and flux - current loop due to the residual core flux is shown in Figs. 4.16 a, 4.16 b and 4.16 c.







Figs. 4.16 a, 4.16 b and 4.16 c Simulation of Rrmanence (Case 1)

At the end of this section, the width of the flux - current loop is reduced by decreasing eddy current. The reduction of the width can be observed by comparing the flux - current loops of Figs. 4.17 a and 4.17 b.

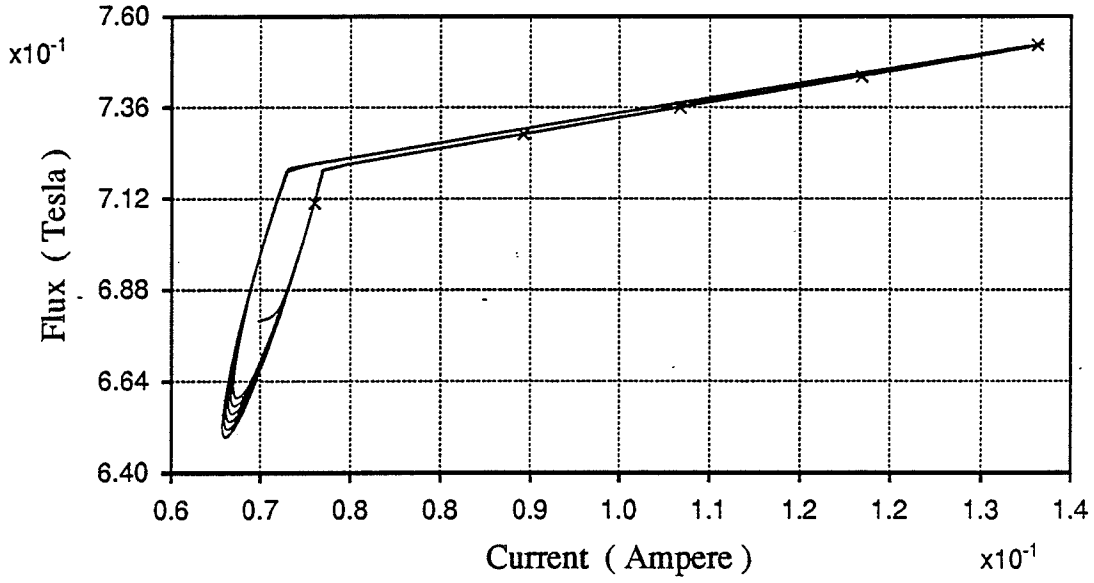


Fig. 4.17 a Flux - Current Loop with High Eddy Current Loss

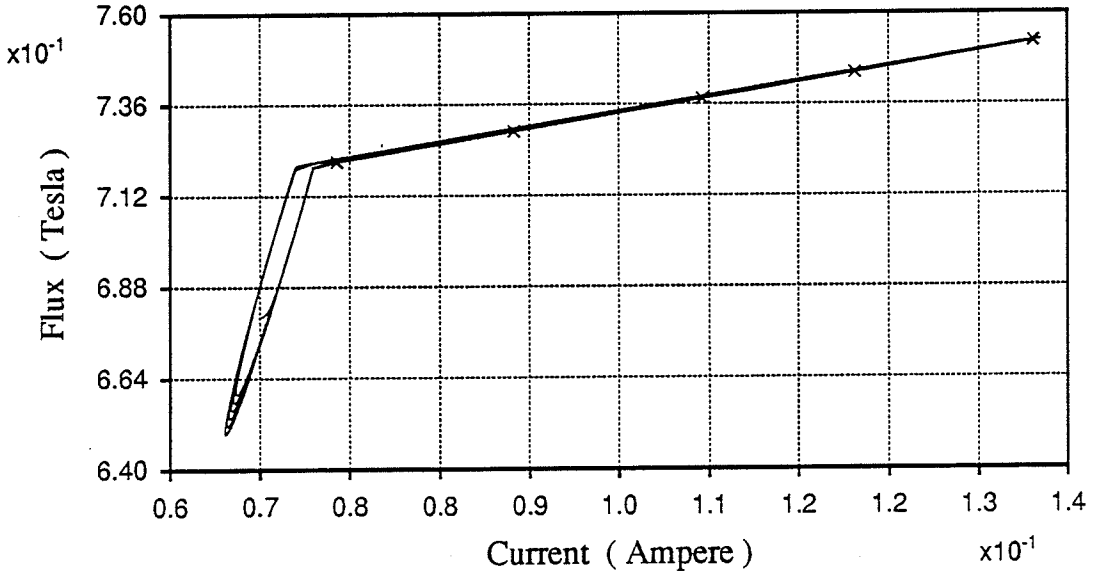


Fig. 4.17 b Flux - Current Loop with Low Eddy Current Loss

CHAPTER 5

MODELING OF POTENTIAL TRANSFORMERS

MODELING OF POTENTIAL TRANSFORMERS

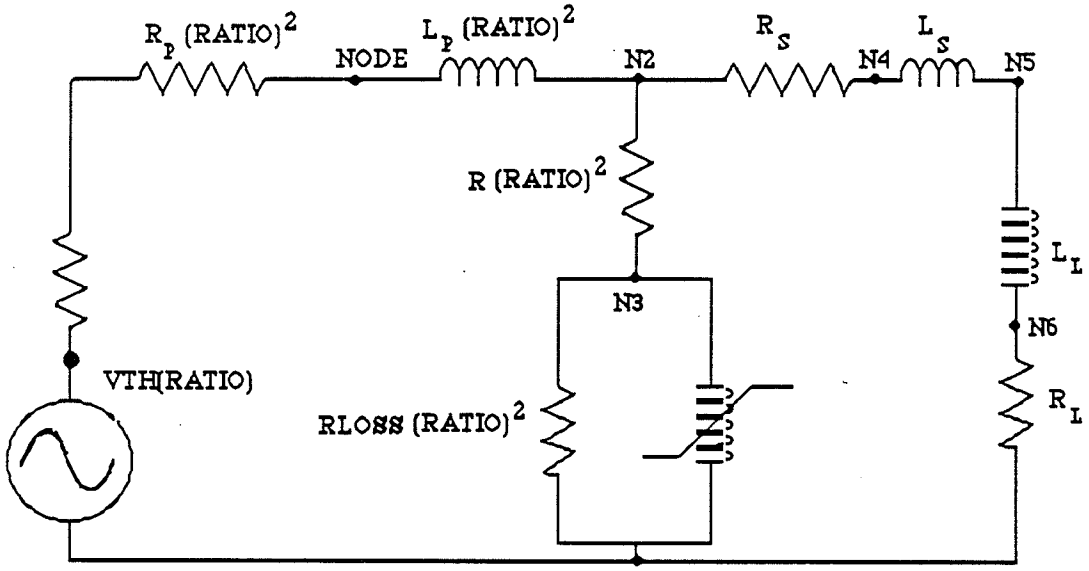
In chapter four, modeling of current transformers was discussed and two different methods for modeling of core saturation were presented. These models are not confined to current transformers and can be easily adapted in any subroutine which includes core nonlinearities. With potential transformers (PT s) core saturation is not a determining factor because one is dealing with high primary voltages and large core and load impedances which basically confine the core current to very low ranges. However, saturation should not be completely ignored since it can contribute to the random phenomenon of ferromagnetism [5].

In the modeling of potential transformers, the core saturation and both the resistive and the inductive components of the core current are included. However, to confirm the previous work done on saturation, neither one of the CT saturation models is implemented here. Instead a new approach is developed. This approach will be discussed in section 5.2.

One major difference between the models of potential and current transformers is that in the latter case all the device elements (like core inductance and winding resistances) are defined within the subroutine and the datafile merely includes the circuit which generates the primary current. However, the lumped circuit elements of the potential transformer are all placed in the datafile.

5.1 - The Exact PT Model

To simulate potential transformers, the well known model of Fig. 5.1 is used.



$$RATIO = \frac{\#\ of\ secondary\ turns}{\#\ of\ primary\ turns} < 1$$

Fig. 5.1 The Equivalent Circuit of Potential Transformer Referred to Secondary Side

Here the phase to ground generation voltage is represented by its Thevenin equivalent circuit. Because of practical considerations which will be discussed later in this chapter, the whole equivalent circuit of Fig. 5.1 is referred to the low voltage secondary side and therefore all the primary side parameters are scaled down. The high tension side includes the core resistance and inductance. In the primary side of Fig. 5.1 there is also a small resistance R which does not exist in the real equivalent circuit. This resistor is negligible compared to the core resistor and is placed for monitoring the core current. It has to be noticed that EMTDC at this stage of its programing is not capable of monitoring the current passing through the parallel branches. Without R the core current which crosses the parallel core elements cannot be directly measured . However, the current that passes through R is basically the same as the core current and if R is small enough it does not cause any significant error. R_p , R_s , L_p and L_s are the resistance and inductance of the primary and the secondary side respectively. Numerical instability caused by the inversion

of the conductance matrix can be avoided if none of these parameters are zero in the data file. The load of the potential transformer is usually a very high impedance resistive component (a meter, for instance) and is modeled as resistive and inductive elements R_l and L_l in series. It is this highly resistive load which causes the secondary current to be small.

The same device can be modeled by transferring all the circuit elements to the high voltage primary side, and theoretically both circuits would have the same response. However, from a practical point of view, the secondary side referred circuit has some advantages over the primary side referred model. In order to understand the advantages of the model referred to the low tension side, one has to review the method of solving electrical circuits using EMTDC. This is briefly explained in section three of chapter four. As mentioned there, the main program replaces an inductor (and a capacitor) with its equivalent resistive model, which is a current source in parallel to a resistor. The obtained resistive network is solved for the node voltages by arranging the conductance matrix and inverting it :

$$[G][V] = [I]$$

$$[V] = [G]^{-1}[I] \qquad 4.3.11$$

It is at this stage that numerical errors sometimes occur. A typical error will be illustrated by an example :

It is assumed that a potential transformer converts 120 kV ac phase to ground voltage to 120 V ac (therefore the turns ratio is 1000). Further, the load and core resistances are assumed to be 10 MΩ each. If the circuit elements are referred to the primary side, then the load resistance will appear to be :

$$10\ M\Omega \times (1000)^2 = 10^{12}\Omega$$

or the load conductance will be 10^{-12} mho. This figure appears in the circuit conductance matrix and since it is very close to zero may be taken as zero by the computer. This, in turn causes division by zero during the inversion of the conductance matrix.

In the same example, if all the circuit elements are referred to the low voltage side, the load resistance remains 10 MΩ and the core resistance reduces to :

$$10\ M\Omega \times (1000)^{-2} = 10\ \Omega$$

Therefore no division by zero occurs and the circuit remains stable.

5.2 - Core Saturation

Potential transformers are designed to handle high potentials. For the 120 kV line of the example of the previous section and under steady state conditions, the secondary current does not exceed a few centiamperes. The order of magnitude of core current is even smaller. It is so small that even if core goes to saturation, it can hardly affect the load current (since PT is a potential driven instrument, the core rarely saturates). That is why the load voltage does not change noticeably when the core is forced to saturate.

In chapter four two different models were developed for core saturation. The first one was based on the linearized flux - current loop and the second one used a piecewise linear inductor in parallel to a loss resistor. The piecewise linear inductor of the second model was defined within the subroutine (and not in the data file) and was replaced by a saturation inductance in the same subroutine without using any switching.

The core inductance of the potential transformer is defined as a linear unsaturated inductor in the datafile. To avoid switching and probable numerical instabilities caused by it, this inductance never changes in the datafile. Instead, whenever the core flux exceeds the knee point flux (defined in the subroutine as FAIKNE), an extra current proportional to the saturated slope of the magnetizing curve will be injected into the core and will be added to the core current. Under normal unsaturated conditions, this current source is zero, and the only magnetizing current is the one which is drawn by the unsaturated inductance. This model was first suggested in reference 7.

5.3 - The PT Algorithm

The FORTRAN subroutine which models the potential transformer is called PT2 where 2 stands for the number of the STOR array locations occupied by the subroutine (to know more about the STOR array see reference 11). The argument of the subroutine consists of the following parameters :

NODE : The connection node of the bus and the potential transformer
NS : The subsystem number (subsystems are also defined in reference 11)
RLOSS : The core resistance seen from the high voltage side
SLIN : The linear portion of the core inductance seen from the high voltage side
SSAT : The saturated portion of the core inductance
CURKNE : The knee point magnetizing current. If this parameter is set negative, then saturation will be neglected

FLUX0 : The initial core flux at time zero

PN : Number of the primary side turns

SN : Number of the secondary side turns.

The flow chart of this program is shown in Fig. 5.2 . The parameters of Fig. 5.2 are defined as :

TIME : The current time

DELT : The time increment

FAIKNE : The knee point flux

DIF : The saturation current pumped into the core

VTH : The Thevenin voltage source referred to the secondary side

EMFP : The primary side induced *emf*

FLUX : The core flux

CURKNE : The knee point current

CORCRN : The core current

EDICRN : The current crossing the core resistance

EXICRN : The excitation current

EMFS : The secondary side induced *emf*

VBURDN : The load voltage (burden voltage)

BRDCRN : The load current

Appendix 2 includes typical data files of the model of potential transformers. There are also two sets of computer printouts. The first set is the output of an unsaturated core and the second set takes core saturation into account.

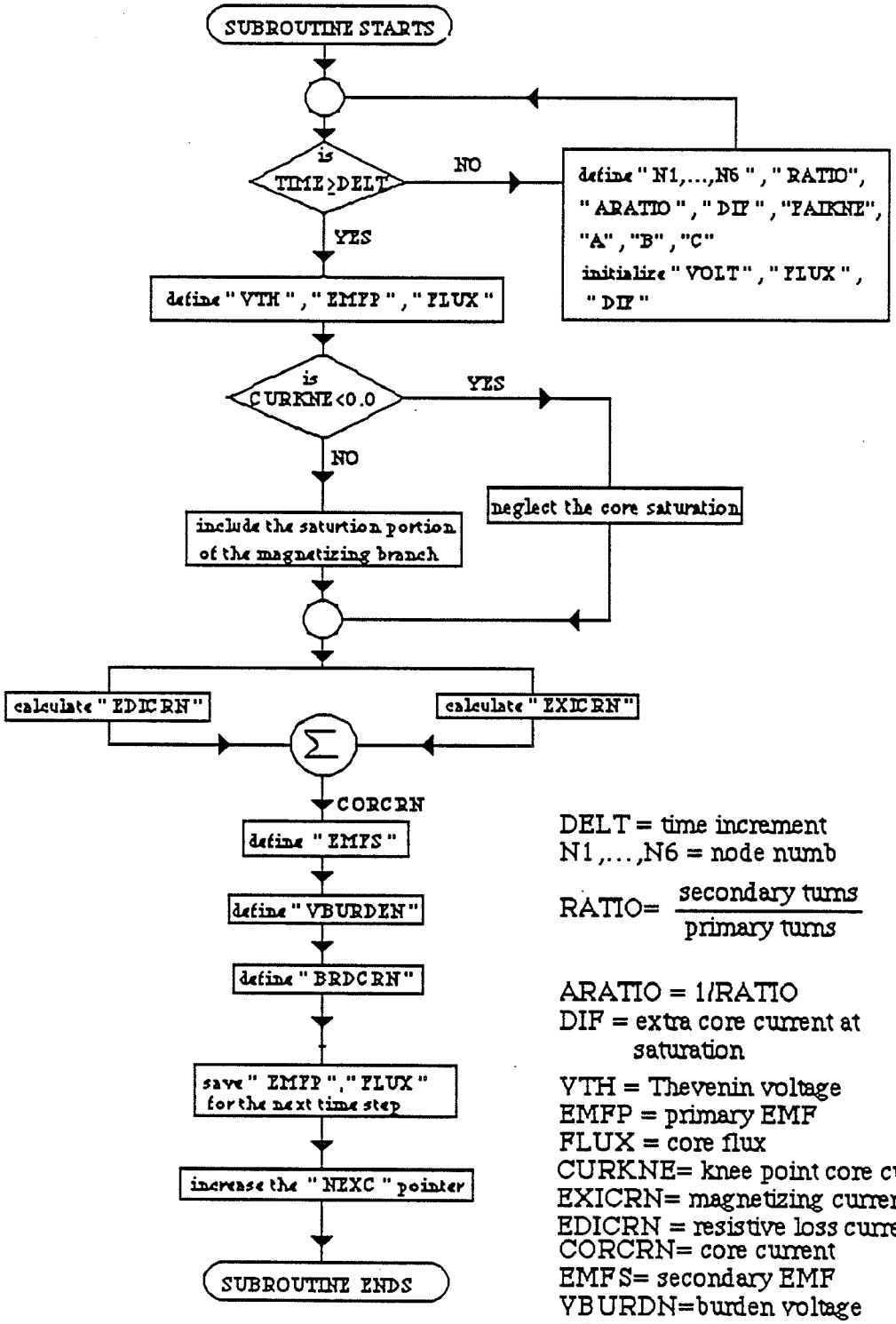


Fig. 5.2 Flow Chart of Subroutine PT2

5.4 - Conclusions

As discussed in section 5.2, the main objective of modeling potential transformers was to develop a model whose output is not noticeably affected by core saturation. The present model of potential transformers meets this requirement. The fact that burden voltage scales down primary voltage without any detectable amplitude or phase distortion is illustrated by Fig. 5.3. For the primary voltage of Fig. 5.3 a, the unsaturated core of Fig. 5.3 b produces the burden voltage of Fig. 5.3 c. For the same primary voltage, the saturated core of Fig. 5.3 d induces the burden voltage of Fig. 5.3 e. In a real potential transformer core saturation rarely occours. However, in order to observe the effect of the core saturation on the response of the potential transformer, in the model core is forced to saturate by lowering the positive kneepoint flux within the datafile.

Apparently the phase and amplitude difference between the two burden voltages are negligible. In other words, in spite of core saturation, fidelity between the primary and burden voltages is conserved.

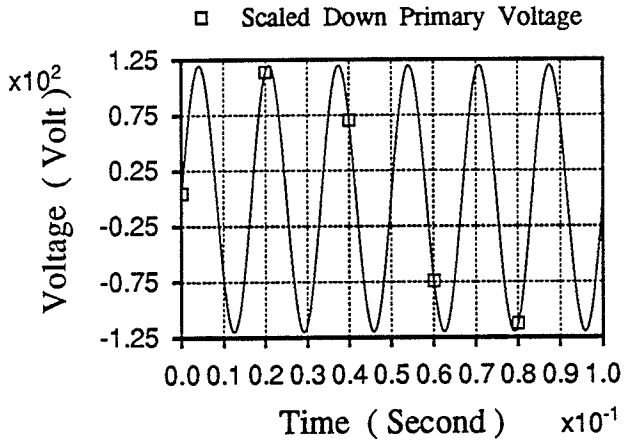


Fig. 5.3 a

PT WITH UNSATURATED CORE

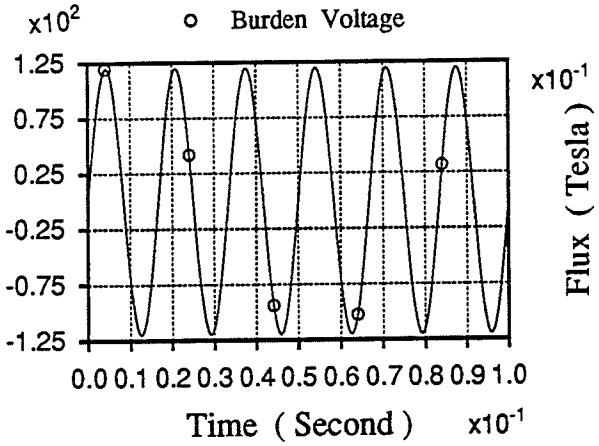


Fig. 5.3 b

PT WITH UNSATURATED CORE

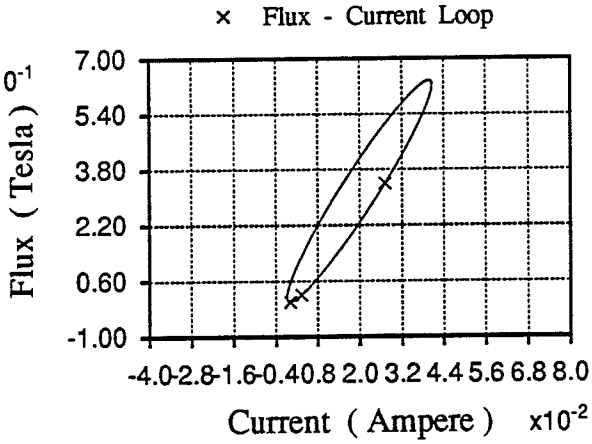


Fig. 5.3 c

PT WITH SATURATED CORE

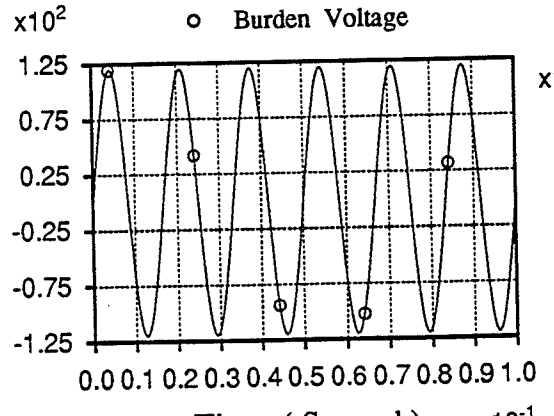


Fig. 5.3 d

PT WITH SATURATED CORE

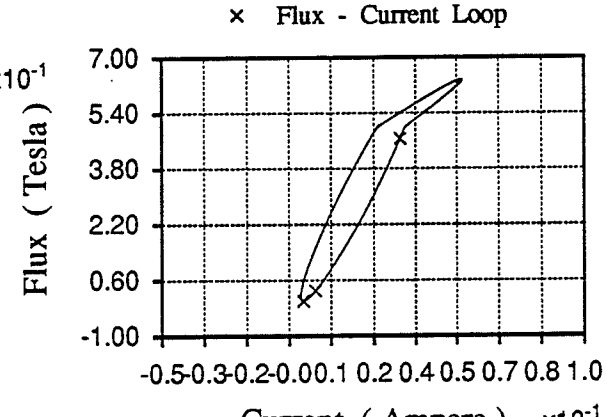


Fig. 5.3 e

Fig. 5.3 PT performance

CHAPTER 6

MODELING OF CAPACITIVE VOLTAGE TRANSFORMERS

MODELING OF CAPACITIVE VOLTAGE TRANSFORMERS

The idea of modeling instrument transformers was discussed in chapter three. Further, the concept and the computer algorithm of the current transformers (CT s) and potential transformers (PT s) were explained in chapters four and five respectively. Yet to be discussed is modeling of capacitive voltage transformers, which is the subject of this chapter.

Capacitive voltage transformers are usually known as CVT s. These are cost effective devices which can scale down the extra high transmission voltages in two steps in order to provide a low voltage level suitable for metering and relaying proposes. The prime concern in the design of CVTs is the fidelity between secondary voltage and transmission line voltage to ground in both the transient and steady state .

Chapter six starts with a review of the history of capacitive potential devices and their evolution to capacitive voltage transformers. In spite of economical and accurate steady state performance, CVT s are prone to subsidence voltage oscillation . The oscillation phenomenon will be discussed in section 6.2. The parameters that affect the transient response of capacitive voltage transformers following the occurrence of a fault will be reviewed in section 6.3. These parameters are important in the design of the CVT model .

At the end of this chapter, the flow chart of the FORTRAN program, which models the CVT as a subroutine of the EMTDC software package, is explained in detail. Typical datafiles of the subroutine CVT2, which models capacitive voltage transformers, are included in appendix 3. Different parameters which affect the transient response of CVT are investigated by this model, and the computer printouts are arranged in appendix 3.

6.1 - Evolution of Capacitive Voltage Transformers

Introduction of high voltage (HV) and extra high voltage (EHV) levels of transmission of electrical power caused many new problems. One of these problems was replacing the conventional magnetically coupled potential transformers with a more economical device because it became evident that insulation expenses exponentially increase at the higher voltage levels. To overcome this problem, other alternatives were sought . Capacitive dividers are known devices for scaling down phase to ground voltages. The circuit of Fig. 6.1 illustrates a capacitive divider.

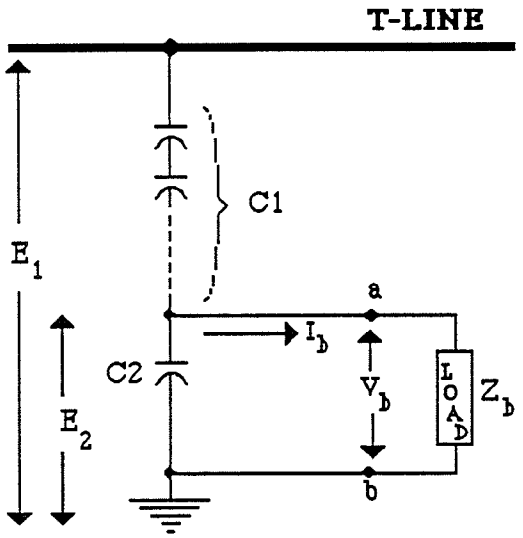


Fig. 6.1 Capacitive Divider

Here Z_b is the load impedance, which can be a metering device. Burden voltage, which is shown by V_b, is measured output. To calculate V_b, the Thevenin equivalent of the original circuit is used. This equivalent circuit is shown in Fig. 6.2 and represents the Thevenin parallel combination of C_1 and C_2 :

$$C_e = C_1 + C_2 \qquad 6.1.1$$

For a burden current of I_b, the burden voltage in its phasor form will be :

$$V_b = V_t - (I_b \times Z_e) \qquad 6.1.2$$

where Z_e is the impedance of the equivalent capacitor.

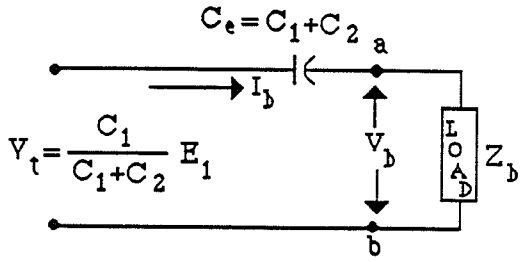


Fig. 6.2 The Equivalent Circuit of A Capacitive Divider

To have a fairly accurate V_b , V_t should be relatively large and Z_e should be small. However, there is a limit to this approach caused by the rated volt-ampere of burden. The other practical problem with this type of divider is the undesired phase shift due to the equivalent capacitor circuit. The phase angle difference between the terminal and load voltages is shown by equation 6.1.2.

The circuit of Fig. 6.3 a is the first adjustment to the shortcomings of capacitive dividers [13]. Here the compensating reactance L is placed in the secondary circuit of a potential transformer to correct the steady state phase shift between the input and burden voltages. L can also be adjusted to compensate for the voltage drop across C_e. The load power factor can be varied by adjusting the variable reactor C_s (Fig. 6.3 a).

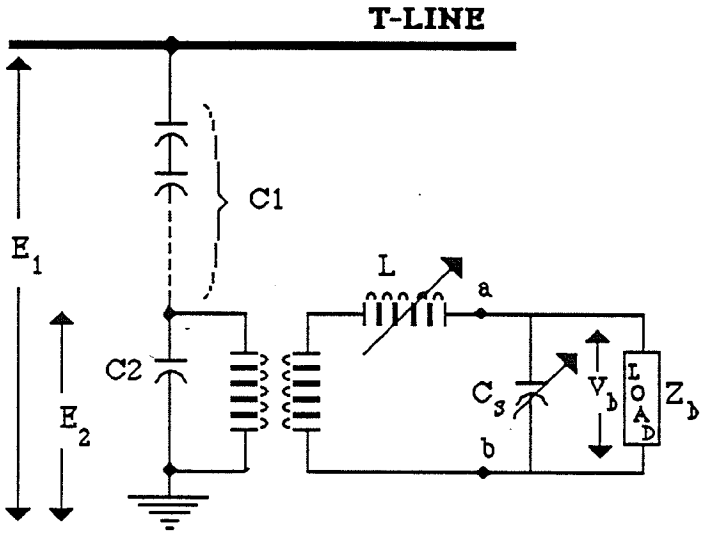


Fig. 6.3 (a) The Phase Correcting Reactor in the Divider Circuit

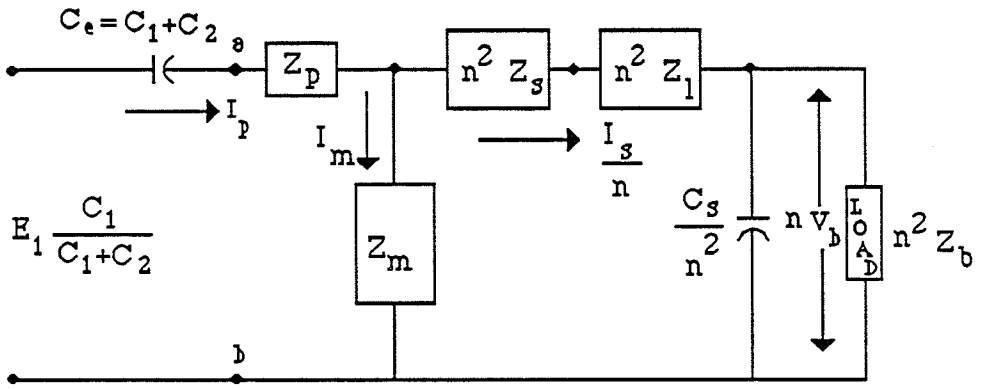


Fig. 6.3 (b) The Equivalent Circuit of Fig. 6.3 (a)

Practically, the circuit of Fig. 6.3 b causes some error due to the magnetizing branch of the intermediate transformer. The magnetizing current of this transformer (I_m) is shunted from the reactor L by the magnetizing branch. Therefore it is not possible to obtain the exact tuning to cancel the capacitive drop due to C_e. Actually there is always a component of current in the primary side which does not appear in the secondary side. The output of this circuit configuration introduces fairly large errors as the load varies on the potential transformer side [13]. The expansion of EHV ties and links, which required metering at EHV levels, encouraged manufacturers to make necessary changes to produce a more accurate capacitive potential divider. To achieve this goal, one can place the tuning reactor in the primary side of PT. In order to enhance source capability, stack capacitance is increased. Tap voltage is also increased, which further improves source capability and allows higher burdens with better regulation. The tap and stack capacitors are mounted in the same housing and are integrated to avoid ratio change due to variation of temperature.

Figs. 6.4 a and 6.4 b show the schematic and the secondary side referred equivalent circuit of the capacitive voltage transformer. This configuration has been chosen as the model of CVT analysis. The nature of load impedance may vary from one application to another. There may also be ferroresonance suppression circuits which are not shown here .

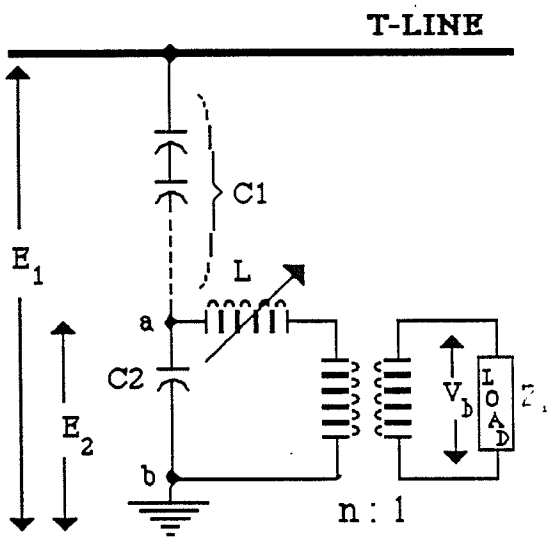


Fig. 6.4 (a) Phase Correcting Inductor in the Primary Side

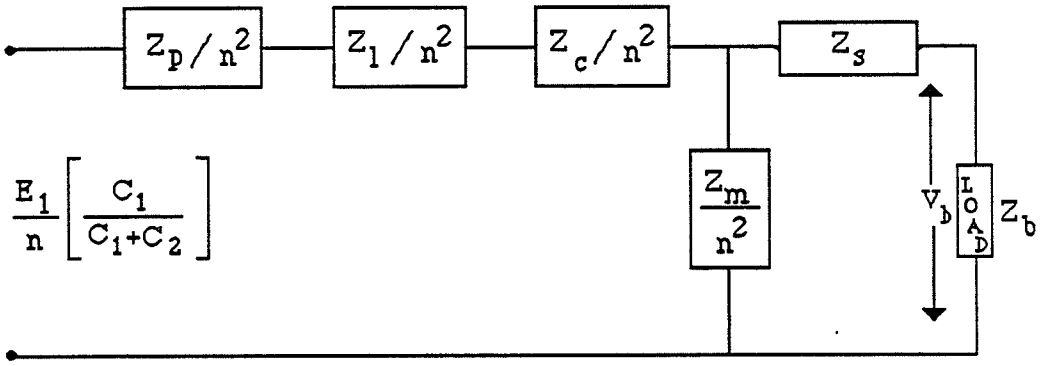


Fig. 6.4 (b) The Equivalent Circuit of Fig. 6.4 (a)

6.2 - Subsidence Transient Voltage

When a fault occurs on a transmission line whose voltage in the steady state is being measured by a capacitive voltage transformer, the reactances present in the equivalent circuit of the CVT act as energy storing devices with a discharge path. The discharge of the stored energy may not be noticeable if the fault occurs in an instant of time when the stored energy in either C_e or L is not significant. However, for faults occurring at zero or crest voltage, the dischargeable energy will be large enough to cause subsidence transient voltage in the secondary side.

To understand why the point of fault initiation is a major factor, consider the equivalent circuit of a basic capacitive potential device without ferroresonant suppression as in Fig. 6.5. For a resistive burden and with the x_l of the reactor and transformer cancelling the x_c of the capacitor, the primary current is in phase with the primary voltage.

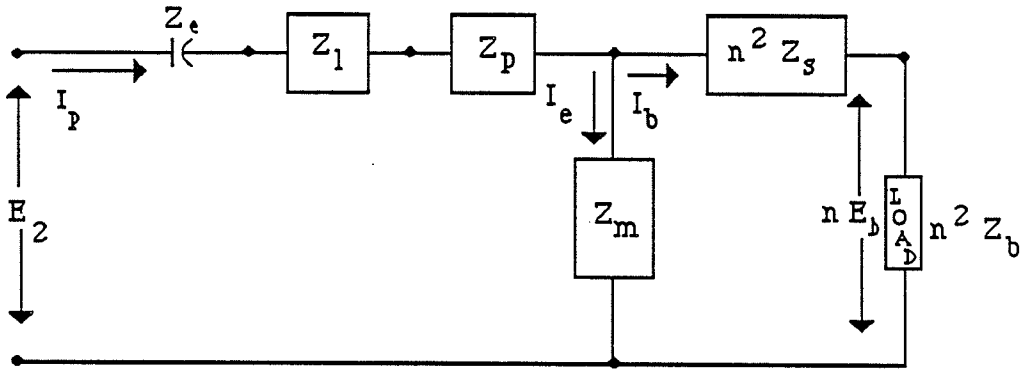


Fig. 6.5 The Equivalent Circuit of CVT Without the Suppression Circuit

The voltage across these reactive components, however, is determined essentially by the burden current and is 90° out of phase with the current. Therefore as the primary voltage and burden current are going through zero, the energy stored in the capacitor $(\frac{1}{2} C_e \times e_c^2)$ is maximum (e_c is the capacitor voltage). Since the capacitor C_e must discharge this maximum energy at the time of the fault, the residual voltage, as will be seen, is also maximum. The phase relationship can be depicted vectorially in Fig. 6.6.

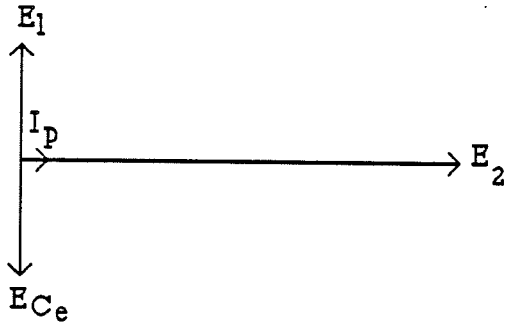


Fig. 6.6 Phasor Diagram of Fig. 6.5

Though the voltage is also maximum on the compensating reactor, the energy $(\frac{L i^2}{2})$ is minimum and therefore does not contribute significantly to the subsidence transient.

At the crest portion of the primary wave, voltage on the capacitor C_e (hence energy stored) is zero, while on the inductor the voltage is also zero but current is at crest and the energy is maximum $\frac{L i^2}{2}$. Since the same amount of energy is stored at crest by the compensating reactor as at zero by the capacitor, the determination of the worst case of subsidence transient is made by the discharge time constant. With maximum energy in the capacitor at primary voltage zero, time constant is essentially :

$$t_c = R \times C$$

whereas with maximum energy in the reactor, time constant is basically :

$$t_l = \frac{L}{R}$$

until the capacitor becomes charged. At this point it is again R C. For example, if C = 0.244 μF, L = 28.7 H and R_b(reflected to primary) = 126.5 KΩ, then:

$$t_c = 126.5 \times 10^3 \times 0.244 \times 10^{-6} = 31 \text{ milliseconds}$$

$$t_l = \frac{28.7}{126.5 \times 10^3} = 0.227 \text{ milliseconds}$$

Clearly the longest response and worst case occurs with maximum energy on the capacitor, at the time the primary wave is going through zero for a resistive burden.

This statement is verified by the computer model of a capacitive voltage transformer. The supporting computer plots are included in sets 1a and 1b of appendix 3 .

6.3 - Factors Influencing Subsidence Transient Voltage

In section 6.2, subsidence voltage was explained and the mechanism of oscillation was discussed . It was also shown that the instant of fault occurrence has an important influence in the magnitude and time constant of the subsidence voltage transient. However, it has to be emphasized that although the most important factor, the instant of fault

occurrence is not the only contributing factor to this phenomenon. Among the other parameters influencing the subsidence voltage are magnitude of divider capacitances, turns ratio of the intermediate potential transformer, ferroresonance suppression circuit, burden magnitude, burden power factor and core magnetizing branch.

A) Magnitude of Divider Capacitances

A larger equivalent capacitor C_e will cause a smaller capacitive reactance

$$X_c = \frac{1}{j\omega C_e}$$

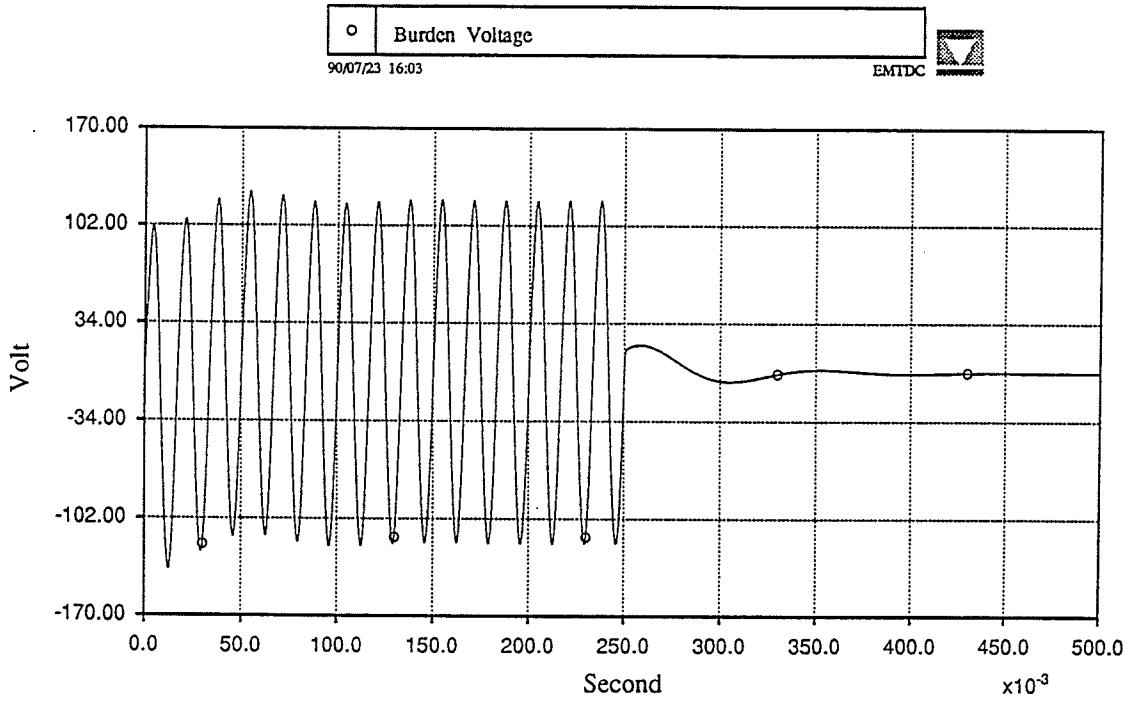
and this in turn leads to a smaller voltage drop across the equivalent capacitor. Consequently, there are smaller stored capacitive energy and decrease in magnitude of the subsidence voltage transient. But the time constant of oscillation actually increases, which is evident because the time constant is directly proportional to C_e. The effect of divider capacitance in changing the magnitude and time constant of the oscillatory wave can be observed in Figs. 6.7 a and 6.7 b and also sets 2a and 2b of appendix 3.

B) Turns Ratio of the Intermediate Potential Transformer

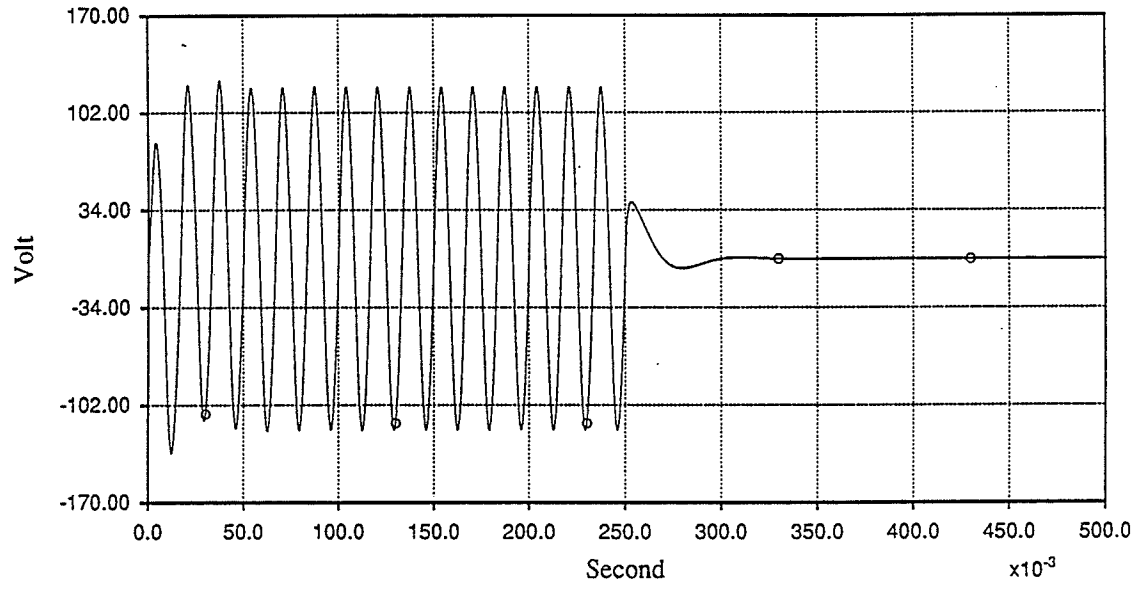
The primary current of the intermediate potential transformer is related to the turns ratio by :

$$I_p = I_s \frac{N_s}{N_p} \qquad 6.3.1$$

where I_p is the primary current, I_s is the secondary current (load current), N_s is the number of turns in the secondary side and N_p is the primary side turns. For a fixed burden current and fixed number of secondary turns, increasing the turns ratio by increasing N_p will cause a smaller primary current and therefore a smaller capacitive voltage drop, which leads to ferroresonance with smaller magnitude. This conclusion is verified by the computer model of a capacitive voltage transformer. Figs. 6.8 a and 6.8 b illustrate the effect of increasing the turns ratio on the burden voltage. The simulation plots of this case are included in sets 3a and 3b of appendix 3.

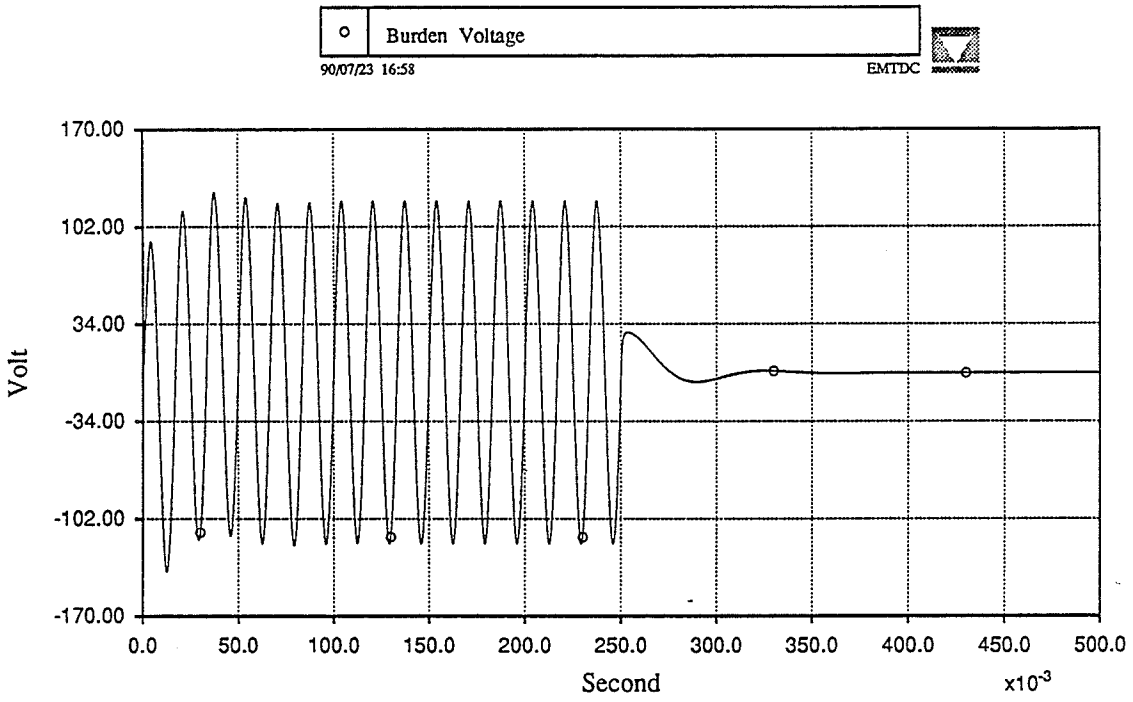


Figs. 6.7 a C_e = 0.244 μF

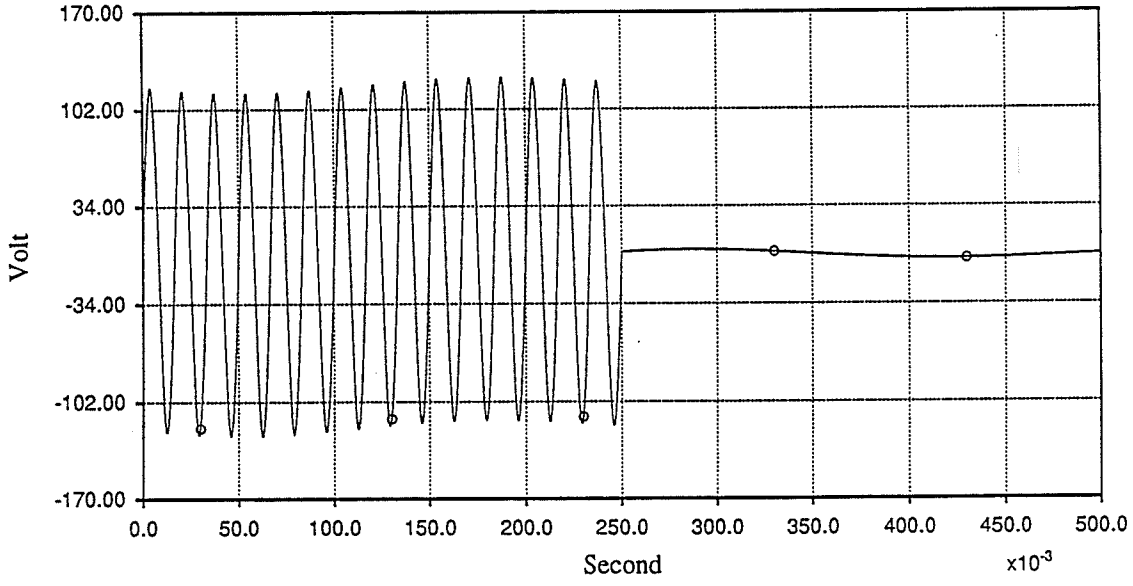


Figs. 6.7 b C_e = 0.087 μF

Figs. 6.7 a and 6.7 b Effect of Decreasing the Equivalent Capacitor On the Transient Response of the CVT



Figs. 6.8 a Turns Ratio of the Intermediate PT = 50.0



Figs. 6.8 b Turns Ratio of the Intermediate PT = 200.0

Figs. 6.8 a and 6.8 b Effect of Increasing the Turns Ratio of the PT On the Transient Response of the CVT

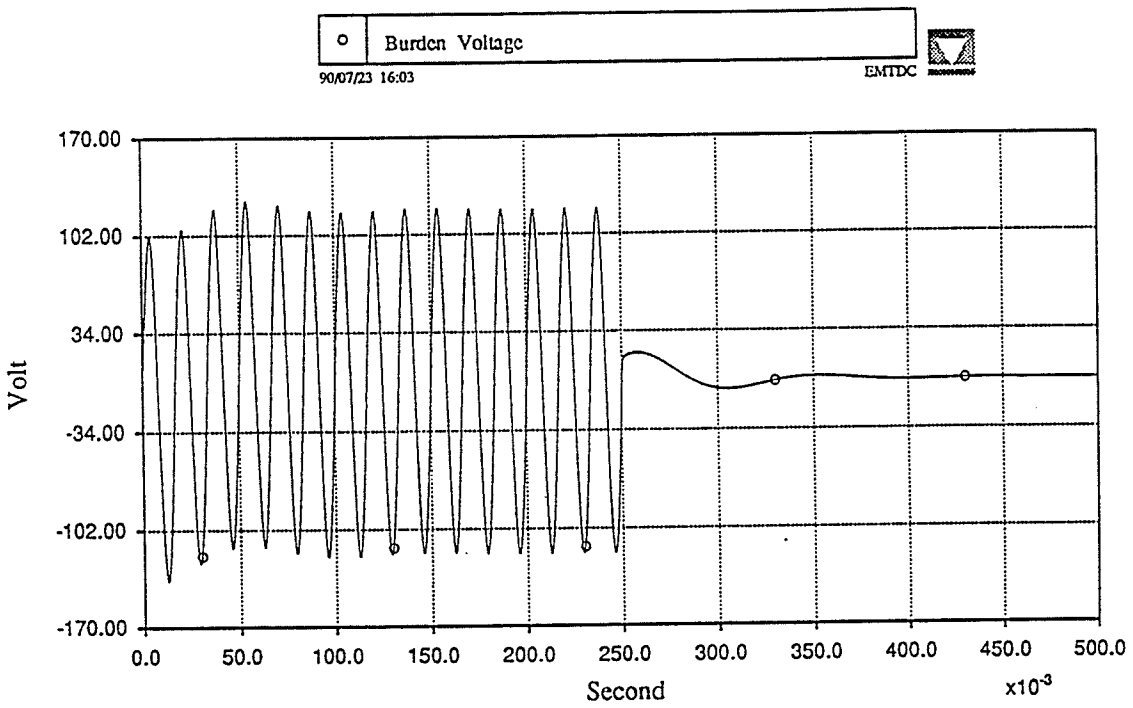
C) Ferroresonance Suppression Circuit

The ferroresonance of the burden voltage of a capacitive voltage transformer can be recorded and analyzed. The Fourier Analysis of such a waveform indicates the frequency components which contribute to ferroresonance. Once such an analysis is done, at least two methods can be used to suppress undesired components. In the first method a tuned filter removes the unwanted oscillations. A simple tuned *RLC* filter is used by at least three manufacturers of capacitive potential devices [14].

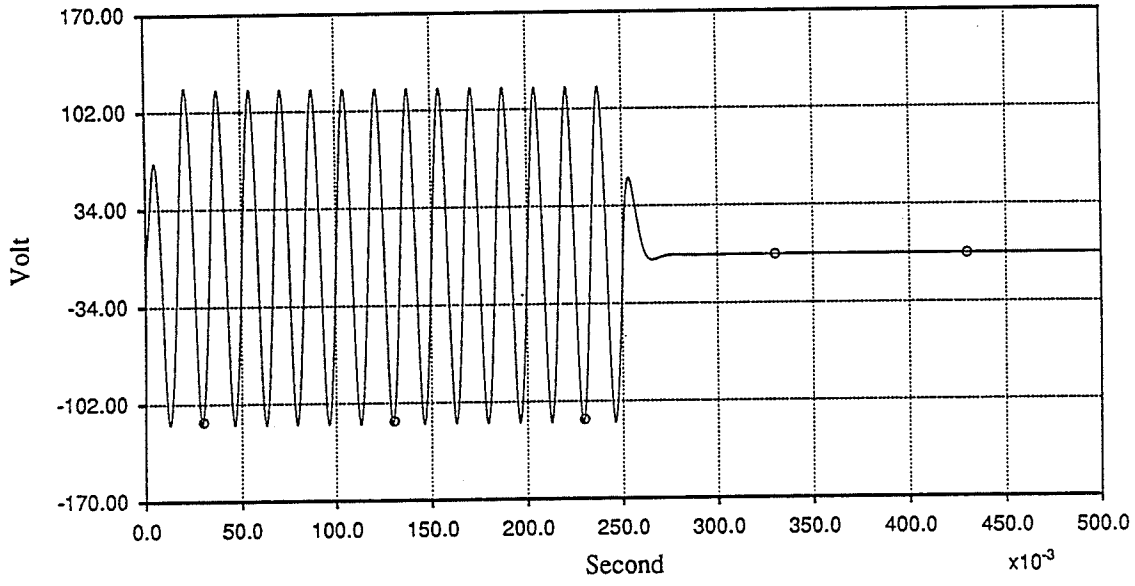
The second possibility is paralleling a permanent damping resistor with the load. The damping effect of this resistor attenuates the amplitude of the subsidence transient. The problem with this type of suppression is that during normal steady state operation it causes the flow of a heavy primary current.

D) The Magnitude of Burden

To observe the effect of burden magnitude, a purely resistive load under zero fault initiation (suppression circuit is neglected for simplicity) is investigated. If the secondary winding was open circuit (infinite burden), the magnetizing current would be the only current passing the primary circuit. For a well designed core, the magnetizing current will be in range of miliamperes and therefore the energy stored in the capacitive component is small and consequently the subsidence transient is small. A decrease in burden resistance will cause an increase in secondary current. This, in turn, increases the primary current which directly increases the stored energy in C_e at the instant of fault.AS expected the magnitude of the subsidence transient increases, but since the resistive load is decreased , the time constant $(t_c = R \times C_e)$ decreases. The magnitude of the resistive burden also determines if the transient is overdamped or oscillatory. The effect of burden magnitude on the subsidence transient voltage is illustrated by decreasing the resistive burden from 36 Ohms (Fig. 6.9 a) to 6 Ohms (Fig. 6.9b). The computer plots of sets 4a and 4b in appendix 3 support these results.



Figs. 6.9 a 36.0 Ohms Resistive Burden



Figs. 6.9 b 6.0 Ohms resistive Burden

Figs. 6.9 a and 6.9 b Effect of Decreasing the Burden Magnitude On the Transient Response of the CVT

E) The Power Factor of Burden

By replacing the resistive load of part D with an RL (or RC) load, the power factor will change from unity to a fraction of one. In this case the burden not only contributes to the damping shape and the time constant of the subsidence transient, but it also acts as a reactive element causing transient response to be of oscillatory nature (usually a low frequency oscillation) and this worsens the response. Figs. 6.10 a and 6.10 b illustrate the change in the subsidence transient voltage due to decrease of power factor from unity to 0.7 . The simulation plots are included in sets 5a and 5b of appendix 3.

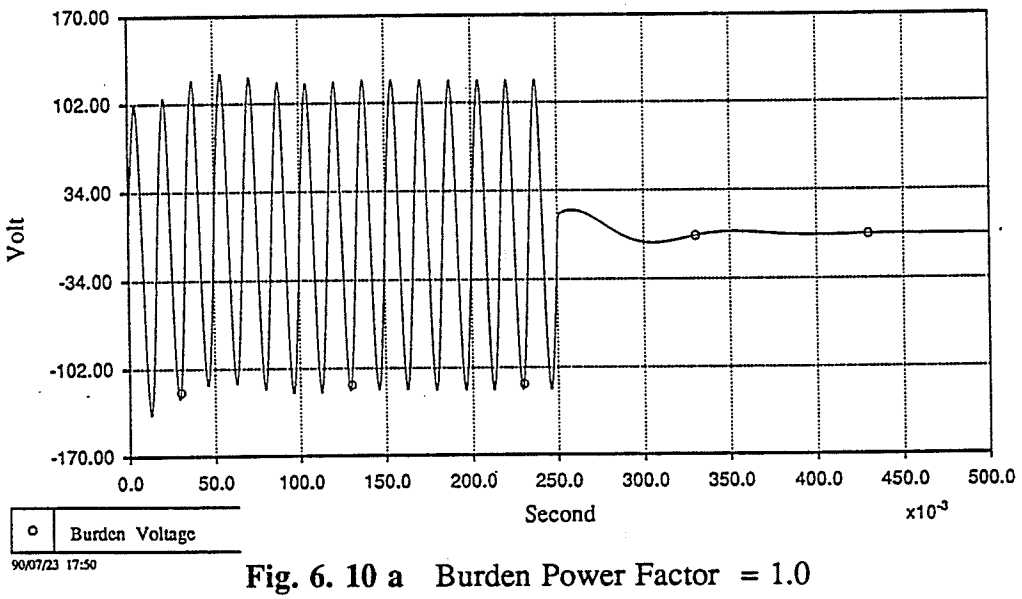


Fig. 6. 10 a Burden Power Factor = 1.0

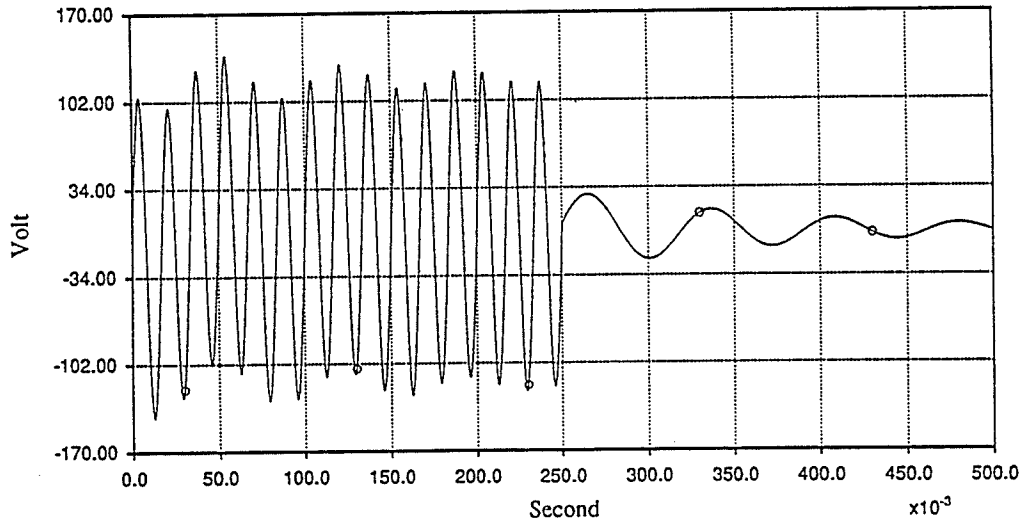


Fig. 6. 10 b Burden Power Factor = 0.7

F) The Core Magnetizing Branch

As mentioned in part D, under normal operating conditions for a well designed core, the core magnetizing impedance is relatively high (in the range of 10 megaohms) and the core current is relatively small. Such a high impedance core can be practically ignored in CVT analysis. However, if this is not the case and the core inductance is low enough to be comparable to other circuit elements, or if the core is driven into saturation, then its effect should not be ignored any more. In fact the magnetizing current drawn by a relatively low impedance core worsens the subsidence transient behavior. The response of the CVT model to a saturated and an unsaturated core is included in sets 3a and 3b of appendix 3.

In summary, different factors contributing to the transient response of capacitive voltage transformers are discussed and the effect of each factor is explained separately. The conclusions of this section are verified by the computer model of capacitive voltage transformers. The model will be discussed in the following section.

6.4 - Computer Model of Capacitive Voltage Transformers

Like other instrument transformers, a capacitive voltage transformer can be tested in the field. However, initiation of a fault on a real network and replacing the different circuit elements for a variety of tests are tedious jobs. Modeling of instrument transformers on a digital computer enables the user to perform the same tests and observe similar results (with a certain degree of accuracy) without dealing with physical apparatus. It is a fast and convenient method which can save a considerable amount of time and effort.

The present subroutine, which is developed to model capacitive voltage transformers in EMTDC, is called CVT2. Here 2 stands for the number of the STOR storage units which are used in this subroutine [11]. Like other EMTDC subroutines, CVT2 can be called by either the main program or any user written subroutine.

The circuit which is modeled by CVT2 is shown in Fig. 6.11. The elements of this circuit are transferred to the secondary side and therefore have to be scaled before being placed in an EMTDC datafile. To avoid any scaling confusion, the circuit elements of Fig. 6.11 are explained here with some illustrative examples.

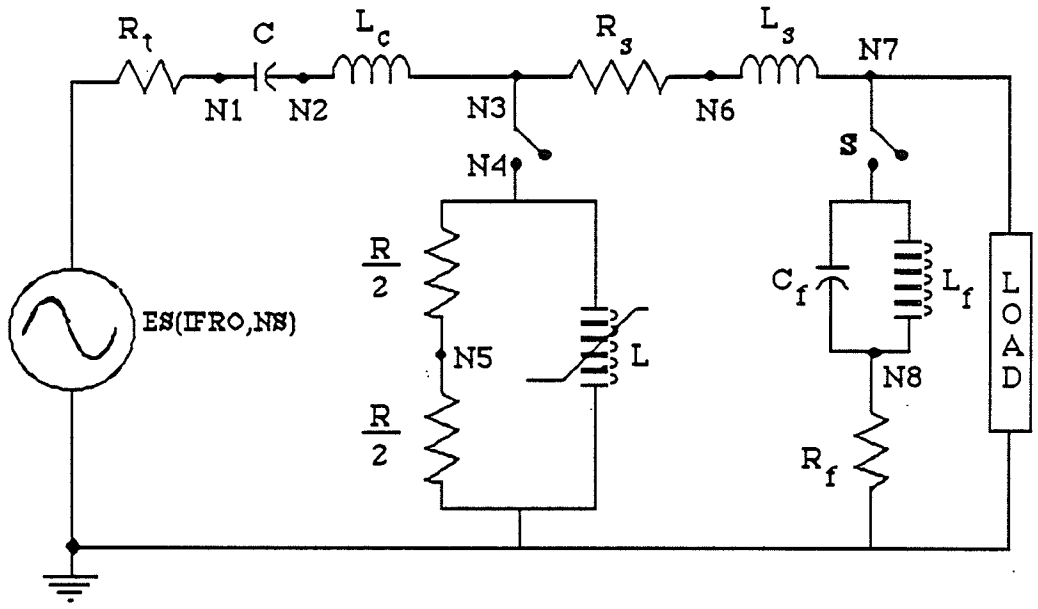


Fig. 6.11 The Equivalent Circuit of the CVT for Computer Modeling

ES : ES represents the tap capacitor voltage which is transferred to the secondary side of the intermediate PT. As an example if the phase to neutral transmission line voltage is 120 kV and the capacitive ratio is :

$$\frac{C_1}{C_1 + C_2} = 0.05$$

and also if the turns ratio of the intermediate potential transformer is 50:1, then 120 kV appears to be :

$$120 \times 0.05 = 6 \text{ kV}$$

at the tap capacitor. When this 6 kV voltage is transferred to the secondary side it acts like a 120 V voltage source. Therefore ES for this example will be 120 V. ES is always expressed in volt.

R_t : R_t is the Thevenin equivalent resistor which appears in a datafile. Its magnitude is chosen to be the resistance of the primary circuit transferred to the secondary side. For a turns ratio of 50:1 and a primary resistance of 1 ohm , R_t appears to be :

$$R_t = 1 \times (50)^{-2} = 4 \times 10^{-4} \ \Omega$$

R_t is expressed in ohm and can be formulated as :

$$R_t = R_p \times (RATIO)^2 \qquad 6.4.1$$

where R_P is the primary resistance and :

$$RATIO = \frac{N_S}{N_P} = \frac{\text{number of secondary turns}}{\text{number of primary turns}} \qquad 6.4.2$$

C : C is the magnitude of the capacitive divider in microfarad transferred to the secondary side. C can be formulated as :

$$C = \frac{C_1 + C_2}{(RATIO)^2} \quad \mu F \qquad 6.4.3$$

where C_1 is the stack capacitance and C_2 is the tap capacitance. The equivalent capacitance C_e is defined as the parallel combination of C_1 and C_2 :

$$C_e = C_1 + C_2 \quad \mu F \qquad 6.4.4$$

L_c : L_c represents the sum of the phase correcting reactor (L) and the primary inductance L_P (if any) both referred to the secondary side :

$$L_c = (L + L_p) \times (RATIO)^2 \qquad 6.4.5$$

L_c is expressed in Henry and satisfies :

$$L_c = \frac{1}{\omega^2 \times C}$$

where C is in Farad .

R : R is the core resistive loss element in Ohm . R is transferred to the secondary side. In order to enable the EMTDC main program to monitor the current passing through the R, R is divided into two equal series resistors R/2 each. It has to be explained that at present time the EMTDC program is unable to detect the current flow in the parallel branches. One method to overcome this deficiency is creating an extra node by halving the core resistance into two equal parts in series. The new configuration does not have two branches in parallel and therefore the branch currents can be monitored.

$$R = RLOSS \times (RATIO)^2 \qquad 6.4.6$$

where RLOSS is the core resistance .

L_m : L_m is the magnetizing core inductance in Henry referred to the secondary side. The unsaturated core inductance is referred to secondary side and appears in a datafile. If core goes to saturation, the program will take care of it by generating more core flux and without changing any parameter in the datafile. Therefore :

$$L_m = \text{SLIN} \times (\text{RATIO})^2 \qquad 6.4.7$$

here SLIN is the core unsaturated inductance. A negative number for L_m in the datafile is interpreted by the program as a flag to ignore the core effect. This is like opening the switch between the nodes N3 and N4 in Fig. 6.11.

L_s : L_s is the secondary inductance in Henry .

S : S represents the switch to include or exclude the ferroresonance suppression circuit. The datafile includes the suppression circuit when S = 1. A negative value for S in the datafile eliminates that circuit.

C_p : C_p is the suppression capacitance in microfarad .

L_f : The suppression inductance in Henry.

R_f : The suppression resistance in Ohm.

R_b : The resistive burden element in Ohm. The burden can have any configuration desired by the user. Here the simplest form is chosen .

N1 , N2 , ... : The node numbers of the equivalent circuit.

The flow chart of Fig. 6.12 illustrates how subroutine CVT2 works.

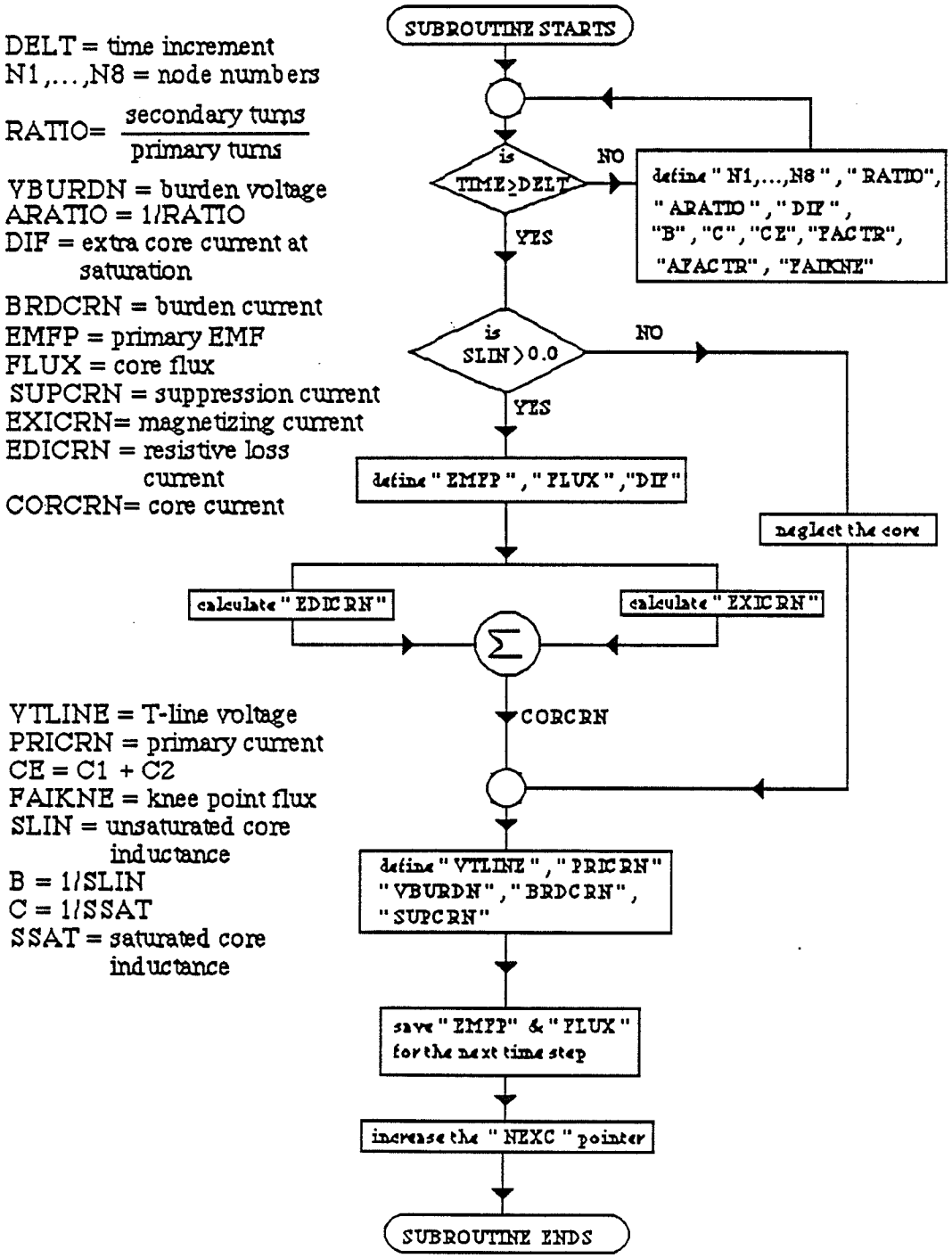
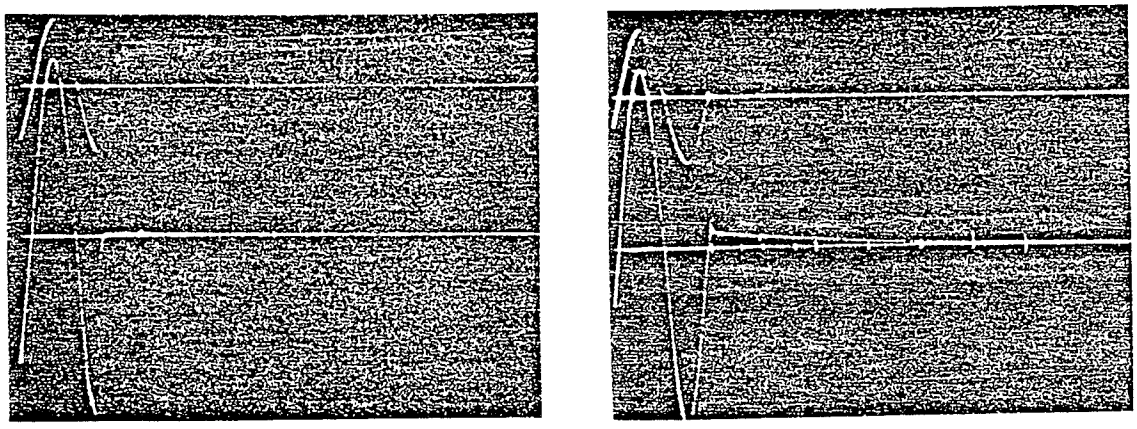


Fig. 6.12 Flow Chart of the Subroutine CVT2

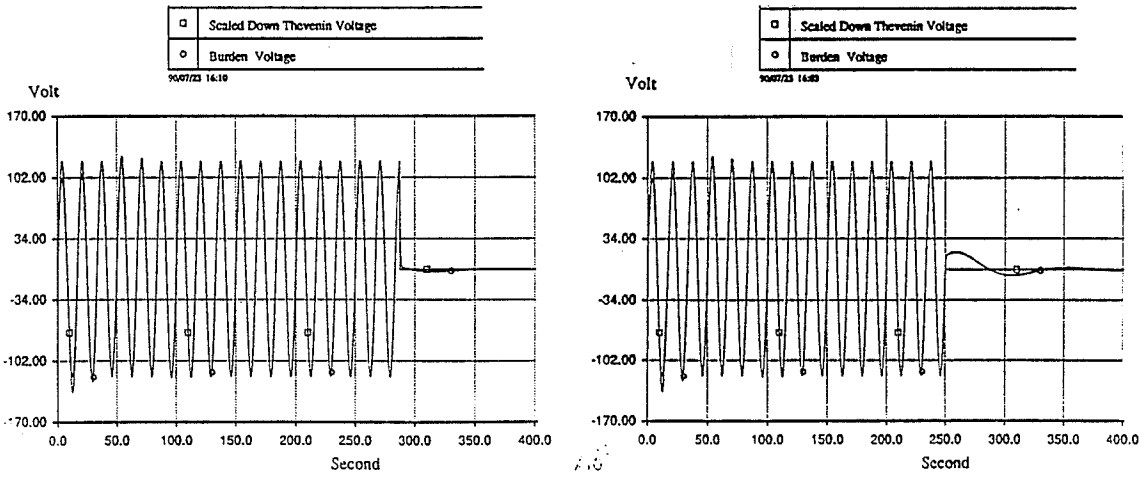
6.5 - Conclusions

Subsidence Transient Voltage is known to be the major problem with capacitive voltage transformers. The factors contributing to the transient voltage have been experimentally tested [14]. The recordings for crest and zero fault initiations are shown in Figs. 6.13 a and 6.13 b :



a) Crest Fault Initiation **b**) Zero Fault Initiation

Figs. 6.13 a and 6.13 b The Experimental Response of the CVT [14]

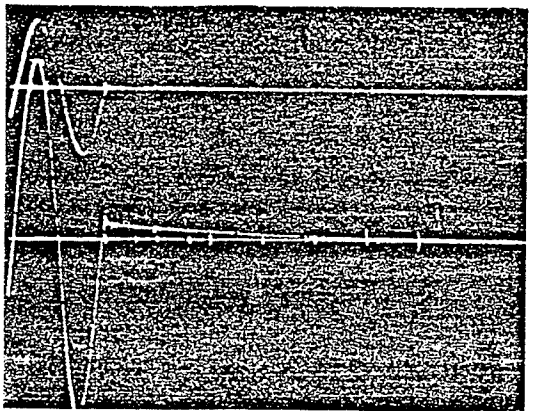


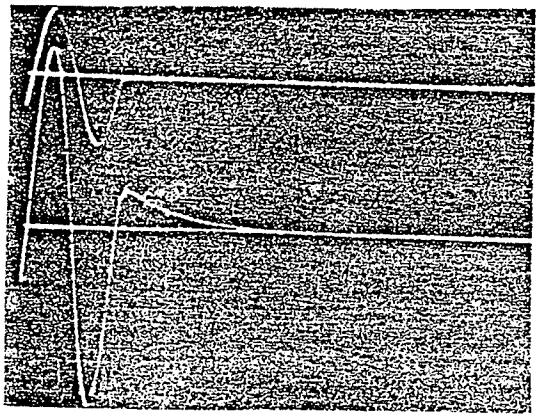
c) Crest Fault Initiation **d**) Zero Fault Initiation

Figs. 6.13 c and 6.13 d - The Simulation Response of the CVT Model

Different tests have been performed to show the simulation capabilities of the developed CVT model.The model response to crest and zero fault initiations are shown in Figs. 6.13 c and 6.13 d. As expected, ferroresonance occurs in both cases and is more severe in zero fault initiation.

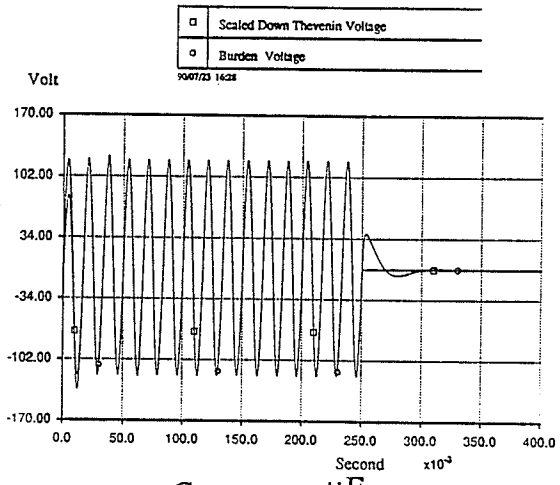
In another test the effect of equivalent capacitance C_e was investigated. In the field, C_e was decreased from 0.244 μF to 0.087 μF. The zero fault initiation field response of the 0.244 μF case is shown in Fig. 6.14 a. The field recording of the zero fault initiated on 0.087 μF case is shown in Fig. 6.14 b. The experimental recordings confirm that as C_e decreases, the subsidence transient becomes more severe. The theoretical base of this statement is discussed in section 6.3 A. The same conclusion can be drawn from the simulation printouts of Fig. 6.14 c for C_e = 0.244 μF and Fig. 6.14 d for C_e = 0.087 μF.

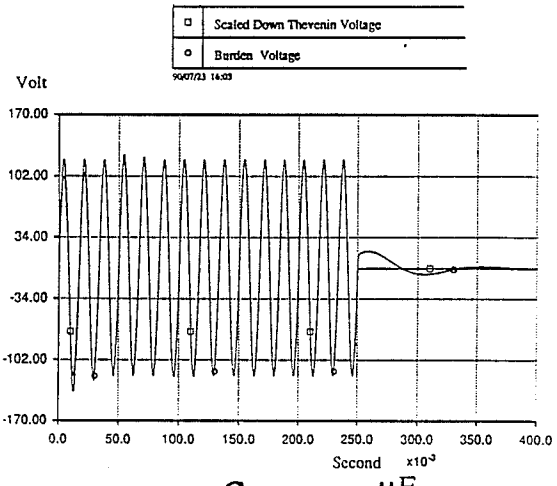




a) C_e = 0.244 μF **b**) C_e = 0.087 μF

Figs. 6.14 a and 6.14 b - The Experimental Response of A CVT [14]





c) C_e = 0.244 μF **d**) C_e = 0.087 μF

Figs. 6.14 c and 6.14 d - The Simulation Response of the CVT Model

The effects of other circuit parameters in severity of ferroresonance are also investigated by the developed model and the results are documented in appendix 3.

CHAPTER 7

RESULTS AND DISCUSSION

Results and Discussion

In the abstract of this thesis it is mentioned that the subroutines developed to model the instrument transformers in the EMTDC package are accurate enough to be used for system simulation purposes. Room for further refinement of the models was also taken into account. Here in chapter seven some possible techniques to improve the existing software are reviewed, and suggestions for future work in this field are made. For those who may want to pursue a similar research area, the three implemented core saturation models are briefly compared and pros and cons of each model with respect to others are shown. Practical problems which were discovered during the development of models are highlighted.

7.1 - Linearization Error

The linearization of the hysteresis loop has already been discussed in chapter four. The error associated with the linearization technique will be illustrated by means of an example. Arbitrary numbers are chosen for simplification.

It can be assumed that for a particular current transformer, the knee point core flux is 0.5 Tesla, the unsaturated slope is 100.0 and the saturated slope is 1.0. It can further be assumed that in some specific instant t_1, core flux is 0.4999 Tesla and one time step later it increases to 0.5001 Tesla. Therefore the core current at each instant of time is :

$I(t_1) =$

$0.499 / 100.0 = 4.99$ miliampere

and

$I(t_1 + \Delta t) =$

$0.5001 / 1.0 = 0.5001$ Ampere

It can be seen that the core current jump in one time step is :

$0.5001 - 0.004999 = 0.495$ Ampere

Although the selected fluxes and currents are not real values, they explain the sudden jump in core current when linear $\varphi - I$ slope changes to saturated slope. This effect is shown in Fig. 7.1.

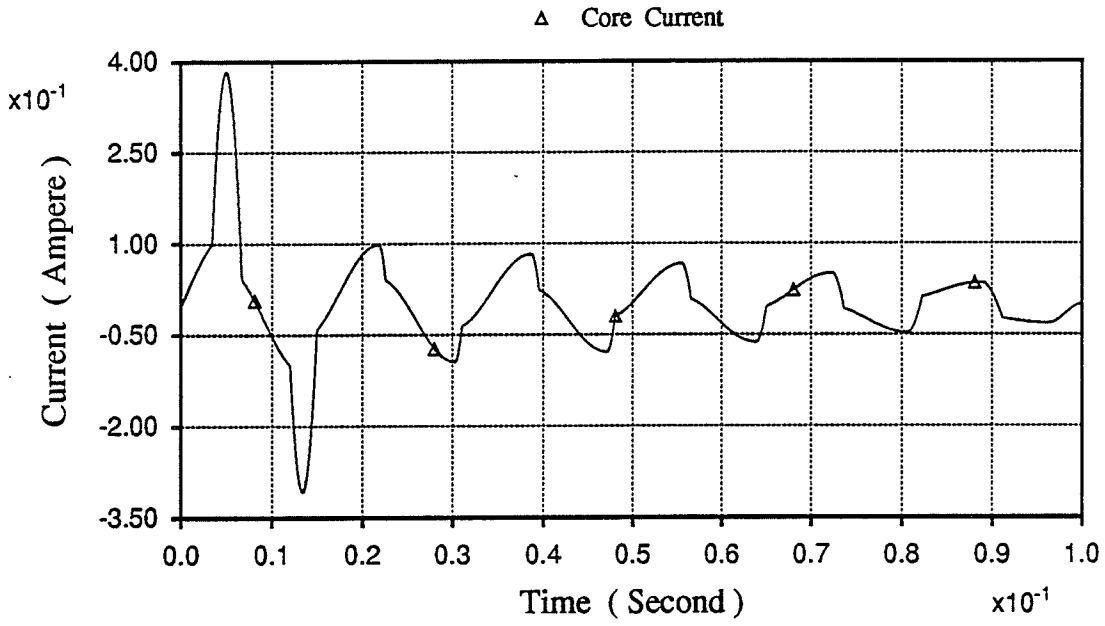


Fig. 7.1 - The Jump in Core Current Due to the Change of Slope

In a physical device,the core current changes smoothly and in a more curved manner. The difference between real core current and core current simulated by the linearized model is referred to as linearization error. In most practical cases this type of error is negligible, and therefore the two slope criteria of the model is adequate. However, if more precision is required, other techniques can be implemented. One such technique of improving the linearized model is explained in section 7.2.

7.2 - Further Refinement of the Linearized Core Model

As mentioned in chapter four, the linearized models of core saturation are based on two slopes : the unsaturated slope and the saturated one. The point of convergence of these two linear slopes on the $\varphi - I$ plane is known as " knee point " . In a real nonlinear hysteresis loop, there is nothing like the point of intersection of two straight lines. Instead,

the knee point is located on a fine and smooth curve which can be named knee portion. The linearized model approximates the knee portion with two straight lines. As the operating point shifts from a point whose flux is slightly less than the knee flux to a point whose flux is slightly greater than the knee flux, the core current suddenly increases.

One possible technique to reduce the linearization error is to define three or more slopes on the hysteresis loop. This is like approximating a nonlinear exponential with linear segments. The greater the number of segments, the closer the corresponding points on the exponential. This method can be used in all three models with two slopes. The programmer has to extend the two slope formulation of each model to a multi - slope formulation. This technique, however, has some limitations. In most practical cases, selecting the accurate data pairs from available manufacturer curves is not easy, and sometimes there is not enough information in the saturation portion. The other constraint is the size of subroutines which grows as more slopes are modeled. An auxiliary program that is able to read data pairs and to calculate slopes which have to be replaced in the main subroutine is a step ahead in further refinement of present linearized saturation models.

7.3 - Comparison of the Core Models

Among the three developed models which simulate a transducer core, case 1 of the current transformer model and the core model of potential transformers are similar. They both represent linear magnetic loss by a linear inductor. A linear resistor models core resistive losses in both cases. The user provides the slope of linear and saturated portions and the core flux at knee point. The only difference between the two models is that in case 1 of a current transformer model the magnetizing branch does not appear as a branch in the datafile. However, in the models of potential transformers and capacitive voltage transformer, the linear magnetizing branch has to be specified as an inductor within the datafile. The subroutine takes care of the saturated portion. Apart from this, both models have similar configurations, and there is close agreement between their responses to the same excitation.

The model of case 2 of a current transformer, however, is somehow different. Here the user does not specify the core resistive losses as a lumped resistor. Instead, the core resistive losses change by variation of the area enclosed by the hysteresis loop. The user is able to adjust the enclosed area by specifying the coordinates of the knee point.

As far as the minor loops are concerned, case 1 of the current transformer model reflects all the curvature of the knee portion (Fig. 7.2).

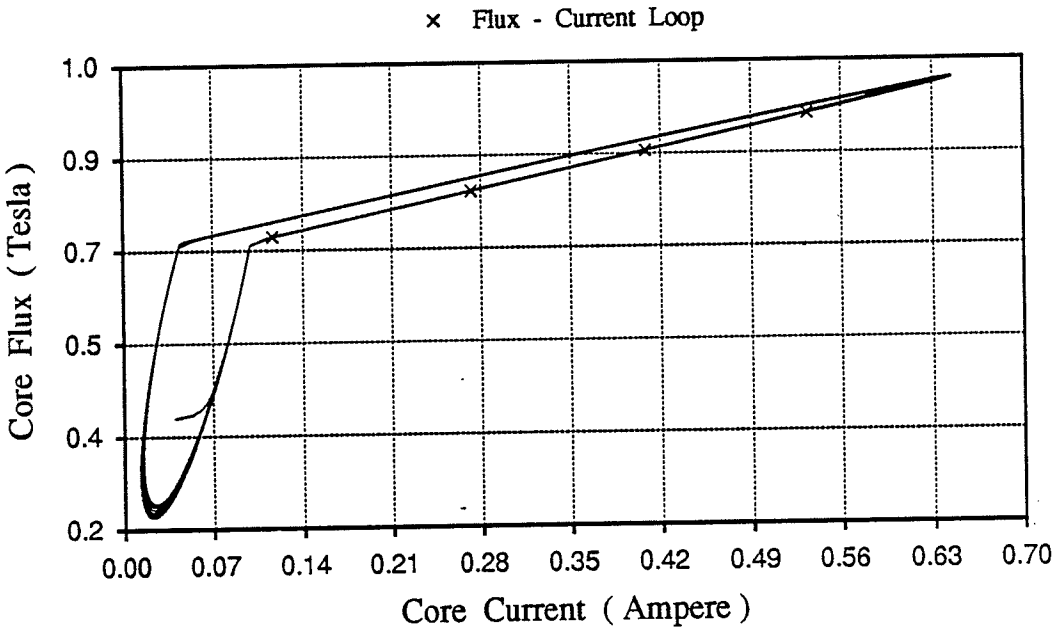


Fig. 7.2 - Simulation of Minor Loops by the CT Model - Case 1

In case 2 of the current transformer model, the parent and minor loops are approximated by parallelograms. Fig. 7.3 is a typical hysteresis loop simulation of case 2 :

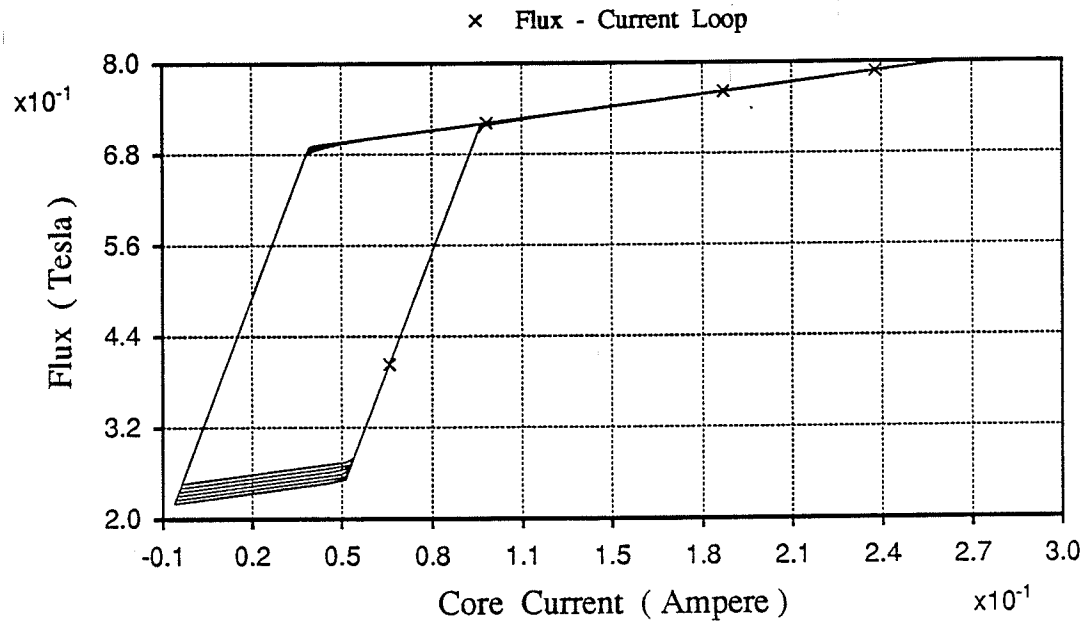


Fig. 7.3 - Simulation of Minor Loops by the CT Model - Case 2

The output of a current transformer model is burden current. Fig. 7.4 and Fig. 7.5 are the burden currents of current transformer models case 1 and case 2 respectively. As can be observed, the burden currents for the same excitation are almost identical. This indicates that the difference is negligible.

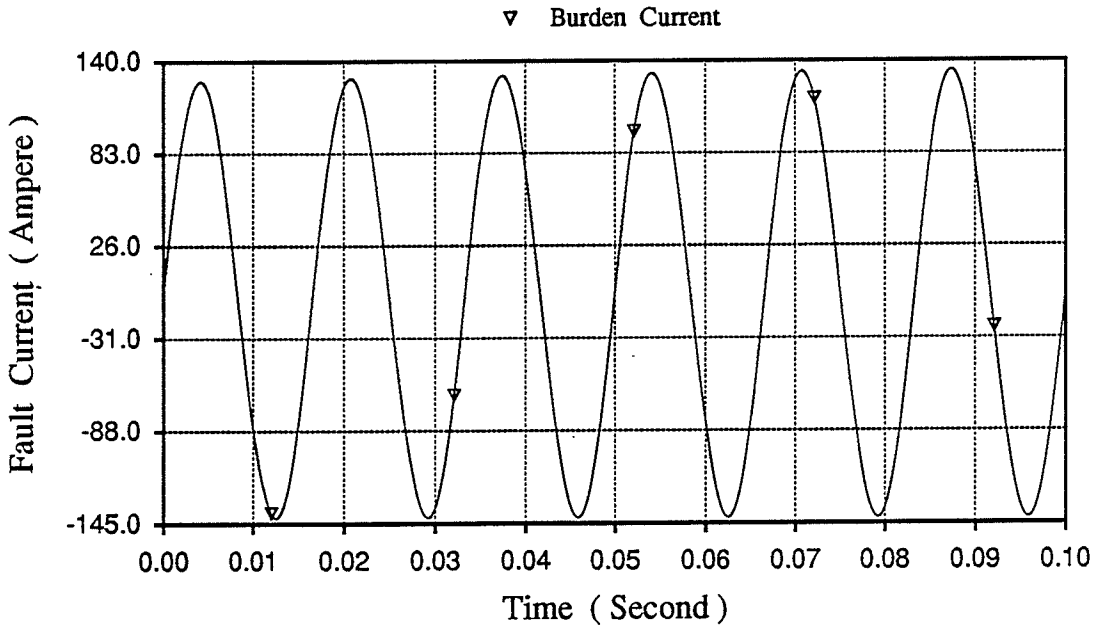


Fig. 7.4 - Simulation of Burden Current by the CT model - Case 1

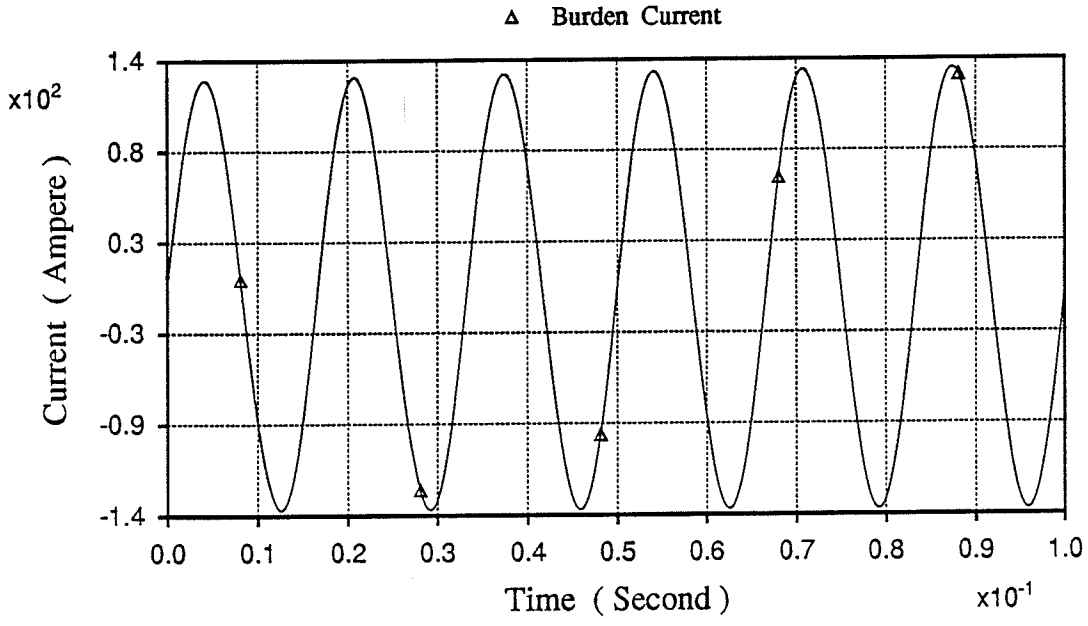


Fig. 7.5 - Simulation of Burden Current by the CT model - Case 2

In summary, the best of the three developed models differs from one application to another. It is up to the user to extract the available parameters from the data sheets and to choose the core model which provides the optimum output for that specific application.

7.4 - The B - H Plane

The core models of instrument transformers are based on the data extracted from the $\varphi - i$ plane. The horizontal component of the knee point is core current and its vertical component is core flux. However, the actual manufacturer curves may not always have the same coordinates. As a matter of fact, in some practical cases the manufacturer provides the B - H curve of the core or in other occasions the v - i curve.

The manufacturer datasheets have to be rescaled and coordinates have to be changed into φ and i before extracting core data for the present models. This is a linear one to one transformation therefore an auxiliary program which reads data from the φ - i plane and converts them to B -H pairs can be regarded in the future development of the models.

7.5 - Frequency Limitation

EMTDC analyzes electrical circuits in the time domain. When used as the software of a digital simulator, the time step of EMTDC is confined to 50 microseconds, which is due to the present limitations of digital simulator.

The period of a 60 Hz sinosoid is 16667 microseconds . When a digital simulator reproduces this waveform there will be 16667 / 50 = 333 discrete points recognized by the simulator on each cycle of the waveform. The 332 small segments between the successive points reproduce the original sinosoid. If the frequency of oscillation decreases to 10 Hz (period = 0.1 second), the number of discrete points on one cycle increases to 100000/50 = 2000. In other words, a digital simulator simulates a 10 Hz sinosoid by 1999 line segments. Compared to the 60 Hz wave, this is a more accurately simulated waveform. As the frequency of the sinosoid decreases, the simulated wave approaches the original one. In fact, the simulated DC is exactly the same as the original DC wave.

The frequency response of capacitive voltage transformers is already investigated in the literature. Lucas [16] presents an EMTDC model of capacitive voltage transformers, which has a relatively flat frequency response up to 1000.0 Hz.

The reliability of the frequency response of the computer model of a CVT is checked versus the experimentally recorded frequency response of the same CVT [17]. The results are in good agreement.

The step change of currents and voltages in an electrical network contains a wide spectrum of frequency. To duplicate the exact step function, a digital simulator has to be able to reproduce all the high frequency components. However, the higher frequencies are filtered out and the reproduced waveform does not have the same sharp corner of the original step function.

Bandwidth constraint also affects the modeling of stray capacitances . As an example, the power frequency impedance of a 5 picofarad capacitor is 530 megaohms, which is virtually an open circuit. At 1.0 KHz, this impedance decreases to 32 megaohms which is still very high and can be neglected. This example explains why the stray and interwinding capacitances are ignored in the developed models.

7.6 - Practical Problems

Most of the problems which were discovered during the development and testing of the models of instrument transformers were due to circuit instability caused by a single inductor between a node and ground. The stabilizing technique which overcomes this type of numerical instability is explained in chapter four and will not be repeated here.

Another problem is illustrated in Fig. 7.5 when the minor loop goes outside the parent loop. The voltage excitation of this datacase is DC + sinosoidal and all the initial conditions are set to zero. The reason for this odd response is that in one time step the core emf, which is initially set equal to zero, suddenly jumps to some positive value corresponding to the DC level. This in turn causes a sharp increase in the core current such that the current drawn by the core in the first time step even exceeds the steady core current. Such a sharp change of core flux never occurs in the real world. To overcome the problem, the expression of the superimposed DC excitation was modified. The DC level was replaced by an exponential function which starts at zero DC level at $t = 0$ and reaches the desired DC level at $t = \tau$. For times greater than τ the DC remains constant at the desired level. Therefore for $t > \tau$ the excitation is DC + sinosoid. However, the step rise of the excitation voltage from zero at $t = 0$ to DC at $t = \Delta t$ is replaced by a gradual rise in τ seconds. The new excitation was tested and overshoot was eliminated. Fig. 7.6 shows the hysteresis loop following the implementation of the exponential approach.

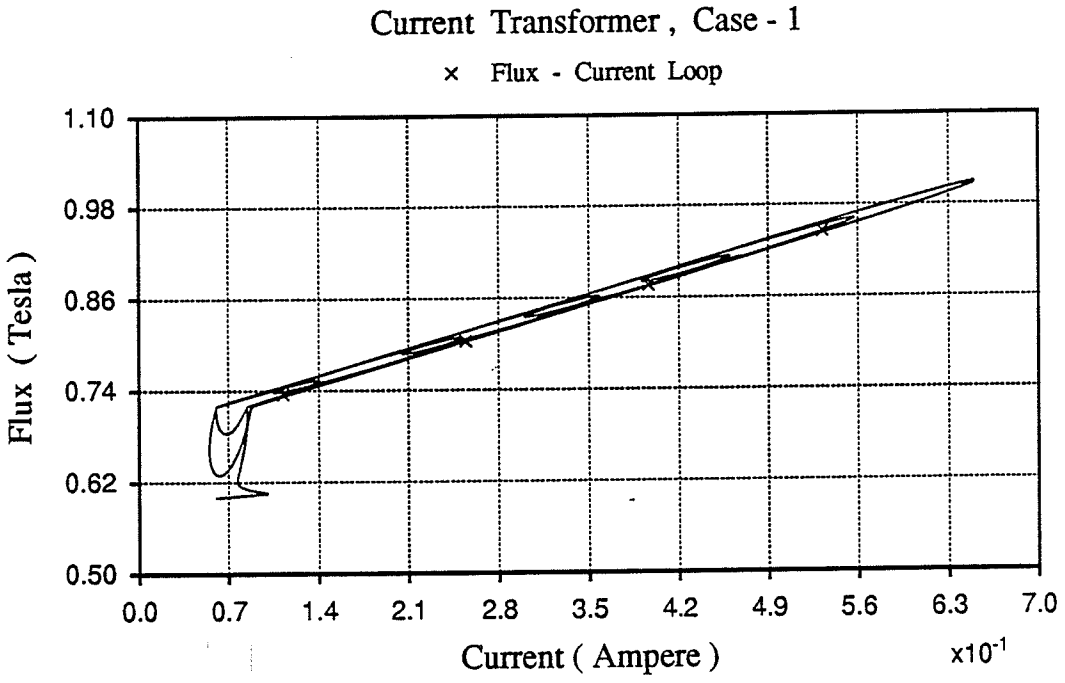


Fig. 7.5 - The Sudden Change of the Core Current

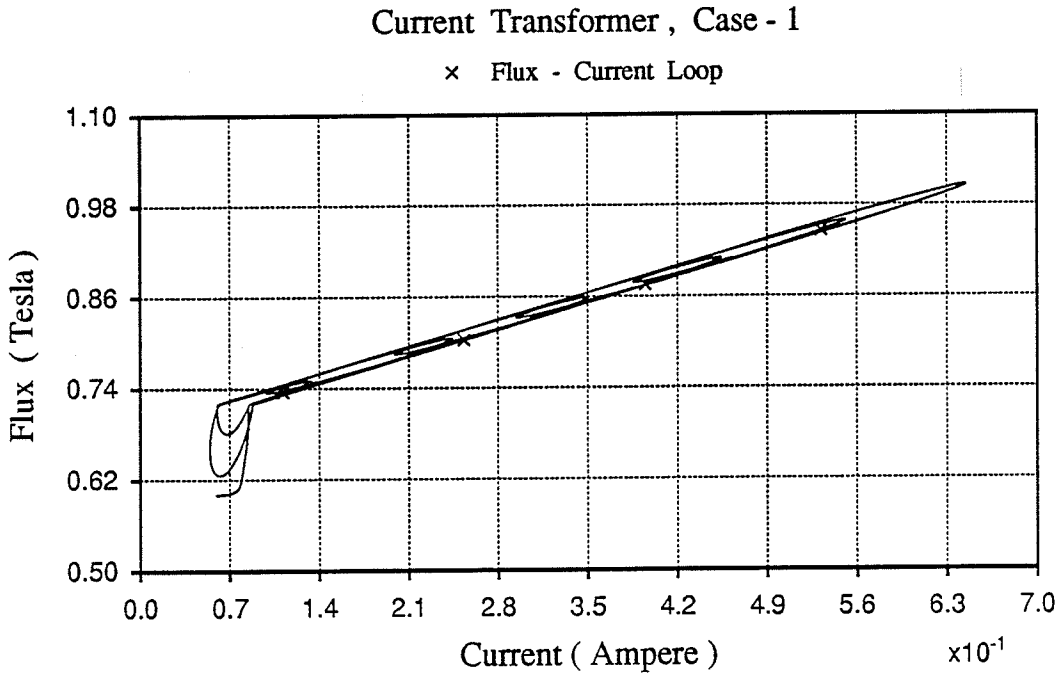


Fig. 7.6 - The Gradual Change of the Core Current

APPENDIX 1

APPENDIX 1

Sample datafiles and computer printouts of the current transformer models are included in this appendix. As mentioned earlier in chapter four, the current transformer is modeled in two different ways. In the first approach which is referred to as *case 1* throughout the text, the core magnetizing branch is modeled as an inductor with two slopes and the core losses are taken care of by paralleling a constant linear resistor to the magnetizing inductor. In *case 2*, however, the flux - current loop is modeled as a single body with adjustable slopes and resistive loss. As expected, the results of both cases for similar excitations are very close. To give the reader a brief overview of what each subroutine is capable of doing, computer printouts of each model for the following typical excitations are attached :

A) Sixty Hertz sinosoidal excitation to observe the inrush current and the steady state parent loop. The current transformer default parameters are chosen such that the core goes into saturation at each cycle.

B) Superimposed DC on sinosoidal sixty hertz excitation to investigate the effect of DC current in the saturation of core. In the real world such a DC component can be from different sources, among them geomagnetically induced current or *GIC* [15].

C) Decaying sixty hertz sinosoidal to illustrate minor loops. The user can decide about the models by comparing the minor loops of each model to those of manufacturer's data sheets and selecting the one which is in closer agreement with practical data.

The fundamental 60 Hz frequency is chosen for convenience, but any linear summation of frequencies from DC up to 1000 Hz can be used as the excitation.

Altogether six sets of computer printouts are shown in appendix one. Each set includes the following graphs :

1 - The core current

2 - The hysteresis loop

3 - The burden current

The model and excitation of each set is :

SET 1 : CASE 1 with sinosoidal excitation.

SET 2 : CASE 1 with superimposed DC on sinosoidal excitation.

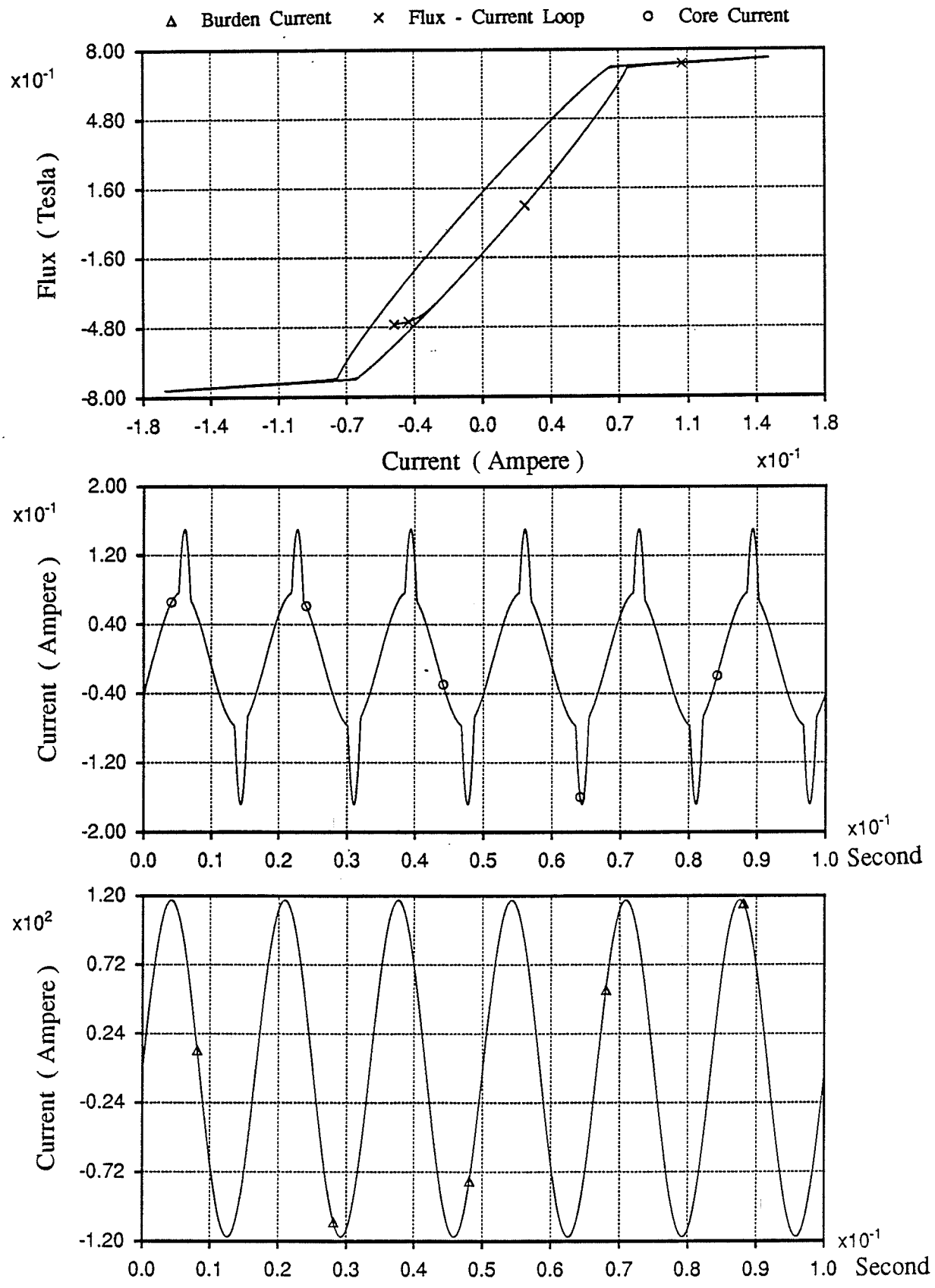
SET 3 : CASE 1 with decaying sinosoidal excitation.

SET 4 : CASE 2 with sinosoidal excitation.

SET 5 : CASE 2 with superimposed DC on sinosoidal excitation.

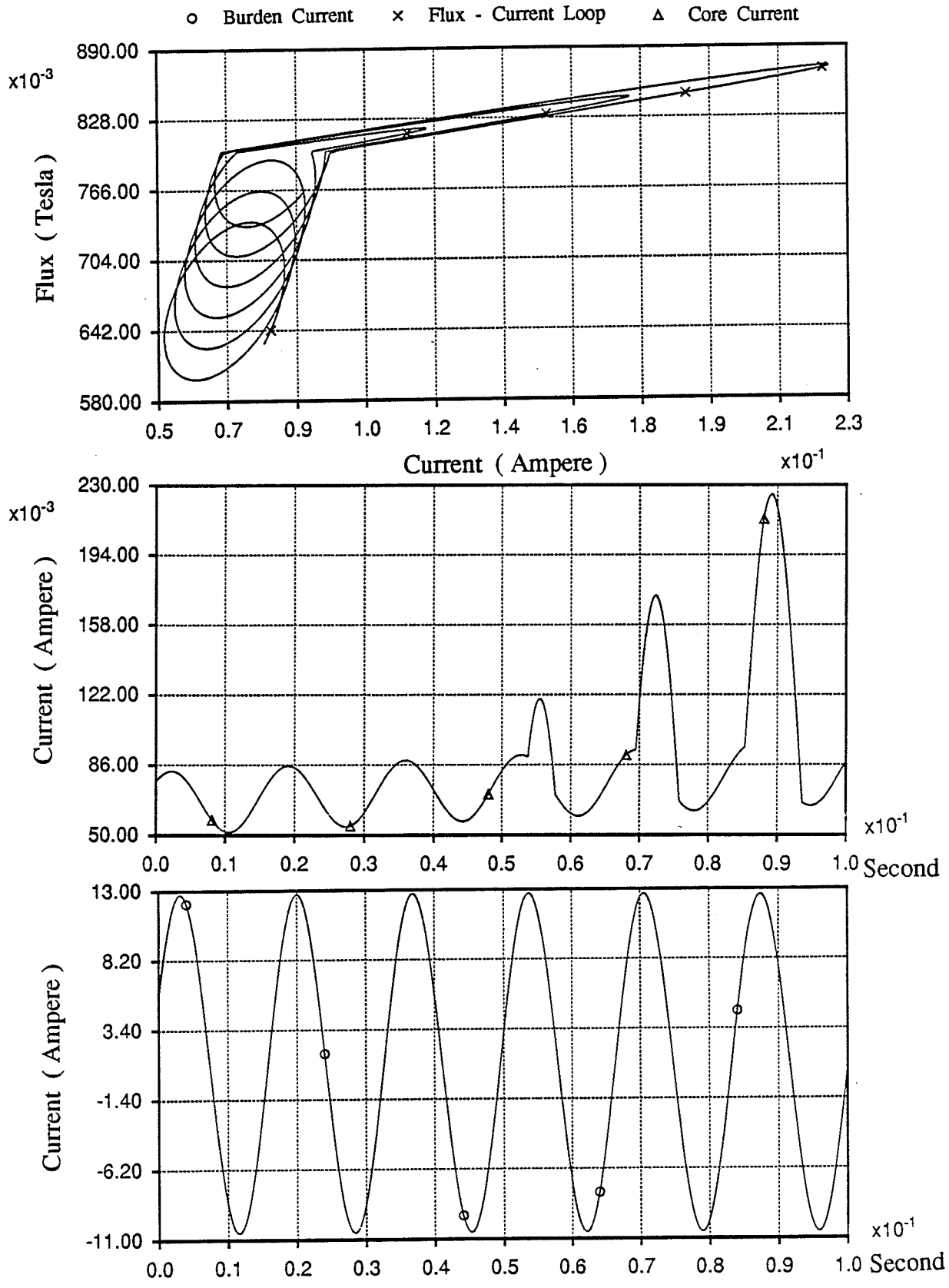
SET 6 : CASE 2 with decaying sinosoidal excitation.

```
DATAFILE OF SUBROUTINE CT9 ( CASE 1 ) - SET 1/ TITLE
  5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  2                               / NUMBER OF NODES
   0.  0.                         / INITIAL NODE VOLTAGES
  1  2  1.E-2  0.  0.             / NETWORK BRANCHES
  2  0  9.  0.  0.                /
999                               / TERMINATES BRANCH DATA
  1  99.E-2                       / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -100   100                      / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    2.    1.    -0.47    0.    0.    0.    0.72    10.    0.5
    2.E+4    240.    1.5    5.E-3    40.    280900.  /
  IFRO, ITO, NS, FLUX0, VOLT0, CURNT0, VC0, FAIKNE, SLIN,
  SSAT, RLOSS, RATIO, BR, BL, R, VMAX
```

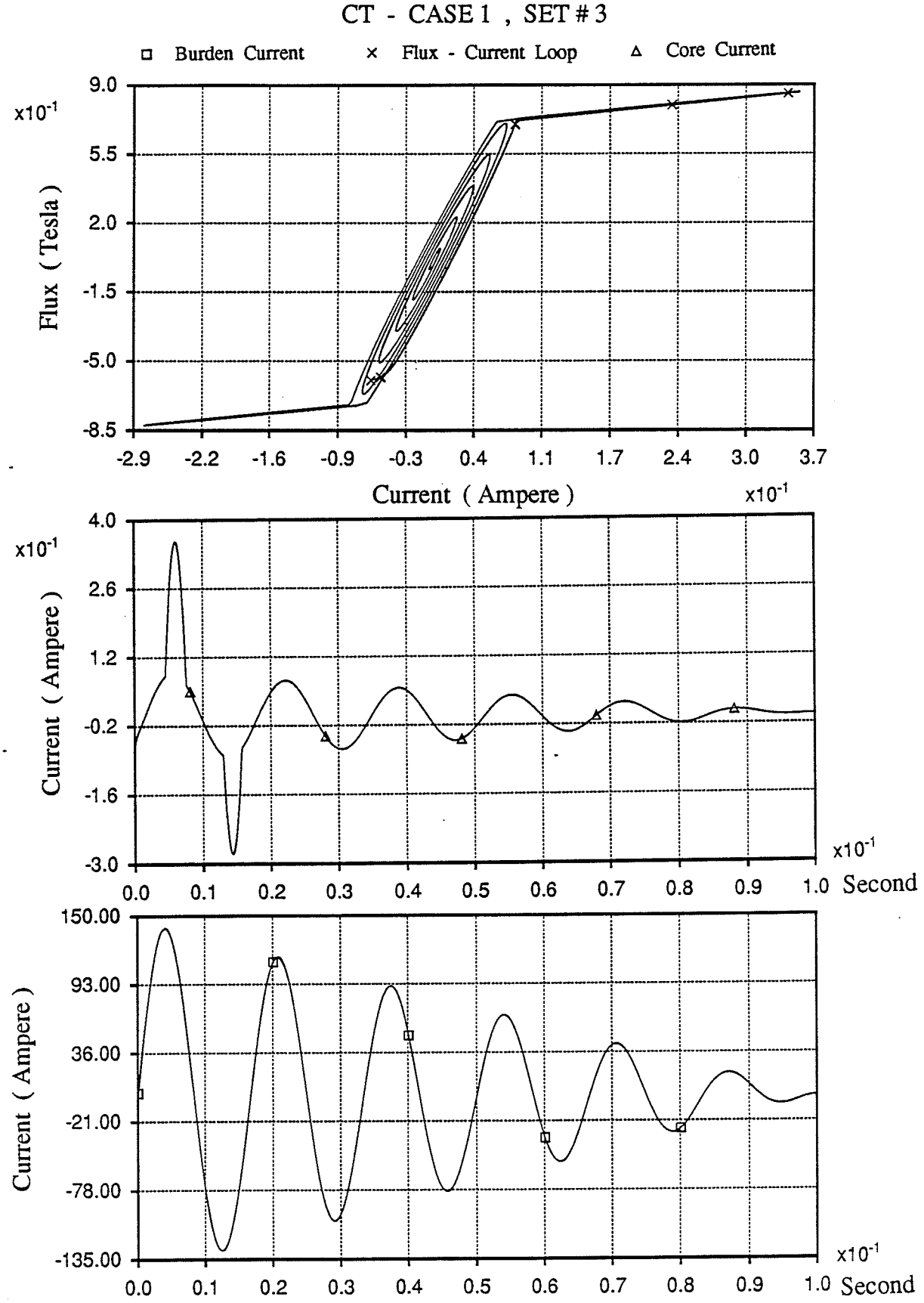

CT - CASE 1 , SET # 1
Δ Burden Current
× Flux - Current Loop
o Core Current
x10-1
8.00
4.80
1.60
-1.60
-4.80
-8.00
Flux (Tesla)
-1.8
-1.4
-1.1
-0.7
-0.4
0.0
0.4
0.7
1.1
1.4
1.8
Current (Ampere)
x10-1
x10-1
2.00
1.20
0.40
-0.40
-1.20
-2.00
Current (Ampere)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
x10-1
Second
x102
1.20
0.72
0.24
-0.24
-0.72
-1.20
Current (Ampere)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
x10-1
Second

```
DATAFILE OF SUBROUTINE CT9 ( CASE 1 ) - SET 2/ TITLE
   5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   2                               / NUMBER OF NODES
    0.  0.                         / INITIAL NODE VOLTAGES
   1  2  1.E-2  0.  0.             / NETWORK BRANCHES
   2  0  9.  0.  0.                /
999                                / TERMINATES BRANCH DATA
   1  99.E-2                       / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
   -100   100                     / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.    2.    1.    0.6     0.    0.    0.    0.8    10.    0.5
     2.E+3     240.    1.5     5.E-3    40.    27940.  /
    IFRO, ITO, NS, FLUX0, VOLT0, CURNT0, VC0, FAIKNE, SLIN,
    SSAT, RLOSS, RATIO, BR, BL, R, VMAX
```

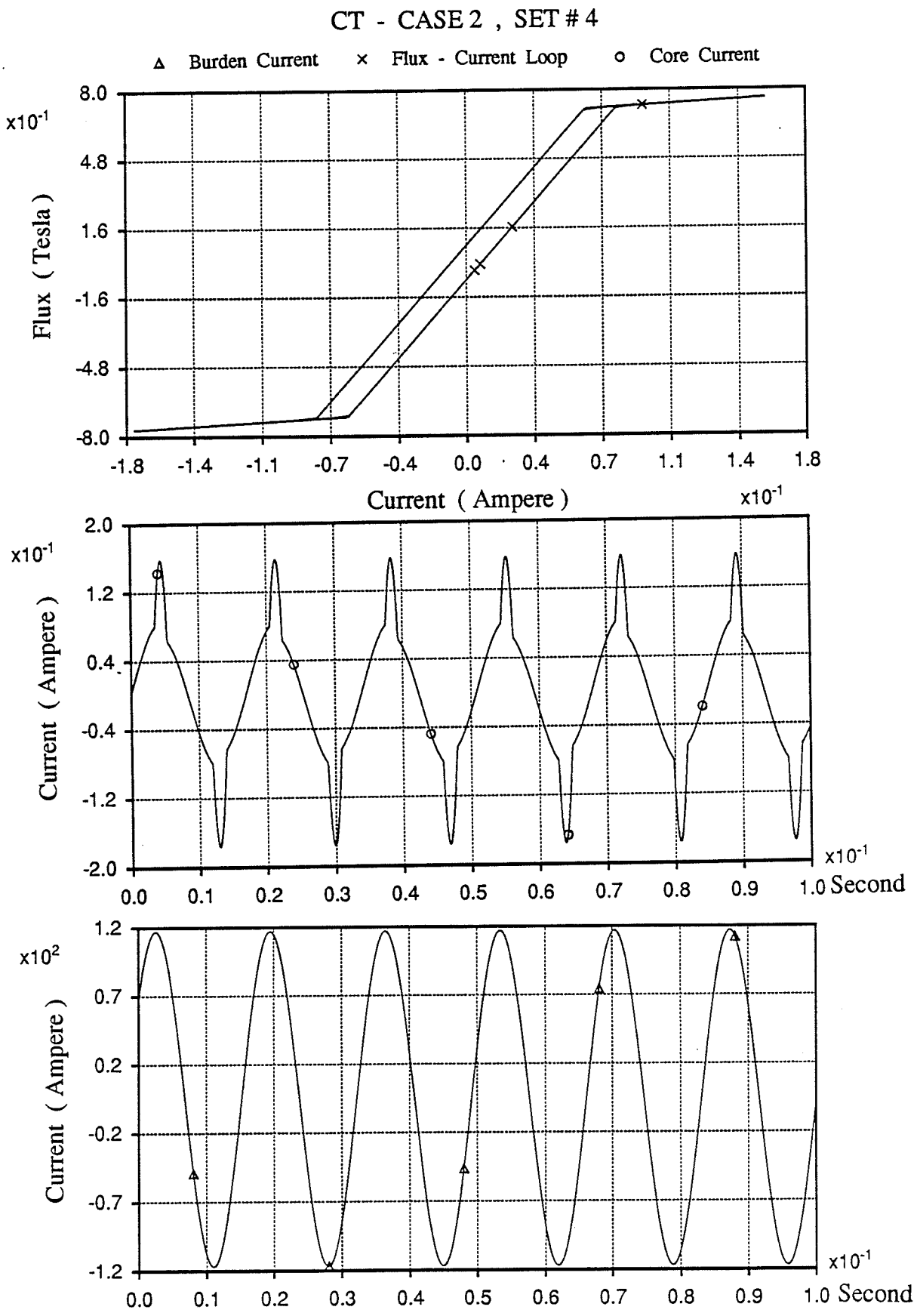
CT - CASE 1 , SET # 2



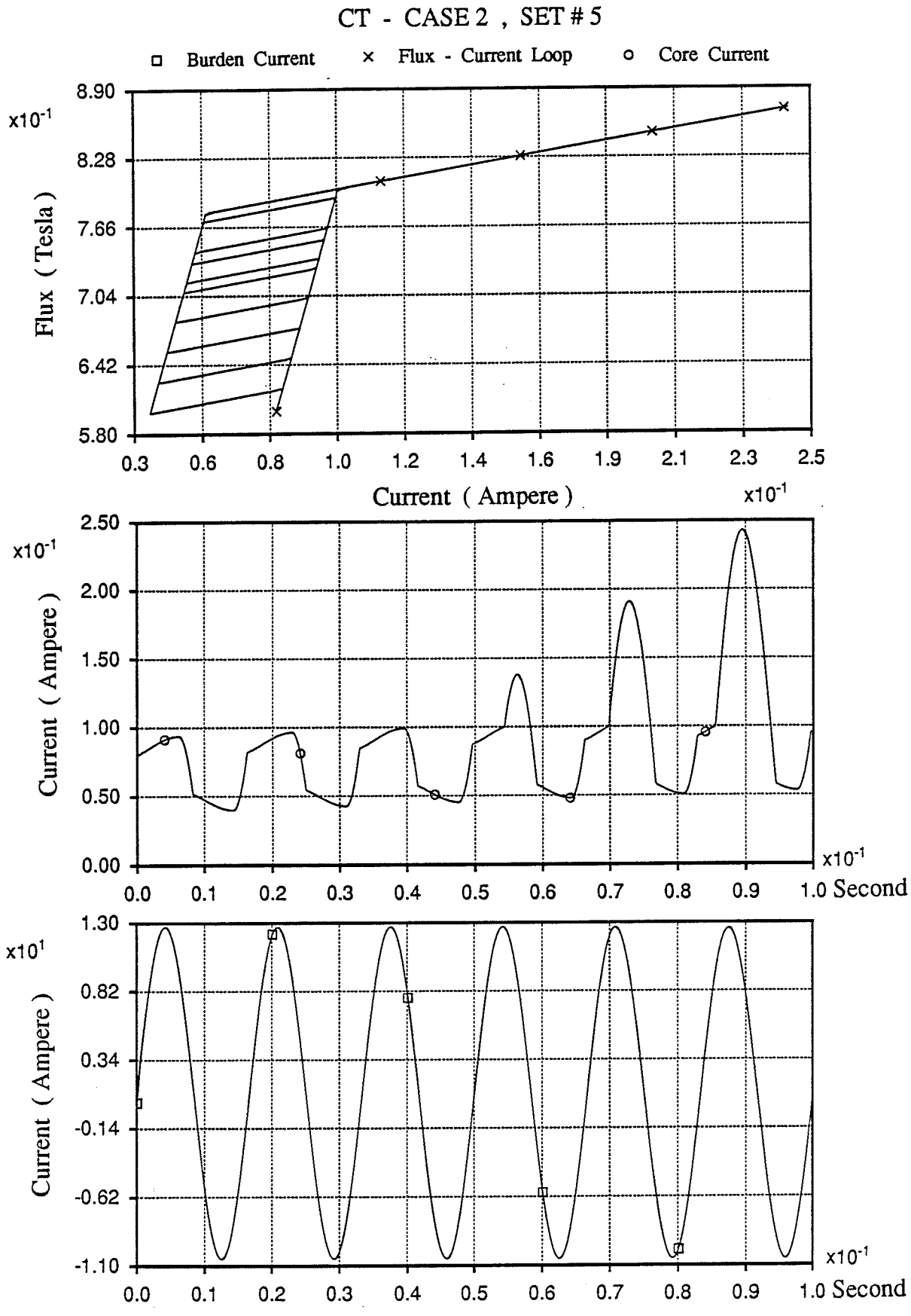
```
DATAFILE OF SUBROUTINE CT9 ( CASE 1 ) - SET 3/ TITLE
  5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  2                               / NUMBER OF NODES
   0.  0.                         / INITIAL NODE VOLTAGES
  1  2  1.E-2  0.  0.             / NETWORK BRANCHES
  2  0  9.  0.  0.                /
999                               / TERMINATES BRANCH DATA
  1  99.E-2                       / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -100   100                      / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    2.    1.    -0.6    0.    0.    0.    0.72    10.    0.5
    2.E+4    240.    1.5    5.E-3    40.    350000.  /
  IFRO, ITO, NS, FLUX0, VOLT0, CURNT0, VC0, FAIKNE, SLIN,
  SSAT, RLOSS, RATIO, BR, BL, R, VMAX
```


CT - CASE 1 , SET # 3
Burden Current
Flux - Current Loop
Core Current
x10-1
9.0
5.5
2.0
-1.5
-5.0
-8.5
Flux (Tesla)
-2.9
-2.2
-1.6
-0.9
-0.3
0.4
1.1
1.7
2.4
3.0
3.7
Current (Ampere)
x10-1
x10-1
4.0
2.6
1.2
-0.2
-1.6
-3.0
Current (Ampere)
x10-1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Second
150.00
93.00
36.00
-21.00
-78.00
-135.00
Current (Ampere)
x10-1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Second

```
DATAFILE OF SUBROUTINE CT9 ( CASE 2 ) - SET 4/ TITLE
  5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  2                               / NUMBER OF NODES
   0.  0.                         / INITIAL NODE VOLTAGES
  1  2  1.E-2  0.  0.             / NETWORK BRANCHES
  2  0  9.  0.  0.                /
999                               / TERMINATES BRANCH DATA
  1  99.E-2                       / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -100   100                      / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    2.    1.    -0.47    0.    0.    0.    0.    0.72    0.08    10.
    0.5    240.    1.5    5.E-3    40.    280900.  /
  IFRO, ITO, NS, FLUX0, VOLT0, CUREQ0, VC0, REMANT,FAIKNE,
  CURKNE,SLIN,SSAT, RATIO, BR, BL, R, VMAX
```

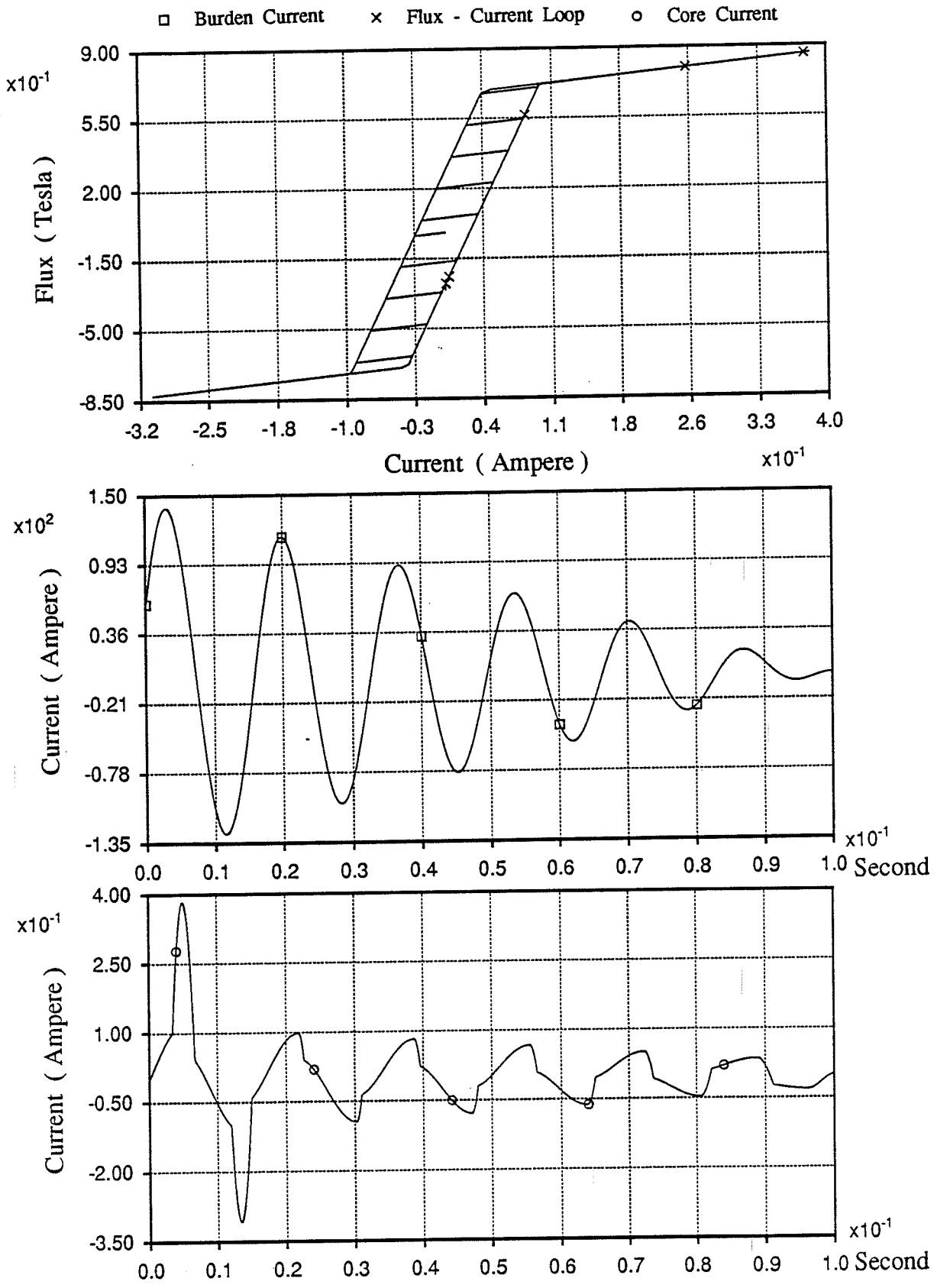

CT - CASE 2 , SET # 4
Burden Current
Flux - Current Loop
Core Current
x10-1
8.0
4.8
1.6
-1.6
-4.8
-8.0
Flux (Tesla)
-1.8 -1.4 -1.1 -0.7 -0.4 0.0 0.4 0.7 1.1 1.4 1.8
Current (Ampere)
x10-1
x10-1
2.0
1.2
0.4
-0.4
-1.2
-2.0
Current (Ampere)
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 Second
x10-1
x10²
1.2
0.7
0.2
-0.2
-0.7
-1.2
Current (Ampere)
0.0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1.0 Second
x10-1

```
DATAFILE OF SUBROUTINE CT9 ( CASE 2 ) - SET 5/ TITLE
  5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  2                               / NUMBER OF NODES
   0.  0.                         / INITIAL NODE VOLTAGES
  1  2  1.E-2  0.  0.             / NETWORK BRANCHES
  2  0  9.  0.  0.                /
999                               / TERMINATES BRANCH DATA
  1 99.E-2                        / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -100  100                       / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    2.    1.    0.6    0.    0.    0.    0.    0.8    0.1    10.
    0.5    240.    1.5    5.E-3    40.    27940.  /
  IFRO, ITO, NS, FLUX0, VOLT0, CUREQ0, VC0, REMANT,FAIKNE,
  CURKNE,SLIN,SSAT, RATIO, BR, BL, R, VMAX
```


CT - CASE 2 , SET # 5
Burden Current
Flux - Current Loop
Core Current
x10-1
8.90
8.28
7.66
7.04
6.42
5.80
Flux (Tesla)
0.3
0.6
0.8
1.0
1.2
1.4
1.6
1.9
2.1
2.3
2.5
Current (Ampere)
x10-1
x10-1
2.50
2.00
1.50
1.00
0.50
0.00
Current (Ampere)
x10-1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0 Second
x10-1
1.30
0.82
0.34
-0.14
-0.62
-1.10
Current (Ampere)
x10-1
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0 Second

```
DATAFILE OF SUBROUTINE CT9 ( CASE 2 ) - SET 6/ TITLE
   5.E-5   1.E-1   10.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   2                               / NUMBER OF NODES
    0.  0.                         / INITIAL NODE VOLTAGES
   1  2  1.E-2  0.  0.             / NETWORK BRANCHES
   2  0  9.  0.  0.                /
999                                / TERMINATES BRANCH DATA
  1 99.E-2                         / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
   -100   100                      / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.    2.    1.    -0.6    0.    0.    0.    0.    0.72    0.1    10.
     0.5    240.    1.5    5.E-3    40.    350000.  /
   IFRO, ITO, NS, FLUX0, VOLT0, CUREQ0, VC0, REMANT,FAIKNE,
   CURKNE,SLIN,SSAT, RATIO, BR, BL, R, VMAX
```

CT - CASE 2 , SET # 6



APPENDIX 2

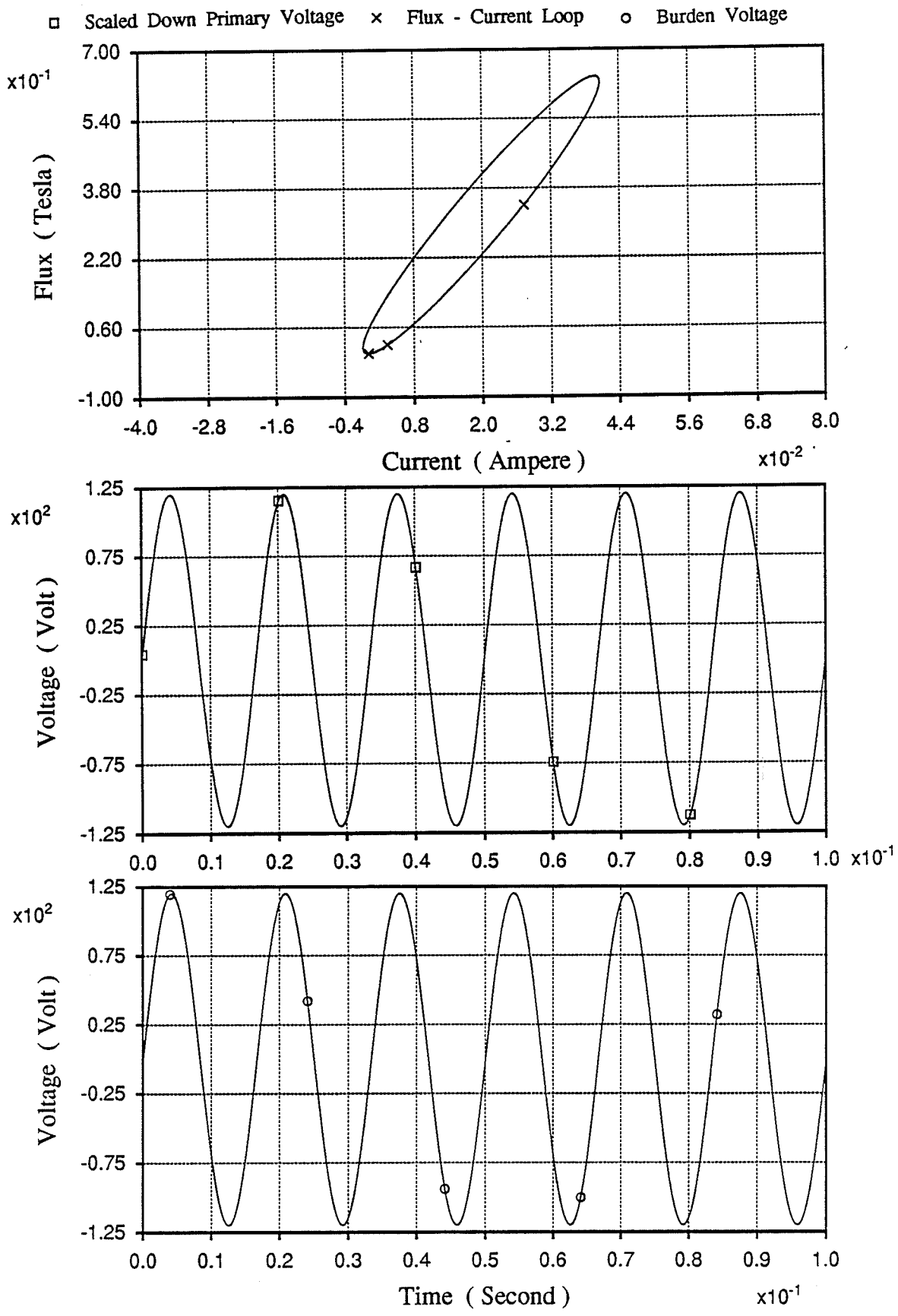
APPENDIX 2

Appendix 2 includes datafiles and sample computer outputs of the model of potential transformers. The subroutine is called *pt2* , and its structure is discussed in chapter five. Illustrative examples of appendix 2 deal with two different types of operating conditions. The first set of data is arranged in such a way that the core of the potential transformer does not go into the saturation region, and therefore the core current is free of harmonics. The second case, however, deals with a core wich is forced into the saturation. Saturation is achieved by shifting the knee point current coordinate in the EMTDC datafile. In both cases the burden voltage is very close to the scaled down primary voltage, and the difference is negligible. This is in accordance with the theoretical facts reviewed in chapter five. In appendix 2 the computer plot of the flux - current loop is also shown to indicate core situation.

Here again 60 Hz primary voltage is chosen for convenience, but the argument of appendix 1 regarding excitations with frequencies from DC to 1000 Hz is still valid.

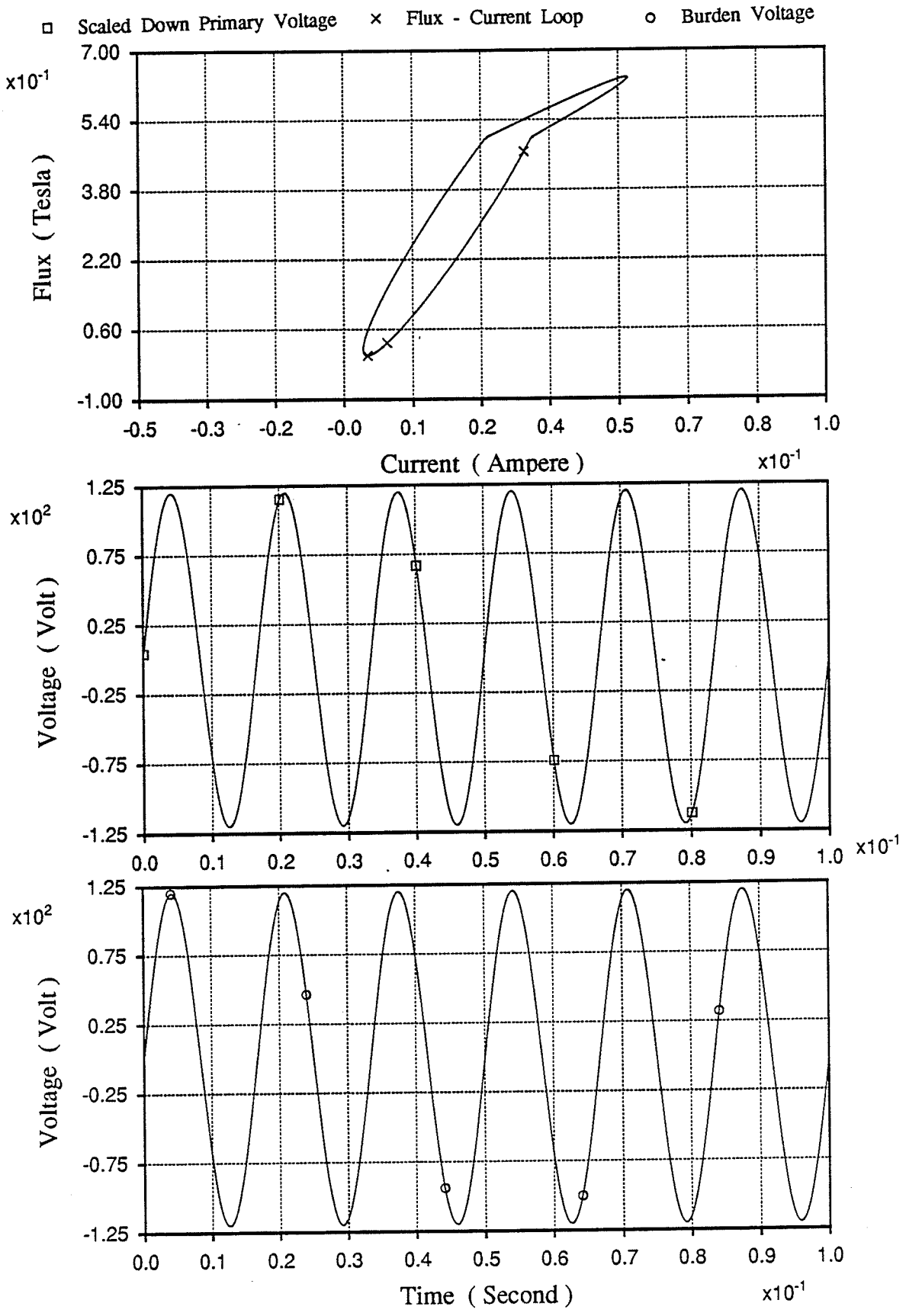
```
DATAFILE OF SUBROUTINE PT2 ( UNSATURATED CORE ) / TITLE
  5.E-5  1.E-1  10.E-5          / DELT, FINTIM, PRTSTP
  1                             / ONE SUBSYSTEM
  6                             / NUMBER OF NODES
  0.                            / INITIAL NODE VOLTAGES
  1    2    0.    4.E-8    0.  / NETWORK  BRANCHES
  2    0    0.    0.32     0.  /
  2    3    200.  0.       0.  /
  3    0    200.  0.       0.  /
  2    4    .005  0.       0.  /
  4    5    0.    1.E-4    0.  /
  5    6    0.    1.E-4    0.  /
  6    0    1.E8  0.       0.  /
999                             / TERMINATES BRANCH DATA
  1  5.E-5  0.  0.  0.  0.      / SOURCE DATA
999                             / TERMINATES SOURCE DATA
999                             / TERMINATES TRANSFORMER DATA
999                             / TERMINATES T-LINE DATA
 -120   120                     / PRINTPLOT LIMITS
 10                             / NUMBER OF OUTPUT CHANNELS
  1.E6   800.   8.  .0013  0.  1.E3  20.  6.E3  1.  1.  -148.E-3 /
  RLOSS,  SLIN, SSAT, CURKNE, FLUX0, PN, SN, VMAX,
  NODE, NS, TS
```

PT WITH UNSATURATED CORE



```
DATAFILE OF SUBROUTINE PT2 ( SATURATED CORE ) / TITLE
  5.E-5   1.E-1   10.E-5              / DELT, FINTIM, PRTSTP
  1                                   / ONE SUBSYSTEM
  6                                   / NUMBER OF NODES
  0.                                  / INITIAL NODE VOLTAGES
  1    2    0.    4.E-8    0.    / NETWORK  BRANCHES
  2    0    0.    0.32     0.  /
  2    3    200.  0.       0.  /
  3    0    200.  0.       0.  /
  2    4    .005  0.       0.  /
  4    5    0.    1.E-4    0.  /
  5    6    0.    1.E-4    0.  /
  6    0    1.E8  0.       0.  /
999                                   / TERMINATES BRANCH DATA
  1   5.E-5  0.  0.  0.  0.       / SOURCE DATA
999                                   / TERMINATES SOURCE DATA
999                                   / TERMINATES TRANSFORMER DATA
999                                   / TERMINATES T-LINE DATA
  -120   120                          / PRINTPLOT LIMITS
  10                                  / NUMBER OF OUTPUT CHANNELS
   1.E6   800.   8.  625.E-6  0.  1.E3  20.  6.E3  1.  1.  -148.E-3 /
   RLOSS,  SLIN, SSAT, CURKNE, FLUX0, PN, SN, VMAX,
   NODE, NS, TS
```

PT WITH SATURATED CORE



APPENDIX 3

APPENDIX 3

The conclusions of chapter six regarding the factors which affect subsidence transient voltage in capacitive voltage transformers are confirmed in appendix 3.

Ten different sets of plots are included in appendix 3. These are *set # 1a, set # 1b, . . ., set # 5a and set # 5b*. Each case differs from the other cases by one or more parameters in its datafile. Therefore the datafile of each set is placed prior to its graphs. The key parameters of each case and their special effect on the subsidence voltage of capacitive voltage transformers are listed later in this appendix. As in the two previous appendices, a 60 Hz sinosoidal is chosen as the excitation and again frequencies of 0 - 1000 Hz are applicable. A line to ground fault is simulated through the subroutine DSDYN to generate subsidence voltage. The instant of fault is changeable and can be fixed by the user through the datafile. Other circuit parameters which affect the transient response of the model following a fault are also placed in the datafile and are adjustable.

Two plots are presented for each set. The first graph of each set is the scaled down Thevenin voltage of the potential transformer. The instant of fault is shown here. The second one is the burden voltage prior to and after the fault. The amplitude and decaying time of the subsidence transient voltage following the fault can be observed.

The reader will be able to compare the magnitude and time constant of different ferroresonant cases by referring to this plot of each set.The function of each set is:

set # 1a : Effect of zero fault initiation, core is not saturated.

set # 1b : Effect of crest fault initiation, all the parameters are the same as in the previous set except for the instant of fault.

set # 2a : Effect of decreasing the equivalent capacitance of set # 1a.

set # 2b : Effect of decreasing the equivalent capacitance of set # 1b.

set # 3a : Effect of variation of turns ratio, n = 50, zero fault initiation, core is not saturated.

set # 3b : Effect of variation of turns ratio, n = 200, zero fault initiation, core is saturated.

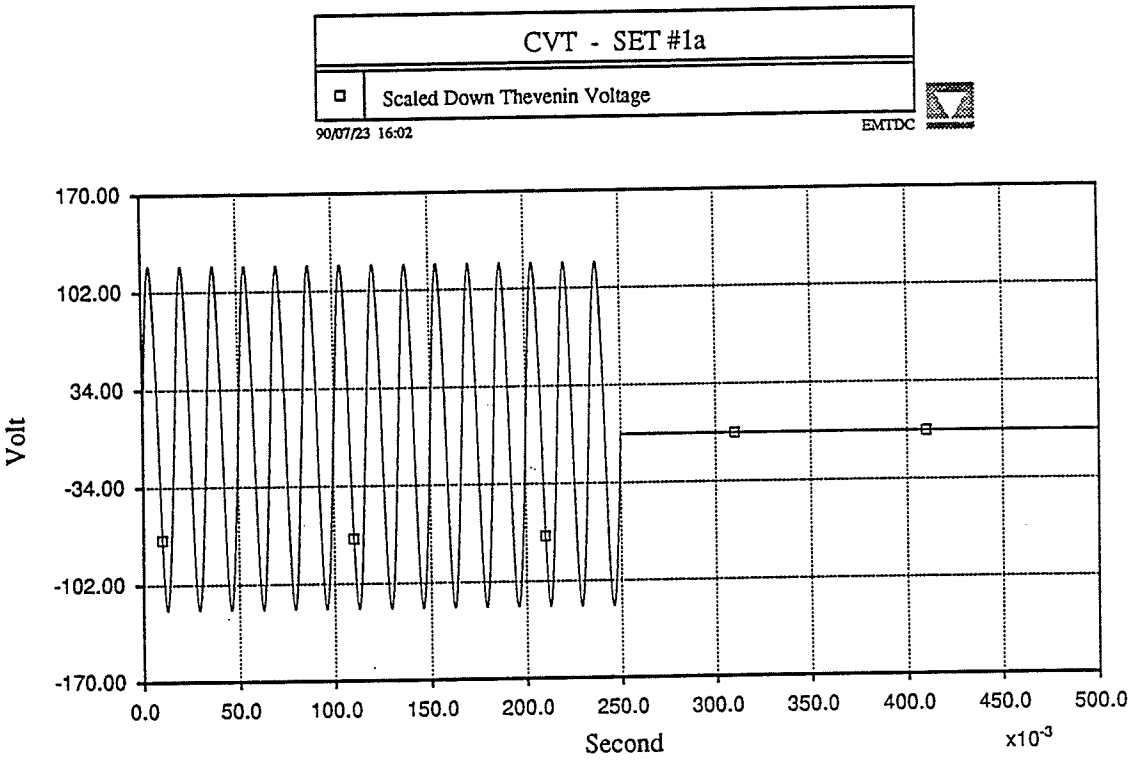
set # 4a : Effect of decreasing the load magnitude at zero fault initiation (from 36 Ohms in set # 1a to 6 Ohms), core is not saturated.

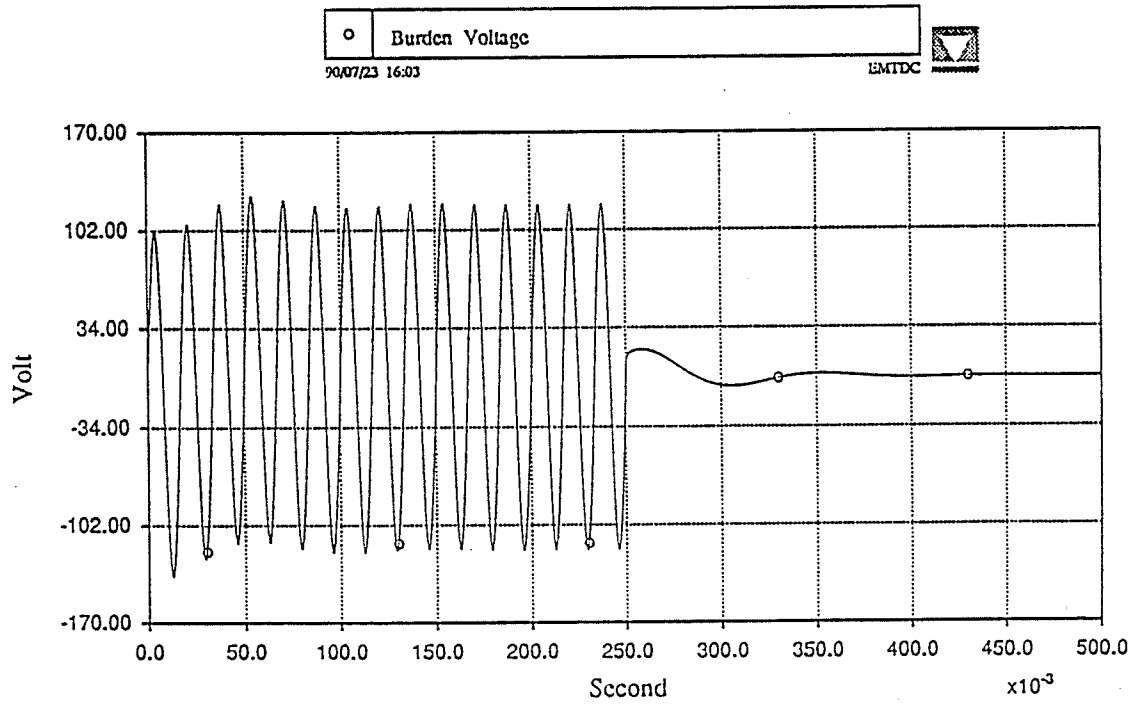
set # 4b : Effect of decreasing the load magnitude at crest fault initiation (from 36 Ohms in set # 1b to 6 Ohms), core is not saturated.

set # 5a : Effect of variation of load power factor, PF = 1.0, core is not saturated.

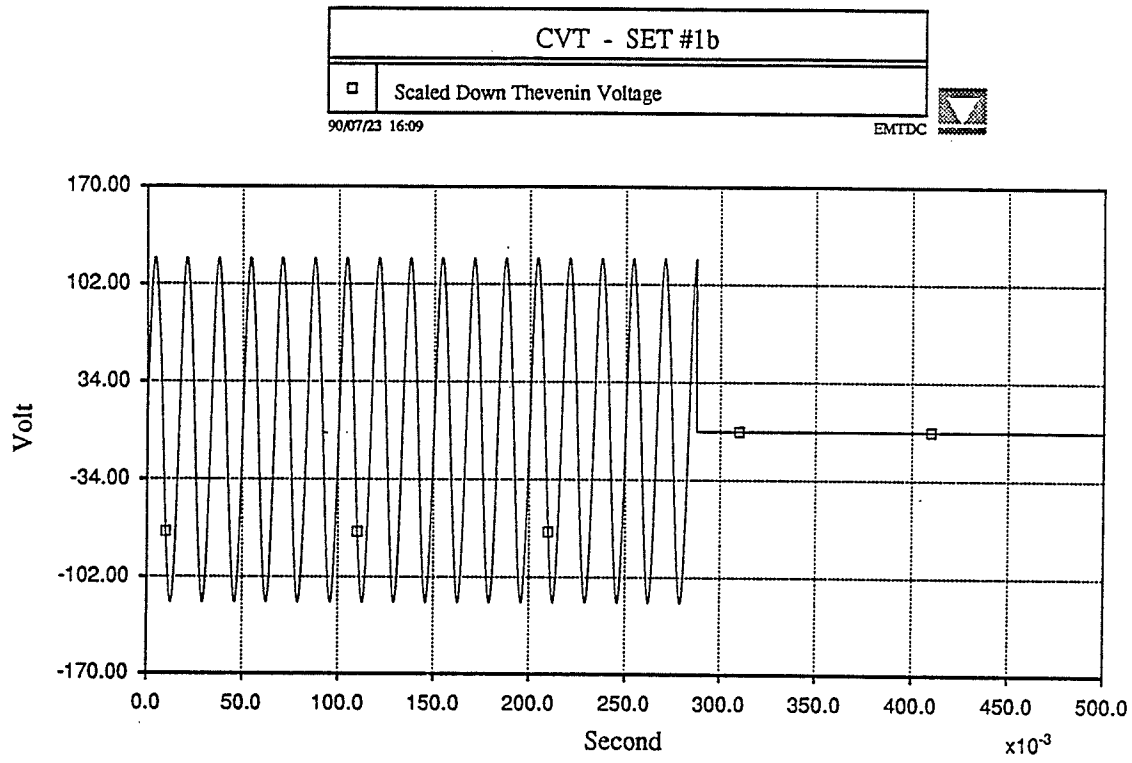
set # 5b : Effect of variation of load power factor, PF = 0.7, core is not saturated.

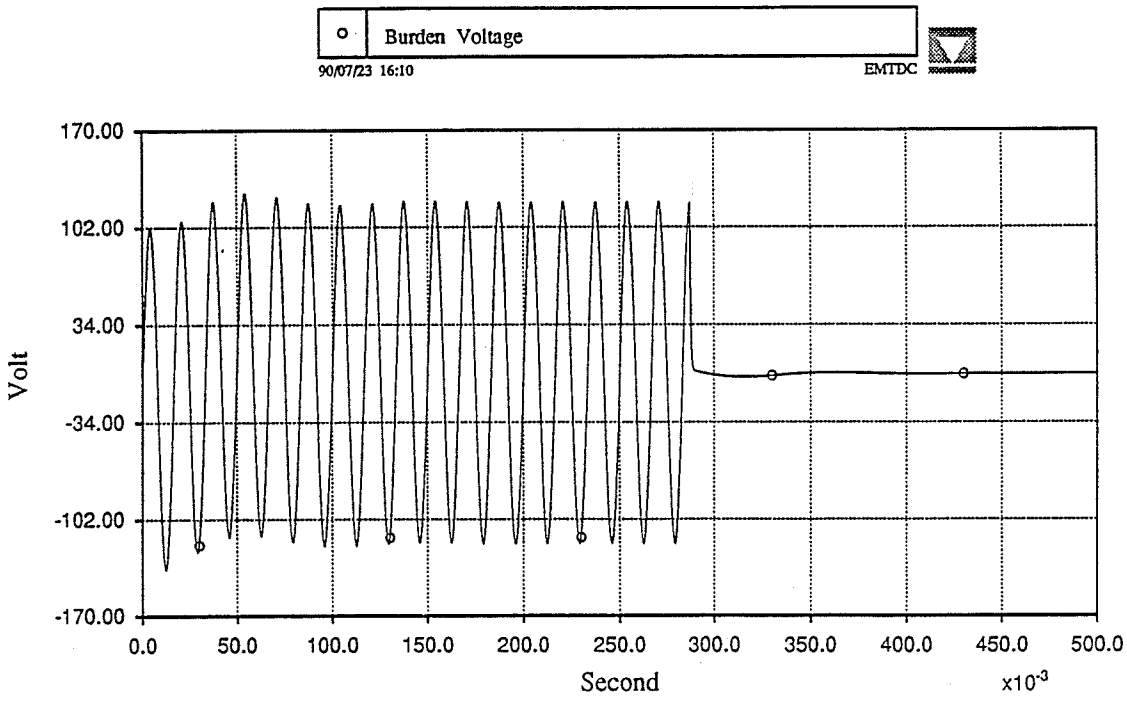
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 1a ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     610.       / capacitive divider (s.u. = scaled up)
   2  3   0.    12.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
   7  0   36.    0.     0.        / load resistance
999                                / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.        / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
   -120   120                      / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.    1.    .25    12.E4    .05    500.    10.    .0122
     0.2318    0.1    800.    8.    0.    -1.    .654  /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET #1a
Scaled Down Thevenin Voltage
90/07/23 16:02
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

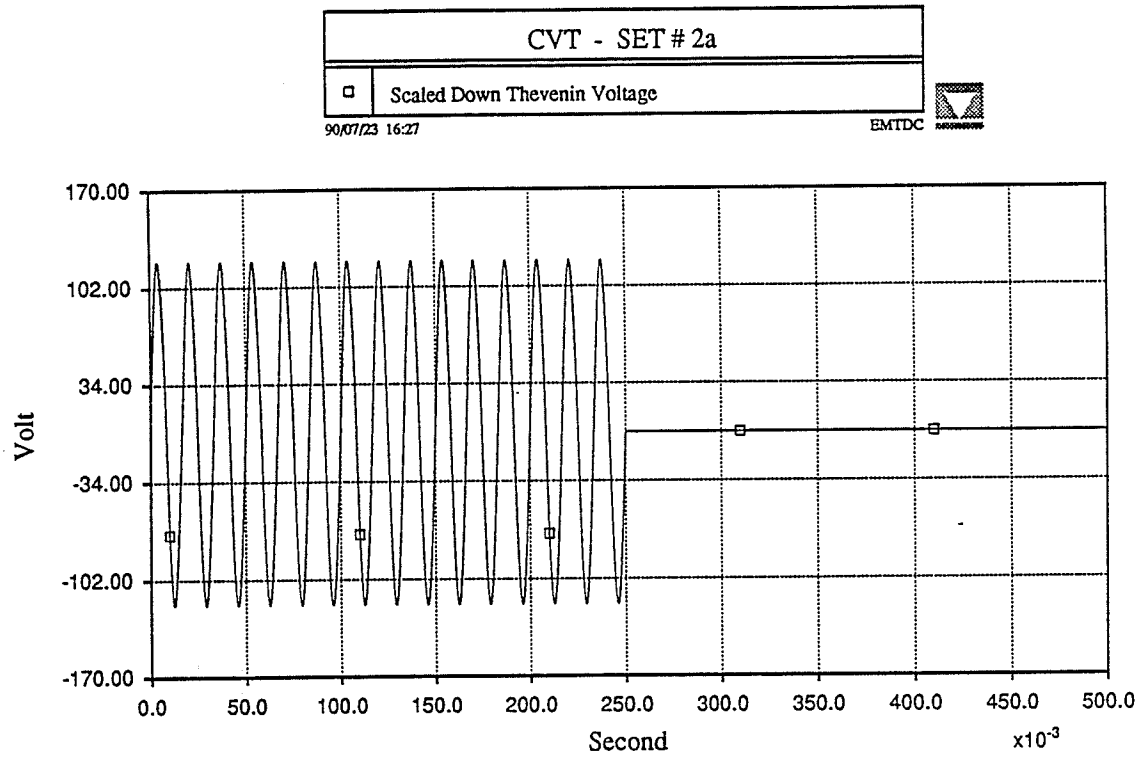

Burden Voltage
90/07/23 16:03
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

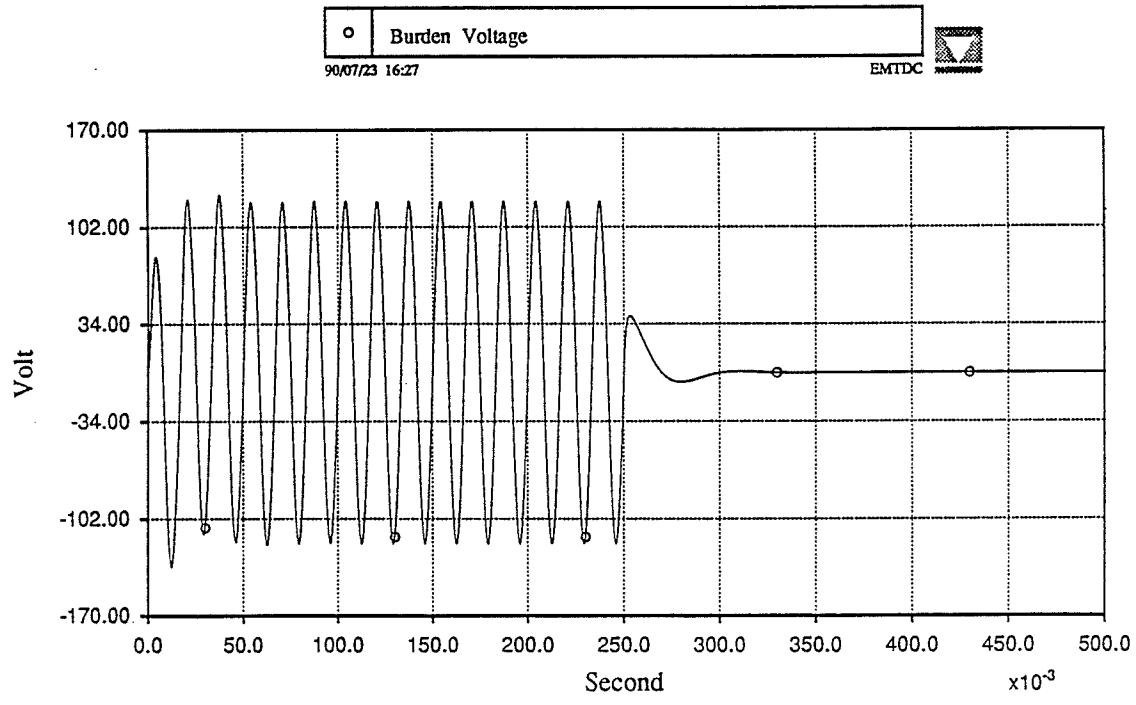
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 1b ) / TITLE
  5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  8                               / NUMBER OF NODES
  0.                              / INITIAL NODE VOLTAGES
  1  2   0.    0.     610.       / capacitive divider (s.u. = scaled up)
  2  3   0.    12.E-3  0.        / correcting inductor (s.d. = scaled down)
  3  4   1.E-2  0.     0.        / core saturation switch
  4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
  5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
  4  0   0.     .32    0.        / core linear slope (s. d.)
  3  6   .1     0.     0.        / secondary resistance
  6  7   0.    1.E-3   0.        / secondary inductance
 -7  8   0.    500.    0.        / suppression inductor
 -7  8   0.     0.  .83494       / suppression capacitor
  8  0   1.     0.     0.        / suppression resistor
  7  0   36.    0.     0.        / load resistance
999                               / TERMINATES BRANCH DATA
  1 1.E-2 0. 0. 0. 0.             / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -120  120                       / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    1.   2875.E-4    12.E4    .05    500.    10.    .0122
    0.2318   .1   800.   8.   0.   -1.   .654  /
  VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
  VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
  VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
  VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
  VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
  VAR(15)=FAULT CLEARING TIME
```


CVT - SET #1b
Scaled Down Thevenin Voltage
90/07/23 16:09
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

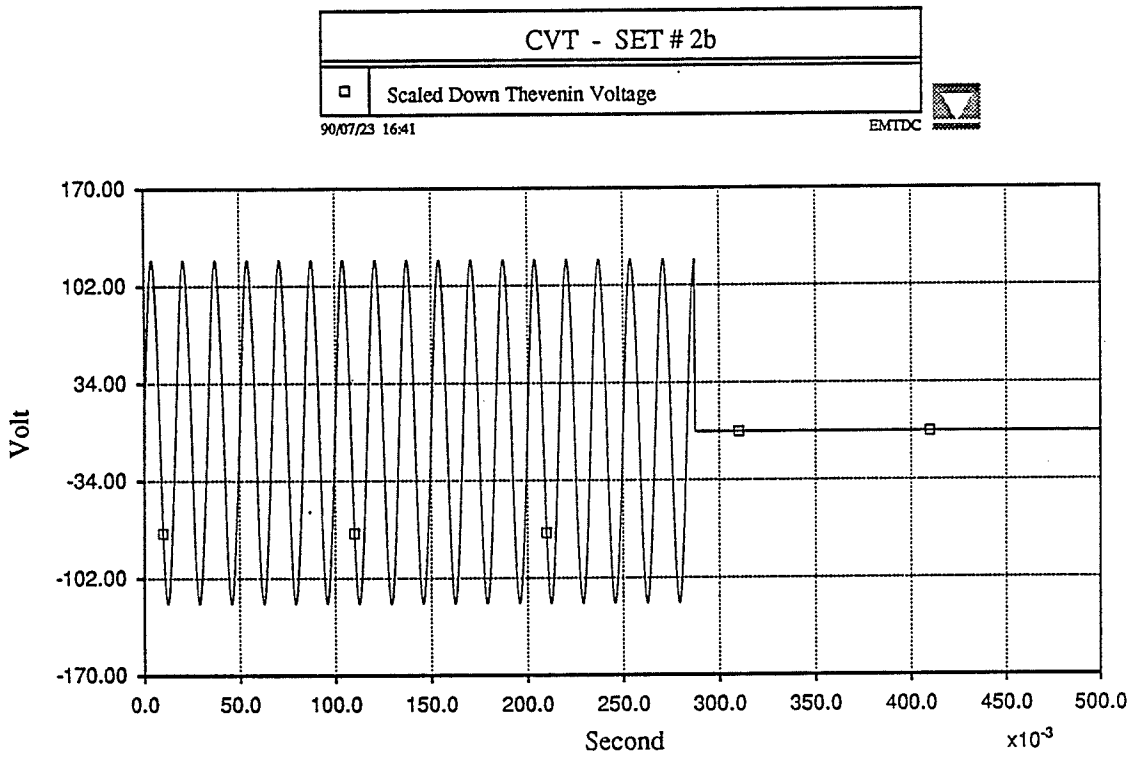

Burden Voltage
90/07/23 16:10
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

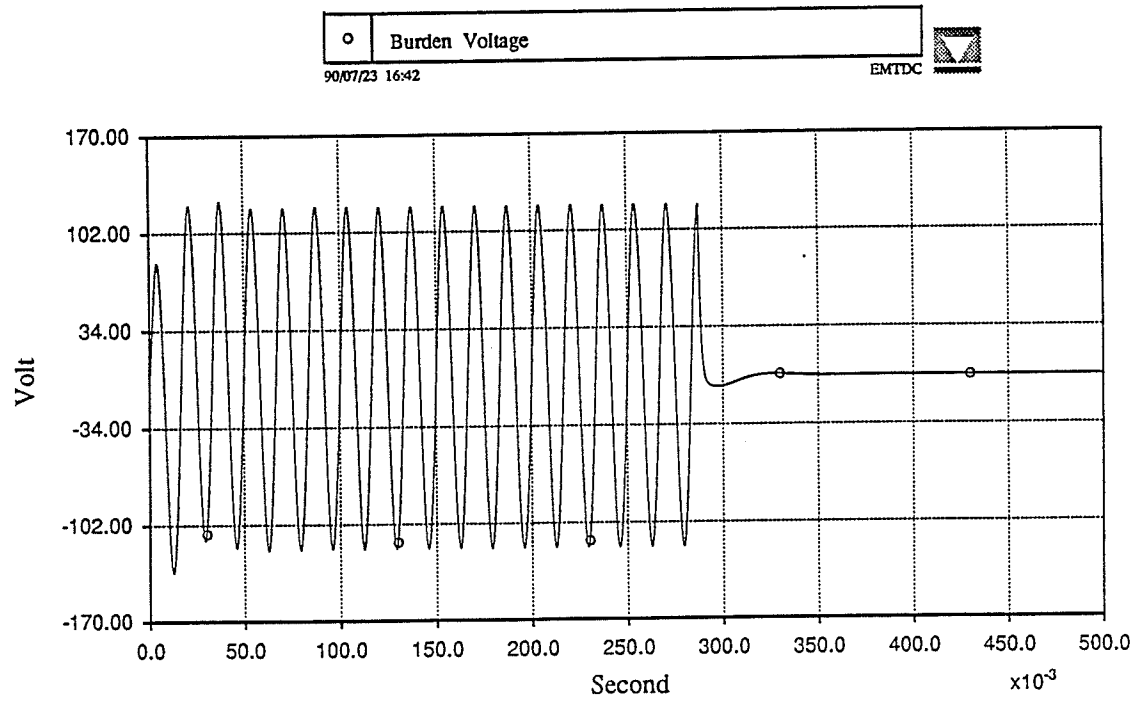
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 2a ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     217.5      / capacitive divider (s.u. = scaled up)
   2  3   0.    32.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
   7  0   36.    0.     0.        / load resistance
999                                / TERMINATES BRANCH DATA
   1 1.E-2 0. 0. 0. 0.             / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
  -120  120                        / PRINTPLOT LIMITS
  10                               / NUMBER OF OUTPUT CHANNELS
   1.    1.    .25    12.E4   .05    500.    10.    .00435
    0.08265   0.1   800.   8.    0.    -1.    .654  /
  VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
  VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
  VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
  VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
  VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
  VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 2a
Scaled Down Thevenin Voltage
90/07/23 16:27
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

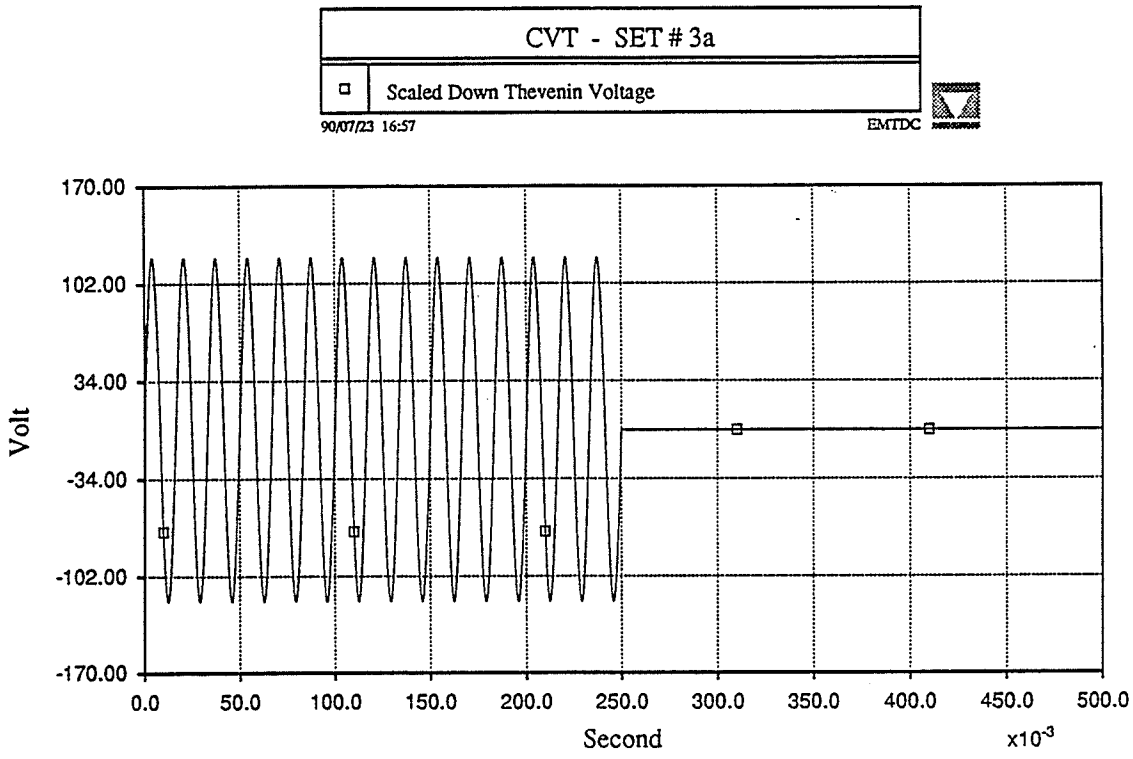

Burden Voltage
90/07/23 16:27
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

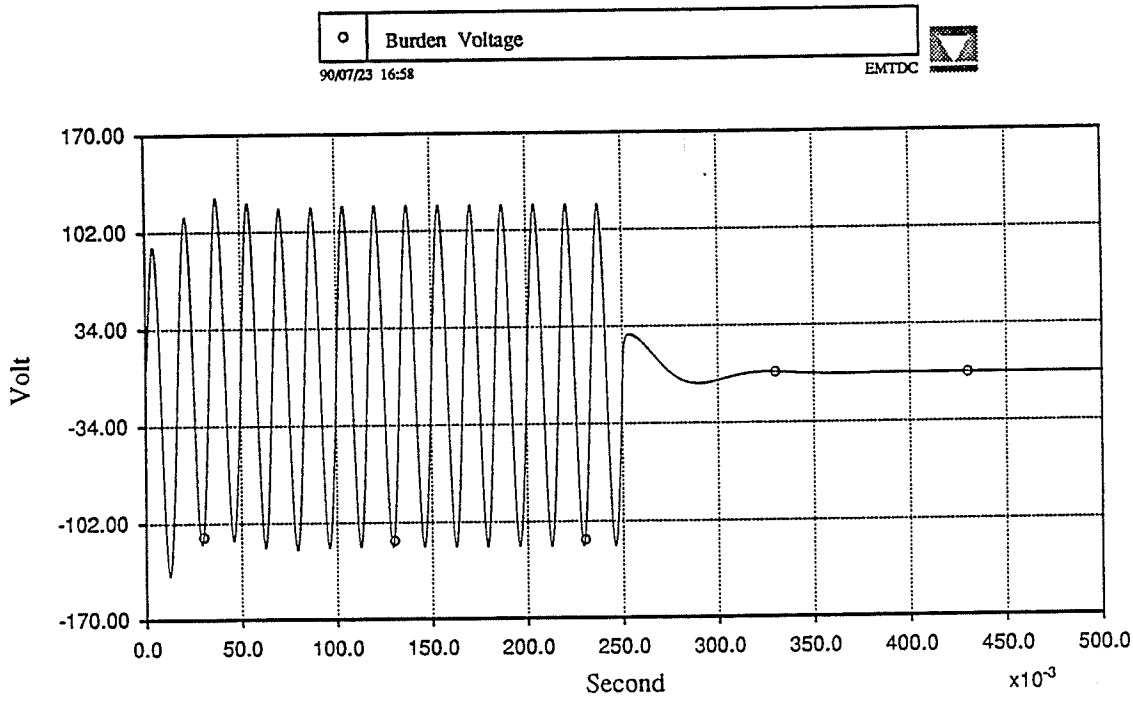
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 2b ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     217.5      / capacitive divider (s.u. = scaled up)
   2  3   0.    32.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
   7  0   36.    0.     0.        / load resistance
999                                / TERMINATES BRANCH DATA
   1 1.E-2 0. 0. 0. 0.             / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
  -120  120                        / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.    1.    0.2875    12.E4    .05    500.    10.    .00435
     0.08265    0.1    800.    8.    0.    -1.    .654  /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 2b
Scaled Down Thevenin Voltage
90/07/23 16:41
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

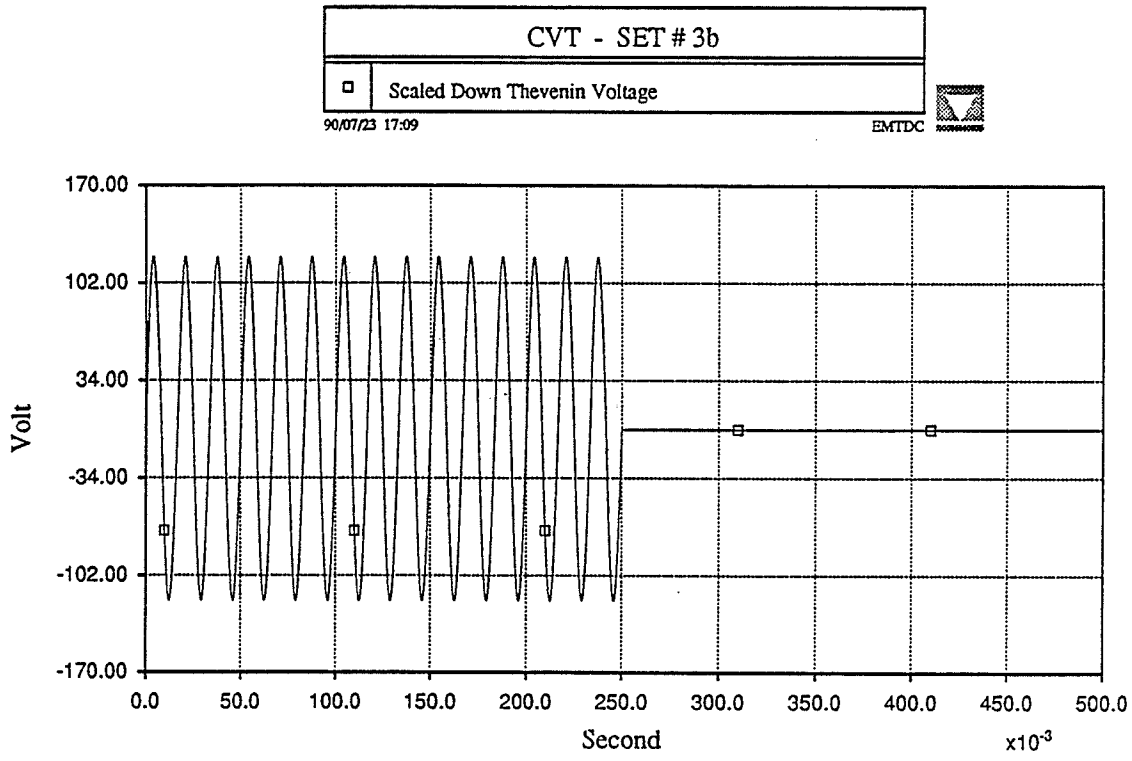

Burden Voltage
90/07/23 16:42
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

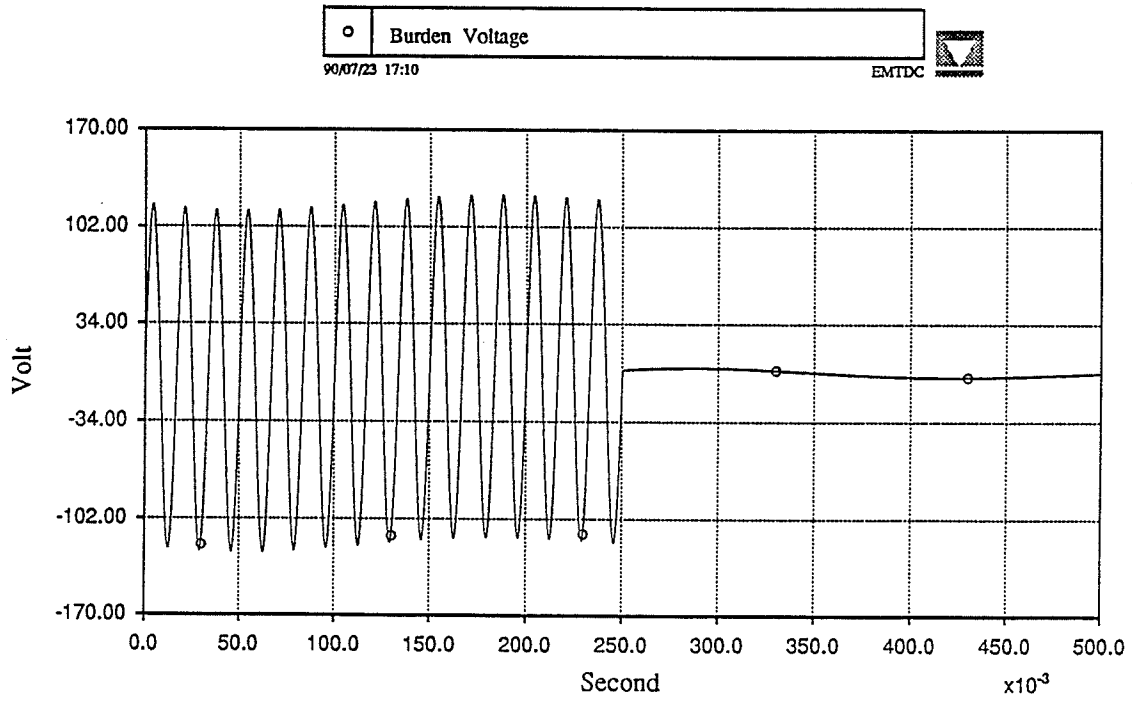
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 3a ) / TITLE
  5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
  1                               / ONE SUBSYSTEM
  8                               / NUMBER OF NODES
  0.                              / INITIAL NODE VOLTAGES
  1  2   0.    0.     342.5      / capacitive divider (s.u. = scaled up)
  2  3   0.    0.0205  0.        / correcting inductor (s.d. = scaled down)
  3  4   1.E-2  0.     0.        / core saturation switch
  4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
  5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
  4  0   0.     .32    0.        / core linear slope (s. d.)
  3  6   .1     0.     0.        / secondary resistance
  6  7   0.    1.E-3   0.        / secondary inductance
 -7  8   0.    500.    0.        / suppression inductor
 -7  8   0.     0.  .83494       / suppression capacitor
  8  0   1.     0.     0.        / suppression resistor
  7  0   36.    0.     0.        / load resistance
999                               / TERMINATES BRANCH DATA
  1 1.E-2  0.  0.  0.  0.         / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
  -120  120                       / PRINTPLOT LIMITS
  10                              / NUMBER OF OUTPUT CHANNELS
   1.    1.    .25    12.E4    .05    500.    10.    .00685
    0.13015   0.1    800.   8.    0.    -1.    .654  /
  VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
  VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
  VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
  VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
  VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
  VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 3a
Scaled Down Thevenin Voltage
90/07/23 16:57
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

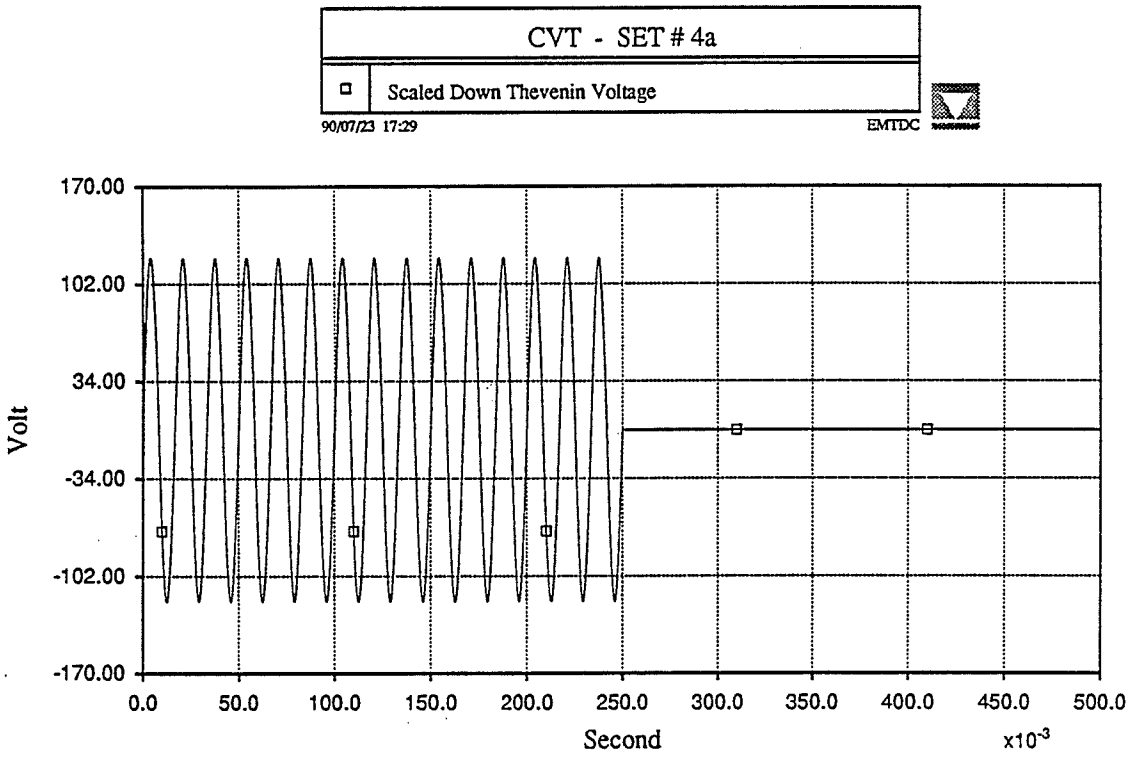

Burden Voltage
90/07/23 16:58
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

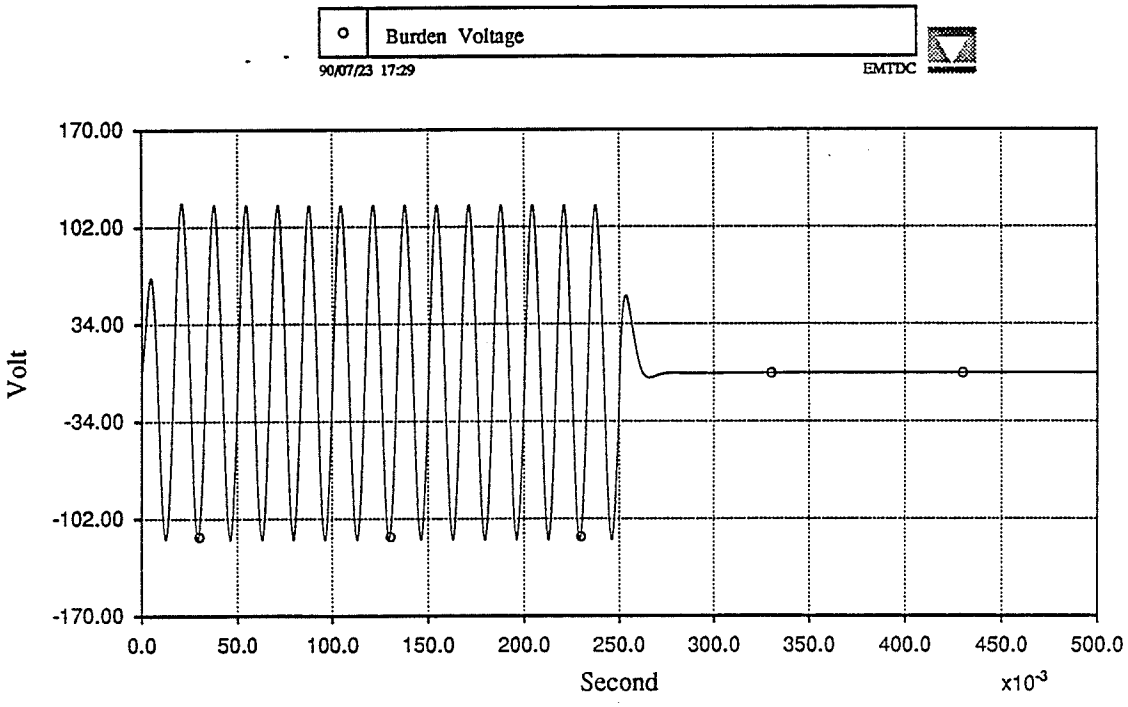
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 3b ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     5480.     / capacitive divider (s.u. = scaled up)
   2  3   0.    128.E-5  0.      / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.       / core saturation switch
   4  5   200.   0.     0.       / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.       / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.       / core linear slope (s. d.)
   3  6   .1     0.     0.       / secondary resistance
   6  7   0.    1.E-3   0.       / secondary inductance
  -7  8   0.    500.    0.       / suppression inductor
  -7  8   0.     0.  .83494      / suppression capacitor
   8  0   1.     0.     0.       / suppression resistor
   7  0   36.    0.     0.       / load resistance
999                               / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.       / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
   -120   120                     / PRINTPLOT LIMITS
   10                             / NUMBER OF OUTPUT CHANNELS
    1.    1.    .25    12.E4    .2    2000.    10.    .0274
     0.1096    0.1    800.    8.    0.    -1.    .654 /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 3b
Scaled Down Thevenin Voltage
90/07/23 17:09
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

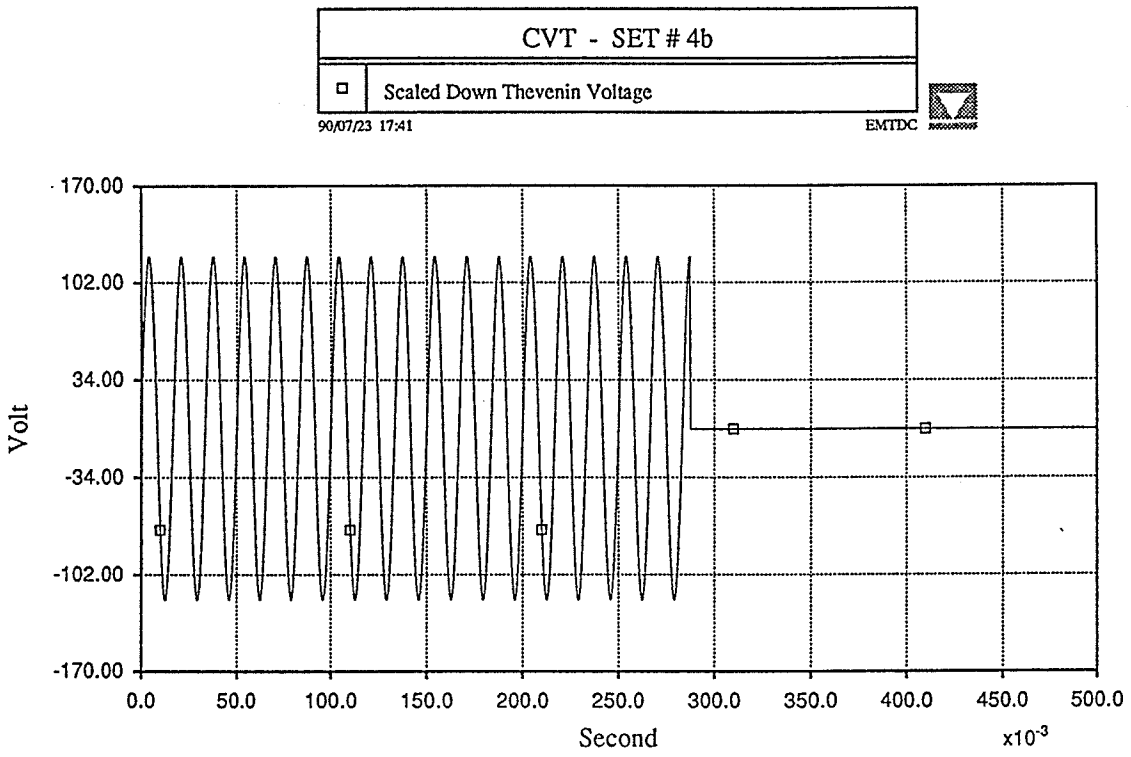

Burden Voltage
90/07/23 17:10
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

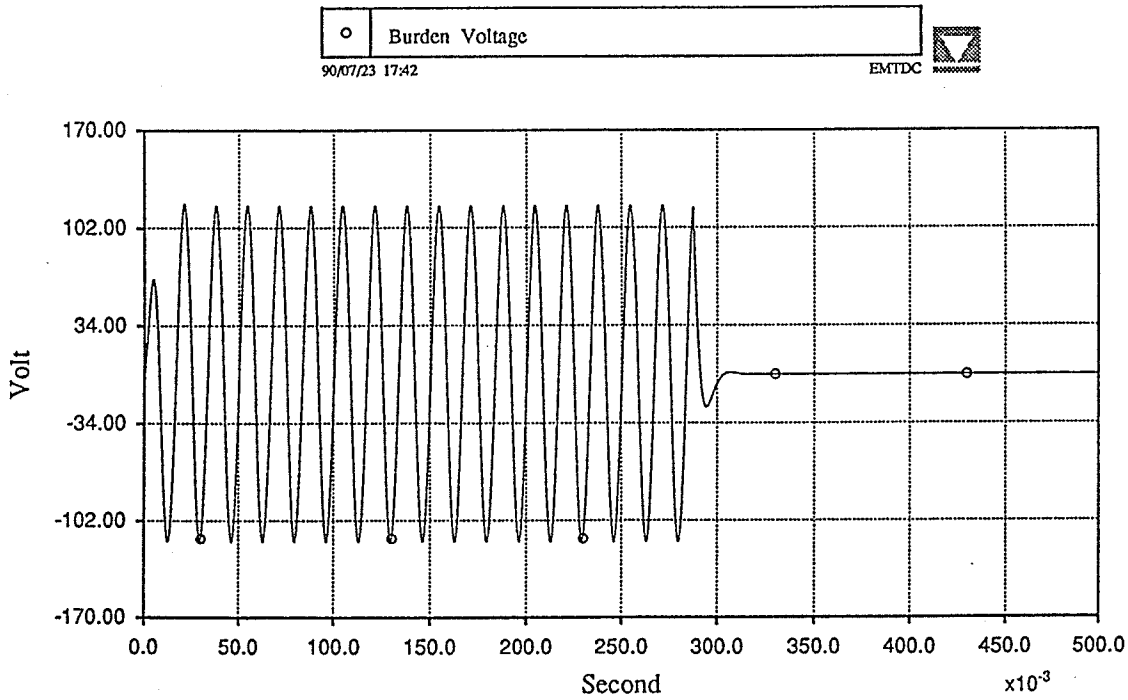
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 4a ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     610.       / capacitive divider (s.u. = scaled up)
   2  3   0.    12.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
   7  0   6.    0.      0.        / load resistance
999                                / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.        / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
  -120   120                       / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.    1.    .25    12.E4    .05    500.    10.    .0122
     0.2318    0.1    800.    8.    0.    -1.    .654 /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 4a
Scaled Down Thevenin Voltage
90/07/23 17:29
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

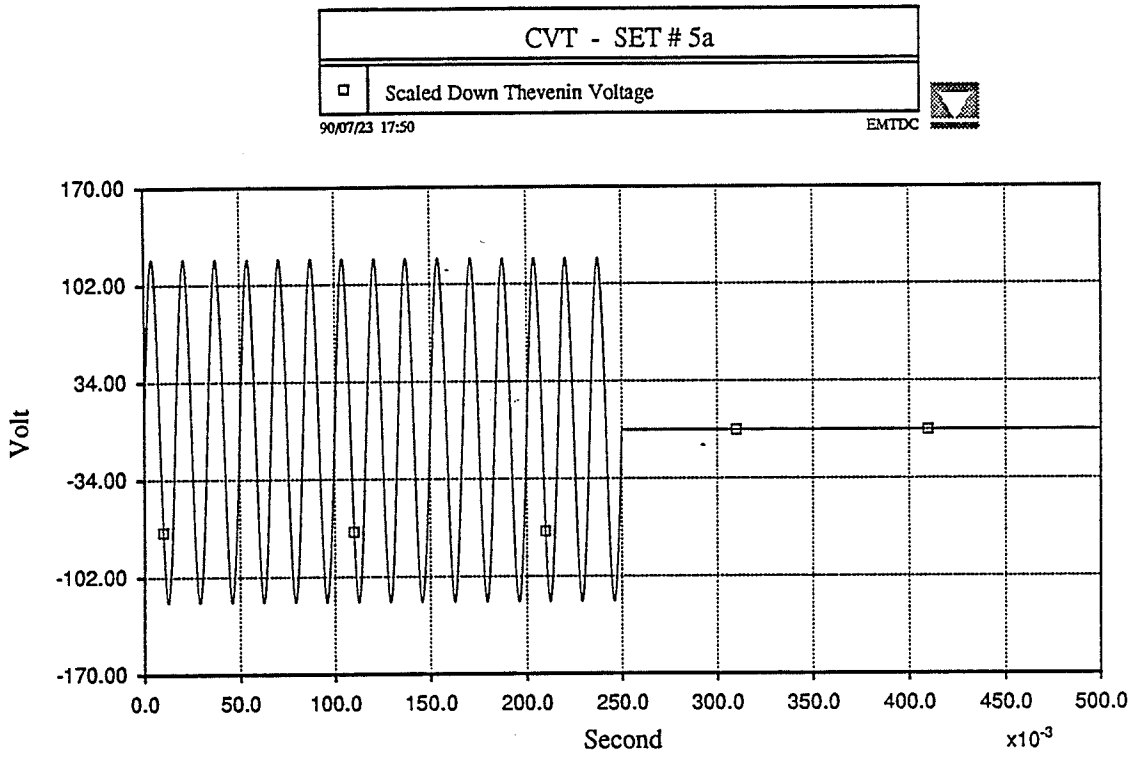

Burden Voltage
90/07/23 17:29
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

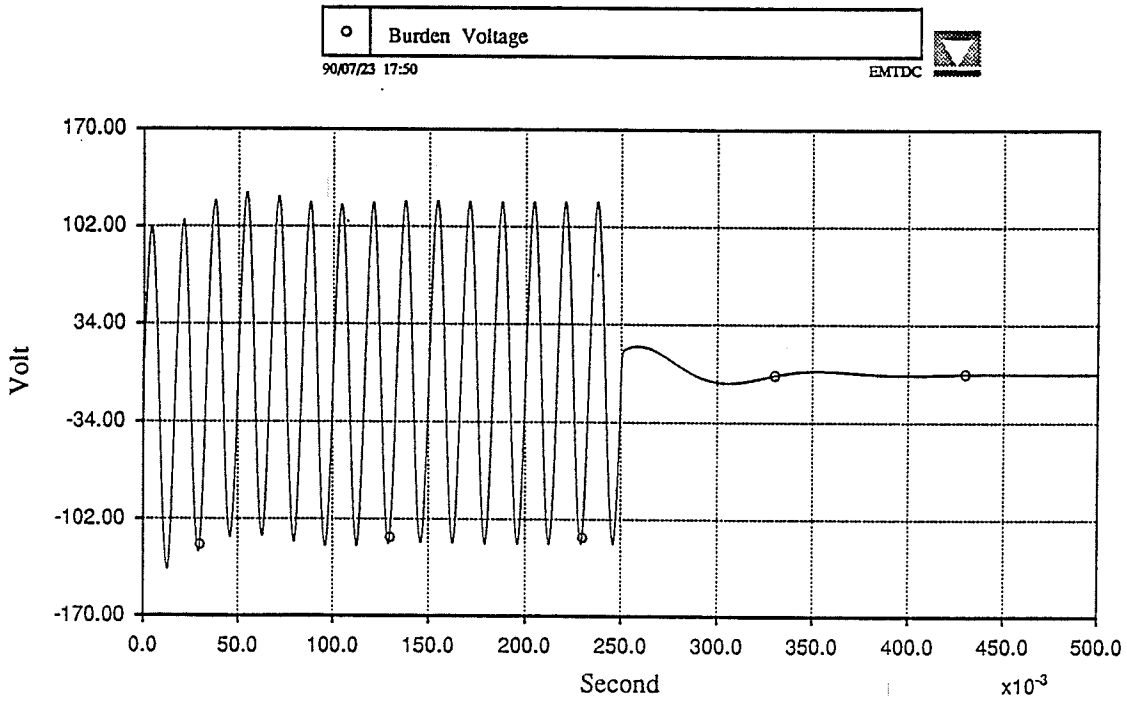
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 4b ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2    0.    0.     610.      / capacitive divider (s.u. = scaled up)
   2  3    0.    12.E-3  0.       / correcting inductor (s.d. = scaled down)
   3  4    1.E-2  0.     0.       / core saturation switch
   4  5    200.   0.     0.       / core resistive loss / 2 (s. d.)
   5  0    200.   0.     0.       / core resistive loss / 2 (s. d.)
   4  0    0.     .32    0.       / core linear slope (s. d.)
   3  6    .1     0.     0.       / secondary resistance
   6  7    0.    1.E-3   0.       / secondary inductance
  -7  8    0.    500.    0.       / suppression inductor
  -7  8    0.     0.  .83494      / suppression capacitor
   8  0    1.     0.     0.       / suppression resistor
   7  0    6.    0.      0.       / load resistance
999                                / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.        / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
   -120   120                      / PRINTPLOT LIMITS
   10                              / NUMBER OF OUTPUT CHANNELS
    1.     1.   2875.E-4    12.E4    .05    500.    10.    .0122
     0.2318    .1    800.    8.    0.    -1.    .654  /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 4b
Scaled Down Thevenin Voltage
90/07/23 17:41
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

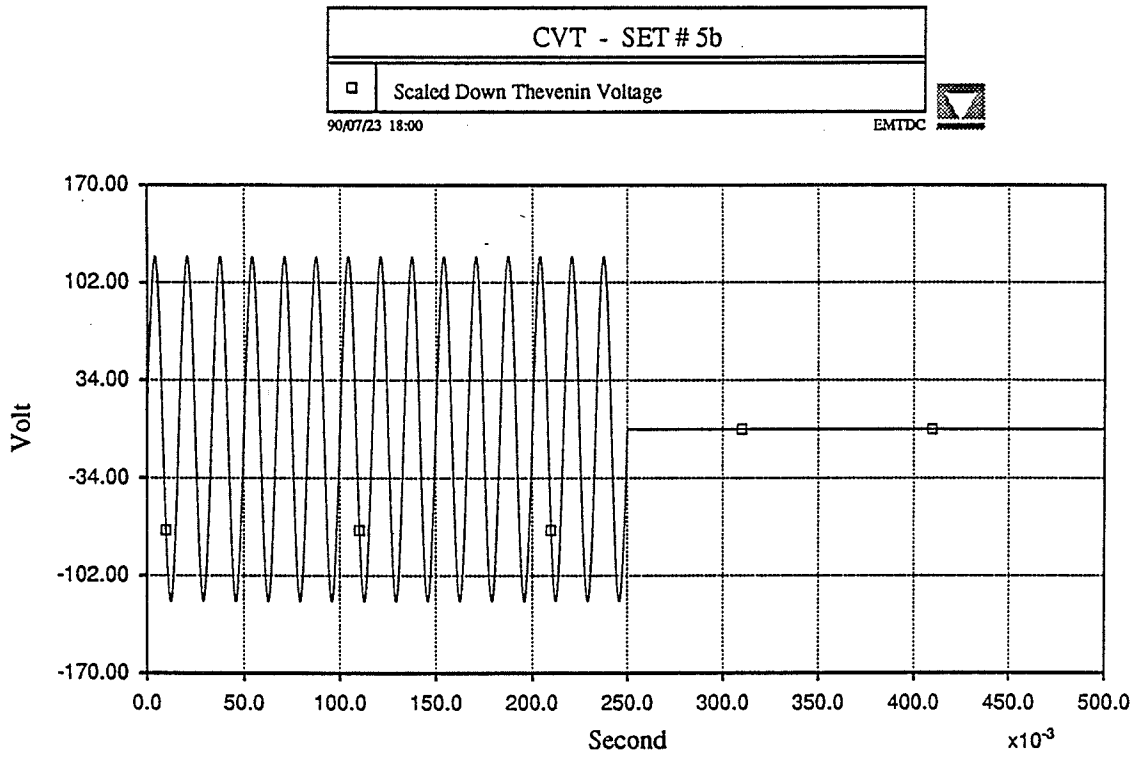

Burden Voltage
90/07/23 17:42
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

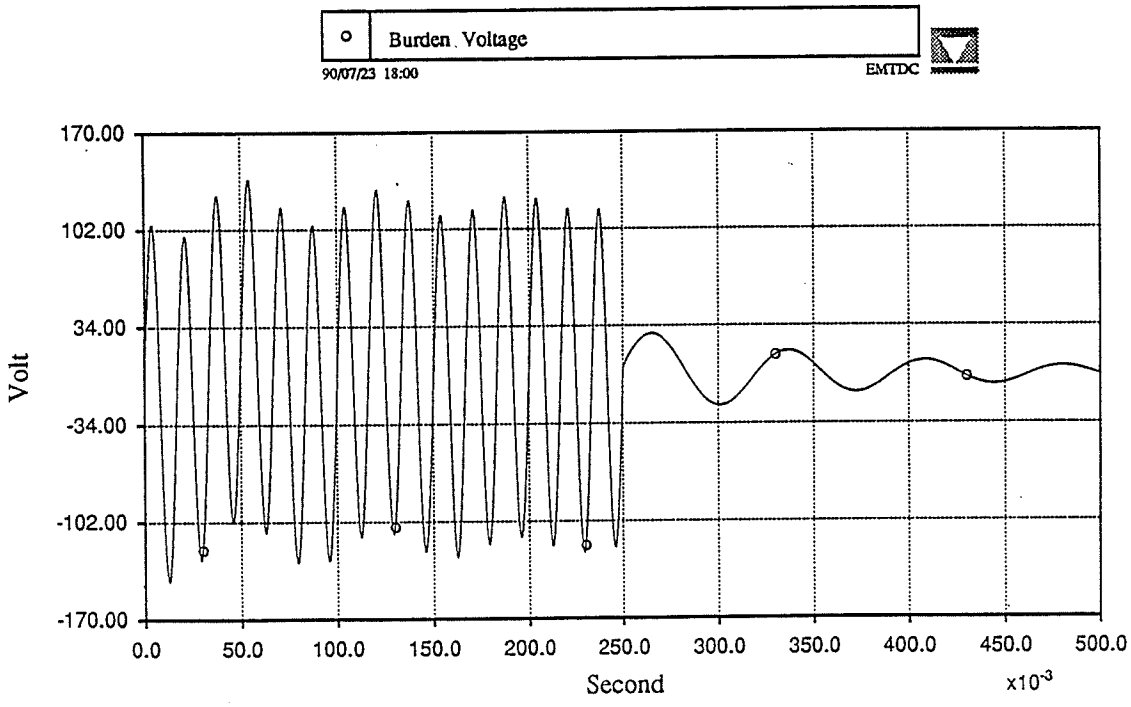
```
DATAFILE OF SUBROUTINE CVT2 ( SET # 5a ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     610.       / capacitive divider (s.u. = scaled up)
   2  3   0.    12.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
   7  0   36.    0.     0.        / load resistance
999                                / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.        / SOURCE DATA
999                                / TERMINATES SOURCE DATA
999                                / TERMINATES TRANSFORMER DATA
999                                / TERMINATES T-LINE DATA
  -120   120                       / PRINTPLOT LIMITS
  10                               / NUMBER OF OUTPUT CHANNELS
   1.    1.    .25    12.E4    .05    500.    10.    .0122
     0.2318    0.1    800.    8.    0.    -1.    .654  /
  VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
  VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
  VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
  VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
  VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
  VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 5a
Scaled Down Thevenin Voltage
90/07/23 17:50
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3


Burden Voltage
90/07/23 17:50
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

```
DATAFILE OF SUBROUTINE CVT2 ( SET # 5b ) / TITLE
   5.E-5   5.E-1   20.E-5          / DELT, FINTIM, PRTSTP
   1                               / ONE SUBSYSTEM
   8                               / NUMBER OF NODES
   0.                              / INITIAL NODE VOLTAGES
   1  2   0.    0.     610.       / capacitive divider (s.u. = scaled up)
   2  3   0.    12.E-3  0.        / correcting inductor (s.d. = scaled down)
   3  4   1.E-2  0.     0.        / core saturation switch
   4  5   200.   0.     0.        / core resistive loss / 2 (s. d.)
   5  0   200.   0.     0.        / core resistive loss / 2 (s. d.)
   4  0   0.     .32    0.        / core linear slope (s. d.)
   3  6   .1     0.     0.        / secondary resistance
   6  7   0.    1.E-3   0.        / secondary inductance
  -7  8   0.    500.    0.        / suppression inductor
  -7  8   0.     0.  .83494       / suppression capacitor
   8  0   1.     0.     0.        / suppression resistor
  -7  0   124.   0.     0.        / load resistance
  -7  0   0.0    .53    0.        / load inductance
999                               / TERMINATES BRANCH DATA
   1  1.E-2  0.  0.  0.  0.        / SOURCE DATA
999                               / TERMINATES SOURCE DATA
999                               / TERMINATES TRANSFORMER DATA
999                               / TERMINATES T-LINE DATA
   -120   120                     / PRINTPLOT LIMITS
   10                             / NUMBER OF OUTPUT CHANNELS
    1.    1.    .25    12.E4    .05    500.    10.    .0122
     0.2318    0.1    800.    8.    0.    -1.    .654  /
   VAR(1)=NODE, VAR(2)=NS, VAR(3)=SWITCHING TIME,
   VAR(4)=VMAX, VAR(5)=THEVENIN VOLTAGE RATIO (C1/Ce),
   VAR(6)=PT'S PRIMARY TURNS, VAR(7)=PT'S SECONDARY TURNS,
   VAR(8)=C1, VAR(9)=C2, VAR(10)=CURKNE, VAR(11)=SLIN,
   VAR(12)=SSAT, VAR(13)=FLUX0, VAR(14)=S,
   VAR(15)=FAULT CLEARING TIME
```


CVT - SET # 5b
Scaled Down Thevenin Voltage
90/07/23 18:00
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3


Burden Voltage
90/07/23 18:00
EMTDC
170.00
102.00
34.00
-34.00
-102.00
-170.00
Volt
0.0
50.0
100.0
150.0
200.0
250.0
300.0
350.0
400.0
450.0
500.0
Second
x10-3

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