A Circuit Model for Switching Loss Estimation in Voltage Source Converters

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Abstract

Insulated Gate Bipolar Transistor (IGBT) based voltage source converter (VSC) applications embedded in power systems are growing. Optimal design of thermal management systems for such converters requires estimation of IGBT losses under various operating conditions, both normal and abnormal. Therefore, development of tools for estimating IGBT losses in EMT simulators is important as converters embedded in large power systems are simulated in EMT simulators.

Two circuit models are developed to simulate turn-on and turn-off transients using a behavioral approach. These circuit models mimic the observed behavior in distinct phases of the turn-on and turn-off transients under the inductive load switching. In this model, the nonlinear nature of the circuit model of the IGBT is treated and converter specific influential parameters are taken in to account. An excellent correlation between the measured and simulated waveforms as well as measured and estimated switching losses is observed. Finally, an efficient method to incorporate switching loss calculation in an EMT program in the form of a lookup table created using the developed transient model is proposed.

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Dedication

To my teachers including parents

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List of Symbols

τ	Carrier life time of the freewheeling diode
τ_{Tail}	Time constant of the tail current
C_{ce}	Collector-to-emitter capacitance
C_{gc}	Gate-to-collector capacitance or Miller capacitance
C_{gc}\`	Fictitious Miller capacitance
C_{ge}	Gate-to-emitter capacitance
C_{ies}	Input capacitance of an IGBT at the short circuited output
C_j	Junction capacitance of the diode
C_{j0}	Zero voltage junction capacitance of the diode
$C_{reservoir}$	Capacitance of the reservoir capacitor
E_{I_Rise}	Energy loss during collector current rising phase
E_{V_Fall}	Energy loss during collector-to-emitter voltage falling phase
g_{fe}	Transconductance of an IGBT
I_c	Collector current
I_{Charge}	Charging current of the Miller capacitor
I_{cm}	Collector current measurement taken to estimate gain during Phase-2 and 3 of turn-on transient

I_D	Diode current
$I_{Discharge}$	Discharging current of the Miller capacitor
I_F	Forward current through the freewheeling diode
I_L	Load current
I_{RM}	Maximum reverse recovery current
K_{g_adjust}	Adjusting factor of the gain
K_i	Ratio between average collector current and load current during Phase-4 and 5 of the turn-on switching event
K_p	Transconductance of a MOSFET
K_V	Ratio between average collector-to-emitter voltage during Phase-2 and -3 of the turn-on transient and supply the voltage
L_s	Total path inductance of the collector current
m	Gradient factor
R_G	Gate resistance
S	Softness factor of the freewheeling diode
t_a	Initial reverse recovery period
t_b	Later reverse recovery period
t_d	Turn-on delay of an IGBT
t_f	Instant of taking 2nd gate-to-emitter voltage measurement in estimating C_{ge}
t_i	Instant of taking 1st gate-to-emitter voltage measurement in estimating C_{ge}
T_{I_Rise}	Duration of the Phase-2 and -3 of the turn-on transient
t_m	Instant of taking measurement in estimating L_s

t_{rr} Total reverse recovery time

T_{V_Fall} Duration of the Phase-4 and -5 of the turn-on transient

V_b Barrier voltage of the diode

V_{cc} Supply voltage to the unit cell

V_{ce} Collector-to-emitter voltage

V_{cem} Collector-to-emitter voltage measurement taken in estimating L_{s1}

V_D Diode voltage

V_{GDH} Voltage level of the turn-on gate drive signal

V_{GDL} Voltage level of the turn-off gate drive signal

V_{ge} Gate-to-emitter voltage

V_{ge_f} Second gate-to-emitter voltage measurement taken in estimating C_{ge}

V_{ge_i} First gate-to-emitter voltage measurement taken in estimating C_{ge}

V_{ge_m} Gate-to-emitter voltage measurement taken in estimating gain for Phase-2 and -3 of the turn-on transient

$V_{ge_plateau}$ Gate-to-emitter voltage plateau

V_j Junction voltage of the diode

V_{syn} Synthesised collector-to-emitter voltage by the controlled source

V_T Gate-to-emitter threshold voltage

β Current gain of the internal BJT

ΔT_s Simulation time step

List of Abbreviations

AC	Alternating Current
BJT	Bipolar Junction Transistor
CPU	Central Processing Unit
DC	Direct Current
EMT	Electro-Magnetic Transient
FACTS	Flexible Alternating Current Transmission Systems
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PCB	Printed Circuit Board
PSCAD	Power System Computer Aided Design
VSC	Voltage Source Converter

Chapter 1

Introduction

In this chapter, the background, motivation, objectives and the scope of the research reported in this thesis are described. A brief overview of the organization of the thesis is also provided for easy navigation.

1.1 Background

Application of voltage source converters (VSCs) in power systems is rapidly growing due to advantages such as absence of commutation failures, ability of independently controlling the active and reactive power, and fast dynamic response [1]. In applications ranging from a few kilowatts to hundreds of megawatts, Insulated Gate Bipolar Transistors (IGBTs) are used [2] as the power electronic switch. In the past, application of VSC technology was limited to low power levels due to lower voltage and current ratings of IGBTs when compared with the thyristor switches used in Line Commutated Converters (LCCs). However, the voltage and current ratings of IGBTs have been significantly improved during the recent past due to advancements in device manufacturing technology [3]. Moreo-

ver, the introduction of new device structures such as punch-through IGBTs, field-stop IGBTs [4], and improved fabrication technologies [5] enhanced the steady state and transient characteristics of modern IGBTs.

Unlike thyristors, which rely on zero crossing points of its current to turn-off, IGBTs are fully controlled switches; i.e. they can be turned on and off at any desired instant of time using the voltage applied to the gate. This enables VSC based inverters to craft sinusoidal signals with low distortion, if they are switched at a frequency much higher than the frequency of the sinusoid to be synthesized. Therefore, the switching frequency of the IGBTs in a VSC producing 50 Hz or 60 Hz waveform is typically in the range of several kilohertz. As a result, the switching loss, which is the product of energy loss per switching event and the number of switching events per second, constitute a significant portion of the power losses in a VSC. Therefore, having an accurate estimate of the switching loss component is important in designing the cooling systems for IGBTs in a VSC [6].

Power losses can occur in an IGBT switch during the conduction state, blocking state, and during switching transients. During the conduction period, although the current through the IGBT could be high, the voltage across the IGBT is small and equals its forward voltage drop. The conduction losses can be easily estimated if the collector current and the forward voltage drop are known. In the blocking state, voltage across the IGBT is high and the losses are due to small leakage currents, which are in the range of microamperes. In contrast, during the switching transients, both the voltage across the IGBT and the current through it undergo changes. There is a period in which a high voltage and a high current exist in the IGBT simultaneously. Thus, the instantaneous power dissipated during a switching transient could rise up to several megawatts in large capacity IGBTs

used in power system applications [7]. However, the switching energy loss per event is small because the duration of switching transient is typically within several hundred nanoseconds. Turn-on energy loss largely depends on the pre-switching voltage across the IGBT and the post-switching current. Similarly, turn-off energy loss largely depends on the pre-switching current through the IGBT and the post-switching voltage. The switching losses are also dependent on the power circuit stray inductances, IGBT internal capacitance values and its transfer characteristics, and characteristics of the gate drive.

It is obvious that the most important step in estimation of the switching losses is the calculation of the currents and voltages that the IGBT is subjected to during the operation of the VSC. These currents and voltages can be calculated through detailed circuit simulations. Power electronics converters embedded in power systems are usually simulated in electromagnetic transient (EMT) simulation programs. In these simulation programs, a power electronic switch is represented as a two-state resistor in series with a voltage source that represents the forward voltage drop [8]. Although this simple model allows accurate calculation of voltages and currents of an IGBT device in a VSC, it does not simulate the current and voltage variations during switching transients. Simulation time steps used in EMT simulations are generally dictated by the dynamics of the power system components such as transmission lines, and simulation time steps in the range of 5-50 μs are typical [9].Thus switching events that occur in a few hundreds of nanoseconds are considered as instantaneous. Fast switching transient are not transferred to the rest of the system via elements having large time constants [10]. Therefore, this characterization does not affect the accuracy of the estimated transient behavior of the rest of the system. Consequently, the real behavior of IGBT switches during the switching transient is ig-

nored in the typical EMT type simulations. This enables simulation of large power systems having embedded power electronic modules within a feasible simulation period. However, the impact of the energy dissipated in an IGBT due to switching cannot be ignored, as these losses significantly contribute to device heating. Thus the results of a typical simulation do not accurately represent the thermal stress on the IGBT switches because the switching losses are ignored or inaccurately estimated. Although the impact of switching losses may not be very significant in the overall scheme for most cases, the simulation approaches that ignore the switching losses do not accurately represent the actual available energy and the energy distribution in a power system at a given time instant. Therefore, it is beneficial to develop an accurate switching loss model to estimate power loss through IGBT switches. Such a power loss estimation model is useful if it can be implemented in an EMT simulation environment without excessively degrading the speed when simulating large power systems with embedded power electronics. That is the models should be capable of estimating the power losses that occur within few hundred nano-seconds (100 ns -300ns) long IGBT switching transients in a simulation environment that typically uses time steps of 5μs -50μs.

1.2 Motivation

There are two main factors that motivated this research: (i) need for an appropriate model for estimation of switching losses of an IGBT, using EMT simulations, which is evident from the lack of switching loss models incorporated in the industry standard EMT simulation software programs, and (ii) impacts of the inaccurate estimation of switching losses on the design of converter thermal management systems.

EMT simulation programs are used to design and analyze the behavior of power systems with embedded power electronic converters as well as low power converter applications. In the context of power systems, a high-power embedded power converter refers to VSC based high voltage direct current (HVDC) transmission systems and flexible AC transmission systems (FACTS) devices. Low-power converter applications include power electronics systems such as motor drives. According to [7], in a 350MW VSC HVDC transmission system, 70% of the power losses occur in the converters. A significant part of the converter loss is due to the switching power losses, which increase with the switching frequency. Hence, accurate estimation of switching losses in VSCs is important. Another aspect is the importance of simulating the converter with the surrounding power system. Use of EMT programs to simulate the power electronic converter together with the power system allows analysis of normal as well as abnormal operating conditions that the converter may be subjected to during its service. Isolated simulation of a converter would not allow realistic analysis of such abnormal operating conditions, during which the IGBTs may be subjected to higher thermal stress.

Energy dissipated in an IGBT device is converted into thermal energy and raises its junction temperature. The thermal management system of a converter, which comprises of heat sinks, cooling fans, or liquid cooling systems, is designed to remove this thermal energy. The thermal management system consumes a significant portion of the total cost of a converter, and the space taken by the module. Therefore, due to economic reasons, the thermal management systems of the converters are designed and manufactured with relatively low safety margins [6]. Increase of IGBT losses beyond the maximum safety limit significantly raises the risk of failure. The ability to accurately simulate the losses and

corresponding thermal stress on IGBT devices in a converter can help identification of the risks of failure during the design stage. This kind of prediction is especially helpful for the designers of power electronic systems to optimize the thermal management systems [11]. With the growing number of applications of VSCs in power systems, the need for an accurate switching losses estimation facility in EMT programs as a design tool is well justified.

There are a number of published research papers that describe different attempts to develop IGBT switching loss models [6], [12]-[16]. However, these previous models fail to meet three key requirements which are vital for successful implementation in an EMT program. These requirements are (i) accuracy of estimation of switching loss, (ii) manageable level of model complexity, and (iii) accessibility to parameters of the model. The gap identified between the requirements and the available models can be examined by dividing the various previously proposed models into three broad categories as (i) empirical models, (ii) circuit models, and (iii) physics based models.

The model complexity of the empirical fittings and circuit models is less when compared to the complexity of physics based model. In empirical modeling, total device power loss or switching energy loss is fitted as a function of the load current because supply voltage is fixed for a two level converter. These models facilitate the estimation of losses at different load currents, once the parameters of the function are estimated from experimental measurements made under certain test conditions [13], [15]. However, switching loss is not merely determined by the characteristics of the IGBT. The switching losses are highly influenced by the gate drive and stray inductance of the converter power circuit. Use of switching loss variations with load currents as specified in the data sheets to find the loss

functions ignores the impact of gate drive and stray inductance. This contributes to significant loss of accuracy. On the other hand, conducting of loss measurements on high power IGBT devices demand facilities that are beyond the approach of most users. The accuracy of estimation could be dubious when the operating voltages and currents are allowed to vary beyond the range of data used for developing the model.

Use of circuit models is another potential approach due to its lower complexity. Circuit models use basic circuit elements to mimic the nonlinear transient behavior. Therefore, it is possible to estimate the transient trajectories of the currents and voltages using these models and use them to estimate the energy loss. Because factors such as stray inductances and gate drive characteristics can be incorporated to the model, switching loss can be estimated more accurately than empirical models. However, since the circuit model attempts to capture the current and voltage variations during the switching transient, the model needs to be solved in very small times steps in the range of several nanoseconds. Therefore, it is not feasible to run such circuit models at each switching event happening in a long EMT simulation due to drastic increase in the computational burden and the simulation time. Consequently, the direct adoption of circuit models into EMT simulation programs is not feasible.

The boundary between circuit and physics model is becoming more and more blurred due to the use of complex physics based mathematical formulations in some circuit models such as [17]. In physics based modeling, switching behavior of an IGBT is modeled by applying physical laws that governs the dynamics of the semiconductor. Physics based models are capable of predicting the switching behavior more accurately than the empirical or circuit models. The physics based models, which are based on partial differential

equations of time and space also need to be simulated at very small time steps, and are more complex than the circuit models. However, the most significant issue of the physics based models is the need for large number of unfamiliar and inaccessible parameters.

1.3 Objectives of the Thesis

The main goal of the research is to develop a switching loss model of an IGBT used for switching an inductive load. Several primitive objectives are to be achieved to fulfill the goal of this research. They are listed in the approximate order to be accomplished.

- Identification of the factors influencing the transient variations of the current and voltage of an IGBT during the switching transients through survey of literature and experimental measurements.
- Development of suitable circuit models that can be used to mimic different phases in IGBT turn-on transient.
- Development of suitable circuit models that can be used to mimic different phases in IGBT turn-off transient.
- Development of procedures for extraction of various parameters in the switching transient models.
- Incorporation of switching loss calculation into an electro-magnetic transient (EMT) simulation program through a suitable procedure to approximate the switching loss based on the switched current and voltage.

1.4 Organization of the Thesis

After this introduction, a comprehensive literature review is presented in Chapter 2. It introduces a test circuit, referred to as the unit switching cell, for measuring IGBT switching waveforms, and describes details of the possible methods of evaluating switching losses in a switching cell. In addition, a brief description of previous approaches used for modeling IGBTs and diodes are presented, and the expected requirements of the models are identified,

Chapter 3 describes the approach used to model the turn-on switching transient. First, the turn-on behavior of an IGBT in a unit switching cell is explained. Then, a set of circuit models that mimic the behavior of each distinct phase is explained. Thereafter, a procedure for extracting parameters of the turn-on transient model is described. Chapter 4 details the turn-off transient model, and the organization of this chapter is similar to Chapter 3. In addition, extracted parameters from the turn-on and turn-off transient measurements are compared.

Chapter 5 presents the validation of the proposed switching transient models. Measured and estimated trajectories are compared at different operating conditions and for different IGBT devices. Performance of both turn-on and turn-off models are evaluated against load current, supply voltage, and gate resistance changes. Chapter 6 evaluates the switching loss estimation performances of the two models and demonstrates the predicted switching loss characteristics. Conclusions and future work are listed in Chapter 7.

Chapter 2

Literature Review

In this chapter, the independent unit required to model a switching transient of an IGBT in a VSC is shown. Currently utilized approaches and potential approaches for estimating switching losses in the basic building block of a VSC are described and compared. The construction and the typical behavior of an IGBT and a power diode are explained. Physics based and circuit modeling approaches for simulating IGBT behavior are detailed. An approach for switching loss estimation in EMT type simulations is explained.

2.1 Voltage Source Converters (VSC)

Voltage source converters are utilized to transform AC electrical power to DC and vice versa. Two converters are used in HVDC systems and typical motor drives. One converter is used to rectify the AC and the other converter to synthesize AC electrical power from DC. However, functionality of a converter is independent of the arrangement of the switches. The same converter can be operated either as a rectifier or as an inverter by

properly selecting the operating sequence of the switches. This feature enables power transfer in both directions with the help of two converters connected through a DC link.

A voltage source inverter utilizes six electronic switches to craft a sinusoidal waveform from a direct current source. Figure 2-1depicts the circuit diagram of a three-phase VSC. An anti-parallel diode is necessary to be connected across each IGBT switch to ensure proper operation under inductive loads. An IGBT is a controlled switch that can be turned-on or turned-off via its gate input. However, a diode cannot be turned off or on via an external input and conducts whenever the voltage of the anode terminal is higher than cathode voltage. Therefore, diodes are classified as uncontrolled switches.

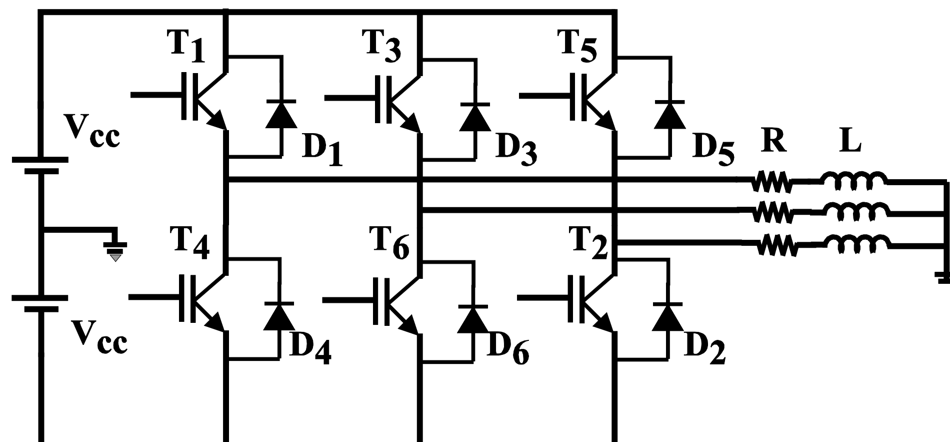


Figure 2-1 Three-phase voltage source converter topology

According to Figure 2-1, each phase of the load can be connected to the DC source via an IGBT. Three upper IGBTs enable current flow in the direction from source to ground and lower IGBTs facilitate current in opposite direction. Anti-parallel diodes facilitate current flow in the opposite direction to the IGBT in the same arm. This circuit arrangement makes it possible to craft a bidirectional or alternating current waveform through each phase of the load using set of unidirectional switches.

Controllability of the conduction through IGBTs via its gate drive enables crafting a sinusoidal waveform across the load. Anti-parallel diodes avoid discontinuity of the current when IGBT switches are open and this conduction phase is referred to as freewheeling. Switches connected to each phase operate independently as no interactions take place among them under normal operation. Therefore, it is possible to treat switches connected to each phase separately. Similarly, it is possible to generate a DC voltage across the DC bus with the help of an appropriate switching sequence when a three phase supply is available at the terminals connected to the load.

2.1.1 Independent Unit-Switching Cell

The switching circuit connected to each separate phase is called a half bridge. Figure 2-2 shows the circuit diagram of a half bridge switch. Two switches in a half bridge operate in a complementary manner. Simultaneous conduction of both upper and lower switches would short circuit the DC bus resulting in disastrous consequences. Thus at the instant of turning-on the IGBT in the upper arm, the IGBT in the lower arm is always in the off state, and vice-versa. Suppose the upper IGBT is conducting and the lower IGBT is in the off state. When the conducting upper IGBT is turned-off, the current through the inductive load, which cannot change instantaneously, is transferred to the anti-parallel diode in the lower arm. The reversal of the voltage induced across the inductive load due to decreasing current provides the forward bias condition required for the diode to conduct. If the upper IGBT is turned on again, the load current is transferred from the anti-parallel diode in the lower arm to the IGBT. Thus, during the turn-on switching transient, the load current in the anti-parallel diode in the opposite arm is transferred to the IGBT, while the

load current in the IGBT is transferred to the freewheeling diode in the opposite arm during the turn-off transient. Therefore, for the purpose of modeling the switching transient of an IGBT, it is adequate to represent only one arm of the half bridge, together with the anti-parallel diode in the opposite arm connected across the load as depicted in Figure 2-2. Fast current transients that take place during a switching event induce significant voltages across the stray inductances along the current path. Figure 2-3 illustrates typical components of the path inductance involved in a half bridge switch. Path inductances between reservoir capacitor $C_{reservoir}$ and switch are represented by $L_{p_C\text{-}SW}$ and $L_{n_C\text{-}SW}$.

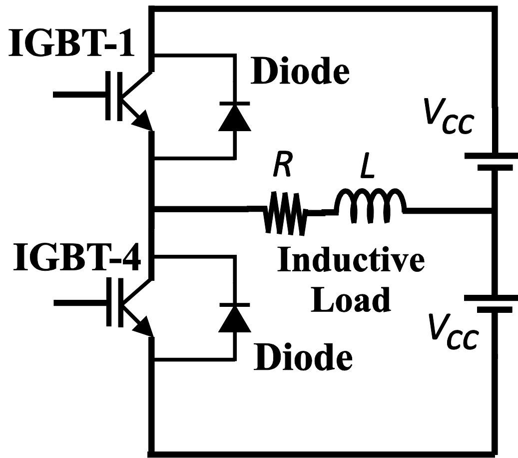


Figure 2-2-Half bridge switch

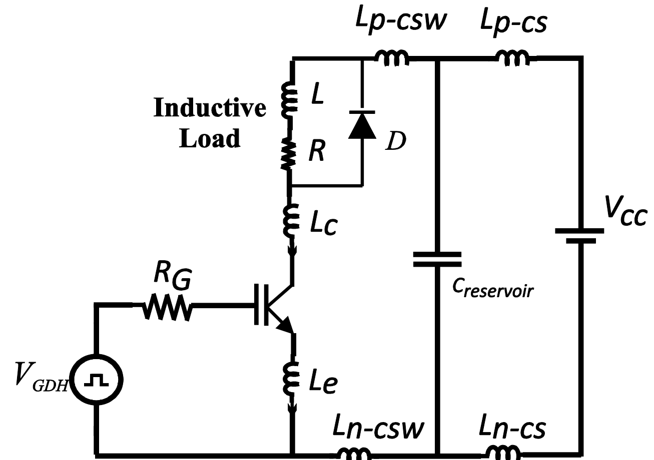


Figure 2-3-Transient model of half bridge

The inductances $L_{p\text{-}CS}$ and $L_{n\text{-}CS}$ are the path inductance between the DC source and the reservoir capacitor. L_e and L_c are total stray inductance between the collector and emitter. These stray inductances can be added and represented as a single equivalent inductance when the same transient current flows through all inductances. Importance of including the stray inductance of the path in transient analysis is emphasized in the literature [18]. Occasionally, path inductance of the gate drive circuit is also included in this model [19], [20]. Often, the sum of all stray inductance components on the output side is represented as a single lumped inductance in the unit switching cell circuit [19], [20] as shown in

Figure 2-4 in switching transient analysis. The simplified unit switching cell circuit shown in Figure 2-4 imposes the conditions that the IGBT is subjected to, if it was used in a three-phase VSC circuit, therefore it is considered as suitable for analysis of the IGBT switching transients.

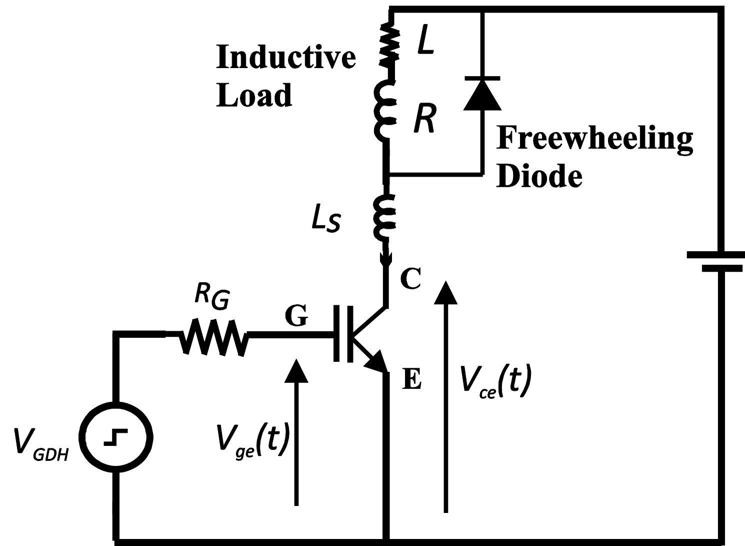


Figure 2-4-Simplified unit cell model

Consequently, this circuit model of the unit switching cell is used for analysis and experimental measurements in this thesis. The unit switching cell circuit is characterized by the layout parameter L_S. The stray inductance L_S is approximately equal to the total series stray inductances up-to the reservoir capacitor because in typical designs, the reservoir capacitance provides the transient currents. The gate drive is characterized by the gate resistance R_G and a step source V_{GDH} having a finite ramp up/down time. Thevenin resistance of the power supply is ignored as the voltage drop across it is much smaller than the voltage drop across the path inductance during transients. The role of the reservoir capacitor shown in Figure 2-3 is to maintain a constant supply voltage during transients. This facilitates use of an ideal source in the model. The load is assumed highly inductive so that the load current remains continuous and almost constant during the switching

transient. This assumption is valid because the time constants of practical loads are in the order of milliseconds or higher while the switching transients last only a few hundreds of nanoseconds.

A switching event in a VSC always involves a pair of switches connected to the load at the time of switching. Most of the time, the IGBTs in a VSC are turned-on when a diode is carrying the load current, and if not the case, the situation can be considered as a zero load current. Variation of the load current during the conduction of the switches can be calculated through EMT simulations. Furthermore, it is assumed that the collector-to-emitter voltage remains at the supply voltage V_{cc} before a turn-on transient and the voltage across the IGBT is raised to V_{cc} after a turn-off transient. Transient behavior of the unit switching cell is explained in the next section.

2.1.2 Switching Behavior of Unit Cell

Switching loss is exclusively determined by the shape of the trajectories of the collector-to-emitter voltage and the collector current during the switching transient. Typical variations of the switching trajectories are shown in Figure 2-5. When the IGBT is in the off state, the total supply voltage can be assumed to appear across it because the forward voltage drop of the freewheeling diode is insignificantly small when compared with the supply voltage.

During the IGBT turn-on process, the freewheeling diodes does not turn-off until the total load current is transferred to the IGBT. Therefore, the current through the IGBT increases rapidly during first stage of the turn-on process as depicted in Figure 2-5. During this current rising period, the voltage across the IGBT drops due to induced emf on the stray in-

ductance L_S. Once the total load current is transferred to the IGBT, the turn-off process of the freewheeling diode begins.

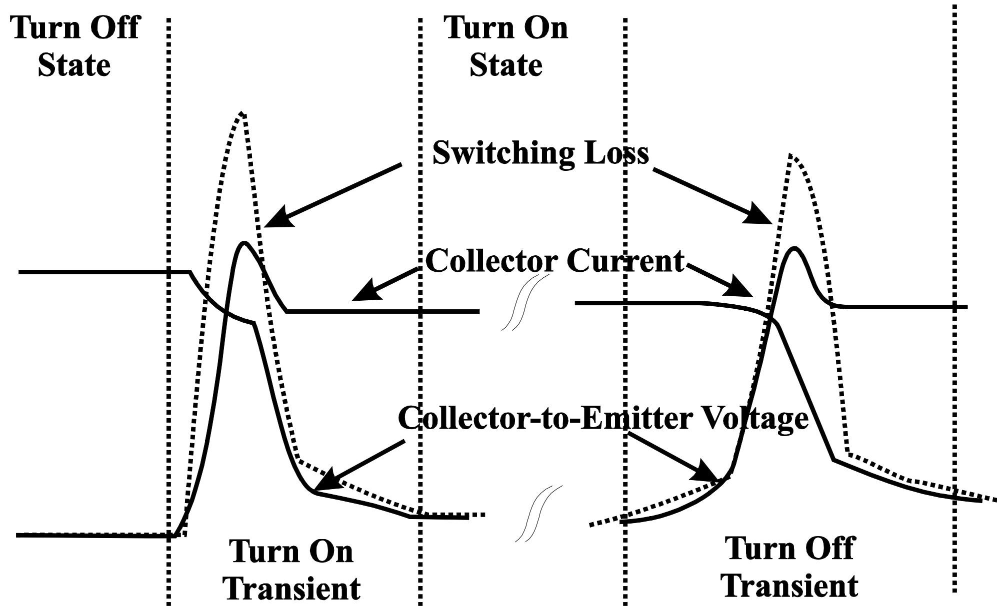


Figure 2-5-Switching transients

A negative current is visible through the terminals of the diode during turn-off due to release of stored charges in the diode. This current is called the diode reverse recovery current, and it causes IGBT current to overshoot beyond the constant load current as depicted in the Figure 2-5. Following the peak of the IGBT current, the voltage across the IGBT starts to falls as the diode starts to gain reverse voltage, and the collector current drops to the load current as the reverse recovery current starts to decay. Existence of a period where there is a high current through the switch simultaneously with a high voltage across it results in a significant power loss during the turn-on process. In addition to the IGBT, a switching power loss occurs in the diode during its turn-off process.

In the IGBT turn-off process, the load current is transferred back to the freewheeling diode. The diode does not start to conduct until the voltage across the diode is forward biased. Therefore, at first, the voltage across the IGBT increases and the diode becomes

forward biased when this voltage rises close to the source voltage. When the diode starts conducting, the current through the IGBT decreases gradually as depicted in the turn-off transient in Figure 2-5. The induced voltage across the stray inductance due to rapidly falling IGBT current appears as an overshoot of the collector-to-emitter voltage. Power dissipation in the diode is comparatively small during its turn-on process and can be ignored.

The focus of this research is to develop a circuit model that mimics switching behavior in terms of the variations of the collector-emitter voltage and the collector current. These variations are adequate to obtain a good estimate of the power losses during the switching transients, and therefore, this thesis does not aim to deal with the physics of the IGBT device in detail. However, the circuit model should capture the individual device dynamics and interactions during the switching processes. The nonlinear nature of the diode and IGBT characteristics during the switching transients make the modeling process a challenging task.

2.2 Approaches for Estimating Switching Losses

The techniques proposed in literature for estimation of switching losses [6], [12]- [16] can be broadly classified as (i) empirical models obtained by fitting appropriate curves to actual loss measurements [12], [13], [16]. (ii) approaches that directly simulate the switching transient using circuit or physics-based dynamic models [19], [20], and (iii) models that use loss equations derived from switching transient models [6], [14]. Brief descriptions of these different approaches are given in the next three sections.

2.2.1 Empirical Switching Loss Models

Empirical models utilize equations fitted to experimental data, or lookup tables for estimating the switching losses of an IGBT at different operating currents and voltages. The main advantage of empirical models is the simplicity. Empirical models require only a few model parameters and a little computational effort. In the lookup table approach, a set of measured switching losses at some intervals of operating conditions are stored in a table. This table is prepared during development of the model. Five to ten entries per each variable is generally sufficient for applications like loss estimation. During the simulation, the loss for a particular switching event is approximately estimated through interpolation, based on the device current, voltage, temperature or combination of these factors. The lookup table approach helps to strike a balance between simulation speed, accuracy, and memory requirements in simulating complex power electronics circuits. The application of a lookup table approach for loss estimation through unit cell is described in [13]. In this study, IGBT and diode losses are estimated at different load currents, voltages, and junction temperatures from the measurements and stored in tables. According to the authors of [13], simulation speeds can be increased by a factor of 10 to 20 times, if the detailed switch models that simulate the switching transients in SABER or PSPICE programs are replaced by the ideal switch models and utilize lookup tables for switching loss estimation. Use of polynomials to fit switching loss characteristics can be found in [15], [16], and [23]. In [23], a polynomial in the form given in Equation 2-1 is suggested to estimate the switching losses.

$$E_{SW} = A_{ON} i^{B_{ON}} + A_{OFF} i^{B_{OFF}} \quad \text{2-1}$$

where E_{sw} is the total switching loss, and i is the current being switched. The constants A_{ON}, A_{OFF}, and B_{OFF} are found by fitting Equation 2-1 to measured data. The fitted constants are dependent on the employed IGBT. A single quadratic polynomial of load current is used for total switching loss estimation in [24]. Reference [25] shows that the total switching loss of an IGBT used in a voltage source converter is directly proportional to the product of the switched current and voltage. Nonlinear equations with three terms featuring products of the different powers of the switched voltage and current have been used to accurately fit the total switching loss in zero current and zero voltage switching converters [15]. Use of a set of polynomials fitted to different loss components (turn-on, turn-off, and diode loss components) is proposed in [26].

Another approach, which is distinct from the above but can be categorized as empirical, is explained in [12]. In this approach, collector-to-emitter voltage, collector current, and diode currents during switching transients are synthesized with the help of measured waveforms. Three measurements are used to synthesize collector current and voltage during the switching transients. However, the voltage transient is assumed to be independent of load current and represented by a single measurement. One of the switching waveforms measured at load currents of 40A, 100A, or 170A has been used to synthesize the waveforms for a given load current (in the range of 0-200 A) by scaling the amplitude. The circuit representation of the model is shown in Figure 2-6. The voltage source V_{ce} and I_c synthesis waveform in transient simulation and voltage source V_{sat1} mimic saturation behavior during steady conduction. Similarly, the voltage source $V_{Forward}$ and current sources I_D mimic the transient behavior of the freewheeling diode. Estimated switching loss is claimed to have an accuracy level above 90%. However, this approach still needs

simulation to run at a time step small enough to capture the variation of transient waveforms and therefore, it is computationally inefficient. Although empirical models are simple and efficient, there are a number of limitations. First, application of the empirical models is valid only for the converters, which are identical to the converter on which the measurements are taken.

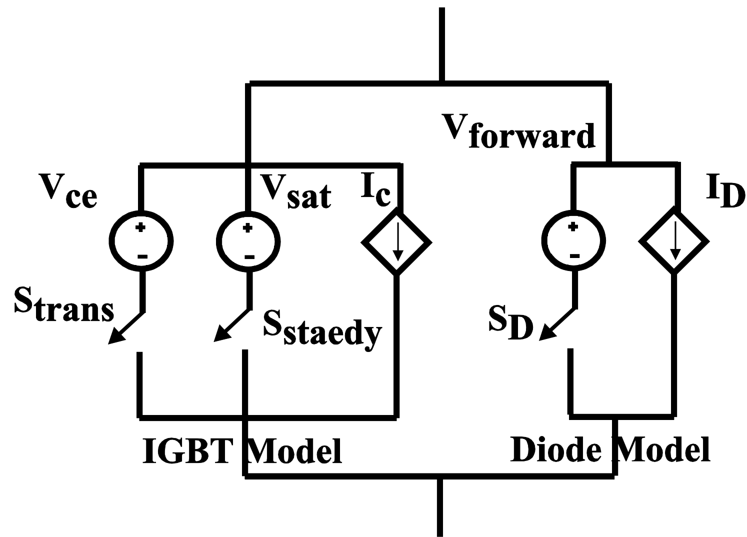


Figure 2-6-Circuit used to inject measured current and synthesis measured voltage in the circuit [12]

This is because factors such as stray inductances and gate drive characteristics, which highly affect the transient behavior and losses during the switching, are not explicitly represented in the empirical models. Therefore, the influence of such factors cannot be taken into account when applying to a converter with different layout. Although some authors suggest use of loss measurements given in the data sheets [14], [15], those measurements also suffer from the same limitation. Furthermore, simple formulations such as loss functions that only depend on the collector current magnitudes often ignore other significant influential factors. The representation of complex switching transients having number of distinct regions of operation with a simple fitting equation as done in [15], [23], [25]

causes inaccuracies. In addition, approaches that require simulation step sizes in the order of nanoseconds [12] are not appropriate for EMT simulation environments.

2.2.2 Switching Loss Estimation Based on Dynamic Models

It is possible to estimate switching losses using models that enable numerical simulation of the switching transients. Understanding of the dynamic behavior of IGBTs and power diodes is essential to develop suitable models. Behavior of power electronic devices such as power diodes and IGBTs share some commonalities due to similarity in the structures. There are two possible modeling approaches. The switching dynamics of an IGBT can be represented using a simple equivalent circuit comprising nonlinear circuit elements. These models can be used to generate the switching waveforms of IGBT voltage and current at terminals [27]. The second approach, which is sometimes referred to as the physics based modeling, involves simulation of the differential equations that govern the variations of internal fields, charge distribution, etc. in the device and relating them with the terminal voltage and current [28]. Although models based on both these approaches can be accurate, they require small simulation steps, high computational effort, and a large number of model parameters.

2.2.3 Switching Loss Estimations Using Algebraic Equations

The switching loss estimation models based on this approach rely on algebraic equations that are functions of not only the device current and voltage, but also of other parameters that depend on the circuit layout, device properties, and the gate driver characteristics. These loss equations are derived considering the circuit models that describe the transient

behavior of IGBTs and diodes. In [6], the product of two mathematical functions that describe the transient variations of the collector current and collector-to-emitter voltage of the IGBT has been integrated to obtain an expression for the switching loss. A refinement of the loss equations reported in [6] to obtain a simpler set of formulae with fewer parameters can be found in [14]. A similar approach has been applied in [29] to estimate the switching losses in a MOSFET based low power converter. In [29], the dynamics of the converter has been modeled in terms of a behavioral switching transient model of a MOSFET. Switching loss has been expressed as a function of the MOSFET parameters and operating condition (current and voltage) of the converter.

2.3 Construction and Transient Behavior of Power Diodes

The structure of a high-power diode is different from a conventional low power p-n junction diode. The semiconductor structure and the typical doping profile of a power diode are depicted in Figure 2-7. A lightly-doped long base semiconductor region called the drift region is included to increase the reverse voltage rating as depicted in Figure 2-7. This lightly-doped region significantly alters the transient behavior [30] and increases the forward voltage drop [31] of a power diode. Conductivity of the diode is considerably dependent on the availability of mobile carriers in the drift region. When P+ and N- junction at x=0 is forward biased, charge carriers are injected through junctions, P+ and N- as well as N- and N+. These charge carriers facilitate conduction of current between the

terminals. However, if the diode switches on with a high *di/dt* rate, it takes some time before this lightly-doped region is flooded with charge as depicted in [31].

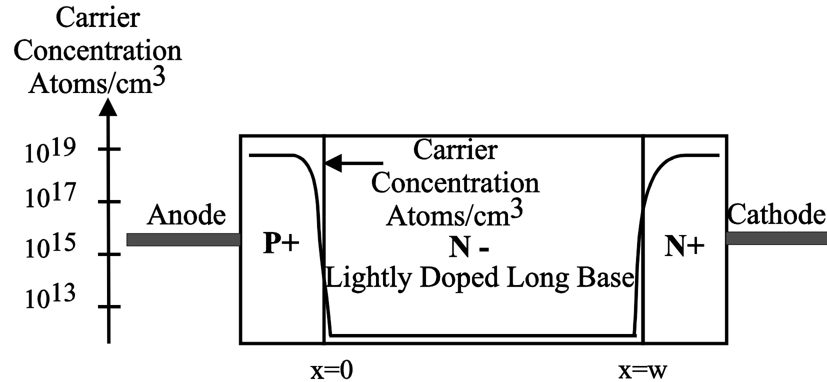


Figure 2-7-Power diode construction and doping profile [31]

The curves marked as $t_1 – t_5$ in Figure 2-8 represent the charge concentration levels at different times after the diode is forward biased with a high *di/dt*. Continuous injection of holes through both junctions causes gradual increase in the free carrier concentration in the drift region as depicted in Figure 2-8.

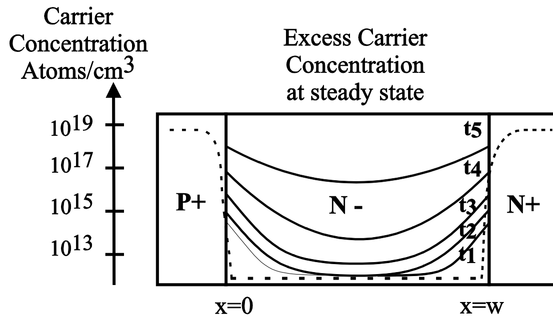


Figure 2-8- Carrier concentration profile

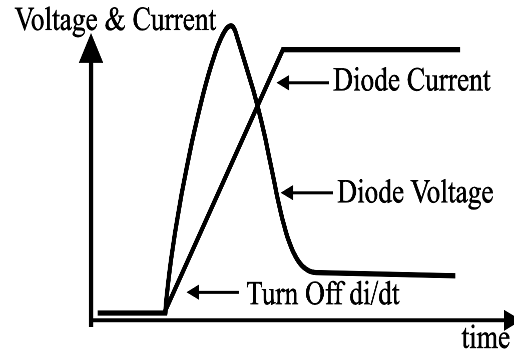


Figure 2-9-V-I Transients

Gradual increase of conductivity due to increase of the excess carrier concentration in the drift region is called conductivity modulation. This kind of phenomena takes place within other electronic power semiconductor devices such as IGBTs. Lower conductivity at the initial phase during the turn-on transient causes an overshoot in voltage if the current rises very rapidly as shown in Figure 2-9 [31]. This turn-on process of a power diode is

called forward recovery process and results in a power loss in the diode during the turn-on transient. Once the diode goes through the forward recovery transient, its forward voltage remains constant at its forward saturation voltage determined by the voltage drop across the junctions and drift region. However, the observed diode voltage overshoot is insignificant when compared with the typical supply voltages applied to the unit cell. Therefore, diode can be considered as an ideal switch during its turn-on transient (coincides with IGBT turn-off transient).

During the turn-off transient, excess carriers in the N- region do not disappear instantaneously as it takes some time for the stored charges to decay via extraction by the external circuit or recombining with accepter atoms as shown in Figure 2-10 [31].The depletion process of the stored charges is influenced by the external circuit [32]. In the unit cell, the diode reverse recovery process takes place when the load current is transferred from the diode to the IGBT. Once the load current is completely transferred to the IGBT, the stored charges within the diode depletes through the IGBT causing an overshoot in the collector current. However, the rate of increase of collector current is governed by the instantaneous gate-to-emitter voltage and transconductance of the IGBT. Therefore, during the initial phase of depleting stored charges, the time rate of decreasing diode current is governed by the IGBT behavior. The collector current approximately follows a linear increase before the reverse recovery phase. This variation follows even after starting the reverse recovery phase as there is no significant change in collector-to-emitter voltage. Therefore, an approximately linear increase of negative current through the diode is visible through the period between t_0 to t_3 as depicted in the Figure 2-11. However, some charge is depleted by the recombination process that takes place within the drift region

while extracting the charges via an external circuit. A space charge region starts to develop around the junction at t_3 and this space charge region facilitates development of reverse voltage across the diode. At this point the diode is unable to support further increase of its reverse current as dictated by the IGBT behavior. However, still it is possible to increase the negative current but not at the same rate as before.

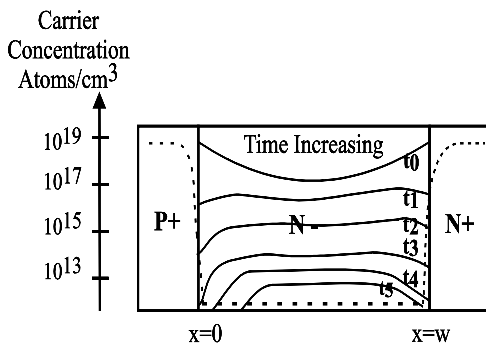


Figure 2-10-Instanatanoues carrier concentration during turn-off [30]

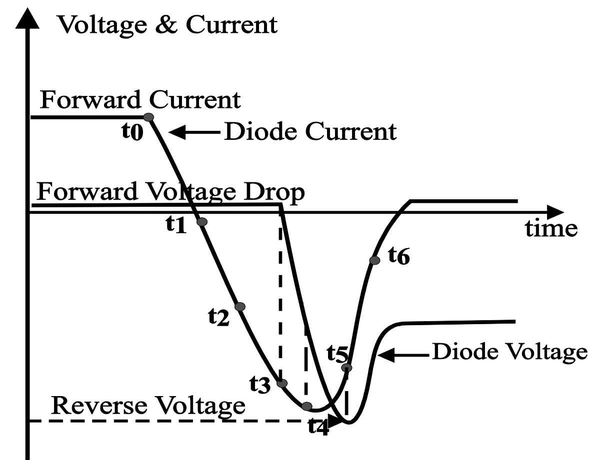


Figure 2-11-V-I Transients during turn-off [31]

Therefore, diode current increases up to t_4 while the slope is decreasing. Finally, the slope of the diode current reaches to zero at t_4. Voltage across the diode must be equal to the supply voltage at t_4 as the time rate of current is zero. After time t_4, diode current starts to decrease. The negative slope of the reverse recovery current induces an emf across the stray inductance. Induced emf causes an increase in the reverse voltage across the diode beyond the supply voltage as the collector-to-emitter voltage of the IGBT does not change rapidly. The diode reverse voltage reaches the peak at t_5. Diode current and voltage decreases at a rate determined by the charge dynamics inside the diode. Behavior of the power diode after instant t_3 can be represented using differential equations that describe the charge physics inside the diode [32], [33].

2.4 IGBT Construction and Operation

An IGBT is a power switching device designed to achieve improved output characteristics similar to a Bipolar Junction Transistor (BJT) switch and superior input characteristics similar to that of a Metal Oxide Silicon Field Effect Transistor (MOSFET). An IGBT can be represented as a cascaded MOSFET and a BJT in circuit modeling. Figure 2-12 shows construction of a typical IGBT and its symbol. As depicted in Figure 2-12, three consecutive regions p+, n-, and p+ forms a PNP bipolar transistor. The n- region marked is called the drift region. The drift region acts as the effective base of transistor. This bipolar transistor determines the output characteristics as it provides the conduction path between the collector and emitter terminals of the IGBT.

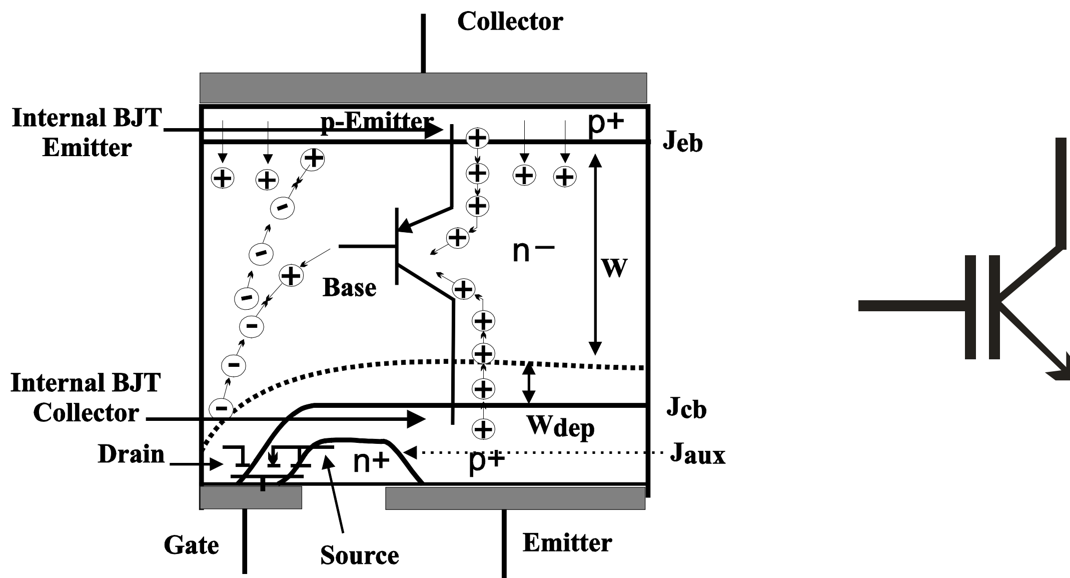


Figure 2-12-Semiconductor structure and symbol of IGBT

The gain of the bipolar transistor is said to be small [34]. Furthermore, a MOSFET structure is fabricated below the gate terminal of IGBT. This MOSFET input stage lowers the driving power requirement of the IGBT. The switching characteristic of an IGBT is sig-

nificantly affected by this MOSFET input stage. When the gate terminal voltage is greater than a certain threshold level, electrons in the p+ region beneath the gate terminal are attracted towards the surface under gate, and the holes are repelled away. In this way, a layer of negative movable charges is formed beneath the gate. This conduction layer is referred to as the inverted layer. The inverted layer provides a path between the external emitter terminal of the IGBT and the collector region of the internal bipolar transistor (pnp-collector). In the absence of an inverted layer, there is no conduction path between the external emitter pin and the collector of the internal bipolar transistor as the junction J_{cb} is reverse biased when the voltage between external collector and the external emitter terminal is positive. In the presence of the inverted channel, application of a positive voltage between the collector and emitter terminals of the IGBT causes holes in the p+ emitter region (pnp-emitter) to be injected through the forward biased base-emitter junction of the internal PNP BJT. The electron current supplied by the MOSFET makes the internal bipolar transistor turn-on as it provides a base current via recombination of holes and electrons. Increase of voltage between the IGBT collector and emitter terminals raises the positive bias on the emitter-base junction, J_{eb}, of the internal BJT. Increase of forward bias across J_{eb} injects more holes from the P+ emitter region into the base region of the internal BJT. At a certain value of IGBT collector-emitter voltage, the hole concentration eventually exceeds the background doping level of n- drift region. The excess carriers drift through the reverse biased collector-base junction, J_{cb}, of the bipolar transistor due to large electric field that appearing across it. The above internal conduction mechanism can be represented with the help of the circuit shown in Figure 2-13 [28]. This circuit model represents the mechanisms that aid the operation of an IGBT. The circuit rep-

resents the control action of the MOSFET over the BJT via supply of base current to the BJT.

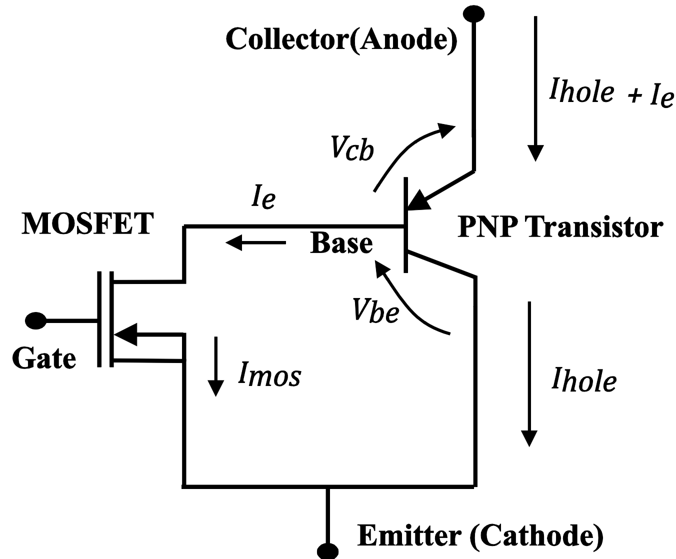


Figure 2-13-Circuit representation of an IGBT

In addition, this circuit model represents the requirement of an appropriate external voltage to achieve the bias requirements of the BJT. However, the above circuit model is inadequate for dynamic modeling purposes simply due to the complex nature of interactions within the device during the turn-on and turn-off. The region marked n- drift region, which is act as the base of the internal BJT, has a number of implications. This region is lightly doped and made wider to support high blocking voltage. In contrast, the base of a low power transistor is thinner when compared with the other two regions. During the turn-off process, once the MOSFET channel is rapidly removed, the internal BJT acts as an open base transistor [28]. During the turn-off process, first the IGBT collector current decreases rapidly due to the decrease of the base current supplied by the MOSFET. However, this collector current decay is abruptly slowed down once the base of the internal BJT is opened. After the base is opened, the ability to control the flow of charges in the

drift region via the gate-to-emitter voltage disappears. Stored charges in the drift regions decay via recombination when the base is open. This process causes a slowly varying current through the terminals of the IGBT called tail current. Therefore, the turn-off collector current transient is characterized by a rapid decrease followed by a slow decaying phase. This type of phenomena cannot be explained using the simple circuit model shown in Figure 2-16.

2.5 Physics-Based Modeling of IGBT and Power Diode Dynamics

Physic-based models of power semiconductor devices are developed with the help of the following basic relationships [35].

- Current density equation
- Current continuity equation
- Charge neutrality equation
- PN Junction equation
- Poisson equation
- Kirchhoff's laws at the device terminal

A combination of different basic relationships is used depending on the phenomenon to be modeled. Resistivity modulation, charge storage effect, and metal oxide semiconductor (MOS) capacitive effects are the major classes of physical phenomena taking place within an IGBT device. The behavior of charges in the lightly-doped drift region significantly affects the conduction characteristics of power switching devices. This effect is re-

ferred to as charge storage effect. Charge storage effect is modeled using a partial differential equation known as the ambipolar equation [22]:

$$D\frac{\partial^2 p}{\partial^2 x} = \frac{p}{\tau} + \frac{\partial p}{\partial t} \qquad 2\text{-}2$$

where D is the ambipolar diffusion constant, τ is the carrier life time. The ambipolar equation is solved to find the excess carrier concentration p in a point x of the drift region at a given time t. Solution for this partial differential equation is obtained by applying proper boundary conditions to the space with appropriate initial conditions. Therefore, physical dimensions of the IGBTs are essential for modeling using this approach. Methods of solving the ambipolar equation have been described in [30]. As mentioned earlier, the turn-off transient of an IGBT lasts for a long period of time due to the time needed to remove the stored charges in the open collector base junction of the internal BJT. The ambipolar equation is often used to model the charge storage effect in the estimation of the tail current.

The resistance between output terminals of a power diode or an IGBT is highly determined by the amount of free charge carriers present in the lightly doped layer. Hole concentration in lightly doped drift layer is determined by the forward bias applied across the junction J_{cb} as described in Section 2.4. As explained earlier in Section 2.3 and Section 2.4 conductivity modulation impacts the behavior of IGBTs and power diodes significantly.

Storage of charges in the zones bounded by the potential differences existing between the zone boundaries creates parasitic capacitances. These capacitances are called as MOS capacitances. Devices with an isolated gate such as IGBTs and MOSFETs have large MOS

capacitances that vary with the voltages across the relevant zones [36]. Thus physics based modeling involve a number of partial differential equations. In addition, physics based formulations should be solved with small time steps. A substantial amount of computational effort is required to simulate physics-based formulations at small time steps. Furthermore, physics based formulations include a number of parameters such as base width, carrier life time, area of the IGBT structure. Such design parameters are not easily accessible. The physics-based approach is unable to achieve the objectives of the research due to the high computational requirement and use of inaccessible parameters.

Some of the above phenomena can be represented in an approximate way in circuit models. For example, the effect of zones with stored charge can be represented as lumped parasitic capacitances between the external electrodes. Therefore, in analyzing the switching behavior an IGBT, it can be approximately modeled as shown in Figure 2-14.

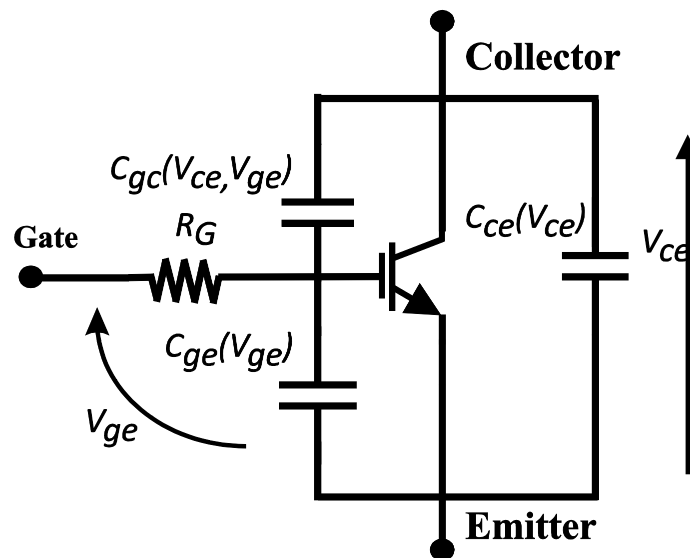


Figure 2-14-MOS capacitances of an IGBT

The capacitance between the collector and the emitter, C_{ce}, is called the junction capacitance, the capacitance C_{ge} between the gate and the emitter is called the gate capacitance, and the capacitance C_{gc} between the collector and the gate is referred to as the transfer ca-

pacitance or Miller feedback capacitance. These capacitances are nonlinear: the change in stored charge per unit voltage variation is not constant at all possible voltages. Therefore, these nonlinear capacitances are represented as voltage dependent MOS capacitances in modeling of the transient behavior. The typical variations of the three capacitances with the collector to emitter voltage are shown in Figure 2-15.

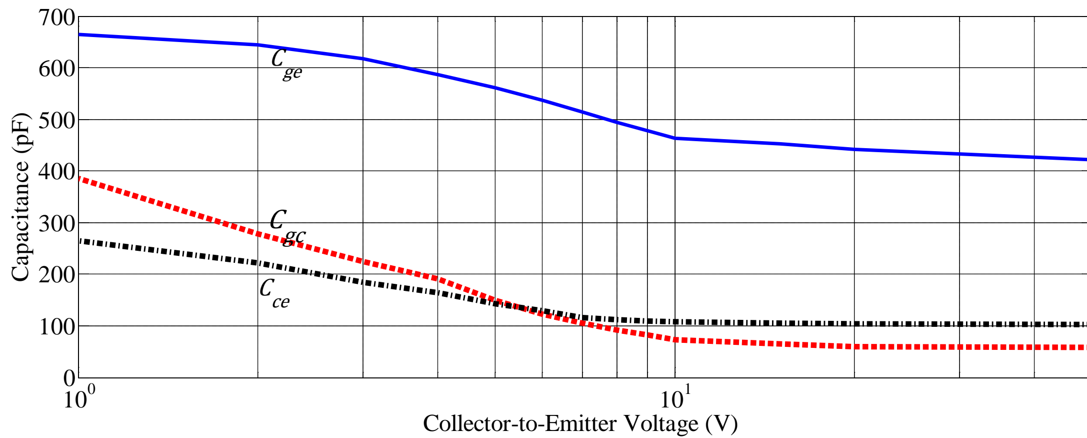


Figure 2-15-Collector-to-emitter voltage dependency of MOS capacitances

2.6 Circuit Model of an IGBT

Circuit models imitate the terminal voltages and currents variation during a switching event with the help of a lump parameter model. The formulations of a circuit model contain a set of ordinary differential equations rather than partial differential equations. Therefore, significantly lower computational effort is required to solve circuit models when compared to the computational effort required to solve physics-based models. In a circuit model, the switching behavior of an IGBT is represented with inter-electrode MOS capacitances and a controlled source. The controlled source mimics the coupling between the gate-to-emitter voltage and the collector current of an IGBT. Figure 2-16 shows the switching model of an IGBT used to simulate the switching behavior of an

IGBT. This circuit model of an IGBT is also called as macro-model or behavioral model of the IGBT. MOS capacitances represent the dynamic behavior as explained in Section 2.5.

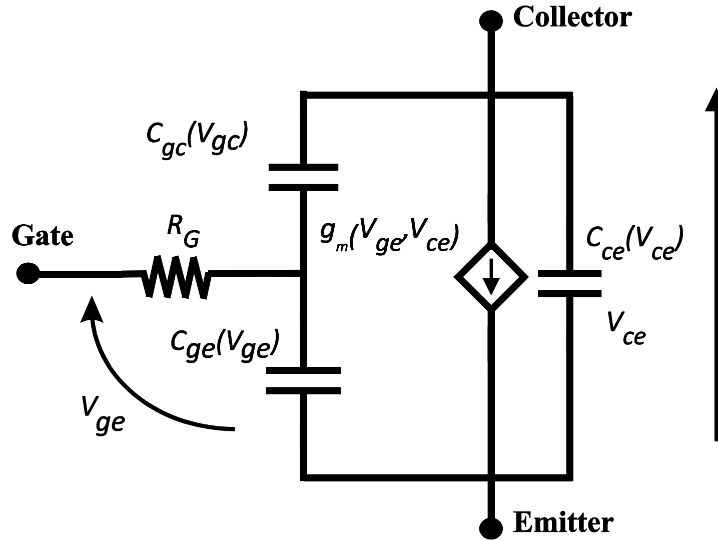


Figure 2-16-Circuit model of IGBT dynamics

The DC current gain of the IGBT is modeled by combining gain characteristics of MOSFET and bipolar transistor [37], [38]. During the switching transients, variation of collector-to-emitter voltage causes changes in the depletion layer width W_{dep} shown in Figure 2-12. The change in the depletion layer width results in a displacement current in the drift region. The direction of this current flow could be into the drift region or out from the drift region depending on whether the drift region width grows or shrinks. In the circuit model this phenomena is represented as charging or discharging of a voltage dependent capacitor. Therefore, in order to preserve the accuracy, the voltage dependency of the MOS capacitances must be taken into account in modeling. Influence of Miller feedback capacitor C_{gc} on switching behavior cannot be ignored [36]. This capacitor is a nonlinear function of collector to gate-to-emitter voltage and represents the state of the stored charges underneath the gate. In the circuit modeling of an IGBT, gain characteris-

tic of an IGBT is approximated with help of individual gain characteristic of the bipolar transistor and the MOSFET. Therefore, the gain of the IGBT should be the product of the gains of the MOSFET and the BJT as per Figure 2-13.

The gain of a MOSFET obeys two different laws below and above a certain voltage between drain and source called saturation voltage. The drain-to-source saturation voltage of a MOSFET is defined as $V_{ds\,(sat)} = V_{ge}\text{-}V_T$, where V_T is the threshold voltage and V_{ge} is the gate-to-emitter voltage of the IGBT. If the drain-to-source voltage is larger than the saturation voltage, the device is said to be operating in the saturation region. Equation 2-3 expresses the gain of a MOSFET when it is operated in the saturation region [38].

$$I_D = k_p\left(V_{ge} - V_T\right)^2 \qquad \text{2-3}$$

where k_p is a constant.

When the drain-to-source voltage is less than the saturation voltage, the MOSFET is said to be operating in the linear region. The gain of the MOSFET is given by Equation 2-4 when it is operated in the linear region [38].

$$I_D = k_p\left[\left(V_{ge} - V_T\right)V_{ds} - {V_{ds}}^2/_2\right] \qquad \text{2-4}$$

Overall gain of the IGBT can be approximated by the gain of the cascaded MOSFET and BJT. The current through the emitter terminal of the BJT is $(1+\beta)$ times the MOSFET output current. β is the DC current gain of the bipolar transistor. According to Figure 2-13, voltage between the drain and source V_{ds} of the MOSFET is such that $V_{ds}=V_{ce}\text{-}V_d$. V_d represents voltage drop in the forward biased emitter base junction of the bipolar transistor. Therefore, saturation voltage $V_{ce\,(sat)} = V_{ge}\text{-}V_T+V_d$. Therefore, the overall gain of

the IGBT in the linear and saturation regions can be expressed respectively by Equation 2-5 and Equation 2-6.

$$I_C = k_p(1+\beta)\left[(V_{ge}-V_T)(V_{ce}-V_d) - {(V_{ce}-V_d)^2}/{2}\right] \quad \text{2-5}$$

$$I_C = k_p(1+\beta)(V_{ge}-V_T)^2 \quad \text{2-6}$$

The behavior described by the above two equations does not consider the high level injection condition and drop across the drift region [38] as in the physics-based approach of modeling. However, two polynomials fitted with the help of experimental observations can be used to correct the behavior. Equation 2-7 and Equation 2-8 depicts the modified gain characteristics.

$$I_C = k_p(1+\beta)\left[(V_{ge}-V_T)(f_1 \cdot V_{ce}-V_d) - {(f_1 \cdot V_{ce}-V_d)^2}/{2}\right] \quad \text{2-7}$$

where $f_1 = a_0 + a_1 V_{ge} + a_2 V_{ge}^2$

The function f_1 makes the saturation voltage of the MOSFET equals to the saturation voltage of the IGBT.

$$I_C = k_p(1+\beta) f_2 (V_{ge}-V_T)^2 \quad \text{2-8}$$

where $f_2 = b_0 + ab_1 V_{ge} + b_2 V_{ge}^2$

These correction functions assure a smooth transition of gain characteristics between saturation and linear region. Collector current transients of IGBT switches occur at much larger collector-to-emitter voltages when compared with gate-to-emitter voltage as depicted in the Figure 2-5. The MOSFET is operated well above the saturation voltage. Therefore, correction of gain characteristics is not essential in estimating collector current transients of the unit switching cell.

2.7 Methodology Suggested for Switching Loss Estimation in EMT Simulations

In this chapter, details of the mechanisms involved in power diodes and IGBT devices were described in simple terms. Various approaches employed for modeling the switching processes were discussed. Based on the survey presented in this chapter, physics based detailed models are not appropriate due to model complexity and the need for large number of parameters, which are generally not disclosed by the manufacturers. The simplest approaches such as lookup tables based on measurements do not take into account the effect of parameters specific to a given converter implementation, and therefore are not accurate. It is apparent that behavioral models based on the empirical fittings or loss equations based on the unit cell behavior are reasonable approaches for loss estimation in EMT type simulation environment. In behavioral models, computational effort, model complexity, and the data requirements are moderate, and at the same time they take into account important internal and external influential factors such as stray inductances and gate drive characteristics. With this approach, it is possible to more accurately estimate switching losses at different possible operating conditions.

In terms of incorporation of the loss model into the EMT simulation environment, the easiest approach is to represent losses as functions of the switched current and voltage imposed on the device. The loss data can be represented using look up tables or using fitted curves. The loss data required to create the lookup tables can be generated using a circuit model. The circuit model can be used to estimate switching losses at intervals of load currents and voltages with specified IGBT parameters, gate drive parameters, and

stray inductance values for a given unit cell prior to the actual simulation. Then the lookup table generated using the unit switching cell circuit model can be used to estimate switching losses during the simulation. Pre-switching and post-switching collector-to-emitter voltages and currents across the IGBT device is determined by EMT simulation with help of ideal switch model.

Circuit models that mimic device behavior at each distinct phase during the switching transient are developed by considering the dominant dynamics and interactions in the unit switching cell in the respective phases.

Chapter 3

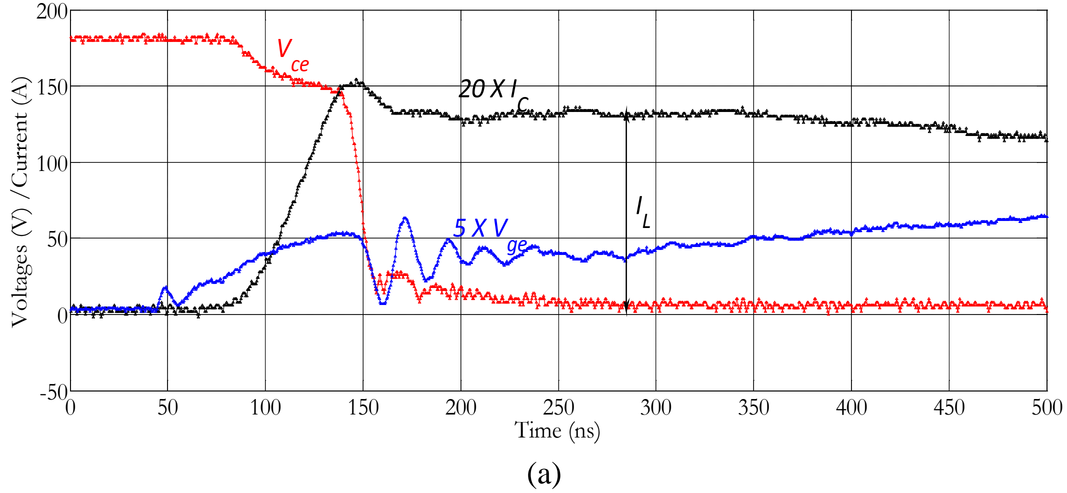
Turn-on Transient Model

In this chapter, turn-on behavior of the unit cell is explained. Design of the turn-on transient model is described step-by-step with the rationale behind the design. A procedure for extracting the parameters required for the turn-on transient model is also proposed.

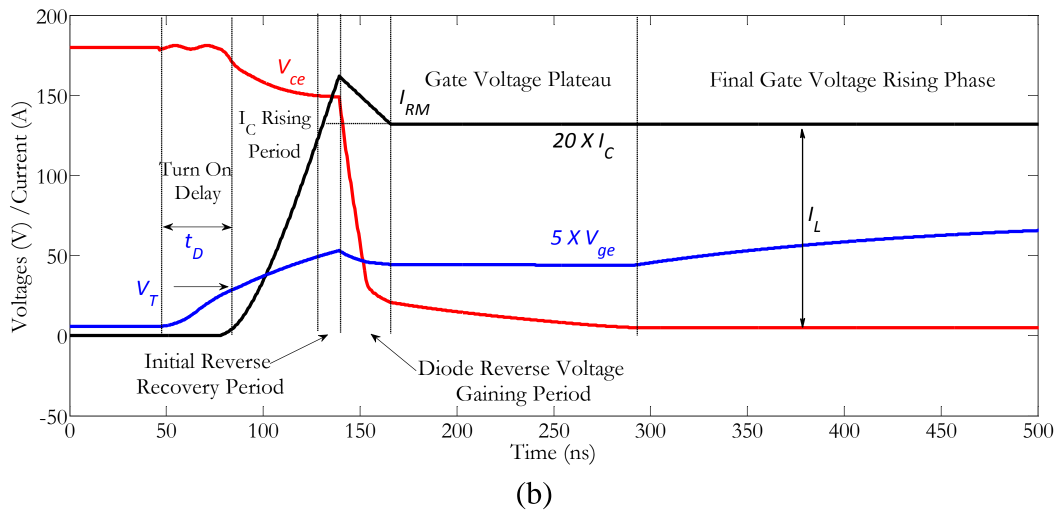
3.1 Turn-on Behavior

The turn-on transient of the unit switching cell follows several distinct phases. These distinct phases of the collector-to-emitter voltage and collector current variations are due to different dynamics that dominate during each of the periods. Therefore, terminal characteristics of the IGBT can be described using the most prominent phenomenon in each phase. Other less significant dynamics can be ignored to simplify the circuit model for the IGBT. Figure 3-1(a) shows the measured trajectories of the collector-to-emitter voltage and collector current during the turn-on transient. Transient measurements are done using a digital storage oscilloscope with the help of a test setup described in Section 5.1. Figure 3-1(b) depicts the approximate variations of the voltage and current for the same transient. Minor oscillations in the voltage and current are ignored in the approximated

waveforms. The emitter terminal voltage of the IGBT is taken as the reference voltage of the unit cell model shown Figure 2-5.



(a)



(b)

Figure 3-1-Distinct phases of the turn-on transient (a) measured waveforms, (b) approximated waveforms

Therefore, collector-to-emitter (V_{ce}) voltage might be referred to as the collector voltage and the gate-to-emitter voltage (V_{ge}) might be referred as the gate voltage in this thesis. The collector current is referred as I_C. Important dynamics of each distinct phase after the approximation are explained below.

3.1.1 Turn-on Delay Period

Once a positive gate drive is applied to the gate terminal, the gate-to-emitter voltage starts to increase. However, output of the IGBT does not respond to the gate-to-emitter voltage variation until it reaches a certain level, which is referred to as gate threshold voltage V_T. Time taken by the gate-to-emitter voltage to reach the threshold value of the IGBT is called turn-on delay and is denote by t_d.

3.1.2 Collector Current Rising Period

As shown the Figure 3-1 (a), the collector current rises simultaneously with the gate-to-emitter voltage when the gate-to-emitter voltage is higher than the threshold voltage V_T. The growth of collector current results in a drop in the collector-to-emitter voltage due to induced emf across the stray inductance. The collector-to-emitter voltage is often considered as following a plateau during this period. However, occasionally collector-to-emitter voltage slightly increases again at the end of this phase or subsequent phase when the rate of rise of the collector current slows down.

3.1.3 Initial Reverse Recovery Period

The collector current overshoots beyond the load current I_L as depicted in the Figure 3-1 (a). This is due to the reverse recovery current of the outgoing freewheeling diode. Since the collector current and the gate-to-emitter voltage are tightly related during this phase, the gate-to-emitter voltage rises with the collector current. The collector-to-emitter voltage does not vary significantly during this phase. As already described in Section 2.3 and depicted in Figure 2-12, voltage across the freewheeling diode is insignificantly low for

most of the time in this phase. However, at the end of the phase, diode voltage suddenly reaches a level that is equal to the difference between the collector-to-emitter voltage plateau and the supply voltage, as the rate of change of the collector current becomes almost zero at the end of the initial reverse recovery period.

3.1.4 Diode Reverse Voltage Gaining Period

The reverse recovery current starts to decay in this phase. The collector-to-emitter voltage falls rapidly when the diode starts to gain reverse voltage during this phase. The gate-to-emitter voltage decreases slightly as the collector current decreases following the tight relationship between the two. Careful examination of Figure 3-1(a) shows that although the collector current is equal to the load current at the end of this phase as well as at the end of the collector current rising phase (or at the beginning of the initial reverse recovery period), the gate-to-emitter voltage at the end of this phase is slightly less than the gate-to-emitter voltage at the end of collector current rising phase. This discrepancy is due to variations in the transconductance (or gain) of the IGBT in the two phases.

3.1.5 Gate-to-Emitter Voltage Plateau Period

After the diode reverse voltage gaining period, the turn-on transient follows a phase where the average gate-to-emitter voltage remains at a constant value below the peak gate drive voltage as seen in Figure 3-1 (a) [14], [22]. The collector-to-emitter voltage decreases and the rate of falling of collector-to-emitter voltage decreases continually. The later part of the collector-to-emitter voltage trajectory is called the collector-to-emitter voltage tail [21].

3.1.6 Final Gate-to-Emitter Voltage Rising Period

Once the collector-to-emitter voltage reaches a value closer to the saturation voltage, the gate-to-emitter voltage starts to rise as depicted in Figure 3-1 (a). The rate of rise of the gate-to-emitter voltage during this phase is less than the rate of the rising gate-to-emitter voltage during the turn-on delay period.

3.2 Modeling of Turn-on Transient

When an IGBT is used in a circuit, its terminal behavior (as described by the variations of the collector current and the collector-to-emitter voltage) is determined not only by the internal processes represented by the equivalent circuit shown in Figure 2-17, but also by the characteristics of the external circuit. Therefore, it is best to focus on the specific behavior of the IGBT within the unit cell for more accurate modeling when a behavioral approach is used. The switching model of the IGBT shown in Figure 2-17 is duplicated in Figure 3-2 for reference in the following discussion.

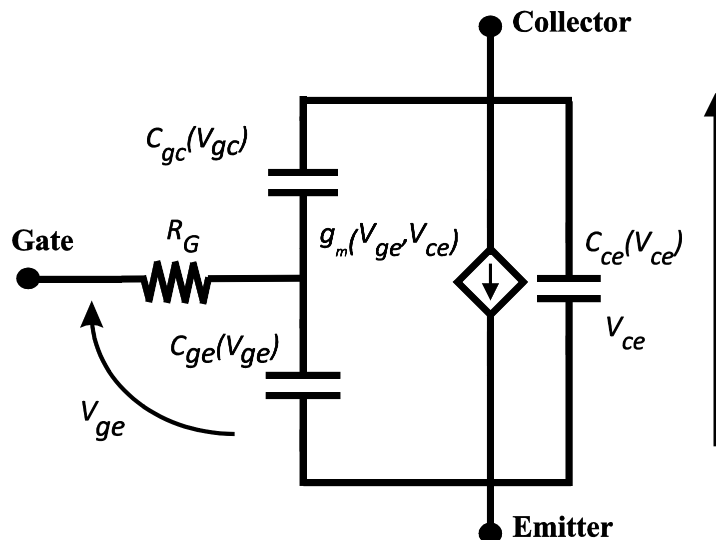


Figure 3-2-Switching model of IGBT

Dynamics represented by each element of this IGBT model may or may not be significant during a given phase in the turn-on transient. Therefore, modeling is achieved by selecting only the essential and dominant process in each distinct phase as described in Sections 3.2.2 through 3.2.7. This involves selection of the components that reflect processes inside the IGBT from the switching model, modeling of the interaction of the IGBT with the external circuit, identification of the parameters that represent selected phenomena, and utilization of special simulation techniques if needed.

3.2.1 Pre-Switching Condition of the IGBT

Pre-switching voltages between the terminals reflect the level of stored charges in the equivalent capacitors or accumulated charges within the physical regions between the terminals. Therefore, it is required to set the stored charges in each capacitor before starting the simulation. Pre-switching voltage across capacitor C_{ce} is approximately the supply voltage as the forward voltage drop across the diode is very small when compared with supply voltage. The saturation voltage of the gate driver appears across C_{ge}. The difference between the above two voltages appears across the C_{gc}. However, the voltage across C_{gc} almost equals the supply voltage as the output saturation voltage level of the gate driver and the diode forward voltage drops are very low. The collector side of the C_{gc} contains positive charges and gate side contains negative charges at this state.

3.2.2 Phase-1: Turn-on Delay Phase Model

Rise of the gate-to-emitter voltage in this phase occurs due to change in stored charges in C_{ge}. In addition, since the collector-to-emitter voltage is fixed, the rising gate-to-emitter

voltage also requires decreasing the voltage across C_{gc} by reducing the amount of stored charges within C_{gc}. This is achieved by supplying positive charges to the negatively charged gate side terminal of C_{gc} from gate drive. Therefore, the gate-emitter capacitance C_{ge} is getting charged and the gate-collector capacitance C_{gc} is getting discharged via gate resistance R_G during this phase. The circuit shown in Figure 3-3 (a) represent behavior of the unit cell in this phase.

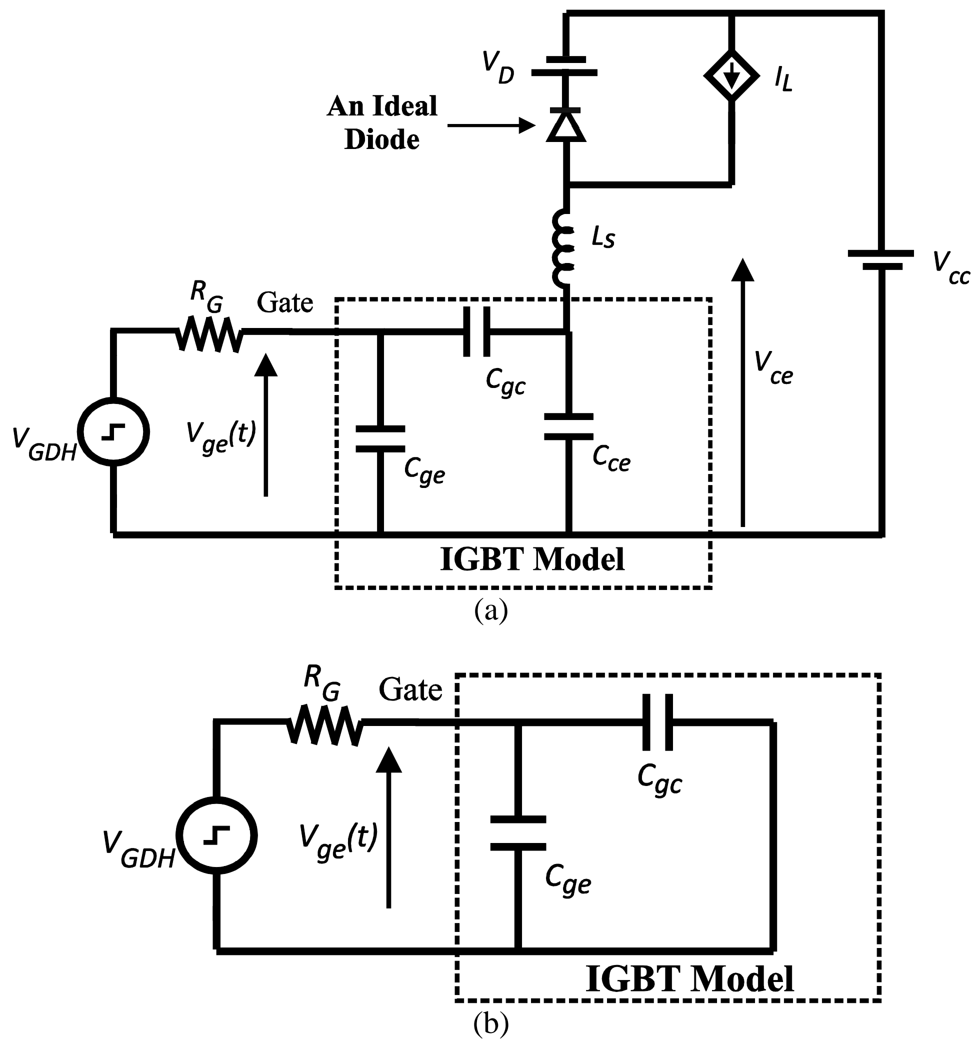


Figure 3-3- Turn-on delay model (a) Model representing the dynamics (b) An approximated model

The freewheeling diode carries the load current I_L as depicted in Figure 3-3 (a) and the collector-to-emitter voltage does not vary during this stage. Alternatively, behavior of the unit cell can be simulated with the circuit model shown in Figure 3-3 (b) as the variation of collector current and collector-to-emitter voltage are insignificant during this phase. The finite rise time of the voltage pulse applied by the gate drive affects the switching transient. The ramp up time of the voltage pulse can be comparable with the turn-on delay in some applications. In such situations, the gate drive can be modeled with a DC step source having a finite ramp up time. During this phase, the capacitance C_{ge} is much larger than C_{gc} and C_{ce}. Also the capacitances C_{ge} as well as C_{gc} are considered fixed capacitors as it is found to be a fair approximation. In addition, internal gate resistance of the IGBT and driver output resistance may need to be taken into account, especially when a lower external gate drive resistance R_G is utilized. Once the gate-to-emitter voltage reached to the threshold voltage level, the circuit model is modified to simulate the approximated dynamics of the next phase with the proper initial conditions estimated during this phase.

3.2.3 Phase-2: Model of the Collector Current Rising Phase

During Phase-2, the collector current increases with the gate-to-emitter voltage as shown in the Figure 3-4. As the collector-to-emitter voltage is much higher than the gate-to-emitter voltage during this phase, the transfer characteristic between V_{ge} and I_C is specified by Equation 2-6 [38], [39]. The gate-to-emitter voltage rises as the gate-emitter capacitance is still getting charged. A fraction of the current supplied by the gate drive discharges the capacitor C_{gc} during this phase. Increase of gate-to-emitter voltage causes an increase in the collector current.

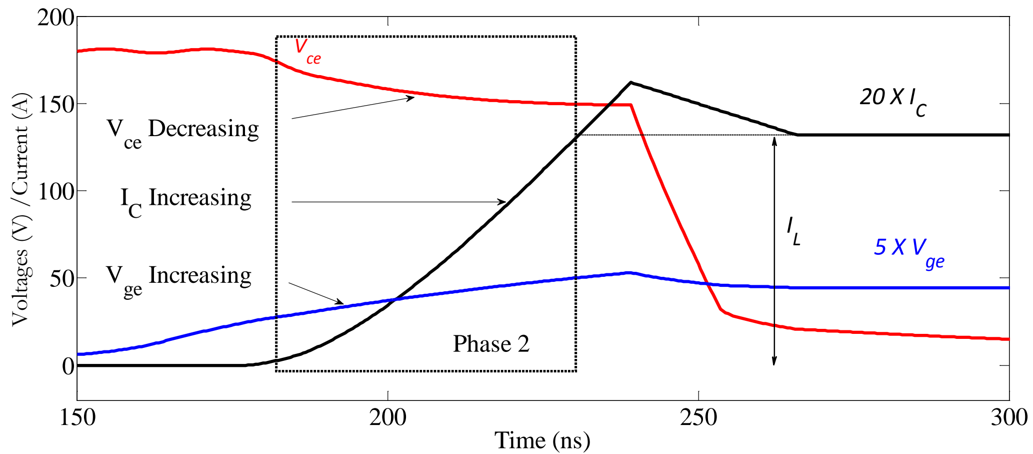


Figure 3-4-Transients during Phase-2

Transient behavior during the phase can be modeled by the circuit depicted in Figure 3-5.

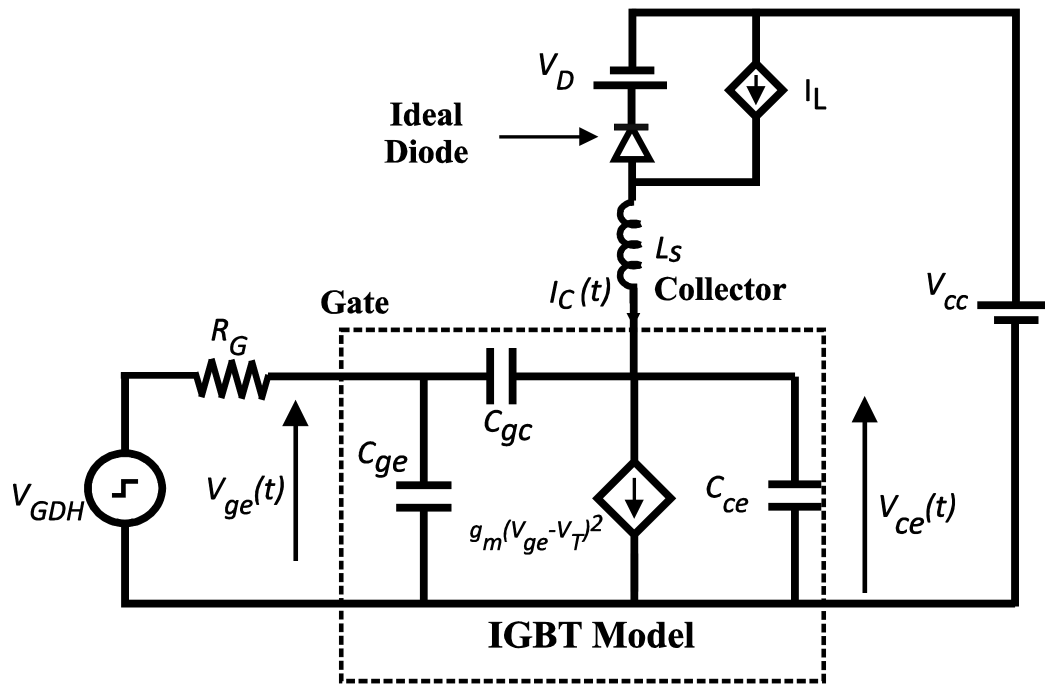


Figure 3-5-Model of the collector current rising phase

As already mentioned, the transfer characteristic between V_{ge} and I_C is specified by Equation 2-6 [38], [39], which is reproduced here for the convenience.

$$I_C = K_{g_adjust} k_p (1+\beta)\left(V_{ge} - V_T\right)^2 \quad \text{3-1}$$

All terms in Equation 3-1 are already defined under Equation 2-6 except the constant K_{g_adjust} which represents the ratio between the actual gain at Phase-2 and Phase-3 in the turn-on transient to the nominal gain of the IGBT, which is observed in the subsequent phases. It is observed that the estimated gain during Phase-2 and Phase-3 in the turn-on transient is less than the nominal gain estimated during the other phases in the turn-on transient. The factor K_{g_adjust} is used to represent the reduced gain during this phase. Transconductance is defined as the rate of change of the collector current with the gate-to-emitter voltage, and its value depends on the gate-to-emitter voltage. Therefore, trans-conductance can be expressed as in Equation 3-2.

$$g_{fe}(V_{ge}) = \left.\frac{\partial I_C}{\partial V_{ge}}\right|_{V_{CE=Const}} = 2K_{g_adjust}(1+\beta)k_p(V_{ge} - V_T) \qquad 3\text{-}2$$

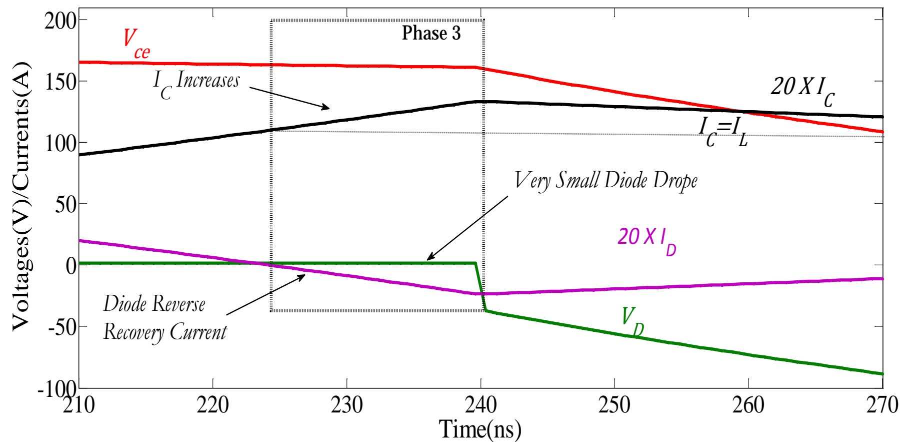
where β is the DC current gain of the bipolar transistor in IGBT, k_p is a constant, V_{ge} is the gate-to-emitter voltage of the IGBT, and V_T is the threshold voltage of the IGBT. An increase of collector current which flows through the IGBT causes a corresponding de-crease of current through the freewheeling diode.

The reason behind the collector-to-emitter voltage drop during this phase is the induced emf across the stray inductance L_s due to changing current through it. Furthermore, time taken to discharge stored charges within the capacitance C_{ce} affect the time rate of falling collector-to-emitter voltage. These effects are represented by the stray inductance L_s and the collector-to-emitter capacitor C_{ce} in the model circuit shown in the Figure 3-5. Reflec-tion of the collector-to-emitter voltage variation to the gate side due to Miller feedback is apparent from the practical observations. The effects of feedback from the collector-to-emitter voltage variation to the gate side as well as the diversion of gate drive current to

discharge the Miller capacitor (C_{gc}) are represented by the capacitance C_{gc} connected between the gate and the collector. As the variation of capacitance of each capacitor is insignificant at higher collector-to-emitter voltages, the capacitors are simulated with fixed values during this phase to achieve a certain degree of simplicity as in [37]. The equivalent circuit shown in the Figure 3-5 is simulated to include all of the above dynamics. This phase is simulated until the collector current reaches the load current I_L. At this point, transfer of load current from the freewheeling diode to the IGBT is completed.

3.2.4 Phase-3: Model of Initial Reverse Recovery Phase

The reverse recovery process of the freewheeling diode begins once the collector current reaches the load current. Stored charges within the base region of the power diode discharge during this phase as explained in Section 2.3. During this phase, the rate of discharging of stored charges in the diode, (or the diode current) is determined by the external circuit [32]. Thus, it is assumed that the collector current continues to rise as (as shown in Figure 3-6(a)) dictated by the increasing gate-to-emitter voltage according to Equation 3-1 [21], as in the previous phase.



(a)

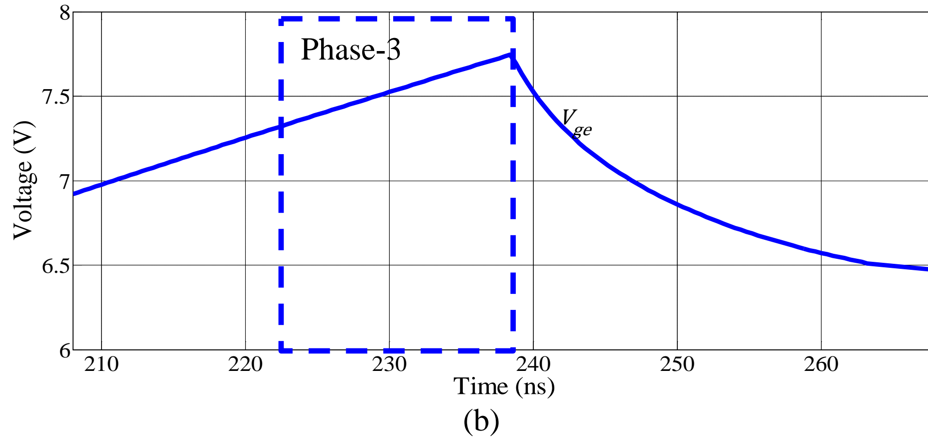


Figure 3-6-Transients during Phase-3 (a) Transients of V_{ce}, I_c, V_d, and I_d (b) Transient of V_{ge}

This is clearly observed in practical measurements. In Phase-3, the ideal diode in the circuit model is replaced with a short circuit as shown in Figure 3-7.

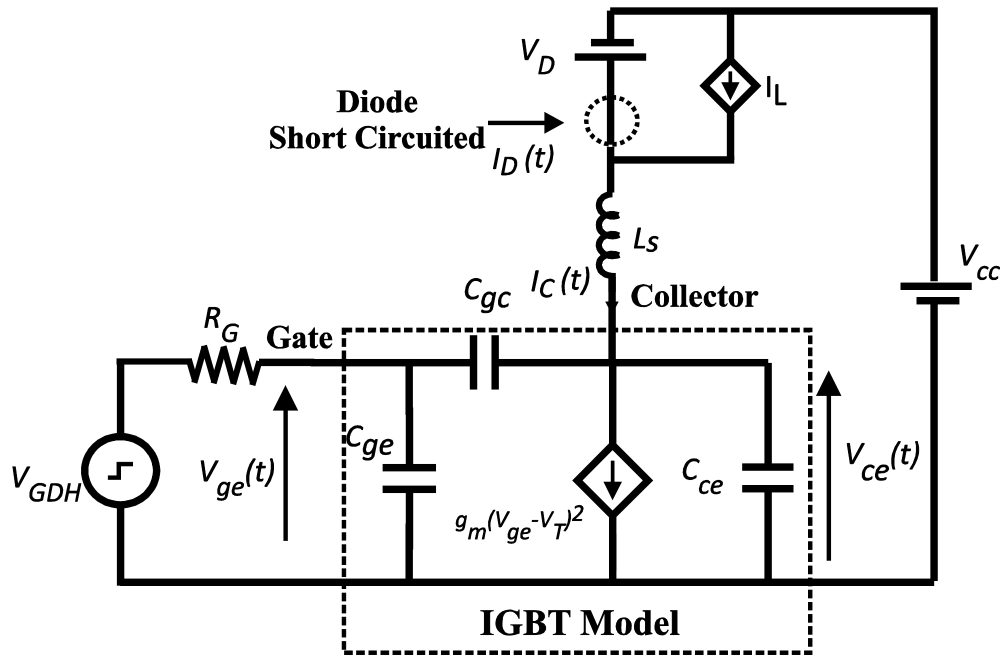


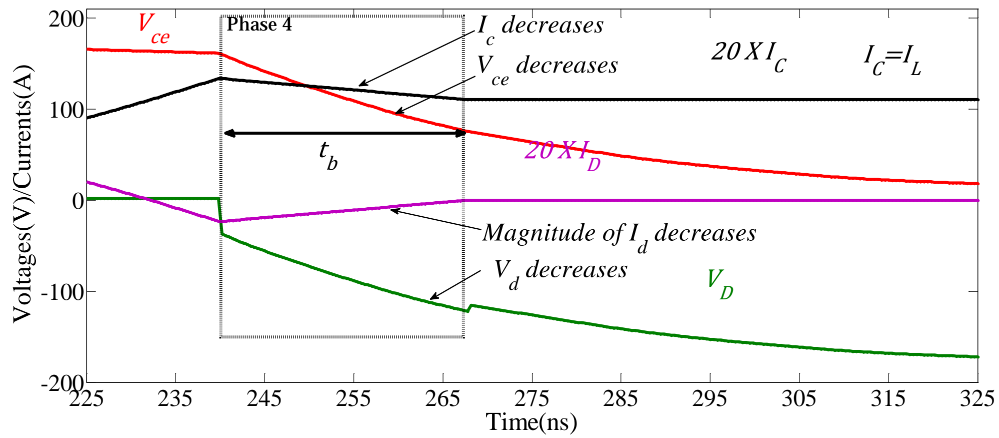
Figure 3-7-Model of the initial reverse recovery phase

The diode is replaced with a short circuit because, (i) the voltage across the diode is still very small in this phase, (ii) the current that depletes the stored charge in the diode is de-

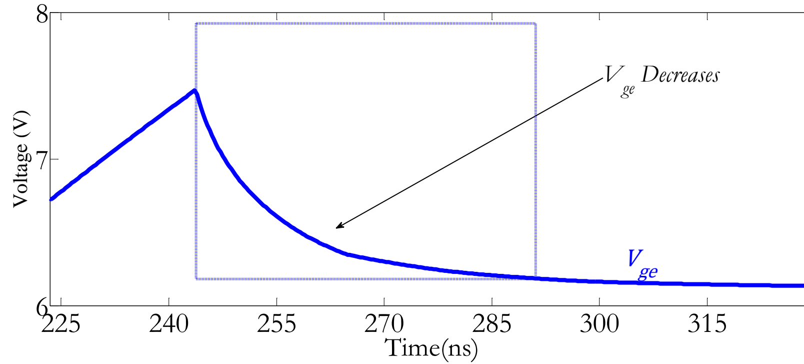
termined by the external circuit, and (iii) the current is in the reverse direction. The collector current is governed by the instantaneous gate-to-emitter voltage of the IGBT. The dynamics that determine the collector-to-emitter voltage is the same as in the previous phase. The model is similar to the model used in Phase-2, except for a short circuit that representing the ideal diode. This circuit is simulated until the collector current reaches (I_L + I_{RM}), where I_{RM} is the peak reverse recovery current. Estimation of the I_{RM} is explained in Section 3.2.8.

3.2.5 Phase-4: Diode Reverse Voltage Gaining Phase

The freewheeling diode gains reverse voltage during this phase and the reverse recovery current decreases as shown in Figure 3-8 (a). In order to retain the simplicity of the model, and based on experimental observations, the fall of diode reverse recovery current is assumed to be linear as in [21], [14]. Therefore, the falling reverse recovery current is modeled with an independent controlled current source that injects a current that falls from I_{RM} to zero during the period t_b shown in Figure 3-8 (a). The current source connected in parallel with the load current source shown in Figure 3-9 represents the variation of diode current during this phase. Instantaneous voltage across the diode is determined by the variation of the collector-to-emitter voltage. Thus the ideal diode is replaced with an open circuit (by opening switch S_1 in Figure 3-9) in Phase-4. The collector current is equal to the sum of instantaneous diode current and the constant load current, and in this phase, both of them are externally defined. Therefore, in contrast to the previous phases, the collector current is driving the circuit dynamics.



(a)



(b)

Figure 3-8-Transient during Phase-4 (a) Transients of V_{ce}, I_C, V_d, and I_d (b) Transient of V_{ge}

Since the collector current is no longer determined by V_{ge}, the controlled current source that determined the collector current is removed from the circuit (by opening switch S_2 and short circuiting the current source with S_3). The collector current passes through the controlled voltage source depicted as V_{syn} in Figure 3-9 , which sets the collector-to-emitter voltage. However, since V_{ge} and I_C are still tightly coupled through Equation 3-1, with the fall of collector current, the gate-to-emitter voltage is also forced to decrease in this phase of the transient.

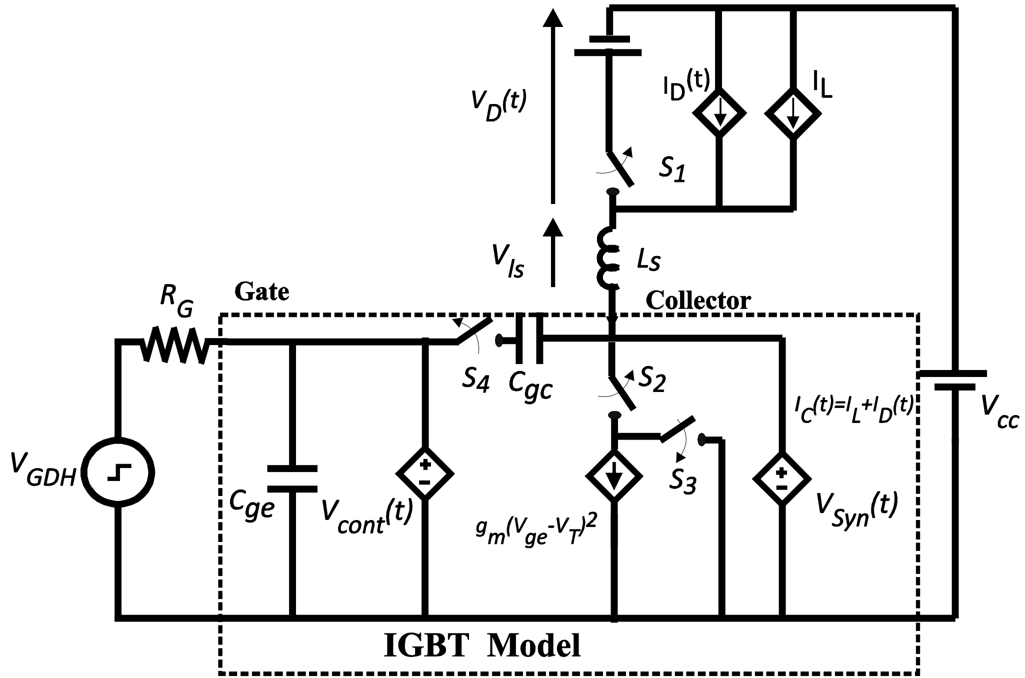


Figure 3-9-Model of the later reverse recovery phase

This drop in gate-to-emitter voltage is clearly visible in measurements, and is modeled in the circuit using the gate side control voltage source V_{cont} shown in Figure 3-9. The instantaneous voltage across gate side control source is calculated from Equation 3-3, which is obtained by rearranging Equation 3-1.

$$V_{ge}(t) = V_T + \sqrt{\left({I_c(t)}/{gain(t)} \right)} \qquad 3\text{-}3$$

Variables used in Equation 3-4 are already defined under the Equation 3-1 except the term $gain(t)$ which represents the variable IGBT gain during this phase. It is assumed that gain increases linearly from the adjusted gain to the nominal gain during this phase. The variation of gain with the collector-to-emitter voltage is estimated using Equation 3-4.

$$gain(t) = \frac{k_p(1+\beta)(1-k_{g_Adjust})(t_0 - t)}{t_b} + k_{g_Adjust} k_p(1+\beta) \qquad 3\text{-}4$$

where t_0 is the time instant of starting the phase and t_b is the duration of the phase.

Slope of the collector to emitter voltage falling trajectory gradually decreases as shown in Figure 3-8. Time taken to release the stored charges in a charge accumulation layer that was developed under the gate during turn-off is described as the reason behind gradual decrease of the rate of change of the collector-to-emitter voltage [22]. This phenomenon is manifested as a variation of the capacitance of C_{gc}. In Figure 3-1, rapid decrease of the collector-to-emitter voltage is apparent during the early period of this phase where C_{gc} is small. Later, the collector-to-emitter voltage falling rate decreases as C_{gc} increases with the decreasing collector-to-emitter voltage. The process behind development of the collector-to-gate voltage due to depletion of the stored charges in the nonlinear capacitor C_{gc} can be modeled as explained below. The discharging current is equal to the rate of change of the stored charge in C_{gc}, which is a function of V_{gc}

$$I_{Discharge} = \frac{d\left[C_{gc}(V_{gc}) \cdot V_{gc}\right]}{dt}$$

where $I_{Discharge}$ is the current that supplies the charges to C_{gc}. Alternatively the above expression can be written using the chain rule as

$$I_{Discharge} = C_{gc}(V_{gc})\frac{dV_{gc}}{dt} + V_{gc}\frac{dC_{gc}(V_{gc})}{dV_{gc}}\frac{dV_{gc}}{dt}$$

C_{gc} is only depended on V_{gc}. Hence, the derivative of C_{gc} with respect to the V_{gc} is a function of V_{gc}. Therefore,

$$I_{Discharge} = \left[\, C_{gc}(V_{gc}) + V_{gc} f(V_{gc})\right]\frac{dV_{gc}}{dt}$$

Consequently the discharging current and the change in collector-to-gate voltage can be related with the help of a fictitious Miller capacitor C_{gc}' as given in Equation 3-5

$$I_{Discharge} = C_{gc}'(V_{gc})\frac{dV_{gc}}{dt} \tag{3-5}$$

where C_{gc}' is the sum of real capacitance C_{gc} and another component that is also dependent on V_{gc} as given in Equation 3-6

$$C_{gc}'(V_{gc}) = C_{gc}(V_{gc}) + V_{gc}f(V_{gc}) \tag{3-6}$$

The decrement of the voltage between collector and gate during a small time period ΔT_s can be found by discretizing Equation 3-5. Equation 3-7 relates small change in collector-to-gate voltage to the charging current with help of fictitious Miller capacitance C_{gc}' defined in Equation 3-6.

$$\Delta V_{gc} \approx \frac{I_{Discharge}\Delta T_s}{C_{gc}'(V_{gc})} \tag{3-7}$$

Positive current flowing into the gate side of the C_{gc} depletes the negative charges stored in the gate side. Therefore, $I_{Discharge}$ results in a decrease of the voltage across C_{gc} or the voltage between collector and gate terminals. Therefore, Equation 3-7 estimates the decrease of collector-to-gate voltage during a time step of ΔT_s (at a particular value of V_{gc}). The discharge rate of C_{gc} is depended on the current supplied from the gate drive and the additional current supplied due to discharging of C_{ge}. Based on the circuit model, the discharging current can be calculated using Equation 3-8.

$$I_{Discharge}(t) = \frac{\left(V_{GDH} - V_{ge}(t)\right)}{R_G} + C_{ge}\frac{dV_{ge}(t)}{dt} \tag{3-8}$$

where V_{GDH} is the output voltage of the gate driver and C_{ge} is the gate to emitter capacitance. The collector-to-emitter voltage is the sum of the voltage across C_{gc} and gate-to-

emitter voltage. However, the collector-to-emitter voltage variation can be attributed to the variation of the voltage across the C_{gc} as the variation of the gate-to-emitter voltage is very small compared to the variation of voltage across C_{gc}. Hence, variation of the collector-to-emitter voltage is assumed to be solely determined by the discharging process of C_{gc} and the effects of C_{ce} are neglected hereafter. Estimated collector-to-emitter voltage is synthesized with the help of a controlled voltage source depicted as V_{syn} in Figure 3-9. Note that the Miller capacitor is removed from the model circuit (by opening switch S_4) at this phase as the effect of the Miller capacitor is modeled with a controlled sourced V_{syn}. The value of V_{syn} is updated in each time step using ΔV_{gc} estimated using Equation 3-7. Equation 3-9 describes instantaneous voltage of source V_{syn}.

$$V_{syn}(t + \Delta T_s) = V_{syn}(t) - \Delta V_{gc}(t) \quad 3\text{-}9$$

Sudden disappearance of the decreasing diode current causes an oscillation of collector-to-emitter voltage-to-emitter voltage as well as gate-to-emitter voltage at the end of this phase. The gate-to-emitter voltage oscillation is more visible than collector-to-emitter voltage oscillation as seen in Figure 3-1. The collector current is no longer determined by the gate-to-emitter voltage after this phase. Therefore, this oscillatory behavior of the gate-to-emitter voltage is not modeled.

3.2.6 Phase-5: Gate-to-Emitter Voltage Plateau

The gate-to-emitter voltage remains at a more or less constant value during this phase. The collector-to-emitter voltage variation last even after decaying the diode transient as depicted in the Figure 3-10. As already described in the previous section, the gate-to-emitter voltage is determined by the collector current which remains almost constant dur-

ing the phase. Therefore, gate-to-emitter voltage also does not vary during this phase. This phase can be simulated by applying a number of modifications to the model that simulated the previous phase. The circuit model shown in the Figure 3-11 is used to simulate the IGBT response during this gate-to-emitter voltage plateau phase.

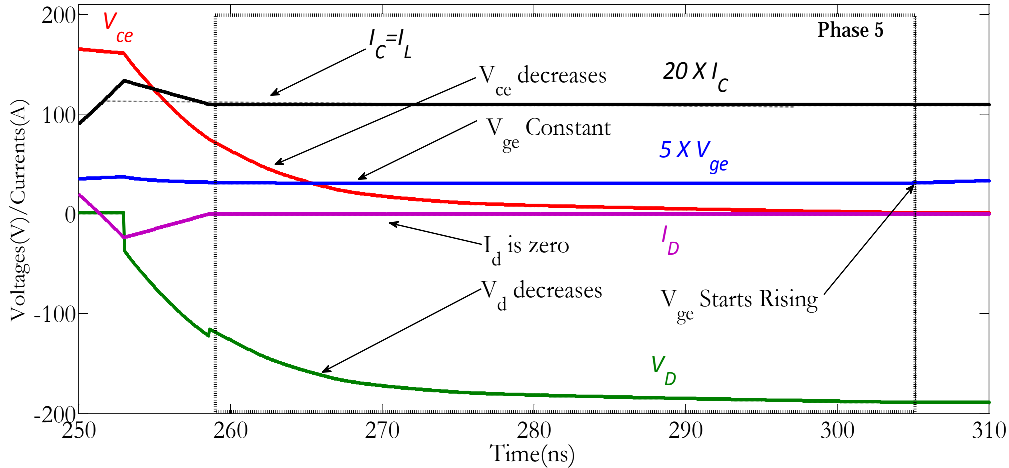


Figure 3-10-Transients at Phase-5

No current flows through the diode at this phase. Current through the variable current source that represented the diode current variation reaches to zero at the beginning of this phase (simulated by opening S_1 and closing S_2). Thus, in phase-5, the collector current is equal to the load current. Therefore, the diode has insignificant effect on circuit behavior. Since the collector current remains constant, there is no voltage drop across the stray inductance. The voltage of the controlled voltage source connected to the gate is required to be fixed at the estimated gate-to-emitter voltage level at the end of the previous phase as depicted in Figure 3-11. Equation 3-7 is used to estimate the collector-to-emitter voltage change as in the previous phase and the controlled source V_{syn} is used to simulate the collector-to-emitter voltage variation in the circuit model. The value of V_{syn} is calculated using Equation 3-7, Equation 3-8, and Equation 3-9 as in Phase-4. However, contribution to

the discharging current given in Equation 3-8 from C_{ge} is zero, as the gate-to-emitter voltage remains constant at a plateau.

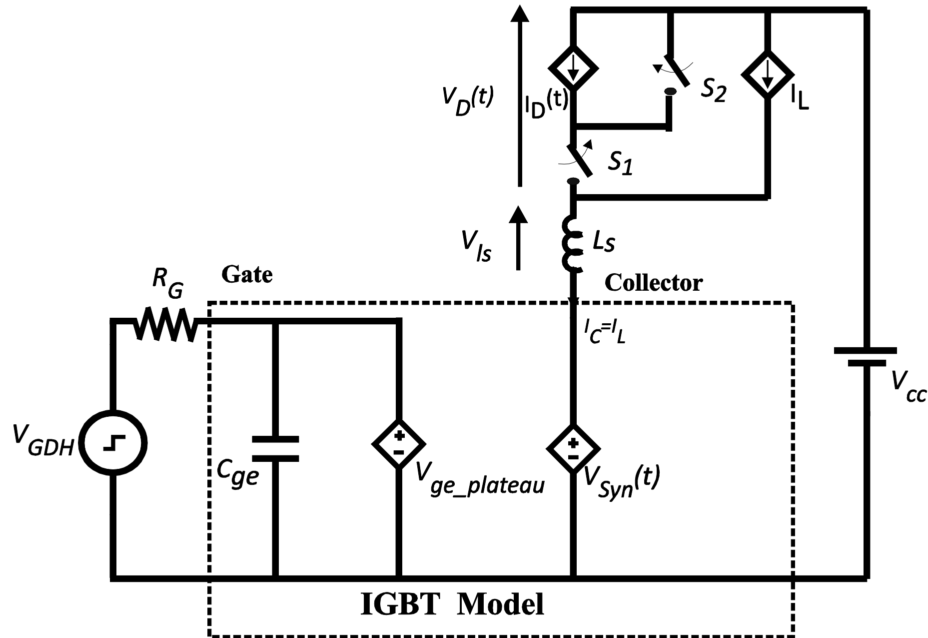


Figure 3-11-Model of the gate-to-emitter voltage plateau phase of turn-on transient

The voltage across the diode during this phase is the difference between the supply voltage and the varying collect-to-emitter voltage. Once the collector-to-emitter voltage drops to the saturation voltage corresponding to the operating condition, the model is switched to simulate the final gate-to-emitter voltage rising phase.

3.2.7 Phase-6: Final Gate-to-Emitter Voltage Rising Phase

As depicted in Figure 3-1 (b), only the gate-to-emitter voltage changes during this phase. Gate-to-emitter voltage starts to increase from the gate-to-emitter voltage plateau and moves towards positive gate drive voltage level V_{GDH}. The rate of increasing gate-to-emitter voltage is determined by C_{ies} (C_{ge} + C_{gc}) as gate drive has to charge both capacitors. For this phase, capacitors can be considered as having fixed capacitance. However,

the value of C_{ies} in this phase is much larger than the fixed capacitance value used in phases 1 and 2 due to low collector-to-emitter voltage (see Figure 3-1(a)). In practical measurements, a small reduction in the collector-to-emitter voltage can be observed. However, this is ignored in the model by considering the impact on the accuracy of the loss estimation.

3.2.8 Diode Turn-off Model

The diode follows a reverse recovery process during the turn-on transient of the IGBT as already explained. The reverse recovery process follows two distinct sub-transients as explained in Section 2.3. Turn-off behavior of a typical power diode is illustrated in Figure 3-12.

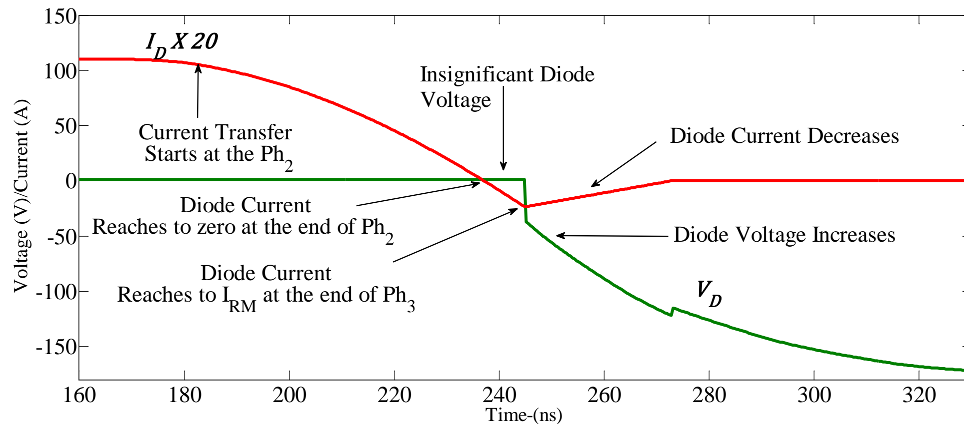


Figure 3-12-Power diode turn-off behavior

The main feature that affects the power losses in the freewheeling diode is the reverse recovery current. The peak reverse recovery current I_{RM} increases with the forward load current it carried before the turn-off. Greater the rate of decreasing of the diode current, smaller the fraction of stored charges depleted via recombination. Therefore, when the rate of decrease of diode current is higher, a large proportion of the stored charges are

depleted as a current through the external circuit. Hence, I_{RM} is increased with the rate of decrease of the diode current during turn-off.

Since the rate of decrease of diode current is usually dictated by the external circuit, the peak reverse recovery current I_{RM} can be approximated by Equation 3-10 [21]:

$$I_{RM} = \sqrt{2\tau I_F \frac{dI_F}{dt}} \qquad 3\text{-}10$$

where τ is the carrier life time, I_F is the pre-switching forward diode current, and dI_F/dt is the rate of decrease of diode current. Manufacture's data sheets contain measured I_{RM} value under a given forward current I_F and cut off rate of current dI_F/dt. Therefore, reverse carrier life time τ can be estimated using the data sheet value of I_{RM} with the measured condition (forward current I_F and cut-off rate dI_F/dt). Once carrier life time of the power diode is determined, I_{RM} corresponding to a switching transient at a given load current is calculated with the help of estimated τ, load current I_L, and slope of current trajectory, which can be estimated during the simulation of Phase-2. In the first phase of reverse recovery where the reverse current is increasing, the diode forward voltage drop remains at the value it had during the forward conducting stage. This phase continues until the collector current reaches the peak reverse recovery current. Note that the peak reverse recovery current is also used as the terminating condition of Phase-3 of the IGBT turn-off process explained in the Section 3.2.4.

The diode reverse voltage gaining phase is simulated as soon as the diode current reaches I_{RM}. The voltage across the diode is negligibly small during the initial reverse recovery as described before. However, the diode reverse voltage suddenly increases to the difference between the supply voltage (V_{cc}) and the collector-to-emitter voltage plateau level at the

end of the initial reverse recovery phase. This is because the time rate change of the reverse recovery current becomes suddenly zero at this point, and therefore, the voltage drop across the stray inductance becomes zero. As voltage across the IGBT capacitances cannot vary suddenly, the difference between the collector-to-emitter voltage and supply voltage V_{cc} appears across the diode. The diode current variation during the later reverse recovery phase is considered independent and therefore, it is an input to the rest of the circuit. Thus the diode is again represented as a current source in the reverse voltage gaining period. The diode reverse current is assumed to fall in a linear fashion during period t_b depicted in Figure 3-12. The linear drop in current is assumed for simplicity, also it closely resembles the practical observations. The parameter t_b can be extracted from data sheets for a given operating condition.

A diode gains the reverse voltage with formation of an immovable space charge region as explained in Section 2.3 [30]. However, it is required to remove charges stored in C_{gc} to enable change in the collector-to-emitter voltage as explained in Section 3.2.5. Therefore, diode voltage is assumed to vary as a response to the collector-to-emitter voltage variation of the IGBT. Estimation of diode voltage is important to estimate the reverse recovery power loss through the freewheeling diode. The effect of the induced voltage across the stray inductance L_s on the diode voltage is taken into account when estimating voltage across the diode. According to the circuit model shown in Figure 3-9, diode voltage variation is evaluated by subtracting the instantaneous collector-to-emitter voltage from the sum of the supply voltage plus the induced voltage across L_s as described in Equation 3-11.

$$V_D(t) = V_{cc} - L_s \frac{dI_c(t)}{dt} - V_{ce}(t) \qquad 3\text{-}11$$

However, diode voltage can overshoot because collector current is decreasing. This simplified model of the diode greatly simplifies the overall model complexity. This diode model is relies on the assumption of the domination of IGBT behavior over the diode during turn-on transient and the validity this assumption will be verified in validation section of the thesis.

3.3 Parameter Extraction

Simulation of significantly important dynamics at each phase leads to a situation where there is a one-to-one relationship between one unknown parameter and a part of the response. Thus the parameters can be evaluated using a measured IGBT turn-on waveform. The IGBT parameters to be determined are (i) gate-to-emitter capacitance C_{ge}, (ii) collector-to-emitter capacitance C_{ce}, (iii) stray inductances L_s, (iv) constant gate-to-collector capacitance (Miller feedback capacitor) C_{gc} at higher collector-to-emitter voltages, (v) a set of capacitance values that represent the variation of C_{gc}', the fictitious C_{gc}' at lower collector-to-emitter voltages after Phase-3, (vi) the nominal gain constant $k_p(1+\beta)$ and (vii) the gain adjusting factor k_{g_Adjust} to estimate gain at lower collector-to-emitter voltages. Furthermore, diode parameters (i) carrier life time τ and (ii) later reverse recovery period t_b need to be estimated. The following section explains parameters that can be estimated during each of the distinct period using measured waveforms.

3.3.1 Parameters from Measurements of Phase-1

Initial gate-to-emitter voltage rise is basically determined by the gate resistance R_G, gate-to-emitter capacitance C_{ge}, and the gate drive characteristics. The gate resistance is the total external resistance between the gate drive and the IGBT plus the internal gate resistance of the IGBT. Ramp up time of a given gate drive can be measured with the help of an oscilloscope. Although C_{gc} is included in the model circuit, C_{gc} has insignificant effect on gate-to-emitter voltage in this phase since C_{ge} is much larger than C_{gc} (often C_{ge} is more than twenty times larger than C_{gc} at this phase). Therefore, C_{ies} is approximated to C_{ge} during this phase for parameter extraction purpose. Considering the charging of C_{ge} from a constant gate drive voltage V_{GDH} through R_G during a time interval from t_i to t_f (t_i is an instant after the ramp up time of the gate drive), Equation 3-12 is obtained by applying the charging equation for an instant t_f where the voltage across the capacitor is.

$$V_{ge_f} = V_{GDH}\left(1 - e^{-(t_f - t_i)/R_G C_{ge}}\right) + V_{ge_i}\left(e^{-(t_f - t_i)/R_G C_{ge}}\right) \qquad 3\text{-}12$$

where V_{ge_i} is the gate-to-emitter voltage at t_i and V_{ge_f} is the gate-to-emitter voltage at t_f. Then the value of C_{ge} can be found using Equation 3-13 which is derived by rearranging Equation 3-12.

$$C_{ge} = \left(\frac{t_f - t_i}{R_G}\right) \times \frac{1}{\ln\left[\frac{(V_{GDH} - V_{ge_i})}{(V_{GDH} - V_{ge_f})}\right]} \qquad 3\text{-}13$$

The gate-to-emitter voltage measurements are usually more impacted by the noise due to relatively low voltage level. The gate-to-emitter voltage is also subjected to transient oscillations due to dynamics ignored in this model, for example those due to inductance of

the gate drive circuit. The following considerations can be used to enhance the accuracy of the C_{ge} estimation when gate-to-emitter voltage measurements are noisy. The first measurement V_{ge_i} should be taken after the decaying the oscillation of V_{ge} that occurs immediately after the gate pulse is applied. This fluctuation of V_{ge} occurs [see Figure 3-1 (a)] due to oscillation of energy between the stray inductance of connecting wires of the gate drive and the capacitor C_{ge}. The second measurement of V_{ge_f} should be taken before the oscillation of the gate-to-emitter voltage that appears just before the instant of starting the conduction of the IGBT, i.e before V_{ge} exceeds the threshold voltage. If the gate-to-emitter voltage measurement is severely impaired by noise, a comparison of V_{ge} measurements and assessed response of V_{ge} with an initial estimation of C_{ge} can be used to refine the estimation. Extracted C_{ge} in Phase-2 can be used to simulate next phase as well.

3.3.2 Parameters from Measurements of Phase-2

Accuracy of the collector-to-emitter capacitance C_{ce} does not significantly influence the accuracy of the estimated response as I_c is much larger than $C_{ce}\frac{dV_{ce}}{dt}$. The collector-to-emitter capacitance C_{ce} is normally ignored in simulating switching transients [40]. The impact of C_{ce} is only accounted during Phase-2 and Phase-3 of the turn-on transient model. Therefore, it is suggested to use the data sheet value of C_{ce} in the simulation. The gate-to-emitter voltage threshold value V_T is the gate-to-emitter voltage at which the collector current I_c starts to flow. Therefore, V_T can be directly estimated from a concurrent measurement of I_c and V_{ge} during a turn-on transient.

Equation 3-14 can be used to estimate the adjusted gain constant for Phase-2 and -3. It is derived from Equation 3-1 that describes the transfer characteristic of the IGBT.

$$K_{g_adjust} k_p (1+\beta) = \frac{I_{cm}}{\left(V_{gem} - V_T\right)^2} \qquad 3\text{-}14$$

where I_{cm} and V_{gem} are respectively a collector current measurement and a gate-to-emitter voltage measurement taken during Phase-2 when the collector-to-emitter voltage variation is minimum. According to the model circuit shown in Figure 3-5, this equation is more accurate when current through C_{ce} is minimum or $\frac{dV_{ce}}{dt}$ is minimum. It is observed that often the rate of change of I_c is constant around I_L. Therefore, V_{ce} is more or less constant when I_c is close to I_L. Furthermore, it is found that measured gate-to-emitter voltage is more stable at around I_L. Therefore, I_{cm} can be fixed to I_L and then V_{gem} should be the gate-to-emitter voltage when $I_{cm} = I_L$.

The induced emf across the stray inductance is solely determined by the slope of the collector current trajectory. Therefore, stray inductance L_s can be estimated from Equation 3-15.

$$L_s = \frac{V_{L_s}}{{dI_c}/{dt}} = \frac{(V_{cc} - V_{cem})}{\left[{dI_c}/{dt}\right]_{t=tm}} \qquad 3\text{-}15$$

where V_{cem} is the collector to emitter voltage at an instant $t=t_m$ and denominator of Equation 3-15 denotes the estimated slope of the collector current I_c when $t=t_m$. Taking accurate measurements of V_{ce} and I_c is not challenging when compared with the gate–to-emitter voltage measurement. However, it is suggested to avoid measurements at the be-

ginning of Phase-2 as there are fluctuations in V_{ce} and I_c . Reliable estimations of L_s can be obtained by considering measurements of I_c that lies between $I_L/2$ and I_L.

According to the model circuit depicted in Figure 3-5, current through the Miller capacitance C_{gc} is given by Equation 3-16 .

$$C_{gc}\frac{dV_{cg}}{dt}=\left(\frac{V_{GDH}-V_{ge}}{R_G}\right)-C_{ge}\frac{dV_{ge}}{dt} \quad 3\text{-}16$$

where V_{GDH} is the gate drive voltage and V_{cg} is the collector-to-gate voltage. Therefore, Miller capacitance C_{gc} can be estimated using Equation 3-17.

$$C_{gc}=\frac{\left[\frac{(V_{GDH}-V_{ge})}{R_G}-C_{ge}\frac{dV_{ge}}{dt}\right]}{\left[\frac{dV_{ce}}{dt}-\frac{dV_{ge}}{dt}\right]} \quad 3\text{-}17$$

The first term in the numerator is the current drawn from the gate drive and can be easily estimated with the help of a gate-to-emitter voltage measurement taken during Phase-2 or -3. The second term in the numerator stands for the current through C_{ge}. Accurate estimation of the slope of the gate-to-emitter voltage is required for estimation of the current through C_{ge} as well as to evaluate the numerator of Equation 3-17. If the gate-to-emitter voltage measurement is noisy, the initial estimation of C_{gc} can be refined by comparing the measured responses and the assessed response.

3.3.3 Parameters from Measurements of Phase-3

The model of the IGBT remains the same as the previous phase during this phase. A single new parameter required to simulate this phase is the carrier life τ. Carrier life τ can be estimated with help of Equation 3-18.

$$\tau = \frac{I_{RM}^2}{\left(2I_F \, {}^{dI_F}/_{dt}\right)} \quad 3\text{-}18$$

where I_F is the forward current through the diode and ${}^{dI_F}/_{dt}$ is the cut-off rate of the diode current. Carrier life time can be estimated with the help of measurements or even using manufactures data sheet information as data sheet information are not as inaccurate as the IGBT switching capacitances given in the data sheets.

3.3.4 Parameters from Measurements of Phase-4

Parameters required to simulate this phase are later reverse recovery period t_b, gain adjusting factor, and some values of C_{gc}' at number of collector-to-emitter voltages. An accurate estimation of t_b cannot be done without simulating diode model based on underline physics. However, a certain degree of simplification can be done using information given in the manufactures data sheets. Data sheets contain plots showing the variation of t_b and/or total reverse recovery time with different forward currents at different the cut-off rates. When merely the total reverse recovery time is specified in the data sheet, t_b can be calculated by subtracting the estimated initial reverse recovery period from the total reverse recovery period. The initial reverse recovery period can be estimated via simulation. Furthermore, t_b can be estimated using softness factor S which is defined as the ratio of the between later reverse recovery period and the initial recovery period. With a known softness factor S, t_b is can be determined using Equation 3-19

$$t_b = \frac{S t_{rr}}{S+1} \quad 3\text{-}19$$

where t_{rr} is the total reverse recovery time. This approach assumes the softness factor does not vary with the load current and cut-off rate of the diode current.

The gain adjusting factor k_{g_Adjust} can be determined as described below. Nominal gain of the IGBT can be estimated by applying Equation 2-6 for gate voltage plateau period (Phase-5). Equation 3-20 is obtained by applying Equation 2-6 to the gate voltage plateau phase and rearranging the terms.

$$k_p(1+\beta) = \frac{I_{cm}}{\left(V_{ge_Plateau} - V_T\right)^2} \qquad 3\text{-}20$$

K_{g_Adjust} is the ratio between the gain estimated from Equation 3-14 and the gain estimated from Equation 3-20

According to the described behavior of the model, the collector-to-emitter voltage is solely determined by the discharging current estimated from Equation 3-8 and the profile of fictitious capacitance C_{gc}'. If the collector-to-emitter voltage variation estimated from Equation 3-7 is approximated to the variation of collector-to-emitter voltage C_{gc}' should be able to estimate from Equation 3-21.

$$\left[C_{gc}'\right]_{V_{ce_mid}} = -\left[I_{Discharge}\right]_{V_{ce_mid}} \frac{(t_H - t_L)}{\left(V_{ce_H} - V_{ce_L}\right)} \qquad 3\text{-}21$$

where $I_{Discharge}$ is the discharging current estimated with help of Equation 3-8, V_{ce_H} is a collector-to-emitter voltage measurement taken at $t=t_H$ and V_{ce_L} is a collector-to-emitter voltage measurement taken at $t=t_L$. Also, $V_{ce_H} > V_{ce_L}$ and therefore $t_L > t_H$. The estimated value of C_{gc}' is corresponds to the average value of the collector-to-emitter voltage (V_{ce_mid}) of the above two collector-to-emitter voltage measurements because Equation 3-21 is applied around this operating point. However, accurate variation of the

gate-to-emitter voltage variation is required to estimate $I_{Discharge}$. Equation 3-8 describes two components of currents that discharge C_{gc}'. The discharging current component due to the release of the stored charges from C_{ge} has to be estimated with the help of the time rate of measured gate-to-emitter voltage variation during this phase. A very small variation of gate-to-emitter voltage results in a significantly large current from C_{ge} as shown subsequently.

According to Figure 3-1, huge oscillations of gate-to-emitter voltage appears during this phase. Therefore, it is almost impossible to use Equation 3-21 to estimate C_{gc}' with practical measurements on gate-to-emitter voltage. This is one reason why Equation 3-21 cannot be used to estimate C_{gc}'. Furthermore, as mentioned in Section 3.2.5, estimated gate-to-emitter voltage during this phase is not accurate as gain adjustment (which is done with a constant factor) is only performed to fix the gate-to-emitter voltage at the end of this phase in the measured gate-to-emitter voltage level. Impact of inaccurate estimation of collector-to-emitter voltage variation due to inaccurate estimation of gate-to-emitter voltage variation can be evaluated as follows. If the whole current supplied by discharging C_{ge} flows through C_{gc}', corresponding voltage variations are given by the following the equation.

$$C_{gc}'\frac{dV_{gc}}{dt} = C_{ge}\frac{dV_{ge}}{dt}$$

The error in estimating collector-to-gate voltage when there is ΔV_{ge} error in estimating gate-to-emitter voltage can be found from the following expression.

$$\Delta V_{gc} = \frac{C_{ge}}{C_{gc}'}\Delta V_{ge}$$

Typical values of C_{gc}' is in the few tens of pico-Farads. Typical values of C_{ge} are in the few hundreds pico-Farads to few nano-Farads. Therefore, a one tenth of a volt error in estimating gate-to-emitter voltage can probably causes tens of volts of error in estimating collector-to-gate voltage. Due to above two reasons, the following trial and error approach is suggested to estimate C_{gc}'. The suggested approach seeks an appropriate value of C_{gc}' that synthesizes collector-to-emitter voltage at the estimated gate-to-emitter voltage transient by the model rather than measurement. Therefore, actual capacitance at actual gate-to-emitter voltage might be different. A comparison of measured collector-to-emitter voltage transient and estimated value of collector-to-emitter voltage (done with a trial value of C_{gc}') is used to refine initial estimation of C_{gc}'. It is enough to estimate capacitance at few collector-to-emitter voltage values. The capacitance values in between those points can be estimated with interpolation during simulation. During the parameter extraction, a new capacitance value at a new collector-to-emitter voltage is estimated when the estimated collector-to-emitter voltage with the help of the previously determined C_{gc}' significantly deviates from the measured collector-to-emitter voltage. Figure 3-13 shows collector-to-emitter voltage transient measurement of IGBT-IRGP4072DPBF and estimations of collector-to-emitter voltages done with calculated values of C_{gc}'.

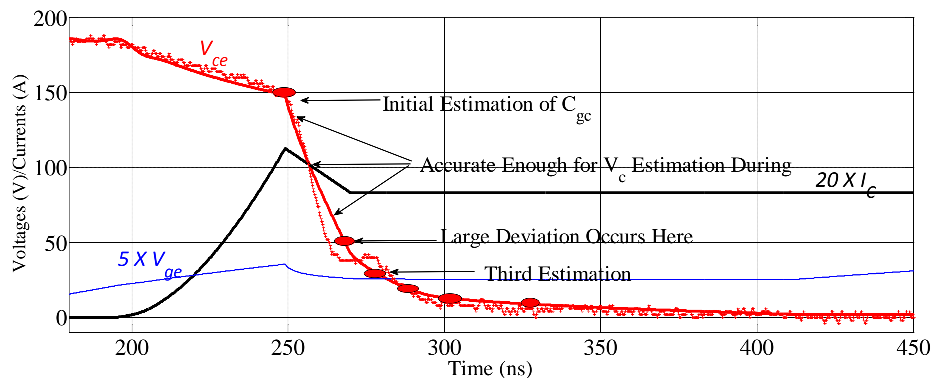


Figure 3-13- C_{gc}' estimation by trial and error

It is found that the estimated collector-to-emitter voltage deviates from the measured collector-to-emitter voltage at around 50V unless C_{gc}' is increased as shown in Figure 3-13. Via trial and error, 60 pF is found to be a good estimation C_{gc}' at a collector-to-emitter voltage of 50V. The model is again simulated by creating another entry for the nonlinear capacitor model at a collector-to-emitter voltage of 50V and the response is again compared with the measurement. The next significantly deviating point is identified as 25V which is marked in the Figure 3-13. Phase-4 ends at this instant of time as depicted in Figure 3-13. Hereafter $I_{Discharge}$ comprises of a single current component which flows from the gate drive. Therefore, Equation 3-21 can be applied. Seven values for C_{gc}' are estimated from trial and error approach to represent collector-to-emitter voltage falling transient of IGBT-IRGP4072DPBF is shown in Table 3-1. Each raw of Table 3-1 represent collector-to-emitter voltage and estimated value of C_{gc}' at the given collector-to-emitter voltage.

Table 3-1-Miller capacitance extraction

Collector-to-emitter Voltage(V)	Capacitance C_{gc}'(pF)
400	25
150	40
50	60
25	120
15	400
10	1200
2	2500

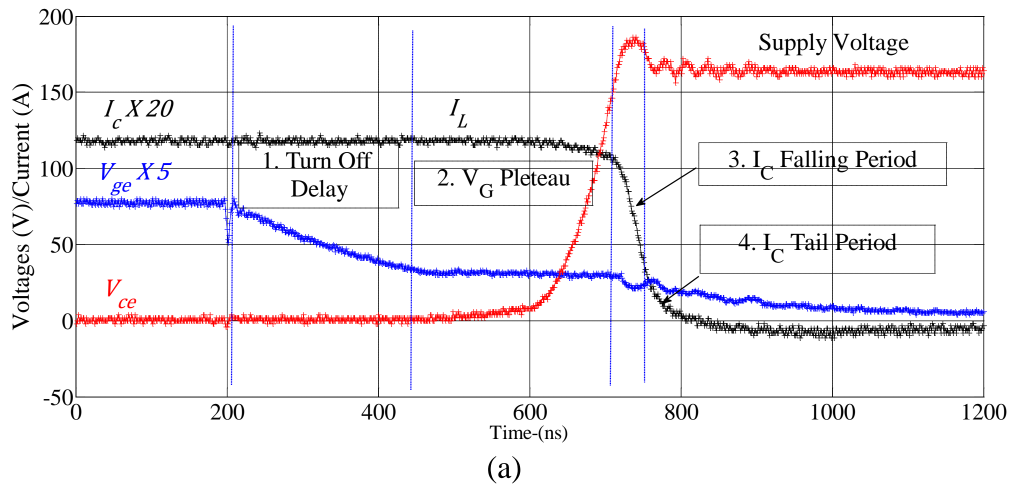
Chapter 4

Turn-off Transient Model

In this chapter, turn-off switching behavior of the unit cell is first described. Design of the model circuit that mimics each phase in the turn-off process is explained. Finally, a comparison is made between the estimated parameters of the turn-off transient model and those extracted for the turn-on transient model.

4.1 Turn-off Behavior and Approximations

Measured switching trajectories of the turn-off switching transient are illustrated in Figure 4-1 (a). The turn-off transient is measured using a digital storage oscilloscope with help of the test setup described in Section 5.1. The turn-off transient is divided in to four distinct phases. Figure 4-1 (b) depicts approximated switching behavior that is to be modeled.



(a)

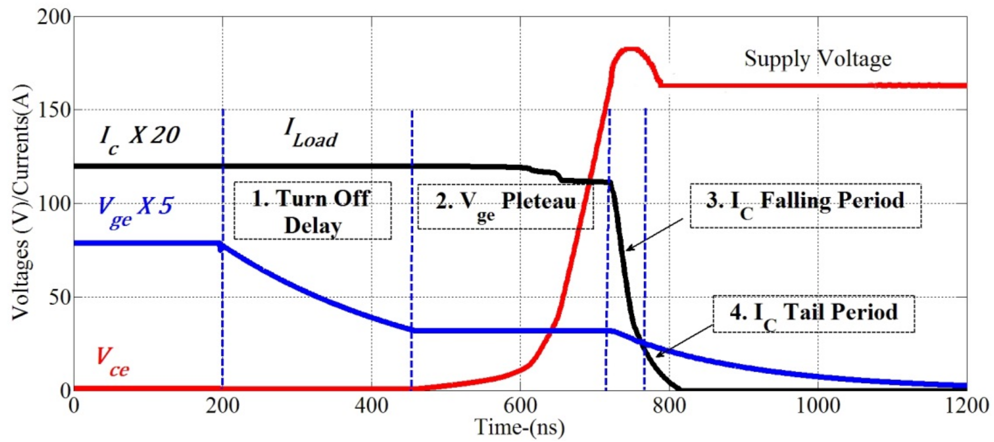


Figure 4-1-(a) Measured and (b) Approximated turn-off behavior

Sections 4.1.1 through 4.1.4 describe the important dynamics during each of these four phases.

4.1.1 Phase-1: Turn-off Delay Period

Once the gate drive voltage changes from its ‘high’ value to ‘low’ value, the gate-to-emitter voltage starts to decrease. However, both the collector current and collector-to-emitter voltage remain more or less unchanged. At the end of this period, the gate-to-emitter voltage enters into a plateau as depicted in Figure 4-1(a) . The gate-to-emitter voltage plateau level is the minimum gate-to-emitter voltage required to maintain the load

current with the nominal gain of the IGBT, when collector–to-emitter voltage is at its saturation level.

4.1.2 Phase-2: Gate-to-Emitter Voltage Plateau Period

Similar to the gate-to-emitter voltage plateau observed in the turn-on transient, the gate-to-emitter voltage remains at a more or less constant value after the initial decrease of gate-to-emitter voltage. During this phase, collector-to-emitter voltage starts to increase. The rate of rise of the collector-to-emitter voltage continually increases as seen in Figure 4-1(a). No apparent collector current variation takes place during this phase. However, a slight decrease in collector current is observed at higher collector-to-emitter voltages, and when the rate of rise of collector-to-emitter voltage is high.

4.1.3 Phase-3: Collector Current Falling Period

Once the collector-to-emitter voltage reaches the supply voltage V_{cc}, the load current transfer from the IGBT to the freewheeling diode begins. The collector current starts to decrease rapidly and the collector-to-emitter voltage overshoots beyond the supply voltage as can be seen in the Figure 4-1(a). Simultaneously the gate-to-emitter voltage decreases as the collector current and the gate-to-emitter voltage are related through the gain equation of the IGBT. A sudden change in the rate of change of the collector current results in an oscillation of the collector-to-emitter voltage at the end of this phase. Simultaneous oscillation is visible in the gate-to-emitter voltage.

4.1.4 Phase-4: Collector Current Tail and Final Gate-to-Emitter Voltage Fall

The rate of decreasing of the collector current suddenly drops at a certain current level and the collector current enters into a regime of gradual fall. This collector current trajectory is termed as the collector current tail in literature. In addition, the gate-to-emitter voltage decays at a lower rate in this phase than the previous phase.

A kind of duality can be observed between turn-on transients and turn-off switching transient of the unit cell. Obviously, after applying the gate pulse, both transients are followed by a delay period before variations in the collector side are started. Whereas turn-off transients initiate after a turn-off delay period that follows a phase of the gate-to-emitter voltage decrease and turn-on transients happen after an initial increase of the gate-to-emitter voltage. During turn-on, first the collector current increases and then the collector-to-emitter voltage starts to decrease. The reason behind this sequence is the freewheeling diode starts to turn-off only after load current is totally transferred to the IGBT. Therefore, voltage across the IGBT does not begin to fall until the freewheeling diode turns-off. In contrast, the collector-to-emitter voltage increases before decreasing the collector current during the turn-off transient. This is because the freewheeling diode does not begin to conduct until it gains a sufficient voltage in correct polarity to forward bias the junction. Once the collector-to-emitter voltage reaches the supply voltage, the freewheeling diode becomes forward biased and starts taking over the load current from the IGBT.

4.2 Behavioral Model of Turn-off Transient

Once the dominant dynamics in each phase are identified, a circuit model is developed for each phase including relevant components of the IGBT switching model shown in the Figure 3-2. Interactions of the IGBT with the rest of the circuit are modeled with some additional circuit components. The effect of the collector-emitter capacitance C_{ce} is assumed to be insignificant during the early phases as described in [21], [40]. In addition, dynamics of the diode is found to be merely a response to the behavior of the IGBT, except for a small contribution to the load current when the collector-to-emitter voltage variation of the IGBT is very rapid. Sections 4.2.1 through 4.2.5 detail the approach of modeling the selected dynamics.

4.2.1 Pre-Switching Condition

The IGBT gate-to-emitter voltage is maintained at the high value of the gate drive V_{GDH}, and the collector-to-emitter voltage is at the saturation level. The saturation voltage is dependent on the gate drive voltage, collector current, and temperature. Therefore, capacitor C_{ge} is charged to the positive gate drive voltage prior to the simulation. Voltage across the Miller capacitance C_{gc} is set to the difference between the gate drive voltage and the collector-to-emitter saturation voltage.

4.2.2 Phase-1: Turn-off Delay

The major occurrence during this phase is the decay of the gate-to-emitter voltage due to change of the gate drive voltage to zero. The load current flows through the collector

terminal of the IGBT. The freewheeling diode is still reverse biased. The collector current will not start to change until the gate-to-emitter voltage drops to a certain threshold voltage. The variation in collector-to-emitter voltage is also assumed to be negligible as per the observations. The circuit model for this period is shown in Figure 4-2.

Decrease of the gate-to-emitter voltage requires removal of stored charges in the gate-emitter capacitance C_{ge}. Since the collector is at a lower voltage than the gate-to-emitter voltage, decreasing gate-to-emitter voltage also requires discharge of the Miller capacitor C_{gc} as well. Therefore, in the circuit model, this phase can be represented as discharging of capacitances C_{ge} and C_{gc} via the effective gate resistance R_G as depicted in Figure 4-2.

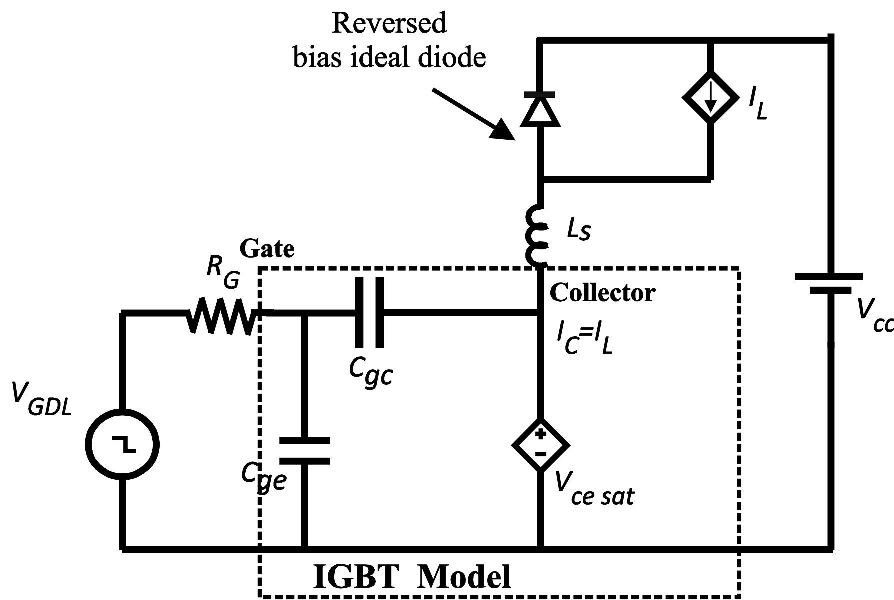


Figure 4-2-Turn-off delay model

Ramp down time of the gate drive and finite output resistance of the gate drive can be included to enhance the accuracy especially at small gate resistances. Once the gate-to-emitter voltage reaches the estimated gate-to-emitter voltage plateau level, the circuit model of the next phase is simulated.

4.2.3 Phase-2: Gate-to-Emitter Voltage Plateau

As explained in Section 4.1.2, the collector-to-emitter voltage rises during this phase while the gate-to-emitter voltage remains at a constant level. This gate-to-emitter voltage level is called gate-to-emitter voltage plateau. However, the collector current does not decrease as the freewheeling diode is still forward biased. The model circuit used to simulate this phase is shown in Figure 4-3.

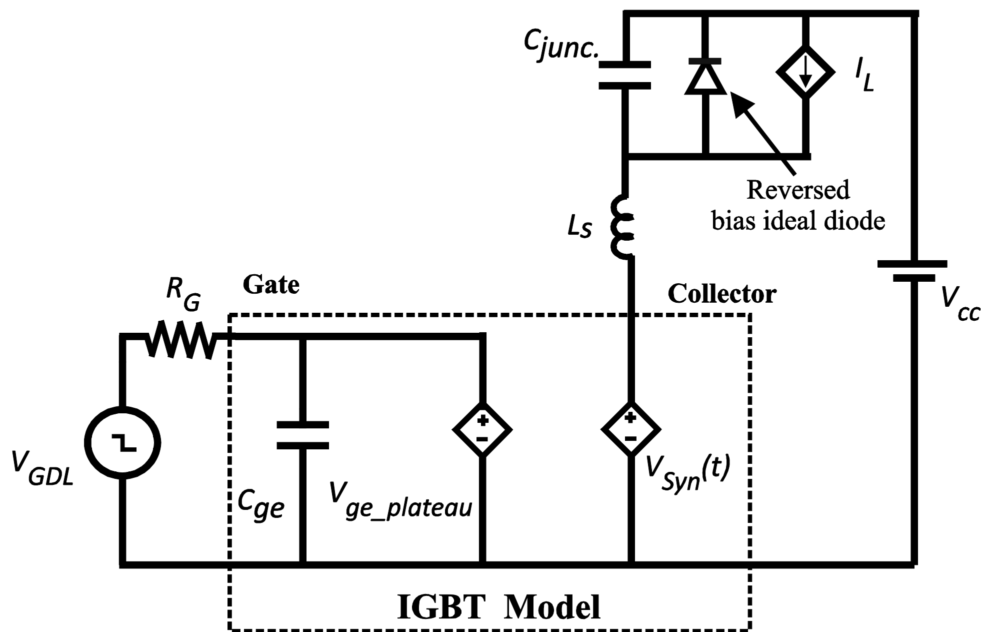


Figure 4-3-Model of the gate-to-emitter voltage plateau during turn-off

The gate-to-emitter voltage plateau $V_{ge_Plateau}$ is estimated applying Equation 3-3 when the collector current equals the load current. Equation 4-1 is obtained by applying Equation 3-3 for gate-to-emitter voltage estimation.

$$V_{ge_Plateau} = V_T + \sqrt{\left({I_L}/{k_p(1+\beta)} \right)} \qquad 4\text{-}1$$

A constant voltage source is positioned at the gate side of the model circuit shown in Figure 4-3 to mimic this gate-to-emitter voltage behavior. The voltage across the gate re-

sistance is fixed at ($V_{ge_Plateau} - V_{GDL}$) and therefore a constant current flows through the gate resistance. The direction of this current flow is from the gate pin of the IGBT to the gate drive as the gate drive voltage is less than the gate-to-emitter voltage plateau.

Since the gate-to-emitter voltage remains constant, the charge level in C_{ge} does not change during this phase. Thus, this constant current removes the stored positive charge from the gate side of Miller capacitance C_{gc}. Removal of positive charges from the gate side of C_{gc} increases the voltage at the collector side of C_{gc} with respect to the gate side. This charge removal process continues until the collector-to-emitter voltage becomes equal to the supply voltage. The collector-to-emitter voltage varies at the same rate as collector-to-gate voltage because the gate-to-emitter voltage is fixed. Shape of the collector-to-emitter voltage trajectory should be solely dependent on the profile of the fictitious Miller capacitance C_{gc}' as in the case of the gate-to-emitter voltage plateau phase of the turn-on transient. The collector-to-emitter voltage variation is synthesized in the same way as Phase-5 of the turn-on transient. The source V_{Syn} shown in the Figure 4-3 represents a dependent source that simulates the collector-to-emitter voltage variation. The collector-to-emitter voltage at a given time step V_{syn} is updated at each time step with estimated value of collector-to gate voltage change ΔV_{gc} as depicted in Equation 4-2.

$$V_{syn}(t + \Delta T_s) = V_{syn}(t) - \Delta V_{gc}(t) \qquad 4\text{-}2$$

Equation 4-3 is used to estimate the collector-to-gate voltage variation during a time step.

$$\Delta V_{gc} \approx \frac{I_{Charge}\Delta T_s}{C_{gc}'(V_{gc})} \qquad 4\text{-}3$$

Variation of the collector-to-emitter voltage during a small time step is estimated by approximating collector-to-emitter voltage variation to the estimated collector-to-gate volt-

age variation. The gate-to-emitter voltage V_{ge} remains constant at a plateau during this phase. Therefore, the charging current is estimated using Equation 4-4:

$$I_{Charge} = \frac{(V_{GDL} - V_{ge_Plateau})}{R_G} \qquad 4\text{-}4$$

where V_{GDL} is the negative output level of the gate voltage drive that is used to turn-off the IGBT. Note that the actual value of I_{Charge} is negative in this phase. The collector current slightly decreases when the collector-to-emitter voltage starts to rise towards the supply voltage V_{cc}. Rising collector-to-emitter voltage reduces the reverse voltage across the freewheeling diode, and a small portion of the load current is diverted for depletion of the stored charges in the reverse biased junction capacitance of the freewheeling diode. This diode junction capacitance is voltage dependent and Equation 4-5 [41],[42] is often used to model it.

$$C_j(V_j) = \frac{C_{j0}}{\left(1 - {V_j}/{V_b}\right)^m} \qquad 4\text{-}5$$

where C_{j0} is the zero voltage junction capacitance, V_j is the junction voltage, and V_b is the barrier voltage. The exponent m is called the gradient factor and lies between 0.33 and 0.5[41]. However, fairly accurate estimations can be done with a constant capacitance as in [21], and therefore, the average diode capacitance is used to retain the simplicity of the overall model. Due to two reasons, the rate of change of collector current is high when the collector-to-emitter voltage is approaching the supply voltage: firstly, the rate of change of collector-to-emitter voltage is large at this voltage due to low C_{gc}, and secondly, the diode capacitance is large at low reverse voltages and therefore, a relatively larger

portion of load current is diverted to deplete the stored charges in the reverse biased junction capacitance.

4.2.4 Phase-3: Collector Current Falling Period

Once the collector-to-emitter voltage reaches the supply voltage, the freewheeling diode becomes forward biased and starts conducting, and therefore at this point, the circuit model for Phase-3 needs to be introduced. Figure 4-4 shows the circuit model of Phase-3.

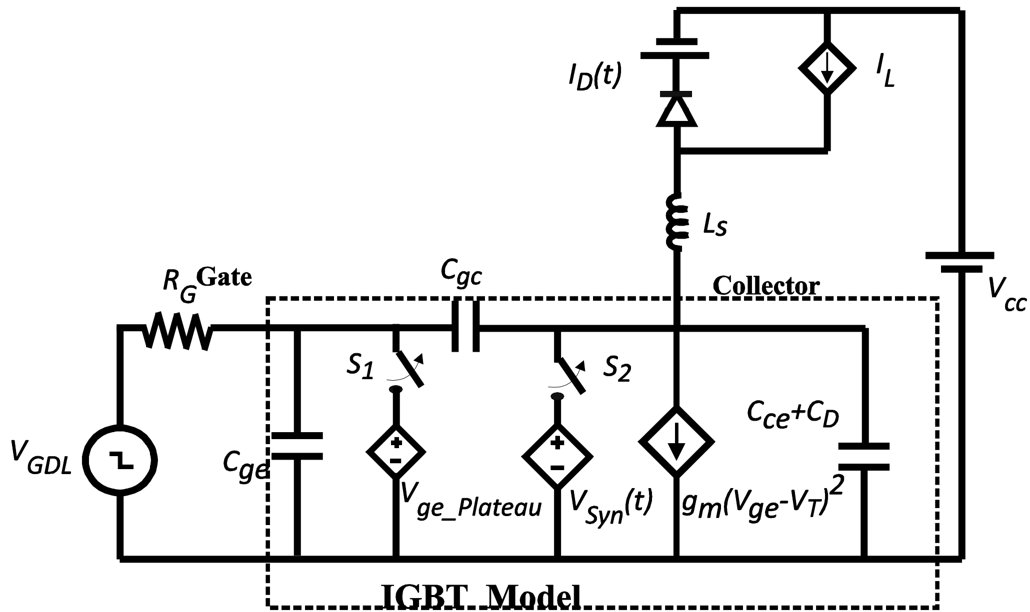


Figure 4-4-Model circuit of I_C falling

Once the freewheeling diode is forward biased, the load current can transfer to the freewheeling diode allowing the collector current to change. Since the collector current is now allowed to change, the gate-to-emitter voltage which was held at a plateau due to coupling with the constant collector current in the previous phase, also becomes free to change. Thus the controlled source $V_{ge_Plateau}$ is removed by opening switch S_1. Now, the collector current decreases simultaneously with the gate-to-emitter voltage and the diode current increases at the rate of decreasing collector current. The rate at which the gate-to-

emitter voltage falls is governed by the discharging rate of the gate-to-emitter capacitance C_{ge} through R_G. Since the lowering gate-to-emitter voltage also requires supplying some negative charge to the gate side of the Miller capacitance C_{gc}, the combined effect can be represented as discharging of both C_{ge} and C_{gc}. The value of C_{gc} used in Phase-2 and 3 of the turn-on model is used in this phase as the collector-to-emitter voltage is high. Coupling between the gate-to-emitter voltage and collector current is still governed by the Equation 2-6 which is re-written as Equation 4-6.

$$I_C(t) = k_p(1+\beta)\big(V_{ge}(t) - V_T\big)^2 \qquad 4\text{-}6$$

The proportional constant $k_p(1+\beta)$ is the nominal gain of the IGBT. The voltage controlled current source shown in Figure 4-4 models the collector current during this phase. The controlled source V_{syn} is disconnected by opening switch S_2, allowing V_{ce} to be freely determined by the other circuit constraints. The collector-to-emitter voltage overshoots beyond the supply voltage due to induced voltage on the stray inductance during rapid fall of the collector current. Measured waveforms show some oscillations on both collector-to-emitter and gate-to-emitter voltages at the end of this phase, which is visible in the Figure 4-1(a). Ringing of the collector-to-emitter voltage occurs due to oscillation of energy between the stray inductance and the collector-emitter capacitance C_{ce} plus the diffusion capacitance C_D of the diode. The effect of two capacitances is simulated with a single capacitor connected between the collector and emitter terminals as shown in Figure 4-4.

4.2.5 Phase-4: Collector Current Tail Period

In this phase, the gate-to-emitter voltage continuously drops due to discharging of C_{ies} (C_{ge} + C_{gc}). The constant capacitance estimated for Phase-2 and Phase-3 of the turn-on

model is used for C_{gc}. However, C_{ge} is different from other phases. The reason behind the difference of the capacitance value of C_{ge} is explained in Section 4.3. The circuit model for this phase is shown in Figure 4-5.

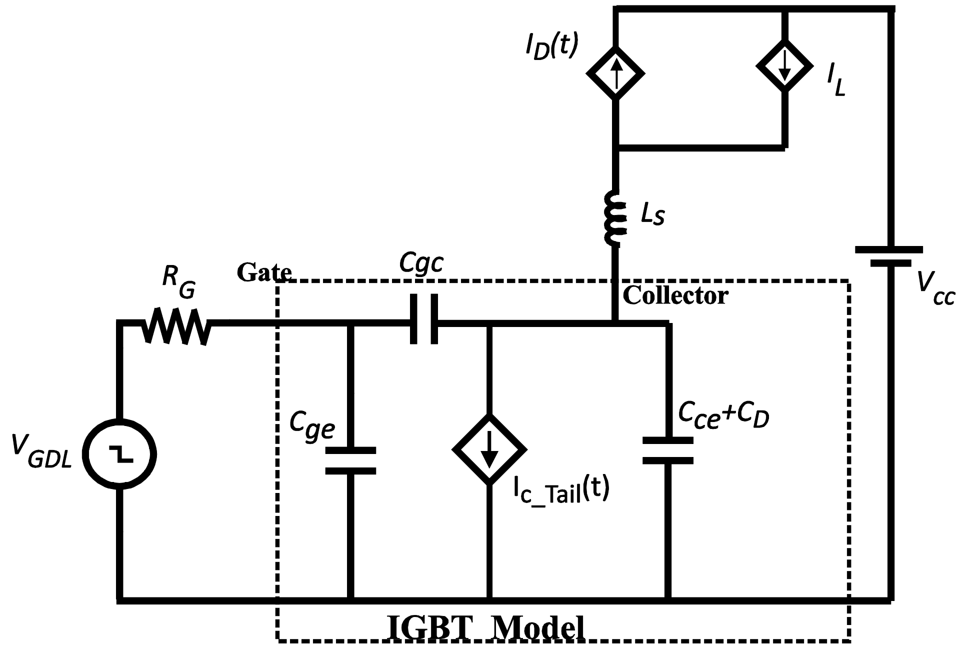


Figure 4-5-Model circuit of the collector current tail phase

The slow collector current fall visible in this phase is often approximated as an exponential decay [43], [44]. The controlled current source used to represent the collector current variation during the previous phase is replaced with an exponentially decaying current source specified in Equation 4-7 [44].

$$I_{C_Tail}(t) = I_{Tail}\, e^{-t/\tau_{Tail}} \qquad 4\text{-}7$$

where I_{Tail} is the amplitude of the collector current tail obtained from measurements and τ_{Tail} is the measured time constant from measurement. Loss estimation is stopped when collector current approximately reaches to the zero.

4.3 Parameters of the Turn-off Model and Their Correlation with Turn-on Model Parameters

Simulation models proposed by many authors use the same set of capacitance in turn-on and turn-off transient models [21], [39], [45]. It is found that estimated MOS capacitances from the turn-off transient measurements are different from the estimated capacitance values for turn-on transient. This difference in the capacitance values can be justified by considering the differences in the collector-to-emitter and gate-to-emitter voltage levels in the two transients. As explained in Chapter 2, these capacitances are voltage dependent and nonlinear; data sheets usually show the collector-to-emitter voltage dependency of Miller capacitance (C_{gc}), output capacitance (C_{gc} + C_{ce}), and input capacitance (C_{gc} + C_{ge}). Those measurements are taken at zero gate-to-emitter voltage V_{ge}. However, these capacitances are also significantly dependent on the gate-to-emitter voltage as described in [46].

Two capacitance values have been used for C_{ge} as well as for C_{gc} in [47]. One set of the capacitances is used when the gate-to-emitter voltage is higher than a certain threshold level; otherwise the second set of values is used. In [38], four different values of capacitances are assigned for C_{ge} in different phases of the turn-on and turn-off transients. These references confirm the dependency of IGBT capacitances on the gate-to-emitter voltage, and the need for taking into account such variation in modeling to retain a sufficient level of accuracy. On the other hand, changes of the supply voltage (V_{cc}) do not significantly change the MOS capacitances because the collector-to-emitter voltage dependency of the MOS capacitances becomes weak at the higher collector-to-emitter voltage as depicted in

Figure 2-16. Although the MOS capacitances are dependent on the gate-to-emitter voltage, and the collector current is related to the gate-to-emitter voltage when operating in the active region, only a very small variation of gate-to-emitter voltage is required for a large change in the collector current. Therefore, changes of the load current do not significantly affect the MOS capacitances. This is because the collector current is proportional to the square of the difference between the gate-to-emitter voltage and the threshold voltage as given in Equation 3-1. This can be explained using the measured turn-on waveform shown in Figure 4-6.

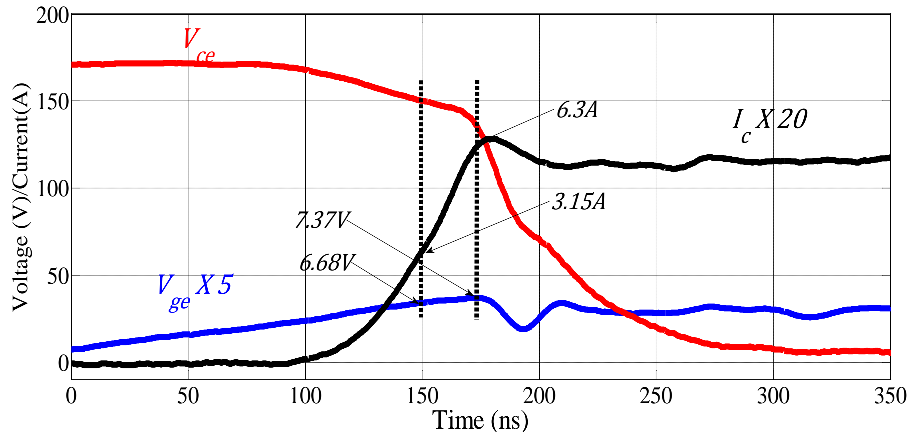


Figure 4-6-Gate-to-emitter voltage and collector current

Note that the maximum collector current is directly related to the load current. According to Figure 4-6, the gate-to-emitter voltage level when the collector current reaches 3.15 A is 6.78V. When the collector current is doubled to 6.3 A, the gate-to-emitter voltage increases only to 7.37 V as shown in the Figure 4-6. The above numerical figures show that in order to increase the collector current by 100%, only 8.7% increase of gate-to-emitter voltage is required. This indicates that the final collector current has only a very limited impact on the gate-to-emitter voltage, and therefore the effect of load current on the MOS capacitances is negligible. Therefore, a constant capacitance can be used to represent C_{ge}

during the entire period from Phase-1 to Phase-3 of the IGBT turn-on transient without scarifying the accuracy. On the other hand, in the turn-off transient, the initial decrease of the gate-to-emitter voltage (during Phase-1) takes place at a very low collector-to-emitter voltage (saturation voltage). Although a constant capacitance can be used to represent C_{ge} in this period as well, its value has to be different from the value used to represent C_{ge} in the initial period of turn-on transient due to the difference of the collector-to-emitter voltage.

In addition to the dependency of the IGBT capacitances with voltages (V_{ce} and V_{ge}) , dependency of the capacitances on the state (on or off) has also been described in the literature. Two different capacitances for C_{ce} are suggested for the turn-on and turn-off transient models by considering the state of the stored excess carriers [48]. In conclusion, the reasons behind the variations of the MOS capacitances and different ways of modeling the variation of switching capacitances are evident in the literature.

4.3.1 Gate to Emitter Capacitance C_{ge}

The turn-on transient is simulated with C_{ge} estimated during the turn-on delay period. A slight variation of C_{ge} is observed during the final gate-to-emitter voltage rising period. However, the same capacitance value of the C_{ge} can be used as any inaccuracy in the estimation of the gate-to-emitter voltage at this phase has only a very small influence on the switching power loss. During the turn-off switching event, the rate of decreasing the gate-to-emitter voltage during the turn-off delay period is found to be different from the rate of decreasing of the gate-to-emitter voltage during the collector current falling phase. In terms of switching power loss estimation performance, accurate estimation of C_{ge} during

the collector current falling phase is more important. However, two capacitance values are utilized for Phase-1 and Phase-3 of the turn-off transient model as in [37]. The method explained in Section 3.3.1 can be applied to find the capacitance C_{ge} with the help of turn-off transient measurements.

4.3.2 Fictitious Miller Feedback Capacitance C_{gc}'

The second term of the charging current depicted in Equation 4-4 is difficult to estimate without an accurate estimation of the gate-to-emitter voltage transient. However, a detailed model of the internal mechanisms of the IGBT is required to estimate the gate-to-emitter voltage transient during Phase-4 of the turn-on transient. Therefore, a set of C_{gc}' values that gives observed collector-to-emitter voltage transient under the estimated gate-to-emitter voltage transient are found for the turn-on transient. Therefore, estimated values of C_{gc}' provides some sort of compensation for the possible errors in estimated gate-to-emitter voltage transient at Phase-4 of the turn-on transient. Use of compensated values of C_{gc}' estimated for the turn-on transient do not yield accurate estimations of collector-to-emitter voltage during the fixed gate-to-emitter voltage region observed in the turn-off transient. Therefore, a different set of C_{gc}' values is necessary for accurate simulation of the turn-off transient. A set of capacitance values can be estimated by applying Equation 3-21 to the turn-off transient measurements.

4.4 List of Model Parameters

All parameters used in the model are listed in Table 4-1. Model utilizes thirteen parameters and three of them extracted from data sheets.

Table 4-1-List of parameters used in the model

Parameter	Symbol	Source of Information
Total Path Inductance of the converter	L_s	Meas. @I_c rising phase
Carrier life time of the diode	τ	Manufacture's Data Sheet
Diode later reverse recovery period	t_b	Manufacture's Data Sheet
Diode junction capacitance	C_{junc}	Meas. @Collector voltage rising phase
Diode diffusion capacitance	C_D	Meas. @ I_c falling phase
Gain of the IGBT	$k_p(1+\beta)$	Meas. @Gate voltage plateau phase
Gain adjusting factor	k_{g_Adjust}	Meas. @I_c rising phase
Collector-to-emitter capacitance	C_{ce}	Manufacture's Data Sheet
Gate-to-emitter capacitance for turn-on switching event	C_{ge}	Meas. @Turn-on delay phase
Gate-to-emitter capacitance for turn-off switching event	C_{ge}	Meas. @ I_c falling phase
Miller capacitance or collector-to-gate capacitance at higher collector voltage	C_{gc}	Meas. @I_c rising phase
Fictitious Miller capacitance for turn-on transient	C_{gc}'	Meas. @Turn-on Phase-4 and Phase-5
Fictitious Miller capacitance for turn-off transient	C_{gc}'	Meas. @Collector voltage rising phase

Chapter 5

Validation of the Switching Transient Models

In this chapter, a brief description of the test setup and the method of measuring the switching transients are given. Then the validation of the turn-on transient model and important observations made during the validation are presented. Finally, the, validation of the turn-off transient model is presented.

5.1 Test Setup and Measuring Transients

Development of a hardware setup that offers minimal undesirable electromagnetic coupling is a challenging task, but it is very important for the model validation. Adverse electromagnetic coupling can cause spurious waveforms that are different from the typical waveforms considered in the model development. Hardware is decomposed into two sections to avoid adverse effects due to interference. An IGBT switch, a freewheeling di-

ode, and a reservoir capacitor are placed on a separate board that handles higher voltages and currents (power board). Another board called the driver board is designed to provide the gate drive. A four-channel high bandwidth digital storage oscilloscope with differential inputs is utilized to capture switching voltage transients. A Hall effect based clip-on sensor is utilized to capture current waveforms.

5.1.1 Hardware Setup Design

The effect of electro-magnetic interferences (EMI) is extremely difficult to quantify. Electromagnetic coupling between signal paths causes various dynamics that are not involved in the simulation model. Negative impacts of stray inductance on switching performance of IGBTs and capturing switching waveforms are explained in [49]. Higher path stray inductance lowers the reliability of operation due to large overshoots in the collector-to-emitter voltage and results in very high level of electromagnetic interferences. There are practical guidelines that help in the design of converter hardware setups with minimum path stray inductance. Guidelines for low stray inductance busbar design and detailed description of bus bar modeling is given in [50]. Generally, the printed circuit boards (PCB) of large power hardware are designed with minimum path length and larger thickness to minimize the stray inductance. Selected path thickness can be checked against the ability to carry expected maximum current. Space between the paths must be adequate to avoid flashover between the paths. The most important aspect is the layout of the PCB. The layout determines the coupling between paths. If the path that connects the gate drive with IGBT is not kept away from the collector side paths having large swing of currents and voltages, induced voltages from collector side might modify the gate drive

signal. All of the above measures are taken to minimize the discrepancy between simulated model and actual hardware to be simulated.

In addition, variation of DC bus voltage during rapid rise of collector current acts as a disturbance to the converter operation and strong DC bus is often utilized in practical converters. The position of the reservoir capacitor determines the voltage drop during fast transients. Therefore, the reservoir capacitor is soldered closer to the terminals of the switching cell. Estimation of minimum capacitance that keeps bus voltage variation within an acceptable voltage tolerance at turn-on transient can be calculated as follows. In the worst case, the total transient current can be assumed supplied by the capacitor. The current contribution from the supply becomes negligible due to large stray inductance of connecting wires. If the expected maximum load current is 20A and the switching period is assumed to be 100ns, the amount of charge depleted during the transient, $\Delta Q_{Discharge}$ can be approximately estimated assuming a linear rise of current.

$$\Delta Q_{Discharge} = \frac{1}{2} \times 20A \times 100ns = 1\mu C$$

The minimum capacitance of the reservoir capacitor that limits the voltage changes at the terminal of the capacitor to 3V is calculated as.

$$C_{min} = \frac{\Delta Q_{Discharge}}{V} = \frac{1\mu C}{3V} = 333nF$$

According to the above result, in order to maintain a constant supply voltage during the switching period, a large capacitor is not essential. Generally larger capacitors have higher series inductance. Therefore, a combination of large and smaller capacitances is often used in practice. In such situations, larger capacitors serve better during load current tran-

sients that last for longer periods and smaller capacitors support the voltage during switching transients.

For validation of the turn-on transient model, it is required to capture turn-on switching transient behavior at a non-zero load current. This is achieved by applying a number of consecutive pulses to the IGBT by means of a special control board and then turning-off the IGBT for a longer period to minimize rise of temperature. Figure 5-1 illustrates functions of the control board.

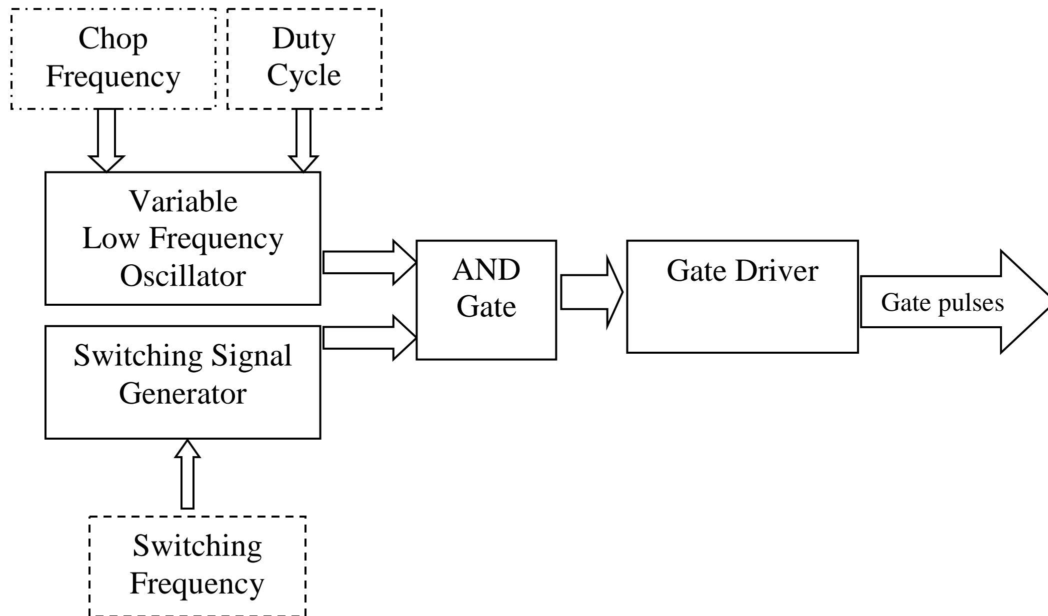


Figure 5-1- Control board of the gate drive

Multiplication of a low frequency signal with a continuous switching pulse train causes a number of consecutive switching pulses when the low frequency pulse is high and then a period where there are no pulses when the output of the low frequency oscillator is low. The ratio between pulse train and the pause period can be adjusted by the duty ratio of the low frequency oscillator.

The periodic of the switching pulses is set to a fraction of time constant of the load. Application of a number such gate pulses facilitates taking measurements at different load currents as depicted in Figure 5-2.

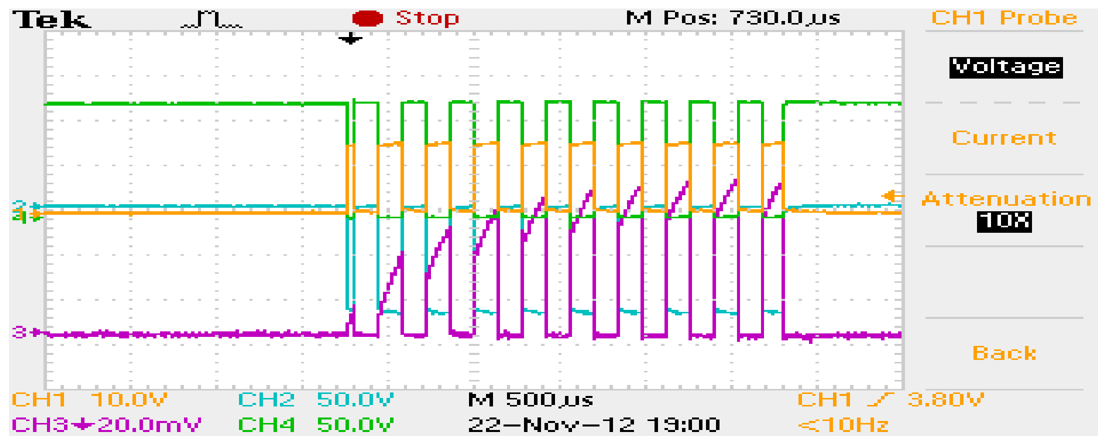


Figure 5-2-A snap-shot of the gate drive signal

The rationale behind the selection of such a waveform is explained below. The frequency of the consecutive gate pulses having higher frequency is referred to as the switching frequency and the frequency of the pulse that enables or disables the switching pulses to pass through the gate is referred to as the burst frequency. Suppose an inductive load having a time constant of 0.5ms is used as the load, then the time taken to raise the current through the inductor to the maximum current is 2.5ms if the duty cycle of the gate drive is 100%. If the switching frequency is set to 2 kHz (periodic time is 0.5ms), it is possible to capture exponentially increasing collector current at least at five equally spaced points during a burst. It is possible to sample the collector current at about 10 points when the duty cycle of the switching signal is 50%. The maximum percentage variation of the load current during a period of 1µs is only 0.2% when the time constant of the load is 0.5ms. Switching events do not last for more than 1µs. Therefore, load current can be assumed constant during the switching period without any loss of accuracy. The ability to adjust

the switching frequency between 1 kHz-6 kHz is used to capture collector current variation at finer steps at different loads. The difference between the two consecutive left edges of the pink bars (collector current traces shown in Figure 5-2) shows the possible steps of collector current at the turn-on transients.

The special gate drive signal facilitates a shorter conduction time of the IGBT when compared with the time that the IGBT that does not conduct. Hence, less dissipation through the IGBT and negligible temperature rise during the experiment. Such a gate drive signal overcomes the need to take temperature measurements during switching transient measurement. Converter is fed with a high power DC amplifier AE TECHRON 224. The amplifier is used to vary the supply voltage to the converter.

5.1.2 Switching Trajectory Measurements

An isolated 4-channel oscilloscope model Tektronix TPS2024 is used to capture the switching transients. The bandwidth of the TPS2024 is 200MHz and the bandwidth requirement is tested as explained below. The rise time of the output signal of the oscilloscope amplifier is estimated for an ideal step input with Equation 5-1[51].

$$t_r \approx \frac{0.35}{Band\ Width} \qquad \text{5-1}$$

Equation 5-1 gives an approximated rise time of the amplifier by assuming single pole dynamic and the estimated rise time is 1.79 ns. This oscilloscope is selected to obtain voltage measurements as the estimated rise time of the amplifying system of the oscilloscope is much less than the rise time of the transient to be captured. A number of ways that can be used to measure current is listed in [52]. Considering ease of use and availability, a Hall effect sensor TEKTRONIX P6303 is selected. The bandwidth of the select-

ed Hall sensor is 15MHz. The estimated rise time of the probe using Equation 5-1 is about 20 ns. This period is about one fifth of the typical rise time of the measured current transients. Limitation of the performances of this current sensor is kept noted when faster transits are captured.

Application of bursts of gate pulses leads to a challenging situation in capturing transients at a desired point as there is no assurance of switching occurring at the same current. Selection of the appropriate combination of trigger signal source, trigger event, and type of coupling of the trigger signal is used to solve the above problem. If it is required to capture the turn-off transient at different collector currents, the amplitude of collector-to-emitter voltage is used to capture the turn-off transient as the collector-to-emitter voltage overshoot is a unique signature that distinguish turn-off transient at different collector currents. This signature enables taking a snapshot within a small fraction of time. The captured data sequence is compared with the simulation response by superimposing the simulation response on to the measured sequence with help of resampling and aligning as in the Section 5.2 and 5.3

5.2 Turn-on Transient Model Validation

Models are validated for a range of values of each input to the model. When possible, measurements are obtained at different model parameter values. This is to ensure the validity of model under changing operating conditions and parameters. The load current and the supply voltage are the two model inputs to be varied. Converter specific model parameters that can be varied are the characteristics of the gate drive and the path induct-

ances of the converter. Gate characteristics include gate resistance, rise time of the gate pulse, and the gate drive voltage.

The extraction of IGBT parameters is illustrated in Sub-section 5.2.1. Then, the turn-on transient model is evaluated under different operating conditions by changing the possible model inputs described above. In this chapter, the accuracy of the model is evaluated qualitatively via visual comparison of similarity between the estimated and measured transient trajectories. In Chapter 6, the accuracy is estimated quantitatively, in terms of the closeness between the estimated and measured switching losses. As the collector current is increasing during both phases 2 and 3, hereafter, the total period of phases 2 and 3 is referred to as the "collector current rising" period. Similarly, phases 4 and 5 together are called collector-to-emitter voltage falling period.

5.2.1 Parameter Extraction

Parameter extraction of the IGBT-IRGP4072DPBF is illustrated here. The turn-on transient measurement of IRGP4072DPBF shown in Figure 5-3 is used to apply the parameter extraction procedure explained in Section 3.3. The gate-to-emitter capacitance C_{ge} can be estimated with the help of Equation 3-13 applied to the duration between the instances *1-I* and *1-f* shown in Figure 5-3.

$$C_{ge} = \left(\frac{t_f - t_i}{R_G}\right) \times \frac{1}{\ln\left[\frac{\left(V_{GDH} - V_{ge_i}\right)}{\left(V_{GDH} - V_{ge_f}\right)}\right]}$$

Substituting the values shown in the graph and 100Ω for R_G

$$C_{ge} = \left(\frac{10 \times 10^{-9}}{100}\right) \times \frac{1}{\ln\left[\frac{(15-1.81)}{(15-2.23)}\right]} = 3.09nF$$

The above equation uses the measured time duration between the instances *1-I* and *1-f* of 10ns. The gain constant during phases 2 and 3 is estimated by applying Equation 3-14 to the Instant-3 shown in Figure 5-3. The threshold voltage V_T of the IGBT is 5.2V.

$$K_{g_adjust}k_p(1+\beta) = \frac{I_{cm}}{\left(V_{gem}-V_T\right)^2}$$

$$K_{g_adjust}\ k_p(1+\beta) = \frac{5.50}{(7.33-5.2)^2} = 1.21\ A/V^2$$

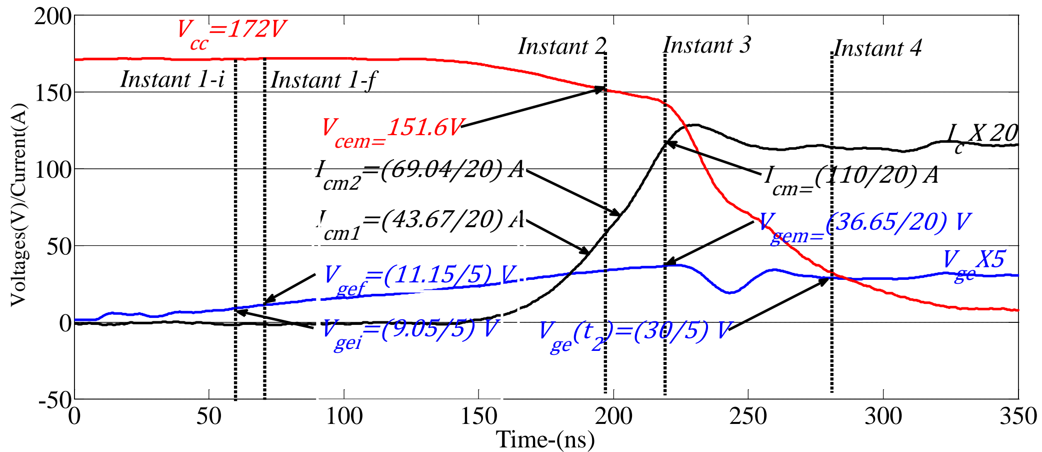


Figure 5-3-Measured turn-on transient of IRGP4072DPBF at *Vcc=172V, IL=5.5A,* and *RG=100Ω*

Stray inductance L_s is estimated using Equation 3-15 with estimated numerical values indicated around Instant-2 of Figure 5-3.

$$L_s = \frac{V_{L_s}}{dI_c/_{dt}} = \frac{(V_{cc}-V_{cem})}{\left[dI_c/_{dt}\right]_{t=tm}} = \frac{(172.0-151.6)}{\left[\frac{(3.45-2.18)}{12\times10^{-9}}\right]} = 192.76nH$$

The above equation uses the interval between two collector current measurements I_{cm1} and I_{cm2} of 12ns. Nominal gain can be estimated from Equation 3-20 to the Instant-4.

$$k_p(1+\beta) = \frac{I_{cm}}{\left(V_{gep}-V_T\right)^2}$$

$$k_p(1+\beta) = \frac{5}{(6-5.2)^2} = 8.60$$

Therefore gain adjusting factor K_{g_adjust} is the ratio between 1.21 and 8.6 or 0.14. The measured collector-to-emitter voltage at the end of the Phase-3 is 145.3V. The set of capacitance values found for the fictitious Miller capacitance for $C_{gc'}$ is shown in Table 3-1 of the Section 3.3.4. Miller capacitance $C_{gc'}$ used to simulate Phase-2 and Phase-3 is assessed first by applying Equation 3-17 to obtain an initial guess and then refining it by comparing the estimated response with the measurement. The estimated capacitance value is 20pF. For C_{ce} , the value given in the data sheet, 75pF (at higher voltages) is used. The IGBT which is designated as APT12GT60BR also used for the model validation and extraction of parameters of the APT12GT60BR is shown below. The turn-on transient measurement of APT12GT60BR shown in Figure 5-4 is used for parameter extraction. The gate-to-emitter capacitance C_{ge} is estimated by applying Equation 3-13 to the instances *1-I* and *1-f* shown in Figure 5-4. The measured duration between these two instant is 4ns and gate resistance R_G is 150Ω.

$$C_{ge} = \left(\frac{4\times 10^{-9}}{150}\right) \times \frac{1}{\ln\left[\frac{(15-2.05)}{(15-2.71)}\right]} = 0.509nF$$

The gain constant is estimated with help of gate-to-emitter voltage and collector current measurements at Instant-3 (when $I_{cm} = I_L$) shown in Figure 5-4. The estimated threshold voltage of this IGBT is 4.1V.

$$K_{g_adjust} k_p(1+\beta) = \frac{4.65}{(8.55-4.1)^2} = 0.24$$

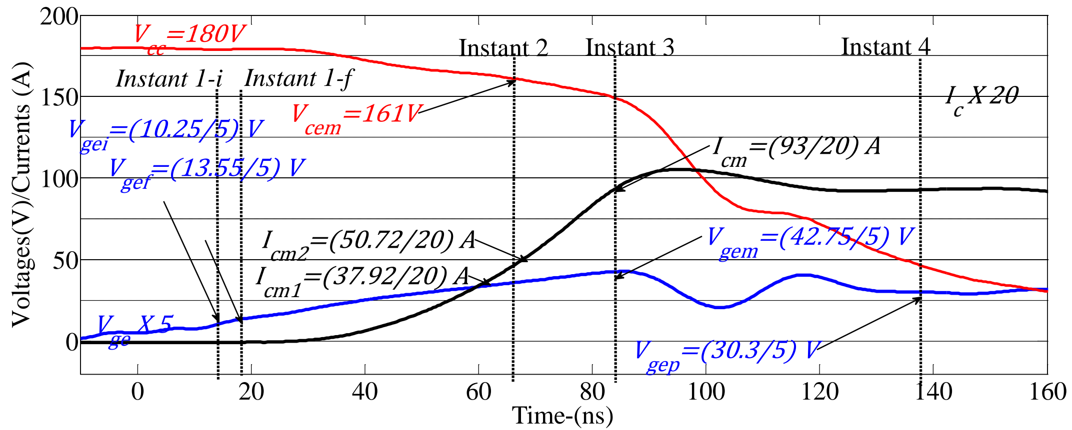


Figure 5-4-Measured turn-on transient of APT12GT60BR when *Vcc=180V, IL=4.65A, and R_G=150Ω*

Stray inductance L_s is estimated using Equation 3-15 with numerical figures as depicted at around Instant-2 in Figure 5-4 and elapsed time duration of 6ns between I_{cm1} and I_{cm2}.

$$L_s = \frac{(180-161)}{\left[\frac{(2.54-1.90)}{6\times10^{-9}}\right]} = 178.13nH$$

The nominal gain can be estimated from Equation 3-1 at Instant-4.

$$k_p(1+\beta) = \frac{4.65}{(6.06-4.1)^2} = 1.21$$

Therefore, the gain adjusting factor is 0.20. Table 5-1 shows estimated values for the fictitious Miller capacitance for $C_{gc'}$.

Table 5-1-Estimated fictitious Miller capacitances for APT12GT60BR

V_{ce} (V)	400	100	50	25	15	10	2
$C_{gc'}$ (pF)	18	25	40	80	100	1500	2800

Estimated Miller capacitance C_{gc} used to simulate Phase-2 and Phase-3 is 30pF. The data sheet value 25pF is used for C_{ce}.

The other IGBT used for the validation is IRG6I320UPBF. Figure 5-5 shows the turn-on transient measurement used to extract the parameters.

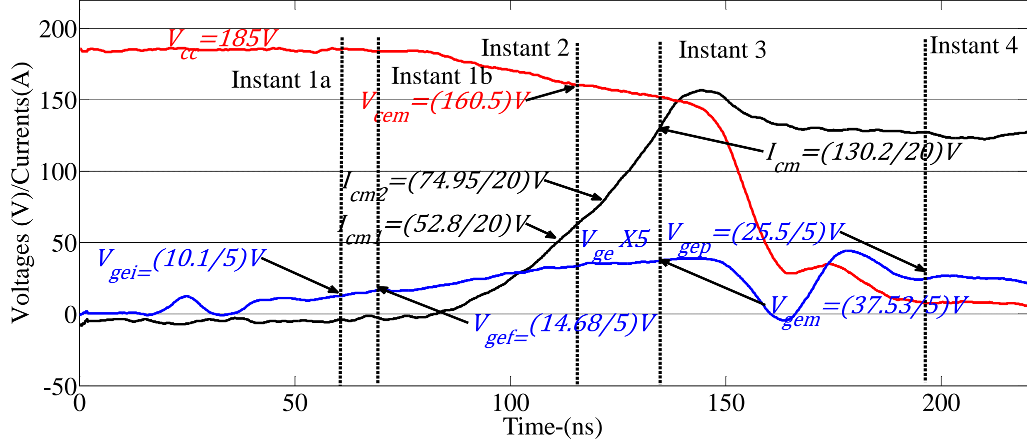


Figure 5-5-Measured turn-on transient of IRG6I320UPBF at *Vcc=185V, IL=6.5A, and RG=150Ω*

Estimated parameters using numerical values shown in the Figure 5-5 is shown below. Elapsed time between instances *1-I* and *1-f* is about 9.4ns and gate resistance is 150Ω.

$$C_{ge} = \left(\frac{9.4 \times 10^{-9}}{150}\right) \times \frac{1}{\ln\left[\frac{(15-2.02)}{(15-2.94)}\right]} = 852pF$$

The gain constant using the threshold value of 4V.

$$K_{g_adjust} k_p(1+\beta) = \frac{6.5}{(7.51-4)^2} = 0.53$$

Stray inductance is estimated below using the measured duration of 8.4ns between measurements I_{cm1} and I_{cm2}.

$$L_s = \frac{(185-160.5)}{\left[\frac{(3.75-2.64)}{8.4\times10^{-9}}\right]} = 185.41nH$$

The nominal gain is estimated from the measurement at Instant-4.

$$k_p(1+\beta) = \frac{6.5}{(5.1-4)^2} = 5.37$$

Therefore, the gain adjustment constant K_{g_Adjust} is 0.098.

Table 5-2 shows estimated values for the fictitious Miller capacitance for $C_{gc'}$.

Table 5-2-Estimated fictitious Miller capacitances for IRG6I320UPBF

V_{ce} (V)	400	100	65	30	15	10	0
$C_{gc'}$ (pF)	10	15	20	50	125	600	1000

The estimated Miller capacitance $C_{gc'}$ used to simulate Phase-2 and Phase-3 is 12 pF. The data sheet value 20pF is used for C_{ce}

5.2.2 Impact of Anti-parallel Diode of the Conducting IGBT

Figure 5-6 depicts a comparison between the estimated response and the measured response. The turn-on transient model described in Chapter-3 ignores the effect of the anti-parallel diode of the conducting IGBT. The antiparallel diode of the IGBT has a finite reverse junction capacitance.

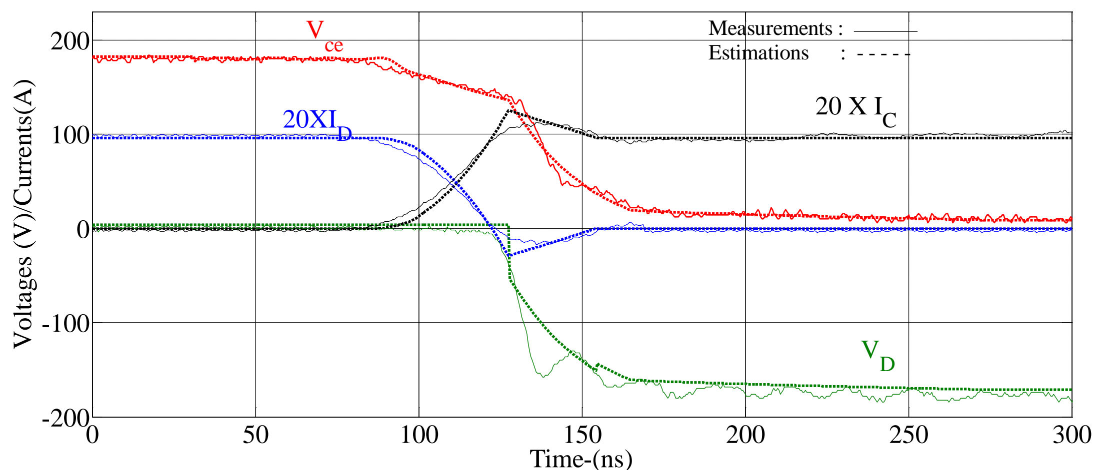


Figure 5-6- Estimated and Measured waveforms during turn-on transient of RGP4072DPBF at V_{cc}=180V, I_L=5A, and R_G=70Ω

Variation of collector-to-emitter voltage should be facilitated via discharging this nonlinear reverse junction capacitance. Depletion of the stored charge in junction capacitance decreases the collector current as the load current is fixed. Junction capacitance is significant at lower voltages where the rate of change of the voltage is not high. Therefore, this effect is ignored as significant deviation of collector current could not be observed in the measurements. Measurements are taken from a co-pack IGBT –IRGP4072DPBF which contains both an IGBT switch and an antiparallel diode ISL91560P2. These measurements are used to check whether the anti-parallel diode of the IGBT significantly affects the accuracy of the model. A close match between the estimated and the measured responses shows that the antiparallel diode does not significantly affecting the accuracy of the switching trajectory prediction. Therefore, the model of the turn-on transient is simplified by ignoring the effect of this nonlinear junction capacitance. All measurements are made with the freewheeling diode ISL91560P2.

5.2.3 Effect of Load Current Changes

With a fixed supply voltage and gate drive, increase of the load current elongates Phase-2 as well as Phase-3. The duration of the Phase-2 increases because a longer time is required to reach greater current level at a given slope. In addition, the maximum reverse recovery current also increases with the load current. Therefore, the period of Phase-3 also becomes longer. Therefore, increase of load current increases the duration of phases 2 and 3, because the rate of increasing of collector current is independent from the load current. The capability to track the load current changes of the model is compared with the help of Figure 5-7 and Figure 5-8. Figure 5-7 compares the model responses at a load

current of 4.15A and Figure 5-8 compares the responses at about 50% higher load current. However, the increment of time taken to reach load current may not proportional to the increment in load current. Later reverse recovery period t_b slightly increases with the load current.

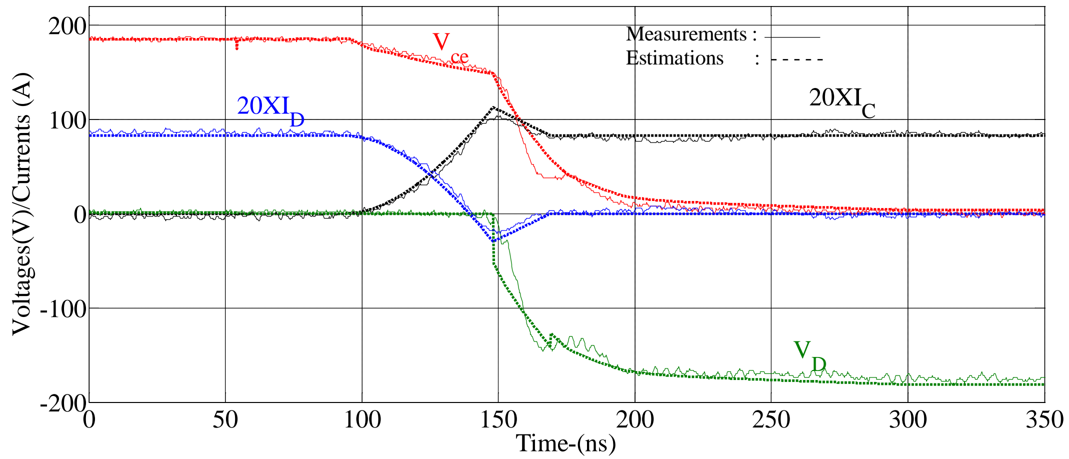


Figure 5-7- Turn-on transient of IRG6I320UPBF at $V_{cc}=185V$ and $I_L=4.15A$ when $R_G=150\Omega$

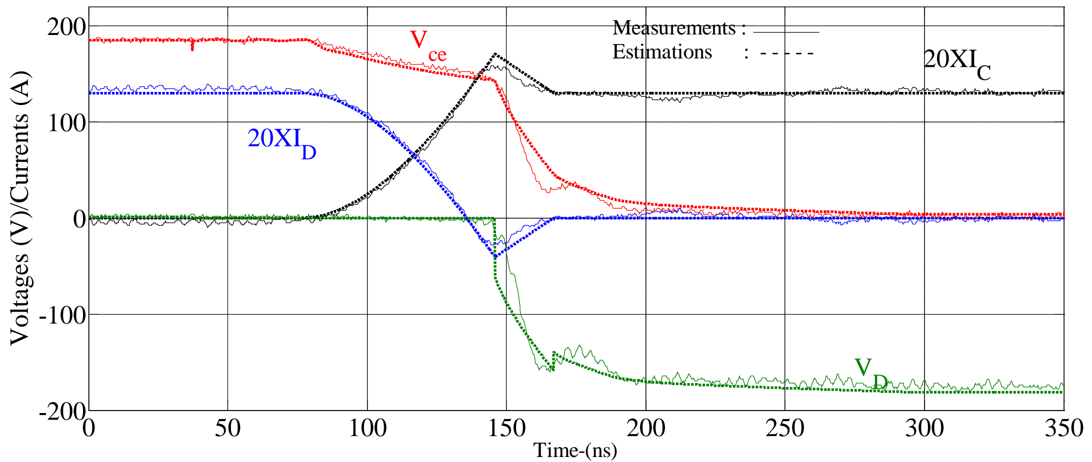


Figure 5-8- Turn-on transient of IRG6I320UPBF at $V_{cc}=185V$ and $I_L=6.5A$ when $R_G=150\Omega$

Adequate correlation of estimated responses in both situations indicates the ability of the proposed model capture the turn-on behavior at different load currents.

5.2.4 Effect of Supply Voltage Changes

Collector-to-emitter voltage variation is determined by the slope of the collector current trajectory during the collector current rising phase. For a given IGBT, the slope of the collector current trajectory is determined by the gate drive and is almost independent from the supply voltage. Consequently an increase or decrease of the supply voltage just brings the collector-to-emitter voltage trajectory up or down by the same amount during Phase-2 and Phase-3. Figure 5-9 compares the measured and estimated responses of the IRG6I320UPBF when the supply voltage is reduced from 185 V to 135V while keeping the gate resistance and the load current the same as in the measurements shown in Figure 5-7.

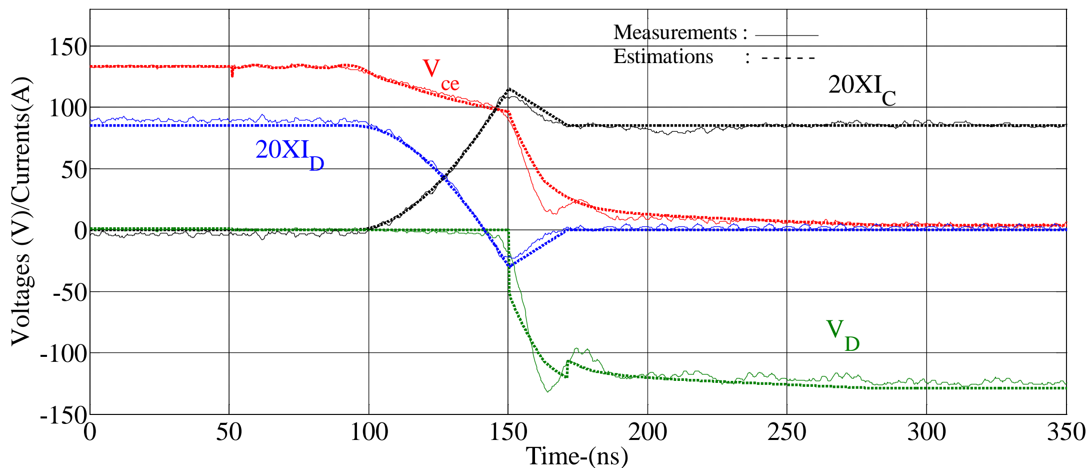


Figure 5-9- Turn-on transient of IRG6I320UPBF at $V_{cc}=135V, I_L=4.15A,$ *and* $R_G=150\Omega$

According to Figure 5-7, the collector-to-emitter voltage trajectory more or less linearly decreases from 185V to 150V when supply voltage is 185V during the collector current rising phase. As indicated in Figure 5-9, the collector-to-emitter voltage drops from 133V to about 98V in the same way when the supply voltage is reduced to 133V. The shape of

the collector-to-emitter trajectory below 98V should be the same in the measurements shown in Figure 5-9 and Figure 5-7. This happens because the shape of the collector-to-emitter voltage trajectory during phases 4 and 5 is solely determined by the profile of the fictitious Miller capacitance and the charge extraction rate as explained in Section 3.2.5 and Section 3.2.6. Profile of the fictitious Miller capacitance is fixed for a given device. The charge extraction rate is fixed at given gate drive and load current.

5.2.5 Effect of Gate Resistance Changes

Changes in the gate resistance do not merely speed up or slow down the switching process. Gate resistance changes affect the turn-on switching process in a number of ways. A high rate of rising collector current at lower gate resistance increases the collector-to-emitter voltage drop during the collector current rising phase. A rapid drop in the collector-to-emitter voltage resist increase of the gate-to-emitter voltage rise due to Miller feedback. Therefore, the feedback effect is more prominent at lower gate resistances. Therefore, a proper model should be able to capture changes in dynamics at different gate resistances. Figure 5-10 and Figure 5-11 compares the accuracy of estimated responses for IGBT-APT12GT60BR with two gate resistance values where one is approximately half of the other. According to Figure 5-11, the model is capable of estimating the increased slope of the collector current trajectory as well as the increased collector-to-emitter voltage drop at the lower gate resistance. Furthermore, decrease of the gate resistance increases the charge supply rate to extract stored charges in Miller capacitances.

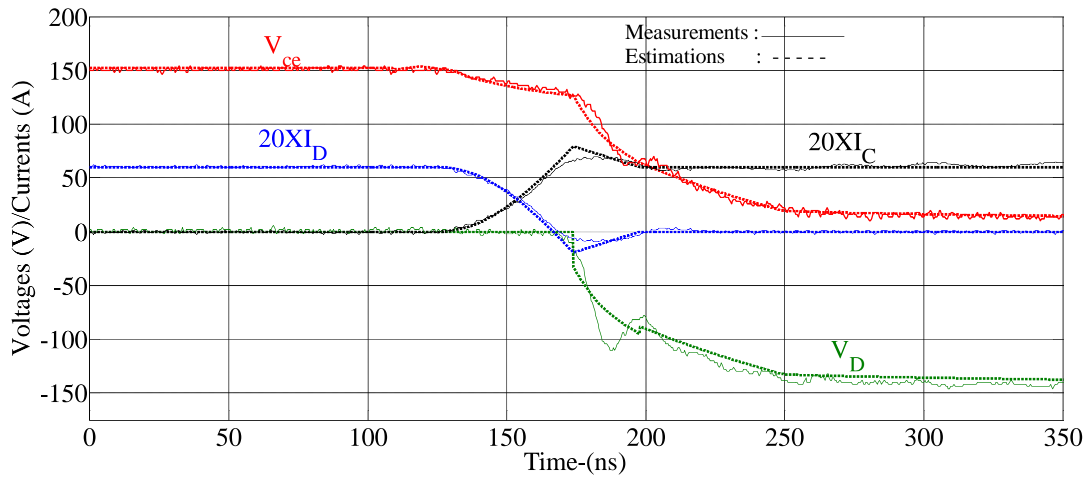


Figure 5-10- Turn-on transient of APT12GT60BR at V_{cc}=152V, I_L=3A, and R_G=150Ω

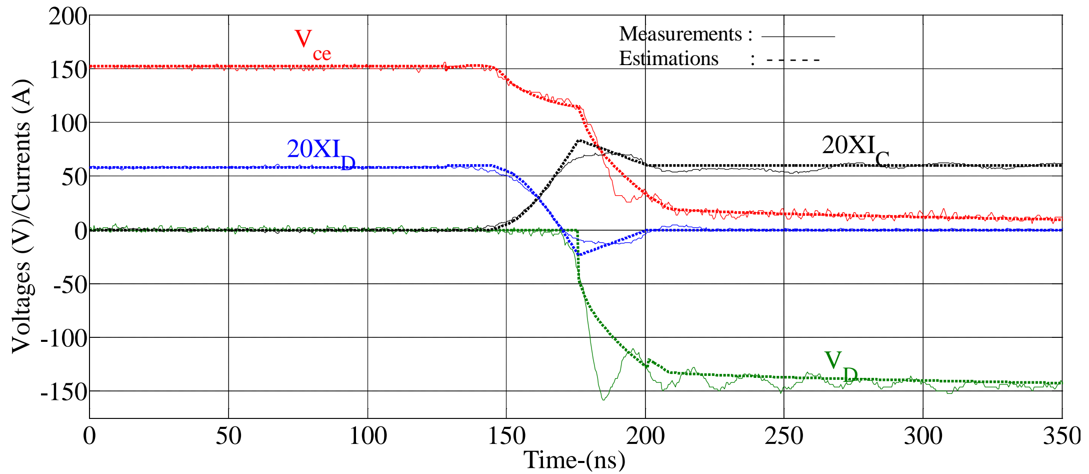


Figure 5-11- Turn-on transient of APT12GT60BR at V_{cc}=152V, I_L=3A, and R_G=70Ω

Match between the estimated and measured responses at different values of gate resistances reflect the effectiveness of modeling the Miller feedback effect.

5.2.6 Validation of Model over Different Operating Points

Figure 5-12 through Figure 5-17 shows the match between estimated and measured responses at different supply voltages, load currents, and gate resistances. These comparisons shows the ability to estimate transient waveforms at an adequate level of accuracy

under a wide range of operating conditions in a wide range using a set of parameters estimated with a single test measurement. Moreover, since the converter specific parameters such as stray inductance and gate resistance are explicitly modeled, they can differ from the test circuit and can be substituted with the values applicable to the converter being studied.

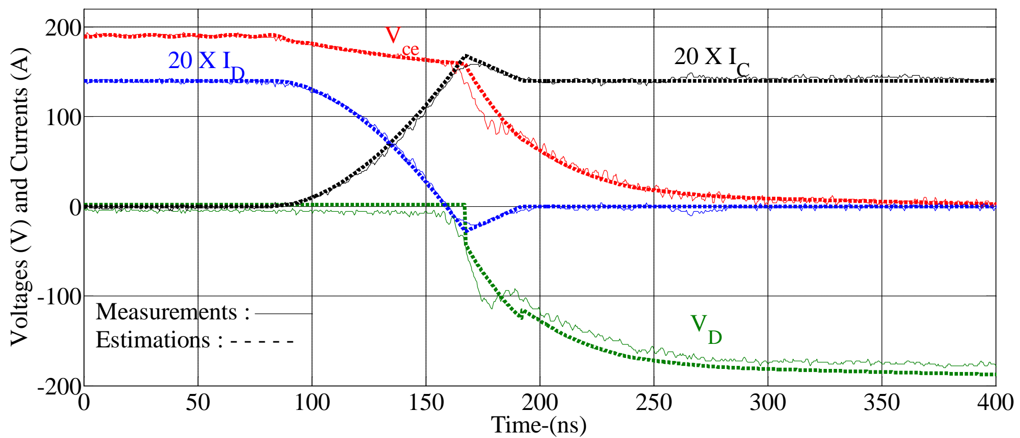


Figure 5-12- Turn-on transient of IRG6I320UPBF at $V_{cc}=190V$, $I_L=7A$, and $R_G=100\Omega$

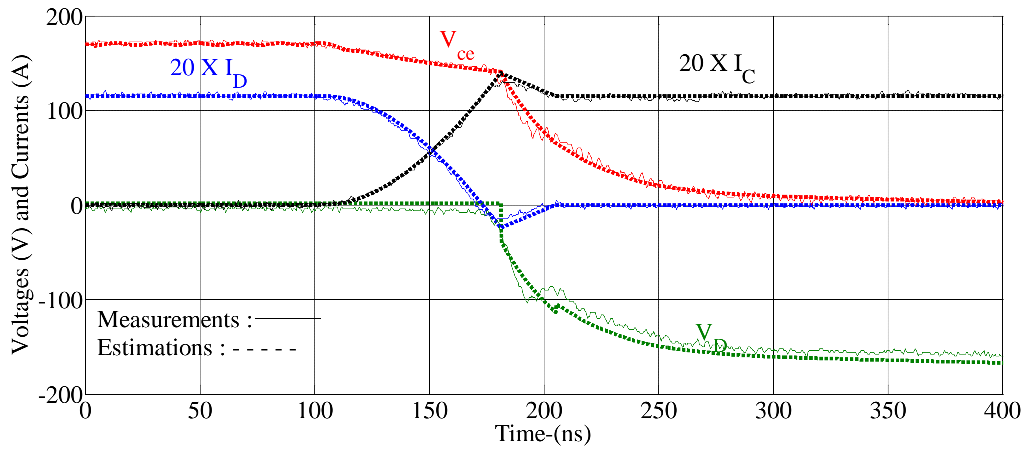


Figure 5-13-Turn-on transient of IRG6I320UPBF at $V_{cc}=170V$, $I_L=5.75A$, and $R_G=100\Omega$

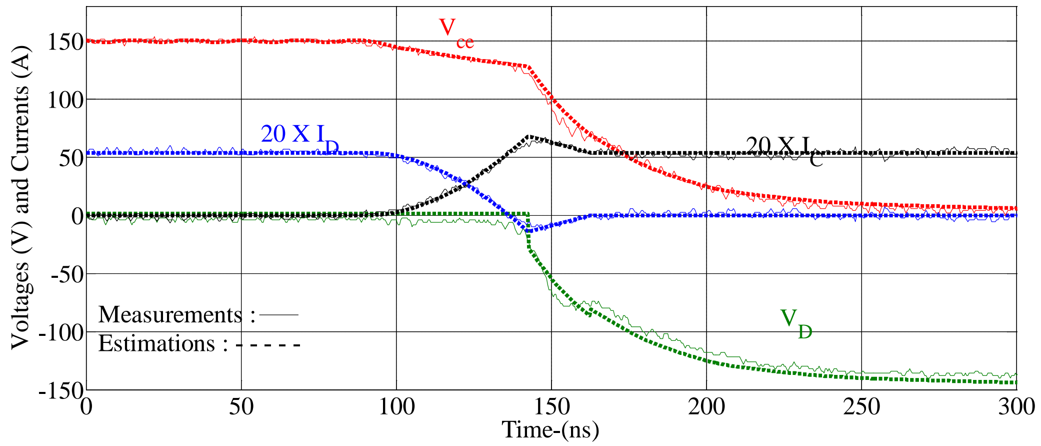


Figure 5-14- Turn-on transient of IRG6I320UPBF at V_{cc}=150V, I_L=2.5A, and R_G=100Ω

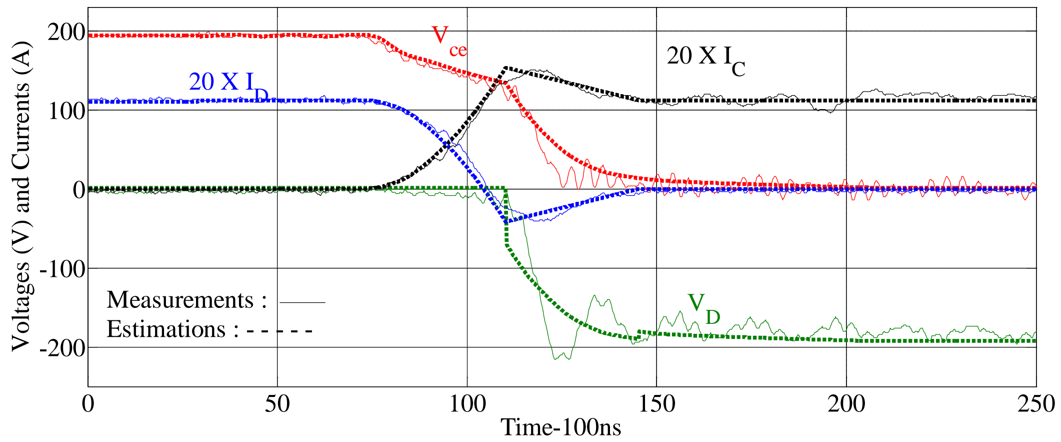


Figure 5-15- Turn-on transient of IRG6I320UPBF at V_{cc}=190V, I_L=5.5A, and R_G=30Ω

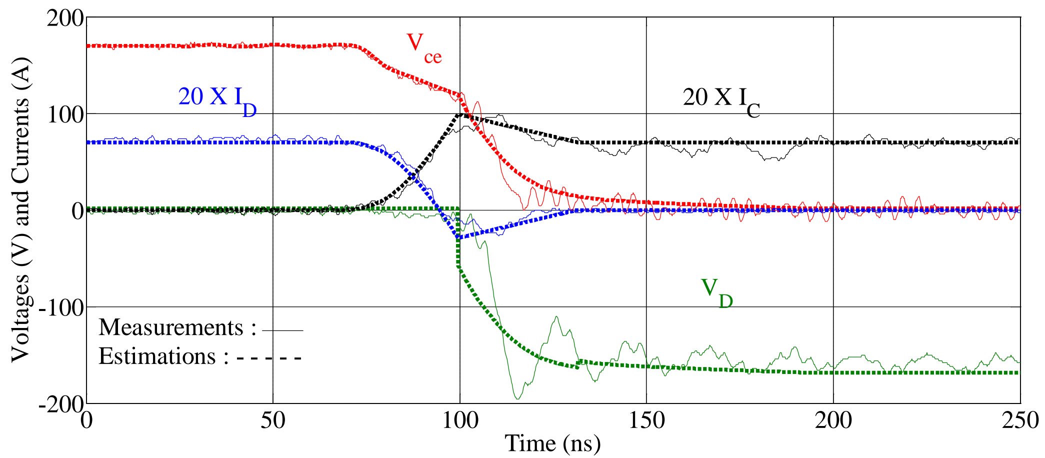


Figure 5-16- Turn-on transient of IRG6I320UPBF at V_{cc}=170V, I_L=3.5A, and R_G=30Ω

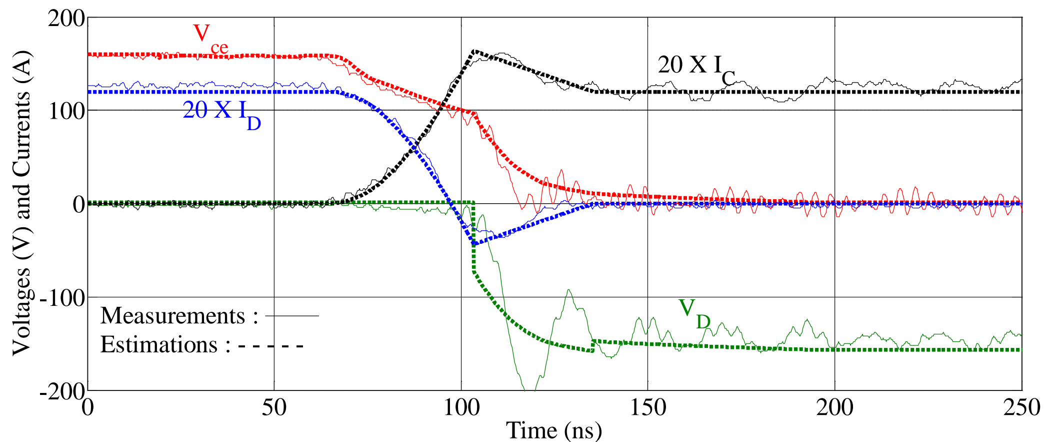


Figure 5-17- Turn-on transient of IRG6I320UPBF at V_{cc}=162V, I_L=6A, and R_G=30Ω

According to Figure 5-15 through Figure 5-17 which shows transients during small gate resistance, some oscillations in the diode voltage and the collector current can be seen when the collector-to-emitter voltage is small. The diode voltage and collector current are respectively the load voltage and load current after the fourth phase. This fluctuation is assumed to be caused by oscillation of the energy between the inductive load and output capacitances of the IGBT.

5.2.7 Miller Feedback Effect

Before applying the gate pulse, the voltage across the Miller capacitor is approximately equal to the supply voltage. In this state, the gate side of the Miller capacitor is negatively charged while the collector side is positively charged. During the turn-on transient, stored charges within Miller capacitance has to be discharged to support the decrease of the collector-to-gate voltage. Therefore, at a fixed collector-to-emitter voltage, a part of the positive charges supplied by the gate drive should flow through Miller capacitor C_{gc} during the first three phases in the turn-on switching transient. Consequently, Miller capacitance has an overall effect of delaying the development of the gate-to-emitter voltage at a fixed

collector-to-emitter voltage. The model circuit having a parallel Miller capacitance and C_{ge} that simulates the turn-on delay appropriately indicates this effect. During Phase-2, the collector-to-emitter voltage decreases when slope of the collector current increases. The reduction of collector-to-emitter voltage should be supported by adding some amount of negative charge to the collector side plate and the same amount of positive charges to the gate side plate. Therefore, increase of the collector current slope decreases the collector-to-emitter voltage and diverts more current from gate drive through the Miller capacitor. This feedback mechanism limits the speed of the collector current rising trajectory. Figure 5-18 depicts the sudden variation of the slope of the gate-to-emitter voltage variation when the collector-to-emitter voltage drops. Therefore, the Miller feedback effect does not allow to increase slope of the collector current continuously. This is one reason behind the approximately linear increase of collector current during the turn-on transient. Figure 5-18 depicts the nearly linear rise of the collector current trajectory as described in [6].

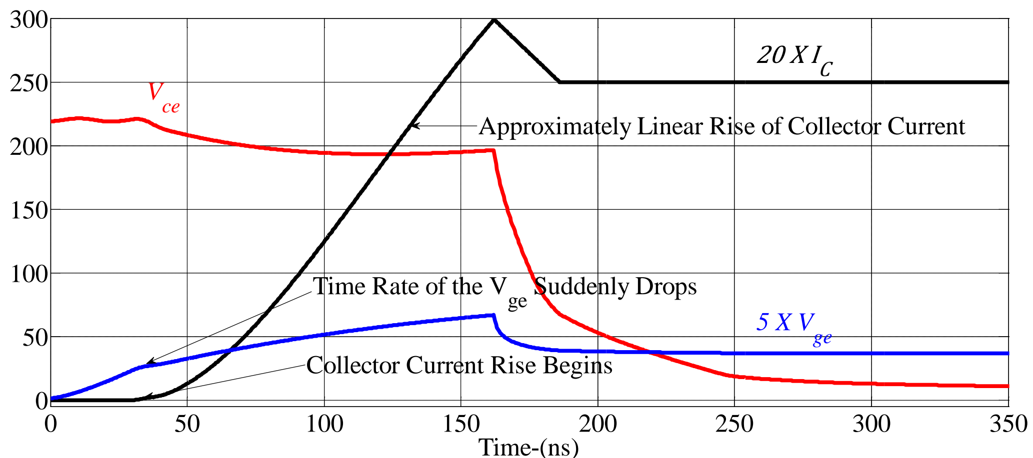


Figure 5-18 Reflection of variation of V_{ce} to V_{ge} due to Miller feedback

The other reason for the linear increase of collector current is that the slope of the collector current is proportional to the square of the instantaneous distance of the gate-to-

emitter voltage from the gate-to-emitter threshold voltage. However, in the absence of Miller feedback or when it is insignificant (occurs when collector-to-emitter voltage variation is insignificant or during constant slope of the collector current), gate-to-emitter voltage should follow an exponential rise. Therefore, continued gain increase is counter balanced by the continuously decreasing rate of change of the gate-to-emitter voltage rise. In the suggested model, the collector current rising phase is simulated with a constant Miller capacitance. Fine correlation between the estimated responses and the measured response shown in Section 5.2.3 to 5.2.6 reflects adequacy of the approach.

5.3 Turn-off Transient Model Validation

Suggested parameters that are different from the values used in the turn-on model are first estimated. The gate-to-emitter capacitance is estimated for Turn-on delay using the capacitor discharging equation. For the fast collector current falling phase, a rough value for C_{ge} is estimated using the capacitor discharging equation by ignoring the Miller feedback effect. The value is refined by comparing the estimated gate-to-emitter voltage transient with measurement. For the IRG6I320UPBF, two capacitance values 1100 pF and 1300 pF are respectively estimated for turn-off delay phase and fast collector current falling phase. The estimated set of fictitious capacitances for the turn-off transient of IRG6I320UPBF is given in Table 5-3.

Table 5-3-Estimated fictitious Miller capacitances of IRG6I320UPBF for turn-off

V_{ce} (V)	300	45	35	20	15	10	0
$C_{gc'}$ (pF)	40	60	120	150	600	900	1400

Similarly those parameters are estimated for the APT12GT60BR. Two capacitance values 450 pF and 500 pF are respectively estimated for the turn-off delay phase and the fast collector current falling phase. The estimated set of fictitious capacitances for the turn-off transient of the IRG6I320UPBF is given in Table 5-4.

Table 5-4-Estimated fictitious Miller capacitances for APT12GT60BR for turn-off

V_{ce} (V)	300	45	35	20	15	10	0
$C_{gc'}$ (pF)	50	70	120	150	900	1800	3000

Values of the other parameters are the same as values used in turn-on transient model. The turn-off transient model is validated once parameters are estimated.

Figure 5-19 compares the estimated and measured trajectories of turn-off switching event of IRG6I320UPBF. Figure 5-19 depicts good correlation between measured and estimated trajectories that is adequate for switching loss estimation. Although not significant, two noticeable deviations between the measured and estimated trajectories can be seen.

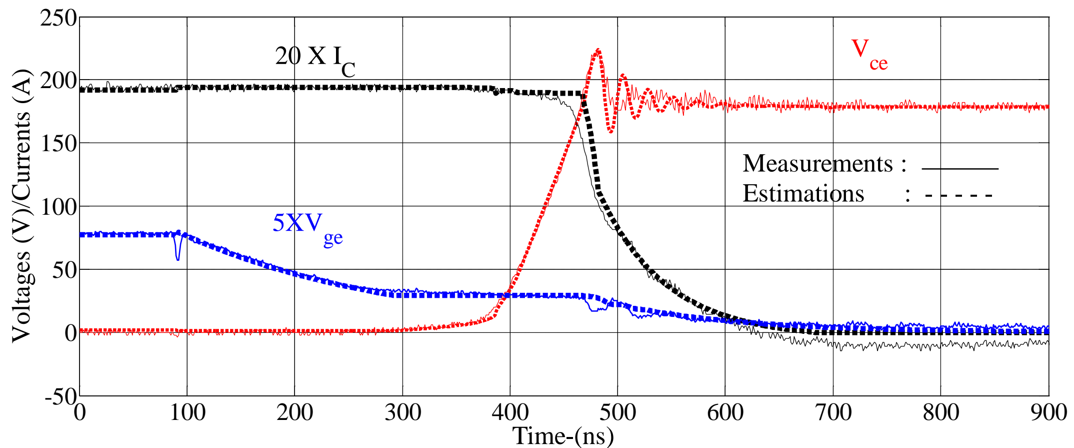


Figure 5-19- Turn-off transient of IRG6I320UPBF at V_{cc}=180V, I_L=9.65A, and R_G=70Ω

The initial collector current drop is gradual in the measurement and the estimated collector-to-emitter voltage overshoot is slightly different from measured. The collector current

drop is due to depletion of stored charges in the reverse biased freewheeling diode. Collector current variation due to the discharging junction capacitance of the freewheeling diode is more prominent during turn-off because the rate of change of voltage across the diode is higher and the capacitance is large. This error could be a result of the approximate diode capacitance model. The estimation of the collector-to-emitter voltage trajectory is accurate at around the supply voltage level as depicted in Figure 5-19. Reverse junction capacitance of diodes is essentially a nonlinear capacitance as described in Equation 4-5. However, use of fixed capacitance facilitates achieving certain level of simplicity and improves the computational efficiency. Therefore, diode reverse capacitance is represented as a fixed capacitance. Simulation of current through the diode with fixed capacitances is a common practice [21].

5.3.1 Reverse Voltage Transient of the Diode Voltage

According to the suggested model, increase of the collector-to-emitter voltage of the IGBT is solely characterized by the gate drive and profile of C_{gc}'. The diode voltage variation is assumed to be merely a response to the collector-to-emitter voltage variation. Validity of the above model is investigated by comparing the measured diode voltage trajectory and the estimated collector-to-emitter voltage trajectory which relied on the above assumption. Figure 5-20 compares the estimated collector-to-emitter voltage trajectory and measured diode voltage trajectory. This estimation is done for the IRG6I320UPBF with the freewheeling diode ISL91560P2. The green trajectory obtained by shifting the DC level of the diode voltage overlaps with the estimated collector-to-emitter voltage. The variation of the collector-to-emitter voltage must be equal to the diode voltage varia-

tion when there is no current change through the stray inductance. Validity of the turn-off model is further elaborated with the help of graphs shown in Sections 5.3.3 through 5.3.4. The measured diode voltage trajectory shows an insignificantly small overshoot of diode voltage as explained in [53].

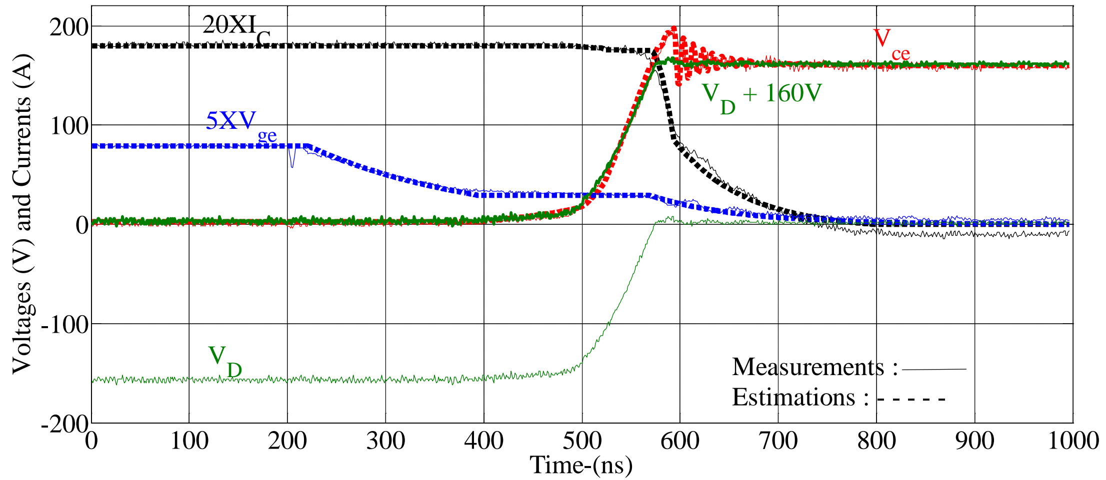
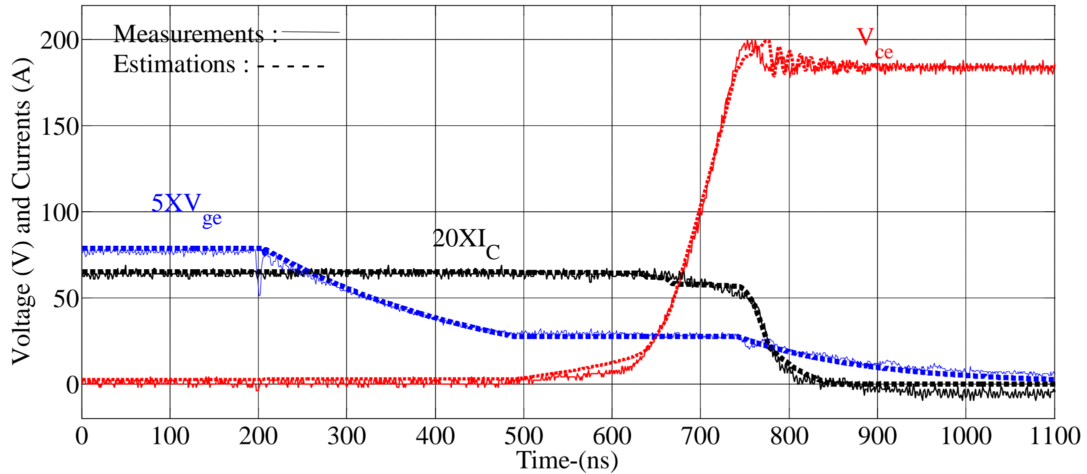


Figure 5-20- Turn-off transient of IRG6I320UPBF at V_{CC}=160V, I_L=9A, and R_G=70Ω

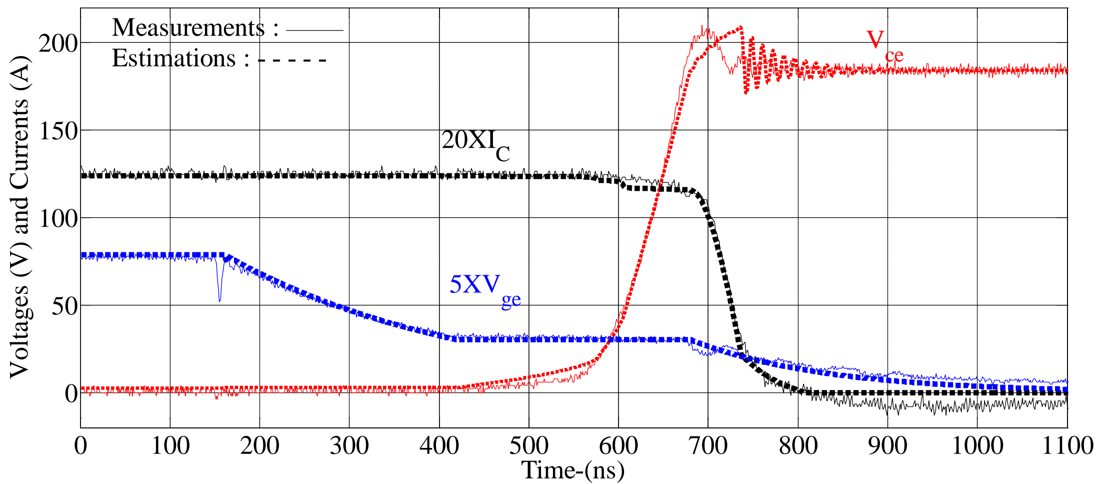
During the turn-off transient, power dissipation across the diode occurs only during the fast collector current falling period where there is an insignificantly small overshoot in diode voltage at finite current through the diode. However, measured amplitude and period of the overshot is very small as indicated in the Figure 5-20. Therefore, the energy loss in this part of the transient is negligible as stated in [14]. In order to retain the simplicity of the model and to avoid necessity of large set of parameters, this loss component is ignored as in [14], [21]. Model responses used in validation of the transient model depicts adequacy of the simple diode model. The ability to mimic switching behavior at a variation of operating point or model parameters is evaluated in the following sections. All measurements made with the freewheeling diode-ISL91560P2.

5.3.2 Effect of Load Current Changes

Load current changes affect the collector current falling phase as well as the collector-to-emitter voltage changing phase. Figure 5-21 (a) and (b) shows measured and estimated responses at two different load currents.



(a)



(b)

Figure 5-21-Turn-off transients of IRG6I320UPBF at V_{cc} =184V and R_G = 100Ω (a) I_L=3.25A (b) I_L=6.2A

The gate-to-emitter voltage plateau level determines the charge supply rate to the C_{gc}' or the rate of rise of the collector-to-emitter voltage. According to Equation 4-1, for a given

IGBT, the gate-to-emitter voltage plateau is determined by the load current. For the IRG6I320UPBF, estimated plateau voltage level shift is just 0.6V for a nearly 90% increase of load. The change in charging current is due to the changes of voltage across the gate resistance. For a gate drive high level voltage of 15.5V, the reduction of charging current is just 4% for a 90% increase in the load current. Thus the change in charging current with the load current change is not very significant due to the large gain of the IGBT. Therefore almost identical collector-to-emitter voltage rising trajectories can be observed despite of the load current changes depicted in Figure 5-21.

According to Equation 4-6, the instantaneous time rate of decreasing collector current during the fast current falling phase is determined by time rate of changing gate-to-emitter voltage and square of the distance of gate-to-emitter voltage from its plateau level. According to the Figure 5-21, the slope of the collector current trajectory gradually increases, reaches a stage where the slope remains more or less constant, and then starts to gradually decrease. The end of the constant collector current slope period cannot be easily identified with visual inspection, as evident from Figure 5-21.

5.3.3 Effect of Supply Voltage Changes

Figure 5-22 (a) and (b) compare the collector-to-emitter voltage rising trajectories when the supply voltage is at 148V and 180V respectively. The supply voltage level fixes the terminating point of the collector-to-emitter voltage rising trajectory. However, according to the proposed model, the shape of the collector-to-emitter voltage rising trajectory should not vary with the supply voltage at a fixed gate drive and for a given IGBT. Although load currents in the measurements are different (by about a 1A), the two observa-

tions are selected by considering the insignificant effect of load current changes on the collector-to-emitter voltage rising trajectory as explained in Section 4.3.

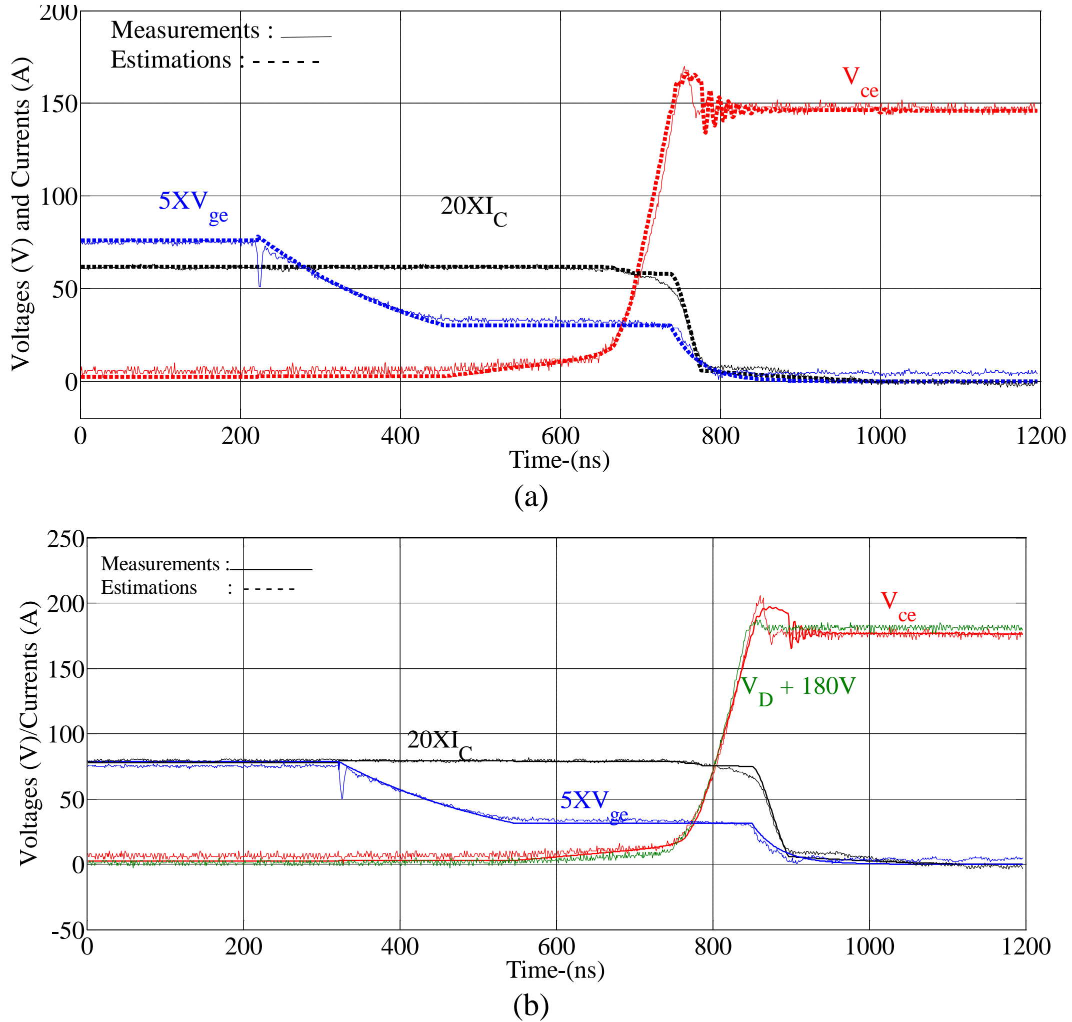
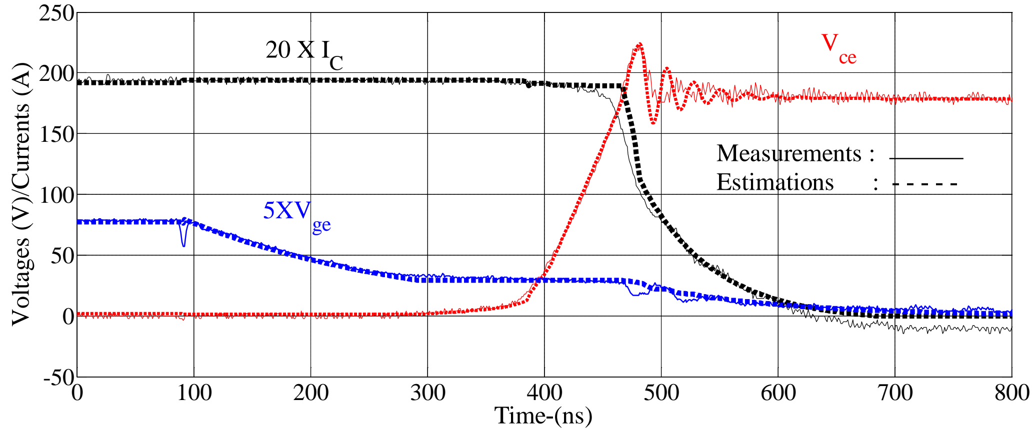


Figure 5-22- Turn-off transient of APT12GT60BR at R_G=100Ω (a) V_{cc}=148V and I_L=3A (b) V_{cc}=180V and I_L=4A.

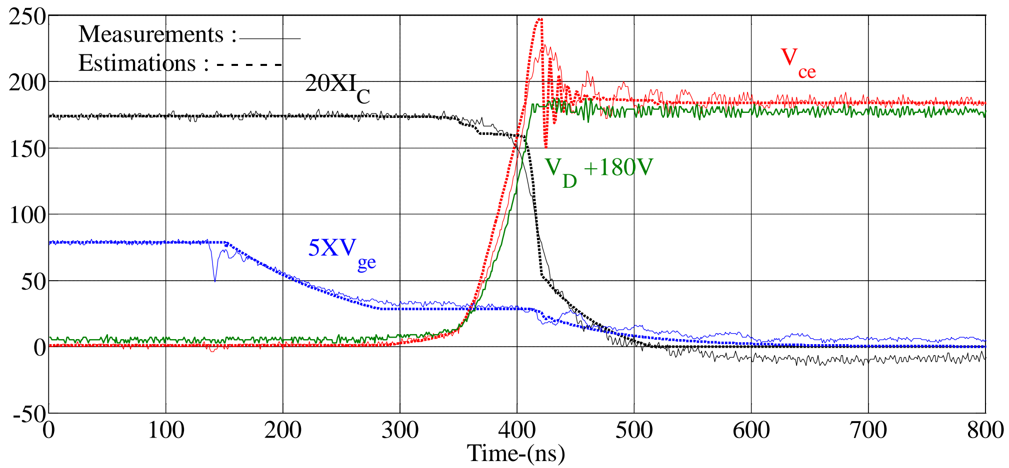
The measured diode voltage trajectories are also projected onto the collector-to-emitter voltage trajectories in the graphs (green curve). Correlation of estimated collector-to-emitter voltages with the measured diode voltage variations further validates the assumption of the domination of the IGBT dynamic over the diode behavior as explained in Section 5.3.1.

5.3.4 Effect of Gate Resistance Change

Figure 5-23 (a) and (b) demonstrate the validity of the model under changing gate resistance values. The gate resistance used in the measurement shown in Figure 5-23-(a) is half of that used in the measurement shown in Figure 5-23-(b).



(a)



(b)

Figure 5-23- Turn-off transient of IRG6I320UPBF at V_{cc} =184V (a) I_L= 9.75A and R_G =70Ω (b) I_L=8.6A and R_G =35 Ω

The effect is similar to the turn-on transient which is described in Section 5.2.5. The change in gate resistance alters the period of the collector-to-emitter voltage rising phase

due to changes in the charging current to the Miller capacitor. In addition, the period of collector current falling phases decreases when gate resistance is decreased as shown in Figure 5-23 (a) and (b). The amplitude of the collector-to-emitter voltage overshoot increases when gate resistance is decreased due to high slope of the collector current fall. The green trajectory in Figure 5-23 (b) depicts correlation of diode voltage with collector-to-emitter voltage.

5.3.5 Validation of Model under a Range of Operating Points

Figure 5-24 through Figure 5-27 compare the measured responses with the estimated response of the IRG6I320UPBF and freewheeling diode ISL91560P2 at different operating points. Again this comparison shows the ability to estimate the turn-off waveform at different operating conditions using a unique set of parameters.

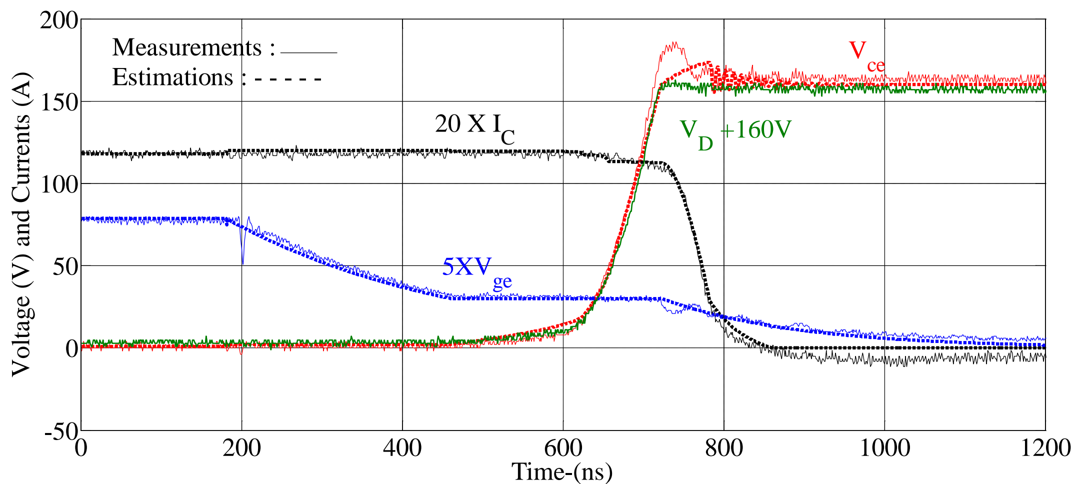


Figure 5-24- Turn-off transient of IRG6I320UPBF at V_{cc}=160V, I_L=6.25A, R_G=150Ω

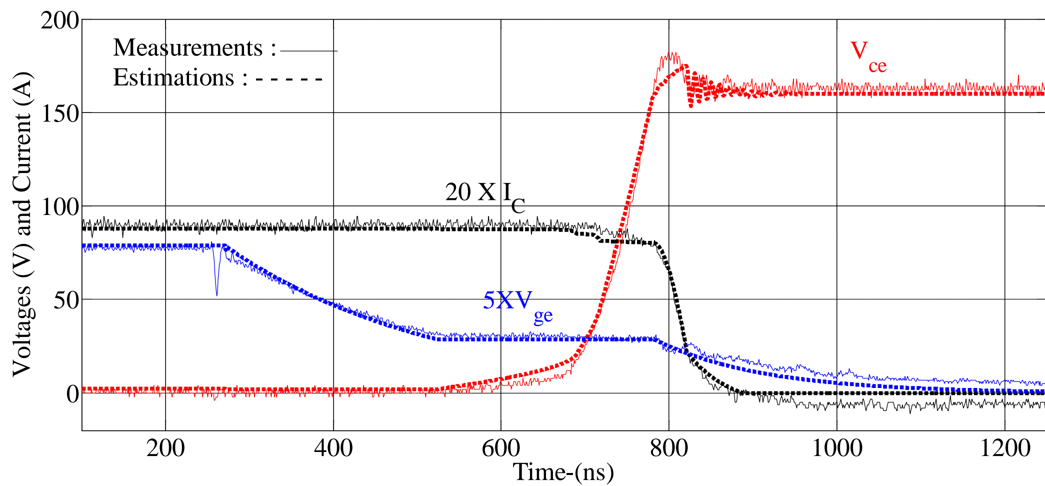


Figure 5-25- Turn-off transient of IRG6I320UPBF at V_{cc}=160V, I_L=4.5A, R_G=150Ω

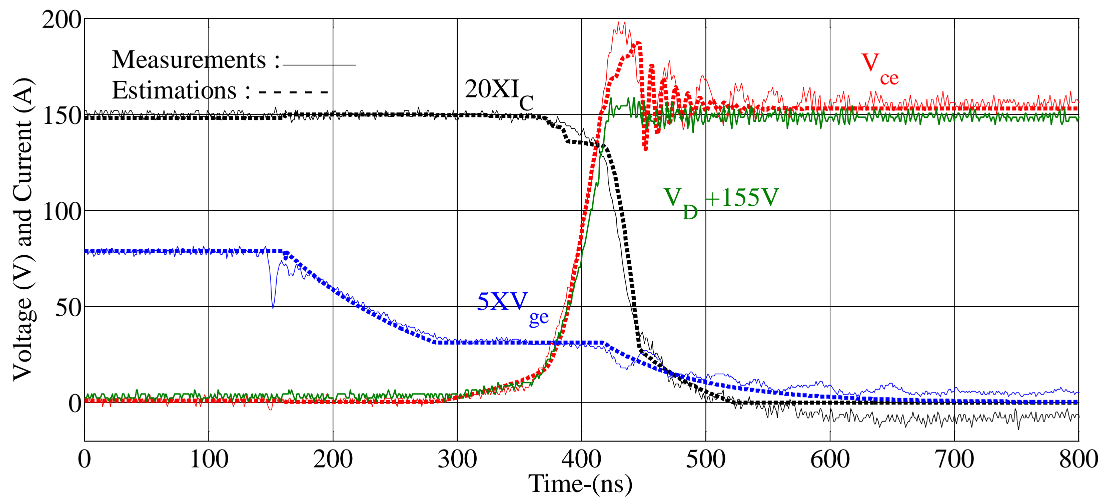


Figure 5-26- Turn-off transient of IRG6I320UPBF at V_{cc}=155V, I_L=7.5A, R_G=35Ω

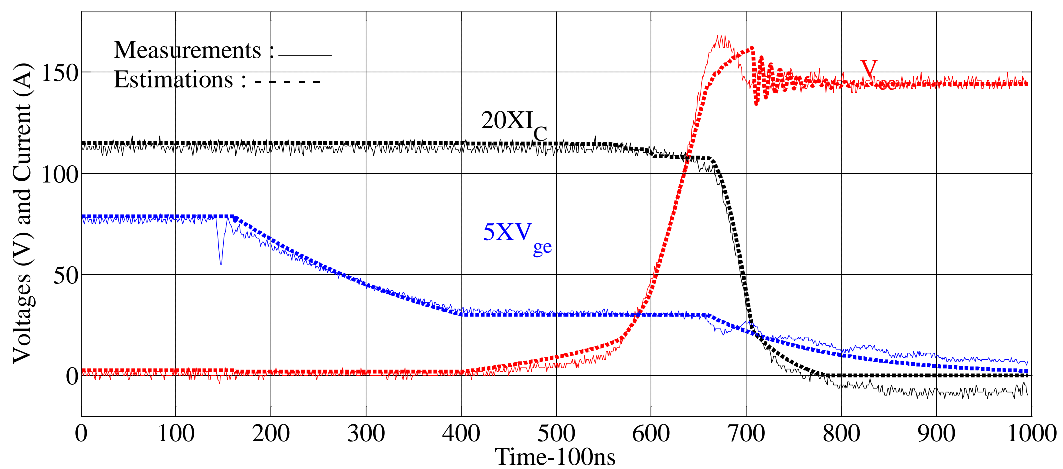


Figure 5-27- Turn-off transient of IRG6I320UPBF at V_{cc}=145V, I_L=5.75A, R_G=100Ω

5.3.6 A Comparison Collector-to-Emitter Voltage Trajectories of Turn-on and Turn-off Switching Transients

Figure 5-28 compares collector-to-emitter voltage changing trajectories at turn-on (Mirrored along the time axis) and turn-off transients.

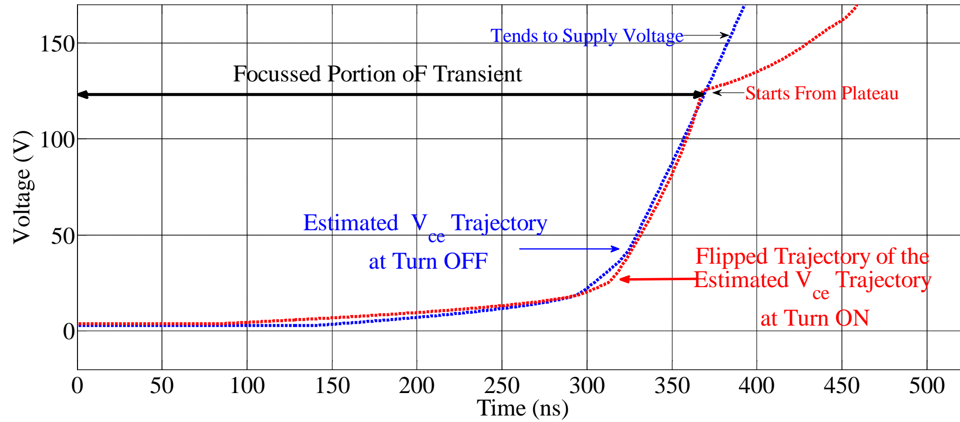


Figure 5-28-Switching transients of APT12GT60BR at 148V

According to the suggested model, the one and only reason for any discrepancy is the second component of current expressed in Equation 3-8. The component of current resulted via depleting stored charges in C_{ge} speeding up the collector-to-emitter voltage falling trajectory during the later reverse recovery phase in the turn-on transient. According to Section 3.2.5, the magnitude of this current component depends on the gate-to-emitter voltage drop or diode current trajectory during later reverse recovery phase. Figure 5-28 depicts close resemblance of collector-to-emitter voltage trajectories when the effect of the current supplied by depleting stored charges in C_{ge} is insignificant.

Chapter 6

Switching Loss Estimation

This chapter presents an evaluation of the accuracy of the estimated switching losses with the proposed turn-on and turn-off transient models, and a discussion of the characteristics of the switching energy losses during turn-on and turn-off switching transients. The chapter also presents an approach for estimation of switching losses through electromagnetic transient simulations using a lookup table constructed with the energy losses estimated from the proposed transient models.

6.1 Loss Estimation Performances of the Switching Transient Models

A model of the IRGP4072DPBF IGBT is created in PSCAD and the model parameters are set to the estimated values listed in Section 5.2.1. Loss estimation performance is evaluated at different load currents and supply voltages to evaluate the accuracy of switching loss estimation under different operating conditions. Table 6-1 compares the measured and estimated values of turn-on switching losses.

Table 6-1-Loss estimation performances for turn-on transient model evaluated with IRGP4072DPBF at R_G=100Ω

V_{CC} (V)	I_L(A)	Turn-on Switching Loss		Accuracy (%)
		Measured (μJ)	Estimated (μJ)	
190	7	86	88	97.7
190	5.5	69	68	98.6
190	3.85	45.5	45.9	99.1
170	7.3	70.9	75.5	93.5
170	3.3	31.1	32.8	94.5
150	6.5	55.5	58.0	95.5

The average energy E_{ave} loss between two sampling points n and $n+1$ of the measured transient waveform is calculated with Equation 6-1.

$$E_{ave} = \frac{(V_{ce}^{n+1} - V_{ce}^{n})}{2}\frac{(I_c^{n+1} - I_c^{n})}{2}T_s \qquad 6\text{-}1$$

where V_{ce}^{n+1} and V_{ce}^{n} are respectively the measured collector voltages at the next and present sampling points. I_c^{n+1} and I_c^{n} measured collector currents at the next and present sampling points. The total switching loss of the measured transient is calculated by adding all individual average energy loss components over the switching transient period. Table 6-1 shows that estimated switching loss values are very close to the experimentally measured values. Accuracy of estimation remains above 93% in all test cases despite the changes in operating point.

A number of IGBTs having different voltage and current ratings are selected for further validation of switching loss calculation models. Table 6-2 gives loss estimation accuracy for four different IGBTs at randomly selected operating points. The turn-on switching

losses of the different IGBTs are different and device dependent. However, regardless of the IGBT used, highly accurate estimations of the switching losses can be obtained with the proposed model when the model parameters are accurately estimated.

Table 6-2- Estimated turn-on switching loss for different IGBTs

IGBT	V_{CC} (V)	R_G (Ω)	I_L(A)	Measured (μJ)	Estimated (μJ)	Accuracy (%)
IRG4BC20WPBF	180	150	6.5	56.0	55.2	98.6
G4PC30FBPF	160	150	4.25	35.7	34.2	95.8
APT12GT60BR	140	150	5.5	78.6	77.0	98.0
IRG6I320UPBF	140	150	4.25	31.9	30.0	94.0

Table 6-3 compares the measured and estimated turn-off switching losses for a few IGBTs evaluated using the proposed turn-off transient model. The table shows an accuracy level comparable to that of the turn-on switching model.

Table 6-3-Estimated turn-off switching losses of few IGBTs

IGBT	V_{CC} (V)	R_G (Ω)	I_L (A)	Measured (μJ)	Estimated (μJ)	Accuracy (%)
IRG4BC20WPBF	180	70	4.8	106.0	107.2	98.8
APT12GT60BR	178	70	3.9	55.8	60.6	91.3
IRG6I320UPBF	180	100	3.15	48.3	50.7	95.0

Turn-off switching losses are estimated for a selected IGBT at random load currents and supply voltage levels. According to Table 6-4, the accuracy of the estimated turn-off switching loss is less at lower supply voltages. Reduced accuracy of the estimated losses at lower supply voltages may be attributed to use of fixed values for the Millar capacitance in the phases where IGBT is presumed to operate at higher collector voltages. At low supply voltages this assumption may be violated, especially when stray inductance is high, resulting in increased errors in the estimated energy losses. The accuracy of estimating turn-off switching losses is generally lower when compared with the accuracy of turn-on loss estimations. However, accuracy of the estimated losses is adequate for most of the operating points. Table 6-1 through Table 6-4 shows the capability of the proposed IGBT turn-on and turn-off transient models to represent the switching behavior at different operating conditions. Table 6-4 shows the accuracy of the estimated turn-off switching loss for the IRG6I320UPBF.

Table 6-4-Loss estimation performances for turn-off transient of IRG6I320UPBF

V_{CC} (V)	I_L(A)	R_G (Ω)	Turn-off Switching Loss		Accuracy (%)
			Measured (μJ)	Estimated (μJ)	
180V	9.65	70	155.0	159.2	97.8
180V	6.30	100	114.8	104.2	90.8
160V	9.00A	70	122.1	126.0	96.8
160V	4.4A	100	47.7	53.6	87.6
150V	6.5A	35	35.1	44.2	74.1
144V	5.75	100	61.4	67.7	89.8

According to Table 6-4, the accuracy reduces at smaller gate resistances. The induced emf across the emitter inductance of the IGBT due to changes in collector current reduces the effective gate-to-emitter voltage applied to the IGBT. This is not accounted for in the model as the emitter stray inductance is lumped in the total path stray inductance to simplify the model. Impact of such simplifications becomes significant at very fast collector current changes that happen at smaller gate resistances. The accuracy of IGBT gain estimations can also be affected by the emitter inductance. In fact, the differences observed in the IGBT gain in different phases could be an artifact resulting from the emitter inductance.

6.2 Loss Characteristics

Understanding of the switching loss behavior is important as it helps IGBT selection, gate drive design, and helps for accurate modeling of the loss behavior.

6.2.1 Turn-on Loss Behavior

Variation of switching losses with the load current and supply voltage is one important loss behavior. Figure 6-1 shows the variation of the estimated turn-on switching loss of IRG4BC20WPBF evaluated at V_{cc}=180V and R_G=150Ω. According to Figure 6-1, switching loss increases nonlinearly with the load current.

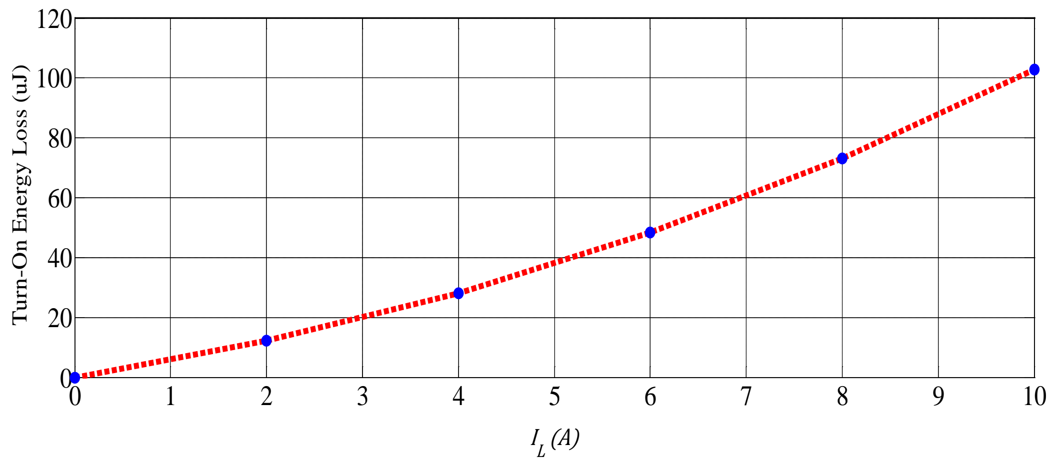


Figure 6-1-Load current versus turn-on switching loss

Figure 6-2 shows the variation of the estimated turn-on switching loss with the supply voltage of the unit cell for IRG4BC20WPBF when I_L=5A and R_G=150Ω. Again, the turn-on energy loss nonlinearly varies with the supply voltage.

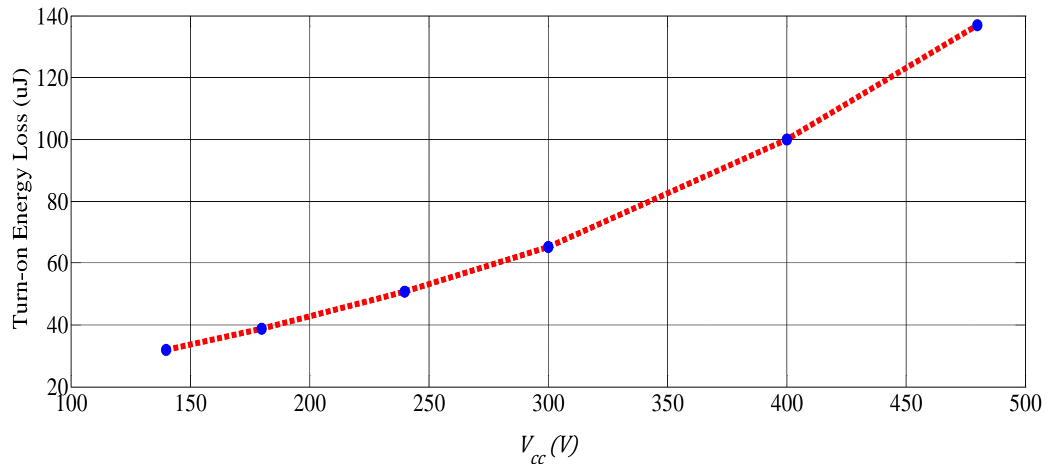


Figure 6-2-Supply voltage versus turn-on switching loss

The proportion energy of loss occurring in each phase is determined by the instantaneous power dissipation during the phase and the duration of the phase. Figure 6-3 shows instantaneous power dissipation and energy loss through the IRG4BC20WPBF evaluated at V_{cc} =180V, R_G = 150Ω, and I_L=6.6A. Power and energy curves are scaled-up by a factor of 1.35 for ease of comparison. According to Figure 6-3, the power dissipation curve fol-

lows the collector current variation during the collector current rising phase.

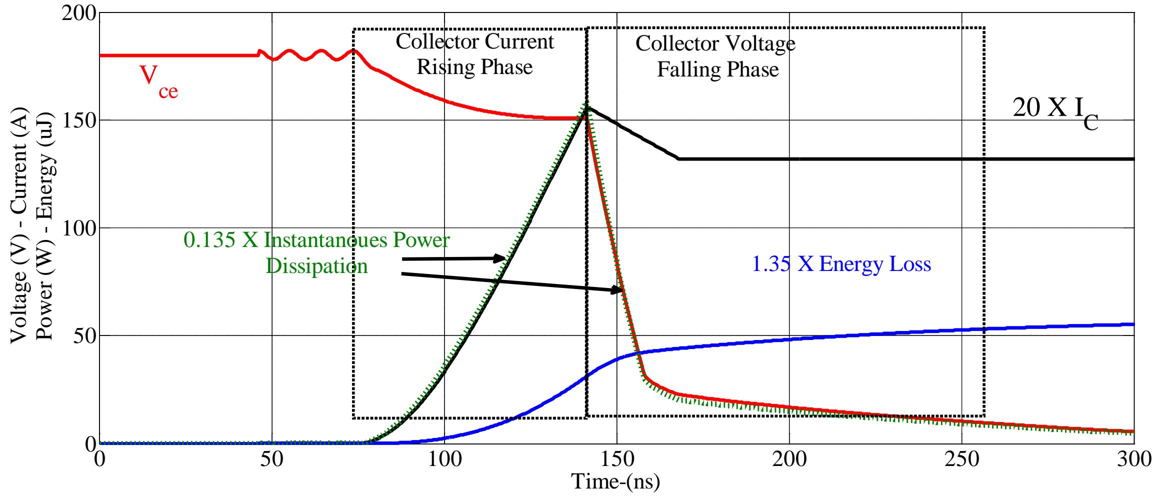


Figure 6-3-Typical loss behavior of turn-on switching transient

Conversely, the power dissipation curve follows the variation of the collector-to-emitter voltage trajectory during collector-to-emitter voltage falling phase. Therefore, under a given operating condition (switching current/supply voltage), energy loss during the collector current rising phase can be approximately determined by Equation 6-2 with an adequate level of accuracy.

$$E_{I_Rise} \cong k_v V_{cc} \int_{0}^{T_{I_Rise}} I_c(t)\, dt \qquad 6\text{-}2$$

where E_{I_Rise} is the energy loss during the collector current rising phase, k_v is the ratio between average collector-to-emitter voltage during the phase and the supply voltage V_{cc}, T_{I_Rise} is the period of the collector current rising phase.

Likewise the energy loss during the collector-to-emitter voltage falling phase can be approximately determined by Equation 6-3.

$$E_{V_Fall} \cong k_i I_L \int_{t_0}^{T_{V_Fall}} V_{ce}(t)\, dt \qquad 6\text{-}3$$

where E_{V_Fall} is the energy loss during the collector-to-emitter voltage falling phase, k_i is the ratio between the average collector current during the phase and load current I_L (This constant approximately equals 1 if I_{RM} is smaller compared to I_L), T_{V_Fall} is the period of the collector current rising phase.

However, the ratio between E_{I_Rise} to E_{V_Fall} is not constant and depends on many external parameters such as stray inductance as well as the parameters of the IGBT. Table 6-5 shows estimated proportions of energy losses during the collector current rising phase and the collector-to-emitter voltage decreasing phases of the turn-on transient. The current ratings shown in the table are continues current ratings at 100° C.

Table 6-5-Estimated proportions of the energy loss in different phases for a few IGBTs

IGBT	Rating	R_G=50Ω		R_G=100Ω	
		I_c Rising Phase (%)	V_c Falling Phase (%)	Ic Rising Phase (%)	V_c Falling Phase (%)
IRG4BC20WPBF	600V/6.5A	70.4	29.6	74.7	25.3
IRG6I320UPBF	330V/16A	60.4	39.6	67.2	32.8
G4PC30FBPF	600V/17A	52.3	47.7	57.8	42.2
APT12GT60BR	600V/12A	36.7	63.3	38.3	61.6
IRGP4072DPBF	300V/40A	50.8	49.2	56.2	43.8

The above estimations are done when supply voltage is 190V and load current of 9A. For a given gate resistance, energy loss during the collector current rising phase is dependent on the gate-to-emitter capacitance C_{ge}, gate-to-emitter threshold voltage level V_T, gain of

the IGBT, and the value of the Miller capacitance at larger collector-to-gate voltage. These parameters are different for various IGBTs. For accurate loss modeling, switching behavior of the specific IGBT should be taken in to account or the model should include behavioral parameters of the IGBT. Energy loss during the collector-to-emitter voltage decreasing phase determined by the Miller capacitance profile, gate voltage threshold level, and gate-to-emitter voltage plateau level which is determined by the trans-conductance. The variation of the above ratio indicates that specific behavior of an IGBT cannot be ignored in loss estimation. Therefore, accurate loss estimation must rely on behavioral parameters of the specific IGBT.

6.2.2 Turn-off Loss Behavior

The behavior of the tail current is an important characteristic of the turn-off switching event. Table 6-6 compares the measured total energy loss during the turn-off switching event with the energy loss during the tail current period for the IRG6I320UPBF at different operating conditions. According to Table 6-6, energy losses during the tail current period increase with the load current. The amplitude of the initial tail current is said to equal to about one tenth of the initial collector current in normal operating condition of the IGBT [14].

Table 6-6-Fraction of energy loss during tail current period

I_L(A)	V_{CC} (V)	R_G (Ω)	Turn-on Switching Loss		Percentage of Tail Loss (%)
			Measured Total Loss (μJ)	Measured Tail Loss (μJ)	
9.65	180	70	155.0	45.8	29.5
7.7	184	70	139.6	14.0	10.0
8.6	184	35	86.7	9.8	11.3
6.30	180	100	114.8	8.5	7.4
9.0	160	70	122.1	41.8	34.2
7.5	150	35	58.5	6.8	11.6
6.5	150	35	35.1	5.0	14.2
5.75	144	100	61.4	4.7	7.7
3.1	146	70	41.2	7.4	18.0

Figure 6-4 shows the estimated instantaneous power curve and energy variation for IRG6I320UPBF at V_{cc} =180V, R_G = 70Ω, and I_L=9.65A plotted with the collector-to-emitter voltage and collector current trajectories.

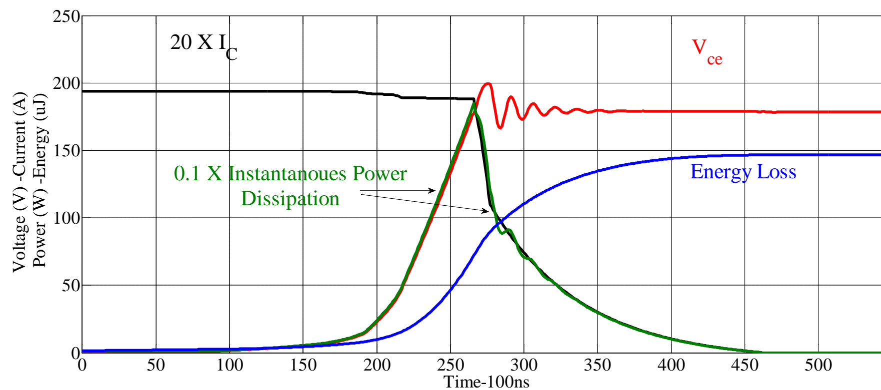


Figure 6-4-Typical loss behavior of turn-off switching transient

Similar to the turn-on transient, a strong correlation between the collector-to-emitter voltage trajectory and the power dissipation curve can be observed during the collector-to-emitter voltage rising phase. Furthermore, the power dissipation curve is strongly correlated with the collector current trajectory during the collector current falling phase. Therefore, energy loss can be estimated with the help of two equations in the form of Equations 6-1 and 6-2.

6.3 Interpolation and Lookup Table Based Loss Estimation

It is not feasible to run transient models at each switching instant in an EMTP like simulation environment as it raises the computational requirement unnecessarily. Therefore, it is suggested to use a lookup table during simulation of power converters embedded in large power systems. The proposed switching transient models can be used to calculate the entries of the lookup table. A table can be created with suitable dimensions considering the expected range of currents and voltages (including the transient currents/voltages). Intervals of the lookup table can be determined as a tradeoff between the expected accuracy and the allowable time for creation of the lookup table. The lookup table can be created during compilation of a simulation case (similar to T-line and Cable modules in PSCAD) and interpolation can be used during the retrieval of the data. Pre- and post-switching IGBT current and voltage at a switching event can be obtained from the EMTP simulation of the electrical circuit with ideal switches as described in [14]. An example of a lookup table is shown in Table 6-7. Here, the energy losses estimated with

the turn-on transient model of the IRG4BC20WPBF are used to create the table. Turn-on switching losses at some random operating points are estimated applying linear interpolation to Table 6-7. The units of switching losses shown in Table 6-7 is μJ.

Table 6-7-Lookup table for turn-on energy loss of IRG4BC20WPBF

	V_{cc} (V)					
I_L (A)	140	180	240	320	400	480
2	10.0	12.2	16.8	25.6	37.4	52.0
4	23.2	28.3	37.1	54.1	77.4	106.6
6	40.6	48.3	61.8	86.8	122.2	166.7
8	62.6	72.8	91.0	123.5	170.5	230.0
10	90.6	102.7	125.6	166.7	224.9	300.6

Turn-on energy losses estimated using the lookup table model are compared with the energy losses estimated using the turn-on transient model in Table 6-8. The last column of the table shows estimation error due to use of linear interpolation/extrapolation between the points. Although use of a lookup table adds an additional error to the estimation, error percentages are very small according to the Table 6-8. The units of switching losses shown in Table 6-8 is μJ. However, the lookup table model can drastically reduce the CPU time. For example, if the switching transient models are used estimate switching losses for a period of 5s in a three-phase converter switched at 1.8kHz, 54000 loss estimations need to be done for turn-on switching loss estimation during the simulation (1800 switching events per switching cell per seconds × 6 switching cells × 5 s).

Table 6-8- Errors of the losses estimated using the lookup table

I_L (A)	V_{cc} (V)	Table	Est.	Error (%)
2.75	220	22.4	21.4	4.4
2.75	440	62.4	61.4	1.6
6.95	220	70.4	69.4	1.4
6.95	440	170.9	170.0	0.5
13	220	177.4	167.5	5.9
13	440	361.5	356.5	1.4

An unacceptably long time will be taken to create such a large number of estimations via simulating of transient models. If the lookup table approach is used with a 5X6 table, the transient model has to be run only 30 times (turn-off model also needed to run 30 times) to create the table. Time taken to make an estimation with a table model is insignificantly small when compared with the simulation period of the transient model. Therefore, the addition of a small error shown in Table 6-8 is offset by a speed up factor of 54000/30. Furthermore, the transient model is required to run only five times for the two level converters as voltage is fixed in two level converters. Therefore, the lookup table approach offers good accuracy and lower CPU time when compared with other approaches. The variation of switching losses with temperature can be represented with the same approach as explained below. Variation of the temperature of the IGBT with the power dissipation can be modeled with a thermal model as explained in [14]. Switching losses can be estimated at different operating temperature levels at different operating conditions. The var-

iation of switching loses with temperature can be represented with another column in the table as in [13]. Reflection of losses through the converter to the EMT environment is important to obtain an accurate network solution to the power system which contains the converter. This can be done by adjusting the saturation voltage that represents the conduction loss and leakage current representing the blocking loss as explained in [14]. In addition, the estimated losses can be injected to the network with a single controlled voltage source as explained in [54]. Collector-to-emitter voltage variation during the collector-to-emitter voltage changing phases is solely determined by the change in the voltage across the Miller capacitance. Change in the voltage across Miller capacitance is solely determined by the charging current which is fixed during the turn-off transient. The charging current is dependent on the gate-to-emitter voltage plateau which is only dependent on load current. Increase in the charging current by a factor k causes the duration of this phase to decrease by a factor of 1/k at a fixed supply voltage. Therefore, for a given IGBT in a given converter, the result of the integration shown in Equation 6-2 decreases by a factor of 1/k. Therefore, loss during the phase decreases by a factor of 1/k. If an expression for the change in charging current with the load current is found, it is possible to estimate the energy loss during the collector-to-emitter voltage rising phase in the turn-off switching event just with the help of a algebraic function. However, one switching loss measurement or estimation during the collector to emitter of the converter is needed for this approach. The approach is applicable to the collector-to-emitter voltage falling phase, when I_{RM} is much less than the load current or with a compensation term at higher I_{RM}. Many references explain that the collector current trajectory increases approximately in a linear fashion. This is confirmed in this thesis. If it is possible to determine

the slope of the collector current trajectory during the turn-on transient, an algebraic function can be used to determine loss during collector current rising phase. Loss characteristics found in this work emphasize that possibility of using algebraic function to very efficiently estimate the switching losses. This approach is different from the published work as it is associated with the dynamic behavior of the unit cell. Furthermore, equations are applied to distinct phases for a given unit cell rather than the whole switching transient or both switching transients together.

6.4 Sensitivity of the Estimated Turn-on Switching Loss to the Model Parameters

The impact of inaccurate estimation of model parameters on accuracy of estimated switching loss is evaluated by calculating the deviation of the estimated switching loss with the model parameters. Table 6-9 shows the estimated turn-on switching loses and expected error that resulted from a ±15% and a ±30% errors in estimating stray inductance L_S. The seventh column in the table shows estimated switching loss at the normal stray inductance. According to Table 6-9, the estimated switching loss is an under estimation if the stray inductance is an overestimation and vice versa. Furthermore, error increases with the load current while the error decreases with the increasing supply voltage. This is as expected.

Table 6-9-Expected error in turn-on energy loss due to inaccurate estimation of L_S

V_{CC} (V)	I_L (A)	-30% (134.4nH)		-15% (163.2nH)		0 192nH	+15% (220.8nH)		+30% (249.6nH)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)	E_{Sw}	E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)
150	3.5	32.5	8.3	31.2	4	30.0	28.9	-3.7	27.9	-7
150	7	70.6	10.7	67.1	5.2	63.8	60.7	-4.9	57.9	-9.2
190	3.5	44.3	6.7	42.8	3.1	41.5	40.2	-3.1	39.0	-6.0
190	7	95.7	8.8	92.0	4.5	88	84.7	-3.7	81.3	-7.6

A typical upper bound on the error in estimating stray inductance is less than 30%. Hence, the maximum expected error due to uncertainty in stray inductance can be considered less than 10%.

The estimated turn-on switching loses and the expected percentage error due to error in estimating the maximum reverse recovery current, I_{RM}, is given in Table 6-10.

Table 6-10-Expected error in turn-on energy loss due to inaccurate estimation of I_{RM}

V_{CC} (V)	I_L (A)	-50%			0		+150%		
		I_{RM} (A)	E_{Sw} (μJ)	Error (%)	I_{RM} (A)	E_{Sw} (μJ)	I_{RM} (A)	E_{Sw} (μJ)	Error (%)
150	3.5	0.4	29.6	-1.3	0.8	30.0	2.1	33.3	11.0
150	7	0.7	63.6	-0.3	1.4	63.8	3.5	70.1	9.9
190	3.5	0.4	40.8	-1.6	0.8	41.5	2.1	45.7	10.1
190	7	0.7	87.9	-0.1	1.4	88	3.5	96.5	9.7

The model input is the measured maximum reverse recovery current at a given test condition. According to the data sheet, measured maximum reverse recovery current of the ISL91560P2 is 3.5A when the load current is 15A and the cut-off rate is 200A/μs. Therefore, sensitivity is calculated for the percentage change of this measured maximum reverse recovery current. Columns 3 to 5 in Table 6-10 indicate respectively the estimated maximum recovery current, estimated turn-on switching loss, and percentage error when this input is 1.75A. Columns 8 to 10 correspond to 8.75A of the measured reverse recovery current. According to Table 6-10, deviation of the estimated turn-on switching loss caused by an error in this input is small.

Table 6-11 shows the expected error due to inaccurate determination of the gate threshold voltage. Accuracy of the estimated switching loss is more sensitive to inaccuracies in gate voltage threshold as evident in Table 6-11. Thus high sensitivity to threshold voltage is results from the square relationship between the gate-to-emitter voltage and the collector current.

Table 6-11-Expected error in turn-on energy loss due to inaccurate estimation of V_T

V_{CC} (V)	I_L (A)	-20% (4.16V)		-10% (4.68V)		0	+10% (7.72V)		+20% (6.24V)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)	E_{Sw}	E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)
150	3.5	26.5	-11.6	28.2	-6.0	30.0	32.0	6.6	34.4	14.7
150	7	55.7	-12.7	59.5	-6.7	63.8	68.7	7.7	74.3	16.4
190	3.5	36.9	-11.1	39.0	-6.0	41.5	44.2	6.5	47.3	14.0
190	7	77.5	-11.9	82.5	-6.3	88	94.7	7.61	102.5	16.4

The estimated switching loss is more inaccurate at higher load currents as inaccurate estimation of the threshold voltage causes larger inaccuracies in the estimated collector current.

Table 6-12 shows the errors in the estimated turn-on switching loss due to inaccurate estimation of the gain.

Table 6-12-Expected error due to inaccurate estimation of adjusted gain

V_{CC} (V)	I_L (A)	-30% (0.84)		-15% (1.02)		0 1.2	+15% (1.38)		+30% (1.56)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)	E_{Sw}	E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	Error (%)
150	3.5	32.8	9.3	31.2	4	30.0	29.0	-3.3	28.3	-5.7
150	7	72.7	13.9	67.7	6.1	63.8	60.9	-4.5	58.4	-8.46
190	3.5	44.7	7.7	43.0	3.6	41.5	40.3	-2.9	39.3	-5.3
190	7	99.5	13.0	93.0	5.7	88	84.6	-3.9	82.0	-6.8

The impact of inaccurate estimation of the adjusted gain is significant at higher load currents and it is less severe at higher supply voltages than lower supply voltages.

6.5 Sensitivity of the Estimated Turn-off Switching Loss to the Model Parameters

Table 6-13 shows a change in the estimated turn-off switching energy loss due to inaccuracies of estimating the stray inductance. According to Table 6-13, inaccuracy of estimating stray inductance has no significant effect on the turn-off switching loss estimation.

Table 6-13-Errors in turn-off switching energy due to variations in the stray inductance

V_{CC} (V)	I_L(A)	-30% (129.8nH)		0 185.4nH	+30% (241.0nH)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	E_{Sw} (μJ)	Error (%)
180	12	188.6	-1.9	192.2	195.7	1.8
180	6	99.7	-0.9	100.6	101.5	0.9

Table 6-14 and Table 6-15 show the change in estimated turn-off switching energy loss due to inaccuracies in the gate threshold voltage and the gain of the IGBT respectively.

Table 6-14-Error in turn-off energy loss estimation due to changes in the gate threshold voltage

V_{CC} (V)	I_L (A)	-10% (3.69V)		0 (4.1V)	+30% (5.33V)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	E_{Sw} (μJ)	Error (%)
180	12	192.9	0.4	192.2	195.3	1.61
180	6	102.3	1.7	100.6	105.6	5.0

Table 6-15-Error in turn-off energy loss estimation due to changes the gain

V_{CC} (V)	I_L (A)	-30% (3.76)		0 (5.37)	+30% (6.98)	
		E_{Sw} (μJ)	Error (%)	E_{Sw} (μJ)	E_{Sw} (μJ)	Error (%)
180	12	201.1	4.6	192.2	186.4	-3.0
180	6	102.0	1.3	100.6	99.6	-0.9

According to the tables, the accuracy of the turn-off switching energy loss estimation is not significantly affected by the inaccuracies in the gain characteristics of the IGBT. Sensitivity analysis indicates that small inaccuracies in the estimated model parameters do not result in large errors in both turn-on and turn-off energy losses. Estimated energy losses are more sensitive to the gate threshold voltage, in comparison to various other parameters in the developed switching loss model.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

The following conclusion can be drawn from the detailed study conducted in this thesis.

7.1.1 Understanding of Switching Behavior of the Unit Cell

A comprehensive understanding of the behavior of the switching cell during the turn-on and turn-off transients was achieved through an in-depth literature survey and experimental measurements at the laboratory.

- ✓ Overall switching behavior of the switching cell is determined by the internal dynamics of the IGBT as well its interaction with the external circuit.
- ✓ Both turn-on and turn-off switching events of the unit cell follow a number of distinct phases. The causes for the distinct behaviors in each phase were clearly identified.

- ✓ It is possible to characterize the dominant processes and interactions in each of these distinct phases in switching transients using a circuit model.
- ✓ The behavioral modeling of the switching cell using a circuit model is an appropriate approach for switching loss estimation through EMT type simulations.

7.1.2 Circuit Based Switching Transient Modeling

Two detailed circuit models were developed to simulate turn-on and turn-off transients of a switching cell of a VSC. A detailed procedure was developed to extract model parameters from a test waveform. The ability of the developed circuit models to simulate the terminal behavior of an IGBT in a unit switching cell during the switching events was verified.

- ✓ In order to correctly simulate the turn-on event, the transient period needs to be divided into five phases. However, modeling of turn-off transient requires only four phases. This additional phase in the turn-on transient is required to take into account two phases in the freewheeling diode revers recovery current.
- ✓ Accurate simulation of the turn-on transient requires modeling of the diode revers recovery process. The simple freewheeling diode model presented in this thesis was found to be adequate to approximately model the reverse recovery process.

7.1.3 Model Parameter Extraction Procedures

The parameter extraction process is challenging but very important to enhance the accuracy and usability of the model.

- ✓ The parameters such as L_s, $k_p(1+\beta)$, and C_{ge} can be directly extracted from the measured switching waveforms.
- ✓ Identification of some parameters such as C_{gc} at higher collector-to-emitter voltages and the fictitious Miller capacitance C'_{gc} can be challenging due to noise in the waveforms.

7.1.4 Nonlinear and Variable Nature of the Parameters

Some parameters in the circuit models are nonlinear and vary during the switching event. However, consideration of the variable nature of the parameters is essential for an accurate simulation of the switching event.

- ✓ Square law of the gain described by Equation 3-1 more accurately represents the transfer characteristics of the IGBT.
- ✓ The value of IGBT gain during Phase-2 and Phase-3 of the turn-on transient is significantly less than the gain observed in the other phases.
- ✓ Consideration of the variable nature of the collector-to-emitter capacitance C_{gc} during collector-to-emitter voltage changing phase is essential to successfully simulate the collector-to-emitter voltage trajectory. However, C_{gc} can be considered as constant for phases in which the collector-to-emitter voltage remains high.
- ✓ Although the gate-to-emitter capacitance C_{ge} is varying, it is adequate to represent it using only two distinct values.

7.1.5 Performances of the Circuit Model

Numerous experimental measurements with several different IGBTs verified the capability of the developed models to accurately simulate the switching waveforms as well as the switching energy losses.

- ✓ A good correlation between the estimated waveforms and measured waveforms could be observed.
- ✓ A worthy level of accuracy of the estimated switching loss could be observed when compared to the estimated and measured switching energy losses.

Under certain operating conditions, variation of the instantaneous power dissipation closely resembles the instantaneous collector current variation during the collector current changing phases; and the instantaneous power dissipation curve closely resembles the collector-to-emitter voltage trajectory during the collector-to-emitter voltage changing phases, in both turn-on and turn-off transients. This property may be utilized to simplify the switching energy loss estimation.

7.2 Future Work

A number of new directions for future research are found during the study. The following extensions and studies are identified as most promising.

Although the proposed model is more accurate when compared with the published circuit models, it contains many model parameters that need to be determined using test waveforms. If possible, reduction of the number of model parameters without significant im-

pact on the accuracy is identified as an important way to enhance the usability of the proposed IGBT switching models.

Energy loss estimation during different phases can be simplified using the properties explained in Section 6.2. Investigation of the possibility of developing a set of algebraic equations to characterize the loss behavior during the collector current rising/falling phases and the collector-to-emitter voltage rising/falling phases will be an important contribution.

The collector-to-emitter voltage plateau level can become significantly small in the converters having high stray inductance. In such converters, there is a possibility for the IGBT to operate in the voltage dependent zone of the Miller capacitance during phases 2 and 3 in the turn-on transient. Therefore, it is required to investigate whether a nonlinear capacitor model is needed in these two phases to make simulation of the turn-on transient accurate in the converters with higher stray inductance.

In practical applications, the temperature of the IGBT varies with time due to load variations as well as changing ambient conditions. According to literature, IGBT gain, gate-to-emitter threshold voltage, and the reverse carrier life-time of the freewheeling diode are highly temperature dependent. Incorporation of the electro-thermal behavior by estimating changes in the temperature and hence the changes in the model parameters are essential extensions.

The switching transient models proposed in this thesis considered hard switching of inductive loads. Extension of the proposed circuit based switching transient modeling approach to cover different soft switching techniques and other devices is another direction of research.

Appendix-A

Estimated Parameters for a few IGBTs

A.1 APT12GT60BR

Estimated values of the parameters for APT12GT60BR are shown in Table A-1 through Table A-3.

Table A-1-List of estimated parameters for APT12GT60BR

Parameter	Estimated Value	Units
$k_p(1+\beta)$	1.21	A/V^2
k_{g_adjust}	0.2	None
C_{ce}	25	pF
C_{ge_ON}	0.509	nF
C_{ge_OFF}	0.5	nF
C_{gc}	30	pF

Table A-2-Estimated fictitious Miller capacitances of APT12GT60BR for turn-on

V_{ce} (V)	400	100	50	25	15	10	2
$C_{gc'}$ (pF)	18	25	40	80	100	1500	2800

Table A-3-Estimated fictitious Miller capacitances for APT12GT60BR for turn-off

V_{ce} (V)	300	45	35	20	15	10	0
$C_{gc'}$ (pF)	50	70	120	150	900	1800	3000

A.2 IRG6I320UPBF

The estimated values of parameters for the IGBT-IRG6I320UBF are shown in Table A-4 through Table A-6.

Table A-4-List of estimated parameters for IRG6I320UPBF

Parameter	Estimated Value	Units
$k_p(1+\beta)$	5.37	A/V^2
k_{g_adjust}	0.098	None
C_{ce}	20	pF
C_{ge_ON}	0.852	nF
C_{ge_OFF}	1.3	nF
C_{gc}	12	pF

Table A-5-Estimated fictitious Miller capacitances of IRG6I320UPBF for turn-on

V_{ce} (V)	400	100	65	30	15	10	0
$C_{gc'}$ (pF)	10	15	20	50	125	600	1000

Table A-6-Estimated fictitious Miller capacitances for IRG6I320UPBF for turn-off

V_{ce} (V)	300	45	35	20	15	10	0
$C_{gc'}$ (pF)	40	60	120	150	600	900	1400

A.3 IRGP4072DPBF

The estimated values of parameters for the IGBT-IRG6I320UBF are shown in Table A-4 through Table A-6.

Table A-7-List of estimated parameters for IRGP4072DPBF

Parameter	Estimated Value	Units
$k_p(1+\beta)$	8.6	A/V^2
k_{g_adjust}	0.14	None
C_{ce}	75	pF
C_{ge_ON}	3.09	nF
C_{gc}	20	pF

Table A-8-Estimated fictitious Miller capacitances of IRGP4072DPBF for turn-on

V_{ce} (V)	400	150	50	25	15	10	2
$C_{gc'}$ (pF)	25	40	60	120	400	1200	2500

Appendix-B

Measured Switching Waveforms

Measured turn-on switching waveforms of the IGBTs used to validate the models are shown in Figure B-1 through Figure B-5.

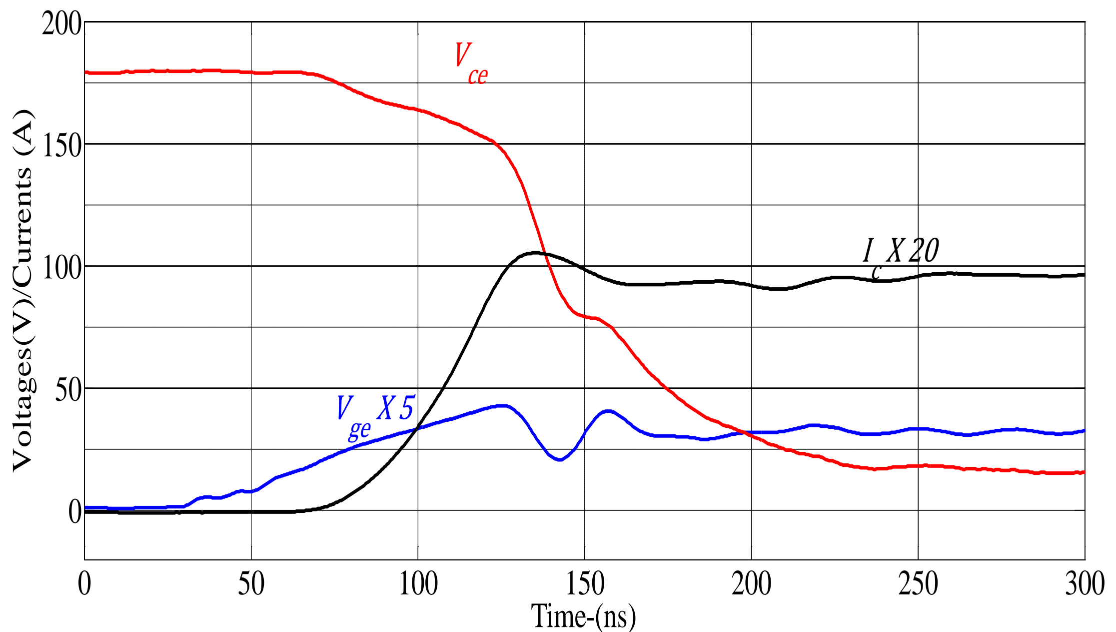


Figure B-1-Measured turn-on waveform of the APT12GT60BR when *Vcc=180V, IL=4.65A, and R_G=150Ω*

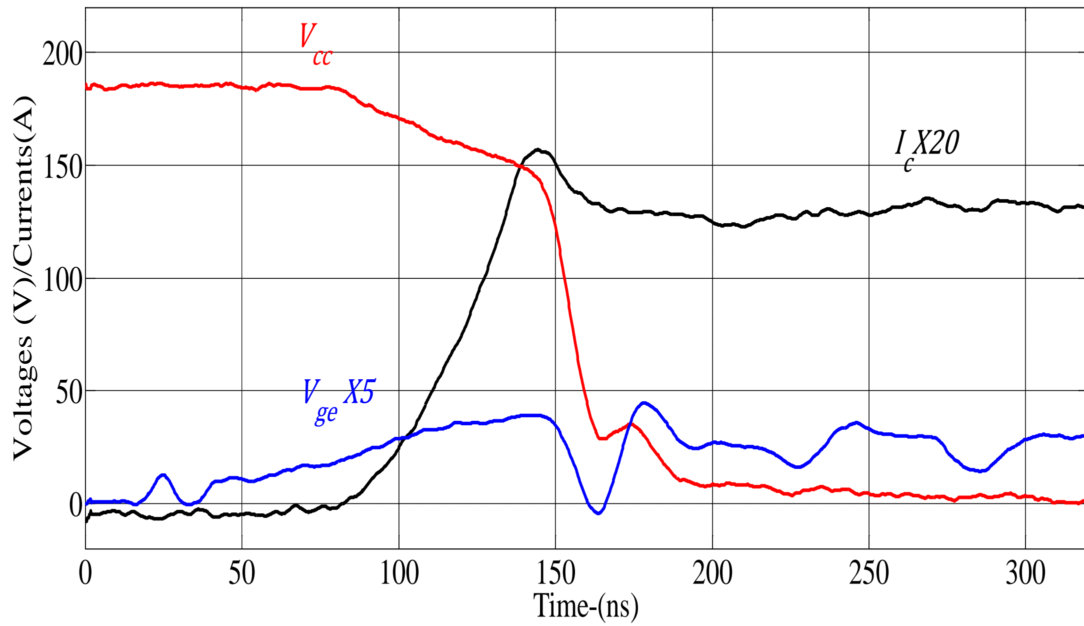


Figure B-2-Measured turn-on waveform of the IRG6I320UPBF at *Vcc=185V, IL=6.5A, and RG=150Ω*

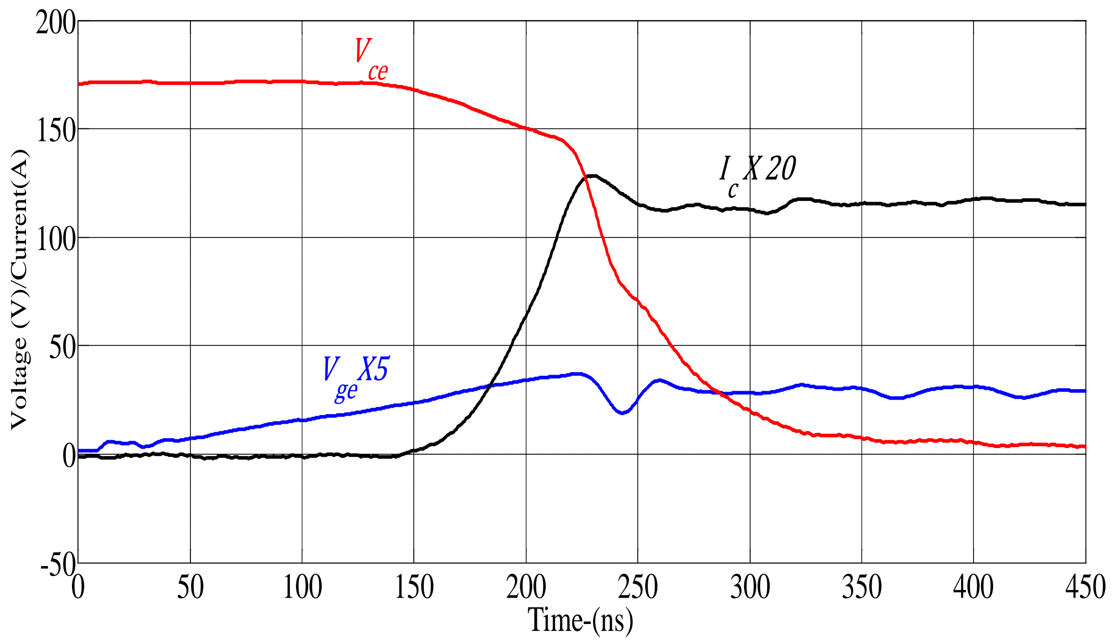


Figure B-3-Measured turn-on waveform of the IRGP4072DPBF at *Vcc=172V, IL=5.5A,* and R_G*=100Ω*

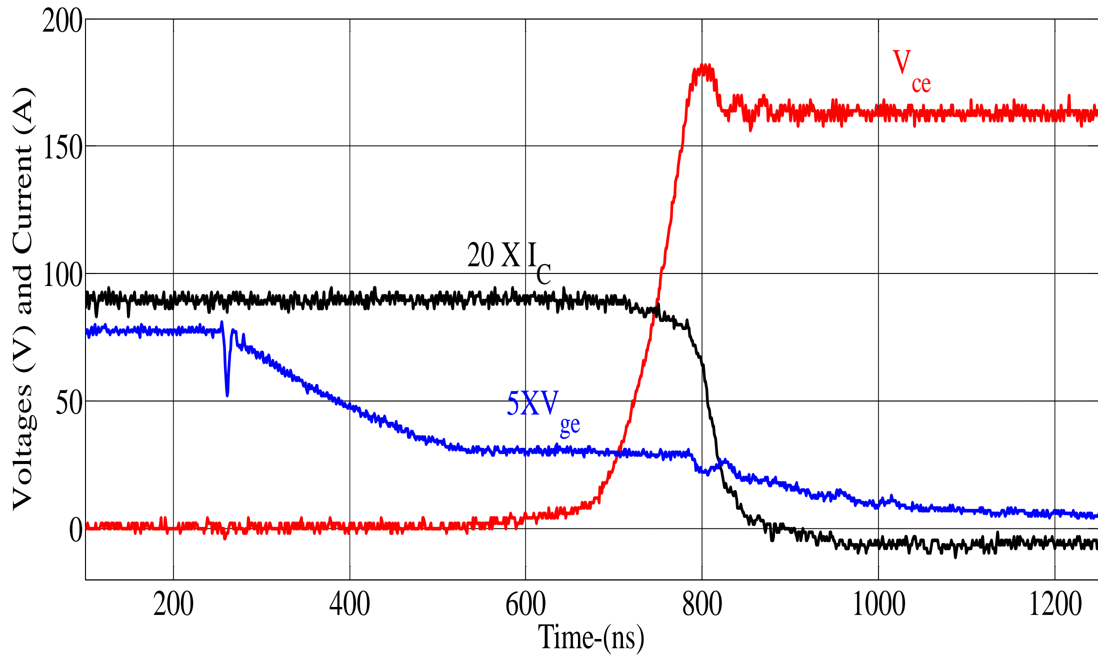


Figure B-4-Measured turn-off waveform of the APT12GT60BR at *Vcc=160V, IL=4.5A,* and $R_G=100\Omega$

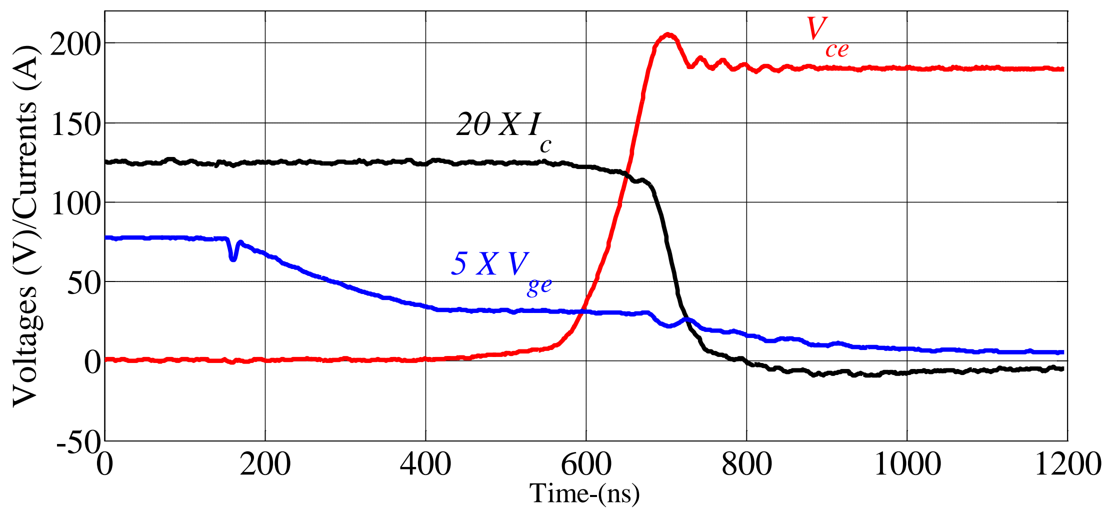


Figure B-5-Measured turn-off waveform of the IRG6I320UPBF at *Vcc=184V, IL=6.2A,*

and $R_G=100\Omega$

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