The Feasibility of a Back-to-Back STATCOM

for Asynchronous Power Transfer

by

DECHUN T WEI

A Thesis

Submitted to the Faculty of Graduate Studies in

partial fulfilment of the requirements for

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Department of Electrical Engineering

University of Manitoba

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A Thesis/Practicum submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements for the degree of

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Dechun T. Wei   © 1996

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Abstract

This thesis investigates the feasibility of using a back-to-back Voltage Source Converter, or STATCOM as a real power controller between independent ac systems. The basic operating features of a back-to-back Voltage Source Converter is simulated not only for the basic six-pulse two-level case but also for the five-level case, since the multi-level STATCOM offers a superior performance in many ways.

Two simple ac systems with very low short circuit ratios were chosen as there is increasing interest in its application with a weak HVDC system. The steady state performance of a back-to-back Voltage Source Converter was tested at an existing HVDC link in parallel. This study is based on an electromagnetic transient simulation program.

The simulation results for a 100 MW back-to-back system is presented with a back-to-back voltage source converter and corresponding control strategies.

The bus voltages are well maintained as the STATCOM can provide fast continuous variation of reactive output power from capacitive to inductive according to the requirement. The slight difference in the sending and receiving end voltages can be adjusted by using either a transformer tap changer or by choosing the proper transformer leakage. Only the Fundamental Frequency Switching (FFS) is considered in this project. The simulation results also indicated that the multi-level design has better performance than a basic six-pulse two-level design in reducing harmonics. An additional merit of a five-level design is that this design is able to increase the voltage ratings of a GTO thyristor inverter for the application of transmission system without having series connection of the GTO thyristors. But the 'voltage unbalance problem' has to be dealt with in five-level case. The tests of a basic six-pulse two-level Voltage Source Converter in parallel with an existing conventional HVDC link in Miles City, Montana proves the feasibility of the design.

List of Symbols

Some of the most frequently occurring abbreviators and symbols used in the thesis are tabulated below. Others are explained where they are used.

ac.......... Alternating current

dc.......... Direct current

μF.............. Microfarad

kA........... Kiloampere

kV........... Kilovolt

rms............. Root-mean-square

MW................. Megawatt

Mvar............ Megavar

FFS................ Fundamental frequency switching

PWM.............. Pulse width modulation

GTO................ Gate Turn Off

HVDC............. High voltage direct current

PI............... Proportional integral

PLL............ Phase lock loop

SCR........... Short circuit ratio

VSC........... Voltage source converter

VCO............... Voltage controlled oscillator

BTB................ Back-to-back

STATCOM............... Voltage source inverter type of static var compensator

EMTDC^{TM}............... Electromagnetic transient Simulation Program package

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Introduction

1.1 BACKGROUND

With the rapid development of the economy and technology, the demand for electrical

power has significantly increased, and more and more power systems are becoming

interconnected to each other by either high voltage direct current (HVDC) transmission

lines or back-to-back (BTB) HVDC converter stations. As a result, the power systems

tend to get larger and larger. The advantages of an interconnected system are better

reliability and economical operation compared with an isolated power system, because an

interconnected system is able to minimize operating cost and reserves, perform a system-

wide unit commitment, coordinate maintance schedules, and maximize the benefits of

emergency procedures. However, because of the growing public impact on environmental

policy and limited utility budget, the building of new transmission facilities, in general,

lags behind the increased needs of power transmission. As a consequence, some

transmission lines are more loaded than was planned when they were built. With the

increased loading of existing transmission facilities, the problem of transient stability after

a major fault can become a power transmission limiting factor [1].

Another feature of large electrical power system development is that there has been an increasing trend to employ HVDC converters in weak ac systems, that is, systems with a short circuit ratio, (SCR), less than 2.5 [2]. It is well known that a traditional HVDC scheme must consume large amounts of reactive power, both at the inverter and rectifier end, which is typically 50 to 60 percent of the real power transmitted at full load because the HVDC converter with conventional thyristors has to use the ac system to turn off the thyristors by forcing the current through a zero point. Therefore, the power transfer capabilities of the back-to-back HVDC system are greatly affected by the static and dynamic behaviour of the reactive power compensators under both normal conditions and severe voltage contingencies. During transients, the reactive power demand may vary over a wide range, and the choices of reactive compensation options at the converter terminal in such cases may become restricted and critical [3]. This is true, especially when the converters are connected to weak ac systems which are not capable of supplying large amounts of reactive power support.

To investigate the above problems, a workshop was held in Porland, Oregon in 1992 to discuss ways in which the cost of HVDC system could be significantly decreased. More recently, a meeting was held on March 28, 1995 in Golden, Colorado, to determine whether there was interest in pursuing a study program to assess the technical performance and economy merits of using voltage source converters (VSC) as a back-to-back link.

The VSC, using gate turn off (GTO) thyristors has been used sucessfully for the

advanced static var compensator (STATCOM) [4] [5] [6] [7] [8]. This is because with the advances in power semiconductor technology, the GTO thyristor can currently block voltages up to 4.5 kV and switch off currents up to 3.0 kA, which make it possible to realize high power VSC type of reactive power compensators, STATCOMS. In Japan, a STATCOM of 80 Mvar rating with 48-pulse inverter connection has been successfully used to stabilize a 154 kV power system [9]. Recently, the Electrical Power Research Institute (EPRI) has also commissioned the design and construction of a scaled model of an 80 Mvar STATCOM for transmission lines [10]. In other words, the STATCOM has been proven to be a technically feasible alternative for the dynamic compensation of ac power transmission system by providing voltage support, increased transient stability, and improved damping. Their performance benefits lead result in the solution of specific application problems with smaller equipment ratings and with better stability than with the conventional devices. Furthermore, recent studies for a STATCOM at an HVDC inverter feeding a very weak ac system, have shown that the STATCOM has superior performance under various ac and dc disturbances [11].

Therefore, it is the topic of this thesis to investigate the possibility of using the STATCOM or VSC as a back-to-back (BTB) tie to transfer real power between asynchronous systems. If it is done, the potential opportunities may exist for improved operating advantages, elimination of the requirements for reactive power compensation, reduced system size, and the possibility of significant reductions in the cost.

In the next two sections, a brief description of a back-to-back HVDC link and a STATCOM configuration will be introduced. Then the motivation of this thesis will be

described.

1.2 DESCRIPTION OF A BTB HVDC SYSTEM

Since the introduction of modern HVDC power transmission in 1954, the dc system has become an important adjunct to a conventional ac power transmission system. A significant application for the dc transmission is the interconnection of differently managed power systems which may be operated synchronously or asynchronously. For instance, a simplified arrangement of a back-to-back HVDC system is shown in Figure 1.1.
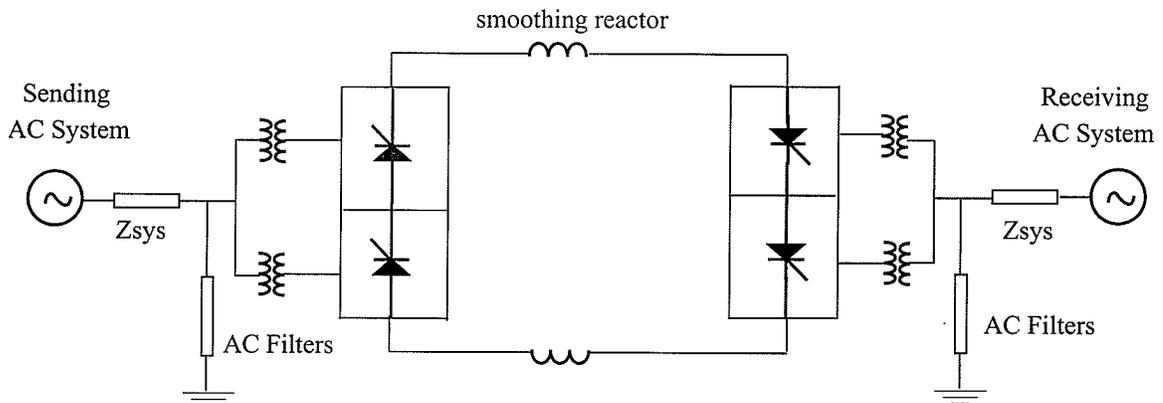
Figure 1.1   Back-to-back HVDC system

In this regard, the major technical contributions of a back-to-back HVDC interconnection are [12]:

1. Fast and exact power transfer can occur between the regional ac systems. This exchange may enable the reduction of spinning reserve requirements or the possible deferring of new generation in the separate regions.

2. No significant changes are needed in the operation and/or management of the

individual power systems.

3. No increase in the short circuit power occurs at the point of interconnection, thus the existing breakers and protection schemes may be kept unchanged.

4. A measure of isolation between the ac system is maintained which can minimize the forming of new loops where flows of active and reactive power may be difficult to control.

5. The dynamic performance of the interconnected ac systems may be enhanced via the fast power and var control features of the dc link.

A BTB HVDC system is usually used when the two adjacent system are close to each other. They differ from point-to-point HVDC transmission in the following ways [13]:

1) The design parameters of the BTB converter station is optimized based on dc current rather than dc voltage, which is a fixed choice for long distance HVDC transmission arising from minimum dc line cost and losses. This usually results in a low nominal dc voltage which can further simplify the design of the converter transformers. For example it economically allows for the construction of a low voltage tertiary winding to which ac filters and other shunt compensation can be connected. Therefore, filter and shunt capacitor switched banks of smaller unit size can be economically realized to permit a fine step change of reactive power.

2) A BTB system can operate under any control scheme, such as constant dc voltage control, constant extinction angle control, constant dc current control or constant reactive power control.

3) With the absence of telecommunication, all control and protection functions of both rectifier and inverter stations can be integrated which simplifies the overall control

structure.

4) The two back-to-back blocks are controlled and operated in a more independent manner than the two poles of a dc transmission system. That is, there are no restrictions for unbalanced operation regarding problems associated with earth return currents.

1.3 CONFIGURATION OF THE STATCOM

1.3.1 THE DESIGN OF A BASIC TWO-LEVEL STATCOM

The development of the high power GTO thyristor has lead to the design of new compensators which are basically a voltage source converter connected to the system through an inductor, usually the leakage reactance of a transformer. The operating principle of the STATCOM is very similar to the conventional rotating synchronous condenser.

The synchronous condenser is an unloaded synchronous machine connected to the power system. Figure 1.2 shows the simplified equivalent circuit of a synchronous condenser, where X_d represents the synchronous reactance of the machine. If a small winding resistance is ignored, the load angle of the machine is zero and the induced voltage, $\vec{E}_f$, is in phase with the system voltage, $\vec{V}_s$. The phase current is given as: $\vec{I}_d = \left(\vec{V}_s - \vec{E}_f \right)/j \cdot X_d$ As the magnitude of $\vec{E}_f$ can be controlled by the field current, the current flowing into or out of the machine can be controlled. For example, if increasing the field current makes the amplitude of the induced voltage of the synchronous condenser larger than the voltage of the ac system, $(E_f > V_s)$, then the current flows through the reactance and winding resistance from the synchronous condenser to the ac system. $\vec{I}_d$ leading $\vec{V}_s$ by 90°. If decreasing the

field current makes the amplitude of the induced voltage of the synchronous condenser smaller than the voltage of the ac system, $(E_f < V_s)$, then the current flows through reactance and winding resistance from the ac system to the synchronous condenser. $\vec{I_d}$ lagging $\vec{V_s}$ by 90°. And, if the amplitude of the induced voltage of the synchronous condenser is equal to the voltage of the ac system, $(E_f = V_s)$, then the current equals zero, no reactive power is exchanged. (In fact, there will be always a small in phase current flowing into the machine to supply the constant and copper losses.) From this point of view, the STATCOM is just an electronic equivalent of the conventional rotating synchronous condenser. The difference is the reactive power output of the STATCOM is controlled by varying the magnitude of the inverter output voltage instead of by varying the field current.
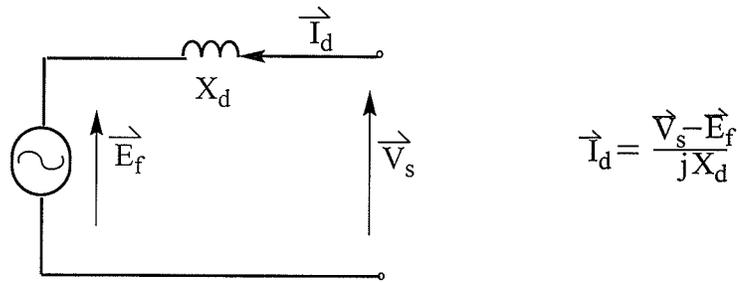
Figure 1.2 A simplified circuit of a synchronous condenser

Figure 1.3 shows the configuration of a basic six-pulse two-level STATCOM, which consists of six GTO thyristors with reverse conducting diodes. If the fundamental of the STATCOM voltage $(\vec{V_i})$ is kept in phase with the ac system voltage $(\vec{V_s})$, then the line current flowing into or out of the STATCOM is always at 90° to the network voltage due to the reactive coupling. When the fundamental of the STATCOM voltage is less than the ac system voltage, reactive power is absorbed by the STATCOM, and the reactive current flows into the STATCOM. On the other hand, when the fundamental of the STATCOM

voltage is higher than the ac system voltage, the reactive power flows from the STATCOM to ac system, reactive power is generated by the STATCOM. Also when the fundamental of the STATCOM voltage is equal to the ac system voltage, the reactive power exchanged is zero. The phase diagrams of a basic six-pulse two-level STATCOM are shown in the Figure 1.4 (a) and (b). Any phase shift in the phase of $\vec{V}_i$ will cause real power to flow into or out of the dc bus thereby charging or discharging the capacitor. Since the current, $\vec{I}_s$, is equal to the difference of $\vec{V}_s$ and $\vec{V}_i$ divided by the reactance, the current can be controlled the current by controlling $\vec{V}_i$.

$$\vec{I}_s = \frac{\vec{V}_s - \vec{V}_i}{jX} \qquad (1\text{-}1)$$

There are two options available for controlling the magnitude of $\vec{V}_i$:

1) Maintain a constant dc bus voltage and use pulse-width modulation (PWM) techniques to control the fundamental voltage as well as limit some of the harmonic voltages produced;

2) Produce a square-wave output voltage using fundamental frequency switching (FFS) and control the magnitude of the ac voltage by controlling the magnitude of the dc capacitor voltage, V_{dc}.
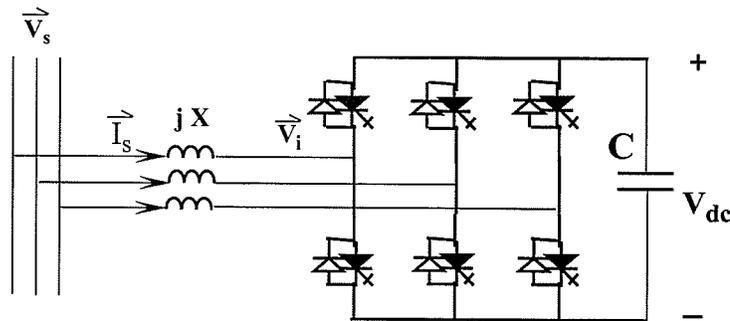
Figure 1.3   A basic Six plus two -level STATCOM
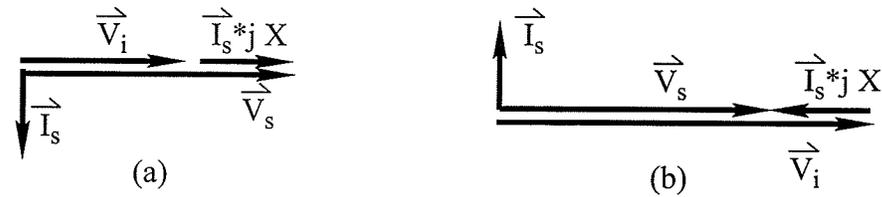
Figure 1.4   A phase diagram of a STATCOM

(a)   Phase diagram for the lagging mode

(b)   Phase diagram for the leading mode

As the switching losses of the GTO thyristor can be quite large, PWM techniques have been found to be inferior to fundamental frequency switching. Therefore, the FFS method will be the only one considered in this study.

With a charged dc capacitor, the waveform obtained from a six-pulse two-level VSC with fundamental frequency switching is the square-wave phase voltage. Figure 1.5 is the firing pulse sequence of the six GTO thyristors and Figure 1.6 shows the output phase voltage waveform of a six-pulse two-level STATCOM. It contains a complete spectrum of odd harmonics, which makes this simple inverter impractical for high power applications.
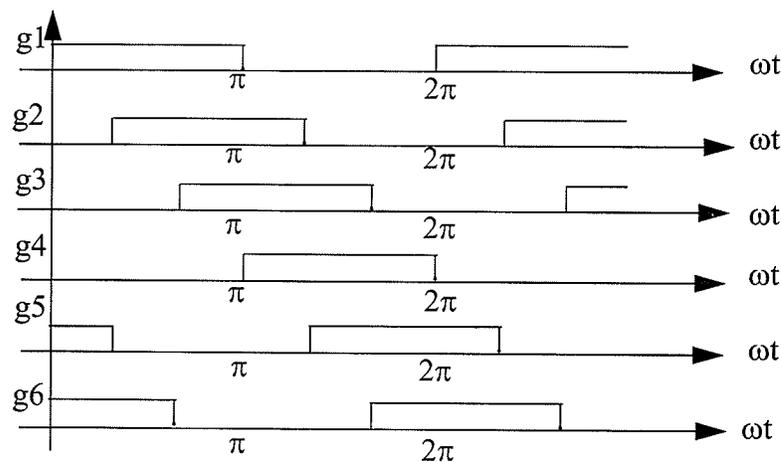
Figure 1.5   Firing pulses for 6-pulse 2-level STATCOM
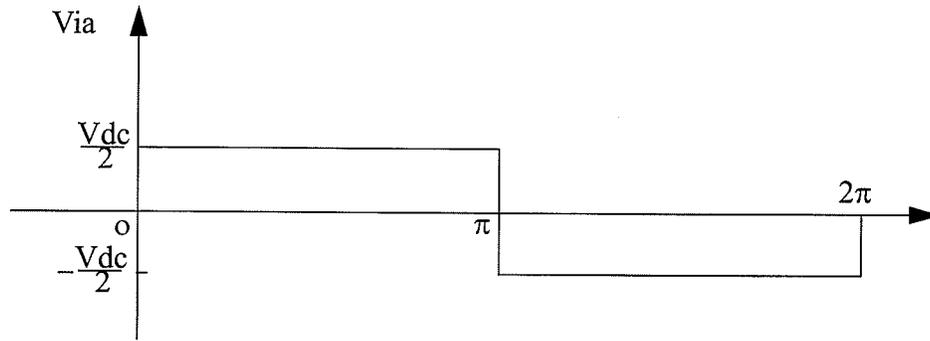
Figure 1.6 The phase voltage for 6-pulse STATCOM

The Fourier series of phase voltage Via is:

$$Via\,(\omega t) \;=\; \frac{2 \cdot Vdc}{\pi} \sum_{1,\,3,\,5\ldots} \frac{1}{n}\sin\,(n\omega t) \qquad\qquad (1\text{-}2)$$

And the line voltage is given by:

$$Vab\,(\omega t) \;=\; \frac{2 \cdot Vdc}{\pi} \sum_{1,\,3,\,5\ldots} \frac{1}{n}\!\left(\sin\,(n\omega t) - \sin n\!\left(\omega t - \frac{2\pi}{3} \right) \right) \qquad (1\text{-}3)$$

It is clear that the triple harmonic will not appear in the line voltage because of the cancellation among the three phases. To reduce harmonics, n basic six-pulse two-level inverters which are operated with appropriate relative phase displacements can be combined so as to obtain a multi-pulse structure as shown in Figure 1.7. Since the lowest harmonic present in the output voltage is equal to the pulse number minus one, the harmonic spectrum of the device improves rapidly with increasing pulse number. For instance, the lowest harmonic for a 12-pulse structure is the 11th, and for a 24-pulse is the 23th. So the multi-pulse circuit configuration is considered practical for high power utility applications [7].
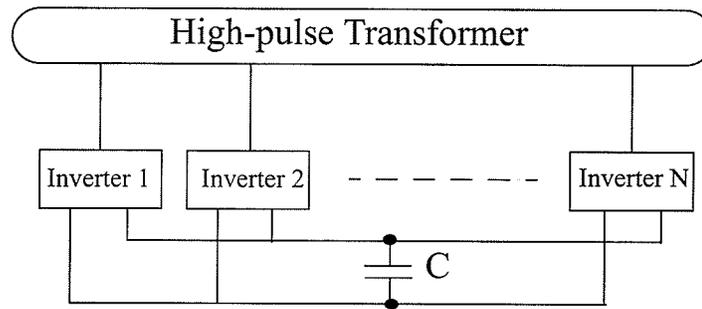
Figure 1.7   High-pulse structure inverter

1.3.2 MULTI-LEVEL STATCOM CONFIGURATION

Another option is to use a multi-level GTO thyristor inverter which offers an attractive alternative to the high-pulse inverter since it is capable of producing a stepped voltage output of low harmonic content, while switching each device only once per cycle [14].

A schematic structure of one pole, or phase, of a five-level GTO thyristor inverter (or STATCOM) is shown in Figure 1.8. Two additional poles would be required for the three-phase inverter where the four dc capacitors are also shared by the other two phases. In this design, each individual GTO thyristor is clamped via a diode clamping circuit to a dc capacitor voltage. It allows the individual switching of the GTO thyristors and results in a stepped waveform of the output voltage which contains no 5th or 11th harmonics if the fundamental frequency switching method is used. In general, for an N-level inverter, (N-1)/2 lower dominant harmonics can be eliminated for N odd and (N/2-1) harmonic for N even.
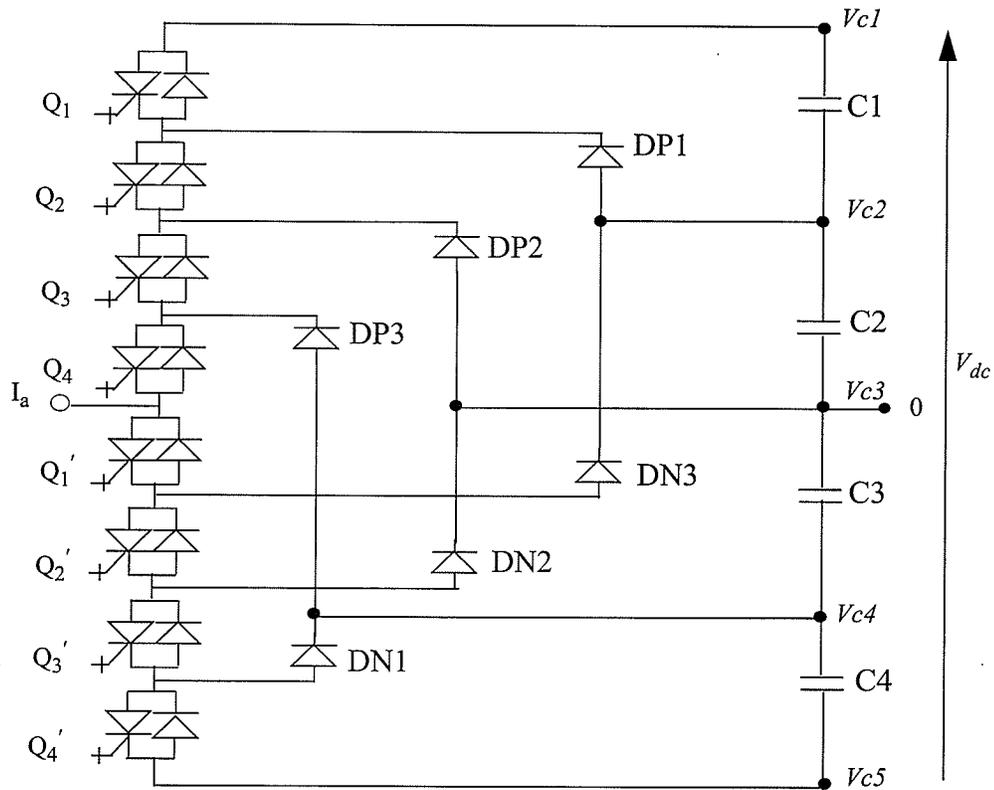
Figure 1.8   Phase diagram of 5-level converter

The advantages of the multi-level STATCOM are [9]:

a) The voltage level can be increased without series connection of GTO thyristors and the necessity of simultaneous switching;

b) The harmonic distortion on the ac side can be greatly reduced without filters or multi-pulse bridge connections.

An N-level diode-clamp converter typically consists of N-1 capacitors on the dc bus or N phase voltage levels. As the number of levels increases, the synthesized output waveform adds more steps, producing a staircase waveform which approaches the sinusoidal waveform with a minimum of harmonic distortion. Ultimately a zero harmonic distortion

of the output waveform can be obtained by an infinite number of levels. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems.

When compared to inverters using pulse-width modulation (PWM) techniques, the multi-level STATCOM has a lower harmonic distortion and reduced switching power losses. It should be noted that the multi-level inverter can also be connected in high-pulse number configurations which will further reduce the harmonic content of the output waveform. For instance, the 12-pulse 5-level inverter would contain no harmonic below the 17th, and the 24-pulse 5-level inverter will not contain harmonics below the 29th. Table 1 gives the switching strategies and the Figure 1.9 shows the phase voltage waveform of a 5-level converter.

Table 1: 5-level converter voltage levels and corresponding switch states

output	state							
Via	Q_1	Q_2	Q_3	Q_4	Q_1'	Q_2'	Q_3'	Q_4'
V1=Vdc/2	1	1	1	1	0	0	0	0
V2=Vdc/4	0	1	1	1	1	0	0	0
V3=0	0	0	1	1	1	1	0	0
V4=-Vdc/4	0	0	0	1	1	1	1	0
V5=-Vdc/2	0	0	0	0	1	1	1	1
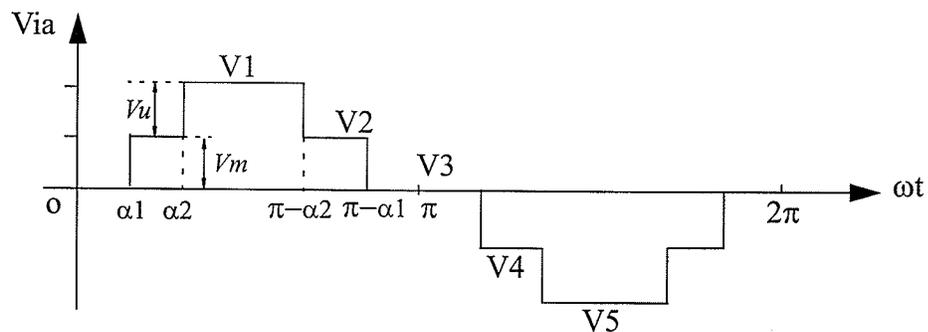
Figure 1.9   Phase voltage waveform of a 5-level converter

The Fouries series of phase Via will be:

$$Via\,(\omega t) = \frac{4}{\pi}\sum_{n}\frac{1}{n}\,[\,Vm\cos\,(n\alpha_1) + Vu\cos\,(n\alpha_2)\,]\,\sin\,(n\omega t) \tag{1-4}$$

If Vu = Vm = Vc, than the magnitude of the Fourier coefficients will be:

$$H(n)\;=\;Vc\cdot\frac{4}{\pi}\cdot\frac{1}{n}\,[\cos\,(n\alpha 1) + \cos\,(n\alpha 2)\,] \tag{1-5}$$

Where n = 1,3,5,......

It should be mentioned that the angles $\alpha 1$ and $\alpha 2$ can be chosen at any angle within the range of $0°$ to $90°$ on the basis of getting a lower harmonic content or a larger fundamental voltage. Hence, $\alpha 1$ and $\alpha 2$ can be switched at such values that two harmonics could be sum to zero. For example, in order to cancel the 5th and 7th harmonic, simply let the equations from (5) be:

$$[\cos\,(5\alpha 1) + \cos\,(5\alpha 2)\,]\;=\;0 \tag{1-6}$$

$$[\cos\,(7\alpha 1) + \cos\,(7\alpha 2)\,]\;=\;0 \tag{1-7}$$

The Newton-Raphson method can be used to solve this non-linear equation (1-6) and (1-7), giving: $\alpha 1 = 5.14°$ and $\alpha 2 = 30.86°$

This means that if we switch to the voltage, V2, at $5.14°$ and to the V1 at $30.86°$ in the positive half cycle of the fundamental, and similarly in the negative half cycle. The output voltage of the five level inverter will not contain the 5th and 7th harmonic components.

1.4 PURPOSE

The purpose of this investigation object was to study the feasibility of a back-to-back STATCOM for asynchronously power transfer by using the basic six-pulse 2-level STATCOM. Controls were designed to regulate the real power transfer as well as the reactive power production or absorption.

In the thesis, the author will also examine the feasibility of using multi-level STATCOM in this application. Particular attention will be paid to the variation of the individual dc capacitor voltage levels during real power exchanges using the FFS method.

In order to test the dynamic performance of the BTB STATCOM under critical conditions, a very weak ac system was chosen for modelling and analysing the system. The studies are conducted using the EMTDC$^{\text{TM}}$ program.

Basic Two-level BTB Converter

2.1 THE STUDY SYSTEM

The study began from a simple case, the six-pulse two-level back-to-back converter. The simplified study system is based on the interconnected system between Saskatchewan and Albert since the tie line between these two systems is very weak, which would make this project closer to the practical situation. As shown in Figure 2.1, a BTB STATCOM converter tie is situated between the sending and receiving end. The SCRs of the ac systems are 1.0 and 2.0 respectively. The damping angle is 85° in the sending end and 80° in the receiving end. Both ac bus voltages are rated at 230 kV, and the maximum power transmission is 150 MW. The transformer chosen is 230/100 kV on both sides. As shown in Figure 2.2, the STATCOMs used in this scheme are six-pulse two-level GTO thyristor converters with a common dc capacitor. The value of capacitance is $100\mu F$. Since the STATCOM can be controlled to generate or absorb the reactive power, no other reactive power compensators are required in the system configurations.
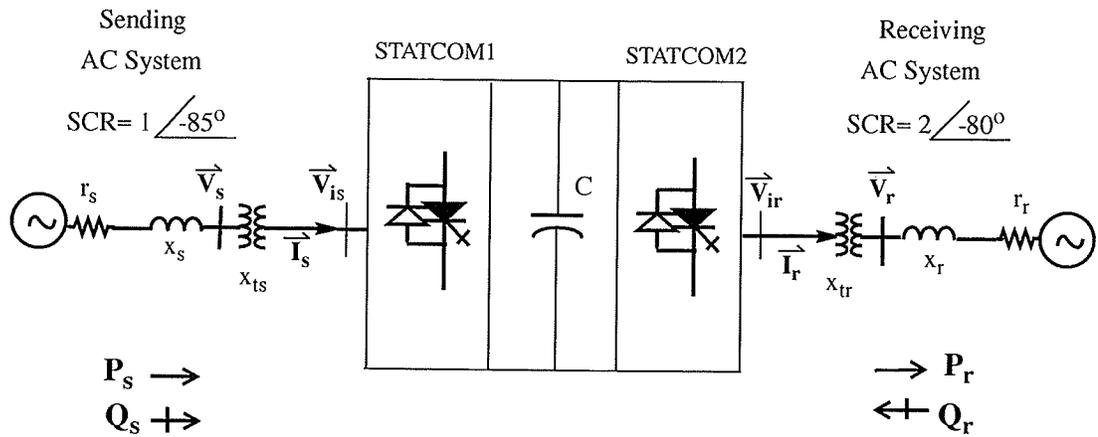
Figure 2.1 Simplified study system scheme
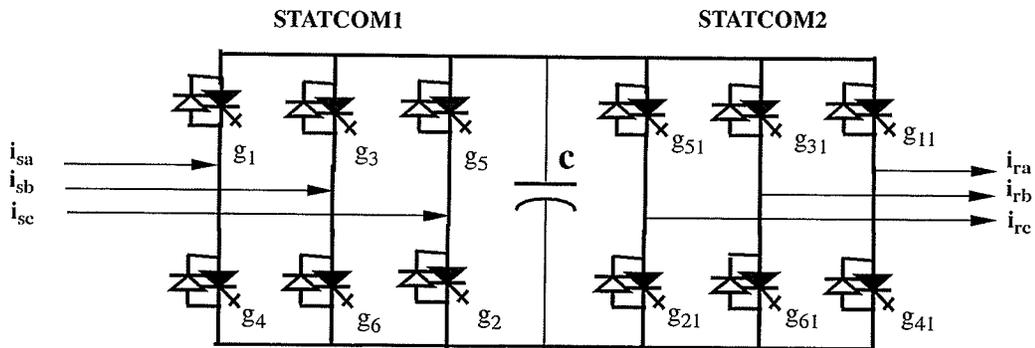
Figure 2.2 Six-pulse 2-level back-to-back STATCOM

2.2 OPERATION PRINCIPLE

As mentioned before, a basic six-pulse two-level GTO thyristor inverter can act as a reactive power compensator. When two identical STATCOMs are interconnected together with a "dc capacitor link" as shown in Figure 2.2, the device is not only able to generate the inductive or capacitive reactive power, to improve the system stability, but is also able to

transfer real power between the two ac systems. This should greatly reduce the cost of HVDC systems through increasing the real power transfer without the installation of extra devices. In order to realize the task of the power transfer, the left-hand side converter serves as the rectifier for the utility interface, and the right-hand side converter serves as the inverter for the ac load.

Considering the dc capacitor voltage as an input, the converters will produce square-waveform output voltages. The fundamental output voltage of the each converter is the function of the voltage value of the dc capacitor which is: $\quad v_{ia}(\omega t) = \dfrac{2 \cdot Vdc}{\pi} \sin \omega t$

In other words, as described in Section 1.3.1, the voltage value across the dc capacitor has a direct influence on the reactive power supplied on the sending and receiving ends. If the voltage of the dc capacitor is kept at a constant value with the precise control of the voltage control loop, then the magnitude of the output voltages ($\hat{V}_{is}$ and $\hat{V}_{ir}$) of the converters will be constant as well. If the converter voltages are maintained in phase with their respective ac system voltages, the STATCOMs behave as two dependent compensators where the amount of reactive power supplied or absorbed will depend on the values of the leakage reactance and the ac system voltage on each sides, as $\hat{V}_{is} = \hat{V}_{ir}$, that is:

$$ Q_s = \frac{(V_s - V_{is}) \cdot V_s}{X_{ts}} \qquad \text{and} \qquad Q_r = \frac{(V_r - V_{ir}) \cdot V_r}{X_{tr}} $$

A voltage control loop can be placed on either side of the system. In this scheme, the voltage control loop is placed on the sending side to maintain that bus voltage at 1.0 pu.

Another control loop is located at the receiving end to control the real power flow in the system by providing the proper phase shift between the converter voltages and their respective system voltages. Taking one case as an example, if an amount of real power (P_r)

is required, the phase shift between the output voltage of the STATCOM2 ($\hat{V}_{ir}$) and the bus voltage on the receiving end ($\hat{V}_r$) must be kept at δ_r, which can be accomplished by controlling the firing instants of STATCOM2. When the power is taken out of the dc capacitor, the voltage across the capacitor tends to fall and causes a decrease of the bus voltage at the sending end. Simultaneously, the voltage control loop will quickly act to charge the capacitor and supply the reactive power demanded for supporting the sending end bus voltage. In the independent control strategy, since the power control and voltage control can't exactly act at same time, the bus voltage will fall first at the transient instant. If the power flow direction is reversed, then the bus voltage will increase at the transient instant. In general, the more real power transferred, the more reactive power is needed to support the bus voltage. Figure 2.3 shows the phasor diagrams of this case. It should be noted that these phasor diagrams can only be combined if the frequency of the two ac systems is the same.

Besides the independent control as described above, where the power controller adjusts δ_r alone and the voltage controller adjusts δ_s alone, the coordinated power control can also be applied where the power controller can adjust δ_r and δ_s together. The transient performance of bus voltages can be greatly improved by coordinated control.

The real power exchanged for the transmission line [18] [19]:

$$P_s = \frac{E_s \cdot V_s \cdot \sin(\delta_s)}{Z_s \cdot \sin(\beta L)} \approx \frac{\delta_s}{Z_s} \approx SCR1 \cdot \delta_s = SCR2 \cdot \delta_r \approx P_r \tag{2-1}$$

Where the wave number in rad/km, β, source voltage and bus voltage, E_s and V_s, are assumed at 1.0 pu.

Since the SCR2 is twice of SCR1 in this study, the δ_r should be approximately one-half of δ_s for the same amount of power exchange. That is, the rate of change of δ_s should be

approximately twice of δ_r. Therefore, a multiplier, M=2.0, can be applied if two identical phase lock loops (PLL) are used in the voltage and power control loop. It should give a better dynamic control of the bus voltage during the change of power reference.

(a) Phase diagram for the receiving end

$$P_r = \frac{|\vec{V}_r|*|\vec{V}_{ir}| \sin(\delta_r)}{X_{tr}}$$

$$Q_r = \frac{|\vec{V}_r|^2}{X_{tr}} - \frac{|\vec{V}_r|*|\vec{V}_{ir}| \cos(\delta_r)}{X_{tr}}$$

(a)

(b) Phase diagram for the sending end

$$P_s = \frac{|\vec{V}_s|*|\vec{V}_{is}| \sin(\delta_s)}{X_{ts}}$$

$$Q_s = \frac{|\vec{V}_s|^2}{X_{ts}} - \frac{|\vec{V}_s|*|\vec{V}_{is}| \cos(\delta_s)}{X_{ts}}$$

(b)
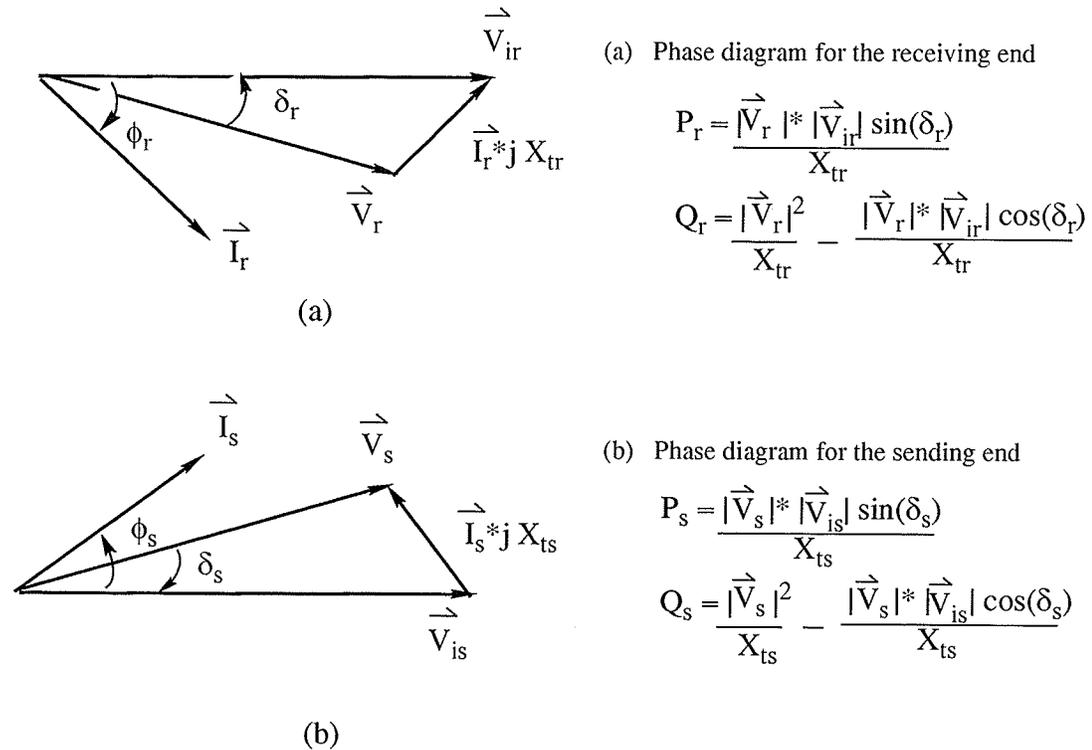
Figure 2.3   A phase diagram of a BTB converter

The maintenance of bus voltage at the receiving end can be achieved through either a transformer tap changer or an adjustment of the transformer leakage. The transformer leakage effect will not be very obvious as the chosen ac systems are very weak which denoted that the inductances of the ac systems are rather large. Since the two ac systems are connected by a common "dc link" through their VSCs which act like ac voltage sources, this type of the back-to-back intertie can be used not only for connecting two asynchronous ac systems; but also as a phase shifter and a unified power flow controller.

2.3 THE TRANSFORMER LEAKAGE EFFECT

In this section, the brief theoretical calculation is made by using Mathcad software to prove that the change of the transformer leakage can affect the bus voltage. Assume that the transmission lines in both sides are lossless, the Vs represents the sending voltage, Vr is the receiving voltage, Zo is the Surge Impedance, Vi is the converter voltages which are the same for two converters, the wave number is β, the L1 and L2 represent the length of transmission line in the sending end and receiving end respectively, the Ps and Qs stand for the real power and reactive power in the sending end, the Pr and Qr stand for the real power and reactive power in the receiving end and δ is the load angle.

(1) Calculation the Surge Impedance Zo [18] [19].

$$Assume \qquad \overline{Vs} = Vs \cdot e^{j \cdot 0} \qquad \overline{Vr} = Vr \cdot e^{j \cdot \delta} = Vr \cdot [\cos\delta - j \cdot \sin\delta]$$

$$From \qquad \overline{Vr}(L) = \overline{Vs} \cdot \cos(\beta \cdot L) - j \cdot Zo \cdot \overline{Is} \cdot \sin(\beta \cdot L)$$

$$We\ get \qquad \overline{Is} = \frac{Vs \cdot \cos(\beta \cdot L) - Vr \cdot \cos(\delta) + j \cdot Vr \cdot \sin(\delta)}{j \cdot Zo \cdot \sin(\beta \cdot L)}$$

Since the Zo is only determined by the structure of the transmission line, to simplify, let Vr = 0. Then

$$\overline{Is} = \frac{Vs \cdot \cos(\beta \cdot L)}{j \cdot Zo \cdot \sin(\beta \cdot L)}$$

$$\overline{Z} = \frac{\overline{Vs}}{\overline{Is}} = j \cdot Zo \cdot \frac{\sin(\beta \cdot L)}{\cos(\beta \cdot L)} = j \cdot Zo \cdot \tan(\beta \cdot L) \qquad \dots\dots\dots\dots\dots\dots\dots\dots (2-2)$$

If: L1 = 600 (km) $\beta = 1.27*10^{-3}$ (rad/km)   Vs = 230 (kV)   Pd = 200 (MW)

The line current: $IL = \dfrac{Pd \cdot 1000}{\sqrt{3} \cdot Vs} = 502.044$ (kA)

In the sending end lossless line, the SCR = 1.0. From the equation (2-2)

$$\frac{Vs}{\sqrt{3} \cdot IL} = Zo \cdot \tan(\beta \cdot L) \qquad \text{............................} \quad (2-3)$$

The equation (2-3) gives the surge impedance: $Zo = 277.177$ (Ω)

In the receiving end lossless line, the SCR = 2.0 which means:

$$Zo \cdot \tan(\beta \cdot L) = \frac{277.177}{2} \qquad \text{............................} \quad (2-4)$$

From the equation (2-4), with the same surge impedance lossless line the length of the receiving end will be: $L2 = 365.077$ (km)

(2) The relationship between Qs,Qr and real power flow (Ps = Pr = P) in the system.

Since $Ps = \dfrac{\sin(\delta)}{\sin(\beta \cdot L1)}$ .... (2-5)

$Qs = \dfrac{\cos(\beta \cdot L1) - \sin(\delta)}{\sin(\beta \cdot L1)}$ .... (2-6)

Combined (2-5) (2-6) together we get equation (2-7). For the receiving end we can get equation (2-8)

$$Qs(P) = \frac{\cos(\beta \cdot L1) - \sqrt{1 - Ps^2} \cdot \sin(\beta \cdot L1)}{\sin(\beta \cdot L1)} \qquad \text{............................} \quad (2-7)$$

$$Qr(P) = \frac{\cos(\beta \cdot L2) - \sqrt{1 - Pr^2} \cdot \sin(\beta \cdot L2)}{\sin(\beta \cdot L2)} \qquad \text{............................} \quad (2-8)$$

According to the equation (2-7) and (2-8), Figure 2.4 gives the curves of Qs, and Qr vs P.
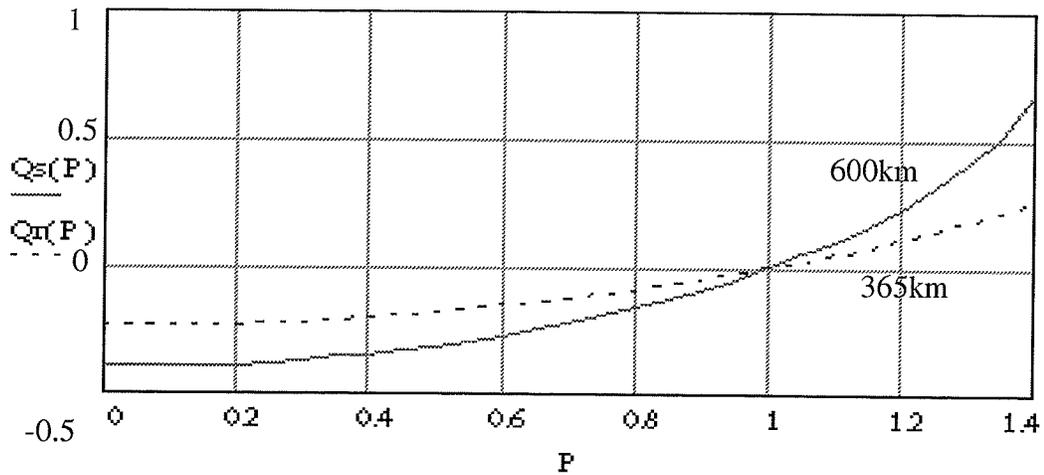
Figure 2.4   Reactive power demand vs real power transferred

(3) The relationship between real power and load angle in pu.

Since

$$Ps(\delta) = \frac{\sin(\delta)}{\sin(\beta \cdot L1)} \qquad \dots\dots\dots\dots\dots\dots\dots\dots (2-9)$$

$$Pr(\delta) = \frac{\sin(\delta)}{\sin(\beta \cdot L2)} \qquad \dots\dots\dots\dots\dots\dots\dots\dots (2-10)$$

According the equation (2-9)(2-10), the Figure 2.5 gives the curves of Ps,Pr vs δ.
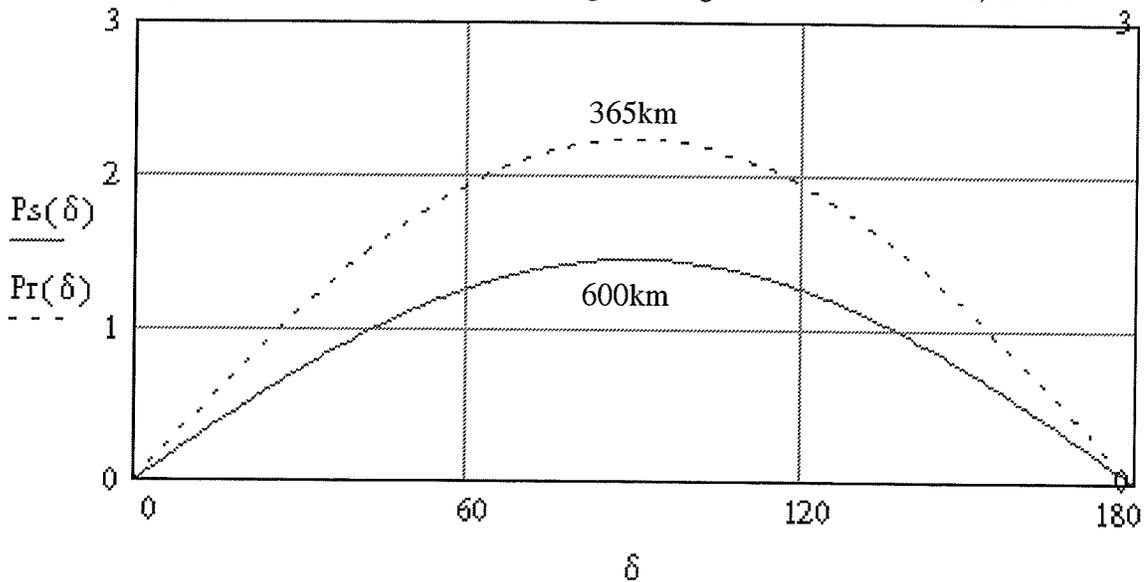
Figure 2.5   Power transferred vs load angle

In the steady state Ps = Pr = P all the time, and the converter output voltage (Vi) is the

same for both converters. The X_{ts},X_{tr} represent the transformer leakage in pu at the sending

end and the receiving end.

From equations (2-7) (2-8) and $\quad Qs = \dfrac{Vs - Vi}{X_{ts}}$

$$Qr = \dfrac{Vr - Vi}{X_{tr}}$$

We get: $\quad Vs\,(P) = \dfrac{\cos(\beta \cdot L1) - \sqrt{1 - P^2} \cdot \sin(\beta \cdot L1)}{\sin(\beta \cdot L1)} \cdot X_{ts} + Vi \qquad \ldots\ldots\ldots\ldots (2-11)$

$$Vr\,(P) = \dfrac{\cos(\beta \cdot L2) - \sqrt{1 - P^2} \cdot \sin(\beta \cdot L2)}{\sin(\beta \cdot L2)} \cdot X_{tr} + Vi \qquad \ldots\ldots\ldots\ldots (2-12)$$

Assume $Vi = 1.0$ pu.

The curve in the Figure 2.6 shows how the bus voltages vary with the different

transformer leakage while $X_{ts}=1.0$ pu and $X_{tr}=1.0$pu, 0.8pu, 0.5pu. It indicates that the bus

voltage will increase with increasing transformer leakage when real power is bigger than

1.0 pu. And the bus voltage will decrease with the increasing of the transformer leakage

when real power is smaller than 1.0 pu in the receiving end.
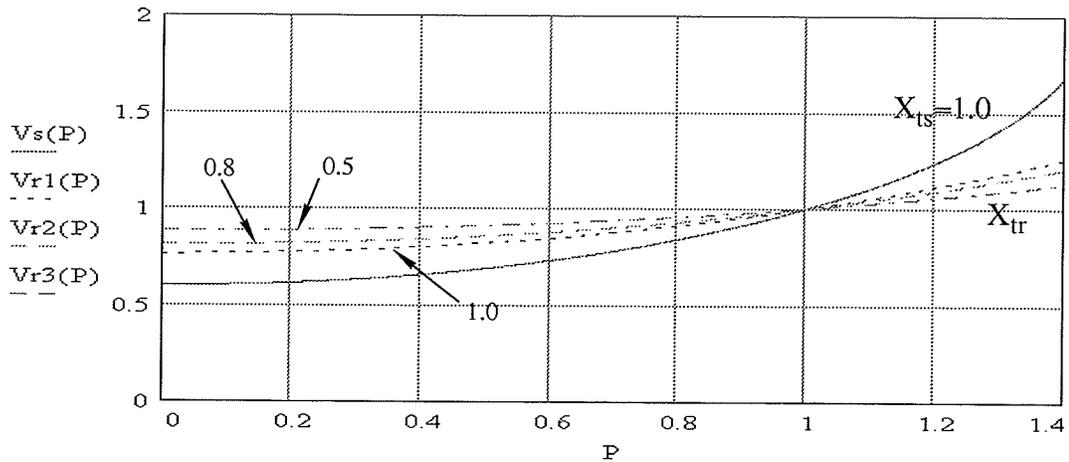
Figure 2.6 Bus voltage variation with the change of transformer leakage

2.4 CONTROL STRATEGY

As mentioned before, in order to control the real power transmission, the sending end converter (STATCOM1) serves as the rectifier to absorb the power from the ac system, while the receiving end converter (STATCOM2) functions as the inverter to generate power into the ac system.

To perform these two tasks, two control loops were designed. At the sending end, a voltage control loop was used to control the bus voltage to a reference value. The control loop relies on a phase-locked loop based firing system as shown in Figure 2.7 [15] [16]. A Voltage Controlled Oscillator (VCO) generates the angle information, the phase of which is compared with that of the commutating bus voltage at the sending end. The filtered phase error from the phase detector, together with the control signal of the terminal voltage error is fed through a Proportional Integral Regulator to change the VCO output frequency. The steady state is reached when the phase error has a value of zero, which indicates synchronism between the ac system on the sending end and the VCO. The nominal frequency of the VCO is controlled by a reference (f_0). The firing pulses for STATCOM1 are issued at the zero crossings of the three phase reference voltage.

Like the voltage control, the power control loop is built in the same way to get the firing pulses for the STATCOM2. As seen in Figure 2.8, the error control signal of the required real power transmission is added to the phase error signal of the phase lock loop for the power control block to adjust the phase angle of the voltage $\hat{V}_{ir}$. The real power error signal could also be fed to the phase lock loop of the voltage control block for investigation of coordinated power control. The reference signals of the firing frequency can be different in

the two ac systems for systems of different frequency.
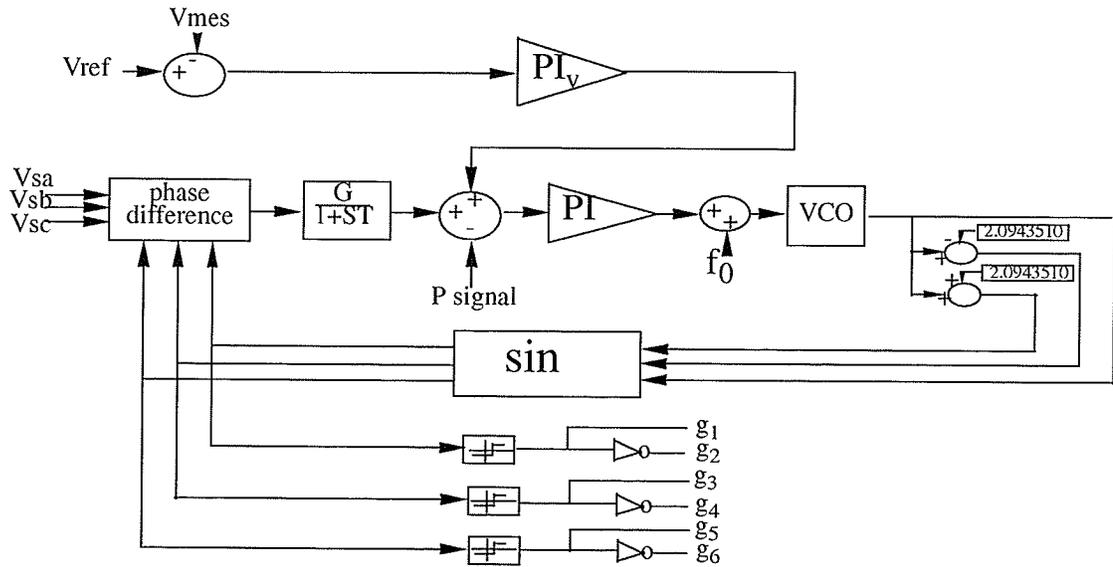
Figure 2.7 Phase lock loop for voltage control
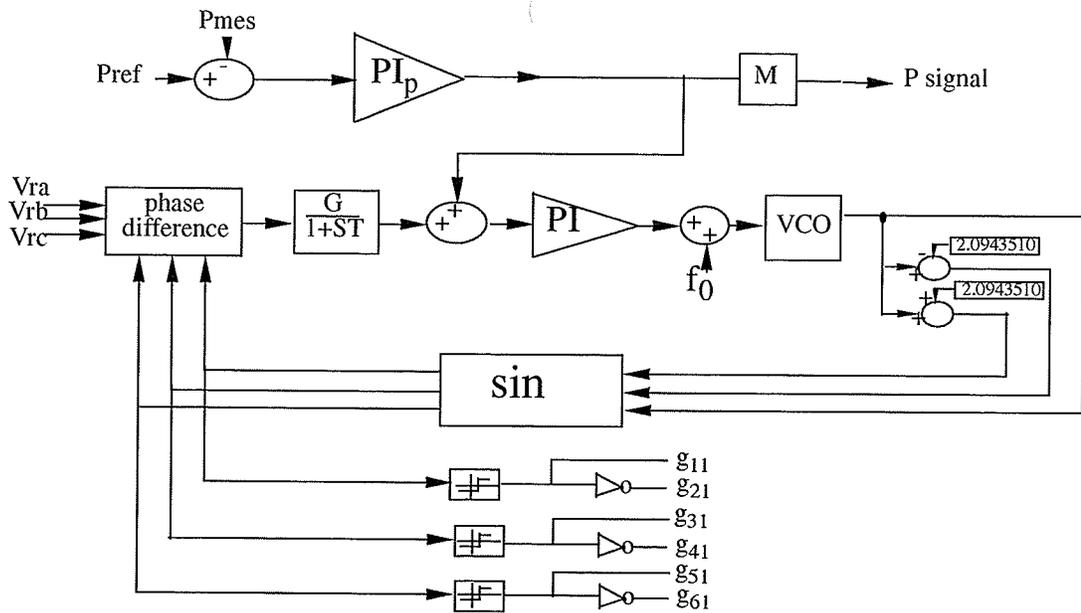
Figure 2.8 Phase lock loop for real power control

2.5 SIMULATION RESULTS

Based on the above analysis and discussion, the simulation results presented next are taken directly from the study system by using the Electromagnetic Transients Simulation Program (EMTDC) package [17]. Two identical PLLs are used in the control strategy.

2.5.1 Independent control

Figure 2.9 shows the real power exchange at both the sending and the receiving ends. It is clear that the power flow is controlled smoothly. The sending power and the receiving power is also well balanced, which illustrates the feasibility and performance of the design and controls.

Corresponding to the power transfer, the bus voltage at the sending end is maintained at the desired level and the transient overvoltage is less than 4.0% for 100MW real power exchange, as shown in Figure 2.10. It should be mentioned that the transient overvoltage can be further reduced by reducing the step of power change or by reversing the power exchange direction which indicated that it is easier to transfer power from strong system to weak system.

Figure 2.11 gives the dc voltage across the capacitor in the back-to-back STATCOM converter. The dc voltage is maintained at a relatively constant value since the power flow in both sides tends to compensate each other due to the control action.

The reactive power supplied by the converters corresponding to real power flow, shown in Figure 2.9, is shown in Figure 2.12. This figure indicates that the stronger receiving end requires less reactive power than the sending end and that the reactive power demand increases with increased power transfer.
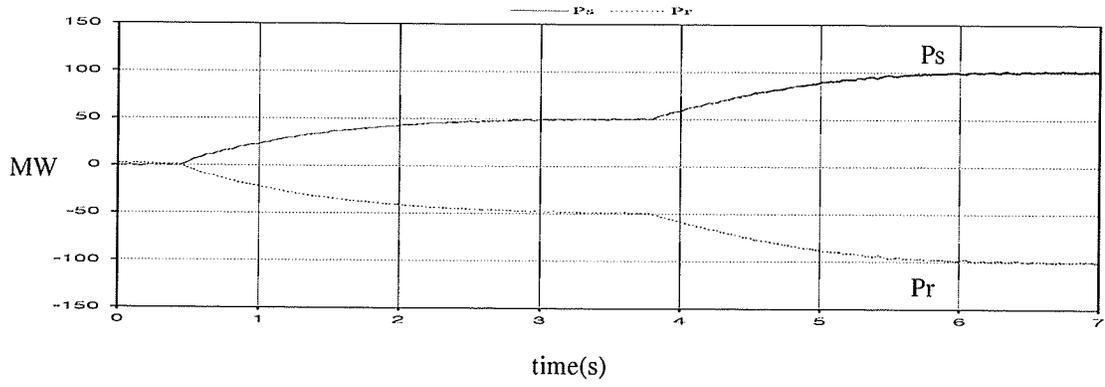
Figure 2.9 Power flow in the system
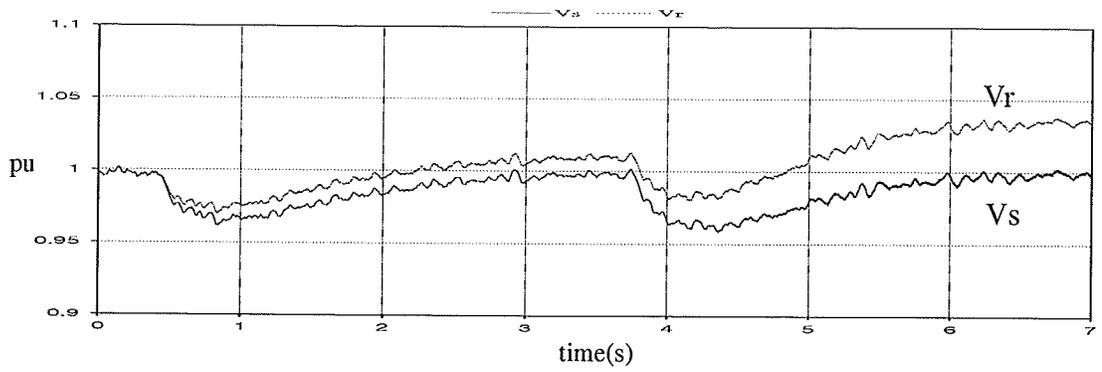
Figure 2.10 Bus voltages in both sides
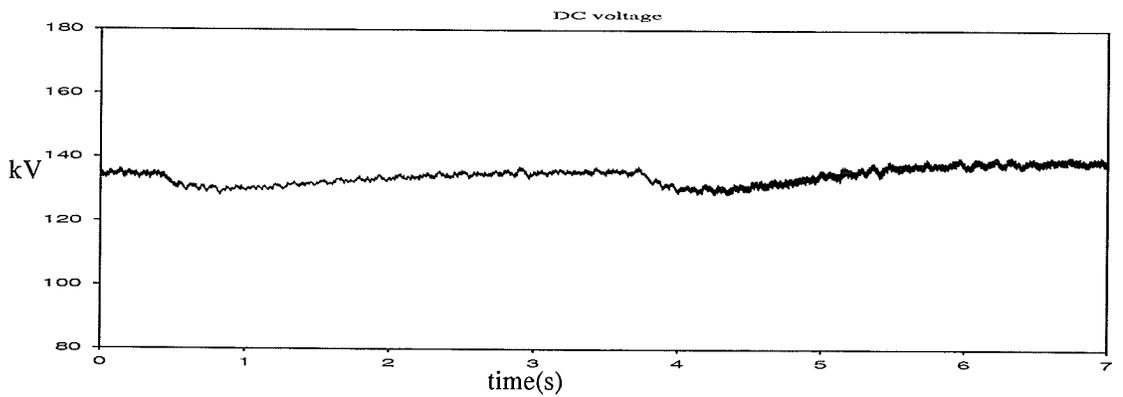
Figure 2.11 Fixed capacitor voltage
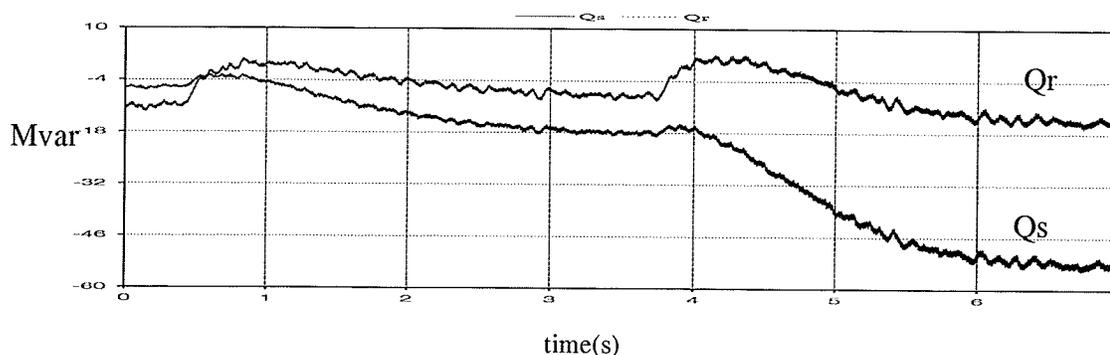
Figure 2.12   Reactive power flow in the system

2.5.2 Power reversal, transformer tap changer and leakage effect

Figure 2.13 indicates that this kind of design can easily exchange the power bidirectionally. From the Figure 2.10, there is a slight difference between the voltage of sending and receiving sides because the voltage control loop is placed at the receiving end only. This problem can be solved through the use of a transformer tap changer or through the adjustment of the transformer leakage as described in 2.3. Figure 2.14 shows that both the sending and the receiving end voltages will be well maintained at 1 pu with a tap changer when power flows in both direction. The transformer tap change data at the receiving end is shown in Table 2.

Table 2: Transformer tap charge data in the receiving end

Real power transferred (pu)	Transformer ratio (pu)
-1.0	0.97
-0.5	0.99
0	1.0
0.5	1.01
1.0	1.04
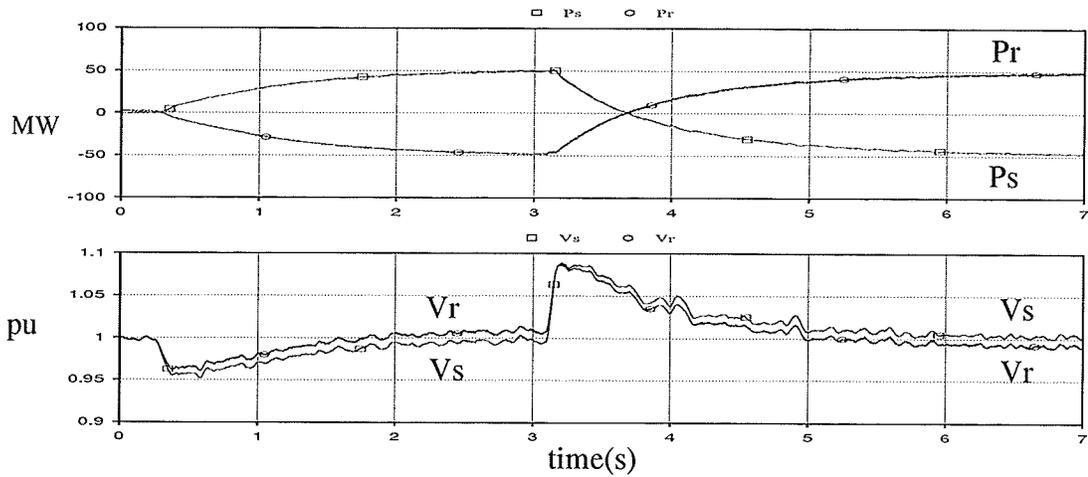
Figure 2.13   Power reversal
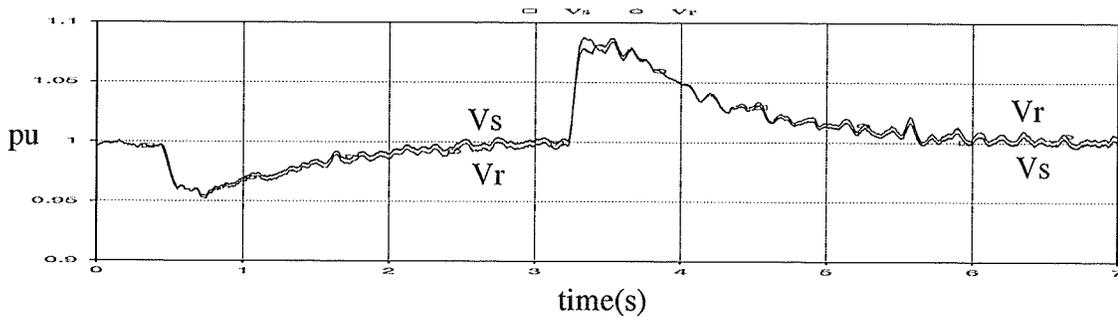
Figure 2.14 Fixed receiving end bus voltage by tap change

Figure 2.15 illustrates the bus voltages when the different transformer leakages are chosen at the receiving end in a bidirtional power flow situation. It indicates that when X_{tr} is increased from 0.10pu to 0.18pu and 0.25pu, the difference decreased in the bus voltage are very small. This is because X_{tr} is just a very small proportion of whole ac system's impedance. Therefore, it may not be an effective way to adjust the bus voltage of the receiving end by varying the transformer leakage in a very weak system.
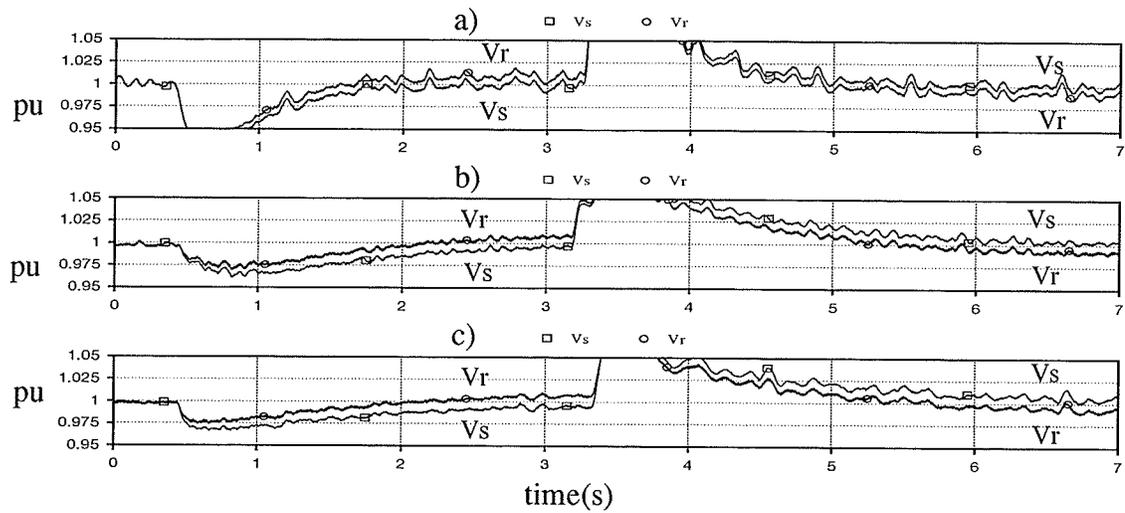
Figure 2.15 Bus voltages when: a) X_{tr}=o.1pu, b) X_{tr}=o.18pu, c) X_{tr}=o.25pu

2.5.3 Coordinated control

Figure 2.16 gives the simulation results with a multiplier, M=2.0. It indicates that the transient performance is better compared with the independent operation (M=0), especially for the dc voltage. However, graph (b) reveals the over-compensation during the transient.

Figure 2.17 gives the simulation results with a multiplier, M=1.0. That is, the rate of change of δ_s used is same as that of δ_r. The simulation results show that the transient performance is improved greatly, which does not seem to match with what is described in section 2.2. Hence, more detail analysis should be done in the future work.

However, during the transient process, the coordinated control has a clear advantage.
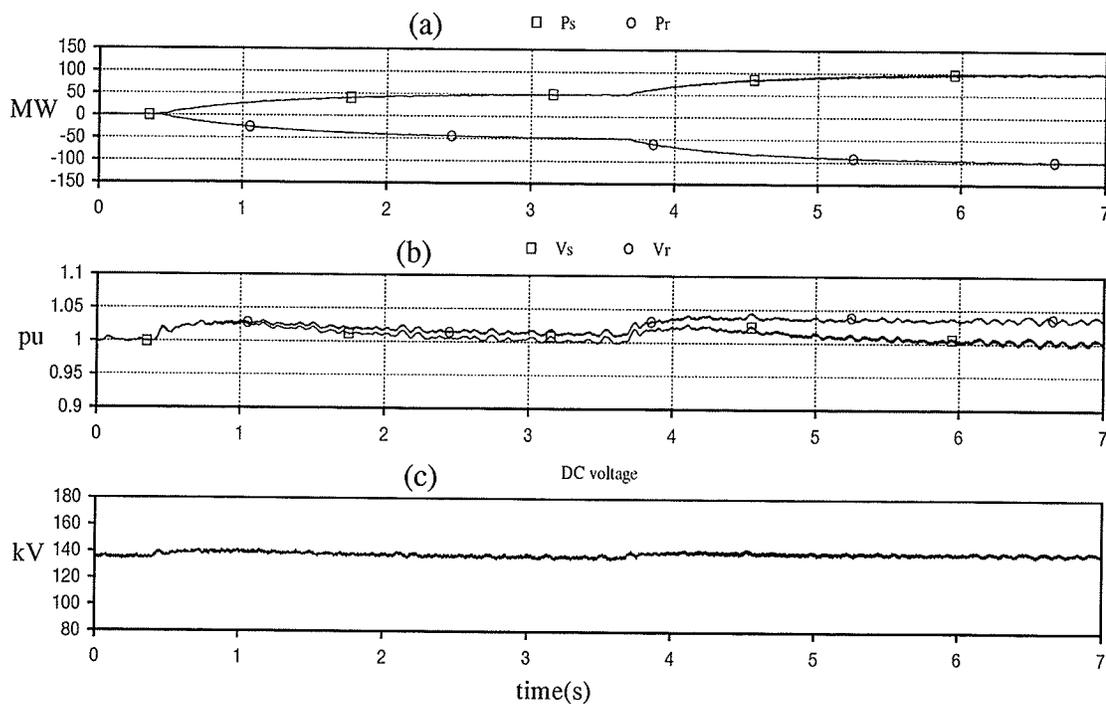
Figure 2.16   Simulation results with M=2.0
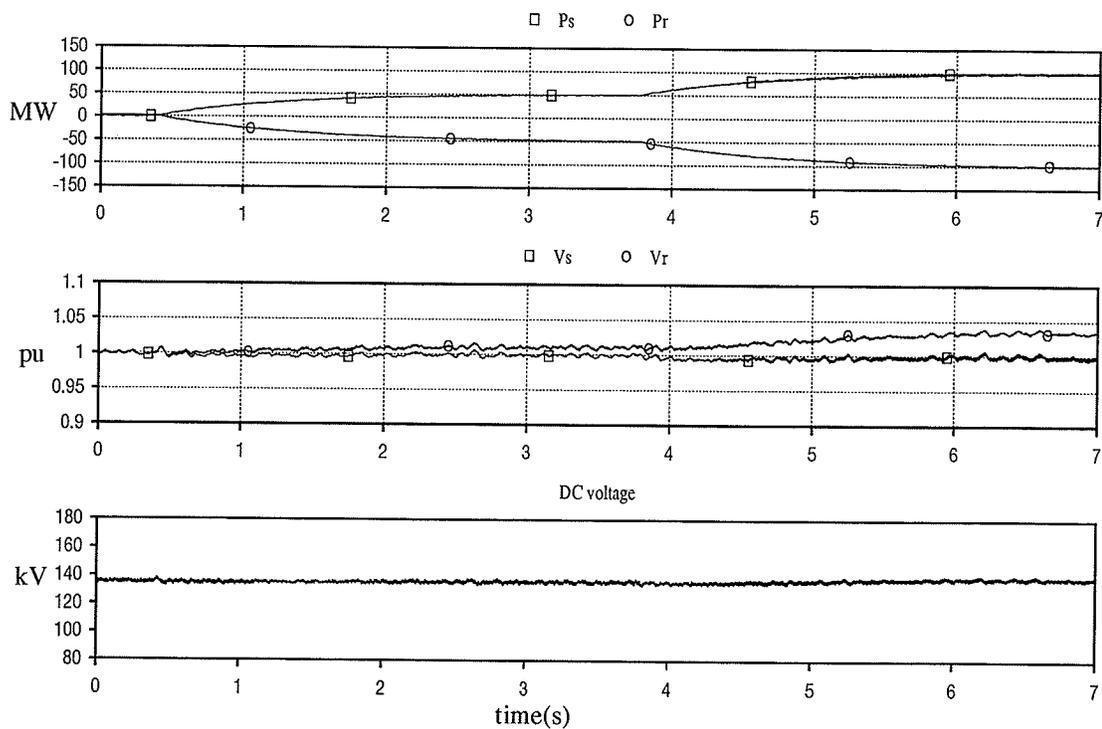
Figure 2.17   Simulation results with M=1.0

Figure 2.18 and Figure 2.19 are the sending end converter voltage and the system

voltages at both sides for the power transfer of 50 MW in the steady state. As the sending

and receiving source voltage are in phase, the converter voltages must be phase shifted to

provide the power transfer along the transmission lines.

Figure 2.20 shows the currents in the two ac systems which contain many harmonics.

Figure 2.21 illustrates the harmonic spectrum of the sending current which contains a

relatively large amount of 5th and 7th harmonics. In the next chapter, it will be shown that

the harmonic components can be significantly reduced by using the multi-level STATCOM
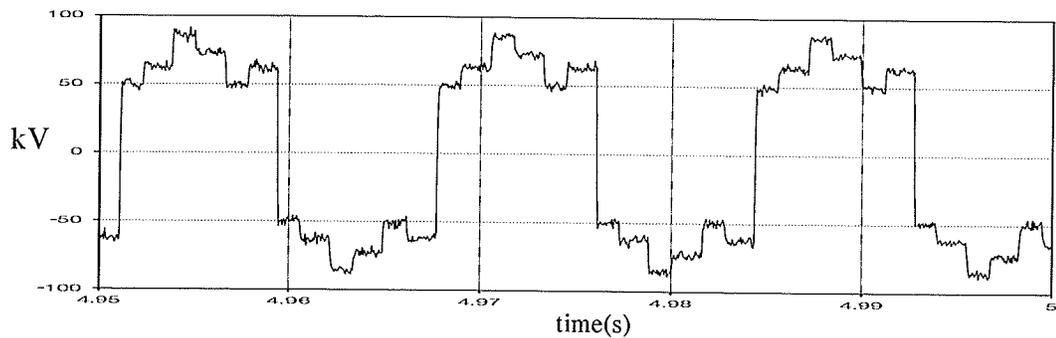
Figure 2.18 Converter voltage in the sending end
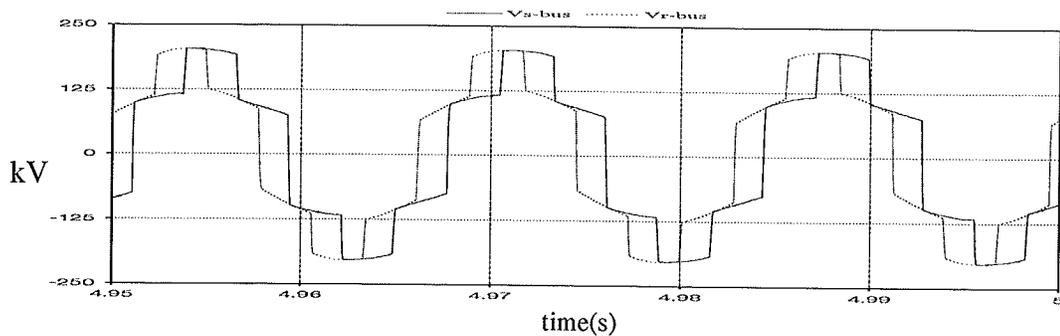
Figure 2.19 System voltages in both sides
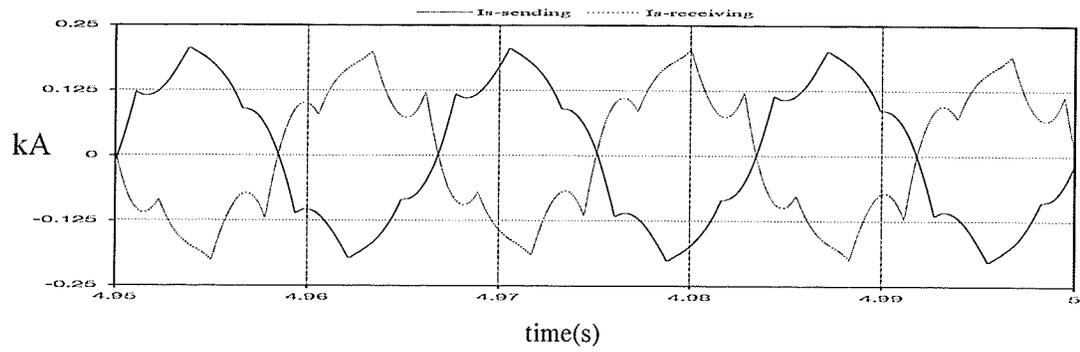
Figure 2.20   Currents in the two ac systems
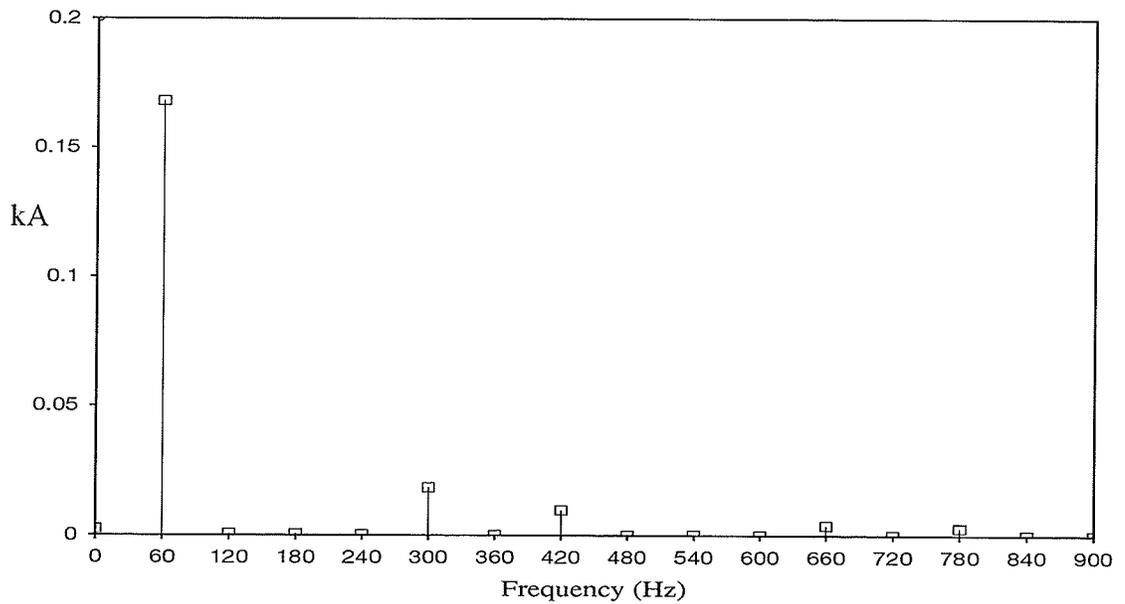
Figure 2.21 Harmonic spectrum of the sending current

Five-level BTB voltage source converter

3.1 THE STUDY SYSTEM

In order to investigate the behaviour of a multi-level STATCOM used for a back-to-back link, two identical five-level STATCOMs were connected on the dc side as shown in Figure 3.1. The same ac systems were chosen for the purpose of comparison. Generally speaking, the operating principle of the multi-level STATCOM is the same as the six-pulse two-level back-to-back converter outlined in the previous chapter. As is known, in order to ensure the STATCOMs will function well during disturbances, it is very important to maintain the dc voltage of the inverter in a certain range and keep it stable. However, the voltages of the two inner capacitors, C2 and C3, tend to be greater than the two outer capacitors, C1 and C4. A system convergence problem will be caused when the voltage difference between the inner and outer capacitor approaches the limit. Therefore, the main problem to be solved with the five-level BTB converter is the 'voltage unbalance' problem. A capacitor voltage balance control loop must be designed in addition to the bus voltage control loop and power flow control loop.
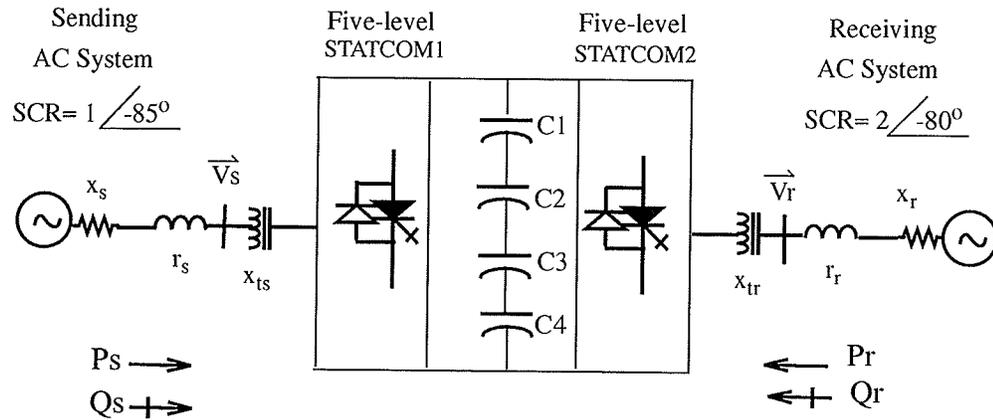
Figure 3.1 Simplified five-level back-to-back scheme

3.2 VOLTAGE UNBALANCE PROBLEM

3.2.1 Unbalance capacitor voltages

In this section, a theoretical calculation is presented which proves that the charge current of the outer capacitor isn't same as the inner capacitor's in the steady state for the five-level BTB converter case.

A simplified circuit is shown in Figure 3.2 and the output waveform is shown in Figure 3.3.
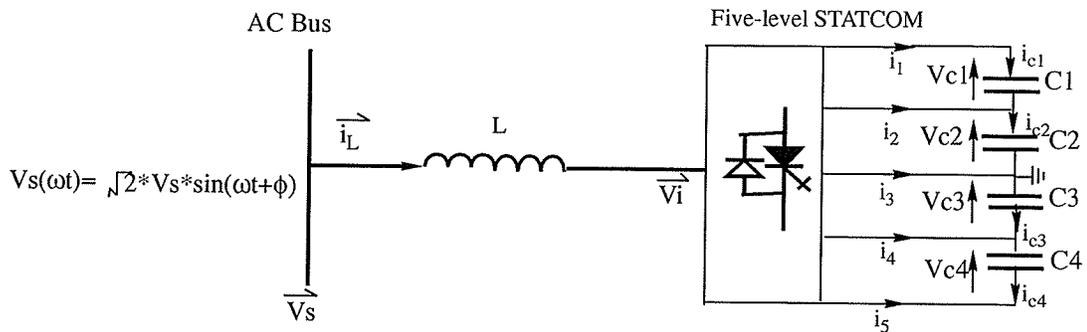
Figure 3.2 Simplified circuit of five-level BTB converter

$$*\qquad \begin{aligned} Vc1 &= V1\text{-}V2 \\ Vc2 &= V2\text{-}V3 \\ Vc3 &= V3\text{-}V4 \\ Vc4 &= V4\text{-}V5 \end{aligned}$$
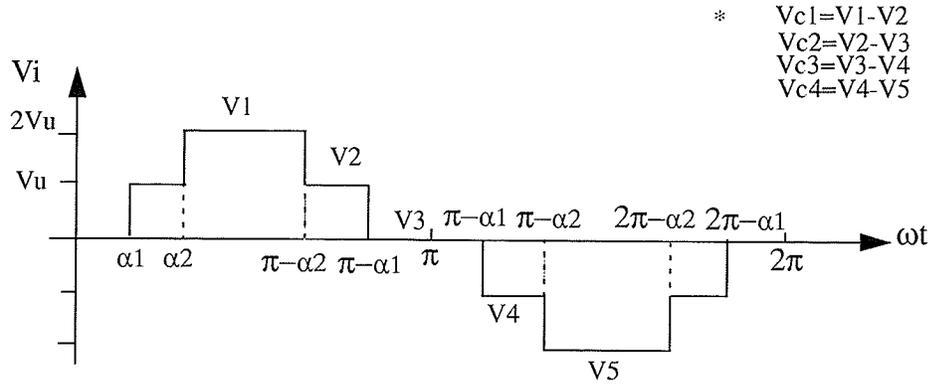
Figure 3.3   Phase voltage waveform of a five-level converter

According to the Fourier Analysis:

$$Vi\,(\omega t) = \frac{4Vu}{\pi} \cdot \sum_{n}^{\infty} \frac{1}{n} \cdot [\cos(n\alpha 1) + \cos(n\alpha 2)] \cdot \sin(n \cdot \omega t)$$

where n=1,3,5......

Fundamental voltage will be: $Vi1\,(\omega t) = \dfrac{4Vu}{\pi} \cdot [\cos(\alpha 1) + \cos(\alpha 2)] \cdot \sin(\omega t)$

Assume the input current has two components, inphase and quadreture:

$$i_L\,(\omega t) = \hat{I}_r \cdot \sin(\omega t) + \hat{I}_x \cdot \cos(\omega t)$$

1) Average current in each branch:

$$\overline{i_1(\phi)} = \frac{3}{2\pi} \cdot \int_{\alpha 2}^{(\pi - \alpha 2)} i_L\,(\omega t)\,d(\omega t) \qquad = \frac{3 \cdot \hat{I}_r}{\pi} \cdot \cos(\alpha 2)$$

$$\overline{i_2(\phi)} = \frac{3}{2\pi} \left[\int_{\alpha 1}^{\alpha 2} i_L\,(\omega t)\,d(\omega t) + \int_{(\pi - \alpha 2)}^{(\pi - \alpha 1)} i_L\,(\omega t)\,d(\omega t) \right]$$

$$= \frac{3 \cdot \hat{I}_r}{\pi} \cdot [\cos(\alpha 1) - \cos(\alpha 2)]$$

$$\overline{i_3(\phi)} = \frac{3}{2\pi}\left[\int_0^{\alpha 1} i_L(\omega t)\,d(\omega t) + \int_{(\pi-\alpha 1)}^{(\pi+\alpha 1)} i_L(\omega t)\,d(\omega t) + \int_{(2\pi-\alpha 1)}^{(2\pi)} i_L(\omega t)\,d(\omega t)\right]$$

$$= 0$$

$$\overline{i_4(\phi)} = \frac{3}{2\pi}\left[\int_{(\pi+\alpha 1)}^{(\pi+\alpha 2)} i_L(\omega t)\,d(\omega t) + \int_{(2\pi-\alpha 2)}^{(2\pi-\alpha 1)} i_L(\omega t)\,d(\omega t)\right]$$

$$= \frac{-3\cdot \hat{I}_r}{\pi}\cdot[\cos(\alpha 1) - \cos(\alpha 2)] = -\overline{i_2(\phi)}$$

$$\overline{i_5(\phi)} = \frac{3}{2\pi}\cdot\int_{(\pi+\alpha 2)}^{(2\pi-\alpha 2)} i_L(\omega t)\,d(\omega t) = \frac{-3\cdot \hat{I}_r}{\pi}\cdot\cos(\alpha 2) = -\overline{i_1(\phi)}$$

2) Average current in each capacitor:

$$\overline{i_{c1}(\phi)} = \overline{i_1(\phi)} = \frac{3\cdot \hat{I}_r}{\pi}\cdot\cos(\alpha 2)$$

$$\overline{i_{c2}(\phi)} = \overline{i_1(\phi)} + \overline{i_2(\phi)} = \frac{3\cdot \hat{I}_r}{\pi}\cdot\cos(\alpha 1)$$

$$\overline{i_{c3}(\phi)} = \overline{i_4(\phi)} + \overline{i_5(\phi)} = \frac{-3\cdot \hat{I}_r}{\pi}\cdot\cos(\alpha 1)$$

$$\overline{i_{c4}(\phi)} = \overline{i_5(\phi)} = \frac{-3\cdot \hat{I}_r}{\pi}\cdot\cos(\alpha 2)$$

3) Power flow into each capacitor:

$$\overline{P_{c1}} = \overline{Vu}\cdot\overline{i_{c1}(\phi)} = \frac{3\cdot \hat{I}_r}{\pi}\cdot Vu\cdot\cos(\alpha 2) \qquad\qquad \ldots\ldots\ldots\ldots\ldots\ldots(3\text{-}1)$$

$$\overline{P_{c2}} = \overline{Vu}\cdot\overline{i_{c2}(\phi)} = \frac{3\cdot \hat{I}_r}{\pi}\cdot Vu\cdot\cos(\alpha 1) \qquad\qquad \ldots\ldots\ldots\ldots\ldots\ldots(3\text{-}2)$$

$$\overline{P_{c3}} = \overline{Vu}\cdot\overline{i_{c3}(\phi)} = \frac{-3\cdot \hat{I}_r}{\pi}\cdot Vu\cdot\cos(\alpha 1) \qquad\qquad \ldots\ldots\ldots\ldots\ldots\ldots(3\text{-}3)$$

$$\overline{P_{c4}} = \overline{Vu}\cdot\overline{i_{c4}(\phi)} = \frac{-3\cdot \hat{I}_r}{\pi}\cdot Vu\cdot\cos(\alpha 2) \qquad\qquad \ldots\ldots\ldots\ldots\ldots\ldots(3\text{-}4)$$

From the equations (3-1) (3-2) (3-3) (3-4), it can be see that the power flows into each capacitor is not same since $\alpha 1$ and $\alpha 2$ are not equal. For this study, $\alpha 1 = 5.14°$ and

$\alpha2=30.86^{\circ}$. The energy flows into C2 and C3 are bigger than into C1 and C4. Therefore, the voltages across the C2 and C3 tend to be greater than those across C1 and C4. This is the reason why a voltage balance control loop is necessary in five-level BTB converter situation.

3.2.2 Design principle of voltage balance control loop

In order to maintain the four capacitor voltages at the same value, a voltage balance control loop is needed. The principle of it can be explained as follow:

Let:

$$V_{ref} = \frac{(V_{c1} + V_{c2} + V_{c3} + V_{c4})}{4}$$

and

$$\Delta_1 = V_{c1} - V_{ref}$$
$$\Delta_2 = V_{c2} - V_{ref}$$
$$\Delta_3 = V_{c3} - V_{ref}$$
$$\Delta_4 = V_{c4} - V_{ref}$$

Δ_1, Δ_2, Δ_3, Δ_4 are fed to regulators of the voltage balance control loop. And, $\delta_1, \delta_2, \delta_3, \delta_4$ are corresponding output signals of regulators of the voltage balance control loop which are used to adjust the firing angles of both STATCOM1 and STATCOM2.

Assume that the real component of the line current with respect to Figure 3.3 is:

$$i_s(\omega t) = \sqrt{2} \cdot I \cdot \sin(\omega t)$$

During the range, $(\alpha_2 + \delta_1) \sim (\pi - \alpha_2 - \delta_1)$, the current i_s flows into the capacitor C1.
During the range, $(\alpha_1 + \delta_2) \sim (\pi - \alpha_1 - \delta_2)$, the current i_s flows into the capacitor C2.

The change of the voltage across the capacitor in one cycle will be:

$$V_{c1} = \frac{1}{C} \cdot \int_{(\alpha_2 + \delta_1)}^{(\pi - \alpha_2 - \delta_1)} \sqrt{2} \cdot I \cdot \sin(\omega t)\, d\omega t$$

$$= \frac{2\sqrt{2} \cdot I}{C} \cdot \cos(\alpha_2 + \delta_1)$$

....................(3-5)

Similarly:

$$V_{c2} = \frac{1}{C} \cdot \int_{(\alpha_1 + \delta_2)}^{(\pi - \alpha_1 - \delta_2)} \sqrt{2} \cdot I \cdot \sin(\omega t)\, d\omega t \qquad \qquad \dots\dots\dots\dots\dots(3\text{-}6)$$

$$= \frac{2\sqrt{2} \cdot I}{C} \cdot \cos(\alpha_1 + \delta_2)$$

Therefore, when Vc1 tends to be smaller than the reference value, the negative Δ_1 produces a negative δ_1 which is added to the firing system of STATCOM1 to increase the conducting time of GTO thyristors, $Q_1 Q_2$, Q_3, Q_4, and provide more charge to C1. From the Equ. (3-5), Vc1 will eventually increase with negative δ_1. If Vc2 tends to be larger, the positive δ_2 is added to the firing system of STATCOM1 to decrease the conducting time of GTO thyristors, Q_2, Q_3, Q_4, Q'_1. From the Equ. (3-6), Vc2 will decrease to approach the reference value. The same thing will occur for Vc3 and Vc4.

For the receiving side, if Vc1 is smaller than the reference value, it indicates that less power should be taken out from C1, and the conduction time of corresponding GTO thyristors, Q_{11}, Q_{21}, Q_{31}, Q_{41}, of STATCOM2 should be shorter than usual. Therefore negative values of the δs should be added to the firing system of STATCOM2.

This design has been based on the assumption of unidirectional power flow. If the power flow is reversed, then the sign of the Δ must also be reversed.

3.3 CONTROL STRATEGIES

In the five-level BTB converter design, not only must the bus voltage be controlled at the desired level with the real power flowing, but in addition the four capacitor voltages must be controlled at the same value all the time, or at least, within a small margin. Therefore the control strategies are more complicated than for the six-pulse two-level type of STATCOM [14]. The two main control loops of this device shown in Figure 3.4 and Figure 3.5 are the voltage control loop in the sending end and the real power control loop at the receiving end. As these control loops are slightly different than those used previously, their function will be briefly described. The Phase Lock Loop1 (PLL1) maintains synchronism between the output voltage of the PLL1 and the ac system voltage at the sending end. The input of the PI1 controller is the error signal derived from the difference between the RMS value of the measured ac system voltage and the voltage reference. The output of the PI1 controller is added to the output of the PLL1 to adjust the firing signal fed to the Gate Drive Logic. A measured voltage lower than the reference voltage produces a negative error signal which is fed to the regulator, PI1, and delays the firing signal of STATCOM1. This causes real power to flow into STATCOM1 and to charge the dc capacitors.

Figure 3.5 is the power control loop which is similar to the voltage control loop. PLL2 is used to synchronize the output voltage of the PLL2 and the ac system voltage at the receiving end. The input to PI2 is the error signal of the measured real power and reference real power. The output of PI2, PLL2 and a auxiliary input signal which is used for the purpose of the dynamic adjustment are added together to adjust the firing angles of the

STATCOM2.
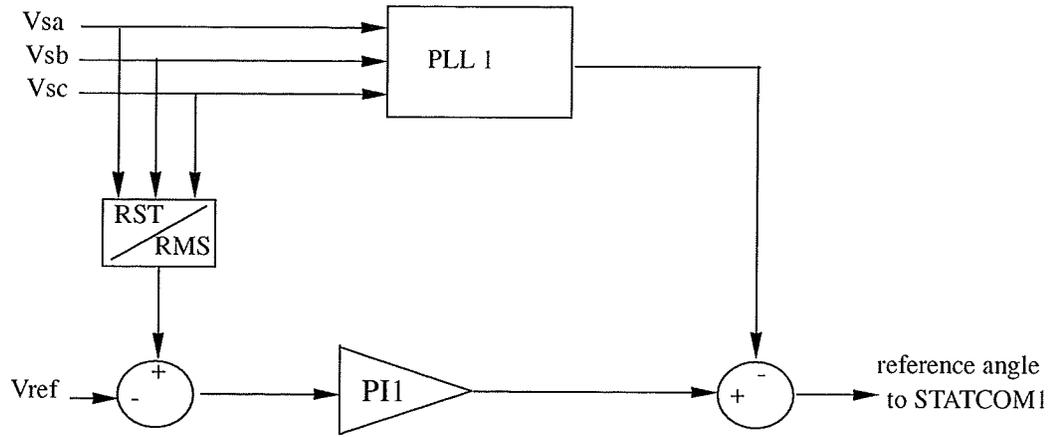
Figure 3.4 Voltage control loop
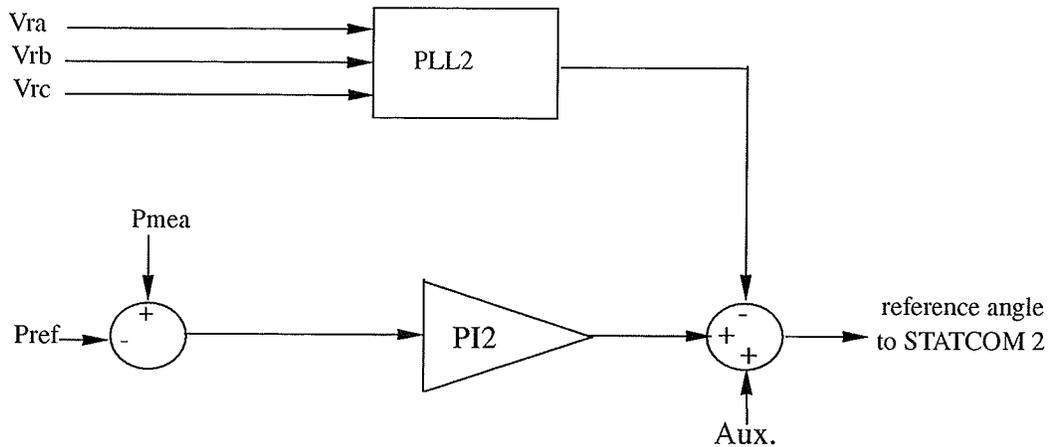
Figure 3.5 Real power control loop

Besides the above controls, the capacitor voltage balance control loop has to be designed

so that the four capacitor voltages can be maintained at the same level. The principle of

voltage balance control is described in the previous section.

Figure 3.6 illustrates the voltage balance control loop. Since the real values of

Vc1,Vc2,Vc3,Vc4 contain ac components [19], the 90Hz, 180Hz, 360Hz filters are used

here. The average value of the four capacitor voltages is chosen to be the reference and each measured capacitor voltage is compared with the reference value. The error signals are fed to a PI controller. According to the sign of power flow direction, the outputs of the PI controllers are used to adjust slightly the firing angles of the STATCOM1 and STATCOM2. The limits applied on those PI controllers are to keep the harmonics within a desired range.
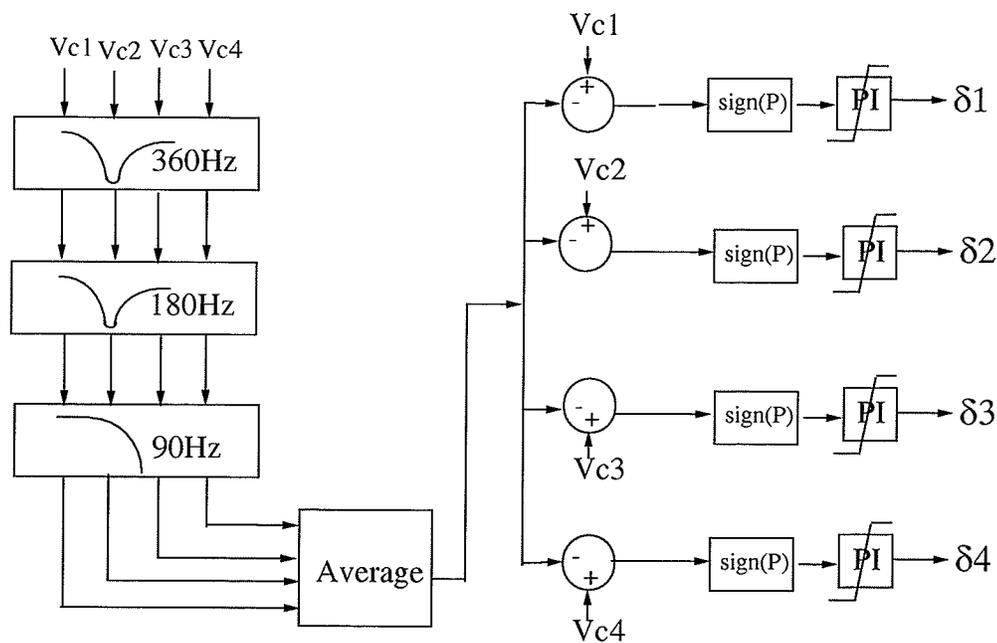
Figure 3.6   Voltage balance control loop

3.4 SIMULATION RESULTS

The simulation results have been carried out on the model described in Figure 3.1 by using the EMTDC^{TM} program. Figure 3.7 shows that the real power exchanged between

the sending end and the receiving end is the same as in a six-pulse two-level inverter. The power is controlled very smoothly.

Corresponding to the power transfer in Figure 3.7, Figure 3.8 presents the rms value of the voltages at both bus terminals, which are well maintained at expected levels.

Figure 3.9 indicates that the dc voltages across the four capacitors are effectively kept at a constant value through the voltage balance control loop; the action of which is shown in Figure 3.10. The maximum amount of adjustment that can be made to the δs is just 0.01 radians, that is 0.57° degrees, which does not have a big effect on harmonic distortion, and the re-introduction of the 5th and 7th harmonics. It is clear that the ripple current of the capacitors becomes larger as the amount of the real power transferred is increased. Also the voltage value of each capacitor is one-fourth that of the six-pulse two-level design because the peak line voltage at the transformer secondary side is spanned by four capacitors. This indicates the size of the energy storage elements required in a five-level BTB converter design can be much less compared with a six-pulse two-level design, which is one of major advantages of the multi-level STATCOM.

Figure 3.11 shows the reactive power required in both sides when 0.5pu and 1.0 pu of real power is transferred in the system. Theoretically, the reactive power demands for the same amount of real power transfer with the same ac systems should be same as for the two-level case. However, the six-pulse two-level BTB system contained large 5th and 7th harmonic components, which generated more reactive power. Hence, this graph is not exactly same as Figure 2.11.

Figure 3.12 and Figure 3.13 clearly show the phase shift produced by the converters and

the stepped output voltage waveforms. The converter currents are quite sinusoidal as shown in Figure 3.14. Especially when they are compared to the six-pulse two-level converter current shown in Figure 2.19.

Figure 3.15 shows the harmonic spectrum of the current in the sending end, in which the biggest harmonic is the 11th as expected.

Figure 3.16 gives some simulation results when the voltage balance control loop is not applied. It shows that Vc2 and Vc3 tend to be bigger than Vc3 and Vc4 because of unequal average charge or discharge current of those four capacitors as described in 3.2.2.
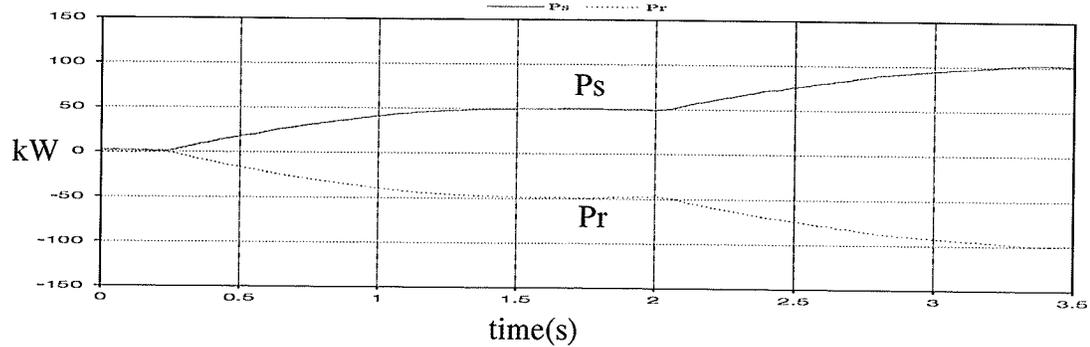
Figure 3.7   Power exchanged in the five-level BTB converter
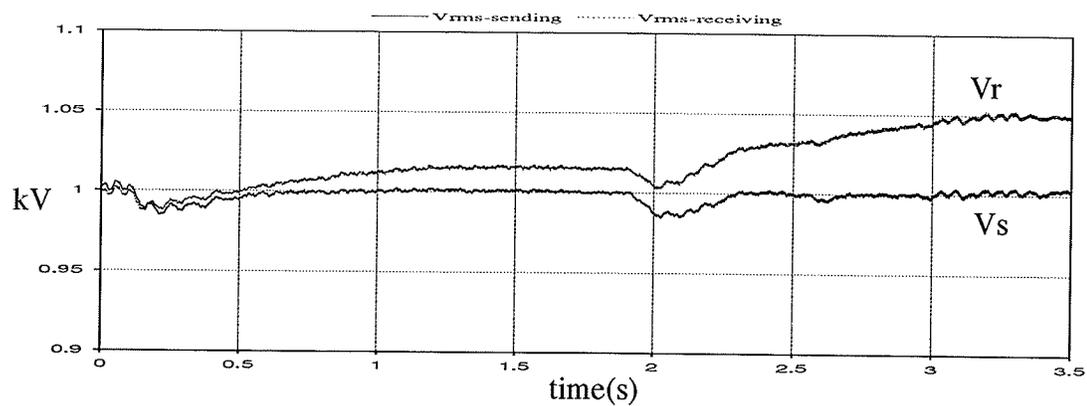
Figure 3.8   Bus voltages in the five-level BTB converter
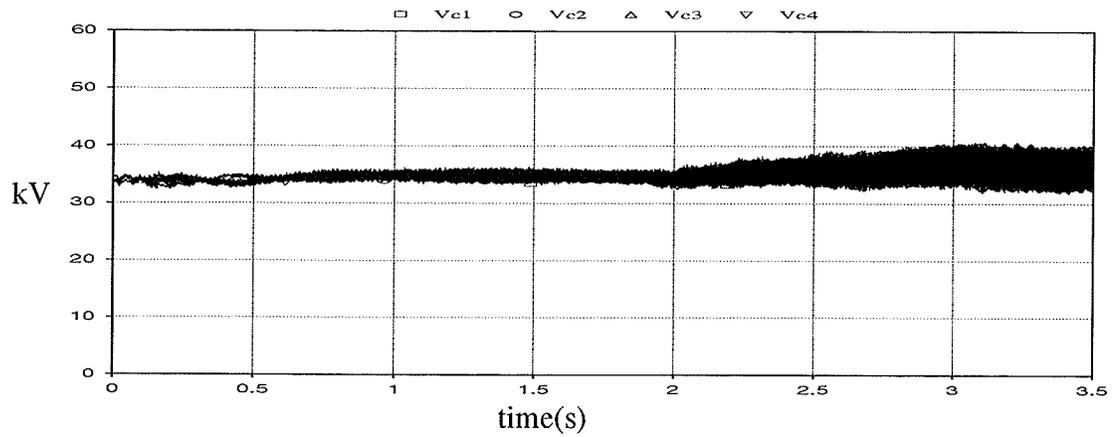
Figure 3.9 Four capacitor voltages in five-level BTB converter
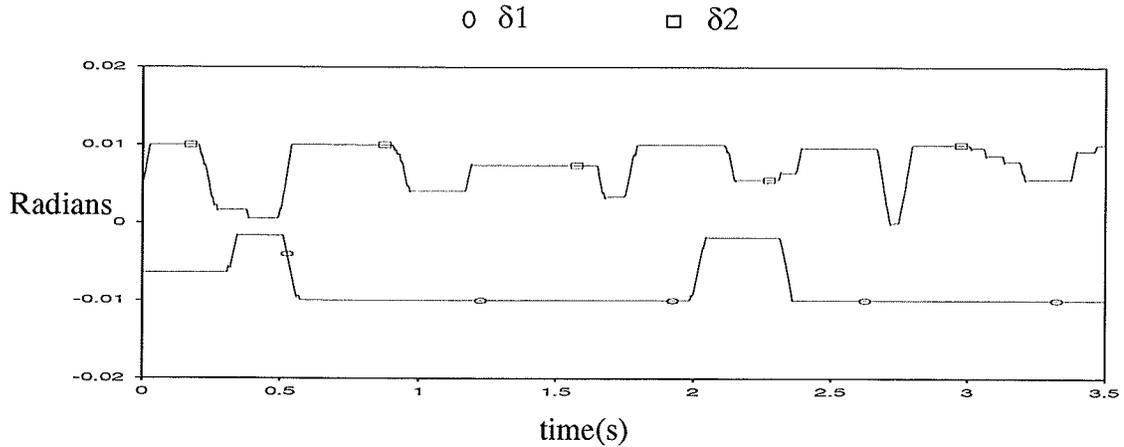
Figure 3.10   Modified amount of firing angles
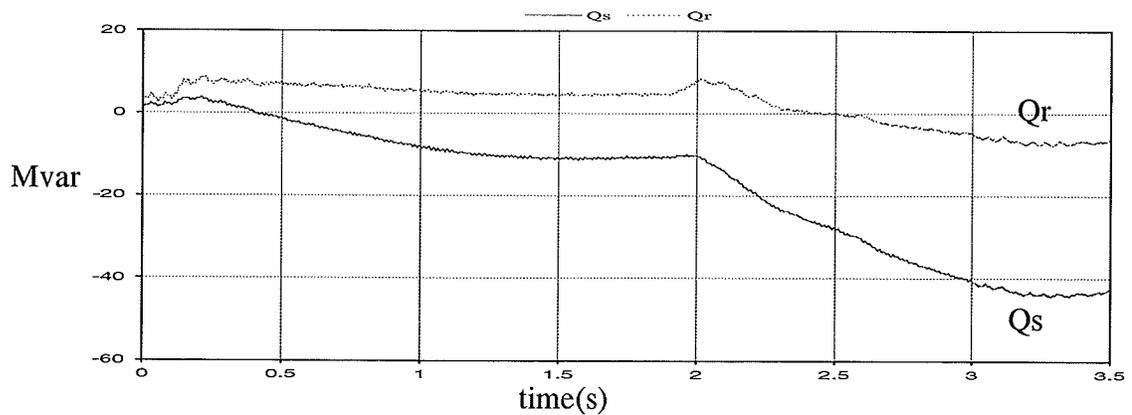
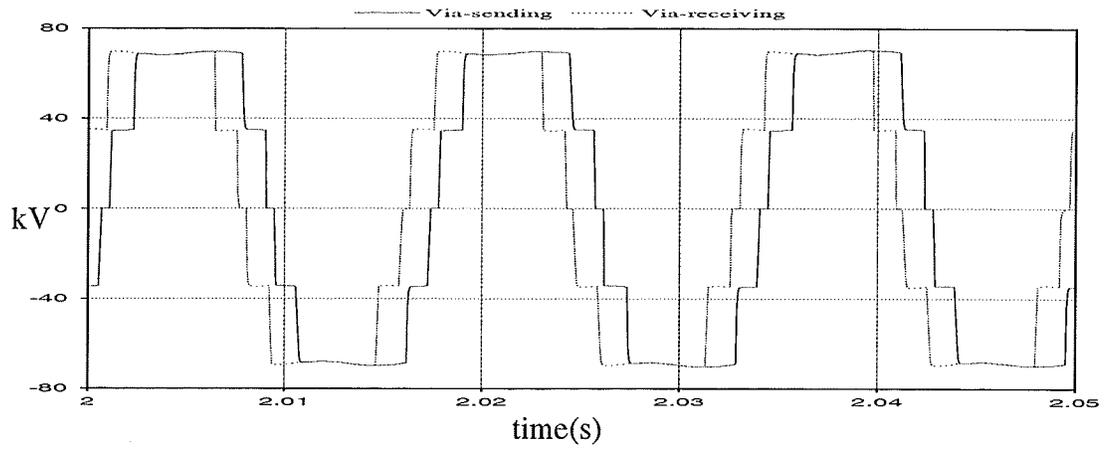Figure 3.11   Reactive power flow in five-level BTB system

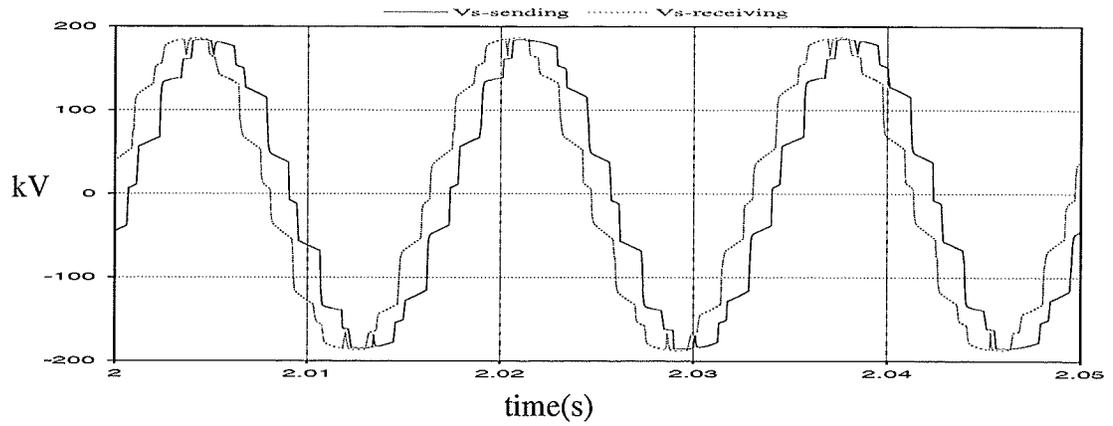Figure 3.12   Converter voltages on both sides
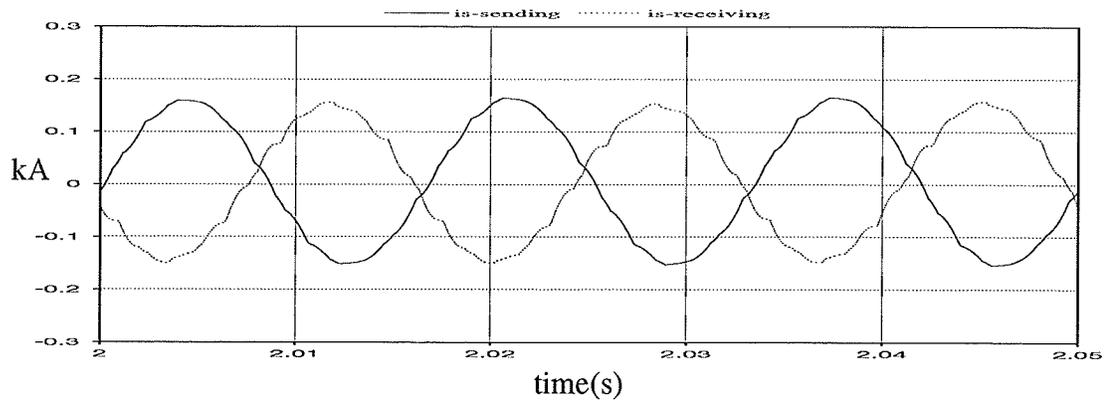

Figure 3.13 Bus voltages on both sides
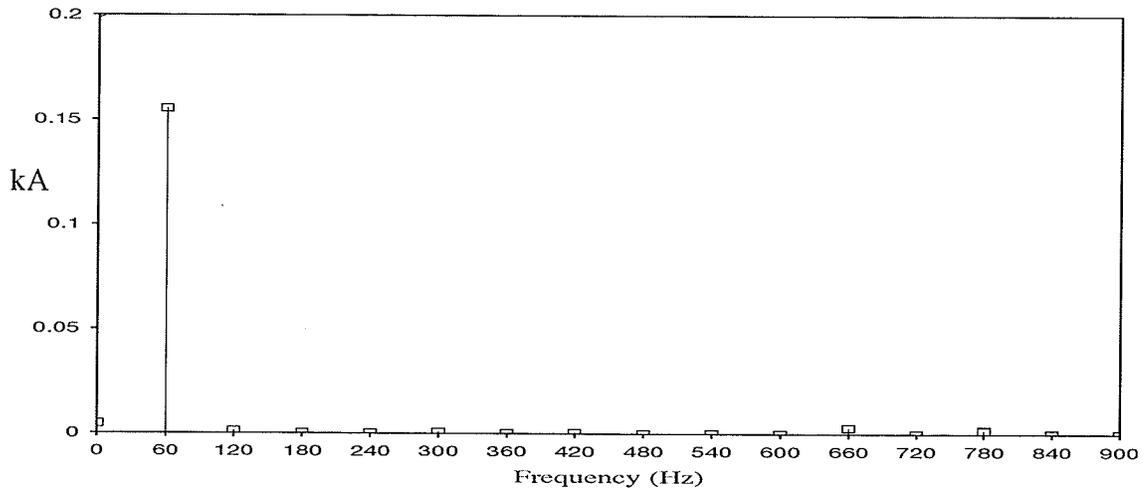

Figure 3.14   System currents on both sides

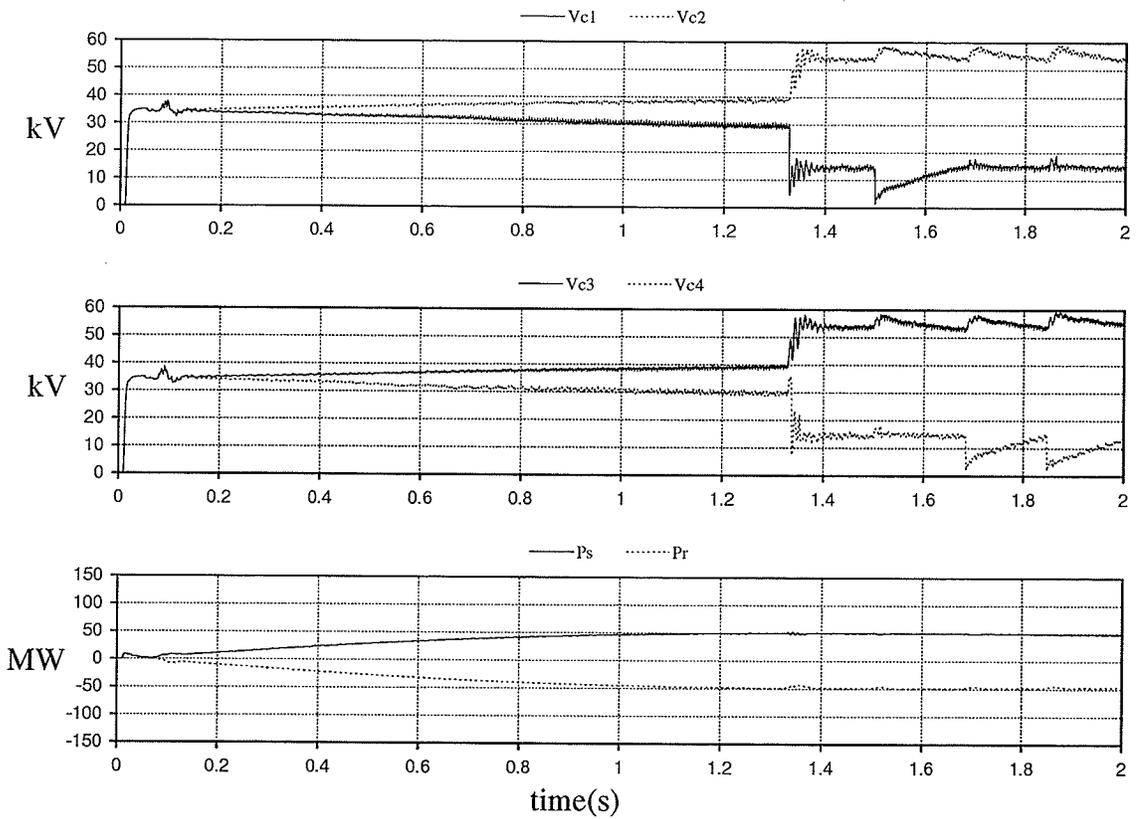Figure 3.15 Harmonic Spectrum of the sending current

Figure 3.16   DC voltages without voltage balance control

3.5 COMPARISON

Based on the above analysis and simulation results, it is clear that both STATCOM designs can be connected back-to-back and used for real power transfer. They could be an alternative option for an HVDC converter station. The major differences of these two designs are indicated as below:

1) Compared with output voltage harmonic reduction, the five-level topology has better performance than the two-level topology. Let's define the Harmonic Distortion Factor as the ratio of the magnitude of nth harmonic component to the magnitude of the fundamental component. The Table 3 illustrates the Harmonic Distortion Factor of these two different designs, in which the biggest harmonic content is the 5th, and the second largest is the 7th for a two-level design, while the biggest harmonic content is the 11th and the second largest is the 13th for a five-level design. It is clear that the high-level topology not only shifts the biggest harmonic to a higher order which is much easier to be filtered, but also it can reduce its magnitude significantly. For instance, the biggest harmonic distortion factor for two-level is 10.998% and is 1.845% for a five level.

2) Another advantage of the multi-level design is that there is no series connection of GTO thyristors in the five-level converter design, since just one GTO thyristor is turned on or off at any instant. Also each GTO thyristor just needs to withstand a maximum voltage equal to $(1/4)Vdc$ and not the full dc voltage for a five-level converter situation. This makes the reductions of device voltage ratings possible.

3) Concerning the design of controls, the basic two-level topology is easier to control than a five-level design, because there is no capacitor voltage unbalance problem for the

two-level design.

4) Although the basic two-level BTB converter requires only twelve GTO thyristors and twelve reverse conducting diodes, while the five-level BTB converter needs forty-eighty GTO thyristors and seventy-two diodes, the power rating of the five-level BTB converter is four times that of the two-level with similar GTO thyristors. It should be noted that the current rating of the clamping diodes can be considerably less than that of the reverse conducting diodes. This indicates that the five-level design should not increase the cost of the system.

Table 3: Harmonic comparison between two-level BTB converter and five-level BTB converter

Converter type	Frequency (Hz)	DF (%)
Six-pulse two level BTB converter	120	0.421%
	180	0.370%
	300	10.998%
	360	0.072%
	420	5.768%
	480	0.089%
	600	0.052%
	660	4.685%
	780	1.677%
	840	0.071%
Five-level BTB converter	120	0.723%
	180	0.150%
	300	0.378%
	360	0.119%
	420	0.283%
	480	0.035%
	600	0.040%
	660	1.845%
	780	1.096%
	840	0.071%

A brief test of BTB Converter

4.1 MILES CITY DC LINK WITH BTB CONVERTER

There is a conventional back-to-back DC tie at Miles City,Montana. which serves as an asynchronous connection between the east and west United States - Canadian alternating current (AC) transmission networks. The SCR of west side ac system is 1.56, and the east side SCR is 2.75. The rated power is 200 MW, the bus voltage is 230 kV at both east and west sides. Presently, there is an increased demand for electrical power transfer, but the strength of the ac system limits the use of thyristor converters. In this section, a basic six pulse two-level back-to-back converter was place in parallel with the existing DC tie to investigate the increased transfer capability.

The existing DC tie model based on the real date of Miles City HVDC station with all of the existing reactive support in service was modelled by Mr. Dennis,Woodford, Executive Director of Manitoba HVDC Research Centre. A basic six-pulse two-level back-to-back converter model was added to the Miles City model to investigate the performance of a parallel scheme in back-to-back connection. The complete model is shown in

Appendix B.

Some simulation results are shown in the following pages.

Figure 4.1 gives the performance of the combined existing dc tie and BTB STATCOMs in the steady state;

Graph (a) is the dc power of existing dc tie in which 1 pu represents 200 MW.

Graph (b) is the smoothed dc voltage on the capacitor in which 1 pu represents 83.68 kV.

Graph (c) is the ac bus voltage on both sides.

Graph (d) is the real power transferred in the sending end and receiving end of the two level BTB converter.

Graph (e) is the reactive power corresponding to the real power in graph (d).

Graph (f) is the DC voltage on the capacitor.

A situation where a BTB STATCOMs may be beneficial is simulated in Figure 4.2. The conventional DC tie is blocked for some reason and the shunt capacitors remain in service.

Graph (a) shows the blocked conventional DC tie is carrying zero power.

Graph (b) shows that the paralleled two level BTB converter can still transfer about 70MW real power in this situation, and graph (c) shows the reactive power flow from the ac systems. Since a temporary overvoltage will take place when a dc block of the existing dc link is applied, the two level BTB converter can absorb the reactive power to maintain the bus voltage at the rated value, as shown in graph (d).
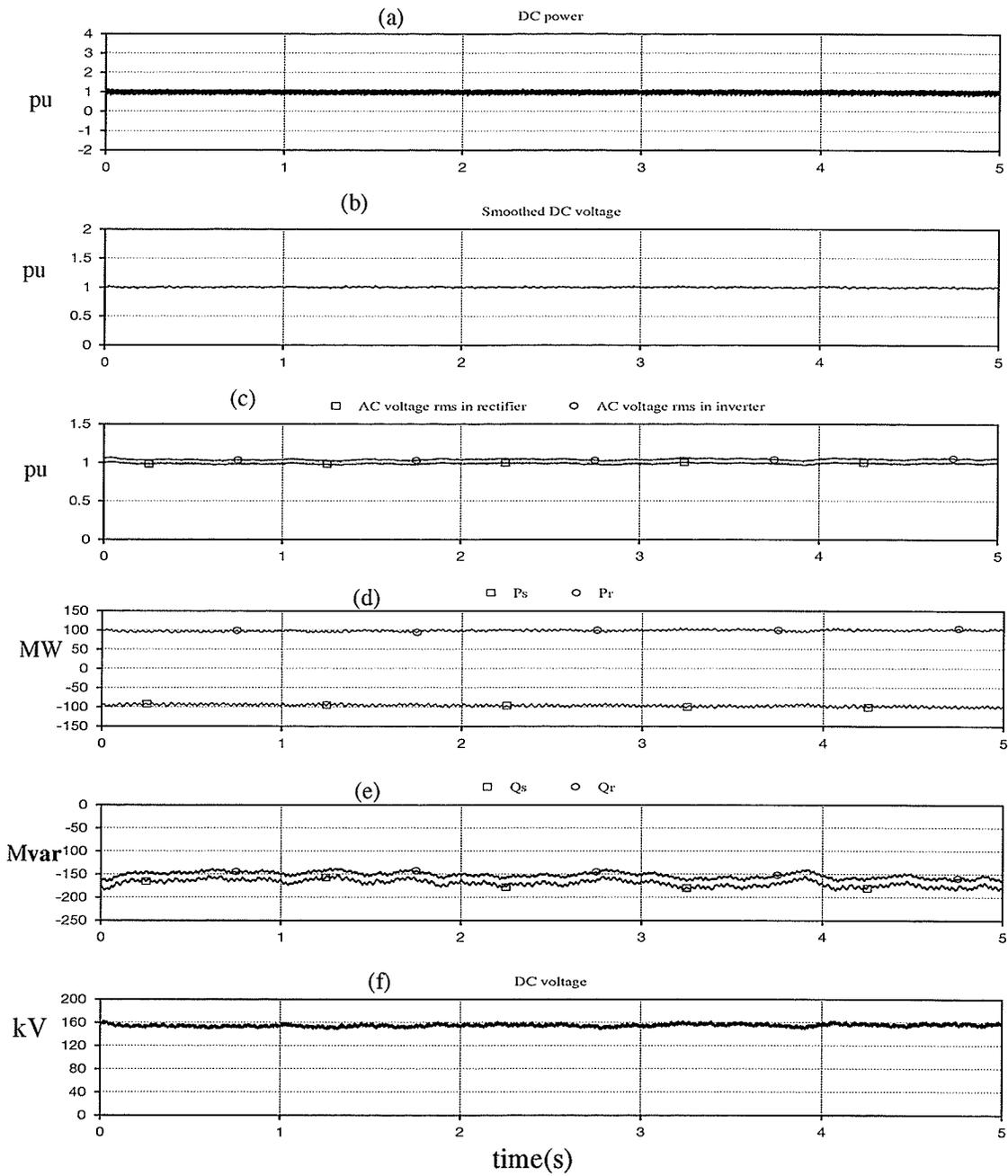
Figure 4.1 Simulation results for a DC tie with a BTB converter in parallel
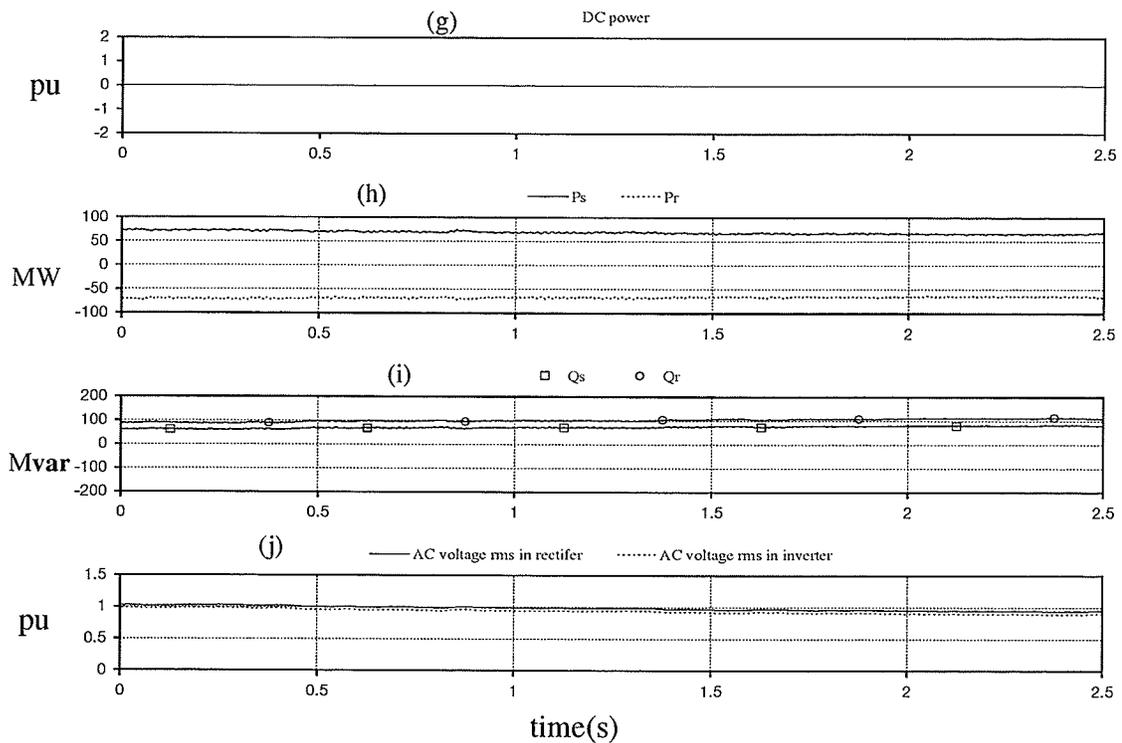
Figure 4.2 System behaves with a blocked conventional DC tie

Based on the above simulation results, it can be seen that a back-to-back STATCOM can increase the power transfer by 50% of the whole system when it is connected in parallel with a conventional HVDC tie. It can also provide the reactive power required to support the bus voltage. In the DC block situation, the BTB STATCOM can absorb a large amount of reactive power while maintaining the bus voltage at the rated level, A transfer of a certain amount of real power can be achieved simultaneously. The dynamic performance of the combined system was not studied since it is out of the scope of this thesis.

Conclusions and Future work

5.1 CONCLUSIONS

The study of the feasibility of a back-to-back STATCOM for asynchronous power transfer opens a new prospect of BTB HVDC applications in power systems. Simplified models of BTB voltage source converters, using the basic six-pulse two-level STATCOM and the five-level STATCOM have been developed, and a real situation of a BTB HVDC STATCOM in parallel with an existing BTB HVDC link in Miles City has been simulated. The studies presented in this thesis revealed the aspects of the design, control, dynamic performance and a comparison of a basic six-pulse two-level BTB STATCOM with a five-level BTB STATCOM. In considering lower harmonic distortion and reduced switching losses, only the fundamental frequency switching method (FFS) was considered.

Based on the simulation carried out using those models, the following conclusions can be drawn:

(1) The well known STATCOM not only can function as a reactive power compensator, but also can transfer real power between two very weak ac systems when they are used in

a BTB connection. They may significantly reduce the cost of the BTB HVDC system.

(2) The BTB STATCOM structure can either be used alone as a real power controller, a phase shifter, an interconnection of two asynchronous ac system or in parallel with a existing conventional BTB HVDC station to increase the amount of real power transferred.

(3) Compared to the basic six-pulse two-level BTB structure, the five-level BTB structure has a better performance in harmonic cancellation and switching losses.

(4) Compared to the five-level BTB structure, the two level BTB structure is easily controlled and has no voltage unbalance problems.

(5) The bus voltage on the receiving end can be maintain by either using a transformer tap changer or by choosing the proper leakage reactance of the coupling transformer.

5.2 FUTURE WORK

* More detailed tests should be done when the BTB HVDC STATCOM is connected with an existing HVDC link in parallel. For instance, transient performance, coordinated control, and fault tests should be studied.

* The control strategy adopted in this thesis are one of the many possible strategies. It has been used because it satisfactorily works for the chosen ac system with very low SCR. However, investigating the various possible strategies and evaluating their merits is necessary for a complete work. For example, the widely known pulse-width-modulation switching method may produce a faster control.

* Optimizing the size of the dc capacitor can make this design more economically attractive.

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Appendix A

Parameters of modelling system:

Ac system: 300 MVA

Rated voltage: 230 kV

X_s=0.93 H R_s=30.74 Ω

X_r=0.46 H R_r=30.4 Ω

Transformer: 150 MVA,   230kV/100kV,   Y-Y

Table 4: Parameters of PI regulator of control loop:

Type of converter	Gain	Time constant
Two-level BTB Converter	G_v=2	T_v=0.15
	G_p=0.003	T_p=15
	G_{PPL}=80	T_{PPL}=6
Five-level BTB Converter	G_v=2	T_v=0.05
	G_p=0.2	T_p=10
	G_{PPL}=10	T_{PPL}=4

Appendix B

Configuration of Miles City 200MW dc link with 100MW 2-level VSC