DEEP-LEVEL TRANSIENT SPECTROSCOPY(DLTS) FOR THE DETERMINATION OF TRAP PARAMETERS IN SEMICONDUCTOR DEVICES

by

Li-chao Kuang

A thesis

presented to the University of Manitoba

in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical & Computer Engineering

Winnipeg, Manitoba, 1997

THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

COPYRIGHT PERMISSION

DEEP-LEVEL TRANSIENT SPECTROSCOPY (DLTS) FOR THE DETERMINATION OF TRAP PARAMETERS IN SEMICONDUCTOR DEVICES

BY

LI-CHAO KUANG

A Thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

ABSTRACT

The design principle and the data acquisition processing of a full-curve computerized deep-level transient spectroscopy (DLTS) system are described in detail. This system is more reliable, flexible and accurate than the conventional methods in the determination of deep level traps in semiconductor devices. The procedures for the evaluation of the bulk traps for p-n junctions and for the evaluation of both the bulk traps and interface states for MOS capacitors are fully discussed. For MOS capacitors, the analysis is based on the rate window concept. The method of minimizing the error in determining the trap energy levels from the transient capacitance spectra is given. We have used the MOS capacitors produced in our Materials and Devices Research Laboratory as an example to demonstrate how to use our new DLTS system to determine their trap parameters. It is found that there are two deep trap levels in the semiconductor bulk and that the interface states are distributed in the forbidden gap.

ACKNOWLEDGMENTS

The author is very grateful to Dr. K. C. Kao for his valuable suggestions, guidance and great patience throughout the whole course of this project.

The author appreciates very much the advice and assistance of Dr. D. J. Thomson, and thanks his colleagues of the Materials and Devices Research Laboratory, in particular, Dr. T. T. Chau for their helpful discussion, and also Mr. B. Bourbonnais for his technical support.

The financial support from the Natural Science and Engineering Research Council (NSERC) is gratefully acknowledged.

TABLE OF CONTENTS

TABLE OF FIGURES

CHAPTER 1

INTRODUCTION

Semiconductors (such as silicon, etc.) and insulators (such as SiO_2, etc.), which form electronic devices, contain defects in the bulk as well as at the interfaces when two different materials are made in contact with each other. Generally, there are two main types of defects, namely chemical defects and physical defects. The chemical defects are due to the incorporation of foreign impurities into the material, while the physical defects are due to the defects of crystallographic points (e.g.vacancies, interstitial, etc.) or the defects in the structure (e.g. stacking faults, dislocations, etc.). In general, defects act as traps which may trap either electrons or holes depending upon the nature of the traps. Traps are also classified into shallow traps and deep traps. The activation energy levels for the shallow traps are generally located far from the Fermi-level in the forbidden band gap (i.e. close to the conduction or valence band edges), while those for the deep traps are close to the Fermi-level. Since all traps tend to capture free carriers, they tend to result in the reduction of electrical or photo-conductivities.

Defects resulting from the irregular crystalline structure or impurities inevitably introduced into the material are mainly due to the fabrication processing. However, impurities intentionally introduced into the material in order to create deep traps may produce desirable effects in electronic devices. For example, deep traps created by incorporating gold into silicon act as stepstones to promote recombination of minority carriers in p-n junctions, thus shortening switching times. Impurity photoconductivity detector is another important application of the effects of deep impurity levels in semiconductors. Deep impurity levels are also of use as temperature sensors in thermister-type applications.

Aside from the valuable effects of deep impurity levels, there are other aspects which are undesirable. For example, deep impurity levels are almost inevitably present in large band gap compound semiconductors, and they can result in undesirable trapping, oscillation, and negative differential resistance phenomena that may lead to considerable frustration to the users of these

materials.

Deep impurities levels are generally characterized in terms of capture cross sections or capture probabilities for electrons, holes or photons. Capture cross sections are usually determined from the lifetime measurements, and photon capture cross section from the absorption coefficients at proper wavelengths. This indirectly gives information about the concentrations and the energy levels of traps.

There are many methods available for the measurements of carrier lifetimes. In general, the concentrations of impurities are measured electrically, while their energy levels are determined optically. In both the electrical and the optical measurements it is normally assumed that the defect level in question is the only imperfection in the material or that the presence of the other unwanted levels can be simply ignored since the spectral lines of deep levels are generally broad. However, such assumptions may encounter some difficulties in interpreting results. Furthermore, in the presence of several levels in the forbidden gap or the level distributed in energy, their fractional occupancy, depends very much on the recombination paths which may vary with illumination intensity, temperature, etc.. Indeed, the ideal situation of considering only one single discrete deep level in the forbidden gap is most unlikely to happen, and extra effort is needed to eliminate the multi-level effects from the observed spectra.

However, to meet this challenging situation for characterization of deep impurity levels, a bias-pulse technique called the deep level transient spectroscopy(DLTS) has been developed. This method of characterization of deep traps is capable of providing relatively accurate and rapid information concerning the capture cross section, the concentration and the energy levels of the traps. Unlike most other techniques for the study of deep levels, DLTS emerges as a direct means to understand the deep levels in technologically important semiconductors as well as a major source of technical information about the deep levels. Of course, the interpretation of transient capacitance experiments is strongly linked to the theory of the deep levels in materials.

The main purpose of the present investigation is to study the measurements of the transient capacitance and the ways of interpreting the experimental results. To know the up-to-date development of this DLTS technique, a brief review is given in chapter II. The design and operation of the DLTS system, including a computerized data-acquisition system are described in chapter III. Some experimental results to demonstrate the use of the DLTS system for the characterization of MOS devices and discussion are given in chapter IV. Conclusions are given in chapter V.

CHAPTER 2

REVIEW OF THE PRINCIPLES AND APPLICATIONS OF DEEP-LEVEL TRANSIENT SPECTROSCOPY(DLTS)

Semiconductors and insulators used for electronic devices all contain impurities and physical defects due to structural irregularities. Some impurities, for example, are intentionally introduced into semiconductors in order to form donor or acceptor centers for producing free electrons or holes, or to create deep-level recombination centers to reduce the lifetime of minority carriers. However, some unavoidable impurities and structural irregularities are always inevitably incorporated into semiconductors or insulators during fabrication processing.

The incorporation of impurities results in the formation of trapping states in the forbidden gap. These states with energy levels close to the edge of either the conduction band or the valence band are called the shallow-level impurities, while those with energy levels close to the Fermi level are called the deep-level impurities. Charge carriers in the conduction band or in the valence band tend to fall into the impurity levels and are trapped until they can gain enough energy to escape from the trapping centers.

The characterization of shallow-level impurities is normally carried out by means of both the electrical and the optical methods, which would provide information about the concentration and the energy levels of the impurities. However, for the characterization of deep-level impurities the methods used are generally related to the effects of the charge carriers trapped in the impurity centers, such as those methods involving capacitance-voltage (C-V) characteristics measurements, current-time, or charge-time, or capacitance-time characteristics measurements commonly used for this purpose[1-4],[6-9].

In this chapter we review mainly the method of deep-level transient spectroscopy(DLTS) which, in general, involves capacitance-time characteristics measurements.

2.1 Basic Principles of DLTS

To describe simply the behavior of deep-level traps, we consider the capacitance of a one-sided abrupt p^+n junction, of which the n-side has a doping concentration N_d, a deep-level electron trap concentration N_T and a deep-level hole trap concentration P_T, and both the electron and the hole traps are uniformly distributed throughout the n-side semiconductor with the trap activation energy of E_T as shown in Fig. 2.1. For simplicity, only the trapping events are considered and the generation-recombination events are ignored.

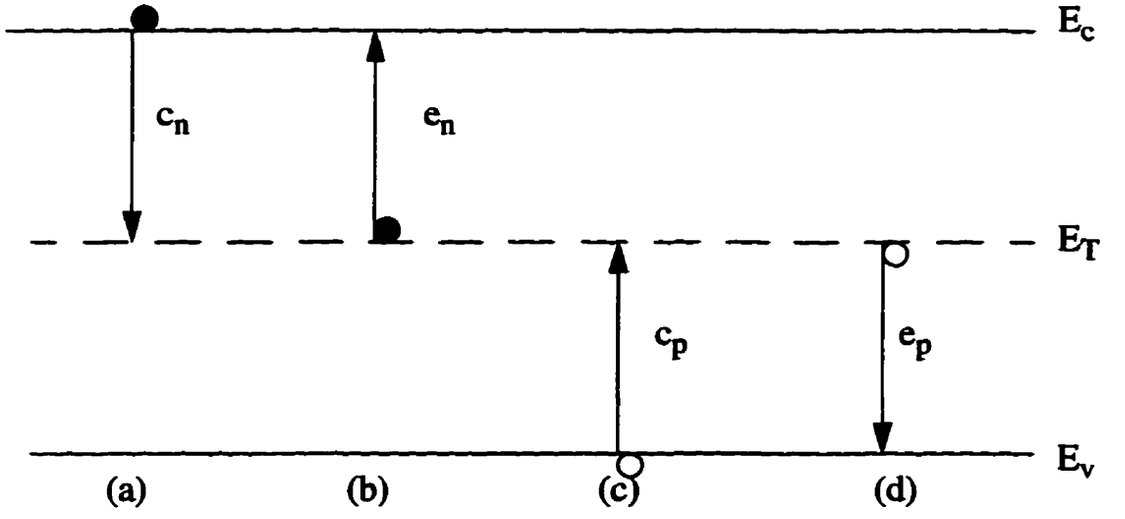


Fig. 2.1 Electron energy band diagram for a semiconductor with deep-level traps.

Figure 2.1 shows that a trap can capture an electron(a) and emit the trapped electron(b), this trap is generally referred to as an acceptor-like trap; and when a trap can trap a hole(c) and emit the trapped hole(d), this trap is generally referred to as a donor-like trap. A trap can assume only one of the two charge states, either a filled state which is occupied by an electron, or an empty

state which is unoccupied.

Supposing that the capture and emission of electrons are dominating, then the total electron trap concentration can be expressed as

$$N_T = n_t + N_0 \tag{2.1}$$

where n_t is the concentration of the trapped electrons (occupied states), N_0 is the concentration of unoccupied states. Similarly, if the capture and emission of holes are dominant, then the total hole trap concentration is:

$$P_T = p_t + P_0 \tag{2.2}$$

where p_t and P_0, are respectively the concentrations of trapped holes (unoccupied states) and neutral traps (occupied traps).

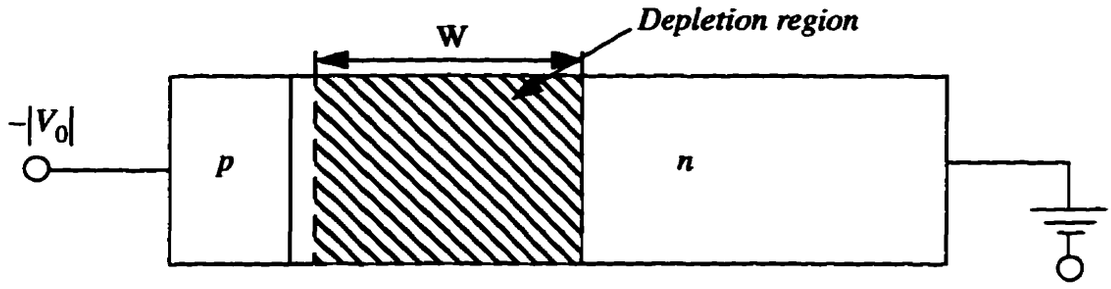


Fig. 2.2 The p^+n junction and the depletion layer.

In the following, we consider an n-type semiconductor containing only electron traps. For a p^+n abrupt junction, when a bias voltage V is applied across the junction, a depletion layer of width W will be formed as shown in Fig. 2.2. The depletion layer capacitance per unit cross-section area without trapped charge is given by[10]:

$$C \equiv \frac{dQ}{dV} = \frac{d(q(N_d)W)}{d\left(\frac{q(N_d)}{2\varepsilon_s}W^2\right)} = \frac{\varepsilon_s}{W} = \sqrt{\frac{q\varepsilon_s(N_d)}{2(V_{bi}+V)}} \tag{2.3}$$

where V_{bi} is the built-in potential; V is the bias voltage, positive for forward bias and negative for reverse bias.

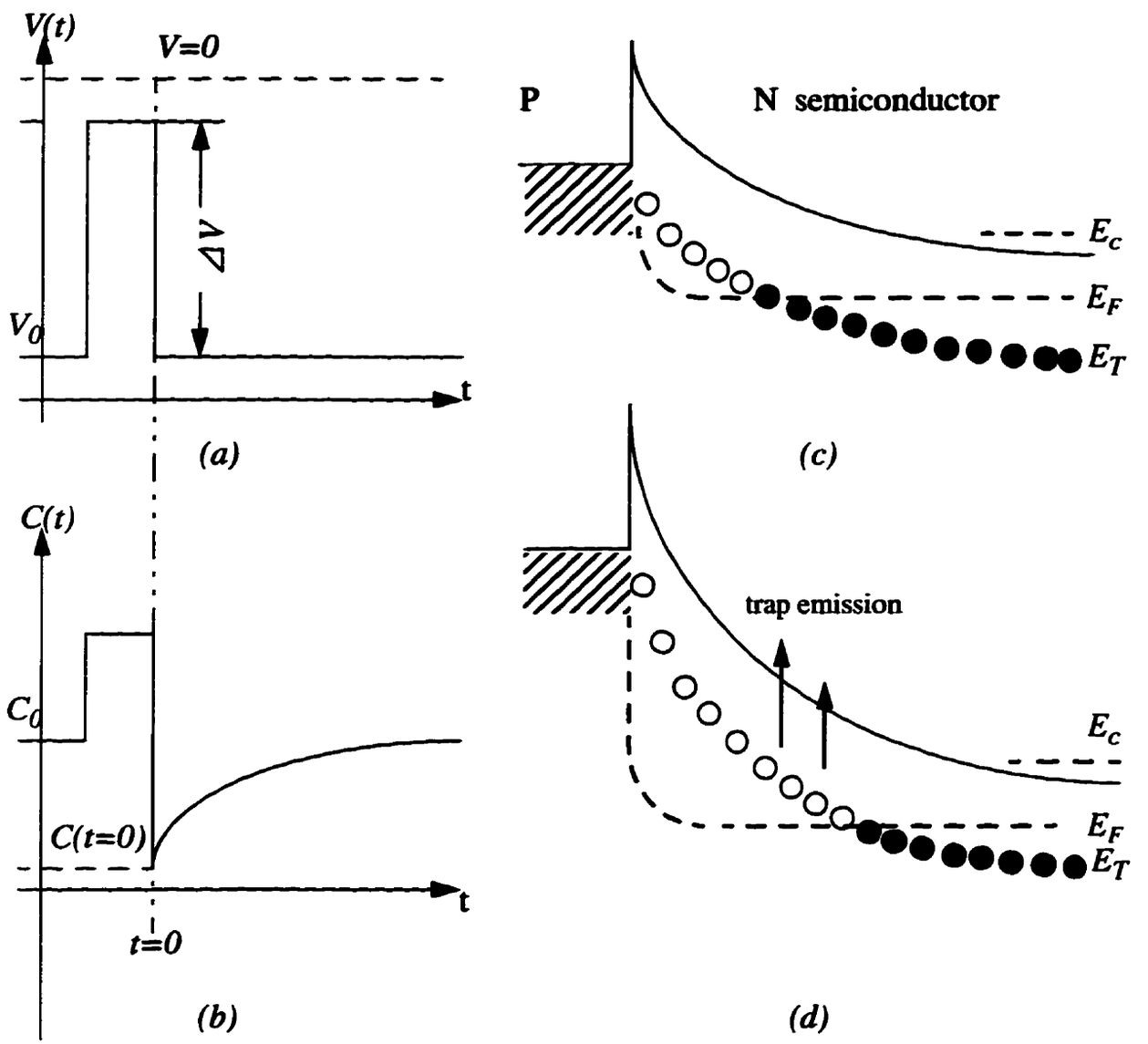


Fig. 2.3. The schematic illustration of a majority injection pulse sequence and energy band bending . (a) bias-time; (b) Capacitance-time; (c) and (d) the energy band bending during the pulse and after pulse.

Supposing that a forward bias pulse ΔV is imposed across the junction which is already in steady quiescent condition with a reverse dc bias $-V_0$ as shown in Fig. 2.3(a), then the capacitance prior to the application of the forward bias pulse is:

$$C_0 = \sqrt{\frac{q\varepsilon_s N_d}{2\left(V_{bi} - V_0\right)}} \tag{2.4}$$

When a pulse $|\Delta V| < |V_0|$ is applied, electrons will be injected into the n-side and they will gradually fill the traps. After a certain period of time, the capacitance will decrease due to the filling of traps.

$$C = \sqrt{\frac{q\varepsilon_s (N_d - n_t)}{2 (V_{bi} - V_0 + \Delta V)}} \tag{2.5}$$

When all traps are filled with electrons, $n_t \approx N_T$.

At the moment when $\Delta V = 0$ at $t = 0$ as shown in Fig. 2.3(b), the capacitance C drops to:

$$C(t = 0) = \sqrt{\frac{q\varepsilon_s (N_d - N_T)}{2 (V_{bi} - V_0)}} \tag{2.6}$$

After $\Delta V = 0$, the trapped electrons are gradually re-emitted to the conduction band as shown in Fig. 2.3(d). This implies that n_t gradually decreases with time and finally $n_t = 0$, then Eq. (2.6) returns to Eq. (2.4) and C becomes C_0. The change of the capacitance C with time after $t = 0$ is referred to as the capacitance transient, which can be written as:

$$C(t) = \left\{\frac{q\varepsilon_s [N_d - n_t(t)]}{2 (V_{bi} - V_0)}\right\}^{1/2} \tag{2.7}$$

or expressed as:

$$\frac{1}{[C(t)]^2} = \frac{V_{bi}-V_0}{q\varepsilon_s[N_d-n(t)]} = \frac{V_{bi}-V_0}{K^2[N_d-n(t)]} \tag{2.8}$$

where $K^2 = q\varepsilon_s$, is a constant.

By defining $S(t) = -dV/d\left(1/C^2\right)$, we obtain:

$$S(\infty) - S(0) = K^2\left[n_t(0) - n_t(\infty)\right] \tag{2.9}$$

Assuming $n_t(0) \approx N_T$ and $n_t(\infty) \approx 0$, then from Eq. (2.9), we have

$$N_T = \frac{S(t)|_{t=\infty} - S(t)|_{t=0}}{K^2} \tag{2.10}$$

Thus, from Eq. (2.10), the deep-level impurity concentration can be determined by the measurement of the C-V characteristics.

Since the change of capacitance with time is due to the emission of the trapped electrons from traps, the capacitance transient reflects the emission process of trapped electrons, and thus the emission rate depends upon the trap activation energy E_T, the trap capture cross section σ_n, the temperature T and the degeneration factor g_n (for simplicity, we assume $g_n = 1$). Therefore, the capacitance transient spectroscopy can be used for the determination of these trap parameters.

For impurities with a single level of activation energy, the capacitance of a p^+n junction after the removal of the forward bias pulse varies with time, and it can be expressed as:

$$C(t) = C_0\left[1 - \frac{n_t(0)}{2N_d}\exp\left(-\frac{t}{\tau_e}\right)\right] \tag{2.11}$$

where $n_t(0)$ the concentration of trapped electrons at $t = 0$, N_d is the doping concentration which can be considered as the free electron concentration, τ_e is the trapped electron emission time con-

stant, which is given by:

$$\tau_e = \frac{\exp\left[\frac{(E_C - E_T)}{kT}\right]}{\gamma_n \sigma_n T^2} \tag{2.12}$$

where $\gamma_n = \left(\upsilon / T^{1/2}\right)\left(N_c / T^{3/2}\right)$, is the body factor, υ is the electron thermal velocity and N_c is the election effective density of states in the conduction band. For a given semiconductor, the body factor is a constant. If the trap concentration is uniformly distributed in the depletion region and $n_t(t = 0) = N_T$, then N_T can be expressed as:

$$N_T = 2N_d \frac{[C_0 - C(0)]}{C_0} \tag{2.13}$$

From Eq. (2.11), Eq. (2.12) and (2.13), we can determine the trap energy level E_T, the trapped electron emission time constant τ_e and trap concentration N_T through a series of proper C-t measurements at various temperatures.

The capacitance transient spectroscopy is a powerful method for the determination of deep level trap parameters. Recently, the automated data acquisition techniques have been widely used to replace the very time-consuming and tedious single-shot measurements by using a dual-gated integrator or a double boxcar. All those techniques provide detailed information about capacitance as a function of time as a spectrum. This is why it is generally referred to as deep level transient spectroscopy(DLTS)[14-17].

2.2 Various Techniques for DLTS

I. Boxcar DLTS

Boxcar DLTS is an automated data acquisition method for the capacitance transient measurements. The basic concept of this method is the rate window. To a capacitance decay curve, a rate window is set at time $t = t_1$ and $t = t_2$. The capacitance at the two points $C(t_1)$ and $C(t_2)$ are taken by a boxcar which outputs a differential signal. Thus

$$\delta C = C(t_1) - C(t_2) \tag{2.14}$$

Figure 2.4 illustrates schematically the process of this technique. With a rate window set at $\Delta t = t_2 - t_1$, δC varies with temperature and reaches a peak δC_{max} at a certain temperature when the emission time constant τ_e is in the same order of Δt as shown in Fig. 2.4(a). This indicates that τ_e changes with the temperature according to Eq. (2.12). The δC_{max} peak shifts along with the temperature as the rate window Δt changes as shown in Fig. 2.4(b)

Figure 2.5 is an Arrhenius Plot which is drawn based on the relation between rate window and temperature at which the peak occurs with this rate window.

Experimentally, the capacitance decay waveform is corrupted with noise, and DLTS is to extract signal from the noise in an automated manner. The boxcar DLTS technique is one of the correlation techniques. It is a signal-processing method in which the input signal is multiplied by a reference signal, a weighting function $w(t)$ and the product is averaged by a linear filter. The output is

$$\delta C = \frac{1}{T}\int_0^T f(t)\, w(t)\, dt \tag{2.15}$$

The input signal $f(t)$ is in fact $C(t)$ given by Eq. (2.11). Equation (2.15) can be rewritten as

$$\delta C = \frac{C_0}{T}\int_0^T \left[1 - \frac{n_t(0)}{2N_d}\exp\left(-\frac{t}{\tau_e}\right)\right] w(t)\,dt \qquad (2.16)$$

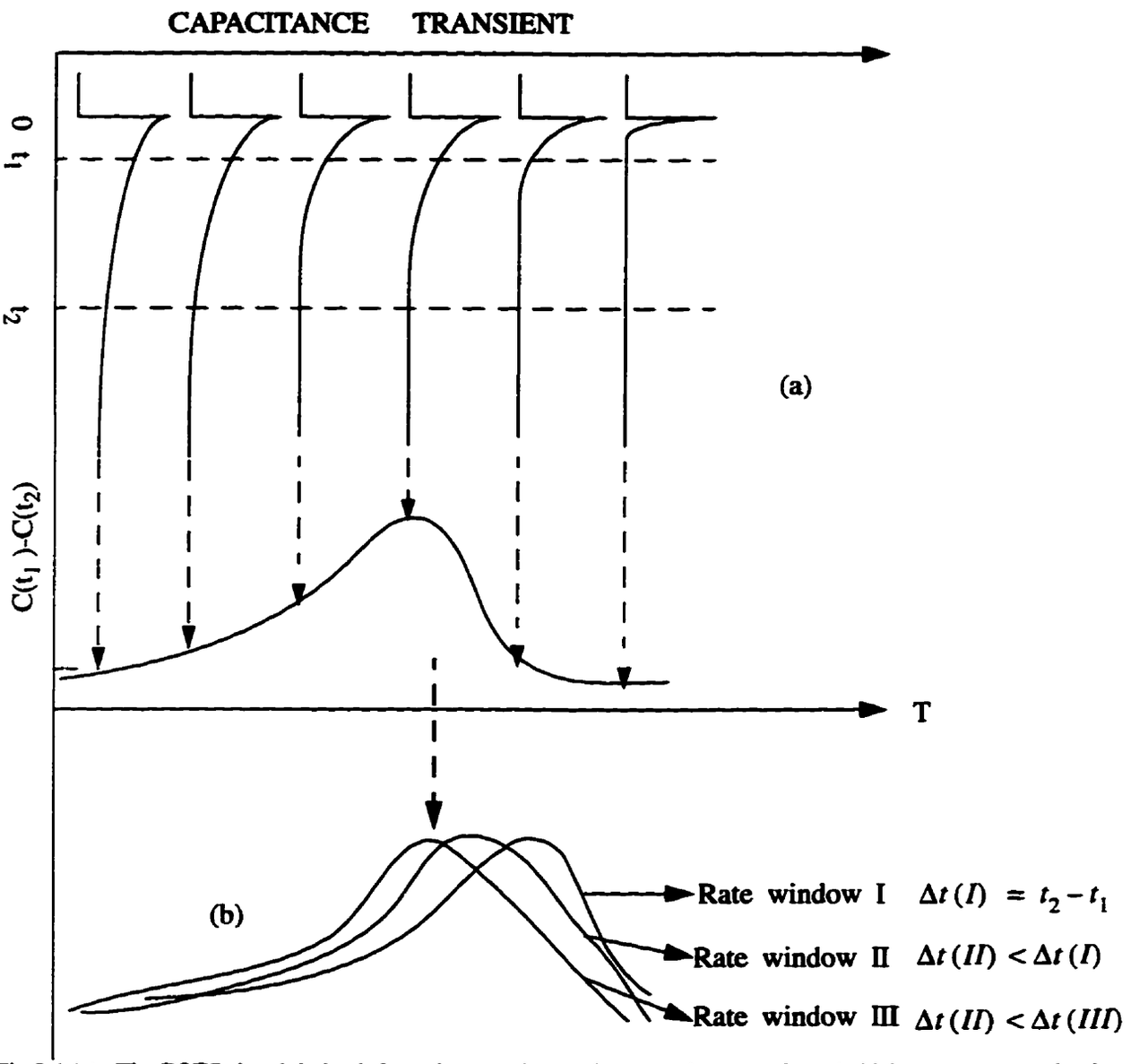


Fig.2.4 (a). The DLTS signal derived from the capacitance change at time t_1 and t_2. At high temperatures, the time constant is much smaller than the window, and at low temperatures the time constant is much larger than the window, while a peak is seen when the emission rate falls within the window; (b). Shift of the peak of DLTS signal as the rate window is varied[16],[18].

For boxcar DLTS, the weighting function is defined as:

$$w(t) = \delta(t-t_1) - \delta(t-t_2) \tag{2.17}$$

and Δt is the rate window width which equals $(t_1 - t_2)$. The DLTS signal then is obtained from Eq. (2.16) and Eq. (2.17) as

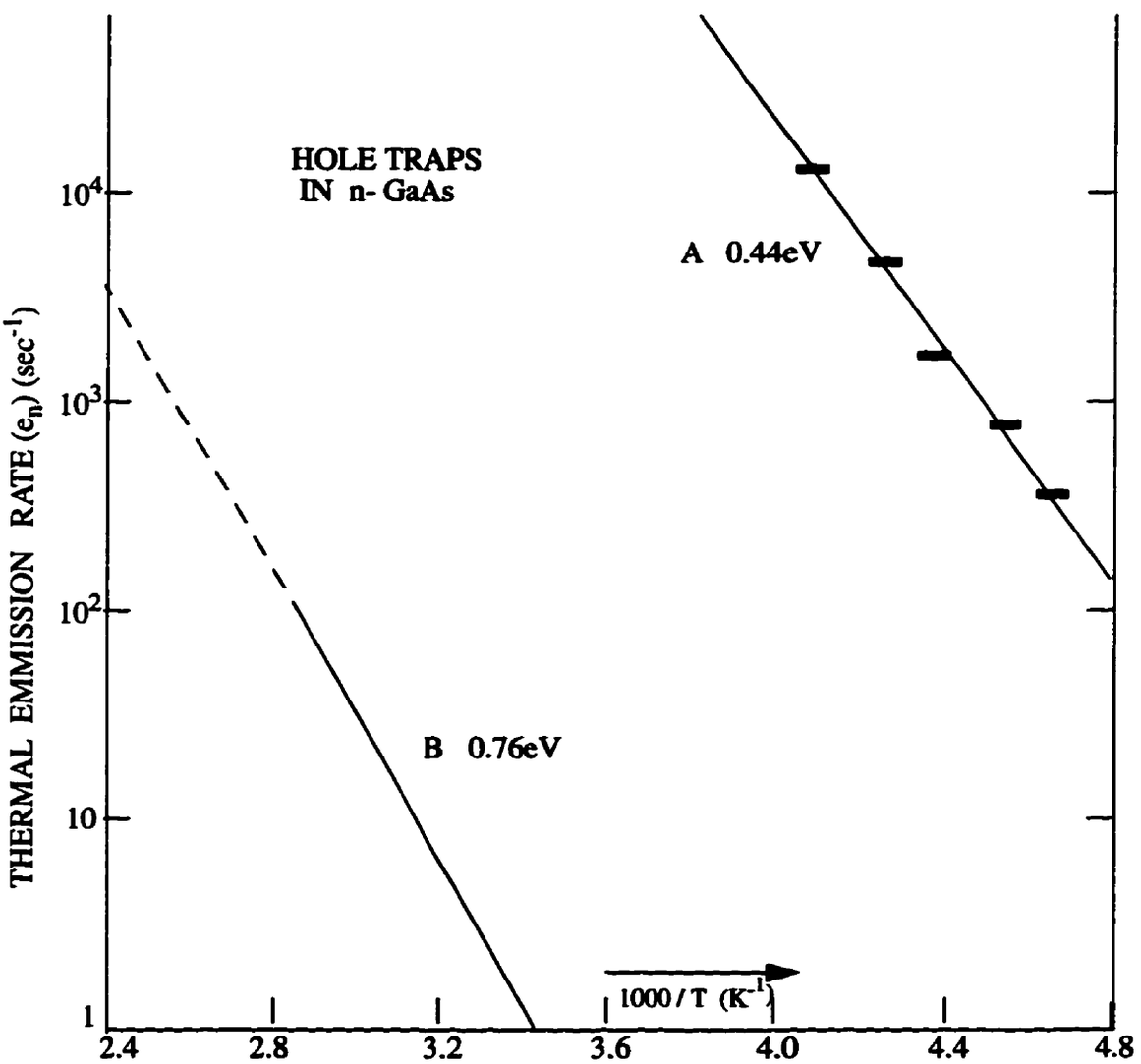


Fig. 2.5 Thermal emission rates vs. 1000 / T determined from the DLTS spectra. The solid lines are determined from careful fixed temperature measurements of the capacitance transients; The dash line are extrapolations of this data. The error bars on the DLTS data represent the uncertainty in locating the peaks in the spectra . The experiments were carried out on an n-GaAs junction [after Miller, et al.[16]].

$$\delta C = C(t_1) - C(t_2) = \frac{C_0 n_i(0)}{2N_d}\left[\exp\left(-\frac{t_2}{\tau_e}\right) - \exp\left(-\frac{t_1}{\tau_e}\right)\right] \tag{2.18}$$

Differentiating Eq. (2.17) with respect to τ_e and setting it to zero, we obtain

$$\tau_{e,\,max} = \frac{t_2 - t_1}{\log\left(\frac{t_2}{t_1}\right)} \tag{2.19}$$

which is the τ_e for the maximum output signal δC_{max} at a certain temperature. From Eq. (2.12), we obtain

$$\Delta E_T = E_C - E_T = kT\left[\log\tau_e + \log\left((\gamma_n\sigma_n) + 2\log T\right)\right] \tag{2.20}$$

The emission rate is $e_n = \frac{1}{\tau_e}$, hence

$$e_{n,\,max} = \frac{\log(t_2/t_1)}{t_2 - t_1} \tag{2.21}$$

It is also known that

$$e_n = \left(\sigma_n \upsilon N_c\right)\exp\left[(E_T - E_c)/kT\right]$$

or
$$e_n = AT^2\exp\left[(\Delta E_T)/kT\right] \tag{2.22}$$

where $A = \gamma_n\sigma_n$, is considered as constant. Thus, from Eq. (2.22), we can also obtain

$$\Delta E_T = 1000k\left\{\frac{\Delta\left[\log\left(\tau_e T^2\right)\right]}{\Delta\left(\frac{1000}{T}\right)}\right\} \tag{2.23}$$

or in the form

$$\Delta E_T = 1000k\left[\frac{\Delta\left(\log\frac{e_n}{T^2}\right)}{\Delta\left(\frac{1000}{T}\right)}\right] \tag{2.24}$$

Thus, from Eq. (2.23) or Eq. (2.24) and Arrhenius Plot, we can obtain ΔE_T.

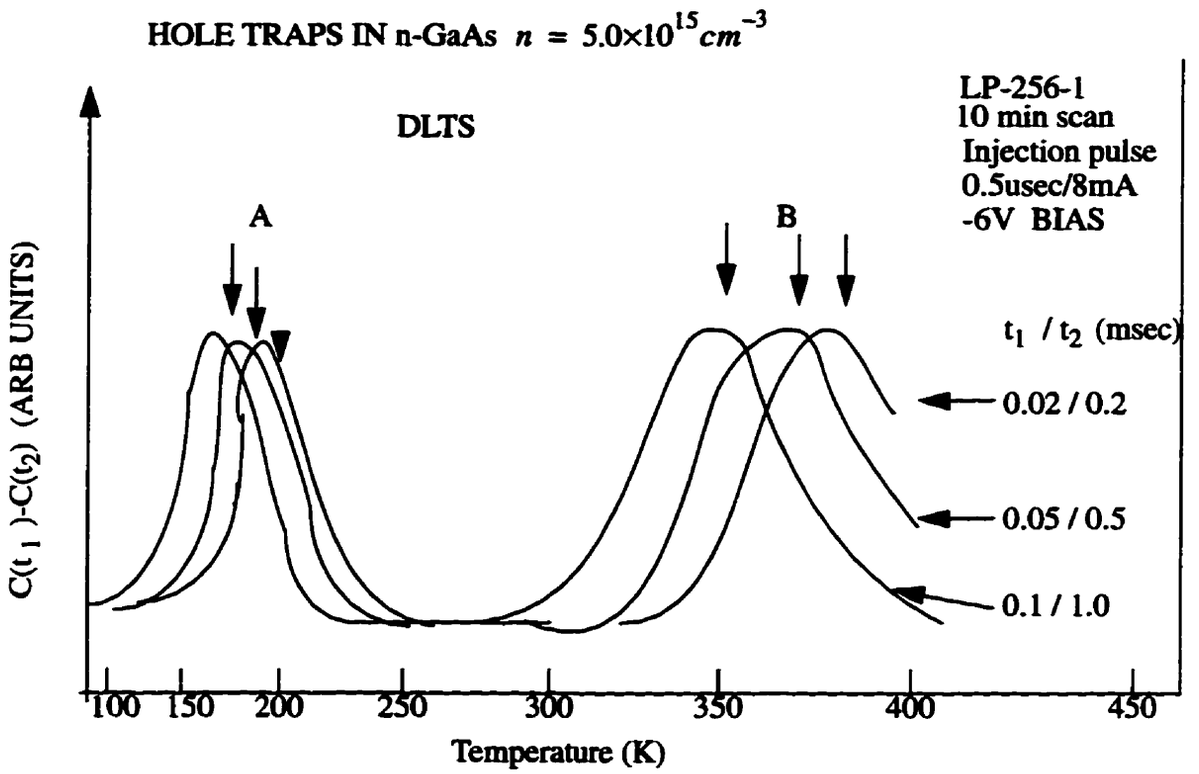


Fig. 2.6. Typical experimental DLTS spectra for hole traps in n-GaAs. The two traps are labeled A and B and have energies measured from the valence band of 0.44eV and 0.76eV, respectively [after Miller, et al.[16]].

Assuming $n_t(0) = N_T$, substituting τ_e from Eq. (2.19) and letting t_1/t_2 to be γ, then putting all together into Eq. (2.18), we obtain

$$N_T = \frac{2N_d \delta C_{max} \cdot \gamma^{(\gamma-1)}}{C_0(1-\gamma)} \qquad (2.25)$$

The boxcar technique usually needs 5 to 10 Arrhenius Plot points, each of which requires 5 to 10 temperature sweeps (from 5-10 $\Delta C \sim t$ plots with different rate windows by changing t_1, t_2). The sampling time can be varied in three ways: (1) vary t_2 with t_1 fixed, ; (2) vary t_1 with t_2 fixed, and (3) vary t_1 and t_2 with t_2 / t_1 fixed. Way (3) is preferred because the peaks shift with temperature without much change in curve shape shown in Fig. 2.6 .

For a typical $\gamma = 2$ in Eq. (2.25) ,

$$N_T = \frac{-8N_d \delta C_{max}}{C_0} \qquad (2.26)$$

The minus sign represents the fact that $\delta C < 0$ for majority-carrier traps.

II. Double-Correlation DLTS

One of the main refinements of the boxcar DLTS technique is Double-Correlation DLTS (DDLTS or D-DLTS) method[19], in which a double-pulse capacitance transient and a double-correlation are used to obtain a higher sensitivity for the detection and analysis of deep level traps. Figure 2.7 shows that in D-DLTS, two pulses of different heights are used to charge the space charge region (SCR). The weighting function gives the output signal

$$\begin{aligned} \Delta C &= [C(t_1) - C(t_2)] - [C'(t_1) - C'(t_2)] \\ &= [C'(t_1) - C(t_1)] - [C'(t_2) - C(t_2)] \\ &= (\Delta C(t_1) - \Delta C(t_2)) \end{aligned} \qquad (2.27)$$

In the first correlation, the capacitance transients after the two pulses are related to form $\Delta C(t_1)$ and $\Delta C(t_2)$ at corresponding delay times after each pulse. In the second step,

$[\Delta C(t_1) - \Delta C(t_2)]$ is used in the same way as ΔC for boxcar DLTS to resolve the emission rate through a temperature scan.

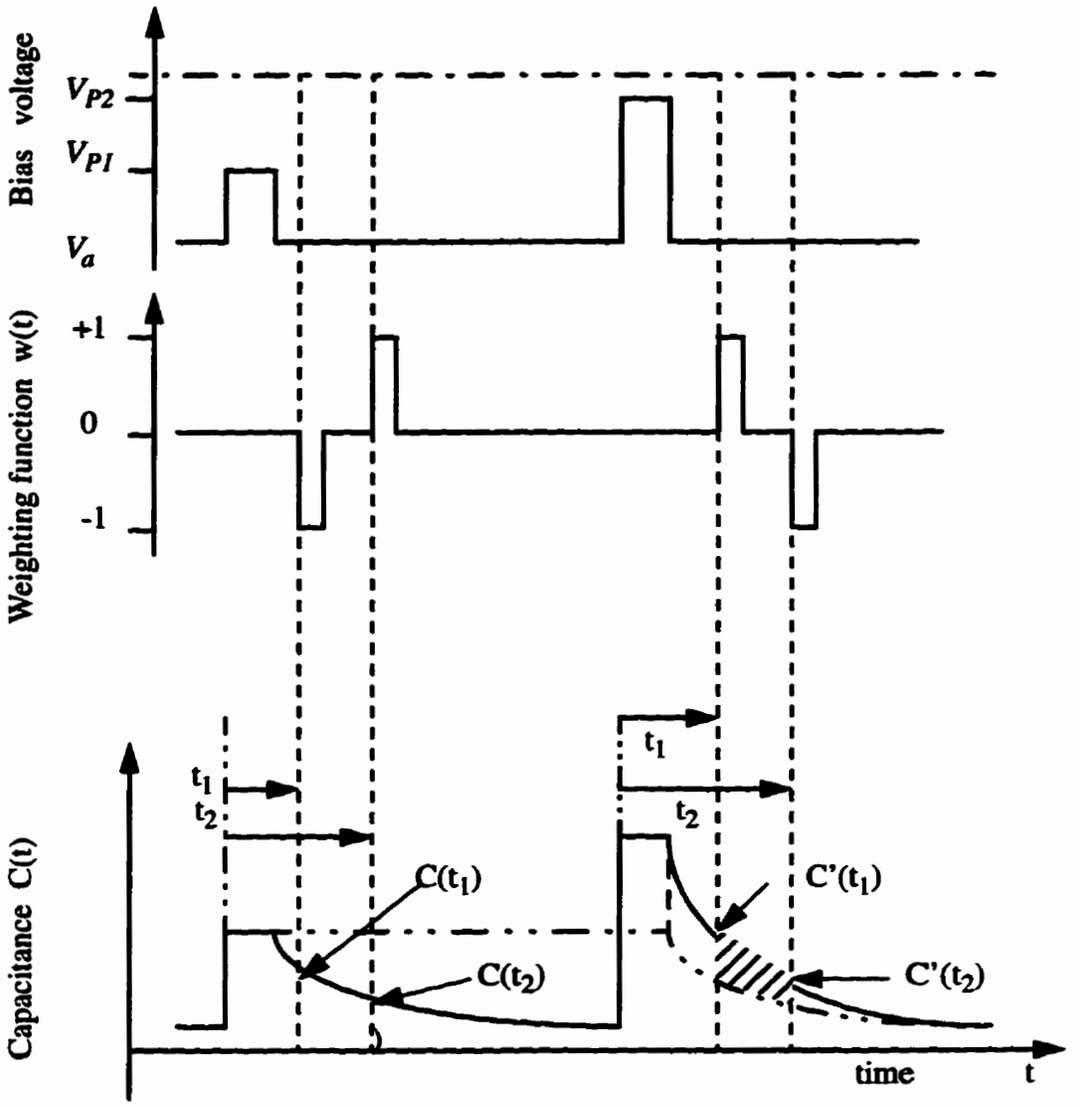


Fig. 2.7. Schematic illustration of the pulse shape, capacitance signal and correlation weighting function as used in DDLTS [after Lefevre et al.[19]].

The D-DLTS has the following advantages over the boxcar DLTS:

(1). All the traps in the rate-window are exposed to approximately the same electric field and thus

a smear-out of the time constant due the field dependence is avoided;
(2). The D-DLTS leads to the subtraction of studious signals and drift to reduce the measurement noise.

The D-DLTS measurement though requires either a four-channel boxcar integrator or an external modification to a two-channel boxcar integrator[20].

III. Lock-in Amplifier DLTS

Better signal / noise ratio can be achieved by using a standard lab instrument -- lock-in amplifier[21-22]. The lock-in amplifier uses a square-wave weighting function shown in Fig. 2.8 with periods set by the frequency of the lock-in amplifier. The DLTS output peak is observed when this frequency bears the proper relationship to the emission time constant at the temperature. Figure 2.8 also shows the signals in both directions, which can be expanded by adjusting the time base generator. The T is the pulse period. A minimum delay time $T_d = 0.1T$, is normally sufficient to eliminate the overload problems[23-26].

For the weighting function

$$w(t) = \begin{cases} 0 & 0 \le t \le T_d \\ 1 & T_d \le t \le T/2 \\ -1 & T/2 \le t \le T - T_d \\ 0 & T - T_d \le t \le T \end{cases} \tag{2.28}$$

The output is given by[20],[21]

$$\delta C = -GC0\frac{n_t(0)\,\tau_e}{N_d T}\exp\left(-\frac{T_d}{\tau_e}\right)\left[1-\exp\left(\frac{-T-2T_d}{2\tau_e}\right)\right]^2 \tag{2.29}$$

where G is the lock-in amplifier and capacitance meter gain.

Differentiating Eq. (2.29) with respect to τ_e and setting it to zero, $\tau_{e,max}$ can be determined from the transcendental equation:

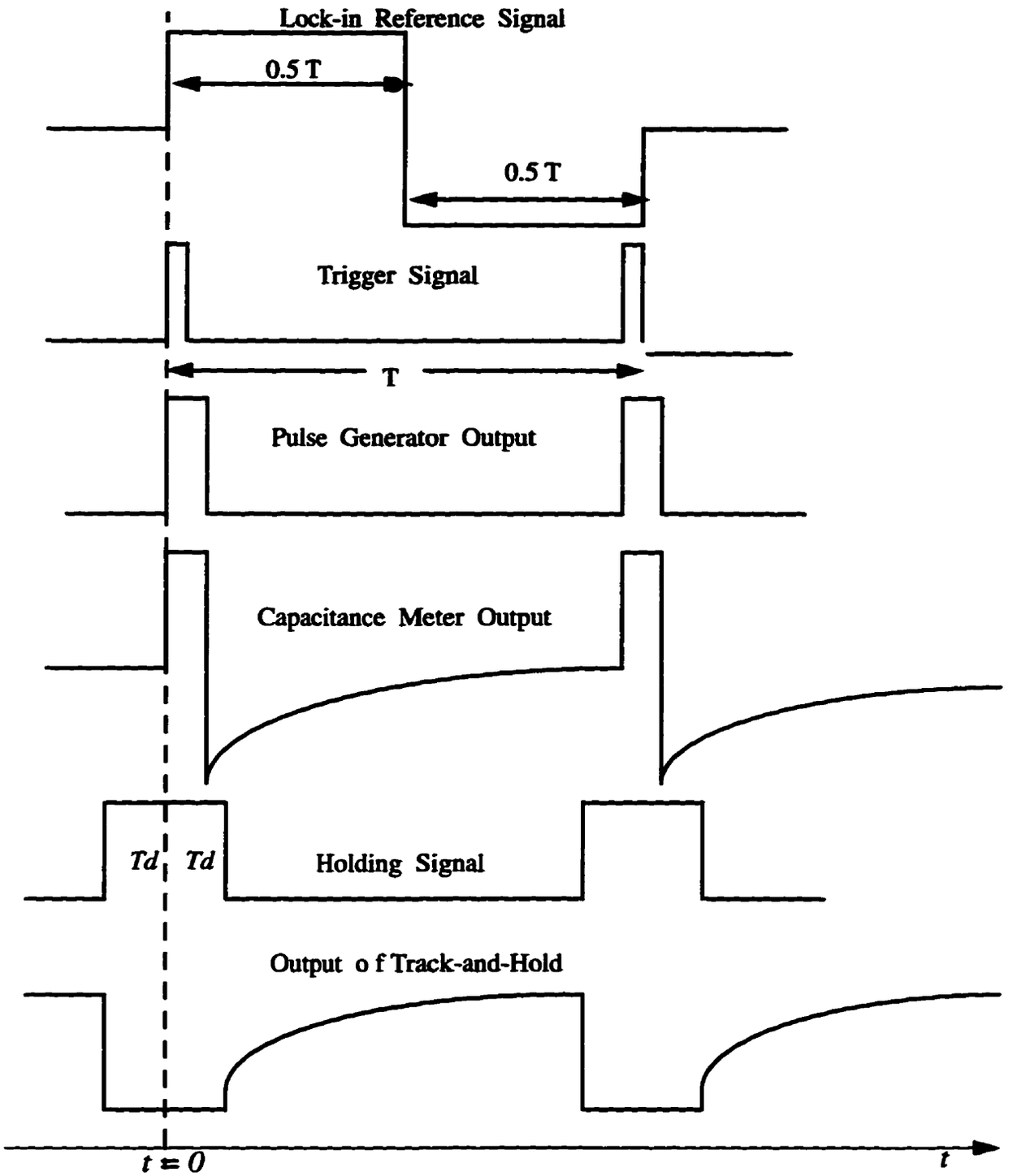


Fig. 2.8. The waveform of weighting function for the lock-in amplifier and the output signals from the pulse generator, capacitance meter, time-base hold generator and track and hold [after Kimerling[21]].

$$\left(1+\frac{T_d}{\tau_{e,max}}\right) = 1+\frac{T-T_d}{\tau_{e,max}}\exp\left(-\frac{T-2T_d}{2\tau_{e,max}}\right) \tag{2.30}$$

For a typical delay time $T_d = 0.1T$, the trap concentration is given by

$$N_T = -8\frac{\delta C_{max}}{C_0}\frac{N_d}{G} \tag{2.31}$$

The active energy level ΔE_T can be obtained from the Arrhenius Plot.

IV. Correlation DLTS

Although the DLTS described before are of correlation techniques, Miller et el.[22] established a lower noise/signal system based on correlation and optimum filter theory. The block diagram of the system is shown in Fig. 2.9.

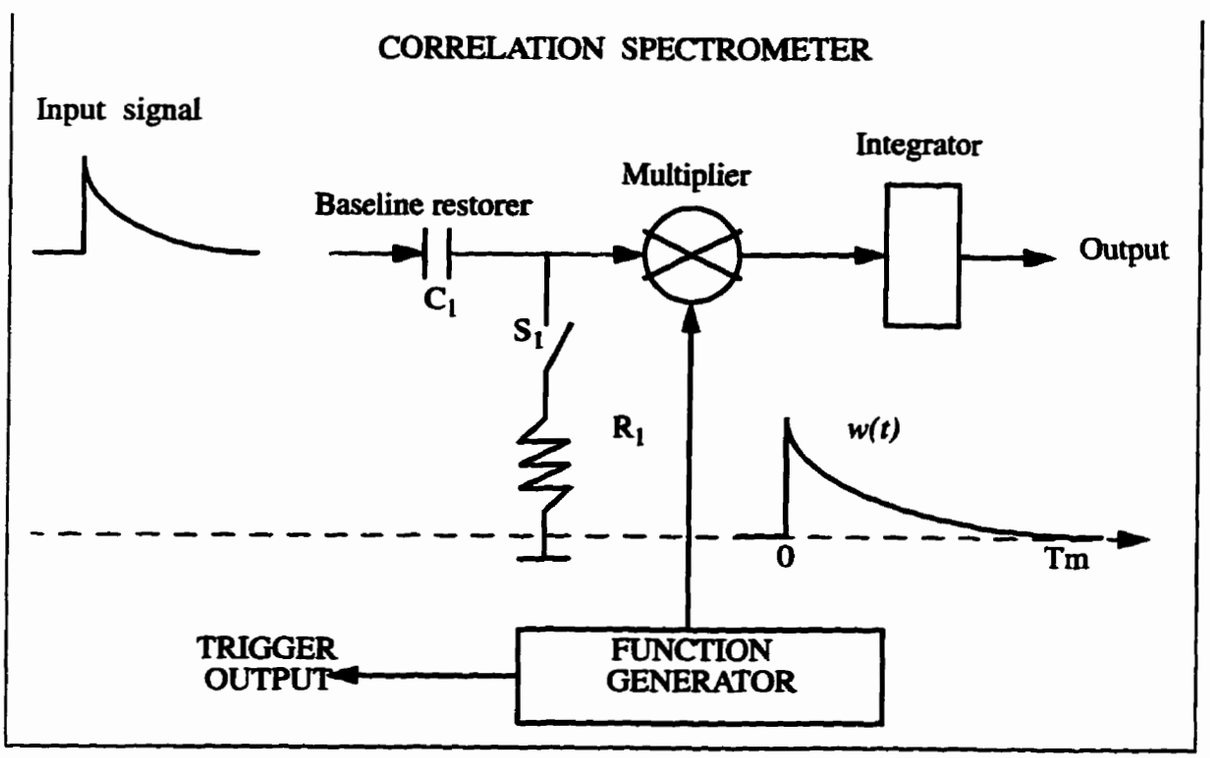


Fig. 2.9 The block diagram of a correlation spectrometer [after. Miller et al.[22]].

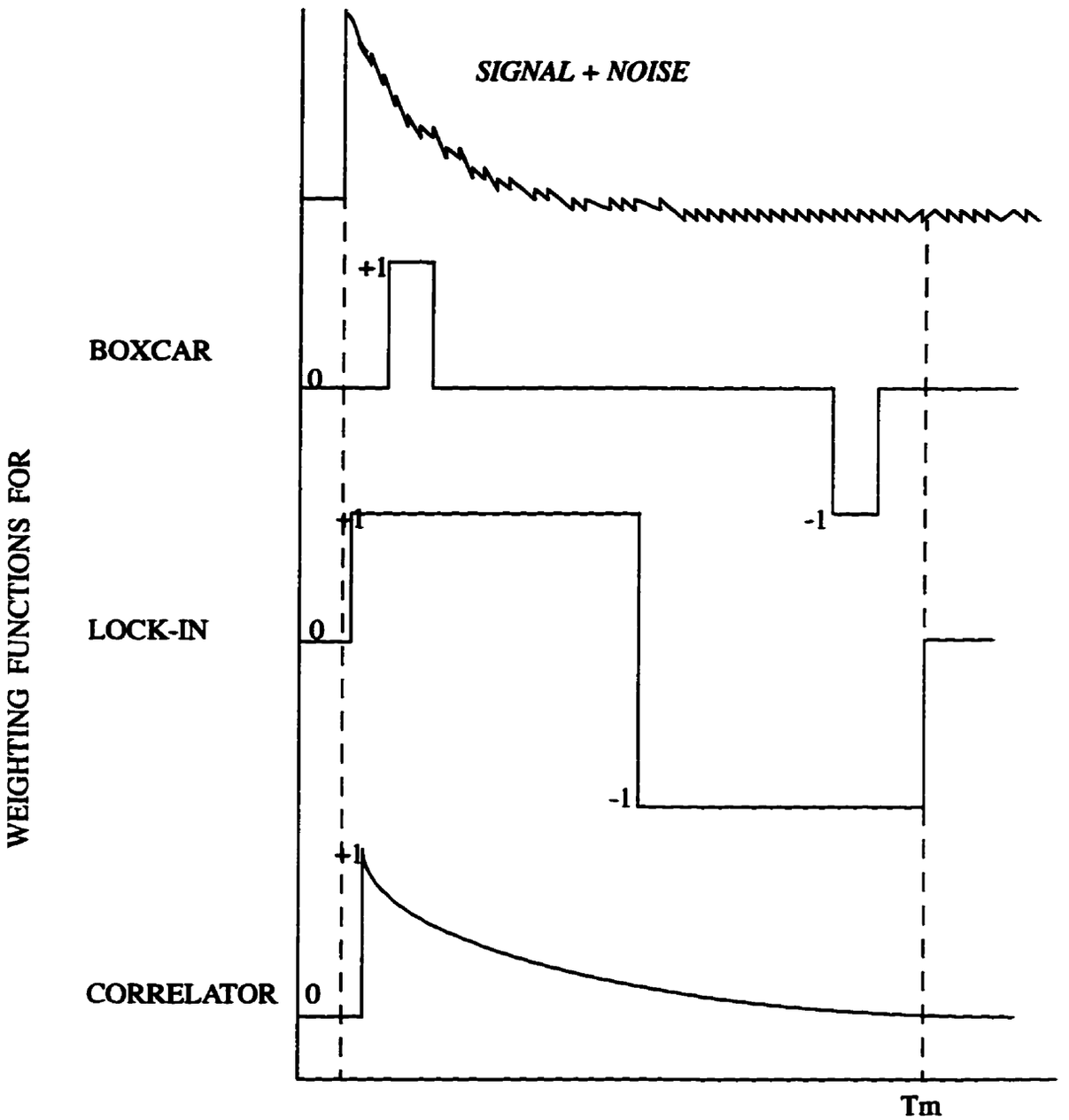


Fig. 2.10 A representative decaying exponential signal (upper waveform) together with three weighting functions $w(t)$ [after Miller etc.[22]].

Suppose that a given signal, of unknown amplitude A, but of known shape $s(t)$, in the presence of noise $n(t)$, is processed through a linear filter with a weighting function $w(t)$. The best estimate E of the signal amplitude

$$E = \int_0^T [As(t) + n(t)w(t)]\,dt \tag{2.32}$$

can be matched only when

$$w(t) = s(t) \tag{2.33}$$

This means that the optimum weighting function has the same shape of the noise-free signal itself, and therefore, for the DLTS system, $w(t)$ should be a decaying exponential function.

Figure 2.10 presents a comparison of weighting functions for boxcar, lock-in amplifier and correlation DLTS. It is obvious that the weighting function largely affects the information collection and hence the resulting noise/signal ratio.

The optimum weighting function for correlation DLTS makes the best signal/noise ratio among the three techniques. Later, some researchers[27-29],[31] have analyzed the correlation method and confirmed that correlation DLTS has a higher signal / noise ratio than either boxcar or lock-in DLTS[30]. In other hand, they also found that since the small capacitance transient rides on a dc background, it is not sufficient to use a simple exponential because the weighting function[27] and the base line restoration[28] are required.

V. CC-DLTS

The basic difference between the Constant Capacitance DLTS (CC-DLTS) and the others is that the capacitance is held constant during the carrier emission measurements. In the meantime the applied voltage is the transient response through a feedback circuit[32-34]. A block diagram of an improved CC-DLTS system is shown in Fig. 2.11.

Just as the capacitance decay curve contains the trap information in the constant voltage method, so does the time-varying voltage in the constant capacitance method. Because the SCR width is held constant and the resulting voltage change is directly related to the change in the SCR charge in CC-DLTS, an equation valid for arbitrary N_T is given

$$V = -\frac{qK_s\varepsilon_0 A}{2C^2}[N_d - n_t(0)\exp(-t/\tau_e)] + V_{bi} \qquad (2.34)$$

Equation (2.34) shows that the *V-t* relationship is exponential in time, the principle of DLTS can then be used in CC-DLTS to get a $\Delta V \sim 1/T$ plot in order to find out τ_e and ΔE_T, N_T. The CC-DLTS has advantages in *G-R* center depth profiling and interface charge measurements[33] due to its high energy resolution and its ability to solve spatial distributed charge densities. CC-DLTS can also be refined by combining with D-DLTS[37]. However, the most successful improvement of this technique is the new designed fast responding feedback circuit[35], which enables the CC-DLTS system to reach a stable value in *0.2ms* after a switching event so as to be practical in the deep-level measurements. For the DLTS analysis on MOS, the CC-DLTS even provides a slightly simpler formulation for the interface-state density calculations[37].

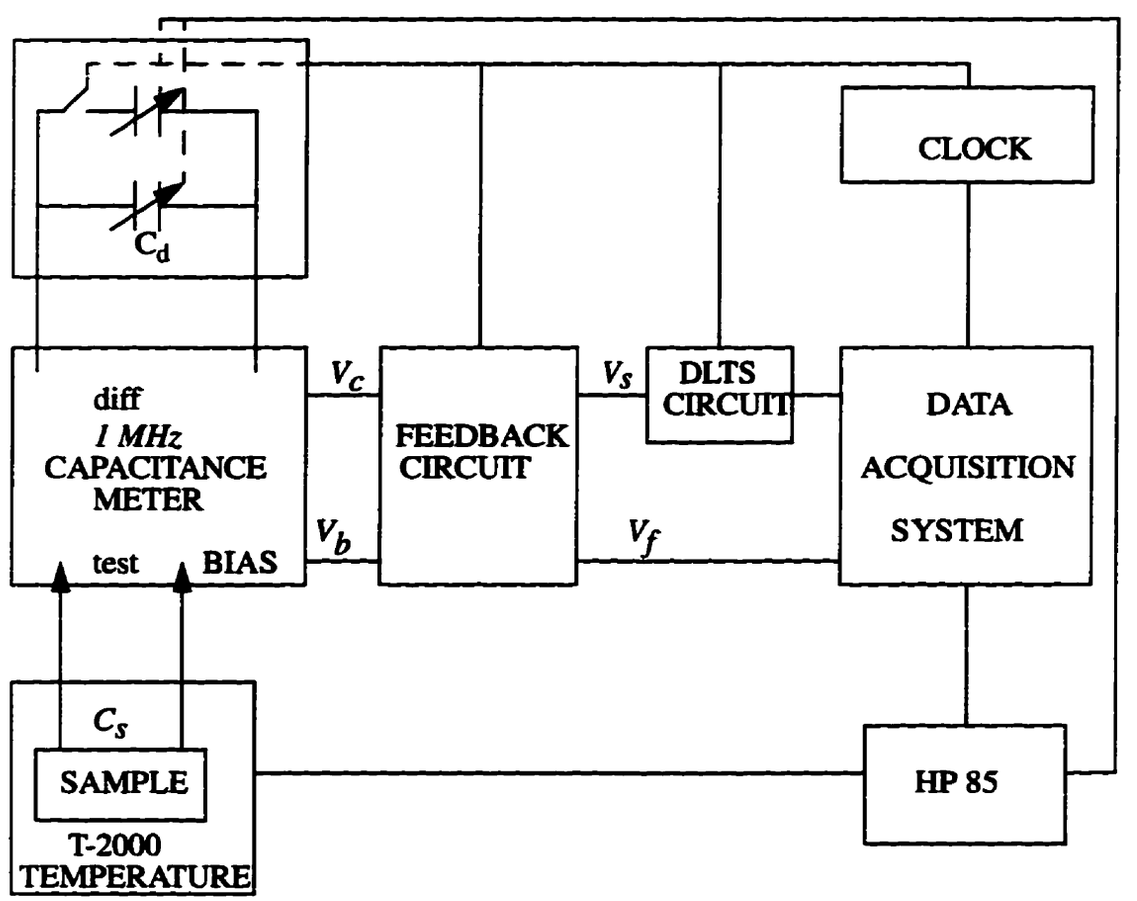


Fig. 2.11. The block diagram of an improved CC-DLTS system [after Shiau, et al.[35]].

2.3. Computerized DLTS

I. Full Curve Acquisition Computer System

As the fast and cheap digital apparatus and computer became available in the late 70's, Wagner et el.[38] initiated computer application to DLTS. Figure 2.12 shows a simple block diagram of a computer DLTS system.

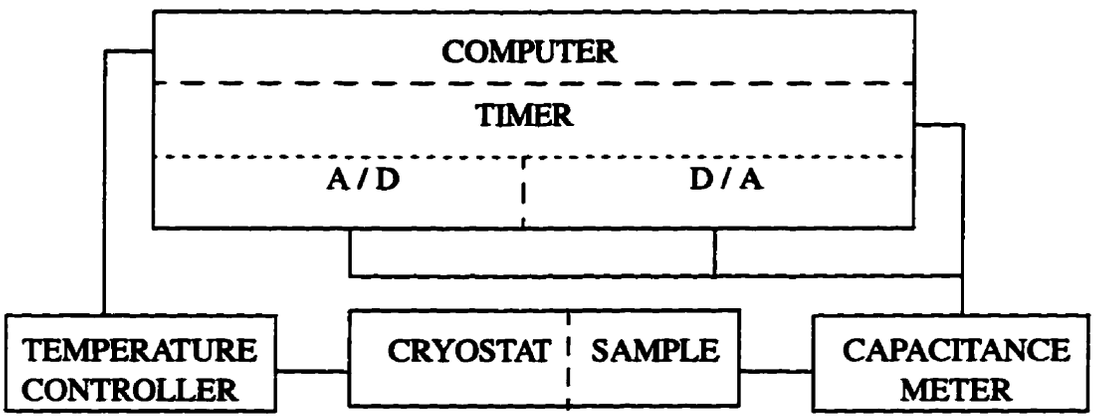


Fig. 2.12 The block diagram of a simple computer-controlled DLTS system [after Jack, etc.[39]]

The entire *C-t* curve is obtained at each of different temperatures by digitizing and storing the capacitance waveform (represented by a reasonably large number of digital data points), and only one scan of sampling temperatures are needed for DLTS measurements, which dramatically reduces the experiment time[19] (In conventional DLTS, such a scan of temperatures can just produce one of the 5-10 points in the Arrhenius Plot).

II. Full Curve Analysis Method

Standard equipment and computer software have simplified the experimental process[40]. A digital filter can be employed to smooth the data waveform stored in the disk so as to improve the signal/noise ratio[41]. Figure 2.13 indicates the function of the digital filter.

The computerized full-curve digital data acquisition technique has made various ways for full

curve analysis. The easy way to use the full-curve data which are collected at a certain temperature is to simply choose different data points as $C(t_1)$ and $C(t_2)$ to get ΔC. Repeating this process with varying the rate window a number of times without further experiments can lead to one point in the Arrhenius plot, the analysis procedure is the same as that in boxcar DLTS[38-39]. The method though needs a wide rate window, i.e. large $(t_1 - t_2)$ for accuracy, which limits the usage efficiency of data[33]. This method also needs improvement in the noise/signal ratio.

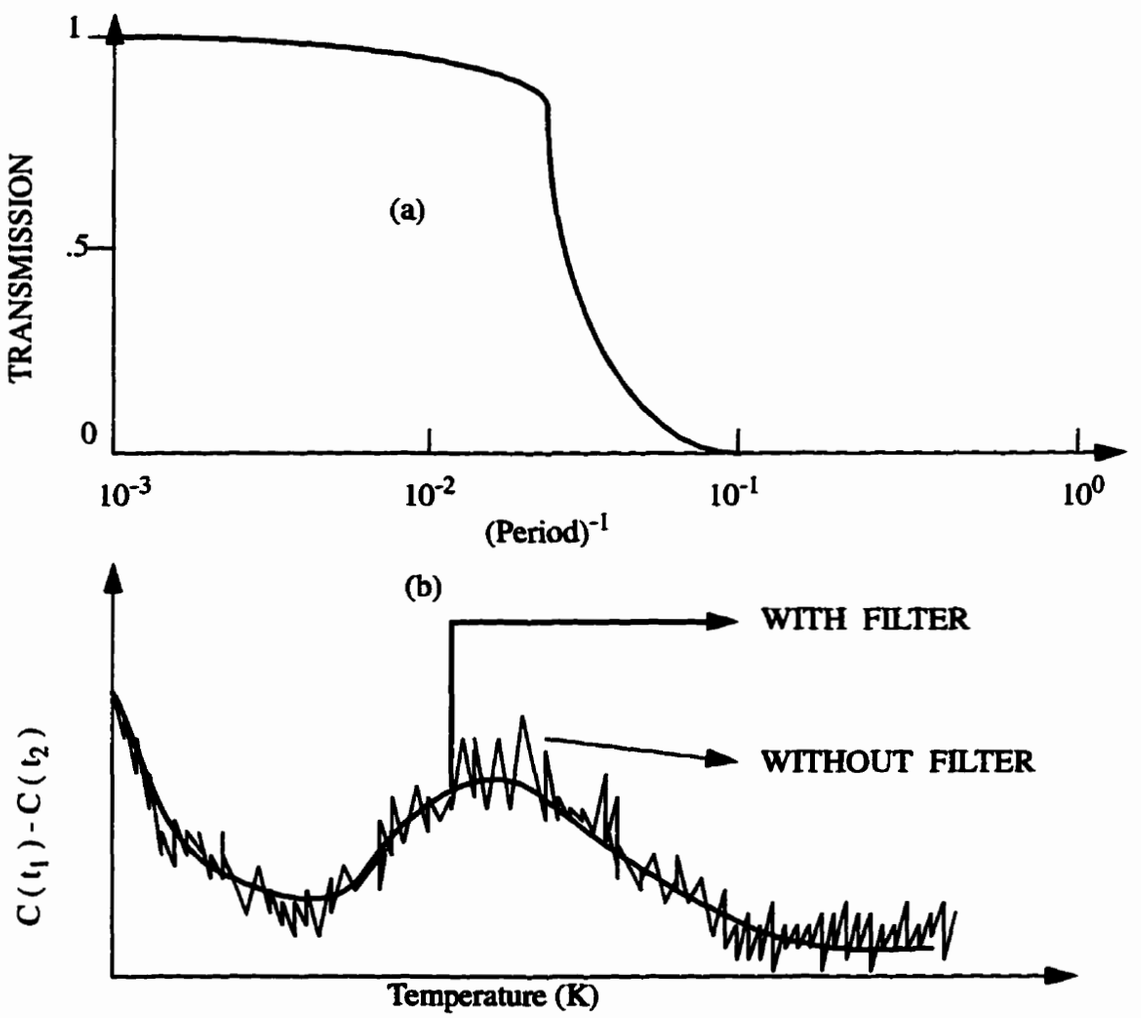


Fig. 2.13 (a). Filter characteristics used in the digital filter routine of the analysis program, the period is given in degree; (b) Illustration of the effect of the filter procedure applied on noisy DLTS spectra [after Holzlein, et al.[41]].

In order to deal with non-exponential or multi-exponential decays and improve the signal/noise ratio, a number of analysis methods have been developed.

1. Fast Fourier Transforms (FFT)

The Fourier transform has the properties that make it useful for the analysis of exponential transients. The basic principles of this method is discussed as following[42-43].

The FFT method proved to fit single exponential accurately through many fits for both synthesized and experimental data. One very important feature of this method is that it is very fast (A typical fit to a 256-point transient requires about 2.5 sec. of microcomputer time in the early 80's). However, FFT is not stable when applied to non-exponential or multi-exponential cases (see Table 2.1). Lately, this problem was somehow improved[44] by decomposing a capacitance transient of a two-exponential waveform with two Fourier transforms.

2. The Method of Moments

The method of moments was transplanted to the DLTS data analysis from biochemical studies[42] which had the similar problems in that they dealt with sums of exponential in levels of noise comparable to those common in DLTS. This method was further improved[45].

The Observed response function $F(t)$ is assumed to be the convolution of an idealized, delta-function response $f(t)$ and excitation function $H(t)$ as given by

$$F(t) = \int_0^t H(u) f(t-u)\, du \tag{2.35}$$

and the idealized response $f(t)$ is assumed to be the sum of the multi-exponential with the form:

$$f(t) = \sum_{i=1}^{N} A_i e^{-\alpha_i t} \tag{2.36}$$

where the amplitudes A_i and emission rate constants α_i are the parameters to be extracted by this method.

Define

$$u_k = \int_0^\infty t^k F(t)\,dt$$

$$\vartheta_k = \int_0^\infty t^k H(t)\,dt \qquad (2.37)$$

$$Gs = \sum_{i=1}^{N} A_i \tau_i^s$$

With Isenberg and Dyson's theory[46-47], the individual time constants can be determined from the set of G_s's, using

$$\begin{vmatrix} 1 & \tau & \tau^2 & \dots & \tau^N \\ G1 & G2 & G3 & \dots & GN \\ G2 & G3 & G4 & \dots & GN+1 \\ \dots & \dots & \dots & \dots & \dots \\ GN & GN+1 & GN+2 & \dots & G2N \end{vmatrix} = 0 \qquad (2.38)$$

A comparison of the boxcar, FFT and method of moments in Table 2.1 shows that the method of moments is superior for both simulated and experimental data. It was later enhanced by adding a fast Fourier transform to improve the base-line offset determination and to facilitate its removal from the data prior to application of the method while incorporating the mean displaced ratio algorithm for noise reduction.

Table 2.1 The activation energies in eV and cross sections in cm^2 for the discernible traps, as obtained by the three methods: boxcar, moment and FFT [after Kirchner, etc..[42]].

Trap energies and cross section for different methods					
METHOD	Trap I HB/HL1	Trap II EB2/EL2	Trap III HL10	Trap IV HL3	Trap V HB4/HL4
Refs.	0.78/0.94 $5\times10^{-16}/4\times10^{-14}$	0.83/0.825 $2\times10^{-13}/1\times10^{-13}$	0.83 2×10^{-13}	0.59 3×10^{-15}	0.44/0.42 $3\times10^{-14}/3\times10^{-15}$
Boxcar	0.55 1×10^{-18}	0.74 1×10^{-14}	0.71 6×10^{-15}	0.25 $4/10^{-21}$	0.39 1×10^{-16}
Moment	0.84 4×10^{-15}	0.82 2×10^{-13}	0.80 8×10^{-14}	0.53 5×10^{-16}	0.46 4×10^{-14}
FFT	0.87 5×10^{-15}	0.98 1×10^{-11}	*unstable*	0.13 8×10^{-23}	0.19 3×10^{-20}

3. Temperature Dependent Pulse-width DLTS

Supposing that a p-n junction has two deep levels with activation energies ΔE_{T1} and ΔE_{T2}. A saturation pulse will fill up traps in both levels, but a certain shorted pulse can leave the deeper level uncharged so that the DLTS signals on the latter case only contains the trap information of the one with less activation energy. Comparing the capacitance transients from pulses with different widths gives a way to study multi-level traps.

In practice[48], the capacitance transient is also approximated by a multi-exponential function of time with the form

$$C(t) = C_0 + \sum_{i=1}^{N} C_i \exp(-e_i t) \tag{2.39}$$

By applying various pulses with widths of six orders from 10 μs to 1s upon an Al_xGa_{1-x} *GRINSCH-SQW* laser diodes, three trap levels were successfully obtained in the measurements, among which two levels had a very small energy difference of 0.049 eV. The experimental process is explained in Fig. 2.14.

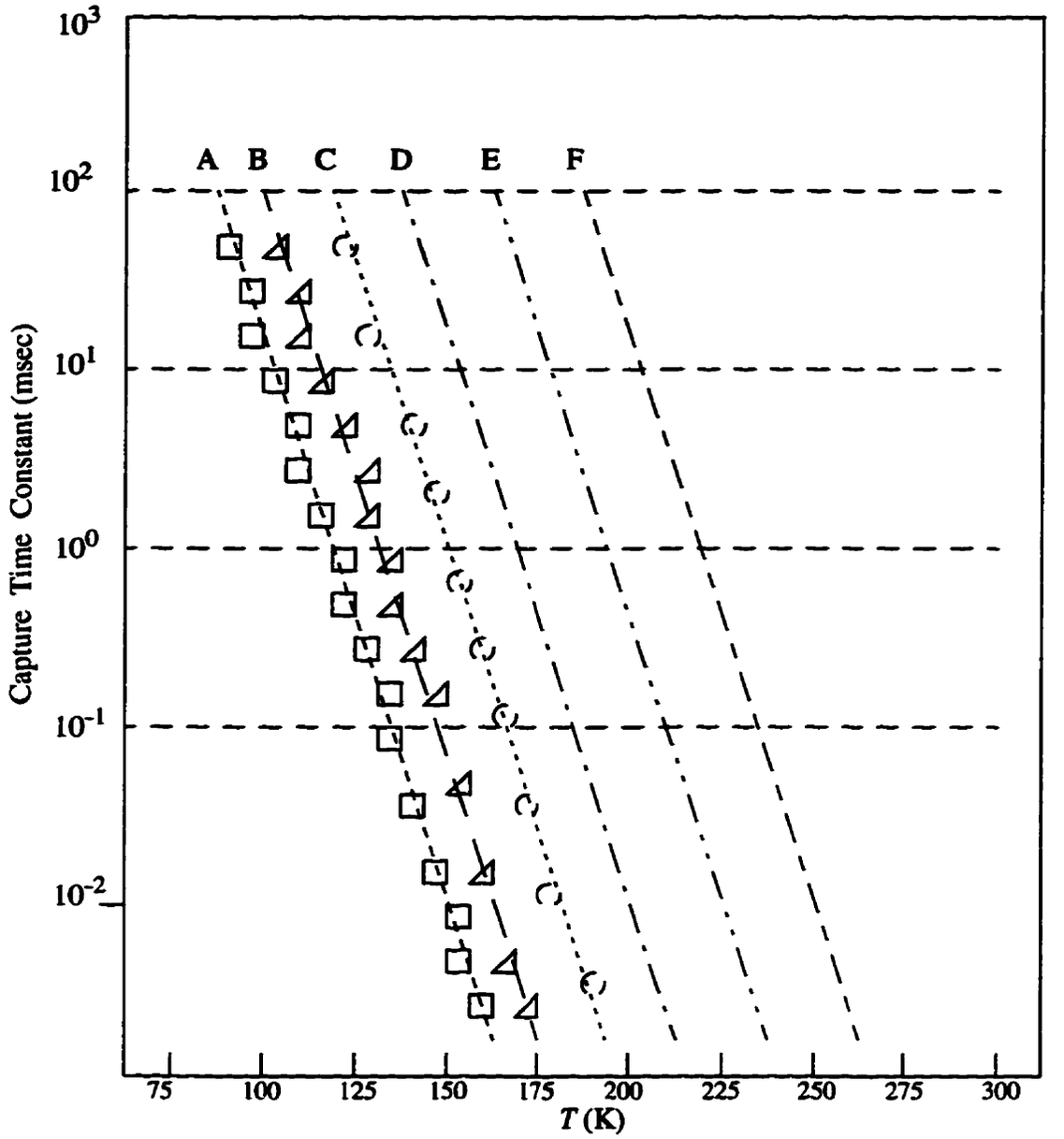


Fig. 2.14 Curves A, B, C, D, E and F correspond 0.1, 1, 10, 10^2, 10^3 and 10^4 times capture time constant of E_{t1} trap, respectively. Curve B corresponds to the averaged or weighted capture time of curves A and C. As long as the applied pulse width follows a curve between curves A and C, a decomposition of the DLTS signal for the shallower trap can be obtained [after Wang, et al.[48]].

Supposing that we have two trap level with emission rate e_{1a} and e_{1b} which could only be seen as one trap e_1 in a conventional rate-window full-width pulse DLTS. First., by filling th shal-

lower trap e_{1a} with a certain narrow pulse, a DLTS signal peak can be obtained in the DLTS spectra, and the active energy ΔE_{T1a} can be obtained for the shallower trap. The second step is following with a wide enough pulse filling both traps whose DLTS peaks are mixed in an ordinary transient. The new DLTS spectra peak is then compared with the former one appears in the first step. For the latter DLTS spectra is a result of two traps, the substitution of the two DLTS spectra will give the solo curve for the deeper trap, therefore, the active energy ΔE_{T1b} can be evaluated for the deeper trap.

Equation (2.39) for this case is rewritten as

$$\frac{\Delta C(t)}{C_0} = C_{1a} \cdot \exp-(e_{1a} \cdot t) + C_{1b} \cdot \exp(-e_{1b} \cdot t) \tag{3.40}$$

where e_{1a} and e_{1b} can be obtained by general analysis on the Arrhenius plot shown in Fig. 2.14.

The amplitudes C_{1a} and C_{1b} are proportional to the concentration of each component, and the height of the DLTS peak is also proportional to the trap concentration,

$$\frac{C_{1a}}{C_{1b}} = \frac{P_{1a}}{P_{1b}} \tag{3.41}$$

From Eq. 3.38 and Eq. 3.39 , C_{1a} and C_{1b} are easily fitted.

4. Multi-point Correlation DLTS.

For a broad response linewidth of the conventional DLTS standard peak as a function of temperature severely restricts the energy resolution of deep level defect measurements, the multi-point correlation DLTS was invented[29] and then improved[49] . It is actually an n-th order filtering correlation method. More than two points are taken in the capacitance decay curve instead of two to get the ΔC curve. The multi-point correlation DLTS with $n \geq 3$ allows obtaining more narrow individual DLTS peaks, which is shown in Fig. 2.15 with simulated DLTS spectrum.

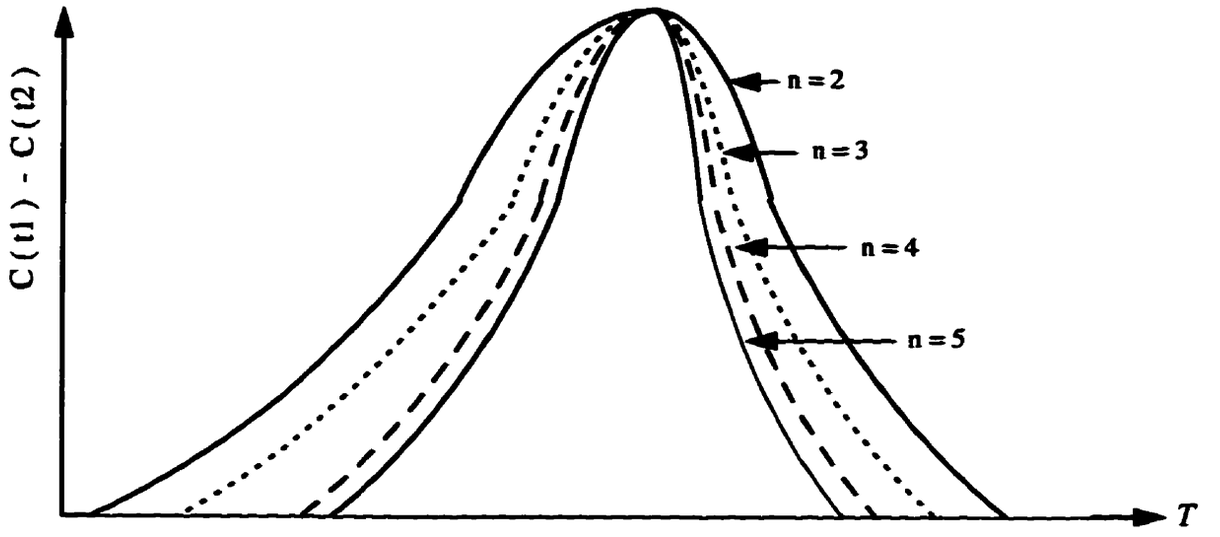


Fig. 2.15 Simulated DLTS spectrum for the energy level $\Delta E_T = 0.49eV$ as a function of the normalized temperature T/T_{mzx} with r = 2 and n as a parameter [after Dmowski, etc.[49]].

5. Parameter Evaluation DLTS

The former described methods either somehow simply follow the conventional DLTS analysis method (like multi-point correlation DLTS and temperature-dependent pulse-width DLTS) or use rate window as the basic concept for the data-acquisition (FFT and moment method). Since we have Eq. (2.39) as a general model for capacitance transient of more than one deep-levels, numerical resolution based on a full-curve-data acquisition has full utilization of the data.

After some early works[50-53] on linear predictive modeling for the analysis of DLTS measurements, Nener et al.[54] established a method to evaluate the activation energy ΔE_T, capture cross section σ_n, and density of deep-level traps N_T from the capacitance transient, called parameter evaluation DLTS. Figure 2.16 shows the schematic diagram of the automated DLTS system. The temperature scan was taken with the step of 5K.

Taking advantage of the full-curve-data acquisition system (fast digital capacitance meter, fast computer, etc.), this method simply uses one of the mature data modelling methods to evaluate the desired parameters in Eq. (2.39) with assuming one, two or even more trap levels.

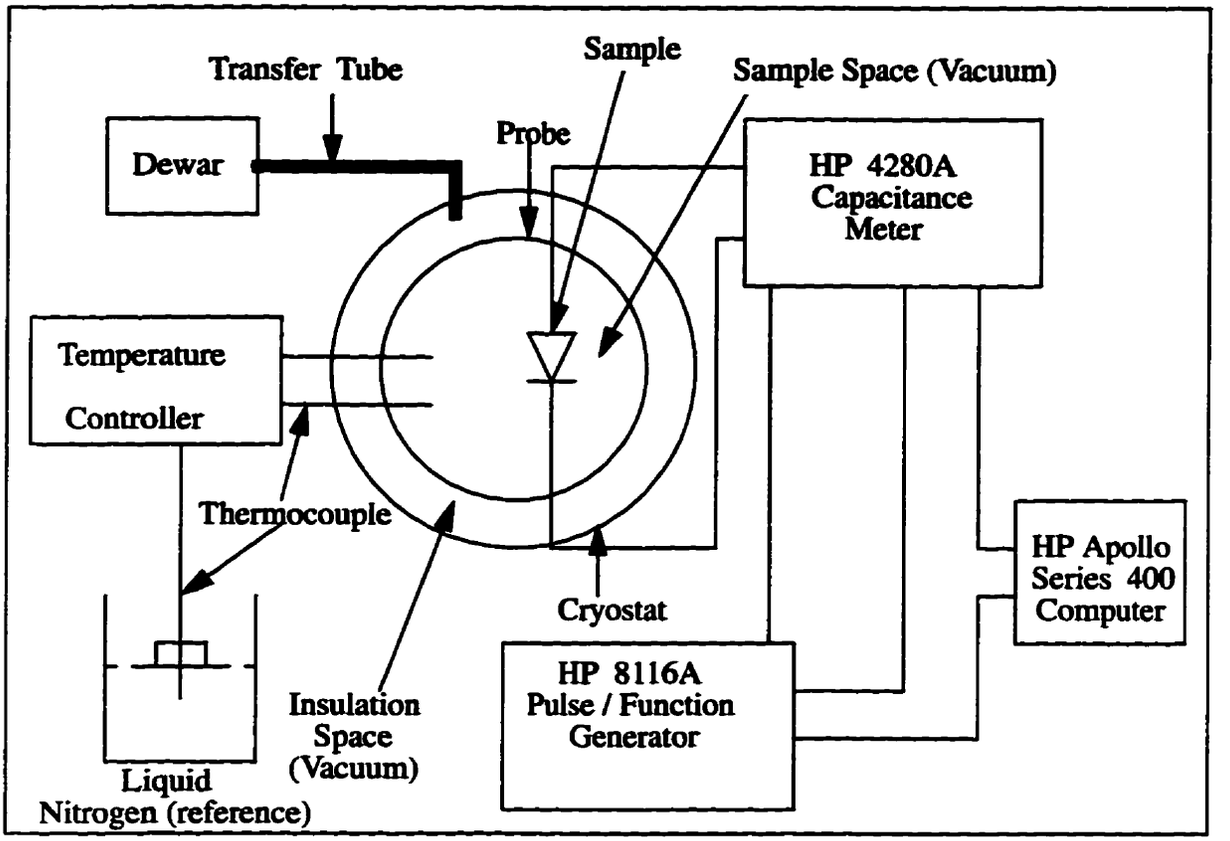


Fig. 2.16 The block diagram of the automated digital DLTS system [after Nener, etc.[54]].

The parameter evaluation with the help of an automated digital computer system has impressive advantages over the methods mentioned above:

1). This technique requires only a single temperature scan;

2). It can resolve multi-exponential transients;

3). The whole system is automated and the calculations can be programmed in a computer;

4). In contrast to FFT and method of moments, this method works directly in the time domain. It is no longer necessary to estimate and remove the baseline before analysis;

5). No weighting function is needed in the data analysis, which will benefits the signal/noise ratio.

III. MOS DLTS

DLTS has been successfully used for the determination of bulk and interface traps for MOS systems. The principle of DLTS for MOS systems are briefly described as follows[55-60]:

MOS system has bulk traps in semiconductor substrate, charge states in semiconductor-oxide interface and inside the oxide. They are inevitably induced to the MOS during the fabrication processing. Consider an MOS capacitor with an n-type Si substrate (Assuming that the oxide charge state is negligible for its small amount). As illustrated in Fig. 2.17(a), a reverse bias V_a is applied to the MOS to keep the Si substrate in deep depletion. The traps with the active energy $E_T > E^a_{FS}$ are empty. In Fig. 2.17(b), A forward pulse V_p changes the substrate from a deep to a weak depletion or accumulation, so that the injected electrons are captured by the interface and bulk traps which are between Fermi-levels E^a_{FS} and E^b_{FS}. After V_p is removed, the newly captured electrons are emitted from both interface and bulk traps as shown in Fig.2.17(c). MOS capacitance transient then consists of interface trap emission as well as bulk trap emission.

1. Electron Emission From Bulk Traps

The electron emission from bulk traps in an MOS system is identical to that in a p-n junction, except that the capacitance of an MOS includes both oxide capacitance and semiconductor depletion region capacitance in series.

Supposing that the boxcar DLTS is applied, and a discrete level bulk traps are considered for simplicity, the capacitance correlation signal ΔC_{max} for the bulk traps can be expressed by:

$$\Delta C_{max} = -S(e_n) \cdot \frac{C^3 N_T(E_T)}{\varepsilon_s C_{ox} N_d} \tag{2.42}$$

where $$S(e_n) = \exp(-e_n t_1) - \exp(-e_n t_2) \tag{2.43}$$

and C_{ox} is the capacitance of the oxide.

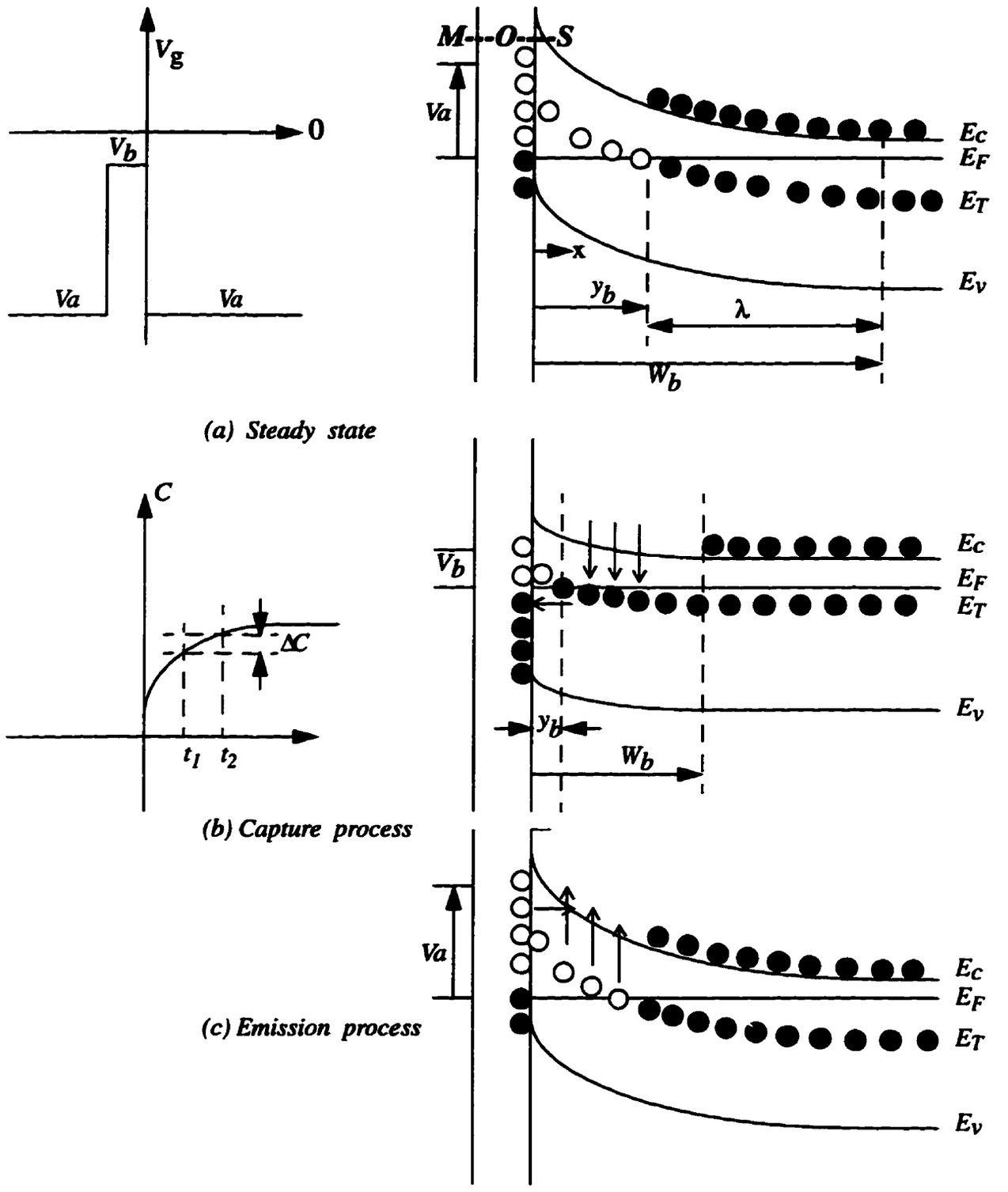


Fig. 2.17 Sequence of the bias voltages and resulting capacitance transients. Energy banding and electron occupancy of interface states and bulk traps in an MOS capacitance with an n-type substrate with a quiescent bias V_a (a), in the trap-filling process with a bias $V_b = (V_a + V_p)$ (b), and in the emission process with the quiescent bias V_a(c).

As $e_n = \sigma_n \upsilon_n N_c \exp\left(\frac{(E_T - E_C)}{kT}\right)$, the correlation signal ΔC reaches to its maximum value when $e_n = \ln(t_2/t_1)/(t_2 - t_1)$.

The energy level and the capture cross-section, the concentration of bulk traps can then be calculated from an Arrhenius plot of the emission rates obtained by various t_1 and t_2, using the same procedure used for the p-n junctions discussed early in this chapter.

2. Electron Emission From Interface states

Assuming that the interface trap density is D_{it}, and the capacitance produced by qD_{it} is much smaller than oxide capacitance C_{HF}. The total capacitance of the MOS

$$\Delta C = \frac{C^3}{\varepsilon_n C_{ox} N_d} \int_{E_{FS}^a}^{E_{FS}^b} S(e_n(E))\, D_{it}(E)\, dE \tag{2.44}$$

where E_{FS}^b and E_{FS}^a are the Fermi-levels for free electrons at the end of the capture process and in the emission process, respectively. If σ_n is not strongly dependent on energy, the energy $E_{it,\,max}$ which gives the maximum $S(e_n(E))$ can be written as:

$$E_{it,\,max} = E_c - kT \ln\left[\sigma_n \upsilon_n N_c \cdot (t_2 - t_1)/\ln(t_2/t_1)\right] \tag{2.45}$$

and the energy distribution range ΔE_{it} at half-maximum of $S(e_n(E))$ is estimated as:

$$\Delta E_{it} = kT \ln(t_2/t_1 + 10) \tag{2.46}$$

Assuming that D_{it} varies slowly in the energy width of 3kT around $E_{it,max}$, the $D_{it}(E)$ term can be taken out of the integral of Eq. (2.44). Then we have

$$\Delta C = -\frac{C^3}{\varepsilon_n N_d} \cdot \frac{kT}{C_{ox}} \cdot D_{it}(E_{it}) \cdot \ln(t_2/t_1) \tag{2.47}$$

Therefore, $E_{it,max}$, D_{it} and capture cross section σ_n can all be calculated from Eq. (2.43), Eq. (2.45) , Eq. (2.46) and Eq. (2.47), using the same method used for the case of bulk traps, by a series of temperature scans.

3. Distinction Between Interface States and Bulk Traps

Equation (2.44) indicates that the ΔC versus T plot of the interface states is directly related to the energy distribution within the energy window between E_{FS}^{a} and E_{FS}^{b} , which are the Fermi-levels at the SiO_2 / Si interface for the reverse bias V_a and for the bias voltage with the pulse V_p respectively. The change of pulse voltage V_p will bring the changes of the shape and the temperature for the peak of the ΔC versus T plot. In contrast, a bulk trap has a certain active energy level so that its emission rate is constant at a certain temperature regardless of the changes of the pulse voltage. Therefore, the shape and the temperature for the peak of ΔC versus T plot for a bulk trap should not change with the pulse voltage.

A $\Delta C \sim T$ curve of the MOS capacitor----MOS DLTS spectra may contain several peaks: one or more than one for the bulk traps and another one for the interface traps. The one which responds to the height of the pulse voltage with changes of the shape and the position along the temperature is treated as interface traps, while the one which does not change in position and shape with the pulse voltage belongs to bulk traps.

4. Effects of Minority-carrier Generation

For an MOS capacitor, the minority-carrier generation can interfere with majority carrier DLTS

spectrum, especially at high temperatures and at high *EHP* (electron-hole pair) generation. The correlation signal ΔC due to the minority carrier generation increases with increment of the quiescent bias voltage V_a in the negative direction, the signal due to emission does not. And the generation usually occurs at high temperatures, so that its effects to $\Delta C_{max} - T$ curve (DLTS spectra) are also at high temperatures. This provides a measure for eliminating the effects of minority-carrier generation to the analysis of MOS DLTS.

The MOSFET's have an advantage over MOS-capacitors for DLTS measurements[58] in two aspects: 1)with a three terminal MOSFET, minority-carriers are collected by the reverse biased source/drain to avoid the effects of minority-carrier generation, in the meantime, majority-carriers are captured by pulsing the gate for the interface trap-majority-carrier characterization in the upper half of the band gap; 2)with the source/drain forward biased, an inversion layer forms allowing interface traps to be filled with minority-carriers while the majority-carriers flow to the source / drain. Therefore, the lower half of the band gap can also be explored without the minority-carrier generation.

Many DLTS applications have been developed in MOS devices by many researchers with little change in the conventional DLTS. The CC-DLTS provides a slightly simpler formula for the analysis[33]. But the entire curve analysis methods have difficulties to be used in the MOS interface-state density detection for the interface-state densities distribute continuously with respect to activation energy, which makes a different mechanism in the transients, and the DLTS spectra contain both interface state and bulk trap emissions. Lately, the multi-point correlation method has been successfully applied for bulk trap and interface state measurements for MOS system with improved sensitivity.

Several researchers[61-70] have used the DLTS as the most efficient tool in investigating the performances of solar cell and other semiconductor devices. Various DLTS systems are recently commercially available as a whole package for more and more DLTS applications in electronic industries.

CHAPTER 3

DESIGN OF A COMPUTERIZED DLTS SYSTEM

3.1. Design Principles

To build a full-curve computerized DLTS system, two key pieces of electric apparatus, besides a fast computer and the generally necessary measurement instruments, are required for the system.

I. A fast capacitance meter--Capacitance measurements involve an integration process which takes a certain amount of time to be completed. A fast capacitance meter has a short measurement time and responds quickly to minimize the time gap between two data.

II. A memory card--A one-by-one data transportation from the capacitance meter to the computer could make a C-t curve nonsense, because its processing time is variable . A memory card stores a number of measurement data directly and releases them in a whole package to the computer later when needed. This can secure the time gap between two stored data to be known and a true C-t curve.

A GPIB (General Purpose Interface Bus) card is also required for the computer to control and to operate the whole system automatically. All electronic components and hardware of the system are commercially available and some are chosen from our laboratory.

3.2. The Details Of The DLTS System

The block diagram of the system is shown in Fig. 3.1. The system consists of three subsystems:

I. The direct measurement subsystem.

(i). Air Product cryostat.: This cryostat is capable of creating a laboratory interface of various temperatures from 15 K to 480 K. It is operated in conjunction with a temperature controller and a thermocouple so that the temperature can be stabilized and adjusted to any pre-determined

value. Our experiments are performed at temperatures from 50K to 315K with 5K a step.

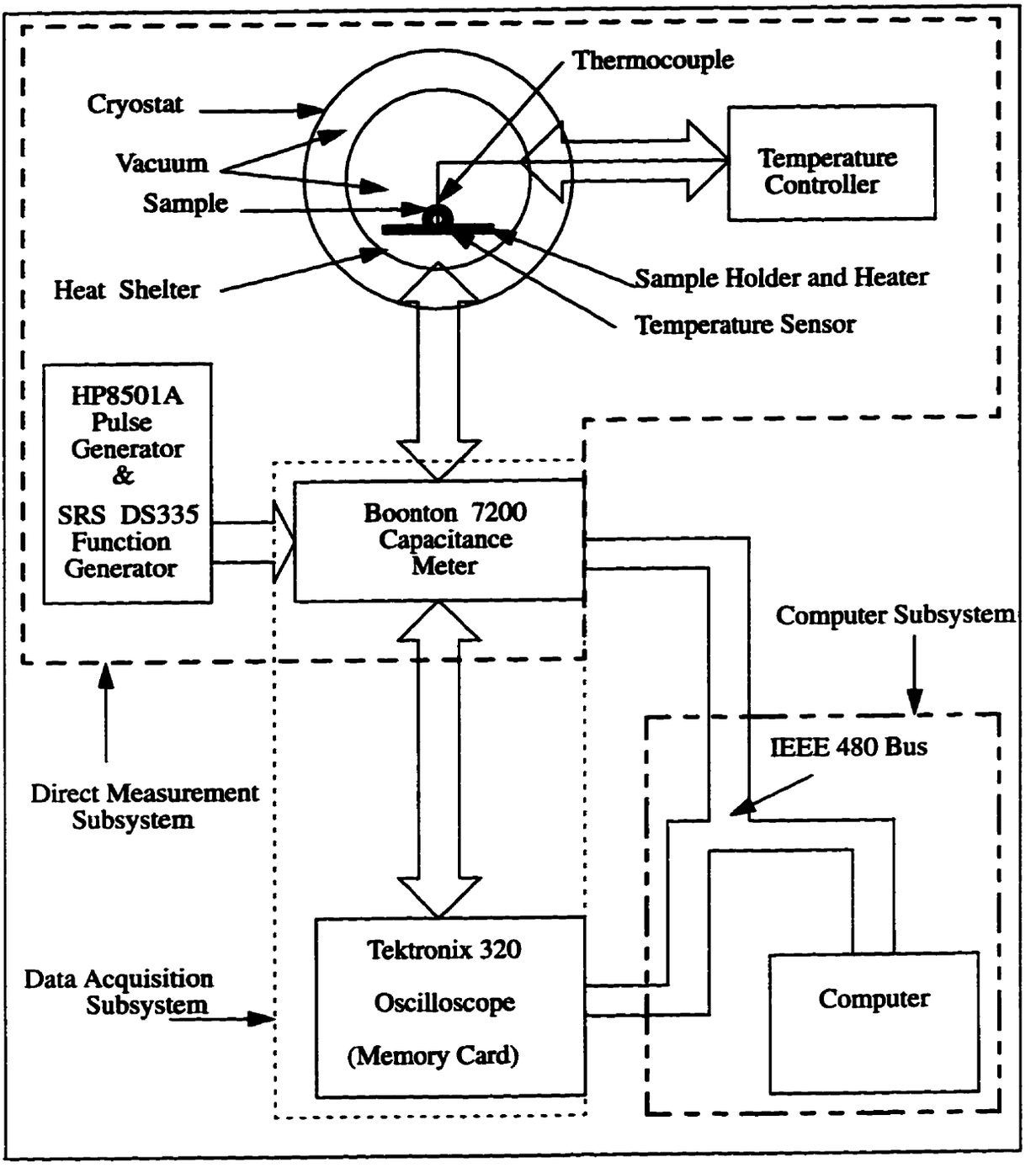


Fig. 3.1 The block diagram of the system.

(ii). Boonton model 7200 capacitance meter: This meter has a fast response feature. The specifications for capacitance measurements are:

Resolution: 0.001 pF	for range	0 to 2 pF;
0.01 pF	for range	2 to 20pF;
0.1 pF	for range	20 to 200pF;
1 pF	for range	200 to 2000pF;

Accuracy: 0.25% of reading + 0.2% of full scale.

By zeroing a standard capacitance or setting the capacitance under a quiescent bias condition C_0 to zero, the capacitance output will directly equal to ΔC so that the measurement range can be kept as small as possible (as long as ΔC's are inside the measurement range) to obtain better resolution and accuracy.

(iii). SRS SD335 function generator and HP8501A pulse generator: The sample is applied with the assigned quiescent bias V_a and pulse voltage $V_b - V_a$ through the test terminal marked "High" on the capacitance meter. Here, V_b is the capture voltage. The pulse amplitude and duration are pre-set and adjusted to any assigned values. The error rate is 0.1% for the range chosen. Figure 3.2 shows the bias voltages applied to the sample. The pulse duration is from 5ms to 200ms.

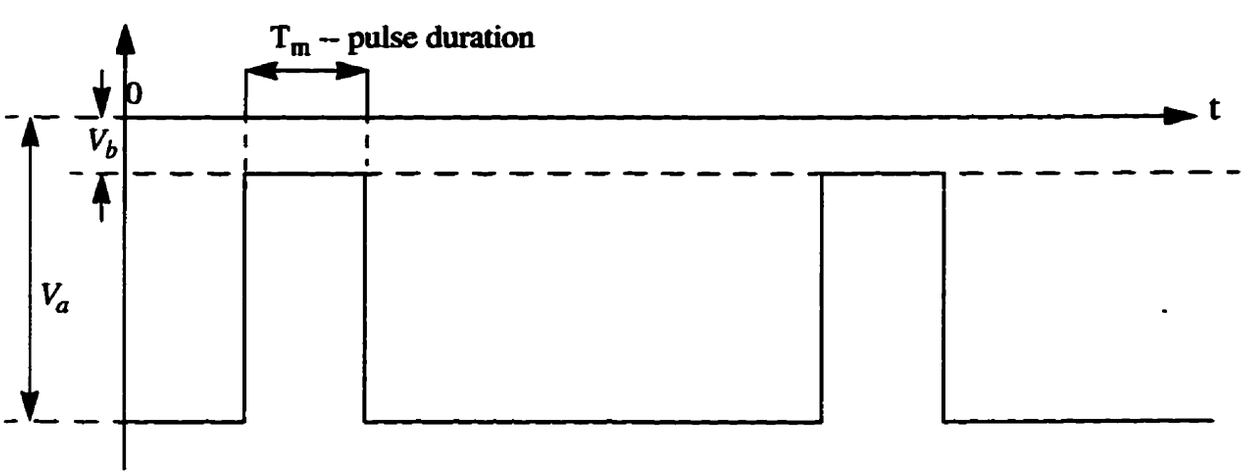


Fig. 3.2 Schematic diagram showing the magnitudes and duration of the voltages applied to the sample.

II. The data acquisition subsystem

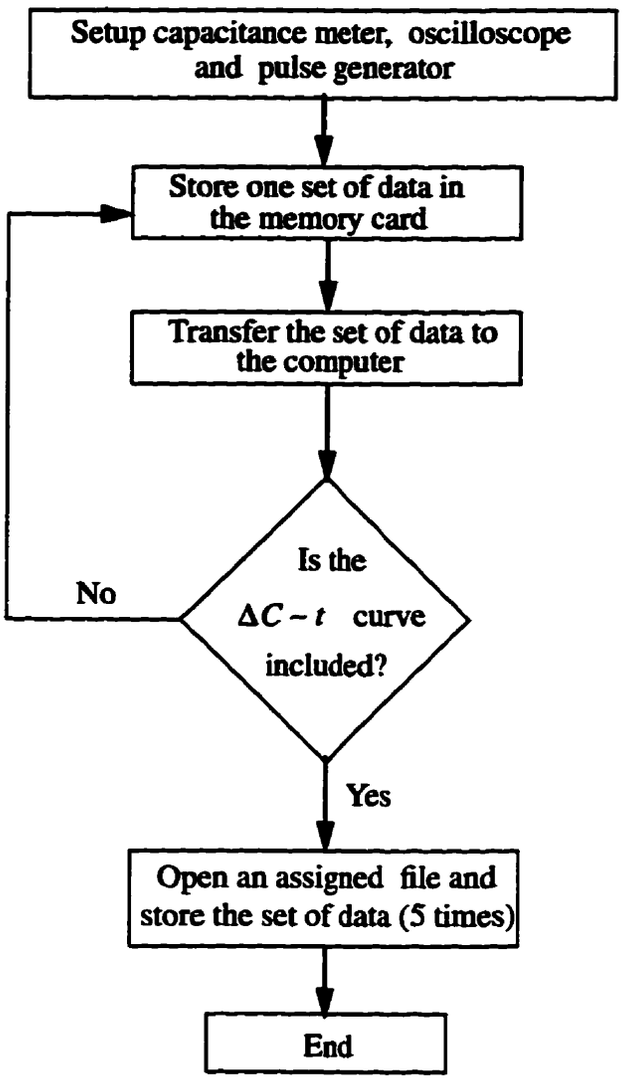
Since the Boonton 7200 capacitance meter is not equipped with a memory card, the digital data directly converted from the capacitance meter can only be transferred to the computer one-by-one. Therefore, Tektronix 320 oscilloscope is used to take the analog signal from the capacitance meter and then convert the signal to digital data. These data are then stored in a built-in memory card with a capacity of one thousand 8-digit data. The time gap between two data can be monitored by the oscilloscope. This provides an excellent means of avoiding the unwanted one-by-one data transportation. The data transportation takes place only after the one thousand desired data have been recorded in the memory card with the time gap properly adjusted between two data.

III. The computer subsystem

A 486 PC computer with a Turbo C++ program compiler is the system controller and raw data terminal. A GPIB card is installed in the system as a medium for the communication among the computer and other apparatus. A set of general functions are pre-defined in the card, which makes the control software much easier and the operation faster. The computer automatically controls the whole system in a time sequence. It sends commands to and receives data from the GPIB bus and puts every set of raw data into a corresponding opened file for further numerical analyses. Here, each of the $\Delta C \sim t$ curves is saved for 5 times.

3.3. The Computer Programs

A system-control program has been developed in Turbo C^{++} for the automatic system operation of the capacitance decay curve measurements for both of the MOS capacitor and the p-n junction. The program is organized in logical blocks shown in Fig. 3.3, and the program is given in Appendix I. The data processing program for the DLTS of the MOS capacitor is organized in a different way from the program for the DLTS of p-n junction.



.Fig. 3.3 The logical procedure of the control program.

I. Data processing program for the MOS capacitor.

The differential capacitance inside a rate window at a temperature T is $\delta C|_T$ which is directly taken from the raw data file, i.e., $\delta C|_T = [\Delta C(t_2) - \Delta C(t_1)]|_T$, while $\Delta C(t)$ is the raw data. The δC's from a temperature scan with one of the rate windows under a certain bias condition are stored in the same file with a certain file name to form a DLTS spectra ($\delta C \sim T$ curve). A data wave-form averaging function is added to the data processing program to eliminate the noise of the system. The outline of the program procedure for the data processing of

MOS analysis is shown in Fig. 3.4 which is the logical blocks of the program. The analysis principle is based on the boxcar DLTS. Data processing and analysis for the MOS capacitor are discussed in chapter 4.

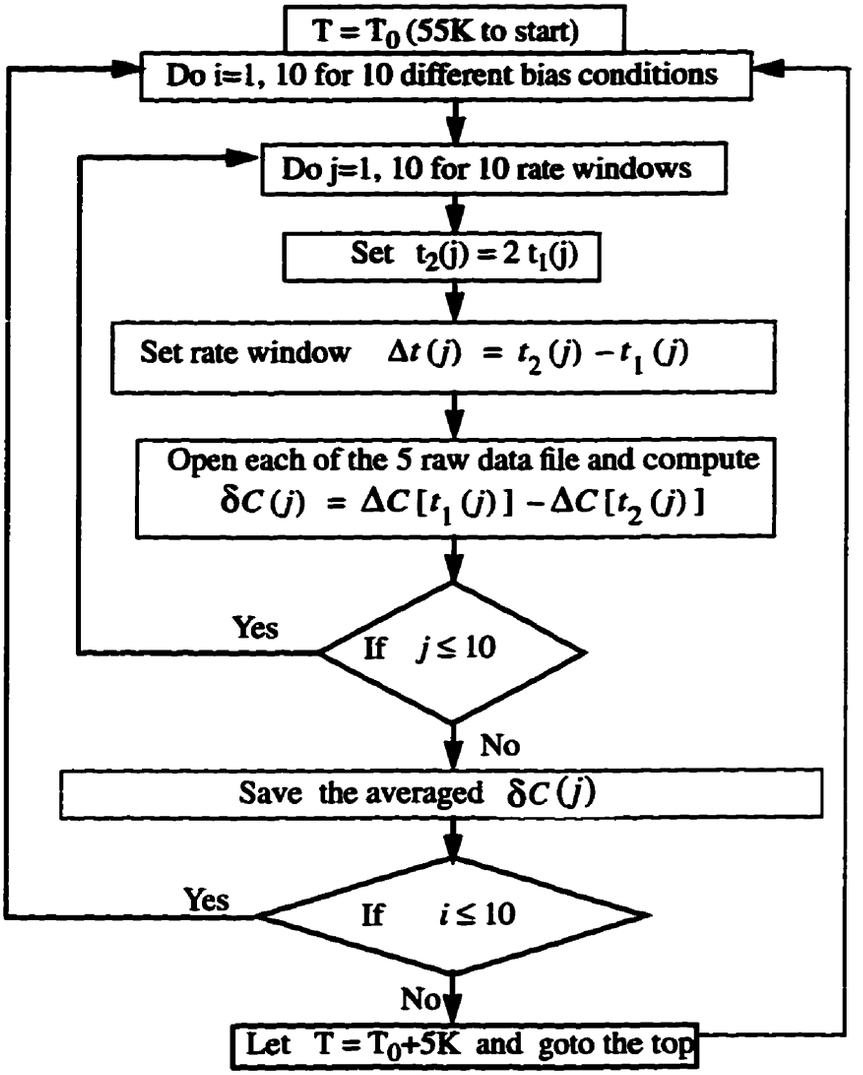


Fig. 3.4. The logical block diagram of the data processing program for the MOS data analysis.

II. Data processing program for p-n junctions.

The method of the parameter evaluation can be used in our computerized DLTS to take the advantage of the full-curve digital data. The numerical analysis program outline is developed. Before running the numerical analysis program, the raw data is also averaged to reduce the noise level. The general expression for a multi-level trap transient of a p-n junction after the application

of a pulse can be expressed as:

$$C(t) = C_0 + \sum_{j=1}^{M} C_j \exp(-e_j t) \qquad (3.1)$$

where C_0 is the capacitance under the quiescent bias condition; C_j is the constant for j-th trap level; e_j is the emission rate of j-th trap level; M is the number of trap levels. For mathematical simplicity, all the parameters in Eq. (3.1) are replaced by $a(j)$, where $j \le m = 2M + 1$ and m is the number of parameters.

For M=1, i.e., in the case of one deep level, Eq. (3.1) can be simplified to:

$$C(t) = a(1) + a(2)\{1 - \exp[-a(3)t]\} \qquad (3.2)$$

$a(j)$ apparently has physical meanings: $a(1)=C(t=0)$; $a(2)=C_0-C(t=0)$ and $a(3)=e_n$, which is the emission rate.

For $M \ge 2$, i.e. in the case of more than one deep levels, Eq. (3.1) can be simplified as

$$C(t) = a(1) - a(2)\exp[-a(3)t] - \ldots - a(m-1)\exp[-a(m)t] \qquad (3.3)$$

where

C_0 = $a(1)$ = capacitance under the quiescent bias condition

$C(t=0)$ = $a(1) - a(2) - a(4) - \cdots\cdots - a(m-1)$

Assuming that each data point (C_i, t_i) has the same standard deviation σ, then the Chi-square fitting can be used to minimize this deviation.

$$\chi^2(\vec{a}) = \sum_{i=1}^{N} \left(\frac{C_i - C(t(i,\vec{a}))}{\sigma} \right)^2 \qquad (3.4)$$

where $\vec{a}$ is the parameter vector [*a(1), a(2),...,a(m)*], N is the number of data points, C_i is the experimental data at ith point, and $C(t_i, \vec{a})$ is from Eq. (3.1) .

With the aid of the Levenberg-Marquart method and the standard of nonlinear least-square routine, we can obtain:

$$\sum_{l=1}^{m} \alpha'_{kl} \delta a_l = \beta_k \qquad (3.5)$$

where δa_l is the increment of the current a_l, and

$$\alpha'_{kl} \equiv \alpha_{kl}(1+\lambda) \qquad k = l$$

$$\alpha'_{kl} \equiv \alpha_{kl} \qquad k \neq l \qquad (3.6)$$

α_{kl} is defined as

$$\alpha_{kl} \equiv \frac{1}{2} \frac{\partial^2 \chi^2}{\partial a_k \partial a_l} \qquad (3.7)$$

The parameter evaluating procedure is then as follows:

i. Take $M=1$ and Eq. (3.2) as the model:

ii. Pick an initial guess for $\vec{a}$ and σ, while *a(1), a(2)* are from the experimental data directly, *a(3)* is roughly estimated as $\left.\frac{dt}{dC(t)}\right|_{t=0}$; σ is the average fluctuation of C_i;

iii. Compute $\chi^2(\vec{a})$;

iv. Pick a modest value for λ in Eq. (3.6) , say $\lambda = 0.001$;

v. Solve the linear equation Eq. (3.6) for $\delta\vec{a}$ and evaluate $\chi^2(\vec{a} + \delta\vec{a})$, and compute σ with the new $\vec{a}$, using

$$\sigma^2 = \left(\sum_{i=1}^{N} (C_i - C(t_i, \vec{a}))^2 \right) / N \qquad (3.8)$$

vi. If $\left|\chi^2(\vec{a} + \delta\vec{a}) - \chi^2(\vec{a})\right| \le 10^{-3}$, go to step viii;

vii. If $\chi^2(\vec{a} + \delta\vec{a}) > \chi^2(\vec{a})$, increase λ by a factor of 10 and go back to step v;

If $\chi^2(\vec{a} + \delta\vec{a}) < \chi^2(\vec{a})$, decrease λ by a factor of 10 and go back to step v;

viii. Compute the incomplete gamma function $Q\left(0.5\nu, 0.5\chi^2(\vec{a})\right)$. If $Q\left(0.5\nu, 0.5\chi^2(\vec{a})\right) <$ 10^{-3}, go back to step ii with an increased new σ by a factor of 3/2 ;

If $\left|Q\left(0.5\nu, 0.5\chi^2(\vec{a})\right) - 1\right| < 0.1$, go back to step ii with a decreased σ by a factor of 2/3;

ix. otherwise, for the rule of thumb, a typical value of $\chi^2(\vec{a})$ for a "moderately good fit is

$$\chi^2(\vec{a}) \approx 0.5\sigma^2 \qquad (3.9)$$

Therefore, if $\left|\chi^2(\vec{a}) - 0.5\sigma^2\right| \le 0.1\chi^2(\vec{a})$, we have a reasonable solution for the parameter evaluation;

x. Start from step i with *M=2* and Eq. 3.3 as the model, carry out the whole process from step ii to step ix;

xi. Compare the quantities of the incomplete gamma function Q for the models of $M = 1$ and $M = 2$, the model with a larger Q is a better model.

The block diagram of the numerical program is shown in Fig. 3.5.

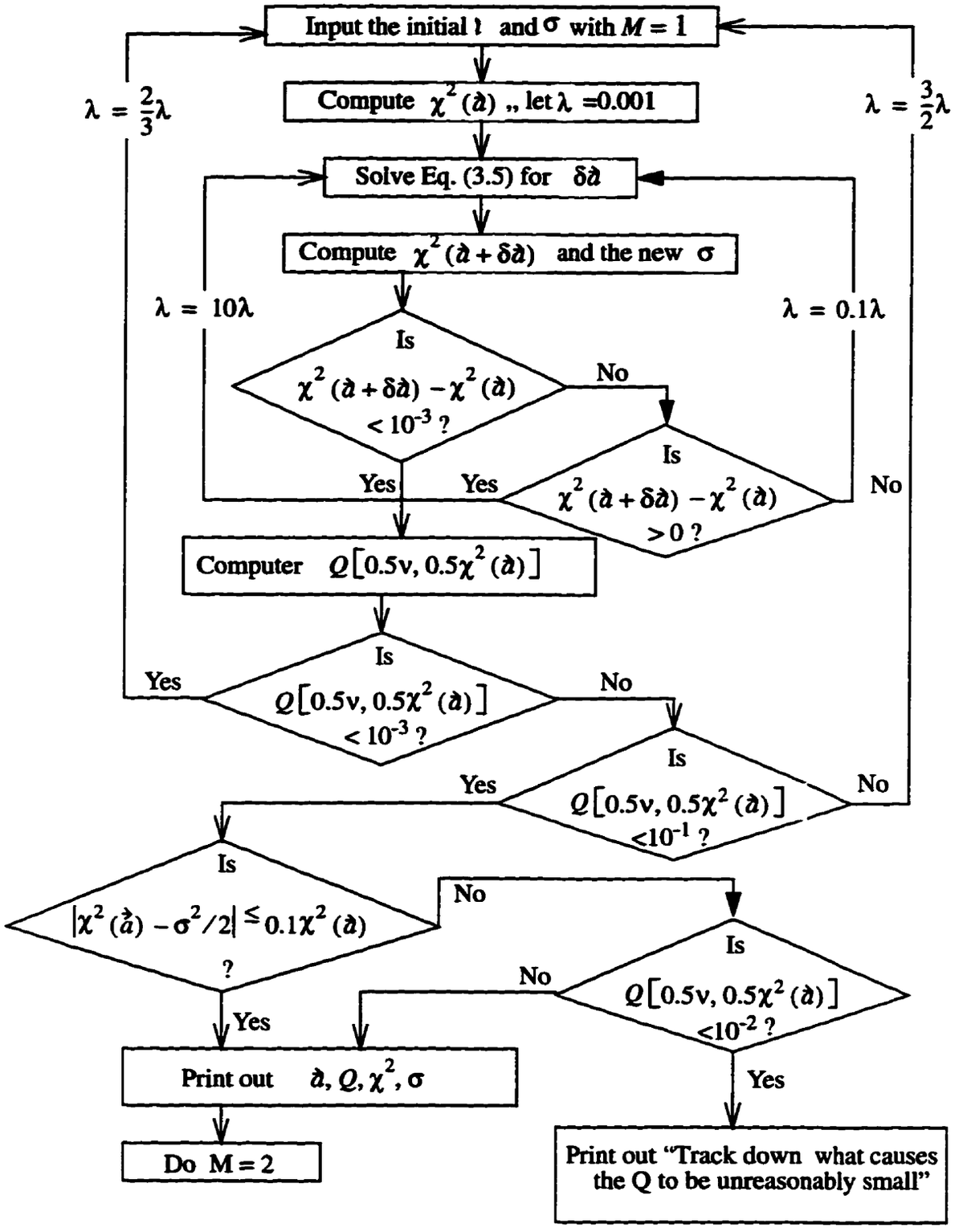


Fig. 3.5. The block diagram of the numerical program for the evaluation of the parameters evaluation DLTS.

CHAPTER 4

EXPERIMENTAL DATA PROCESSING AND DISCUSSIONS

In this chapter, we describe the experimental data processing using MOS capacitor samples and discuss the results. The MOS capacitor samples were fabricated in our Materials and Devices Research Laboratory. The SiO_2 films were deposited on n-type, <100> oriented, 2-4Ω-cm silicon wafers as substrates at $300°C$ using a microwave ECR plasma system[71]. The substrates were cleaned by the RCA method with $17\times10^6\Omega-cm$ deionized water. Prior to loading, the substrates were dipped in a reduced HF/H_2O solution(1/100 cm^3) to remove the native oxide on the substrate surfaces. Aluminium counter electrodes of $860\mathring{A}$ in thickness and $7\times10^{-2}cm^2$ in area were vacuum-deposited through a shadow mask to form MOS capacitors.

4.1. Steady C-V Characteristics

The Boonton 7200 capacitance meter is programmed to automatically carry out the measurements of the high frequency C-V characteristics. The voltage applied to the MOS capacitor sweeps from -8V to 8V in order to obtain both the strong forward and the reverse bias conditions for capacitance measurements. The frequency at which the capacitance is measured is 1.0MHz. Because the minority-carrier response time is about 0.01--1 second[10], the rise rate of the applied voltage is set at 0.1V/sec so that the *C-V* characteristics can be treated as steady high frequency *C-V* characteristics. Figure 4.1 shows the *C-V* characteristics at room temperature(T=299K).

Assuming that the interface charge capacitance is much less than the oxide capacitance C_{ox} and can be ignored, the MOS capacitance C can be expressed as:

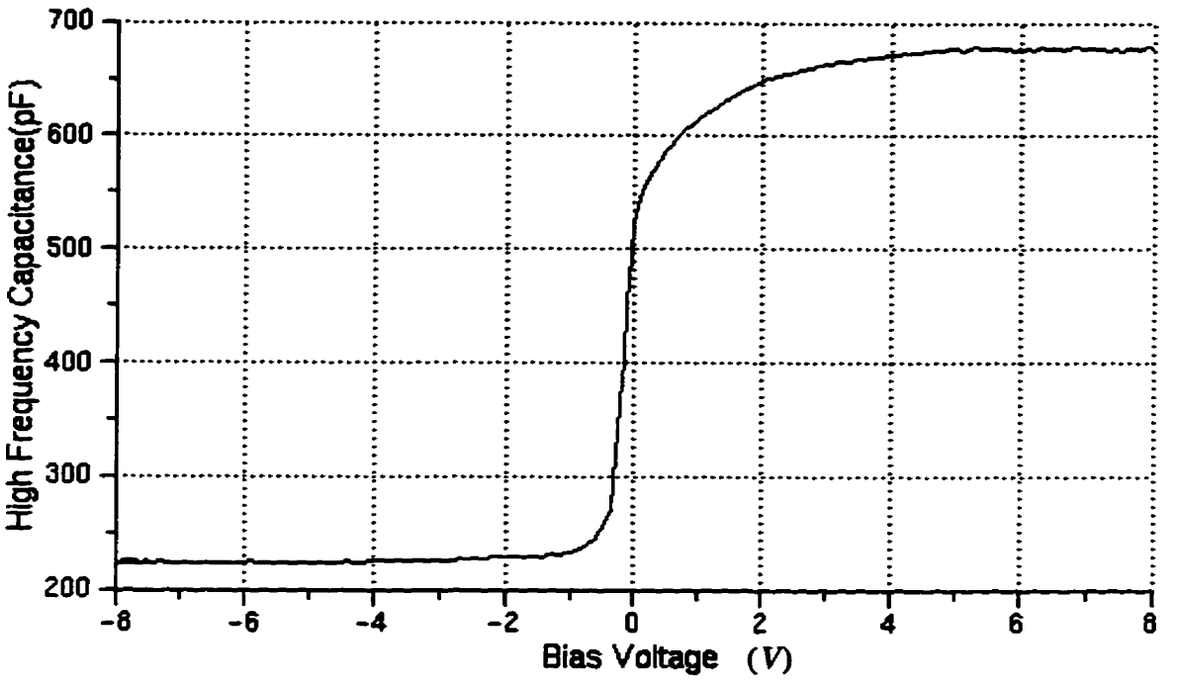


Fig. 4.1. The high frequency C-V characteristics of the MOS capacitor at $T = 299K$. $C_{max} = 677\,\text{pF}$, $C_{min} = 224\,\text{pF}$, and $C(V = 0) = 523\,\text{pF}$.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{4.1}$$

where C_s is the capacitance of the depletion region of the semiconductor. When the MOS capacitor is strongly forward-biased, C reaches its maximum value C_{max} which, in fact, is equal to C_{ox}; when the MOS capacitor is strongly reverse-biased, its capacitance becomes the minimum value C_{min}. With the measured maximum and minimum values of the MOS capacitance, the capacitance of semiconductor in the strong reverse bias condition, C_{SR}, can be expressed as:

$$\frac{1}{C_{SR}} = \frac{C_{ox} - C}{C_{ox} \cdot C} = \frac{C_{max} - C_{min}}{C_{max} \cdot C_{min}} \tag{4.2}$$

With the known value of C_{SR}, the doping concentration of the n-type semiconductor for the MOS capacitor can be determined by[72]:

$$N_d = \frac{2\phi_{i,inv} C^2_{SR}}{qK_s\varepsilon_0 A^2} \tag{4.3}$$

where $\phi_{i,inv}$ is the surface potential in strong inversion, which is equal to $2\phi_F$, in which ϕ_F is the Fermi level of the n-type semiconductor with respect to the intrinsic fermi level. ϕ_F is given by:

$$\phi_F = \left(\frac{2kT}{q}\right)\ln\left(\frac{N_d}{n_i}\right) \tag{4.4}$$

where n_i is the intrinsic concentration of the semiconductor. Practically, $\phi_{i,inv}$ is slightly larger than $2\phi_F$[39b]. Thus, an empirical relationship between C_{SR} and N_d has been developed for silicon at room temperature[73]. With C_{SR} known, the doping concentration of n-Si can be determined by the expression:

$$\log(N_d) = 30.38759 + 1.68278\log(C_{SR}/A) - 0.03177\,[\log(C_{SR}/A)]^2 \tag{4.5}$$

where A is the area of the electrode of the MOS capacitor. Using this equation, C_{SR} is in F and A in cm^2 and N_d in cm^{-3}. For the MOS capacitor samples used for this investigation, the electrode area $A = 7\times10^{-2} cm^2$. The measured values of C_{max} and C_{min} are, respectively, 677pF and 224pF. The calculated C_{SR} from Eq. (4.2) is 334.83pF and N_d from Eq. (4.5) is 4.79×10^{16} cm^{-3} for the temperature of 299K.

4.2. Capacitance Transient Measurements

After a quiescent bias voltage (a strong reverse bias voltage) is applied to the MOS sample and the quiescent capacitance C_0 is measured, a forward bias voltage is superimposed to the quiescent bias voltage and applied to the sample. This forward bias pulse results in the filling of both the interface states and the bulk traps. As soon as the removal of the pulse at $t = 0$, the capacitance $C(t)$ will gradually decay because of the thermally-activated detrapping process. In this section, we shall describe the data collecting and processing in our DLTS system.

Because that the memory card in the digital oscilloscope can store only 1,000 data at once, the typical capacitance decay curves appearing on the screen of the digital scope are like the one in Fig. 4.2 (a) if a whole decay curve contains only 1,000 data points. Figure 4.2 raises a problem for the one-thousand-data-point data collecting technique: For a whole decay curve, the fast responding part of the curve gives information about the traps with activation energy closer to the conduction band edge, and the slow responding part about deep levels with activation energy closer to the Fermi-level. The number of data points for the fast responding part of the decay curve could be too small for the further analysis (With $t \leq t_s$, the curve in Fig. 4.2 (b) contains only ten data points). If the one-thousand data points are only for the fast responding part of the curve, i.e. the curve before $t \leq t_s$ in Fig. 4.2 (b), then the slow responding part of the decay curve will be lost.

To secure the information for all-round energy levels of bulk traps and interface states above the mid-gap in detail and in best resolution, and to provide a way to improve the signal/noise ratio, we rearrange the data collecting procedure as follows:

I. Apply one of the assigned bias conditions on the sample after an assigned temperature has been stabilized:

a. Apply a quiescent bias voltage on the sample and set the capacitance meter at zero. This allows the capacitance meter to display and to transfer the measurement data on $\Delta C = C(t) - C(0)$;

b. Since ΔC is much smaller than $C(0)$, it is possible to use a smaller test range of the capacitance in order to have a better resolution. For example, the test range of the capacitance

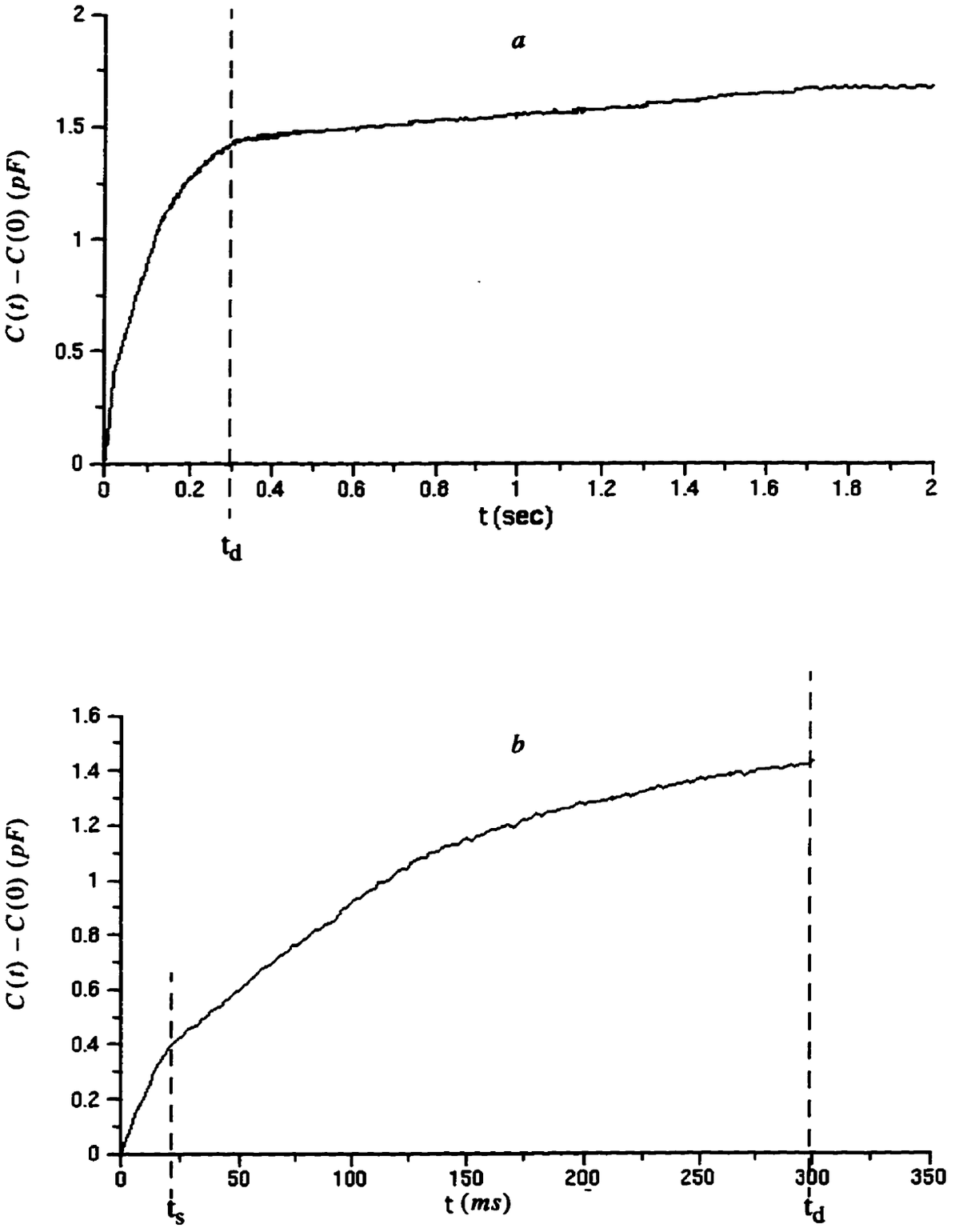


Fig. 4.2. (a).Typical full $\Delta C \sim t$ curve for $T = 210$K. (b). the part of the curve from t = 0 to t = t_d. The time gap between two data points is 2ms for both of (a) and (b).

meter can be reset to $0.000pF - 2.000pF$ for curves in Fig. 4.2 to get the best resolution of the capacitance meter, which is $0.001pF$ rather than $0.01pF$ for test range up to 20.00pF;

II. Adjust the settings of the digital oscilloscope until only the part of $\Delta C \sim t$ curve before t_s would appear on the screen (refer to curve in Fig. 4.2 (b)) within the full range(1,000 data points) and, store them in the memory card built in the oscilloscope;

III. Transfer the digital data from the memory card to a computer, open a data file to store the data. This step is repeated four more times so that this part of $\Delta C \sim t$ curve is recorded five times by five separated data files. Therefore, a data point can be later averaged to reduce the signal noise;

IV. Adjust the settings of the oscilloscope so that the part of $\Delta C \sim t$ curve before t_d will fully appear on the screen, and repeat step III;

V. Adjust the settings of the oscilloscope until the curve on the screen becomes flat to store the whole capacitance decay curve, which gives more detail information for the deeper level traps and the effects of minority-carrier injection. Then repeat step III.

4.3. Determination of Temperatures for the Peaks in DLTS Spectra

The mechanism of interface states is different from that of bulk traps, so that the method of parameter evaluation of DLTS for p-n junctions no longer applies to the DLTS analysis for MOS systems. Thus, we have to use the rate window method with refinement by the automated full decay curve acquisition technique.

The conventional rate window methods as described in chapter 2 have a limited number of assigned rate windows and differential capacitance data. With our new data collecting technique, we can have as many data points as needed in one temperature scan so that the choices and the number of rate windows are unlimited. This gives another advantage of this system over the conventional ones.

The modified DLTS procedure based on the rate window concept is as follows:

I. Collect the full $\Delta C \sim t$ curves in the way described in section 4.2 to ensure that all needed data are acquired;

II. Improve the signal/noise ratio by averaging the five ΔC data taken at exactly the same time in the five $\Delta C - t$ decay curves acquired at the same bias conditions and same temperature;

III. Apply a number of carefully chosen rate windows to the $\Delta C \sim t$ curves from the temperature scan to obtain $\delta C \sim T$, i.e. capacitance transient curves. δC is $C(t_1) - C(t_2)$ for a rate window (t_1, t_2);

IV. For any of the δC peaks appearing in a $\delta C \sim T$ curve for a specific rate window, the temperature at which the δC peak occurs and the rate window are used to plot a point in an Arrhenius plot;

V. Properly chosen rate windows give a complete Arrhenius plot for the determination of deep level parameters. For instance, rate window (t_1, t_2) has T_1 as the temperature at which the δC peak occurs. The peak shifts to another temperature T_2 when the rate window is changed to (t_1', t_2'). Assuming that the capture cross section σ_n is independent of the temperature, Eq.(2.23) for the energy level ΔE_T of traps can be rewritten as:

$$E_T - E_c = \frac{\ln\left(\frac{\ln(t_2/t_1)}{t_2 - t_1}/T_1^2\right) - \ln\left(\frac{\ln((t_2')/(t_1'))}{t_2' - t_1'}/T_2^2\right)}{\frac{1}{kT_1} - \frac{1}{kT_2}} \qquad (4.6)$$

where E_c is the energy level of the conduction band edge.

Equation (4.6) indicates that the resolution of ΔE_T is defined by the resolution of the reading of T_1 and T_2. Practically, an error on the reading of the temperature for the occurrence of δC peak is inevitable and this is caused mainly by: 1). signal noise; 2). the uncertainty of the reading of the temperatures at which δC peaks occur; 3). the measurement errors. The third cause can be distinguished simply by comparing the data. By averaging the $\Delta C \sim t$ data, the signal noise can be minimized. The final resolution for ΔC reaches $\pm 0.0016pF$ (the fluctuation of the straight line of $\Delta C - t$ curve after the decay process), which is close to that of the capacitance

meter(0.001pF). Apparently, the key for the resolution of deep level parameters is how to properly determine the temperature at which the δC peak occurs.

Experimentally, a temperature scan can only be taken at a number of temperature points within the scan range rather than a perfect continuous scan. When the scan is at temperatures 5K apart in our experiments, for a particular rate window, a δC_{max} peak can occur at a certain temperature point T_0, as well as at two temperature points T_0 and $T_0 + 5K$ which happen to share the same δC_{max} peak if $|\delta C(T_0) - \delta C(T_0 + 5K)| \leq 0.0032pF$. The temperature for the δC_{max} peak can then be taken as T_0 for the former case or as $T_0 + 2.5K$ for the latter. Apparently, when a solo T_0 represents the temperature for the δC_{max} peak, the actual temperature for the δC_{max} peak for the particular rate window could be at anywhere within the range of $T_0 \pm 1.25K$, and $T_0 + 2.5K$ could represent those within the range of $T_0 + 2.5K \pm 1.25K$. The experimental uncertainty of the temperature for ΔC_{max} peak, δT, is then 1.25K for any of the temperature readings for ΔC_{max} peaks.

In the meantime, the resolution of the readings of ΔC of the decay curve transferred to the data files also limits the resolution of the readings of the temperature for δC_{max} peaks. If a rate window (t_1, t_2) gives a δC_{max} peak at T_0, the capacitance peak $\delta C_{max}(T_0)$ can be expressed as:

$$\delta C_{max}(T_0) = A_1 [\exp(-e_n(T_0) t_1) - \exp(-2(e_n(T_0) t_1))] \qquad (4.7)$$

when $t_2 = 2t_1$, $e_n(T_0) = \frac{\ln 2}{t_1}$ and $\delta C_{max}(T_0) = 0.25A_1$, where A_1 is approximately constant.

Theoretically, the difference between δC at temperature T_0 and that at $T_0 \pm \delta T'$, i.e, $\Delta(\delta C) = \delta C(T_0 \pm \delta T') - \delta C_{max}(T_0)$, which can be evaluated by:

$$\Delta(\delta C) = A_1\left[\exp\left(-e_n\left(T_0 \pm \delta T'\right)t_1\right) - \exp\left(-2e_n\left(T_0 \pm \delta T'\right)t_1\right)\right] - 0.25A_1 \qquad (4.8)$$

$$\text{where } e_n\left(T_0 \pm \delta T'\right) = e_n\left(T_0\right)\left\{\left[2 - \frac{\Delta E_T}{kT_0}\right]\left(\pm\frac{\delta T'}{T_0}\right) + 1\right\} \qquad (4.9)$$

As we have the uncertainty of capacitance readings $\Delta(\delta C) \approx 0.0032pF$ for capacitance measurements at all temperature points, the fluctuation of δC can cause an error $\delta T'$ on the temperature reading T_0 for the δC_{max} peak. The error $\delta T'$ can be expressed as a function of $\Delta(\delta C)/\delta C_{max}$, T_0 and the activation energy level of the deep level ΔE_T. From Eqs. (4.8) and (4.9), we can write

$$\left[2 - \frac{\Delta E_T}{kT_0}\right]\left(\pm\frac{\delta T'}{T_0}\right) = f\left(\Delta(\delta C)/\delta C_{max}\right) = const \qquad (4.10)$$

If $\Delta E_T \gg 2kT_0$, Eq. (4.10) can be approximated to:

$$\pm\delta T' \approx const\frac{kT_0^2}{\Delta E_T} \qquad (4.11)$$

Equation (4.11) strongly indicates that the $\delta C(T) \sim T$ curve appears with the δC_{max} peak occurring in the low temperature range with $\delta T' \le \delta T$. In other words, the resolution of the determination of the temperature for the δC_{max} peak calculated by Eq. (4.8) should not be larger than 1.25K, which is the experimental uncertainty of the temperature readings for δC_{max} peaks. A pre-processing procedure is developed to set the highest temperature for the occurrence of the δC_{max} peak so that the resolution of the temperature reading, $\delta T'$, equals the uncertainty of temperature reading, δT. The procedure is as follows:

I. Set a maximized rate window to get a $\delta C(T) - T$ curve with the lowest temperature T_2 for the occurrence of a chosen peak;

II. Set another rate window to give a reasonably low temperature T_1 for the peak;

III. Obtain ΔE_T from Eq. (4.4). This ΔE_T will be refined later;

IV. Substitute $\Delta(\delta C) \approx 0.0032pF$ and $\delta T' = 1.25K$ into Eqs. (4.8) and (4.9) to calculate T_0. A peak occurring at a temperature higher than T_0 cannot be read with a resolution larger than 1.25K due to the fluctuation of ΔC.

The DLTS using the Arrhenius plot to determine the activation energy of deep levels usually deals with the error processing with presuming no errors in temperature reading and the Arrhenius plotting. Our DLTS methods can determine the trap parameters by the Arrhenius plot following the δC_{max} peak processing with known errors in the Arrhenius plotting due to the uncertainty of the temperature readings.

A δC_{max} peak can occur at different temperatures with various rate windows. For example, a peak can occur at T_1 and T_2 at two corresponding rate windows, the errors on the temperature readings are δT_1, δT_2 with $\delta T_1 \le 1.25K$, $\delta T_2 \le 1.25K$. In general, for these temperature reading errors, the corresponding error for ΔE_T can be calculated from Eq.(4.6) as:

$$\begin{aligned}\delta(\Delta E_T) &= \frac{d(\Delta E_T)}{dT_1}\delta T_1 + \frac{d(\Delta E_T)}{dT_2}\delta T_2 \\ &= \left(\frac{T_2(\Delta E_T)}{T_1(T_2-T_1)} - \frac{2kT_2}{(T_2-T_1)}\right)\delta T_1 + \left(\frac{T_1(\Delta E_T)}{T_2(T_2-T_1)} - \frac{2kT_1}{(T_2-T_1)}\right)\delta T_2 \\ &\qquad \ldots\ldots \qquad (4.12)\end{aligned}$$

Because that the experimental uncertainty of the temperature reading is fixed, when we have $|\delta T_1| \le 1.25K$, $|\delta T_2| \le 1.25K$, $\delta(\Delta E_T)$ has a predictable value. For example, $T_1 > T_2$, T_2 is the lowest temperature at which δC_{max} peak occurs with maximum rate window. And T_1 is obtained by the pre-processing procedure as T_0 from Eq. (4.8). This ensures that neither δT_1 nor

δT_2 is larger than the uncertainty of temperature readings which is 1.25K. Equation (4.12) then can be used to accurately calculate the error rates of this model on the determination of energy level parameters with the data pre-processing procedure defining the temperature range (T_1, T_2). The reason that T_1 should be as close as possible to the up-bound of the temperature range defined before is that Eq. (4.12) requires the maximum $|T_1 - T_2|$ for the minimum $\delta(\Delta E_T)_{max}$.

4.4. The Effects of Minority-Carrier(hole) Generation

Figure 4.3 shows the generation and the flow of minority-carriers(holes) by diffusion. Various quiescent bias V_a's are assigned for DLTS measurements to distinguish the effects of hole generations on majority carrier emission from either bulk traps or interface states. V_a varies from very strongly to mildly reverse-bias (V_a = $-3.5V, -3.0V, -2.5V, -2.0V$) while the capture voltage V_b is kept at $-1.0V$, so that the effects of hole generation can be clearly seen in the DLTS spectra. With $t_1 = 2ms$ and $t_2 = 2t_1$, a DLTS spectrum with several peaks is shown in Fig. 4.4.

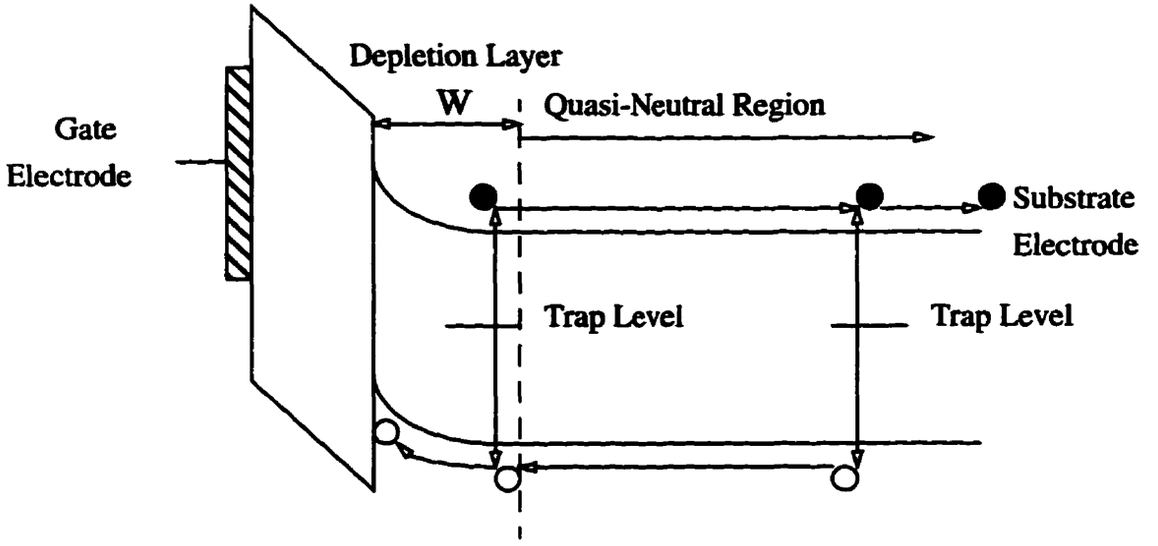


Fig. 4.3. Schematic illustration of minority-carrier flow through MOS (n-Si) by diffusion.

In Fig. 4.4, peak I is in the very low temperature region and is not affected by the bias conditions, therefore it can be excluded from the effects of minority-carrier generation. Peak J slightly decreases and shifts towards a lower temperature with increasing V_a from -2.5V to -2.0V (the change is too small to be clearly seen in Fig. 4.4), while no further change is observed when V_a changes from -2.5V to -3.0V and -3.5V. Later this peak is proved to be that due to the interface states. Peak K does not show clear change with increasing V_a from -2.0V to -3.5V. Only peak G in the high temperature region constantly increases with increasing V_a in the negative direction without shifting in temperature. Thus, peak G can be considered to be due to the hole generation. The effects of the hole generation on DLTS spectra is at high temperature region (over 250K) so that it does not affect the DLTS spectra of interface states and semiconductor bulk traps, which can be seen in Fig. 4.4 as peaks I, J and K are in the low temperature region(below 250K for the rate window at $t_1 = 2ms$, $t_2 = 4ms$).

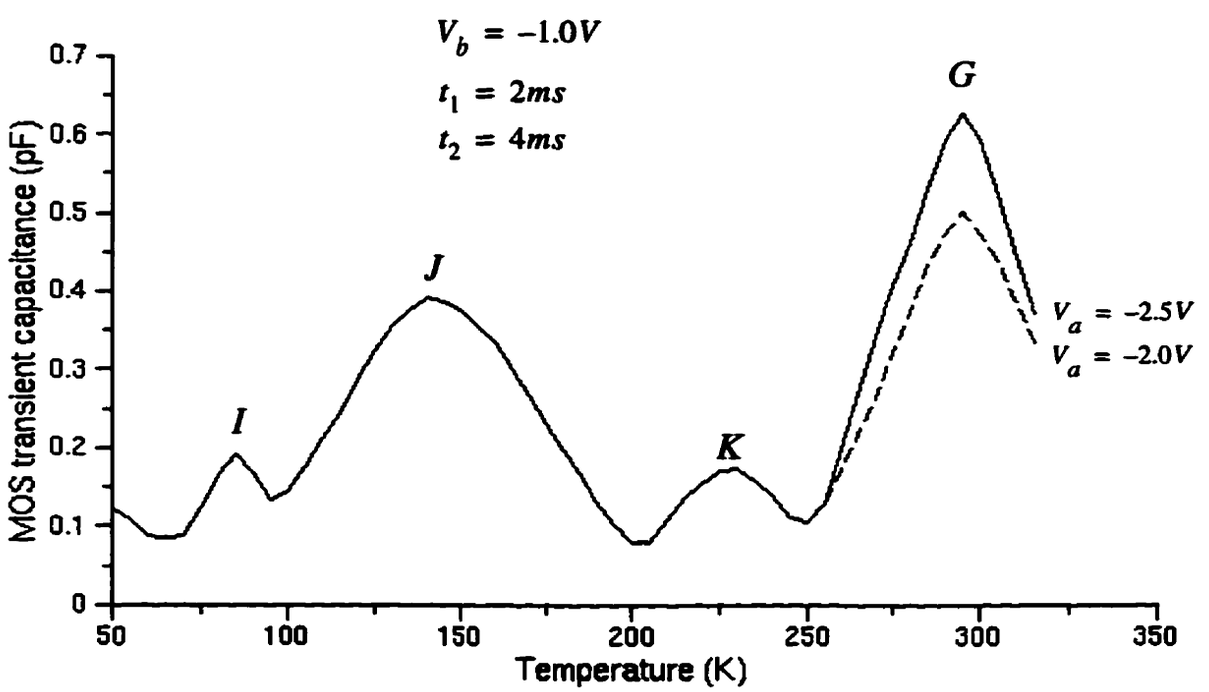


Fig. 4.4. DLTS spectrum of the MOS capacitor with an n-type Si substrate. Peak I, J, and K do not change much where peak G significantly drops when Va changes from -2.5V to -2.0V.

4.5. The Distinction Between Bulk Traps and Interface States and for the Determination of Their Parameters

I. Distinction between Bulk Traps and Interface States

As discussed in Chapter 2, the peak due to the interface states in the DLTS spectra shifts along the temperature but that due to bulk traps do not when the capture voltage changes with a constant quiescent bias (or the quiescent bias changes with a constant capture voltage). In Fig. 4.5, the three peaks in the DLTS spectra **I**, **J** and **K** are due to bulk traps and interface states, except peak **G** in Fig. 4.4, which is separated for the effects of hole generation. Peak **J** in Fig. 4.4 starts shifting when V_a changes from *-2.5V* to *-2.0V*, implying that a proper reverse bias for the distinction between bulk traps and interface states can be set in this range.

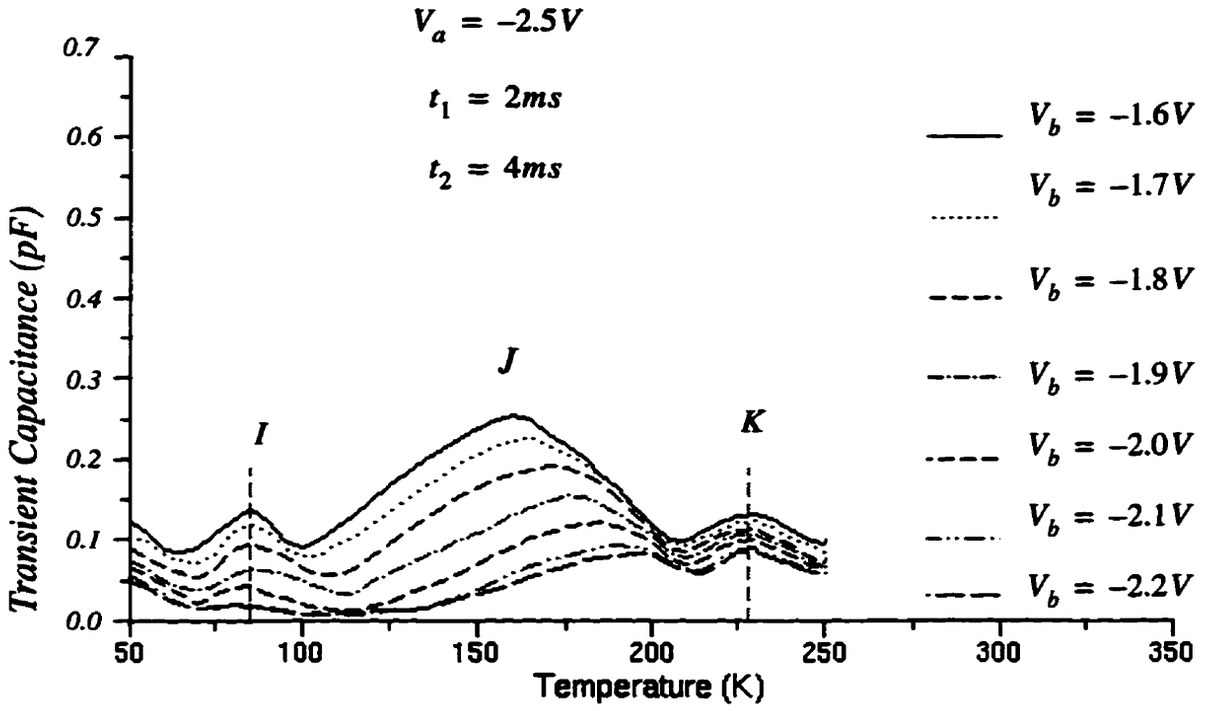


Fig. 4.5. Variation of DLTS spectra of interface states (peak **J** shifts along the temperature) and that of bulk traps (peak **I** and **K** do not shift) with capture voltage V_b.

Setting reverse quiescent bias $V_a = -2.5V$ and changing the capture pulse V_b from $-1.6V$ to $-2.2V$ with a step of $0.1V$, we obtain the DLTS spectra for the rate window at $t_1 = 2ms$, $t_2 = 4ms$, which are shown in Fig. 4.5. This figure shows clearly the DLTS spectra at various pulse voltages. The peak **J** shifts to higher temperature as V_b increases in the reverse direction due to interface states, while peaks **I** and **K** do not shift. The three peaks are then sorted as: **I** and **K** are that due to bulk traps, **J** is that due to interface states.

II. Determination of Bulk Trap Parameters

Figure 4.6 shows the Arrhenius plot of $\ln\left(e_n/T^2\right) \sim 1/kT$ for the bulk traps with the bias conditions $V_a = -2.5V$, $V_b = -1.0V$. For peak **K** in Fig. 4.5, the first rate window is set at $(t_1, t_2) = (15s, 30s)$ and the temperature at which peak K occurs is found at T = 160K. The second rate window is set at $(t_1, t_2) = (1s, 2s)$ in order to get a reasonably low temperature

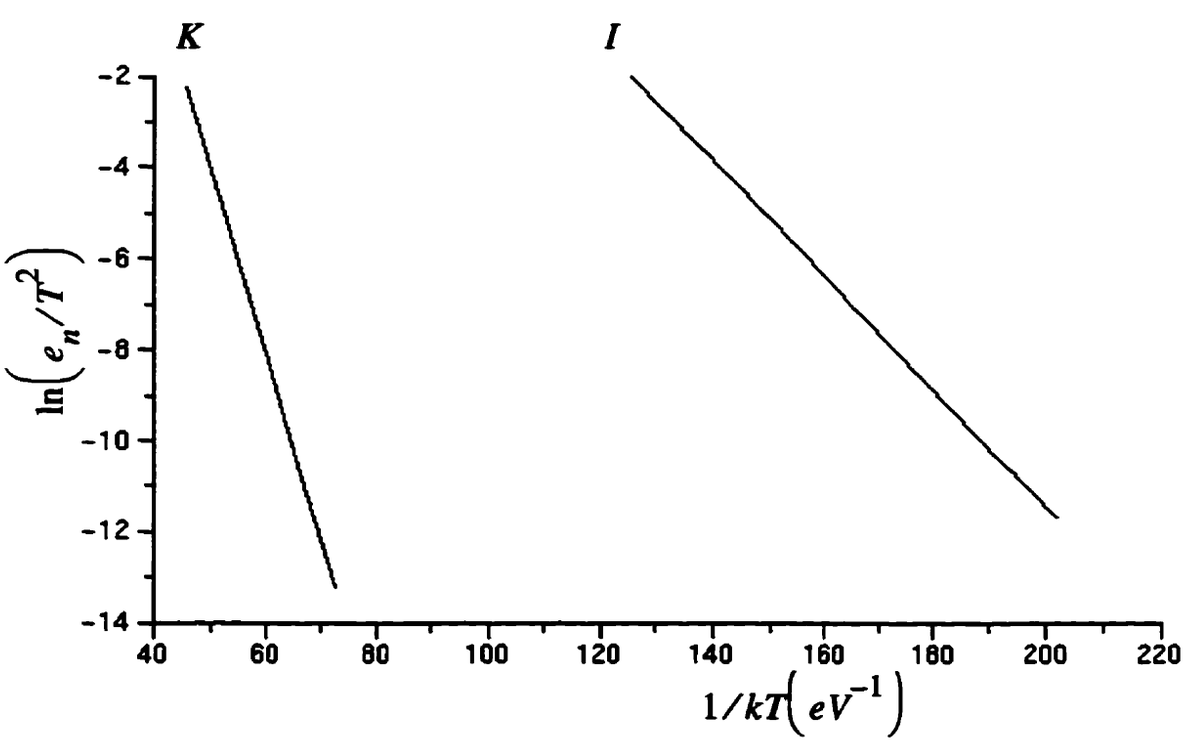


Fig. 4.6 Arrhenius plot for the determination of energy levels of bulk traps with $V_a = -2.5V$ and $V_b = -1.0V$.

for the peak to occur at T = 175K. From Eq. 4.6, ΔE_T is estimated as 0.4068 eV. By using this estimated ΔE_T in Eqs. 4.7 and 4.8 with $\Delta C_{max} = 0.1920pF$, $T_0 = 255K$ for peak K. The ΔE_T is estimated as 0.1277eV for peak I by choosing rate windows at (25s, 50s) and (1s, 2s) with corresponding temperatures $T = 57.5K, 65K$, respectively, for the occurrences of the δC_{max} peaks. With $\Delta C_{max} = 0.1728pF$, the up-bound of the temperature for peak I is calculated from Eqs. 4.8 and 4.9 as $T_0 \approx 95K$. The Arrhenius plots are therefore drawn within the temperature range (57.5K, 95K) and (160K, 255K) for peak I and K, respectively, by properly setting rate windows.

Table 4.1. The activation energy levels, the capture cross sections, the trap densities and their possible errors for bulk traps of the MOS capacitor.

	Energy levels ΔE_T $(E_T - E_c)$ (eV)	Trap density N_T (cm^{-3})	Capture cross section σ_n (cm^{-2})
Bulk trap(peak I)	$-0.4066 \pm 0.026eV$	2.30×10^{11}	1.08×10^{-14}
Bulk trap(peak K)	$-0.1268 \pm 0.018eV$	2.06×10^{11}	1.02×10^{-15}

Table 4.1 gives the energy levels, the trap densities, the capture cross sections and their possible errors in the determination of the parameters of the two bulk traps. The errors in the calculated energy levels from Eq. (4.12) are within the maximum error in temperature reading $\delta T_1 = \delta T_2 = 1.25K$. The capture cross sections are from Eq. (2.42) for which the coefficient γ for the n-type silicon is:

$$\gamma_n = \left(\upsilon / T^{1/2}\right)\left(N_c / T^{3/2}\right) = 1.07 \times 10^{21}\left(cm^{-2} s^{-1} K^{-2}\right) \qquad (4.12)$$

The trap densities are calculated by Eqs. (2.40), (2.41) and (2.43), which can also be expressed as:

$$N_T = -4\frac{\varepsilon_s C_{ox} N_d}{C^3}\Delta C_{max} \tag{4.13}$$

III. Determination of Interface State Parameters

The energy distribution and capture cross section of interface states are determined by setting $V_a = -2.2V$ and changing V_b from $-1.0V \rightarrow -2.0V$ by a step of 0.2V. For each of the bias conditions, the activation energy of interface states and capture cross section are determined using the

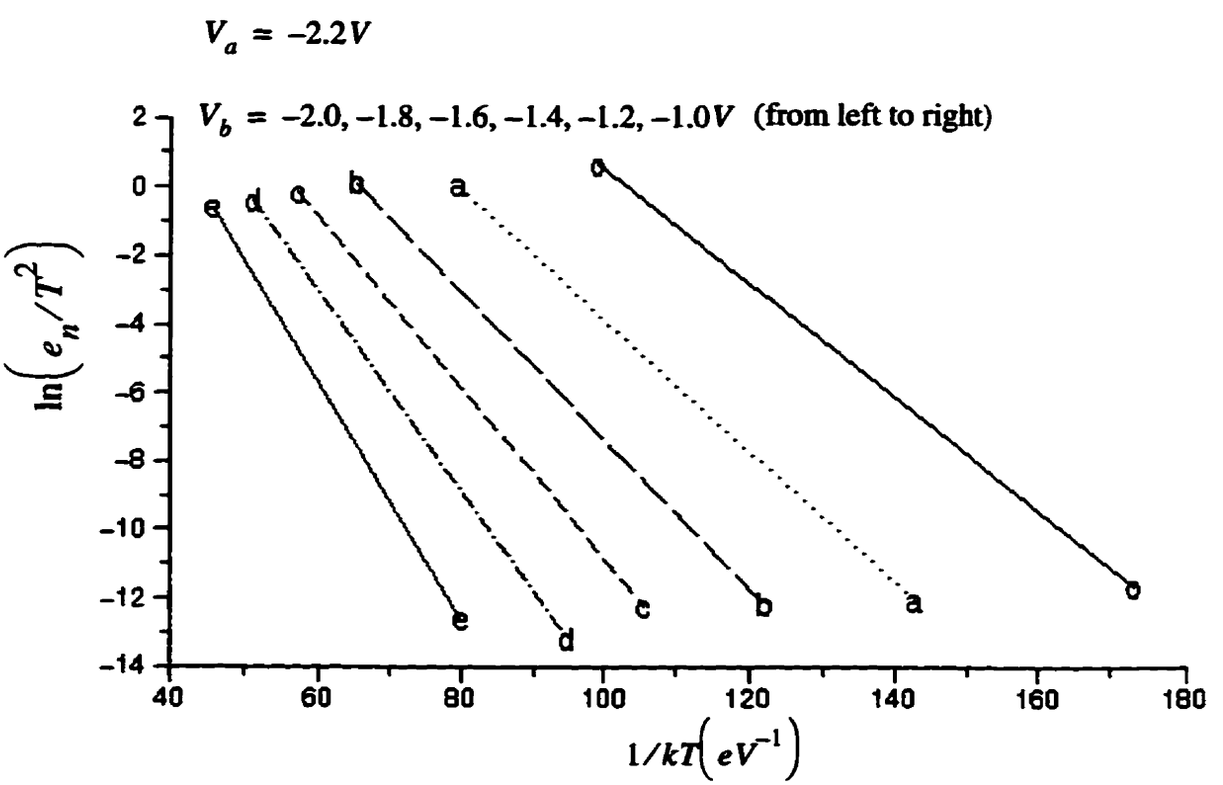


Fig. 4.7. Arrhenius plot for interface states under various bias conditions.

same methods used for the determination of the bulk trap parameters. When $V_b > -1.0V$, peak J and peak I interfere each other so that the temperatures and the heights ΔC_{max}'s for the peaks can not accurately be read. When $V_b = -2.1V$, the ΔC_{max} is too small to be accurately measured for the Arrhenius plotting.

Figure 4.7 is the Arrhenius plots at various bias conditions. When V_a is kept constant , the larger the V_b in the reverse direction, the higher the emission rate of electrons from deeper interface states. Therefore, the various pulse conditions can give a series of Arrhenius plots for the determination of interface state parameters at different energy levels.

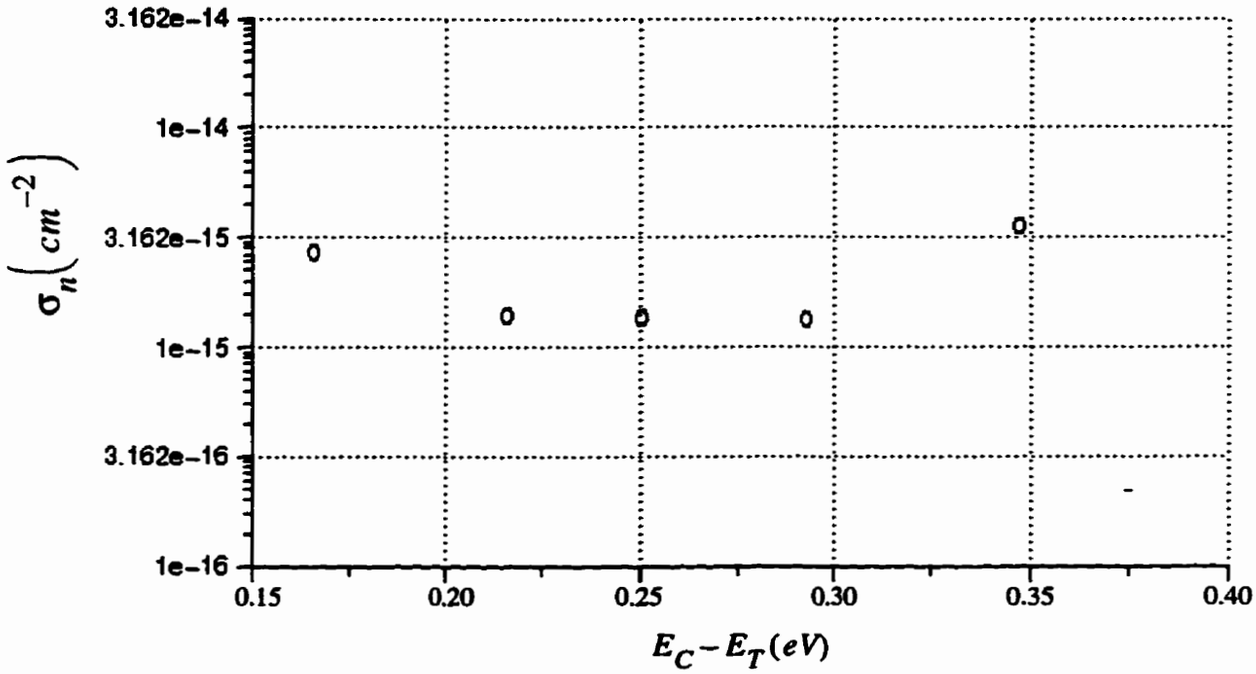


Fig. 4.8. The energy distribution of capture cross section of the interface states.

Figure 4.8 shows the energy distribution of the capture cross section indicating that the capture cross section does not change much while the activation energy of the interface states increases from $\sim -0.1659eV$ to $\sim -0.3474eV$.

Table 4.2. The parameters of interface states.

Capture voltage V_b (V)	activation Energy ΔE_T (eV)	Capture cross section σ_n (cm^{-2})	Interface density D_{it} ($eV^{-1}cm^{-2}$)
-1.0 V	-0.1659 ± 0.014	2.774×10^{-15}	1.85×10^{13}
-1.2 V	-0.1913 ± 0.015	2.569×10^{-15}	1.31×10^{13}
-1.4 V	-0.2162 ± 0.014	1.412×10^{-15}	5.13×10^{12}
-1.6 V	-0.2508 ± 0.014	1.382×10^{-15}	2.65×10^{12}
-1.8 V	-0.2928 ± 0.015	1.359×10^{-15}	1.78×10^{12}
-2.0 V	-0.3474 ± 0.016	3.661×10^{-15}	1.23×10^{12}

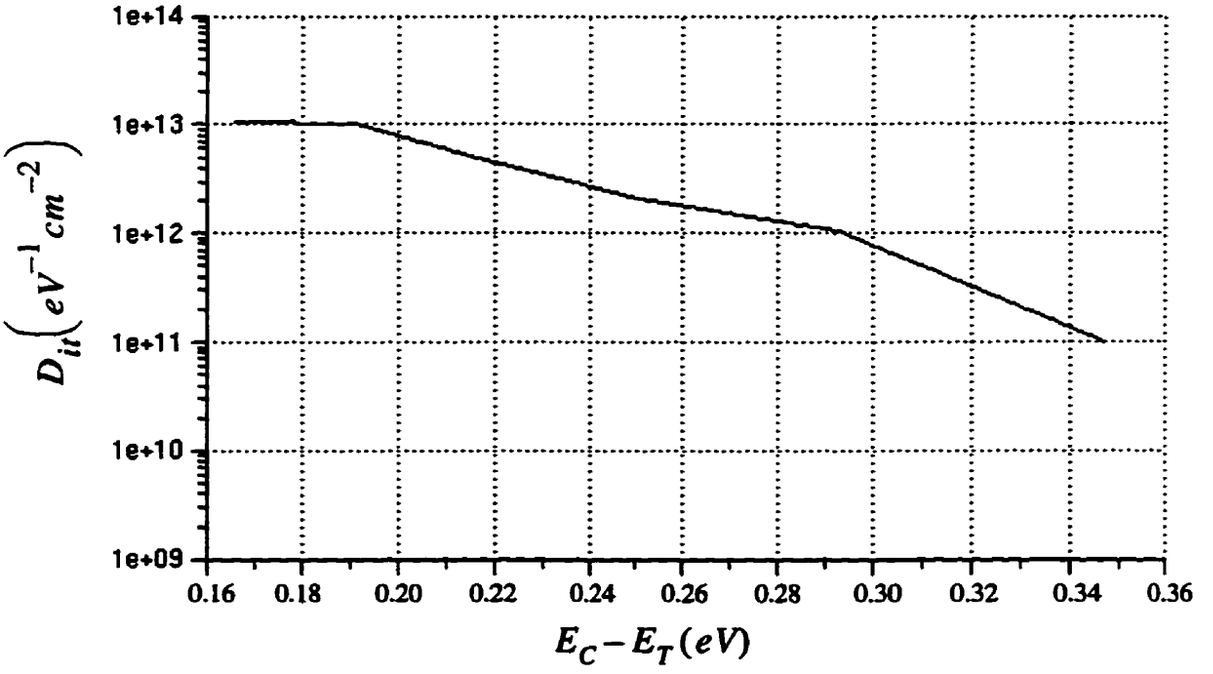


Fig. 4.9. The energy distribution of interface state density measured from the conduction band edge.

Table 4.2 gives the parameters of the interface states. The energy levels are in the range of about $-0.1659eV \sim -0.3474eV$. With Eq. (2.47) and the $\Delta C_{max}(T) \sim T$ relations at the rate window $(t_1, t_2) = (2ms, 4ms)$ (randomly picked) for all the six pulse heights, we can obtain the energy distribution of interface density $D_{it}(E_T)$ which is shown in Fig. 4.9.

However, the $D_{it} \sim E_T$ distribution can be obtained by the high frequency capacitance~voltage method, but this method has the disadvantage that only the $D_{it}(E_T)$ for E_T close to the midgap of forbidden zone can be determined. For similar MOS samples, Chau[71] has reported that $D_{it} \sim 6.0\times10^{11} cm^{-2} eV^{-1}$ at around the midgap. Our result determined by the DLTS method is $D_{it} = 1.23\times10^{12} cm^{-2} eV^{-1}$ at $0.3474eV$ below the conduction band edge, which is comparable to Chau's result. It should be noted that Eq. (4.40) indicates that $D_{it}(E_T)$ tends to decrease with increasing $\Delta E_T = E_c - E_T$.

CHAPTER 5
CONCLUSIONS

A DLTS system has been designed and built for the measurements of capacitance transients with the aim of determining the trap parameters in semiconductor devices. This system is reliable, fast, automated, flexible and easy in handling data acquisition. Analytical methods have also been developed for the determination of the trap parameters for p-n junctions and MOS devices.

Our new data collecting techniques have one major advantage, that is, we can have as many data points as needed in one temperature scan so that the choice and the number of rate windows are unlimited for the analysis of an MOS device. The parameter evaluation through numerical methods can be applied to the analysis of a p-n junction.

The density of interface states of an MOS system can be determined by the measurement of the high-frequency capacitance-voltage characteristics--a conventional method. But this method can determine only the density of the interface states close to the midgap in the forbidden zone. Our method is far better than the conventional method, we can determine the energy distribution of the density of interface states as well as trap densities in the semiconductor bulk by only one temperature scan.

REFERENCES

1. K. C. Kao and W. Hwang, *Electrical Transport in Solids*, Pergamon Press, 1981.
2. A. G. Milnes, *Deep Impurities in Semiconductors*, Wiley-Interscience, New York, 1973.
3. S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. Wiley, New York, 1981.
4. R. Williams, "*Determination of Deep Centres in Conducting Gallium Arsenide*", J. Applied Physics, V37, 3723-3731, July 1966.
5. C. T. Sah, L. forbes, L. I. Tosier, and A. F. Tasach, Jr., "*Thermal and Optical Emission and Capture Rates and Cross Sections of Electrons and Holes at Imperfection Centres in Semiconductors from Photo and Dark Junction Current and Capacitance Experiments", Solid-State Elec-tronics. V13, 759-788, June 1970.*
6. L. D. Yau and C. T. Sah, "*Measurement of Trapped-Minority-Carrier Thermal Emission Rates from Au, Ag, and Co Traps in Silicon*", Appl. Phys. Lett. V21,157-158, Aug. 1972.
7. C. T. Sah and J. W. Walker, "*Thermally Stimulated Capacitance for Shallow Majority-Carrier Traps in the Edge Region of Semiconductor Junctions", Appl. Phys. Lett. V22, 384-385, Nov.1973.*
8. W. W. Chen and C. T. Sah, "*Defect Centers in Boron-Implanted Silicon*", J. Appl. Phys. V42, 4768-4773.
9. M. Jaros, *Deep Levels in Semiconductors*, A. Hilger, Bristol, 1982.
10. E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley, New York, 1982.
11. D. K. Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, Inc. New York, 1990.
12. R. R. Senechal and J. Basinske, "*Transient Phenomena in the Capacitance of GaAs Schottky Barrier Diodes*", J. Appl. Phys. V39, 4581-4589, Aug. 1968
13. C. T. Sah, "*Bulk and Interface Imperfections in Semiconductors*", Solid-state Electron. V19, 975-990, Dec. 1976.
14. D. V. Lang, "*Deep-Level Transient Spectroscopy: A New Method to Characterize Traps in*

Semiconductors", J. Appl. Phys. V45, 3023-3032, July 1974.

15. D. V. Lang, "*Fast Capacitance Transient Apparatus: Application to ZnO and O Centers in Gap of p-n Junctions*", J. Appl. Phys. V45, 3014-3022, July 1974.
16. G. L. Miller, D. V. Lang and L. C. Kimerling, "*Capacitance Transient Spectros-copy*", Annual Review of Material Science, Annual Reviews, Palo Alto, CA, V7,377-448, 1977.
17. D. V. Lang, "*Space-Charge Spectroscopy in Semiconductors*", in Topics in Applied Physics: Thermally Stimulated Relaxation in Solids(P. Braunlich, ed.), 37, pp. 93-133,Springer, Berlin, 1979.
18. F. W. Sexton and W. D. Brown, "*A Low-Cost Microprocessor-Based Deep-Level Transient Spectroscopy(DLTS) System*", IEEE Tran. on I. & M. IM-30, No. 3, 186-193, Sept. 1981.
19. H. Lefevre and M. Schulz, "*Double Correlation Technique(DDLTS) for the Analysis of Deep Level Profiles in Semiconductors*", Appl. Phys. V12, 45-53, Jan. 1977.
20. K. Kosai, "*External Generation of Gate Delays in a Boxcar Integrator--Application to Deep Level Transient Spectroscopy*", Rev. Sci. Instrum. V53, 210-213, Feb. 1982.
21. L. C. Kimerling, "*New Developments in Defect Studies in Semiconductors*", IEEE Trans. Nucl. Sci. NS-23, 1497-1505, Dec. 1976.
22. G. L. Miller, J. V. Ramirez and D. A. H. Robinson, "*A Correlation Method for Semiconductor Transient Signal Measurements*", J. Appl. Phys. V46, 2638-2644, June 1975.
23. D. S. Day, M. Y. Tsai, B. G. Streetman and D. V. Lang, "*Deep-Level Transient Spectroscopy: System Effects and Data Analysis*", J. Appl. Phys. V50, 5093-5098, Aug. 1979.
24. M. D. Miller and D. R. Patterson, "*Transient Capacitance Deep Level Spectrometry Instrumentation*", Rev. Sci. Instrum. V48, 237-239, March 1977.
25. Y. Tokuda, N. Shimizu and A. Usami, "*Studies of Neutron-Produced Defects in Silicon by Deep-Level Transient spectroscopy*", Japan. J. Appl. Phys. V18, 309-315, Feb. 1979.
26. A. Rogatgi, J. R. Davis, R. H Hopkins and P. G. Mcmullin, "*A Study of Grown-in Impurities in Silicon by Deep-Level Transient Spectroscopy*", Solid-State Electron. V26, 1039-1051, Nov. 1983.
27. M. S. Hodgart, "*Optimum correlation Method for Measurement of Noisy Transients in Solid-State Physics Experiments*", Electron. Lett. V14, 388-390, June, 1978.
28. C. R. Crowell and S. Alipanahi, "*Transient Distortion and n-th Order Filtering in Deep Level Transient Spectroscopy(D^nLTS)*", Solid-State Electron. V24, 25-36, Jan. 1981.

29. E. E. Haller, P. P. Li, G. S. Hubbard and W. L. Hansen, "*Deep Level Transient Spectroscopy of High Purity Germanium Diodes/Detectors*", IEEE Trans. Nucl. Sci. NS-26, 265-270, Feb. 1979.

30. K. Dmowski and Z. Pioro, "*Noise Properties of Analog Correlators with Exponentially Weighted Average*", Rev. Sci. Instrum. V58, 2185-2191, Nov. 1987.

31. K. Dmowski and A. Jakubowski, "*Sensitivity Analysis of Bulk Traps Detection in Analog Deep-Level Transient Spectroscopy Measurement Systems with Exponentially Weighted Average*", Rev. Sci. Instrum. V60(1), 106-112, Jan. 1989.

32. G. Goto, S. Yanagisawa, O. Wada and H. Tadanashi, "*Determination of Deep-Level Energy and Density Profiles in Inhomogeneous Semiconductors*", Appl. Phys. Lett. V23, 150-151, Aug. 1973.

33. N. M. Johnson, "*Measurement of Semiconductor-Insulator Interface States by Constant-Capacitance, Deep-Level Transient Spectroscopy*", J. Vac. Sci. Technol. V21, 303-314, July /Aug. 1982.

34. G. L. Miller, "*A Feedback Method for Investigating Carrier Distributions in Semiconductors*", IEEE Trans. Electron Dev. ED-19, 1103-1108, Oct. 1972.

35. J-J. Shiau, A. L. Fahrenbruch and R. H. Bube, "*A Method to Improve the Speed* and Sensitivity

of Constant-Capacitance Voltage Transient Measurements", Solid-State Electron. V30, 513-518, May 1987.

36. M. F. Li and C. T. Sah, "*A New Method for the Determination of Dopant and Trap Concentration Profiles in Semiconductors*", IEEE Trans. Electron Dev. ED-29, 306-315, Feb. 1982.

37. N. M. Johnson, D. F. Bartelink, R. B. Gold and J. F. Gibbons, "*Constant-Capacitance DLTS Measurement of Defect-Density Profiles in Semiconductors*", J. Appl. Phys. V50, 4828-4833, July 1979.

38. E. E. Wagner, D. Hiller and D. E. Mars, "*Fast Digital Apparatus for Capacitance Transient Analysis*", Rev. Sci. Instrum. V51, 1205-1211, Sept. 1980.

39. M. D. Jack, R. C. Pack and J. Henriksen, "*A Computer-Controlled Deep-Level Transient Spectroscopy System for Semiconductor Process control*", IEEE Trans. Electron Dev. ED-27,

2226-2231, Dec. 1980.

40. E. K. Evangelou, A. D. Hovevas, G. E. Giakoumakis and N. G. Alexandropoulos, "*A Microcomputer Based Deep Level Transient Spectroscopy System*", Solid-State Comm. V80, 247 -249, 1991.

41. K. Holzlein, G. Pensl, M. Schulz and P. Stolz, "*Fast Computer-Controlled Deep* Level Transient Spectroscopy System for Versatile Applications in Semiconduc*tors*", Rev. Sci. Instrum. V57, 1373-1377, July 1986.

42. P. D. Kirchner, W. J. Schaff, G. N. Maracas, L. F. Eastman, T. I. Chappell and C. M. Ranson, "*The Analysis of Exponential and Nonexponential Transients in Deep-Level Transient Spectroscopy*", J. Appl. Phys. V52, 6462-6470, Nov. 1981.

43. M. Okuyama, H. Takakura and Y. Hamakawa, "*Fourier-Transformation Analysis of Deep Level Transient Signals in Semiconductors*", Solid-State Electron. V26, 689-694, July 1983.

44. A. Le Bloa, Dang Tran Quan and Z. Guennouni, "*FETDLTS: A Novel Isothermal DLTS Method Using Fourier Transforms*", IEE Proceedings A. Sci. Meas. & Tech., V4, No.3, 325 -336, Mar 1993

45. K. Ikossi-Anastasiou and K. P. Roenker, "*Refinements in the Method of Moments for Analysis of Multiexponential Capacitance Transients in Deep-Level Transient Spectroscopy", J. Appl. Phys. V61, 182-190, Jan. 1987.*

46. R. D. Dyson and I. Isenberg, "*Analysis of Exponential Curves by A Method of* Moments, With Special Attention to Sedimentation Equilibrium and Fluores*cence Decay*", Biochem. V10, 3233-3241, 1971.

47. I. Isenberg, R. D. Dyson and R. Hanson, "*Studies of The Analysis of Fluores cence Decay Data by the Method of Moments*", Biophys. J., V13, 1090-1115, 1973.

48. L. W. Wang and C. H. Wu, "*A Novel Technique of Analysing Multiexponential Transients for DLTS Spectra*", Solid-State Electron. V35, 1771-1777, 1992.

49. K. Dmowske, K. Bethge and Ch. Maurer, "*A Multipoint Correlation Method for* Bulk Trap and Interface State Measurements in MOS Structures from Capaci*tance, Voltage, and Current Transients*", Rev. Sci. Instrum. V62, 1955-1963, 1991.

50. J. E. Stannard, H. M. Day, M. L. Bark and S. H. Lee, "*Spectroscopic Line Fit ting to DLTS Data*", Solid-State Electron. V24, 1009-1013, Nov. 1981.

51. F. R. Shapiro, S. D. Senturia and D. Adler, "*The Use of Linear Predictive Modeling for the*

Analysis of Transients from Experiments on Semiconductor Defects", J. Appl. Phys. 55, 3453-3459, May 1984.

52. M. Henini, B. Tuck and C. J. Paul, "*A Microcomputer-Based Deep Level Transient Spectroscopy(DLTS) System*", J. Phys. E: Sci. Instrum. V18, 926-929, Nov. 1985.
53. R. Langfeld, "*A New Method of Analysis of DLTS-Spectra*", Appl. Phys. A44, 107-110, Oct. 1987.
54. B. D. Nener, S. T. Lai, L. Faraone and A. G. Nassibian, "*Parameter Evaluation in Automated Digital Deep-level Transient Spectroscopy(DLTS)*", IEEE Trans. V42, 913-920, Oct. 1993.
55. K. L. Wang and A. O. Evwaraye, "*Determination of Interface and Bulk Trap States of IGFET's*

    Using Deep-Level Transient Spectroscopy", J. Appl. Phys. V47, 4574-4577, Oct. 1976.
56. K. L. Wang, "*A Determination of Interface State Energy during the Capture of Electrons and Holes Using DLTS*", IEEE Trans. Electron Dev. ED-26, 819-821, May 1979.
57. K. L. Wang, "*MOS Interface-State Density Measurements Using Transient Capacitance Spectroscopy*", IEEE Trans. Electron Dev. ED-27, 2231-2239, Dec. 1980.
58. M. Schulz and N. M. Johnson, "*Transient Capacitance Measurements of Hole Emission from Interface States in MOS Structures*", Appl. Phys. Lett. V31, 622-625, Nov. 1977.
59. M. Schulz and N. M. Johnson, "*Evidence for Multiphonon Emission from Interface States in MOS Structures*", Solid-State Comm. V25, 481-484, Feb. 1978.
60. K. Yamasaki, M. Yoshida and T. Sugano, "*Deep Level Transient Spectroscopy of Bulk Traps and Interface States in Si MOS Diodes*", Japan. J. Appl. Phys. V18, 113-122, Jan. 1979.
61. J. L. Zhao, *Y. Gao, X. Y. Liu, K. Dou, S. H. Huang, J. Q. Yu, J. C. Liang and H.* K. Gao, "Studies on Deep Levels in GaAs Epilayers Grown on Si by Metal-Organic Chemical Vapour Deposition, Part III: 0.78 and 0.84eV Photoluminesc*ence Emissions*", J. Materials Sci. Lett. V14, July 1995.
62. A. Malinin, H. Tomozawa, T. Hashizume and H. Hasegawa, "*Characterization* of Deep Levels

    in Si-doped In_x-Al_1-xAs Layers Grown by Molecular Beam Epi*taxy*", Japan. J. Appl. Phys. V34, Feb. 1995.
63. T. Torchinskaya, V. I. Kooshnirenko, L. V. Shcherbina and C. J. Miner, "*Characterization of Deep-Level Defects and Their Connection with the Performance of In_x-Al_1-xAs p-i-n*

Photodiodes", Proceedings SPIE. V2336, 233-236, 1994.

64. H. J. Song, S. H. Yun and W. T. Kim, "*Deep Levels in $TlGaS_2$ Single Crystal*", Solid State Comm. V94, 225-229, Apr. 1995.
65. P. Kaminski, G. Gawlik and R. Kozlowski, "*Deep Levels in Rapid Thermal Annealed GaAs*", Materials Sci. Eng. B28, 439-443, Dec. 1994.
66. E. O. Sveinbjornsson and O. Engstrom, "*Hydrogen-Gold-Related Deep Levels in Crystalline Silicon*", Materials Sci. Forum V143-4, 821-826, 1994.
67. Y. Tokuda, I. Katoh, H. Ohshima and T. Hattori, "*Observation of Hydrogen in Commercial Czochralski-Grown Silicon Wafers*", Semi. Sci. Tech. V9, 1733-1735, Sept. 1994.
68. R. J. Walters, R. L. Statler and G. P. Summers, "*Temperature Coefficients and Radiation Induced DLTS Spectra of MOCVD Grown n+p InP Solar Cells*", Eleventh Space Powersd Research & Tech. Conf., NASA Lewis Research Center, Cleveland, Ohio, May 7-9, 1991.
69. R. J. Walters and G. P. Summers, "*Deep Level Transient Spectroscopy Study of Proton Irradiated p-Type InP*", J. Appl. Phys., 69(9), 6488-6494, May 1991,
70. R. J. Walters, C. J. Keavney, S. R. Messenger, G. P. Summers and E. A. Burke, "*The Effect of Dopant Density on the Radiation Resistance of MOCVD InP Solar Cells*", 22nd IEEE Photovaltaic Space Conf., Las Vegas, NV, Oct. 1991
71. T. T. Chau, PH. D Thesis, "*ECR Microwave Plasma Processing Techniques and Effects of Deposition Parameters on Properties of MOS Systems*", June, 1995.
72. S. D. Brotherton and J. Bicknell, "*Measurement of Minority Carrier Capture Cross Sections and Application to Gold and Platinum in Silicon*", J. Appl. Phys. 53, 1543-1553, March 1982.
73. B. Hamilton, A. R. Peaker, and D. R. Wight, "*Deep-State-Controlled Minority- Carrier Lifetime in n-Type Gallium Phosphide*", J. Appl. Phys. 50, 6373-6385.

Appendix

Appendix I An Example of the Control Program

```
#include<iostream.h>
(#include<time.h>
#include "c:\\hpib\\cfunc.h"
#include "c:\\hpib\\chpib.h
#include <stdio.h>
#define isc       7L
#define scope     701
#define srqline   1
#define cmeter    718
// void initialize()
void cmetersetup();
void readout();
int error;
class timer
{
double start,end;
public:
 timer\(\); //construtor
 ~timer\(\); //destructo
};
   timer::timer()
{
 start=(double) clock();
//  cout<<"start= "<<start<<"\n";
```

```
  timer::~timer()
{
  end=(double) clock();
  cout<<"end="<<end<<"\\n";
  cout<<"elapsed time="<<(end-start)/CLK_TCK <<"\\n";
 }
main()
{
long i;
long j;
char    *codes
//void  readout();
 timer ob;
for (j=1;j<=4;j++)
{
 codes="DAT:SOURCE CH2";
 error=IOOUTPUTS(scope,codes,14);
 codes="DAT:ENC ASCI";
 error=IOOUTPUTS(scope,codes,12)
if (j==1)
{
 codes="BI 0 VO BO";
 error=IOOUTPUTS(cmeter,codes,10);
//initialize ()  ;
//cmetersetup ();
//trigger ();
}
//  cout<<i;
 if (j==2) {
  codes= "WT BI 10 VO TM"
//    if (i==2) {  codes="BI 15 VO";
```

```
    error = IOOUTPUTS(cmeter,codes,14);}
    if (j==3) {
    codes="TR 0 VO IM TM";
    error=IOOUTPUTS(cmeter,codes,13);}
    codes="DAT:STAR 1";
    error=IOOUTPUTS(scope,codes,10);
    codes="DAT:STOP 1000"
    error=IOOUTPUTS(scope,codes,13);
    codes="CURV?"
    error=IOOUTPUTS(scope,codes,5);
    readout();
  }
}
 void  readout()
{
float  readings[1000]
int   i;
int   numvalues;
numvalues=1000;
error=IOENTERA(scope,readings,&numvalues);
printf("\\n the readings are:\\n");
 for (i=0; i<numvalues; i++)
 {
  printf("%f \\n", readings[i]/256)
  }
```