Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs

by

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Abstract

The recent introduction of a new converter topology, the modular multilevel converter (MMC) is a major step forward in voltage sourced converter (VSC) technology for high voltage, high power applications. To obtain a multilevel ac output waveform, a large number of semiconductor switches has to be used in the converter. The number of switches in the MMC for HVDC transmission is typically two orders of magnitudes larger than that in a two or three level VSC used in earlier generation. This large device count creates a computational challenge for electromagnetic transients (EMT) simulation programs, as it significantly increases the simulation time. The purpose of this research is to investigate whether the simulation can be speeded up.

This research develops an efficient, time-varying Thévenin's equivalent model for the MMC converter based on partitioning the system’s admittance matrix. EMT simulation results show that the proposed equivalent model can drastically reduce the computational time without loss of accuracy. The use of the proposed equivalent method is demonstrated by simulating a point to point MMC based HVDC transmission system successfully with more than 100 levels. This approach enables what was hitherto not practical; the modeling of large MMC based HVDC systems on personal computers.

With the assumption of ideal switch operation and using an equivalent average capacitor value based approach, an average valued model of MMC is also proposed in this thesis. The average model can be accurately used in most of the system level studies. The control algorithms and other modeling aspects of MMC applications are also presented in this thesis.

One of the advantages of multilevel converters is the low operating losses as the smaller switching frequency of each individual power electronics switch and the low voltage step change during each switching. Using a recently developed, time domain simulation approach, the operating losses of the MMC converter are estimated in this thesis. When comparing the MMC operating losses against the losses of two-level VSC, the power loss for the two-level VSC is found to be significantly higher than the power loss of the MMC.

Acknowledgments

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List of Acronyms

2S-DIRK	Two Stage–Diagonally Implicit Runge–Kutta
AC	Alternating Current
CPU	Central Processing Unit
DC	Direct Current
EMF	Electromotive Force
EMT	Electromagnetic Transients
GCT	Gate Commutated Thyristor
GTO	Gate Turnoff Thyristor
HF	High Frequency
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
LCC	Line Commutated Converter
MMC	Modular Multilevel Converter
PCC	Point of Common Coupling
PI	Proportional–Integral
PLL	Phase Locked Loop
PWM	Pulse–Width Modulation
RMS	Root Mean Square

SPWM	Sinusoidal Pulse–Width Modulation
STATCOM	Static Synchronous Compensator
THD	Total Harmonic Distortion
VSC	Voltage Sourced Converter

List of Principle Symbols

C, C_{pu}	Sub-module capacitance and per-unitized capacitance
C_{eff}	Equivalent capacitance of 'ON' state sub-modules
D_n	Individual harmonic distortion
G	Conductance matrix
g_C	Equivalent conductance of sub-module capacitor
g_T, g_D	Equivalent conductance of IGBT and diode
I_{ceq}	Magnitude of equivalent current source of sub-module capacitor
$\underline{J}(t)$	Source current vector
L_f, C_f	Inductance and capacitance of second harmonic current
m	Modulation index
N	Number of sub-modules in multi-valve
N_u, N_l	Number of 'ON' state sub-modules in upper and lower multi-valves
P_{ac1}, Q_{ac1}	Real power and reactive power at bus1
P_c, Q_c	Active power and reactive power exchanged between ac system and converter
P_{on}, P_{off}	'ON' state power losses and 'OFF' state power losses
R_{c0}	Equivalent resistance of sub-module capacitor
R_{ceq}	Equivalent resistance of sub-module capacitor and power loss resistor

R_p, g_P	Equivalent resistance and conductance for power loss of sub-module capacitor
t	Time
U_{dc}, I_{dc}	Pole to pole dc voltage and dc line current
$\underline{V}(t)$, $\underline{I}(t)$	Node voltage vector and branch current vector
V_{ac}, I_{ac}	AC bus voltage and ac line current
V_c, I_c	Sub-module capacitor voltage and capacitor current
V_{c0eq}	Magnitude of equivalent voltage source of sub-module capacitor
V_{ceq}	Magnitude of equivalent voltage source of sub-module capacitor and power loss resistor
V_{fb}, I_{fb}	Full-bridge sub-module voltage and current
V_{hb}, I_{hb}	Half-bridge sub-module voltage and current
V_{mv}, I_{mv}	Multi-valve voltage and current
V_{mveq}, R_{mveq}	Thévenin equivalent voltage and resistance of multi-valve
V_{out}, I_{out}	Converter output voltage and current
V_{sm}, I_{sm}	Sub-module voltage and current
X_l	Reactance between converter ac terminal and ac bus
Y	Admittance matrix
δ	Phase angle of converter output voltage with respect to ac bus voltage
ΔT	Time-step
ΔV	Voltage difference between converter ac terminal and ac bus
ω	Angular frequency

Introduction

1.1 Background

Today, a greater focus is directed at how electricity is generated and distributed in an environmental friendly manner with high reliability and efficiency. Traditionally, ac (alternating current) based transmission schemes were used for transmitting power from (remote) generating stations to the load centers. However for long transmission, ac based schemes introduce numerous challenges due to the inherent limitations in ac technology such as high transmission losses, low transmission capacity over long distances, and undesirable power flow scenarios with a direct connection of two ac systems [1]. These technical and economical limitations of the ac technology have led to the development of high voltage direct current (HVDC) transmission as a supplement to ac transmission [2].

In 1954, the world's first commercial HVDC link based on mercury arc converters began operation between the Swedish mainland and the island of Gotland. This was followed by many small and larger mercury arc schemes around the world. Around 20 years later, in the early 1970s, thyristor semiconductors started to replace the mercury arc valves in converters [3].

An HVDC system based on thyristor valves, also referred to as a line commutated converter (LCC) is an efficient and economical way of transmitting large amounts of electrical power over long distances using overhead transmission lines or underground/submarine cables [4], [5]. The LCC based HVDC schemes can be used to interconnect two or more asynchronous power systems, where traditional ac connections cannot be used [6].

In recent years, voltage sourced converter (VSC) based HVDC technology has made significant progress with the development and advancement of power semiconductor devices, such as insulated gate bipolar transistors (IGBTs), gate turnoff thyristors (GTOs), and gate commutated thyristors (GCTs) [3]. Earlier versions of VSCs included converters that produced two- or three- level stepped waveforms. More recently, multilevel topologies that can produce multiple levels have become possible and are referred to as modular multilevel converters (MMC) [7].

The conventional, LCC requires an external network to extinguish the currents in its valves. In contrast, the VSC can be given an electric gate pulse to turn ‘OFF’ its valves. The VSC based HVDC systems thus have many advantages over the LCC, such as the ability to operate into weak or dead networks without reactive power support, independent control of active and reactive power, less filtering requirement, simpler implementation of multi-terminal configurations, and black start capability. The VSC based HVDC systems are currently available for small to medium scale power transmission applications [8]-[11].

The multilevel converter generates a multi-step ac waveform with a very small increment at each voltage step and the new multilevel topology, MMC has been proposed and applied for HVDC applications [7], [12]. The block diagram of a single phase MMC is shown in Figure 1-1.

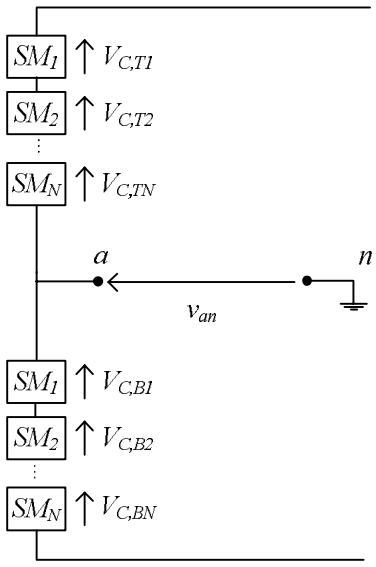


Figure 1-1: Block diagrams of single-phase MMC

The MMC uses a stack of identical modules, each corresponding to one step in the resulting multilevel ac waveform at the converter terminals as shown in Figure 1-2. The topology is easily adaptable to any voltage level, as the number of modules can be adjusted in proportion to the selected dc voltage. The resulting waveform has a very small harmonic content and has reduced transient voltage stresses, hence lower high frequency (HF) noise. The switching frequency of each individual power electronic switch is smaller than that of a two-level converter and the voltage step at each level is also smaller. These factors contribute to reduce the switching loss.

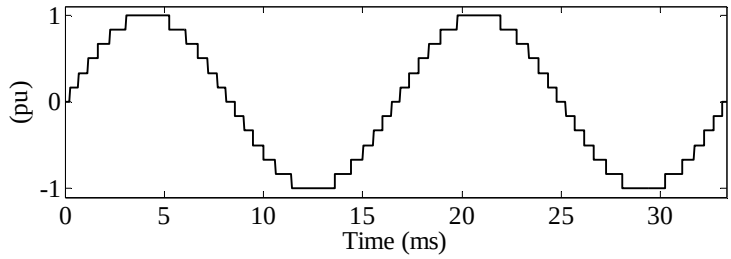


Figure 1-2: MMC output waveform for 24 sub-modules per phase

1.2 Problem Definition

A large number of power electronics switch modules (sub-modules) is used in MMC operation to reduce the voltage stress on each switching element and to generate very small sized steps in the output voltage waveform. Therefore, the number of semiconductor switches in a MMC based HVDC transmission system is typically two orders of magnitude larger than that in a two- or three- level VSC. The large number of switching elements in the MMC introduces a challenge for modeling the converter in electromagnetic transients (EMT) simulation programs. In EMT programs, every operation of a switch is represented as an impedance change which requires a re-triangularization of the network's admittance matrix. As the number of electrical nodes (and hence the admittance matrix size) in the MMC is very large, the number of nodes is very large so the matrix re-triangularization is thus very slow. Therefore, it is essential to provide acceptable solutions for the above issue in order to study and analyse the converter operation.

Simplified averaged models have been proposed in literature for dynamic and steady state behaviour of MMC converter [13]. However, as these methods do not model every level independently, they do not represent the converter in full detail and hence, are unable to simulate capacitor voltage balancing algorithms and abnormal operations of the converter such as failure of a module's control system or failure of the module itself. To overcome these drawbacks, a new modeling approach for the MMC is introduced in this thesis. It partitions the solution into two parts, with the external network solution being implemented in an EMT program and with the MMC represented by a suitable Thévenin's equivalent. The proposed equivalent model is detailed in chapter 4.

1.3 Motivation behind the Research

The MMC is a major step forward in VSC converter technology for HVDC transmission. The control methods and operational analysis of the converter are relatively sparse. The unreduced, full detailed modeling method is extremely difficult in MMC simulation in EMT programs due to the computational inefficiency, thus an accurate modeling approach is required for the detailed studies of the converter on EMT programs. This motivated the investigation of possible solutions for developing an efficient MMC model for use with EMT programs. The EMT program in this case is PSCAD/EMTDC™, one of the widely used EMT simulation tools for power systems [14].

1.4 Objective and Contribution of the Research

The overall objective of this research is to develop an efficient model of the MMC based HVDC converters in EMT simulation programs.

This overall research goal was achieved with the following major contributions:

- Development of a full detailed (unreduced) model of MMC in EMT simulations
- Development and improvement of the voltage balancing algorithm for sub-module capacitors
- Proposing an exact, efficient model for MMC in EMT simulations
- Validating the proposed equivalent model by comparison with EMT time-domain simulations with the full detailed model ("Relative" validation as actual experimental validation is not possible)
- Applying the proposed equivalent model on MMC based HVDC applications
- Development of an average model of MMC
- Estimation switching loss for the MMC converter operation.

1.5 Thesis Outline

The thesis is organized as follows:

Chapter 2 of this thesis summarizes the operational and control aspects of VSC based HVDC systems. The various multilevel converter topologies are also discussed in this chapter.

Chapter 3 details the recently developed modular multilevel converter topology and its controls.

Chapter 4 summarizes the approach of efficient modeling of MMC for electromagnetic transient simulation programs.

Chapter 5 presents the validation of proposed models using full detailed electromagnetic transient simulation model. It also presents the computational efficiency obtained using proposed models for EMT simulations.

Chapter 6 shows the use of the proposed equivalent model in simulating several HVDC transmission applications.

Chapter 7 includes results of estimated operating losses of MMC using a recently developed, time domain simulation approach.

Chapter 8 summarizes the work that is presented and suggests topics for future research and development into the proposed efficient modeling of MMC.

Voltage Sourced Converter

2.1 Introduction

The VSC is a modern converter technology used in high power and high voltage applications. Unlike the thyristors used in conventional LCC [4], [5], the VSC valves, such as IGBTs or GTOs can be turned 'ON' and 'OFF' using a gate signal without a voltage support from the ac system. Thus, the switching characteristics of VSC switching elements make the converter more controllable as compared with the LLC based HVDC converters [15].

Also, the nominal operating frequency of high power IGBTs is in the range of 1-2 kHz whereas the thyristor operations are limited to the power frequency of the ac system (50 or 60 Hz). Therefore particularly in the conventional two- or three- level VSC converters, high frequency pulse-width modulation (PWM) techniques are often used in generating the converter output voltages. PWM can generate the desired output waveforms with reduced lower order harmonic components which reduce the ac filtering requirements.

The VSC converter technology in HVDC transmission applications is discussed in this chapter.

2.2 Basic Two-level Voltage Sourced Converter

The switching cell of a two-level voltage sourced converter is shown in Figure 2-1. One switching cell has two switching elements and they are allowed to conduct one at a time. Since the voltage sources are directly connected to the load through the switches, the load voltage (output voltage) pattern can be varied by changing the firing pulse arrangement of the switch. However, the current can either lag or lead the voltage for a non-resistive load hence switches should be capable of allowing bi-directional flow of current. As IGBTs aren't allowed bi-directional flow of current when they are in conduction mode, an anti-parallel diode is connected with each IGBT of the switching cell.

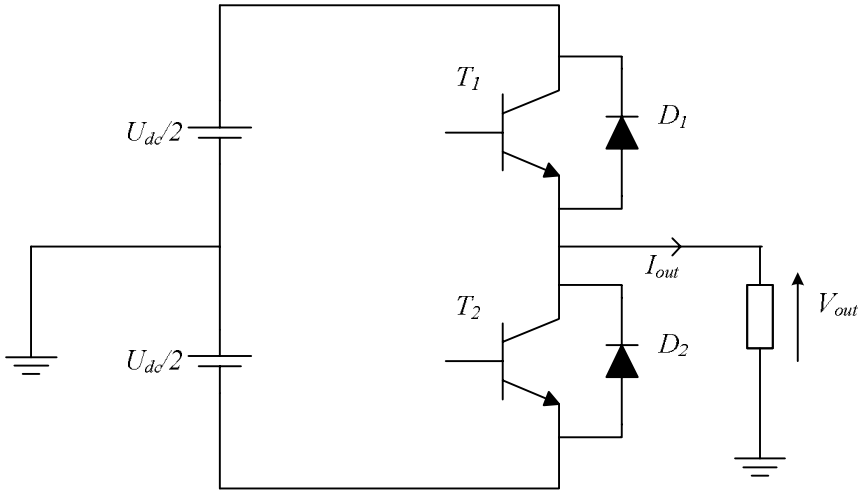


Figure 2-1: A switching cell of a two-level voltage sourced converter

With periodic equidistant firing at constant intervals, the voltage and current waveforms are obtained for an inductive load and shown in Figure 2-2. Note that the converter is referred to as a two-level converter because the output voltage, V_{out} can have one of two values: $U_{dc}/2$ or $-U_{dc}/2$ depending on whether switch combination T_1/D_1 is conducting or T_2/D_2 is conducting.

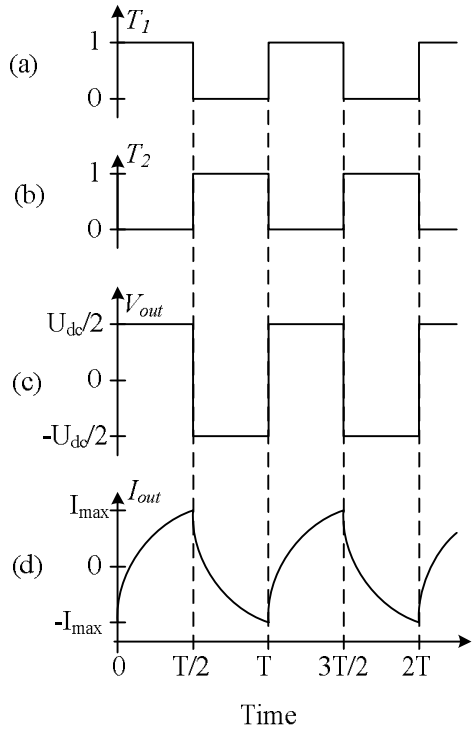


Figure 2-2: Voltage and current waveform shapes for a given switching pattern on a VSC switching cell

For three-phase operation, three such switching cells are placed next to each other, connected to the same dc source as shown in Figure 2-3. Predetermined firing pulses for the phases; a, b, and c are issued with proper phase shifts.

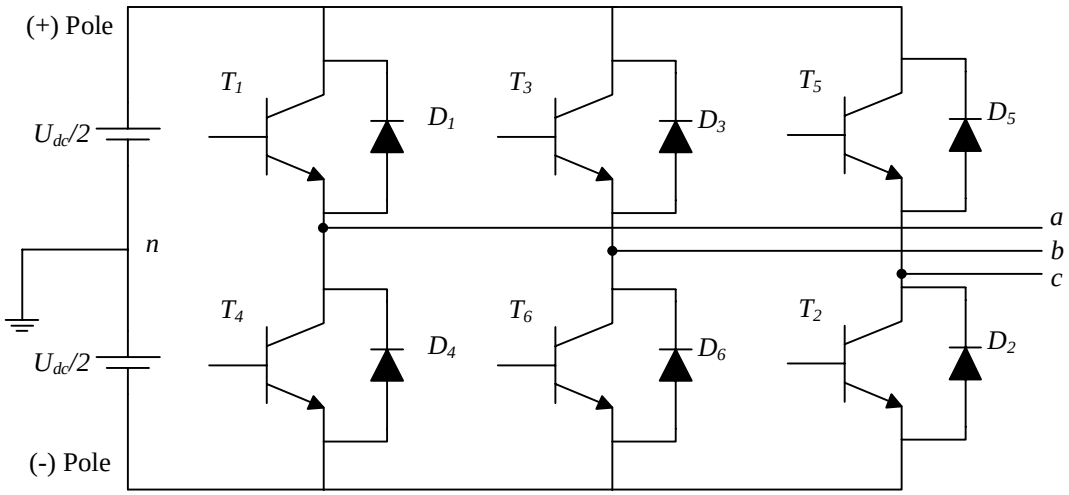


Figure 2-3: Three-phase voltage sourced converter

High frequency PWM is often used to generate VSC output waveforms. The most common and popular technique of carrier based methods is sinusoidal PWM (SPWM) in which the desired output voltage is achieved by comparing the desired reference waveform (modulating signal) with a high-frequency triangular 'carrier' wave.

During SPWM switching operation in a two-level VSC, when the phase reference signal is greater than the carrier signal, that phase connects to the positive dc pole and when the reference is less than the carrier, the phase connects to the negative pole. The SPWM switching operation applied in two-level VSC is shown in Figure 2-4. The carrier signal and the three phase reference signals are shown in Figure 2-4(a). The corresponding three phase output waveforms are in Figure 2-4(b)-(d). In this example, the carrier frequency is equal to 1260Hz (21x60Hz) and the modulation index, the ratio of peak value of reference waveform to the peak value of voltage of carrier waveform is 0.8.

The amplitude of the desired output voltage is determined by the dc link voltage and the modulation index. The switching frequency is equal to the frequency of the carrier

signal. Changes to the desired waveform in phase angle or magnitude can be made by instantaneously changing the PWM pattern. Thus, the VSC is considered as a controllable voltage source.

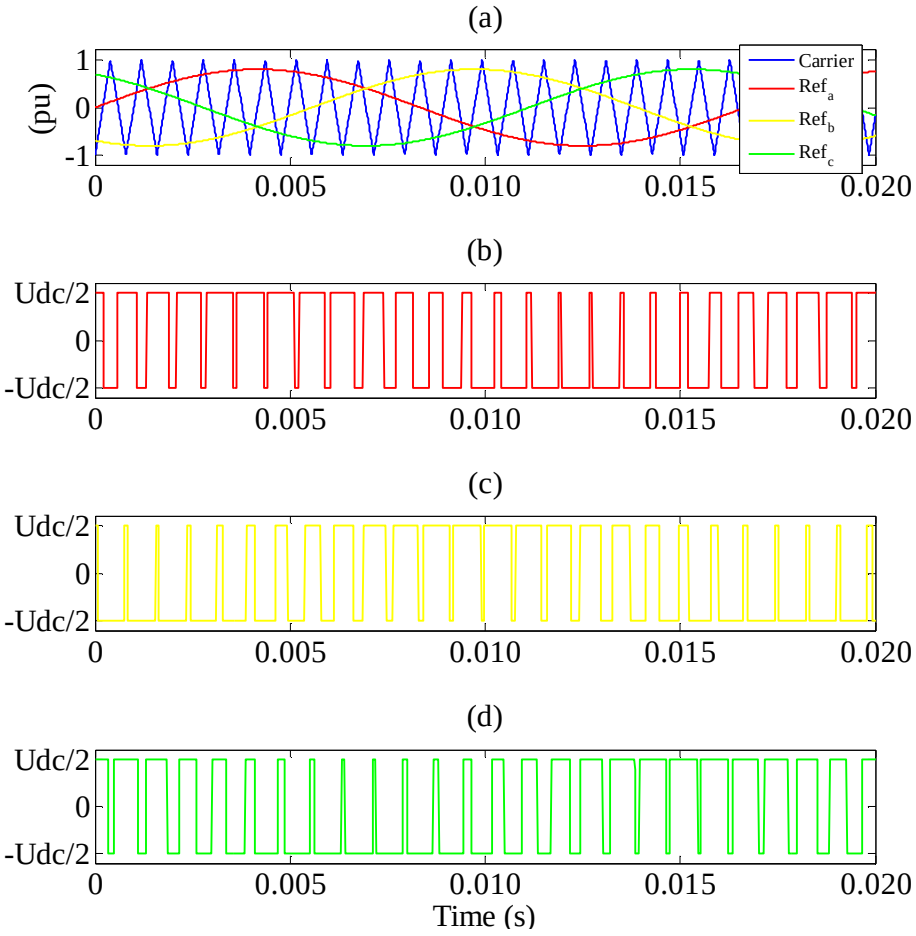


Figure 2-4: Sinusoidal PWM outputs for a two-level VSC:

(a) Carrier and reference, (b) Phase 'a', (c) Phase 'b', and (b) Phase 'c' output waveforms

The frequency plot for the waveforms of Figure 2-4(b)-(d) is shown in Figure 2-5. The resulting chopped square waveforms contain a replica of the desired waveform at its fundamental frequency, with the higher frequency components being at frequencies, close to the carrier (switching) frequency and its integer multiplies.

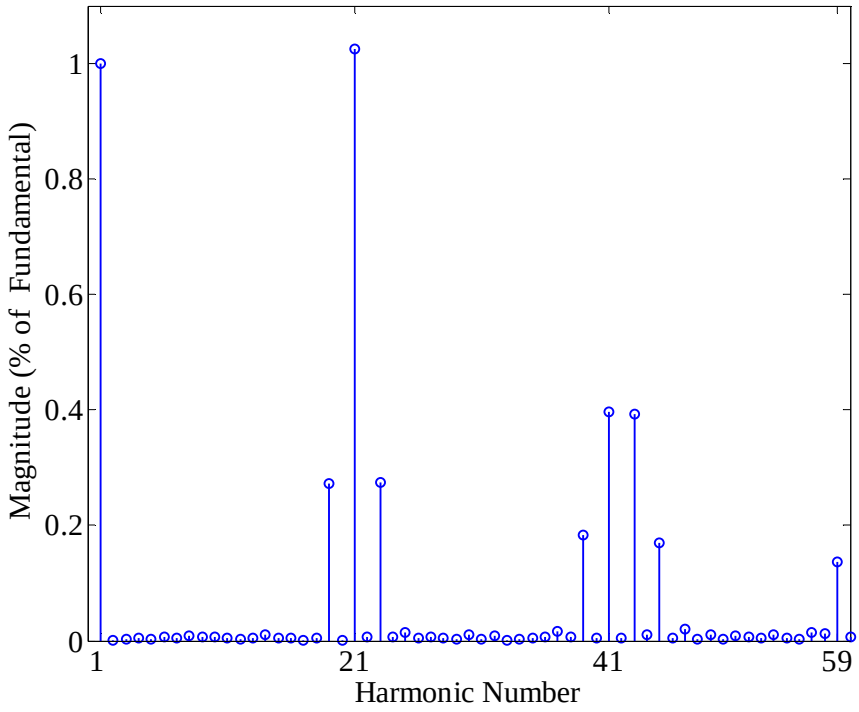


Figure 2-5: Frequency spectrum of sinusoidal PWM

2.3 Two-level VSC Based HVDC System Configuration

Similar to the conventional LCC based HVDC scheme, the VSC based HVDC system also has two converters for rectifier and inverter operation. In VSC, the roles of inverter and rectifier can be interchanged between the stations at any time without voltage polarity reversal. Both stations can independently generate or consume reactive power at the connection point depending on the requirement of the connected ac grid. A typical two-level VSC based HVDC system is shown in Figure 2-6, consisting of converters, converter transformers, ac filters, phase reactors, dc capacitors, dc cables, and control systems [16].

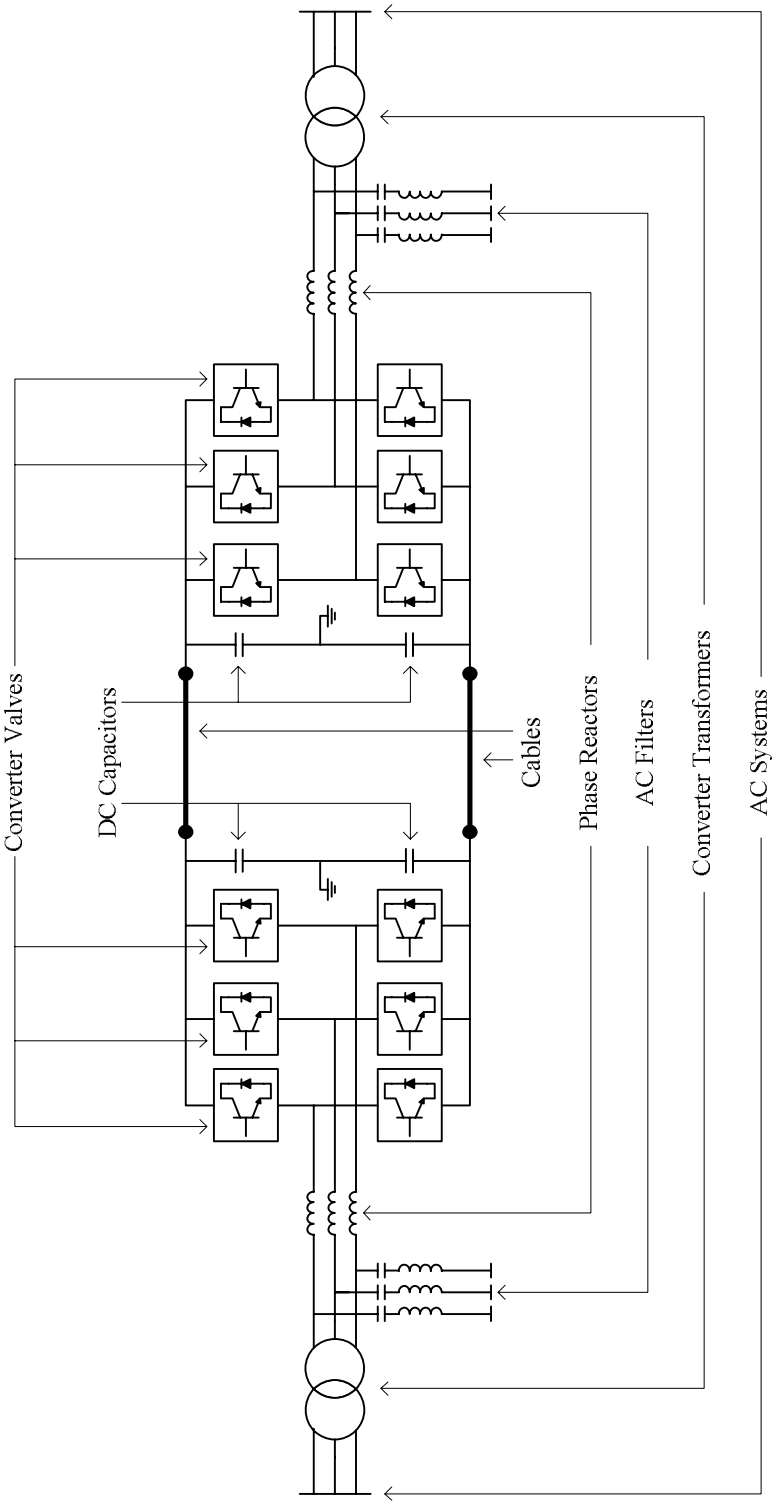


Figure 2-6: Two-level VSC based HVDC circuit diagram

2.3.1 Voltage Sourced Converter Valve Group

Figure 2-7 shows a two-level VSC converter and its valve group which comprises a number of series connected IGBT/diode switches. As the dc link voltage is directly connected with the valve group, the number of IGBT switches is selected based on the required voltage blocking capability of each valve group and the voltage rating of individual IGBT/diode switch.

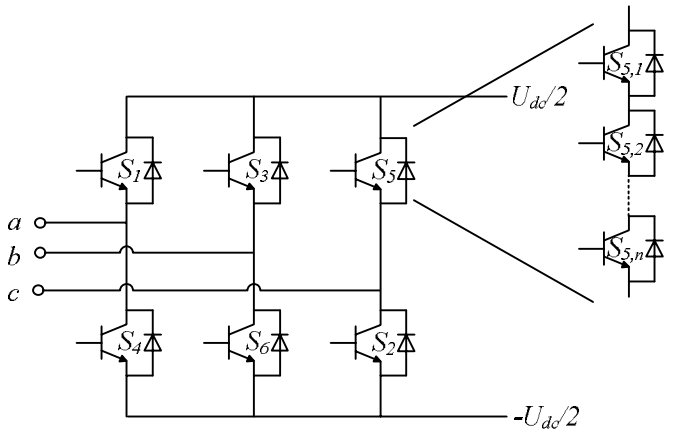


Figure 2-7: Two-level voltage sourced converter and valve group

As all the switches in a valve group are fired simultaneously, the functionality of the valve group is similar to a single IGBT/Diode operation. The operation of the two-level VSC has been discussed in section 2.2.

2.3.2 VSC Transformer

Normally, the converters are connected to the ac system via transformers. The most important functions of the transformer are;

1. to transform the ac system voltage to a value suitable for the converter voltage rating
2. to provide a reactance between converter ac terminals and ac system

The transformer is exposed to the converter ac voltage. In two-level converter operation, the magnitude of the converter ac voltage switches between the converter positive dc bus voltage and the negative dc bus voltage within a few microseconds. Such steep voltage steps in the shape shown in Figure 2-2, result in high stresses in the transformer insulation [17].

2.3.3 Phase Reactors

Since the VSC is an ac voltage source with low internal impedance, a series inductive interface with the ac system is essential. The electric reactor is acting as an energy linking unit between VSC converter and ac power system. In some cases, this inductive interface can be provided by the leakage inductance of the converter transformer otherwise, when it is not sufficient, a combination of the transformer inductance and the phase reactors is used [18].

2.3.4 AC Filters

In LCC based HVDC systems, the ac filters serve the dual purpose of diminishing ac harmonics and supplying reactive power at fundamental frequency. Since a VSC can operate at any desired power factor, the latter requirement is not essential, and therefore converter configurations are chosen to achieve acceptable harmonic levels for utility

application with small harmonic filters [19]. The harmonics introduced by the PWM operation in two-level VSC are at higher orders compared to the fundamental frequency. Therefore, high order filters are required and some of the harmonics are naturally diminished with the damping of the electrical network. Series or shunt filters, or a combination of both, may be necessary to achieve the harmonic performance set by the design.

2.3.5 DC Capacitors

On the dc side, there are two identical capacitor stacks. The main objective of the dc capacitor banks is to serve as energy storages in order to control the power flow in two-level VSC based HVDC [15]. In addition, it can be used to reduce the voltage ripple on the dc side caused by the PWM switching operation. Due to PWM switching action, the current flowing to the dc side of a converter contains harmonics which will result in a ripple on the dc side voltage. The magnitude of the ripple depends on the dc side capacitor size and the switching frequency. Therefore, the size of these dc capacitors is a function of the stored energy at the rated dc voltage and the permissible dc voltage ripple [15].

2.3.6 DC Transmission Lines

To transmit electric energy over a distance, both cables and overhead transmission lines can be used. Even though, the overhead lines are economical at the initial stage of

the project, in the long term operation, the underground cable system has significant advantages as listed below [20]:

- An underground cable has no visual impact on the landscape. Once it is installed, the cable route can be used for temporarily purposes such as agriculture and farming.
- Due to reduced risk of damage for the cables from natural causes such as storms, lightning, wind, and earthquakes, the system reliability is enhanced as the cable system is less likely to have line faults [20].
- The width of the corridor to install the underground cable can be as narrow as 4 meters, which will give greater flexibility with the selection of a transmission route [20].
- Underground cables rarely meet with public opposition and often receive political support. Operation and maintenance costs of the transmission easement are virtually eliminated as there is no need for long term contracts to maintain the easement with suitable access roads, thermo-graphic checks of conductors' joints, and insulator replacements [20].
- There are considerable cost savings to the community in terms of amenity, property values, and possible health risks.
- The cable can be easily laid across sea or other water body and hence it does not make a significant impact on usable lands.

2.3.7 Control System

The basic control structure used for VSC based HVDC transmission system is shown in Figure 2-8. As an integrated power transmission system, the control of active power in the converter station should be coordinated. The coordination of active power control between the stations is realized by designating only one converter controlling the dc side voltage whereas other converter controls the active power. A constant dc voltage control gives a “slack bus” which will result in an automatic balance of active power flow between stations. Controlling ac voltage or reactive power, however, is independent for each station. Depending on the requirement and the limitations of the connected ac grid, the control can be switched between “AC voltage control” and “Reactive power control” modes [21].

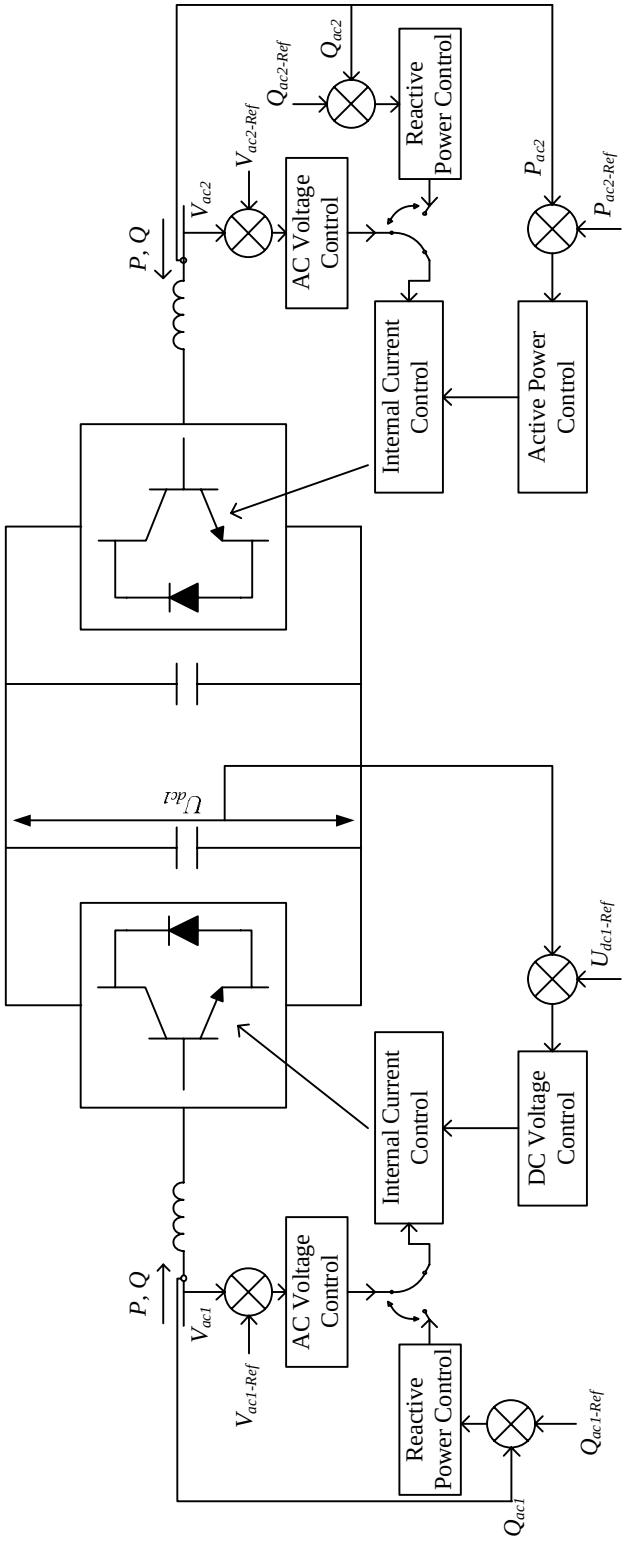


Figure 2-8: Basic control structure of VSC based HVDC system

2.4 Operating Principle of VSC Based HVDC System

The fundamentals of VSC based HVDC system operation can be explained by considering each terminal as a voltage source connected to the ac transmission network via a three-phase reactor. The two terminals are interconnected by a dc link, as schematically shown in Figure 2-9. X_l is the total reactance of the converter transformer and the phase reactor (if equipped) and V_{ac} and V_{out} are rms voltages at the point of common coupling (PCC) and at the converter terminals respectively. The phase displacement angle of the converter output voltage with respect to the ac system voltage is δ and the voltage difference between the PCC and the VSC is ΔV. U_{dc} and I_{dc} are the dc link voltage and current. The active power and reactive power exchanged between the VSC and the ac system are P_c and Q_c. In the following discussion, the active power is defined as positive if the converter absorbs power from the ac system and reactive power is positive if the converter injects power to the ac system. The phase displacement angle is considered to be positive if the ac voltage leads the converter output voltage the in phase.

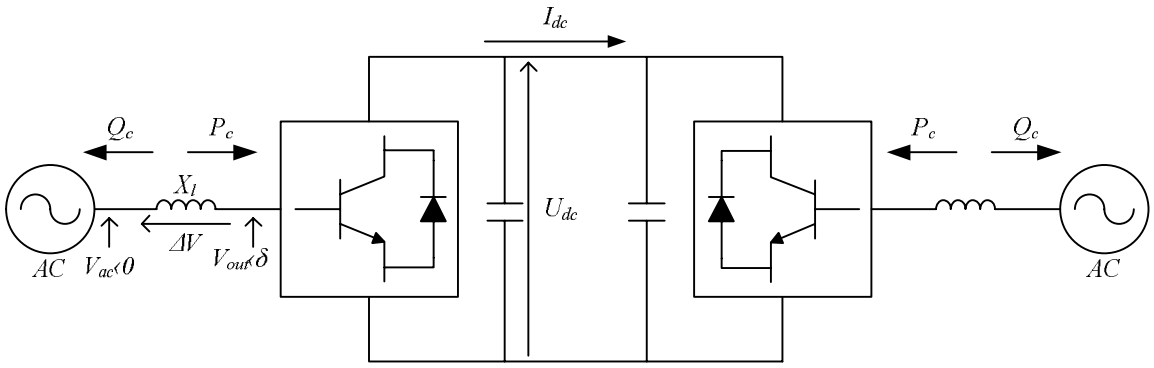


Figure 2-9: VSC based HVDC transmission operation

If the voltage at the dc link, U_{dc} is assumed to be constant then the fundamental frequency component of converter phase output ac voltage can be obtained as given in Equation (2-1).

$$v_{out(1)_p}(t) = m\frac{U_{dc}}{2}\sin(\omega t + \delta) \qquad \textbf{2-1}$$

Here, m is the modulation index.

The rms value of the fundamental component of the converter line to line output voltage, $V_{out(1)}$ is directly proportional to the dc link voltage U_{dc}, as given in Equation (2-2).

$$V_{out\,(1)} = \sqrt{\frac{3}{2}} \cdot m\,\frac{U_{dc}}{2} \qquad \textbf{2-2}$$

Assuming the impedance between the PCC and the converter terminals is inductive, the real power and reactive power can be expressed as in Equation (2-3) and Equation (2-4) respectively [22].

$$P_c = U_{dc} \cdot I_{dc} = -\frac{V_{ac} \cdot V_{out(1)}}{X_l} \sin(\delta) \quad \textbf{2-3}$$

$$Q_c = -\frac{V_{ac}\left(V_{ac} - V_{out(1)} \cos(\delta)\right)}{X_l} \quad \textbf{2-4}$$

Equation (2-3) shows that the active power is proportional to the dc current and the dc voltage. Also, it is mainly determined by the phase-displacement angle δ. A negative phase shift ($V_{out(1)}$ lags V_{ac}) results in that the active power flows from the ac network to the converter. The reactive power is mainly determined by the difference between the magnitudes of the PCC voltage and the converter output voltage according to Equation (2-4). The reactive power is fed from the voltage with higher magnitude towards the voltage with the lower magnitude. These features permit the independent control of the reactive and active power which is a major advantage for the VSC.

In Equations (2-3) and (2-4), the only controllable parameters are the phase displacement angle, δ and the amplitude of the fundamental frequency component of converter output voltage $V_{out(1)}$. As given in Equation (2-2), the magnitude of the fundamental component of the converter voltage depends on the modulation index, m. Therefore, the active power and reactive power can then be controlled by controlling the phase angle, δ and the modulation index, m respectively.

2.4.1 Four – Quadrant Operation of VSC

Figure 2-10 shows the phasor diagram for the VSC converter connected to the ac network. In Figure 2-10, I_{ac} is the ac line current. The direction of active power flow

decides the rectifier or inverter operation of converter and the capacitive and inductive modes of the converter are determined using the direction of reactive power absorption.

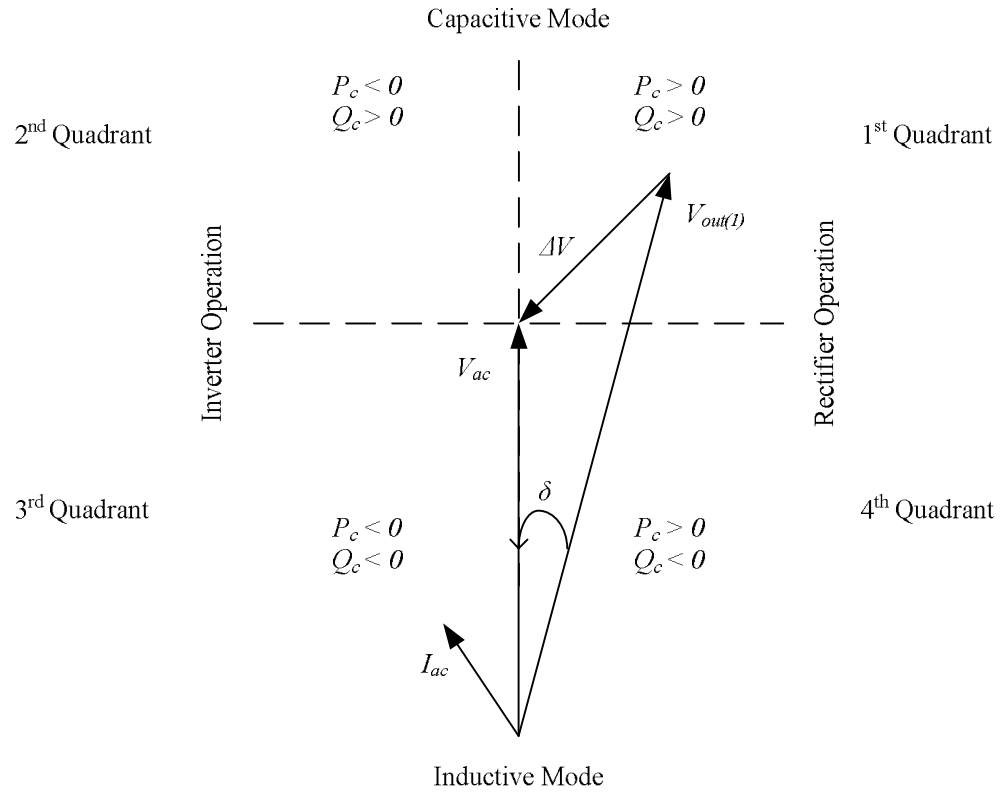


Figure 2-10: Phasor diagram of VSC and direction of power flows

As shown in Figure 2-10, the ac system voltage, V_{ac} leads the converter ac output voltage, $V_{out(1)}$ by an angle δ in the first quadrant. The converter absorbs the active power from ac system. The converter output voltage magnitude is higher than ac system voltage thus, the converter injects reactive powers to the ac system. This is the capacitive mode of rectifier operation of the converter.

In the second quadrant, real power is negative and the reactive power is positive. This means converter injects both real power and reactive power to the ac system and this is

the capacitive mode of inverter operation. In this case, the converter output voltage amplitude is higher than ac bus voltage but it leads the ac bus voltage by an angle δ.

Both the active and reactive powers are negative in the third quadrant. The converter injects real power to the ac system and absorbs reactive power from the ac system. This is the inductive mode of inverter operation. In this case, the ac bus voltage magnitude is higher than the converter output ac voltage and it leads by an angle δ.

In the fourth quadrant the converter absorbs both the real power and reactive power from the ac system. This is the inductive mode of rectifier operation. The converter output ac voltage lags behind the ac system voltage but its magnitude is less than the ac system voltage.

The phasor diagram can be used to illustrate the ability of VSC to operate in all four quadrants of P-Q diagram [15].

2.4.2 P – Q Diagram for VSC Operation

Using the Equations (2-3) and (2-4), the relationship between the real power and reactive power of VSC based HVDC system connected to an ac system can be derived as given in Equation (2-5).

$$P_c^{\,2} + \left(Q_c - \frac{V_{ac}^{\,2}}{X_l} \right)^2 = \left(\frac{V_{ac} \cdot V_{out(1)}}{X_l} \right)^2 \qquad \textbf{2-5}$$

According to Equation (2-5), P-Q relationship of the VSC based HVDC transmission system is shown in Figure 2-11 [22]. If the output voltage of the converter $V_{out(1)}$ is

reduced using PWM, it is possible to supply any active and reactive power within the circle.

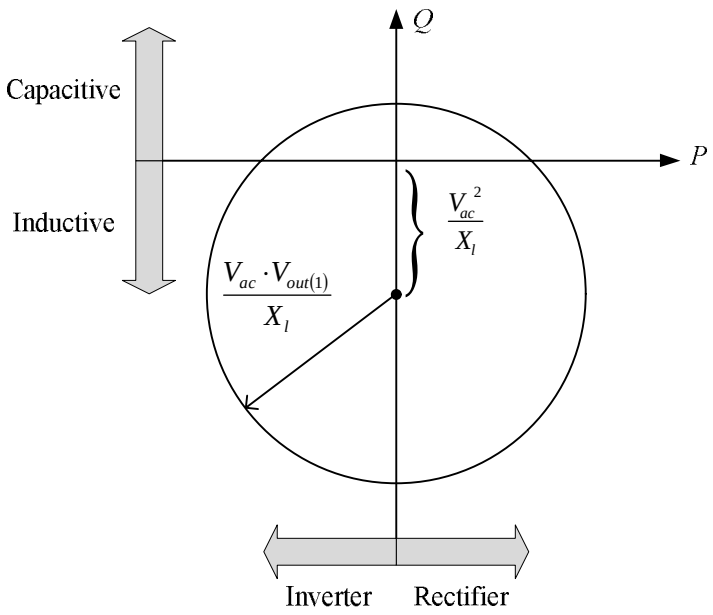


Figure 2-11: P - Q relationship of VSC based HVDC system connected to an ac system

However, there are operational limits of the converter which limit the transfer capability of active and reactive powers [23].

1. Converter Current Limitation

This is imposed by the current rating of the converter valve. Since both the active power and reactive power contribute to the current flowing through the valve, this limitation is manifested as a circle. Accordingly, if the converter is intended to support the ac system with reactive power absorption/injection, the maximum active power has to be limited to make sure that the converter current is within the limit.

2. Over-voltage and Under-voltage Magnitude

The over-voltage limitation is imposed by the direct voltage level of the VSC. The under voltage limit, however, is limited by the active power transfer capability, which requires a minimum voltage magnitude to transmit the active power.

Applying the current and voltage limitations of the VSC, the operating range of the theoretical P-Q capability diagram is reduced. The modified P-Q diagram is shown in Figure 2-12 [23].

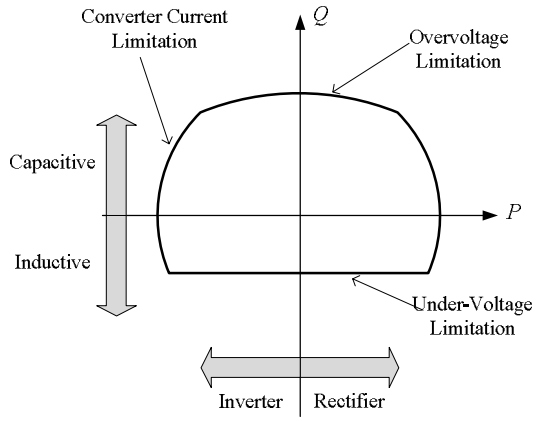


Figure 2-12: Reduced operating range of P – Q diagram

2.5 Advantages and Applications of VSC Based HVDC

The following factors make VSC based HVDC transmission attractive over the LCC based HVDC topology [24].

1. Independent Control of Reactive Power and Active Power [25], [26]

With PWM, the VSC based HVDC offers rapid control of active and reactive power control independently. It is possible to enhance the system transient stability, and to improve the damping of low frequency power oscillations by controlling the active power. The reactive power control has a significant contribution on system stability. Therefore, VSC based HVDC has the degree of freedom to facilitate the any (or all) compensation requirement of ac network.

2. Operation in Extremely Weak Systems [15], [16]

Since the VSC switches are force commutated (i.e. turned 'ON' or turned 'OFF' on command), the converter is able to build its own ac voltage at any predetermined frequency without the need for ac voltage support. Therefore, it is possible to feed ac systems with low short circuit power or even passive networks with no local power generation. Also, the converter can be controlled to supply or absorb reactive power. Therefore, it may be used to supply industrial installations or large wind farms without other reactive power support.

3. Power Quality and System Stability Improvement [27], [28]

Reactive power and ac voltage are direct controllable parameters in VSC based HVDC. Therefore, continuous adjustment of power or voltage feedback can improve the power quality and system stability.

4. Black Start Capability [29], [30]

Restoring power after a wide-area power outage, or blackout, can be difficult and time consuming, as power plants need to be restarted under the condition of no power supply from the grid. The ac grid, which is already at an outage or "blackout", can be started up by using HVDC converter station. It can provide effective voltage and frequency stabilization during the restoring process with VSC based HVDC systems. This will make the restoration less complicated and more reliable.

5. Multi-terminal VSC Based HVDC Grids [31]-[34]

A multi-terminal VSC based HVDC scheme consists of three or more converter terminals with different control objectives. An interconnection between different converters to a common bipolar dc bus can reduce operational costs while increasing reliability.

Conventional, LCC based HVDC systems face a steep challenge when it comes to multi-terminal connections, as it needs reversal of voltage polarity during reversal of power flow. Since maintaining a constant dc voltage during all conditions is an important characteristic of the multi-terminal schemes, the conventional, LCC based HVDC is not a good candidate for it. In contrast, a VSC based HVDC system alters the power direction by changing the direction of the current. This makes it easier to use VSC based HVDC scheme in systems with multiple terminals.

The aforementioned advantages promote the demand for VSC based applications in HVDC field and it can be foreseen that more and more VSC based transmission projects

will be put into operation in the future. A number of existing and potential applications of these systems are discussed below:

1. Network Interconnections [35], [36]

In recent years, due to the increased demand in energy markets, certain regional network tie lines are fully loaded frequently and thus restrict the economic power transfer between adjacent regions. Regional interconnections enhanced through VSC based HVDC links can effectively improve the transfer capability between regional networks.

2. Transmission Bottleneck Mitigations [37]

Transmission congestion occurs when actual or scheduled flows of electricity across a portion of network are restricted below desired levels and transmission line bottlenecks are caused by system stability limitations. Series and shunt compensation may have been used already to alleviate the congestion and right of way problems may prohibit new transmission lines.

A VSC based HVDC system can also be installed in parallel with the ac system where the transmission bottleneck occurs. For parallel ac/dc transmission schemes, full power flow controllability of VSC based HVDC system allows optimized power sharing between ac lines and the dc link. It has been shown in system studies that the transient stability issues due to transmission bottlenecks can be reduced by introducing a VSC based HVDC scheme in parallel due to effective damping control and dynamic voltage support. In addition, the transfer capability can be increased by more than the rating of the VSC based HVDC system.

3. Integration of Renewable Energy Sources [35], [38]

The VSC based HVDC system is the most suitable candidate for reliable and robust power transmissions in connecting offshore wind or other renewable, remotely located power generation into the main grid due to compact converter station and flexible voltage and frequency control.

4. DC In-feed to Large Urban Areas [35], [39]

A multi-terminal HVDC grid can be used to improve or partly replace an existing network which is applicable when large scale expansions of a city is foreseen.

5. DC Segmented Grid [40]

An inordinate spending on equipment and very complex systems are required when cascading network segments using ac based technology. Also, installing more ac tie lines and devices will add to the complexities of grid operations and dynamics which are at the core of increased concerns over supply reliability. Alternative means to minimize the risk of cascading outages should be explored.

One long standing proposal involves dc aided segmentation which is defined as the decomposition of any large inter-regional grid into a set of asynchronously operated, dc interconnected sectors. It has also been suggested that dc aided segmentation can be used to expand transfer capability.

Due to these large number of potential applications, VSC schemes are being progressively developed for high voltage and high power transmission systems.

2.6 Challenges in VSC Based HVDC Systems

Along with numerous advantages, conventional VSC based HVDC technology faces certain challenges and issues which are discussed below.

Since each switching event creates losses in the semiconductors, high frequency PWM increases the converter losses. In the initial development of VSC based HVDC applications, the switching frequency used to be in the range of 1.5 KHz to 2.0 kHz. However in subsequent stages of development, the switching frequency for two-level VSCs has been brought down to about 1 kHz in order to reduce losses. It may be possible to go even further, but this would call for increased filtering, which would partly outweigh the benefits of VSC.

One further limitation of VSC is the requirement of series connection of a large number of IGBTs (or GTOs) when two-level or three-level converters are used, which is challenging. Also, higher initial cost (converter cost), sensitivity to dc side faults, and the fact that the technology is still fairly new are some other drawbacks of this converter topology [41], [42].

Many of these drawbacks and limitations of the two- or three- level converters can be eliminated by using a topology which is capable of creating an approximately sinusoidal voltage waveform at the ac terminals. Converters with that capability are called multilevel converters.

2.7 Multilevel VSC Topologies

The multilevel converter generates a near sinusoidal, staircase voltage waveform using multiple levels, typically obtained from capacitor voltage sources. Also, it has the ability to significantly reduce the voltage stress on each switching device due to the utilization of multiple levels on the dc bus. The resulting waveform can be designed to closely follow a sine wave, hence the required ac side filters are minimal or zero. The switching frequency of each individual power electronics switch is only a fraction compared to that of a two-level converter. The voltage step at each level is also smaller. These factors result in considerable switching loss reduction.

Numerous multilevel topologies have been introduced for different high power, high voltage applications such as, static var compensation, variable speed motor drives, and high voltage system interconnections [43]-[46]. Three of the most common designs are;

1) Diode clamped multilevel converter
2) Flying capacitor based multilevel converter
3) Modular multilevel converter (MMC)

2.7.1 Diode Clamped Multilevel Converter

The single phase circuit arrangement of the inverter structure of a diode clamped converter is shown in Figure 2-13 [47], [48]. In this circuit, a common dc bus voltage is split into five levels using four series-connected bulk capacitors C_1, C_2, C_3, *and* C_4. The voltage stress across each switching device is limited to the corresponding capacitor voltage neglecting the drop across the clamping diodes.

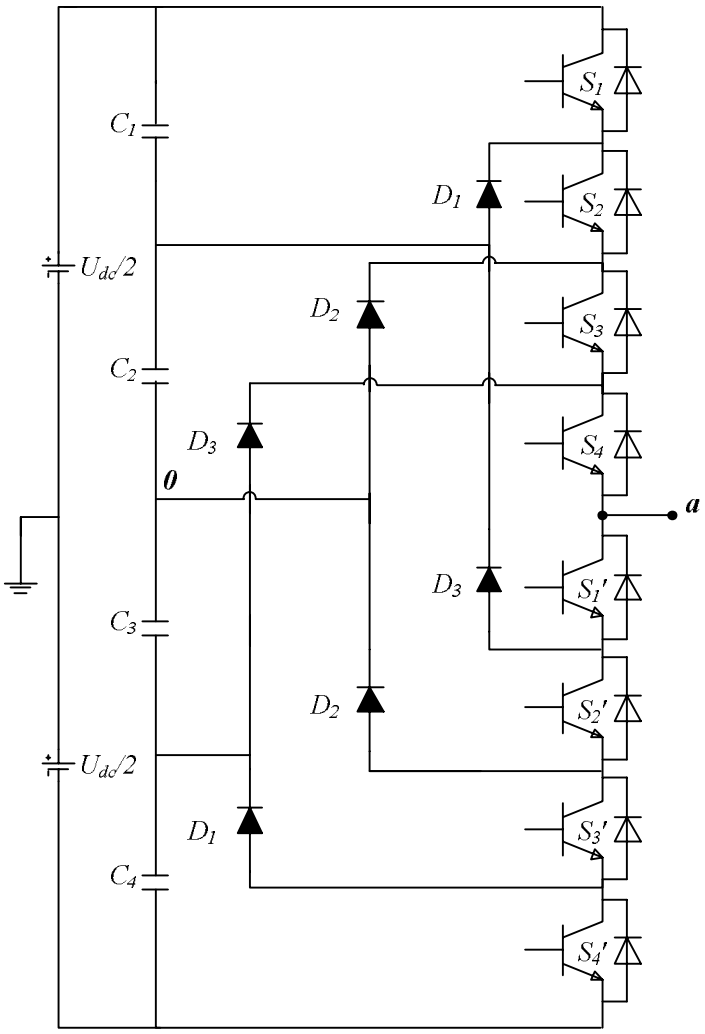


Figure 2-13: Phase leg of a diode clamped multilevel converter

Table 2-1 lists the output voltage levels possible for one phase of the inverter with the negative dc rail voltage v_0 as a reference. The state '1' corresponds the switch being on, and '0' corresponds to the switch being 'OFF'. Each phase has four complementary switch pairs such that turning on one of the switches of each pair requires the other complementary switch be turned 'OFF'. The complementary switch pairs for phase leg are (S_1, S_1'), (S_2, S_2'), (S_3, S_3'), and (S_4, S_4'). Table 2-1 also shows that in a diode clamped

inverter, the switches on for a particular phase leg are always adjacent and in series. For a five-level inverter, a set of four switches is on at any given time.

Table 2-1: Diode-clamped five-level inverter voltage levels and corresponding switch states

Voltage, v_{a0}	Switch State							
	S_1	S_2	S_3	S_4	S_1'	S_2'	S_3'	S_4'
$U_{dc}/2$	1	1	1	1	0	0	0	0
$U_{dc}/4$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-U_{dc}/4$	0	0	0	1	1	1	1	0
$-U_{dc}/2$	0	0	0	0	1	1	1	1

Although each active switching device is required to block only a single step of the output voltage v_{a0}, the clamping diodes require different ratings for reverse voltage blocking. As an example, in Figure 2-13 when all the lower switches S_1' to S_4' are turned on, D_3 must block three voltage levels, or $3U_{dc}/4$. Similarly, D_2 must block $U_{dc}/2$ and D_1 must block $U_{dc}/4$. If the inverter is designed such that each blocking diode has the same voltage rating as the active switches, D_k will require k diodes in series; consequently, the number of diodes required for each phase would be $(m-1) \times (m-2)$ for an m-level diode clamped inverter. Thus, the number of blocking diodes is quadratically related to the number of levels in a diode clamped converter.

The efficiency of the converter is high because all devices are switched at the fundamental frequency. The diode clamped method can be applied to higher level converters which gives minimum harmonics distortion to the system. Adding a voltage level involves adding power electronics switches to each phase but it does not require an

increase in the voltage rating of an individual switch. Unfortunately, the number of the achievable voltage levels is quite limited not only due to voltage clamping requirement but also due to voltage unbalancing problems, circuit layout, and packaging constraints [43].

2.7.2 Multilevel Converter Using Flying Capacitors

A single phase circuit for a five-level flying capacitor multilevel inverter is shown in Figure 2-14 [49].

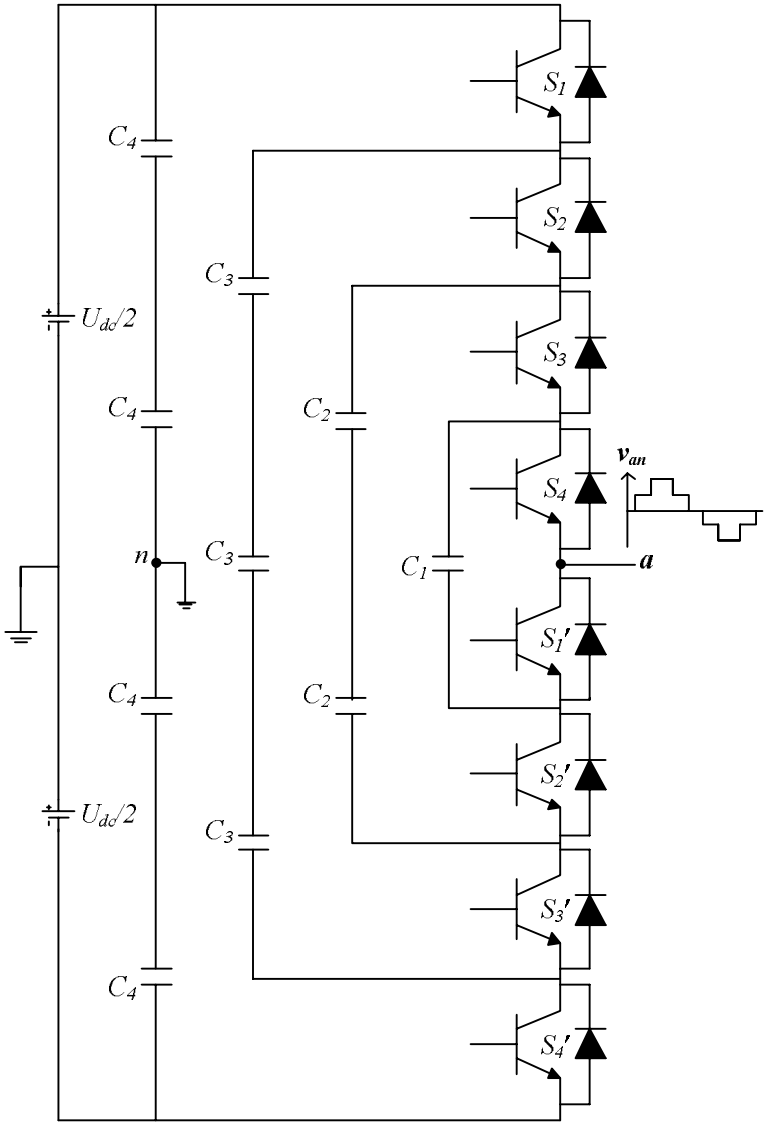


Figure 2-14: Capacitor clamped five-level inverter circuit topology

All capacitors are charged to the same voltage $U_{dc}/4$ for the arrangement in Figure 2-14. The output voltage of the inverter, v_{an} can be synthesized by the following switch combinations.

1. For voltage level $v_{an} = U_{dc}/2$, turn on all upper switches $S_1 – S_4$.
2. For voltage level $v_{an} = U_{dc}/4$, there are three combinations:

a. S_1, S_2, S_3, S_1'

b. S_2, S_3, S_4, S_4'

c. S_1, S_3, S_4, S_3'

3. For voltage level $v_{an} = 0$, there are six combinations:

a. S_1, S_2, S_1', S_2'

b. S_3, S_4, S_3', S_4'

c. S_1, S_3, S_1', S_3'

d. S_1, S_4, S_2', S_3'

e. S_2, S_4, S_2', S_4'

f. S_2, S_3, S_1', S_4'

4. For voltage level $v_{an} = - U_{dc}/4$, there are three combinations:

a. S_1, S_1', S_2', S_3'

b. S_4, S_2', S_3', S_4'

c. S_3, S_1', S_3', S_4'

5. For voltage level $v_{an} = - U_{dc}/2$, turn on all lower switches; S_1' – S_4'.

Similar to phase '*a*', two independent sets of capacitors have to be provided for other two phases as well, thus requiring a large number of bulk capacitors for a three phase converter operation. Despite the large number of storage capacitors providing extra ride through capability during power outages, high voltage level systems are more difficult to package and more expensive with the requirement of bulky capacitors. By proper selection of capacitor combinations, it is possible to balance the capacitor charge. However when it involves real power conversions, the selection of a switch combination

becomes very complicated and the switching frequency needs to be higher than the fundamental frequency.

The real power transfer is a burden in multilevel VSC topologies as described in sections 2.7.1 and 2.7.2. Hence, it limits the applicability of those topologies especially in HVDC power transmissions.

2.7.3 Modular Multilevel Converter

This new and particularly powerful topology is a revolutionary in HVDC transmission. As it is the main focus of this thesis, it is described in detail in next chapter.

Modular Multilevel Converter for HVDC Transmission

3.1 Introduction

As introduced in chapter 2, the recent development in VSC technology, the MMC is a major step forward in VSC based HVDC transmission [7], [50], [51]. This arrangement is designed to lower the switching frequency, avoid connecting the devices in series, enable scaling, and modular structure for different power level and voltage level.

The operational and control aspects of MMC topology are discussed in the following sections of this chapter. The results of several time domain simulations are presented to illustrate the various aspects of MMC operation.

3.2 MMC Circuit Structure

The block diagram of three-phase MMC is shown in Figure 3-1 [51]. Each phase unit consists of two multi-valves; an upper and a lower multi-valve, each containing '*N*' number of series-connected power sub-modules.

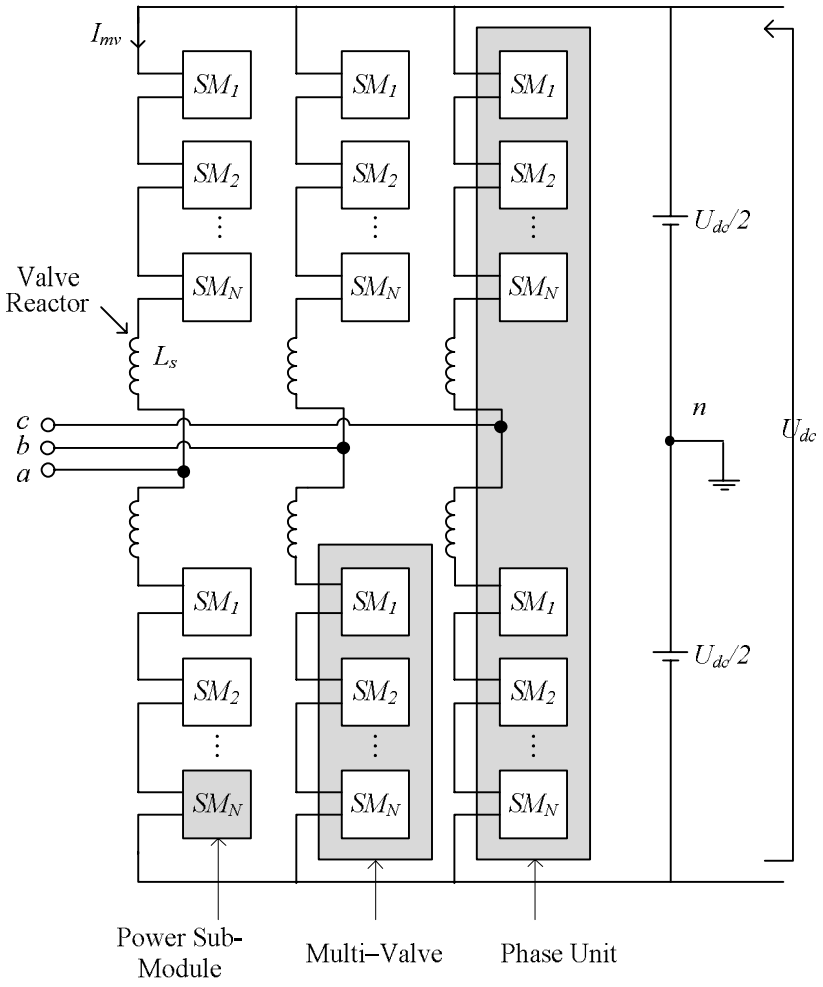


Figure 3-1: Three-phase MMC with 'N' sub-modules per multi-valve

Depending on the structure of cascaded sub-modules, modular multilevel converters can be divided into two categories; (1) Half-bridge and (2) Full-bridge. The structure of these modules is shown in Figure 3-2.

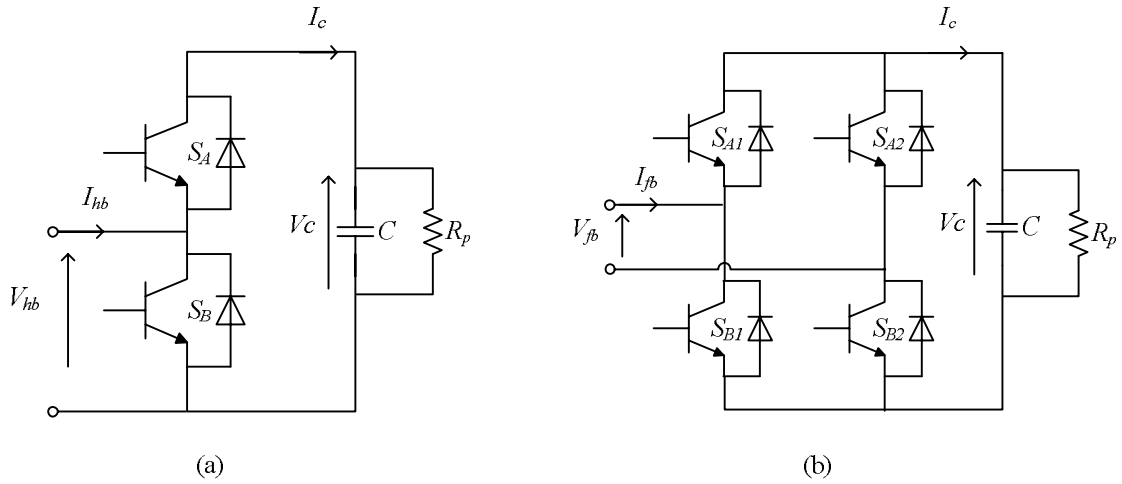


Figure 3-2: Sub-module of MMC converter:

(a) Half–bridge sub-module and (b) Full–bridge sub-module

3.2.1 Half–Bridge Sub–Module

The half–bridge sub-module contains two IGBT/diode switches (S_A and S_B) and a capacitor, C as shown in Figure 3-2(a). The power loss of the half–bridge sub–module capacitor is represented by the resistor, R_p in Figure 3-2. In normal operation, exactly one of S_A and S_B is on at a given time instant [51].

Assuming the capacitor voltage V_c is a constant, the output voltage V_{hb} of each half-bridge sub-module can take on one of two different voltage levels; V_c or zero. With S_A in the 'ON' state, voltage V_{hb} is equal to V_c, and when S_B is 'ON', V_{hb} is zero as given in Equation (3-1). Therefore, it is possible to selectively and separately control each of the individual half-bridge sub-modules in the converter to provide a voltage which is either V_c or zero.

$$V_{hb}(t)=\begin{cases}V_c & if\ S_A-ON\ \&\ S_B-OFF\\ 0 & if\ S_B-ON\ \&\ S_A-OFF\end{cases} \quad \textbf{3-1}$$

3.2.2 Full–Bridge Sub–Module

Figure 3-2(b) shows the basic building block of the full-bridge sub-module which consists of four IGBT switches S_{A1}, S_{A2}, S_{B1} and S_{B2} and a capacitor *C*. In normal operation, each module can generate output voltage of $+V_c$, *0*, or $-V_c$ as given by Equation (3-2):

$$V_{fb}(t)=\begin{cases}+V_c & if\ S_{A1},S_{B2}-ON\ \&\ S_{A2},S_{B2}-OFF\\ 0 & if\ S_{B1},S_{B2}-ON\ \&\ S_{A1},S_{A2}-OFF\\ 0 & if\ S_{A1},S_{A2}-ON\ \&\ S_{B1},S_{B2}-OFF\\ -V_c & If\ S_{A2},S_{B1}-ON\ \&\ S_{A1},S_{B2}-OFF\end{cases} \quad \textbf{3-2}$$

The full-bridge modular structure was primarily used in static synchronous compensator (STATCOM) applications [52]-[55]. However, it is now being developed as a technology also for use in HVDC transmission [56], [57].

The MMC converters have similar ability to reduce the harmonic content of the ac side waveform [53], [58], [59]. The advantage of half-bridge structure is a smaller switching element count and reduced power loss. However, this structure cannot limit the over-current resulting from a dc side fault. The full-bridge sub-modules can produce a reverse voltage which opposes the driving ac voltage and hence provides a negative back electromotive force (emf) to the flow of the fault currents resulting from the dc side faults. This structure however has a larger switching element count and hence, higher converter cost and operating losses as compared to the half-bridge topology.

The modular structure of the MMC can be easily used to increase the voltage rating and power rating of the converter by adding more power sub-modules into each multi-valve. As the full dc bus voltage is utilized by all the sub-modules in normal operation, the voltage rating of sub-module is determined by the rated dc bus voltage of the system. Also, none of these topologies require series connection of several semiconductor switches, which has been a challenge in earlier VSC configurations.

From the dc side, all three phase units are shown to be a parallel connection of three voltage sources. In practice, there will be a small difference in instantaneous values of all three voltages. Therefore, a valve reactor is inserted into each multi-valve (L_s in Figure 3-1) to reduce the circulating currents between individual phase units [60]. Also, the reactor is capable of reducing the current rising rate during low impedance dc side faults. Therefore, the faults can be easily detected and the IGBTs can be turned 'OFF' at low critical levels of fault currents. This provides very effective and reliable protection method for the converter [61].

The half-bridge sub-module converters are more common and the more widely used type in MMC based HVDC transmission applications. However, the significant operational differences between the half-bridge and full-bridge sub-module converters are highlighted in the applicable sections.

3.3 Output Voltage Waveform Synthesis

Two output voltage synthesis methods proposed for the MMC operation; (a) nearest level estimation [60] and (b) multilevel PWM [7] are discussed below.

3.3.1 Nearest Level Estimation

The switches of sub-modules can be controlled in an appropriate way, so that the individual step from each sub-module provides a multilevel near-sinusoidal waveform similar to the requested sinusoidal voltage reference, v_{ref} as shown in Figure 3-3 [60], [62], [63].

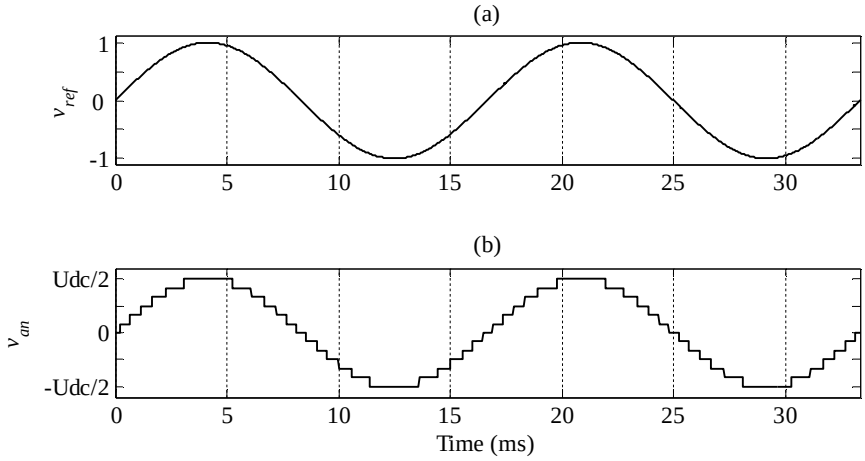


Figure 3-3: Output waveform from nearest level estimation:

(a) Reference waveform and (b) MMC output waveform for 12 sub-modules/multi-valve

When the sub-module output voltage is equal to V_c, it is said to be in the 'ON' state, and when it is zero, it is considered to be 'OFF'. To determine the required 'ON' state sub-modules at a particular instant, the reference sine wave is compared with total 'N' discrete equidistant quantization thresholds. The number of sub-modules, required to be 'ON' in the upper and lower multi-valves is thus determined as given in Equation (3-3).

$$N_l = round\left(v_{ref} N\right)$$
$$N_u = N - N_l \qquad \textbf{3-3}$$

3.3.2 Multilevel PWM

Various modulation methods have also been discussed for generating output waveforms using MMC [7], [64]-[66]. Carrier phase-shifted, multilevel sinusoidal PWM is one of the most commonly used modulation strategies for MMC operation. It can effectively reduce the generated harmonic voltages using low switching frequency [64].

Multilevel PWM uses '*N*' number of triangular carrier signals, which can be modified in phase in order to reduce the output voltage harmonic content. The l^{th} carrier is phase shifted by an angle equal to $2(l-1)\pi / N$ in this modulation. By comparing a sinusoidal reference waveform with the '*N*' carrier waveforms, the firing signals are generated for the '*N*' sub-modules in the multi-valve. Each transition in the multilevel output from one level to next level can be determined corresponding to the respective phase shift in modulating signal and carrier [64], [66].

Figure 3-4(a) shows the modulation signal and two phase shifted carrier signals for a 6 sub-modules per multi-valve case. In this example, the modulation frequency index is equal to 3; hence each cell is switched at a low switching frequency of 180Hz for a fundamental frequency of 60Hz. Consequently, the effective switching frequency per phase leg becomes 2.28 kHz (2*6*180) for 6 sub-modules per multi-valve case. For the carrier waveforms in Figure 3-4(a), the resultant sub-modules' output voltage waveforms are shown in Figure 3-4(b and c). In Figure 3-4(d), the converter output waveform generated by carrier phase-shifted sinusoidal PWM is presented. This modulation technique produces an even duty cycle for each sub-module.

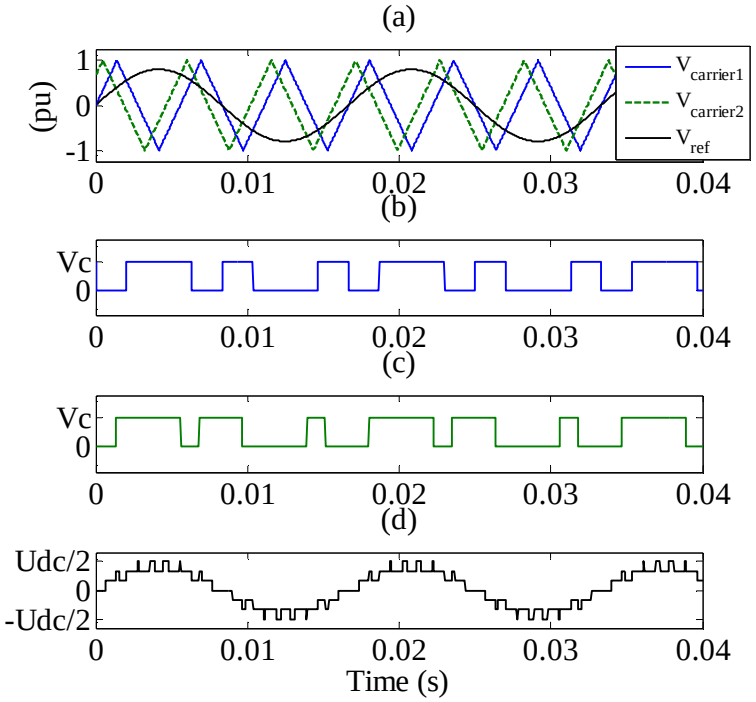


Figure 3-4: Carrier phase shifted multilevel SPWM waveforms:

(a) Sinusoidal reference and carrier, (b & c) Sub-module output voltages, and (d) MMC output voltage

With the above waveform synthesis methods, the full dc bus voltage appears across the all 'ON' state *(N_u + N_l = N)* sub-modules. Hence, since all capacitor voltages are required to be the same, each must be equal to [51], [62]:

$$V_c = U_{dc} / N \qquad \textbf{3-4}$$

where, *N* is the total number of sub-modules in a multi-valve.

Therefore, with an increased number of sub-modules in a multi-valve, each capacitor uses a small fraction of the dc bus voltage. Thus, a large sub-module count can reduce the device ratings of the sub-module. Even with low voltage rating switching devices, the

converter is capable of handling very large voltages, in the range of several hundred kilo-Volts [60].

The "nearest level estimation" based approach produces waveforms with an acceptable amount of harmonics content when a suitable number of MMC levels are employed as will be exemplified in section 3.5.2. It is the least computational complex method of the aforementioned techniques and thus is mainly considered for simulations in this thesis.

3.4 Capacitor Voltage Balancing

From Figure 3-2, it is evident that when the sub-module is 'ON', the capacitor, C has an increasing voltage if the module current is positive. It has a decreasing voltage if the current is negative. The capacitor voltage remains unchanged when the sub-module is 'OFF'. Note that the output waveform synthesis algorithm in section 3.3 merely states that there are N_u and N_l sub-modules 'ON' in the upper and lower multi-valves at any instant. If all the capacitor voltages remain constant during the converter operation, N_u and N_l sub-modules can be arbitrarily selected from the upper and lower multi-valves. However, the 'OFF' sub-modules maintain constant capacitor voltages, whereas the 'ON' sub-modules experience an increase or decrease of their capacitor voltages depending on the current direction. To maintain all capacitors at a common voltage, a capacitor voltage balancing control mechanism is required.

The objective of this capacitor voltage balancing controller is to generate firing pulses for each sub-module to maintain the sub-module's capacitor voltage at a constant value

as given in Equation (3-4). One of the commonly used capacitor voltage balancing algorithms, proposed for the MMC operation based on ranking of capacitor voltage values [62] is discussed below.

3.4.1 Capacitor Voltages Ranking Based Approach

The block diagram of the capacitor voltage balancing control algorithm for the MMC is shown in Figure 3-5 [62].

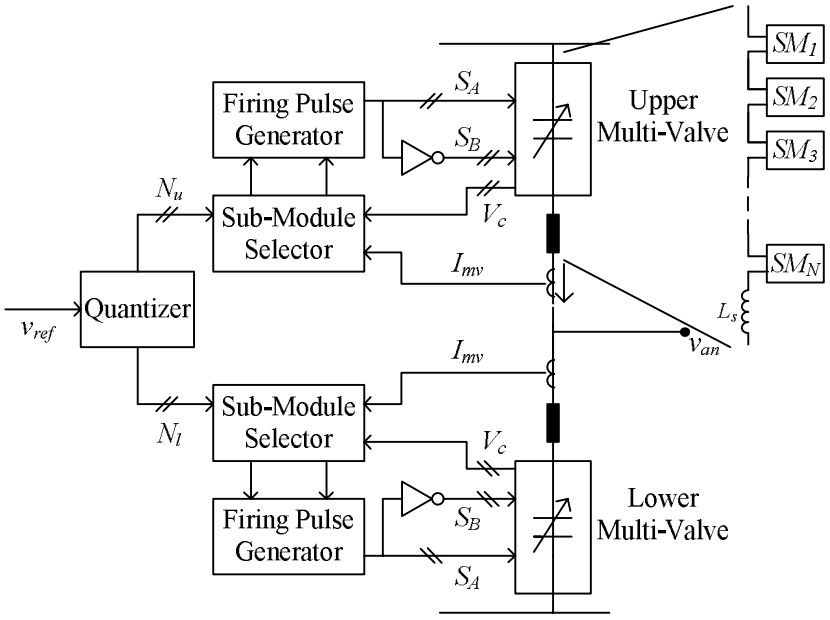


Figure 3-5: Firing pulse control unit of MMC

As discussed in section 3.3, the total number of 'ON' state sub-modules is varied from 0 to N (N is the total number of sub-modules in a multi-valve) during one cycle generation of the converter output voltage waveform. Therefore for a specified number of 'ON' state sub-modules in a multi-valve, there are different switching combinations which are referred to as 'redundant switch states'. In a modular multilevel converter, the

redundant switch states are groups of switch states that produce the same phase voltage, providing all the capacitor voltages are equal in magnitude. As shown in Figure 3-5, when the 'Quantizer' demands the required number of 'ON' state sub-modules to the 'Sub-Module Selector', the duty of this unit is to select the most suitable candidate sub-modules from the multi-valve for turn 'ON' and turn 'OFF'. The property, being used by the 'Sub-Module Selector' for capacitor voltage balancing approach is discussed below.

The sub-module selector measures the capacitor voltages of each sub-module in the multi-valve and creates a table for each multi-valve by ranking capacitors in order of increasing voltages. This sorted table is referred to when there is a step change in quantizer's output waveform. Consider that there are N_u number of 'ON' state sub-modules in the upper multi-valve. If the current, I_{hb} is positive (in Figure 3-2:), these sub-modules experience an increase in their capacitor voltages. Therefore at the next turn on opportunity, the sub-module at the bottom of the sorted list (*i.e.* with lowest voltages) is selected in order to allow an increase in its capacitor voltage. When the current, I_{hb} is negative, the highest charged capacitors are selected from the sorted array hence their voltages can be decreased. This process is invoked at each time a new switching is requested, (*i.e.* for each step of the quantized waveform N_u). Also, the same capacitor voltage equalising principal can be applied for the lower multi-valve as well.

The capacitor voltages of sub-modules can be controlled in a narrow band by applying this methodology for all three phases [7].

3.4.2 Capacitor Voltage Balancing Using Multilevel PWM

The carrier phase shifted multilevel PWM technique can also be used to balance the sub-module capacitor voltages by adjusting the phase of the carrier [67]. Generally, the carrier phase shifted multilevel PWM technique creates a more regular dc side voltage compared to the capacitor voltage ranking based method and hence produces an ac voltage waveform with lower harmonics [68]. However, the computation complexity of carrier phase shifted multilevel PWM is higher than the capacitor voltage ranking based approach.

3.5 Operational Aspects of Modular Multilevel Converter

In this section, some of the basic operational aspects of the MMC are discussed using a performance analysis of the converter by simulating the converter in the PSCAD/EMTDC program [14]. The converter is simulated as an inverter. A constant dc source is connected to the dc side of the converter and ac terminal connects to an inductive load.

3.5.1 Generating Multilevel AC Waveform

In this study, one phase of the MMC is simulated for different number of sub-modules (*i.e.*: *N* changed from 2 to 96) in the converter. A schematic diagram of single phase MMC circuit with '*N*' number of sub-modules is shown in Figure 3-6. The internal

controllers of the converters are used for capacitor voltage balancing and generation of firing signals as discussed in section 3.4.1.

In these simulations, the converter ac terminal is connected to a fixed R-L load of 50 MW+40 Mvar. A constant dc voltage source of magnitude equal to 240 kV is connected at the dc bus. For these rated conditions, a constant per unit capacitance (250 ms) is chosen for the module capacitors. It is noted that the per unitization of the capacitance is described in section 3.5.4.

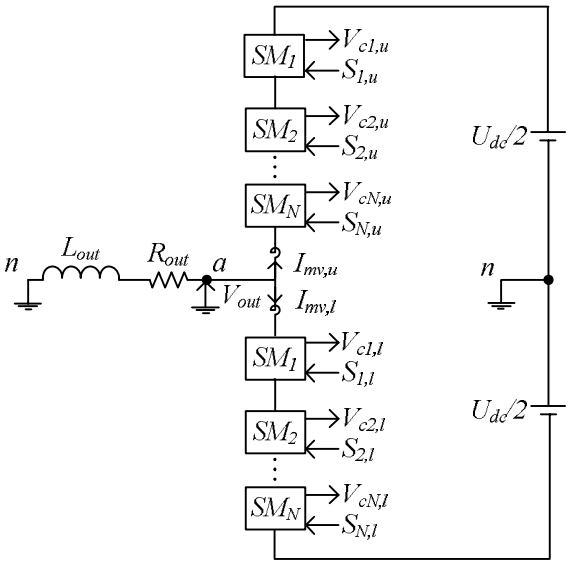


Figure 3-6: Single phase MMC converter

Figure 3-7(a) shows the reference sinusoidal waveform, and each subsequent graph (from (b) to (g)) is for converter with different number of sub-modules.

The step changes of output voltages can be clearly visible up to 24 levels. For converters with a large number of sub-modules, the waveform is essentially sinusoidal and closely follows the reference waveform. Therefore, these simulation results are

evidence that the filtering requirement for terminal ac waveform of MMC is minimal or can operate even without ac filters.

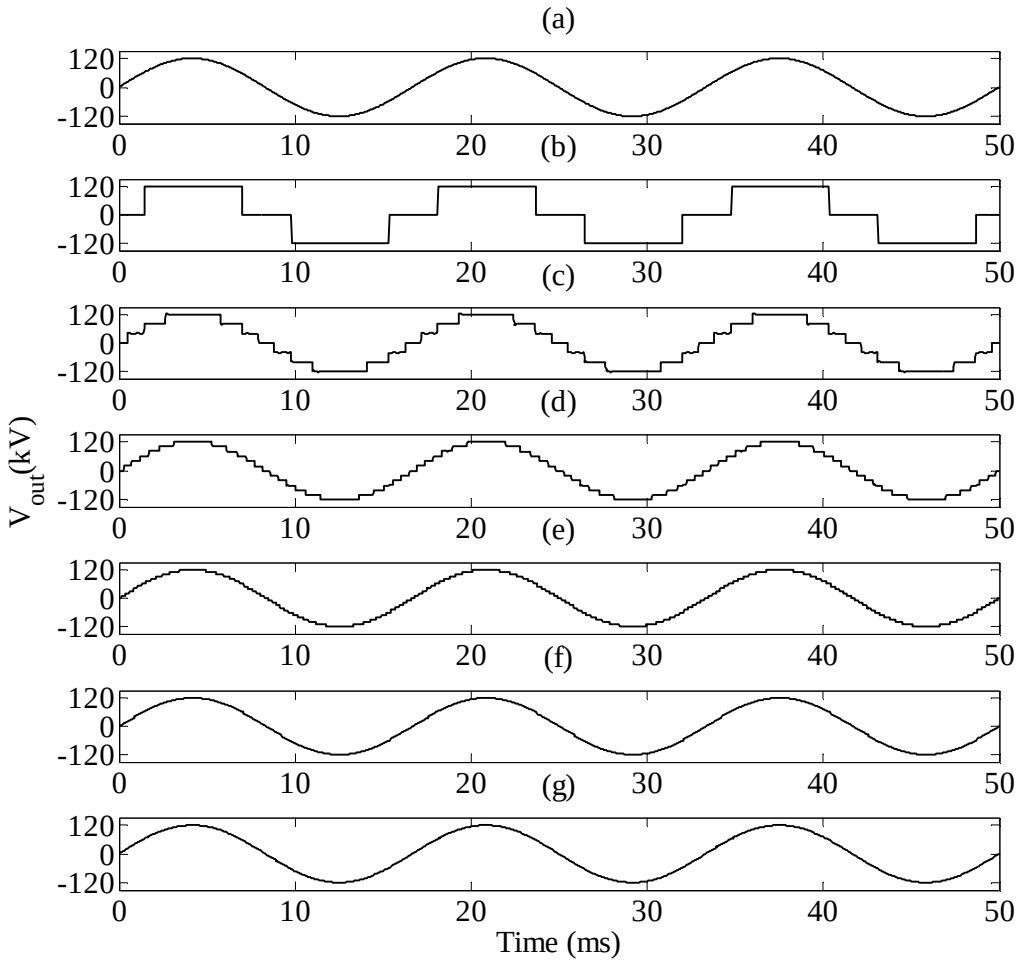


Figure 3-7: MMC ac output waveforms:

(a) Sinusoidal reference waveform and output voltage waveforms for (b) 2, (c) 6, (d) 12, (e) 24, (f) 48, and (g) 96 sub-modules per multi-valve

3.5.2 Harmonics Analysis of Output AC Waveform

In this section, the harmonic contents for MMC output voltage waveforms are analyzed using two indices recommended by IEEE 519 Standard [69];

1. Individual harmonic distortion (D_n): magnitude of the n^{th} harmonic as a percentage of the fundamental.
2. Total harmonic distortion (THD): root mean square of all harmonics, expressed as a percentage of the fundamental

A commonly used limits recommended by IEEE 519 Standard for these in HVDC systems are D_n less than 1% for each harmonic, and THD less than 2%, considering all harmonics up to the 50^{th} [69].

Figure 3-8 shows the maximum D_n and THD values for the MMC output waveforms generated using "nearest level estimation" and "multilevel PWM" methods as discussed in section 3.3, with the above thresholds indicated, as the number of sub-modules per multi-valve is increased. The harmonic analysis is done by circulating a Fourier analysis of the idealised stepped waveforms.

When the nearest level estimation approach is used, all harmonic limits are satisfied with more than 22 sub-modules per multi-valve. The MMC with this number of sub-modules can therefore be operated without any ac filters, which is a significant advantage. Actual MMC installations use a larger number of modules, because they operate at high dc voltages and the additional modules reduce the voltage stress per module.

When using the multilevel PWM approach, the harmonic limits are satisfied with 22 sub-modules per multi-valve for 300 Hz carrier frequency and 25 sub-modules for 180 Hz. However, with a smaller number of sub-modules, the THD and maximum D_n values for multilevel PWM are significantly larger compared with that of the nearest level

estimation approach. Comparing harmonic indices generated using the PWM approach for two carrier frequencies; 180Hz and 300Hz, it is clear that the harmonics can be lower with a higher switching frequency. Even though, the carrier frequency is generally selected to be lower, the value should be chosen as a trade-off between the typical restrictions on harmonic injection into the grid and the converter losses as higher switching frequency indeed increases the switching losses of the converter.

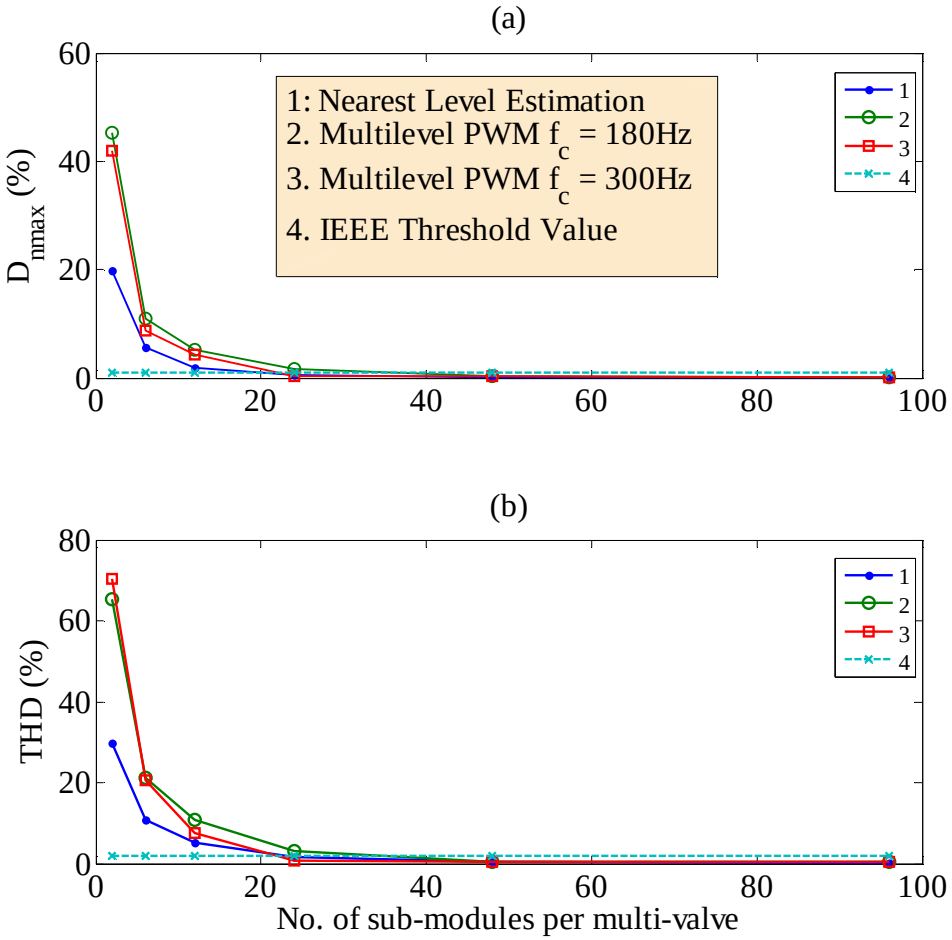


Figure 3-8: Harmonic analysis of MMC output waveforms:

(a) Maximum individual harmonic and (b) THD variations with no. of sub-modules

3.5.3 Performance of Capacitor Voltage Balancing

In this section, the performance of capacitor voltage balancing controller, described in section 3.4.1, is presented by disabling and enabling the control operation for different time intervals. First, the controller is disabled at 0.5 s. Capacitor voltages start to diverge from their nominal value. The capacitor voltages of two sub-modules that show the widest deviations are shown in Figure 3-9(a). These deviations are caused by the different capacitor conduction (charging or discharging) intervals which depend on the sub-module's duty cycle. The sub-modules having the longest 'ON' period either overcharge or undercharge based on the current direction.

However, when the balancing controller is re-enabled at 1.5s, the capacitor voltages are quickly restored to their nominal values. The corresponding converter output voltage waveforms around the 1.33s mark with capacitor voltage balancing disabled, and at the 2.2s mark with voltage balancing enabled are shown in Figure 3-9(b). In this simulation, there are 12 sub-modules in a multi-valve. The above results show that the voltage balancing controller is rapidly able to equalize the capacitor voltages.

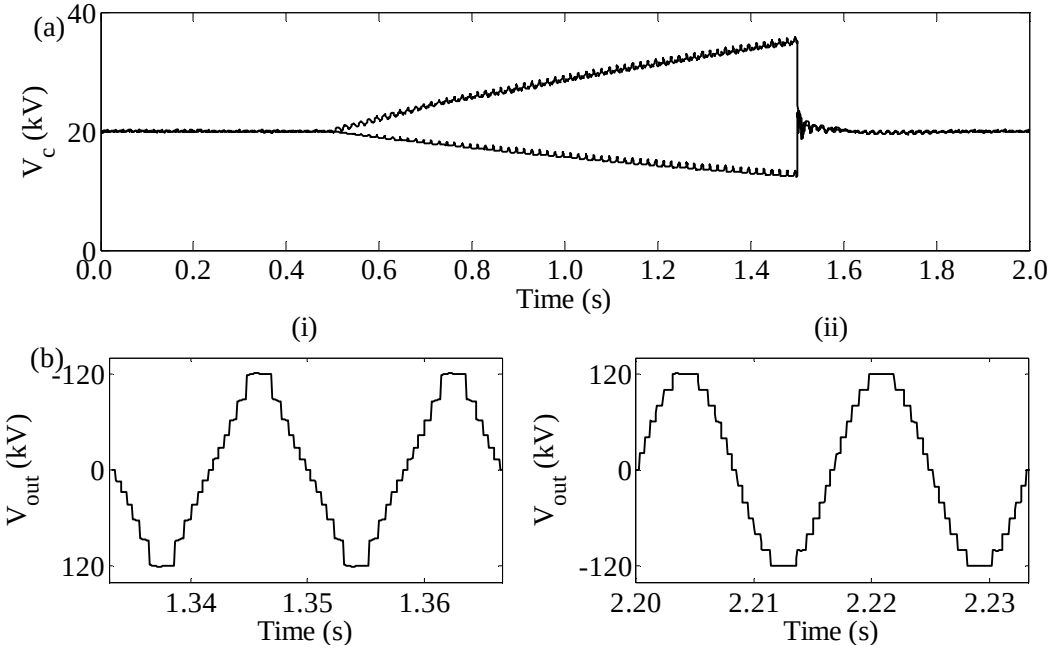


Figure 3-9: Performance of capacitor voltage balancing algorithm:

(a) Capacitor voltages of 2 candidate sub-modules, and (b) MMC output voltage (i) without and (ii) with voltage balancing in operation.

3.5.4 Impact of Capacitor Size on Performance

A smaller size of the sub-module capacitance results in more dc side ripple voltage. If the ripple is too large, it can significantly distort the ac side voltage waveform and eventually makes an unequal power flow in the converter legs [51], [70]. The voltage ripples can be minimized by increasing the module capacitor value. On the other hand, large capacitance makes lower voltage ripples and thus slower response to active power control. The cell capacitance is selected to meet with the permissible voltage ripple requirement as well as to achieve significantly fast responses for power control [71].

The sub-module capacitance can be estimated as given in Equation (3-5) [71].

$$C = \frac{2\,C_{pu}\sqrt{P_c^{\,2} + Q_c^{\,2}}}{6\,N\,V_c^{\,2}} \qquad \textbf{3-5}$$

Here C_{pu} is the per-unitized capacitor size which is customary expressed as the total capacitor energy stored at rated dc voltage for all capacitors in the converter, to the complex power rating (kJ/MVA or milliseconds) of the converter. P_c and Q_c are the converter's rated real power and reactive power, N is the number of sub-modules per multi-valve and V_c is the nominal value of sub-module voltage. The number 6 in Equation (3-5) arises from the fact that there are 6 multi-valves with N sub-modules per valve in a three phase converter [71].

Typically, the sub-module capacitor value is chosen in order to keep the capacitor voltage fluctuations within a range of ±10% [72]. Figure 3-10 shows the variation of a typical sub-module capacitor voltage depending on the size of the capacitance used. In this test, the energy stored in sub-module capacitor is varied in the range of 10–60 kJ/MVA. V_c is equal to 40 kV, P_c is 150 MW, Q_c is 120 Mvar, and N is equal to 12. The calculated capacitance values (C) for the selected range of C_{pu} values are shown in Table 3-1.

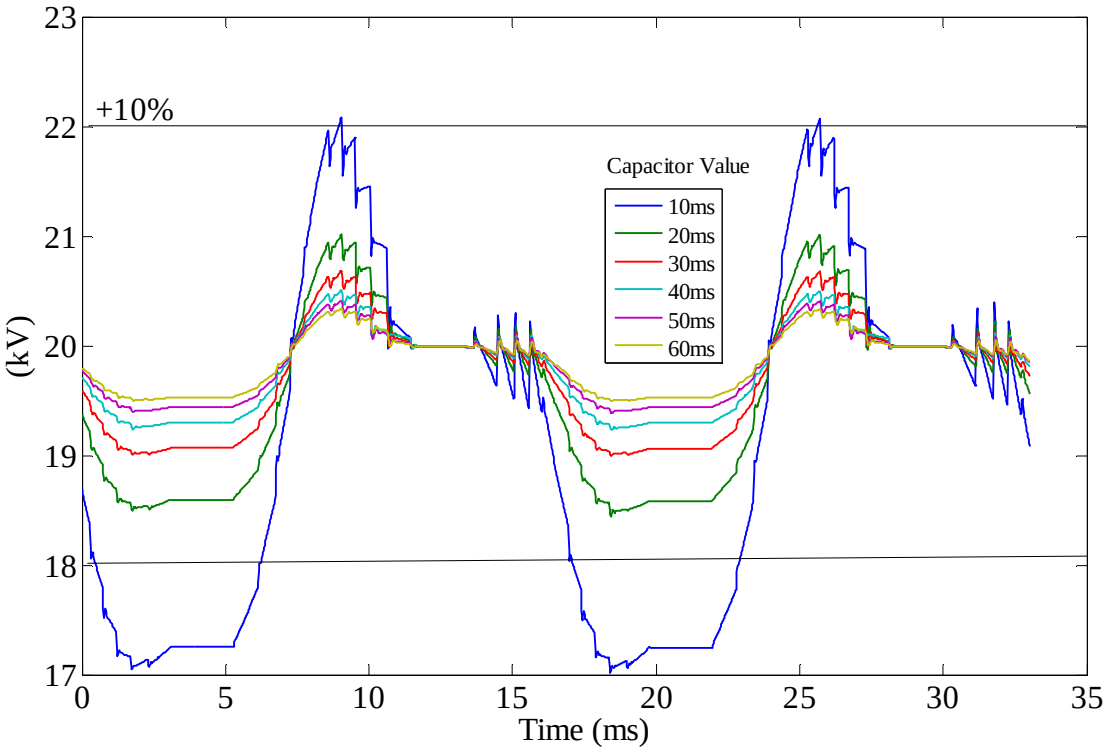


Figure 3-10: Average capacitor voltage fluctuation for different sub-module capacitance values

Table 3-1: Calculation of capacitance values

C_{pu} (kJ/MVA or ms)	Capacitance, C (μF)
10	133
20	267
30	400
40	534
50	667
60	800

The resulting ac output voltage for different sub-module capacitance values (from 10 ms to 60 ms) for a thirteen-level MMC is shown in Figure 3-11. For a capacitance

value of 30 ms or larger (Figure 3-11(c-e)), the waveform is essentially the same. However, capacitance values smaller than 30 ms (Figure 3-11(a-b)) introduce distortion. From the results of this typical example (Figure 3-10 & Figure 3-11), it can be concluded that the sub-module capacitor energy storage requirement should be larger than 30 ms. By referring to Table 3-1, the minimum capacitance is chosen to be 400 μF for this example case.

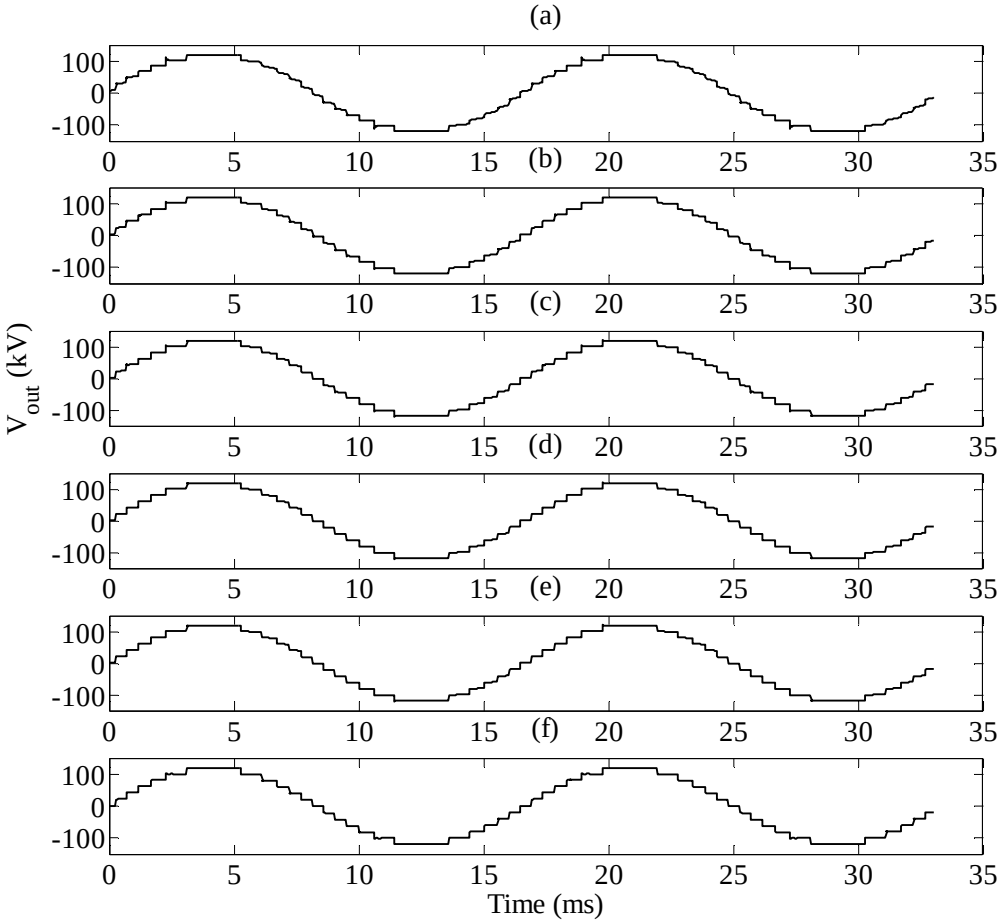


Figure 3-11: Output voltage waveforms for different capacitance values:

(a) 10 ms, (b) 20 ms, (c) 30 ms, (d) 40 ms, (e) 50 ms, & (f) 60 ms (Note: Slope in steps for C_{pu}<30 ms)

3.5.5 Harmonic Suppression of Arm Circulating Current

Since the three phase units of MMC are in parallel connection on the dc side, the inequality of the three generated dc voltages lead to a balancing current among the individual phase units. Using an explicit analytical approach, it is found that harmonic contents exist in the arm circulating currents as in the form of even multiples of fundamental frequency component and a dc component [73]. It is further found that the second order harmonic has the largest magnitude in the circulating current. If the second order harmonic component is not suppressed it will increase the losses and current rating requirements of the converter [72].

One of the options to reduce this second order harmonic component is by means of control of the arm voltages [74]. This will however add an extra complexity to the MMC internal control systems and will cause a reduction of the maximum output voltage by limiting the allowable room for control actions. Another option is to insert a tuned filter to mitigate the second order harmonic significantly. This hardware option is simple to implement as it does not require any controller modifications and hence is also commonly used [72]. The drawback of this method is that adding extra components into the converter (high voltage inductors and capacitors) increases the converter cost [74].

Due to the simplicity in the controls, a tuned filter is used to suppress the second harmonic component of the circulating current in this thesis.

1. Filter Parameters Calculation

When the filter is inserted into the circuit, the valve reactor (L_s) should be connected in series with filter inductor (L_f) as shown in Figure 3-12. Therefore, L_s and L_f collectively

contribute to the total phase inductance of the multi-valve. Typically, the inductor value is chosen to be 10~15% of the system impedance [72], [75]. The filter inductors are connected in parallel with a filter capacitor (C_f). The capacitance value is chosen such that the second order harmonic in the circulating current is blocked. The filter capacitance is then given as in Equation (3-6).

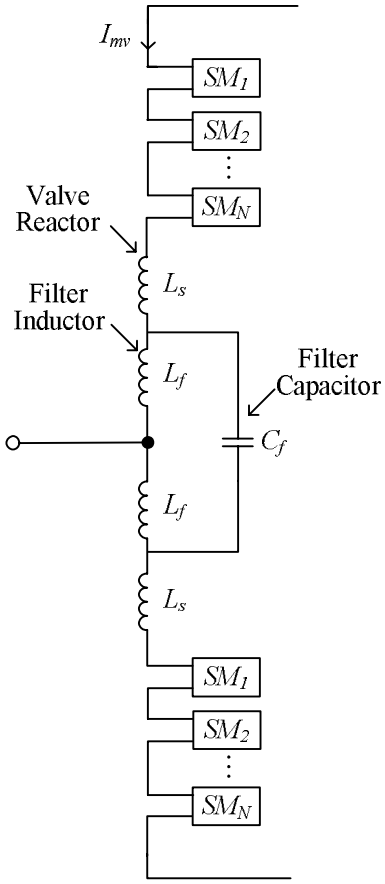


Figure 3-12: Second harmonic eliminating filter

$$C_f = \frac{1}{\left(2\omega_0\right)^2 \left(2L_f\right)} \qquad \textbf{3-6}$$

Here, $2L_f$ is the inductance of the filter and ω_0 is the fundamental angular frequency.

This size of the filter inductance can then be expressed as a fraction (p) of the total multi-valve inductance as in Equation (3-7)

$$p = \frac{L_f}{\left(L_f + L_s\right)} = \frac{L_f}{L_{TOT}} \qquad \textbf{3-7}$$

$$\text{where, } L_{TOT} = \text{Total multi-valve inductance}$$

Since L_{TOT} is a constant, the filter parameters (L_f and C_f) and valve reactor (L_s) can be expressed as a function of p.

$$\begin{aligned} L_s &= (1-p)L_{TOT} \\ L_f &= pL_{TOT} \\ C_f &= \frac{1}{8\omega_0^{\,2} pL_{TOT}} \end{aligned} \qquad \textbf{3-8}$$

2. Filter Performance Analysis

Table 3-2 summarizes the harmonic content of the multi-valve current without a filter and with a filter for several values of p. In this test, the load impedance is chosen to be $95.239\angle 42°\Omega$ and total multi-valve inductance is set to 10% of the load impedance. A constant dc voltage source of magnitude equal to 240 kV is connected at the dc bus and there are 12 sub-modules in a multi-valve.

Table 3-2 shows that when the second harmonic filter is not included, the magnitude of the second harmonic component of the multi-valve current is about more than 70% of the total current. Generally, the larger the value of p (i.e. larger filter inductance), the smaller the harmonic content as seen in Table 3-2. The only anomaly is for p = 0.9, where the second harmonic tends to increase.

Having a larger portion of the inductance in the filter, can reduce the size of the filter capacitance and hence, the cost. A drawback with using a high value of *p* is, however, a reduced damping of high frequency components. Therefore, the impact on higher order harmonics must also be considered to determine filter parameters. Failing to take this effect into consideration may render unacceptable operating conditions resulting in increased losses and current rating requirements [76].

Table 3-2: Harmonic content of the multi-valve current without a filter and with a filter for several filter parameters

p	Filter Parameters			$\sqrt{\sum_{h=2}^{31}(I_h)^2}$ (A)	$\lvert I_1 \rvert$ (A)	$\lvert I_2 \rvert$ (A)
	L_s (mH)	L_f (mH)	C_f (µF)			
No filter	2.526	0.000	∞	0.4637	0.6316	0.46201
0.35	1.642	0.884	994.824	0.0276	0.6306	0.00073
0.50	1.263	1.263	696.377	0.0334	0.6310	0.00052
0.65	0.884	1.642	535.675	0.1230	0.6305	0.00003
0.90	0.253	2.273	386.876	0.0896	0.6308	0.00161

Figure 3-13 shows the waveforms of upper multi-valve current and a typical capacitor voltage of a sub-module when the filter is not inserted to MMC. The multi-valve current and the capacitor voltages when the second harmonic current suppression filter is inserted are shown in Figure 3-14.

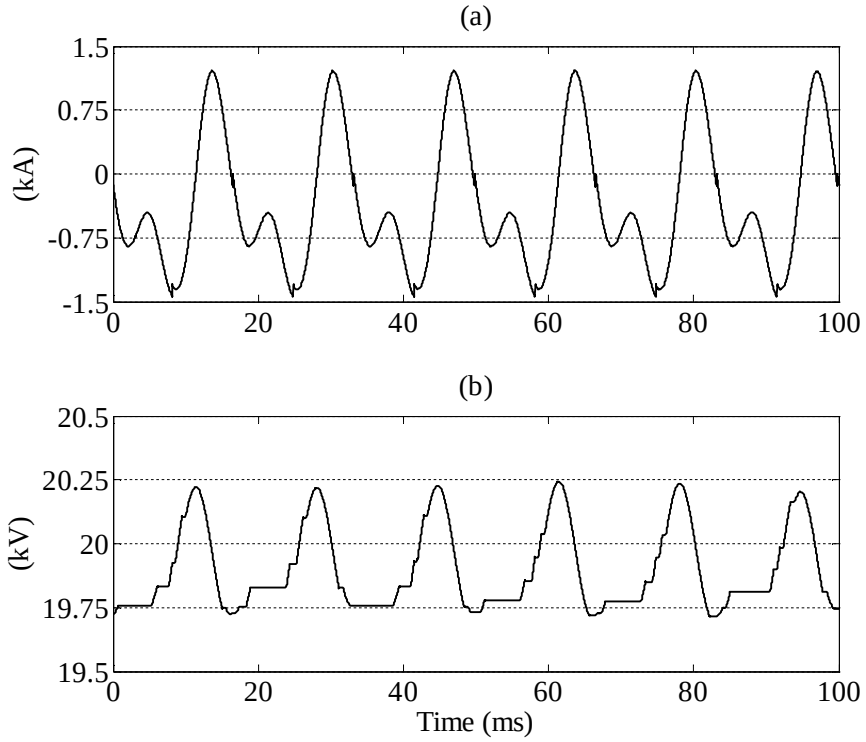


Figure 3-13: MMC output waveforms without second order current harmonic filter: (a) Multi-valve current and (b) Sub-module capacitor voltage.

When the filter is inserted, the distortion of the multi-valve current disappears as the filter intentionally mitigates the most of current harmonics. Consequently, the capacitor voltage ripple is also decreased by more than 50% of that when the filter is not in operation. In this example, the filter parameters are chosen for $p = 0.35$.

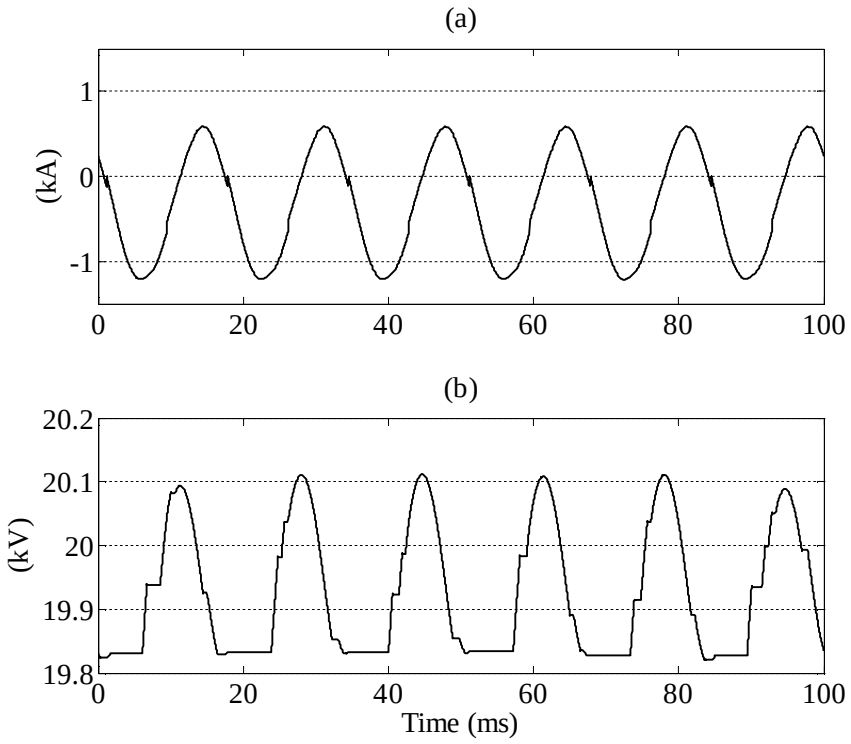


Figure 3-14: (a) MMC output waveforms with second order current harmonic filter: (a) Multi-valve current and (b) Sub-module capacitor voltage.

Modeling of Modular Multilevel Converter on Electromagnetic Transients Programs

4.1 Introduction

A large sub-module count is used in MMC based high voltage, high power applications in order to minimize the harmonic content of the converter output voltage waveform and to reduce the voltage rating of individual sub-module [77]. Therefore, the MMC has a very large number of switch elements. In half-bridge sub-module converters, each of the *N* sub-modules of the 6 multi-valves in a three phase MMC contains 2 switch elements, giving a total of 12*N* switches per converter. With 100 sub-modules per multi-valve, this gives 1200 switches per converter. This number is doubled when the full-bridge sub-modules are used in the converter.

However, the large number of switching elements in the MMC introduces a challenge for modeling the converter on EMT simulation programs. To properly model the switching operation, the admittance matrix which has a size equal to the total number of

nodes in the network subsystem, must be inverted (in reality re-triangularized, which is computationally more efficient) every time a switch operates. As each connection between the MMC switch elements is one node, the resulting matrix size would be in the thousands, making the inversion task extremely slow. Hence, the traditional approach of MMC simulation would not be practical.

To overcome the computational effort of MMC simulation in EMT simulation programs, this thesis develops an efficient model for the converter using the method of Nested Fast and Simultaneous Solution [78]. It partitions the solution into two parts, with the external network solution being implemented in the main EMT solver. Each phase of the MMC is interfaced as a specially designed Thévenin equivalent, thereby greatly reducing the number of nodes. The MMC is solved separately in an efficient manner, by exploiting its simple topology.

The main contribution of this thesis, the efficient modeling of MMC for EMT type simulations, is presented in this chapter.

4.2 Traditional Admittance Matrix Solution for Modular Multilevel Converter

Using Dommel's algorithm each dynamic element in the electrical system can be modeled as a Norton equivalent current source in parallel with a conductance through the application of trapezoidal integration [79]. The current source is updated each time-step and is a function of the history of the network in earlier time-steps.

4.2.1 Conductance Matrix Formation

Using this trapezoidal rule integration method, the capacitor can be represented as an equivalent current source I_{Ceq}, and a conductance g_C, as shown in Figure 4-1 and the values of I_{Ceq} and g_C are determined using Equation (4-1) [79].

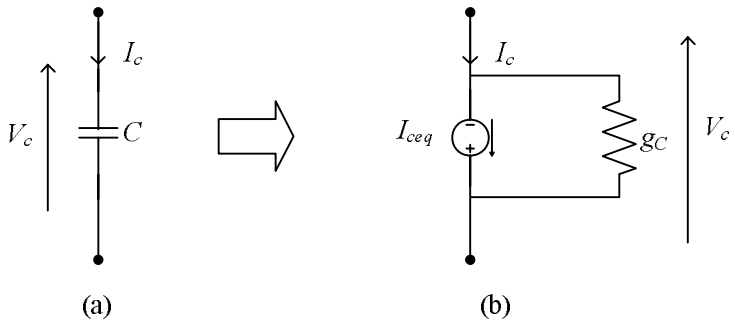


Figure 4-1: Capacitor equivalent impedance circuit

$$g_C = \frac{2C}{\Delta T}$$
$$I_{ceq}(t-\Delta T) = -\left(g_C V_c(t-\Delta T) + I_c(t-\Delta T)\right) \quad \textbf{4-1}$$

It is noted that $I_{ceq}(t\text{-}\Delta T)$ is known at time t from the capacitor current and voltage values at time $(t\text{-}\Delta T)$ (in the previous time-step). Since the parallel connection of an IGBT and a diode acts as a bi-directional switch, only one device is conducting at any instant of time. Therefore, the IGBT/diode pair is still considered as a single resistive element which can have one of the two values corresponds to the 'ON' or 'OFF' states. This simple representation is sufficiently accurate to simulate the system level electrical behavior [80]. Using the resistive representation of switching elements, the equivalent impedance circuit for the IGBT/diode switch combination can be obtained as shown in

Figure 4-2. g_T is the conductance of IGBT-*T*, g_D is the conductance of diode-*D*, and the total conductance of the switch combination is g_T'.

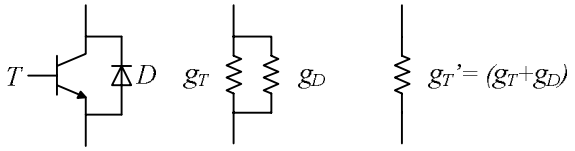


Figure 4-2: IGBT/diode switch equivalent impedance circuit

The value of conductance, g_T depends on the IGBT switch state and is either the 'ON' state conductance, g_{T_ON} or the 'OFF' state conductance, g_{T_OFF} at any instant in time. Similarly, the value of g_D is either the diode 'ON' state conductance, g_{D_ON} or the 'OFF' state conductance, g_{D_OFF} as given in Equation (4-2).

$$g_T(t) = \begin{cases} g_{T\_ON} \text{..... if } IGBT\text{-ON} \\ g_{T\_OFF} \text{.....if } IGBT\text{-OFF} \end{cases} \quad \text{and} \quad g_D(t) = \begin{cases} g_{D\_ON} \text{..... if } Diode\text{-ON} \\ g_{D\_OFF} \text{.....if } Diode\text{-OFF} \end{cases} \qquad \textbf{4-2}$$

With these steps, an equivalent conductance (or admittance) circuit for an MMC sub-module can be derived as shown in Figure 4-3.

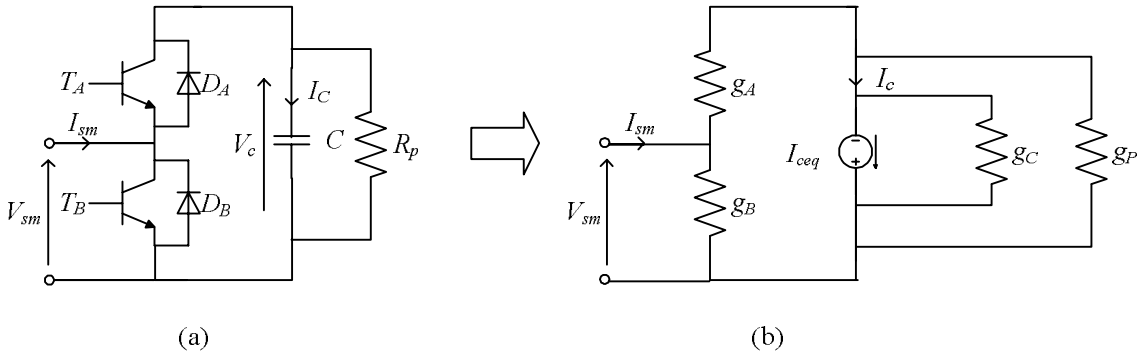


Figure 4-3: Sub-module equivalent conductance circuit

Depending on three possible switch states, the conductance, g_A (and g_B) can have a value as given by Equation (4-3). The conductance g_P can be determined using the value of capacitor loss resistance.

$$g_A(t)=\begin{cases} g_{T\_ON}+g_{D\_OFF} \text{ ..... if } T_A\text{-ON, } D_A\text{-OFF} \\ g_{T\_OFF}+g_{D\_ON} \text{ .....if } T_A\text{-OFF, } D_A\text{-ON} \\ g_{T\_OFF}+g_{D\_OFF} \text{ .....if } T_A\text{-OFF, } D_A\text{-OFF} \end{cases} \quad \& \; g_B(t)=\begin{cases} g_{T\_ON}+g_{D\_OFF} \text{ ..... if } T_B\text{-ON, } D_B\text{-OFF} \\ g_{T\_OFF}+g_{D\_ON} \text{ .....if } T_B\text{-OFF, } D_B\text{-ON} \\ g_{T\_OFF}+g_{D\_OFF} \text{ .....if } T_B\text{-OFF, } D_B\text{-OFF} \end{cases} \qquad \textbf{4-3}$$

As the sub-modules in a multi-valve have a daisy-chain structure, an equivalent conductance circuit for this structure is easily derived by stringing the sub-module equivalent conductance circuits as shown in Figure 4-4.

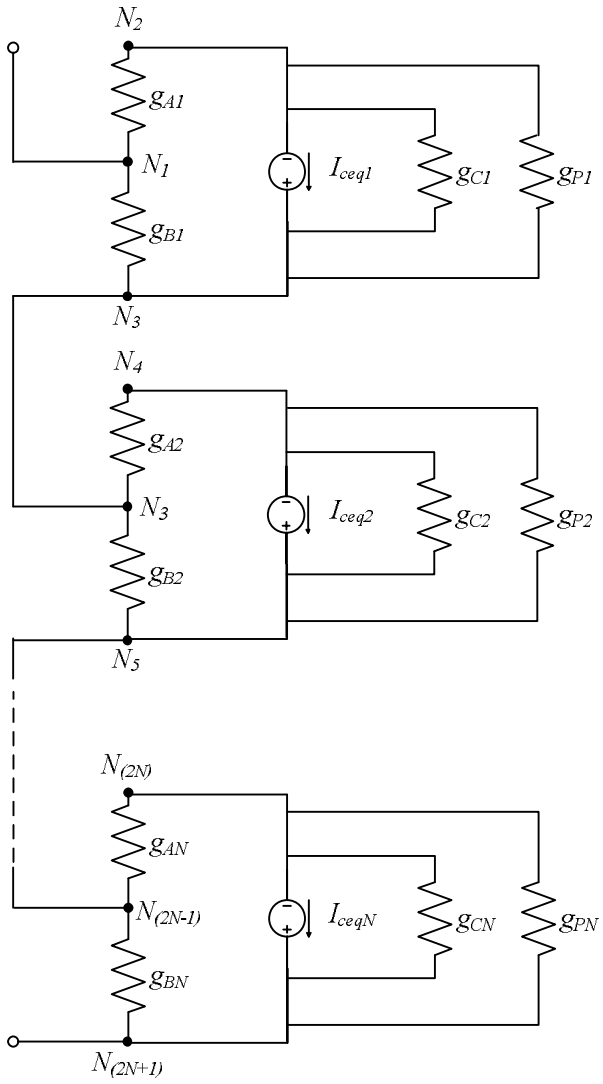


Figure 4-4: Multi-valve equivalent conductance circuit

Using the equivalent conductance circuit shown in Figure 4-4 the corresponding nodal conductance matrix for the multi-valve can be formed as given in Equation (4-4). The number of rows and columns of the resultant nodal conductance matrix is each equal to the number of nodes in the network. The circuit shown in Figure 4-4 has $(2N+1)$ nodes hence, the number of rows and columns of the resultant nodal conductance matrix is each equal to $(2N+1)$, where N is the number of sub-modules in a multi-valve. When modeling

a three-phase MMC for high voltage, high power applications which typically have a large sub-module count, the size of the resultant nodal conductance matrix becomes very large.

$$G=\begin{bmatrix} g_{A1}+g_{B1} & -g_{A1} & -g_{B1} & 0 & .. & .. & 0 \\ -g_{A1} & g_{A1}+g_{C1}+g_{P1} & -(g_{C1}+g_{P1}) & 0 & .. & .. & 0 \\ g_{B1} & -(g_{C1}+g_{P1}) & g_{B1}+g_{C1}+g_{P1}+g_{A2}+g_{B2} & -g_{A2} & -g_{B2} & .. & 0 \\ 0 & 0 & -g_{A2} & g_{A2}+g_{C2}+g_{P2} & -(g_{C2}+g_{P2}) & .. & 0 \\ .. & .. & .. & .. & .. & .. & .. \\ 0 & 0 & 0 & .. & .. & .. & .. \\ 0 & 0 & 0 & .. & .. & .. & g_{BN}+g_{CN}+g_{PN} \end{bmatrix} \quad \textbf{4-4}$$

Similar to the nodal conductance formation, the column vectors of node voltages and branch currents can be obtained for the circuit shown in Figure 4-4 as given in Equation (4-5).

$$\underline{V}(t)=\begin{bmatrix} V_1(t) \\ V_2(t) \\ V_3(t) \\ \vdots \\ \vdots \\ V_{2N}(t) \\ V_{(2N+1)}(t) \end{bmatrix}_{(2N+1)\times 1} \qquad \underline{I}(t-\Delta T)=\begin{bmatrix} 0 \\ -I_{ceq1}(t-\Delta T) \\ I_{ceq1}(t-\Delta T) \\ \vdots \\ \vdots \\ -I_{ceqN}(t-\Delta T) \\ I_{ceqN}(t-\Delta T) \end{bmatrix}_{(2N+1)\times 1} \quad \textbf{4-5}$$

$\underline{V}(t)$ is the unknown node voltages at time t. $\underline{I}(t-\Delta T)$ is a known equivalent current source vector of sub-module capacitors which are functions of the past history of the network.

4.2.2 Nodal Equations Based Solution

With all the elements in the multi-valve represented by current source-conductance equivalents, the admittance matrix equations are readily written, resulting in an equation of the form given in Equation (4-6)

$$[G]\cdot\left[\underline{V}(t)\right]=\left[\underline{I}(t-\Delta T)\right] \quad \textbf{4-6}$$

Using this approach, the system equations can be reduced to a set of simultaneous linear algebraic equations that describe the state of the system. From Equation (4-6), the unknown node voltages can be readily calculated as given in Equation (4-7);

$$\left[\underline{V}(t)\right]=[G]^{-1}\cdot\left[\underline{I}(t-\Delta T)\right] \quad \textbf{4-7}$$

In EMT simulation programs which use the above approach, the node voltages calculation is conducted in every solution time-step and the history current terms are updated accordingly. As long as the conductance matrix [*G*] remains unchanged, it is not required to invert the conductance matrix in each time-step as the initially inverted solution of [*G*] matrix can be used in subsequent time-steps.

For large sparse systems such as those which occur in many network problems, matrix inversion is very inefficient for computing direct solutions. By means of an appropriately ordered triangular decomposition, the inverse of a sparse matrix expressed as a product of sparse matrix factors thereby gaining a significant advantage in speed. With this method, direct solutions are computed for sparse matrix factors instead of a full matrix. Optimally ordered triangular factorization of sparse matrices is more efficient and offers computational advantages in some applications [81].

When forming the conductance matrix, nodes with switches connected are arranged at the bottom. Then, the triangular factorization is carried out only for nodes without switches (upper part of triangular matrix). This also yields a reduced matrix for the nodes with switches. Whenever a switch position changes, this reduced matrix is first modified to reflect the actual switch positions as shown in Figure 4-5. Then, the triangular factorization is completed (lower part of triangular matrix) [79].

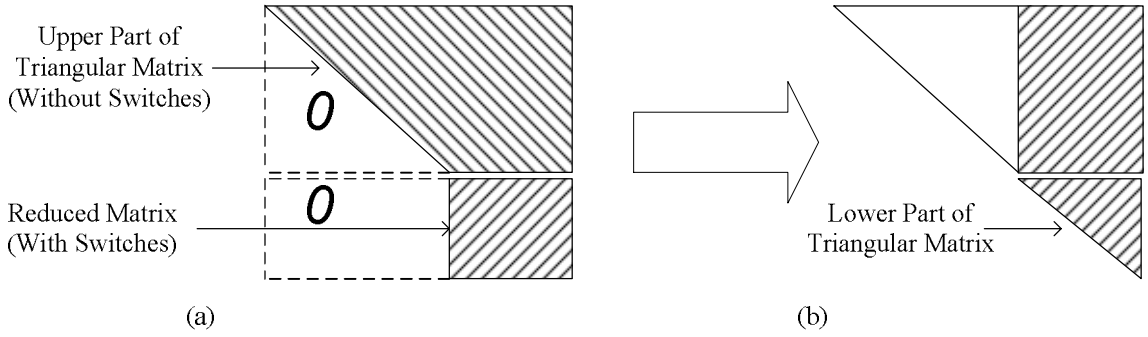


Figure 4-5: Triangular matrix computation with switching devices:

(a) Initial matrix formation and (b) After each switch operation.

These traditional approaches are being employed in most EMT simulation programs for efficiently computing for solving linear systems of equations without explicit inversion.

However even with the above advanced methods, the large number of switching elements in the MMC introduces a challenge in modeling the converter in EMT simulation programs especially in three-phase systems. To properly model the switching operation, the admittance matrix must be inverted (re-triangularized) every time a switch operates. As the resulting matrix size would be in the thousands and a large portion of the

system conductance matrix is composed of the switching elements, thus making the inversion task extremely slow. Therefore, the traditional modeling approach for the MMC in EMT simulation is computationally very inefficient.

4.3 Nested Fast and Simultaneous Solution Approach

A recent enhancement to the Dommel's algorithm is the use of Nested Fast and Simultaneous Solution which partitions the network into smaller sub-networks and solves the admittance problem for each separately [78]. Although, this multi-step hierarchical approach increases the number of steps in the solution, the size of each of the admittance matrices is much smaller than that of the full network, which can lead to a reduction in simulation time. The algorithm is explained using the two-part network as shown in Figure 4-6.

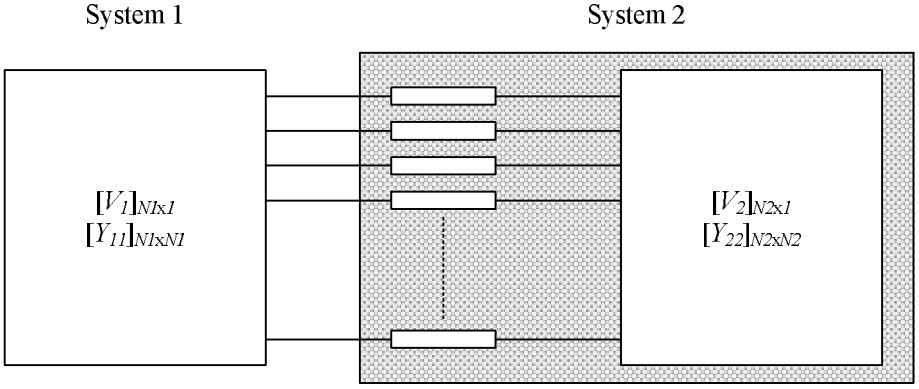


Figure 4-6: Two–part network system

The equivalent admittance matrix formulation for this network can be written as in Equation (4-8):

$$\begin{pmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{pmatrix} \begin{pmatrix} V_1 \\ V_2 \end{pmatrix} = \begin{pmatrix} J_1 \\ J_2 \end{pmatrix} \quad \textbf{4-8}$$

where,

Y_{11}, Y_{22} are admittance matrices for the partitions 1 and 2 respectively,

Y_{12}, Y_{21} are admittance matrices for interconnections,

V_1, V_2 are unknown node voltage vectors for the partitions, and

J_1, J_2 are source current vectors (obtained from branch history and other sources).

Assuming the number of nodes in the two partitions to be N_1 and N_2 respectively, a straightforward, direct solution for the unknown voltage vector $[V_1, V_2]^T$ would require an admittance matrix of size $(N_1+N_2)x(N_1+N_2)$ to be inverted (or re-trianguarized).

The second row of Equation (4-8) can be rearranged in the form of Equation (4-9) to express voltage V_2 as a function of V_1 and other sources.

$$V_2 = -Y_{22}^{-1} Y_{21} V_1 + Y_{22}^{-1} J_2 \quad \textbf{4-9}$$

Substituting Equation (4-9) into the first row of Equation (4-8) yields Equation (4-10).

$$J_1 = Y_{11} V_1 + Y_{12} (Y_{22}^{-1} J_2 - Y_{22}^{-1} Y_{21} V_1) \quad \textbf{4-10}$$

Note that the quantity in parenthesis is the Norton equivalent of V_1 as seen from the boundary nodes of system 1 and includes a term for the Norton current source $(Y_{12} Y_{22}^{-1} J_2)$ and a term $(Y_{12} Y_{22}^{-1} Y_{21})$ for the Norton admittance.

Equation (4-10) can be further simplified to Equation (4-11) which is a set of linear equations of dimension N_1. It can be solved for V_1. Once V_1 is known, it can be substituted into Equation (4-9) to calculate V_2. Once all voltages are known, all currents can readily be calculated. Note that this procedure requires inversion of two matrices, Y_{22} of dimension N_2 x N_2 and $\left(Y_{11} - Y_{12}{Y_{22}}^{-1}Y_{21}\right)$ of dimension N_1 x N_1. Although the above example describes a partition of the original system into two subsystems, the approach can be generalized to multiple subsystems. In the equivalent model proposed in this thesis, each multi-valve is modeled as its own subsystem, which reduces the maximum subsystem size even further.

$$V_1 = (Y_{11} - Y_{12}{Y_{22}}^{-1}Y_{21})^{-1}(J_1 - Y_{12}{Y_{22}}^{-1}J_2) \quad \textbf{4-11}$$

Applying the formal procedure for Nested Fast and Simultaneous Solution [78] still requires inversion of fairly large matrices corresponding to each multi-valve, whereas the direct derivation of the Norton Equivalent (or Thévenin equivalent) can still reduce computations very drastically. Therefore, rather than apply the procedure in a formal mathematical manner using Equation (4-9) and Equation (4-10) as in the original paper, the Norton equivalent for the MMC can be obtained in a very straightforward manner directly by inspection as discussed in the following sections.

4.4 Derivation of MMC Equivalent Models

A specially designed Thévenin equivalent model is derived to represent each multi-valve of the MMC converter in detail as discussed below.

4.4.1 Equivalent Resistive Circuit for a Capacitor

Using the trapezoidal rule integration method, the capacitor can be represented as an equivalent voltage source V_{c0eq}, and a resistor R_{c0eq}, as shown in Figure 4-7(b) and the values of V_{c0eq} and R_{c0eq} are given in Equation (4-12) [79].

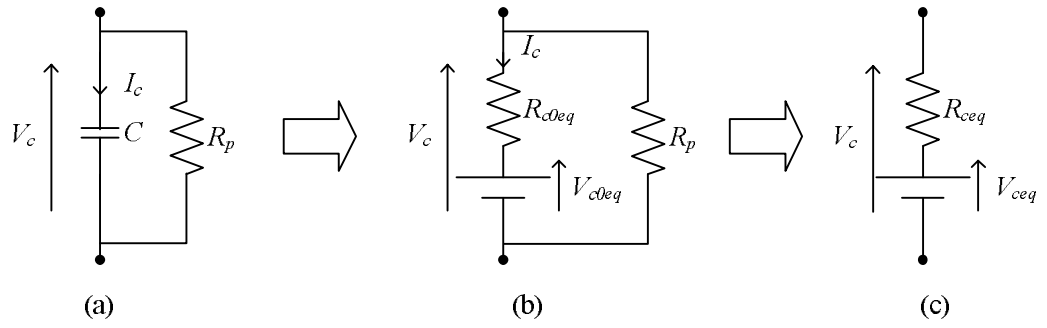


Figure 4-7: Capacitor equivalent circuit

$$R_{c0eq} = \frac{\Delta T}{2C}$$
$$V_{c0eq}(t-\Delta T) = \left(\frac{\Delta T}{2C} I_c(t-\Delta T) + V_c(t-\Delta T)\right) \quad \textbf{4-12}$$

The value of equivalent resistance R_{c0eq} depends on the sub-module capacitance, C and simulation time-step, ΔT. The equivalent voltage, V_{c0eq} is calculated at time t using the capacitor current and voltage values in the previous time-step (history terms).

The final equivalent shown in Figure 4-7(c), is the simplified resistive circuit of the capacitor equivalent, when considering the loss resistance R_p. The values of V_{ceq} and R_{ceq} are given in Equation (4-13).

$$R_{ceq} = \frac{R_{c0eq}\, R_p}{\left(R_{c0eq} + R_p\right)}$$

$$V_{ceq}\left(t - \Delta T\right) = \left(\frac{R_p}{R_{c0eq} + R_p}\right) V_{c0eq}\left(t - \Delta T\right) \qquad \textbf{4-13}$$

4.4.2 Thévenin Equivalent for a Half-Bridge Sub-Module

With these steps, an equivalent resistive circuit for a half-bridge sub-module has been derived as shown in Figure 4-8.

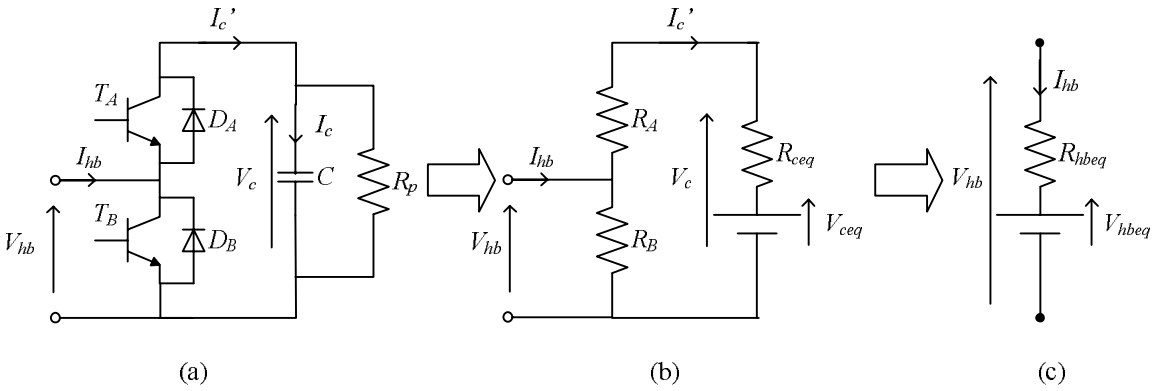


Figure 4-8: The electrical equivalent of a half-bridge sub-module

In Figure 4-8(b), R_A and R_B represent the switching resistances of two IGBT/Diode pairs. The values of resistors, R_A and R_B depend on the switch state and can acquire one of three possible values as given in Equation (4-14). Here, R_{T_ON} and R_{T_OFF} are the IGBT 'ON' state resistance and 'OFF' state resistance and R_{D_ON} and R_{D_OFF} are the diode 'ON' state resistance and 'OFF' state resistance.

$$R_A(t)=\begin{cases}\left(\dfrac{R_{T\_ON}\cdot R_{D\_OFF}}{R_{T\_ON}+R_{D\_OFF}}\right)\text{.....if } T_A-\text{ON},\ D_A-\text{OFF}\\ \left(\dfrac{R_{T\_OFF}\cdot R_{D\_ON}}{R_{T\_OFF}+R_{D\_ON}}\right)\text{.....if } T_A-\text{OFF},\ D_A-\text{ON}\\ \left(\dfrac{R_{T\_OFF}\cdot R_{D\_OFF}}{R_{T\_OFF}+R_{D\_OFF}}\right)\text{.....if } T_A-\text{OFF},\ D_A-\text{OFF}\end{cases},\quad R_B(t)=\begin{cases}\left(\dfrac{R_{T\_ON}\cdot R_{D\_OFF}}{R_{T\_ON}+R_{D\_OFF}}\right)\text{.....if } T_B-\text{ON},\ D_B-\text{OFF}\\ \left(\dfrac{R_{T\_OFF}\cdot R_{D\_ON}}{R_{T\_OFF}+R_{D\_ON}}\right)\text{.....if } T_B-\text{OFF},\ D_B-\text{ON}\\ \left(\dfrac{R_{T\_OFF}\cdot R_{D\_OFF}}{R_{T\_OFF}+R_{D\_OFF}}\right)\text{.....if } T_B-\text{OFF},\ D_B-\text{OFF}\end{cases} \quad \textbf{4-14}$$

Equation (4-15) represents the final Thévenin equivalent circuit of the half-bridge, shown in Figure 4-8(c). As given in Equation (4-15), the half-bridge sub-module voltage, V_{hb} can be determined using the sub-module current value, I_{hb} and the previous time-step Thévenin equivalent voltage value, V_{hbeq}.

$$V_{hb}(t)=R_{hbeq}I_{hb}(t)+V_{hbeq}(t-\Delta T)$$

where

$$R_{hbeq}=R_B\left(1-\frac{R_B}{R_A+R_B+R_{ceq}}\right) \quad \textbf{4-15}$$

$$V_{hbeq}(t-\Delta T)=\left(\frac{R_B}{R_A+R_B+R_{ceq}}\right)V_{ceq}(t-\Delta T)$$

4.4.3 Thévenin Equivalent of a Full-Bridge Sub-Module

The approach used to model the half-bridge sub-modules, can be further modified to obtain a Thévenin equivalent circuit for the full-bridge sub-modules as shown in Figure 4-9.

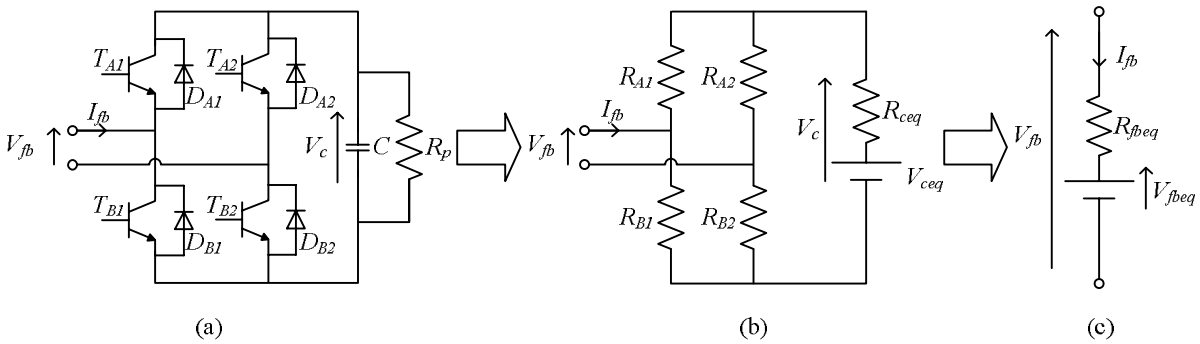


Figure 4-9: The electrical equivalent of a full-bridge sub-module

In Figure 4-9(b), R_{A1}, R_{B1}, R_{A2}, and R_{B2} represent the resistances of the switches T_{A1}/D_{A1}, T_{B1}/D_{B1}, T_{A2}/D_{A2}, and T_{B2}/D_{B2} respectively. Here, switch T_{A1}/D_{A1} stands for the single switched formed by the parallelly connected individual switch elements T_{A1} and D_{A1}. The values of resistor R_{A1}, R_{B1}, R_{A2}, and R_{B2} depend on the switch state and can acquire one of three possible values as given in Equation (4-16). Here, R_{T_ON} and R_{T_OFF} are the IGBT 'ON' state resistance and 'OFF' state resistance and R_{D_ON} and R_{D_OFF} are the diode 'ON' state resistance and 'OFF' state resistance.

$$R_{A1}(t)=\begin{cases} R_{T\_ON-D\_OFF} \text{.....if } T_{A1}-\text{ON}, D_{A1}-\text{OFF} \\ R_{T\_OFF-D\_ON} \text{.....if } T_{A1}-\text{OFF}, D_{A1}-\text{ON} \\ R_{T\_OFF-D\_OFF} \text{.....if } T_{A1}-\text{OFF}, D_{A1}-\text{OFF} \end{cases} \quad R_{A2}(t)=\begin{cases} R_{T\_ON-D\_OFF} \text{.....if } T_{A2}-\text{ON}, D_{A2}-\text{OFF} \\ R_{T\_OFF-D\_ON} \text{.....if } T_{A2}-\text{OFF}, D_{A2}-\text{ON} \\ R_{T\_OFF-D\_OFF} \text{.....if } T_{A2}-\text{OFF}, D_{A2}-\text{OFF} \end{cases}$$

$$R_{B1}(t)=\begin{cases} R_{T\_ON-D\_OFF} \text{.....if } T_{B1}-\text{ON}, D_{B1}-\text{OFF} \\ R_{T\_OFF-D\_ON} \text{.....if } T_{B1}-\text{OFF}, D_{B1}-\text{ON} \\ R_{T\_OFF-D\_OFF} \text{.....if } T_{B1}-\text{OFF}, D_{B1}-\text{OFF} \end{cases} \quad R_{B2}(t)=\begin{cases} R_{T\_ON-D\_OFF} \text{.....if } T_{B2}-\text{ON}, D_{B2}-\text{OFF} \\ R_{T\_OFF-D\_ON} \text{.....if } T_{B2}-\text{OFF}, D_{B2}-\text{ON} \\ R_{T\_OFF-D\_OFF} \text{.....if } T_{B2}-\text{OFF}, D_{B2}-\text{OFF} \end{cases} \quad \textbf{4-16}$$

where,

$$R_{T\_ON-D\_OFF}=\left(\frac{R_{T\_ON}\cdot R_{D\_OFF}}{R_{T\_ON}+R_{D\_OFF}}\right), \quad R_{T\_OFF-D\_ON}=\left(\frac{R_{T\_OFF}\cdot R_{D\_ON}}{R_{T\_OFF}+R_{D\_ON}}\right), \quad R_{T\_OFF-D\_OFF}=\left(\frac{R_{T\_OFF}\cdot R_{D\_OFF}}{R_{T\_OFF}+R_{D\_OFF}}\right)$$

Equation (4-17) represents the final Thévenin equivalent circuit of the full-bridge, shown in Figure 4-9(c).

$$V_{fb}(t)=R_{fbeq}\cdot I_{fb}(t)+V_{fbeq}(t-\Delta T) \quad \textbf{4-17}$$

The value of full-bridge sub-module voltage, V_{fb} is a function of the sub-module current, I_{fb} and the previous time-step Thévenin equivalent voltage, V_{fbeq}. The derivation of the equivalent circuit parameters shown in Figure 4-9(c) is discussed below.

1. *Thévenin Equivalent Resistance*

By definition, if all the sources within the network are replaced by their internal resistances then the impedance seen looking into the port from outside is the Thévenin resistance. Therefore, the capacitor equivalent voltage source, V_{ceq} in Figure 4-10(a), is short circuited to obtain the equivalent resistance as shown in Figure 4-10(b). An intermediate stage of the derivation process is shown in Figure 4-10(c) and the parameters of $\overline{\overline{R_1}}$, $\overline{\overline{R_2}}$, and $\overline{\overline{R_3}}$ are given in Equation (4-18).

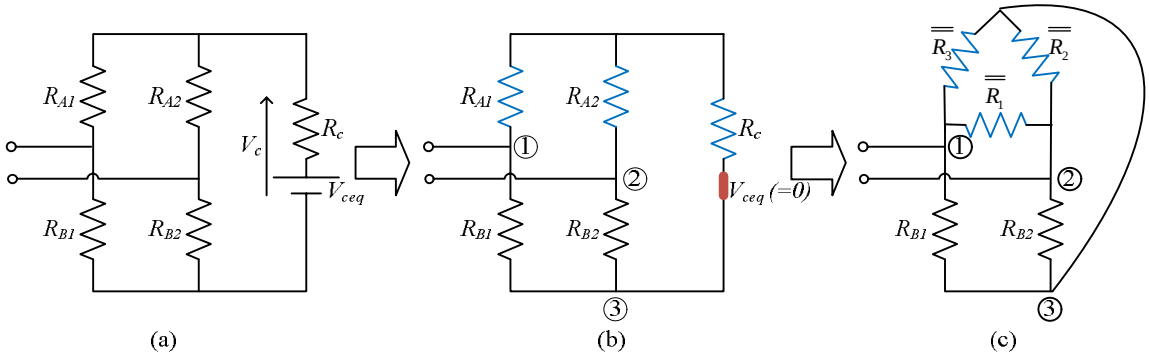


Figure 4-10: Derivation of Thévenin equivalent resistance for full-bridge sub-module

$$\overline{\overline{R_1}} = \frac{R_{A1}R_{A2} + R_{A2}R_c + R_cR_{A1}}{R_c}$$
$$\overline{\overline{R_2}} = \frac{R_{A1}R_{A2} + R_{A2}R_c + R_cR_{A1}}{R_{A1}} \qquad \textbf{4-18}$$
$$\overline{\overline{R_3}} = \frac{R_{A1}R_{A2} + R_{A2}R_c + R_cR_{A1}}{R_{A2}}$$

The circuit shown in Figure 4-10(c) can then be simplified as shown in Figure 4-11(a). Figure 4-11(b) shows the final Thévenin equivalent resistance whose parameters are given by Equation (4-19).

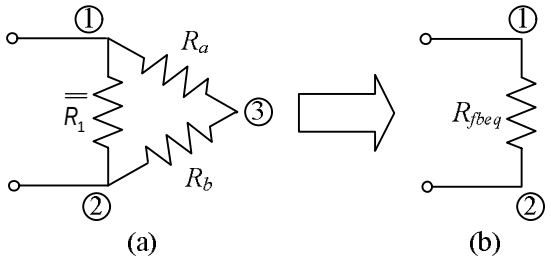


Figure 4-11: Thévenin equivalent resistance of full-bridge sub-module

$$R_{fbeq} = \frac{R_1\left(R_a + R_b\right)}{\overline{\overline{R_1}} + \left(R_a + R_b\right)}$$

where, **4-19**

$$R_a = \frac{R_{B1}\overline{\overline{R_3}}}{\left(R_{B1} + \overline{\overline{R_3}}\right)} \quad \text{and} \qquad R_b = \frac{R_{B2}\overline{\overline{R_2}}}{\left(R_{B2} + \overline{\overline{R_2}}\right)}$$

2. Thévenin Equivalent Voltage Source

If the two terminals are open, then the open circuit voltage across the network must be equal to the Thévenin equivalent voltage source. Therefore, the full-bridge sub-module Thévenin voltage equivalent is calculated as shown below.

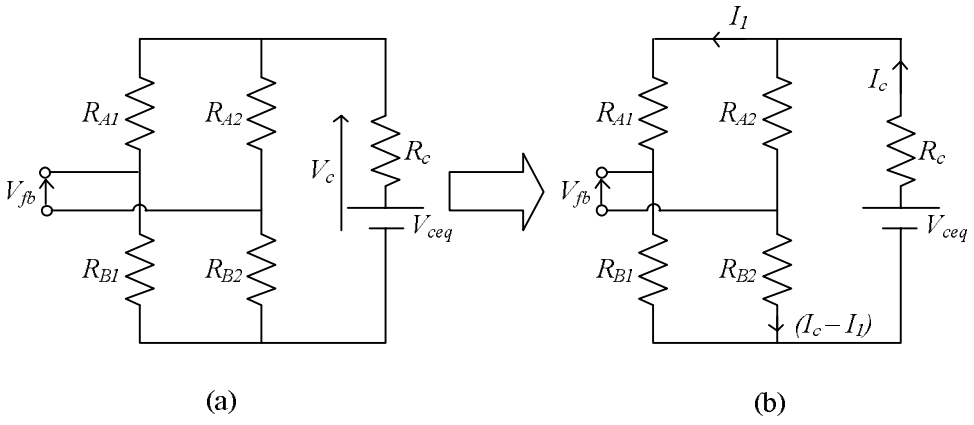


Figure 4-12: Derivation of Thévenin equivalent voltage source for full-bridge sub-module

The branch currents of the full-bridge sub-module equivalent shown in Figure 4-12(b), can be determined as given in Equation (4-20).

$$I_1(t) = \left(\frac{R_{A2} + R_{B2}}{R_{A1} + R_{A2} + R_{B1} + R_{B2}} \right) I_c(t)$$

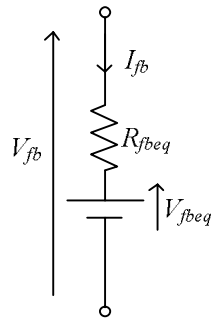
where,

$$I_c(t) = \frac{V_{ceq}(t - \Delta T)}{\left(R_c + \frac{(R_{A1} + R_{B1})(R_{A2} + R_{B2})}{R_{A1} + R_{A2} + R_{B1} + R_{B2}} \right)} \quad \textbf{4-20}$$

The final of Thévenin equivalent voltage can be calculated as given in Equation (4-21).

$$V_{fbeq}(t - \Delta T) = \left(\frac{(R_{A2}R_{B1} - R_{A1}R_{B2})}{R_c(R_{A1} + R_{A2} + R_{B1} + R_{B2}) + (R_{A1} + R_{B1})(R_{A2} + R_{B2})} \right) V_{ceq}(t - \Delta T) \quad \textbf{4-21}$$

Thus, the final Thévenin circuit for the full-bridge sub-module is given in Figure 4-13. Here, R_{fbeq} is as given in Equation (4-19) and V_{fbeq} as given in Equation (4-21).



(c)

Figure 4-13: Thévenin equivalent circuit for full-bridge sub-module

4.4.4 Dynamic Model for Multi-Valve (Half-Bridge or Full-Bridge)

By daisy chaining the individual sub-module equivalents of half-bridge (Figure 4-8(c)) or full-bridge (Figure 4-9(c)), an equivalent circuit for the multi-valve can be constructed as shown in Figure 4-14.

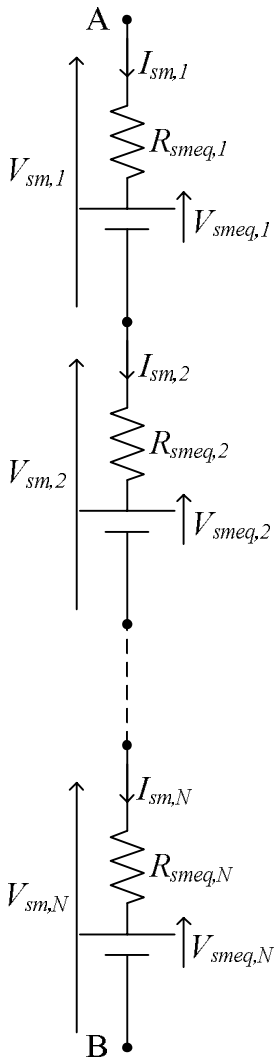


Figure 4-14: Electrical equivalent of a multi-valve

This structure corresponds to system 2 (see Figure 4-6), and due to the daisy-chaining, the resultant matrix Y_{22} (Figure 4-6) is sparse and has a banded diagonal, making its inversion more computationally efficient. However, as it turns out, its Thévenin equivalent can be determined very simply, and so even this mathematical step can be simplified. Since output terminals of the sub-modules are series connected, the multi-valve voltage is the sum of all the individual sub-module voltages as given in Equation (4-22):

$$\begin{aligned} V_{mv}(t) &= \sum_{i=1}^{N} V_{sm_i}(t) \\ &= \left[\sum_{i=1}^{N} R_{hbeq_i}\right] \cdot I_{mv}(t) + \left[\sum_{i=1}^{N} V_{hbeq_i}(t-\Delta T)\right] : \text{for half - bridge modules} \\ &= \left[\sum_{i=1}^{N} R_{fbeq_i}\right] \cdot I_{mv}(t) + \left[\sum_{i=1}^{N} V_{fbeq_i}(t-\Delta T)\right] : \text{for full - bridge modules} \\ &= R_{mveq} \cdot I_{mv}(t) + V_{mveq}(t-\Delta T) \end{aligned} \qquad \textbf{4-22}$$

where, N = number of sub - modules per multi - valve.

Equation (4-22) can be converted into a Thévenin equivalent circuit consisting of a series connected equivalent voltage source, $V_{mveq}(t\text{-}\Delta T)$ and a resistor R_{mveq}. Because the same multi-valve current I_{mv}, passes through all sub-modules, this equation can be used to develop a dynamic equivalent model for the multi-valve as in Figure 4-15, which is simple, yet exact.

Note that as the half-bridge model and full-bridge model yield the same Thévenin equivalent as shown in Figure 4-15, the above approach is equally applicable to either configuration.

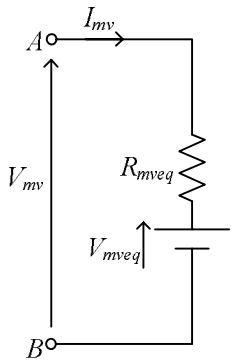


Figure 4-15: Electrical equivalent for a MMC multi-valve

The nodal admittance matrix solver (EMT solver) requires a Norton equivalent, for which the conversion from the Thévenin equivalent is straightforward and trivial. Each multi-valve in the MMC is thus reduced to a single two-node element in the main EMT solver as shown in Figure 4-16, and thus the size of the resultant admittance matrix of the full network is reduced typically by several orders of magnitude. This greatly speeds up the computation as shown later.

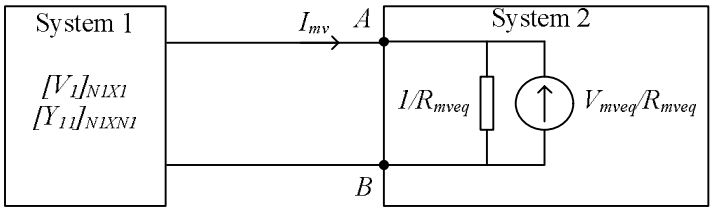


Figure 4-16: Two-part network with reduced number of nodes

4.4.5 Calculation of Individual Sub–Module Internal Branch Currents and Node Voltages

As all the sub-modules are now collapsed into a single equivalent, their individual identities are no longer available in the main network solver. The Thévenin equivalent solver however, does consider each sub-module separately and internally calculates

branch currents and node voltages. Therefore, the proposed equivalent model is a detailed representation of the multi-valve. The Thévenin equivalent solver requires the multi-valve current, I_{mv} *(=*I_{hb}*)* from the main network solver and previous time-step value of the N capacitor voltages (V_{c0eq_R}, $R \in \{1,\ldots N\}$) to calculate the internal voltages and currents of each sub-module.

1. Half-Bridge Model

The sub-module internal currents and voltages, as marked in Figure 4-17 can readily be calculated using Equation (4-23). These values are obtained using a simple circuit solution of Figure 4-17(a).

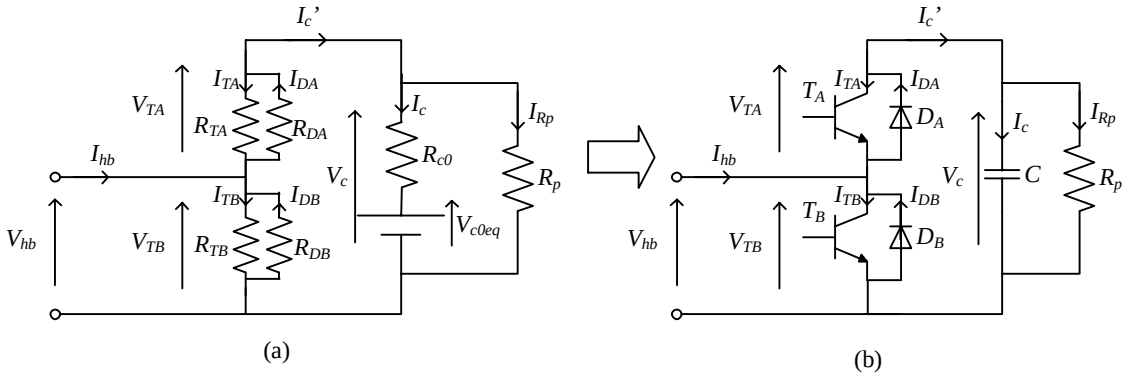


Figure 4-17: Calculation of internal branch currents and node voltages of a half-bridge sub-module

The values of capacitor voltages, V_c are made available for the capacitor voltage balancing controller as described in Section 3.4.1. Also, it is required to store the values of capacitor voltages and capacitor currents to calculate the capacitor equivalent source voltage, V_{c0eq} in the next time-step as given in Equation (4-12).

$$I_c'(t)=\frac{(R_p+R_{c0})R_B(t)I_{hb}(t)-R_pV_{c0eq}(t-\Delta T)}{R_p[R_A(t)+R_B(t)+R_{c0}]+R_{c0}[R_A(t)+R_B(t)]}$$

$$I_{Rp}(t)=\frac{R_B(t)I_{hb}(t)-[R_A(t)+R_B(t)]I_c'(t)}{R_p}$$

$$I_c(t)=I_c'(t)-I_{Rp}(t)$$

$$V_{TA}(t)=-I_c'(t)R_A(t)$$

$$V_{TB}(t)=[I_{hb}(t)-I_c'(t)]R_A(t)$$

$$V_c(t)=V_{TA}(t)+V_{TB}(t)$$

4-23

$$I_{TA}(t)=\frac{V_{TA}(t)}{R_{TA}(t)} \quad \& \quad I_{DA}(t)=-\frac{V_{TA}(t)}{R_{DA}(t)}$$

$$I_{TB}(t)=\frac{V_{TB}(t)}{R_{TB}(t)} \quad \& \quad I_{DB}(t)=-\frac{V_{TB}(t)}{R_{DB}(t)}$$

$$\text{where, } R_A(t)=\frac{R_{TA}(t)R_{DA}(t)}{R_{TA}(t)+R_{DA}(t)} \quad \& \quad R_B(t)=\frac{R_{TB}(t)R_{DB}(t)}{R_{TB}(t)+R_{DB}(t)}$$

2. Full Bridge Model

A similar calculation can be made for the full-bridge converter model as well and the equations are given in Equation (4-24) for the sub-module internal currents and voltages, as marked in Figure 4-18.

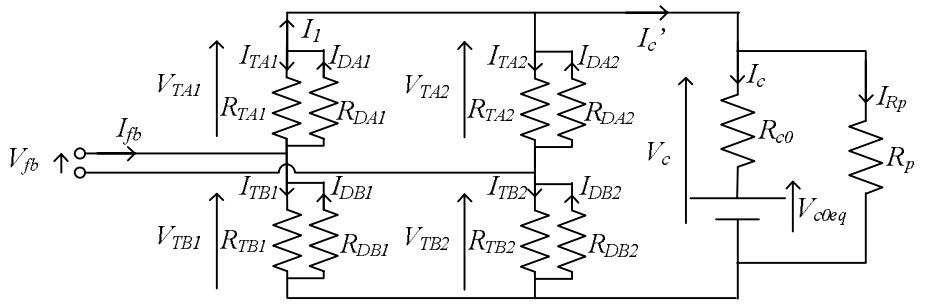


Figure 4-18: Internal branch currents and node voltages of a full-bridge sub-module

$$I_c'(t)=\frac{\left[R_{A2}(t)R_{B1}(t)-R_{A1}(t)R_{B2}(t)\right]\cdot I_{fb}(t)-R_{tot}(t)V_{ceq}(t-\Delta t)}{R_cR_{tot}(t)+\left[\left(R_{A1}(t)+R_{B1}(t)\right)\left(R_{A2}(t)+R_{B2}(t)\right)\right]}$$

$$I_{Rp}(T)=\frac{I_c'(t)R_{C0}+V_{c0eq}(t-\Delta t)}{R_{c0}+R_p}$$

$$I_c(t)=I_c'(t)-I_{Rp}(t)$$

$$I_1(t)=\frac{-\left(V_{ceq}(t-\Delta t)+R_cI_c'(t)-R_{B1}(t)I_{fb}(t)\right)}{\left(R_{A1}(t)+R_{B1}(t)\right)}$$

$$V_{TAI}(t)=-I_1(t)R_{A1}(t) \quad , \quad V_{TA2}(t)=-\left(I_c'(t)-I_1(t)\right)R_{A2}(t)$$

$$V_{TBI}(t)=\left(I_{fb}(t)-I_1(t)\right)R_{B1}(t) \quad , \quad V_{TB2}(t)=-\left(I_{fb}(t)-I_1(t)+I_c'(t)\right)R_{B2}(t)$$

$$V_c(t)=V_{TAI}(t)+V_{TBI}(t)$$

$$I_{TAI}(t)=\frac{V_{TAI}(t)}{R_{TA1}(t)} \quad \& \quad I_{DAI}(t)=-\frac{V_{TAI}(t)}{R_{DA1}(t)}$$

$$I_{TA2}(t)=\frac{V_{TA2}(t)}{R_{TA2}(t)} \quad \& \quad I_{DA2}(t)=-\frac{V_{TA2}(t)}{R_{DA2}(t)} \qquad \textbf{4-24}$$

$$I_{TBI}(t)=\frac{V_{TBI}(t)}{R_{TB1}(t)} \quad \& \quad I_{DBI}(t)=-\frac{V_{TBI}(t)}{R_{DB1}(t)}$$

$$I_{TB2}(t)=\frac{V_{TB2}(t)}{R_{TB2}(t)} \quad \& \quad I_{DB2}(t)=-\frac{V_{TB2}(t)}{R_{DB2}(t)}$$

where,

$$R_{A1}(t)=\frac{R_{TA1}(t)R_{DA1}(t)}{R_{TA1}(t)+R_{DA1}(t)} \quad \& \quad R_{A2}(t)=\frac{R_{TA2}(t)R_{DA2}(t)}{R_{TA2}(t)+R_{DA2}(t)}$$

$$R_{L1}(t)=\frac{R_{TB1}(t)R_{DB1}(t)}{R_{TB1}(t)+R_{DB1}(t)} \quad \& \quad R_{U2}(t)=\frac{R_{TB2}(t)R_{DB2}(t)}{R_{TB2}(t)+R_{DB2}(t)}$$

$$R_c=\frac{R_{c0}\cdot R_p}{R_{c0}+R_p} \quad \& \quad V_{ceq}(t-\Delta t)=\left(\frac{R_p}{R_{c0}+R_p}\right)V_{c0eq}(t-\Delta t)$$

$$R_{tot}(t)=\left[R_{A1}(t)+R_{A2}(t)+R_{B1}(t)+R_{B2}(t)\right]$$

4.4.6 Selection of Switch ON/OFF Status

Considering the gate signal, device terminals voltage (V_{ce}), and current direction (I_{ce}), a decision can be made whether the IGBT (T) or diode (D) of the switching device is ‘ON’ at any moment in time. IGBT/diode switch can have one of three switching states depending on the device conduction;

T – ON/D – OFF *T – OFF/D – ON* *T – OFF/D – OFF*

In each of these states, the switch resistance is $R_{T\_ON\text{-}D\_OFF}$, $R_{T\_OFF\text{-}D\_ON}$, and $R_{T\_OFF\text{-}D\_OFF}$ respectively. The possible transitions when the switch is in each of the above states are listed below and can be summarized by the state transition diagram shown in Figure 4-19 [82].

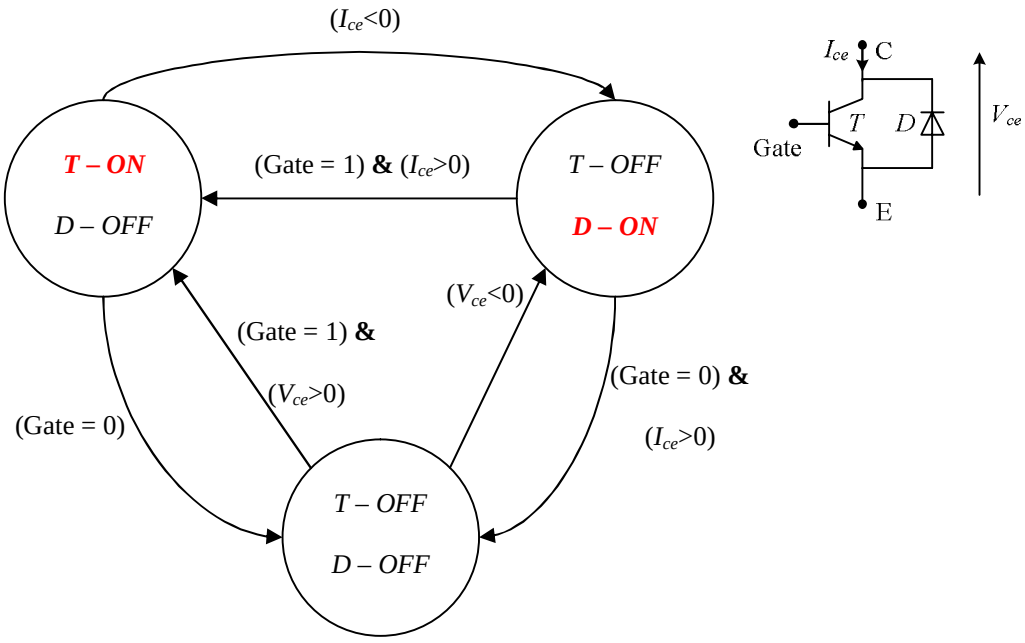


Figure 4-19: State transition diagram for an IGBT/diode switch combination

1. When the switch is in the *T-ON/D-OFF* state, i.e., it is carrying forward current (I_{ce}>0) and there is a gate pulse, the switch resistance is $R_{T\_ON\text{-}D\_OFF}$. The switch can make a transition to the other states as follows:
   a. If the current reverses (I_{ce}<0) then the IGBT turns 'OFF', and the diode spontaneously turns 'ON'. The switch thus attains the *T-OFF/D-ON* state.

b. If the gate pulse is stopped and the current is in the forward direction, (GATE=0), then the IGBT turns 'OFF'. The switch attains the *T-OFF/D-OFF* state.

2. When the switch is in the *T-OFF/D-ON* state, the current is in the reverse direction (I_{ce}<0). The gate pulse may be 0 or 1 (note GATE=1 will not result in IGBT conduction if the IGBT is reverse biased). The switch resistance is $R_{T\_OFF\text{-}D\_ON}$.

   a. If GATE = 1 and the current suddenly changes direction (I_{ce}>0) the IGBT turns 'ON' and the diode turns 'OFF'. The switch now attains the *T-ON/D-OFF* state.

   b. If GATE = 0, and the current attempts to go positive, the diode instantly turns 'OFF' and the system attains the *T-OFF/D-OFF* state.

3. When the switch is in the *D-OFF/T-OFF* state, neither IGBT nor diode is conducting (I_{ce}=0) and the switch resistance is $R_{T\_OFF\text{-}D\_OFF}$. The switch can make transition to one of the conducting states as follows:

   a. If GATE = 1 and IGBT has a forward biased voltage (V_{ce}>0) the IGBT turns 'ON'. The switch now attains the *T-ON/D-OFF* state.

   b. If the voltage across the switch is negative (V_{ce}<0) the diode turns 'ON'. It is not necessary to apply a gate pulse in this situation.

Note that, instead of having separate 'ON' resistance values for the diode and IGBT, a single 'ON' resistance R_{ON} for the 'ON' combination would also be possible to use in this model. Then, the state 1 and state 2 would have the same resistance R_{ON}.

When testing the proposed model with the above switch conduction logic, it readily became apparent that a deficit in the model was the lack of a “blocking” facility. The converter is said to be in the “blocked” state when applying ‘OFF’ gate signals to all sub-module switches. In a typical MMC circuit operation, immediately after blocking on the converter, the anti-parallel diode starts to conduct and the IGBT current does not get chopped to zero instantaneously.

As the proposed model comprises of a series of discrete calculations and due to the consequence of the order of these calculations, it was artificially chopping the current (for a single time-step) and as the circuit is inductive, it resulted in a large spurious overvoltage spike across the valve reactor. To avoid such phenomenon, a modification is introduced to the formal diode conduction logic. Using the preceding current direction of IGBT, the appropriate diode conduction is determined immediately after blocking. This prevents the occurrence of the large spurious voltage across the IGBT which the inductive current chopping had caused [83].

Figure 4-20 shows the possible conduction states of diodes (time = t) by considering the normal operation in the previous time-step prior to blocking. For the proceeding time-step (i.e.: time $\geq t+\Delta T$), the conduction states are selected based on the state transition diagram shown in Figure 4-19.

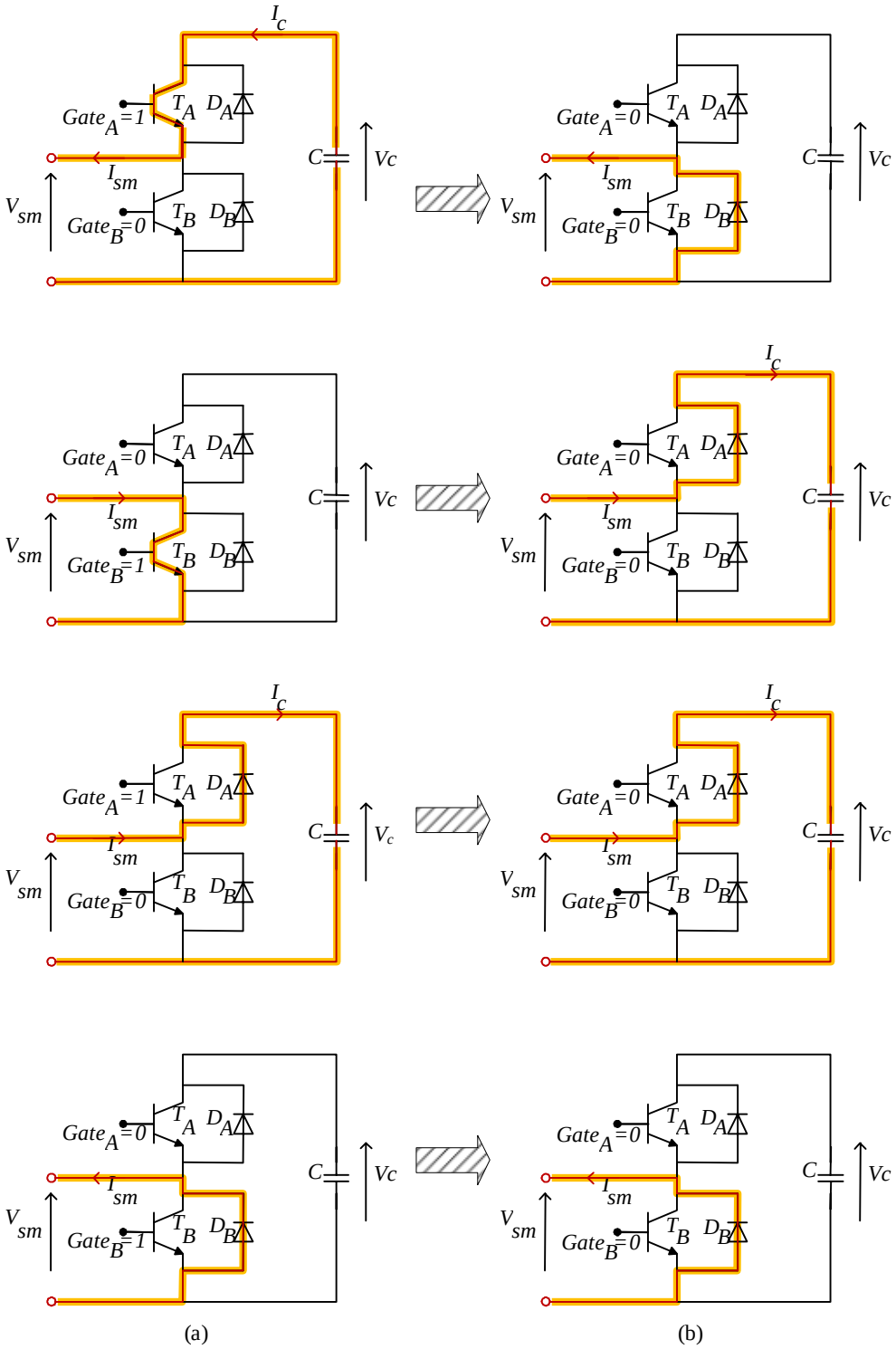


Figure 4-20: Diode selection diagram on half-bridge sub-module blocking:

(a) Prior to blocking (time = *t*-*ΔT*) and (b) Immediately after blocking (time = *t*)

4.4.7 PSCAD Block of MMC Equivalent Models

The developed models are implemented into a commercial EMT program. The program selected is PSCAD/EMTDC, one of the widely used programs for EMT simulations. The large component library of the program allows modeling of large, complex circuits. This makes possible the study of large electric networks that include MMC based HVDC converters.

Figure 4-21 shows the PSCAD block that models a multi-valve of MMC. The inputs to this block are those that are required to determine the parameters of the Thévenin equivalent. In Figure 4-21(a), *TA* and *TB* are the required half-bridge switching signal vectors (i.e. the n^{th} element of the vector is the 'ON/'OFF' command for the n^{th} sub-module) which used to determine the values of resistors, R_A and R_B in Figure 4-8(b). Similarly, *TA1*, *TB1*, *TA2*, and *TB2* in Figure 4-21(b), are the switching signal vectors of the full-bridge sub-module converters.

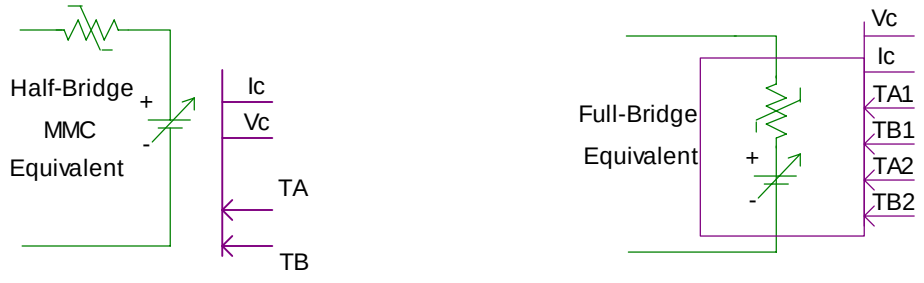


Figure 4-21: PSCAD blocks of proposed equivalent model for an MMC multi-valve with: (a) Half-bridge sub-modules and (b) Full-bridge sub-modules

V_c and I_c output the calculated values of capacitor voltages and capacitor currents of individual sub-modules. The number of sub-modules *(N)* is user selectable at the

beginning of the simulation. These input/output ports and input parameters required by the PSCAD/EMTDC block are described in more details in Appendix A.

4.4.8 Simulation Time-step and Interpolation

With finite time-steps, the actual time for switching device to turn 'ON' or 'OFF' may lie within the time-step. In order to improve the accuracy, many simulation programs such as PSCAD/EMTDC, use an interpolation technique is applied so as to readjust the time-step to coincide more closely with the exact switching instant [84]. This typically reduces any simulation spikes and also permits the use of larger time-steps.

However, with a large number of sub-modules a small time-step has to be used anyway. For example, consider a 60 Hz fundamental frequency and 100 sub-modules per phase. Each step in MMC waveform occurs at an average period of 16.7ms/100 = 167 μs. Hence, a typical time-step would be (as a rule of thumb) about 1/10 (≈ 20 μs) of the average switching period which gives a smooth waveform as selected in this simulation. It is entirely possible that this time-step could be slightly increased (but not beyond 167 μs) if interpolation is added. This effort is left for future work.

4.5 Derivation of an Average Valued Model

A detailed model as derived in section 4.4, can accurately represent the converter in time domain simulations and therefore, is mostly used in converter level studies. However for most system level studies, a detailed converter representation of MMC based HVDC system may not be required for the analysis. In these higher level system

studies, the use of the proposed equivalent model of the converter can add extra complexity into the simulation such as the need to include capacitor voltage balancing which is not necessary for system level studies.

An average valued model of MMC that consists of half–bridge sub-modules is proposed in this thesis for such studies. The derivation of the average model is discussed in this section.

4.5.1 Average Capacitor Valued Model of Converter

The average model is derived assuming an ideal switching operation for the IGBT/diode combination. This assumption gives an infinite 'OFF' state resistance and zero 'ON' state resistance for the switches. With this assumption, the resultant equivalent circuits for the half-bridge sub-module during module capacitor conducting and non-conducting states are shown in Figure 4-22(a) and (b) respectively. When T_A/D_A is 'ON' in Figure 4-22(a), the module output terminal voltage is equal to the magnitude of the capacitor voltage, as there is no voltage drop considered across 'ON' state switch. When the capacitor is not conducting as shown in Figure 4-22(b), the module is bypassed through switch T_B/D_B giving zero output voltage to the module terminals.

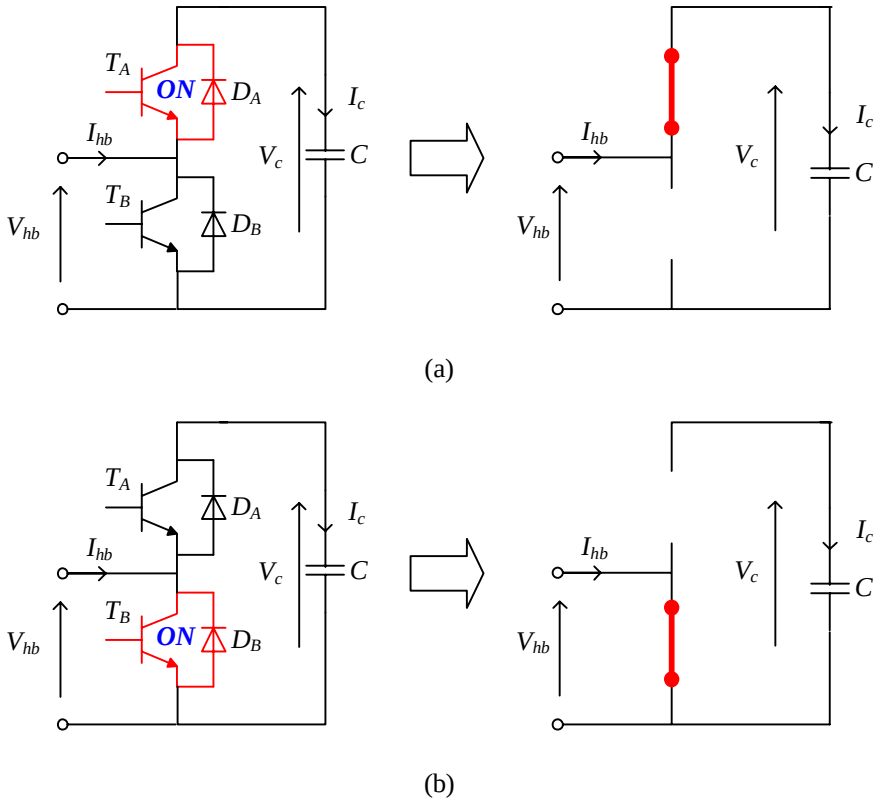


Figure 4-22: Half-bridge sub-module equivalent circuit during capacitor conducting and non-conducting states

With the assumption of ideal switch operation, a single equivalent capacitor can be defined for all conducting capacitors in a multi-valve as the same multi-valve current passing through all conducting capacitors. The capacitance value depends on the number of conducting sub-module capacitors as given in Equation (4-25).

$$C_{eff}(t) = \frac{C}{N(t)} \qquad \textbf{4-25}$$

Where, C is the half-bridge sub-module capacitance, and $N(t)$ is the number of conducting capacitors in each multi-valve.

The required number of conducting capacitors, $N(t)$ is determined by instantaneous

voltage order (i.e. as given in Equation (3-3)). The voltage order change order varies with time when generating multilevel output voltage, so that the required number of conducting capacitors is also time variant. The value of time varying equivalent capacitance is given in Equation (4-25). In general, the voltage-current relationship for a time-varying capacitor is given in Equation (4-26).

$$I_c(t) = V_c(t)\frac{d}{dt}C(t) + C(t)\frac{d}{dt}V_c(t) \quad \textbf{4-26}$$

However in MMC operation, the change of equivalent capacitance is discrete in nature and all conducting capacitors have the same incremental increase or decrease in their voltages during conductive switching as the same multi-valve current is passing through them. Therefore rather than applying the general formula to calculate capacitor voltage in Equation (4-26), the capacitor voltage can be determined by considering an average capacitor voltage, $\overline{V_c}(t)$ for a given *N(t)* as given in Equation (4-27).

$$\overline{V_c}(t) \approx C_{eff}(t)\int I_{mv}(t)\cdot dt \quad \textbf{4-27}$$

where, $I_{mv}(t)$ is the multi-valve current.

Note that the average capacitor voltage $\overline{V_c}(t)$ in Equation (4-27) is equal to the multi-valve voltage. The Thévenin equivalent voltage and resistance parameters for the multi-valve equivalent can be obtained by solving Equation (4-27) using the trapezoidal integration rule as given in Equation (4-28). In Equation (4-28), ΔT is the time-step of the EMT algorithm.

$$\overline{R_c}(t) = \frac{\Delta T}{2C_{eff}(t)}$$
$$\overline{V_{ceq}}(t-\Delta T) = \overline{R_c}(t-\Delta T) I_{mv}(t-\Delta T) + \overline{V_c}(t-\Delta T) \quad \textbf{4-28}$$

The Thévenin equivalent resistive circuit for the multi-valve equivalent derived using an average capacitor value method is shown in Figure 4-23.

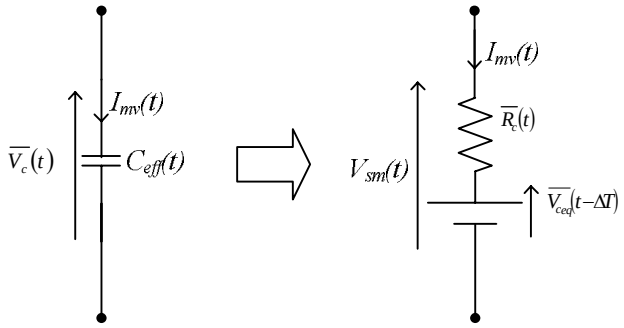


Figure 4-23: Average capacitor valued model

In this model, the magnitude of the output voltage is determined based on the number of conducting capacitors. i.e. the quantization of the sine wave reference voltage as given in Equation (3-3) if the nearest level estimation method discussed in section 3.3.1 is used. However, it does not consider firing signals as an input to calculate the required voltage level and no capacitor voltage balancing controls are represented. Therefore, this model can be considered as a simpler version of proposed equivalent model in section 4.4.

Accuracy and CPU Efficiency of Proposed Model

5.1 Introduction

The performance of the proposed dynamic model is compared against a full, unreduced model of the MMC simulated on the PSCAD/EMTDC program. The unreduced model is referred to as the "full detailed model". Computation speed and accuracy comparisons are conducted for a single converter phase.

5.2 MMC with Half–Bridge Sub-Modules

In these simulations, the converter is operated as an inverter as shown in Figure 5-1. The converter ac terminal is connected to a fixed load; R_{out} is equal to 50 Ω and L_{out} is 120 mH. A constant dc voltage source of magnitude U_{dc} = 240 kV is connected at the converter dc terminals. A constant capacitance of 3000 μF is chosen for the module capacitors as discussed in section 3.5.4. Only twelve half-bridge sub-modules are used so that the steps in the output waveform are noticeable. Also, this is a manageable number

for simulating the full detailed model. An actual MMC application typically has significantly larger number of modules [70], as will be exemplified in a later example.

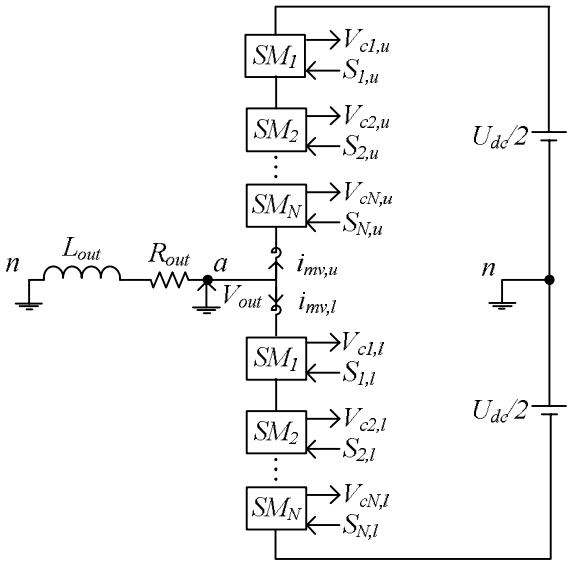


Figure 5-1: Inverter operation of single phase MMC

5.2.1 Accuracy

Testing against an actual prototype was not possible and hence the waveforms generated by the proposed equivalent model are compared against the full detailed model in order to assess the relative accuracy of the equivalent approach under different operating conditions.

1. Simulation of Normal Operation

The half-bridge sub-module and converter waveforms are shown for comparison in Figure 5-2. Waveforms for the firing signal, capacitor voltage for a typical module (e.g.: the top-most module in the upper multi-valve), capacitor current, upper multi-valve

current, and the output voltage of the converter are shown. These results are essentially identical for the proposed equivalent model and the full detailed model. Therefore, the proposed equivalent model is able to capture the behaviour of each half-bridge sub-module separately as well as accurately represent the behaviour of the complete multi-valve.

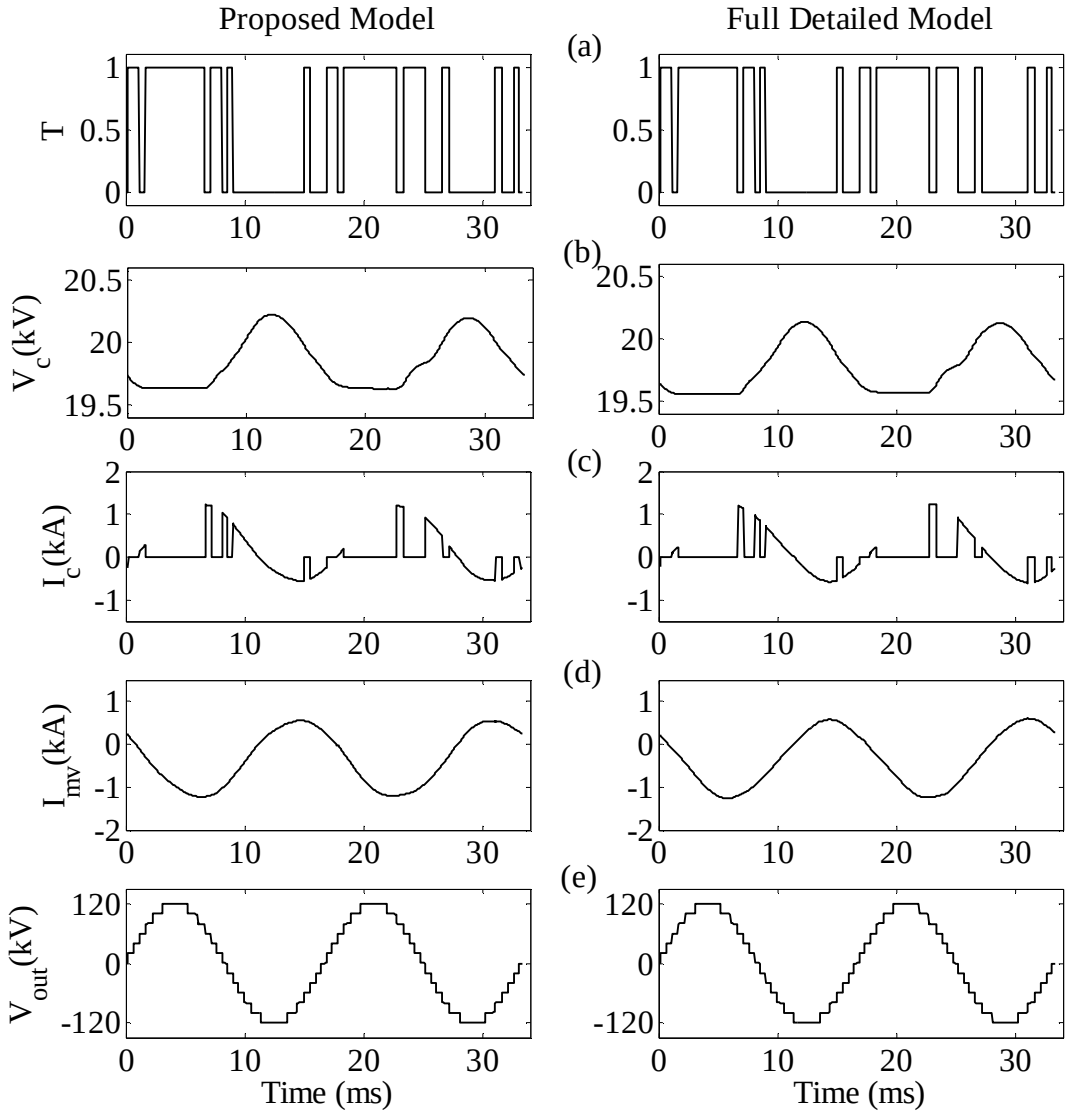


Figure 5-2: MMC and half-bridge sub-module waveforms comparison during normal operation: (a) Firing signal, (b) Module capacitor voltage, (c) Capacitor current, (d) Upper multi-valve current, and (e) MMC output voltage

2. Simulation of a Module Switch Failure

The MMC output waveforms for the failure of a semiconductor switch in a single sub-module for the proposed equivalent model and full detailed model are shown in Figure 5-3(b) and (c) respectively. In this case, the lower switch in the sub-module is assumed to fail into a permanently 'ON' state at 1s as shown in Figure 5-3(a). The proposed equivalent model matches the transients as well as steady state behaviour of the full detailed model even for this condition of mal-operation.

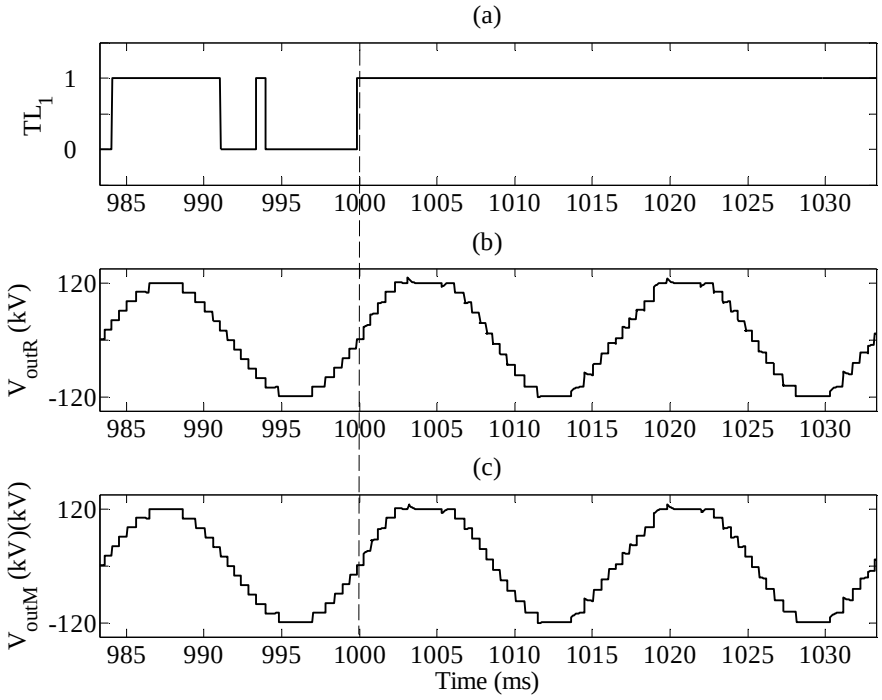


Figure 5-3: MMC output waveforms during a firing failure of a single sub-module: (a) Firing signal of a half-bridge sub-module switch, (b) MMC output voltage waveforms using full detailed model, and (c) MMC output voltage waveforms using proposed equivalent model.

In contrast to averaged models [13], [85] that can simulate only the MMC's external behaviour but are unable to model abnormal operation of the converter such as failure of

a module's control system or failure of the module itself, the proposed equivalent model is capable of representing the exact behaviour of such operation in a manner identical to the full detailed model.

3. Simulation during an Internal Fault of a Half-Bridge Sub-Module

As all the modules are collapsed into a single equivalent, simulation of half-bridge sub-module internal faults is not straightforward in this modeling approach. However, one of the possible means of simulating such an event using this proposed equivalent model is to connect the model in series with a detailed module circuit to represent the multi-valve as shown in Figure 5-4. Then, the internal failure can be applied in the detailed module.

Consider '*N*' number of half-bridge sub-modules and the j^{th} module has an internal fault. In Figure 5-4, the multi-valve (from *A1* to *B2*) is segmented into three sections as below.

- Equivalent model1 (*A1-B1*) represents half-bridge sub-modules from 1 to (*j*-1).
- Equivalent model2 (*A2-B2*) represents half-bridge sub-modules from (*j*+1) to *N*.
- The j^{th} half-bridge sub-module (*B1-A2*) is modeled in details.

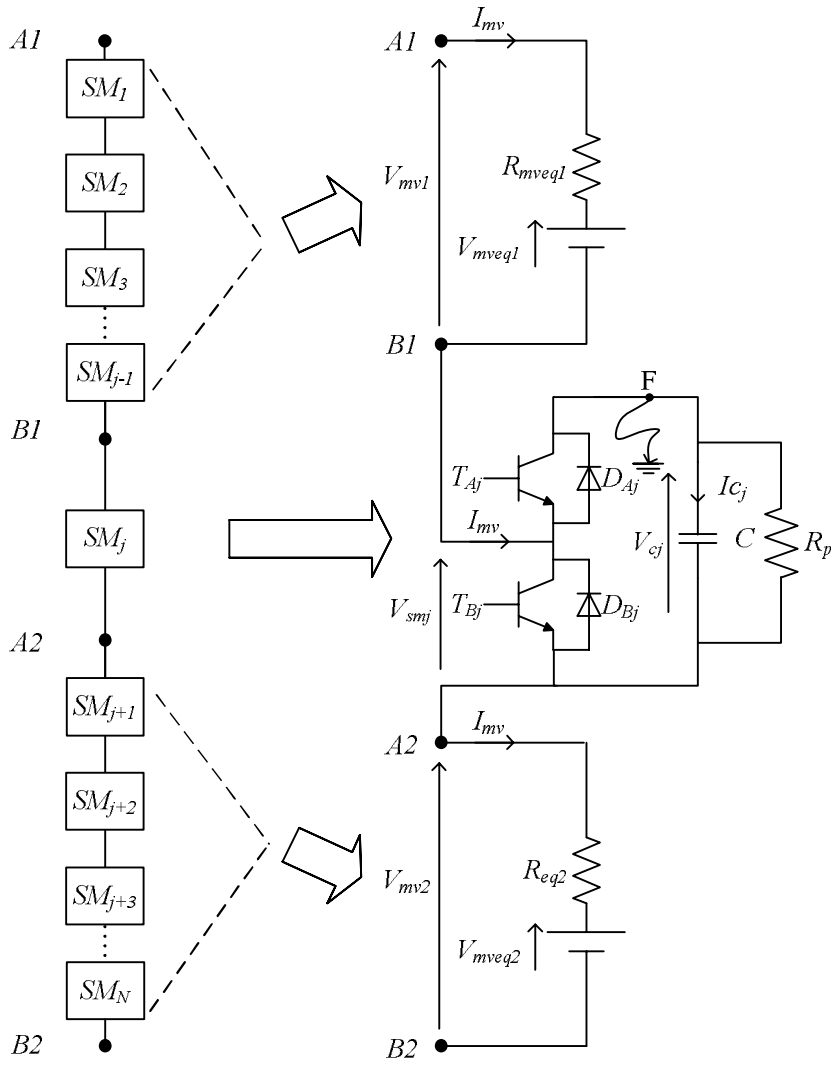


Figure 5-4: Simulating an internal failure of a half-bridge sub-module.

This circuit arrangement enables simulating internal fault(s) of an individual half-bridge sub-module.

For a multi-valve consisting of 12 modules, the converter waveforms are obtained by applying a permanent line to ground fault at point 'F' of the 5th half-bridge sub-module (see Figure 5-4) at 1 s. For the comparison, the waveforms are compared against simulation results of a full detailed model and are shown in Figure 5-5. The results of this

example confirm that the proposed equivalent model can maintain the accuracy of the full detailed model for faults within the module.

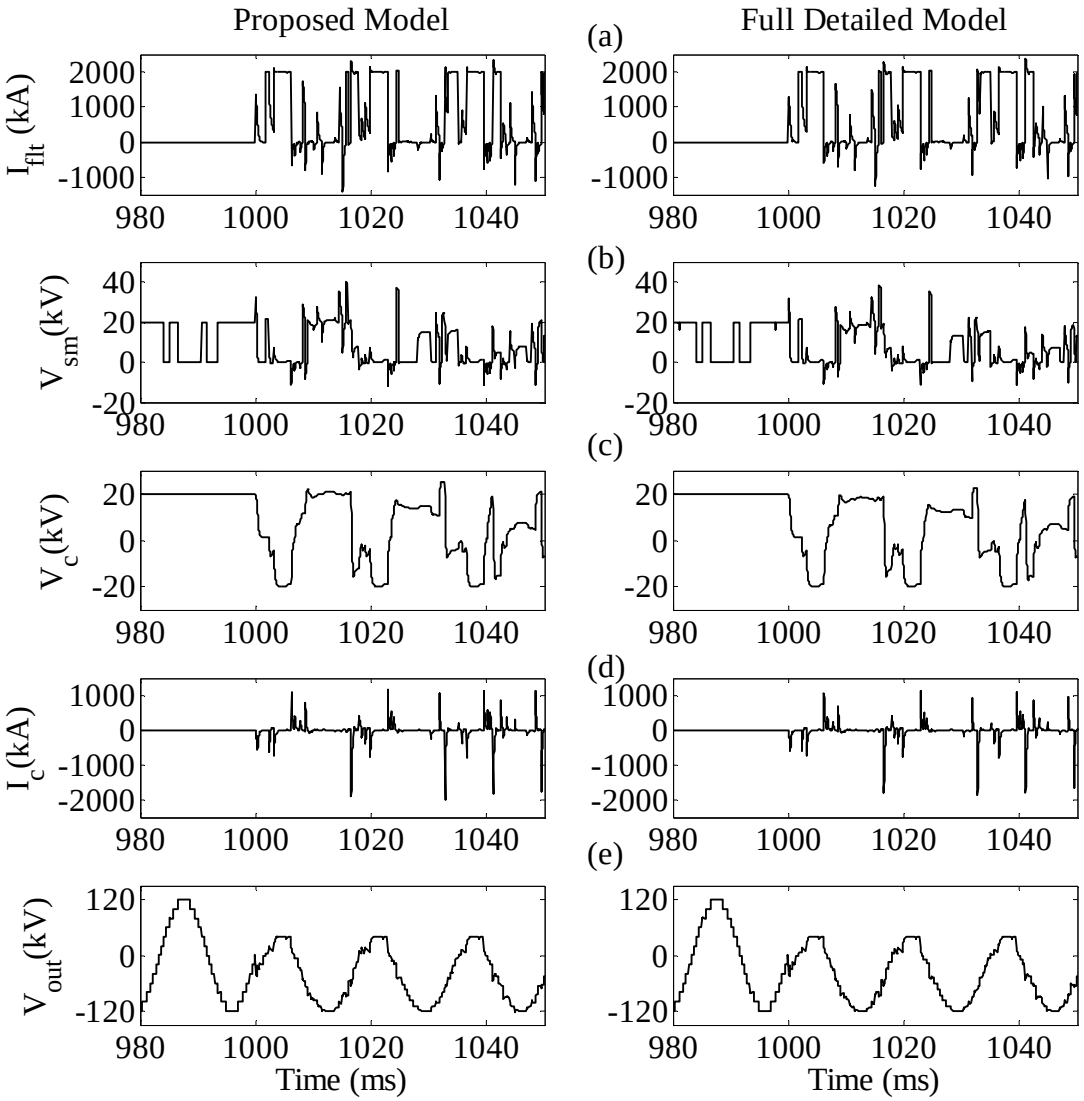


Figure 5-5: Waveforms comparison during an internal failure of half-bridge sub-module: (a) Defective half-bridge sub-module internal fault current, (b) Defective module output voltage, (c) Defective module capacitor voltage, (d) Capacitor current, and (e) MMC output voltage

This circuit arrangement can easily be extended for simulating multiple defective half-bridge sub-modules where the non-defective sub-modules are represented by the proposed equivalent model for improved simulation efficiency.

4. Simulation during Initial Charging of Module Capacitors

To see the waveform comparison during the capacitor charging from their initial zero voltages, the converter phase shown in Figure 5-6 is simulated. The converter ac terminal is connected to a single phase ac voltage source where the magnitude is equal to 120 kV (rms) and the source impedance is $12\angle 80^\circ\ \Omega$. The converter firing signals are initially blocked for 0.1 s to assure that only diodes are conducting during this period. Note that diode conduction allows only the increase of capacitor voltages in the sub-module. When the capacitor voltage reaches its steady value, the firing pulses are applied to the converter at 0.1 s.

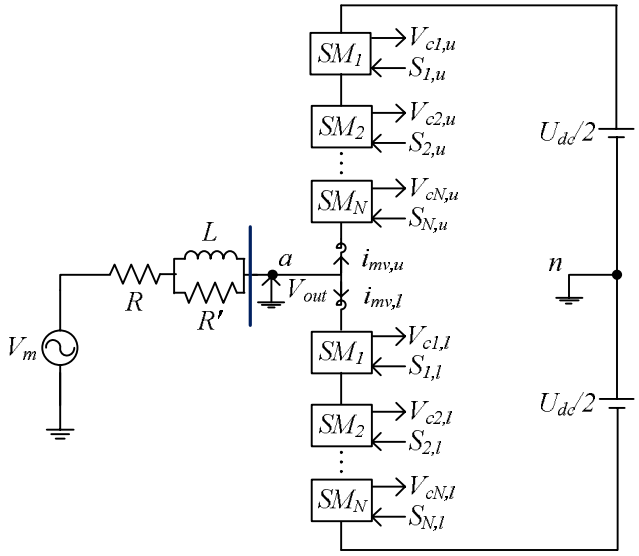


Figure 5-6: MMC model for capacitor charging effect

The results obtained using the proposed equivalent model and full detailed model are shown in Figure 5-7 for comparison. The waveforms of sub-module capacitor voltage $V_{c1,u}$, converter output voltage V_{out}, and converter output current are shown during the converter blocking and de-blocking stages up to first 0.15 s duration.

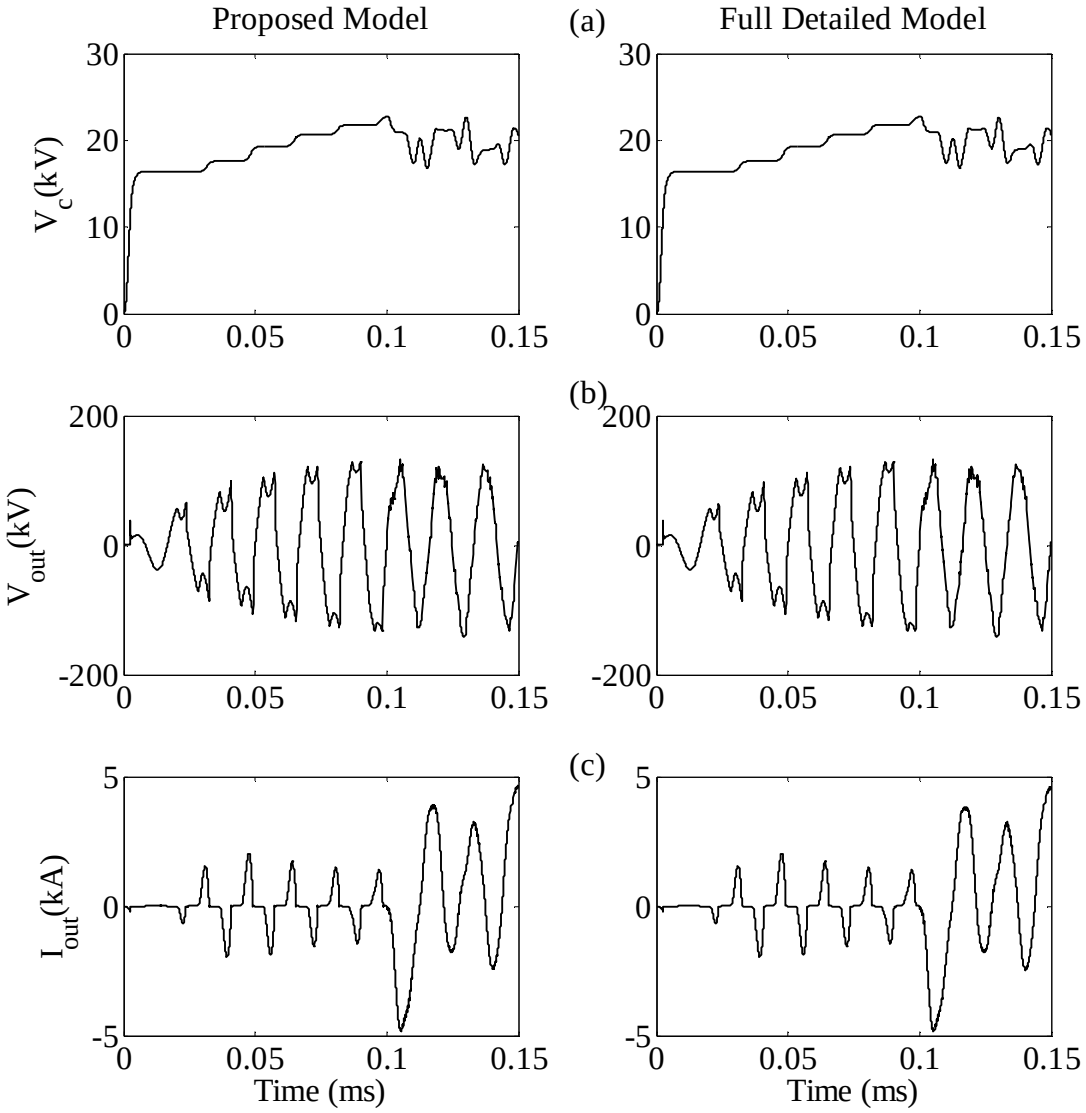


Figure 5-7: MMC waveforms comparison during module capacitor charging:

(a) Half-bridge sub-module capacitor voltage, (b) MMC output voltage, and (c) Output current

The proposed equivalent model can produce identical results during this capacitor charging process as shown in Figure 5-7. Also, the results exactly match during the transient at which the converter operation is changed from the blocked state to de-blocked state. This example shows that the proposed equivalent model can be accurately used to simulate the charging of module capacitors.

5. Simulation during Converter Blocking For a DC Pole-to-Pole Fault

The same circuit arrangement as shown in Figure 5-6 is used to compare the results during a short circuit (pole to pole) failure of the dc bus. In this test, the dc source is immediately short circuited through a low impedance (0.01 Ω) resistor at 1.0 s and the converter firing signals are blocked at 1.002 s.

The results obtained using the proposed equivalent model and full detailed model are shown in Figure 5-8 for comparison. The waveforms obtained in this test show that the proposed equivalent model can be effectively used in simulating dc side faults.

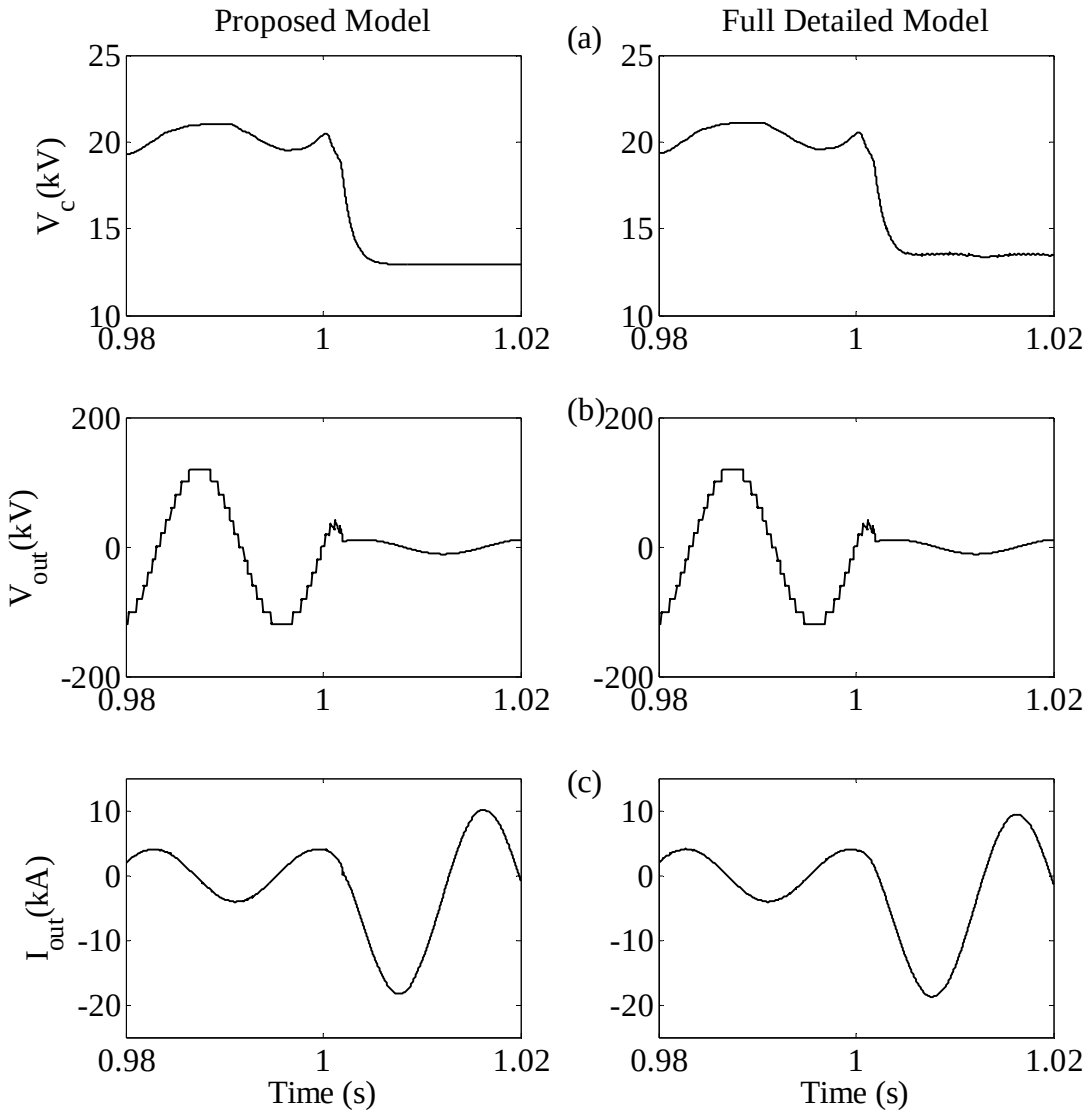


Figure 5-8: MMC waveforms comparison during a dc side fault of the converter:

(a) Half-bridge sub-module capacitor voltage, (b) MMC output voltage, and (c) output current

In actual MMC based HVDC system operation, the converter is predominantly blocked for dc side faults to avoid the discharge of the module capacitors' energy into the dc side faults. However, the present generation of half-bridge sub-module converters cannot fully suppress dc side faults until the converter ac side breaker opens. These

protective measures applied in existing MMC based HVDC systems are discussed in chapter 6.

6. Simulation during AC Line Fault

In this test, a ground fault is applied on the ac bus and waveforms are obtained using the proposed and full detailed model for comparison. A low impedance resistive fault is applied between the converter ac terminal and the system impedance (point ‘a’ in Figure 5-6) at 1.0 s.

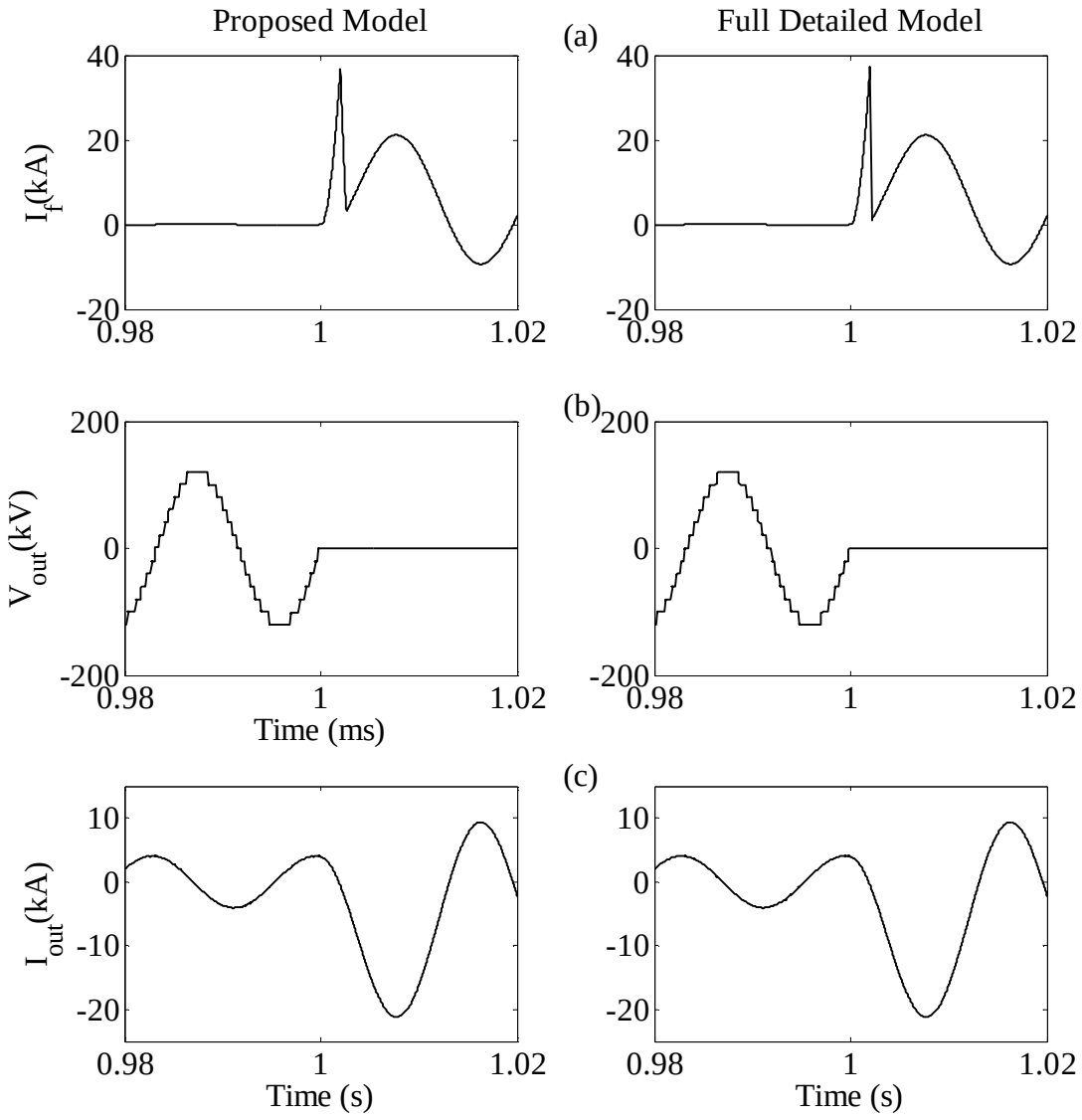


Figure 5-9: MMC waveforms comparison during an ac fault of the converter:

(a) Fault current, (b) MMC output voltage, and (c) AC system current

The fault current, converter ac terminal voltage and system ac currents are shown in Figure 5-9 and both models show identical results also in this analysis.

5.2.2 CPU Efficiency

To measure the CPU (central processing unit) efficiency of the proposed equivalent model, a 5 second period is simulated with a simulation time-step of 20 µs. The simulations are conducted on a Microsoft Windows 7 Professional (64-bit) platform with a 3.10 GHz Intel Core i5-2400 CPU, 4.00 GB of RAM running PSCAD X4 (Version 4.4.1.0). Table 5-1 tabulates the CPU times for the proposed equivalent model and the full detailed model for different number of half-bridge sub-modules.

Table 5-1: Time comparison of MMC models with half-bridge sub-modules

No. of Half-Bridge Sub-Modules (Per Multi-Valve)	Run Time (S)		Speed Up Ratio (%) (Full/Proposed)
	Full Detailed Model	Proposed Equivalent Model	
2	7	2	350
6	11	2	550
12	22	12	183
24	50	13	385
48	291	15	1940
72	924	18	5133
96	3799	20	18995
120	6695	24	27896

The data are also plotted on a semi-log graph in Figure 5-10 to provide a more visual comparison. As the number of half-bridge sub-modules grows, the CPU time of the full detailed model grows at a much faster rate than that of the proposed equivalent model. For 120 half-bridge sub-modules per multi-valve (*i.e.* 240 in total), the detailed simulation takes approximately two hours whereas the proposed model takes 24 s, a speedup of 27,896 % or over 278 times faster.

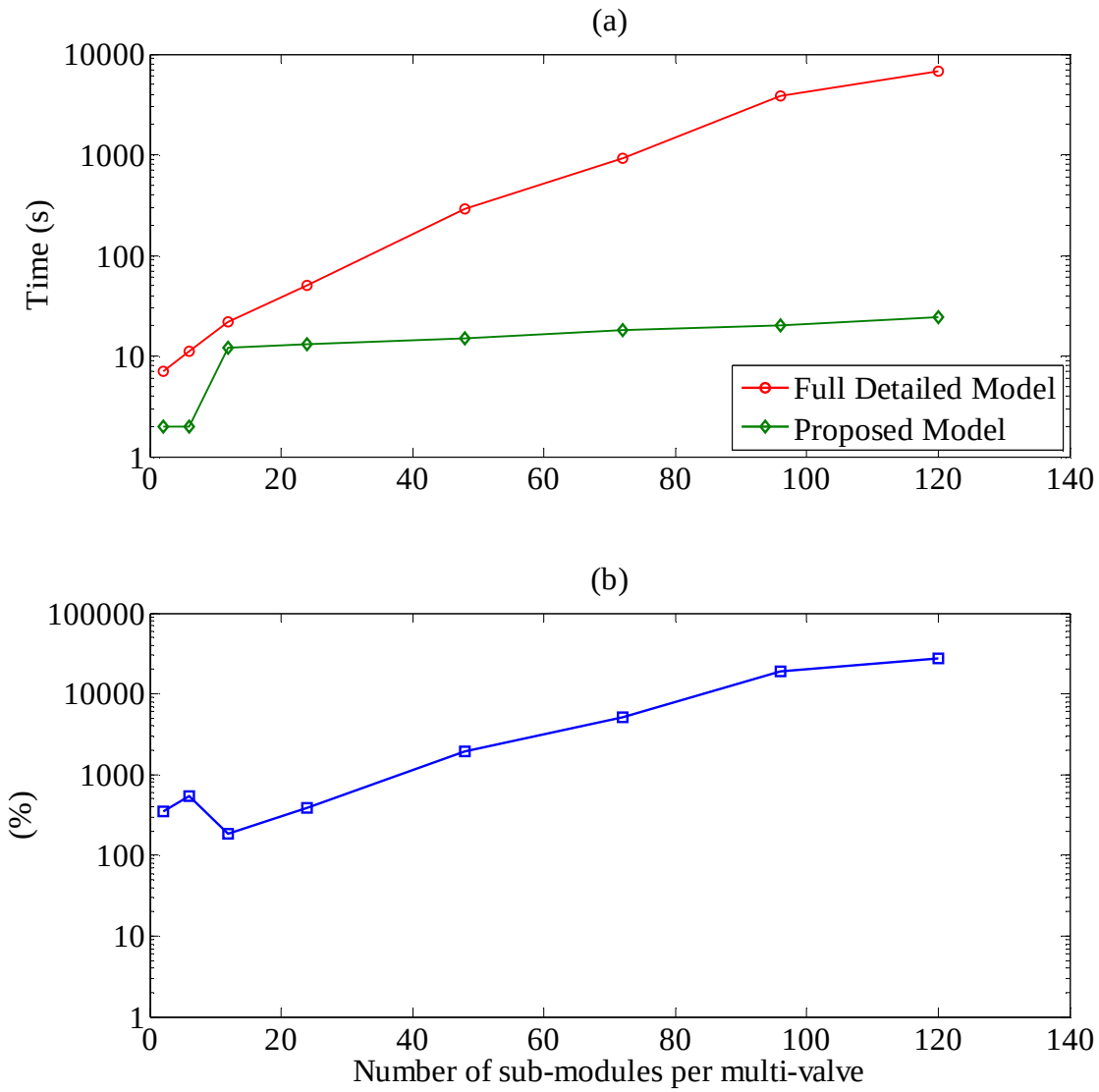


Figure 5-10: Run time efficiency of proposed equivalent model:

(a) CPU Times for full detailed model and proposed equivalent model and (b) Speed-up ratio

1. Time Comparison for Different Numerical Integration Methods

The trapezoidal rule has been traditionally used in EMT solvers to construct a time-domain Norton equivalent model of typical power system elements [79] as mentioned in section 4.2. The form for the half-bridge sub-module equivalent derived in

Equation (4-13) uses this method. One of the main advantages of the trapezoidal rule is that it is "A-stable" and reasonably accurate. A-stability implies that the method does not diverge for any time-step [86], assuming that the actual system is stable.

However, recently there have been other A-stable methods used for obtaining the equivalent that claim superior accuracy to trapezoidal integration. The Two–Stage–Diagonally Implicit Runge–Kutta (2S-DIRK) is one such method [87]. This method is presented in Appendix B.

In addition to the conventional EMT approach of trapezoidal integration, the proposed equivalent is also implemented using this method. The CPU time measured for both the trapezoidal and 2S-DIRK integration methods of the proposed converter equivalent model is presented in Table 5-2. However, results show that 2S-DIRK approach did not make any significant difference to the speed or accuracy of the algorithm.

Table 5-2: Time Comparison for Different Integration Methods

No. of Half-Bridge Sub-Modules (Per Multi-Valve)	Run Time (S)	
	Trapezoidal Integration	2S-DIRK Integration
2	2	1
6	2	2
12	12	13
24	13	13
48	15	16
72	18	19
96	20	21
120	24	24

5.3 MMC with Full–Bridge Sub-Modules

Similar to the above comparisons, the performance of the proposed equivalent model for the full-bridge converter is also compared against the full detailed model.

5.3.1 Accuracy

The full detailed model and the proposed model are simulated under different operating conditions to assess the accuracy of the proposed equivalent model. For this comparison, only a single phase is modeled. The converter ac terminal is connected to a fixed load; R_{out} is equal to 50 Ω and L_{out} is 120 mH. A constant dc voltage source of magnitude 150 kV is connected at the converter dc terminals. The module capacitance is equal to 5000 μF and each multi-valve has 10 full-bridge sub-modules in these simulations.

A range of different scenarios are conducted as is done for the half-bridge sub-modules earlier but only two candidate scenarios are presented. All scenarios result in identical simulation between the full detailed model and the proposed equivalent model.

1. Simulation during Steady State Operation

In this test, the converter waveforms are obtained for the steady state operation of the converter models. Figure 5-11 shows waveforms for a module capacitor voltage (the top-most module in the upper multi-valve), converter output voltage, output current and upper multi-valve current for comparison. The waveforms obtained from the proposed

equivalent model and from the full detailed model are essentially identical. Therefore, the proposed equivalent model can be successfully used in simulation of the MMC with full-bridge sub-modules.

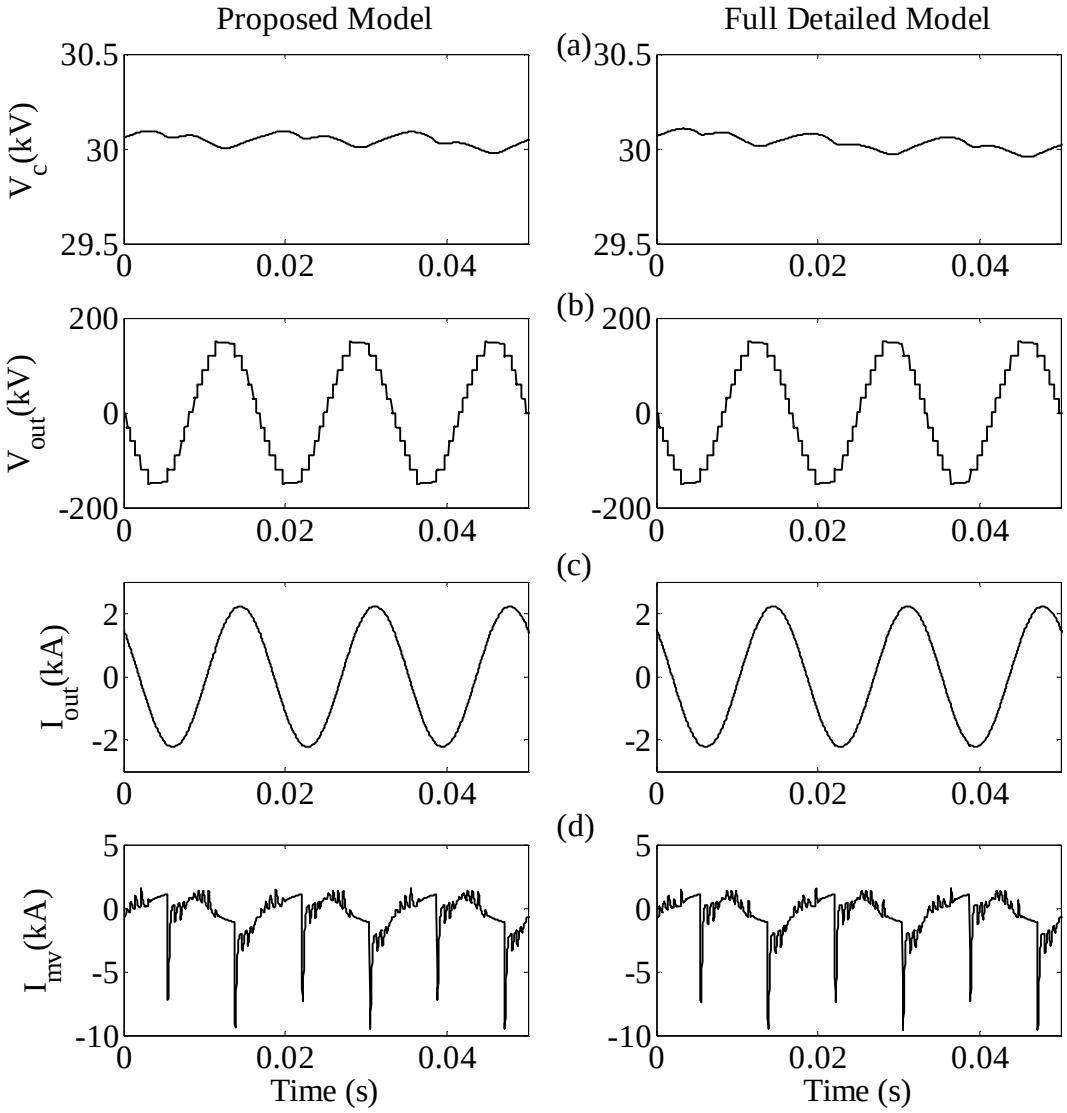


Figure 5-11: MMC waveforms comparison during steady state operation:

(a) Full-bridge sub-module capacitor voltage, (b) MMC output voltage, (c) Output current, and (d) Upper multi-valve current

2. Simulation during a Firing Failure

The waveforms are compared after one of the lower switches of the full-bridge sub-module (TB1 in Figure 4-9(a)) fails i.e. it is permanently turned 'OFF' at 0.03 s. the converter output voltage, output current, and upper multi-valve current are shown in Figure 5-12 for comparison. This example also shows that the proposed equivalent model can be accurately used to simulate the firing failures.

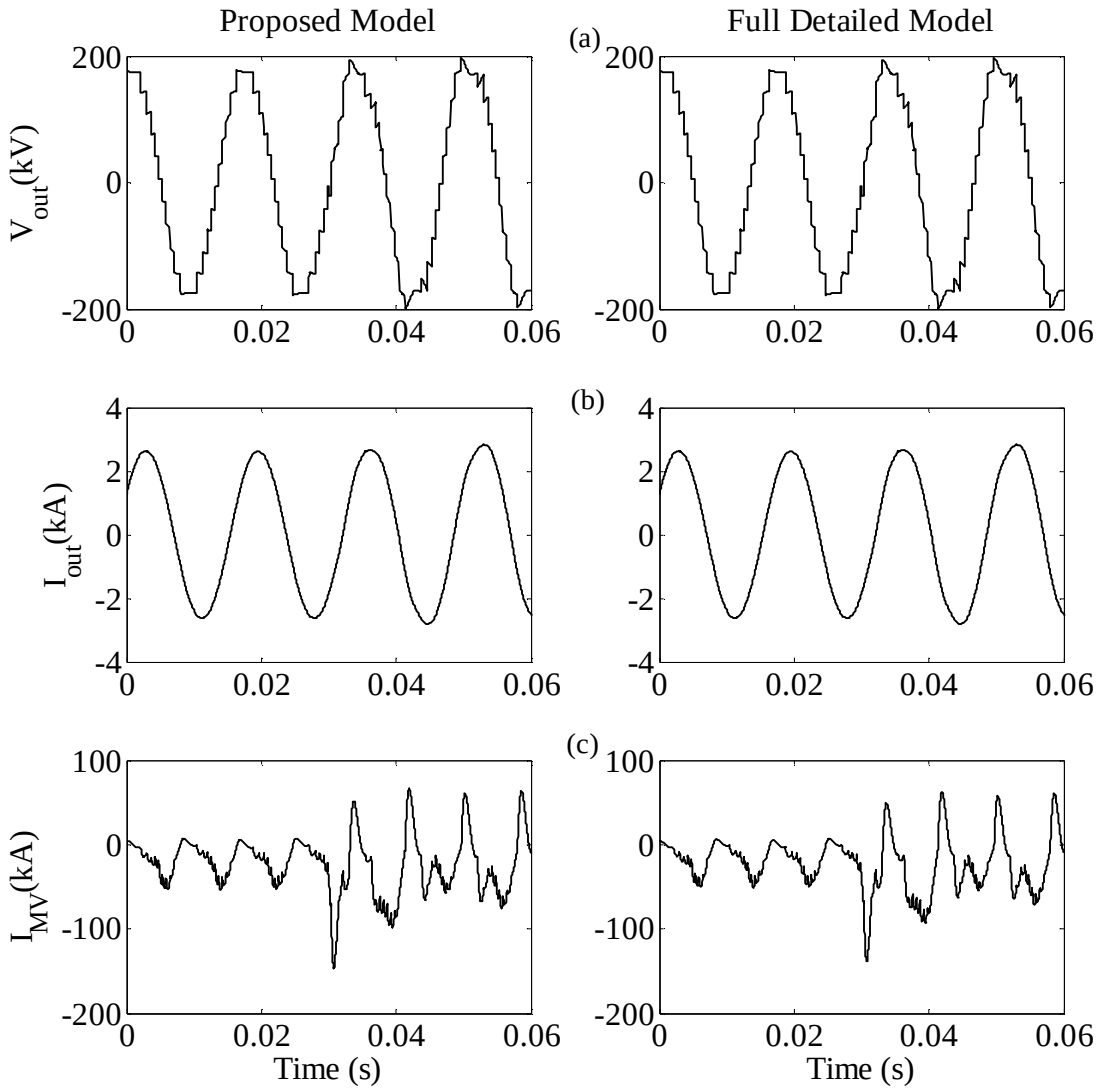


Figure 5-12: MMC waveforms comparison during firing failure:

(a) MMC output voltage, (b) Output current, and (c) Upper multi-valve current

5.3.2 CPU Efficiency

A 5-second period is simulated with a simulation time-step of 20 μs. The simulations are conducted on a Microsoft Windows 7 Professional (64-bit) platform with a 3.10 GHz Intel Core i5-2400 CPU, 4.00 GB of RAM running PSCAD X4 (Version 4.4.1.0).

Table 5-3 tabulates the CPU times for the proposed equivalent converter model and the full detailed model for different number of full-bridge sub-modules.

Similar to the speed-up ratio measured for the half-bridge converter module case, when the number of full-bridge sub-modules grows, the CPU time of the full detailed model grows at a much faster rate than that of the proposed model. For 120 full-bridge sub-modules per multi-valve (*i.e.* 240 in total), the detailed simulation takes more than twelve hours whereas the proposed model takes 24 s, a speedup of 185,775 % or over 1857 times faster.

Table 5-3: Time comparison of MMC models with full-bridge sub-modules

No. of Half-Bridge Sub-Modules (Per Multi-Valve)	Run Time (S)		Speed Up Ratio (%) (Full/Proposed)
	Full Detailed Model	Proposed Equivalent Model	
2	4	1	400
6	12	2	600
12	27	3	900
24	91	4	2275
36	272	6	4533
48	725	8	9062
72	8149	12	67908
96	27602	17	162365
120	44586	24	185775

5.4 Comparison of Average Valued Model

The performance of the average valued model is analysed by simulating two single phase converter models under different operating conditions to assess the accuracy of the

proposed average model against the full detailed model. The converter ac terminal is connected to a fixed load; R_{out} is equal to 50 Ω and L_{out} is 120 mH and a constant dc voltage source of magnitude 120 kV is connected at the converter dc terminals. The module capacitance is equal to 3000 μF. The full detailed model has 24 half-bridge sub-modules in the phase arm.

1. Simulation during Normal Steady State Operation

The MMC output voltage, output current, upper multi-valve current and voltage of the equivalent average capacitor are shown in Figure 5-13 for the steady state operation. The capacitor voltage waveform for averaged model is $\overline{V_c}/N$, where $\overline{V_c}$ is the total capacitor voltage and N is the number of sub-modules. This allows comparison with a typical waveform of an individual capacitor in the detailed model. The results show that converter output waveforms (Figure 5-13(a) and (b)) of the average model are essentially identical to those of the full detailed model. The behaviour of the converter internal variables such as multi-valve current waveform and capacitor voltage waveform (Figure 5-13(c) and (d)) reasonably match, though less closely with the results of the full detailed model. This is because the representation of all capacitor as a single capacitor is an approximation and cannot give the detailed waveforms of current and voltage in any typical capacitor. However from the system point of view as seen in Figure 5-13(a) and (b), the accuracy is excellent.

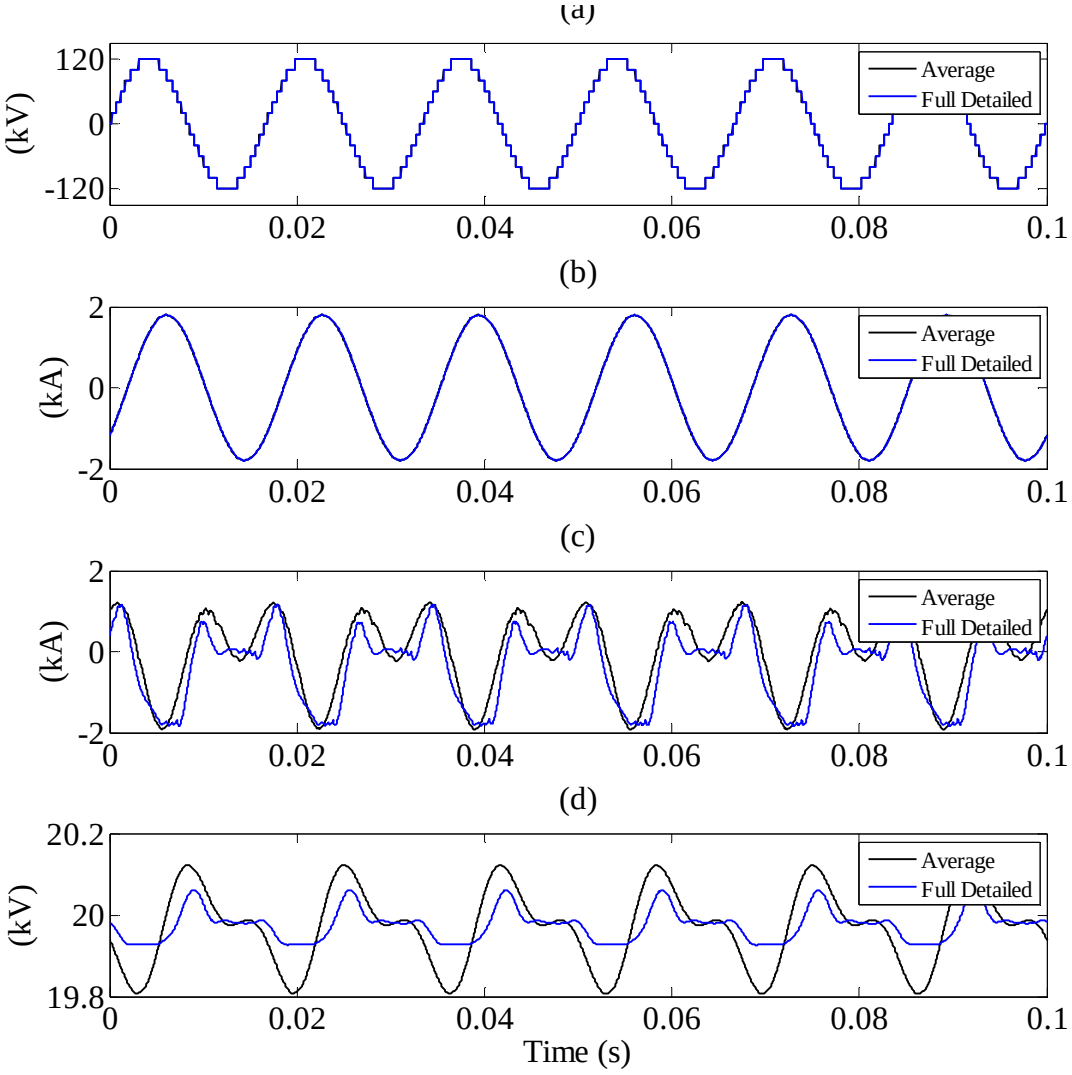


Figure 5-13: MMC waveforms comparison during normal operation:

(a) MMC output voltage, (b) Output current, (c) Upper multi-valve current, and (d) average capacitor voltage (avm) and typical capacitor voltage (full detailed)

2. Simulation during AC Line Fault

In this test, a ground fault is applied on the ac bus and waveforms are obtained using the proposed average model and full detailed model for comparison. A low impedance resistive fault is applied at the converter output terminals at 1.5 s. This test also shows

that the average valued model can be used to study the average behaviour of the converter during the ac line faults. Note that a large deviation of the multi-vale current can be seen in the results. However, external system level waveforms are an excellent match. So, it is not recommended that this model can be used for multi-valve current limit determination etc.

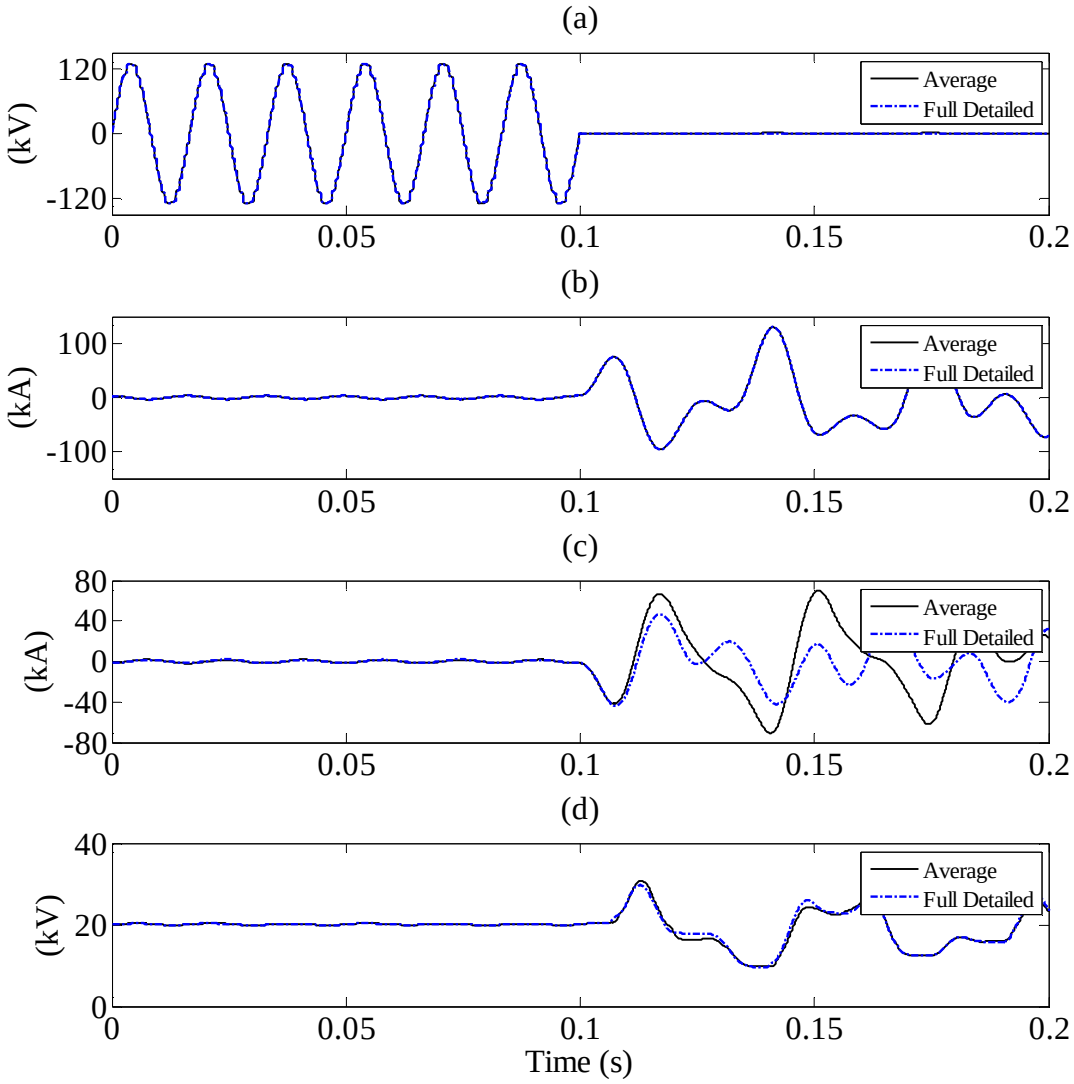


Figure 5-14: MMC waveforms comparison during ac line fault:

(b) MMC output voltage, (b) Output current, (c) Upper multi-valve current, and (d) average capacitor voltage (avm) and typical capacitor voltage (full detailed)

3. Limitation of the average valued model

A number of tests are carried out to analyse the performance of the proposed average valued model but only the tests (discussed above) show a high accuracy in the results. Simulating dc faults and converter pulse blocking are still a challenge in this proposed model. Figure 5-15 shows waveforms between detailed and average valued model for a dc line fault. The discrepancies between the full detailed model and average model can be clearly shown in the converter output waveforms and multi-valve currents in Figure 5-15. The commutation process of the IGBT/diode switch combination is not properly modelled in the proposed average valued model and the uncontrollable current flow during the dc line fault can cause these differences in the waveforms.

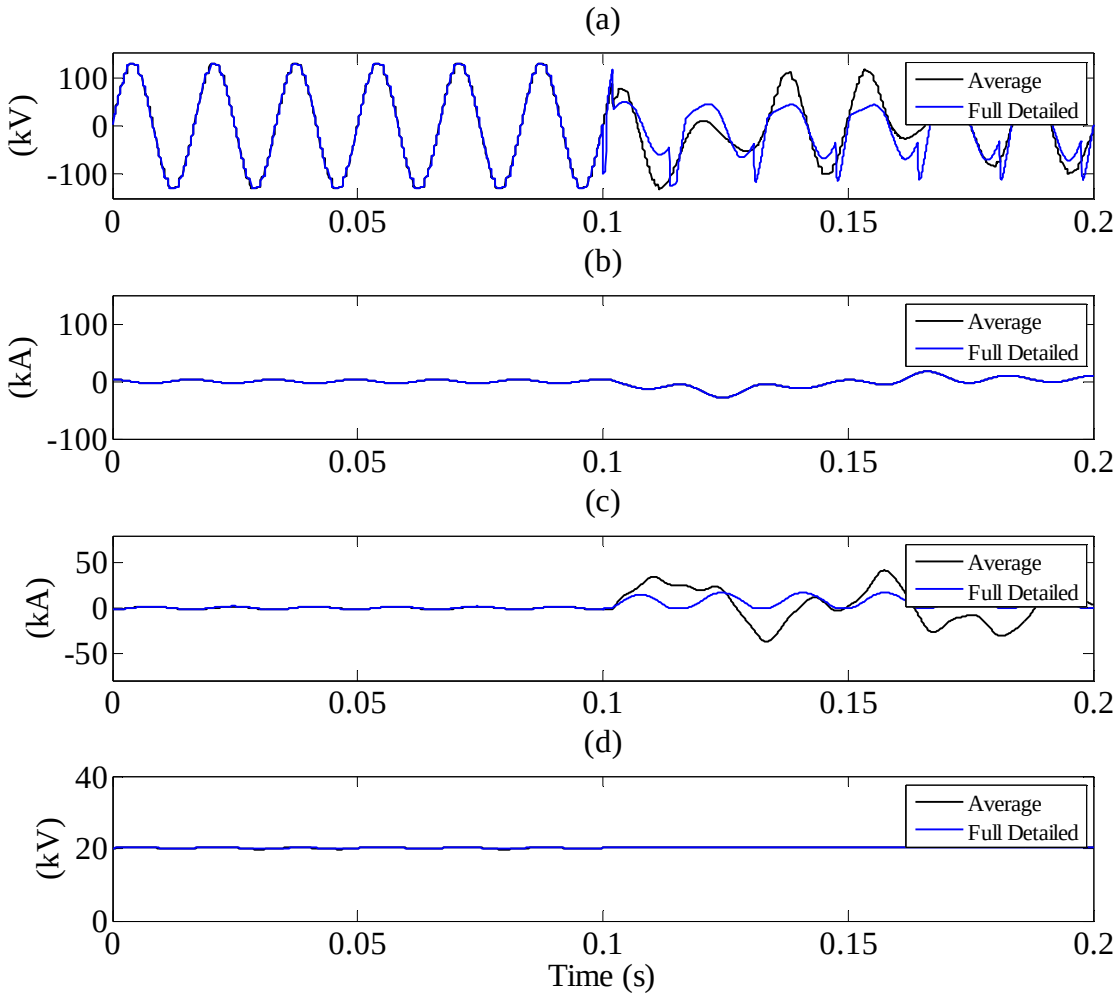


Figure 5-15: MMC waveforms comparison during dc fault:

(a) MMC output voltage, (b) Output current, (c) Upper multi-valve current, and (d) average capacitor voltage

At present, the proposed average model shows good steady state and transients' results except for dc faults. It could therefore be used in a range of studies such as HVDC controller tuning and recovery from ac faults. However, the high speed Thévenin equivalent MMC model developed in this thesis can handle any situation and could be used for more difficult cases. The improvement of the average valued model to handle dc faults etc. is kept for future researchers.

Modeling a Point to Point MMC based HVDC System

6.1 Introduction

This chapter uses the proposed equivalent model in the time domain simulation of a complete point to point MMC based HVDC transmission system. The simulation has 100 sub-modules in each multi-valve, totalling 1200 modules considering both sending end and receiving end converters. To simulate such a system with the traditional approach, each module individually in full detail would have been prohibitive in CPU time. The chapter shows that the power of the proposed approach can achieve the simulation.

6.2 MMC Based HVDC System Configuration

A block diagram of a typical MMC based HVDC system, designed to transfer power between two ac systems through a dc link is shown in Figure 6-1 [88] [65]. The MMC based HVDC system (Figure 6-1) is schematically similar to the conventional two-level VSC based HVDC system (Figure 2-6). However, the principal differences between the

MMC based HVDC system and conventional two-level VSC based HVDC system can be seen in the ac filters, soft starting resistors, and dc capacitors as discussed below.

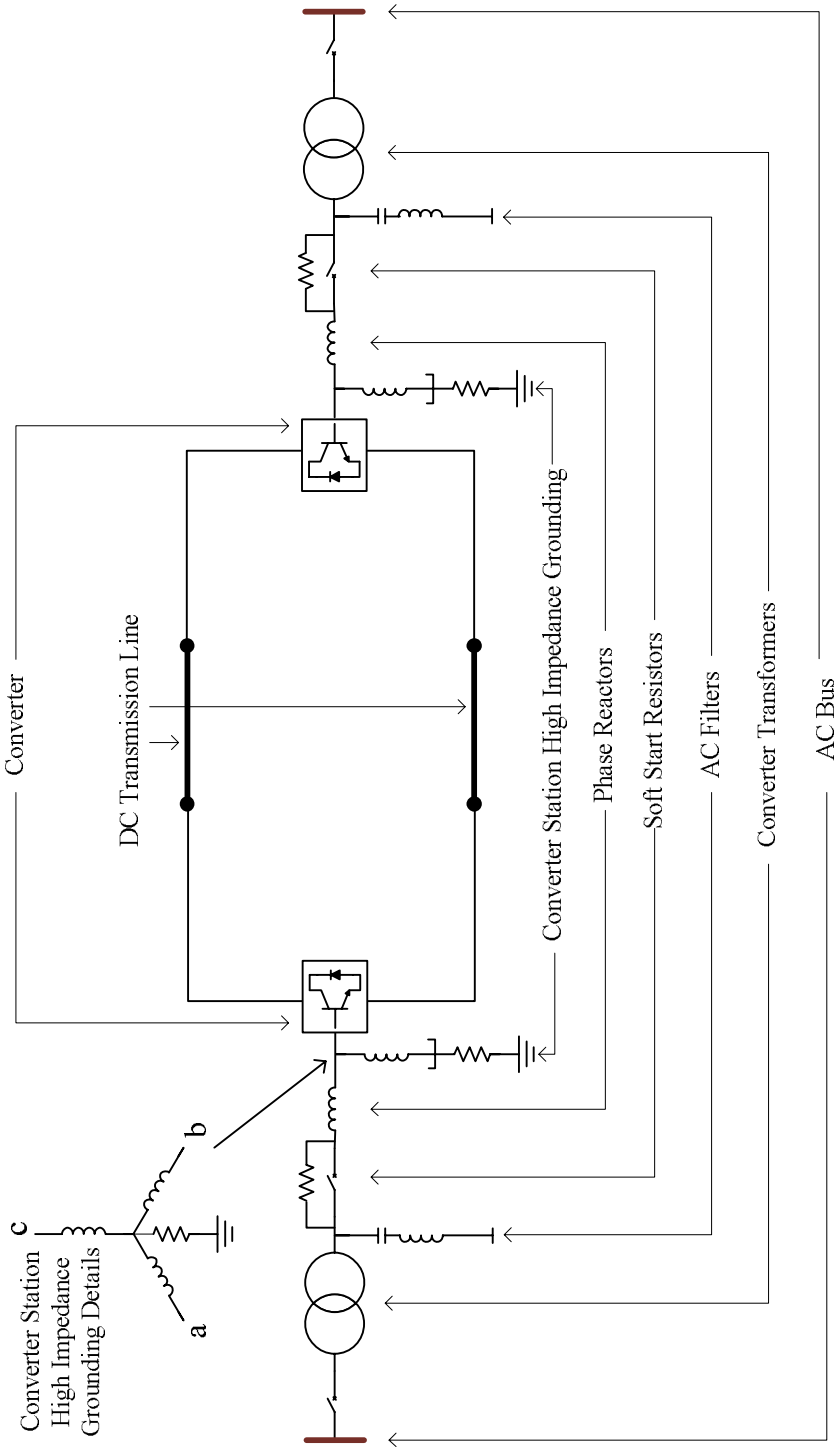


Figure 6-1: Schematic diagram of MMC based HVDC system

1. AC Filters

AC filters are usually not required in MMC applications as the converter output waveform is essentially sinusoidal. However, a small ac filter (L-C filter) can be added to the converter ac terminal if the number of voltage levels used is small and all the harmonic requirements are not satisfied for a certain design of MMC based HVDC system [72], [89].

2. Converter Station Grounding

One distinctive characteristic of the MMC is that its arm currents are continuous. Therefore, the dc bus capacitor is not strictly required. The module capacitors act as energy storages and the MMC can be operated without additional capacitors installed in the dc link [7], [70] . If this is done, the converter ground reference cannot be provided by grounding the midpoint of dc link capacitors such as in conventional 2-level converters.

In this MMC topology, the converter station is grounded through star-shaped inductance grounding equipment [90] in the ac side, as shown in Figure 6-1.

3. Soft Starting Resistors

A breaker with a pre-inserted resistor is added to each phase of MMC to limit the charging current of module capacitors during the converter start-up and restoring. During the capacitor charging process, the capacitor behaves like a short circuit, when the capacitor has zero charge initially. This results in drawing a very high initial charging current from the converter bus. Addition of the extra resistance into the charging current path can keep the initial current within acceptable limits for other devices connected in the path such as converter transformer and phase reactor. When the capacitors are

charged to the desired voltage level, the resistor is bypassed from the circuit. The value of the resistor is determined by considering a number of parameters such as the total number of sub-modules, module capacitance, and maximum allowable charging current of the system [91].

6.3 Simulation of MMC Based HVDC Transmission System

6.3.1 Simulation Model

Using the proposed MMC model, a simulation case is developed for a symmetrical mono-pole HVDC transmission system as shown in Figure 6-2 to evaluate the performance of the proposed MMC model when simulating the dynamic performance of the system. In this simulation model, the ac system is modeled using a Thévenin equivalent voltage source and impedance. Bus 1 (Bus_1) and bus 2 (Bus_2) are rated at 230 kV and 115 kV respectively. The Thévenin impedance is determined so that the SCR (short circuit ratio) of both ac systems is equal to 2.5. The impedance is mostly inductive but has a resistive component providing an impedance angle of 80° at fundamental frequency. The dc system is rated at 400 MW and ±200 kV. These voltage and power ratings are similar to the "Trans Bay Cable Project" which is the world's first commercial operation of MMC based HVDC transmission system [77]. In this scheme, MMC_1 operates as a rectifier feeding the dc link. The receiving-end converter MMC_2 operates as an inverter and converts the dc link power back to ac.

Typically, an actual MMC converter can consist of 100 (or more) half-bridge sub-modules per multi-valve [70]. To be consistent with these numbers, 100 modules are used in a multi-valve in this simulation model. This large system would have been extremely challenging to model using the traditional approach on present day personal computers without an approach such as the one developed in this thesis. Therefore, the proposed equivalent model is used to model the MMC in the simulation. The complete system data for this HVDC system is presented in Appendix C.

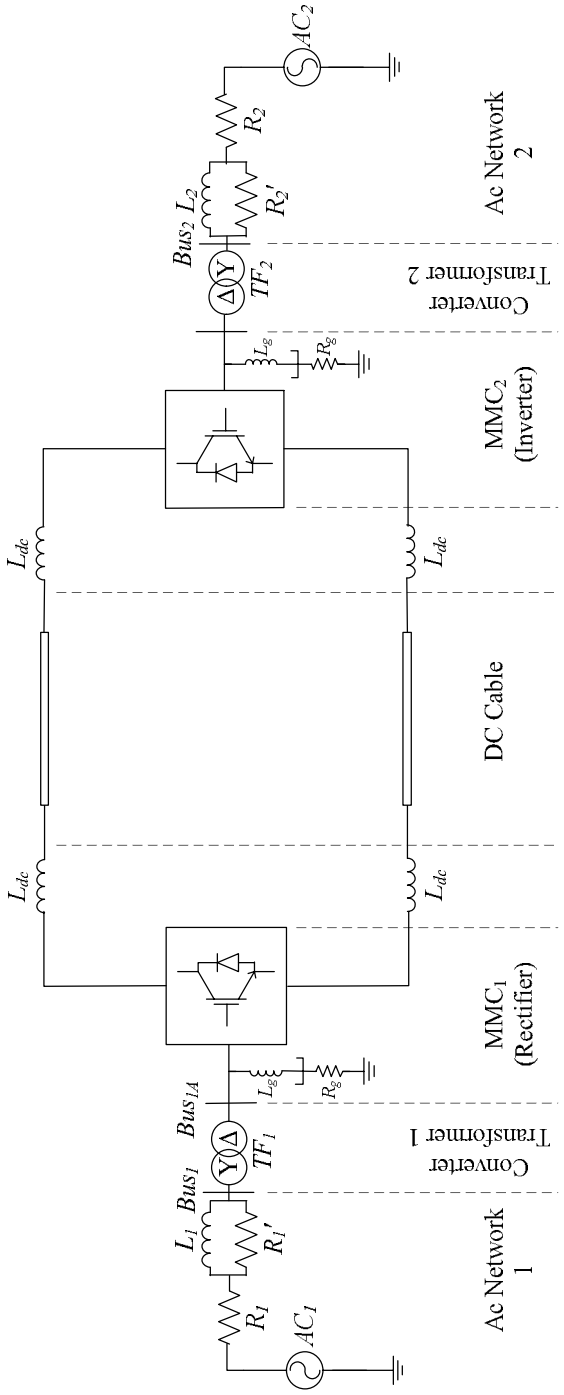


Figure 6-2: MMC based HVDC system

6.3.2 Controls for MMC Based HVDC System

As the MMC is essentially a controllable ac voltage source, converter voltage magnitude can be controlled via the modulation index, '*m*' and phase angle of the voltage offset δ. The direct control strategy [92] is applied for the system controllers. The advantage of the direct control strategy is its simplicity. The converter MMC_1 is responsible for controlling the dc voltage and Bus_1 ac voltage. MMC_2 operates in the power control mode and regulates the power transfer.

1. Rectifier Side Controller:

The dc voltage is regulated by control of the phase shift angle, δ_1 between the VSC generated converter side ac voltage waveform at Bus_{1A} and the ac system voltage waveform at Bus_1 in Figure 6-2. The phase locked loop (PLL) tracks the angle θ of the fundamental positive sequence phase voltage. The regulated angle, δ_1 is added with the PLL angle θ to determine the phase angle of converter terminal voltage with respect to the phase angle of the bus voltage. This effectively changes the real power flow between the ac bus and the converter bus. The local bus-bar voltage is also maintained at its reference by controlling the magnitude of Bus_{1A} waveform via the modulation index, m_1. These signals (δ_1, m_1) are generated via the proportional-integral (PI) control loops shown in Figure 6-3. They are then fed to the reference signal generator which generates three sinusoidal reference signals for the firing controller of MMC as described in section 3.4.

The angle from the PLL is used to synchronize the turning 'ON'/'OFF' of the power devices and to calculate and control the flow of active/reactive power [93], [94].

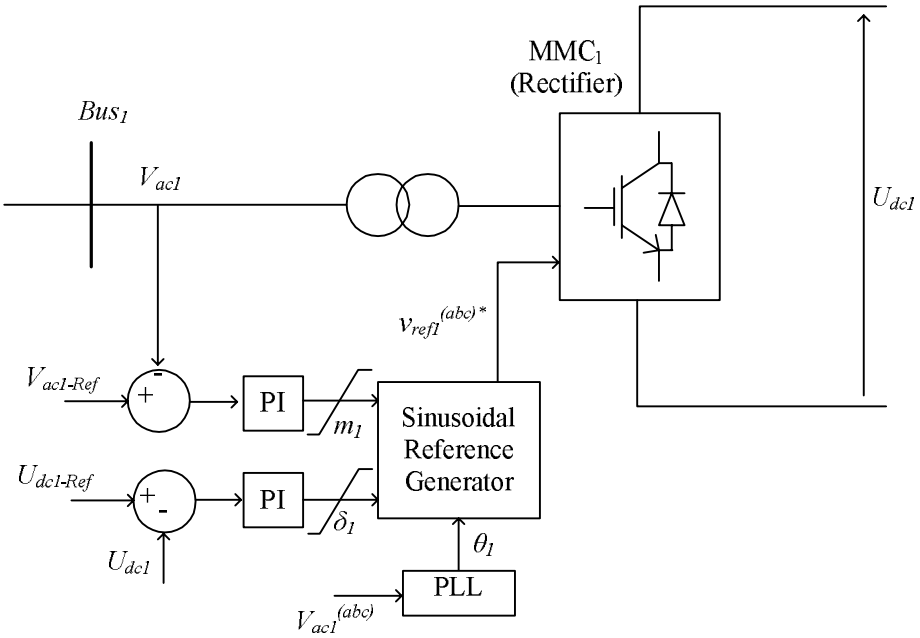


Figure 6-3: Rectifier side converter controller

2. Inverter Side Controller:

The structure of the inverter side controller is shown in Figure 6-4, and is similar to that of the rectifier controller. The main difference is that the delay angle, δ_2 is generated from the power error signal, which is the difference between the ordered power, P_{Ref} and the measured power, P at Bus_2. The modulation index, m_2 as in the rectifier controller regulates the ac bus bar voltage. Similar to the rectifier side controller, three sinusoidal reference signals are internally generated for the firing controller of MMC_2.

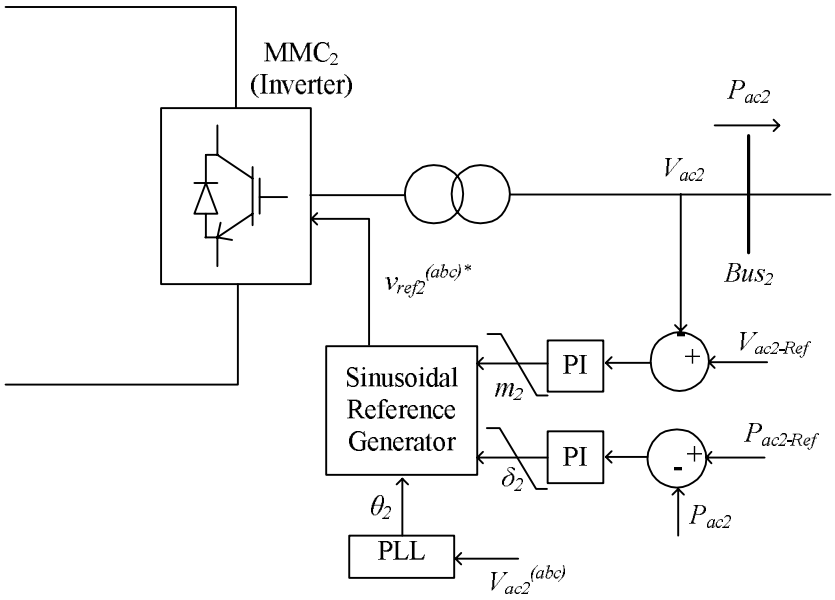


Figure 6-4: Inverter side converter controller

6.3.3 Simulation of a Power Order Change of HVDC System

Figure 6-5 shows the converter ac and dc waveforms of rectifier and converter sides when the power order is changed from 1 pu to 0.5 pu (*i.e.:* from 400 MW to 200 MW). Waveforms of the real power measured at the inverter bus, inverter bus (Bus_2 in Figure 6-2) voltage, dc voltage at the rectifier side, and rectifier bus (Bus_1 in Figure 6-2) voltage are shown. These results show that the power order change (to 90% of final setting) can be achieved in 60 ms, with less than 10% fluctuation in the ac or dc voltages. The dc voltage is restored to within 5% of its rated value in about 500 ms.

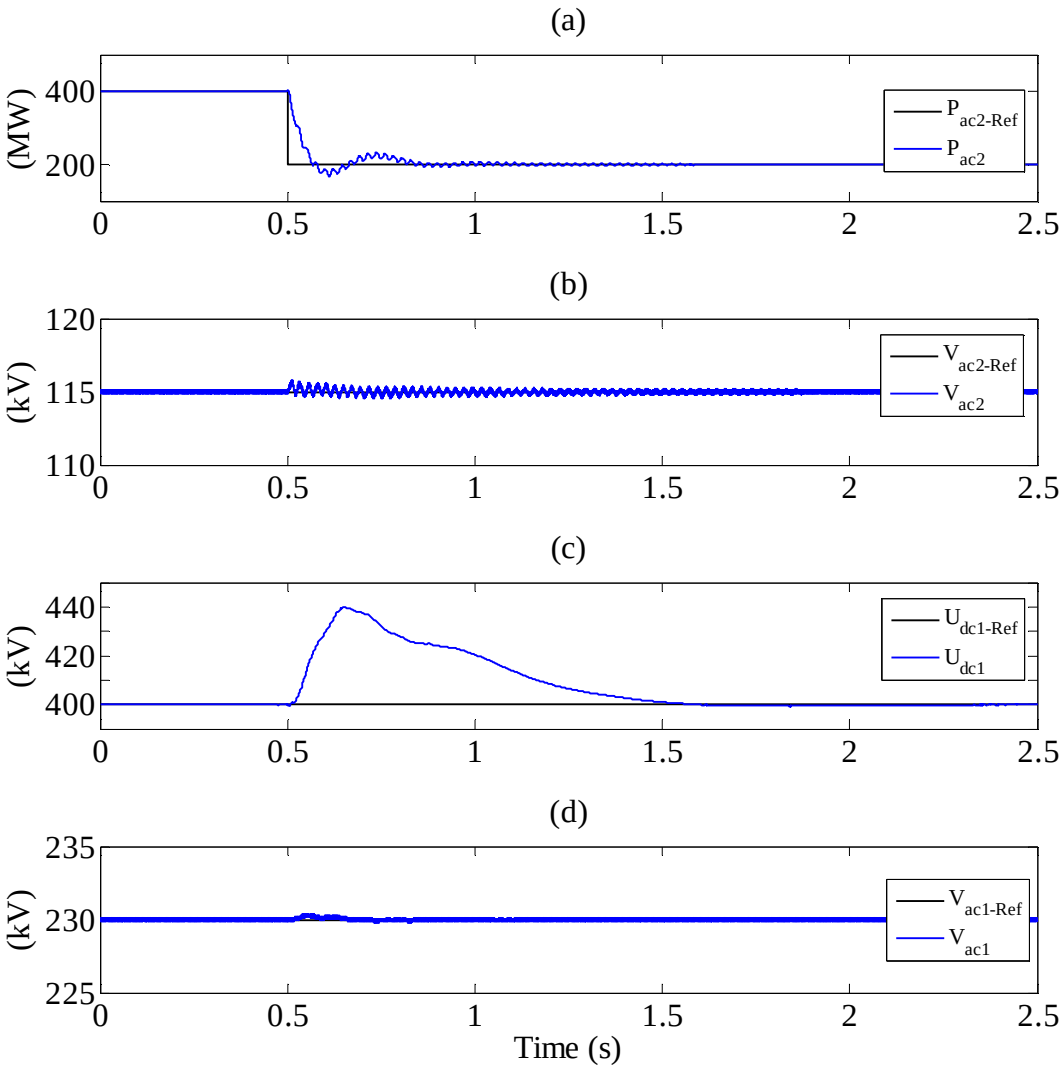


Figure 6-5: Comparison of system responses for change in power reference from 1pu to 0.5pu: Inverter side (a) Power, (b) Busbar1 voltage, and Rectifier side (c) DC voltage, d) Busbar2 voltage

The actual waveforms of rectifier side ac voltages on the valve side and ac system side, as well as the line currents are shown in Figure 6-6. The MMC output waveforms are effectively sinusoidal, even though there are no ac filters. It is noted that the changes in current and voltage on the rectifier side due to the power order change on inverter side appear with a small time delay. However, the time axis used in Figure 6-6 is not large

enough to observe the voltage and current transients in the waveforms. These simulations demonstrate that the proposed equivalent converter model can be effectively used in the simulation of full HVDC systems.

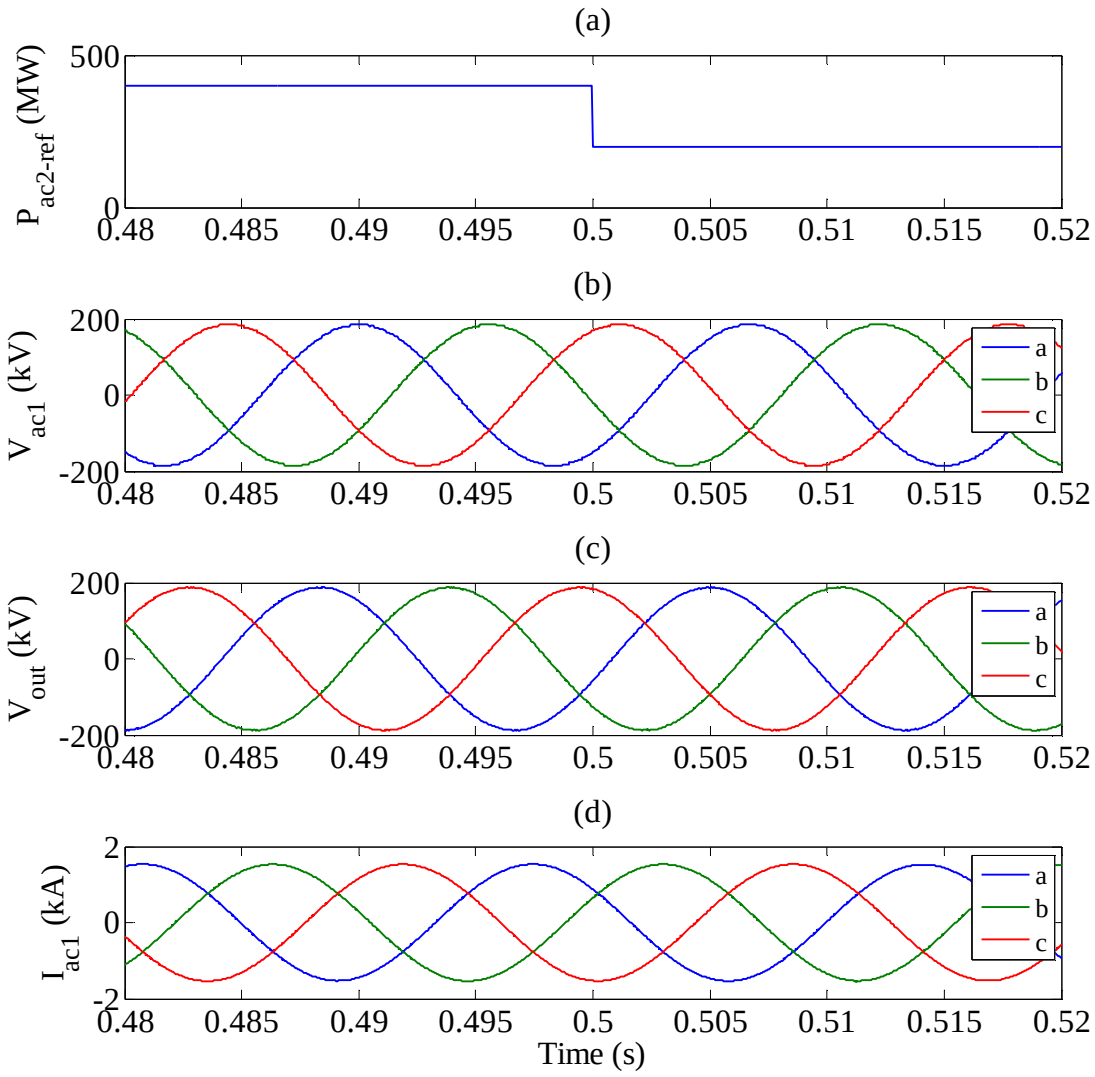


Figure 6-6: Rectifier side ac voltage and current waveforms of MMC based HVDC system: (a): Power order change, (b) Valve side voltages, (c) AC system side voltages, and (d) AC line currents

6.3.4 Simulation of a Line to Ground Fault at Inverter side AC Bus

A 6-cycle duration (100 ms) line-to-ground fault is applied at 0.5 s, to the inverter side bus bar (Bus_2 in Figure 6-2) on phase 'A'. The system responses of the inverter bus real power, inverter ac bus voltage, rectifier side dc voltage, rectifier ac bus voltage, and upper sub-module capacitor voltages of rectifier and inverter ends are shown in Figure 6-7. The results show that the inverter station is still able to maintain its pre-fault dc link power during the fault. The system can be restored back to steady state operation within 0.45 ms after the fault is cleared. As the two ac systems are decoupled through the dc link, the disturbance applied in the inverter side makes a relatively small impact on the rectifier side dc voltage or ac bus voltage.

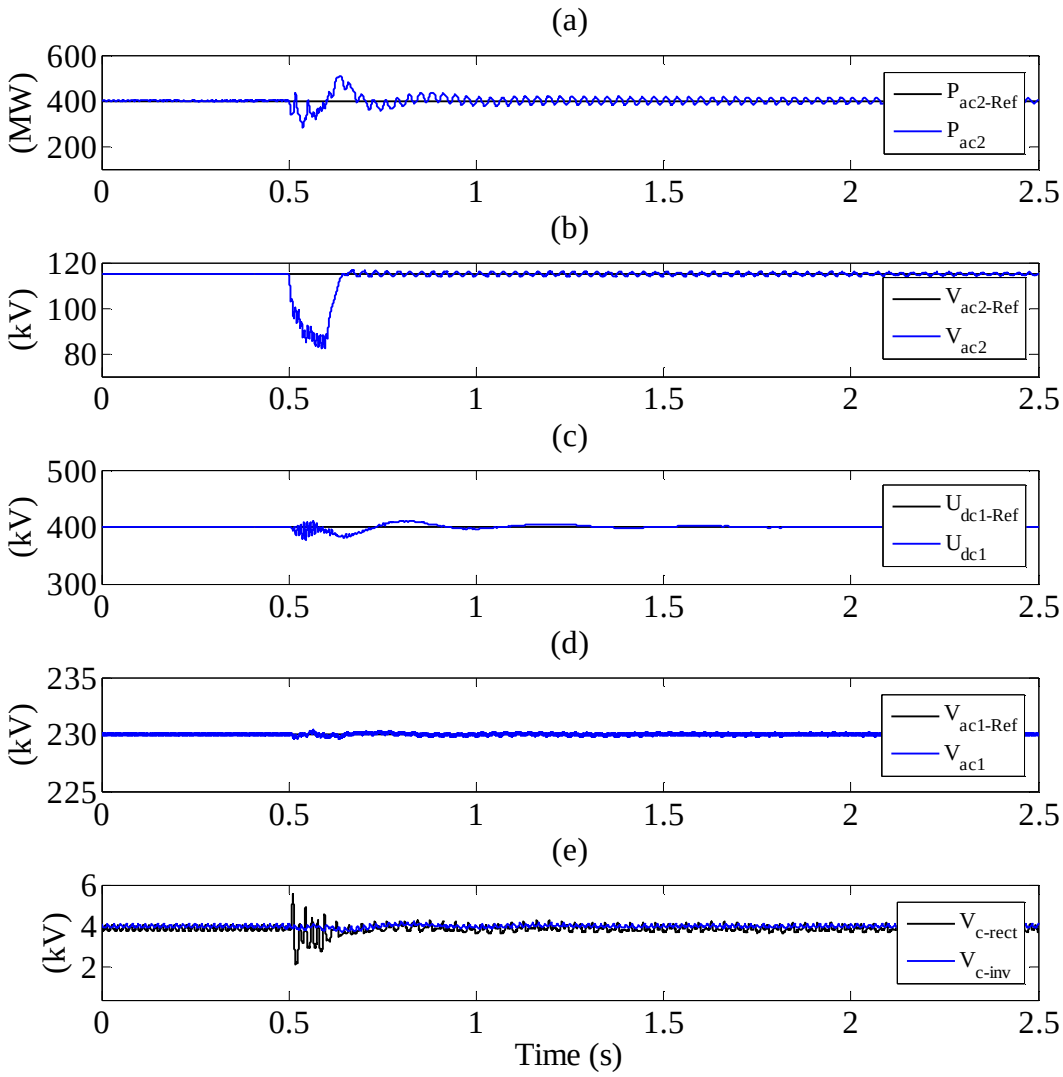


Figure 6-7: System responses during an ac line to ground fault on inverter bus: Inverter side (a) Power, (b) Busbar1 voltage, Rectifier side (c) DC voltage, (d) Busbar2 voltage, and (e) Sub-module capacitor voltages

6.3.5 Simulation of a DC Pole to Ground Fault

In this test, a permanent ground fault is applied on the positive dc pole at 75 km away from the rectifier end and the system responses observed during the fault transient are

shown in Figure 6-8. The fault current immediately reaches to a maximum of about 5 kA after the fault is applied at 0.05 s and starts decreasing as shown in Figure 6-8(a). Figure 6-8 (b) shows that the dc power transmission continues without an interruption due to the pole to ground fault applied on the dc cable. The module capacitor voltages also remain unchanged during the fault as shown in Figure 6-8 (c).

A significant impact due to the fault can be observed on the measured dc pole voltages for this ground fault. When the fault is applied on the positive dc pole, the faulty (positive) pole voltage reduces to zero and the healthy (negative) pole voltage increases to 2 pu as shown in Figure 6-8 (d). Even though, the 400 MW power transmission is not interrupted in this case, the 2pu voltage increase on the healthy pole of the cable can initiate additional insulation failures on the cable. Therefore, the voltage must be restored to the rated value as quickly as possible to prevent further damages to the cable. One way to isolate the faulted cable from the system is to open the ac breakers at both ends of the system.

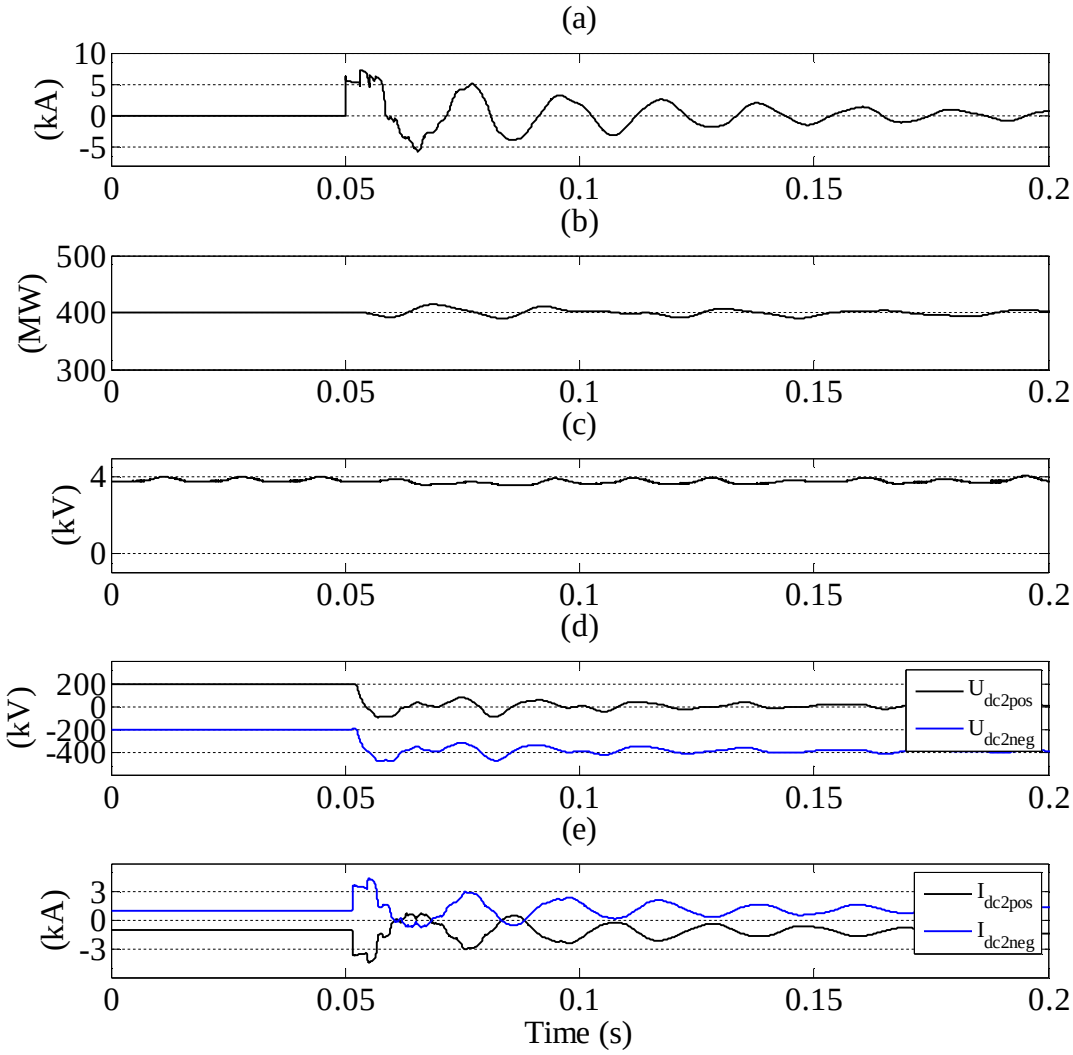


Figure 6-8: System responses during a dc pole to ground fault:

(a) Fault current, (b) Inverter bus real power, (c) Sub-module capacitor voltage, (d) Rectifier side dc voltage, and (e) Rectifier side dc current

6.3.6 CPU Efficiency – HVDC System Simulations

The CPU run time is measured for a 5 second run of full HVDC system simulations at 20 μs solution time-step as in section 5.2.2. By comparing the CPU run times for the full detailed model and the proposed equivalent model as shown in Table 6-1, the CPU

efficiency of the proposed equivalent model becomes clear. With 96 half-bridge sub-modules, the estimated CPU time with the traditional approach would be over 5 days, whereas it is less than 1.5 minutes with the proposed method. The 5 days of CPU run time was estimated by conducting a short duration run (0.5 s). Needless to say, the full detailed simulation is not practical for systems with sub-modules in the range of 100 or more.

Table 6-1: Time Comparison of MMC-HVDC Simulation

Half-Bridge Sub–Modules/ Multi–Valve	Run Time (s)		Speed Up Ratio (%) (Trad./Equival.)
	Full Detailed System	Proposed Equivalent System	
12	375	20	1875
24	5993	28	21404
96	452150 (estimated)	78	579679

The proposed equivalent model was also used successfully to study large system such as connection of offshore wind power plants. This work was done in collaboration with Dr. S. K. Chaudhary and Dr. R. Teodorescu of Aalborg University and is reported in [95]. This shows the usefulness of the proposed equivalent model in simulation of large networks with MMC.

Switching Loss Estimation of Modular Multilevel Converters

7.1 Introduction

The proposed equivalent model developed in earlier chapters did not have details of the semiconductor switch. However, an approach developed by Rajapakse and Gole [96] can be adapted to make the MMC model report losses. This is the subject of this chapter.

In this section, the operating losses of the MMC converter are estimated using a time domain simulation approach described in [96]. This method considers only the pre- and post- switching voltage and current values, and interpolates the wave-shape between these instants using physics of the switching process, which lasts only about several hundreds of nanoseconds. Information required to conduct the interpolation can be obtained from datasheet values. The switching power loss is then readily calculated by multiplying these estimated waveforms. As this method has been developed for EMT type simulation program, the MMC losses can be estimated for steady-state operation, and also during transients and abnormal operating conditions. Using this comprehensive approach, the effect of circuit parameters on converter losses can also be studied.

In this study, the steady state operating losses of MMC and the impact of converter output waveform synthesis methods (as discussed in section 3.3) on the losses are investigated. Finally, the operating losses of half-bridge sub-module, MMC based HVDC systems are compared with the conventional, two-level VSC based HVDC systems.

At present, the method is only implemented with the full detailed model. The example below uses a 13-level MMC. The results of this section can be used to compare losses for different types of MMC switching control methods and to compare MMC losses with those that would occur with a conventional two-level VSC.

7.2 Converter Switching Loss

The converter switching loss is contributed by the losses of switching devices and can be grouped into three main categories:

7.2.1 Conduction Losses

Conduction losses arise due to the 'ON' state resistance as the 'ON' state voltage across the device is not zero. The conduction dissipations are computed in a straightforward manner by multiplying the 'ON' state voltage by the 'ON' state current as given in (7-1).

$$P_{on}(t) = V_{on}(t) \cdot I_{on}(t) \quad \textbf{7-1}$$

where,

$V_{on} = \text{ON - state voltage}$

$I_{on} = \text{ON - state current}$

7.2.2 Off-state Losses

Similarly, 'OFF' state losses are calculated using the leakage current and device blocking voltage during the 'OFF' state as in (7-2).

$$P_{off}(t) = V_{off}(t) \cdot I_{off}(t) \quad \textbf{7-2}$$

where,

V_{off} = OFF-state voltage

I_{off} = OFF-state current (leakage current)

7.2.3 Switching Transient Losses

a) Turn 'ON' losses

b) Turn 'OFF' losses

The calculation of switching transient losses is a challenge, as the switching transient event occurs over a very short time period (about 100-200 ns). Therefore, it is difficult to accurately capture switching transients; particularly with the several micro-second time-step used in typical electromagnetic transients (EMT) simulations of power electronic systems.

However, the approach developed in [96] estimates the switching period waveforms from the pre- and post- switching voltages and currents and semiconductor datasheet information without explicit simulation. The losses can then be calculated by analytical integration of the estimated waveforms, and have been shown to be relatively accurate [96]. Calculation details are given in Appendix D.

7.3 Loss Evaluation Model

The loss evaluation approach used in this study is schematically presented in Figure 7-1 [96]. The model has been implemented in the PSCAD/EMTDC simulations program. The switching device model available in the host program has been modified to capture more parametric data which are input to the device loss estimation model. The losses in the device are estimated by observation of the pre- and post-switching currents and voltages using the algorithm described in Appendix D [97].

The algorithm fills in the intermediate sub-microsecond values of voltage and current during the larger simulation time-step (tens of micro-seconds). The intermediate values are derivable from the pre- and post–switching voltages, currents, and other physical data. Thus, the EMT type simulation can be conducted with a larger time-step with the developed formula providing an estimate of the loss at each switching.

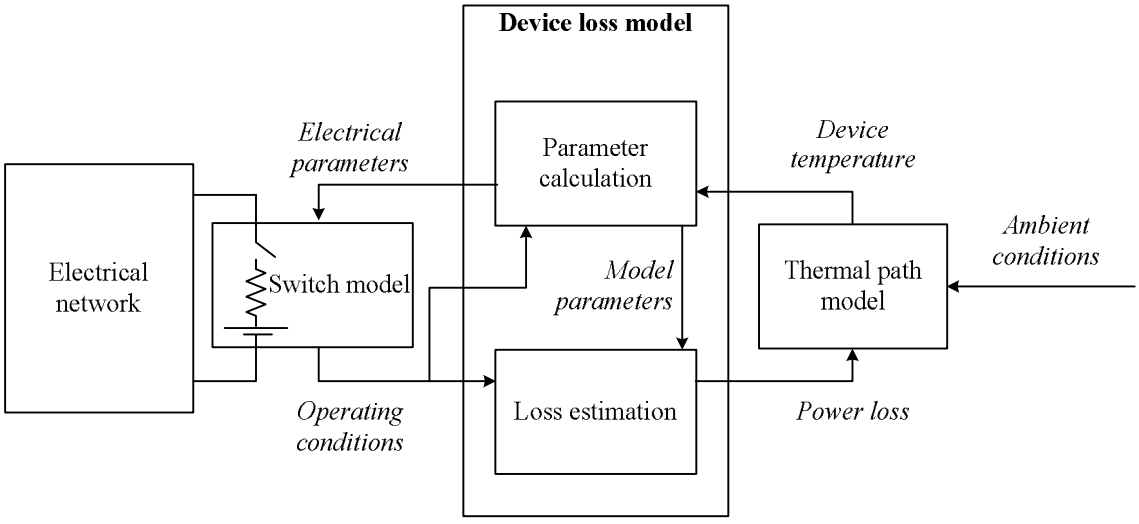


Figure 7-1: Block diagram of the device loss estimation model

These estimated losses, are the inputs to a dynamic model of the heat-management system (thermal path) which computes the temperature changes in various parts of the system. Because the device losses are functions of temperature, the computed device temperature is then used to change the parameters of the switch loss model for the next time-step [96].

7.3.1 Thermal Model of IGBT

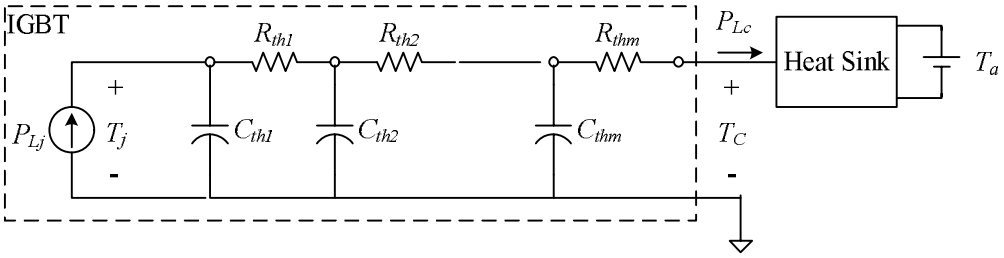


Figure 7-2: Equivalent thermal network of a semiconductor switching device

From a thermal point of view, the IGBT can be represented by a lumped parameter equivalent circuit as in Figure 7-2 [96]. Here, the power loss of the device is P_{Lj}, the junction and case temperatures are T_j and T_c respectively. R_{thi} and C_{thi} represent the thermal resistance and capacitance of various layers of the semiconductor device. The number of stages usually depends on the number of materially different layers in the thermal path. The approach to extract these thermal parameters is discussed in detail in Appendix D. In this study, the heat sink model is not considered however, a constant (ambient) temperature is input as the case temperature assuming the heat sink maintains the constant temperature input. Because the device losses are function of temperature, the computed device temperature is then used to change the parameters of the switch loss model for the next time-step.

7.4 MMC Loss Evaluation

The switching loss model developed in [96], [97] is applicable to IGBT devices subject to “hard switching”. In hard switching during the turn ‘ON’ and turn ‘OFF’ processes, the power device has to withstand high voltage and current simultaneously resulting in high switching loss and stress. The MMC switching elements, IGBTs are also subjected to hard switching and the proposed IGBT switching model [96], [97] can be directly applied to estimate the power losses of MMC converters.

In this loss evaluation, the effect of two output voltage synthesis methods (a) nearest level estimation and (b) multilevel PWM is analysed. Note that these output voltage synthesis techniques are already discussed in section 3.3.

7.5 Comparison of Converter Losses

To evaluate the converter losses using the above approach, the inverter operation of a point to point HVDC system is simulated using the PSCAD/EMTDC program. The rectifier operation is modeled as a constant dc source and a detailed model for the inverter is used as shown in Figure 7-3. Two separate simulation cases are developed for half-bridge sub-module MMC and conventional two-level VSC converters for the comparison of resulting converter losses.

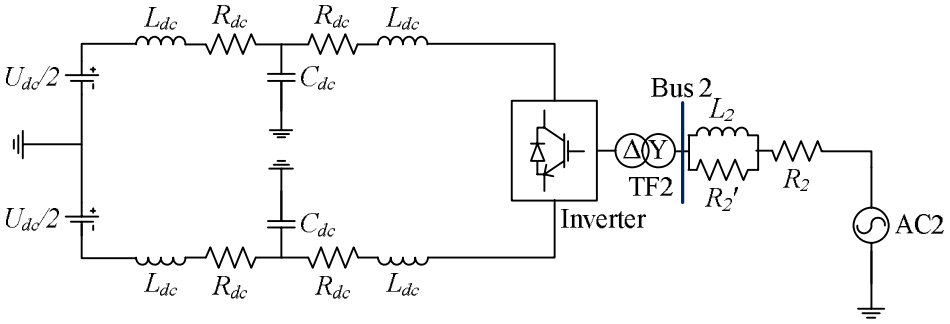


Figure 7-3: Equivalent inverter model of a HVDC system

7.5.1 MMC Based HVDC System

In this study, 24 half-bridge sub-modules (per phase) are used in each phase of the converter, thus it gives a total of 144 IGBT/diode semiconductor switches for a three phase converter. Each phase of the converter is modeled as shown in Figure 1-1 (see chapter 1). The dc system's ratings are selected as 25 MW and ±14 kV, which is the same power level used in Alstom's MaxSine demonstrator project [98]. As given in Equation (3-4), the rated sub-module voltage is equal to 2.33 kV. The inverter controller is responsible for regulating the power (25 MW) and ac voltage (15 kV) at Bus 2. Toshiba ST1500GXH24, rated at 4.5 kV/1.5 kA is chosen as the IGBT/Diode switch [99]. The blocking voltage of this switching device has a more than 93% of overvoltage limit.

The internal controls of the converters are used for capacitor voltage balancing and generation of firing signals as discussed in section 3.4. Two separate simulations are carried out for the two output voltage synthesis methods.

1. Nearest Level Estimation Based Approach

Figure 7-4 shows the resulting power loss and voltage waveforms when the nearest level estimation based method is used as the voltage balancing technique. This technique is already discussed in section 3.3. As shown in Figure 7-4(a), the converter power loss that is estimated using the method discussed in section III is equal to 0.23 MW per converter or 0.46 MW considering both the rectifier and inverter. This is 1.84% of the total transmitted power. Figure 7-4(b) shows the measured power and rms voltage at bus 2. The converter output voltage and top most sub-module capacitance voltage (phase A) are shown in Figure 7-4(c) and Figure 7-4(d) respectively. Calculation also shows the THD of the ac voltage waveform is 6.02%.

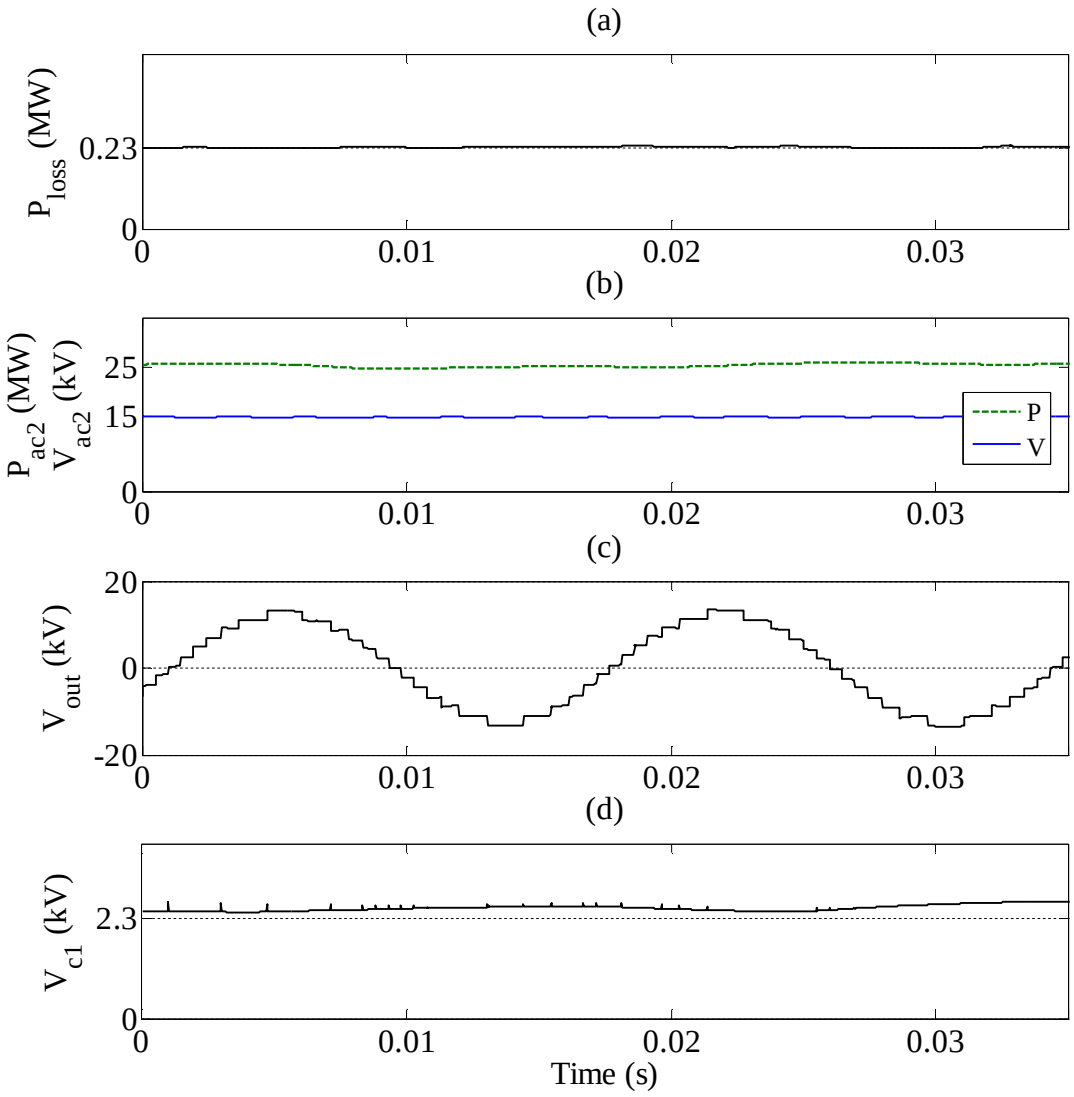


Figure 7-4: Loss estimation of MMC for nearest level estimation based approach: (a) Inverter side power loss, (b) Power and rms voltage at inverter side Bus 2, (c) Inverter output voltage, and (d) Top-most sub-module capacitor voltage of phase 'A'.

2. Multilevel Carrier-Based PWM

A similar analysis is carried out to estimate the power loss for the multilevel carrier based PWM, also discussed earlier in section 3.3.The resulting power loss and voltage waveforms are shown in Figure 7-5. As shown in Figure 7-5(a) and Figure 7-5(b), when

the converter transmits 25 MW, the resulting power loss for a single converter is 0.22 MW per converter, giving a total MMC system loss of 1.76% of the rated power. The converter output voltage and top most sub-module capacitance voltage (phase A) are also shown in Figure 7-5(c) and (d) respectively. Analyzing the ac voltage waveform yields a THD figure of 5.42%. In this test, the carrier frequency is chosen as 360 Hz to assure the fluctuation of sub-module capacitor voltages within the range of ±7.5%.

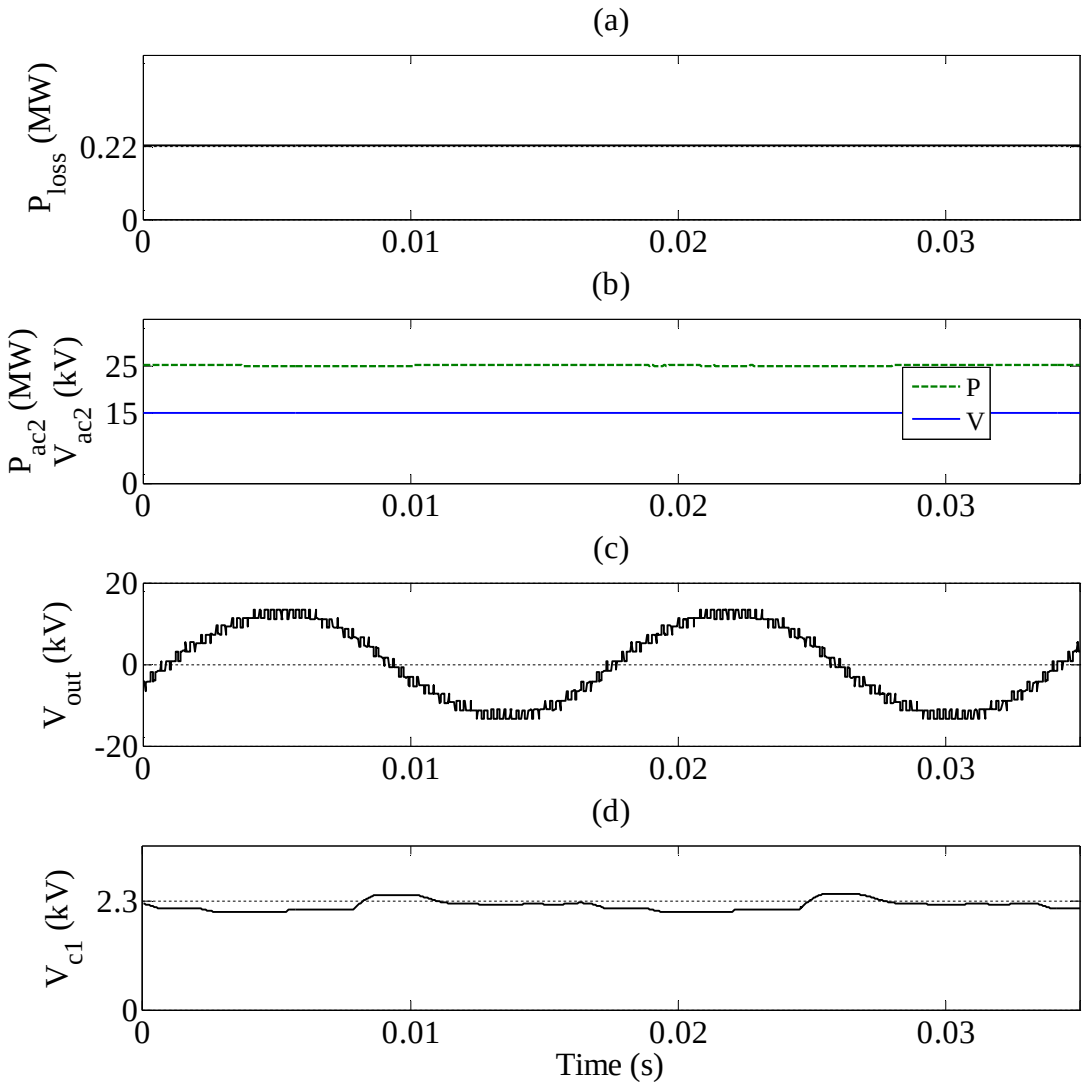


Figure 7-5: Power loss estimation of MMC for multilevel PWM based approach: (a) Inverter side power loss, (b) Power and rms voltage at inverter side Bus 2, (c) Inverter output voltage, and (d) Top-most sub-module capacitor voltage of phase 'A'.

7.5.2 Two-level VSC Based HVDC System

In this section, similar loss estimation is carried out for a two-level VSC based HVDC converter, shown in Figure 7-6. T_i's represented a group of series connected

IGBT/diode switches. To be comparable with the MMC based inverters, eight ST1500GXH24 switches (S_i) are used for the valve group (T_i) as shown in Figure 7-6. In this arrangement, the dc blocking voltage capability for each valve group is 36kV which is well above the rated dc voltage (28kV), giving 28.5% of overvoltage margin.

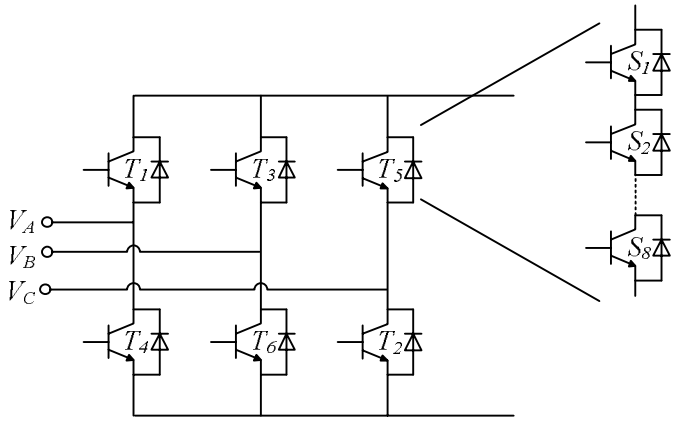


Figure 7-6: Two-level voltage sourced converter and valve group.

The output voltage waveforms are synthesized using the SPWM with the carrier frequency of 540 Hz (9 times the fundamental frequency). The converter losses are estimated using the same approach discussed above and the resulting waveforms are shown in Figure 7-7. As seen in Figure 7-7(a), the converter loss is equal to 0.32 MW per converter when 25 MW (Figure 7-7(b)) is transmitted giving 2.56% total power loss for the 2-level VSC. Figure 7-7(c) shows the unfiltered converter output voltage (phase), which has a THD value of 139%.

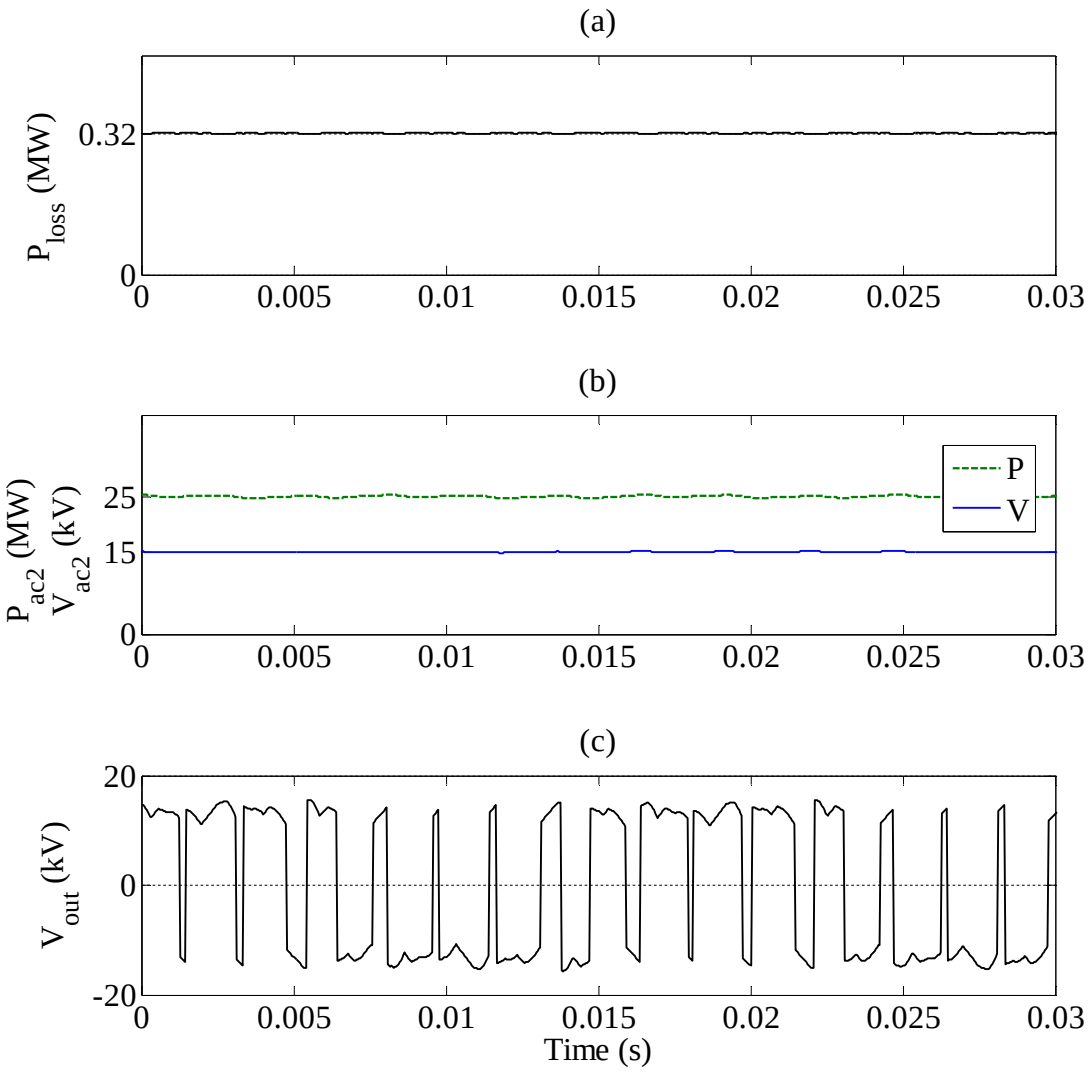


Figure 7-7: Power loss estimation of two-level VSC:

(a) Inverter side power loss, (b) Power and rms voltage at inverter side Bus 2, and (c) Inverter output voltage.

7.6 Results Summary

The approach in [97] can be adopted to investigate losses in MMC converters for different output waveform synthesis methods. Table 7-1 summarizes the converter power

losses and total harmonic distortion for different approaches discussed above. The power loss computed for a lower power setting is also presented. The results show that the converter power loss as a percentage of the transmitted power is marginally increased when the transmitted power is decreased. The power loss of the two-level VSC is significantly higher than the power loss of the MMC. The THD figures for the MMC are also significantly lower than that for the two-level VSC. For the MMC, the multilevel PWM method appears to have slightly less THD than the nearest level estimation based approach in this study.

Table 7-1: Converter power losses comparison.

Converter Type	No. of Sub-Modules/Phase	Power Loss per Converter (MW)	Total Power (MW)	HVDC System Power Loss (%)	THD (%)
MMC (Nearest level estimation)	24	0.23	25	1.84	6.02
	24	0.20	20	2.00	5.82
MMC (Multilevel PWM)	24	0.22	25	1.76	5.42
	24	0.20	20	2.00	5.40
2-VSC (SPWM)	N/A	0.32	25	2.56	139
	N/A	0.29	20	2.90	141

Conclusions and Recommendations for Future Research

8.1 Conclusions

An approach for modeling modular multilevel converters with a very large number of switching devices was introduced in thesis. The simulation results showed that the proposed equivalent model can drastically reduce the computational time without loss of accuracy. The proposed model was used to simulate a point to point HVDC transmission system for several applications and showed that it could be used effectively in full network simulation cases.

The following major contributions are made in this thesis:

- Using the 'Nested Fast and Simultaneous Solution' algorithm, an approach for modeling MMC was introduced for EMT simulations. The approach was based on a Thévenin equivalent representation for the converter phase arm of MMC with half–bridge sub-modules. The approach was extended to an MMC with full–bridge sub-modules as well. The ability to maintain the individual identity of every sub-module is a distinct advantage of the proposed equivalent model in detailed simulation of the converter in EMT programs.

- Several time domain comparisons were carried out using the proposed equivalent model and a full detailed model to evaluate the accuracy and the run time efficiency of the proposed model. The speed-up factor in CPU run time of the proposed equivalent model increased with the number of sub-modules and was typically higher than two orders of magnitude for a large sub-module count.
    - For the half-bridge sub-module converter phase, the detailed simulation took approximately two hours whereas the proposed equivalent model took 24 s, a speedup of 27,896 % or over 278 times faster when the multi-valve consists of 120 half-bridge sub-modules.
    - The detailed simulation took more than twelve hours whereas the proposed model took only 24 s, a speedup of 185775 % or over 1857 times faster for MMC with 120 full-bridge sub-modules per multi-valve.
- The proposed equivalent model was able to reproduce the identical results for the cases considered in this thesis.
- Using the proposed MMC equivalent model, a complete point-point MMC based HVDC transmission system was studied in EMT environment. The simulation had 100 sub-modules in each multi-valve, totalling to 1200 modules considering both sending end and receiving end converters. Simulating such a system using the traditional approach would have been

prohibitive in CPU time in a present day personal computer. The study results showed that the proposed equivalent model can be effectively used in full network simulations.

- In the MMC, a mechanism for voltage balancing is essential. The function of the capacitor voltage balancing controller is to maintain all sub-module capacitor voltages at the same value, i.e. to equalize the capacitor voltages. Possible methods for doing this were described and demonstrated through the use of simulation. The capacitor voltage balancing controller was rapidly able to restore balanced capacitor voltages.
- Using a specially designed switching model, the converter losses of a MMC based HVDC system were evaluated. The simulation results showed that the power losses of the MMC based HVDC system are about 1.8 percent of the total transmitted power. When comparing the losses of MMC based HVDC system and those of conventional, two-level VSC based HVDC system; the two-level VSC had 45 percent higher power losses. The losses were also marginally sensitive to the output waveform synthesis methods.
- With the assumption of ideal switch operation and using an equivalent average capacitor value based approach, an average model of MMC was introduced in this thesis. The proposed average model was able to accurately model steady state behaviour and ac system faults, but not successful in modeling dc side faults and in converter pulse blocking.

- Several operational aspects of MMC were discussed in this thesis. MMC output waveform synthesis methods (nearest level estimation and multilevel PWM) were discussed and modeled for an EMT program. The harmonic content was computed for each output waveform method. The sizing of sub-module capacitance was analysed using the output waveform of MMC. Also, a second harmonic current filter was implemented to successfully suppress the harmonics on the MMC arm current.

The minor contributions:

- The thesis also investigated some lesser important aspects.
    - Determination of capacitance size to limit distortion of output waveforms.

      It was found that a per-unit capacitance size of 30ms or larger would be able to meet the permissible voltage ripple requirement of the capacitor voltage waveform.
    - Determination of number of levels to keep within acceptable harmonics limits.

      The results of a case study showed that with more than 22 sub-modules per multi-valve, all harmonic limits are satisfied when the nearest level estimation approach is used and with 25 sub-modules per multi-valve using the multilevel PWM approach.

8.2 Future Work

Prior to progress this research, there was no efficient way to simulate an MMC based HVDC system in EMT programs. The proposed MMC equivalent model has created great potential for the research and development of the field of VSC based HVDC systems. Several applications that the proposed equivalent model can be effectively used are listed below;

- Performance study of existing capacitor voltage balancing algorithms
- Development of new capacitor voltage balancing algorithms
- Engineering design of MMC systems
- Fault current analysis in MMC based HVDC systems
- Development of HVDC control algorithms, more suitable to the MMC

Although the efficient modeling approach was developed for the specific case of the MMC, it is easily adaptable for the EMT simulations of other power-electronic convertor topologies with very large switch counts.

Developing a solution to represent a MMC dynamic behaviour using an average model is challenging and complicated. The average MMC model originated in this thesis can be further developed to successfully simulate dc faults and other transients.

Including interpolation to better represent the precise switching instant can be investigated as a further development to the proposed model. If the interpolation is added it is possible to use a slightly higher time which can potentially achieve even faster CPU run time in the simulation.

However, the process of interpolation itself adds more computation so the exact time savings (if any) will need to be further investigated.

8.3 Thesis Publications

The contribution of this thesis has led to the following publication;

- U. N. Gnanarathna, A. M. Gole, and R. P. Jayasinghe, "Efficient Modeling of Modular Multilevel HVDC Converters (MMC) on Electromagnetic Transient Simulation Programs," *IEEE Transactions on Power Delivery*, vol.26, no.1, pp.316-324, Jan. 2011.
- U.N. Gnanarathna, A.M. Gole, A.D. Rajapakse, and S.K. Chaudhary, “Loss Estimation of Modular Multi-Level Converters using Electro-Magnetic Transients Simulation”, International Conference on Power System Transients, IPST-2011, Delft, The Netherlands, Jun. 2011.
- U. N. Gnanarathna, S. K. Chaudhary, A. M. Gole, and R. Teodorescu, “Modular Multi-level Converter Based Hvdc System for Grid Connection of Offshore Wind Power Plant”, 9th International Conference on AC and DC Power Transmission IET London UK, Oct. 2010.

- U. N. Gnanarathna, A. M. Gole, and S. K. Chaudhary, “Multilevel Modular Converter for VSC-HVDC Transmission Applications: Control and Operational Aspects”, 16th National Power Systems Conference, NPSC-2010, Hyderabad, India, Dec. 2010.

Appendix A

User Guide of the Proposed MMC Models Developed in PSCAD/EMTDC Simulation Program

A.1 Half-Bridge Sub-Module Equivalent Model

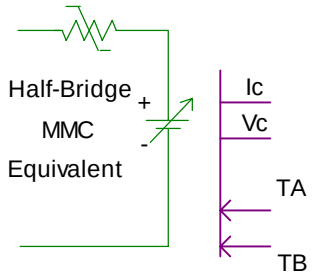


Figure A-1: PSCAD block of proposed equivalent model for MMC multi-valve with half-bridge sub-modules

The connection ports of the PSCAD block are described below.

Connection Ports:

Vc: Outputs the capacitor voltage values which are internally calculated in the Thévenin equivalent solver. This is a real variable and the dimension is equal to the number of modules.

Ic: Outputs the capacitor currents which are internally calculated in the Thévenin equivalent solver. This is a real variable and the dimension is equal to the number of modules.

TA: Inputs the firing signals vector for the upper switches in each module. This is an integer variable with the dimension equal to the number of modules.

TB: Inputs the firing signals vector for the lower switches in each module. This is an integer variable with the dimension equal to the number of modules.

Input Parameters:

The input parameter list of the proposed MMC model is shown in

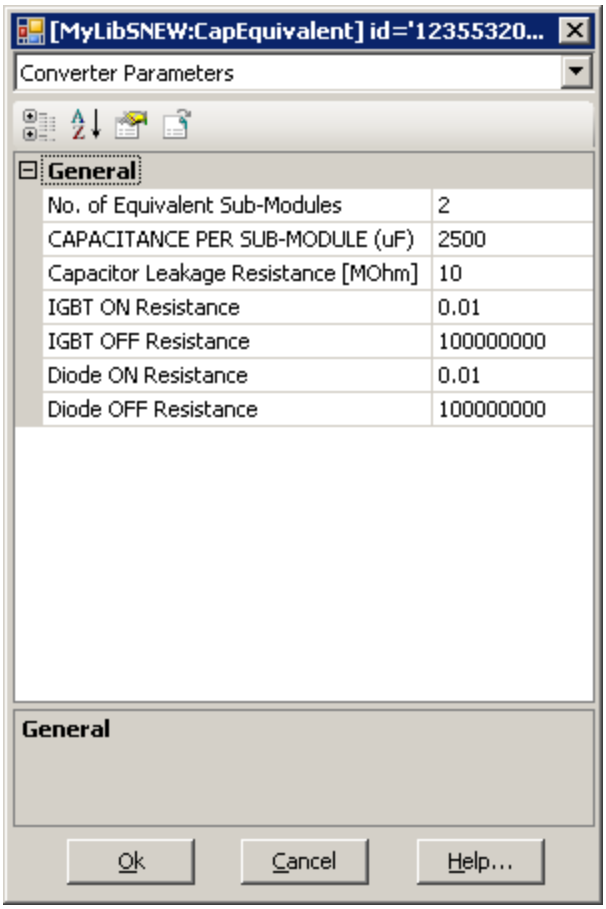


Figure A-2. The user can input the values for module capacitance and the equivalent switch resistance values. The number of modules, represented by the equivalent MMC multi-valve equivalent is user selectable and the user can enter the appropriate number. The sizing of the converter can easily be changed for each run by varying this value.

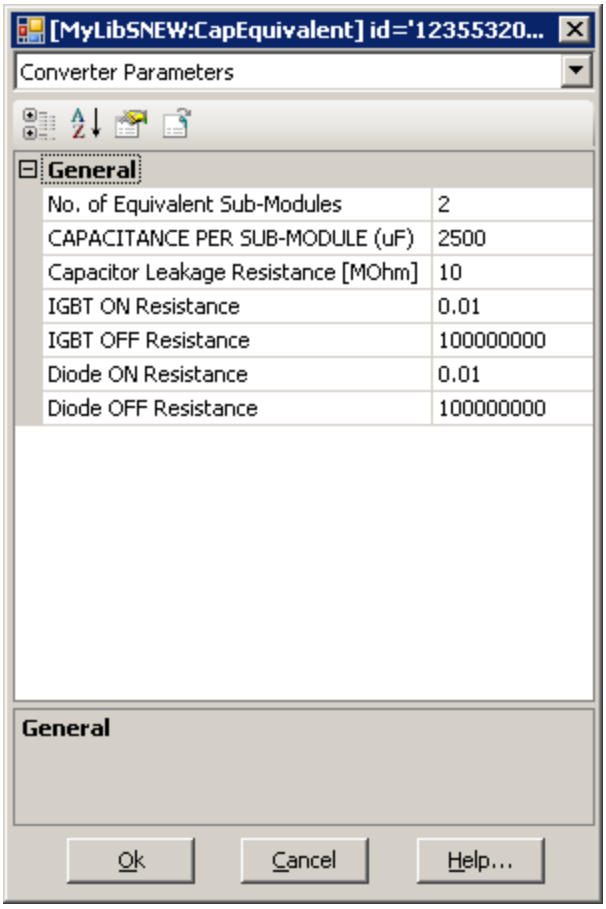


Figure A-2. Input parameter list of equivalent model for half-bridge sub-module MMC

The data type, signal type, and the units are listed below.

No. of equivalent sub-modules (N)	Integer	Variable	The total number of modules represented by the MMC model
Capacitance per module	Real	Variable	The capacitance value of each module. [μF]
Capacitor leakage resistance	Real	Variable	The equivalent leakage resistance of module capacitor (losses) [MOhm]
IGBT ON resistance	Real	Constant	Resistance of IGBT switching element when in the ON state (conducting) [Ohm]
IGBT OFF resistance	Real	Constant	Resistance of IGBT switching element when in the OFF state (non-conducting) [Ohm]
Diode ON resistance	Real	Constant	Resistance of Diode switch when in the ON state (conducting) [Ohm]
Diode OFF resistance	Real	Constant	Resistance of Diode switch when in the OFF state (non-conducting) [Ohm]

Note:

1. The valve reactor has not been considered in modeling the equivalent MMC multi-valve model. The user should connect a separate equivalent inductor to model the valve reactor of each multi-valve.

2. There is no intrinsic limit for the “number of equivalent modules per multi-valve” but the limit is introduced by the computing power available.

3. Reducing the capacitor value will at some point may require a smaller time-step.

Output Data:

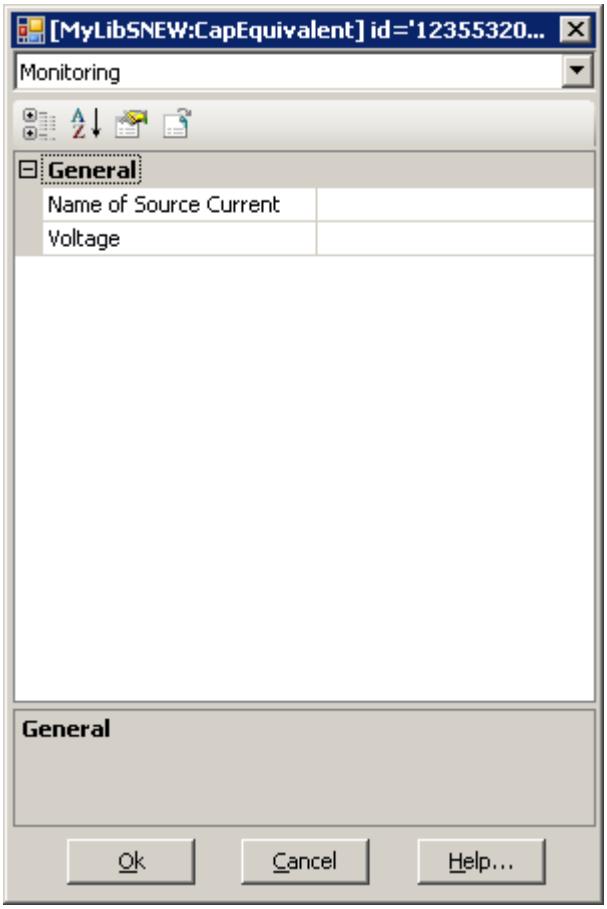


Figure A-3. Output data list of equivalent model for half-bridge sub-module MMC

Two optional outputs can be used in this equivalent model as shown in Figure A-3. These are internally calculated by the Thévenin equivalent solver. If the voltage across the module and the branch current are required to measure, these outputs can be used.

Name of source current	Text	Output	This parameter outputs the current passing across the equivalent circuit model. i.e.: multi-valve current [kA].
Voltage	Text	Output	The total voltage drop across the equivalent circuit model (multi-valve) is given by this signal [kV].

A.2 Full-Bridge Sub-Module Equivalent Model

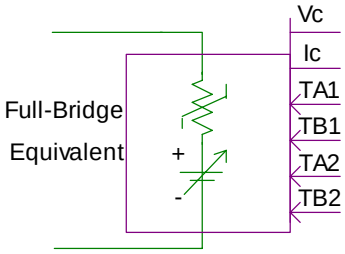


Figure A-4: PSCAD block of proposed equivalent model for MMC multi-valve with full-bridge sub-modules

Connection Ports:

Vc: Outputs the capacitor voltage values which are internally calculated in the Thévenin equivalent solver. This is a real variable and the dimension is equal to the number of modules.

Ic: Outputs the capacitor currents which are internally calculated in the Thévenin equivalent solver. This is a real variable and the dimension is equal to the number of modules.

TA1: Inputs the firing signals for upper switch vector 1 in each module. This is an integer variable with the dimension equal to the number of modules.

TB1: Inputs the firing signals for lower switch vector 1 in each module. This is an integer variable with the dimension equal to the number of modules.

TA2: Inputs the firing signals for upper switch vector 2 in each module. This is an integer variable with the dimension equal to the number of modules.

TB2: Inputs the firing signals for lower switch vector 2 in each module. This is an integer variable with the dimension equal to the number of modules.

Input Parameters:

The input parameter list of the MMC model is shown in Figure A-5.

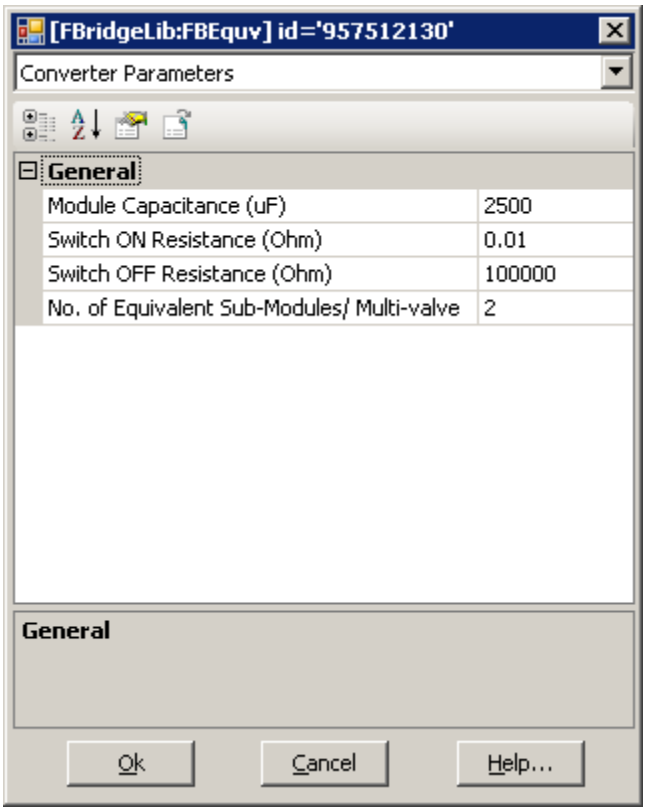


Figure A-5. Input parameter list for full-bridge sub-module MMC model

The data type, signal type, and the units are listed below.

Module Capacitance	Real	Variable	The capacitance value of each module. [μF]
Switch ON resistance	Real	Constant	Resistance of switching element when in the ON state (conducting) [Ohm]
Switch OFF resistance	Real	Constant	Resistance of switching element when in the OFF state (non-conducting) [Ohm]
No. of equivalent sub-modules/ Multi-valve	Integer	Variable	The total number of modules represented by the MMC model

Output Data:

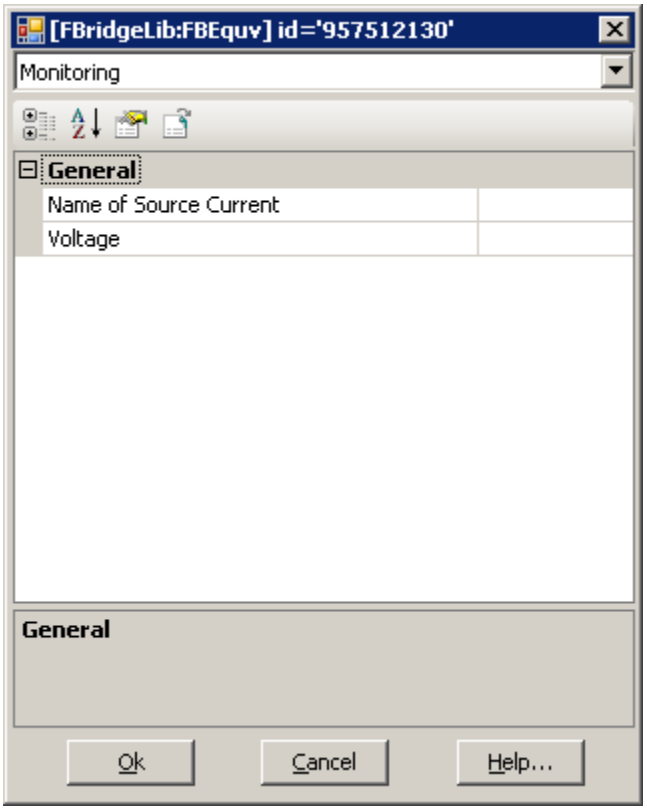


Figure A-6. Output data list of half-bridge sub-module MMC model

Two optional outputs can be used in this equivalent model as shown in Figure A-6. These are internally calculated by the Thévenin equivalent solver. If the voltage across the module and the branch current are required to measure, these outputs can be used.

Name of source current	Text	Output	This parameter outputs the current passing across the equivalent circuit model. i.e.: multi-valve current [kA].
Voltage	Text	Output	The total voltage drop across the equivalent circuit model (multi-valve) is given by this signal [kV].

Appendix B

2–Stage Diagonally Implicit Runge–Kutta (2–S Dirk) Integration Scheme

The 2S-DIRK method of numerical integration has been proposed for EMT simulations [87].

Consider the following differential equation;

$$\frac{dy}{dt} = f(t, y) \qquad \textbf{B-1}$$

In Equation (B-1) *t* is time and *f* is a function of time and the variable, *y*.

When the 2S-DIRK integration scheme is applied in integrating the equation given in Equation (B-1) from the previous time-step $t = t_{n-1}$ to the present time-step $t = t_n$, the solution is obtained using two-stage calculation as discussed below.

The first stage calculates an intermediate value of *y* at $t = \tilde{t}_n$ which is between t_{n-1} and t_n.

$$\tilde{t}_n = t_{n-1} + \Delta\tilde{T}, \qquad \Delta\tilde{T} = a(\Delta T) \qquad \textbf{B-2}$$

where, $a = 1 - 1/\sqrt{2}$ and $\Delta T = t_n - t_{n-1}$ is the time step.

If the intermediate value of *y* at $t=\tilde{t}_n$ is $\tilde{y}_n$, the first stage formula can be written as in Equation (B-3):

$$\tilde{y}_n = y_{n-1} + \Delta\tilde{T} \cdot f\left(\tilde{t}_n, \tilde{y}_n\right) \quad \textbf{B-3}$$

Another intermediate value is calculated using $\tilde{y}_n$ as given in Equation (B-4)

$$\tilde{y}_{n-1} = \alpha y_{n-1} + \beta\tilde{y}_n \quad \textbf{B-4}$$
where, $\alpha = -\sqrt{2}$ and $\beta = 1+\sqrt{2}$

The final solution of y_n at $t=t_n$ is determined at the second stage:

$$y_n = \tilde{y}_{n-1} + \Delta\tilde{T} \cdot f\left(t_n, y_n\right) \quad \textbf{B-5}$$

Using this 2-S DIRK method, the relationship between the voltage *v* and current *i* can be derived for a liner capacitor as given in Equation (B-6):

$$\begin{aligned}
&\text{Voltage current relationship:} && \frac{dv}{dt} = \frac{1}{C} i \\
&\text{First Stage:} && i_n = \frac{C}{\Delta\tilde{T}}\tilde{v}_n - \frac{C}{\Delta\tilde{T}} v_{n-1} \\
&\text{Variable Conversion:} && \tilde{v}_{n-1} = \alpha v_{n-1} + \beta\tilde{v}_n \\
&\text{Second Stage:} && i_n = \frac{C}{\Delta\tilde{T}} v_n - \frac{C}{\Delta\tilde{T}}\tilde{v}_{n-1} = g\, v_n - j_t
\end{aligned} \quad \textbf{B-6}$$

The second stage allows the construction of a circuit model of the form in Figure B-1.

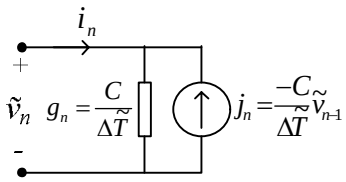


Figure B-1: Capacitor equivalent circuit for 2S-DIRK method

Appendix C

Parameters of MMC-based HVDC System

Table C-1: Parameters of MMC-based HVDC system

AC System 1	AC System 2
$V_{BUS1(L-L)}$ = 230 kV	$V_{BUS2(L-L)}$ = 115 kV
R_1 = 6.903 Ω	R_2 = 1.726 Ω
L_1 = 0.138 H	L_2 = 0.035 H
R_1' = 1190.95 Ω	R_2' = 714.567 Ω
SCR = 2.5	SCR = 2.5
L_g = 0.5 H	L_g = 0.5 H
R_g = 10000 Ω	R_g = 10000 Ω
Transformer 1	Transformer 2
S = 600 MVA	S = 600 MVA
Ratio = 230/245 kV	Ratio = 230/115 kV
X_{TF1} = 15 %	X_{TF2} = 15 %
DC System	
Sub-module capacitance	C = 5 mF
DC smoothing reactance	L_{dc} = 0.01 H
DC rated voltage	$U_{dc}/2$ = ±200 kV
DC cable	L_c = 3.03 mH/km
	R_c = 11.06 mΩ/km
	C_c = 0.39 μF/m
	Length = 200 km

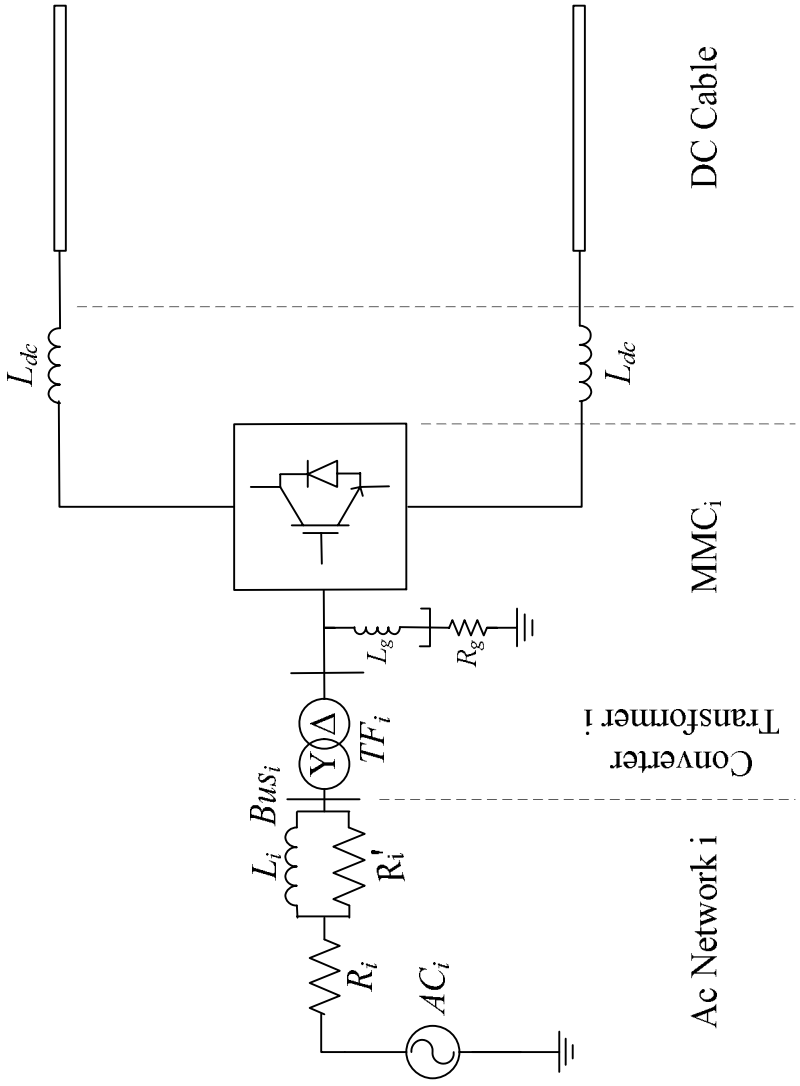


Figure C-1: MMC based HVDC converter station main circuit

Appendix D

Evaluation of Switching Losses and Thermal Performance in Power Electronic Systems

This method presents a simple set of formulae for switching losses based on the predicted device current and voltage waveforms. The predicted waveforms conform to the physics of the switching process and take into account the dependency of the switching losses on various factors such as the switching voltage, switching current, stray inductance and the reverse recovery process of the freewheeling diode. A detailed validation of the model was conducted using a simple laboratory set-up and by comparison with published loss curves by the manufacturer [97].

D.1 Approximate Loss Formulae for Estimation of IGBT/Diode Switching Losses

Diode Turn ‘ON’ **Loss Formula:**

In modern fast recovery diodes used with IGBTs, the turn ‘ON’ loss is negligible (less than 1%) compared to the turn ‘OFF’ loss [97]. Therefore, formulae to model diode turn ‘‘ON’ losses are eliminated in this approach.

Diode Turn 'OFF' Loss Formula:

Idealized approximation of diode turn 'OFF' waveforms is shown in Figure D-1.

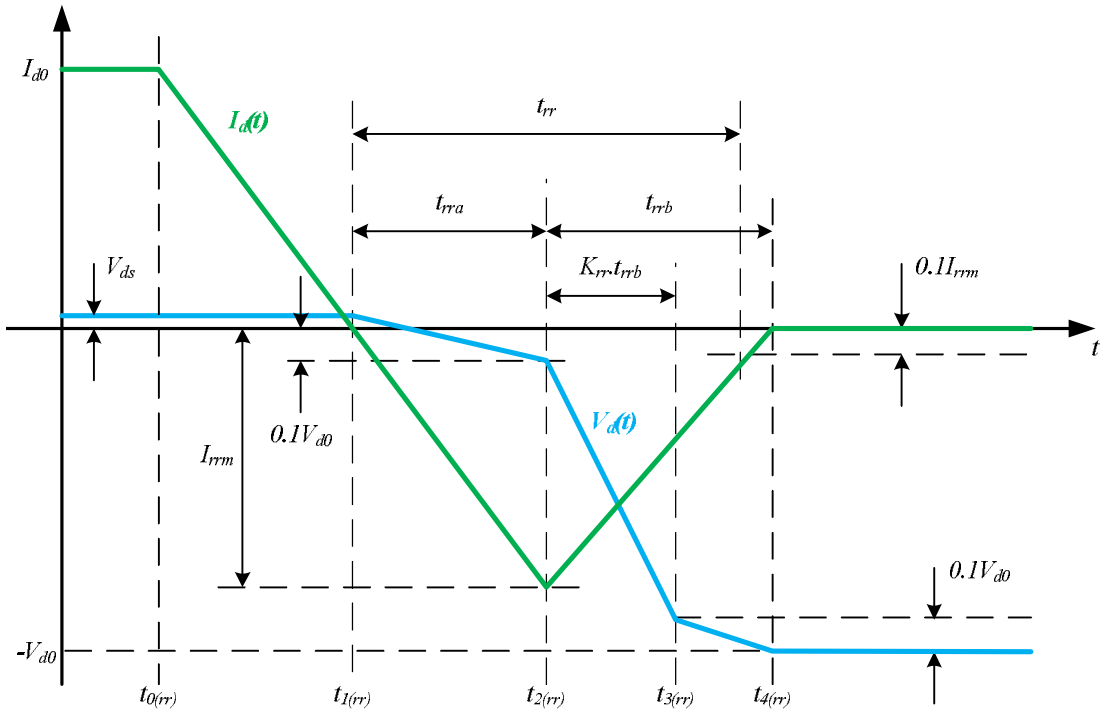


Figure D-1: Approximated waveforms of diode turn 'OFF' transient [97]

The waveforms can be characterized using the parameters I_{rrm} (peak reverse recovery current), and t_{rr} (the reverse recovery time). Knowing the initial dI_d/dt, (which depends on the IGBT turn 'ON' rise time), the parameters t_{rra}, and t_{rrb} are estimated as:

$$t_{rra} = \frac{I_{rrm}}{\left(\left.\frac{dI_d}{dt}\right|_{t_{1(rr)}}\right)} \qquad \textbf{D-1}$$

$$t_{rrb} = 1.11\left(t_{rr} - t_{rra}\right)$$

It is also assumed that the diode voltage drops to 90% of its reverse blocking voltage during $[t_{2(rr)},\ t_{3(rr)}] = k_{rr} t_{rrb}$. An energy loss occurs in the diode during the reverse recovery, particularly during building up of reverse voltage. This can now be computed as given in Equation (D-2).

$$W_{rec} = \int_{t_{0(rr)}}^{t_{4(rr)}} V_d(t) I_d(t) dt$$

$$= 0.5 V_{ds} I_{d0} \frac{I_{d0}}{\left(\left. \frac{dI_d}{dt} \right|_{t_{1(rr)}} \right)} + 0.33 V_{d0} I_{rrm} t_{rra} \qquad \textbf{D-2}$$

$$+ V_{d0} I_{rrm} \left(0.467 - 0.433 k_{rr} + 0.15 k_{rr}^{\ 2} \right) t_{rrb}$$

The parameter $k_{rr}[0.0 - 1.0]$ can be determined by substituting data sheet value of W_{rec} and the corresponding measuring conditions to Equation (D-2).

IGBT Turn 'ON' Loss Formula:

Figure D-2 shows approximate waveforms for the hard turn 'ON' transient of an IGBT.

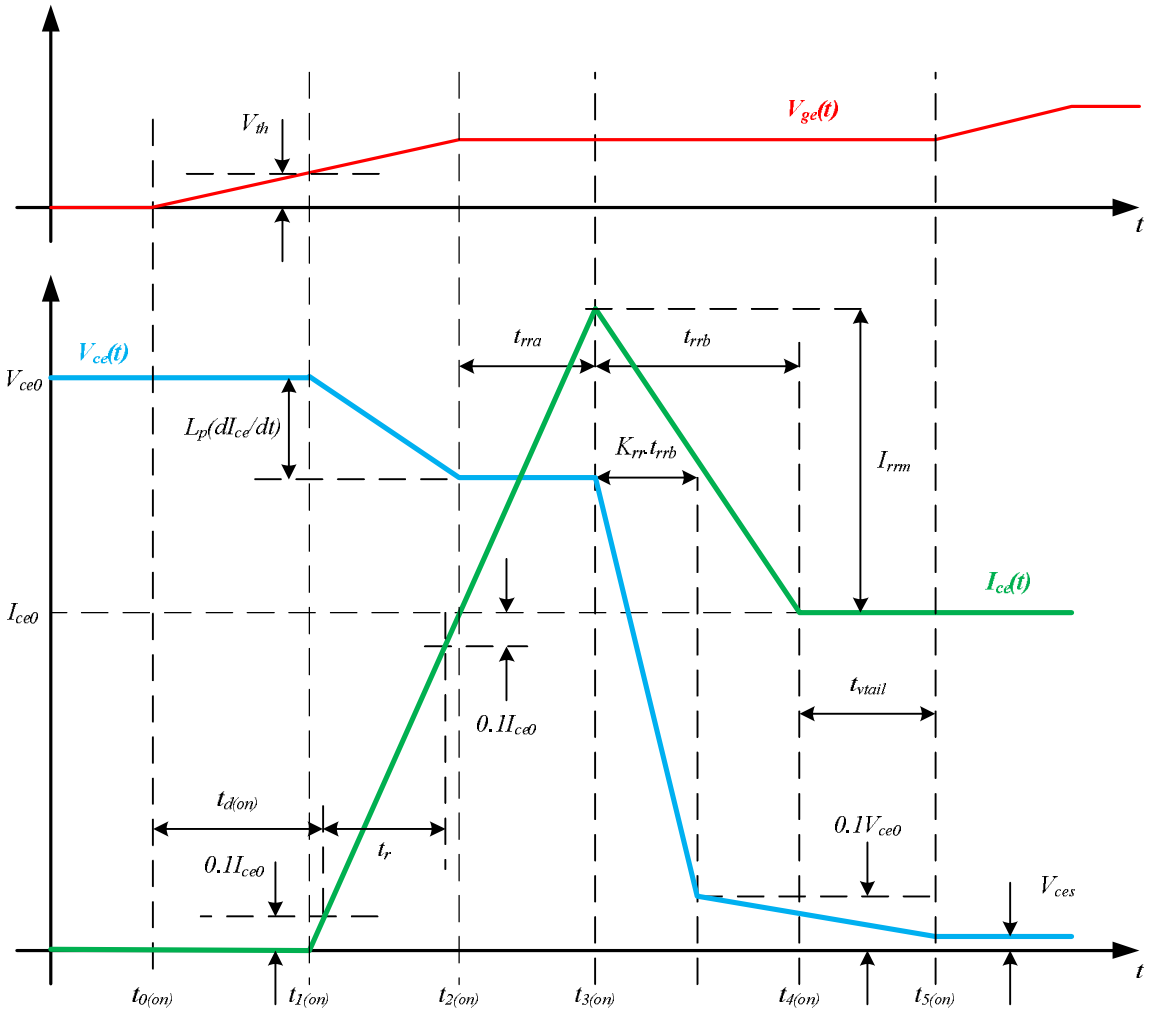


Figure D-2: Hard switching turn 'ON' transient waveforms for loss calculation [97]

In data sheets, the turn-on behavior is characterized by the turn on delay time $t_{d(on)}$, the rise time t_r, and the turn-on energy W_{on}. The turn 'ON' gate pulse applied at $t_{0(on)}$

raises the gate voltage V_{ge} gradually. When V_{ge} reaches a threshold voltage V_{th}, the collector current, I_{ce} starts to rapidly rise and the load current in the freewheeling diode of the opposite leg gradually transfers to the IGBT. The rate of rise of collector current can be determined as give in Equation (D-3)

$$\frac{dI_{ce}}{dt} = \frac{0.8I_{ce0}}{t_r} \quad \textbf{D-3}$$

During this current rise, the device (collector-emitter) voltage, $V_{ce}(t)$ experiences a drop due to parasitic inductance L_p. It is assumed that the voltage $V_{ce}(t)$ drops linearly over the period $\left[t_{1(on)}, t_{2(on)}\right]$ and reaches a plateau in the voltage waveform. This plateau voltage V'_{ce0} can be found as:

$$V'_{ce0} = V_{ce0} - L_p \frac{dI_{ce}}{dt} = V_{ce0} - \frac{0.8I_{ce0}}{t_r} L_p \quad \textbf{D-4}$$

When the load current is fully transferred to the IGBT at $t_{2(on)}$, the outgoing freewheeling diode starts to turn 'OFF' and forces its reverse recovery current through the IGBT. The duration, during which the reverse recovery current increases, can be computed by substituting Equation (D-3) into Equation (D-1):

$$t_{rra} = \frac{I_{rrm}}{0.8I_{ce}} t_r \quad \textbf{D-5}$$

The turn 'ON' energy loss can be computed as;

$$
\begin{aligned}
W_{on} &= \int_{t_{0(on)}}^{t_{4(on)}} V_{ce}(t) I_{ce}(t) dt \\
&= 0.05 V_{ce0} I_{ce0} t_{d(on)} + 0.225 V_{ce0} I_{ce0} t_r + V'_{ce0} I_{ce0} (0.394 t_r + t_{rra} + 0.55 k_{rr} t_{rrb}) \\
&\quad + 0.5 V'_{ce0} I_{rrm} t_{rra} + 0.5 V_{ces} I_{ce0} t_{vtail} + V'_{ce0} I_{rrm} (0.033 + 0.483 k_{rr} - 0.167 k_{rr}^{\ 2}) t_{rrb} \\
&\quad + V'_{ce0} I_{ce0} k_{vtail} [0.5(1 - k_{rr}) t_{rrb} + 0.05 t_{vtail}] + 0.167 V'_{ce0} I_{rrm} k_{vtail} (1 - k_{rr}) t_{rrb}
\end{aligned}
\qquad \textbf{D-6}
$$

where,

$$k_{vtail} = \frac{t_{vtail}}{t_{vtail} + (1 - k_{rr}) t_{rrb}}$$

IGBT Turn 'OFF' Loss Formula:

The IGBT's turn 'OFF' behaviour shown in Figure D-3 is characterized in data sheets by the turn 'OFF' delay time, $t_{d(off)}$ fall time, t_f and turn 'OFF' energy, W_{off}. The turn 'OFF' process starts on the application of negative gate voltage at time $t_{0(off)}$. The initial period $\lfloor t_{0(off)}, t_{1(off)} \rfloor$ which gate-emitter voltage, V_{ge} reduces but the collector-emitter voltage, V_{ce} remains essentially unchanged, is assumed to be equal to $k_{off} t_{d(off)}$ as indicated in Figure D-3. Thereafter, the collector-emitter voltage rises rapidly at a rate given in Equation (D-7).

$$\frac{dV_{ce}}{dt} = \frac{0.9 V_{ce0}}{(1 - k_{off}) t_{d(off)}} \qquad \textbf{D-7}$$

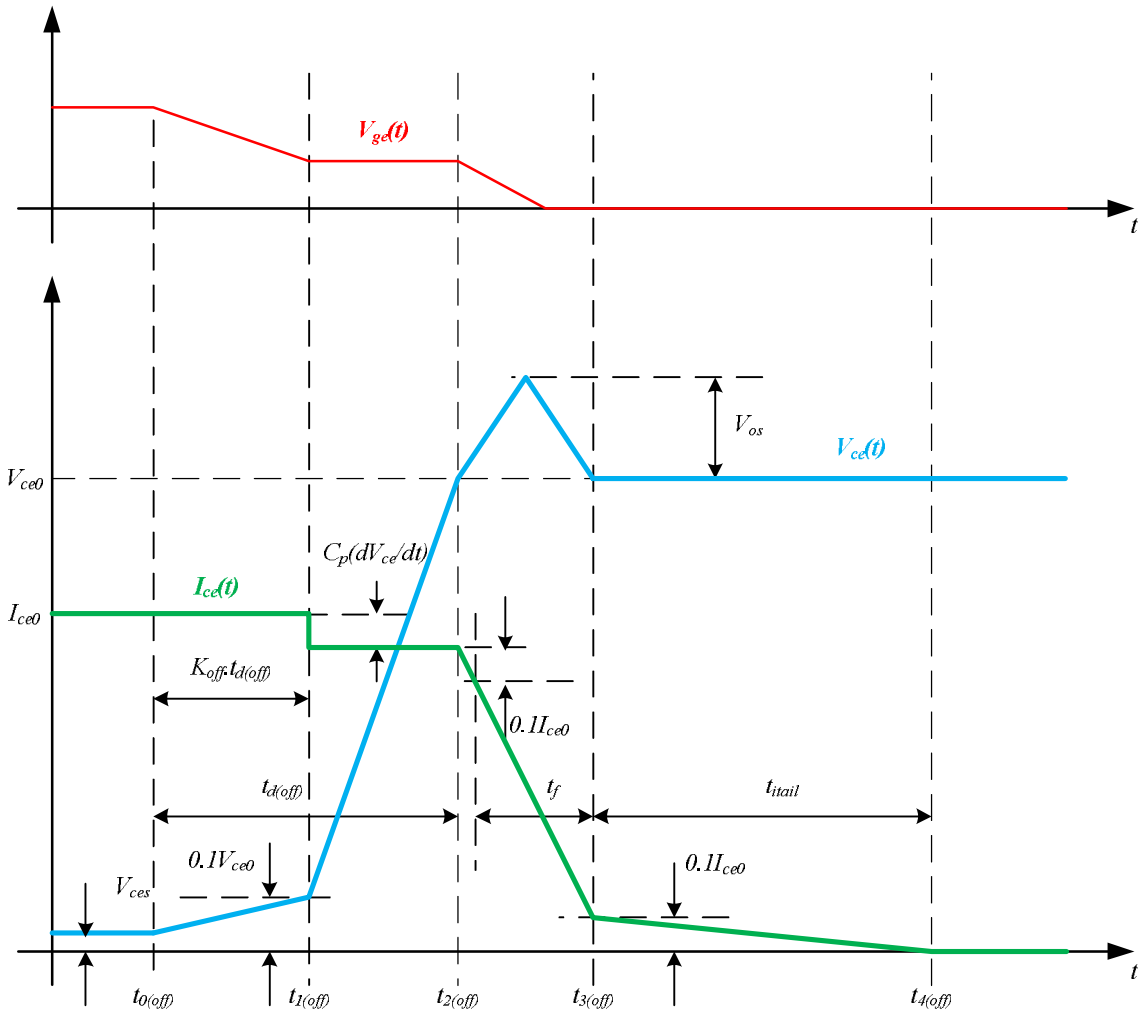


Figure D-3: Approximated hard switching turn 'OFF' transient waveforms [97]

Considering the idealized waveforms, the resulting plateau in the collector current, I'_{ce0} can be approximately determined as:

$$I'_{ce0} = I_{ce0} - C_p \frac{dV_{ce}}{dt} = I_{ce0} - \frac{0.9V_{ce0}}{(1-k_{off})t_{d(off)}} C_p \qquad \textbf{D-8}$$

In Equation (D-8), C_p is the parasitic capacitance. The parasitic inductance produces an overshoot in the voltage V_{ce}:

$$V_{os} = L_p \frac{dI_{ce}}{dt} = \frac{0.8I'_{ce0}}{t_f} L_p \qquad \textbf{D-9}$$

Based on the idealized waveform, an approximate expression for the turn 'OFF' energy can be developed as:

$$\begin{aligned} W_{off} &= \int_{t_{0(off)}}^{t_{4(off)}} V_{ce}(t) I_{ce}(t) dt \\ &= 0.5 V_{ces} I_{ce0} k_{off} t_{d(off)} + 0.05 V_{ce0} I_{ce0} k_{off} t_{d(off)} + 0.275 V_{os} I'_{ce0} t_f \\ &\quad + 0.55 V_{ce0} I'_{ce0} (1 - k_{off}) t_{d(off)} + V_{ce0} I'_{ce0} \left[0.55 t_f + 0.05 t_{itail} \right] \end{aligned} \qquad \textbf{D-10}$$

D.2 Modeling IGBT Thermal Path

The junction temperature of the device is an important parameter as an excessive value can damage the device. The mounting of the device and the heat sink become important in determining the heat removal performance. Therefore, an accurate model is required for thermal performance analysis of the power electronic circuit [96].

Thermal Model of the IGBT:

A thermal model of the IGBT switching device can be represented as shown in Figure D-4. P_{Lj} is the power loss in the device and the junction temperature and case temperature are denoted by T_j and T_c, respectively. R_{thi} and C_{thi} represent the thermal resistance and capacitance of various layers of the semiconductor device. The heat sink

can be modeled as a single lumped thermal capacitance C_m and resistance R_{sa} from the sink to the ambient temperature T_a [96].

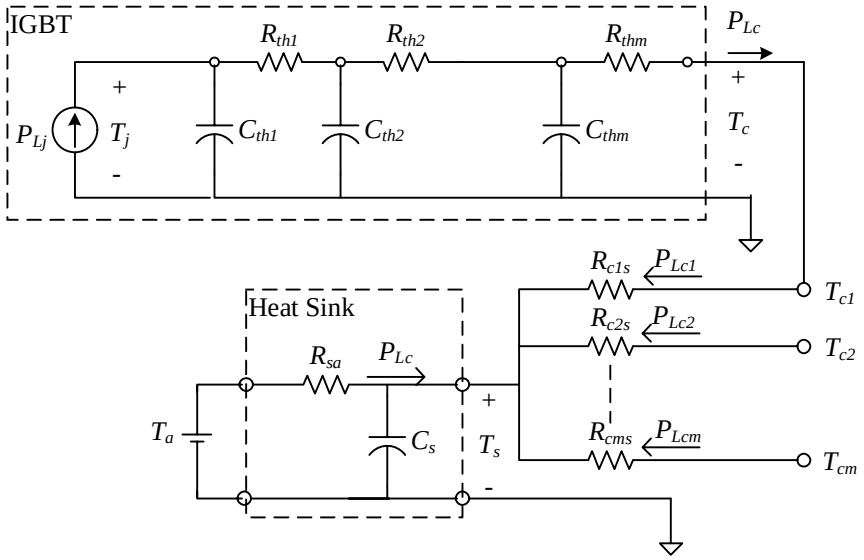


Figure D-4: Equivalent thermal network of a semiconductor device and heat sink

Extraction of Model Parameters:

The information required to obtain thermal network parameters is commonly given in the form of a single-pulse junction to case transient thermal impedance Z_{th} which can be approximated in the form of [96]:

$$Z_{th}(t) = A_0 + \sum_{i=1}^{n} A_i e^{-a_i t} \qquad \textbf{D-11}$$

where, $A_0 \ldots A_n$ and $a_1 \ldots a_n$ are constants to be found through an appropriate curve fitting technique.

Using Equation (D-11), the transfer function of the network can be obtained for a case of two exponential terms as given in Equation (D-12).

$$Z_{th}(s) = \frac{\kappa_1 + s\kappa_2}{1 + s\kappa_3 + s^2\kappa_4} \qquad \textbf{D-12}$$

where, $\kappa_1 = A_0 \quad \kappa_2 = A_0\left(\frac{1}{a_1} + \frac{1}{a_2}\right) + A_1\left(\frac{1}{a_1}\right) + A_2\left(\frac{1}{a_2}\right)$

$$\kappa_3 = \frac{1}{a_1} + \frac{1}{a_2} \quad \kappa_4 = \frac{1}{a_1 a_2}$$

Alternatively, the transfer function of the thermal equivalent network in Figure D-4 can be obtained in terms of R_{thi} and C_{thi} as:

$$Z_{th}(s) = \frac{(R_1 + R_2) + s(R_1 R_2 C_2)}{1 + s(R_1 C_1 + R_2 C_1 + R_2 C_2) + s^2(R_1 C_1 R_2 C_2)} \qquad \textbf{D-13}$$

By comparison of the coefficients of Equation (D-12) and Equation (D-13), the expressions for R_{thi} and C_{thi} are obtained as;

$$R_{th1} = \frac{\kappa_2^{\,2}}{(\kappa_2\kappa_3 - \kappa_1\kappa_4)}$$

$$R_{th2} = \frac{\kappa_1 - \kappa_2^{\,2}}{(\kappa_2\kappa_3 - \kappa_1\kappa_4)} \qquad \textbf{D-14}$$

$$C_{th1} = \frac{\kappa_4}{\kappa_2}$$

$$C_{th2} = \frac{(\kappa_2\kappa_3 - \kappa_1\kappa_4)^2}{\kappa_2\left(\kappa_1\kappa_2\kappa_3 - \kappa_1^{\,2}\kappa_4 - \kappa_2^{\,2}\right)}$$

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