Dynamic Performance of Static and Synchronous Compensators at an Inverter Bus in a Very Weak Ac System

by

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DYNAMIC PERFORMANCE OF STATIC AND SYNCHRONOUS COMPENSATORS AT AN INVERTER BUS IN A VERY WEAK Ac SYSTEM

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A Thesis submitted to the Faculty of Graduate Studies of the University of Manitoba in partial fulfillment of the requirements for the degree of

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Abstract

This thesis investigates the effect of different reactive power compensator options at HVdc converter terminals where the ac system has a very low Short Circuit Ratio. The investigations include performance under overvoltage, undervoltage and system faults. The studies are conducted using an electromagnetic transient simulation program. Five dynamic compensators schemes comprising of Static Var Compensators (SVC) and/or Synchronous Compensators (SC) are considered. It is shown that the SVC has the fastest response for load rejection type of overvoltages, but can cause serious problems with recovery during undervoltages caused by single phase faults while operating with weak ac systems. This is a deviation from the behavior of SVC operating in strong ac systems where the SVC performance is superior than the SC for all disturbances. The effect of local loads on the system dynamics has also been investigated. The results show that the effect of the loads modelled separately is very similar to that modelled as part of the system equivalent.

The thesis also introduces a new concept called the "Control Sensitivity Index (CSI)" for the stability analysis of HVdc converters connected to weak ac systems. CSI for a particular control mode can be defined as the rate of change of the controlled quantity with respect to the controlling quantity. It provides valuable information about the stability of the system. It is also useful in defining variable gains and can be used to design adaptive dc controllers. The theoretical results of CSI for different control modes have been verified against detailed electromagnetic transient simulations.

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Chapter 1

Introduction

1.1 INTRODUCTION

This thesis is arranged in two main parts: *i) Dynamic Performance of HVdc Compensators* and *ii) Stability Analysis of HVdc Systems.*

The first part discusses the overvoltage, undervoltage and fault recovery performance of dynamic voltage control schemes comprising of synchronous compensators and static var compensators. This study has been conducted on a system that is weaker than the systems used in any of the earlier studies and it uses a faster synchronous compensator.

The second part introduces a new concept called the "Control Sensitivity Index" for the stability analysis of HVdc systems connected to weak ac systems. This analysis based on this concept provides additional insights into dc controller behavior and directly relates the instabilities associated with weak ac systems to dc controllers in a way that is never shown before. The knowledge can be utilized in the design of faster and robust dc controllers.

The following section provides a brief background on the reactive power requirement of HVdc terminals in establishing the motivation for the research reported in this thesis.

1.2 MOTIVATION

It is an inherent feature of the HVdc links to consume reactive power, both at the inverter and rectifier end, which is typically 50 to 60 percent of the real power transmitted at full load. During transients, the reactive power demand may vary over a wide range. The duration of this fluctuation depends to a large extent upon the ac system impedance characteristics and dc controls. The voltage at ac busbars of the converter station depends upon the reactive and real power characteristics of the converter.

To control this voltage, the reactive power supply at the ac busbars of the converter station needs to be controlled in accordance with the converter reactive power demand. An excess of reactive power supply at the ac bus will lead to overvoltages at the ac bus, while a deficit in its supply will lead to undervoltages. The magnitude of these voltage variations for a given amount of reactive power imbalance depends upon the characteristics of the ac system impedance.

As is the general practice [1], it is best to compensate the entire reactive power requirement of the converter at the converter station in order to minimize transmission loss, loss of transmission capacity, and regulation effort. Harmonic filters provide a portion of the reactive power requirement. The remaining portion of the reactive power is provided by either the fixed capacitors or the dynamic voltage control devices (VCD) or both. For converters connected to weak ac systems where the short circuit ratio (SCR)# is less than 2.5, it is necessary to have dynamic VCD to control the overvoltages since otherwise the overvoltages can reach dangerously high values during disturbances such as a dc block.

Due to the developments in HVdc technology (such as faster compensators, better controllers) in the past decade, there has been an increased trend to plan and install HVdc converters connected to weak ac systems (SCR < 2.5) [1], [2]; which has led to increased research in this field. Both IEEE and CIGRE have formed separate working groups to study the dynamic interaction of HVdc converters with weak ac system. Among the effects that are of special concern to the design and operation of HVdc converters connected to weak ac networks are: high temporary overvoltages (TOV), low frequency resonances, risk of voltage instability, long fault recovery times, and increased risk of commutation failure [3]. Many of the above phenomena are closely related to the ac voltage regulation at the converter bus. Dynamic control of the voltage at the converter bus alleviates some of the difficulties associated with the operation of the HVdc systems with weak ac systems. Synchronous compensators (SC) are the most widely used voltage control devices for such applications. Among the other voltage control devices currently in use, static var compensators (SVC) are gaining popularity for dc application.

Static var compensators have been widely used and accepted as a more effective and economical alternative to synchronous compensators for ac transmission systems [5], [6]. They are becoming a popular alternative to the SCs in the HVdc schemes as well. But in certain cases, synchronous compensators might be preferable, especially when the ac system has an extremely low short circuit ratio. The Itaipu receiving station [7] and, more recently, the Nelson River System

upgrade [8] are two examples of where synchronous compensators have been chosen over static compensators after considering both alternatives.

Earlier research by Nyati [9] et al [10] has indicated that the static compensators provide a much faster system response than the synchronous compensators but this claim requires re–examination because of the advances in modern day excitation systems for synchronous compensators, which greatly increase their speed of response. Their study [10] examined HVdc systems with stronger ac systems than the one used in this thesis and concentrated on overvoltage studies. Flueckiger [11] studied the performance of various compensators prior to Nyati. His study used load flow and transient stability simulations in the phasor domain and considered only overvoltages due to dc block disturbances. This thesis investigates the performance of synchronous and static compensators, used either individually or in combination, at the inverter bus connected to a very weak ac system. The aspects considered include overvoltage control as well as the dynamics of recovery from various system disturbances including undervoltage events. The investigation is conducted using an electromagnetic transient simulation program, EMTDC™ [12]. These results are reported in Part I of the thesis.

During the process of developing the ac–dc system for the study in Part I, some difficulties associated with the operation of very weak HVdc systems were encountered. That led to a further investigation of the stability aspects of weak systems which is presented in Part II of the thesis.

A brief summary of both parts of the thesis is provided in the next section.

1.3 SUMMARY

1.3.1 Part I: Dynamic Performance of HVdc Compensators

In Chapter 2 the *CIGRE benchmark model for HVdc control studies* [13] is modified to develop the study system. The benchmark model represents an inverter ac system of SCR 2.5 with fixed capacitors for reactive power support. The modified model has an inverter SCR of 1.5 (effective SCR of 0.97) and replaces the fixed capacitors with different voltage control options. The controls from the benchmark model are modified to accommodate the lower SCR system. Five different

Refer to Section 1.4 for the definition of SCR

dynamic reactive power compensation options are studied. The simulation results are compared with each other as well as with the base case using fixed capacitors. The five dynamic compensation options studied are:

1) Static var compensator (SVC)

2) Synchronous compensator (SC)

3) An equal mix of the two

4) A 75% SC and 25% SVC mix

5) A 25% SC and 75% SVC mix

The simulation results in Chapter 3 for the various ac and dc disturbances indicate that the SVC has the fastest response for load rejection type of overvoltages, but can cause serious problems with recovery during undervoltages caused by single phase faults while operating with weak ac systems. This is a deviation from the behavior of SVC operating in strong ac systems where SVC performance is superior than SC, under all disturbances. Because of the natural coordination between SC and SVC, a mix of these two devices (SC+SVC) for weak ac systems gives a better performance than the devices individually.

Two different ways of modelling the local loads at the HVdc terminal have been investigated – i) as part of the system equivalent and ii) as a separate shunt load. The results reiterate that the two methods yield the same results.

1 .3 .2 Part II: Stability Analysis of HVdc Systems

During the process of developing a low SCR inverter ac system for the study in Part I, simulation of a dc system was attempted with an inverter ac system of SCR 1.0 and a strong rectifier ac system. The rectifier was in constant current control and the inverter was in constant extinction angle control. The system experienced sudden commutation failures as the dc current approached 1.0 pu during startup although the dc load flow provided a stable operating point at 1.0 pu current. Thus it became impossible to bring the system to steady state at rated conditions. This led to a suspicion that there could be some inherent instabilities in the design of the constant extinction angle controller at the inverter. The subsequent investigation provided the reason behind the above problem and was later developed into a new concept called the "Control Sensitivity Index (CSI)" for the stability analysis of HVdc converters connected to weak ac systems [14].

The CSI for a particular control mode can be defined as the rate of change of the controlled quantity with respect to the controlling quantity. An explanation of this definition is provided in Chapter 5 . The index is calculated based on the steady state equations of the combined ac–dc system and provides valuable information about the stability of the system. For example, a sign change in the index normally indicates onset of instability. The index also plays an important role in defining variable gains and can be used to design adaptive dc controllers.

The control sensitivity indices for three dc control modes have been presented. The CSI results for constant power control mode have been verified against the Maximum Power Curve (MPC) results. The CSI for constant extinction angle control has been verified against the Voltage Stability Factor (VSF). The theoretical conclusions drawn from CSIs for different control modes have been verified against a detailed transient simulation of a dc system based on the CIGRE Benchmark [13].

1 .4 DEFINITION OF SCR AND ESCR

The short circuit ratio (SCR) indicates the relative strength of the ac system with respect to the rated dc power and is a very significant parameter for the results in this thesis. There are several definitions of SCR and a standard definition is yet to be adopted. This section states clearly, for the purpose of this thesis, the definition of SCR and ESCR in order to avoid any ambiguity that may arise otherwise.

The SCR is defined as the ratio of the short circuit MVA of the ac system at the ac busbar with the dc blocked and the ac voltage re–adjusted to its nominal voltage V_t, to the rated dc power P_{dc} at that bus [15]. This ratio is equivalent to the system Thevenin admittance expressed in per unit with the rated dc power as the MVA base and rated ac voltage as the voltage base (see Appendix I for derivation of equivalence) [16].

$$SCR = \frac{Ac\ short\ circuit\ MVA}{P_{dc-rated}} = \frac{1}{Z_{sys-pu}}$$

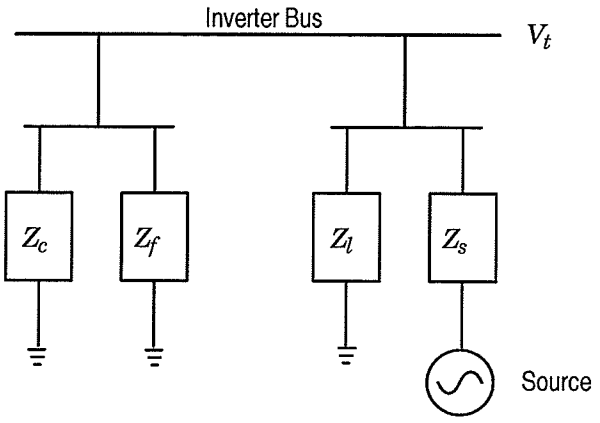


Figure 1 .1 : Equivalent Circuit of the ac System

Figure 1 .1 shows the equivalent circuit of the inverter ac system used in this thesis. Referring to Figure 1 .1 , if filter impedance Z_f and capacitor impedance Z_c are not included in the calculation of the short circuit MVA of the ac system, the ratio is simply called the short circuit ratio (SCR). If Z_f and Z_c are included along with the receiving ac system impedance Z_s and the local load Z_l in the calculation of short circuit MVA of the ac system, then the ratio is called the effective short circuit ratio (ESCR). Thus, the SCR and ESCR of a system represented by Figure 1 .1 are calculated using Equations (1 .1) and (1 .2), respectively [16].

$$SCR = \left(\frac{1}{Z_s} + \frac{1}{Z_l} \right) Z_{base} \qquad (1.1)$$

$$ESCR = \left(\frac{1}{Z_s} + \frac{1}{Z_l} + \frac{1}{Z_f} + \frac{1}{Z_c} \right) Z_{base} \qquad (1.2)$$

where $Z_{base} = \frac{V_t^2}{P_{dc}}$

Chapter 2

The Study System

2.1 INTRODUCTION

The objective of this chapter is to describe an HVdc system on which the dynamic performance of various compensator schemes involving synchronous compensators and static var compensators is to be investigated through the medium of digital simulation. Hereafter, this HVdc system will be referred to as *"the study system"*.

The response of compensators largely depends on several factors, such as their rating in relation to the converter capacity, dc controls and ac system impedance characteristics. Therefore it is necessary to have a basis on which the dynamic performance of different types of compensators can be compared.

The study system, presented in detail in the section to follow, is developed using the CIGRE benchmark model [13] as a base (reference) system since the benchmark has been established to provide a common reference system to researchers conducting comparative performance studies, either of various devices or of control concepts.

2.2 THE STUDY SYSTEM

The study system is shown in Figure 2.1. It is a 1000 MW, 500 KV, 12 pulse, monopolar HVdc system. The inverter SCR (refer to Section 1.4 for definition) is $1.5 \angle -75^{\circ}$ corresponding to a very weak ac system. At the inverter end, the damped high frequency and low frequency filters together provide 300 Mvar, and the SVC and SC combination provides around 260 Mvar to fully compensate for the inverter reactive power requirement. The rectifier SCR is $2.5 \angle -84^{\circ}$ corresponding to a relatively stronger system.

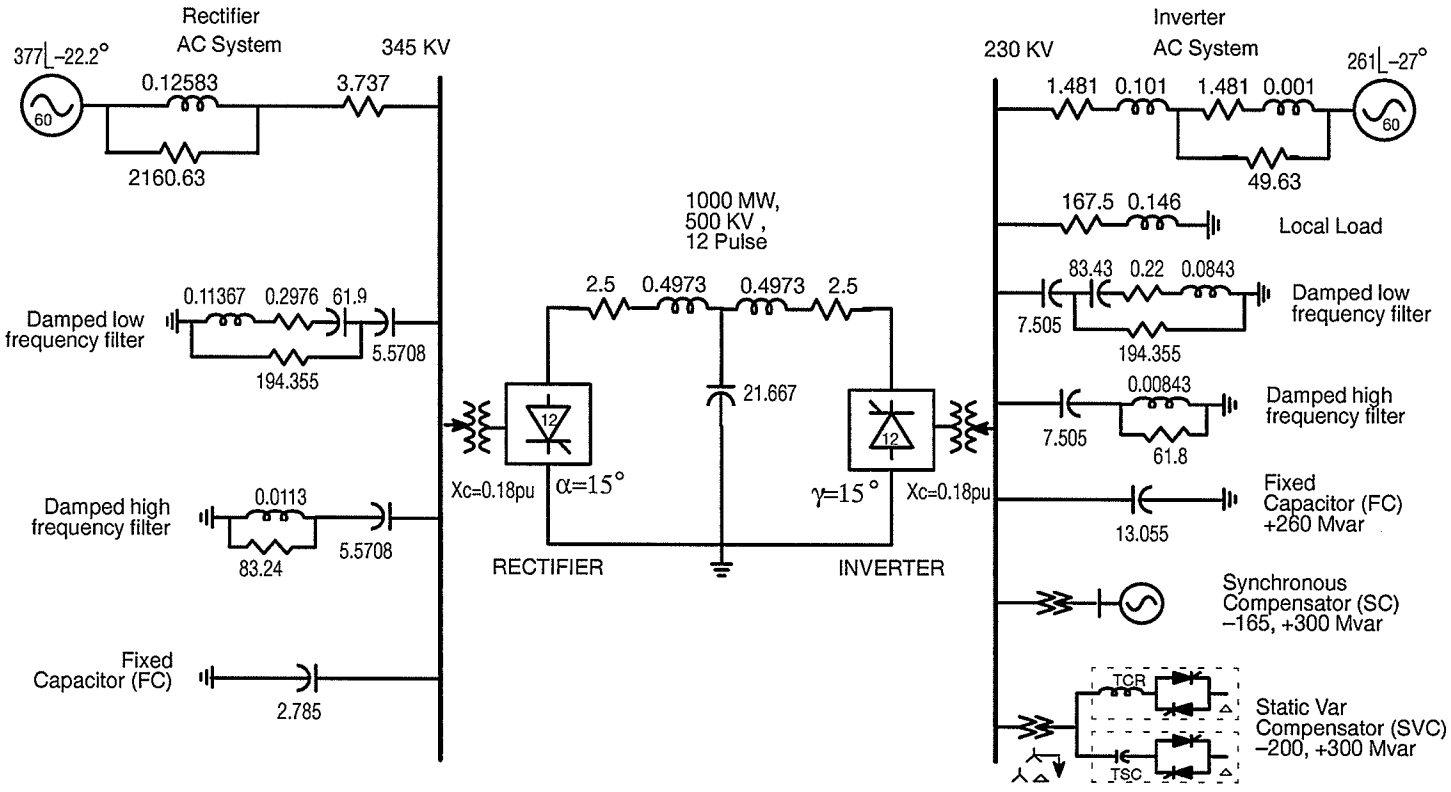


Figure 2.1 : The Study System

The following are the two most significant differences between the benchmark system and the study system.

1 Unlike the benchmark the study system has dynamic reactive power compensators (SC,SVC).

2 The study system has a very weak receiving ac system (SCR=1.5) whereas the benchmark has a relatively stronger receiving ac system (SCR = 2.5).

The nominal frequency of the study system is 60 Hz (North American standard) whereas the nominal frequency of the benchmark is 50 Hz (European standard). The modifications to the benchmark leading to the study system are presented in detail in the sections to follow.

2 .2 .1 Dc Circuit

The rectifier, the inverter, the converter transformers and the dc cables are all identical to those in the benchmark model. Dc controls are discussed in a later section.

2 .2 .2 Rectifier Ac System

Except for the following single change, the rectifier ac system of the study system is identical to that of the benchmark model.

- The ac filters Q factor was increased by reducing the resistance in the tuned branch of the damped low frequency filter. The present value of this resistance is 0.2976 Ω and is in accordance with the modification [17] proposed for the second benchmark model.

2 .2 .3 Inverter Ac System

As in the case of rectifier, the resistance in the tuned branch of the damped low frequency filter at the inverter side is also reduced [17]. Its present value is 0.22 Ω.

When a compensating device is placed into the CIGRE benchmark model , the ac filter and fixed capacitor bank ratings have to be modified in order to keep the reactive power generated locally to the same level as the reactive power demand of the inverter. The inverter SCR had to be

changed from $2.5\angle -75^{\circ}$ to $1.5\angle -75^{\circ}$ to create a very weak receiving system. Consequently, the following modifications were made.

- The ac filters were resized to 300 Mvar while keeping their impedance frequency response profile similar to that in the benchmark.

- Fixed capacitor banks were replaced by an SC and SVC of suitable ratings as discussed in a later section.

- A local R–L load of 300 MVA with a power factor of 0.95 was added at the inverter ac bus to represent the damping and regulating effects of the local loads. The inverter side ac system was modified accordingly to ensure that the load flow at the inverter bus is unchanged. Figure 2 .1 shows the values of all the impedances and the ac source voltages. The inverter SCR of the study system is $1.5\angle -75^{\circ}$ as compared to $2.5\angle -75^{\circ}$ of the benchmark.

2 .2 .4 Effect of SCR on Dc Controls

The sensitivity of the inverter voltage to the dc current increases with decreasing ac system strength (SCR) [18]. When the SCR of the system is altered, adjusting the compensator controls and dc controls may be necessary for the proper operation of the ac/dc system. By comparing the simulated responses of the benchmark and a weaker system (derived from the benchmark), this section verifies whether the dc controls, as used in the benchmark, are adequate for the weaker system.

Figure 2 .2 shows the inverter ac RMS voltage during a five cycle, three phase to ground fault at the inverter bus with SCR of 2.5 and 1.5. The system with inverter SCR=1.5 is obtained from the benchmark system (SCR=2.5) by decreasing the ac system admittances proportionately. It is clear from Figure 2 .2 that the voltage of system with SCR=1.5 could not recover to its pre–fault value after the disturbance. Its cause can be traced back to inverter current error control circuit of the original dc controls in the benchmark model.

Figure 2 .3 shows the current error control circuit in the benchmark model. Figure 2 .4 shows the current error signals during the disturbance for the benchmark (SCR=2.5) and for the weaker (SCR=1.5) system. The benchmark is deliberately designed to have a parallel resonance near

second harmonic frequency on the ac side and a near–fundamental frequency resonance on the dc side [1], [19]. The unfavorable effect of this resonance on dc controls will increase if the SCR is reduced. This is evident from Figure 2 .4 where the current error signal oscillates at near–fundamental frequency and has a large magnitude after the disturbance. This prevents the gamma controller from properly settling down after a fault.

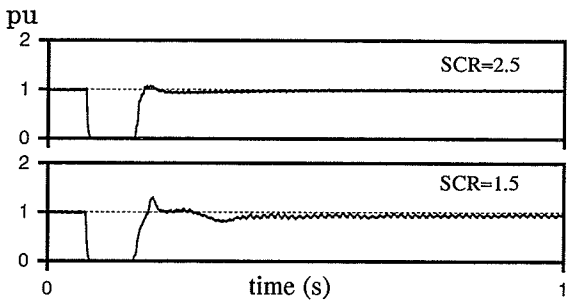


Figure 2 .2 : Inverter ac RMS voltage for a 3 phase to ground fault with SCR of 2.5 and 1.5

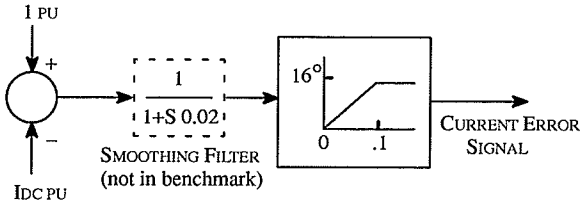


Figure 2 .3 : DC Current Error Control Circuit

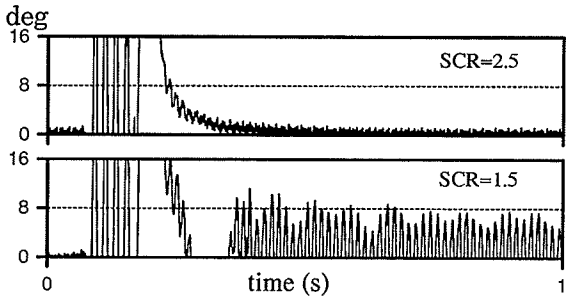


Figure 2 .4 : Current Error Signal

A smoothing filter with a time constant of 0.02 seconds is introduced at the current error measurement to eliminate the high frequency oscillations as shown inside the dotted box in Figure 2 .3 . With this modification, the oscillations in the current error signal are diminished and the inverter voltage returns to its rated value after the disturbance as given in Figure 2 .5 .

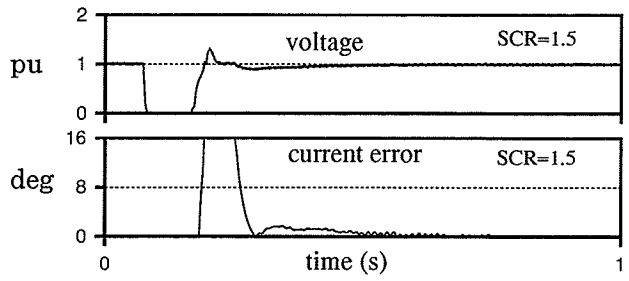


Figure 2 .5 : Inverter Voltage and Current Error After DC Control Modification

2 .2 .5 Dc Controls

The following three modifications were made to the original dc controls before being used in the study system. The first two modifications were necessary because the receiving side of the study system is weaker than the receiving side of the benchmark system and the last one was implemented so that the dc line faults could be studied.

- Introduction of a 20 ms lag in the measurement of the current error signal (Figure 2 .3). This is necessary to smooth out any ripple on the dc current from causing firing angle changes that cause long delays in recovering from disturbances.

- Introduction of a firing angle reduction and ramping circuit at the inverter to recover rapidly from the commutation failures. This modification was necessary to recover from single line to ground faults when the SVC was the sole compensating device. Section 3 .2 provides further details on this circuit along with some comparative simulation results to support the need for such a circuit.

- Introduction of a force–retard ramp (by which the converter firing angle is forced to 135° and gradually ramped back) for both the converters for clearing dc faults. Section 3 .8 .1 provides further details on the force–retard circuit.

The block diagrams of the dc controls are provided in the Appendix–III for convenience, although they are identical to the controls of the benchmark system [13] except for the above additions.

2 .2 .6 SCR and ESCR of the Study System

The definitions of SCR and ESCR are given in Section 1 .4 . The SCR of the inverter side of the study system is $1.5\angle -75°$. The inverter ESCRs (with FC, SVC, or SC) during normal operation

are shown in Table 2 .1 . The impedances of FC and SVC used in the calculation of inverter ESCR are those corresponding to the normal operating point, delivering 260 Mvar at 1 pu voltage. The impedances of the SC correspond to a 300 Mvar synchronous compensator [8].

ESCR, FC	ESCR, SVC	ESCR, SC
$0.97\angle -66°$	$0.97\angle -66°$	$2.36\angle -80°$

Table 2 .1 : ESCR of the Study System at Normal Operating Point (SCR = $1.5\angle -75°$)

It should be noted that it is possible to have different ESCR for a system with a given SCR depending upon the amount of compensation provided. If there is an SVC in the system, the ESCR changes with the reactive power supplied by the SVC within its operating range. The SVC decreases its capacitive impedance during low voltage conditions to generate more capacitive Mvar which can result in reduced ESCR. The reduction of ESCR by the SVC during under voltage conditions may be of considerable consequence for a very weak receiving system. The variation of ESCR of the study system within the operating range of the SVC is shown in Figure 2 .6 .

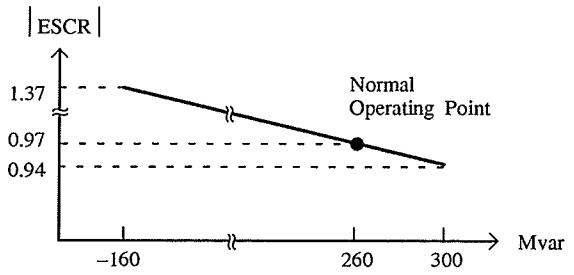


Figure 2 .6 : Range of ESCR of the Study System with the SVC

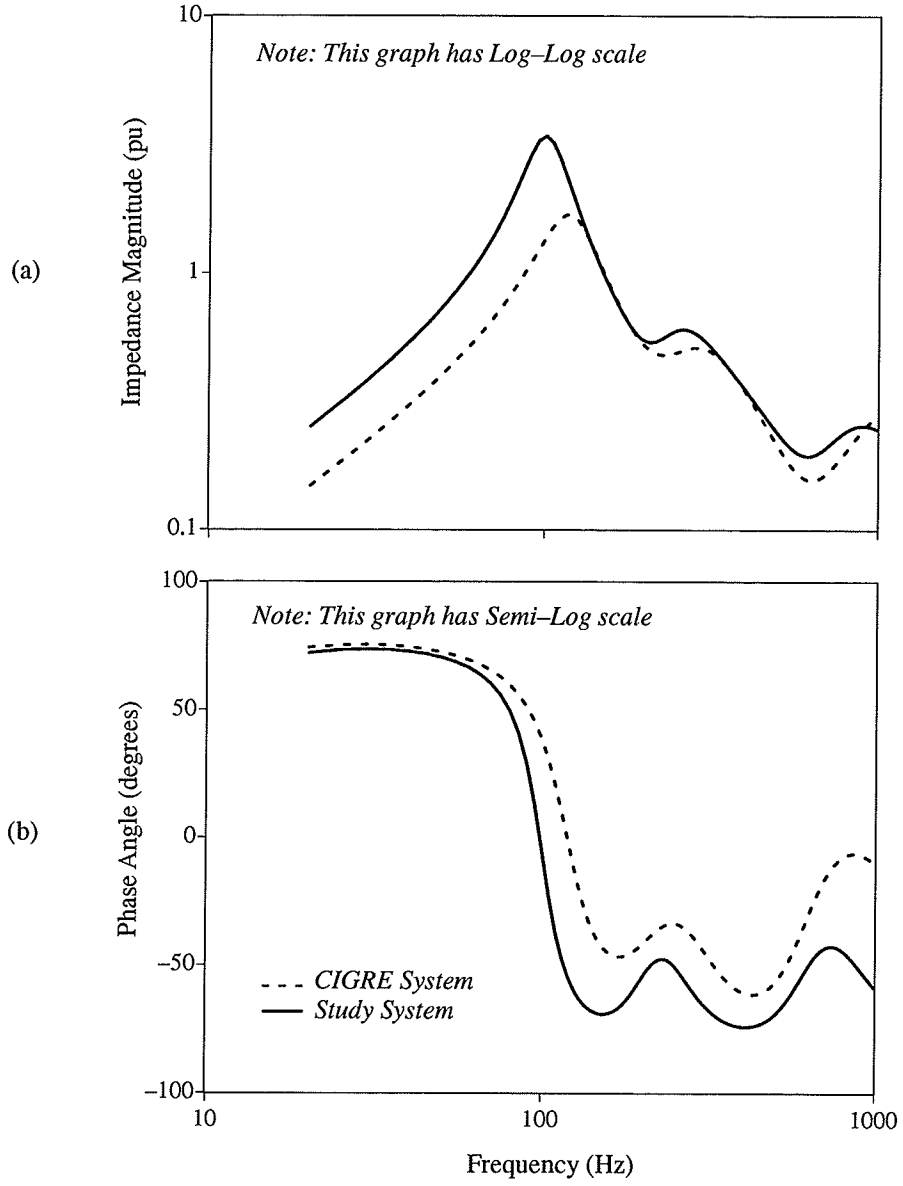


Figure 2 .7 : Frequency Response of the Impedance of the Inverter ac System (Local Load, Filters and Fixed Capacitors Only): (a) Magnitude, and (b) Phase Angle (1 pu Impedance = 52.9 Ω)

2 .2 .7 Frequency Response of Inverter Ac System

Figure 2 .7 shows the frequency response (magnitude and phase angle) of the ac system impedance of the study system (Local Load, Filters and Fixed Capacitors only), and the CIGRE benchmark model. Notice the increased impedance magnitude at the parallel resonance frequencies and the detuning of first parallel resonance frequency from second harmonic (120 Hz) frequency to about 100 Hz due to the change in the ac system equivalent parameters. The

phase angle of the study system is identical to that of the benchmark around the fundamental frequency and differs slightly at higher frequencies.

2 .2 .8 Reactive Power Characteristics at the Inverter Bus

Figure 2 .8 shows the inverter voltage profile vs SVC reactive power supply for the study system of Figure 2 .1 . It illustrates various steady state operating points at normal operation and when the dc is blocked. An SVC rating of –160, +260 Mvar (minimum requirement, refer Section 2 .3) is assumed.

With the SVC blocked and the filters being the only reactive power source at the inverter bus, the inverter voltage would be about 0.72 pu (point–e) in constant current mode. To bring the inverter to the rated power and voltage, SVC has to supply 260 Mvar (point–a). If there is a dc block at this point, the inverter voltage would instantaneously shoot up to 1.6 pu (point–b). Then the SVC will bring the voltage to point–c (1.1 pu). When the dc is unblocked, the inverter voltage would fall to point–d on the regular system characteristics because of the inductive SVC. However, the SVC would bring the system back to the normal operating point–a. All the above steady state operating points with various operating conditions are verified by simulation.

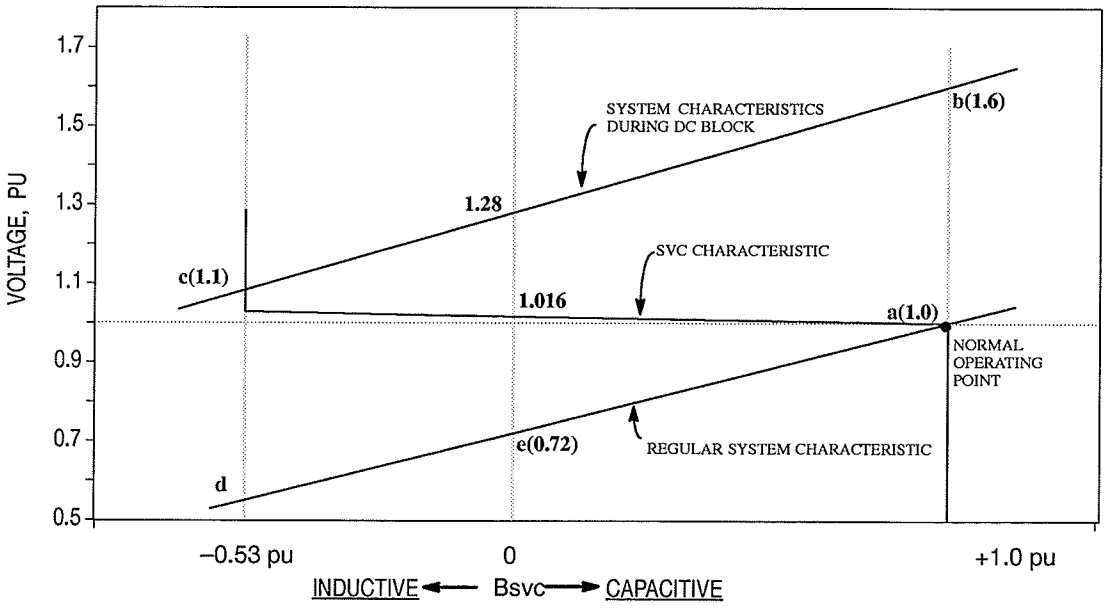


Figure 2 .8 :Reactive Power Characteristics of the Study System with SVC

2 .3 COMPENSATOR SIZING

From the analysis in Section 2 .2 .8 it is clear that the minimum (inductive) rating of the compensator should be at least –160 Mvar and the maximum (capacitive) rating should be at least 260 Mvar. This rating may be increased depending upon any other considerations.

The highest temporary overvoltage (TOV) at the inverter ac bus during permanent dc block is 1.7 pu with fixed capacitors and filters connected. A dynamic compensator of 160 Mvar inductive can bring the TOV to 1.1 pu without switching filters. The capacitive rating of the compensators to fully compensate for the reactive power requirement at the inverter bus at rated power and voltage (so as to obtain unity power factor at the inverter bus looking into the ac system) is 260 Mvar. Thus, a compensator of –160, +260 Mvar rating will meet the above requirements. However, dynamic compensators of slightly higher ratings than this have been used here to provide some additional control range especially during under–voltage conditions.

2 .4 STATIC VAR COMPENSATOR

The SVC model and its controls used in this study are very similar to that of Reference [20].

2 .4 .1 SVC Configuration [20]

The SVC model used here is a 12 pulse TSC and TCR combination. The SVC transformer is modelled by nine coupled windings on the same core. Three windings represent the primary winding and three windings each represent the star and delta secondaries. The TCR and TSC elements are connected in delta, both at star and delta secondaries. The change in TSC stages is effected by changing the capacitance of one stage instead of adding or removing a bank of capacitors. The SVC transformer saturation is modelled as well.

The firing pulses for the TCR thyristors are generated by a grid control system [21] internal to the SVC model. This grid control system uses d–q–z transformation. The SVC model needs TCR firing angle and TSC switching signal from an external control circuit. The SVC controls and its characteristics are discussed in the following sections.

2 .4 .2 SVC Controls

The block diagram of the SVC controls is shown in Figure 2 .9 . The main control units are: measurement unit, error unit, P–I regulator, TSC/TCR allocator, and linearized alpha order generator [20].

Three phase line currents and voltages are measured on the primary side of the SVC transformer. The SVC reactive power (Q_{SVC}, positive if the SVC is capacitive) is calculated from the instantaneous values of current and voltage to calculate the droop contribution ($K \cdot Q_{SVC}$). The sum of measured voltage ($V_{measured}$), droop contribution, and supplementary signal, if any, is passed through filters to eliminate any specific resonant frequency component and high frequency noise. This filtered signal is subtracted from the reference voltage and the resulting error is passed through a proportional and integral regulator. The reference voltage can be adjusted depending upon the operating conditions. The output of the regulator is the susceptance (B_{SVS}) of the SVC and is limited to the ratings (H and L) of the SVC. This susceptance requirement is distributed among the TSC and TCR by the allocator. Hysterisis between the capacitor stages is built into the allocator. Depending upon the B_{SVS} requirement, a capacitor (TSC) ON/OFF signal is generated by the allocator. Then the allocator generates the B_{TCR} order such that the sum of B_{TSC} (susceptance of TSC stages that are ON) and B_{TCR} equals B_{SVS} requirement. The B_{TCR} is passed on to an alpha angle generator, which consults a five segment linearized curve of the relationship between B_{TCR} and firing angle (α), to generate an alpha order. The TSC ON/OFF signal and the alpha order are directly fed to the main SVC circuit.

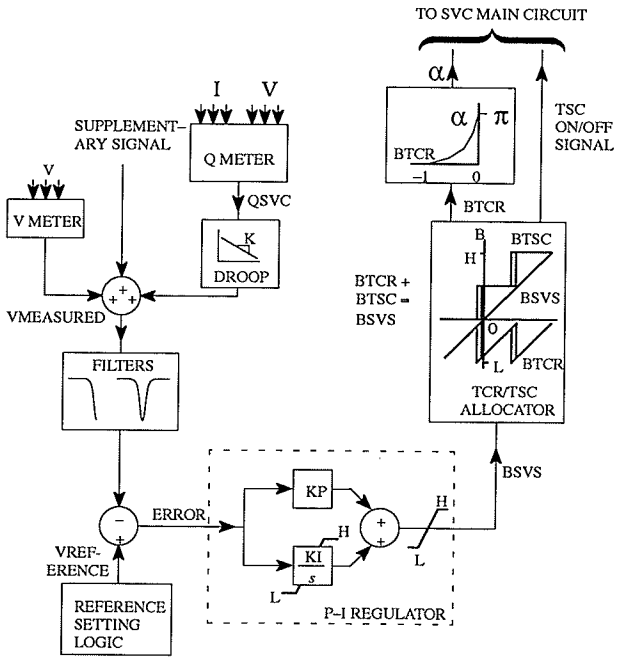


Figure 2 .9 : The SVC Controls

2 .4 .3 TSC/TCR Allocator Characteristics

The allocator characteristics with hysterisis for a two stage TSC/TCR system is shown in Figure 2 .10 . The two TSC stages are of equal ratings. Notice the continuously variable nature of the the B_{SVS} throughout the entire operating range (refer to Section 2 .4 .2 for the definitions of B_{SVS}, B_{TSC}, and B_{TCR}). The sudden changes in the B_{TSC} during capacitor switchings are offset by the equal and opposite changes in the B_{TCR} according to equation (2 .1).

$$B_{TCR} = B_{SVS} - B_{TSC} \qquad (2.1)$$

TSC RATING: 1.0 PU

TCR RATING: 0.6 PU

SWITCHING POINTS

POINTS	Bsvs
a	-0.10
b	-0.05
c	0.40
d	0.45

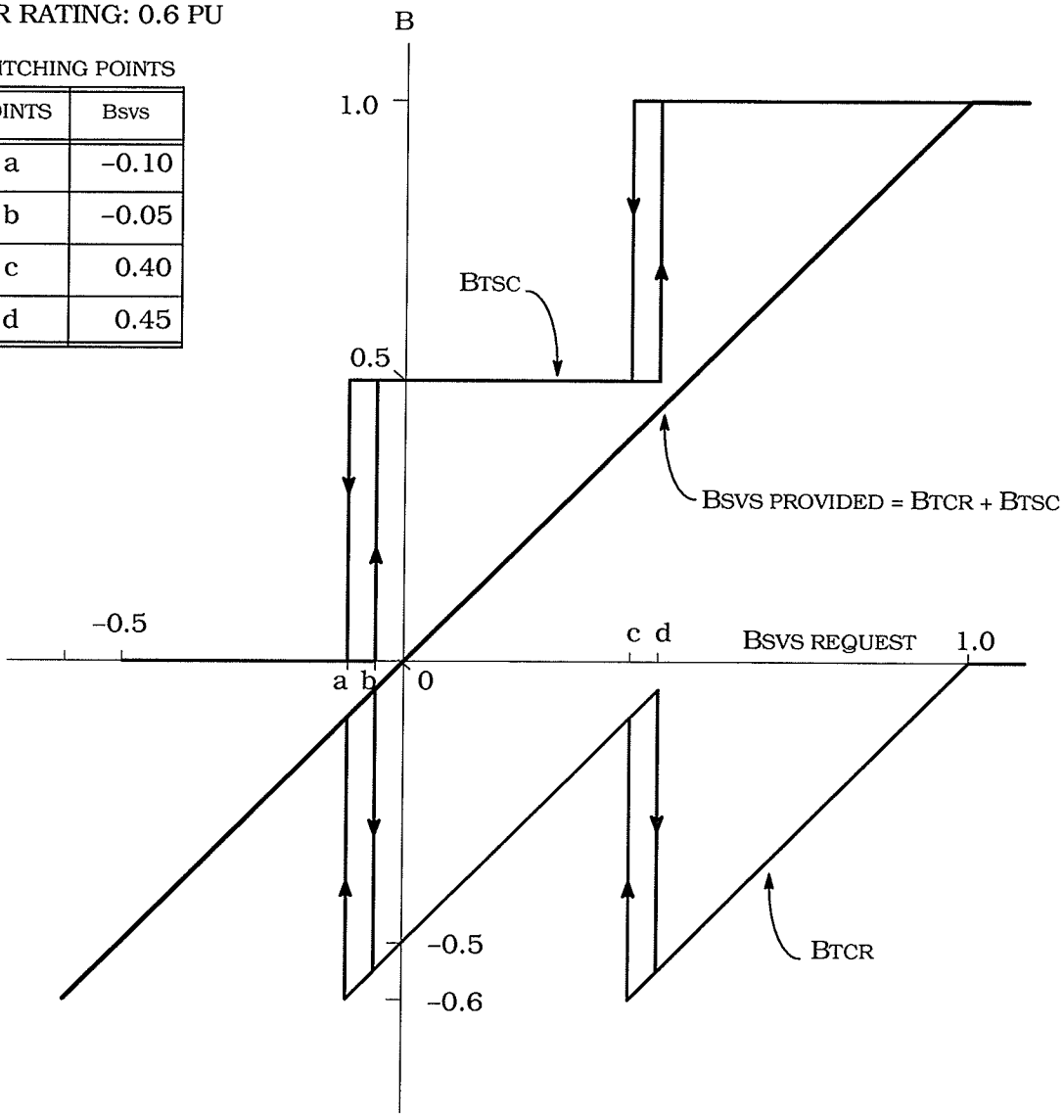


Figure 2 .10 : A Two Stage TSC/TCR Susceptance Characteristics with 10% Hysterisis

2 .4 .4 V – Q Characteristics of an SVC

The V–I characteristics of an SVC with droop is shown in Figure 2 .11 . The line A–B is the controllable region of SVC. Segment B–C is the unstable region under certain circumstances. After the SVC reaches its limits, its output is proportional to its current. When the production demand on the SVC caused by low–voltage is higher than the SVC limits, the production of reactive power itself goes down, causing further reduction of terminal voltage. Unless the reduced voltage reduces the reactive power demand sufficiently, the system will suffer voltage collapse. This is a typical voltage instability situation with constant power loads and one of the reasons why constant power control of dc during certain fault conditions is not stable [3], [15]. As to the absorption side of the SVC, beyond its limits (point A), the SVC loses its control but does not lead to any instability.

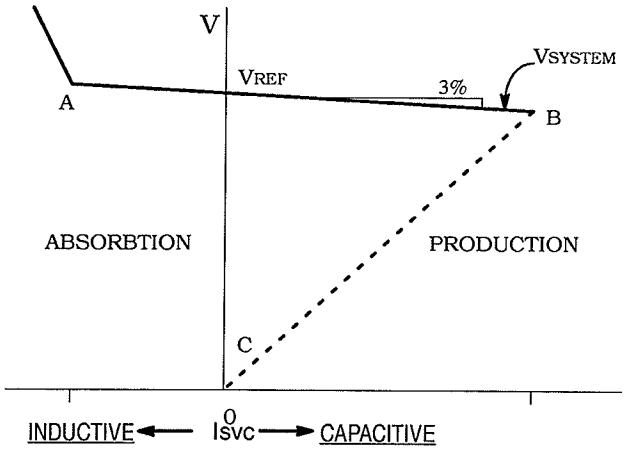


Figure 2 .11 : V–I Characteristics of an SVC with Droop

2 .5 SYNCHRONOUS COMPENSATOR

The synchronous compensator model is represented with Park's equations and includes damper windings and a solid state exciter. The data for the synchronous compensator and unit transformer are based on the recently installed –165, +300 Mvar (nominal rating) synchronous compensator on the Nelson River HVdc system [8].

The block diagram of the static exciter for the synchronous compensator is shown in Figure 2 .12 . The time constants and field forcing limits correspond to those available on modern day exciters. The time constants are significantly smaller and the field forcing limits

are significantly larger than those used by Nyati [10] and Gama [22]. These new parameters have a considerable effect on the speed of response of the synchronous compensator. A 3% current droop based on the full range of the compensator is used.

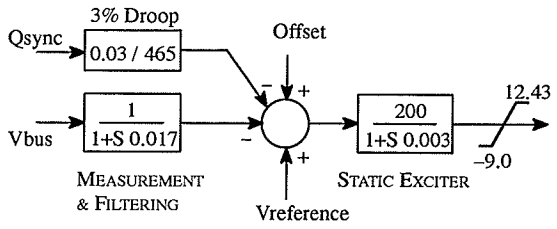


Figure 2 .12 : Static Exciter for Synchronous Compensator

2 .6 COMPENSATION SCHEMES

One fixed compensation scheme and five dynamic compensation schemes with varying ratios of SC and SVC are studied in the next chapter and the details are given below.

1. Fixed Capacitors Only (*FC*), Base Case: This schemes is used as the base case for comparison with the performance of other schemes. Only fixed capacitors of 260 MVar are used in this scheme along with 300 Mvar of filters, to fully compensate the inverter at the rated power. Like the original CIGRE benchmark model, there are no dynamic compensators.

2. Synchronous Compensator Only (*SC*): Only a synchronous compensator of rating –165, +300 Mvar is used as the dynamic voltage control device at the inverter bus of the test system. At steady state, the filters supply 300 Mvar and the synchronous compensator supplies the remaining 260 Mvar.

3. Static Var Compensator Only (*SVC*): Here, two static var compensators of rating –100, +150 MVar each are used as the dynamic voltage control devices at the inverter bus of the test system. At steady state, the filters supply 300 MVar and the SVCs supply the remaining 260 Mvar. The SVC controller uses a 3% droop as in the case of SC. The proportional and integral gains of the SVC controller (2 .9) are chosen to obtain the fastest possible SVC response without jeopardizing the stability of the system.

4. SC and SVC Sharing Equally (*SC+SVC*): The synchronous compensator and one SVC (–100, +150) are connected to the inverter bus in this scheme with the rating of the SC

halved to 150 Mvar. In steady state the SC and SVC each supply 130 Mvar. Filters supply 300Mvar, as in other two cases.

5. SC Sharing 75% and SVC Sharing 25% (*3SC+SVC*): The rating of the synchronous compensator in this scheme has been scaled down to (–120, +225) Mvar which is equal to 75% of the SC rating in the *SC* scheme. The total rating of the SVC in this scheme is (–50, +75) which is equal to 25% of the total rating of the SVC in the *SVC* scheme. In steady state, the SC supplies 195 Mvar and the SVC supplies 65 Mvar.

6. SC Sharing 25% and SVC Sharing 75% (*SC+3SVC*): The rating of the synchronous compensator in this scheme has been scaled down to (–40, +75) Mvar which is equal to 25% of the SC rating in the *SC* scheme. The total rating of the SVC in this scheme is (–150, +225) Mvar which is equal to 75% of the total rating of the SVC in the *SVC* scheme. In steady state, the SC and SVC supply 65 and 135 Mvar, respectively.

2 .6 .1 A Comparison of the Ratings of All Compensation Schemes

The Mvar ratings of all the five dynamic compensator schemes and the base case (*FC*) discussed above are depicted in Figure 2 .13 . The horizontal label at the bottom of the chart represents the name of the scheme. Total height of the bar represents the rating of the scheme and the height of the individual shade represents the rating of the individual devices (SC, SVC) for that scheme.

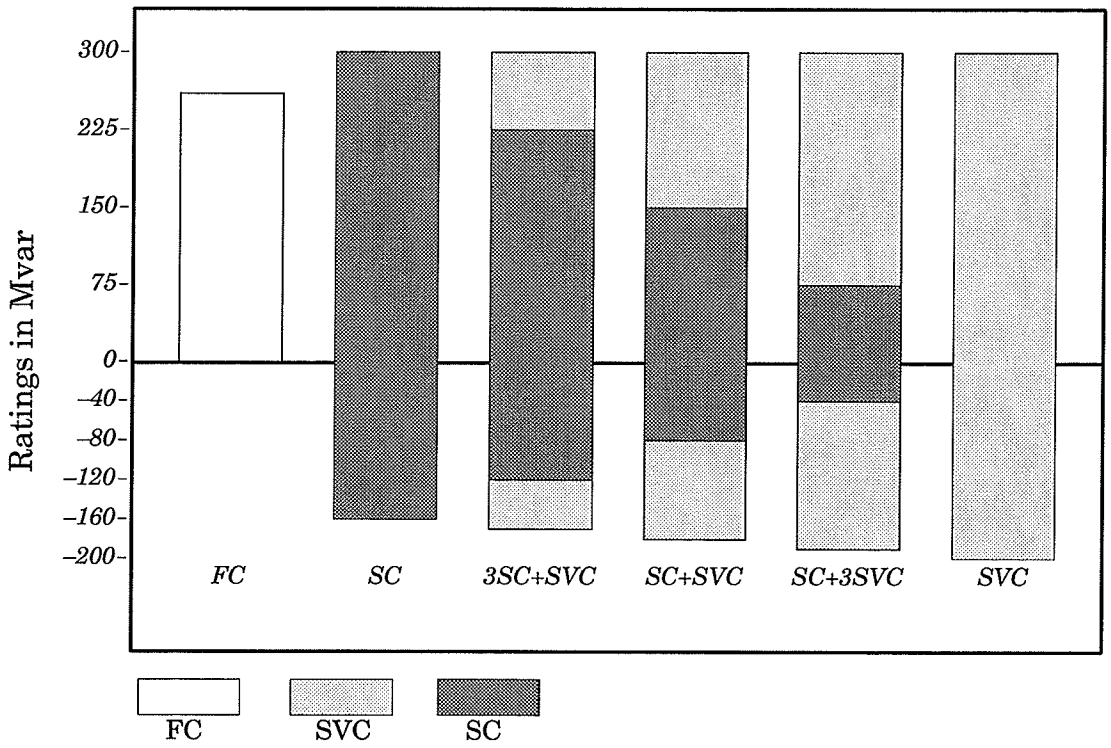


Figure 2 .13 : Device Ratings in Various Compensation Schemes

2 .7 DEFINITION OF SPEED OF RESPONSE OF COMPENSATORS

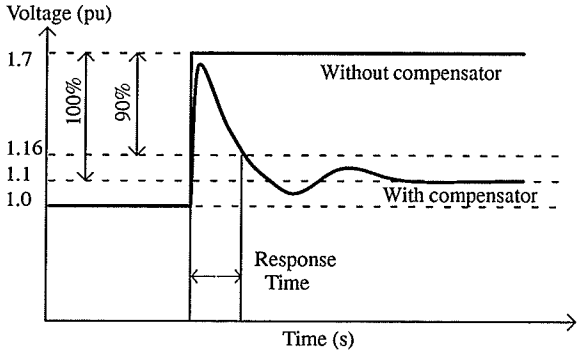


Figure 2 .14 : The Definition of Response Time of Compensators [1]

For a dc block disturbance, the fundamental frequency temporary overvoltage, without compensator action or filter capacitor tripping is 1.7 pu for the study system. The dynamic compensation schemes discussed above are designed to bring this overvoltage to 1.1 pu in the steady state without tripping of the filter capacitors. Further reduction is usually achieved by a switching action such as partial filter tripping. The response time of the compensator is defined

as the time taken for the compensator to accomplish 90% of its total final correction. This definition is depicted graphically in 2 .14 and will be used to measure the response time of various compensation schemes in the next chapter. This definition is from reference [1] by CIGRE 14.03.

2 .8 DISTURBANCES

Various ac faults, both on the inverter and rectifier ac systems, and dc faults have been studied. Details on these faults and the simulation results are presented in the next chapter on simulation results.

Chapter 3

Compensator Performances

3.1 INTRODUCTION

Many tests were conducted to study the performance of different compensator schemes. Although it would have been ideal to present in detail all the simulation results of all the tests, it is not feasible considering the readability and the volume of the thesis. Only such parameters (curves) of a given test essential in discussing the dynamics of that test have been presented. Some of the results presented in this chapter can be found in Reference [23][#].

Out of a total of six compensator schemes studied, the following four schemes were studied in detail. The compensator ratings for all the schemes are given in Section 2.6.

i) Fixed Capacitor Only (*FC* [§]), Base Case

ii) Synchronous Compensator Only (*SC*)

iii) Static Var Compensator (*SVC*)

iv) SC and SVC sharing equally (*SC+SVC*)

The other two schemes, the studies regarding which have been reported here in brief, are:

v) SC sharing 75% and the SVC sharing 25% (*3SC +SVC*)

vi) SC sharing 25% and the SVC sharing 75% (*SC +3SVC*)

Schemes v) and vi) are intended to demonstrate how the compensator performance varies with the ratio of the SC and the SVC mix. These results are presented at the end of this chapter.

The author of the thesis is one of the authors of the paper.

§ The italicized *FC, SC and SVC* represent the compensation schemes using the devices Fixed Capacitors, Synchronous Compensators, and Static Var Compensators, respectively. Non–italicized, they represent the actual devices themselves.

3 .2 SVC WITH VERY WEAK AC SYSTEMS

The dc control of the system with *SVC* scheme is different from the dc controls of the system with other schemes due to an additional feature. A commutation failure protection circuit was introduced which could be activated on detection of the first commutation failure to avoid repeated failures.

The need for such a commutation failure protection circuit (CFPC) or some other measure for the *SVC* scheme is shown in this section through simulation results.

3 .2 .1 SVC Without Commutation Failure Protection Circuit

Figure 3 .1 shows the inverter dc power recovery for a five cycle single phase to ground fault at the inverter bus for all four schemes. The complementary resonances in the model, and low ESCR of the inverter compounded by the asymmetry in the firing of the valves introduced by the single line to ground fault, result in responses which are in general worse than the three phase fault case. These effects are most pronounced in the *SVC* scheme which has the lowest ESCR of all the schemes when both TSCs are connected and the TCR is completely off. There is a single commutation failure with the fixed capacitors (*FC*) and multiple commutation failures with the *SVC*. There are no commutation failures in the schemes where SC is present because the ac system is stronger with the SC than with the FC or SVC. Although *FC* and *SVC* schemes have the same ESCR during the steady state operation, the *SVC* has an increased number of commutation failures than the *FC* scheme during the recovery from the L–G fault. This behavior can be attributed to the dynamics of the SVC. Immediately after the fault is cleared, the SVC senses the low voltage as the ac voltage is recovering causing the TCR to back off while keeping all the capacitors on. As in the case of *FC*, the first commutation failure occurs with the *SVC*. The dynamic control of TCR during recovery from the first commutation failure combined with the already low ESCR of the system produces subsequent commutation failures with the SVC. However, with fixed capacitors, subsequent commutation failures do not occur due to the absence of dynamic perturbations as caused by the TCR of the *SVC* scheme and also due the ESCR being slightly higher during recovery with FC than with SVC.

By considerably decreasing the SVC gains repeated commutation failures can be avoided. But the smaller SVC gains slow down the SVC response to an unacceptable degree. The option of reducing the SVC gains to such low levels had to be excluded from the list of possible remedies

since it is necessary to maintain a reasonably fast SVC response to effectively control the overvoltages and minor undervoltages. This prompted an investigation of other options to avoid the repeated commutation failures. The solution adopted here is to force the inverter firing angle to a minimum value on detection of the first commutation failure, and then gradually ramp up the firing angle so that the control is smoothly transferred back to the valve group controller.

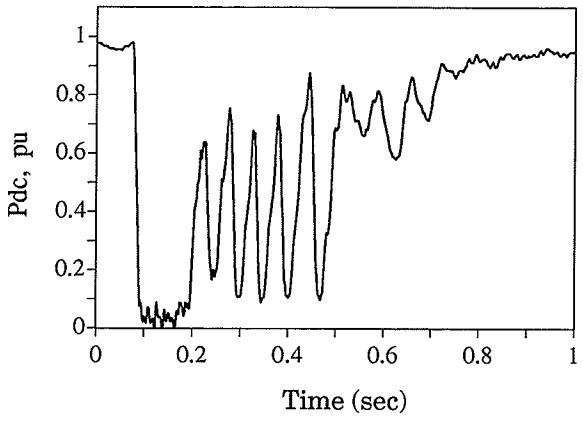


Figure 3 .1 : Dc Power for SVC case for a L–G Fault at the Inverter Bus without Commutation Failure Protection Circuit

3 .2 .2 The Commutation Failure Protection Circuit (CFPC)

Figure 5 .1 gives the details of the commutation failure protection circuit designed to work for the kind of disturbances used in this thesis. A two step ramp is adopted to expedite the recovery. The slopes of the ramp are selected by trial and error to give the fastest recovery without causing repeated commutation failures. During normal operation when there is no commutation failure, the output from the ramp circuit is 180° and the α order from the valve group controller is less than 180°. The α order from the valve group controller is passed onto the valves through the minimum selection block. On detection of a commutation failure, the firing angle is reduced to 110° for 200 milliseconds. This period usually includes the duration of the fault since the first commutation failure occurs at the onset of the fault which causes extreme low voltages at the inverter bus. The firing angle is then ramped up rapidly to 130° during the next 300 milliseconds to enable a fast initial recovery. However, the inverter cannot sustain this high rate of ramp at the time of the transition to the valve group controller. The ramp is made more gradual beyond 130°. The transition of the control modes usually takes place between 135° and 150°. The ramp is activated if there is a commutation failure during the fault.

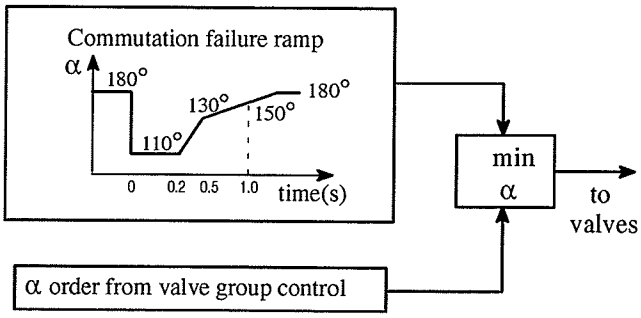


Figure 3 .2 : Firing Angle Reduction and Ramping Circuit

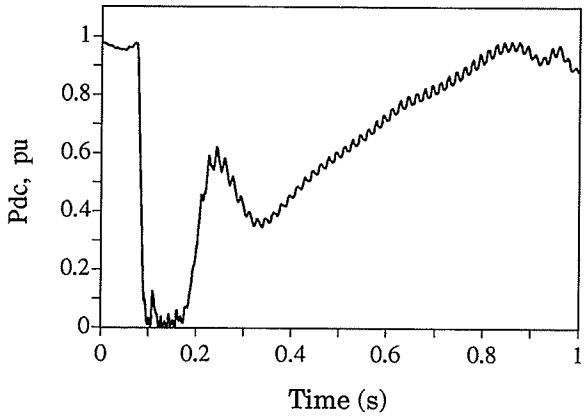


Figure 3 .3 : Dc Power for SVC case for a L–G Fault at the Inverter Bus with Commutation Failure Protection Ramp

3 .2 .3 Improved Results with CFPC for the SVC

Figure 3 .3 depicts the same results as in Figure 3 .1 but with the commutation failure protection circuit incorporated. Naturally, the recovery is slowed down due to the ramp, but repeated commutation failures are prevented. Figure 3 .4 shows the inverter extinction angle (gamma), firing angle, and dc current, both with and without the commutation failure protection circuit. Thus, several commutation failures result if the CFPC is absent.

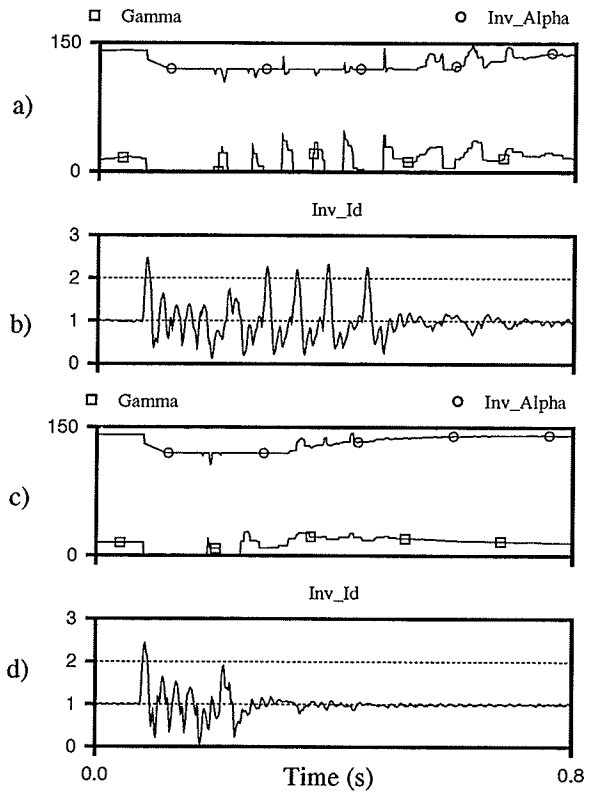


Figure 3 .4 :Results of an L–G Fault with SVC : a) and b) without Commutation Failure Protection Circuit, c) and d) with the Circuit.

All the test results of *SVC* case presented in this chapter for comparing the compensator performance include the protection circuit discussed above. However, the circuit activated only when there is a commutation failure. Thus, the CFPC is activated neither during a remote fault nor during a dc block fault. This ensures that the slow CFPC ramp is only applied if necessary, and normally the SVC has a very fast response.

3 .3 DISTURBANCES

The sections to follow describe the performance of various options under different disturbances. The disturbances considered are:

Inverter Faults

1. Inverter Close–in Single Phase to Ground fault, (ICL–G)
2. Inverter Close–in Three Phase to Ground fault, (ICLLL–G)

3. Inverter Remote Single Phase to Ground fault, (IRL–G)

4. Inverter Remote Three Phase to Ground fault, (IRLLL–G)

Rectifier Faults

5. Rectifier Close–in Single Phase to Ground fault, (RCL–G)

6. Rectifier Close–in Three Phase to Ground fault, (RCLLL–G)

Dc Faults

7. Permanent DC (Inverter) Block, (DC–Blk)

8. DC Line Fault, (DCL–G)

All the ac faults are for a duration of five cycles. The discussion of the results are arranged in the above order.

3 .4 INVERTER CLOSE–IN FAULTS

Single phase and three phase to ground faults at the inverter bus have been analyzed in this section.

3 .4 .1 Inverter Close–in Single Phase to Ground Fault (ICL–G)

Figure 3 .5 and Figure 3 .6 show the inverter dc power and ac rms voltage recovery for a five cycle single phase to ground fault at the inverter bus. The following observations were made.

– The *SC* and the *SC+SVC* schemes give the fastest power recovery time to 0.8 pu power. The fixed capacitor recovery is somewhat slower.

– The *SVC* shows the poorest recovery time, partly due to the commutation failure protection action discussed earlier, which is necessary to be included with the SVC option. Although the SVC itself is a fast acting device, its use in a very low SCR system can produce repeated commutation failures. The thyristor switched capacitor (TSC) banks of the SVC lower the ESCR and the further rapid control action of the thyristor controlled reactor (TCR) in this low ESCR environment causes unstable operation. The protection circuit discussed in Section 3 .2 .2 has been utilized to prevent commutation failures. Lowering the SVC gains is another way of preventing this instability, but in that case, the response time for controlling temporary overvoltages – the prime purpose of the SVC – becomes unacceptable.

– The recovery of ac rms voltage (Figure 3 .6) is similar to the dc power recovery discussed above.

The responses are more oscillatory for this single phase fault than those for a three phase fault discussed in Section 3 .4 .2 due to the asymmetry in the firing introduced by the single line fault. The single phase fault takes a slightly longer time to recover than the three phase fault. Table 3 .1 gives the time required to recover 0.8 pu power for all the schemes.

FC	SC	SVC	SVC+SC
335 ms	135 ms	585 ms	135 ms

Table 3 .1 : Recovery Times for ICL–G Fault from Figure 3 .5

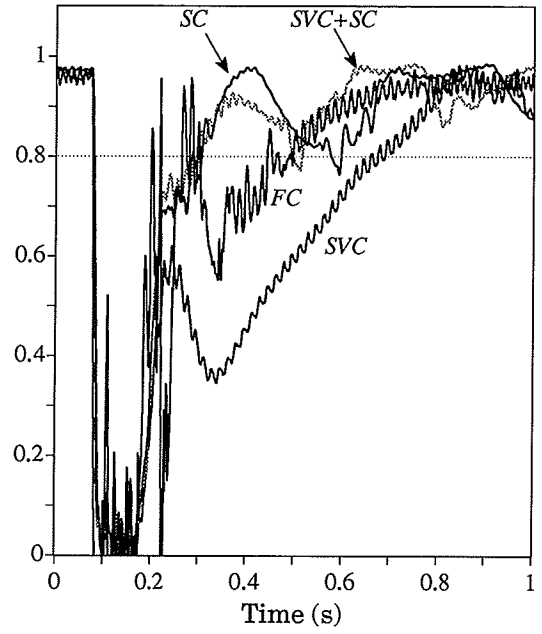


Figure 3 .5 : Inverter dc Power, ICL–G

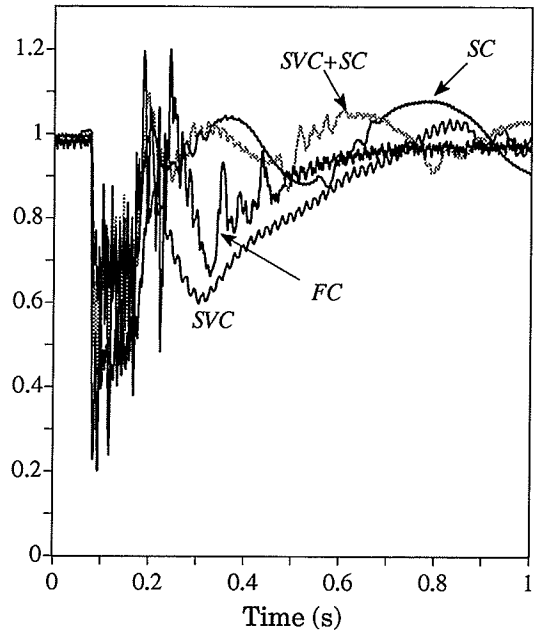


Figure 3 .6 : Inverter Vrms, ICL–G

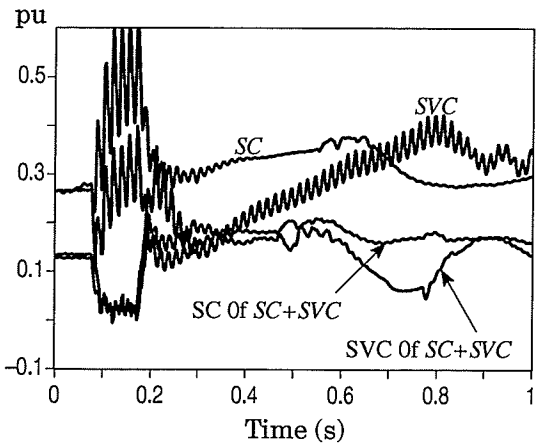


Figure 3 .7 : Compensator Q, ICL–G

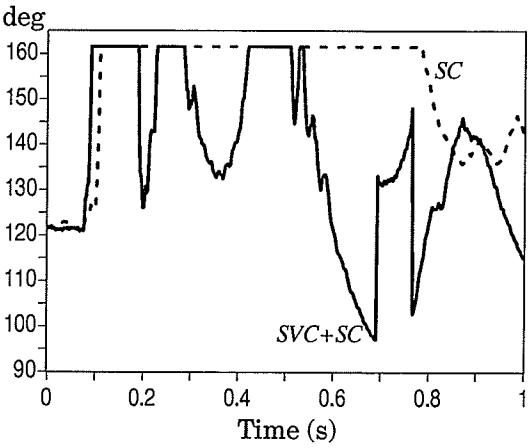


Figure 3 .8 : TCR Firing Angle, ICL–G

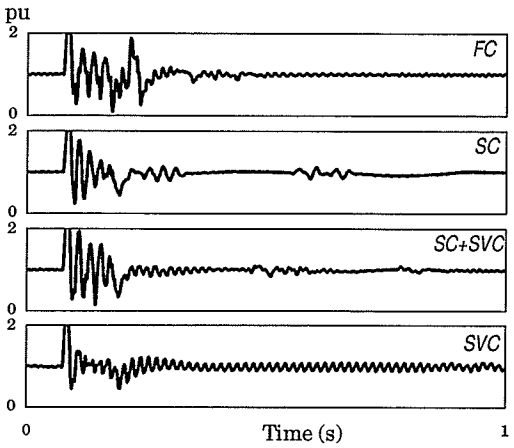


Figure 3 .9 : Inverter Dc Current, ICL–G

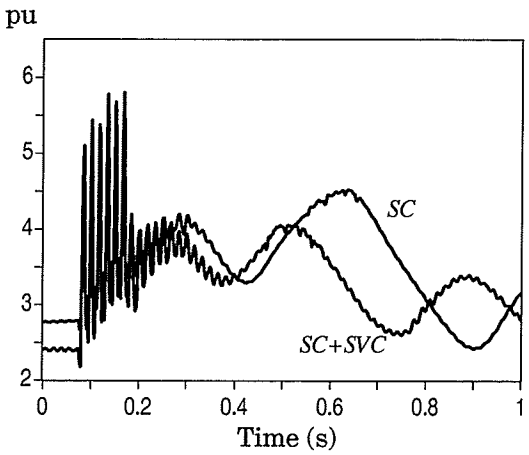


Figure 3 .10 : SC Field Current, ICL–G

The reactive power of the SC and the SVC for different schemes is presented in Figure 3 .7 . The steady state reactive power supplied by either of the compensators for the *SC+SVC* scheme is about half of that of *SC* or *SVC* scheme. When both compensators are connected, they share the reactive power requirement equally. The reactive power supplied by the *SVC* during recovery is significantly less compared to that supplied by the *SC* scheme due to the commutation failure protection circuit being active. However, in comparing the reactive power of the two devices for the *SC+SVC* scheme, the SVC oscillates with a phase difference of 180° with respect to the SC, thus providing a smooth joint supply of Vars. This shows the natural coordination between the two devices when used in conjunction with each other. The positive effect of such a coordination can also be seen from the smoother recovery of power and voltage (*SC+SVC* in Figures 3 .5 and 3 .6). The SVC also assists the SC in reducing its electro–mechanical swings in power and voltage.

Figure 3 .8 shows the alpha order for the TCR. Notice the higher oscillations in the *SC+SVC* scheme as the SVC tries to compensate for the SC oscillations. Figure 3 .9 shows the inverter dc current. Figure 3 .10 gives the synchronous compensator field current. The assistance of the SVC in controlling the voltage oscillations at the SC terminal (which is also the SVC voltage bus) results in reduced oscillation in the SC field current in the *SC+SVC* scheme, and thus results in more damping of power oscillations.

3 .4 .2 Inverter Close-in Three Phase to Ground Fault (ICLLL–G)

Figure 3 .11 shows the inverter dc power during a five cycle three phase to ground fault at the inverter bus. The *SC* or *SC+SVC* schemes offer similar recovery. Recovery for the Fixed

capacitor scheme is somewhat slower than recovery of other schemes with SC in them. In preventing repeated commutation failures, the *SVC* scheme has to make use of the commutation failure protection circuit, thereby increasing the power recovery time. Table 3 .2 gives the time required to recover to 0.8 pu dc power for all the schemes.

FC	SC	SVC	SVC+SC
235 ms	135 ms	485 ms	135 ms

Table 3 .2 : Recovery Times for Inverter LLL–G Faults from Figure 3 .11

The ac rms voltage at the inverter bus is shown in Figure 3 .12 . Figure 3 .13 presents the compensator reactive power for the different schemes. The dc current at the inverter is given in Figure 3 .15 . The α order of the TCR of the SVC and the field current of the SC are shown in Figures 3 .14 and 3 .16 , respectively. On comparing the results of this fault with the corresponding quantities of the single phase fault, it can be seen that the L–G fault is more severe than the LLL–G fault. This is a variation from what is normally experienced in systems with high SCR, in which the LLL–G fault is more severe.

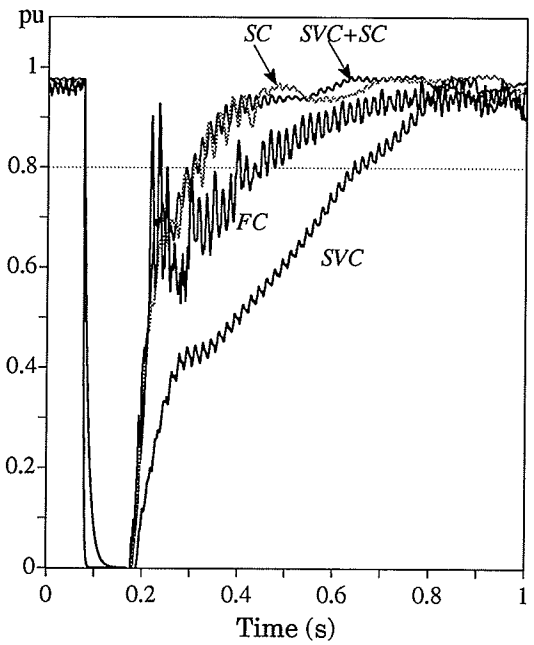


Figure 3 .11 : Dc Power, Inverter ICLLL–G

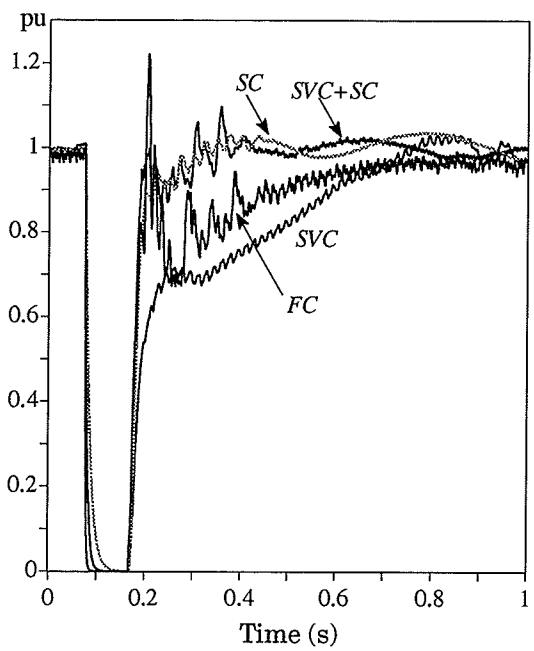


Figure 3 .12 : Inverter Vrms, Inverter ICLLL–G

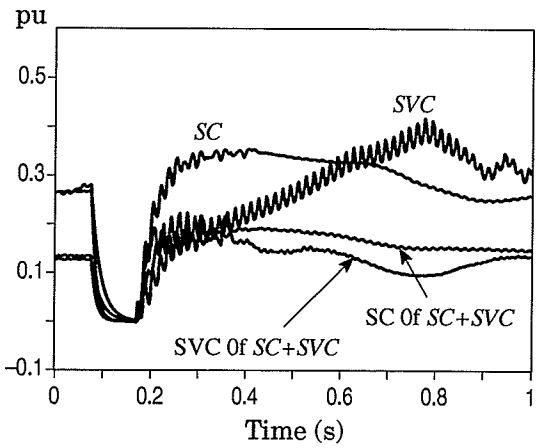


Figure 3 .13 : Compensator Q, ICLLL–G

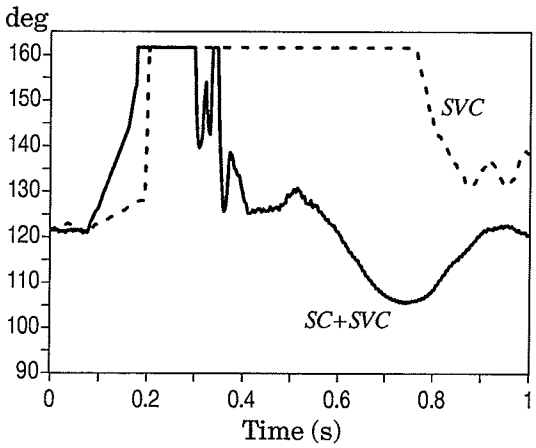


Figure 3 .14 : TCR Firing Angle, ICLLL–G

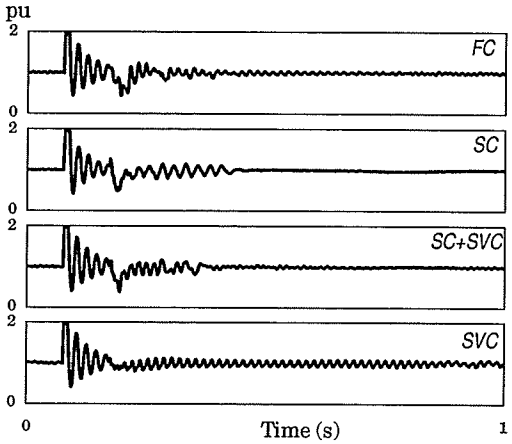


Figure 3 .15 : Dc Current, ICLLL–G

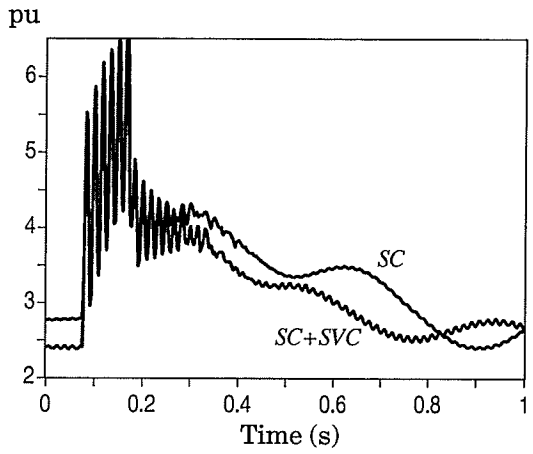


Figure 3 .16 : SC Field Current, ICLLL–G

3 .5 INVERTER REMOTE FAULTS

In the simulation, the ac system equivalent was modelled in two identical sections connected in series. The remote faults are created by applying either a LLL–G or L–G short circuit for five cycles at the junction of these sections. The recovery of all schemes for these faults is faster than recovery of the corresponding close–in faults.

3 .5 .1 Inverter Remote Single Phase to Ground Fault (IRL–G)

Figure 3 .17 presents the dc power during a remote single line to ground fault on the inverter side ac system. Although the power recovery with the *SVC* is more oscillatory than the *SC* for the first 300 ms after the fault is cleared, the *SVC* settles down faster than the *SC*. Broadly speaking, the power recovery of all four schemes for this fault is alike.

The rms voltage at the inverter bus is shown in Figure 3 .18 . The ac voltage during the fault is about 0.7 pu with no commutation failures and the recovery is faster than in the close–in single

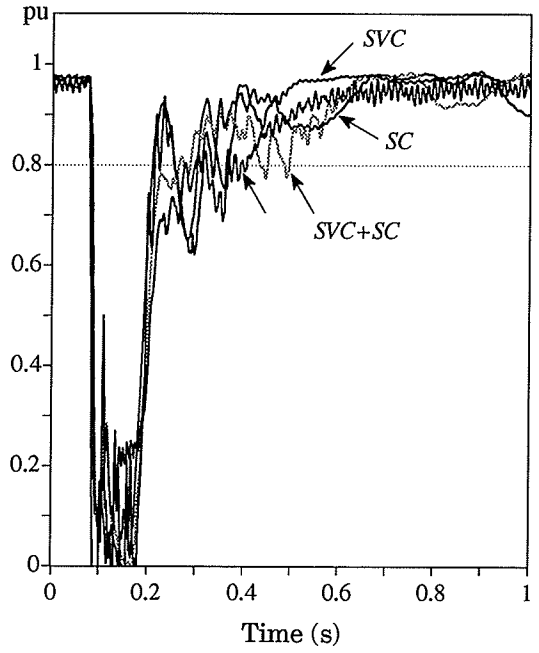


Figure 3 .17 : Dc Power, IRL–G

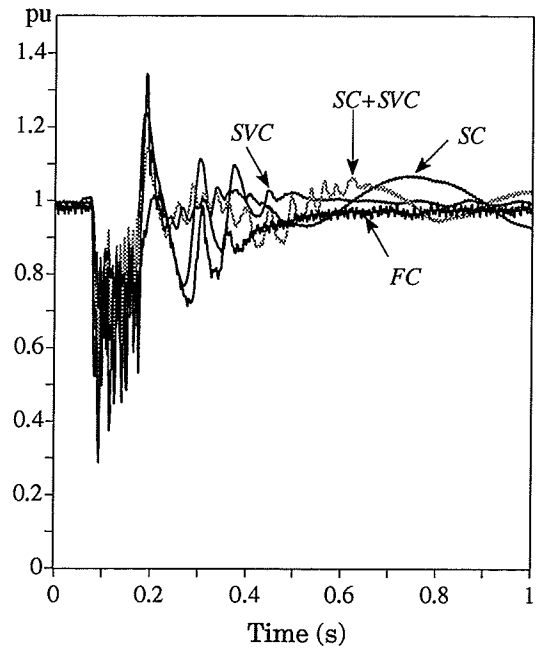


Figure 3 .18 : Inverter Vrms, IRL–G

phase fault. Since there are no commutation failures during recovery from the fault, the CFPC for *SVC* is not activated. The ac voltage fluctuates the most in the *SVC* scheme during the initial period of recovery but it is the first scheme to settle down to steady state value as well.

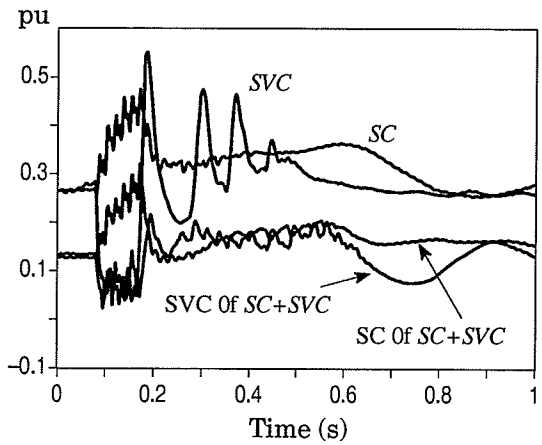


Figure 3 .19 : Compensator Q, IRL–G

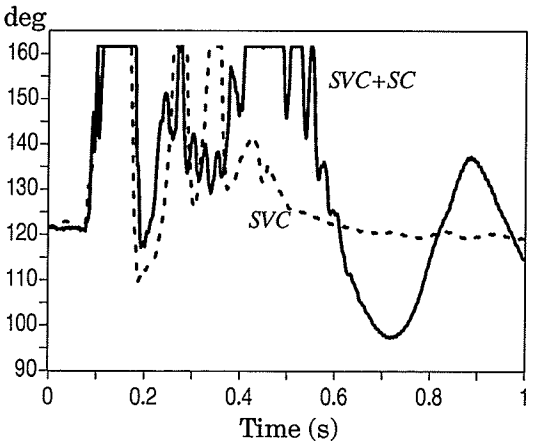


Figure 3 .20 : TCR Firing Angle, IRL–G

Figure 3 .19 shows the compensator reactive power. Notice the large oscillations in the *SVC* Vars, corresponding to the fluctuation in the ac voltage, immediately after the fault is cleared. Such oscillations in the *SC+SVC* case are eliminated because of the voltage support provided by the SC during the initial recovery. Figure 3 .20 shows the alpha angle of the TCR. The near–two hertz oscillations in the alpha order after 0.6 seconds is due to the result of the SVC's effort to

counteract the near–two hertz voltage oscillations produced by the synchronous compensator's mechanical inertia. Inverter dc current and the synchronous condensor field current are presented in Figures 3 .21 and 3 .22 , respectively.

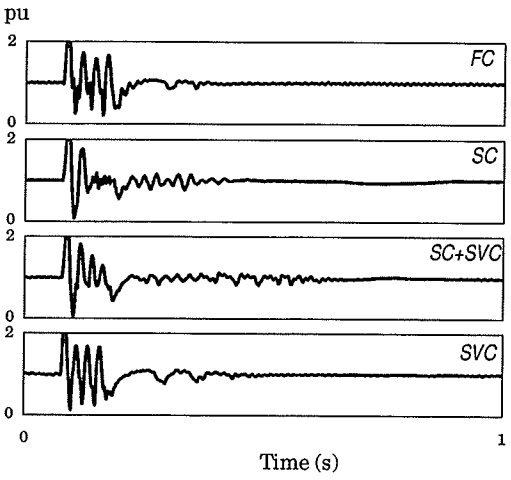


Figure 3 .21 : Dc Current, IRL–G

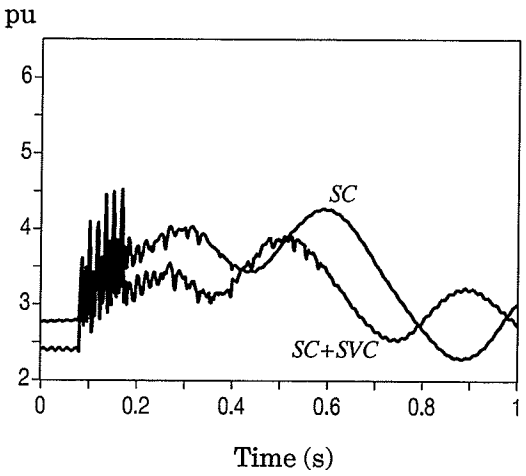


Figure 3 .22 : SC Field Current, IRL–G

3 .5 .2 Inverter Remote Three Phase to Ground Fault (IRLLL–G)

Figure 3 .23 shows the dc power during a remote three phase fault on the inverter side ac system. Like the remote single phase fault discussed in Section 3 .5 .1 , the CFPC is not active here as well. It is clear that the power recovery of the *SC* is the fastest while the *SVC* is the slowest – even slower than the fixed capacitor scheme. This obviously needs some explanation for the *SVC* case. An examination of the ac voltage recovery of *SVC* (Figure 3 .24) indicates that the voltage recovery is also the slowest. The TCR α order from Figure 3 .25 shows that the TCR is completely off during the entire recovery period and the capacitor banks of the TSC are fully on due to sustained undervoltage condition. Thus the SVC operates like a fixed capacitor. Then the *SVC* should perform at least as fast as the fixed capacitor scheme. The measured gamma form Figure 3 .26 for the *FC* and the *SVC* case indicates that the gamma controller of the *SVC* scheme has difficulty in settling down to its steady state value. Referring back to Section 2 .2 .4 , we had observed that as the ESCR (SCR) of the system becomes smaller, the interaction between ac side dynamics with the dc controls increases, causing longer recovery time, and that the dc controls were adjusted for an ESCR of 0.97 corresponding to the *FC* case. Since the TCR is completely off while the TSC is completely on, the system ESCR is lower than the ESCR of the *FC* scheme. The low ESCR system causes the long recovery period for the *SVC*. Hence, the gamma controller has to settle down before the TCR can regain control. The recovery period for

the *SVC* can be improved by modifying the dc controls. As such, the results from this test cannot be used for evaluating the *SVC* performance. However, they serve to point out that the dc control should be designed such that it is suitable for the lowest ESCR the SVC can create within its operating range.

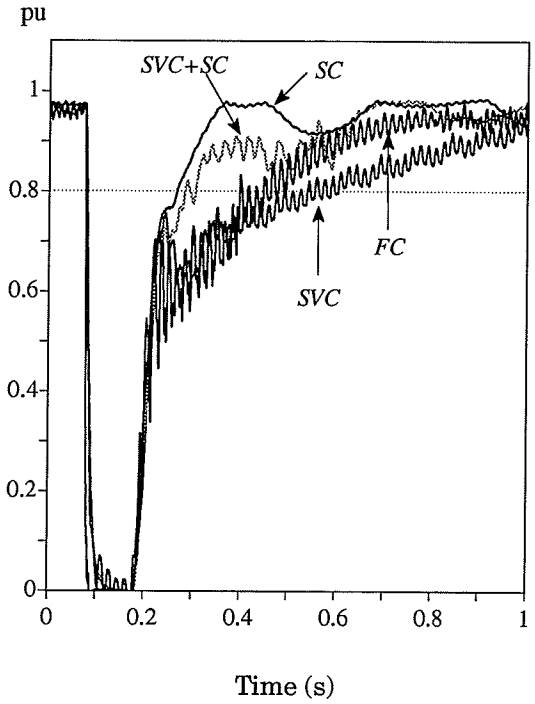


Figure 3 .23 : Dc Power, IRLLL–G

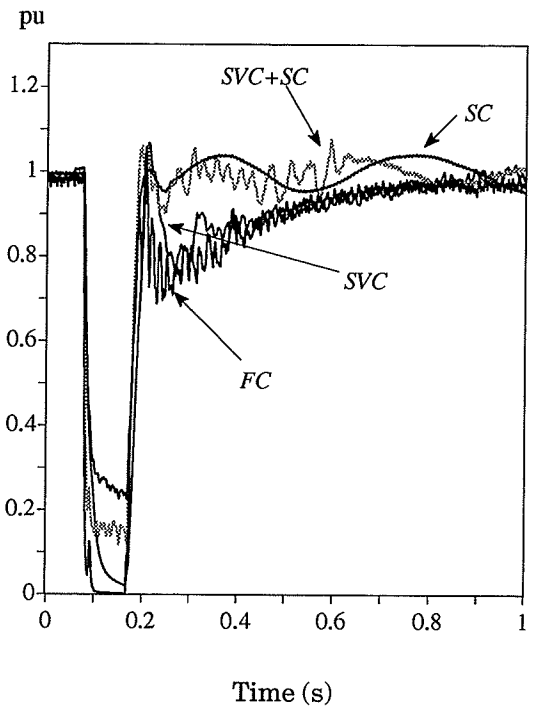


Figure 3 .24 : Inverter Vrms, IRLLL–G

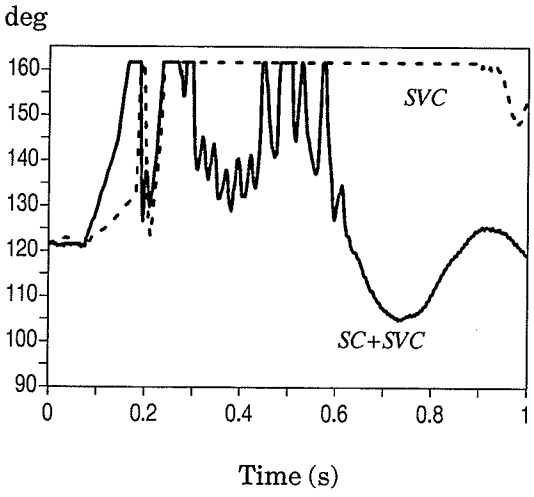


Figure 3 .25 : TCR Alpha Angle, IRLLL–G

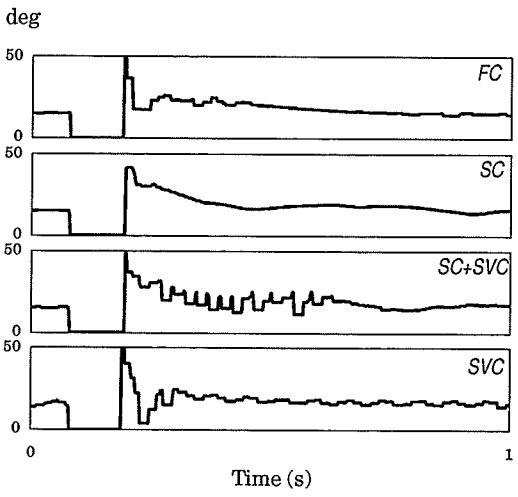


Figure 3 .26 : Measured Gamma, IRLLL–G

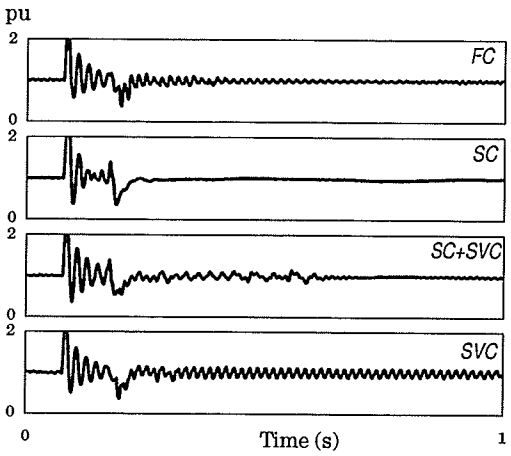


Figure 3 .27 : Inverter Dc Current, IRLLL–G

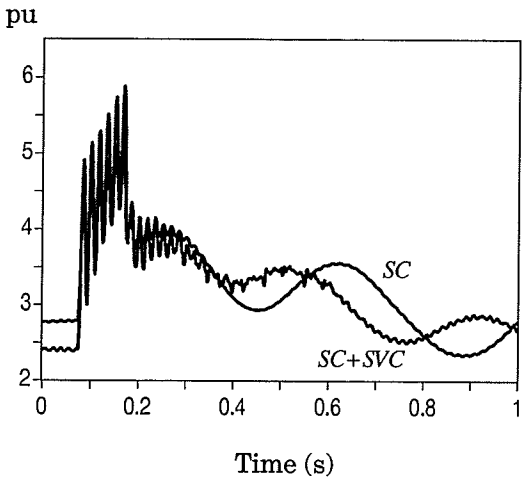


Figure 3 .28 : SC Field Current, IRLLL–G

3 .6 RECTIFIER FAULTS

Single phase and three phase to ground fault at the rectifier bus have been analyzed in this section.

3 .6 .1 Rectifier Close–in Single Phase to Ground Fault (RCL–G)

As shown in Figure 3 .29 the dc power recovery during a single phase to ground fault at the rectifier busy is similar for all four compensation schemes. The rms voltage at the inverter bus is shown is shown in Figure 3 .30 and the voltage recovery is similar for all four compensation schemes. There are no commutation failures in any of the schemes as can be seen from Figure 3 .31 . The CFPC is not active for the SVC option. The effect of harmonic disturbances due to this fault is more severe than that during a single line fault at the inverter. This can be seen by comparing the dc currents shown by Figures 3 .32 and 3 .9 for rectifier and inverter single line faults, respectively. As a result of the interference of the dc current disturbances with the dc controls, the power and voltage recovery beyond 0.8 pu (approximately) takes an abnormally longer time. The effect is seen in all four schemes. The dc controls can be tuned to improve the recovery time of all the schemes, but this effort is not included in the scope of this thesis.

In general, the rectifier single line to ground fault is not as severe as the corresponding inverter fault. The recovery time is shorter in case of rectifier single line fault as compared to the corresponding inverter fault.

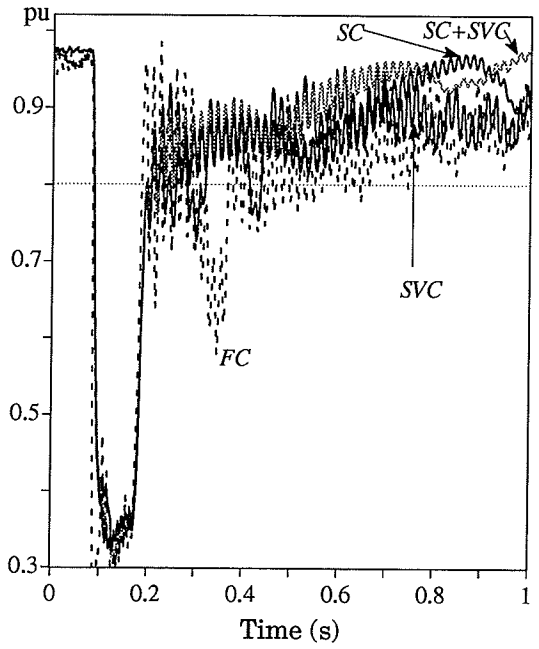


Figure 3 .29 : Inverter Dc Power, RCL–G

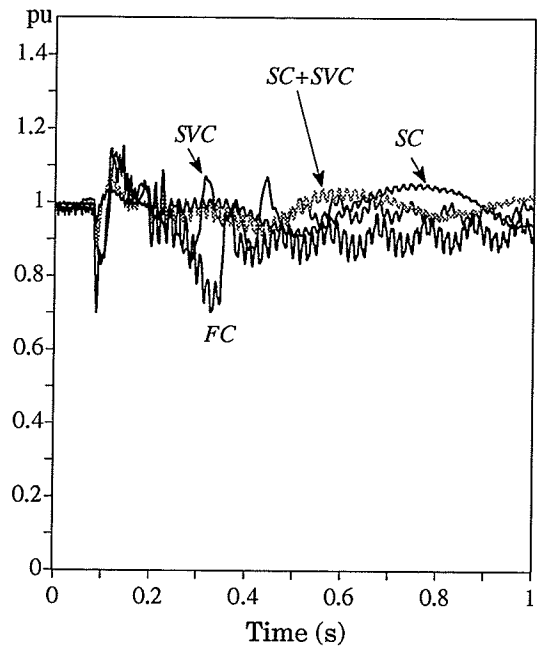


Figure 3 .30 : Inverter Vrms, RCL–G

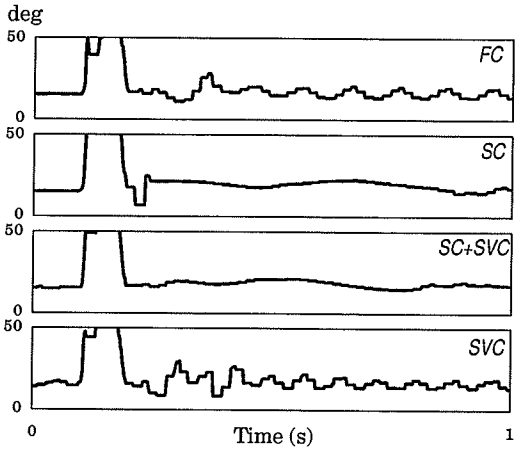


Figure 3 .31 : Measured Extinction Angle, RCL–G

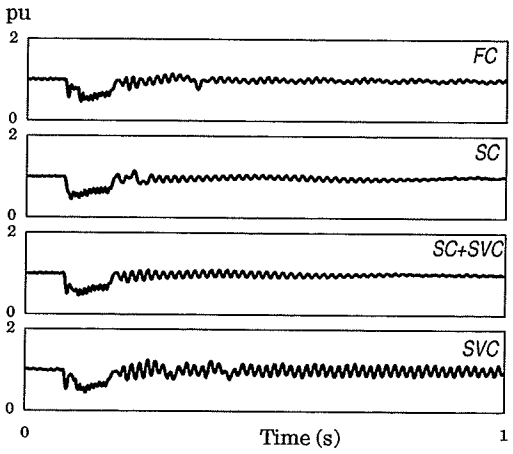


Figure 3 .32 : Dc Current, RCL–G

3 .6 .2 Rectifier Close–in Three Phase to Ground Fault (RCLLL–G)

All the observations made in the previous section (3 .6 .1) regarding the rectifier single line to ground fault (RCL–G) hold true in the case of a three phase to ground fault (RCLLL–G) at the rectifier. However, the recovery from a three phase fault is less severe than the recovery from a single phase fault. This is consistent with the observations made in Section 3 .4 regarding the close–in faults at the inverter. The dc power, ac rms voltage, extinction angle, and the dc current are shown in Figures 3 .33 , 3 .34 , 3 .35 , and 3 .36 , respectively. Note that the dc current during fault is not zero because of the dc line time constant being larger than the duration of fault.

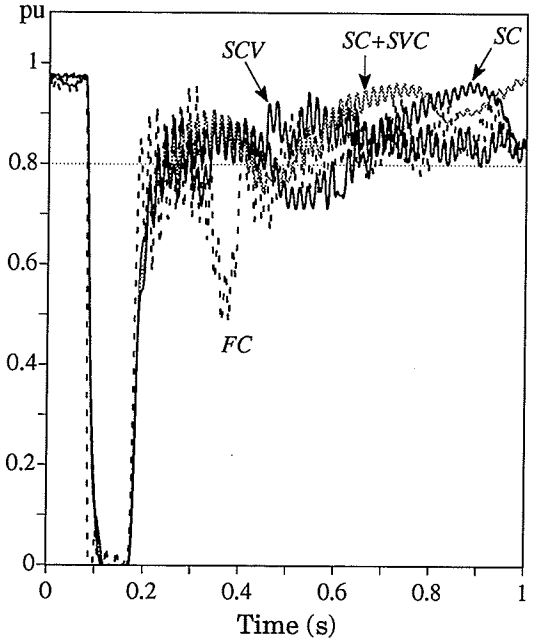


Figure 3 .33 : Inverter Dc Power, RCLLL–G

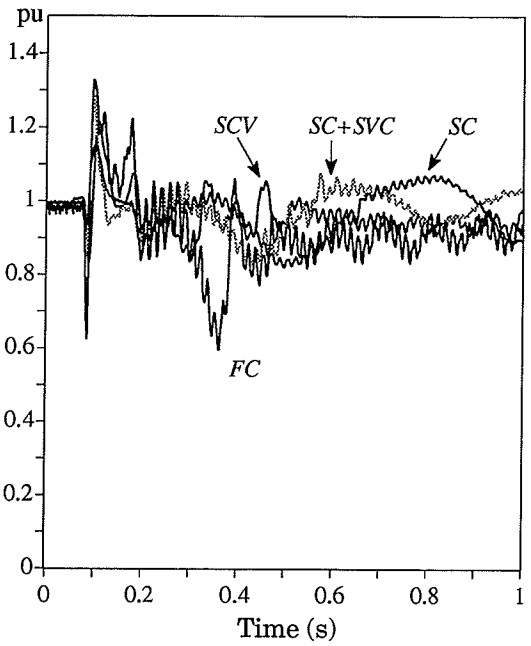


Figure 3 .34 : Inverter Vrms, RCLLL–G

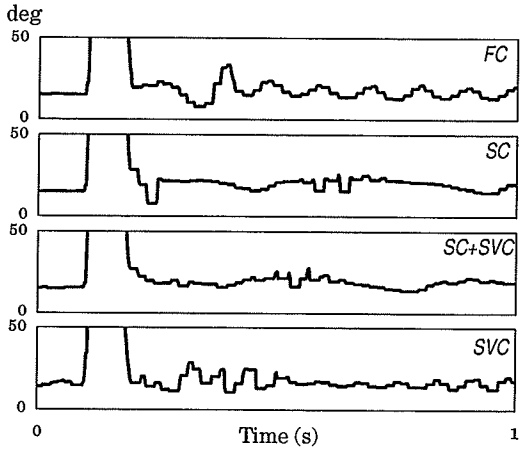


Figure 3 .35 : Measured Extinction Angle, RCLLL–G

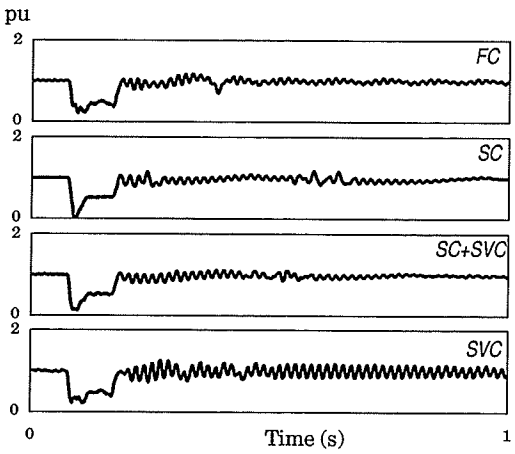


Figure 3 .36 : Dc Current, RCLLL–G

3 .7 PERMANENT DC BLOCK (DC–Blk)

Figure 3 .37 gives the temporary overvoltage (TOV) magnitudes for a permanent block of the inverter. The dc voltage at the mid–point of the dc cable is shown in Figure 3 .38 . The dc voltage goes to zero during the dc block, however the dc current (Figure 3 .39) is maintained at the current order level through the bypass switch at the inverter. The power transfer will become zero as the dc voltage goes to zero. The compensator reactive power (Q) is shown in Figure 3 .40 . The steady state reactive power supplied by the compensators depend on the reactive power rating of the compensators. The steady state reactive power supply after the fault is slightly

higher than the compensator rating because of the higher than nominal voltage (1.1 pu) after the dc block.

The TCR alpha angle is shown in Figure 3 .41 . Immediately following the dc block both the capacitor stages of TSC are disconnected as indicated by the sudden increase of the TCR alpha angle. However, the TCR and the TSC combined provides a smooth reactive power supply as shown in Figure 3 .39 due to the properly designed SVC controller that coordinates the TCR and the TSC.

The field current of the synchronous machine for the *SC* and *SC+SVC* scheme is shown in Figure 3 .42 . The field current is reduced to zero in less than 400 ms after the dc block. Such a short time is achieved mainly due to the high field forcing limits which help the SC to bring down the the overvoltage faster than the earlier designs of synchronous compensators used by Nyati [10], and Gama [22].

The following comments can be made:

- The base case (*FC*) with fixed capacitors produces an initial overvoltage peak of 1.7 pu and subsequently decays due to converter transformer saturation (Vsat = 1.22 pu) [13] to a steady state value of 1.37 pu. There is no voltage control action taken in the base case.
- The *SC* scheme produces a smaller first overvoltage peak (1.3 pu) which is subsequently reduced with a response time of 470 ms (see Section 2 .7 for a definition of response time). Moreover, the response has a two Hertz oscillation due to the rotor dynamics of the synchronous machine
- The *SVC* scheme has the initial peak of 1.7 pu, same as the base case, but reduces the overvoltage more rapidly (response time of 173 ms) as compared to the *SC* scheme. There are also no rotor inertia related oscillations.
- The *SC+SVC* combination gives a first peak of 1.5 pu, smaller than that of the *SVC* scheme. The response time is 173 ms, similar to the *SVC* scheme. The oscillations are also significantly less than those compared with the SC case.

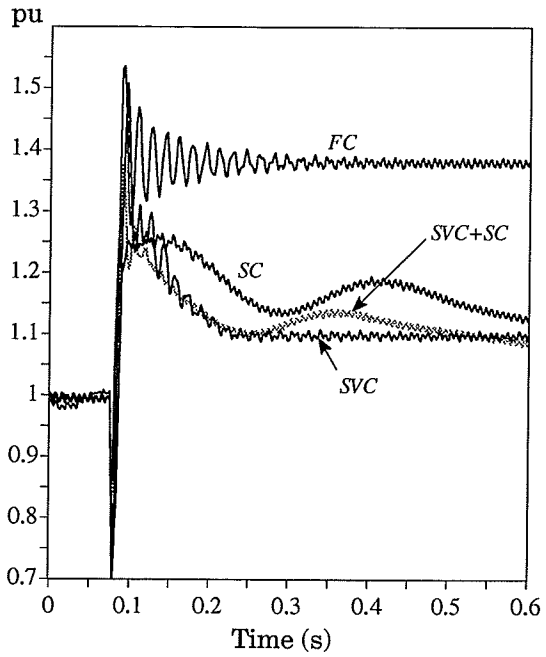


Figure 3 .37 : Inverter ac RMS Voltage, DC–Blk

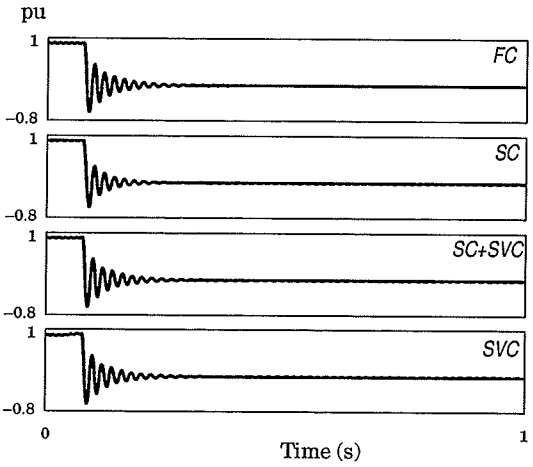


Figure 3 .38 : Mid–Point Dc Voltage, DC–Blk

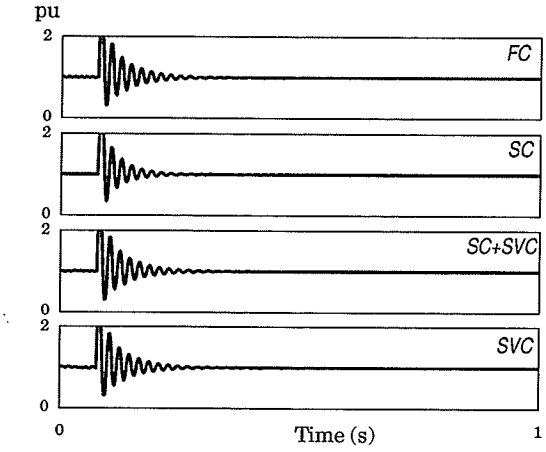


Figure 3 .39 : Dc Current, DC–Blk

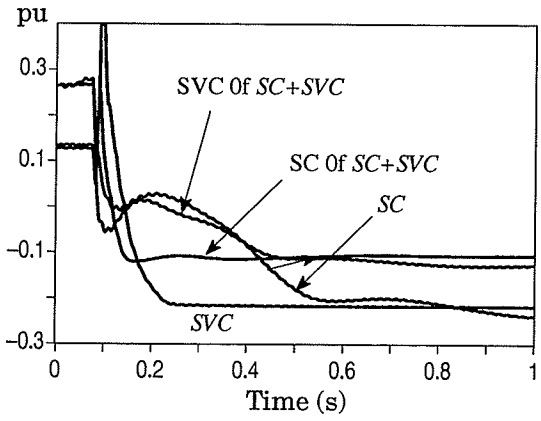


Figure 3 .40 : Compensator Q, DC–Blk

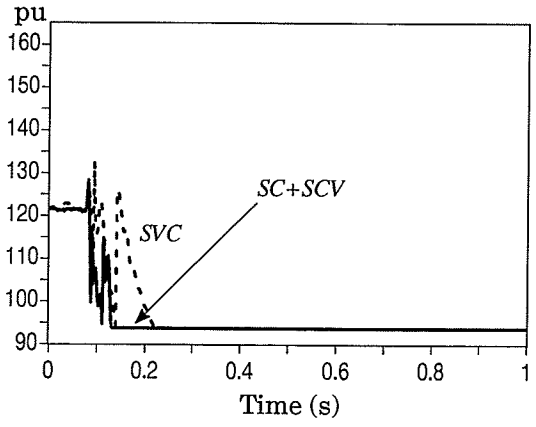


Figure 3 .41 : TCR Alpha Angle, DC–Blk

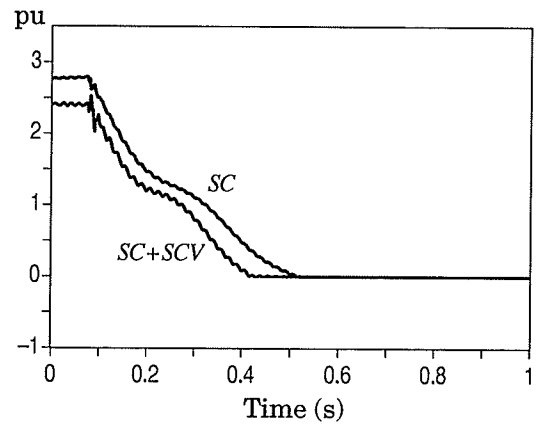


Figure 3 .42 : SC Field Current, DC–Blk

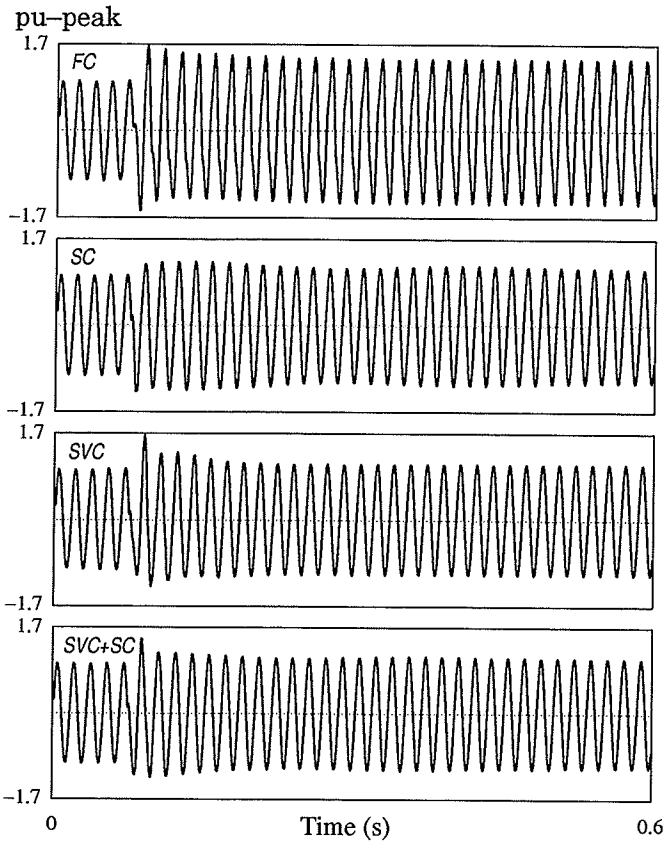


Figure 3 .43 : Phase A Voltage During Permanent dc Block

Figure 3 .43 shows the instantaneous voltages in one phase in order to show the magnitude of the first peak (1 pu–peak base = $\sqrt{2}$· pu base). Table 3 .3 gives the *Response Time* obtained from Figures 3 .37 and the magnitude of the first peak of overvoltage calculated based on Figure 3 .43 .

	Response Time	First Peak of TOV
SC	470 ms	1.30 pu
SVC	173 ms	1.70 pu
SC+SVC	173 ms	1.50 pu

Table 3 .3 : Response Time and First Peak of TOV for Dynamic Compensator Schemes for a dc Block

3 .8 DC LINE FAULT (DCL–G)

3 .8 .1 Force–Retard Circuit

Faults on the dc side are cleared by force–retarding the firing angle of the rectifier and the inverter as shown in Figure 3 .44 . The firing angle at the converters is increased to 135° and

maintained there for 100 milliseconds (*deionization time*), after which it is gradually ramped down to 0° during the next 100 milliseconds so that the normal control modes can take over smoothly. The data for the force–retard circuit is similar to that used in the Nelson River system, however, some adjustments were made to this circuit by trial and error to make it suitable for the study system. The ramp rate was adjusted to enable a commutation failure–free recovery for the *SC* scheme and the deionization time was adjusted to insure that the magnitude of the post fault power swings of the synchronous compensator are minimum. This force–retard circuit is used in all the schemes.

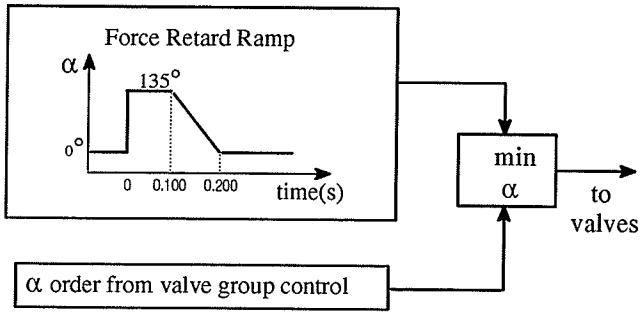


Figure 3 .44 : Force Retard Circuit for Rectifier and Inverter

3 .8 .2 Simulation Results

The dc fault studied in this section is created by short circuiting the dc line to ground at the mid–point of the dc cable. Figure 3 .45 shows the dc power during such a fault. The *FC* scheme has a better recovery than the *SC* scheme. Due to its inertia, the synchronous compensator develops the frequency swings during the force retard operation and these swings last for about two seconds after the initial recovery. Consequently, the ac voltage and the dc power are also affected. A careful selection of the deionization time and the rate of ramp can reduce these oscillations but cannot eliminate them. The *SVC* suffers from repeated commutation failures if the commutation failure protection circuit (CFPC) is not activated. Hence the results presented here are with the CFPC active. The power recovery of the *SVC* with active CFPC is superior to that of *SC* scheme due to the absence of *SC* power swings. The power recovery with the *SC+SVC* scheme is marginally better than that of the *SC* scheme.

Figure 3 .46 shows the ac rms voltage at the inverter bus. There is overvoltage in all schemes during the dc fault because the dc power is reduced to zero and the reactive power consumption

of the inverter is drastically reduced. The control of overvoltage by the different schemes during the dc line fault is somewhat similar to that during the dc block fault discussed in Section 3 .7 . All three dynamic compensation schemes were able to control the overvoltage to below 1.1 pu within the first 100 ms from the onset of the fault. Because of the rotor inertia, the synchronous compensator has the worst recovery of all schemes. The fixed capacitor option has the best recovery although the overvoltage during the fault is the highest with this option. The *SC+SVC* scheme has one commutation failure, whereas the *SC* and the *FC* schemes have none.

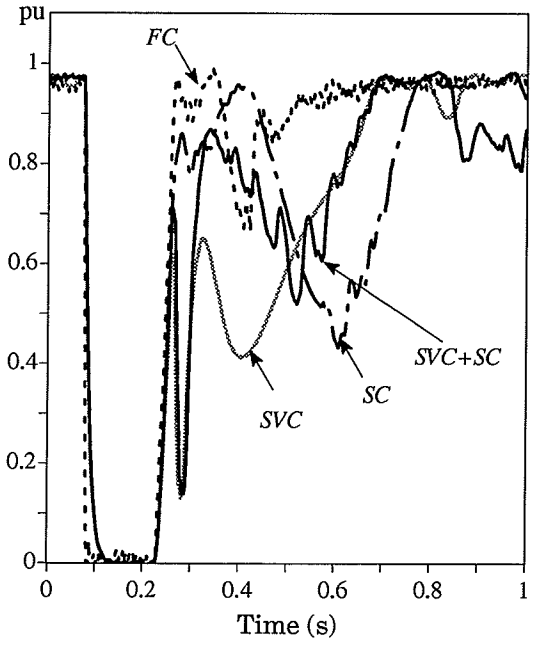


Figure 3 .45 : Inverter dc Power, DCL–G

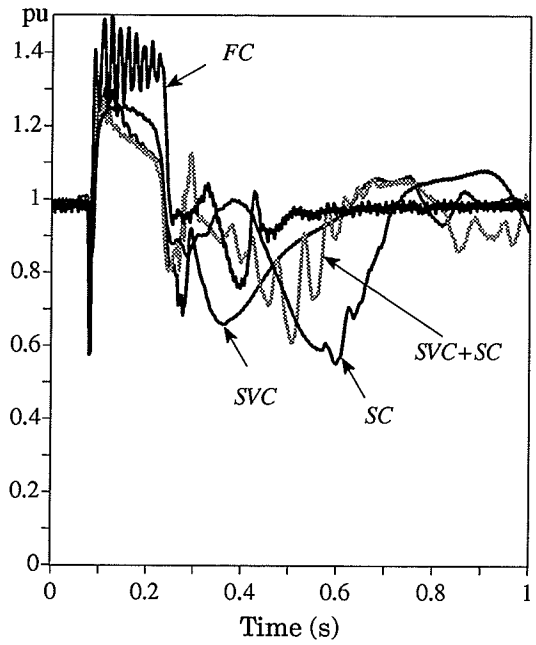


Figure 3 .46 : Inverter Vrms, DCL–G

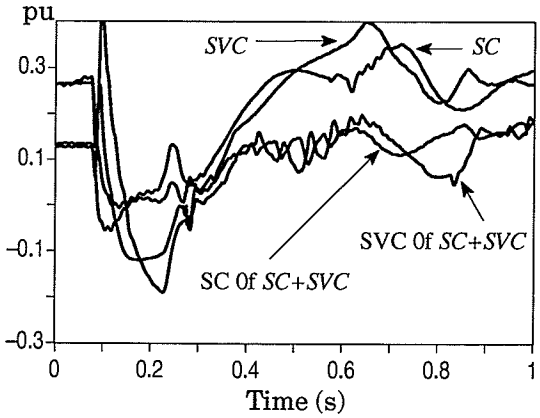


Figure 3 .47 : Compensator Q, DCL–G

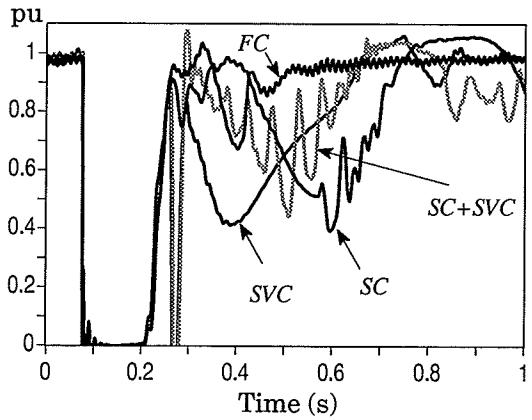


Figure 3 .48 : Mid–point Dc Voltage, DCL–G

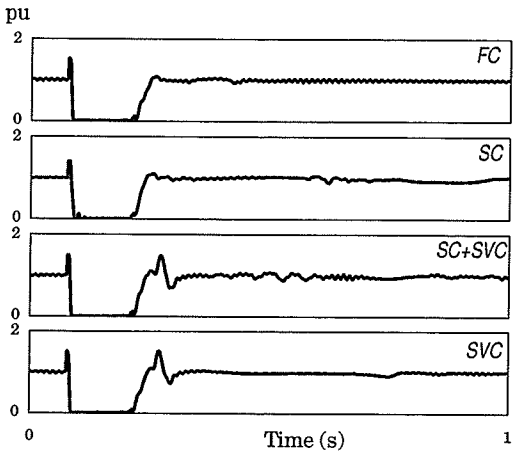


Figure 3 .49 : Rectifier Dc Current, DCL–G

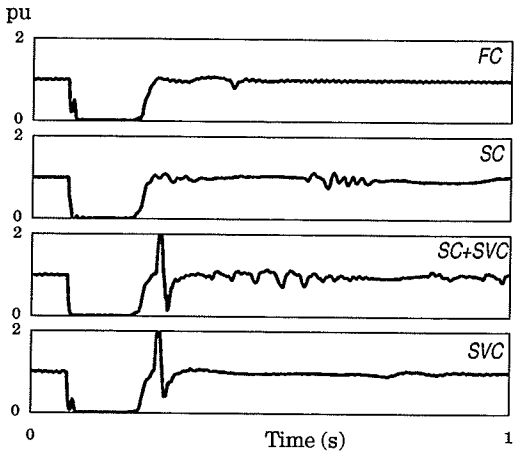


Figure 3 .50 : Inverter Dc Current, DCL–G

The reactive power supplied by the compensators is shown in Figure 3 .47 . The voltage at the mid–point of the dc cable where the fault occurred is given in Figure 3 .48 . The dc current plots of Figures 3 .49 and 3 .50 are useful in showing that the force–retard was effective in driving the converter currents to zero to facilitate the clearing of the fault.

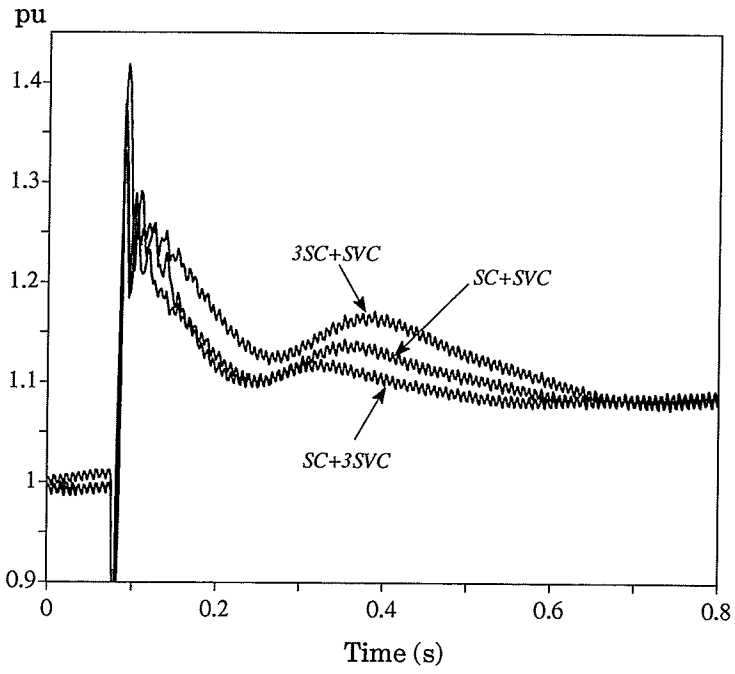


Figure 3 .51 : Inverter ac RMS Voltage During a dc Block Fault with Different Combinations of SC and SVC

3 .8 .3 Other Combinations of SC and SVC

This section presents the overvoltage performance during a dc block disturbance for two schemes with a mix of SC and SVC (the scheme with an equal mix SC and SVC *(SC+SVC)* has been

discussed in detail in earlier sections). They are:

- SC sharing 75% and the SVC sharing 25% (*3SC +SVC*)
- SC sharing 25% and the SVC sharing 75% (*SC +3SVC*)

As can be seen from Figure 3 .51 , an increased share of SC results in a more oscillatory response and a longer time to reach steady state. On the other hand, an increased share of SVC causes a higher initial overvoltage (peak). An equal mix of SC and SVC appears to be a better solution for this system.

3 .9 CONCLUSIONS

The following conclusions can be made based on the study system and the simulation results presented in this chapter..

- CIGRE benchmark model has been successfully modified to include dynamic compensators and a very low SCR receiving ac system.
- *SVC* has fastest response for load rejection type of faults but has to be slowed down to avoid repeated commutation failures during close–in ac faults for very weak ac systems. Thus, it has the slowest response for close–in ac faults.
- *SC* limits the 1st overvoltage peak to the lowest value of all the options considered (1.3 pu). However, it has a larger *response time* as compared to that of the *SVC*. It also exhibits low frequency electromechanical oscillations.
- *SVC+SC* option provides the best overall response with a recovery time of within 200 ms for all disturbances considered.

Chapter 4

Effect of Local Load

4 .1 INTRODUCTION

This chapter investigates the modelling of a local load at the converter station. In the CIGRE benchmark model [13] for instance, the ac system (apart from ac harmonic filters) is represented as a single Thevenin equivalent that includes the local load. Alternatively, the local load can be explicitly represented with the Thevenin equivalent representing the remote ac system only. A local load representation of the later sort has been used for the simulation in Chapter 3 .

In the case of HVdc system, the dynamics of the receiving ac system is different when synchronous compensator (SC) is used instead of fixed capacitors (FC) for reactive power supply. Thus, the effect of local load is studied for two cases having: (i) FC, and ii) SC. The behavior with static var compensator (SVC) can be predicted based on the outcome with the FC.

The results from this chapter reveal that it makes no difference, if modelled properly, whether the local load is represented separately or it is lumped with the ac network. Details of the modelling of the local load, the ac system frequency responses, and the analysis of the simulation results are presented in the following sections.

4 .2 EFFECT OF LOCAL LOAD WITH FIXED CAPACITORS

In this section, the two ways of representing the local load and the resulting system frequency responses are discussed in detail. The two models are different only in the way in which the local load is incorporated in the model. The observations made from the frequency scan of the ac network are verified against simulation results.

4 .2 .1 Representation of Local Load

The two different ways of representing the local load are illustrated in Models A and B below.

4.2.1a Model A: The inverter ac system with fixed capacitors and filters is shown in Figure 5.7 The subject of investigation in this section is the equivalent network inside the dashed box. The R and L values of this network are obtained simply by multiplying the corresponding values in the Cigre benchmark model [13] of SCR=2.5 by the number 1.65 (2.5/1.5) so that the new system SCR is 1.5.

4.2.1b Model B: Network for Model B is shown in Figure 5.8. The filters and the capacitors are identical to the ones in Model A. The equivalent ac network inside the dotted box is split into an R–L impedance (local load) and an ac voltage behind a network so that the Thevenin impedances of the two models are exactly the same at 60 Hz.

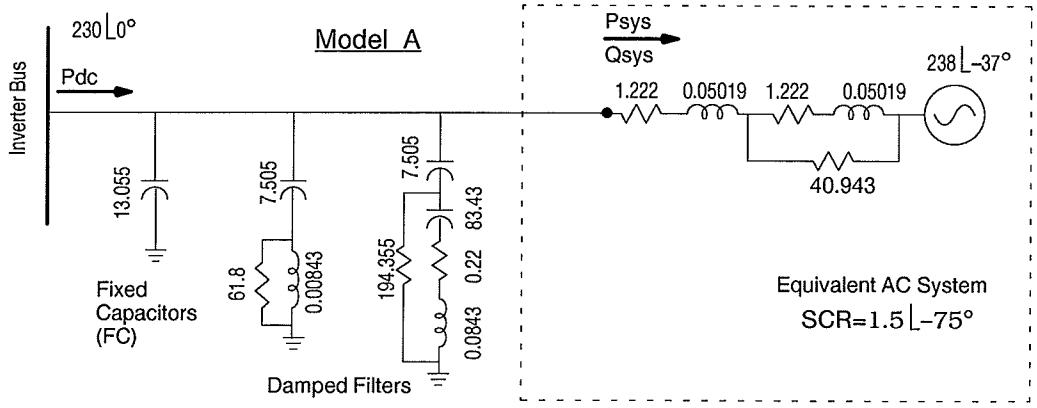


Figure 4.1 : Inverter ac system equivalent with the local load lumped with the network

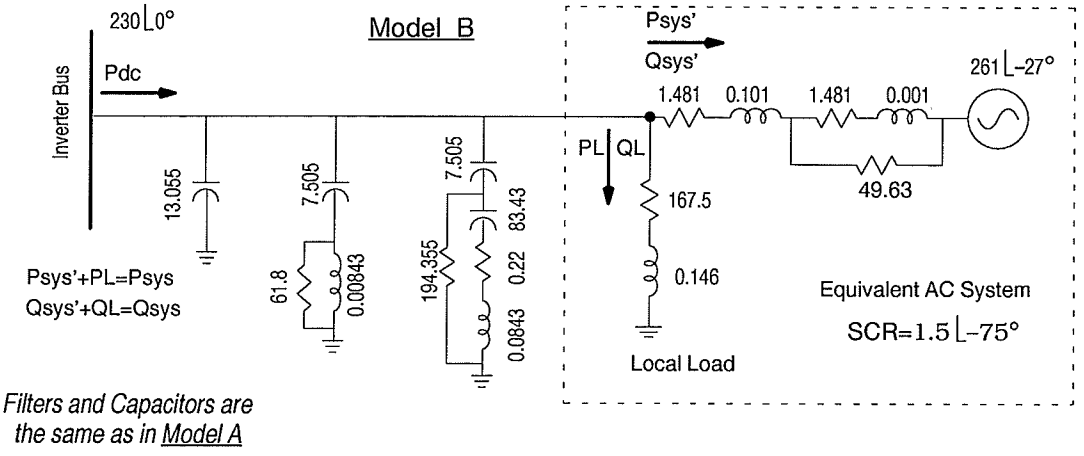


Figure 4.2 : Inverter ac system equivalent where the local load is modelled separately

4 .2 .2 Frequency Responses

The SCRs of both the systems are equal to 1.5 ⌊–75°. The impedance profiles of the equivalent ac networks (inside the dotted box) are shown in Figures 4 .3 (i) and (ii). Their impedance magnitudes are similar up to about third harmonic frequency after which Model B has a slightly higher impedance. Model A has a slightly higher impedance angle for frequencies below the fundamental frequency, and slightly lower angles for frequencies above the fundamental frequency. The impedance profiles of the entire ac network including the filters and fixed capacitors are shown in Figures 4 .4 (i) and (ii). As can be seen from Figures 4 .3 and 4 .4 , the system impedance profile is nearly alike in both magnitude and angle for both models. This indicates that the two equivalent networks modelled as in Figures 4 .1 and 4 .2 should respond very similarly under all dynamic conditions.

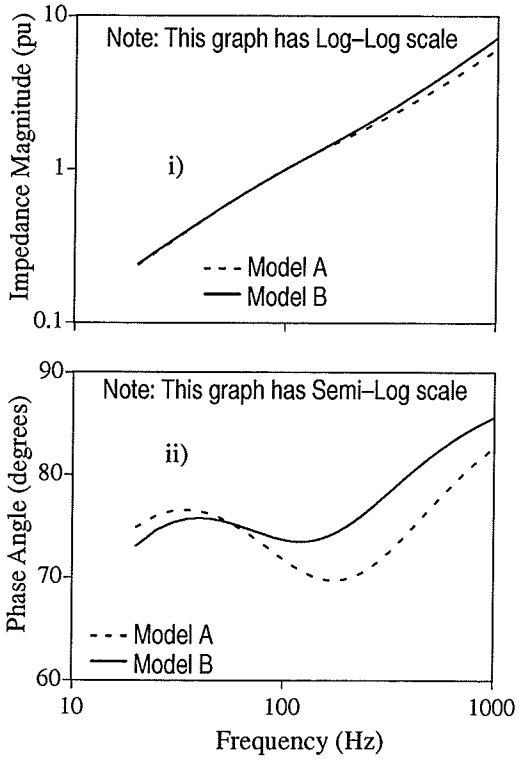


Figure 4 .3 : Frequency Response of the Impedance of the Equivalent Network Enclosed inside the Dotted Box: (i) Magnitude, and (ii) Phase Angle (1 pu Impedance = 52.9 Ω)

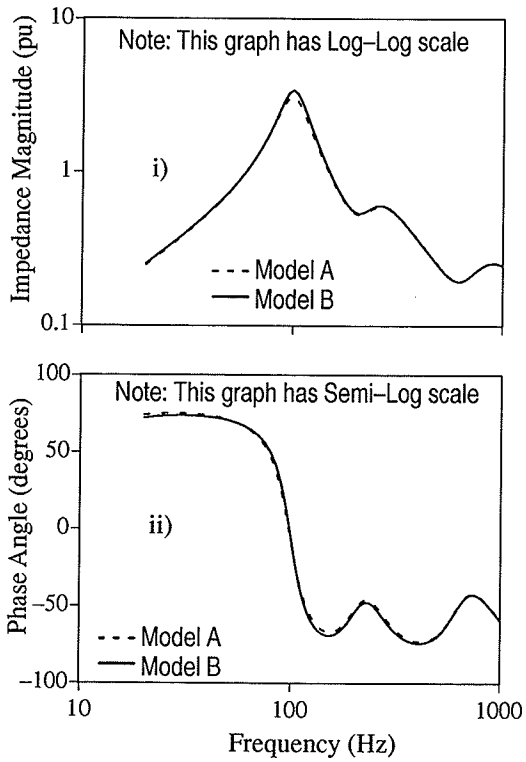


Figure 4 .4 : Frequency Response of the Impedance of the Complete Ac System (Local Load, Filters and Fixed Capacitors Only): (i) Magnitude, and (ii) Phase Angle

4 .2 .3 Simulation Results with FC

The observations made from the frequency scan of the ac system impedances is verified by simulation results for a five cycle single line to ground fault (L–G) at the inverter bus. Figures 4 .5 and 4 .6 show the dc power and ac rms voltages, respectively, at the inverter bus for both the models. After the fault is cleared, the responses for both models are identical upto about three cycles. The responses continue to be similar after this time, except that the response of model A is slightly delayed (phase shifted). The phase shift can be attributed to the nonlinearities introduced by the commutation failure and the differences in the impedance angles as shown in Figure 4 .3 (ii). Simulation results with other disturbances also show similar dynamic responses as discusses above. Therefore it is clear that modelling the local load separately or by grouping it with the ac system equivalent as in Figures 4 .2 and 4 .1 renders identical dynamic behavior of the system as their Thevenin equivalents are the same.

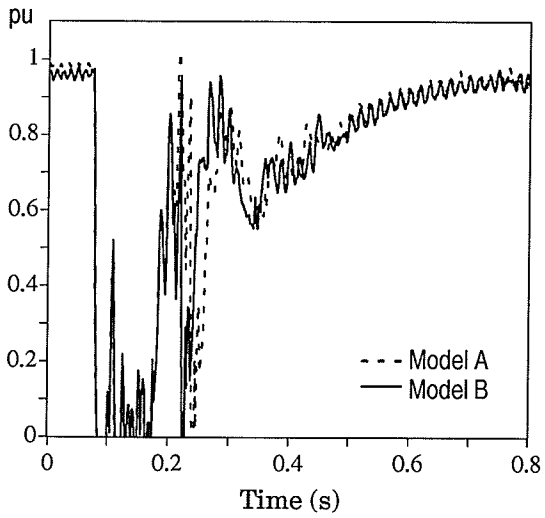


Figure 4 .5 : Dc Power with FC, L–G fault

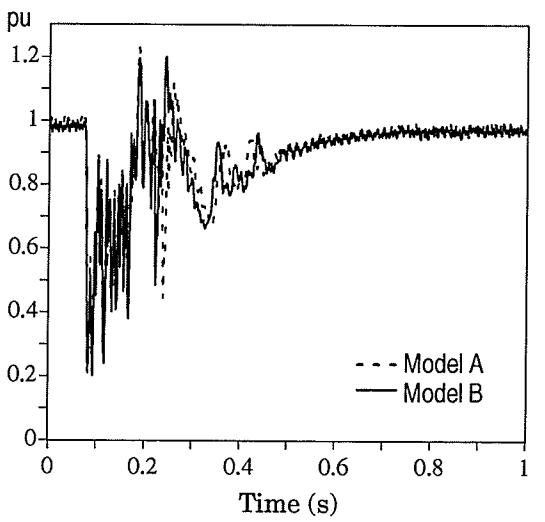


Figure 4 .6 : RMS Ac Voltage with FC, L–G Fault

Since the nature of modelling the local load does not effect the bevaviour of the system with fixed capacitors, it should not make any difference if the FCs were to be replaced by the SVC.

4 .3 EFFECT OF LOCAL LOAD WITH SYNCHRONOUS COMPENSATOR

This section investigates the effect of modelling the local load if the FCs were to be replaced by the synchronous compensators. Simulation results are presented for the modified Models A and B by replacing the fixed capacitors with synchronous compensators. Figures 4 .7 and 4 .8 give the inverter dc power and the rms ac voltage, respectively, for a five cycle single phase to ground

fault at the inverter bus. The real and reactive powers of the synchronous compensator are shown in Figures 4 .9 and 4 .10 , respectively.

An examination of these figures reveals that there is no difference between the transient responses of Models A and B for the disturbance studied. Since the two models are identical from the point of view of Thevenin's equivalent, it is imperative that they be identical in all respect, including their dynamic responses.

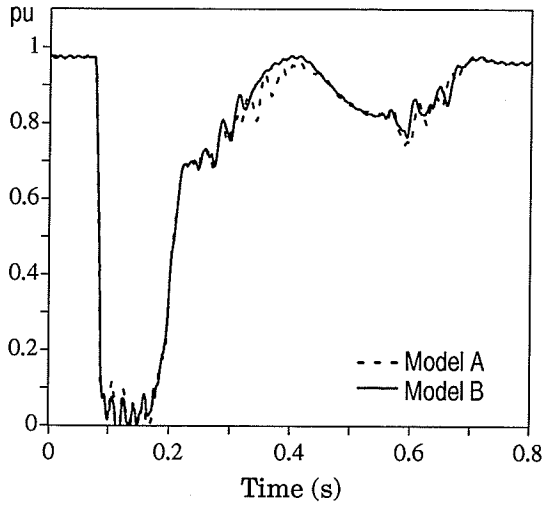


Figure 4 .7 : Dc Power with SC, L–G Fault

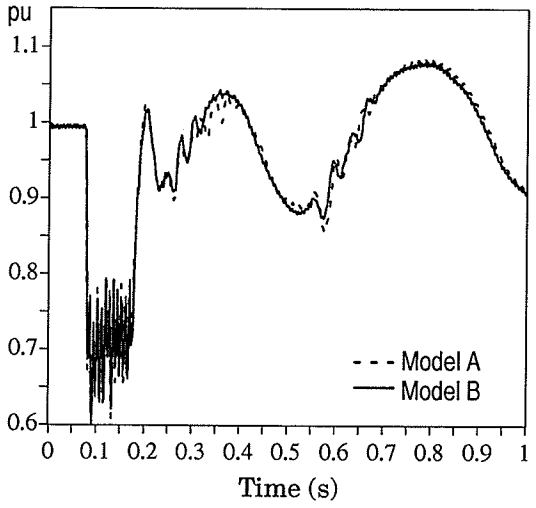


Figure 4 .8 : RMS Ac Voltage with SC, L–G Fault

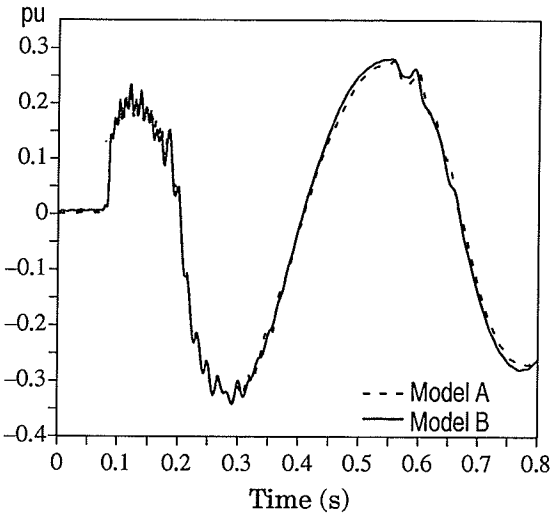


Figure 4 .9 : SC Real Power, L–G Fault

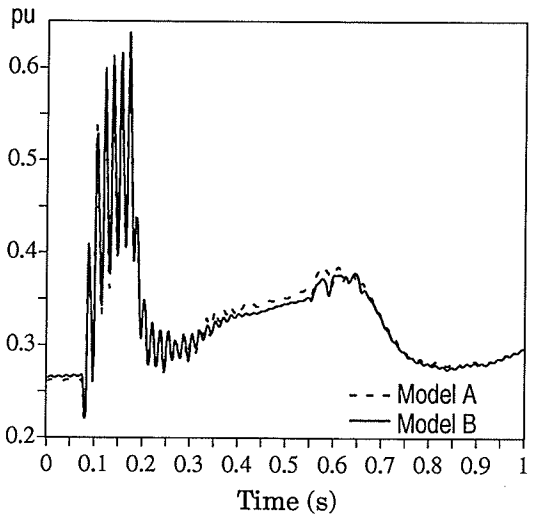


Figure 4 .10 : SC Reactive Power, L–G Fault

4 .4 CONCLUSIONS

The results from this chapter reveal that it makes no difference, if modelled properly, whether the local load is represented separately or it is lumped with the ac network. This has been verified

by frequency scan of the ac system impedance and also by transient simulation results both with fixed capacitors and synchronous compensators. Thus, a single lumped equivalent ac network that includes the effect of local load can be used for the system studies without any loss of accuracy while simplifying the modelling effort. For the ac/dc system considered in the previous chapter (Chapter 3), the difference in the system response by modelling the local load separately or by lumping it into the equivalent network is negligible.

Chapter 5

Steady State Stability Analysis

5 .1 INTRODUCTION

A new concept called the "Control Sensitivity Index" (CSI) is developed in this chapter for the stability analysis of HVdc converters connected to weak ac systems. A brief review of the current literature in the above area precedes the detailed discussion on CSI.

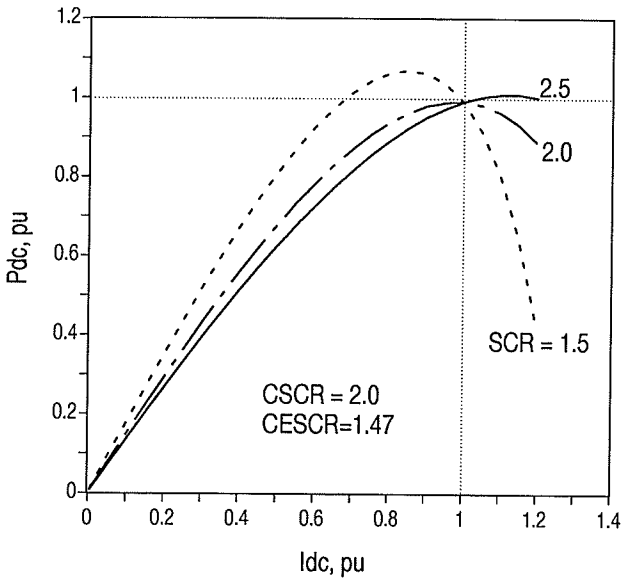


Figure 5 .1 : Maximum Power Curves for Constant Power Control, γ=15°, X_c=0.18 pu

Ainsworth [24] in 1980 introduced the concept of *"Maximum Power Curves (MPC)"* for HVdc systems with the rectifier in constant power control, and the inverter in constant extinction angle (γ) control. Figure 5 .1 shows these curves for a strong rectifier system and a fully compensated weak inverter systems (refer to Figure 5 .4 for system details). The MPC gives useful information about the *Maximum Available Power (MAP)* or *Peak Available Power (PAP)* of the system for a given SCR & ESCR. When the dc current is increased beyond the current corresponding to MAP, the dc power output decreases instead of increasing and thus renders the

constant power control mode unstable for current orders beyond MAP. For a system with SCR=2.0, the MAP is 1 pu which is the normal operating point. For SCR less than 2.0, the normal operating point is beyond MAP and hence, the conventional constant power control is unstable. The critical SCR (CSCR) for this mode of dc control is 2.0 corresponding to a critical ESCR (CESCR) of 1.47.

Hammad et al [25], [26] adopted a purely ac system approach by examining *Voltage Stability Factor (VSF)* at the ac/dc commutating voltage bus. VSF is defined as the incremental change in the ac voltage at the commutating bus due to a small reactive power change at that bus, i.e., dV/dQ. A negative VSF would indicate instability. Like MPC, VSF can be used to determine the CESCR. Figure 5 .2 shows the VSF for a typical ac/dc system with a strong rectifier system and a fully compensated inverter system of varying SCR. The rectifier is in constant current control and the inverter is in constant extinction angle (CEA) control. The critical SCR for this control mode is 0.9 corresponding to a critical ESCR of 0.4 at which the VSF becomes infinity. Systems with ESCR below CESCR are unstable according to the definition of VSF.

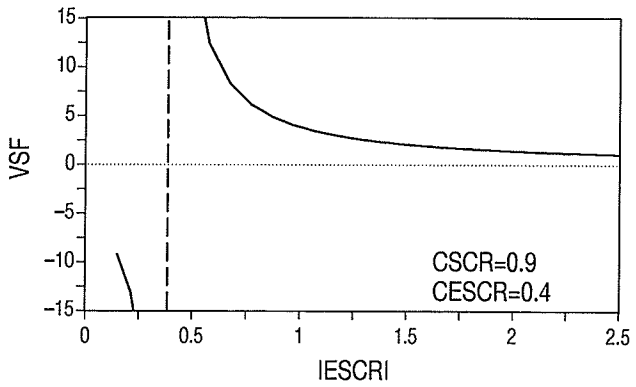
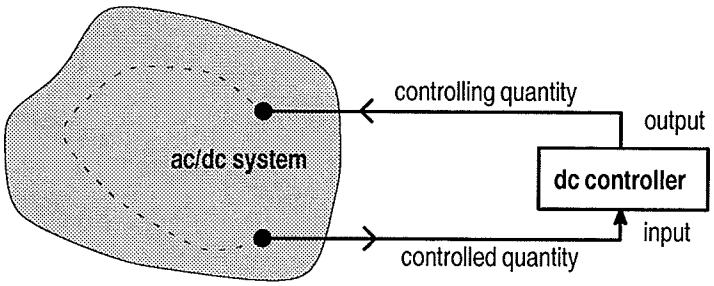


Figure 5 .2 : VSF for Constant γ Control, γ=15°, X_c=0.18 pu

Both MPC and VSF methods are based on the steady state equations assuming fundamental frequency operation and provide valuable insight into the basic mechanisms of instabilities such as voltage collapse associated with HVdc converters connected to low SCR ac systems. They are more realistic than earlier approaches which used concepts such as the short circuit ratio or the effective short circuit ratio. Since their introduction, these concepts (MPC & VSF) have found practical applications and have also become the subject of many publications.

Thio & Davies [8] have successfully used the MPC concept for analysis and dimensioning of synchronous compensators for the Nelson River HVdc system. Frankén and Andersons' [27]

paper on the application of VSF is particularly interesting. They have developed a mathematical model of an ac–dc system using vector and matrix notations and have used this linearized model to analyze a number of stability related properties of the system through the VSF concept. One of the important results obtained through this model is the mathematical proof that MAP and VSF are completely equivalent in the constant power control mode (i.e., VSF is infinity at MAP). Other results obtained using the model include the derivation of VSF for gamma control mode, stability of converter transformer tap changer and dynamic stability of SVC. Piloto et al [28] demonstrate the application of the VSF method to a converter connected to a weak ac system and verify their results with an EMTP simulation. Part I of the *Guide for Planning Dc Links Terminating at Low SCR Ac Systems* [29], produced by the CIGRE/IEEE joint task force, extensively covers the current developments in this area with a comprehensive bibliography.



$$CSI = \frac{controlled\ quantity}{controlling\ quantity}$$

Figure 5 .3 : The definition of CSI

The "Control Sensitivity Index" (CSI) approach developed here is based on relating the sensitivity of the power system response to the output of the controller under consideration. *It is defined for a particular control mode as the rate of change of the controlled quantity with respect to the controlling quantity*. Figure 5 .3 illustrates this definition. The input to the controller (which is a system quantity) is controlled by the output of the controller through the ac/dc system. CSI focuses directly on the controller input/output characteristics and indicates how the controller affects the stability of the system. It is in this way that the CSI differs from VSF which uses a uniform criterion (i.e. dV/dQ at ac bus) for the analysis of voltage stability although both approaches yield the same results for quantities such as the critical effective short circuit ratio (CESCR) – the ESCR at which the instability sets in. However it is shown here that for a certain controller type (eg. constant γ controller) the straight forward application of the VSF method only indicates the instability whereas the proposed CSI approach not only identifies the instability but also provides the solution to make the system stable through control modification. For example, in constant extinction angle control, a positive CSI indicates onset of instability.

It also plays an important role in defining non–linear gains for the dc controller. Like MAP and VSF, CSI is calculated based on the steady–state fundamental frequency equations, and hence, does not consider instabilities resulting from controller or system dynamics.

In the sections to follow, the theoretical evaluation of CSIs for various control modes are verified against a detailed electromagnetic transient simulation of a system based on the First CIGRE Benchmark [13] for HVdc systems.

5 .2 THE APPROACH

The method used in these investigations is explained with the aid of the inverter system shown in Figure 5 .4 which shows an HVdc inverter connected into an ac system with equivalent impedance Z_s (refer to Appendix V for a detailed system diagram). The ac filters and fixed capacitors are shown as an impedance Z_f which supply about 0.56 pu reactive power at 1.0 pu voltage. The converter transformer commutation reactance X_c is 0.18 pu. The extinction angle γ is 15° unless specified otherwise. In steady state operation the voltage E_s is adjusted to give the terminal voltage V_t a magnitude of 1.0 pu. The CSIs in the following sections are plotted against ESCR magnitude. This variable ESCR is achieved by varying only the SCR magnitude (SCR=$1/Z_{s\ pu}$). The SCR angle (i.e., angle of Z_s) and the compensation Z_f are kept constant.

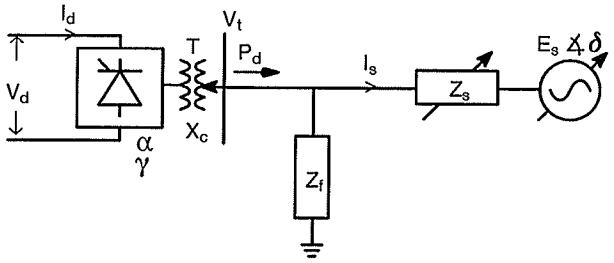


Figure 5 .4 : Inverter Connected to Ac System

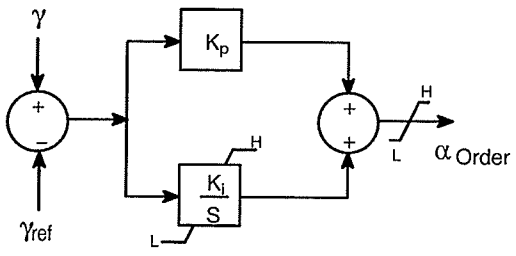


Figure 5 .5 : A Conventional Extinction Angle Controller

The constant extinction angle (CEA) mode of operation is examined here. Figure 5 .5 shows a block diagram for a conventional extinction angle controller. The gains K_p and K_i are normally positive which means that if the measured extinction angle γ is larger than the order γ_{ref}, then the error causes the firing angle order α to increase. This strategy assumes that the increase in α will cause γ to decrease, i.e. that the quantity $d\gamma/d\alpha$ is negative. However if for a given converter loading or ESCR the quantity $d\gamma/d\alpha$ becomes positive, the controller will change α in the wrong direction from that required to bring the value of γ back to γ_{ref}. The operating point therefore becomes unstable. The index $d\gamma/d\alpha$ could therefore be designated as the control sensitivity index (CSI) for the extinction angle controller. A positive value of CSI would indicate instability. Also the magnitude of CSI is a measure of how sensitive the response of the system is to an α order change. A high magnitude indicates that very small changes in α result in large changes of γ and thus aids in the selection of controller gains. In fact, in a situation where $d\gamma/d\alpha$ is negative, stable operation is possible if the sign of the controller is reversed. This may be achieved at the input summing junction by reversing the signs of γ and γ_{ref} inputs. The same effect is also achieved by introducing negative values for K_p and K_i.

If it is assumed that the rectifier controls and the line smoothing reactors maintain an essentially constant dc current, the following equations [30] can be used to evaluate $d\gamma/d\alpha$:

$$V_t = \frac{\left(\sqrt{2}\ X_c\ I_d\right)}{T\ (\ \cos\alpha + \cos\gamma\ )} \qquad (5.1)$$

$$\phi\ = \cos^{-1}\left[\frac{\cos\alpha\ -\ \cos\gamma}{2}\right] \qquad (5.2)$$

$$V_d\ = \frac{3\sqrt{2}}{\pi}\ T\ V_t\ \cos\gamma\ -\ \frac{3}{\pi}\ X_c\ I_d \qquad (5.3)$$

$$P_d\ = V_d\ I_d \qquad (5.5)$$

$$I_s\ = \frac{P_d}{\sqrt{3}\ V_t\ \cos\phi}\ e^{j\phi}\ -\ \frac{V_t}{\sqrt{3}\ Z_f} \qquad (5.4)$$

$$E_s \angle\delta\ = V_t - \sqrt{3}\ Z_s\ I_s \qquad (5.6)$$

where the variables are as defined below:

V_t : Line to line voltage on the ac busbar

X_c : Commutation impedance

I_d : Dc current

T : Transformer turns ratio

α : Firing angle of inverter

γ : Extinction angle

ϕ : Power factor angle of converter ac current

V_d : Dc voltage

P_d : Dc power

I_s : Ac current entering the system, i.e, filter current + converter current

Z_f : Impedance of ac filters

E_s : Source voltage of system equivalent

δ : Phase angle between E_s and V_t

Z_s : Impedance of system equivalent

The control sensitivity index $d\gamma/d\alpha$ can be computed by linearizing the equations (5 .1) through (5 .6) and solving for a small change $\Delta\gamma$ in the extinction angle in response to a small change $\Delta\alpha$ in the firing angle and then calculating the ratio $\Delta\gamma/\Delta\alpha$. During this calculation, the quantities I_d and $|E_s|$ are held constant and an ideal current controller at the rectifier end is assumed. Only one control mode is investigated at a time.

Note that the above calculations for CSI only involve network equations and do not include controller gains. However, the CSI relates the change in the controlled quantity of the network (i.e., γ) to the controller's output (α). A controller is designed considering a certain system characteristics, (i.e., γ decreases with increasing α). If this characteristic changes sign, it implies the onset of instability as the controller will now attempt to vary its output in a direction opposite to that required to restore the controlled quantity to its reference value. Thus, the controller parameters are not necessary in determining this steady state stability limit.

A word of caution – in a more rigorous formulation, the system and controller dynamics must be included in the determination of stability. However, the above simplistic approach based on only steady state equations gives excellent results in most cases.

A typical program listing for CSI calculations to solve equations (5 .1) through (5 .6) using *Mathcad* [31] software is available in Appendix V. *Mathcad* is just one of the many tools available to perform these calculations.

5 .3 CONTROL SENSITIVITY INDICES

Control Sensitivity Indices are presented here for the case of constant extinction angle, constant power and constant voltage control modes.

5 .3 .1 Constant Extinction Angle Control

As described in the earlier section, a typical extinction angle controller attempts to regulate γ through controlling the firing angle α. The CSI $d\gamma/d\alpha$ is therefore the index of interest. Figure 5 .6 shows $d\gamma/d\alpha$ as a function of the ESCR of the ac system. It is assumed that the rectifier is operating in constant current control mode and therefore the dc current I_d is assumed fixed (at a value of 1.0 pu for the plots in Figure 5 .6). The graphs in Figure 5 .6 have been plotted for different damping angles of the system equivalent impedance Z_s. For an angle of 75°, the critical ESCR is about 0.4 (SCR=0.9). For a smaller damping angle of 65°, CESCR is larger (about 0.6) whereas if the equivalent is purely inductive (90°), the system is stable at any ESCR. This appears counter–intuitive because it indicates that a system with very low damping can be stable at extremely low ESCR values. However, evaluating the critical ESCR by a full scale EMTDC simulation verifies this result.

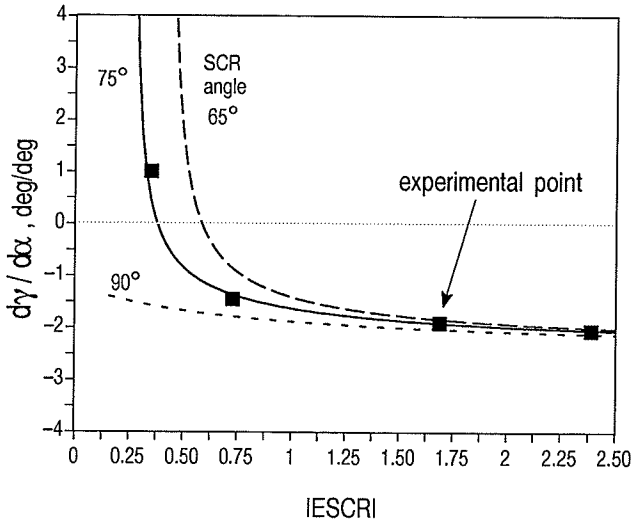


Figure 5 .6 : Calculated and Simulated CSI $d\gamma/d\alpha$ v/s ESCR for I_d = 1.0 pu

The theoretically obtained CSI values are verified with those obtained "experimentally" from simulation. The squares in Figure 5 .6 show the CSI values obtained from the simulation for an SCR angle of 75°. As is obvious from the figure, the agreement is very good. In the simulation the inverter was operated at a constant firing angle corresponding to the steady state solution.

A small step change $\Delta\alpha$ was made and the corresponding extinction angle change $\Delta\gamma$ was measured from which the index was calculated.

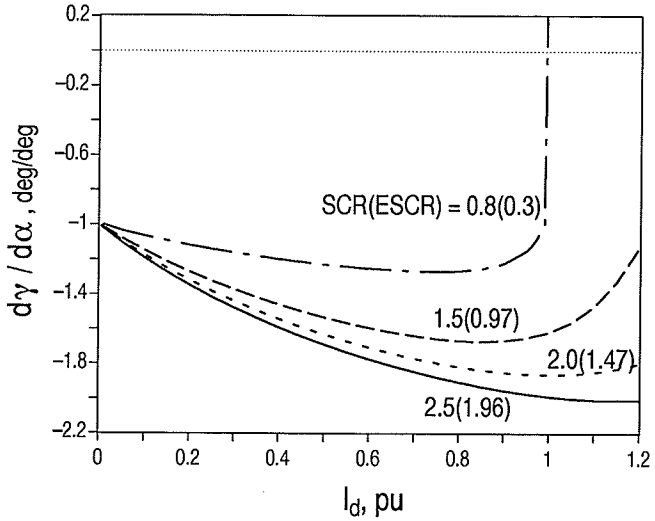


Figure 5 .7 : CSI $d\gamma/d\alpha$ v/s I_d for Various Fixed ESCR

Figure 5 .7 shows how the CSI varies with the amount of dc current for a fixed ESCR (impedance angle assumed fixed at 75°). For an ESCR of 0.3 (SCR 0.8), the dc current cannot exceed 1.0 p.u., without loss of stability. For stronger systems, this current can be larger than the rated current.

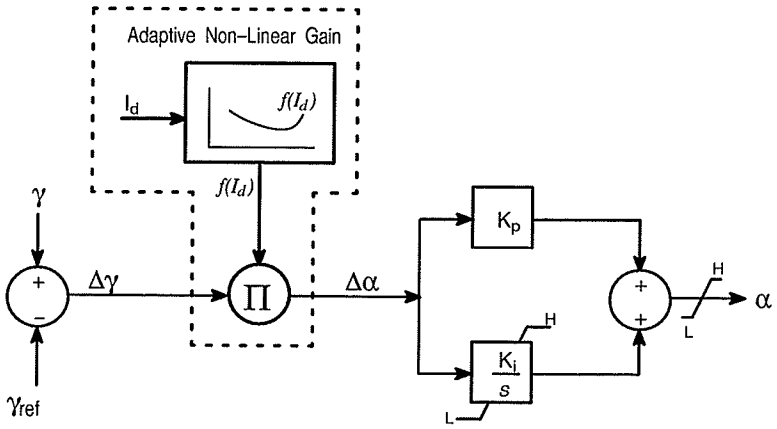


Figure 5 .8 : Adaptive Extinction Angle Controller

One other application of the information shown in Figure 5 .7 could be to design an adaptive non–linear gain block for the extinction angle controller. For a given short circuit ratio, the gain could be adjusted according to the reciprocal of the $d\gamma/d\alpha$ index as the current varies. Figure 5 .8 shows the block diagram for such a controller. This ensures uniform sensitivity of the γ response over the entire operating range. It should be noted that the use of a different

characteristic for each SCR may be impractical due to the difficulty of determining the SCR at an HVdc converter station. However, Figure 5 .7 shows that for SCR greater than 2.0 (ESCR > 1.47), the characteristics come closer together and one can use an average characteristic in the controller.

The results of Figure 5 .6 indicate an interesting possibility. If one were to reverse the sign of the controller (input summing junction or the gains) a controller would result that would maintain γ constant when $d\gamma/d\alpha$ was positive i.e., the controller would only be stable for low ESCRs and unstable for ESCR values larger than the critical ESCR. Figure 5 .9 shows transient simulation plots of γ, α and the ac voltage for such a situation (The ESCR is 0.3 which is below the critical value of 0.4 for an SCR angle of 75°). Initially the firing angle is held at a constant value corresponding to the steady state operating point solution and then at t=0 the gamma controller is switched in with the controller sign reversed (negative). With the sign reversed, the controller takes over and maintains γ at the reference value. Later at t=0.15 s the controller reverts to its conventional configuration by making the controller sign positive. With the conventional controller, the extinction angle rapidly moves away from the reference value of 15° and ultimately results in commutation failures indicating the instability of the γ control mode. At t=0.45 s, the controller sign is changed back to negative and the system recovers from commutation failure.

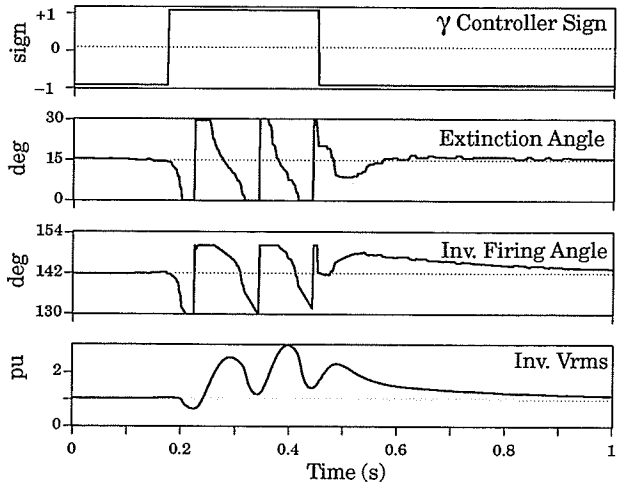


Figure 5 .9 : Converter Responses with Conventional γ Controller and with its Sign Reversed

Although the critical ESCR can be calculated using the VSF approach, a straight forward calculation of VSF indicates that γ control is never possible below CESCR. For example the VSF calculation for constant γ control in [25] uses the constraint $\Delta\cos(\gamma)= 0$ without any regard to the sign of the controller and hence does not yield different results for the two cases (positive and negative sign). By focusing directly on the controller input/output behavior as in the case of CSI calculation, the reason for this stable operation below the CESCR value becomes directly apparent.

5 .3 .2 Constant Power Control

When the rectifier is in constant power control operation, the power controller normally adjusts the current order so that the ordered power is achieved. Thus the index dP_d/dI_d could be used as the CSI. This criterion is the same as the MAP criterion by Ainsworth [24] and later shown to be exactly equivalent to the VSF at the critical point by Frankén et al [27]. The inverter is assumed to be in constant extinction angle (CEA) control. Shown in Figure 5 .10 is the CSI (dP_d/dI_d) for the test system with a very strong rectifier ac system and an inverter side system of varying short circuit ratio. As can be seen, the critical ESCR value is in the neighborhood of 1.47 (SCR 2.0). Figure 5 .10 also shows the variation of the CSI with different equivalent system damping angles. The damping angle does not appear to play as important a role in this case as in the case of the extinction angle controller since the critical ESCR is virtually independent of the damping angle.

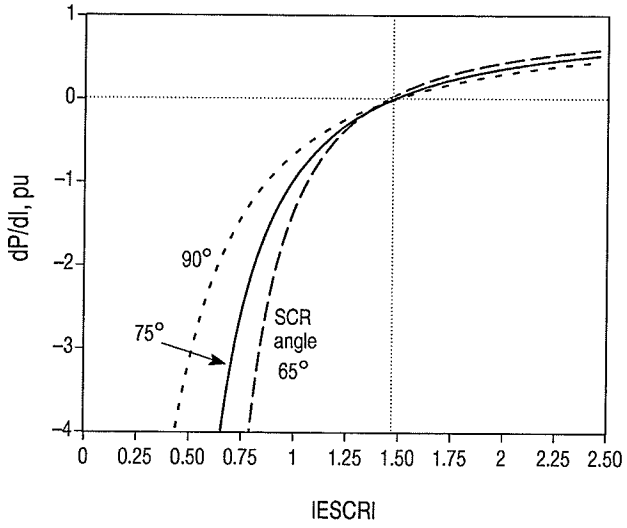


Figure 5 .10 : dP_d/dI_d for Constant Power Control

5 .3 .3 Constant Voltage Control

The CSI for voltage control at the inverter is discussed here. The rectifier is assumed to be operating at a constant current. The inverter dc voltage is maintained constant through control of the firing angle. The relevant CSI is thus $dV_d/d\alpha$. Figure 5 .11 shows $dV_d/d\alpha$ as a function of ESCR and the critical ESCR appears to be 0.25 (SCR 0.74).

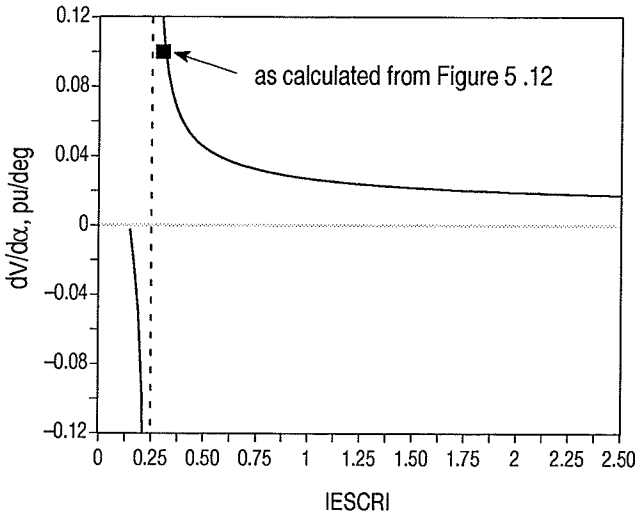


Figure 5 .11 : CSI for Constant Voltage Control

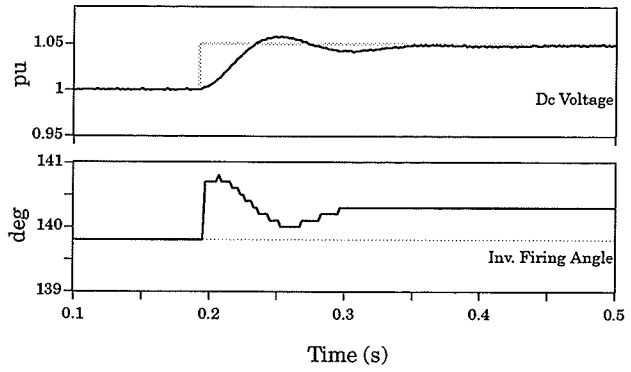


Figure 5 .12 : Step Change in V_{ref} for Inverter in Constant Voltage Control

Figure 5 .12 shows digital simulation results for a 5% increase in dc voltage order for an inverter connected to a system of ESCR 0.3 (SCR 0.8). As can be seen, the change in the firing angle is 0.5 degrees which gives a value for $dV_d/d\alpha$ of 0.1 pu/deg, which agrees with the theoretical calculation in Figure 5 .11 . The critical ESCR is also confirmed through simulation. The CSI ($dV_d/d\alpha$) value from Figure 5 .11 indicates that a voltage controller should have smaller gains

if the system ESCR is in the vicinity of critical value as the system is extremely sensitive to firing angle changes.

5 .3 .4 Comparison of the Three Modes of Control

Figure 5 .13 shows a graph of CSI for the three control modes discussed above. It is clear that the critical ESCR is the smallest (0.25) for the inverter in voltage control with the rectifier at constant I_d, indicating this to be a superior control mode (amongst the three control modes) for inverters connected to very weak ac systems. The critical ESCR (1.47) is the highest when the rectifier is in the power control mode. For the inverter in constant extinction angle control with the rectifier in constant current operation, the critical ESCR (0.4) is slightly larger than that in the constant voltage control mode. Table 5 .1 summarizes the critical short circuit ratios for all three control modes as obtained from CSIs for ac systems with SCR angle of 75°.

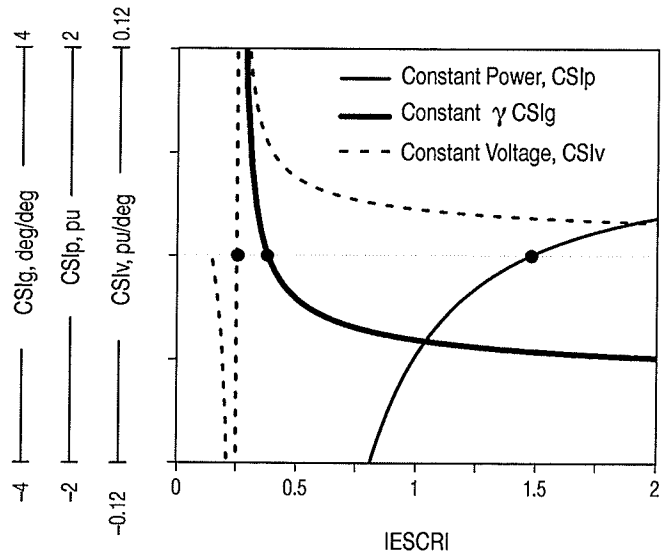


Figure 5 .13 : CSI for Three Control Modes

Control Mode	CSI	CSCR	CESCR
Constant Voltage	$dV_d/d\alpha$	0.74	0.25
Constant Extinction Angle	$d\gamma/d\alpha$	0.90	0.40
Constant Power	dP_d/dI_d	2.00	1.47

Table 5 .1 : Summary of Control Sensitivity Indices

5 .4 LIMITATIONS OF THE CSI METHOD

As described earlier, the CSI method like the VSF method relies on steady state equations and assumes fundamental frequency voltages on the ac side. No dynamics are considered. For a complete stability analysis one has to analyze the eigenvalues of the linearized differential equations of the system. Presented here is a calculation of CSI for the inverter in constant current control. In this case the CSI yields an incorrect CESCR. The rectifier ac system is assumed to be strong with the rectifier operating at a constant firing angle (i.e., stuck on its minimum α limit). The inverter current controller regulates the current I_d through the inverter firing angle α. The angle α is increased if the current is to be reduced and so one expects the system to be stable if $dI_d/d\alpha$ is negative. Figure 5 .14 shows this index as a function of ac system strength and it appears that the system is unstable at an ESCR of 2.9 (SCR 3.4). However, by means of digital simulation, one can verify that stable operation below this limit is possible.

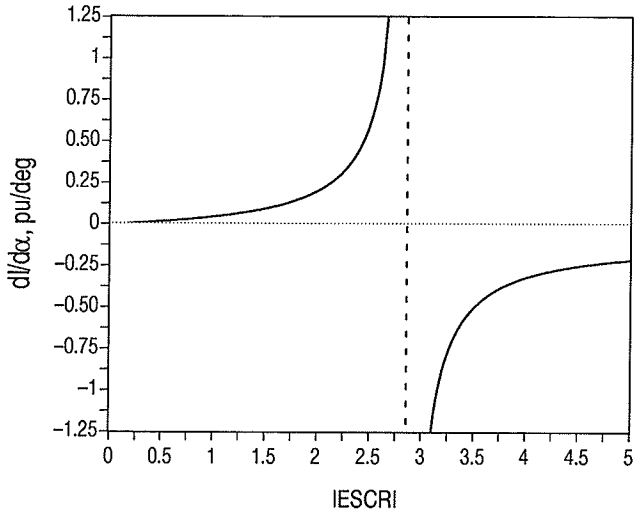


Figure 5 .14 :CSI for Constant Current Control on the Inverter

Figure 5 .15 shows simulated firing angle and dc current waveforms for an inverter in current control for two systems of different SCR. The dc current order is stepped up by 5% at t=0.2 s by an order change. For the system with SCR 5.0 (ESCR 4.46), the firing angle is decreased as expected indicating a negative $dI_d/d\alpha$. This is compared with the response of the system with SCR 2.5 (ESCR 1.96), which is on the unstable side of the stability regime from Figure 5 .14 . The inverter with SCR 2.5 operates quite stably in this region contrary to what one expects from the CSI. However, the controller appears to increase the firing angle order (in the steady state) after the order change indicating a positive $dI_d/d\alpha$. The steady state response of the controllers

in the two cases are in opposite directions for the same current change and conform to the calculated CSI values, and yet both systems are stable.

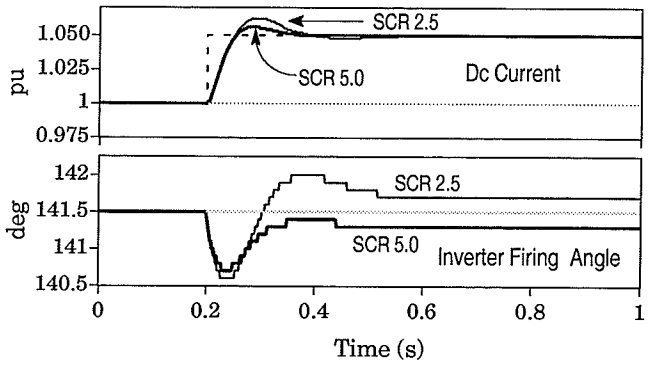


Figure 5 .15 : Step Change in I_d for Constant Current Control

From Figure 5 .15 one sees that the instantaneous response of the controller in both cases is in the same direction. Initially the firing angle (α) order decreases due to an increase in current order. The dc current initially increases in both cases in response to this decreasing firing angle although $dI_d/d\alpha$ is positive in one case and negative in the other. The steady state changes, however, are in the opposite direction for the two cases as expected from the different signs of $dI_d/d\alpha$. This simulation shows that even for systems with SCR less than 3.4 (ESCR < 2.9), the short term dynamics has the negative characteristics although $dI_d/d\alpha$ is positive considering steady state equations. Thus the system is dynamically stable even though the steady state equations indicate otherwise. A more rigorous approach using eigenvalue analysis is therefore recommended.

5 .5 CONCLUSIONS

The Control Sensitivity Index is a new approach for analysis of dc converters in weak systems. Following remarks can be made based on the CSI analysis of three modes of dc controls.

- For constant extinction angle control (CEA) mode, the critical short circuit ratio varies with the damping angle of the system impedance. The magnitude of the critical short circuit ratio increases with a decreasing damping angle.
- Contrary to CEA mode of control, the damping angle does not appear to play an important role in determining the critical short circuit ratio for the constant power control mode.

- The inverter voltage control with rectifier constant current control is the most stable control option for weak systems amongst the three modes investigated.
- The CSI provides more insight into the operation of the controller than other methods of analysis. It has been demonstrated (Section 5 .3 .1) that such information can be used to improve the stability of the system and also in the design of adaptive dc controllers.

Chapter 6

CONCLUSIONS

6.1 CONCLUSIONS

6.1.1 Compensator Performance

The CIGRE Benchmark Model has been successfully modified to include dynamic compensators and a very low SCR receiving ac system. Based on simulations carried out using this model, the following conclusions can be drawn:

- The static var compensator *(SVC)* has the fastest response in controlling a dynamic overvoltage such as that which result from a load rejection (dc block). However, the capacitance of the thyristor switched capacitor (TSC) banks has an effect of lowering the effective short circuit ratio. This leaves the system susceptible to instability resulting from repeated commutation failures when control action changes the firing angle of the SVC's thyristor controlled reactor (TCR). In order to prevent the instability, the firing angle of the inverter is reduced and then slowly ramped back. This results in a considerable increase in recovery time for the *SVC* option.

- The synchronous compensator option limits the first overvoltage peak to the lowest value (1.3 pu) of all the options. It also has fast recovery from all the faults considered. However, it shows the slowest response when controlling temporary overvoltages. It also exhibits a low frequency oscillation due to the dynamics of the rotor.

- The static var compensator–synchronous compensator *(SVC+SC)* mix provides the best overall performance. It has the same response time for controlling dynamic overvoltage resulting from a load rejection (dc block) as the synchronous compensator *(SC)* option, but does not suffer from the poor recovery from faults that the *SVC* option exhibits. The dc recovery time for this option is within 200 ms for all the disturbances considered.

6 .1 .2 Effect of Local Loads

The effect of (modelling) local loads on the system dynamics has also been investigated. The results show that, modelling the local load separately and as part of the system equivalent are very similar.

6 .1 .3 Stability Analysis

- The *Controller Sensitivity Index* is a new approach for analysis of dc converters in weak systems. The index provides valuable information about the stability of the system. It is also very useful in defining variable gains for the controllers and can be used to design adaptive dc controllers.
- The control sensitivity indices for three dc control modes have been presented. The CSI results for constant power control mode have been verified against the Maximum Power Curve (MPC) results. The CSI for constant extinction angle control has been verified against the Voltage Stability Factor (VSF). The theoretical conclusions drawn from CSIs for different control modes have been verified against a detailed transient simulation of a dc system based on the CIGRE Benchmark.
- The CSI method is however based on steady state network equations at fundamental ac frequency and ignores system dynamics. It is not as detailed as eigenvalue analysis or time domain simulation.

6 .2 FURTHER WORK

The control strategies adopted in this thesis for the *SVC* option is one of the many possible strategies. It has been used because it satisfactorily works for a system with very low SCR ac system. However, it is not necessarily the best possible strategy for the *SVC* in a dc system connected to very weak ac system. Investigating the various possible strategies and evaluating their merits is a complete study by itself and there is a need for such a study as there is increasing interest in installing weak HVdc systems. The following are some of the suggestions for SVC controls operating into weak HVdc systems.

- SVC as Fixed Capacitor: Treating the SVC as a fixed capacitor with the nominal susceptance during the fault and recovery will guarantee a performance similar to that of the fixed capacitors case. However, that would mean not utilizing the dynamic nature of the SVC; the very reason the SVC is preferred over FC.

- Adaptive Controls: SVC controller gains can be changed during the fault condition so as to increase the stability and enhance the recovery process. Different sets of gains can be used for different types of faults to get the best recovery after identifying the type of fault through some means. The control sensitivity indices (CSI) of Chapter 5 may be helpful in designing such an adaptive controller.

- Coordination: Coordination of the dc controls with the SVC controls could be explored to improve the performance during recovery from disturbances. One such modifications was employed in this thesis by using a commutation failure protection circuit (CFPC) to prevent repeated commutation failures during close–in ac faults at the inverter side. Alternate strategies are worth exploring.

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Appendix

APPENDIX I : SCR AND ESCR

SCR is defined as the ratio of the short circuit MVA at the ac busbar, to the dc power taken from the same busbar [15].

$$\text{SCR} = \frac{\text{Short Circuit MVA}}{\text{HVDC Power}} \qquad \text{(A.1)}$$

This ratio can be established to give different values depending upon whether or not the local loads, compensators, and filters have been included while calculating the short circuit MVA.

The SCR can also be defined as the ac system Thevenin admittance expressed in per unit of dc power [16]. The effect of dc power rating on ac voltage regulation is expressed in a more relevant manner by a measure of system equivalent impedance rather than equation (A.1), although both give the same numerical value as explained below.

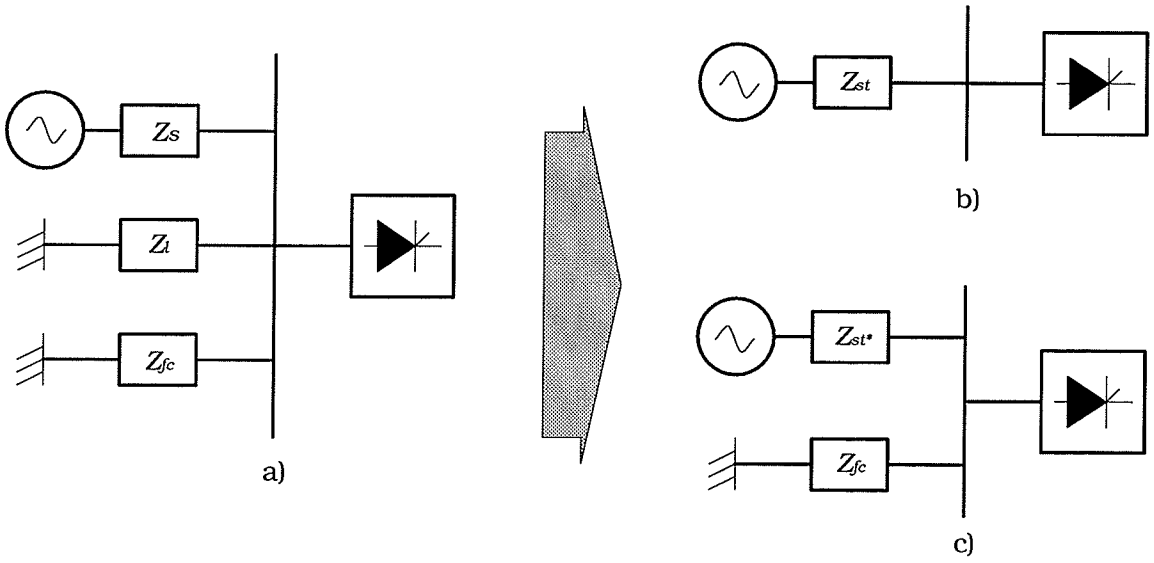


Figure A.1 : Equivalent Circuits for SCR and ESCR Calculations

Referring to Figure A.1.a and A.1.b, let Z_{st} be the Thevenin source impedance which equals source impedance Z_s, filters and compensator impedance Z_{fc}, and local load impedance Z_l in parallel expressed on the base impedance X_{ac}. If the HVDC power P_{dc} and the nominal ac voltage V are used as the base quantities, then X_{ac} is given by:

$$X_{ac} = \frac{3V^2}{P_{dc}}$$

$$\frac{1}{Z_{st}} = \frac{1}{Z_s} + \frac{1}{Z_{fc}} + \frac{1}{Z_l}$$

The pu Thevenin source impedance z_{st} [16] is given by

$$z_{st} = \frac{Z_{st}}{X_{ac}} = \frac{Z_{st}}{V^2} P_{dc} = \frac{P_{dc}}{MVA^*} = \frac{1}{SCR^*}$$

The MVA^* is the short circuit MVA with the dc blocked and the ac busbar voltage readjusted to the rated value V. SCR^* is called effective short circuit ratio (ESCR) if Z_{fc} is included in the calculation of Z_{st} as in Figure A.1.b, and simply SCR if Z_{fc} not included as in Figure A.1.c. Local load Z_l is included in Z_{st} in the calculation of both ESCR and SCR.

APPENDIX II : COMPENSATOR DATA

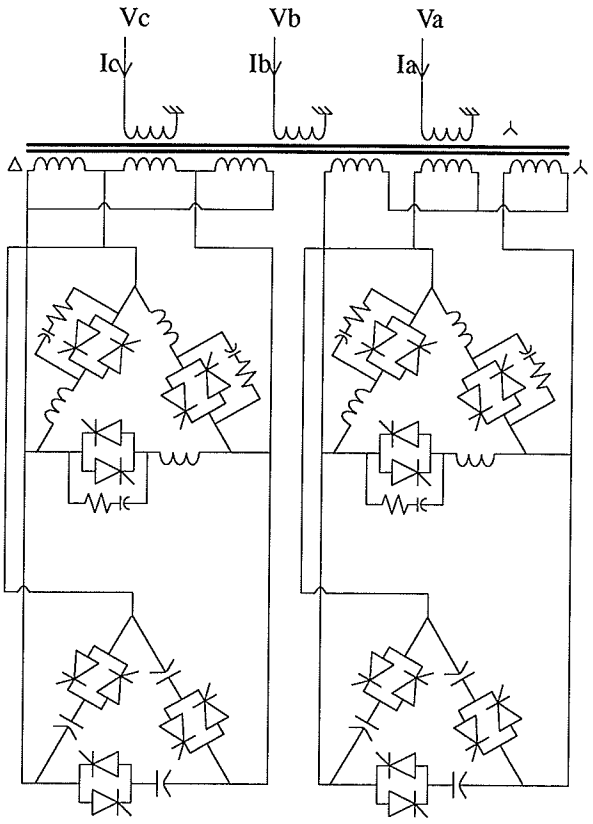
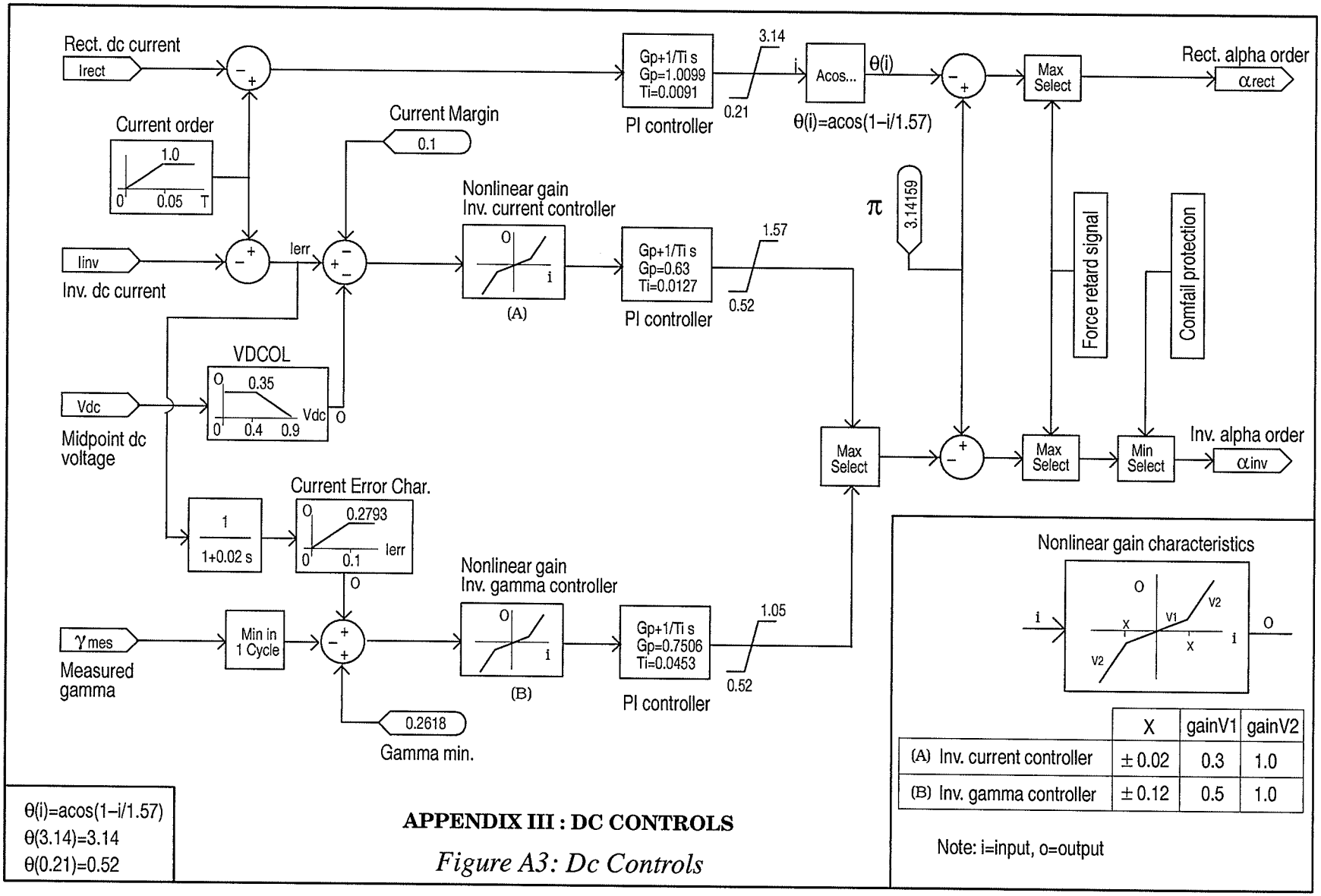


Figure A 2: SVC Main Circuit

Parameters	Values	Units
Duration of Time Step	25	μ *sec*
PLL Integral Gain	900	
PLL Proportional Gain	100	
3 Phase MVA Transformer MVA	150	MVA
Positive Seq. Leakage (Prim–Star)	0.17	pu
Positive Seq. Leakage (Prim–Delta)	0.17	pu
Positive Seq. Leakage (Star–Delta)	0.021	pu
Rated Primary Voltage, L–L	230.0	KV
Rated Secondary Voltage, L–L	12.0	KV

Primary Magnetizing Current	0.4	pu
Delta Magnetizing Current	0.4	pu
Delta Magnetizing Current	0.4	pu
Air Core Reactance	0.4	pu
Inrush Delay Time Constant	0.18	sec
Knee Voltage	1.7	pu
Loss Shunt Conductance	0.00001	Ω^{-1}
Total MVA of TCR	90.0	MVar
Thyristor Snubber Resistance	1000.0	Ω
Thyristor Snubber Capacitance	0.3	μF
Thyristor ON Resistance	0.005	Ω
Thyristor OFF Resistance	10000.0	Ω
Total MVA of TSC	150.0	MVar
Parallel Resistance Across Each Cap. Stage	500.0	Ω
Number of Capacitor Stages	2	
Scaling Factor	2	

Table A 1 .1 : SVC Main Circuit Data



	X	gainV1	gainV2
(A) Inv. current controller	± 0.02	0.3	1.0
(B) Inv. gamma controller	± 0.12	0.5	1.0

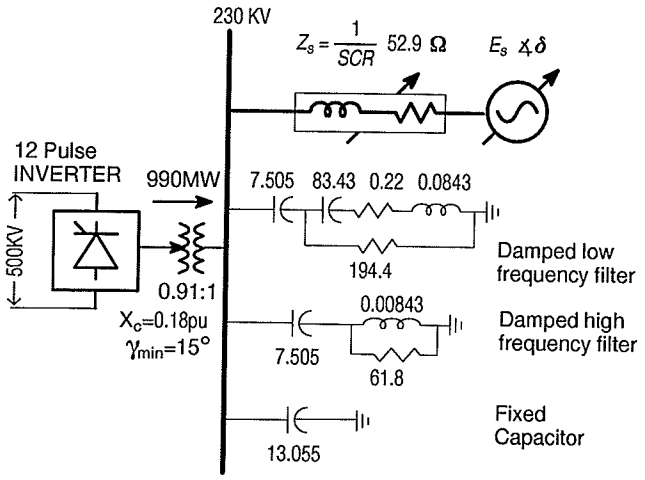
Note: i=input, o=output

APPENDIX III : DC CONTROLS

Figure A3: Dc Controls

APPENDIX IV: SYSTEM DATA FOR CSI SIMULATION

All simulations are carried out with the 1000 MW, 12 pulse, 500 KV dc system as shown in Figure A.4. The ac system impedance and the source voltage are adjusted for different SCR so that rated voltage is maintained at the inverter bus in the steady state. Converter controls and other data are as given in the First CIGRE Benchmark [13].



All Resistances in Ω, Inductances in H, Capacitances in μF

Figure A.4 : Inverter System

APPENDIX V: A Typical Mathcad File for CSI Calculation

This file calculates $d\gamma/d\alpha$ for different SCR magnitudes

Units:

$deg := \frac{\pi}{180}$ $rad := \frac{180}{\pi}$ $MVA := 1$ $KA := 1$ $KV := 1$ $MW := 1$ $\Omega := 1$

System Base Quantities:

$MVAbase := 1000 \cdot MW$ $KVbase := 230 \cdot KV$

$Zbase := \frac{KVbase^2}{MVAbase}$ $Zbase = 52.9$

Given System Parameters:

$$Zf := \frac{1}{\left[\frac{1}{0.096 - (j \cdot 175.924)} + \frac{1}{(-j \cdot 203.179)}\right]}$$ Filter + Capacitors

$Vd := 495 \cdot KV$ $Pd := 990 \cdot MW$ $Xcpu := 0.18$

$\gamma := 15 \cdot deg$ $Nbr := 2$ $Vac := 230 \cdot KV$

Variables:

$scr \equiv 2.5$ $angle \equiv 75$

$SCR(scr) := scr \cdot e^{(-j \cdot angle \cdot deg)}$ $Zs(scr) := \frac{Zbase}{SCR(scr)}$ System Impedance

$$ESCR(scr) := Zbase \cdot \left(\frac{1}{Zf} + \frac{1}{Zs(scr)}\right)$$

Load Flow Calculations:

$Id := \frac{Pd}{Vd}$ $Id = 2 \cdot KA$

$TrZbase := \frac{211^2}{600}$ $Xc := Nbr \cdot Xcpu \cdot TrZbase$ $Xc = 26.713 \cdot \Omega$

$$Ell := \frac{\left[Vd + \left(\frac{3}{\pi}\right) \cdot Xc \cdot Id\right]}{(1.35 \cdot \cos(\gamma))}$$ $Ell = 418.725$ i.e., $Vd = 1.35\ Ell\ Cos(\gamma) - (3/\pi)\ Xc\ Id$

$TR := \frac{Ell}{2 \cdot 230}$ $TR = 0.91$

Calculation of Power Factor: Cos(Φ)

$$\text{cos\_alpha} := \frac{\sqrt{2}\cdot Id\cdot Xc}{Ell} - \cos(\gamma \qquad \alpha := \text{acos}(\text{cos\_alpha}) \qquad \alpha = 141.766\cdot\text{deg}$$

$$\mu := \pi - \alpha - \gamma \qquad \mu = 23.234\cdot\text{deg}$$

$$pf := \frac{(\cos(\alpha) + \cos(\alpha + \mu))}{2} \qquad \phi := -\text{acos}(pf) \qquad \phi = -151.129\cdot\text{deg}$$

$$Iac := \frac{(-Pd)}{\left[\left(\sqrt{3}\right)\cdot pf\cdot 230\right]}\cdot e^{(j\cdot\phi)} \qquad Iac = -2.485 - 1.37j$$

$$If := \frac{230}{\left(\sqrt{3}\cdot Zf\right)} \qquad If = 4.119\cdot 10^{-4} + 1.408j$$

$$Is := If + Iac \qquad Is = -2.485 + 0.038j$$

$$Esys(scr) := Vac + \sqrt{3}\cdot Zs(scr)\cdot Is \qquad Esys(scr) = 205.08 - 87.6j$$

$$Es(scr) := |Esys(scr)| \qquad Es(scr) = 223.006\cdot KV$$

$$\delta := \arg(Esys(scr)) \qquad \delta = -23.13\cdot\text{deg}$$

Evaluation of dγ/dα:

$$\alpha := \alpha + \Delta\alpha \qquad \Delta\alpha \equiv 0.2\cdot\text{deg}$$

$$Ellx(\gamma) := \sqrt{2}\cdot Xc\cdot\frac{Id}{(\cos(\alpha) + \cos(\gamma))} \qquad \phi(\gamma) := -\text{acos}\left(\frac{\cos(\alpha) - \cos(\gamma)}{2}\right)$$

$$Vdx(\gamma) := 1.35\cdot Ellx(\gamma)\cdot\cos(\gamma) - \frac{3}{\pi}\cdot Xc\cdot Id \qquad Pdx(\gamma) := Vdx(\gamma)\cdot Id$$

$$Isx(\gamma) := \frac{-Pdx(\gamma)}{\left[\sqrt{3}\cdot\frac{Ellx(\gamma)}{(2\cdot TR)}\cdot\cos(\phi(\gamma))\right]}\cdot e^{(j\cdot\phi(\gamma))} + \frac{Ellx(\gamma)}{\left(\sqrt{3}\cdot 2\cdot TR\right)}\cdot\frac{1}{Zf}$$

Given

$$Es(scr)\cdot\cos(\delta) - \frac{Ellx(\gamma)}{(2\cdot TR)} - \text{Re}\left(\sqrt{3}\cdot Isx(\gamma)\cdot Zs(scr)\right) = 0$$

$$Es(scr)\cdot\sin(\delta) - \text{Im}\left(\sqrt{3}\cdot Isx(\gamma)\cdot Zs(scr)\right) = 0$$

$$\gamma\delta(scr) := \text{Find}(\gamma, \delta) \qquad gamma(scr) := \gamma\delta(scr)_0 \qquad delta(scr) := \gamma\delta(scr)_1$$

Results:

$$d\gamma\_over\_d\alpha(scr) := \frac{(gamma(scr) - \gamma)}{\Delta\alpha} \qquad d\gamma\_over\_d\alpha(scr) = -1.99$$

List of Figures