DC Capacitor Voltage Balancing in Multi-Level Converters

By

Mehrdad Espah Boroojeni

A thesis submitted to the Faculty of Graduate studies of
The University of Manitoba
in partial fulfilment of the requirements for the degree of

MASTER OF SCIENCE

Department of Electrical and Computer Engineering
University of Manitoba
Winnipeg, Manitoba

Abstract

Multi-level converters that provide more than two levels of voltage to achieve an output waveform closer to sinusoidal waveform with less distortion are very attractive to power applications. This thesis investigates several multi-level converter topologies and different modulation strategies such as pulse-width modulation and space vector modulation. Attention is paid in particular to SVM strategy. Although SVM strategy is applicable for *N*-level converter, this thesis only focuses on five-level and three-level diode clamped converter (DCC).

Despite their appealing harmonic spectrum and low losses, multi-level converters are known to suffer from inherent voltage imbalance on their dc side. The thesis presents a method in order to balance the dc side capacitor voltages for an *N*-level converter. The presented balancing method is based on minimizing a cost function which is related to voltage divergence of the dc capacitors. This method is used for a three-level SVM to overcome the voltage drifting problem.

Acknowledgments

First of all, I would like to thank my advisor, Dr. Filizadeh, for his encouragement, guidance and support. During my master's program, he has always helped me and encouraged me. I should say that, I was very lucky to have had the opportunity to work with him.

I would like to express my appreciation to all of my friends and colleagues in the Department of Electrical Engineering of University of Manitoba. Also I would like to thank all the staff in the Electrical Engineering Department especially Traci Hofer, Amy Dario, and Erwin Dirks for their kindness and their help.

I wish to thank Dr. Gole for his guidance and recommendation. I also enjoyed and learned a lot by attending his courses.

I would also like to thank the Manitoba Hydro and the Mathematics of Information Technology and Complex Systems (MITACS) for their partial financial support.

Finally, I would like to thank my lovely parents for everything that they have done for me. Their unconditional help and support encourage me during all my life.

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

In recent years a new breed of power electronic converters, commonly referred to as voltage-source converters, is being pursued for application in power systems. A conventional voltage source converter topology, known as a two-level converter, has so far been the most widely used converter in power system applications; however it creates several harmonic components beside the fundamental frequency component and has a high $\frac{dv}{dt}$ switching stress, both leading to power quality and loss issues. The switching losses generated by two-level converters increase when higher quality waveforms are generated. This effectively plagues the use of this topology for high-power applications where excessive losses cannot be tolerated.

Significant improvements in the output voltage quality and converter losses can be obtained by increasing the voltage levels generated at the converter output. A multi-level converter is a power electronic circuit capable of generating such voltages. In comparison with a two-level converter, a multi-level converter has less harmonic distortion and less $\frac{dv}{dt}$ switching stress. By increasing

the number of levels, the output waveform of a multi-level converter becomes smoother and closer to a sine wave; however with more levels both the circuit component count and complexity increase.

In the literature several types of multi-level converter topologies have been proposed. The earliest topology was the three-level diode clamped converter, which was also known as neutral point clamped converter [1]. In this topology the intermediate dc link has a total voltage of V_{dc} which is divided to *N*-levels via *N*-1 capacitors. There are also other multi-level topologies such as flying capacitor converter and cascaded converter. A flying capacitor converter is similar to a diode clamped converter; however it uses capacitors instead of clamping diodes, which makes this topology a bulky and expensive converter. The cascaded converter needs an isolated dc source for each bridge. It should be noted that all the multi-level topologies will be explained in detail in Chapter 2 of this thesis.

Among these topologies, the diode clamped converter is the most exploited and analyzed in the literature so far, particularly for electric power transmission [2-6]. Control and modulation methods for diode clamped converters and voltage balancing strategies for the dc-side capacitors are the main research focus for this topology. Because of these reasons, the attention is paid to diode clamped converter in this thesis.

1.2 Problem Definition

For proper operation, multi-level converters need to receive equal dc voltages on their dc side. If dc sources, i.e. batteries, are used, it is relatively straightforward to ensure that the dc side voltages remain equal during the operation of the converter. This luxurious case, however, does not normally exist in reality. DC side voltage is often provided with passive capacitors [7].

Therefore these dc capacitors need to have equal shares of the dc voltage. One of the main drawbacks of the multi-level diode-clamped converters is that they experience unequal and drifting voltages on their dc sides, which leads to malfunction of the converter and distortion of the ac-side voltage waveform.

The current solutions to the problem can be categorized into circuit-based solutions and control and switching modifications. In the literature a number of approaches have been proposed for voltage drift phenomena, including the following:

- In order to maintain the capacitor voltages at their desire value, use of isolated dc sources for each capacitor is proposed in [8]. The switching pattern for this approach is not very complicated; however, using isolated dc sources adds to the cost and complexity of the system.
- In order to balance the dc capacitor voltages, use of auxiliary converters to inject current to the dc side intermediate branch is proposed in [9-12]. Using an auxiliary converter requires supplementary hardware, which makes the system expensive and complex.
- In order to balance and maintain the dc capacitor voltages, modifications to the switching pattern of the converter are proposed in [13-15].

For the first two approaches, additional power hardware is needed, which makes the converter circuitry expensive and more complex. In comparison with these two approaches, the third approach provides an economically reasonable method to solve the voltage balancing problem; however it requires a more complicated switching strategy.

This thesis proposes a method to equalize the dc capacitor voltages based on the switching pattern modification for an *N*-level diode clamped converter and then verifies this method for a three-level diode clamped converter by using computer simulation.

1.3 Thesis Objectives

The main objectives of this thesis can be divided into three parts, as follows.

1. A literature survey on several multi-level topologies and different modulation strategies. This thesis explains the most typical multi-level converter topologies and discuses their advantages and disadvantages; at the same time, it documents general concepts about commonly used switching techniques, e.g. pulse-width modulation (PWM) and space-vector modulation (SVM).
2. Multi-level converters present inherent problems with regards to balancing the voltages on the dc-side capacitors. Another objective of this work is to present a voltage balancing method for multi-level diode clamped converter, which is arguably the most common topology at the present time. Also, the solution is verified using extensive computer simulations using the PSCAD/EMTDC transient simulation program for a three-level diode clamped converter.
3. Another objective of this thesis is to develop accurate, yet computationally efficient, models for multi-level converters. The thesis aims to develop a SVM model for the multi-level converters in the PSCAD/EMTDC transient environment.

1.4 Thesis Outline

Following this introductory chapter, this thesis is divided into the following chapters.

Chapter 2. *Multi-level converter topologies*

An expanded introduction for the main multi-level converter topologies is provided in this chapter. At the same time, the merits and drawback of each topology in comparison with other topologies is described and discussed.

Chapter 3. *Switching strategies for multi-level converters*

Different modulation strategies are explained in this chapter. In the first section the pulse-width modulation strategy for multi-level converter is presented. This chapter then talks about space vector modulation strategy. This part elaborates principles of operation of space vector modulation (SVM) and also a method for calculation of the duty cycles for the vectors is presented. After explaining this concept, it explains the method for three-level SVM. The three-level SVM is also implemented and all the outputs are shown. At the end of this chapter a brief introduction about over-modulation is presented.

Chapter 4. *Space vector modulation for five-level Converter*

At the first section of this chapter, space vector modulation for five-level converter is explained in detail. Then this chapter proposed a new method to implement the five-level SVM. At the end simulation results for implemented five-level converter are provided.

Chapter 5. *Balancing techniques for N-level converters*

This chapter introduces a dc-side capacitor voltage balancing method for multi-level converters. After explaining the concept for an *N*-level converter, it elaborates the capacitor balancing method for three-level converter. At the end, in order to verify the balancing method, simulation results for various conditions are shown.

Chapter 6. *Conclusions and future work*

A summary of the conclusions of this thesis and some recommended future directions are presented in this chapter.

Chapter 2

Multi-Level Converter Topologies

2.1 Introduction

Recently the *multi-level* converters have become very attractive for the medium and high power applications [16]. Increasing the number of levels in the multi-level converters leads to nearly sinusoidal output voltage, less converter losses and smaller *dv*/*dt*. These characteristics make multi-level converters very popular for the power industry [1, 8, 17-19].

The focal task of multi-level converters is to synthesize a sinusoidal voltage from several levels of voltages. As the number of levels increases, the synthesized output waveform includes more steps; therefore it approaches to an actual sine wave. This implies a better harmonic spectrum compared with the classic two-level topology.

The main shortcomings of multi-level converter are: (i) they need a large number of semi-conductor devices, i.e. diodes and controlled switches, than their two-level counterparts[20, 21]; (ii) using such number of devices leads to further complexity in the control and firing pulse generation circuits; (iii) in multi-level converters, capacitors are usually used instead of dc

voltage sources. Voltage balancing of these capacitors is a challenging task in this area [11, 22-26];

2.2 Multi-level converter topologies

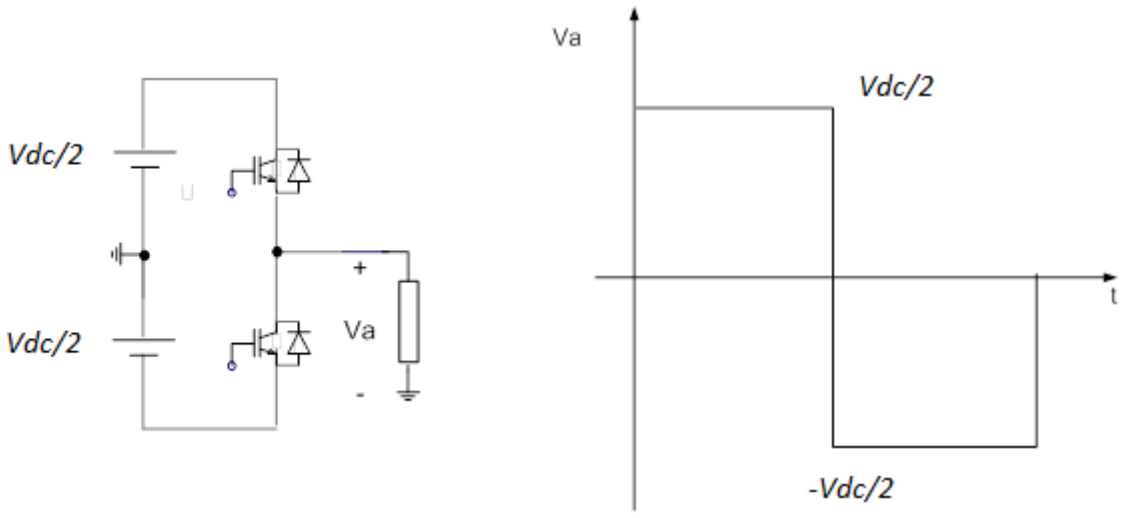
Although there are a large number of multi-level converter topologies in the literature [16, 27-30], four different major converter structures will be explained in this chapter. Before continuing further, it should be illustrious that the term "*multi-level converter*" is used to refer to a power electronic circuit that may operate as an inverter or a rectifier. The most typical multi-level topologies are:

- Diode-clamped converter (DCC)
- Flying capacitor converter (FCC)
- Cascaded converter
- Modular multi-level converter (MMC)

A brief description of each converter topology is presented next.

2.2.1 Diode clamped converter

In 1981, A. Nabae, I. Takahashi and H. Akagi introduced a new neutral-point-clamped PWM inverter (NPC-PWM inverter) [1]. This converter had better harmonic spectrum compared with conventional two-level inverter. Fig. 2.1 shows a typical output voltage waveform for a two-level converter.



(a) Converter tolopology (b) Typical voltage waveform

Fig. 2.1 A two-level converter (one phase shown)

The voltage consists of a fundamental frequency component and several harmonic components. Presence of harmonics leads to power quality and loss issues, particularly when the harmonic content of the waveform mostly lies in the low frequency spectrum [31]. Moreover, in two-level converter each transistor should tolerate a voltage stress equal to $V_{dc}/2$ (see Fig. 2.2).

In the new converter, two additional transistors per phase are deployed (see Fig. 2.3a). Therefore, each transistor tolerates a voltage equal to $V_{dc}/4$. Therefore, by using identical transistors with the ones used in two-level converter, the dc link could be equal to $2V_{dc}$.

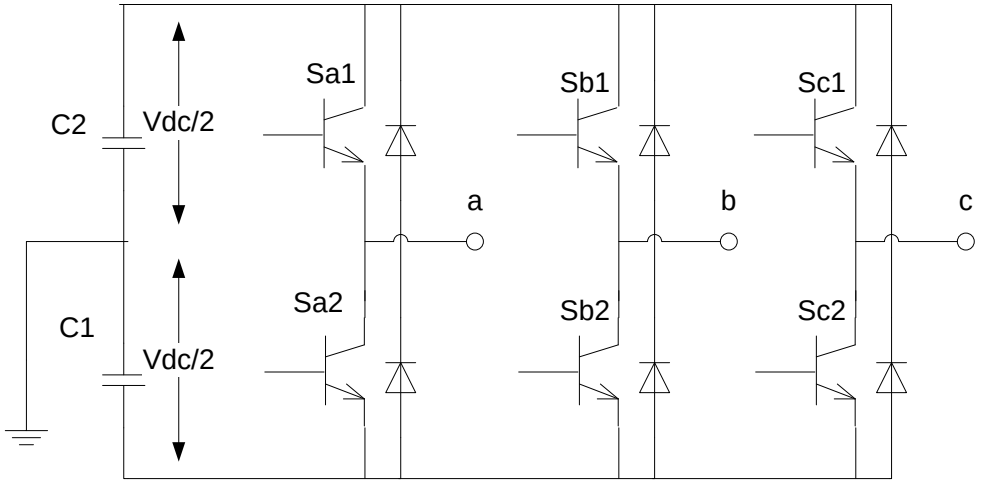
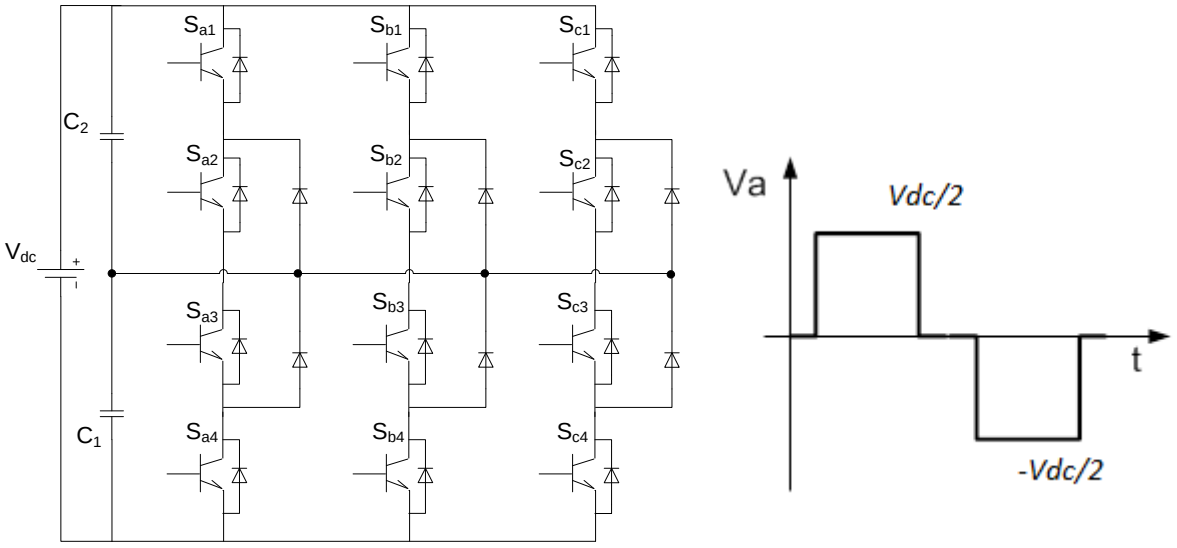


Fig. 2.2 schematic of a two-level converter

Fig. 2.3(b) and Fig. 2.4(b) show typical voltage waveforms that can be obtained through the operation of three-level and five-level converters, respectively. As seen the voltage waveforms comprise several levels that can be suitably used to create waveforms with more resemblance to an actual sine wave. This implies a better harmonic spectrum without having to incur significant switching losses.

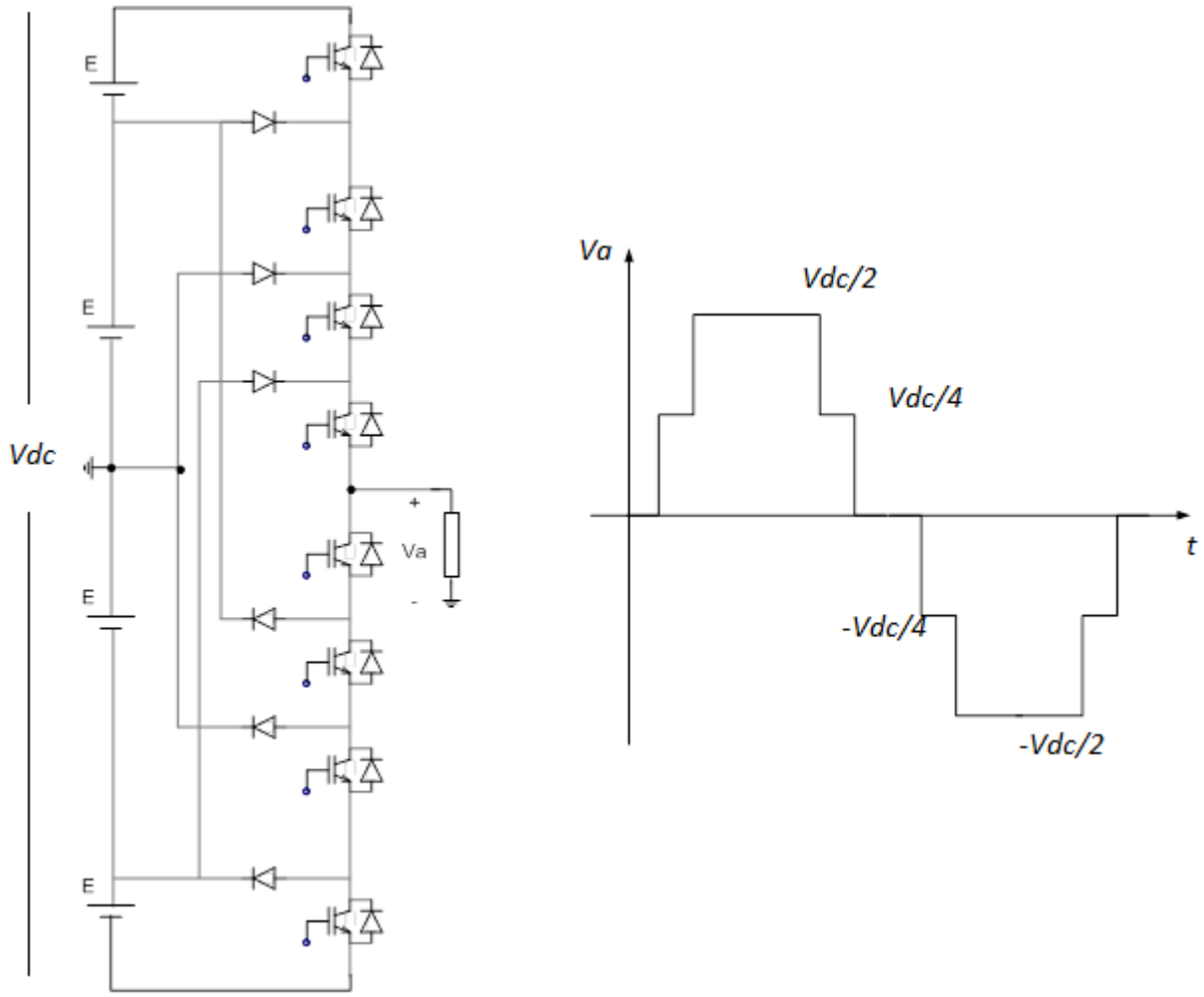


(a) Converter tolopology (b) Typical voltage waveform

Fig. 2.3 Three-level Diode-Clamped Converter

This topology has been extended for higher level converter to achieve more levels in the output phase voltage with respect to zero. Fig. 2.4a shows a five-level edition of DCC type converter. All the possible switching configurations for three-level and five-level configurations can be seen in Table 2.1

In general for *N*-level DCC topology, *N*-1 adjacent switches of each leg must be in the on-state. As a result, the output phase voltage takes *N* discrete values in the range of $V_{dc}/2$ and $-V_{dc}/2$ [32].



(a) Converter tolopology (b) Typical voltage waveform

Fig. 2.4 Five-level Diode-Clamped Converter (one phase shown)

TABLE 2.1 Possible switching in (a) three-level and (b) five-level DCC

Voltage V_{a0}	*Switch State*			
	S_{a1}	S_{a2}	S_{a3}	S_{a4}
$V_{dc}/2$	ON	ON	*OFF*	*OFF*
0	*OFF*	ON	ON	*OFF*
$-V_{dc}/2$	*OFF*	*OFF*	ON	ON

(a)

Voltage V_{a0}	*Switch State*							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a5}	S_{a6}	S_{a7}	S_{a8}
$V_{dc}/2$	ON	ON	ON	ON	*OFF*	*OFF*	*OFF*	*OFF*
$V_{dc}/4$	*OFF*	ON	ON	ON	ON	*OFF*	*OFF*	*OFF*
0	*OFF*	*OFF*	ON	ON	ON	ON	*OFF*	*OFF*
$-V_{dc}/4$	*OFF*	*OFF*	*OFF*	ON	ON	ON	ON	*OFF*
$-V_{dc}/2$	*OFF*	*OFF*	*OFF*	*OFF*	ON	ON	ON	ON

(b)

2.2.1.1 Advantages and disadvantages of the DCC topology

The main advantages of diode-clamped converter in comparison with other multi-level topologies are:

- The number of capacitors that are used in DCC is lower than other topologies. Although it needs some extra clamping diode, but its low number of reactive devices is very important from the standpoint of cost [33].
- They can be connected to only one dc link voltage as can be seen in Fig. 2.3.

- When the number of levels is high enough, harmonic content is negligibly small, which can be used to avoid or reduce the need for extensive filtering.

However, practical experiences with this topology reveal some technical difficulties that complicate its application for high power converters; these include:

- The issue of maintaining the voltage balance of the capacitors for the converters with more than three levels has been shown to be impossible for some operating conditions[34]. These problems appear when working with low modulation indices and high power factor.
- For converters with more than three levels the clamping diodes are subjected to high voltage stress equal to $V_{dc}(n\text{-}2)/(n\text{-}1)$. Therefore, series connection of diodes is required. This complicates the design and cost concerns.

2.2.2 Flying capacitor converter

Flying capacitor converter (FCC) was introduced by Meynard and Foch in 1992 [35] and has been considered to be the most technically viable alternative to the diode-clamped topology. Compared with other multi-level converter topologies, it presents advantages and disadvantages [35, 36]. Fig. 2.5 illustrates the three-level version of this topology.

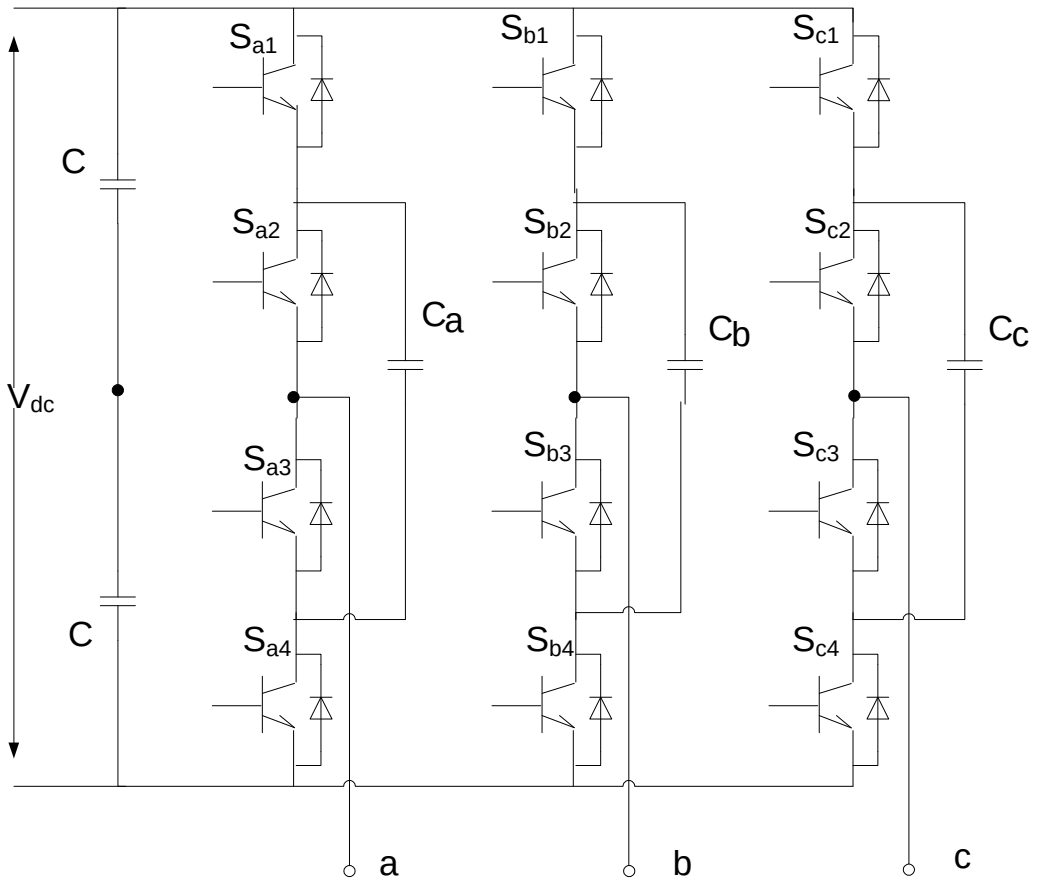


Fig. 2.5 Three-level Flying Capacitor Converter

Each phase-leg of this topology has an identical structure, which is similar to diode clamped topology except that instead of using clamping diodes, capacitors are used. The voltage synthesis in this topology has more flexibility than the diode-clamped converter. One advantage of the flying capacitor converter is that its inner voltage level can be achieved by different combinations. Table 2.2 shows a list of all combinations of phase voltage levels that are possible for the five-level circuit.

TABLE 2.2 Flying capacitor five-level converter redundant voltage levels

Output Voltage V_{a0}	*Switch State*							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{á1}$	$S_{á2}$	$S_{á3}$	$S_{á4}$
$V_{a0} = V_{dc}/2$ (no redundancies)								
$V_{dc}/2$	1	1	1	1	0	0	0	0
$V_{a0} = V_{dc}/4$ (3 redundancies)								
$V_{dc}/2 - V_{dc}/4$	1	1	1	0	0	0	0	1
$V_{dc}/4$	0	1	1	1	1	0	0	0
$V_{dc}/8 - V_{dc}/8 + V_{dc}/4$	1	0	1	1	0	1	0	0
$V_{dc}/4 - V_{dc}/8 + V_{dc}/8$	1	1	0	1	0	0	1	0
$V_{a0} = 0$ (4 redundancies)								
$V_{dc}/4 - V_{dc}/4$	1	1	0	0	0	0	1	1
$V_{dc}/8 - V_{dc}/4 + V_{dc}/8$	1	0	0	1	0	1	1	0
$-V_{dc}/8 + V_{dc}/4 - V_{dc}/8$	0	1	1	0	1	0	0	1
$-V_{dc}/8 + V_{dc}/8 - V_{dc}/8 + V_{dc}/8$	0	1	0	1	1	0	1	0
0	0	0	1	1	1	1	0	0
$V_{a0} = -V_{dc}/4$ (3 redundancies)								
$V_{dc}/8 - 3V_{dc}/8$	1	0	0	0	0	1	1	1
$-V_{dc}/8 + V_{dc}/8 - V_{dc}/4$	0	1	0	0	1	0	1	1
$-V_{dc}/4 + Vdc/8 - Vdc/8$	0	0	1	0	1	1	0	1
$-V_{dc}/4$	0	0	0	1	1	1	1	0
$V_{a0} = -V_{dc}/2$ (no redundancies)								
$-V_{dc}/2$	0	0	0	0	1	1	1	1

2.2.1.1 Advantages and disadvantages of FCC topology

The main advantages of the flying capacitor converter are:

- In this topology phase redundancies are available to control the dc link capacitor voltage compared with other multi-level topologies.

- Both real and reactive power flow can be controlled in opposed to cascaded converter [8, 37, 38]

This topology has a few disadvantages as follows:

- By increasing the number of levels, a large number of capacitors are required. This fact is important due to the cost of these devices.
- Switching losses is high and efficiency is poor for real power transmission [39].
- Flying capacitors require being set up to the same voltage level, presenting difficulty in pre-charging the capacitors and converter startup.

2.2.3 Cascaded Converter

The cascade converter or full bridge converter is formed by two single-phase inverters with separated voltage sources [40]. In Fig. 2.6 a basic three-phase three-level cascaded converter is shown.

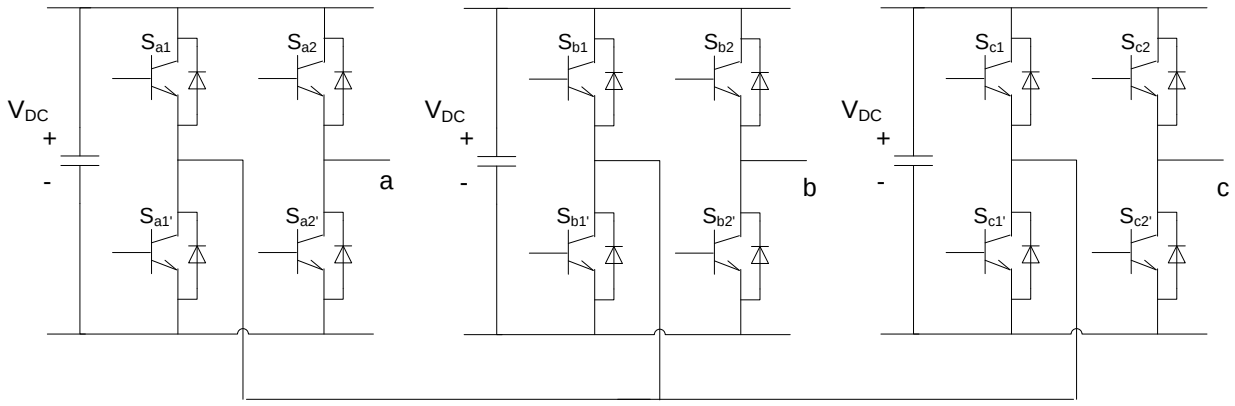


Fig. 2.6 Three-phase three-level Cascaded converter

Considering the three-level basic cell for phase a, it is clear that by using different combination of the four switches S_{a1}, S_{a2}, $S_{a1'}$, and $S_{a2'}$, it can produce three different level output voltage

$+V_{dc}$, 0, and $-V_{dc}$. In order to achieve $-V_{dc}$, switches S_{a1} and $S_{a2'}$ are turned on, while $+V_{dc}$ can be achieved by turning on switches S_{a2} and $S_{a1'}$. The output voltage is 0, when S_{a1} and S_{a2}, or $S_{a1'}$ and $S_{a2'}$ are turned on [8].

To build a multi-level cascaded converter, one can easily connect this three-level converter in series. In order to build an *N*-level (*N* is odd) cascaded converter, (*N*-1)/2 three-level units are needed. Fig. 2.7 shows two three-level cascaded converters in series to build a five-level cascaded converter. It should be pointed out that each three-level unit needs an independent dc voltage source.

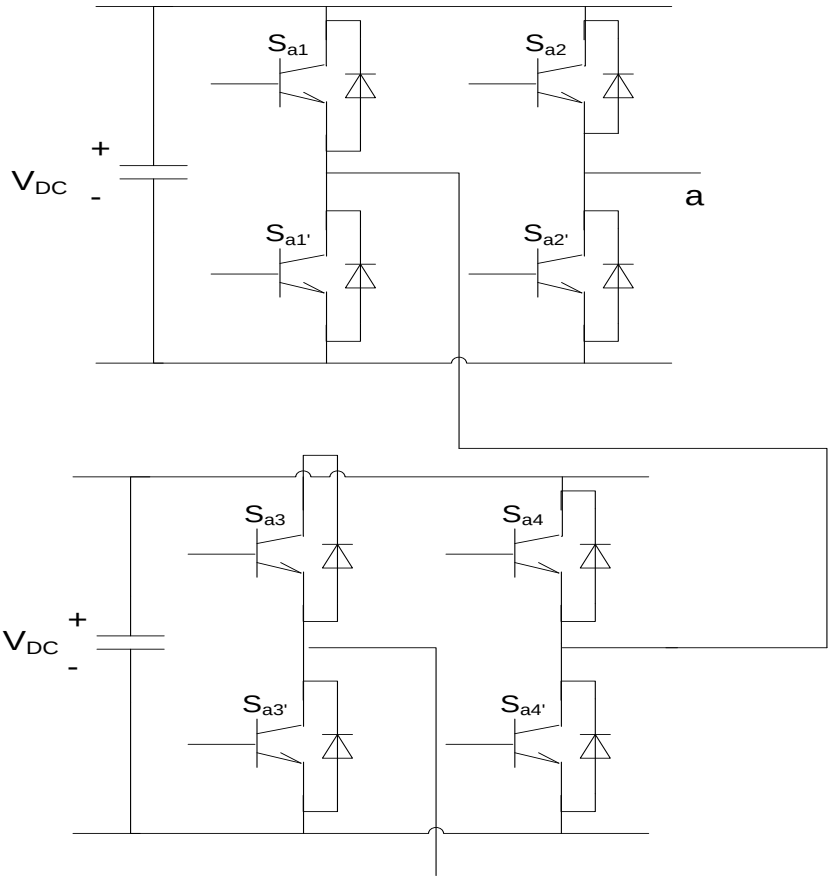


Fig. 2.7 Five-level cascaded converter (single phase shown)

In conventional cascaded converter, all the dc voltage sources have exactly the same value. However, different dc voltage sources level can be applied in order to achieve different output

voltage level; this is one of the most advantageous features of this approach. The number of levels in the output voltage can be increased without using any new component. For instance, in Fig.2.8 by using two different voltage sources, V_{dc} and 2 V_{dc}, the cascaded converter can generate seven-level (0, +/- V_{dc}, +/- 2 V_{dc}, +/- 3 V_{dc}) in the output voltage.

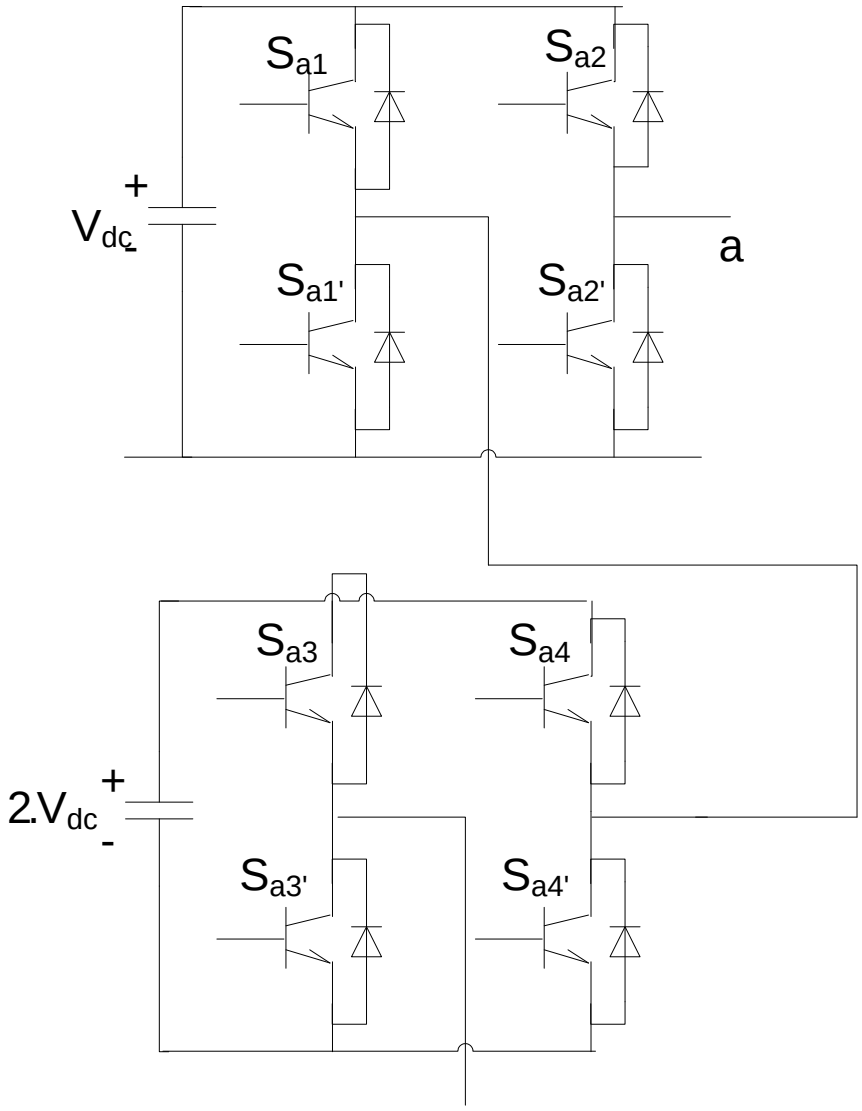


Fig. 2.8 Seven-level cascaded converter (single phase shown)

2.2.4 Modular Multi-level Converter

A next generation multi-level converters is the modular multi-level converter (MMC) [41-43], which was first introduced in 2001 [44]. The MMC is suitable for high power conversion (e.g. HVDC-Plus [45]), network interties on power generation and transmission, and also medium voltage converters [46, 47] due to its easy assembly and flexibility in the power circuit [46]. Fig. 2.9 shows one-phase of a three-level modular multi-level converter.

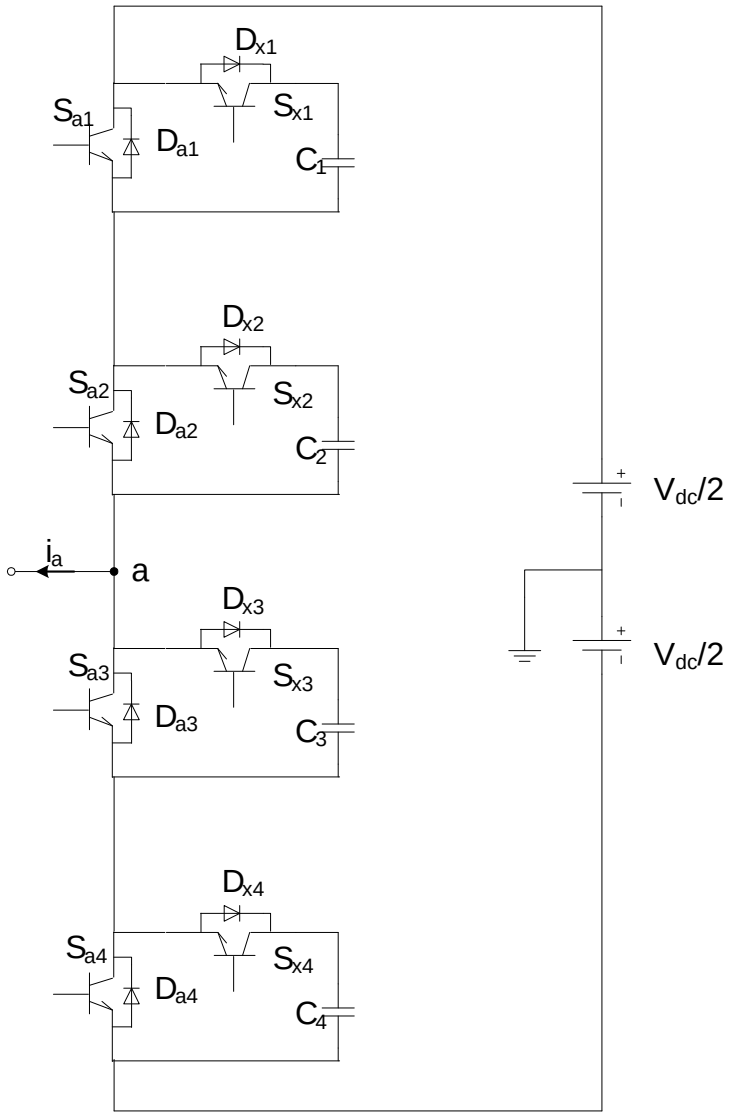


Fig. 2.9 Three-level modular converter (single phase shown)

In Fig. 2.9 in each leg *i*, there are four complimentary pairs of switches, (S_{i1}, S_{x1}), (S_{i2}, S_{x2}), (S_{i3}, S_{x3}), and (S_{i4}, S_{x4}), where S_i switches are the main switches and S_x ones are the auxiliary switches. For the complimentary switching pair, turning on one of the switches implies the other one has to be turned off; for example, turning on S_{i1} means S_{x1} should be turned off. Moreover, in a three-level configuration, at each instant of time, two of the main switches and two of the auxiliary ones must be turned on. Clearly by using different combinations of the four switches, three different levels of output voltage can be achieved. For instance, when the switches S_{a1} and S_{a2} (main switches) and S_{x3} and S_{x4} (auxiliary switches) are turned on, the output voltage is $V_{a0} = V_{dc}/2$. Similarly, the output voltage is $V_{a0} = -V_{dc}/2$ when S_{a3} and S_{a4} (main switches) and S_{x1} and S_{x2} (auxiliary switches) are turned on. To achieve the output voltage $V_{a0} = 0$, there are four different switching combinations. Table 2.3 summarises different voltage levels and their corresponding switching states for a three-level modular converter.

TABLE 2.3 Possible switching states for a three-level modular converter

Voltage V_{a0}	*Switch State*							
	S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{x1}	S_{x2}	S_{x3}	S_{x4}
$V_{dc}/2$	ON	ON	*OFF*	*OFF*	*OFF*	*OFF*	ON	ON
0	ON	*OFF*	ON	*OFF*	*OFF*	ON	*OFF*	ON
	OFF	ON	ON	*OFF*	ON	*OFF*	*OFF*	ON
	OFF	ON	*OFF*	ON	ON	*OFF*	ON	*OFF*
	ON	*OFF*	*OFF*	ON	*OFF*	ON	ON	*OFF*
$-V_{dc}/2$	*OFF*	*OFF*	ON	ON	ON	ON	*OFF*	*OFF*

For a three-phase *N*-level modular converter, the total number of needed capacitors is 6(*N*-1), and the number of switches per phase is 4(*N*-1).

In this chapter several multi-level converter topologies were introduced. In order to achieve desired output voltage, different switching configurations have been proposed in the literature. In the next chapter attention is paid to modulation strategies – pulse width modulation and space vector modulation - for the diode clamped converter.

Chapter 3

Switching Strategies for Multi-Level Converters

3.1 Introduction

In a previous chapter, different multi-level converter topologies were discussed. In order to produce the desired output voltage, different switching methodologies exist for different converter topologies. Modulation strategies are responsible for switching control in the converter. Several modulation strategies have been proposed in the literature [48-52]. Pulse Width Modulation (PWM) and Space Vector Modulation (SVM) are two popular modulation strategies, which will be explained in this chapter.

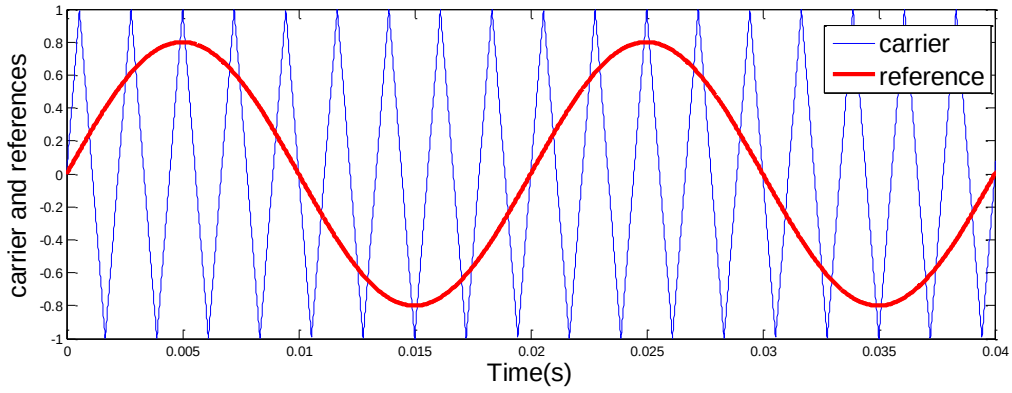
3.2 PWM Modulation

3.2.1 Principles of operation of PWM modulation

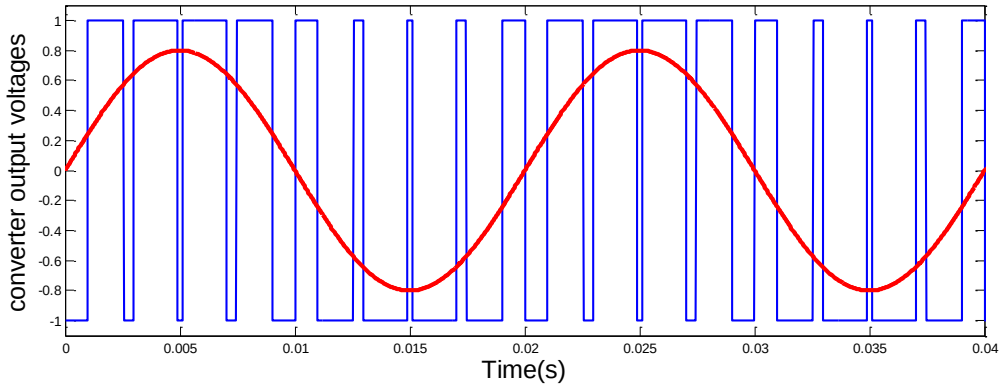
The simplest PWM technique compares a reference waveform at low frequency F_r with a triangular or saw-tooth carrier at a higher frequency F_s (sampling frequency). If the magnitude of

the reference signal is greater than that of the carrier signal, the switch will be turned on; otherwise it will be turned off.

Sinusoidal PWM (SPWM), in which the reference waveform is a sinusoidal waveform, is the conventional PWM method to control the switchings of a voltage source converter. In Fig. 3.1 a sinusoidal reference signal is modulated using a triangular carrier to obtain a high frequency PWM pulse train. SPWM controls each phase independently of other phases. Therefore, for a three phase converter, three separated SPWM controllers with reference waveforms that are 120^{o} out of phase are needed. The carrier waveform remains the same for all phases.



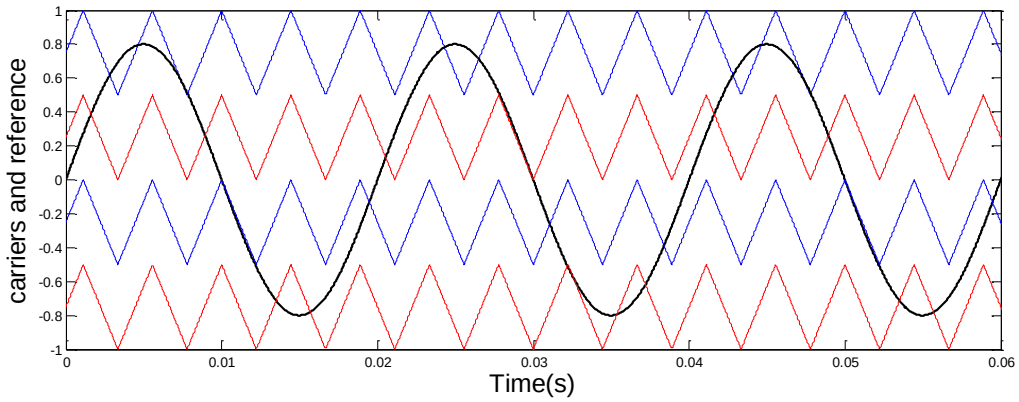
(a)



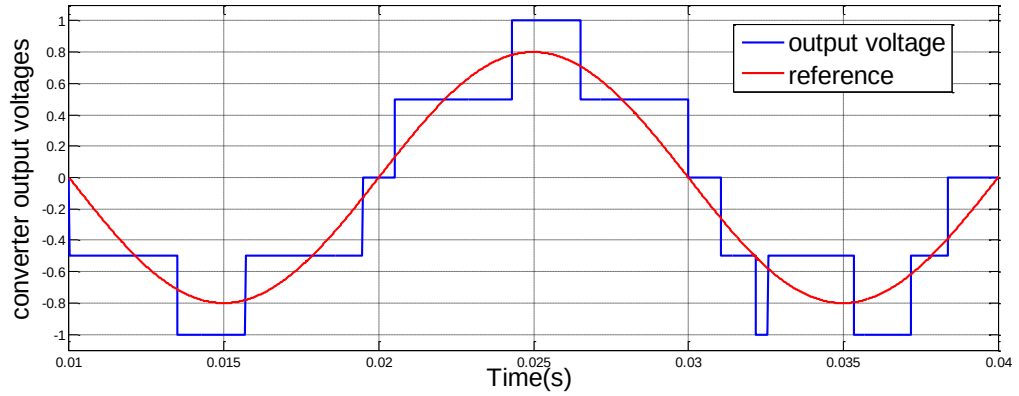
(b)

Fig. 3.1 Conventional two-level PWM (a) reference and carrier waveform (b) output voltage

Moreover, multi-level PWM can be obtained using more than one triangular carrier. For an N-level diode clamped converter, N-1 triangular carries are needed. All the triangular carriers have the same frequency and amplitude, and the generated output voltage is shaped in contiguous levels in the range of $-(N\text{-}1)V_{dc}/2$ to $(N\text{-}1)V_{dc}/2$. Several Multi-carriers PWM methods are proposed in the literature [53]. As an example, a five-level PWM scheme is shown in Fig 3.2. The phase disposition (PD) method is used in this case. As shown the reference sinusoidal waveform is compared with four triangular carriers to create the output voltage pulses. If the reference waveform is greater than the upper triangular carrier, the output voltage will be $2V_{dc,}$ however if it is less than the upper triangular carrier and greater than second up triangular carrier the output is $V_{dc.}$ The output is 0 when the reference vector is less than second up triangular and greater than second low triangular carrier. While the reference vector is less than second low triangular and greater than the lower one, the output voltage will be reached to - $V_{dc.}$ The output voltage is equal to -2 V_{dc} when the reference vector is less than the lower triangular carrier.



(a)



(b)

Fig. 3.2 Five-level PWM (a) carriers and reference (b) output voltage waveform

3.3 Space Vector PWM

3.3.1 Principles of SVM modulation

A schematic representation of an *N*-level diode-clamped converter is shown in Fig. 3.3.

In SVM, the converter is controlled through the concept of converter states. Each combination or switching state corresponds to a defined set of three phase voltage. The total number of switching states for an *N*-level converter is N^3. Fig. 3.4 represents the space vector (SV) diagram for the two-level converter.

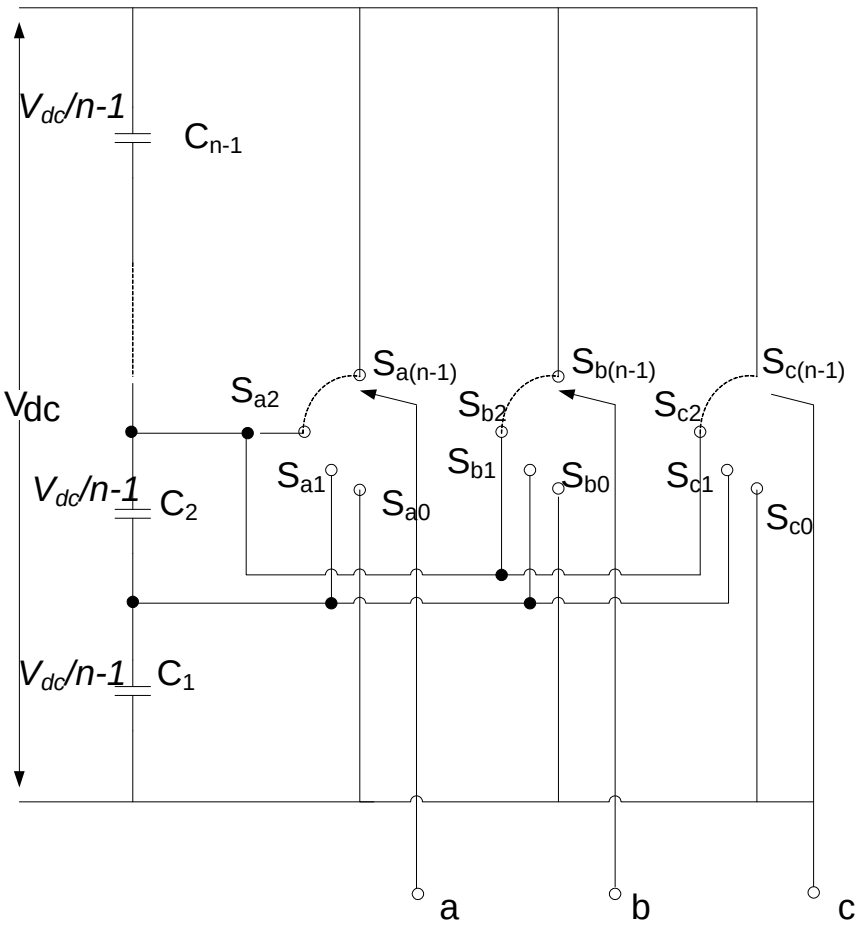


Fig. 3.3 Schematic representation of an n-level diode-clamped converter (adapted from [33])

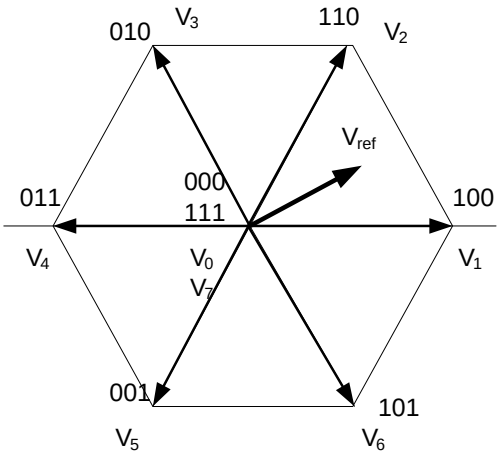


Fig. 3.4 SV diagram for a two-level converter

Any set of balanced three phase voltages in the abc frame can be represented into a dq-plane by applying Clark's transformation [54, 55]. In the same way, any set of reference phase voltages V_a, V_b, and V_c can be mapped into two dimensional plane as $\mathbf{V_{ref}}$ by using the same transformation as follows.

$$\vec{V}_{ref} = 2/3\,(V_a(t) + V_b(t)e^{j2\pi/3} + V_c(t)\,e^{-j2\pi/3}) \tag{3.1}$$

In two-level SVM, there are eight possible states (2^3=8). States are numbers in the binary from 000 to 111, where the digits from left to right show the states of phases a, b, and c, respectively. As shown in Fig. 3.4 the six active vectors V_1 to V_6 (100, 110, 010, 011, 001, 101) have equal lengths and are separated by 60^o in the plane. The other two vectors lie in the origin because of their null lengths (000,111). These two vectors produce the same line-to-line voltage, therefore they are redundant states.

As the number of levels at the converter output increases, the number of redundant space vector increases. For three-level and five-level converters there are seven and thirty-seven redundant vectors, respectively. Fig. 3.5 shows a SV diagram of the three-level converter. As shown the three-level converter has six double vectors which each one has two different redundant states and one triple vector in the origin which has three different redundant states. Proper selection of these redundant vectors will help to achieve desired performance characteristics and can also be used in capacitor voltage balancing.

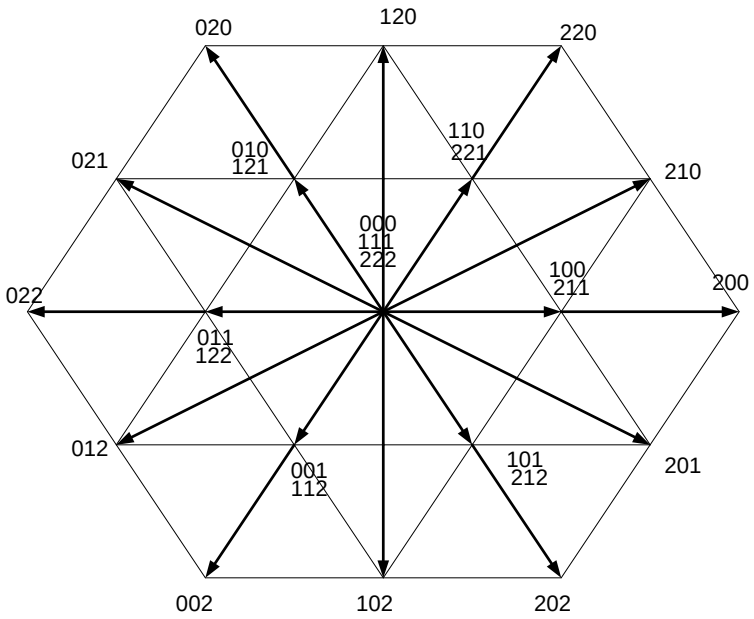


Fig. 3.5 SV diagram for the three-level converter

Computational burden to synthesize the reference voltage waveform is mostly associated with tragicomic calculations for:

(i) Identification of the sector and triangle where the tip of the reference vector lies

(ii) Identification of adjacent switching voltage vectors of the reference voltage

(iii) Calculation the on-duration time intervals of the switching vectors

Moreover, in the conventional SVM, each triangle has its own equations for the calculation of on-duration time interval. For the three-level SVM and five-level SVM, there are four and sixteen triangles in each sector, respectively.

3.3.2 Calculation of the duty cycle

In SVM, the reference voltage vector, which rotates in the dq-plane at the desired output voltage frequency of f, is sampled at the sampling frequency $F_s=F_{sn}.f$ in each period where F_{sn} is normalized sampling frequency. The normalized sampling frequency F_{sn} must be chosen as an

integer multiple of 6 (the hexagon has six equal sub-sections) in order to avoid non-characteristic harmonics.

This section will introduce a simple method for calculation of the on-duration time intervals of the switching vectors for multi-level converter. The method for calculation duty cycles is based on determining projections of the reference vector. At any sampling instant, the tip of the voltage vector lies in a triangle formed by the three switching vector adjacent to it, as shown in Fig. 3.6.

In Fig. 3.6, vectors $\vec{m}_1$ and $\vec{m}_2$ are the projections of $\vec{V}_{ref}$ onto the vectors $\vec{V}_2 - \vec{V}_1$ and $\vec{V}_3 - \vec{V}_1$, respectively.

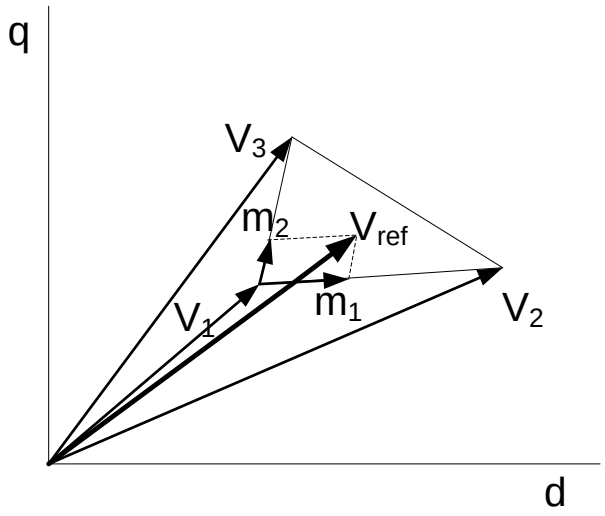


Fig. 3.6 Projections of reference vector V_{ref}

Hence, the reference vector can be written as follows.

$$\vec{V}_{ref} = \vec{m}_1 + \vec{m}_2 + \vec{V}_1 \tag{3.2}$$

or

$$\vec{V}_{ref} = m_1 (\vec{V}_2 - \vec{V}_1)/ I_1 + m_2 (\vec{V}_3 - \vec{V}_1)/ I_2 + \vec{V}_1 \tag{3.3}$$

where I_1 and I_2 are the lengths of the vectors $\vec{V}_2 - \vec{V}_1$ and $\vec{V}_3 - \vec{V}_1$, respectively. Therefore, (3.3) can be written as follows.

$$\vec{V}_{ref} = m_1.\vec{V}_2/I_1 + m_2.\vec{V}_3/I_2 + (\vec{V}_1 - m_1.\vec{V}_1/I_1 - m_2.\vec{V}_1/I_2 \quad (3.4)$$

or

$$\vec{V}_{ref} = \vec{V}_2(m_1/I_1) + \vec{V}_3(m_2/I_2) + \vec{V}_1(1 - m_1/I_1 - m_2/I_2) \quad (3.5)$$

According to (3.5) the duty cycle of the vectors are as follows.

$$D_1 = 1 - m_1/I_1 - m_2/I_2, \qquad D_2 = m_1/I_1 \text{ and } \qquad D_3 = m_2/I_2 \quad (3.6)$$

where D_1, D_2, and D_3 are the duty cycles for vector $\vec{V}_1$, $\vec{V}_2$, and $\vec{V}_3$, respectively. In order to simplify the calculation of these duty cycles, the length of the vectors in the triangular regions for the balanced SV diagram are normalized to unity; in other words $I_1=I_2=1$.

Therefore, equations (3.5) and (3.6) can be modified as follows.

$$\vec{V}_{ref} = \vec{V}_2 m_1 + \vec{V}_3 m_2 + \vec{V}_1(1 - m_1 - m_2) \quad (3.7)$$

and

$$D_1 = 1 - m_1 - m_2, \qquad D_2 = m_1 , \quad \text{and} \qquad D_3 = m_2 \quad (3.8)$$

Similarly, if the tip of the reference voltage vector lies in any other triangle, the duty cycles of the switching vectors can be calculated similarly. In the next section, this method will be used to calculate the duty cycles for the three-level SVM.

3.4 Three level converter

3.4.1 SVM operation for three level converters

The task of the modulator is to find the triangle in which the tip of the reference vector lies, and calculate the durations needed (duty cycles) of each vector in order to synthesize the reference vector by using the nearest three vectors, as follows.

$$\vec{V}_{ref} = \vec{V}_1 D_1 + \vec{V}_2 D_2 + \vec{V}_3 D_3 \tag{3.9}$$

In Fig. 3.7 the space vector diagram of a three-level converter is shown. In order to find the nearest three vectors to the reference vector, the diagram is divided into six separate sectors (similar to highlighted sector) and each sector is further separated into four triangular regions.

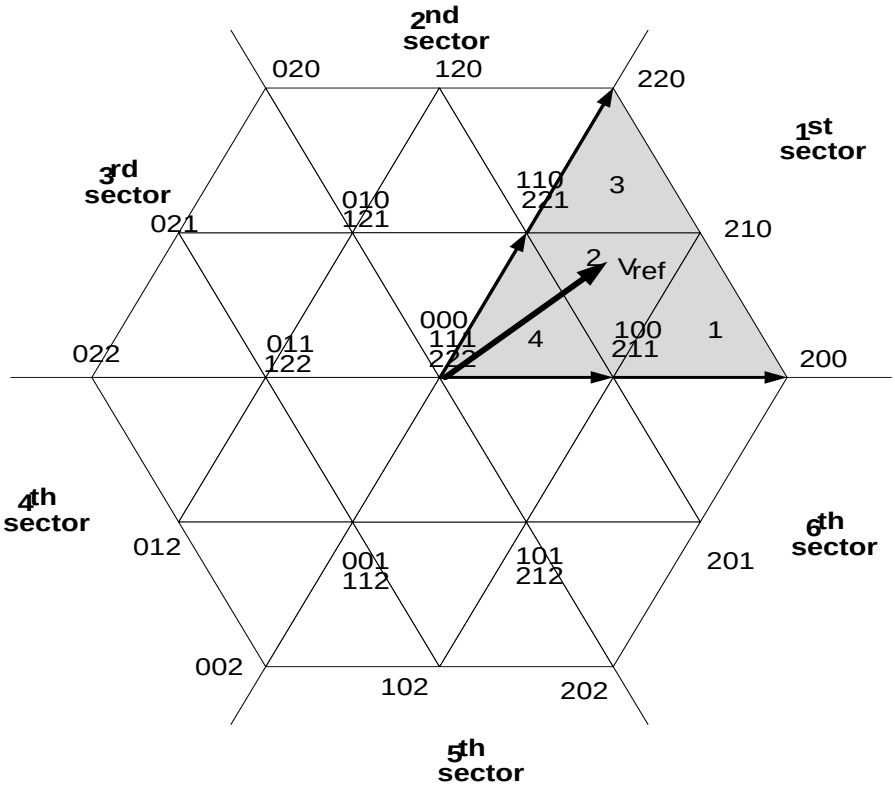


Fig. 3.7 Space vector diagram of a three-level converter

As mentioned before, for two-level VSC, states numbering are from 000 to 111. For three-level VSC the states are numbered from 000 to 222. Each digit shows the level of the voltage for the respective leg (a, b, c from left to right). That is, 0 means that the phase voltage is switched to $-V_{dc}/2$, 1 means it is switched to 0, and 2 means it is switched to $V_{dc}/2$.

In Fig 3.7 four different groups of vectors can be distinguished:

1) The "zero vectors" at the origin (000, 111, and 222)
2) The "large vectors" (200, 220, 020, 022, 002, and 202), which generate either the highest or the lowest output voltage for the converter. In comparison with the two-level converter, these vectors are equivalent to the active vectors.
3) The "medium vectors" (210, 120, 021, 012, 102, and 201), whose length defines the amplitude of the reference voltage vector. The length of these vectors is $\frac{\sqrt{3}}{2}$ of the large vectors.
4) The "short vectors" (100, 211, 110, 221, 010, 121, 011, 122, 001, 112, 101, and 212), which have half of the length of the large vectors.

3.4.2 Calculation of the duty cycles for three-level converter

According to the symmetry of all the six sectors, it is easier to reflect the reference vector to the first sector in order to simplify the calculation. Moreover, in any of six sectors the amplitude of the reference vector must be normalized to fit into the diagram. Note that the length of each side of the triangles is unity.

In Fig. 3.8, the maximum possible length for the reference vector ($\mathbf{V}_{ref}$) is two units; nevertheless its length is limited to $\sqrt{3}$. If the lengths of the reference vector go longer than $\sqrt{3}$, over-

modulation is produced (over-modulation will be explained at the end of this chapter). This is because at such values, the tip of the reference vector will exit the hexagon at some portion of the revolution.

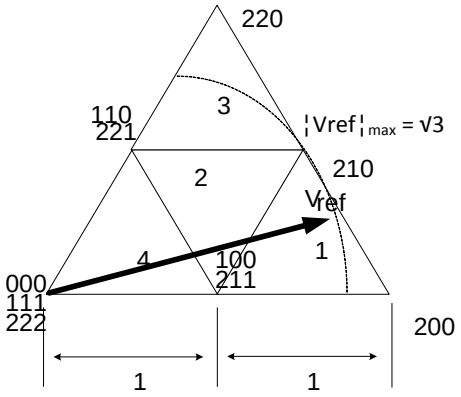


Fig. 3.8 Maximum possible length for normalized reference vector in three-level SVM

Basically modulation index m uses values in the interval $m \in [0,1]$. Therefore, the length of the normalized vector will be as follows.

$$V_{ref} = \sqrt{3}m$$

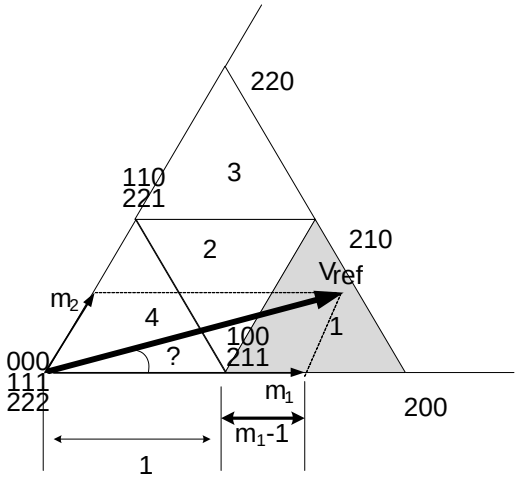


Fig. 3.9 Projection of the V_{ref} in region 1, for three-level converter

In Fig. 3.9 the normalized reference vector is projected into $\vec{m}_1$ and $\vec{m}_2$ (section 3.3.2)

The solution for the lengths of $\vec{m}_1$ and $\vec{m}_2$ can be shown to be.

$$m_1 = V_{ref}(\cos\theta - \sin\theta/\sqrt{3}) \tag{3.10}$$

$$m_2 = 2V_{ref}(\sin\theta/\sqrt{3}) \tag{3.11}$$

The first step for the modulator is to determine that in which triangle the tip of the reference voltage lies. After projecting the normalized reference vector into $\vec{m}_1$ and $\vec{m}_2$, it is clear that the tip lies in the region 1, if $m_1 > 1$ (Fig. 3.9). Similarly the condition for region 2 is that m_1 and $m_2 \leq 1$, and $m_1 + m_2 > 1$ (Fig. 3.10). The tip of the reference voltage lies in region 3 if $m_2 > 1$ (Fig. 3.11). Finally the conditions for region 4 are m_1 and $m_2 \leq 1$, and $m_1 + m_2 \leq 1$ (Fig. 3.12). Table 3.1 summarizes the conditions needed to determine the region where the reference vector lies.

TABLE 3.1 conditions needed to ascertain the region for SVM three-level

Region	Condition
1	$m_1 > 1$
2	$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 > 1$
3	$m_2 > 1$
4	$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 \leq 1$

After determining the region, the next step is to calculate the duty cycles of the nearest vectors in the first sector. For instance, in region 1, according to equation (3.8), the duty cycles are as follows.

$$D_{200} = m_1 - 1$$
$$D_{210} = m_2 \tag{3.12}$$
$$D_{100,211} = 2 - m_1 - m_2$$

The equations for every single triangle regions (1, 2, 3, and 4) are different. Fig. 3.10 shows the projection of the reference vector in region 2.

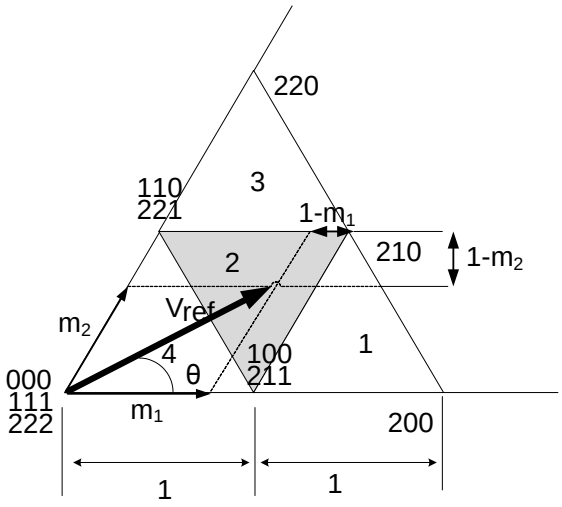


Fig. 3.10 Projection of the V_{ref} in region 2, for three-level converter

The duty cycle for this region can be calculated as follow:

$$D_{100,211} = 1 - m_2$$
$$D_{110,221} = 1 - m_1 \tag{3.13}$$
$$D_{210} = m_1 + m_2 - 1$$

Similarly for region 3, where the tip of the reference vector lies in the upper triangle, the duty cycles are as follows.

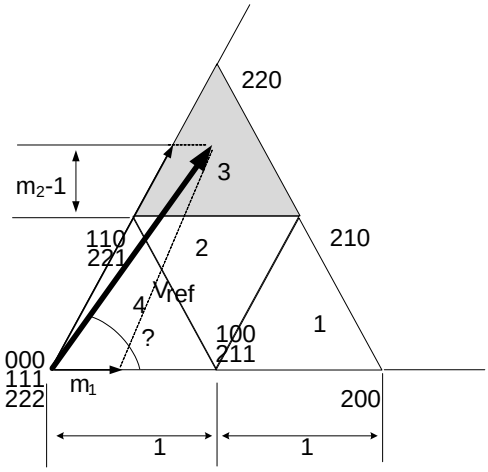


Fig. 3.11 Projection of the V_{ref} in region 3, for three-level converter

$$D_{210} = m_1$$

$$D_{220} = m_2 - 1 \tag{3.14}$$

$$D_{100,211} = 2 - m_1 - m_2$$

And finally for the region 4, the equations are expressed as follows.

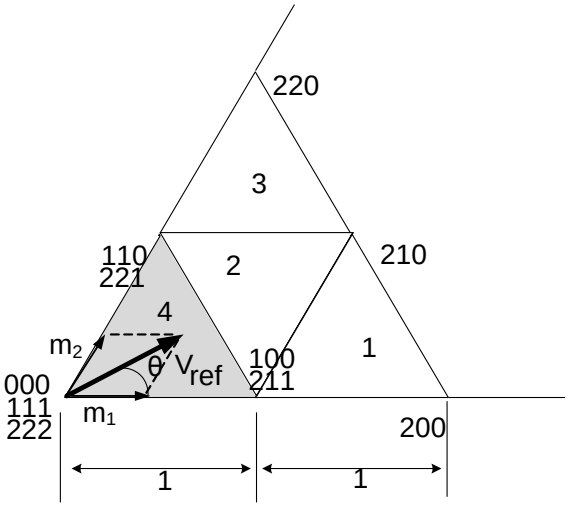


Fig. 3.12 Projection of the V_{ref} in region 4, for three-level converter

$$D_{100,211} = m_1$$

$$D_{110,221} = m_2 \tag{3.12}$$

$$D_{000,111,222} = 1 - m_1 - m_2$$

3.4.3 Simulation results

The simulation results of a two-level and a three-level DCC are shown for different values of modulation index (m) and switching frequency (F_{sn}) in the PSCAD/EMTDC simulation environment. The dc link voltage of the converter is taken as 1000 V. Fig. 3.13 shows simulation waveform of the ac side line to line voltage for a two-level converter.

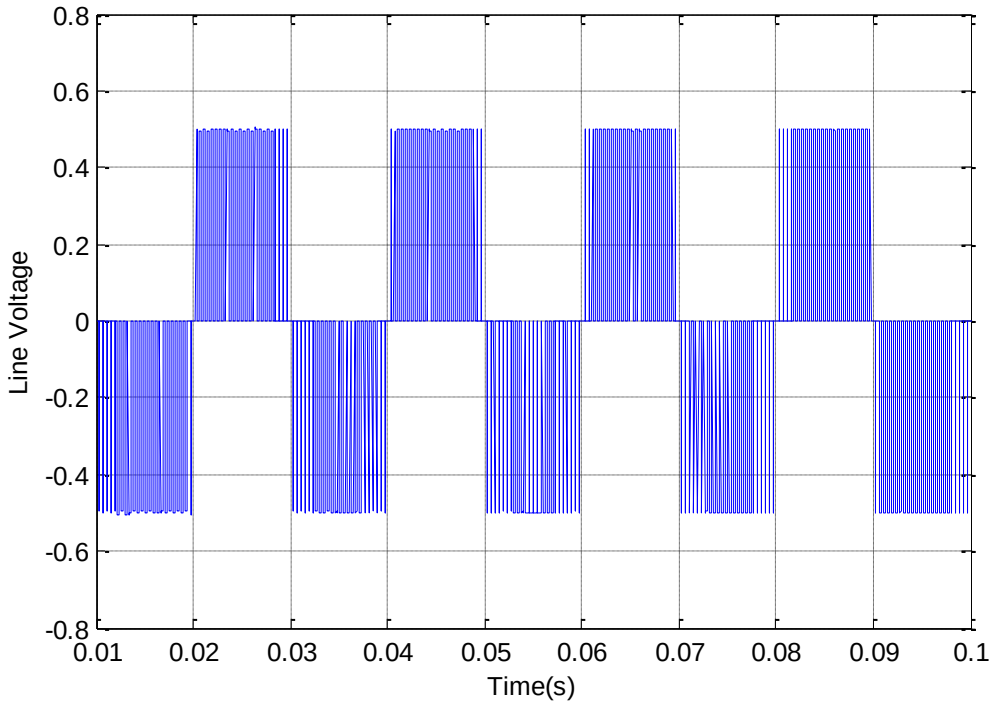
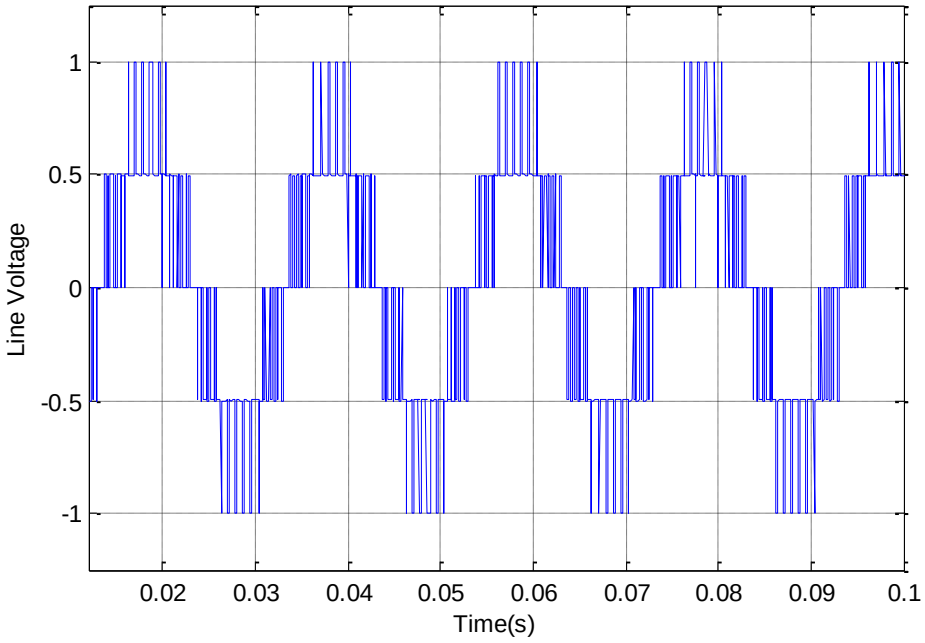


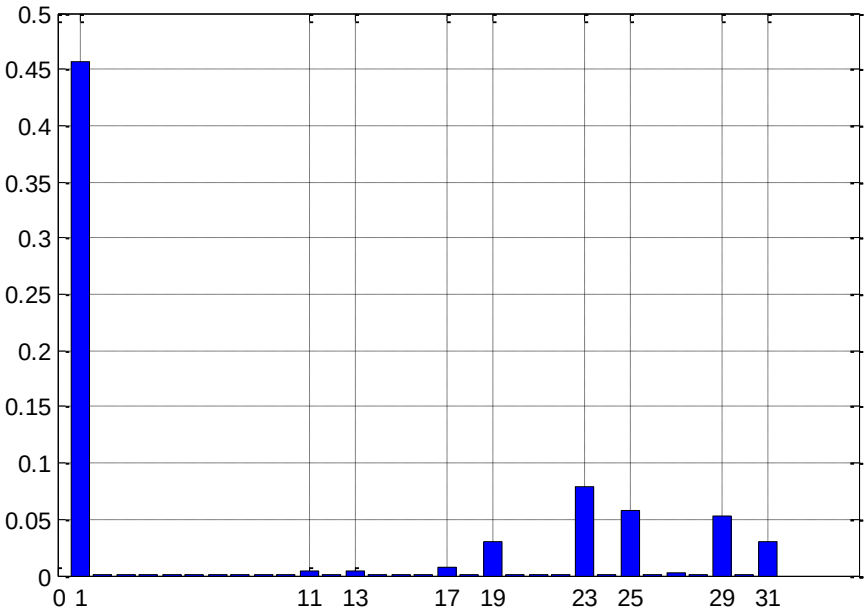
Fig. 3.13 The ac side line voltage and for a two-level converter;

m=0.8, F_{sn} = 24

Figs. 3.14 through Fig. 3.16 show the PSCAD/EMTDC based simulation results for a three-level DCC, and for different modulation index values. Fig. 3.14 shows the line to line ac side output voltage waveform and its spectrum for m = 0.8 and sampling frequency F_s equal to 24 times of the output frequency, f. As can be seen in this figure the output voltage waveform has main harmonic at the f=50. The other harmonics are around the switching frequency and its multiples beside the main harmonic. For instance, 29-th and 31-st harmonics have a large value. Figs. 3.15 and Fig. 3.16 show the line to line output voltage at the ac side for a three-level converter for m = 0.65 and m= 0.4, respectively. It is clear that as the level of the converter increases the line voltage appears closer to the desired sinusoidal waveform.



(a)



(b)

Fig. 3.14 (a) The ac side line voltage, (b) harmonic spectrum of line voltage, of a three-level converter;

m = 0.8, F_{sn} = 24

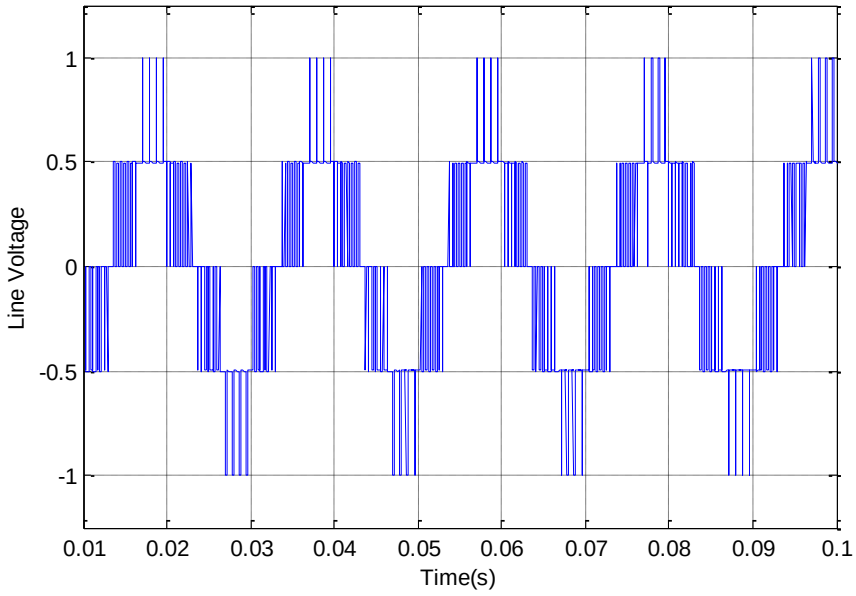


Fig. 3.15 The ac side line voltage of a three-level converter; m=0.65, F_{sn} = 24

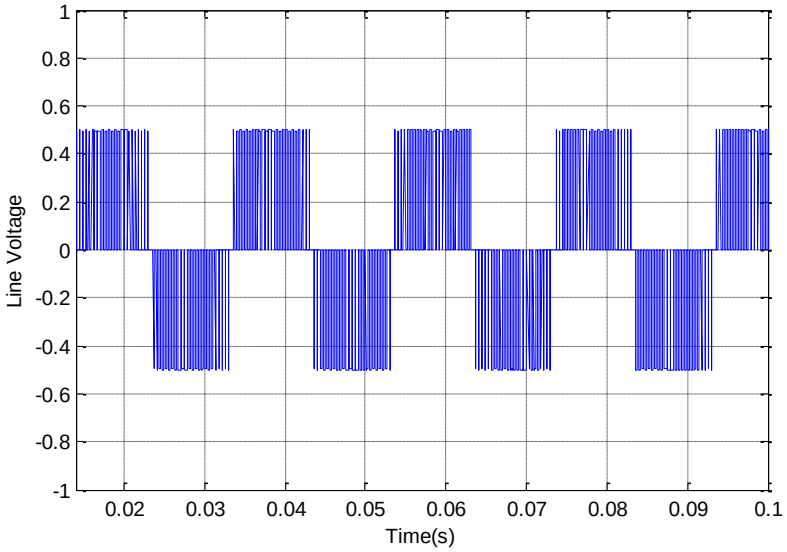


Fig. 3.16 The ac side line voltage of a three-level converter; m=0.4, F_{sn} = 24

3.5 Over-modulation

As mentioned before, among different topologies of multi-level converter, the three-level neutral point clamped converter (diode clamped converter) is a widely used topology. However, in this

topology, for certain switching states, the neutral point fluctuates. This problem is well explained in the literature [56]. The neutral point fluctuation deteriorates the performance of the converter at high modulation indices and over-modulation region.

In section 3.4.2, it was mentioned that the maximum possible length for normalized reference vector in three-level SVM is $\sqrt{3}$ (or *m*=1), which happens when it reaches the boundary of the hexagon (see Fig. 3.8). Any further increase in the modulation index leads the normalized reference vector to be partially outside the hexagon. This condition means the converter goes to the over-modulation mode of operation and ceases to be in a linear mode. Several schemes are proposed in the literate to compensate for the over-modulation region [57-64]. Over-modulation compensation aims to increase the linear mode of operation of the space vector modulation [65]. In this section one of these approaches is explained for the three-level DCC.

3.5.1 Operation of a three-level DCC in linear and over-modulation mode

Based on the value of the modulation index *m*, there are three modes of operation: linear mode, over-modulation mode I, and over-modulation mode II. In Fig. 3.17, the dashed line shows the trajectory of the normalized reference vector which is circular. Note that only the first sector is shown; it can be easily applied to other sectors. By increasing the modulation index, the length of the reference vector increases until at *m*=1, it reaches its maximum allowance length, in the other words; the circular trajectory becomes inscribed by the hexagon. It occurs at the reference vector angle $\alpha = \pi/3$. This is the upper limit for the linear mode of operation. The on-duration time for this region was previously explained in this chapter.

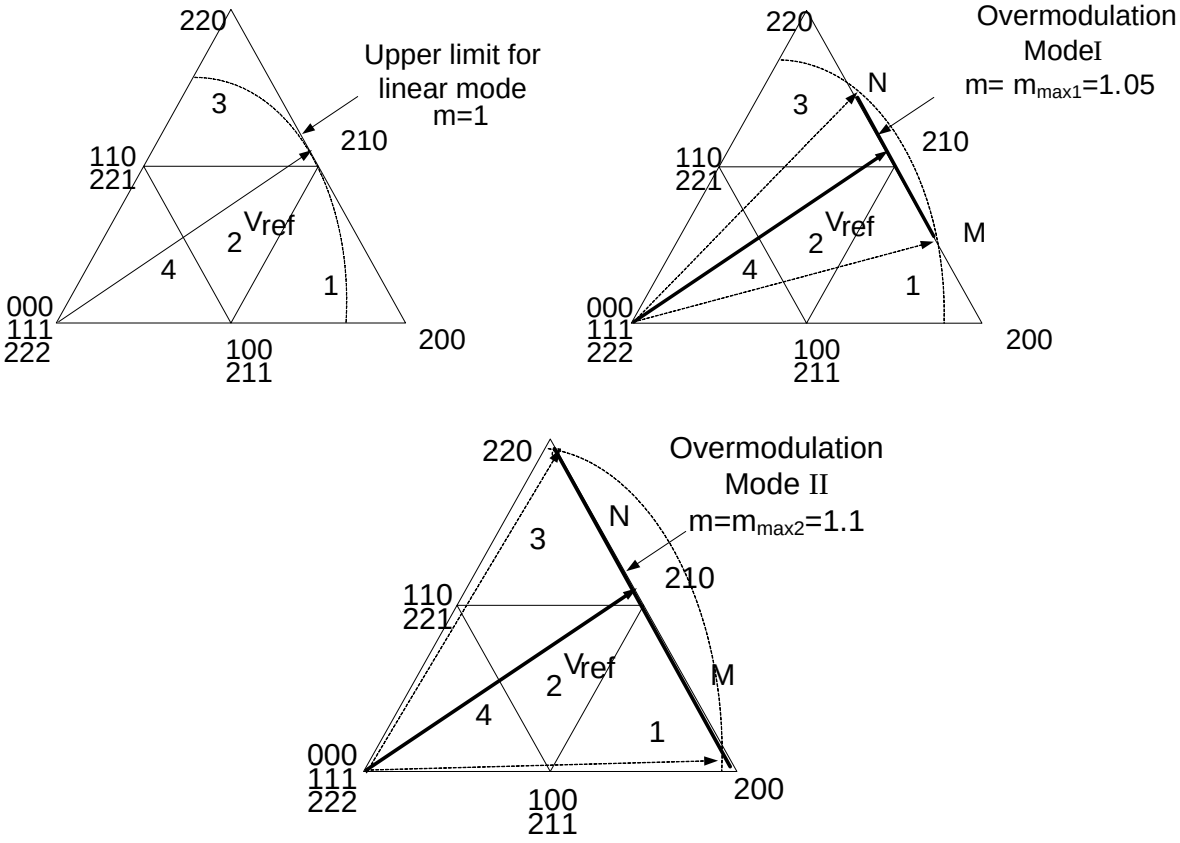


Fig. 3.17 Different modes of operation in three-level SVM

Any further increase in the modulation index leads to the over-modulation mode. In order to achieve continuous control over the voltage in over-modulation mode, this region is divided to two different modes [62, 66]. The maximum value for modulation index in mode I and mode II have been selected at m_{max1}= 1.05 and m_{max2}= 1.1, respectively [67]. The upper limit for mode I is at $m= m_{max1}$ and m_{max2} is maximum possible modulation index. The operation at the $m=m_{max2}$ is called as six-step operation. The calculations of on-duration time for each mode is proposed in [67, 68]

Chapter 4

Space Vector Modulation for Five-Level Converters

4.1 Five-level DCC

4.1.1 Principles of operation

Fig. 4.1 shows a schematic diagram of a three-phase, five-level diode clamped converter. At the dc side, it consists of four capacitors C_1- C_4. For the DC side voltage of V_{dc}, ideally each capacitor has the voltage equal to $V_{dc}/4$. On the other hand, at the ac side the output phase voltage has five separated levels of voltage, i.e. $V_{dc}/2$, $V_{dc}/4$, 0, - $V_{dc}/4$, and -$V_{dc}/2$. As shown in the Fig. 4.1 in each leg there are four complimentary pairs of switches, (S_1, $\acute{S}_1$), (S_2, $\acute{S}_2$), (S_3, $\acute{S}_3$), and (S_4, $\acute{S}_4$). For the complimentary switching pair, turning on one of the switches means the other one has to be turned off.

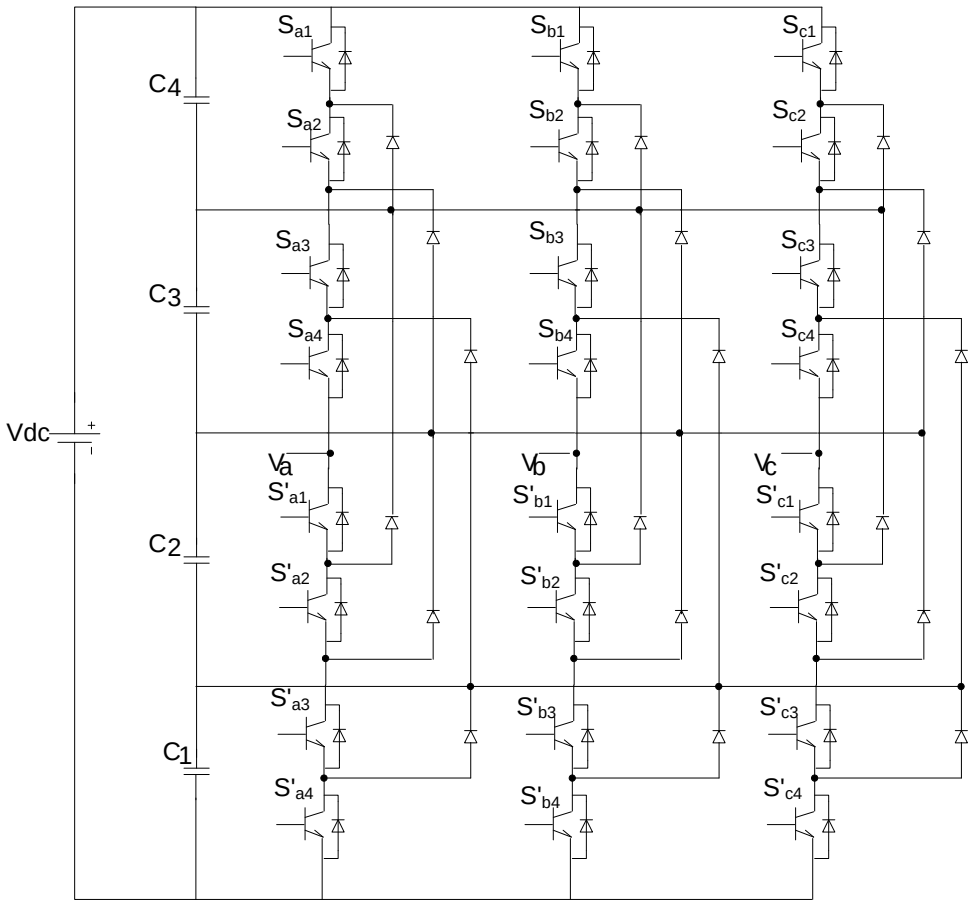


Fig. 4.1 Schematic diagram of a three-phase, five-level diode clamped converter

In this section the SVM method explained earlier will be applied to the five-level diode-clamped converter. The SV diagram for five-level DCC topology is shown in Fig. 4.2. The goal of this method is to find the triangle in which the tip of the reference vector lies. Each sector, which includes sixteen small triangles, is divided into four large triangles. Each of these large triangles is then considered as one sector of a three-level hexagon. Note that the large triangles in the five-level SVM have the same order of numbering that was used for the three-level SVM. For example, in the three-level SVM the nearest triangle to the origin is numbered as region 4 (Fig. 3.7), and similarly, in the five-level SVM the large triangle number 4 is the nearest triangle to the origin as well (Fig. 4.2).

In this method, similar to the three-level SVM, the large triangle that contains the tip of reference vector is found based on the projection of the normalized reference vector.

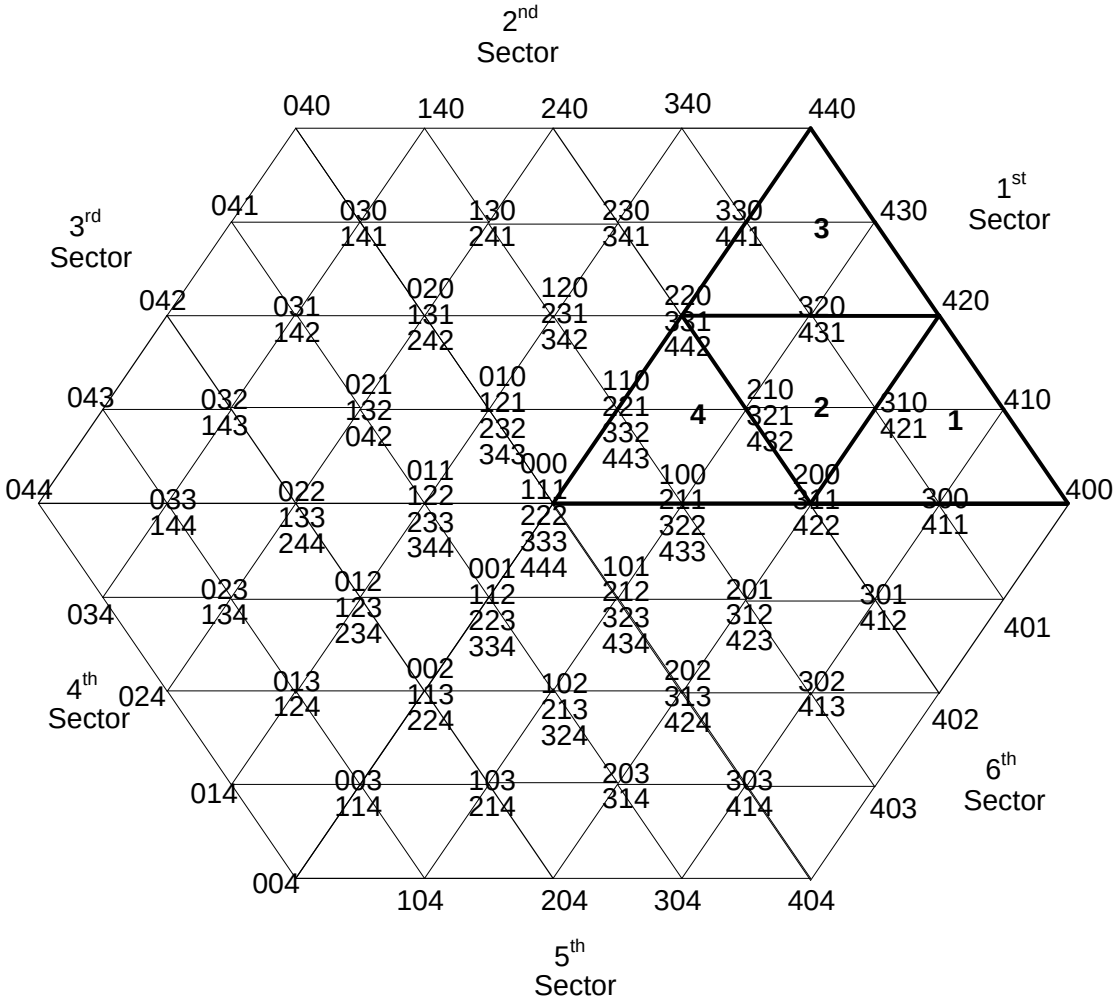


Fig. 4.2 Five-level vector diagram divided into big regions

Fig. 4.3 shows the case for which the normalized reference vector is located in the region 4 of the large triangle 1. The projections of the reference voltage, m_1 and m_2, are also shown. As seen, all the large triangles have four regions. Therefore the first step to find the triangle in which the tip of the reference vector lies is to determine the large encompassing triangle.

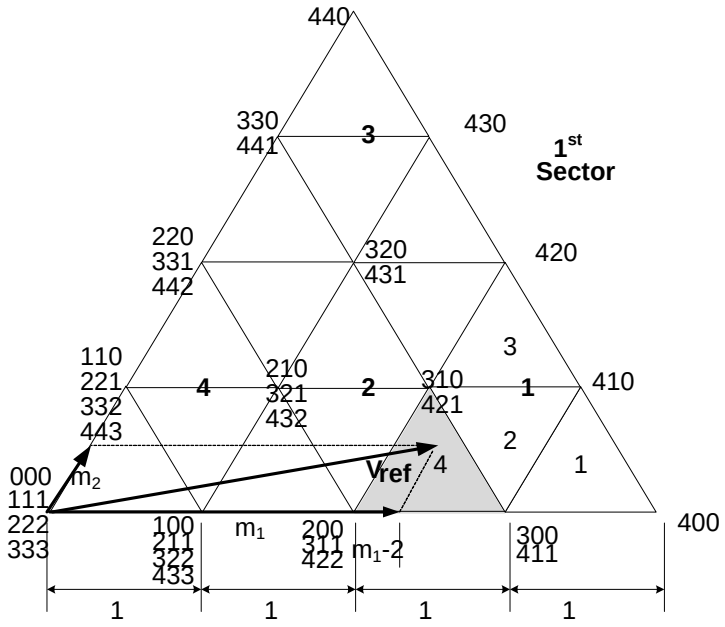


Fig. 4.3 Projection of the normalized reference vector into triangle 1, region 4

Eventually in order to find the region where the tip of the reference vector lies, each of these large triangles is divided into four different region (see section 3.4), and each of these regions is then considered as a sector similar to those in a two-level SVM (Fig. 3.4). Similarly, by decomposing the normalized reference vector, the region that bounds the tip of the reference vector will be found. Fig 4.4 shows the cases where the normalized reference vector is located in regions 1, 2, and 3 of the large triangle 1.

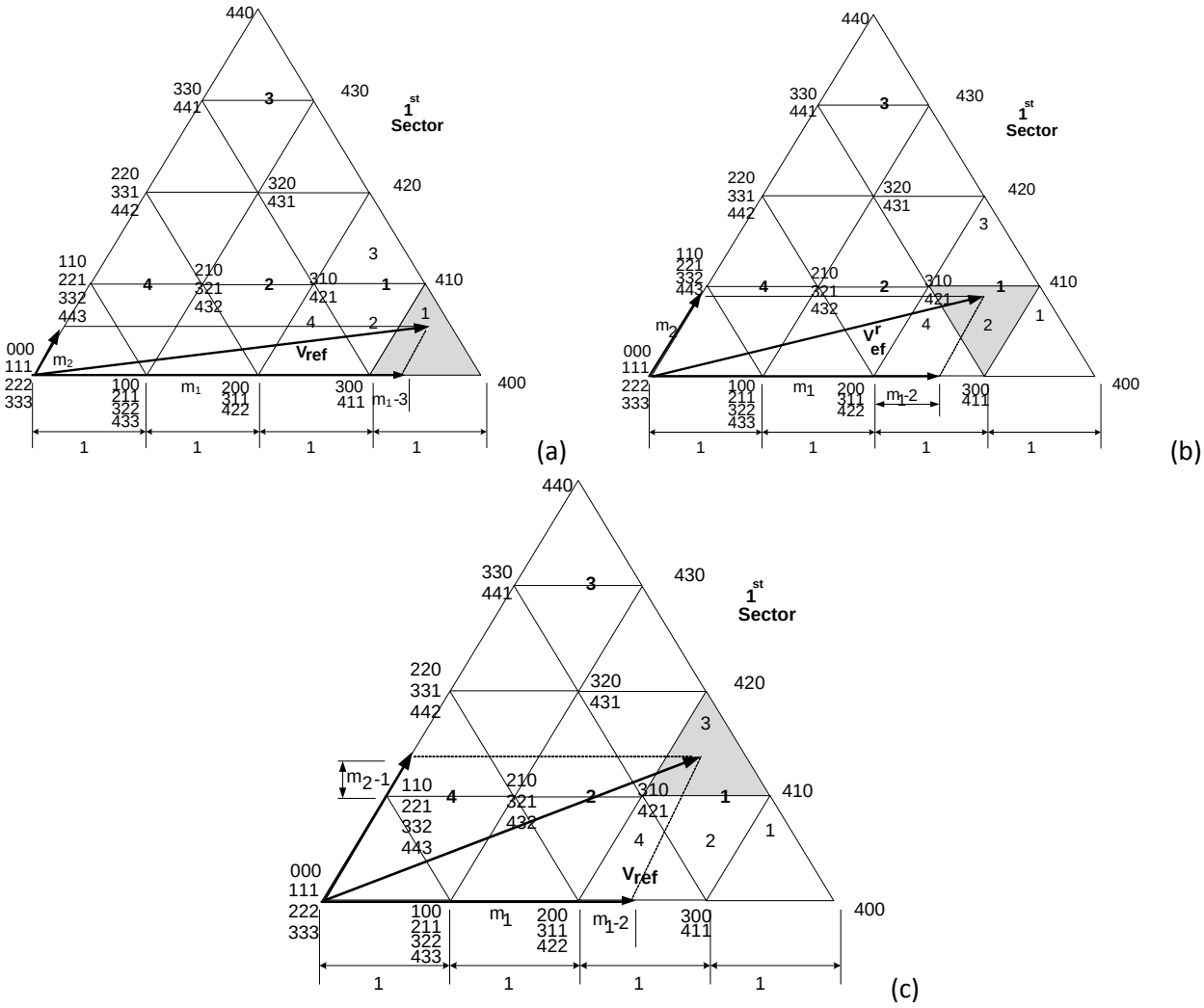


Fig. 4.4 Projection in triangle 1, regions 1, 2, and 3

Table 4.1 summarizes the conditions needed to ascertain the large triangle where the tip of the reference vector lies.

TABLE 4.1 Summery of conditions of regions and triangles of vectors in the first sector

Large triangle	Condition	Region	condition
1	$m_1>2$	1	$m_1>3$
		2	$m_1 \leq 3$ & $m_2 \leq 1$ & $m_1 + m_2 >3$
		3	$m_2 >1$
		4	$m_1 \leq 3$ & $m_2 \leq 1$ & $m_1 + m_2 \leq 3$
2	$m_1 \leq 2$ $m_2 \leq 2$ $m_1+m_2 >2$	1	$m_1 \leq 1$
		2	$m_1>1$ & $m_2 >1$ & $m_1 + m_2 \leq 3$
		3	$m_2 \leq 1$
		4	$m_1>1$ & $m_2 >1$ & $m_1+ m_2 > 3$
3	$m_2 >2$	1	$m_1>1$
		2	$m_1 \leq 1$ & $m_2 \leq 3$ & $m_1 + m_2 >3$
		3	$m_2 >3$
		4	$m_1 \leq 1$ & $m_2 \leq 3$ & $m_1 + m_2 \leq 3$
4	$m_1 \leq 2$ $m_2 \leq 2$ $m_1+m_2 \leq 2$	1	$m_1>1$
		2	$m_1 \leq 1$ & $m_2 \leq 3$ & $m_1 + m_2 >1$
		3	$m_2 >1$
		4	$m_1 \leq 1$ & $m_2 \leq 1$ & $m_1+ m_2 \leq 1$

4.1.2 Calculation of the duty cycle

In Fig. 4.5, the theoretical maximum length for the reference vector (V_{ref}) is four-unity value; nevertheless its length is limited to $2\sqrt{3}$ to ensure operation in the linear range. If the length of the reference vector is larger than $2\sqrt{3}$, over-modulation is produced.

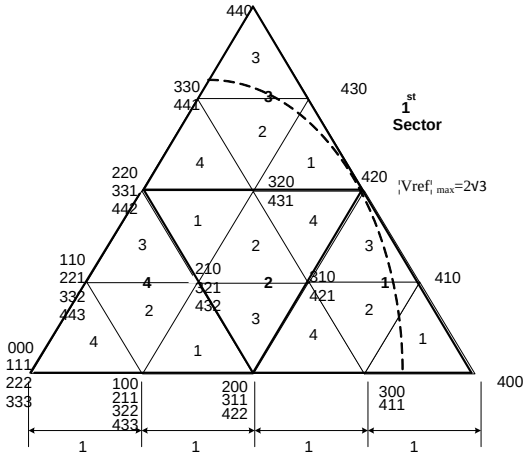


Fig. 4.5 Maximum amplitude of the normalized reference vector

According to the general method described in section 3.3.2, the components m_1 and m_2 describe the duty cycles of the vectors. For example in Fig 4.4a, the tip of the normalized reference vector lies in region 1 of large triangle 1. Therefore, the duty cycles for this region are as follows.

$$D_{400} = m_1 - 3$$

$$D_{410} = m_2 \qquad (4.1)$$

$$D_{300,411} = 4 - m_1 - m_2$$

Fig 4.4 (b), shows the case that the tip of the reference vector lies in Region 2 of big triangle 1. The duty cycles for this region are as follows.

$$D_{310,421} = 3 - m_1$$

$$D_{300,411} = 1 - m_2 \qquad (4.2)$$

$D_{410} = m_1 + m_2 - 3$

Table 4.2 shows the duty cycles for the vectors in all the regions of every single of four triangles.

TABLE 4.2 Triangles and regions of the vectors in first sectors

Large triangle	Region	Duty cycles
1	1	$D_{400} = m_1 - 3$ $D_{410} = m_2$ $D_{300,411} = 4 - (m_1 + m_2)$
	2	$D_{300,411} = 1 - m_2$ $D_{310,421} = 3 - m_1$ $D_{410} = m_1 + m_2 - 3$
	3	$D_{410} = m_1 - 2$ $D_{420} = m_2 - 1$ $D_{310,421} = 4 - (m_1 + m_2)$
	4	$D_{300,411} = m_1 - 2$ $D_{310,421} = m_2$ $D_{200,311,422} = 3 - (m_1 + m_2)$
2	1	$D_{210,321,432} = 2 - m_2$ $D_{220,331,442} = 1 - m_1$ $D_{320,431} = (m_1 + m_2) - 2$
	2	$D_{310,421} = m_1 - 1$ $D_{320,431} = m_2 - 1$ $D_{210,321,432} = 3 - (m_1 + m_2)$
	3	$D_{200,311,422} = 1 - m_2$ $D_{210,321,432} = 2 - m_1$ $D_{310,421} = (m_1 + m_2) - 2$
	4	$D_{310,421} = 2 - m_2$

		$D_{320,431} = 2 - m_1$ $D_{420} = (m_1 + m_2) - 3$
3	1	$D_{420} = m_1 - 1$ $D_{430} = m_2 - 2$ $D_{320,431} = 2 - (m_1 + m_2)$
	2	$D_{320,431} = 3 - m_2$ $D_{330,441} = 1 - m_1$ $D_{430} = m_1 + m_2 - 3$
	3	$D_{430} = m_1$ $D_{440} = m_2 - 3$ $D_{330,441} = 4 - (m_1 + m_2)$
	4	$D_{320,431} = m_1$ $D_{330,441} = m_2 - 2$ $D_{220,331,442} = 3 - (m_1 + m_2)$
4	1	$D_{200,311,422} = m_1 - 1$ $D_{210,321,432} = m_2$ $D_{100,211,322,433} = 2 - (m_1 + m_2)$
	2	$D_{100,211,322,433} = 1 - m_2$ $D_{110,221,332,443} = 1 - m_1$ $D_{210,321,432} = m_1 + m_2 - 1$
	3	$D_{210,321,432} = m_1$ $D_{220,331,442} = m_2 - 1$ $D_{110,221,332,443} = 2 - (m_1 + m_2)$
	4	$D_{100,211,322,433} = m_1$ $D_{110,221,332,443} = m_2$ $D_{000,111,222,333,444} = 1 - (m_1 + m_2)$

4.1.3 Extending the calculation for all sectors

Since all the calculations for the SVM algorithm have been done only for the first sector, the next step is applying the equations to the other sectors. According to the symmetry of all six sectors, these calculations can be applied for other sectors using only minor adjustments. It can be performed by simply interchanging the states of the output phases.

For example, as shown in Fig. 4.6a the tip of the normalized reference vector lies within the shaded triangle in sector 3. Fig. 4.6a illustrates that the adjacent switching states of the reference voltage in sector 3 are (020, 131, 242), (031, 142), and (030, 141). Mapping this shaded triangle in sector 3 to sector 1 results in another shaded triangle in sector 1. As shown in Fig. 4.6 (b) adjacent mapped switching states in sector 1 are (200, 311, 422), (310, 421), and (300, 411). Based on both adjacent switching states of V_{ref} and corresponding switching state in sector 1, we can detect the following relation:

Sector* 3:* (020, 131, 242), (031, 142), (030, 141),

↕ ↕ ↕ ↕ ↕ ↕ ↕

Sector* 1:* (200, 311, 422), (310, 421), (300, 411)

As explained before the switching state (xyz) shows the state of phase-a, phase-b, and phase-c respectively (abc). Therefore, each switching state of sector 1 (abc) corresponds to voltages v_a, v_b, and v_c. Then its equivalent switching pattern in sector 3 can be easily deduced by interchanging the order of switching state to v_c, v_a, and v_b, .i.e. (cab). The relationship between switching states indicates that based on switching states for sector 1, by interchanging the output states, the switching states for sector 3 can be deduced. For instance for switching states (200) in sector 1, switching states (020) in sector 3 can be deduced by interchanging phase-a to phase-b,

phase-b to phase-c, and phase-c to phase-a. Similarly this rule can be applied to switching state (421) in sector 1, to deduce its equivalent switching state in sector 3 as (142).

This relation is valid for all corresponding switching in sector 1 and sector 3.

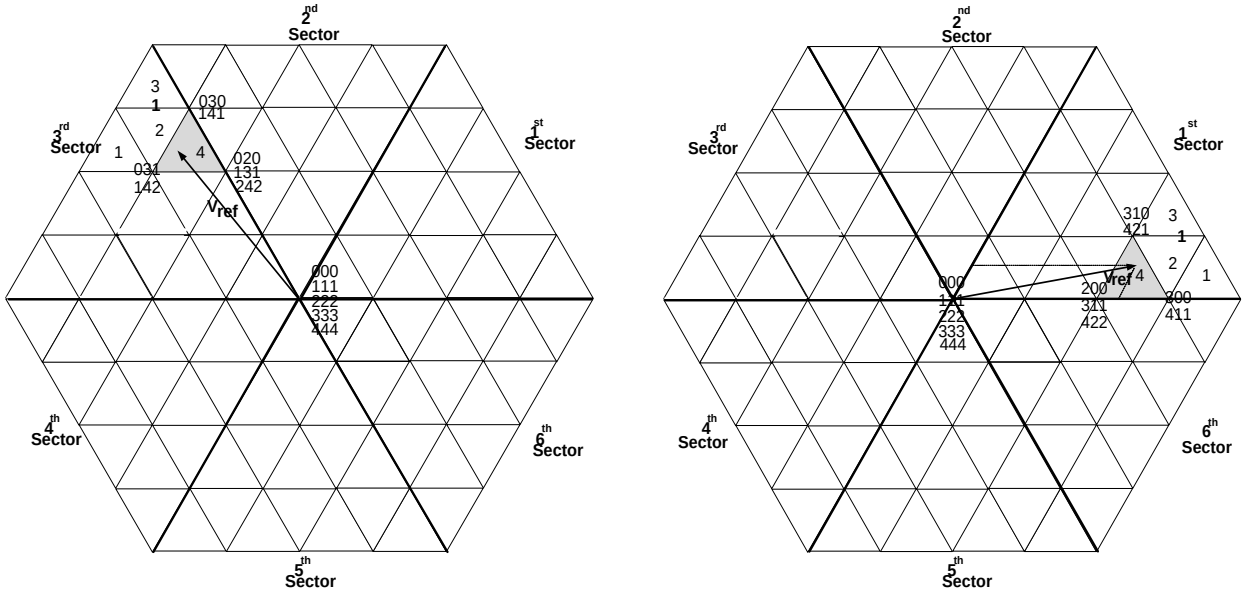


Fig. 4.6 Adjacent switching states of V_{ref} (a) in sector 3, (b) in sector 1

The visual inspection implies that this relationship between the switching states of sector 1 and sector 3 also exists between the switching state of sector 1 and the other sectors. Table 4.3 shows the interchanges of the output states between first sector and other sextants. It should be noted that the sequence of the vectors obtained in the other sectors maintains the same switching frequencies that are defined in the first sector.

TABLE 4.3 Interchanging the output states between sextants

1st sector	2nd sector	3rd sector	4th sector	5th sector	6th sector
a	a → b	a → b	a → c	a → c	a
b	b → a	b → c	b	b → a	b → c
c	c	c → a	c → a	c → b	c → b

4.1.4 Developed Model and Simulated Result

In this section, a digital model of an SVM modulated for a five-level voltage source converter is presented. Digital implementation and SVM testing are conducted in the simulation program PSCAD/EMTDC [69].

Phase angle and normalized magnitude (modulation index) of the voltage reference vector, and sampling frequency are the controllable factors of the output waveforms. Fig 4.7 shows the PSCAD component for a five-level voltage source converter.

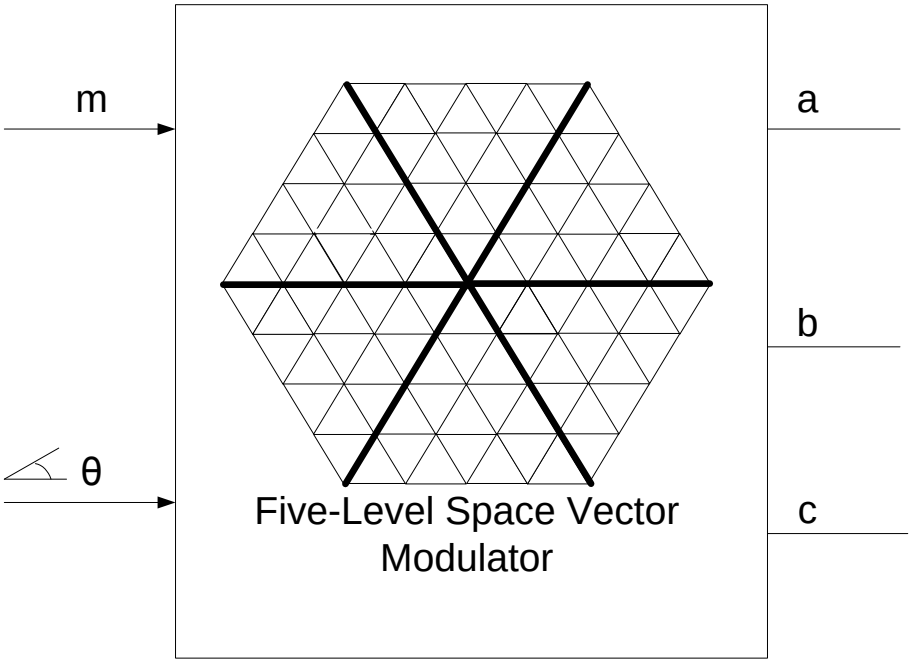
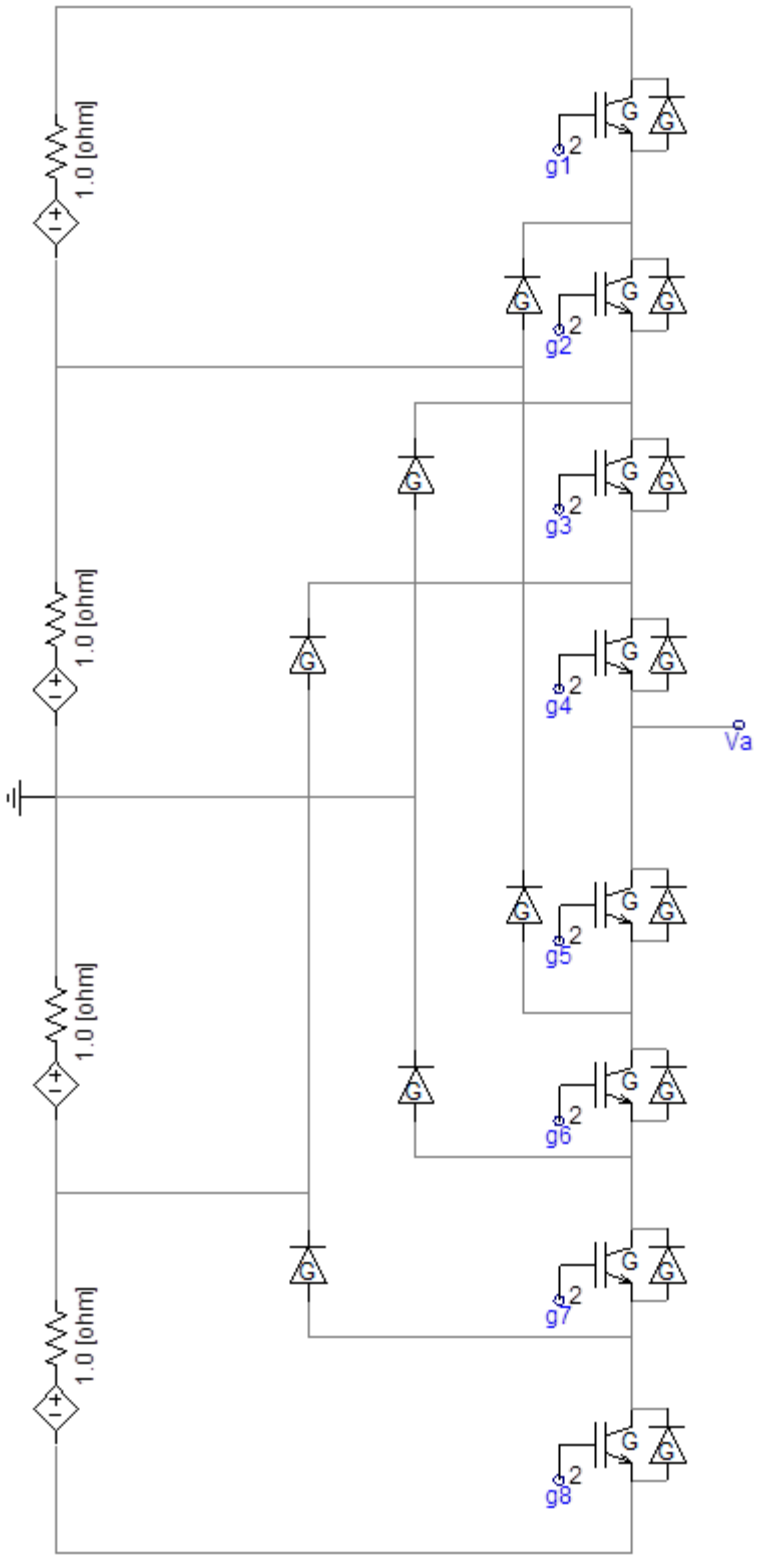
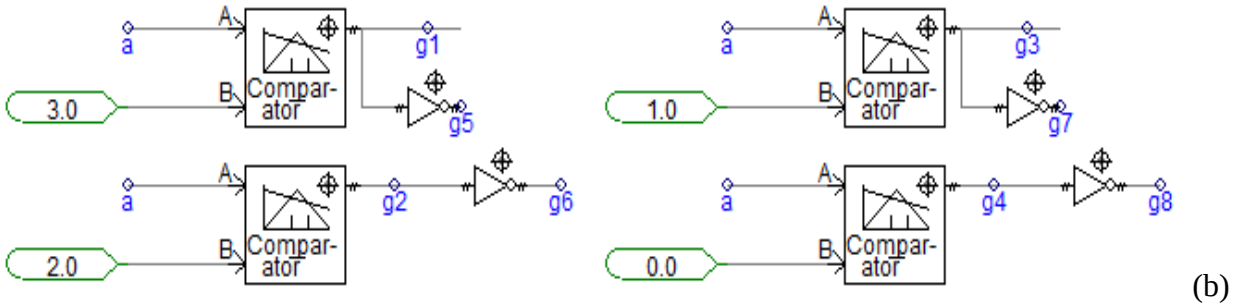


Fig. 4.7 Developed five-level SVM in PSCAD

Output signals of this component are the reference waveforms that are used to generate the gating signals for the phase-a, phase-b, and phase-c of the converter, respectively. For example, in order to generate the gating signals for phase-a (Fig. 4.8a, g1 to g8), the output signal is compared with some constant values (Fig. 4.8b). Fig 4.8a also shows the diode-clamped VSC.



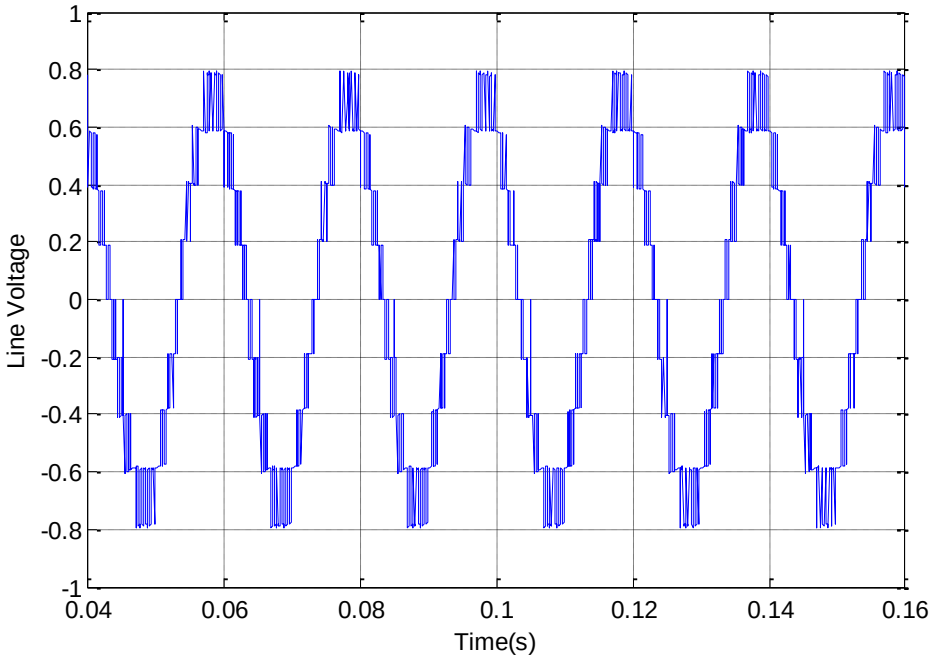
(a



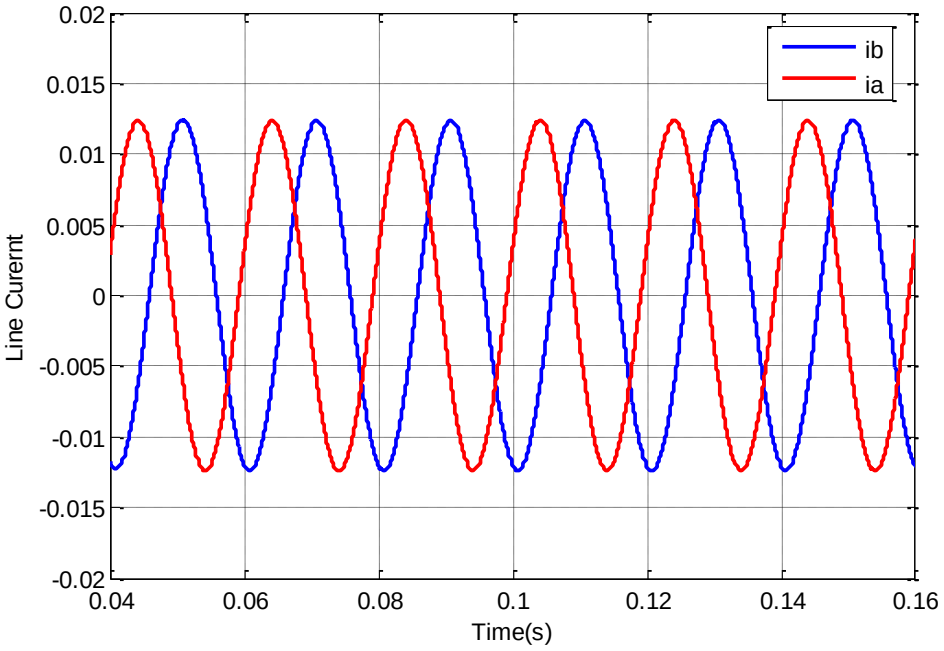
(b)

Fig. 4.8 (a) Five-level VSC model in PSCAD, (b) Generation the gate signal for phase-a

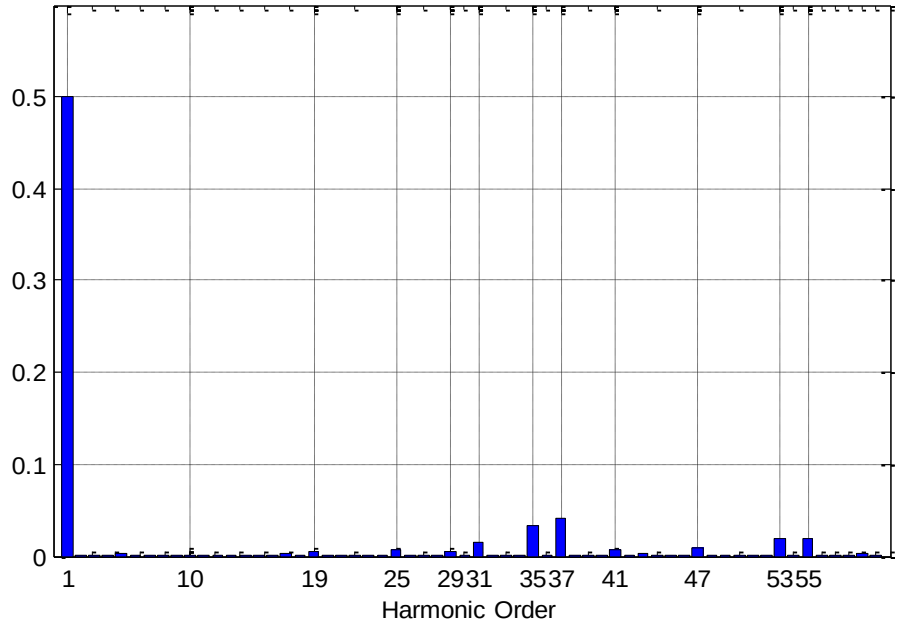
The simulation results of a five-level DCC for different values of modulation index at the normalized sampling frequency F_{sn} of 36 and dc-link of 800 V are presented in Figs 4.9 to 4.11. Fig. 4.9a and Fig. 4.9b show the line voltage and line current of the ac side for m=0.9. In Fig. 4.9b, since the load is inductive, higher order harmonics of the current are reduced by the load and the current waveform is nearly sinusoidal. As shown in Fig. 4.9c, the first group of the harmonic components is centered around the 36th harmonic.



(a)



(b)



(c)

Fig. 4.9 AC side (a) line voltage, (b) line current (c) harmonic order of a five-level DCC; m= 0.9, F_{sn} = 36

Two other graphs, Figs. 4.10 and 4.11, show the ac side voltage and current waveforms of a five-level DCC for m=0.4 and m=0.6, respectively. As seen, by decreasing the modulation index m, the magnitude of the line voltage will be decreased and also the shape of the waveform is less similar to sinusoidal shape. However, because the load still has an inductive nature, the higher order harmonics of the current are filtered and the current output waveform is still sinusoidal in its general shape. In Fig 4.10, because the modulation index is low, i.e. m=0.4, the five-level converter acts similar to a three-level converter (Fig. 3.15).

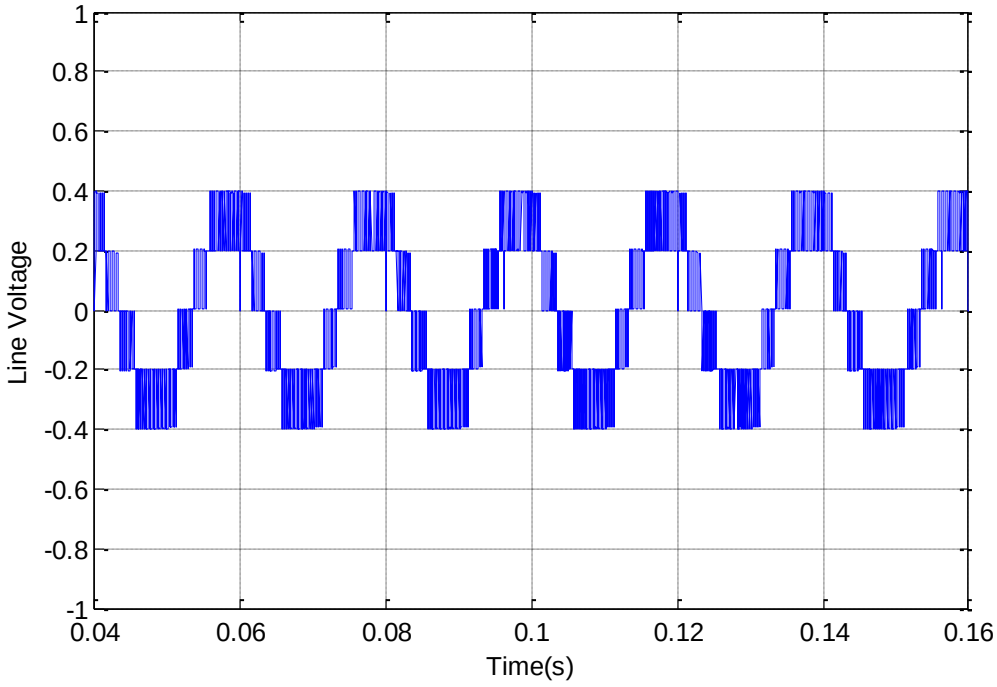
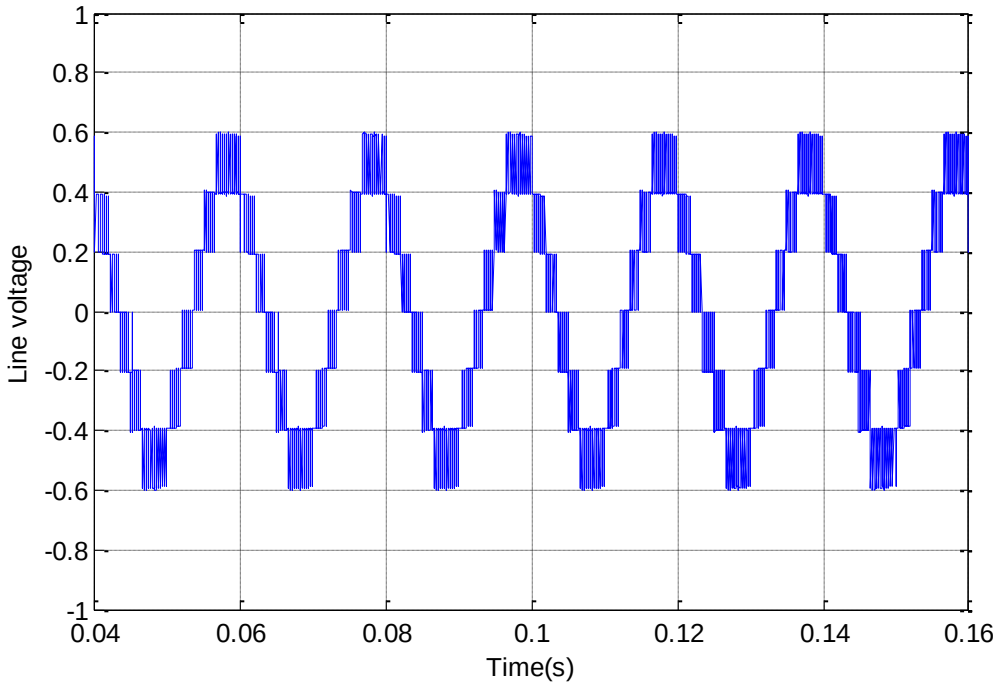
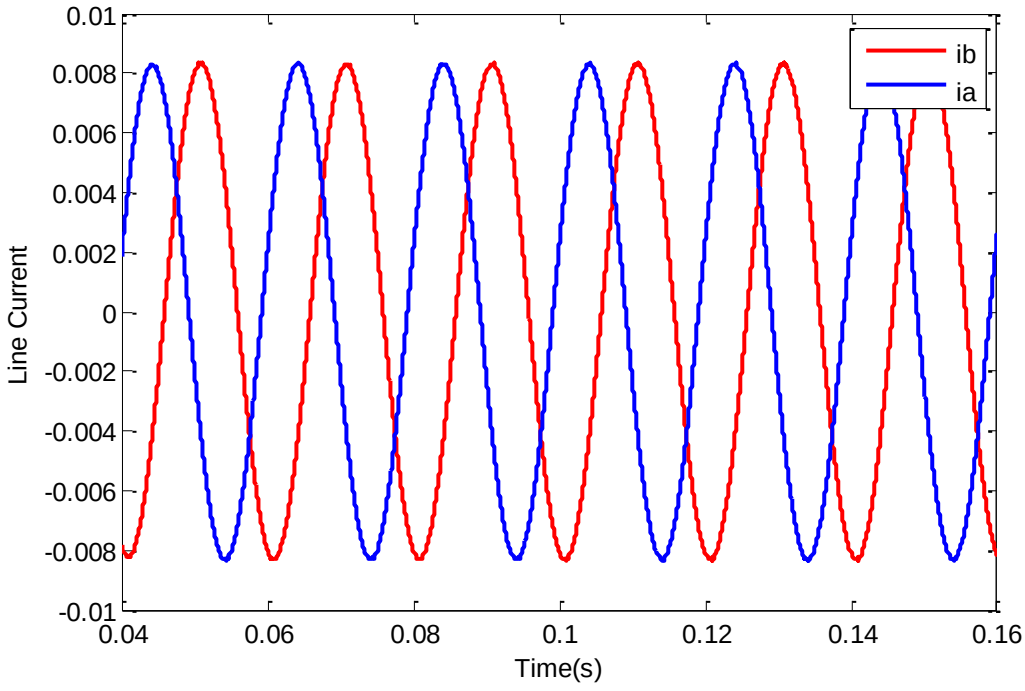


Fig. 4.10 AC side voltage waveform of a five-level DCC; m = 0.4, F_{sn} = 36



(a)



(b)

Fig. 4.11 Ac side(a)voltage waveform, (b)current waveform of a five-level DCC; m= 0.6, F_{sn}=36

Chapter 5

Balancing Techniques for *N*-Level Converters

A voltage balancing criterion for selecting the redundant vectors is explained in this section. Although this method has been proposed earlier, in the existing body of literature it is not clearly described and also there is not enough evidence that verifies this method for all the conditions. This chapter explains the balancing method in detail first and then applies it to a three-level diode clamped converter.

In an *N*-level diode clamped converter (DCC), the total electrical energy stored in (*N*-1) dc capacitors is as follows.

$$E = \frac{1}{2} C \sum_{k=1}^{n-1} V_{C_k}{}^2 \tag{5.1}$$

where

$$\sum_{k=1}^{n-1} V_{C_k} = V_{dc} \tag{5.2}$$

and V_{C_k} is the voltage across the k-th capacitor. The assumption is all the capacitors (C) are identical and have the same capacitance, i.e. $C_1 = C_2 = \ldots = C_{n-1} = C$. The total energy E reaches its minimum when all the capacitors have the reference voltage V_{dc}/n-1. Therefore, to achieve voltage balancing the control system should minimize the energy E. Hence, by changing the variable from V_{C_k} to $(V_{C_k} - \frac{V_{dc}}{n-1})$, a new parameter P is defined as follows.

$$P = \frac{1}{2} C \sum_{k=1}^{n-1} \Delta V_{C_k}{}^2 \tag{5.3}$$

where, $$\Delta V_{C_k} = V_{C_k} - \frac{V_{dc}}{n-1}$$

ΔV_{C_k} is voltage deviation of capacitors. In (5.3) since both the parameters C and $\Delta V_{C_k}{}^2$ are positive, thus P always has a positive value. P can be minimized, if capacitor voltages are maintained at the reference voltage V_{dc}/n-1 [70]. In order to minimize (5.3), the mathematical condition is as follows.

$$\frac{dP}{dt} = C \sum_{k=1}^{n-1} \Delta V_{C_k} \frac{dV_{C_k}}{dt} = \sum_{k=1}^{n-1} \Delta V_{C_k} i_{C_k} \leq 0 \tag{5.4}$$

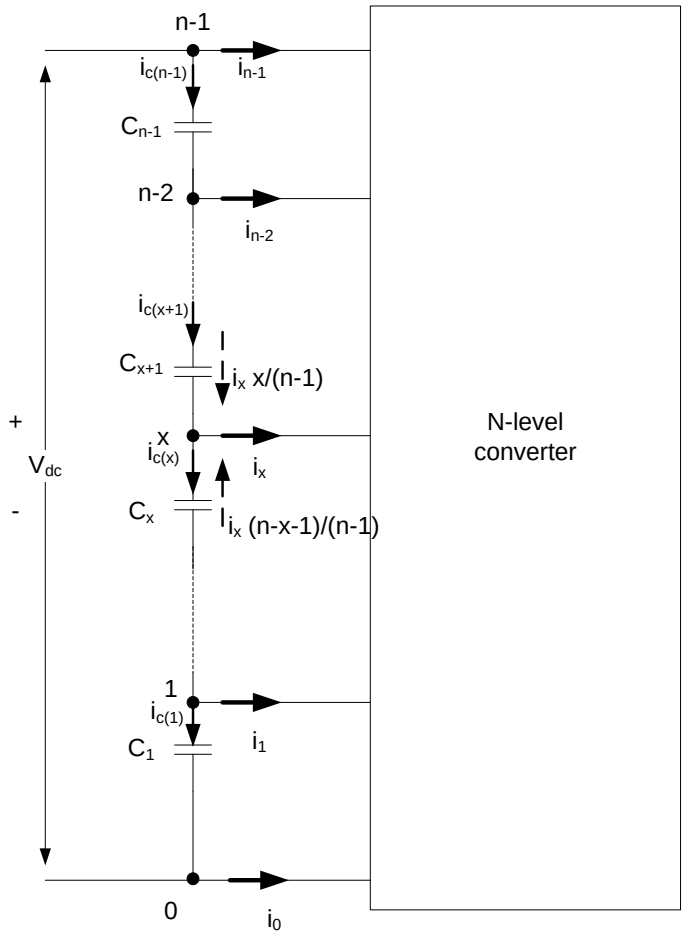


Fig. 5.1 Distribution of the branch current in the capacitors (adapted from [33])

where i_{C_k} is the current through capacitor C_k. The current in the dc link capacitors (i_{C_k}) is related to dc-side intermediate branch current (i_x). According to Fig 5.1 and considering the superposition principle, the current in the dc-link capacitors can be expressed as follows.

$$i_{C_k} = \sum_{x=1}^{k-1} \frac{x}{n-1} i_x - \sum_{x=k}^{n-2} \frac{n-x-1}{n-1} i_x \tag{5.5}$$

or

$$i_{C_k} = \frac{1}{n-1} \sum_{x=1}^{n-2} x i_x - \sum_{x=k}^{n-2} i_x \tag{5.6}$$

Substituting (5.6) into (5.4), the following balancing condition is deduced as follows.

$$\sum_{k=1}^{n-1} \Delta V_{C_k} \left(\sum_{x=1}^{n-2} x i_x - (n-1) \sum_{x=k}^{n-2} i_x \right) \leq 0 \tag{5.7}$$

imposing

$$\sum_{k=1}^{n-1} \Delta V_{C_k} = 0 \tag{5.8}$$

Replacing the voltage of capacitor $\Delta V_{C_{(n-1)}}$ from (5.8) into (5.7) the balancing condition is simplified as follows.

$$\sum_{k=1}^{n-2} \Delta V_{C_k} \left(\sum_{x=k}^{n-2} i_x \right) \geq 0 \tag{5.9}$$

By applying the averaging operator over one sampling period (T_m) to (5.9), the following equation is deduced.

$$\frac{1}{T_m} \int_{jT_m}^{(j+1)T_m} \sum_{k=1}^{n-2} \Delta V_{C_k} \left(\sum_{x=k}^{n-2} i_x \right) dt \geq 0 \tag{5.10}$$

If T_m is adequately small compared with the dynamics of capacitor voltages, then the capacitor voltages can be assumed as constant during one modulation period. Therefore, the best combination of the vectors is such that maximize the following equation.

$$\sum_{k=1}^{n-2} \Delta V_{C_k}(j) \left(\sum_{x=k}^{n-2} \frac{1}{T_m} \int_{jT_m}^{(j+1)T_m} i_x dt \right) \geq 0 \tag{5.11}$$

or

$$\sum_{k=1}^{n-2} \Delta V_{C_k}(j) \left(\sum_{x=k}^{n-2} \bar{i}_x(j) \right) \geq 0 \tag{5.12}$$

where $\Delta V_{C_k}(j)$ is the voltage deviation of capacitor C_k over the sampling period j, and $\bar{i}_x(j)$ is the average of dc-side intermediate branch current over the sampling period j. These currents can be expressed as follows.

$$\bar{i} = DSi_{ph} \tag{5.13 a}$$

where $i_{ph} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T$ (5.13 *b*)

and $S = \begin{pmatrix} S_1 + S_6 & S_2 + S_3 & S_4 + S_5 \\ S_2 + S_5 & S_1 + S_4 & S_3 + S_6 \\ S_3 + S_4 & S_5 + S_6 & S_1 + S_2 \end{pmatrix}$ (5.13 *c*)

where S_i defines the sector that the tip of the reference vector lies, such as follows.

$$S_i = \begin{cases} 1 & V_{ref} \text{ lies in the sector } i \\ 0 & V_{ref} \text{ lies in other sectors} \end{cases}$$

and in (5.13 a) D will be expressed as follows.

$$D = \begin{bmatrix} \sum\limits_{\substack{i,j,k \neq n-2 \\ i \geq j \geq k}} [d_{(n-2)jk} - d_{i(n-2)(n-2)}] & \sum\limits_{\substack{i,j,k \neq n-2 \\ i \geq j \geq k}} [d_{i(n-2)k} - d_{(n-2)j(n-2)}] & \sum\limits_{\substack{i,j,k \neq n-2 \\ i \geq j \geq k}} [d_{ij(n-2)} - d_{(n-2)(n-2)k}] \\ \vdots & \vdots & \vdots \\ \sum\limits_{\substack{i,j,k \neq 2 \\ i \geq j \geq k}} [d_{2jk} - d_{i22}] & \sum\limits_{\substack{i,j,k \neq 2 \\ i \geq j \geq k}} [d_{i2k} - d_{2j2}] & \sum\limits_{\substack{i,j,k \neq 2 \\ i \geq j \geq k}} [d_{ij2} - d_{22k}] \\ \sum\limits_{\substack{i,j,k \neq 1 \\ i \geq j \geq k}} [d_{1jk} - d_{i11}] & \sum\limits_{\substack{i,j,k \neq 1 \\ i \geq j \geq k}} [d_{i1k} - d_{1j1}] & \sum\limits_{\substack{i,j,k \neq 1 \\ i \geq j \geq k}} [d_{ij1} - d_{11k}] \end{bmatrix}$$

$$\forall i, j, k \in \{0,1,2,...,n-1\}$$

Elements of the matrix D indicate the on-duration time intervals of the switching vectors for sector1. For example D for a five-level converter can be written as follows.

$$D = \begin{bmatrix} D_{11} & D_{12} & D_{13} \\ D_{21} & D_{22} & D_{23} \\ D_{31} & D_{32} & D_{33} \end{bmatrix}$$

where

$$D_{11} = D_{300} + D_{310} + D_{320} + D_{311} + D_{321} - D_{433} + D_{322} \quad (5.14\ a)$$

$$D_{12} = D_{430} + D_{431} + D_{432} \quad (5.14\ b)$$

$$D_{13} = D_{443} - D_{330} - D_{332} - D_{331} \quad (5.14\ c)$$

$$D_{21} = - D_{422} + D_{200} + D_{210} - D_{322} + D_{211} \quad (5.14\ d)$$

$$D_{22} = D_{321} + D_{420} + D_{421} + D_{320} \quad (5.14\ e)$$

$$D_{23} = D_{432} + D_{442} - D_{220} + D_{332} - D_{221} \quad (5.14\ f)$$

$$D_{31} = - D_{411} + D_{100} - D_{211} - D_{311} \quad (5.14\ g)$$

$$D_{32} = D_{410} + D_{310} + D_{210} \quad (5.14\ h)$$

$$D_{33} = D_{421} + D_{431} + D_{441} + D_{321} + D_{331} - D_{110} + D_{221} \quad (5.14\ i)$$

5.1 Voltage balancing for a three-level converter

This section considers the performance of the modeled three-level DCC system of Fig. 5.2b.

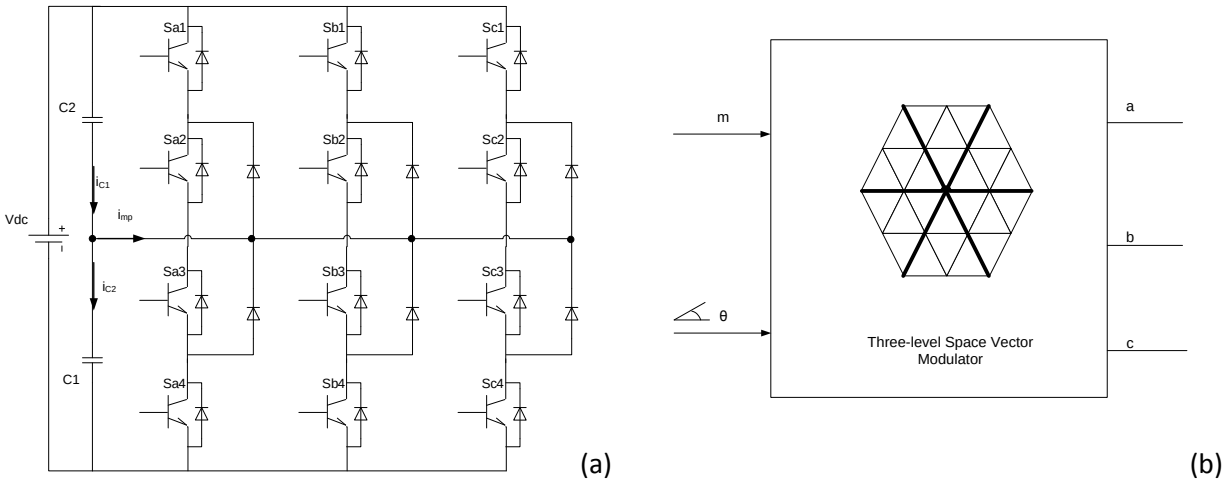


Fig. 5.2 (a) schematic of a three-level DCC, (b) modeled three-level DCC in PSCAD/EMTDC

All the voltage balancing expression in previous section can be applied to the three-level converter. In the particular case of *n*=3, cost function *P* in equation (5.3) becomes as follows.

$$P = \frac{1}{2} C \sum_{k=1}^{2} \Delta V_{C_k}{}^2 \tag{5.15}$$

where $\Delta V_{C_k} = V_{C_k} - \frac{V_{dc}}{2}$. Based on proper selection of redundant vectors, *P* can be minimized when the capacitor voltages are balanced [71]. In order to minimize (5.15), the mathematical condition is as follows.

$$\frac{dP}{dt} = C \sum_{k=1}^{2} \Delta V_{C_k} \frac{dV_{C_k}}{dt} = \sum_{k=1}^{2} \Delta V_{C_k} i_{C_k} \leq 0 \tag{5.16}$$

According to Fig. 5.2a

$$i_{c2} = i_{c1} + i_{mp} \tag{5.17}$$

Considering that $\sum_{k=1}^{2} \Delta V_{C_k} = 0$, (5.16) can be simplified as follows.

$$\Delta V_{C_1}(i_{mp}) \geq 0 \tag{5.18}$$

By applying the averaging operator and assuming that modulation period, T_m, is adequately small, the balancing condition is simplified as follows.

$$\Delta V_{C_1}(j)(\bar{i}_{mp}) \geq 0 \tag{5.19}$$

where $\Delta V_{C_1}(j)$ is the voltage deviation of capacitor C_1 at the sampling period j, and $\bar{i}_{mp}(j)$ is the average value of the mid-point current. Hence, in order to achieve the balancing condition at the dc side, the best combination of the nearest vectors to the reference vector should be checked for each sampling period.

According to expression (5.13a), in order to calculate (5.19), the average mid-point current can be evaluated as follows.

$$\bar{i}_{mp} = DSi_{ph} \tag{5.20a}$$

where

$$i_{ph} = \begin{bmatrix} i_a & i_b & i_c \end{bmatrix}^T \tag{5.20b}$$

and

$$S = \begin{pmatrix} S_1 + S_6 & S_2 + S_3 & S_4 + S_5 \\ S_2 + S_5 & S_1 + S_4 & S_3 + S_6 \\ S_3 + S_4 & S_5 + S_6 & S_1 + S_2 \end{pmatrix} \tag{5.20c}$$

and

$$D = [D_1 \quad D_2 \quad D_3] \tag{5.21}$$

D_1 and D_2 and D_3 denote the on-duration time intervals of the redundant switching voltage vectors, such as:

$$D_1 = D_{100} - D_{211} \tag{5.22a}$$

$$D_2 = D_{210} \tag{5.22b}$$

$$D_3 = D_{221} - D_{110} \tag{5.22c}$$

Elements of matrix S define the sector which in the tip of the reference vector located on, such as follows.

$$S_i = \begin{cases} 1 & V_{ref} \text{ lies in the sector } i \\ 0 & V_{ref} \text{ lies in other sectors} \end{cases}$$

Assuming that the reference vector lies in the first sector, one will have:

$$S = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

For each sampling period, based on the value of the averaged mid-point current $\bar{i}_{mp}$, which is calculated from (5.20), the equation (5.19) will be evaluated for different adjacent redundant vectors to the reference voltage vector.

5.1.1 Simulated results

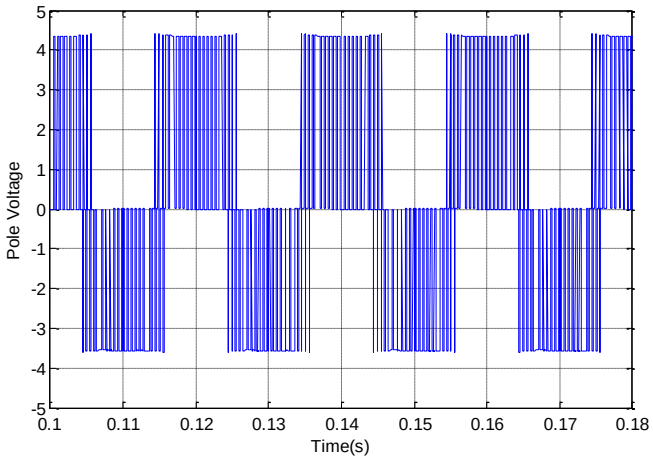
Simulated results are obtained for the three-level diode clamped converter (Fig. 5.2a) in the PSCAD/EMTDC environment. Two case studies are presented in this section. The studies are conducted to show the effectiveness of the explained capacitor voltage balancing strategy. The

first case investigates the conventional SVM strategy on a three-level converter. Line voltage and its harmonic spectrum under the inductive load are considered in this case. Capacitor voltages are also shown for different values of modulation indices.

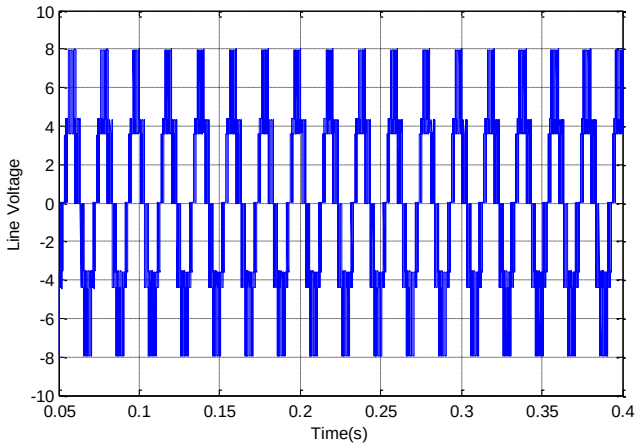
For the second case the performance of the proposed voltage balancing strategy on a three-level converter is evaluated. Capacitor voltages are considered under the same load condition. Line voltage and its harmonic are also shown in this study.

Study 1: The developed model of a three-level converter (Fig 5.2b) is used to simulate the operation at m=0.9 for two different conditions. In the first case the initial values for capacitor C_1 and C_2 are equal, and in the second case those values are different. In both cases the dc-side is supplied by a dc source V_{dc}= 8 kV and the normalized sampling frequency is kept constant at F_{sn}=36.

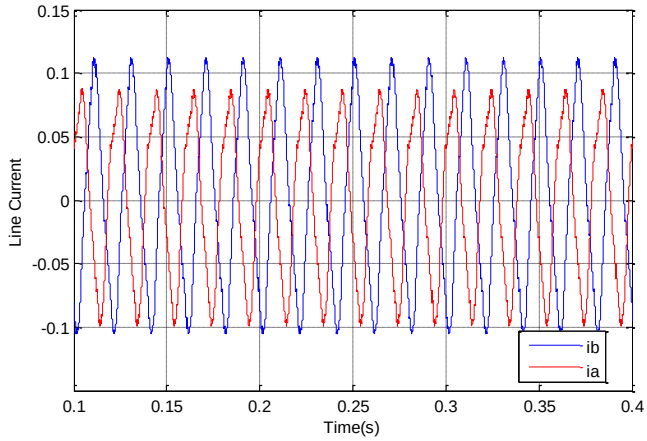
Case 1: Fig. 5.3a shows the pole voltage for m=0.9 while the initial values for both capacitor voltages are equal to 4 kV. It is evident that the pole voltage has three levels as expected, however the positive side and negative side are not symmetric, i.e. the positive side is greater than $V_{dc}/2$ and negative side is less that $V_{dc}/2$. Fig. 5.3b and Fig. 5.3c show the line voltage and phase current, respectively.



(a)



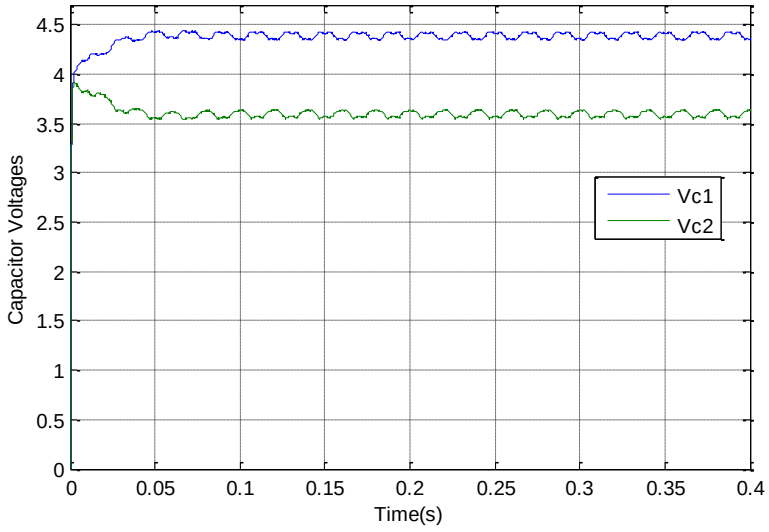
(b)



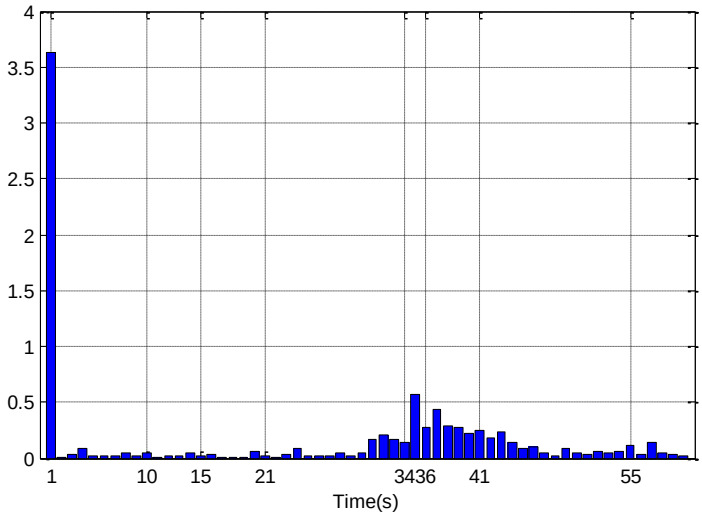
(c)

Fig. 5.3 (a)pole voltage, (b)line voltage, (c) phase current for a three-level DCC; m=0.9 and F_{sn}=36, equal capacitor voltage values

Fig. 5.4a and Fig. 5.4b show the capacitor voltages and harmonic spectrum for this case. As can be seen in Fig. 5.4a, both capacitors have the same initial values equal to 4 kV. This figure shows that if the proper combination of switching is not chosen in the conventional SVM, the capacitor voltages will be drifting. Fig 5.4b also shows that the ac-side voltage harmonic as well as the dc side capacitor voltages is influenced by the selected switching combination.



(a)

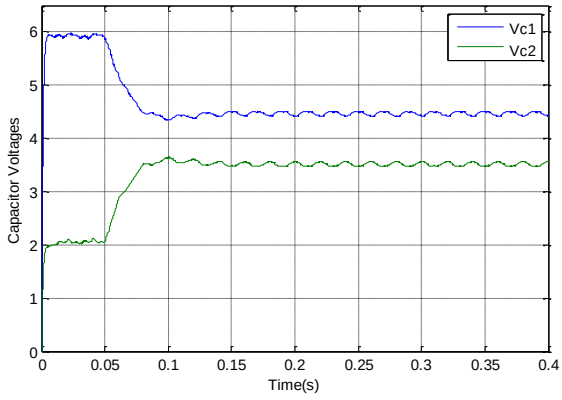


(b)

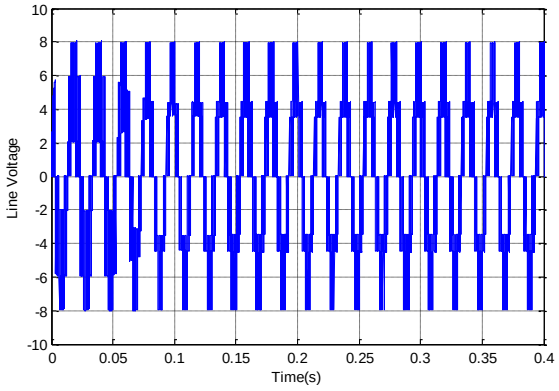
Fig. 5.4 (a)dc capacitor voltages, (b)harmonic spectrum of the ac side line voltage, for a three-level DCC; m=0.9 and F_{sn}=36

Case 2: The only different between this case and case1 is that the initial values for capacitor voltages are set to different values such as V_{C1} = 6 kV, and for V_{C2} = 2 kV. After 5 ms, both capacitor are connected to one dc source V_{dc}=8 kV. The reason of this study is to find out that if there is any imbalance in the system, whether the conventional SVM is able to solve the imbalances and bring the capacitor voltages back together or there still will be imbalances.

Fig. 5.5a shows that after 5 ms the capacitor voltages tend to be equal, but because of the switching pattern the voltages still diverge. Ideally speaking, the capacitor voltages should both stay at 4kV at the end, however obviously they drift. Fig. 5.5b shows the line voltage for this case.



(a)

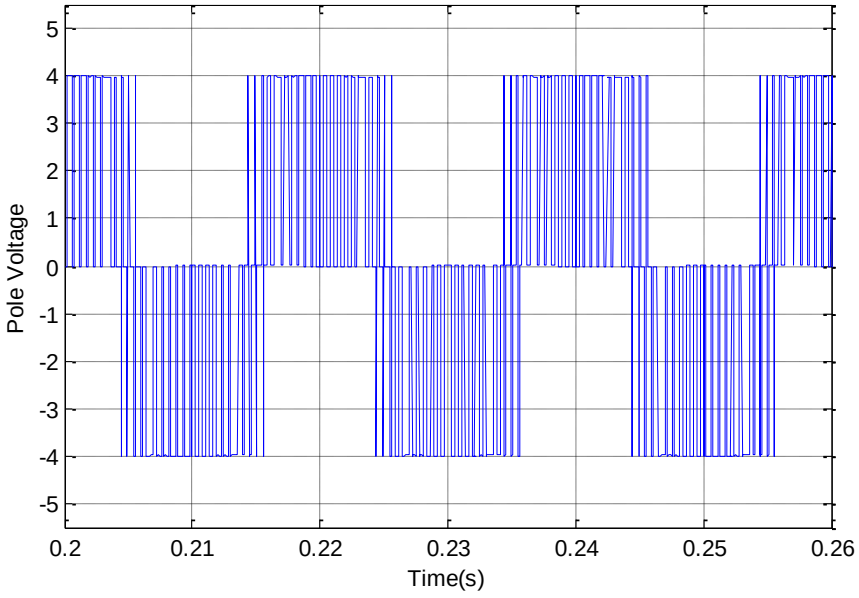


(b)

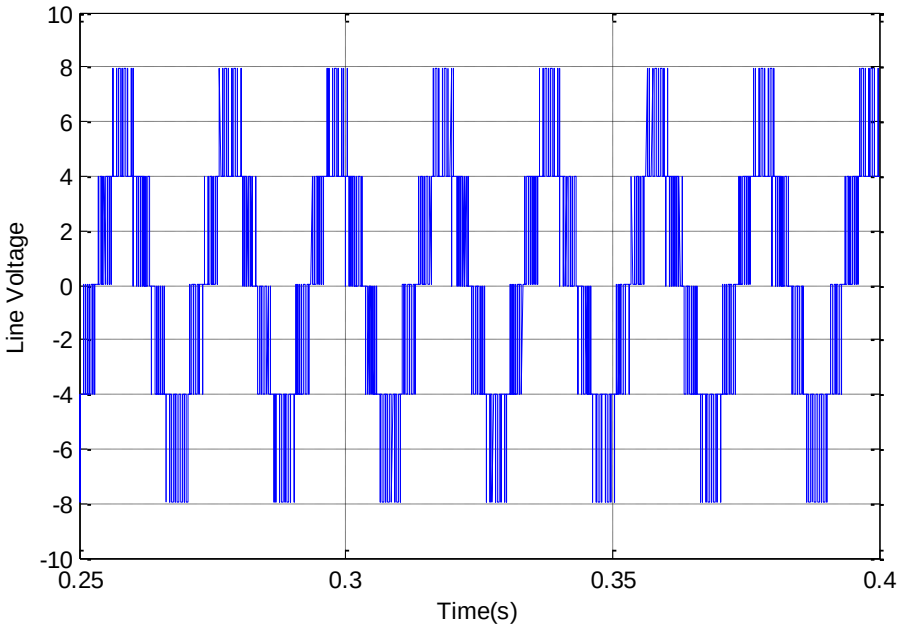
Fig. 5.5 (a) dc capacitor voltages, (b) line voltage, for a three-level DCC; m=0.9 and F_{sn}=36, unequal initial capacitor voltages

Study 2: This study shows the effectiveness of the explained voltage balancing method for a three-level converter under various conditions. In the first case, initially capacitor voltages have equal values at V_{C1}=V_{C2}= 4 kV. After 10ms, both capacitors will be connected to one dc source V_{dc}= 8 kV.

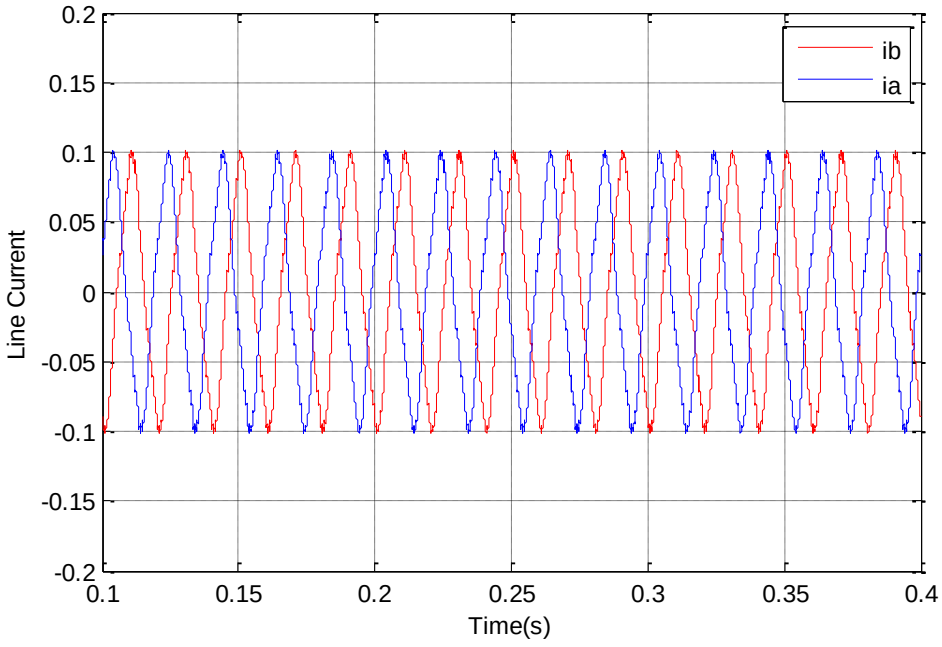
Case1: Fig. 5.6 and Fig. 5.7 show the performance of the explained voltage balancing strategy when the three-level converter operates at m=0.9. As shown in Fig. 5.6a, the pole voltage varies between $-V_{dc}/2$ and $V_{dc}/2$. Two other figures, Fig. 5.6b and Fig. 5.6c show the ac-side line voltage and ac-side current, respectively.



(a)



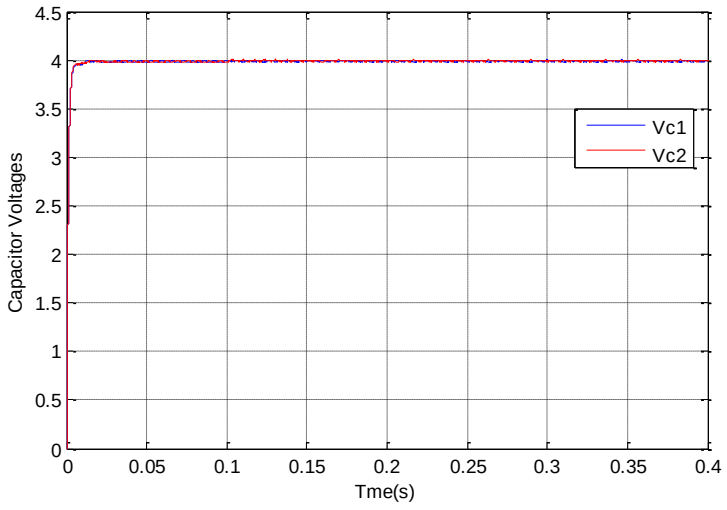
(b)



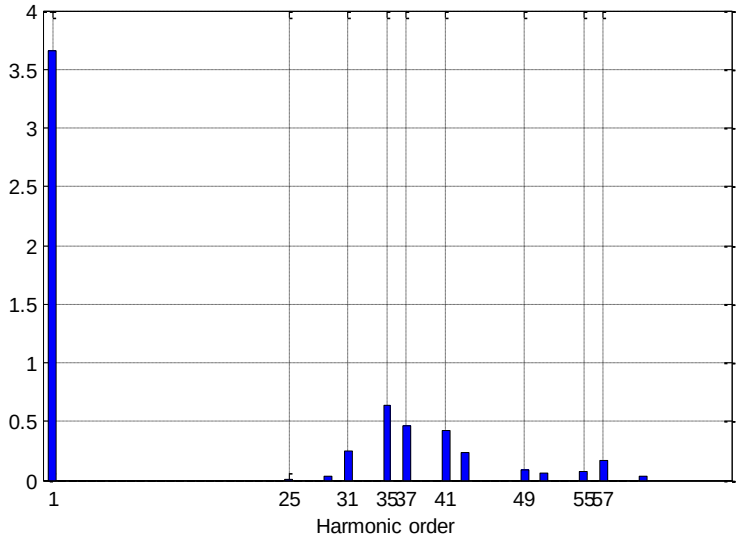
(c)

Fig. 5.6 (a)pole voltage, (b)line voltage, (c) phase current for a three-level DCC with using the voltage balancing method; m=0.9 and F_{sn}=36; equal initial capacitor voltages

Fig. 5.7a shows the capacitor voltages for this condition. As can be seen the capacitor voltages remain at their normal value, i.e. 4kV. Fig. 5.7b shows the harmonic spectrum of the ac side line voltage for this case. As shown in this figure, the first group of harmonics is shifted around the 36^{th} harmonic. It should be noted that, in contrast with the study 1 (Fig. 5.4b), in this case the 36^{th} harmonics is automatically eliminated.



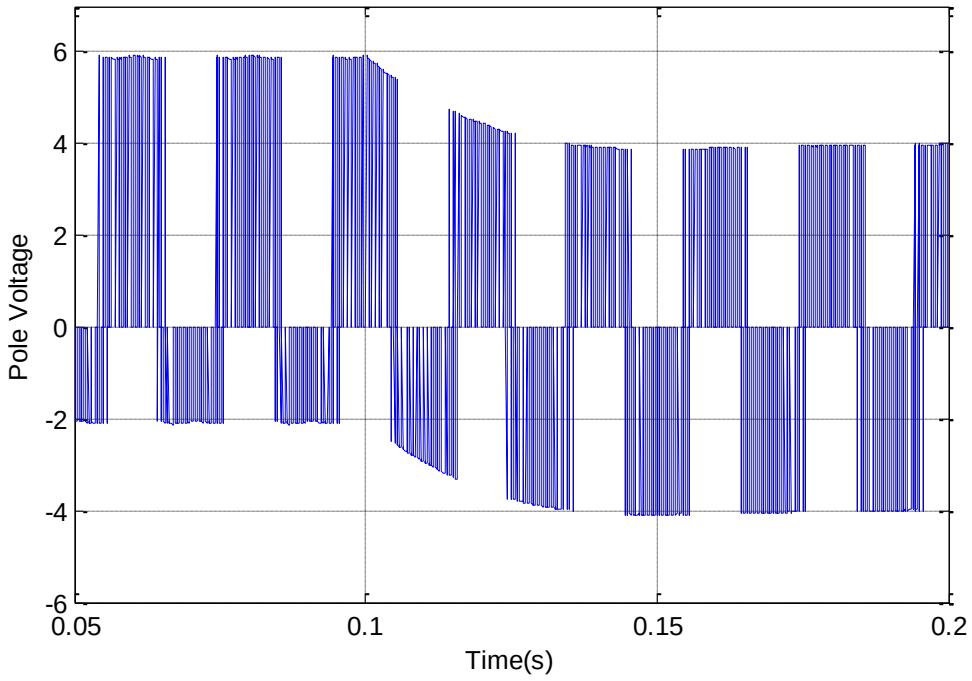
(a)



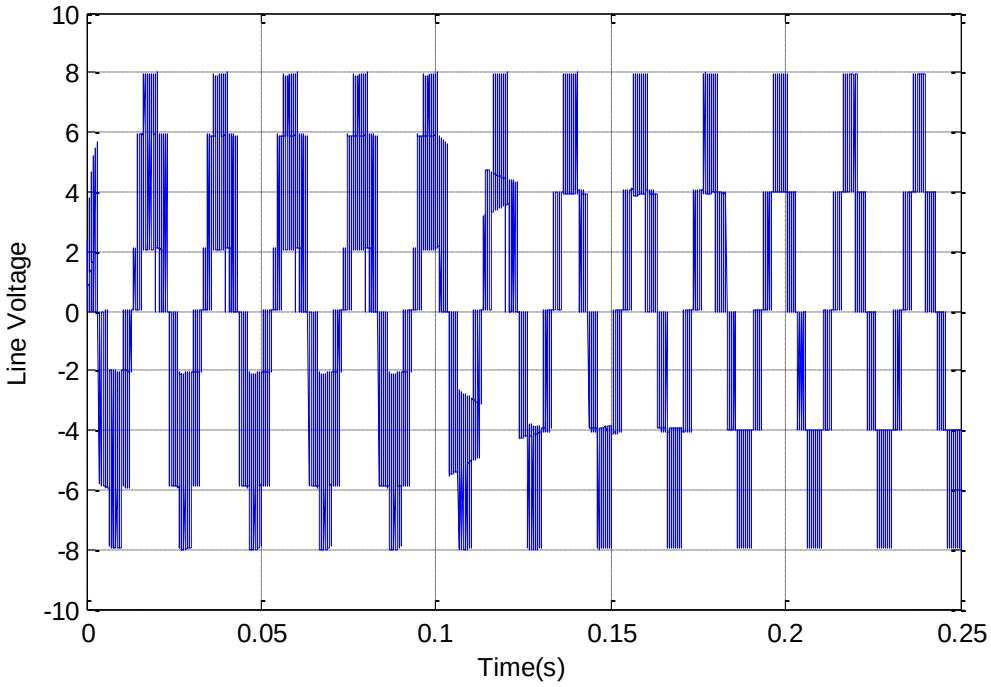
(b)

Fig. 5.7 (a) dc capacitor voltages, (b) line voltage, for a three-level DCC with using voltage balancing method; m=0.9 and F_{sn}=36; equal initial capacitor voltages

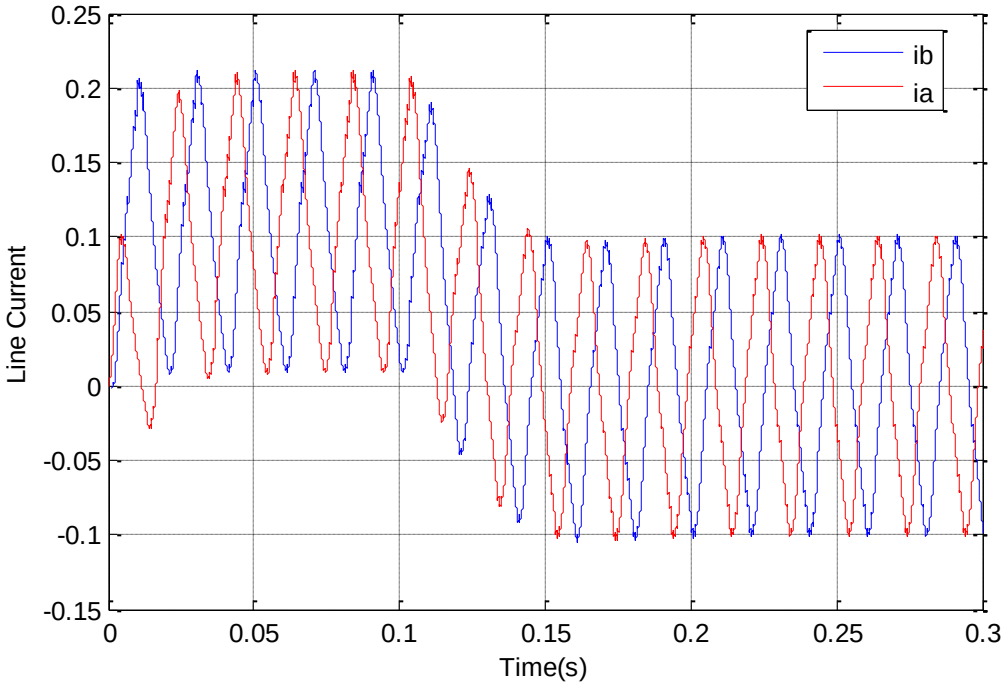
Case 2: This case illustrates the performance of the explained dc capacitor voltage balancing criteria while the three-level DCC system operates at m=0.9. Initially the DC capacitor voltages of the three-level converter have unequal values at V_{C1}=6 kV, and V_{C2}=2kV. After 10 ms both capacitors will be connected to one dc source V_{dc} =8kV. Fig. 5.8a shows the pole voltage for this condition. As can be seen, clearly it has three levels at the end. Fig. 5.8b and Fig. 5.8c also show the ac side line voltage and current, respectively.



(a)



(b)



(c)

Fig. 5.8 (a)pole voltage, (b)line voltage, (c) phase current for a three-level DCC with using the voltage balancing method; m=0.9 and F_{sn}=36; unequal initial capacitor voltages

Fig. 5.9 shows the capacitor voltages for the three-level DCC. As can be seen, capacitor voltages converge to their normal value $V_{C1} = V_{C2} = 4$ kV; however initially they have unequal voltage values.

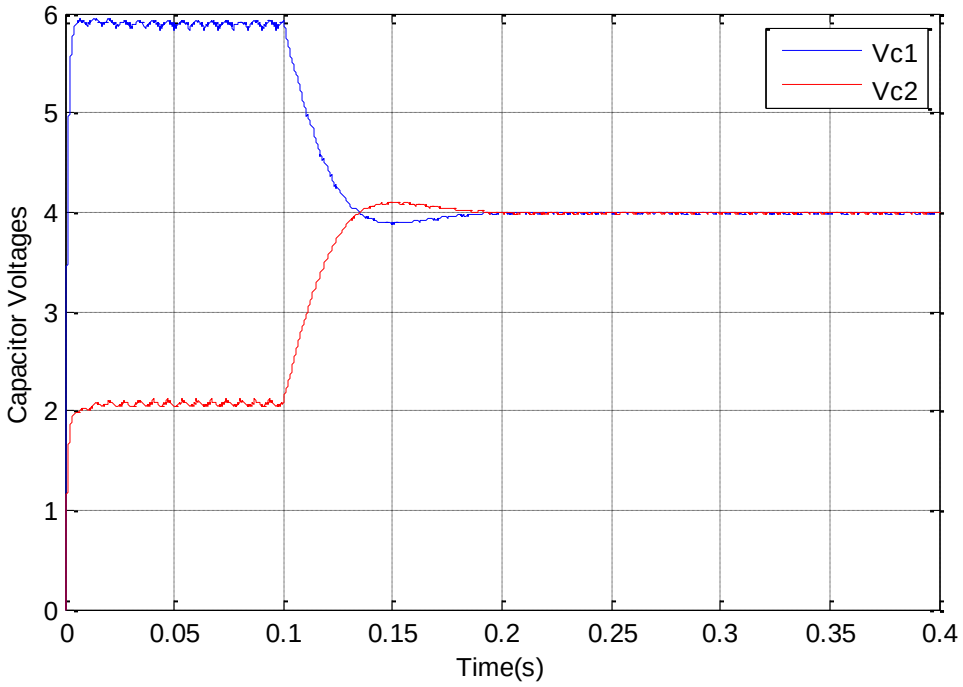


Fig. 5.9 dc capacitor voltages for a three-level DCC with using voltage balancing method; m=0.9and F_{sn}=36; unequal initial capacitor voltages

Comparing study 1 and study 2 concludes that without a proper switching pattern the DC capacitor voltages for a three-level DCC system will diverge from their desired values (Fig 5.4a and Fig. 5.5a); however by choosing proper redundant switching states based on the voltage balancing criteria the voltage drift phenomenon is counteracted.

Although the proposed balancing technique is not a new approach to overcome the dc capacitor voltage drifting phenomenon in diode clamped multi-level converters, in the literature there was not enough evidence to verify this method for all the conditions. Simulation results in this

chapter demonstrate that using this balancing condition will lead to dc capacitor voltage balancing even if the dc capacitors of the converter do or do not have the same initial voltage levels.

Chapter 6

Conclusions, Contributions and Future Work

6.1 Contributions and Conclusions

The main contributions and conclusions of the thesis are summarized below:

1. A through and comprehensive study of the different multi-level converter topologies and different modulation strategies are provided in this thesis.
2. In this thesis, an SVM model for two-level diode clamped converter is developed in the PSCAD/EMTDC transient simulation program.
3. Besides the two-level converter component, the SVM models for three-level and five-level converters have also been implemented in the PSCAD/EMTDC transient simulation program. These components are able to operate for different modulation indices as well as different sampling frequencies. For the five-level SVM, this thesis proposed a method to calculate the on-duration time intervals for switching vectors based on expanding the three-level SVM. In the new method each sector of the five-level SVM can be divided

into four large triangles instead of sixteen small triangles. Each of these large triangles is then considered as a sector of a three-level SVM.

4. In general, as the number of levels in the converter increases, consequently, the number of redundant switching states increases. This thesis has provided a dc capacitor voltage balancing method for multi-level diode clamped converters that in each sample of time selects the proper redundant switching states to solve the voltage drifting problem at the dc capacitors.
5. The dc capacitor voltage balancing method is developed for the three-level SVM. From the simulation results, it is observed that the developed method is able to equalize the dc side capacitor voltages without using any additional power circuits.
6. In this thesis, the three-level SVM is simulated for different switching strategies. Based on the simulations, it is shown that among all the switching strategies, the provided balancing method leads to better capacitor voltage balancing at the side and also better harmonic spectrum for output voltage at the ac side.

6.2 Future work

A number of additional future research topics are suggested as follows.

1. Laboratory implementation of the developed strategies for simulation verification is an important complementary task that is important to be pursued.
2. More research could be done on other types of multi-level converters than the diode clamped converter, such as flying capacitor, cascaded converter and modular multi-level converter. Their advantages and disadvantages for different power applications should be analyzed in order to find the best topologies in each case.

3. In this thesis, three-level SVM and five-level SVM have been implemented in the PSCAD/EMTDC transient simulation program in two different components. Additional work can be done in order to design a single component which operates for different converter levels.

References

[1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Transactions on Industry Applications,* pp. 518-523, 1981.

[2] S. R. Minshull, C. M. Bingham, D. A. Stone, and M. P. Foster, "Compensation of Nonlinearities in Diode-Clamped Multilevel Converters," *IEEE Transactions on Industrial Electronics,* vol. 57, pp. 2651-2658, 2010.

[3] D. Dupuis and F. Okou, "Modeling and control of a five-level Diode-Clamped Converter based StatCom," *IEEE International Conference on Industrial Technology* 2009, pp. 1-6.

[4] A. Yazdani and R. Iravani, "Dynamic model and control of the NPC-based back-to-back HVDC system," *IEEE Transactions on Power Delivery,* vol. 21, pp. 414-424, 2006.

[5] B. T. Ooi, G. Joos, and X. Huang, "Operating principles of shunt STATCOM based on 3-level diode-clamped converters," *IEEE Transactions on Power Delivery,* vol. 14, pp. 1504-1510, 1999.

[6] X. Yuan and I. Barbi, "Fundamentals of a new diode clamping multilevel inverter," *IEEE Transactions on Power Electronics,* vol. 15, pp. 711-718, 2000.

[7] M. Saeedifard, R. Iravani, and J. Pou, "Analysis and control of DC-capacitor-voltage-drift phenomenon of a passive front-end five-level converter," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 3255-3266, 2007.

[8] J. S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Transactions on Industry Applications,* vol. 32, pp. 509-517, 1996.

[9] N. Hatti, Y. Kondo, and H. Akagi, "Five-level diode-clamped PWM converters connected back-to-back for motor drives," *IEEE Transactions on Industry Applications*, vol. 44, pp. 1268-1276, 2008.

[10] F. Z. Peng, J. S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage-source converter system with balanced DC voltages," *Power Electronics Specialists Conference* 1995, pp. 1144-1150 vol. 2.

[11] Z. Pan, F. Z. Peng, K. A. Corzine, V. R. Stefanovic, J. M. Leuthen, and S. Gataric, "Voltage balancing control of diode-clamped multilevel rectifier/inverter systems," *IEEE Transactions on Industry Applications,* vol. 41, pp. 1698-1706, 2005.

[12] T. Ishida, K. Matsuse, K. Sugita, L. Huang, and K. Sasagawa, "DC voltage control strategy for a five-level converter," *IEEE Transactions on Power Electronics,* vol. 15, pp. 508-515, 2000.

[13] S. Busquets-Monge, S. Alepuz, J. Rocabert, and J. Bordonau, "Pulsewidth Modulations for the Comprehensive Capacitor Voltage Balance of n-Level Two-Leg Diode-Clamped Converters," *IEEE Transactions on Power Electronics*, vol. 24, pp. 1951-1959, 2009.

[14] M. Saeedifard, H. Nikkhajoei, and R. Iravani, "A space vector modulated STATCOM based on a three-level neutral point clamped converter," *IEEE Transactions on Power Delivery,* vol. 22, pp. 1029-1039, 2007.

[15] A. K. Gupta and A. M. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Transactions on Industrial Electronics,* vol. 53, pp. 1631-1639, 2006.

[16] M. Marchesoni and M. Mazzucchelli, "Multilevel converters for high power AC drives: A review," *IEEE International Symposium on Industrial Electronics* 1993, pp. 38-43.

[17] R. H. Baker, "Bridge converter circuit," *RH Baker, US Patent*, 1981.

[18] P. W. Hammond, "Medium voltage PWM drive and method" *PW Hammond, US Patent* 1997.

[19] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. VanCoevering, "A multilevel voltage-source inverter with separate dc sources for static var generation," *IEEE Transactions on Industry Applications*, vol. 32, pp. 1130-1138, 1996.

[20] T. Meynard, M. Fadel, and N. Aouda, "Modeling of multilevel converters,", *IEEE Transactions on Industrial Electronics* vol. 44, pp. 356-364, 1997.

[21] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications,* vol. 37, pp. 611-618, 2001.

[22] B. P. McGrath and D. G. Holmes, "Analytical modelling of voltage balance dynamics for a flying capacitor multilevel converter," *IEEE Transactions on Power Electronics,* vol. 23, pp. 543-550, 2008.

[23] M. Marchesoni and P. Tenca, "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 752-765, 2002.

[24] S. Busquets-Monge, S. Alepuz, J. Bordonau, and J. Peracaula, "Voltage balancing control of diode-clamped multilevel converters with passive front-ends," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1751-1758, 2008.

[25] A. Von Jouanne, S. Dai, and H. Zhang, "A multilevel inverter approach providing DC-link balancing, ride-through enhancement, and common-mode voltage elimination," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 739-745, 2002.

[26] K. A. Corzine and X. Kou, "Capacitor voltage balancing in full binary combination schema flying capacitor multilevel inverters," *IEEE Power Electronics Letters,* vol. 1, pp. 2-5, 2003.

[27] F. Zhang, F. Z. Peng, and Z. Qian, "Study of the multilevel converters in DC-DC applications," *Power Electronics Specialists Conference*, 2004, pp. 1702-1706 Vol. 2.

[28] L. M. Tolbert and F. Z. Peng, "Multilevel converters as a utility interface for renewable energy systems," IEEE *Power Engineering Society* 2000, pp. 1271-1274 vol. 2.

[29] T. A. Meynard and H. Foch, "Multilevel converters and derived topologies for high power conversion," *IEEE IECON 21st International Conference on Industrial Electronics,* 1995, pp. 21-26 vol. 1.

[30] B. Mwinyiwiwa, Z. Wolanski, B. T. Ooi, and Y. Chen, "Multilevel converters as series VAr compensators," IEEE *Power Electronics Specialists Conference* 1997, pp. 338-343 vol. 1.

[31] M. Saeedifard, A. Bakhshai, and G. Joos, "Low switching frequency space vector modulators for high power multimodule converters," *IEEE Transactions on Power Electronics,* vol. 20, pp. 1310-1318, 2005.

[32] N. S. Choi, J. G. Cho, and G. H. Cho, "A general circuit topology of multilevel inverter," *Power Electronics Specialists Conference*, 1991, pp. 96-103.

[33] J. Pou Fèlix, "Modulation and control of three-phase PWM multilevel converters," 2002.

[34] M. Marchesoni and P. Tenca, "Theoretical and practical limits in multilevel MPC inverters with passive front ends," *European Conference on Power Electronics and Applications,* 2001, pp. 1–12.

[35] T. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters" *IEEE Power Electronics Specialists Conference* 1992, pp. 397-403 vol. 1.

[36] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE journal,* vol. 2, pp. 45-50, 1992.

[37] G. Sinha and T. A. Lipo, "A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters," *International Conference on Industrial Electronics,* 1997, pp. 670-675 vol. 2.

[38] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," *IEEE Transactions on Industry Applications,* vol. 35, pp. 36-44, 1999.

[39] S. Khomfoi and L. M. Tolbert, "Multilevel power converters," *Power Electronics Handbook,* 2006.

[40] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non conventional power converter for plasma stabilization," *IEEE Power Electronics Specialists Conference* 1988, pp. 122-129 vol. 1.

[41] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," *In Proc EPE France,* 2003.

[42] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Transactions on Industrial Electronics,* vol. 52, pp. 662-669, 2005.

[43] M. Glinka and R. Marquardt, "A New Single Phase AC/AC–Multilevel Converter for Traction Vehicles Operating on AC Line Voltage," *In Proc EPE France,* 2003.

[44] R. Marquardt, "Stromrichterschaltungen mit verteilten Energiespeichern," *German Patent DE,* vol. 10, p. 031.

[45] *Introduction Into* HVDC PLUS, Siemens AG, Berlin, Germany, 2008.[Online]. Available: https://www.energy-portal.siemens.com

[46] M. Hagiwara and H. Akagi, "PWM control and experiment of modular multilevel converters," *IEEE Power Electronics Specialists Conference* 2008, pp. 154-161.

[47] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," *Power Tech Conference Proceedings* 2003, p. 6 pp. Vol. 3.

[48] J. Holtz, "Pulsewidth modulation-a survey," *IEEE Transactions on Industrial Electronics,* vol. 39, pp. 410-420, 1992.

[49] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proceedings of the IEEE,* vol. 82, pp. 1194-1214, 1994.

[50] S. R. Bowes and D. Holliday, "Optimal regular-sampled PWM inverter control techniques," *IEEE Transactions on Industrial Electronics,* vol. 54, pp. 1547-1559, 2007.

[51] M. Manjrekar and G. Venkataramanan, "Advanced topologies and modulation strategies for multilevel inverters," *IEEE Power Electronics Specialists Conference*, 1996, pp. 1013-1018 vol. 2.

[52] B. S. Suh, G. Sinha, M. D. Manjrekar, and T. A. Lipo, "Multilevel power conversion-an overview of topologies and modulation strategies," *Proceedings of the 6th International*

Conference on Optimization of Electrical and Electronic Equipments, 1998, pp. AD-11-AD-24.

[53] L. M. Tolbert and T. G. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Transactions on Industry Applications,* vol. 35, pp. 1098-1107, 1999.

[54] A. A. Notes, "Implementing Space Vector Modulation With ADMC401 AN401-17," *Analog Devices, Jan,* 2000.

[55] T. Instruments, "Clarke & Park Transforms on the TMS320C2xx," *Application Report BPRA,* vol. 48.

[56] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Transactions on Power Electronics,* vol. 15, pp. 242-249, 2000.

[57] A. K. Gupta and A. M. Khambadkone, "A general space vector PWM algorithm for multilevel inverters, including operation in overmodulation range," *IEEE Transactions on Power Electronics,* vol. 22, pp. 517-526, 2007.

[58] A. K. Gupta and A. M. Khambadkone, "A simple space vector pwm scheme to operate a three-level npc inverter at high modulation index including overmodulation region, with neutral point balancing," *IEEE Transactions on Industry Applications,* vol. 43, pp. 751-760, 2007.

[59] G. Narayanan and V. Ranganathan, "Extension of operation of space vector PWM strategies with low switching frequencies using different overmodulation algorithms," *IEEE Transactions on Power Electronics,* vol. 17, pp. 788-798, 2002.

[60] H. J. Park and M. J. Youn, "A new time-domain discontinuous space-vector PWM technique in overmodulation region," *IEEE Transactions on Industrial Electronics,* vol. 50, pp. 349-355, 2003.

[61] A. Tripathi, A. M. Khambadkone, and S. Panda, "Direct method of overmodulation with integrated closed loop stator flux vector control," *IEEE Transactions on Power Electronics,* vol. 20, pp. 1161-1168, 2005.

[62] D. C. Lee and G. M. Lee, "A novel overmodulation technique for space-vector PWM inverters," *IEEE Transactions on Power Electronics,* vol. 13, pp. 1144-1151, 1998.

[63] S. K. Mondal, B. K. Bose, V. Oleschuk, and J. O. P. Pinto, "Space vector pulse width modulation of three-level inverter extending operation into overmodulation region," *IEEE Transactions on Power Electronics,* vol. 18, pp. 604-611, 2003.

[64] A. M. Hava, "Carrier based PWM-VSI drives in the overmodulation region," *University of Wisconsin,* 1998.

[65] A. M. Hava, R. J. Kerkman, and T. A. Lipo, "Carrier-based PWM-VSI overmodulation strategies: analysis, comparison, and design," *IEEE Transactions on Power Electronics,* vol. 13, pp. 674-689, 1998.

[66] J. Holtz, W. Lotzkat, and A. M. Khambadkone, "On continuous control of PWM inverters in the overmodulation range including the six-step mode," *IEEE Transactions on Power Electronics,* vol. 8, pp. 546-553, 1993.

[67] A. R. Bakhshai, G. Joos, P. K. Jain, and H. Jin, "Incorporating the overmodulation range in space vector pattern generators using a classification algorithm," *IEEE Transactions on Power Electronics,* vol. 15, pp. 83-91, 2000.

[68] A. M. Khambadkone and J. Holtz, "Compensated synchronous PI current controller in overmodulation range and six-step operation of space-vector-modulation-based vector-controlled drives," *IEEE Transactions on Industrial Electronics,* vol. 49, pp. 574-580, 2002.

[69] H. Manitoba, "Research Centre,'PSCAD/EMTDC user's manual',"

[70] M. Marchesoni, M. Mazzucchelli, F. Robinson, and P. Tenca, "A minimum-energy-based capacitor voltage balancing control strategy for MPC conversion systems," *Proceedings of the IEEE International Symposium on Industrial Electronics*, 1999, pp. 20-25 vol. 1.

[71] B. Mwinyiwiwa, Z. Wolanski, Y. Chen, and B. T. Ooi, "Multimodular multilevel converters with input/output linearity," *IEEE Transactions on Industry Applications,* vol. 33, pp. 1214-1219, 1997.