Development of a ZeptoFarad (10^{-21} F) Resolution Capacitance Sensor for Scanning Capacitance Microscopy

By

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Department of Electrical and Computer Engineering
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DEVELOPMENT OF A ZEPTOFARAD (10^{-21}F) RESOLUTION CAPACITANCE SENSOR FOR SCANNING CAPACITANCE MICROSCOPY

BY

THANG DUC TRAN

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of

Manitoba in partial fulfillment of the requirement of the degree

of

MASTER OF SCIENCE

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ABSTRACT

Over the years, technological advancements in the semiconductor industry have resulted in a high density of devices accompanied by a continuous reduction of their minimum feature sizes. This development introduces a host of new characterization challenges. One of the key requirements of this industry is a two-dimensional carrier profile of state-of-the-art devices. Here we present a technique, the Schottky Scanning Capacitance Microscopy (SSCM) developed by the University of Manitoba SPM lab, for measuring carrier profiles on semiconductor device cross-sections. SSCM utilizes a sharp conducting probe tip that is raster scanned in contact with the sample surface. As a result of the work function difference between the two materials, a space charge depletion region and therefore a capacitor is formed at the interface. By applying a small ac voltage, the voltage derivative of the contact capacitance can be measured with a capacitance sensor and a lock-in amplifier. These voltage derivative measurements are used to delineate regions of different doping levels and dopant type with high spatial resolution. In this thesis we also present experimental results obtained from imaging cross-sections of a wide variety of semiconductor devices. These results demonstrate the capability of SSCM to perform two-dimensional imaging on device cross-sections providing simultaneously surface topographic and capacitance profiles.

A newly designed capacitance sensor is presented. The complete capacitance sensor incorporates a voltage-controlled oscillator (phase-locked to a crystal oscillator operating at 10 MHz), a coupled transmission line resonator, an amplifier and a peak detector. During normal operation, a tip is attached to the resonator and scanned on the sample surface. The variation of the tip-to-sample capacitance shifts the resonant frequency of the resonator, resulting in a modulation of the amplitude of the oscillator signal. By extracting the envelope of the amplitude modulation signal, the voltage derivative of the contact capacitance can be measured. Experimental results have shown that the sensitivity of the sensor is about 1×10^{-21} $F/\sqrt{Hz}$ with a peak-to-peak sense voltage of less than 500 mV.

A conversion algorithm was written to convert the measured data to carrier concentration. Both one-dimensional (1D) and two-dimensional (2D) carrier concentrations

versus position were presented. The results of 1D converted SSCM data compare reasonably with 1D Secondary Ion Mass Spectroscopy (SIMS) data.

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LIST OF ACRONYMS

1D	One Dimension
2D	Two Dimension
AFM	Atomic Force Microscopy
BJT	Bipolar Junction Transistor
CAD	Computer-Aided Design
CPD	Contact Potential Difference
DRAM	Dynamic Random Access Memory
EFM	Electrostatic Force Microscopy
HDD	Heavily Doped Drain
KPFM	Kelvin Probe Force Microscopy
LF	Low Frequency
LNA	Low Noise Amplifier
MOS	Metal-Oxide Semiconductor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NTRS	National Technology Roadmap for Semiconductor
PLL	Phase Lock Loop
RF	Radio Frequency
RTA	Rapid Thermal Annealing
S/D	Source/Drain
SCM	Scanning Capacitance Microscopy
SEM	Scanning Electron Microscopy
SEMATECH	Semiconductor Manufacturing Technology
SFM	Scanning Force Microscopy
SIA	Semiconductor Industry Association
SIMS	Secondary Ion Mass Spectroscopy
SKPM	Scanning Kelvin Probe Microscopy
SOR	Successive Over-Relaxation
SPICE	Simulated Program with Integrated Circuit Emphasis
SPM	Scanning Probe Microscopy
SRM	Scanning Resistance Microscopy
SRP	Spreading Resistance Profiling
SSCM	Schottky Scanning Capacitance Microscopy
STM	Scanning Tunneling Microscopy
TEM Mode	Transverse Electromagnetic Mode
TEM	Transmission Electron Microscopy
UHV	Ultra High Vacuum
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integrated Circuit

CHAPTER 1

INTRODUCTION

1.1 Significance Of Dopant Profile Measurements

For the last four decades the semiconductor industry has been advancing at a remarkable rate. This rate of advance is without precedent in any technology industry. Improvement in both device density and speed will be made by the scaling down of device dimensions. The average device density of the Dynamic Random Access Memory (DRAM) has been roughly doubling every year over the last 20 years. Currently, most semiconductor manufacturers are working with device sizes on the order of 0.18 μm in production, while many are fine tuning 0.165 μm processes. Some of these companies have already decided on the process technology for 0.13 μm feature sizes.

In the U.S., the Semiconductor Industry Association (SIA) released the National Technology Roadmap for Semiconductors (NTRS) last year (2000) **[1]**. In this roadmap, trends were defined even more rigorously than at any time in the past. Table 1.1 shows DRAM specifications given by the NTRS. In comparing the 2000 edition of the NTRS with the 1997 Roadmap, it should be noted that the long-term average annual reduction rate in feature size is projected to continue at approximately 11% per year (about 30% in three years). Furthermore, the 150 nm minimum feature size was changed to 130 nm for 2001 **[1]**. In addition, the early introduction into the market place of 130 nm technology, which, in 1997, was predicted to occur in the year 2003, is now forecast to occur in the year 2001, representing a continuation of the 3-year cycle for DRAM technology. The overall schedule for introduction of a new product generation has once again been accelerated by two additional years. Table 1.2 shows some of the projections that were extracted from the National Technology Roadmap for Semiconductors 1997 **[2]**.

Table 1.1 DRAM Specifications given by NTRS (2000)

Year of First Product Shipment	1997	1999	2001	2004	2008	2011	2014
Minimum feature size (μm)	0.25	0.18	0.13	0.09	0.06	0.04	0.03
S/D Extension Junction Depth, nominal (nm)	50-100	30-60	25-43	20-35	16-26	11-19	8-13
Drain Extension Xj (nm)	70-150	36-60	25-43	20-35	16-26	11-19	8-13
DRAM Capacity (bits/chip)	256M	1G	4G	16G	64G	256G	1T

Source: *The National Technology Roadmap for Semiconductors, 2000 Update*

Table 1.2 DRAM Specifications given by NTRS (1997)

Year of First Product Shipment	1997	1999	2001	2003	2006	2009	2012
Minimum feature size (μm)	0.25	0.18	0.15	0.13	0.10	0.07	0.05
S/D Extension Junction Depth, nominal (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20

Source: *The National Technology Roadmap for Semiconductors, 1997*

In the next 10 years, people in DRAM manufacturing will be dealing with typical feature sizes of 0.13 μm to 0.030 μm. A transition of device dimensions from micrometer to nanometer scales will be made by the semiconductor microelectronic industry. Technologies of both fabrication and characterization will be challenged by the expected transition [3]. Characterization technologies must be developed to monitor and analyze the fabrication process. In addition, the characterization technology also provides a means to verify Computer-Aided Design (CAD) VLSI device and process simulation [4]. Characterization requirements for semiconductor materials and devices cover a wide range of applications. These applications include analysis of starting materials, thin film processing, ion implanting, dopant profiling, contamination analysis and final device qualification. Most conventional characterization technologies will no longer be capable of characterizing

devices with these small feature sizes. New technologies need to be developed to improve characterization parameters, the most important of which are spatial resolution, sensitivity, and repeatability.

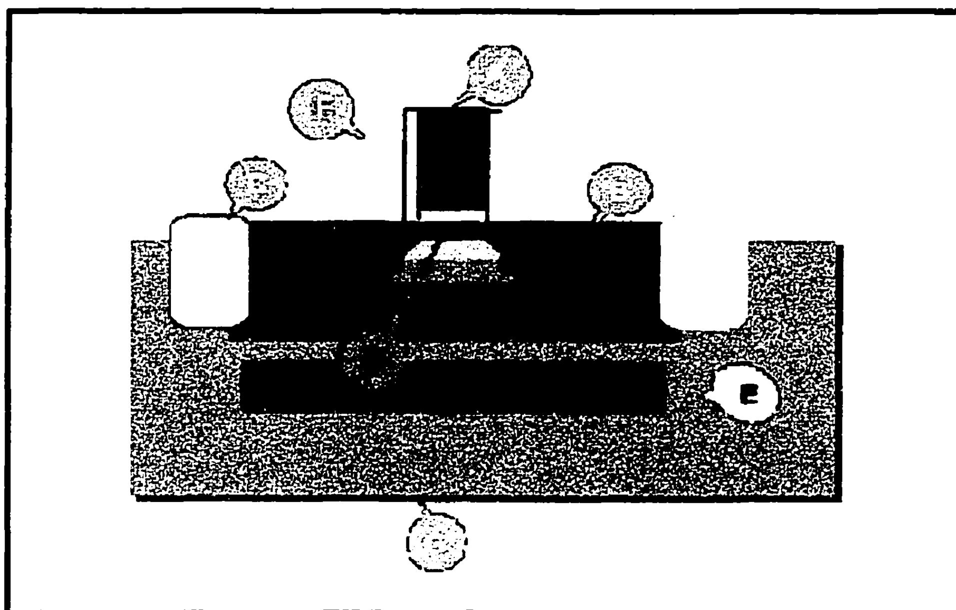
Among the many different types of characterization technologies that need to be developed, two-dimensional (2D) dopant profiling is one of the most important techniques. Determination of the 2D dopant profile in processed silicon with sub-nanometer spatial resolution with 10% accuracy is identified as a high priority technology in the roadmap for the development of next generation integrated circuits. Scaling devices to smaller geometries is expected to have significant impact on processes used for doping drain extensions, channels, and channel edges, and implies more abrupt and shallow dopant profiles. Due to shallow 2D junctions, one-dimensional (1D) dopant profiles can no longer be used for predicting device behavior. Figure 1.1 shows the cross-sectional view of a typical front end process metal-oxide-semiconductor field-effect-transistor (MOSFET) structure with an ultra-shallow junction and retrograde channel doping[1] [5]. One of the important applications of 2D profiling is in characterizing the dopant profile near the gate edges, where the dopant density has an abrupt profile. The transistor performance is very sensitive to the dopant profile around the junction between the heavily doped source/drain region and the channel. A direct 2D dopant profiling technique with nanometer scale resolution is necessary to characterize devices with such small dimensions.

More specifically, direct 2D dopant profiling with nanometer scale resolution provides a double utility in the manufacturing process. First, direct measurement of the 2D dopant profile in device structures provides the means for improved process simulators [6][7]. These process simulators are used where possible to reduce the need for the experimental exploration of the process parameter space. The complex design of modern transistors often begins with process and device simulations. These simulations are useful

1. Retrograde channel doping is used to improve short channel effects and to increase surface channel mobility by creating a low surface channel concentration followed by a highly doped subsurface region. The low surface concentration increases surface channel mobility by minimizing channel impurity scattering while the highly doped subsurface region acts as a barrier against punch through. To be effective, the retrograde depth must be less than the source/drain extension depth and should evolve from a low to high concentration very quickly.

only as far as they can represent reality. Direct measurement of 2D dopant profiles in VLSI devices may provide data that will allow for verification, correction, and tuning of models built into the process simulators. High resolution dopant profile measurements will also be useful as direct input into electrical device simulators as well as for early prediction of device performance.

Secondly, the direct measurement of 2D dopant profile in VLSI devices will influence the process optimization directly. Optimization of implantation and diffusion process steps can be achieved by the rapid feedback afforded by nanometer scale, high sensitivity measurements. These measurements will allow the processes to be tightly controlled to maintain high quality and improve the overall yield of the processes. All of these factors are critical to the VLSI manufacturers.



A: Gate Stack
B: Source/Drain-Extension
C: Isolation
D: Channel
E: Wells
F: Field Oxide
G: Starting Material

Figure 1.1 Schematic diagram of a typical front end MOSFET device
Source: *The National Technology Roadmap for Semiconductors, 1999 Front End Processes*

1.2 Introduction To Dopant Profiling In Semiconductors

Doping is a process through which impurities are introduced into a semiconductor substrate to change the resistivity or to form a junction in a semiconductor. For silicon device fabrication, there are two main doping methods: thermal diffusion and ion implantation **[8][9]**. In the early years, semiconductor doping was typically performed by long, high temperature annealing in a source of dopant atoms. With the advent of VLSI base circuits and their smaller feature sizes, diffusion became a process limitation. The limitation was mainly caused by side diffusion, poor total dopant dose control, surface doping and dislocation generation. Modern junctions are typically formed by ion implantation followed by fast, lower temperature annealing to activate the dopant atoms. This method overcomes the limits of the thermal diffusion technique and has additional benefits. Although scattering effects during implantation can cause a nonuniform distribution around mask edges, there is almost no side diffusion caused by thermal annealing if rapid thermal annealing is used. With ion implantation there is better control of the location and number of dopants placed into the wafer. Also, photoresist and thin metal films can be used as doping barriers along with the usual silicon dioxide layers. Given these benefits, it is not surprising that the majority of the doping steps for advanced circuits are done by ion implantation.

Typically, boron is used for P-type doping while phosphorus and arsenic are used for N-type doping **[9]**. In N-type silicon material, each doped element (P or As atoms with five valence electrons) forms four bonds with surrounding silicon atoms, providing an additional weakly bound electron. At room temperature, this electron is excited to the conduction band to become a free electron, and the doped element becomes a positive ion. The silicon is N-type because of the addition of the negative charge carrier, and the doped element is called a "donor". Similarly, in P-type silicon material, when a boron atom with three valence electrons substitutes for a silicon atom, an additional electron is accepted to form four covalent bonds around the boron, and a positive charged "hole" is created in the valence band. In this case, the doped element becomes a negative ion and is called an "acceptor". The conductivity of a material is essentially proportional to the density of the free charge carriers.

However, not every dopant atom is electrically active, or ionized in silicon material. This depends upon the sample preparation conditions, such as non-equilibrium activation, and deactivation by clustering and precipitation. Normally, a method called Rapid Thermal Annealing (RTA) is used for activation after the ion implantation step. This process is usually conducted at high temperature (~1000° C) for less than 1 minute. The annealing process is not only required to activate the dopant, but also is used to reduce the lattice damage introduced by implantation. The equilibrium condition is hard to achieve for every implanted atom in this short a time period. In addition, defects in silicon can trap the implanted atoms and deactivate them.

It is necessary to distinguish between chemical dopant density and electrically active density. Therefore, dopant profile methods must be differentiated based on whether they measure chemical density or the electrically active density. The knowledge of chemical dopant profile is important for calibration of diffusion models for process simulators. On the other hand, the electrically active dopant profile determines the critical parameters of real devices. Accurate determination of the electrically active dopant profile is also important for sub-micron and sub-nanometer technology development.

1.3 Dopant Profile Measurement

The continued optimization of silicon devices provides a great challenge to both conventional as well as currently developing characterization capabilities. However, conventional dopant profiling techniques are limited to 1D profiling measurements.

For 2D[2] profiling, sensitivity and spatial resolution are always key. However, there is a trade-off between these two parameters. Normally, higher spatial resolution means smaller detection area and requires higher sensitivity. Achieving very high spatial resolution

2. For the work done in this thesis, 2D refers to a surface on which tip is scanned. 2D measurements consist of multiple scan lines taken from the prepared surface of the sample. A 1D measurement is simply a single scan line of data.

without losing sensitivity is one of the biggest challenges for researchers developing dopant profiling techniques.

For the semiconductor industry, characterization efforts for silicon technology must provide leading edge analysis in a timely and economic manner. The best characterization data are often of little value if a key technical decision on a processing parameter cannot be made rapidly enough to keep a silicon device production line operating. The capability of in-line and in-situ measurements is one of the most important directions for future manufacturing. The following is a review of existing dopant profile methods based on sensitivity, spatial resolution, 1D or 2D measurement capabilities, type of measured dopant density (chemical or electrically active), speed, destructiveness, in-line and in-situ capabilities.

1.4 Review of Existing Dopant Profiling Techniques

1.4.1 Secondary Ion Mass Spectroscopy (SIMS)

Secondary ion mass spectroscopy is one of the most powerful and widely used techniques for semiconductor doping characterization. It is a widely used method for impurity profiling, and provides accurate and reliable results. Due to its high sensitivity, this technique provides an excellent independent standard to which other dopant profiling techniques may be compared. In this technique, the sample to be analyzed is bombarded with a primary ion beam of energy 1-10 keV, and the secondary ions sputtered from the sample are collected and counted [12]. Secondary ions are analyzed with a mass spectrometer. Subsequently, the mass spectrum provides a quantitative measurement of the chemical composition of the sputtered material. This method is used to measure the chemical or atomic dopant concentration.

Technically, SIMS is a very sophisticated system, and is very expensive. One of the

limitations of SIMS is that it is a destructive method and has long turnaround time. Since it can accurately measure the dopant profile only in the sputtering direction, it can be used only for large device or test device characterizations. Because of its relative complexity, many factors can affect the accuracy and sensitivity of the measurements [10][11]. For example, the different nature of primary ions, and different impact energies of the primary ions, can affect the sputter rate. Also, this rate is usually uneven near the surface of a sample. The accuracy of standard SIMS results at very shallow depths is limited due to an initial transition region in the data which results from surface effects that lead to non-uniform sputtering of the sample[13][14].

The environment under which SIMS is operated also affects the measurements. SIMS identifies the sputtered ions using their mass-to-charge ratios. It is difficult to accurately detect the presence of $^{31}P+$ ions when water vapor is present. This is because ^{30}Si reacts with H forming $^{31}SiH+$ ions which have a mass to charge ratio similar to $^{31}P+$ ions. As a result, SIMS measurements are required to be performed in a high vacuum with high resolution detectors. In addition, the sensitivity of SIMS varies widely with both the impurity being measured and the beam used for sputtering (cesium and oxygen are typically used) [15]. This variation in sensitivity can render the interpretation of measured results difficult.

In SIMS measurements, the sputtering process leaves a crater on the bombarded sample, which increases in depth with time. A depth profile of dopant atoms can be obtained as a function of time by measuring the depth of the crater after the SIMS measurement. By using this depth measurement, a plot of dopant concentration versus depth can be constructed. SIMS has a depth resolution on the order of 1 nm - 2 nm and is sensitive enough to detect some elements present in concentrations less than 10^{15} cm^{-3}. However, its lateral resolution is poor and extends over several devices. Higher sensitivity SIMS measurements can be achieved when larger beam spot sizes are used. This is because there are more atoms are ejected from the sample. The poor lateral resolution of the SIMS technique makes the use of SIMS impractical for 2D dopant profiling on nano-meter scale devices.

Conventionally, SIMS is the principal 1D diagnosis technique for depth profiling the dopant distributions in semiconductor structures. However, some new methods have been

proposed for the utilization of SIMS in the analysis of lateral diffusion **[16,17,18,19]**. One of these methods employs specially fabricated samples, which allows material to be collected from a large number of similar volumes to obtain high resolution, high sensitivity, 2D profiles. The sample geometry is such that the lateral spread is magnified many times allowing the larger reactive ion probes to be used (larger beam spot size), with a consequent increase in ion yield and therefore sensitivity. The dopant to be investigated is implanted into 400 stripes, each 1.5 μm wide, and 2 mm long. The stripes are then sectioned at 0.1^{o} by 300 plasma etched trenches 3 μm wide, and 2 mm long (a more detailed explanation of sample preparation can be found in **[16]**). The primary ion beam is rastered over the sample with the linescan direction perpendicular to the original implanted stripes. Instead of recording the secondary ion signal for a complete rastered frame, as in normal depth profiling, the signal for each linescan is recorded. Subsequent scans encounter more or less of the implanted stripe, due to the sectioning, and the difference between scans is directly related to the difference in concentration in the lateral direction. Thus, the lateral profile may be deduced for the exposed surface. Because each successive complete frame contains lateral data for the corresponding depth, a complete two-dimensional map can be acquired. With this technique, an effective lateral resolution of 50 nm and sensitivity of about $1x10^{14}$ cm^{-3} was obtained **[16][17]**. However, complex mathematical processing of raw data is required to produce a 2D dopant profile.

Another 2D SIMS method was demonstrated, wherein two-dimensional doping profiles were determined from multiple one-dimensional secondary ion mass spectroscopy profiles using computed tomography techniques **[20]**. This method also requires a long analysis time and relies on many factors such as special sample preparation, extensive data processing and manipulation, extensive modeling and experimentally defined parameters. Although the described methods are capable of measuring 2D dopant profiles, they all suffer from some artifacts that distort the profile. In addition, the analyzed samples are very different from real devices; thus they do not necessarily reflect the true dopant distributions in real devices.

1.4.2 Transmission Electron Microscopy

Transmission electron microscopy (TEM) is a high resolution technique used for two dimensional carrier delineation. This technique utilizes a transmission electron microscope to obtain images of junctions. The high spatial resolution of TEM, approaching 2 Å, is a strength of this technique. TEM images a sample by transmitting an electron beam at 50 - 400 keV through the sample. As the beam passes through the sample, it is scattered or diffracted by the atoms in the sample. The transmitted beam is projected onto a screen for viewing or onto a photographic plate. By analyzing the image of the transmitted electron beam, one can determine the location of doped regions on the sample.

TEM has a high spatial resolution, but the image contrast is quite insensitive to the presence of impurities or dopant atoms **[21]**. Only for very high concentration levels, above 1×10^{19} cm^{-3}, a significant contrast change in the TEM image is observed mainly due to the change of the lattice parameter of silicon. In order to image one or two-dimensional dopant profiles, one has to artificially enhance the contrast between areas with different dopant concentrations. The enhancement can be done by reducing the thickness of select doped regions by preferential etching or by the preferential creation of lattice defects in selected doped regions **[21]**.

One of the main weaknesses of the TEM technique is the difficulty of sample preparation. The sample must be thin enough so that the electron beam can be trasmitted through. Samples must be prepared to thicknesses of the order of 0.1 - 1 µm depending on the accelerating voltage of the electron beam. Thus, the samples are hard to handle and time consuming to prepare. Another difficulty that is commonly encountered with the TEM technique is the interpretation of TEM images. Due to the wide variety of beam scattering processes, interpretation of images can be more complicated than with other dopant profiling techniques.

1.4.3 Chemical Staining and Selective Doping Etching Method

Methods which use chemicals to delineate junctions have been used for a long time. These methods take advantage of the fact that one doped region on the semiconductor will react differently to chemical attack than another region of a different doping type or concentration.

Both chemical staining and chemical etching are electrochemical processes. The dopant density detected by these methods is the electrically active dopant density. Staining is a method in which the particular metal is selectively deposited on silicon using the principle of galvanic displacement reactions [22] or electrolytic techniques [23]. Generally, staining solutions plate the N-type region more than the P-type and are thus useful for junction delineation. N-type devices decorated with copper metal have been observed by TEM and Scanning Electron Microscopy (SEM). However, it was found that the copper grain sizes were too large to locate the junction accurately [22].

The chemical etching method has been extensively studied. It is based on the observation that the etch rate of silicon in certain etching solutions can be related to carrier concentration. When these etching solutions are applied to the sample surface, a topography will appear due to the different etch rate for different carrier densities. The silicon etching solution commonly used is a mixture of HF and HNO_3 in which the HNO_3 oxidizes the silicon surface while HF removes the oxide layer formed. The etching rate of silicon is controlled by the slowest of these two processes. The resulting topography of the etched sample has a profile that represents the surface dopant profile of the sample. By using high spatial resolution resolving devices such as a TEM, SEM, Scanning Tunneling Microscope (STM) or Atomic Force Microscope (AFM), the treated surface topography is imaged and the doping profile can be extracted.

Because chemical staining and chemical etching methods do not yield the doping profile directly, the analysis of raw data for these methods relies on an independent dopant profile technique for calibration. Sample preparation depends on which resolving device is to be used. The samples required by TEM are very thin (normally 0.1 - 1 μm), fragile and time consuming to prepare. Furthermore, the interpretation of TEM images is complicated. STM

measurements require a conducting sample surface [24]. Since there is a native oxide layer on a typical silicon surface, the STM imaging must be done in an ultra high vacuum (UHV) chamber and is very sensitive to contamination on the sample surface. Measurements with an AFM can directly give the topographical profile of the sample. Additionally, it is a nondestructive method with high spatial resolution and does not require extensive sample preparation [25]. In contrast SEM can only determine the isoconcentration contours. In order to extract the dopant densities using SEM, an independent method is needed for calibration.

The disadvantage of the etching technique is that it is a destructive method in nature and has a complex etching mechanism. The etching step can be applied only once per specimen. Furthermore, the reproducibility and controllability are poor if the etching solution is not properly selected [24][26]. Although chemical methods have some disadvantages, they have been successfully used by several research groups to delineate pn junctions with 10 nm spatial resolution over a dynamic range of 1×10^{17} - 1×10^{20} cm^{-3} carrier concentrations [24][27].

1.4.4 Electrostatic Force Microscopy and Kelvin Probe Microscopy

Electrostatic force microscopy (EFM) utilizes a non-contact mode atomic force microscope (AFM) to measure the forces between a tip and sample. The EFM operation can be briefly described as follows: a cantilever with a sharp tip is mounted on a piezoelectric bimorph[3] and vibrated at its resonant frequency ω_0. When the tip approaches the sample, the force gradient of the tip-sample interaction modifies the effective spring constant of the cantilever, resulting in both a resonant frequency shift, and a vibration amplitude reduction at the drive frequency. The motion of the tip is monitored by a differential interferometric detection system (details of the experimental setup can be found in [28]). One of the interferometer outputs provides a signal to a feedback loop that adjusts the height of the tip

3. Bimorph is the flexing-type piezoelectric element. The principle is similar to the bimetal thermometer. It is made of two thin plates of piezoelectric material that are glue together. When a voltage is applied, the element is bent in the direction that is perpendicular to the element axis.

via a piezoelectric tube to keep the vibration amplitude constant during a scan. Therefore, the movement of the piezotube in the z direction represents the corresponding topography of the sample surface. At the same time, a sinusoidal voltage is supplied to the tip at a frequency ω. Due to the potential difference between the tip and the sample, an electrostatic force is created. The electrostatic force is then detected at frequency ω by an optical interferometer and a lock-in amplifier.

Since the potential difference between the tip and the sample depends on the dopant concentrations, in principle, the dopant concentrations can be extracted from the measured force between the tip and the sample. The electrostatic force measurement technique was demonstrated [28] and used to image the migrating surface ions on Si_3N_4 in fringing lateral fields.

The idea of scanning Kelvin probe microscopy (SKPM) is based on the observation that the contact potential difference (CPD) between two materials depends on a variety of parameters such as the work function, adsorption layers, oxide layers, dopant concentrations, and temperature changes in the sample [29][30]. In principle, measurements of the CPD can be used to obtain information concerning these parameters. A common method to measure the contact potential difference is the vibrating capacitor method or Kelvin method [29][30]. In this method, two conductors are arranged as a parallel plate capacitor with a small spacing that is vibrated periodically. In a simple model, the contact potential between the two materials is $V_{CPD} = 1/\exp(\Phi_2 - \Phi_1)$, where Φ_1 and Φ_2 are the work functions of the conductors. A vibration of the distance between the two conductors at frequency ω results in a current that is given by [31]

$$i(t) = V_{CPD}\, \omega \Delta C \cos \omega t \qquad (1.1)$$

where ΔC is the amplitude of the variation in capacitance. For the actual measurement of V_{CPD}, an additional external voltage (bucking voltage) is applied between the two conductors until the space between them is field free and the current i(t) goes to zero (details of the experimental setup can be found in [29]). The interpretation of the bucking voltage is central to an understanding of the Scanning Kelvin Probe Microscope's ability to measure local

surface potentials.

The Kelvin method has a high sensitivity for potential measurement but integrates over a large portion of the conductor including some of the side walls and does not provide a lateral image of the variation of the CPD on the surface. To overcome this difficulty, a higher lateral resolution CPD measurement technique, namely Kelvin Probe Force Microscopy (KPFM) was developed [32][33]. This method utilizes some aspects of both EFM and SKPM. The principle is similar to the Kelvin method except that forces are measured instead of currents. It also uses much a smaller tip to trace features on the sample surface, resulting in a greater lateral spatial resolution. Henning *et al.* [33] have applied the KPFM to the problem of profiling dopant concentrations in two dimensions in silicon microstructures. By measuring the electrochemical potential difference which minimizes the electrostatic force between probe tip and sample surface, Henning *et al.* were able to estimate the work-function difference between the tip and sample and extract the dopant concentration of a lightly doped drain MOSFET. With this technique, a lateral spatial resolution of less than 100 nm and a voltage sensitivity of better than $5mV/\sqrt{Hz}$ was obtained [33]. A similar spatial resolution was demonstrated by Clayton *et al.* [32] in studying of the atomic ordering of a GaInP sample. The results of this study show that the KPFM is capable of distinguishing between ordered and disordered regions in GAInP.

1.4.5 Spreading Resistance Profiling (SRP) and Nano-SRP

Spreading Resistance Profiling is one of the longest-lived carrier density profiling techniques and is still widely used in the semiconductor industry. This technique derives the local resistivity of a semiconducting surface from the resistance between probes that are placed perpendicular to the sample surface. The samples used for SRP measurements can be as thick as 1000 μm to as thin as 0.1 μm by using specially conditioned metallic alloy probes (such as a tungsten-osmium alloy) [34][35]. For thin samples, a beveling technique is required to expand the area of interest and therefore increase the spatial resolution.

Spreading Resistance measurements are performed by stepping two metal probes over a beveled sample surface as shown in Figure 1.2. As the probes are stepped over the surface, the probes are biased, and the electrical current through the probes is measured at each step. The measured current is then used to calculate the sample local spreading resistance, and the resistivity of the sample is then determined from the expression:

$$R_{sp} = \frac{k\rho}{2r} \qquad (1.2)$$

where k is an empirical constant, ρ is the semiconductor resistivity and r is the effective electrical contact radius of the probe. The resistivity ρ is then converted to carrier density by using proportional constants or a look-up table. In practice, the interpretation of measured R_{sp} is complex, as distortions in the measured data can be caused by many factors such as carrier spilling [36], surface charge [37], the actual nature of probe contacts, sample orientation and preparation. Therefore, the dopant profile extracted greatly depends on the model used to relate the raw data to the carrier concentration.

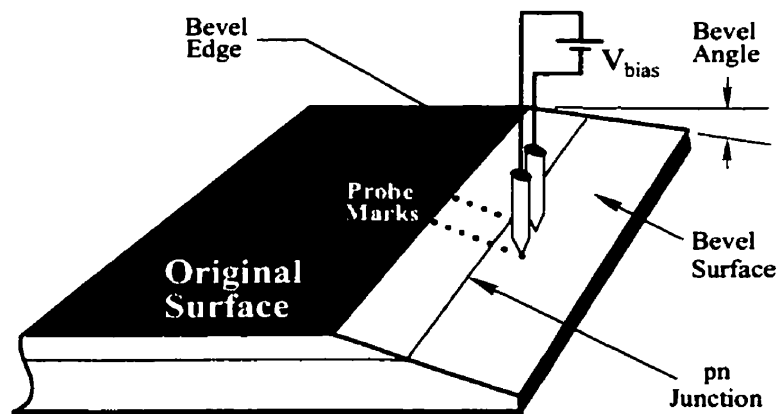


Figure 1.2 Two-Probe spreading resistance measurement.

Another factor, which can add errors to the measured dopant profile, is introduced by the sample preparation method (beveling). Actually, electrically-active carrier density is measured by SRP instead of chemical dopant density. The carrier density can be very different from the chemical dopant density for steep dopant gradient samples **[36]**. After beveling, the dopant gradient is much smaller than before beveling, so that the carrier distribution is also altered.

Compared with other dopant profiling techniques, SRP has weaknesses such as: (1) sample preparation is difficult, because great care must be taken to ensure that the bevel angle of the sample is well controlled. (2) SRP measurements are destructive due to the footprints left on the sample surface. (3) SRP does not work well for semiconductors other than Si or Ge, though advances have been made in modifying the current-voltage (I-V) characteristics so that SRP could be used for GaAs and InP semiconductors **[35]**. (4) Finally, the conventional SRP cannot be used for 2D dopant measurement due to the large separation between the probes (10 - 100 μm) and the size of the probe imprints (1 - 10 μm). However, SRP is widely accepted and is being used for 1D dopant profiles due to its high dynamic range (normally 1×10^{12} to 1×10^{21} cm^{-3} can be achieved).

Another technique that has similar properties as SRP and may be able to measure dopant concentrations in two dimensions is called Nano-SRP. Nano-SRP differs from the conventional SRP by using a single metallic probe to measure the spreading resistance between the tip and the sample surface. Here a biased probe is placed in contact with a semiconductor surface while the back of the sample is grounded to provide a return path for current flow. The back contact is normally large to avoid the contribution of the contact resistance to measured resistance. In Nano-SRP measurements, the tip is loaded with a force high enough (between 70 - 260 μN) so that it can break through the native oxide layer to made a good electrical contact with the silicon **[38]**. The spreading resistance is then measured by stepping the probe on the sample surface. By using a small tip and small step sizes, higher spatial resolution can be achieved. Additionally, a small contact size and the possibility to make very small steps imply that one can measure directly on a vertical cross section of the structure instead of beveled surface. Thus, time for sample preparation can be reduced. Nano-SRP has some advantages over conventional SRP techniques, but it is still a

destructive method.

1.4.6 Scanning Resistance Microscopy (SRM)

Scanning Resistance Microscopy has been implemented by combining the scanning force microscope (SFM) and the measurement of resistance between a tip and a sample [39][40]. The resistance measurements are performed by scanning a sharp, conducting probe on the surface of the sample under test (see Figure 1.3). A constant bias voltage is applied to the SRM probe, and the current flow between the probe and the sample is monitored. The magnitude of the measured current is used to obtain information on the local resistivity of the probe-surface interface, from which carrier density can be extracted.

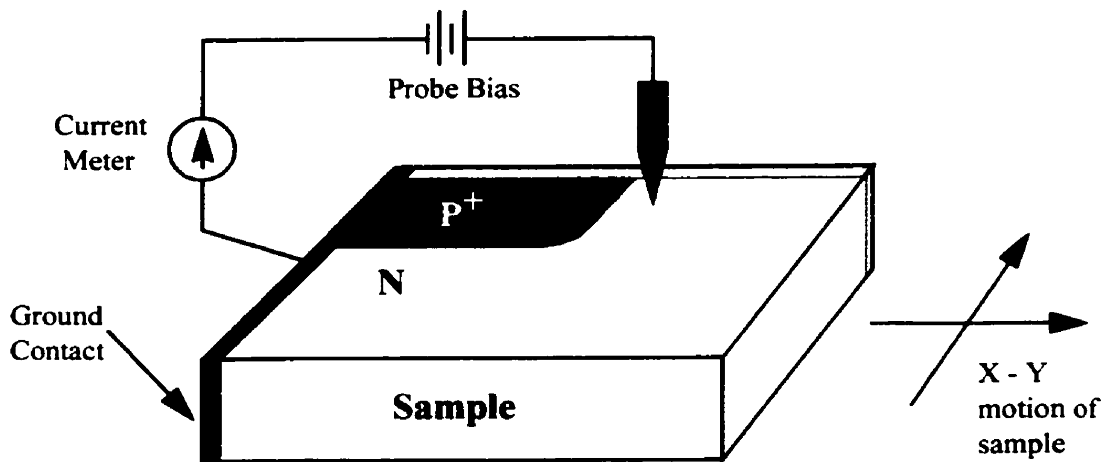


Figure 1.3 Schematic of a resistance measurement.

Basically, SRM works much like SRP and Nano-SRP. However, there are several essential differences between SRM operation and spreading resistance measurements. Firstly, the sample is scanned beneath the SRM probe tip instead of stepping the probe over the sample surface (the tip can also be scanned on the sample surface while the sample is kept stationary). Thus, the SRM obtains a continuous resistivity profile of the surface. By moving the probe in a raster pattern on the sample surface, two-dimensional resistance

profiles can be obtained [41]. Secondly, the SRM probe size is much smaller (around 30 nm) and the contact force is much lower (~ 100 nN) than SRP. Combining a small probe tip and low contact force is a key point that enables SRM to obtain high spatial resolution. A lateral spatial resolution of less than 35 nm was achieved by Shafai *et al.* [40] when SRM was used to delineate a pn junction sample. Finally, SRM is a nondestructive method. A sample can be re-used or investigated many times. However, SRM requires a clean and conducting sample surface. The tip must be made in a good electrical contact with the sample surface. Since SRM signals strongly depend on the applied tip pressure, stable results can be achieved only when an appropriate pressure is applied. Bias voltage is also an important factor when SRM is used to measure dopant profiles. For example, SRM is insensitive to dopant concentration changes in a lightly doped region ($N < 10^{17}$ cm^{-3}) if the SRM probe is biased such that the contact resistance is the dominant measured resistance. In order to profile semiconductor in a lightly doped region, the probe must be biased such that the spreading resistance dominates.

A new approach was taken by Nxumalo *et al.* [42] to improve the performance of SRM. In this approach, the SRM probe voltage is modulated in order to maintain a constant current across the tip-surface contact. It has been shown [42] that a significant improvement can be obtained by using constant current mode for dopant measurements. By using this imaging mode in conjunction with a diamond doped tip, a lateral spatial resolution of 20 nm was achieved by Nxumalo *et al.* To date, no quantitative measurements have been done to convert the SRM signal to dopant density. A more detailed explanation of SRM can be found in [42].

1.4.7 Scanning Capacitance Microscopy (SCM)

The scanning capacitance microscope has great potential for the measurement of doping profiles with nanometer scale lateral resolution. This approach is based upon the general concepts used in 1D capacitance-voltage (C-V) profiling [43]. In the earlier stage of SCM development, the SCM was operated in a non-contact mode and focused on the measurement of topographical and dielectric properties of metallic and insulating surfaces

[Ref. 44, 45, 46]. Capacitance measurements were performed using a small conducting probe placed in close proximity to the sample under examination. The probe was vibrated with a small amplitude at a frequency where excess noise was not significant. Using a simple model of a parallel plate capacitor, the capacitive gradient can be modelled as the inverse square of the gap spacing between the probe and the sample $dC/dz = (Area)\varepsilon_0\varepsilon/d^2$. This strong dependence of the capacitive gradient on the separation can be used to control the height of the probe above the surface. By employing a feedback control loop to maintain the position of the probe with respect to the surface so that the amplitude of the differential capacitance at the modulation frequency is kept constant **[46]**, the properties of the sample surface can be studied (a control loop can also be used to maintain a constant gap between the tip and the sample **[45]**).

Over the last ten years, the capacity of SCM to perform dopant profiling on semiconductor surfaces has been explored by a number of research groups. C. C. Williams *et al.* and his research group have used the SCM in the area of semiconductor characterization **[Ref. 47,48,49,50]**. Instead of holding a probe tip over the sample surface, the sample surface was covered by a thin layer of oxide and the probe tip placed in contact with the oxide layer. The probe was biased with a small signal AC voltage added to a DC bias, resulting in creation of a depletion region. A capacitor was formed in the sample beneath the tip contact point. The width of the depletion region depended on probe bias voltage as well as local dopant concentration. By monitoring the depletion capacitance as a function of probe position, it was possible to distinguish between regions of different dopant concentration. Two-dimensional dopant profiles can be easily be obtained with this technique by scanning a probe tip in a raster pattern on the sample surface.

For SCM measurements at constant bias voltage as described above, it has been expected that depletion width varies with dopant concentration, resulting in a variable spatial resolution. To overcome this problem, a new approach was developed by Williams *et al.* In this approach, a feedback loop is employed in which the magnitude of the AC bias voltage applied to the probe is adjusted to maintain a constant capacitance change (and therefore nearly constant depletion width) as the tip is scanned across a dopant gradient **[48]**. The feedback signal therefore can be used to extract the dopant profiles. The operation of SCM

just described is normally referred to as constant capacitance mode. Also, an analytical quasi-1D model was developed to convert the measured data to dopant density. By modeling the tip as a conducting sphere in contact with an oxide on a conducting plane, the tip-sample capacitance can be numerically calculated as a function of tip bias, tip radius, dielectric constant, oxide thickness, and dopant density [49]. In practice, however, the tip shape for SCM is relatively undefined (unknown parameter), though tip profiling techniques have been developed. The tip becomes worn after a short time in SCM scanning (sometimes in as short as several line scans) [51]. Therefore, the quantities of the extracted dopant density depend on the accurate determination of time-varying input parameters, especially the tip radius. Additionally, only relative dopant profiles can be measured by the SCM method without the use of dopant density standards. A reference point at which the dopant density is known by an independent means is needed to find the absolute dopant concentration. Some researchers ([48][49]) have measured dopant density by using the highest dopant density measured by SRP as the reference point (the quantitative dopant density has been extracted at the doped levels between 10^{17} and 10^{20} cm^{-3}).

SCM is a nondestructive technique and measures carrier density, rather than dopant density. It has been shown that when the dopant density varies moderately over a scale comparable to the Debye length[4], the carrier density is a reasonably good measure of the activated dopant density [48]. However, the presence of the oxide layer separating the tip and the sample limits the spatial resolution of the technique.

4. Debye length is a characteristic length or screening length for semiconductor. It is defined as: $L_D = \sqrt{\frac{\varepsilon kT}{q^2 N}}$, where k is the Boltzmann constant, T is the absolute temperature, q is the electronic charge, ε is the dielectric constant of the semiconductor, and N is the local density of doping.

1.4.8 Scanning Tunneling Microscopy (STM)

The Scanning Tunneling Microscope (STM) developed in 1981 by G. Binnig *et al.* **[52]**, has been used extensively for the topographic imaging of surfaces with atomic, or near atomic resolution. The STM is based on a phenomenon called quantum mechanical tunneling. When a voltage is applied between a sharp metal probe tip and the surface of an electrically conductive material, a very small tunneling current will be produced provided that the tip is positioned a few nanometers from the surface (see Figure 1.4). The very high resolution of the STM relies on the exponential dependence of the tunnel current on the separation distance between the metal tip and the scanned surface, according to the expression given in **[53]**:

$$I_T \propto \exp\left(-A\varphi^{1/2}s\right) \qquad \textbf{(1.3)}$$

where I_T is the tunneling current, **A** is a empirical constant, φ is a function of the tip and the surface work functions, and **s** is the separation between the tip and surface. It is this sensitivity that makes it possible to monitor and detect changes in the separation distance. A piezoelectric tube is used to control the position of the tip in three-dimensions relative to the sample and scan the probe tip parallel to the surface. The tip's position perpendicular to the surface is determined from the output of a feedback circuit which sends a voltage signal to the particular piezo element that moves the tip towards or away from the surface in order for a preset tunneling current to be maintained. The displacement of the tip set by the voltage applied to the piezo drives in the z direction then yields a topographic picture of the surface. From equation (1.3), scanning the tunnel tip at constant tunnel current implies that $\varphi^{1/2}s$ is constant. Thus, the z displacement of the tunnel tip gives the surface topography only for a constant work function φ, and therefore a constant tip-sample separation distance s. Any contamination present on the sample surface can modify the work function, resulting in alteration of the tip-sample gap that is needed to maintain a constant tunneling current. In this case, the z displacement no longer represents a true surface topography of the surface to be studied. For this reason, STM requires a clean sample surface and normally operates in an ultrahigh vacuum chamber.

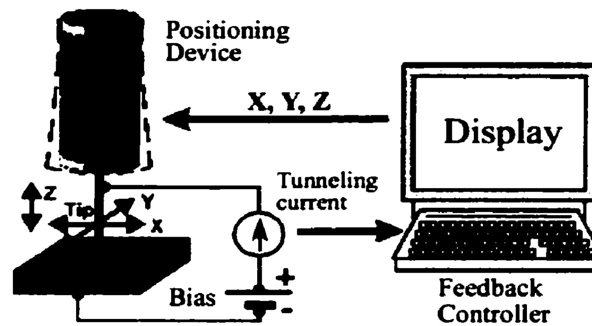


Figure 1.4 Schematic of a Scanning Tunneling Microscope

A number of different studies have been undertaken to investigate the potential for STM to be used as a device for pn junction delineation [54][55][56]. However, it is not possible to distinguish between p-type and n-type materials in the usual mode of operating the STM in which only the topography of the surface is imaged. To identify the semiconductor type (pn junction), a new approach called Current Imaging Tunneling Microscopy was developed [54]. In this approach, the tip-sample separation distance is held fixed by a reference tunnel voltage and tunnel current varies while the tip is scanned across the junction. By studying the voltage-current characteristics (I-V curves) at different locations, a significant current flow has been observed when the tip is placed on one material type compared to the other while an appropriate tunnel voltage is applied. The pn junction could be delineated with a lateral resolution of 100 nm by measuring the current flow between the tip and the sample. Similarly, by using the current imaging technique, a two-dimensional image of a pn junction with 30 nm lateral resolution was obtained with the help of a special biasing scheme [55][56]. However, this technique can only be used for scanning relatively flat surfaces.

STM is a non-destructive technique. However, it can not be used to study non-conducting surfaces or surfaces showing significant oxidation. Surfaces must be cleaned of surface oxide and should be placed under high vacuum if they are to be studied for any length of time. The presence of native oxide can cause the probe tip to crush against the

surface while the tunnel gap is kept constant by a feedback circuit. The crushing occurs when the oxide layer grows larger than the tunnel gap. The electrical characteristics of the probe tip may be changed after this collision, resulting in subsequent measurement errors.

1.4.9 Metal-Semiconductor C-V Measurements and Schottky Scanning Capacitance Microscopy (SSCM)

Capacitance-voltage (C-V) measurements have been used for more than 40 years to measure important material characteristics of semiconductors. In the past, the impurity concentration of semiconductor material has been obtained by measuring the capacitance of the Schottky barrier[5] as a function of reverse bias voltage, and one-dimensional depth profiles have been determined **[57][58]**. In this technique, a Schottky contact is placed over the region of the sample where the measurement is to be performed (Schottky contacts are usually formed by depositing a dot of metal alloy on the sample surface). A reverse bias DC voltage is applied to the contact, which causes a reverse bias space-charge depletion region to form. By measuring the Schottky contact capacitance as a function of reverse bias voltage, the depletion width can be calculated from a simple equation (1.4) assuming that the junction can be represented as a parallel plate capacitor:

$$W = \frac{\varepsilon A}{C} \tag{1.4}$$

where W is the width of the space-charge depletion region, ε is the dielectric constant of the semiconductor, A is the junction area, and C is the measured capacitance. The impurity concentration as a function of the depletion width can be found from equation (1.5) **[58]**. Generally, a series of voltage-capacitance measurements for several depletion widths are performed and the impurity concentration versus depth can be constructed by differentiating the raw capacitance-voltage data:

5. Details of the Schottky barrier and the Schottky contact can be found in **[9]**.

$$N(W) = \frac{2}{q\varepsilon A^2}\left(\frac{d(1/C^2)}{dV}\right)^{-1} \tag{1.5}$$

where q is the electronic charge, and N(W) is the net impurity concentration at the edge of the depletion layer.

The proposed C-V method can be used to obtaine the absolute impurity concentration. However, the junction area must be accurately determined. Errors in determining the area lead to errors in calculating both the depletion width W and the impurity concentration N(W). In addition, measurement depths are limited to a minimum depth of at least that of the zero bias space-charge region formed by the Schottky contact, and to a maximum depth by voltage breakdown. C-V measurements can be performed with the Schottky contact slightly in forward bias. With a large forward bias, however, a difficulty of the capacitance measurement will be encountered due to the presence of the shunt contact conductance.

Schottky Scanning Capacitance Microscopy (SSCM) has been developed and is currently used in our Scanning Probe Microscopy (SPM) lab for delineation of semiconductor dopant profiles. Measurements are made of local Schottky contact capacitance existing across the depletion region at the metal-semiconductor interface. Actually, an alternate method of the C-V measurement is used for 2D characterization of dopant profiles in real semiconductor devices. The Schottky Scanning Capacitance Microscope operates as in Figure 1.5. A conducting probe with a small radius of curvature is placed in contact with a clean, oxide-free semiconductor surface. Due to the work function difference between the two materials, a space-charge region is created and therefore a capacitor is formed at the metal-semiconductor junction. The contact depletion capacitance is a function of bias voltage across the junction and the dopant concentration of the semiconductor. A small constant AC voltage is applied to the sample with the probe grounded[6], resulting in a modulation of the depletion-layer capacitance. Under the assumption of a planar junction and an abrupt approximation, the

6. The probe is grounded at low modulation frequency via the resonator that is a part of the capacitance sensor (see Chapter 5)
(DC voltage can also be applied with low frequency AC voltage simultaneously).

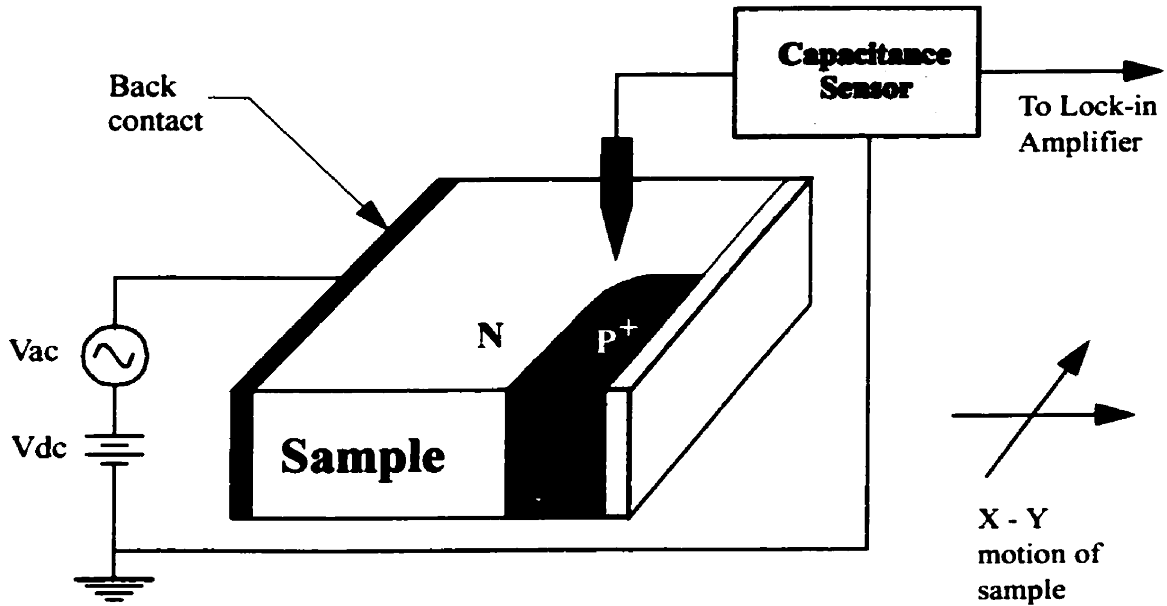


Figure 1.5 Schematic of a local Schottky contact capacitance measurement.

carrier concentration can be determined from expression (1.6) by measuring the depletion-layer capacitance change *dC/dV* due to the modulation voltage Vac. The derivation of equation (1.6) can be found in Chapter 3 of this thesis.

$$N = \frac{8\,(V_{bi} - V)^3}{q\varepsilon}\left(\frac{dC}{dV}\right)^2 \tag{1.6}$$

where V_{bi} is the built-in potential across the junction, q is the electronic charge, ε is the dielectric constant of the semiconductor, and V is the external bias voltage. In principle, equation (1.6) tells us that the dopant concentration can be determined if *dC/dV* is measured. *dC/dV* can be measured using a capacitance sensor and a lock-in amplifier. The principle of operation for a lock-in amplifier such as the SR510 can be found from http://www.srsys.com.

The capacitance sensor has been designed and has the ability to detect capacitance

changes in the order of less than an atto-Farad (10^{-18} F). The AC component of the capacitance sensor output depends on the magnitude of the depletion-layer capacitance change that in turn is a function of the modulation voltage. By measuring the sensor output using a lock-in amplifier, dC/dV can be measured directly, and therefore the dopant concentration can be determined without differentiating the raw capacitance-voltage data. Since the magnitude of dC/dV depends on the local dopant concentration, by rastering the sample beneath the tip and measuring dC/dV while the tip moves across a region of changing dopant density, 2D dopant concentration profiles can be obtained. Also, the sign of dC/dV depends on the local dopant type, thus making the SSCM technique ideal for pn junction delineation with high spatial resolution. Compared with other dopant profiling techniques, there are several attractive features of the SSCM technique:

1) By combining the AFM technique with the Schottky contact depletion C-V approach, both topography and dopant profiles can be obtained simultaneously with high spatial resolution. The SSCM measurement is a quick method. Typically, it takes less than one minute to measure a 1D profile, or five minutes to obtain a whole 2D image. Quick characterization is very suitable for the analysis of real devices in manufacturing fabrication.

2) SSCM measurements can be applied directly on the sample surface or its cross-section without beveling. The beveling technique can be used to magnify the region to be examined; however, the dopant distribution may be altered after beveling.

3) SSCM is a nondestructive technique. The same images are always obtained in the same area regardless of scanning times. One sample can be used many times without damage. This feature leads to a high degree of reproducibility.

4) The SSCM approach is based on the measurement of carrier density, rather than dopant density directly **[60]**. However, it has been shown that when the dopant density varies moderately over a scale comparable to the Debye length (Debye length is 13 nm at concentration of 10^{17} cm^{-3} and 0.4 nm at 10^{20} cm^{-3}), the carrier density is a reasonably good measure of the activated dopant density **[43]**.

5) No extensive sample preparation is needed for SSCM measurements. First, the sample to be imaged is sawed or cleaved to expose its cross-section. The sample cross-section is then polished by a series of diamond lapping films with different grit sizes. Finally, the sample surface is finished with colloidal silica and rinsed with de-ionized water to remove any chemical solution that might be left on the surface. The test sample can be imaged immediately following the polishing process. It has been shown in [59] that the SSCM measurements are relatively insensitive to surface conditions. Therefore, SSCM measurements can be performed in air and do not require high vacuum. However, it is still important to clean the surface of native oxide to maintain the integrity of the contact as Schottky rather than MOS (Metal-Oxide-Semeconductor structure). The surface native oxide can be removed using a HF solution.

6) Due to the absence of any insulating layer between the tip and the sample surface, the SSCM measurement is free of problems caused by trapped charge and charge migration. Also, the absence of insulation reduces both the complexity and time for sample preparation.

7) The spatial resolution obtained by the SSCM technique can be very high depending on the contact area. A small contact area can be achieved by using a sharp micro-machined probe tip and maintaining a small contact force between the tip and the sample. Typical commercial tips have a radius of curvature less than 30 nm.

The SSCM technique also has several drawbacks:

1) SSCM does not directly measure the dopant density. The measured capacitance data need to be converted to dopant density either by modeling or by means of a calibration curve.

2) The spatial resolution is limited by the tip size and the Debye length. The doping profile determined by the C-V method should be expected to provide a spatial resolution of the order of a Debye length [9]. The Debye length is a function of carrier density (it is inversely proportional to the square root of carrier density). The theoretical calculation of the Debye length suggests that higher spatial resolution can be achieved for higher

dopant density.

3) As with conventional SCM, SSCM measurements at constant bias voltage (constant voltage mode) with non-homogeneous dopant profiles are also subject to a spatial resolution that varies with dopant density. Operating SSCM in constant capacitance mode can solve this problem. However, this mode of operation has not been implemented in our SPM laboratory to date.

In this thesis, SSCM has been used to delineate pn junctions of real semiconductor devices. Dopant profiles of state-of-the-art devices such as MOSFETs and BJTs have been imaged. To demonstrate the ease of use and potential of this technique, working semiconductor devices in very large scale integrated circuits (VLSI) such as devices from a 486 DX microprocessor chip were also imaged. In order to obtain the dopant density from the measured capacitance signal, either modeling or calibration curves are required. The later approach has been used in this thesis. Calibration curves were obtained by measuring dC/dV of a series of standard samples with known dopant densities. The measured capacitance image was imported into the Mathlab software package in the form of a two-dimensional matrix. Each element of the matrix represented the magnitude of measured dC/dV at each pixel on the original image. By comparing dC/dV at each pixel to the calibration curve, the 2D dopant density was calculated.

For both conventional SCM and SSCM, the heart of these microscopes is a capacitance sensor. A new high frequency, ultra sensitive capacitance sensor has also been designed and used for SSCM measurements in this research. With this new capacitance sensor, a sensitivity of about 1×10^{-21} $F/\sqrt{Hz}$ measured in a 1 Hz bandwidth with a peak-to-peak sense voltage on the probe tip of less than 500 mV was achieved.

1.5 Scope of the Thesis

This thesis presents the use of SSCM for semiconductor device analysis. The initial work on this technique was done and used by former researchers at the University of Manitoba to delineate a variety of devices [59]. Significant improvements in the SSCM instrumentation in terms of resolution have been made by employing a newly designed capacitance sensor and micro-machined probe tips. Furthermore, calibration curves have been constructed and a conversion algorithm developed to convert the measured capacitance signal to dopant density. The organization of this thesis is briefly described as follows:

- Chapter 2 describes the experimental setup. All the components required for SSCM measurements are discussed in detail.
- Chapter 3 gives the theoretical and practical considerations for operation of the SSCM. The metal-semiconductor model is presented. The parameters that make up the model are also estimated. These parameters are used to simulate the performance of the designed capacitance sensor in the following chapter.
- Chapter 4 presents in detail the design of the capacitance sensor. Factors that affect the sensitivity of the sensor are addressed. The performance of the sensor is tested and compared to the simulation results.
- Chapter 5 presents experimental results obtained by the SSCM measurements with the newly designed capacitance sensor. Various state-of-the-art semiconductor devices are imaged and analyzed.
- Chapter 6 concludes the thesis with the conversion algorithm that is used to convert the measured dC/dV data to carrier concentration. Both 1D and 2D carrier concentrations of some images obtained in Chapter 5 are presented. The limitations of this analysis method are discussed.

CHAPTER 2

INSTRUMENTATION & EXPERIMENTAL SETUP

2.1 Introduction

Operation of the Schottky Scanning Capacitance Microscope (SSCM) is based upon the measurement of the depletion-layer capacitance between a nanometer scale conducting tip and a sample. An Atomic Force Microscope (AFM) is used to position the conducting tip on the sample surface and keep a constant force between the tip and the sample. The topography of the sample surface can be obtained using the AFM. A capacitance sensor is electrically connected to the tip and a bias voltage is applied to the sample with the tip being grounded. The tip-sample contact capacitance is measured as a function of applied bias voltage. By scanning the tip over the sample surface, both topographic and capacitance profiles are obtained simultaneously.

In order to make full use of the SSCM's potential for high resolution measurements, a system should be capable of providing fine control of the SSCM probe position with respect to the sample. The system must be able to control the probe position in the plane parallel to the sample surface (X, Y plane), and the vertical separation between the probe and the sample (Z). Fine control in the X, Y plane is required to obtain high resolution two-dimensional capacitance measurements. Fine control in the Z direction is required to maintain a low probe-surface contact force, thus maintaining a small contact area. As a result, high resolution can be obtained. Using an AFM, the position of the probe tip can be precisely controlled in three directions X, Y, Z.

2.2 Atomic Force Microscope (AFM)

In 1986 Gerd Binnig and Hemrich Rohrer shared the Nobel Prize in Physics for inventing the Scanning Tunneling Microscope (STM) and discovering that it can distinguish individual surface atoms and provide unprecedented resolution in images of surfaces. The success of the STM has led to the invention of a host of other scanning probe microscopes which rely on scanning a sharp tip over a sample surface. The AFM is one of the most successful of the new SPMs [61]. The AFM was developed and primarily used as a device to resolve topographical surface features. It measures the force on a sharp tip created by its proximity to the surface of the sample.

Topographic AFM images can be obtained as follows: 1) A cantilever with a sharp tip is placed in contact with the sample surface as shown in Figure 2.1. 2) The sample under test is mounted on a piezoelectric tube which is used to scan the sample beneath the probe tip. 3) Upon encountering a surface feature, the probe is deflected vertically. The probe's deflection is detected, and a control signal is produced. 4) A feedback loop is employed which responds to the control signal by moving the sample in such a way that the interacting force (repulsive force) between the tip and sample is kept constant throughout the entire scanning process. 5) Topographic images of the sample surface can be depicted by recording the variation in the vertical Z position as the tip scans across the surface.

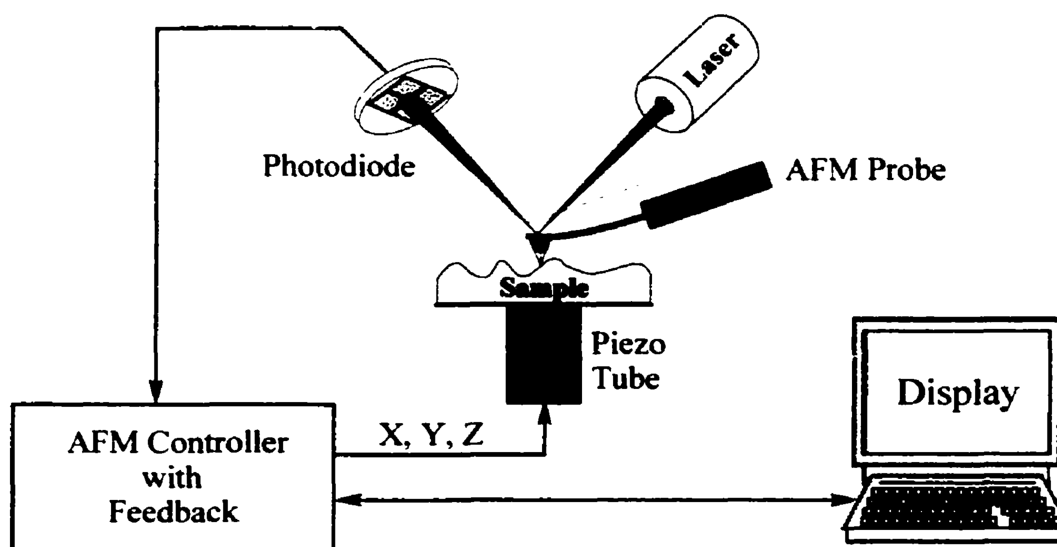


Figure 2.1 Schematic view of the AFM operating principle.

The spatial resolution of the AFM operating in contact-mode is of order of 10 nm in the X, Y plane, and less than 1 nm in the Z direction. The AFM achieves such high resolution by using a probe with a small radius of curvature, and by applying a very small loading force on the tip (on the order of 10^{-7} to 10^{-11} N) which makes the contact area between the tip and the sample exceeding small. The spring of the cantilever used by the AFM is a critical component in order to track the surface at or approaching the atomic level. The spring should be as soft as possible to maximize the deflection for a given force. Since more movement of the cantilever yields a more detectable signal, a better signal to noise ratio can be obtained. At the same time, a stiff spring with high resonant frequency is required in order to minimize the sensitivity to vibration noise from the building (near 100 Hz). By modeling the tip and cantilever as a simple mass spring system, the resonant frequency of the cantilever is given by **[61]**

$$f_o = \frac{1}{2\pi}\sqrt{\frac{k}{m_o}} \qquad \textbf{(2.1)}$$

where k is the spring constant of the cantilever, and m_O is the effective mass that loads the spring. A soft spring cantilever can be obtained by decreasing the spring constant k. Equation (2.1) tells us that resonant frequency of the soft cantilever can be made high if the effective mass loading the spring m_O is reduced proportionally such that the ratio k/m_O is kept large. For these reasons, it is not surprising that a typical AFM probe is usually made of a very flexible cantilever with a very small tip attached to its end.

In order to obtain high spatial resolution, the contact area should be kept as small as possible. However, the minimum contact area is limited by adhesive forces between the tip and soft materials **[62]**. Adhesive forces effectively act as an additional load that increases contact area and thus reduces imaging resolution. In some cases, these forces can be as large as 100 nN for various systems operating in air **[63]**. To improve imaging resolution by reducing the adhesive forces, several alternative approaches have been proposed, such as: sharpening the tip, operating the AFM with negative applied forces by slightly pulling the tip away from the surface, or operating the AFM with the tip and sample immersed in water.

However, these approaches also have their own limitations. For example, sharpening the tip can decrease the adhesive forces. However, sharpening increases the risk of sample damage through inelastic deformation. Operating the AFM with negative applied forces can cause the contact to be unstable. Another alternative is to image soft samples in the noncontact mode. This is a second mode of operation commonly used in AFMs (attractive mode). For noncontact mode, a sharp tip is placed in close proximity to the sample surface (typically few nanometers above the surface). The tip is vibrated at a frequency around the resonant frequency of the cantilever. By using a control feedback loop to keep the amplitude of vibration constant when the tip is scanned over the sample surface, a topographic image can be obtained. Since the tip is not touching the sample surface, the tip can be kept sharp for a long period of time, and the risk of damaging the sample due to mechanical contact can be prevented. In ref **[61]**, the AFM was used in noncontact mode while an STM was used to sense the deflection of the cantilever. A lateral resolution of 30 Å and a vertical resolution less than 1 Å was achieved.

2.3 Schottky Scanning Capacitance Microscope Description

Schottky Scanning Capacitance Microscopy has been implemented by combining the AFM and the measurement of the depletion-layer capacitance between a tip and a sample. The instrument is a custom built AFM which was previously developed and constructed in the University of Manitoba SPM laboratory. Figure 2.2 shows a photograph of the SSCM stage that has been used in the lab. A piezoelectric tube scanner is mounted on an aluminum plate supported by two micrometers and a picomotor driver (Model 8701 Newfocus Inc.). These micrometers are used for sample coarse positioning in Z direction prior to scanning. The supporting plate including the piezoelectric tube is held on an X, Y translation stage. Therefore, the region of interest on the sample surface can be easily pre-located using this translation stage. Samples under test are mounted on a piezoelectric tube and scanned beneath

a stationary probe tip. After the sample is mounted, the X-Y-Z translation stage is used to bring the sample to the tip within a few hundred micrometers with the aid of an optical microscope. The picomotor is then used for the final fine approach to the tip until mechanical contact is made. The cantilever deflection and hence the force is controlled by a SPM digital controller that stops the picomotor when the output of the spring deflection sensor is equal to a set-point given by an operator.

The spring deflection sensor used with SSCM is an optical beam bounce system. It consists of a laser source, a laser reflection mirror, and a photo detector. In this beam bounce system, a laser beam is shone on the mirror. This mirror is mounted on a lever that allows it to be positioned such that the reflection of incident laser beam falls on the upper side of the cantilever. The reflection of the beam bouncing off the cantilever is then detected by split cell photodetector. During scanning, the output of the photodetector provides a feedback signal that is used to maintain a constant force on the tip and obtain a topographic image.

The tip used for SSCM measurements can be either an electrochemically etched tungsten wire [59] or a microfabricated probe tip [64]. Tips are electrically connected to a resonator[7] that is stationary located below the spring deflection sensor. The spring deflection sensor and the resonator are mounted on a SSCM stage head which can be freely flipped up and down along its horizontal axis so that a bad tip can be replaced easily.

SSCM measurements are performed at ambient conditions in a dark environment. The SSCM stage is enclosed in an aluminum box that serves as a common ground plane to which all the ground terminals of the measuring equipment are tied. The aluminum box can also reduces the 60 Hz noise coupling into the measurements from the laboratory lights. In order to reduce acoustic noise, the walls of the SSCM box are lined internally with acoustic absorbing foam material. To avoid the natural frequency vibrations (i.e. building vibration or any movement within the laboratory), the SSCM box is placed on a vibration isolation table. The isolation table is made of a massive stone sitting on the air support legs. Additionally, all power supplies and equipments that can generate vibrations such as transformers, computers, are kept away from the isolation table.

7. The resonator is a part of the capacitance sensor. Details of the resonator can be found in Chapter 4.

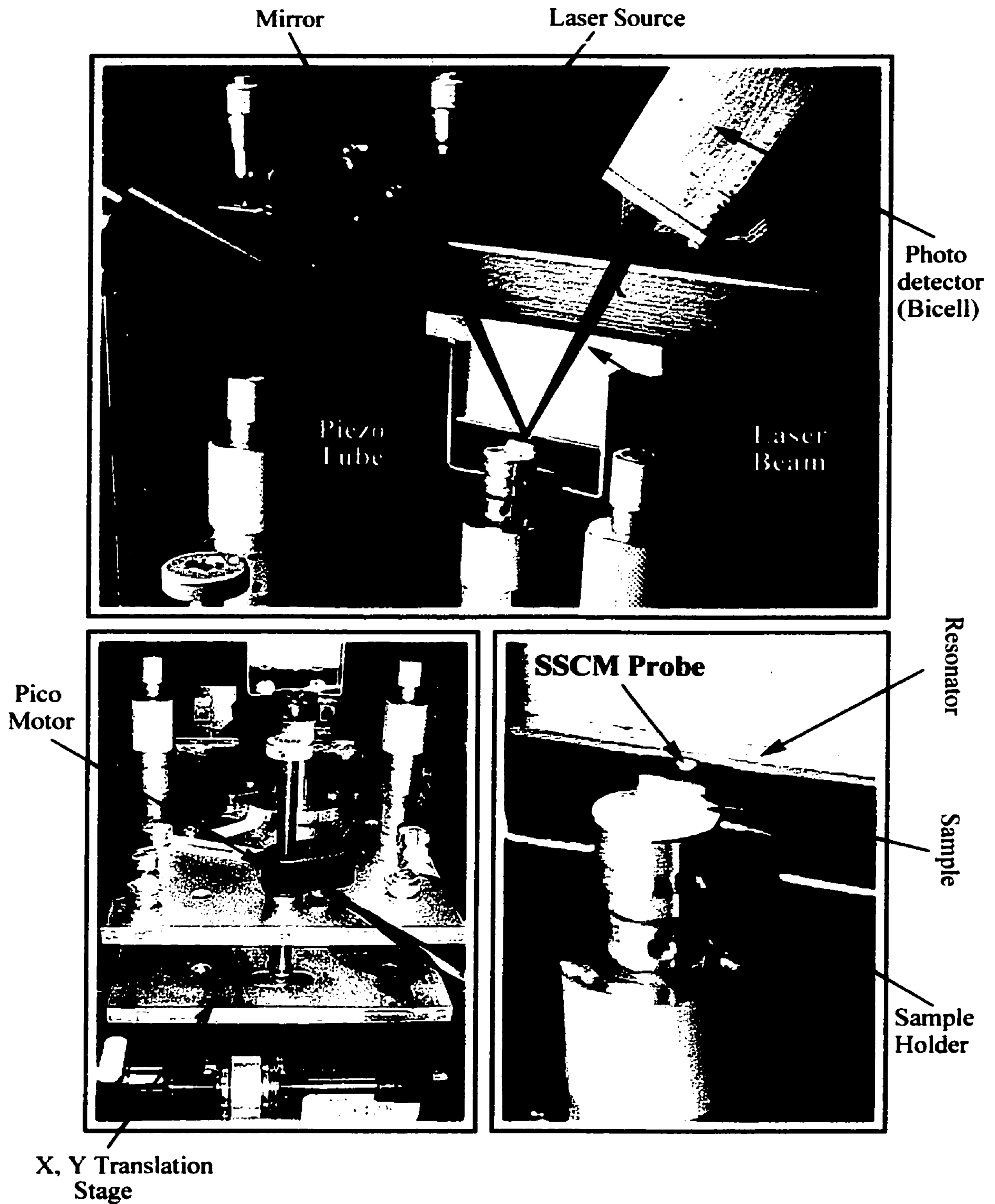


Figure 2.2 A photograph of the SSCM stage and a close up view

2.4 SSCM/AFM Experimental Setup

In this section, the experimental setup for SSCM measurements is described. Figure 2.3 shows a schematic circuit of the SSCM/AFM. One of the main advantages of an AFM based SSCM, is that AFM control of the vertical position of the SSCM probe is performed independently of capacitance measurements. Thus, the AFM can be used to obtain

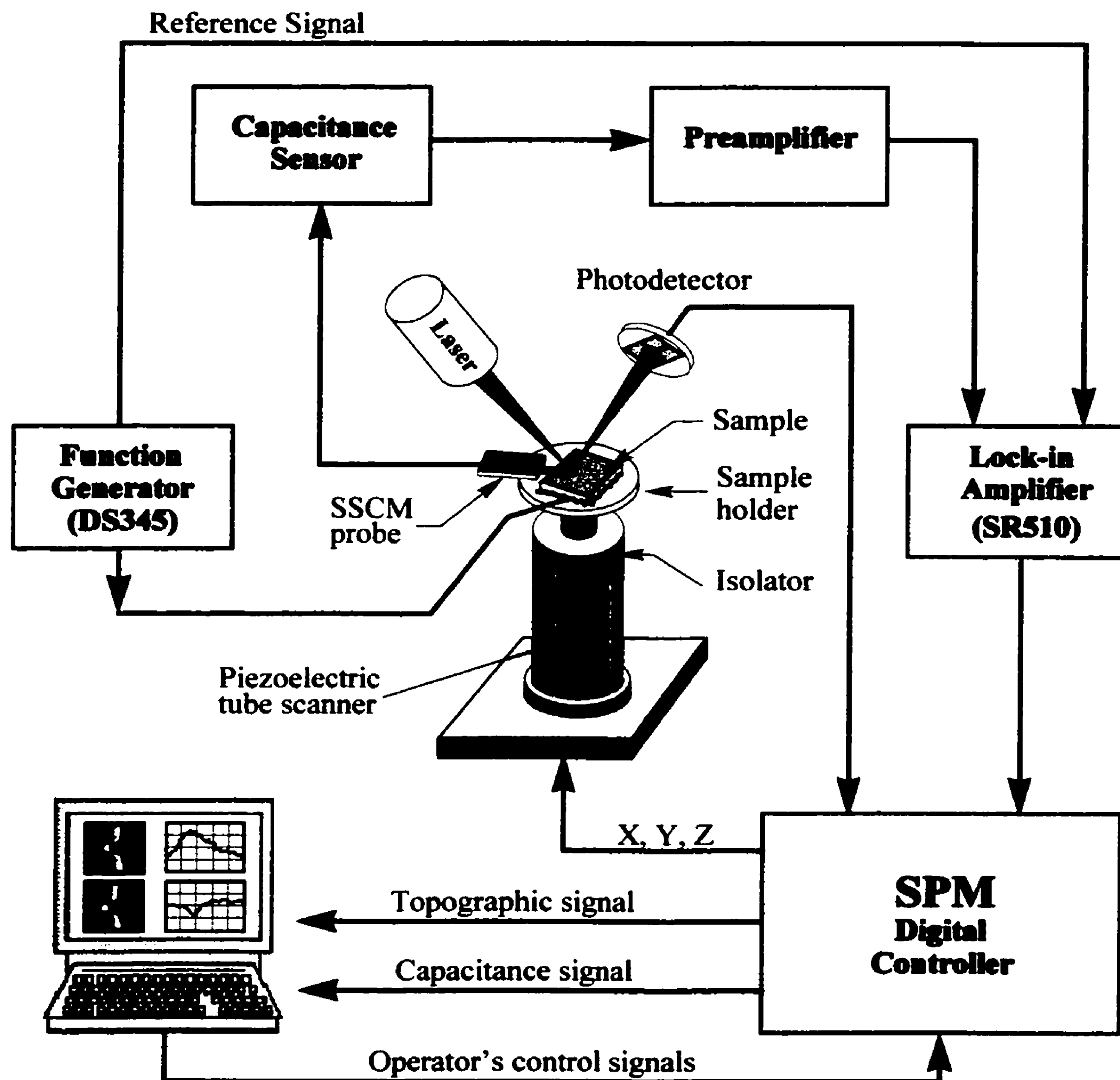


Figure 2.3 A Block Diagram of SSCM experimental setup.

surface topography information, while the SSCM obtains capacitance information. The overall operation principle and that of individual components of the SSCM will be discussed in more detail in later sections of this chapter.

Within this system, the surface topographic profile is resolved in a similar manner to the AFM system described in section 2.2. Here the semiconductor sample being imaged is mounted on a piezoelectric tube and scanned beneath the SSCM probe tip. As the sample is scanned, the cantilever will be deflected vertically due to the change in topography on the sample surface. Deflection of the cantilever is then monitored by an optical beam bounce system that acts as a spring deflection sensor. The output of the deflection sensor is changed as the cantilever is deflected, providing a feedback signal that is used to control the deflection of the cantilever. A SPM digital controller is used that responds to the feedback control signal by adjusting the height of the sample, compensating for the deflection of the SSCM probe. It does this by adjusting the voltage applied to the Z direction of the piezoelectric scanner to move the sample toward or away from the tip such that the output of the deflection sensor is kept equal to a pre-selected set point. As a result, the applied voltage represents the topography of the sample surface. At the same time, the SPM digital controller can also supply the voltages required by the X and Y piezo elements of the piezoelectric scanner to scan the sample in a raster fashion. By recording the voltages applied to the piezoelectric scanner, a two-dimensional topographic image can be obtained.

Along with the topographic image, capacitance profiles can be obtained by measuring the depletion-layer capacitance. Measurements of this capacitance are performed as follows: 1) A small amplitude AC modulation signal is applied to the sample using a function generator (Model Standford DS345), with the tip grounded. 2) Application of the sinusoidal voltage across the Schottky barrier gives rise to a modulation of the contact capacitance due to the change of depletion-layer width. 3) The variation of the contact capacitance is measured by a capacitance sensor which is electrically connected to the SSCM probe. 4) The amplitude of the AC component of the capacitance sensor's output is proportional to the magnitude of the contact capacitance change which is in turn a function of the dopant density in semiconductor body and the modulation voltage. However, its phase depends on the type of semiconductor material. 5) This AC component is amplified by a

preamplifier and detected by a lock-in amplifier (Model SR510). The reference signal used for the lock-in detection technique is provided by the synchronizing output of the function generator. 6) The lock-in amplifier will generate a DC (or near DC) voltage output that depends on the amplitude of its input signal (output of the capacitance sensor) and the phase calibration of the measurement system. 7) The output signal of the lock-in amplifier is then sent to the SPM digital controller for processing and recording on a computer. 8) By keeping the amplitude of the modulation signal constant, the lock-in amplifier's output is related to the dopant density. Therefore, the output of the lock-in amplifier can be used to map out the dopant density while the SSCM tip is scanned across the sample surface.

There are a number of benefits that arise from utilizing the modulation of depletion-layer capacitance. First, the modulation technique allows the separation of very small contact capacitance (order of 10^{-18} F) from a large stray capacitance (order of 10^{-12} F) that is coupled to the SSCM probe from its surrounding environment. Second, the noise spectrum of the capacitance sensor is flat above a few kilohertz. Modulating the depletion-layer at high frequency can minimize the pickup noise signals and also avoid the "1/f" noise of the electronic system. The SSCM measurements are normally performed with a modulation frequency of 80 - 100 kHz from which minimum noise levels can be obtained. Third, the lock-in amplifier technique can be employed, and the noise can be further reduced by selecting an adequate bandwidth. Finally, the surface states at the Schottky contact between the probe and the sample cannot respond to the AC voltage swing when it is applied at high frequencies. As a result, contributions due to these surface states are small enough that they can be neglected during the determination of capacitance.

In the SSCM measurements, the spatial resolution relies on the tip-to-surface contact area which in turn depends on the force between the tip and the sample surface. However, this force can be controlled by the operator by selecting a set-point via the computer interface. The smaller the set point is, the less the cantilever is deflected vertically, and therefore the smaller the contact is. Typically, the set points used for the SSCM measurements are from 100 to 200 mV. This corresponds to a force of 25 nN - 50 nN exerted on the tip (this value was calculated for a microfabricated probe tip described in the next

section). With a cantilever of high spring constant, the set point should be low in order to make the contact area small (small force) to obtain high spatial resolution. Before loading the tip on the sample, care should be taken to ensure that the laser beam reflected off the cantilever falls on the center of the split cell photodetector, with half of the laser beam falling on each cell. In the other words, the photodetector should be aligned such that its output signal is as close to zero as possible. Failure to do this can cause the cantilever to be broken when the picomotor is used to bring the sample in contact with the tip. Details of the photodetector can be found in an appendix A.

2.5 The SSCM Probes

There are several different types of probes used in SPM applications. These probes are characterized by the properties required for the particular type of microscope they are to be used with. Some of these properties are: tip sharpness, cantilever resonant frequency, and whether or not the tip is conductive. For SSCM, the tip needs to be sharp and highly conductive. Within the last couple of years, two types of tip-cantilever system have been employed in the SSCM measurements in our laboratory. These are: (1) electrochemically etched tungsten wires, and (2) microfabricated probe tips.

2.5.1 Electrochemically Etched Tungsten Probe

Tungsten tips are made by simply electrochemically etching tungsten wire. A tungsten tip is fabricated as follows: 1) One end of a tungsten wire of diameter of approximately 250 μm is placed in a bath of 4M NaOH solution. 2) The wire is typically biased at 10 V with respect to a second electrode that is also placed in the etching solution. 3) The resulting current passes through the tungsten wire, into the solution, and is collected by a second electrode. After a short period of time (a few minutes), the submerged part of the tungsten is etched away and the tungsten wire is broken at the etching point. 4) Since the

etching process is anisotropic, that is it has different etching rates in different directions, a very sharp tip is formed at the end of the tungsten wire. A tip with a radius of curvature of 100 nm can be obtained by this method [59]. The tip is mounted in a tube that has been attached to the end of a triangular shaped stainless steel foil cantilever. In another approach, the etched tungsten wire can also bent at an angle of 90° so that tip and cantilever can be made by a single tungsten wire. The advantages of using tungsten tips are their low-cost and ease of fabrication. However, drawbacks are relatively poor repeatability of sharpness and shape.

2.5.2 Silicon Microfabricated Probe

Silicon tips are used for most commercial AFMs and are commercially available. With state-of-the-art micromachined technology, the silicon tips can be made with repeatable shape and radius of curvature. The typical radii of curvature are 10-30 nm. AFM tips are micromachined using standard microlithographic methods. They are made in batch processes from either silicon or silicon nitride, making them very reliable and relatively inexpensive. Silicon nitride is unusually resistant to mechanical fatigue. Probes constructed from this material can be flexed through an angle 90° and back to their relaxed position without breaking.

Silicon microfabricated tips have several advantages. Firstly, identical tips can be made by the current micromachined technology. The Scanning Probe Microscopes have widespread use as metrological tools. Since the critical metrological parameters like resolution and sensitivity are determined by the tip size and shape, similarity of tips is very important. Secondly, silicon tips can easily be mass-produced. Therefore, these commercially available tips support commercialization of the SPMs for dopant profile measurements. Finally, the cantilevers of silicon tips are usually made flat and can be coated with other materials such as metals. This is useful in spring deflection sensing techniques.

In this thesis, microfabricated silicon tips (Model NT-MDT SCS12/W_2C coated series) are utilized for SSCM measurements. These tips are purchased from the NT-MDT

company. Figure 2.4 shows close up SEM images of the tip and cantilever that has been fabricated by the NT-MDT. The dimensions of the chip (probe mount) from which cantilevers are mounted on are also given in Figure 2.4(a). Probes consist of a flexible cantilever and a cone shaped tip that is located very close to the edge of the cantilever. Tips and cantilevers are fabricated on a single piece of silicon wafer. Fabricated probes are then attached to a silicon chip that is 1.6 mm wide, 3.6 mm long, and 0.45 mm thick. This chip acts as a probe mount and is used for handling purposes. After fabrication, the tip and cantilever side of the chip are heavily doped with boron. The dopant concentration of the tip is unknown. Hcwever it is expected that most of silicon doped tip has dopant density higher than 10^{20} cm^{-3}. Since the dopant density of real devices is usually below 10^{20} cm^{-3}, the depletion in the tip is much weaker than that of the devices. In order to increase the conductivity and minimize the oxidation of tip surface, tips and the cantilever side of the SCS12 chip are coated with 25 nm

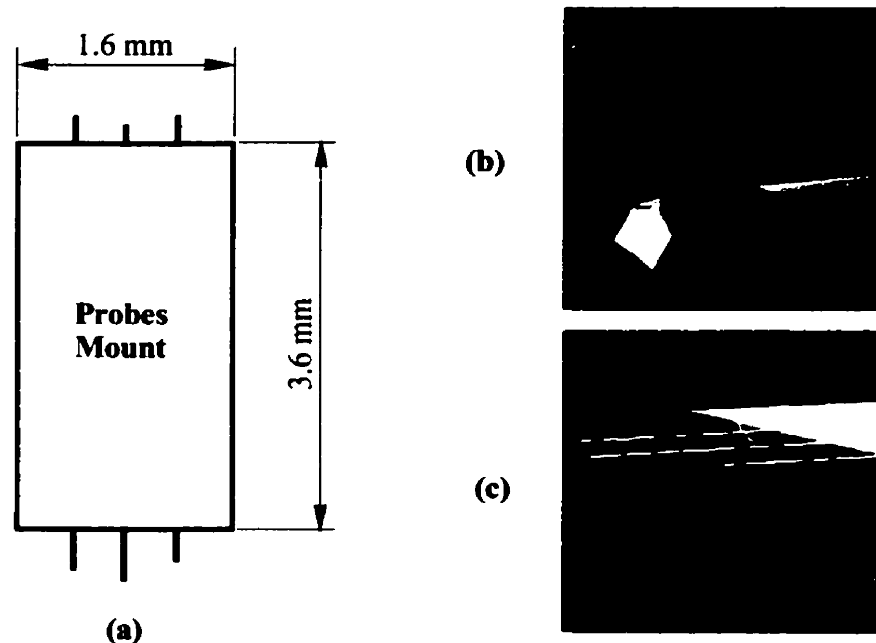


Figure 2.4 Images of the microfabricated silicon probe (NT-MDT SCS12 series).
(a) Dimension of the chip (probe mount with 6 straight cantilevers)
(b) Close up SEM image of the SCS12 silicon tip
(c) Close up SEM image of the SCS12 silicon cantilevers at the edge of the chip.

tungsten carbide film. The upper side (reflective side) of cantilever is coated with aluminum film to increase the reflectivity to that found to be useful for optical deflection detection methods. Metal coatings on the reflective side of cantilever can also prevent light penetration into the silicon cantilever and its reflection from the other surface. Besides increasing the conductivity, coating tips with metal has several advantages including high mechanical stability, high chemical stability, low tip surface oxidation, and high resistance to tip wear. However, its drawback is the increase in the tip's radius of curvature. A typical radius of curvature of the SCS12 tip including coating is in order of 30 nm. Without coating, it can be as small as 10 nm.

The silicon cantilever of the SCS12 series is normally shipped along with six straight cantilevers mounted on a single chip. There are three on each side of the chip (see Figure 2.4(c)). These cantilevers have identical tips. However they have different characteristics such as length, spring constant, and resonant frequency. The variety of cantilevers on a chip allows for easy selection of a spring constant appropriate for a particular application. For SSCM measurements, the longest and softest cantilever is usually chosen to minimize the probe-surface contact force. However, the other types of cantilevers can also be used. The cantilever chip is glued onto the transmission line resonator that is a part of the capacitance sensor, using silver epoxy to make a good electrical contact. Because there are three cantilevers on each side of the chip, care should be taken to prevent the contribution of the unused tips to the measured signal. Touching unused tips on the sample surface while scanning can result in a double image.

2.5.3 Mechanical Characteristics Of The SSCM Probe

Besides the sharpness of the tip, mechanical characteristics such as force constant and resonant frequency of the cantilevers are important parameters for SSCM measurements. The force constant of the cantilever plays a part in the spatial resolution of the SSCM. A low force constant is required to minimize the probe-surface contact force. The mechanical resonant frequency controls the speed at which the surface can be tracked. A high resonant

frequency would enable the scans to be made at higher speed.

The force constant (spring constant), k, is defined as the amount of force required to deflect the cantilever. The force constant of a single rectangular beam of length "*l*" and moment of inertia "*I*" is given by **[65][100]**:

$$k = \frac{3EI}{l^3} \text{ N/m} \quad \textbf{(2.2)}$$

where E is the Young's modulus of elasticity of the beam material[8]. The moment of inertia depends on the cross section of the beam. For a rectangular cross-sectional beam with a width "*w*" and thickness "*t*", the moment of inertia "*I*" as given in **[100][101]** is $I = \frac{wt^3}{12}$. Substituting *I* into equation (2.2), the force constant becomes:

$$k = \frac{Ewt^3}{4l^3} \text{ N/m} \quad \textbf{(2.3)}$$

The resonant frequency of a solid rectangular lever with a concentrated load one end is given by **[42]**:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{Ewt^3}{4l^3(m_c + 0.24wtl\rho)}} \text{ Hz} \quad \textbf{(2.4)}$$

where ρ is the density of the cantilever material[9], m_c is a concentrated mass loaded at one end of the cantilever (tip's mass). From the given dimensions of a rectangular cantilever that are frequently used in our laboratory, the force constant and resonant frequency can be calculated using $E = 1.5\text{x}10^{11}$ N/m^2 (assuming that tip's mass is very small so that it can be neglected in

8. Young's modulus of silicon ranges from $1.4\text{x}10^{11}$ to $1.8\text{x}10^{11}$ N/m^2
9. Density of silicon is 2328 kg/m^3

equation 2.4).

Cantilever physical dimensions

Cantilever thickness: 2.0 μm

Cantilever width: 35 μm

Cantilever length: 350 μm

Calculated force constant k = 0.25 N/m

Calculated resonant freq f_r = 21 kHz

The theoretical values of force constant and resonant frequency are calculated from a model in which the cantilever is fixed at one end. In practice, these values may differ since the tip is in contact with the sample surface. It was shown in [94] that the resonant frequency of the cantilever should be increased when the SSCM is in operation. In addition, the metal coating layer on the cantilever may also effect the calculated values for the force constant and resonant frequency. However, since this coating layer is very thin (~ 25 nm), the contribution of the coating is expected to be small.

2.5.4 Tip Artifacts

Electrochemically etched tungsten wire and microfabricated probe tips have successfully been used for the SSCM measurements in our laboratory. Although tungsten probes are easily made, tungsten is very brittle. It has been observed and shown in [42] that cutting a tungsten wire sometimes results in formation of a crack that runs along the length of the wire. After etching, a wire with a crack will form in a tip that is split into two and is referred as double-tip artifact. Imaging the sample with this tip can cause the surface features to be repeated.

The double-tip artifact has also been observed when a microfabricated tip is used for the SSCM measurements, especially when the tip and the sample are used for a long period of time. The source of this artifact is not understood. However, there are two factors that may cause this effect. First, it is suggested that the metal coating layer on the tip may flake off and be dragged along with the tip while the tip is scanned on the sample surface. Second, it may be due to sample surface contamination. Sample surface contamination may deposit foreign conducting material on the tip around its apex. The double-tip artifact has not been observed when the SSCM measurements are performed using a new tip and a cleaned sample surface. Therefore, keeping the sample surface clean is important.

Figure 2.5 shows the topographic and capacitance (dC/dV) profiles of a test "Round Robin P-MOS" device with a double tip effect. In Figure 2.5(b), the dark region represents the P-type Source/Drain of the device and the white region is the N-type substrate. Gates are located at the center of the images. From these images, a double transistor is clearly visible in which one is located beside the other.

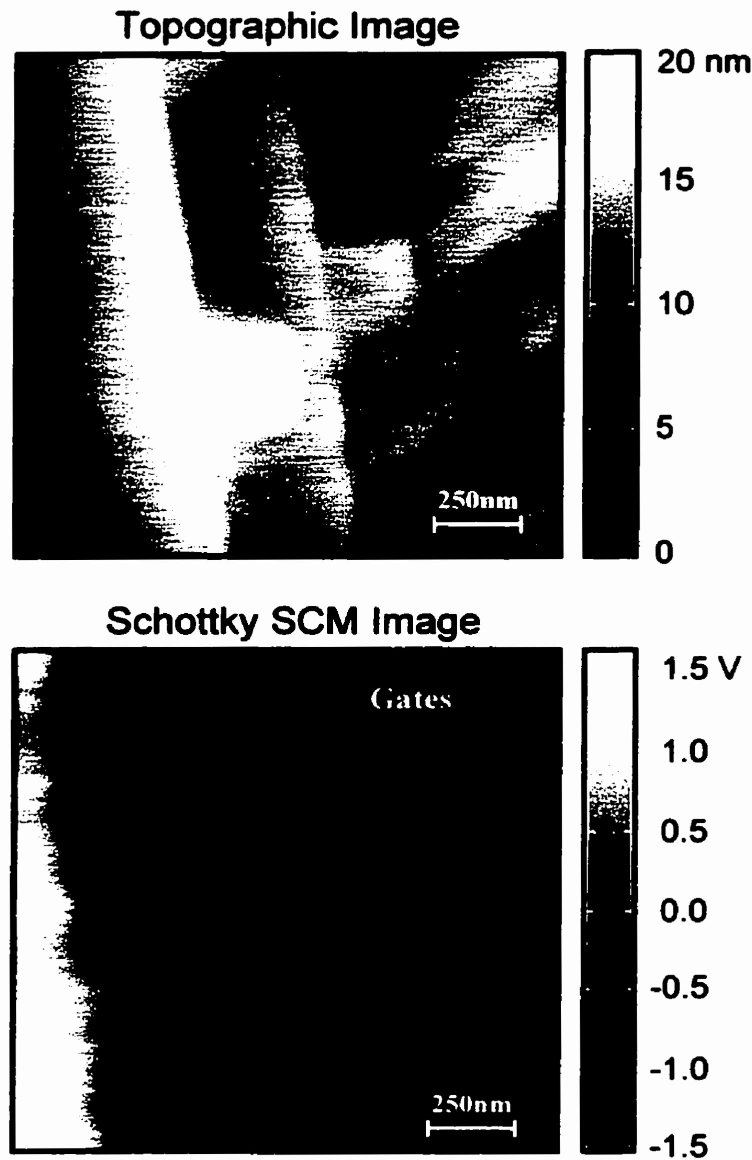


Figure 2.5 Profile of a P-MOS device showing an example of a double tip artifact. It should be noticed that the units used for the Schottky SCM image are the units of the lock-in amplifier output (volts).

2.6 Sample Preparation

In this work, all SSCM measurements were performed on the cross-sectional surface of a sample. However, SSCM can also be performed on the top surface. Sample preparation starts by cleaving or sawing to expose the cross-sectional surface. The back of the cleaved sample (substrate side) is scratched with a diamond pen in order to make an ohmic contact for the modulation signal that modulates the depletion-layer capacitance. The sample is mounted in a cross section orientation on the side of a sample holder using silver epoxy to make a good electrical contact. The sample holder is a cylindrical aluminum block (Figure 2.6). A portion of the sample holder is removed along the cylindrical axis to provide a flat surface to which the sample is attached.

The sample and its holder play an important role in the determination of the capacitance sensor sensitivity. Sensitivity is significantly decreased if the cantilever hangs over the substrate of the sample under test. The area that the sample holder covers underneath the resonator also contributes to a reduced sensitivity. The larger the area is, the lower the sensitivity becomes. This is due to larger amount of stray capacitance coupled to the resonator. For this reason, the sample should be mounted such that the substrate is facing the sample holder and devices are oriented away from the holder. During the SSCM measurements, the tip is scanned on the sample surface such that the cantilever is on the side opposite the sample holder. This configuration prevents the cantilever from hanging over the substrate and minimizes stray capacitance.

A piece of thin glass is attached to the sample on the side of interest (Figure 2.6(b)). There are two reasons for attaching the glass. First, glass mounted on the sample face prevents chipping of the edge of interest during polishing. Second, it supports the tip during scanning so that tip does not fall off the edge of the sample surface.

A signal wire is the attached to the silver epoxy. The epoxy is left to cure in a heated oven at 120° C for about 20 minutes. Silver epoxy upon hardening bonds the sample to its holder firmly.

After baking, the sample is polished with a series of diamond lapping films. The

initial polish is obtained using a 15 μm diamond film, followed by 6, 3, 1, and 0.5 μm films. The final polishing is accomplished with 0.05 μm colloidal silica. The sample is then rinsed with de-ionized water to remove any remaining contamination from polishing process. Before imaging, the polished sampled is cleaned with an acid (HF solution) to remove native oxide. Samples that have been exposed to air for a significant length of time are also cleaned with HF to ensure a clean cross section for imaging.

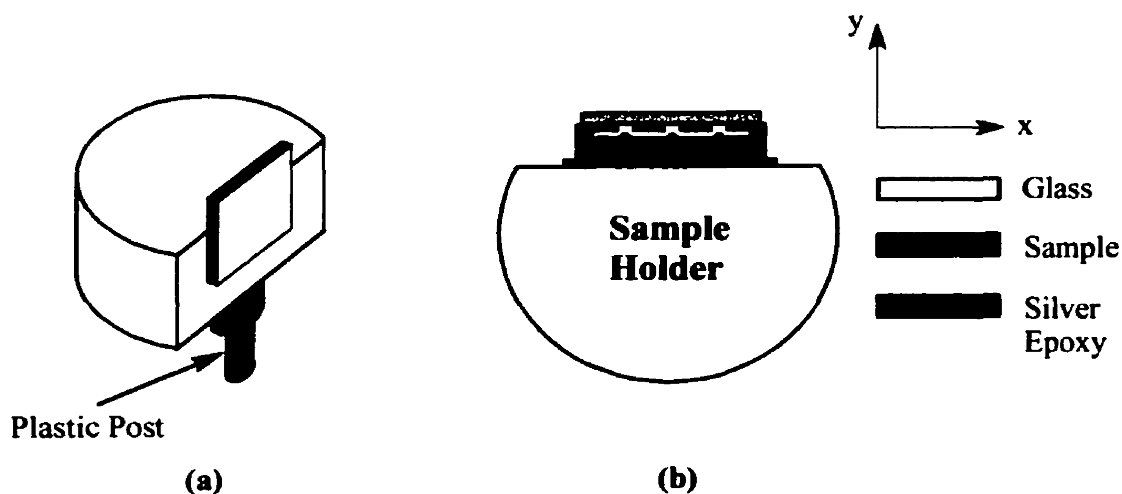


Figure 2.6 A drawing showing how the sample is mounted on the sample holder
(a) A pictorial view of a sample holder including a sample
(b) A top view of Figure 2.6(a)

CHAPTER 3

THEORETICAL CONSIDERATIONS

Carrier profiles with SSCM are based on the measurement of the junction capacitance formed between a conducting probe tip and the semiconductor surface. Therefore, it is important to develop an energy band model for the junction that can be used to interpret SSCM data. In this chapter, the electrical properties of the tip-silicon junction for a conducting tip are analyzed. The analysis is based on the well known theory of the metal-semiconductor junctions. An equivalent circuit representing the metal-semiconductor contact is constructed and the components of this circuit are calculated based on the properties of the metal making up the tip and the type of semiconductor. Calculated values of the equivalent circuit's elements are used as input parameters for simulating the performance of the capacitance sensor presented in Chapter 4.

3.1 Schottky Contact Capacitance Measurements

As mentioned in Chapter 2, the dependence of variations in junction depletion layer width (depletion layer capacitance) on the ionized impurity concentration at the edge of the depletion layer is the basis for determining impurity concentration using SCM. A schematic diagram for the depletion-layer capacitance measurement is shown in Figure 3.1. Here a conducting tip is placed in contact with the semiconductor sample. The tip is biased with an AC modulation voltage added to a DC bias (the sample is grounded). The AC voltage modulates the depletion layer width resulting in the change in the depletion-layer capacitance. The variation of the tip-to-sample capacitance is then measured by a capacitance sensor and lock-in amplifier. In previous work, the capacitance measurements were

performed by employing the RCA capacitance sensor. The schematic of capacitance measurement using this sensor is shown in Figure 3.1. Now, a newly designed capacitance sensor is used. Due to the configuration of the new design, the bias voltage is applied to the sample and the tip is grounded. However, the results obtained by both are the same.

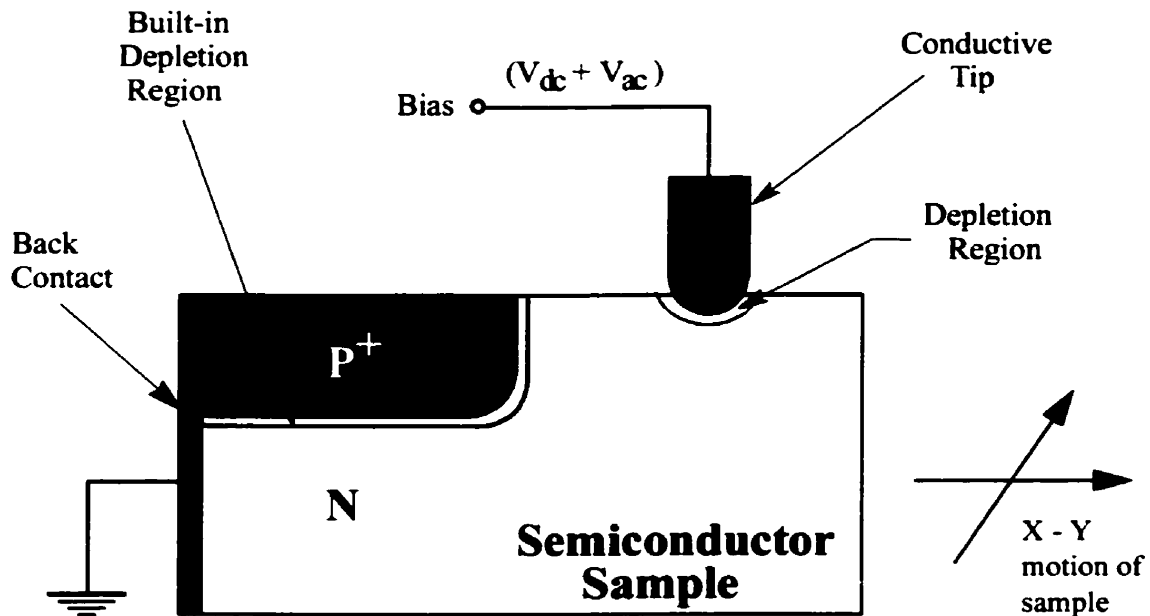


Figure 3.1 Schematic circuit of an SSCM that shows space charge regions at the interface between the conducting tip and the sample

3.2 Equivalent Circuit

When the SSCM is in operation, a conducting tip is scanned across the sample surface in a raster pattern. A scan rate of 0.5 to 1 Hz (2 to 1 s/line scanning rate) on the fast axis is normally used in SSCM imaging. For modelling purposes, however, it has been assumed that the tip is stationary relative to the sample surface while a measurement is being taken at each point. This is reasonable since the RF probe frequency is typically 2 - 3 GHz. An equivalent circuit of the tip-sample looking from the tip side toward the sample can be

modeled as shown in Figure 3.2. In this circuit, the tip-surface junction is modeled as a parallel combination of a capacitor (depletion capacitor) and a resistor (contact resistor) connected in series with a bulk spreading resistance (a circuit that is enclosed in an upper shaded rectangula). R_C is the contact resistance experienced by carriers when they cross the junction interface. This resistance is a consequence of the potential barrier that exists at the interface after the semiconductor and tip are brought into contact in thermal equilibrium. The presence of the potential barrier implies that the region is depleted of majority charge carriers. The space charge region located at the interface results in the formation of a junction capacitance C_C. R_{sp} is the spreading resistance under the probe tip. The spreading resistance is the resistance experienced by charge flowing within the body of the sample in the vicinity of the tip.

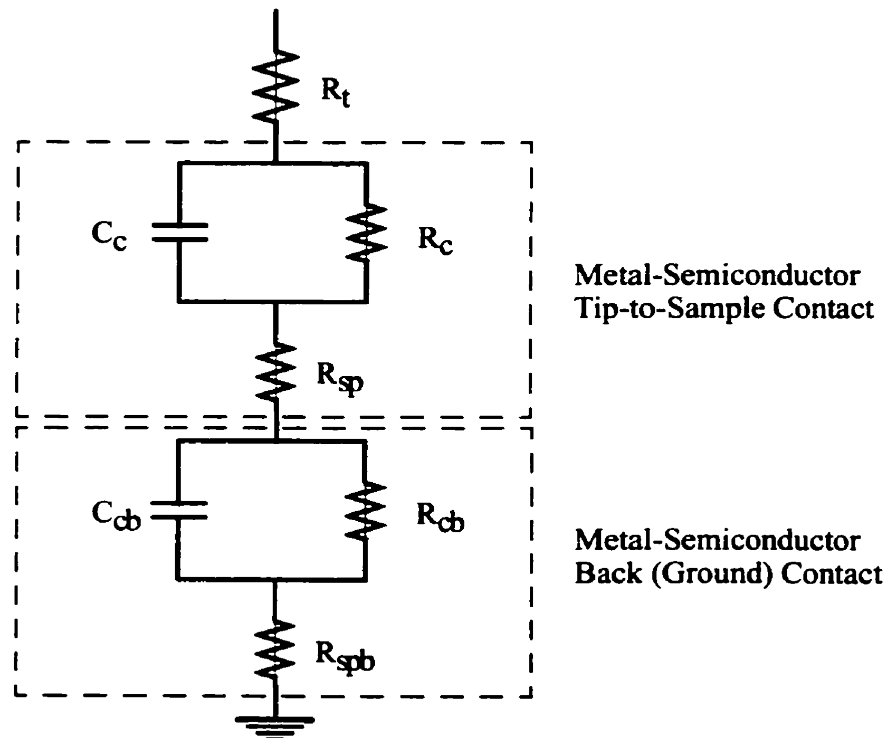


Figure 3.2 An equivalent circuit of a metal tip on a semiconductor sample

As mentioned in section 2.6, the sample is mounted on its holder using silver epoxy. The back of the sample (substrate) is scratched with a diamond pen to make a good electrical contact with conductive silver epoxy. The substrate and silver epoxy form another metal-semiconductor contact. The expected equivalent circuit of the back contact is therefore the same as the tip-sample contact and it is indicated in a lower dashed rectangle in Figure 3.2. Because the back contact area is very large (at least few mm^2 or more) compared to the tip-sample contact, the spreading resistance and contact resistance of the back contact is small and can be neglected when an equivalent circuit of the tip-sample is modeled. Furthermore, the back contact capacitor is much lager than the tip-sample depletion capacitor. Since these capacitors are connected in series, the equivalent capacitance is of the order of the tip-sample depletion capacitance.

Other components that should be mentioned are stray capacitance and tip resistance R_t. Stray capacitance is formed by field lines that are coupled to the probe from the environment surrounding the probe. Because the SSCM probe is made of silicon, it is expected that the probe (including the probe mount) has a finite resistance. The presence of these two components may effect the performance of the capacitance sensor. They are discussed in Chapter 4.

3.3 Metal-Semiconductor Contact Capacitance Formation

The potential barrier formed when metal contacts a semiconductor arises from the separation of charges at the metal-semiconductor interface such that a high-resistance region devoid of mobile carriers is created in the semiconductor. The depletion capacitance of this barrier for a given probe-surface potential difference is a function of the barrier width which in turn depends on the carrier density in semiconductor. Application of a potential difference across the barrier changes the barrier width, which in turn results in a change in the capacitance of the barrier. The analysis below deals with a metal-n-type semiconductor contact. However, the results can be applied to the other types of metal-semiconductor contact.

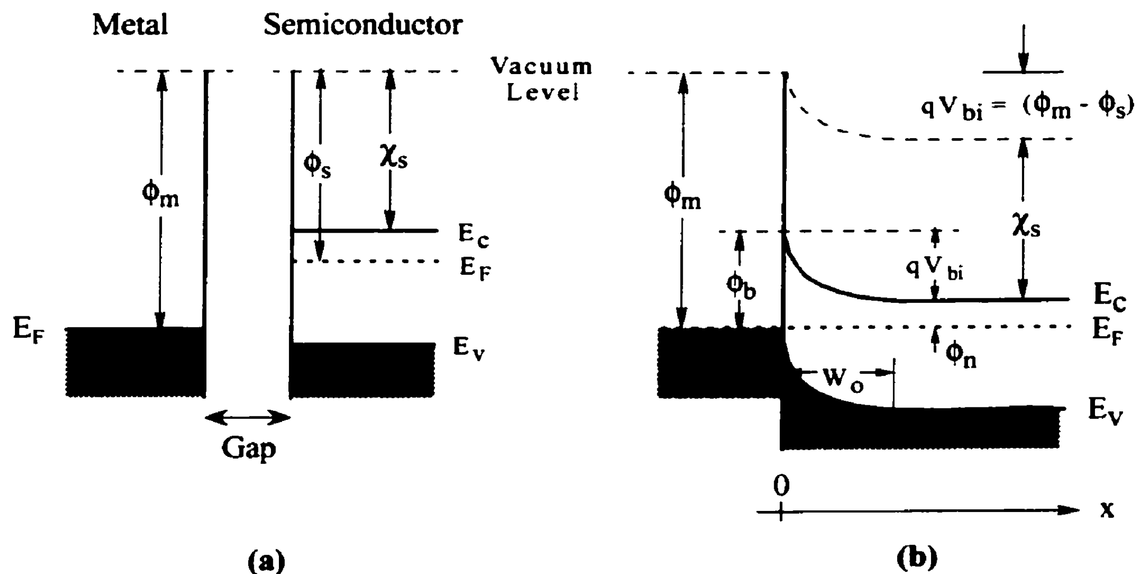


Figure 3.3 Electron energy band diagrams of metal contact to n-type semiconductor with $\phi_m > \phi_s$. (a) before contact, (b) after contact. It should ne noted that the energy levels are full up to E_F and E_V in (a)

The energy band diagrams in Figure 3.3 illustrate the process of barrier formation. The contact is assumed to be intimate, thus there is no interfacial layer present between the metal and semiconductor. Figure 3.3a shows the electron energy band diagram of a metal with work function ϕ_m and an n-type semiconductor with work function ϕ_s which is smaller than ϕ_m. The work function of a metal is defined as the amount of energy required to raise an electron from the Fermi level (E_F) to the vacuum level. The work function ϕ_s of the semiconductor is defined similarly. However, the value for a given semiconductor, besides being influenced by surface contamination, depends on the position of the Fermi level in the semiconductor, and thus upon the carrier density. A surface parameter that does not vary directly with doping is the electron affinity χ_s defined as the energy difference of an electron between the vacuum level and the lower edge of the conduction band (E_C). It should be noted that the semiconductor depicted in Figure 3.3a possesses no net charge at its surface (assuming that there are no surface states) , and therefore there is no bending of the bands at the surface.

When the metal and semiconductor make intimate contact, electrons from the conduction band of the semiconductor flow into the metal until the Fermi level on the two sides is brought into coincidence. The conduction band electrons which cross over into the metal leave a positive charge of ionized donors behind, so the semiconductor region near the metal is depleted of mobile electrons. Thus, a positive charge is established on the semiconductor side of the interface and the electrons which cross over into the metal form a thin sheet of negative charge. These charge layers form a space charge region at the metal-semiconductor interface.

As the electrons move out of the semiconductor into the metal, the free electron concentration in the semiconductor region near the boundary decreases. Since the separation between the conduction band edge E_C and the Fermi level E_F increases with decreasing electron concentration, and since E_F remains constant throughout in thermal equilibrium, the conduction band edge E_C bends up as shown in Figure 3.3b. The valence band edge E_V will move up parallel to the conduction band edge E_C because the band gap of the semiconductor is not changed by making contact with the metal. The vacuum level in the semiconductor follows the same pattern as E_C since the electron affinity of the semiconductor is assumed to remain unchanged even after metal contact is made. The amount of band bending is equal to the difference between the two vacuum levels, which is the difference of two work functions and is given by:

$$qV_{bi} = (\phi_m - \phi_s) \qquad \textbf{(3.1)}$$

where q is the electronic charge, V_{bi} is the built-in potential difference across the junction and is expressed in volts.

3.3.1 Barrier Height of a Metal-n-Type Semiconductor Contact

For an ideal metal-n-type semiconductor contact, the barrier height ϕ_b looking from the metal towards the semiconductor is given by:

$$\phi_b = (\phi_m - \chi_s) \quad \textbf{(3.2a)}$$

Since

$$\phi_s = \chi_s + \phi_n \quad \textbf{(3.2b)}$$

Substituting equations (3.2a) and (3.2b) into equation (3.1) the relationship between the built-in potential and the barrier height of the junction will become:

$$qV_{bi} = \phi_b - \phi_n \quad \textbf{(3.3)}$$

where ϕ_n is the difference between E_C and E_F of the semiconductor, and is given by [9]:

$$\phi_n = kT\ln\left(\frac{N_c}{N_D}\right) \quad \textbf{(3.4)}$$

where k is the Boltzmann constant, T is the temperature, N_D is the dopant concentration of the semiconductor (donor concentration), and N_C is the effective density of states in the conduction band of the semiconductor ($N_C = 2.8\times10^{19}$ cm^{-3} for silicon) [9].

3.3.2 Barrier Height of a Metal-p-Type Semiconductor Contact

For an ideal metal p-type semiconductor contact, the energy band diagram is shown in Figure 3.4 (consider the case of $\phi_m < \phi_s$). As seen from this figure the barrier height ϕ'_b for holes is given by the relation

$$\phi'_b = \chi_s + E_g - \phi_m \quad \textbf{(3.5)}$$

where E_g represents the band gap of the semiconductor. From equation (3.2a) and (3.5) the relationship between the band gap and these barrier heights is obtained as $\phi_b + \phi'_b = E_g$. Similarly, the built-in potential for the p-type semiconductor is given by:

$$qV'_{bi} = \phi'_b - \phi_p \quad (3.6)$$

and

$$\phi_p = kT\ln\left(\frac{N_v}{N_A}\right) \quad (3.7)$$

where ϕ_p is the difference between E_V and E_F of the semiconductor, N_A is the doped acceptor concentration, and N_V is the effective density of states in the valence band of the semiconductor ($N_V = 1.04 \times 10^{19}\ cm^{-3}$ for silicon) [9].

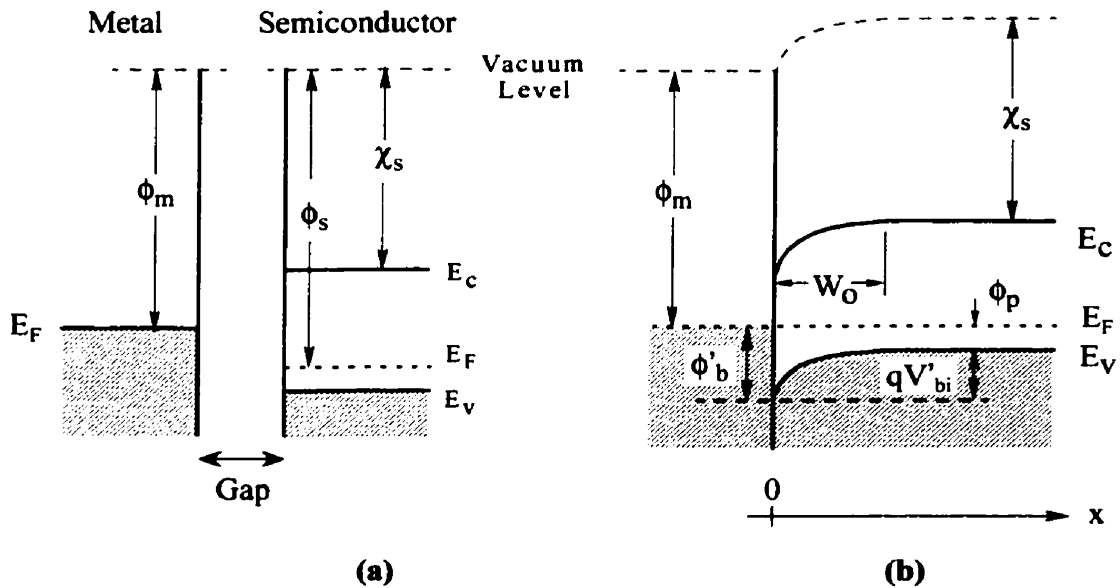


Figure 3.4 Electron energy band diagrams of metal contact to p-type semiconductor with $\phi_m < \phi_s$. (a) before contact, (b) after contact.

In most practical metal-semiconductor contacts, the ideal situations shown in Figure 3.3b and Figure 3.4b are never reached because there is usually a thin insulating layer of oxide (interfacial layer) on the surface of the semiconductor. Also there are several factors that affect barrier height such as bias voltage applied across the metal-semiconductor contact, surface states, and image forces that can lower the barrier height [9][69]. Analysis of these effects is very complicated. To simplify the problem, the metal-semiconductor contact is assumed to be ideal and the factors mentioned above are ignored in the following subsequent calculations.

3.3.3 Barrier Width

For non-heavily and uniformly doped silicon at room temperature, Boltzmann statistics can be used to calculate the carrier densities. It is assumed that the semiconductor is n-type and all the donors are ionized. Taking the potential ϕ to be zero in the neutral bulk region of the semiconductor at the edge of the space charge layer, the majority carrier density n(x) and minority density p(x) are represented by the following expressions:

$$n(x) = n_o \exp\left(\frac{q\phi(x)}{kT}\right) \quad \textbf{(3.8a)}$$

$$p(x) = p_o \exp\left(-\frac{q\phi(x)}{kT}\right) \quad \textbf{(3.8b)}$$

where n_o and p_o represent the equilibrium electron hole concentrations in the neutral semiconductor. At any point in the semiconductor the 1-D Poisson equation can be written as:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_s}[N_D + p(x) - n(x)] \quad \textbf{(3.9)}$$

N_D is the donor concentration, and ε_s is the dielectric constant of silicon. The x-axis is chosen

as shown in Figure 3.3b. Substituting equation (3.8a) and (3.8b) into equation (3.9) the 1-D Poisson equation becomes:

$$\frac{d^2\phi(x)}{dx^2} = -\frac{q}{\varepsilon_s}\left[N_D - n_o \exp\left(\frac{q\phi(x)}{kT}\right) + p_o \exp\left(-\frac{q\phi(x)}{kT}\right)\right] \qquad \textbf{(3.10)}$$

A closed form solution of equation (3.10) is not possible. For simplification purposes, an approximation is made. The approximation is that the free carrier concentrations are assumed to fall abruptly from their equilibrium values n_O and p_O in the bulk neutral region to a negligibly small value in the barrier space charge region. Using this approximation, the equation (3.10) can be written as:

$$\frac{d^2\phi(x)}{dx^2} = \begin{cases} -\frac{q}{\varepsilon_s}N_D & 0 < x < W \\ 0 & x > W \end{cases} \qquad \textbf{(3.11)}$$

where W represents the width of the depletion region. Integrating equation (3.11) twice and applying appropriate boundary conditions such as $d\phi/dx = 0$ at x = W, and $\phi = 0$ at x = W, the Poisson equation (3.11) can be solved analytically and the depletion region width W is obtained as given below

$$W = \sqrt{\frac{2\varepsilon_s}{qN_D}\left(V_{bi} - V\right)} \qquad \textbf{(3.12)}$$

V is the potential difference applied across the metal-semiconductor junction (or external bias voltage). From equation (3.12), the width of depletion region at zero bias W_O is obtained by setting V = 0. It can also be seen that W decreases below its value W_O in the case of forward bias[10] and increases above W_O in case of reverse bias[11].

3.3.4 Depletion Layer Capacitance

From equation (3.12), a change in the voltage across the Schottky barrier junction causes a change in the depletion region. This change is accomplished by the movement of charge carriers into the space charge layer or out of this region. This change in the depletion region charge gives rise to a change in capacitance. The space charge Q_{SC} per unit area stored in the depletion layer is given by:

$$Q_{sc} = qN_D W \quad \textbf{(3.13a)}$$

Substituting equation (3.12) into equation (3.13) the space charge Q_{SC} becomes

$$Q_{sc} = \sqrt{2q\varepsilon_s N_D\left(V_{bi} - V\right)} \quad \textbf{(3.13b)}$$

The depletion layer capacitance per unit area is defined as

$$C \equiv \frac{|\partial Q_{sc}|}{\partial V} \quad \textbf{(3.14a)}$$

Thus

$$C = \sqrt{\frac{q\varepsilon_s N_D}{2\left(V_{bi} - V\right)}} = \frac{\varepsilon_s}{W} \quad \textbf{(3.14b)}$$

By differentiating equation (3.14b) with respect to voltage V, a carrier charge density can be expressed in terms of the voltage derivative of contact capacitance (*dC/dV*) as:

$$N_D = \frac{8\left(V_{bi} - V\right)^3}{q\varepsilon_s}\left(\frac{dC}{dV}\right)^2 \quad \textbf{(3.15)}$$

10.For the metal-n-type semiconductor, forward bias means V is a positive value (positive polarity applied to the metal with respect to the semiconductor body)

11.For reverse bias, V is a negative value (negative polarity applied to the metal with respect to semi-conductor body)

Equation (3.15) leads to the concept of determining the carrier density by measuring the voltage derivative *dC/dV*. This is the basic principle of the Schottky Scanning Capacitance Microscope that has been used in our laboratory.

3.3.5 Capacitance Voltage (C-V) Curves

Using equation (3.14b), the ideal 1D capacitance-voltage (C-V) curves can be calculated. Figure 3.5 is a plot of depletion capacitance versus probe-to-sample voltage for a tungsten contact to n-Si and to p-Si semiconductors. Calculations were performed for a constant dopant density of $1 \times 10^{17}\,cm^{-3}$. In this calculation, the barrier heights for W-n-Si and W-p-Si contacts were assumed to be constant and did not change with bias voltages. The values of barrier height were taken to be 0.67 eV and 0.45 eV for W-n-Si and W-p-Si contacts respectively [9]. Although the SSCM utilizes a silicon tip coated with tungsten-carbide, the C-V curves are expected to be similar to those shown in Figure 3.5, because the work functions of these two materials are similar ($\phi_W = 4.55\,eV$ and $\phi_{W2C} = 4.58\,eV$).

Figure 3.5 shows that increasing the positive bias applied to the metal with respect to semiconductor (forward bias) will increase in the contact capacitance for the n-type semiconductor. The increase in contact capacitance is due to a reduction in the depletion width under forward bias. On the other hand, increasing the negative bias applied to the metal (reverse bias) will increase the depletion width and therefore decreases the contact capacitance. The opposite is true for a metal p-type semiconductor contact (see the blue curve in Figure 3.5).

Measurements of the depletion region capacitance under large forward bias are difficult because the Schottky diode (formed by a tip and sample) is conducting and the capacitance is shunted by a large conductance. However, the capacitance can be easily measured as a function of the reverse bias. For doping profile applications, a sample under test usually contains both n-type and p-type semiconductor. A reverse bias placed on a tip relative to one type of semiconductor however becomes a forward bias when this tip is

scanned on the other type. For that reason, the SSCM measurements are normally performed with a zero DC bias added to a small amplitude AC bias that is in turn applied between the tip and the sample. A slight DC bias may be applied to preferentially enhance the measurement sensitivity of one type (at the expense of the other type). Figure 3.5 also indicates that the capacitance derivative obtained at zero DC bias can be used to delineate between n-type and p-type regions in a single scan.

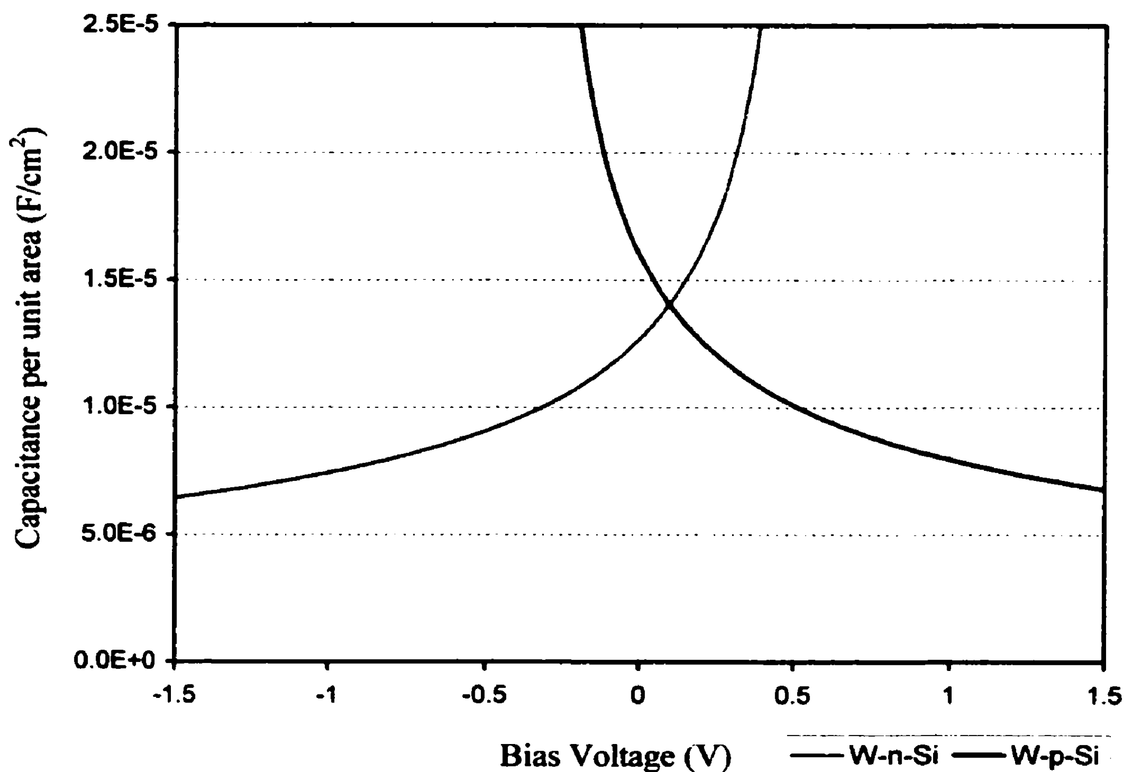


Figure 3.5 Typical C-V curves for a metal-n-type semiconductor and a metal-p-type semiconductor contact.

3.3.6 Depletion Capacitance and dC/dV Versus Substrate Concentration

The curves shown in Figure 3.6 represent the dependence of the contact capacitance and capacitance derivative *dC/dV* on the substrate dopant density for an ideal contact between a tungsten tip and the surface of n-type and p-type silicon. The calculation is done for a tip surface contact radius of 30 nm (radius of curvature of a typical silicon coated tip) and at zero bias. These curves tell us that both depletion capacitance and *dC/dV* monotonically increase with increasing substrate dopant density. For each doping level, the depletion capacitance and the magnitude of *dC/dV* calculated for a W-p-Si contact is larger than for a W-n-Si contact.

Although the y-axes of the plots in Figure 3.6 are expressed in terms of (F) and (F/V), the lock-in amplifier output does not directly give the value of *dC/dV* in terms of (F/V). The output is only proportional to the variation of the contact capacitance for a given amplitude of the modulation AC bias. In addition, the magnitude of measured *dC/dV* depends on the tip-sample contact area. Larger contact area produces larger voltage at the lock-in amplifier output and vice versa. However, the trend of the detected *dC/dV* is expected to be similar to that shown in Figure 3.6b.

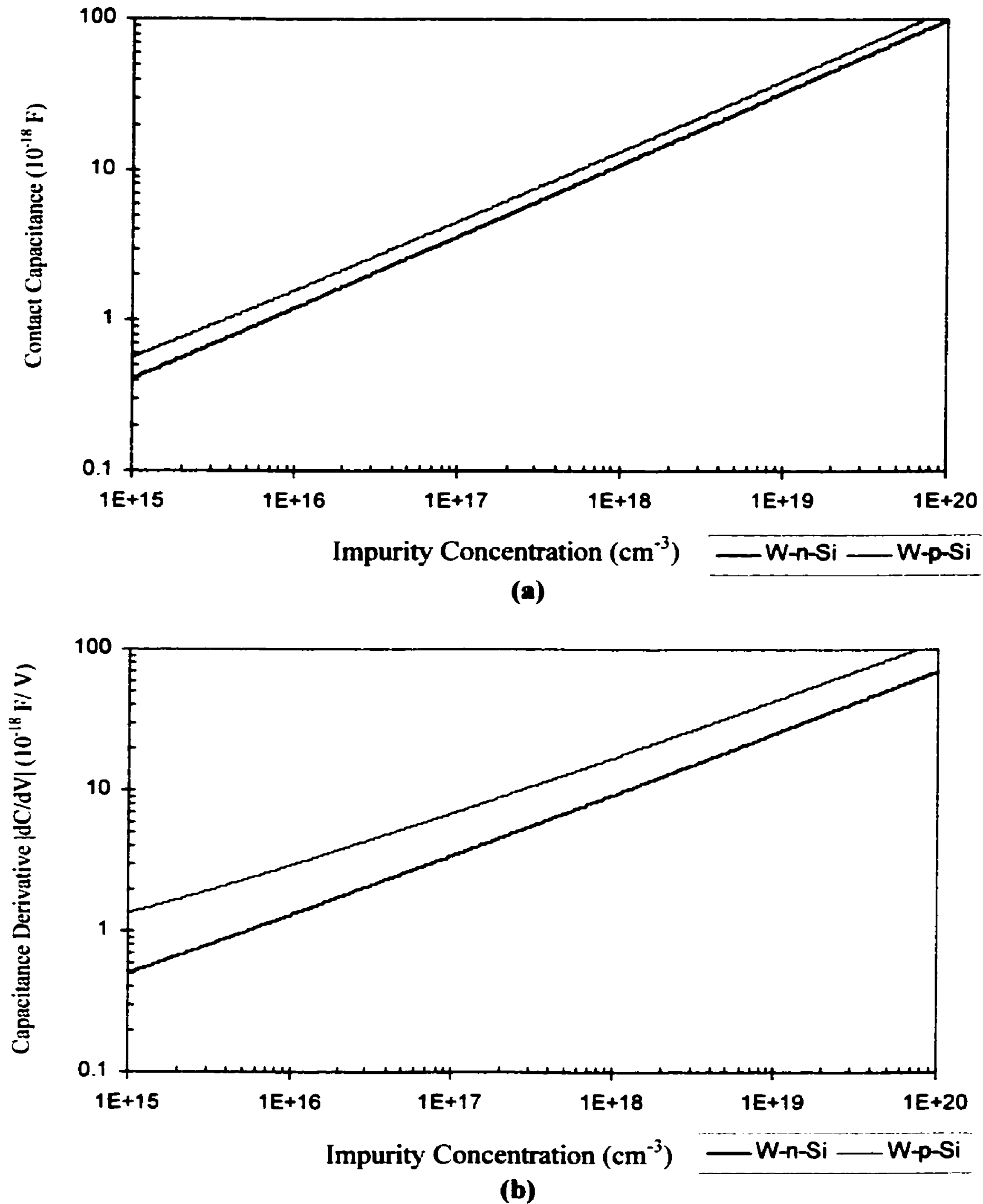


Figure 3.6 Calculated depletion layer capacitance and dC/dV versus impurity concentration at zero bias for both n-type and p-type semiconductor. The contact radius is assumed to be 30 nm.
(a) Depletion capacitance of W-n-type and W-p-type semiconductor.
(b) dC/dV of W-n-type and W-p-type semiconductor.

3.3.7 Detecting Changes in Dopant Type

As shown in Figure 3.5, the sign of *dC/dV* depends on the local dopant type. Therefore, the change in type of semiconductor in a test sample can be easily identified by observing the sign of the measured *dC/dV* data. When the SSCM probe tip is scanned across a pn junction (metallurgical junction), the built-in depletion region of the pn junction can be located at a point where the *dC/dV* curve crosses the zero voltage axis. In the other words, $dC/dV = 0$ if the tip is placed on the built-in depletion region of a pn junction. The fact that there is no carrier charge within the depletion region means that there is no capacitance to be detected.

The dependence of the sign of *dC/dV* on the dopant type can be explained as follows: 1) When a metal tip is placed in contact with homogeneous n-type silicon, a change in bias voltage (assume a sinusoidal signal) applied to the tip will cause a change in the depletion capacitance. 2) If the capacitance sensor is connected to the tip, changes in the tip-to-sample capacitance will shift the center frequency of the resonant circuit and result in a modulation of the amplitude of the oscillator signal. Therefore, the magnitude of the AC component of the sensor's output is proportional to the amplitude of the bias voltage and its phase is 180° out of phase with the bias signal (the increase in a positive bias will increase depletion capacitance and decrease the amplitude of the drive signal). 3) If the tip is now placed on a p-type silicon, the phase of the AC component of the sensor output is in phase with the bias signal. The increase in a positive bias will decrease depletion capacitance and increase the amplitude of the drive signal.

From this discussion, it has been seen that the phase of the AC component of the sensor's output is shifted 180° while the tip is crossing from one type of semiconductor to the other type. This 180° phase shift will cause a change in sign of the lock-in amplifier output when it is used to detect the output of the capacitance sensor.

3.3.8 Detecting Changes in Dopant Concentration

A theoretical calculation suggested that the magnitude of *dC/dV* is a function of dopant concentration. A region of higher dopant concentration produces a larger *dC/dV* than a region of lower dopant concentration (see Figure 3.6b). Changes in dopant concentration can be detected by simply measuring *dC/dV* while the SSCM probe tip is scanned across a dopant gradient. Unfortunately, in practice the measured *dC/dV* does not follow theoretical predictions. Experimental results shown that *dC/dV* increases as the dopant density increases from 1×10^{15} to 1×10^{18} cm^{-3} and decreases beyond these values (see Figure 6.1). The drop in *dC/dV* at high doping levels poses some difficulties when one attempt to explain the phenomenon using the basic theory of a well-behaved metal-semiconductor contact. It is thus impossible to determine whether a region to be scanned is heavily doped or lightly doped (since these two regions may have the same value of *dC/dV*) unless the location of one doped region is known in advance. For the real MOSFET devices presented in this thesis, however, the heavily doped region of a source/drain can be identified as a region that is located next to the gate and a lightly doped region on the substrate side.

The exact cause for the decrease in *dC/dV* at high doping levels is not well understood. One possible explanation may be found by considering the variation of depletion layer thickness as carrier concentration is increased. In general, a probe current tunneling through the junction results in the capacitance sensor seeing a shunt resistor (contact resistance) in parallel with the depletion capacitor (see Figure 3.2). In normal operation, the capacitive component dominates junction response, and the resistive component can be neglected. For dopant concentration in excess of 1×10^{18} cm^{-3}, the width of the depletion layer is diminished, and the tunneling resistance drops. The drop in this resistance may degrade the sensor's performance and therefore decrease the sensor output.

When the dopant concentration further increases, the depletion width becomes thinner or even collapses. The contact capacitance is then shorted by the parallel resistor. Decreasing this resistive component can lower the quality factor (Q) and increase the resonator loss. As will be seen in Chapter 4, the sensitivity of the sensor is directly proportional to (Q) and the gain of the resonant circuit. As a result, decreasing either of these

two factors can cause a significant decrease in the sensor's output signal.

In order to investigate the effects of the contact resistance on the performance of the capacitance sensor, factors affecting contact resistance are investigated in the following sections.

3.4 Contact Resistance

A detailed discussion of charge transport across a metal-semiconductor junction is given in Appendix B. The calculations of contact resistance presented here are based on the assumption that the thermionic and field emission act in parallel. The total current that flows across the metal-semiconductor junction is the sum of the thermionic emission current and field emission current $J_T = J_{TE} + J_{FE}$. The contact resistance is defined as the slope of the I-V characteristic curve of the junction diode (made up of a metal tip and semiconductor sample) at an operating point (given bias) and it is given by:

$$R_c(V) = \frac{1}{S}\frac{\partial V}{\partial I}\bigg|_{V = V_{dc}} \quad (3.16)$$

where S is the contact area.

Using equations B.1 to B.6 (appendix B) for thermionic emission current, field emission current and equation (3.16), the contact resistance can be calculated as a function of dopant concentration and bias voltages. Figure 3.7 shows the expected magnitude of contact resistances versus dopant concentration at zero bias for ideal W-n-Si and W-p-Si contacts. Calculations were performed at room temperature ($T = 300^{o}$ K) and for a probe-surface contact radius of 30 nm. For calculation purposes, it is assumed that the barrier height of the metal-semiconductor contacts is constant and does not change with dopant concentration because of surface states. The ideality factor used for the calculations is also assumed to be 1 ($n = 1$).

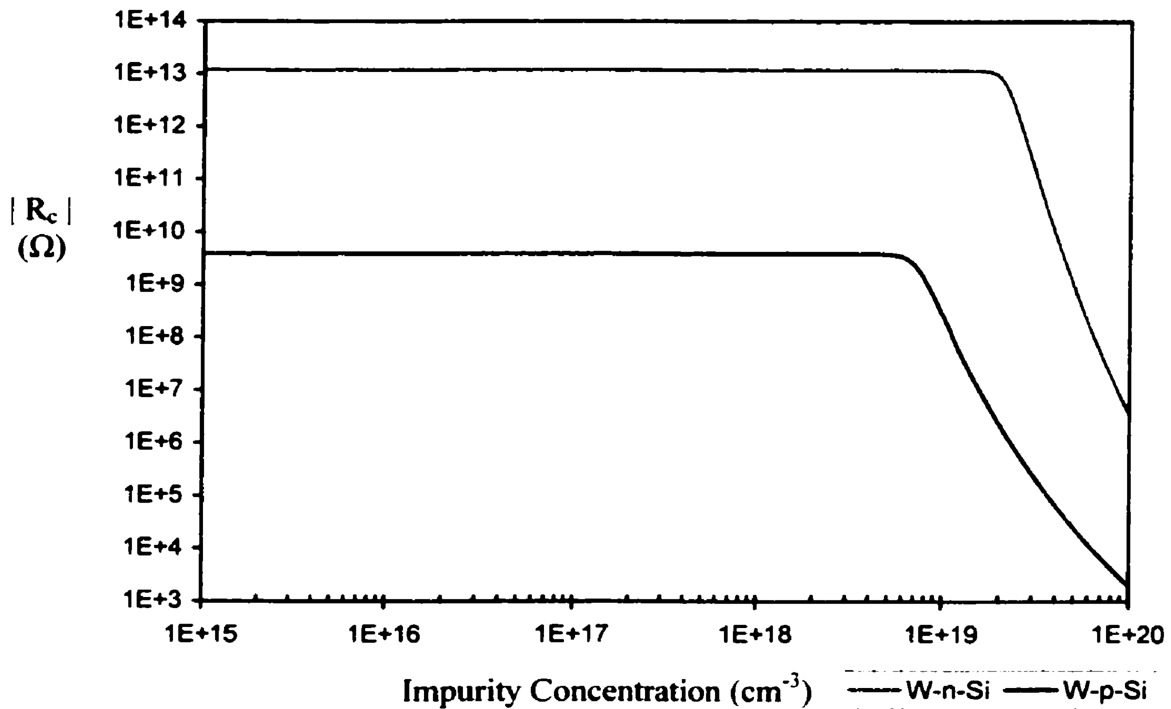
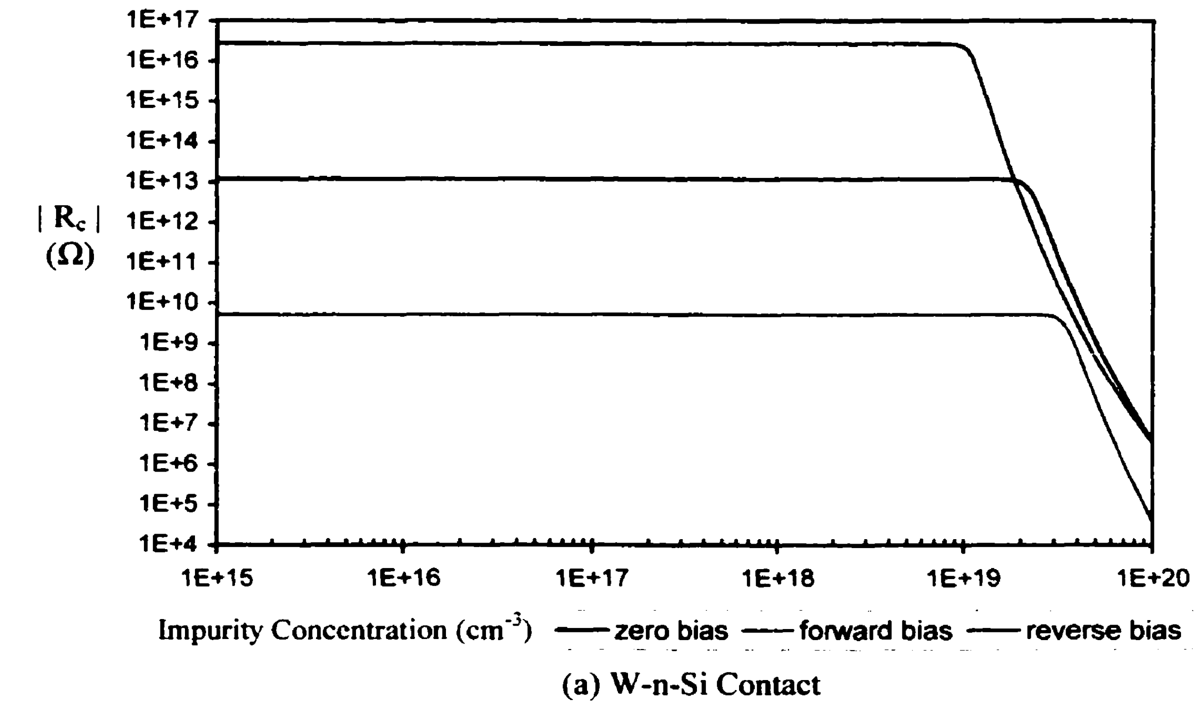


Figure 3.7 Magnitude of contact resistance versus dopant concentration at zero DC bias voltage for both W-n-Si and W-p-Si contacts. Calculations were performed for a temperature T = 300° K and contact radius = 30 nm.

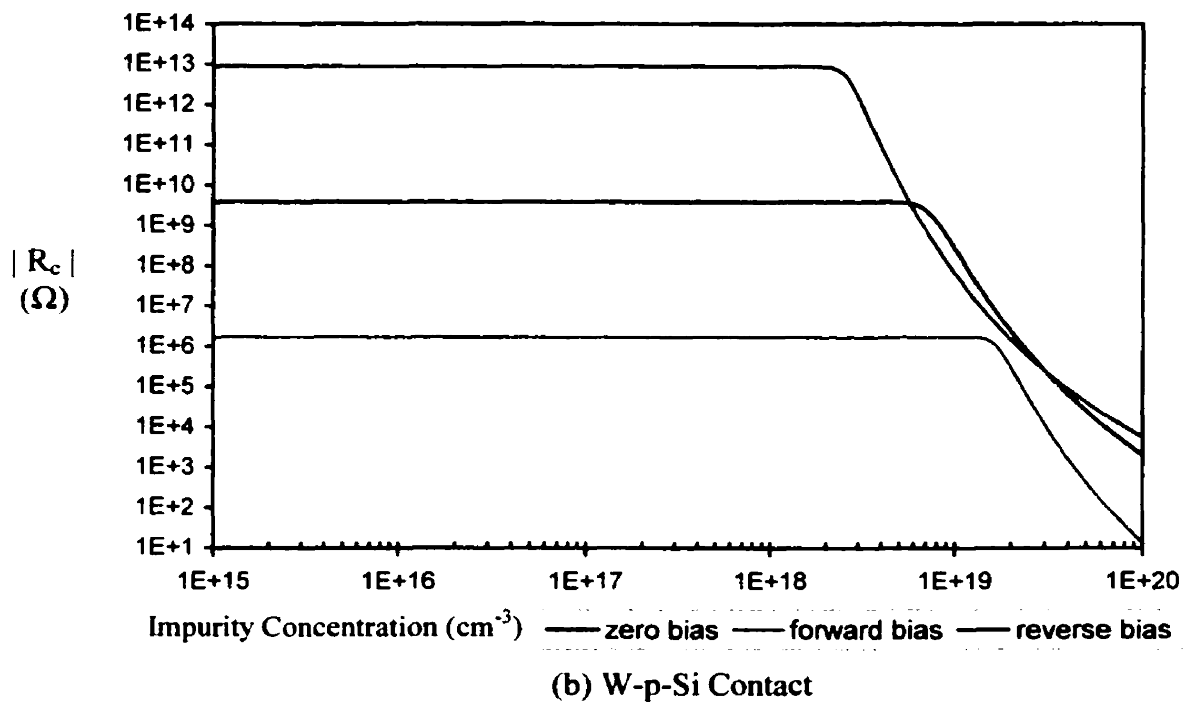
From these plots we can observe that the contact resistance is formed by a metal tip on either type of silicon is constant for dopant concentrations below 4×10^{18} cm^{-3}. In this range of dopant concentration, the field emission current is the dominant means of current flow. Furthermore, it can be seen in Appendix B that the field emission current is independent of dopant concentration. This can explain why the contact resistance is constant over a wide range of dopant concentration. When the dopant concentration is increased above 4×10^{18} cm^{-3}, the depletion width getting thinner, the tunneling current becomes dominant. As a result, the contact resistance drops. The plots also show that the contact resistance of W-n-Si contacts are higher than W-p-Si contacts for a given dopant concentration. This is due to the fact that the barrier height of the W-n-Si contacts is higher

than the barrier height of the W-p-Si contacts.

Figures 3.8 (a) and (b) are the plots of contact resistance versus dopant concentration at different tip-to-surface voltages for an ideal W-n-Si and W-p-Si contact respectively. In these plots, calculations were performed at zero bias and ±200 mV bias applied across the metal-semiconductor junction. Here the sign convention is chosen such that a positive bias on the metal relative to n-type semiconductor forward biases the junction and negative bias on the metal relative to n-type semiconductor reverse biases the junction. The opposite convention is applied for a metal-p-type semiconductor junction. A positive bias on the metal relative to p-type semiconductor reverse biases the junction and vice versa. The curves in Figure 3.8 (a) and (b) show that the contact resistance at a given dopant concentration is decreased if the junction is forward biased. Under reverse bias, the contact resistance is increased except at high doping levels ($>1\times10^{19}$ cm^{-3}) where the contact resistance is less sensitive to bias voltage.



(a) W-n-Si Contact



(b) W-p-Si Contact

Figure 3.8 Magnitude of contact resistance versus dopant concentration for different bias voltages at room temperature. Contact radius was taken to be 30 nm.
(a) Contact resistance for a tungsten n-type silicon contact
(b) Contact resistance for a tungsten p-type silicon contact

3.5 Spreading Resistance

Spreading resistance or "bulk resistance" is produced by the bulk semiconductor as distinct from the barrier layer, and is associated with the spreading of lines of current flow from the contact into the semiconductor. For a hemispherical contact, the spreading resistance is given by the expression:

$$R_{sp} = \frac{\rho}{2\pi r} \tag{3.17}$$

where ρ is the semiconductor resistivity, and r is the contact radius. It can be seen from equation (3.17) that the spreading resistance only depends on the semiconductor resistivity and contact radius. Since the semiconductor resistivity is a function of dopant concentration, spreading resistance is expected to change with dopant concentration. The curves in Figure 3.9 show spreading resistance as a function of dopant concentration for n-type and p-type silicon. Spreading resistance for either type of silicon decreases as the dopant concentration increases. In addition, the spreading resistance of the p-type is higher than the spreading resistance of the

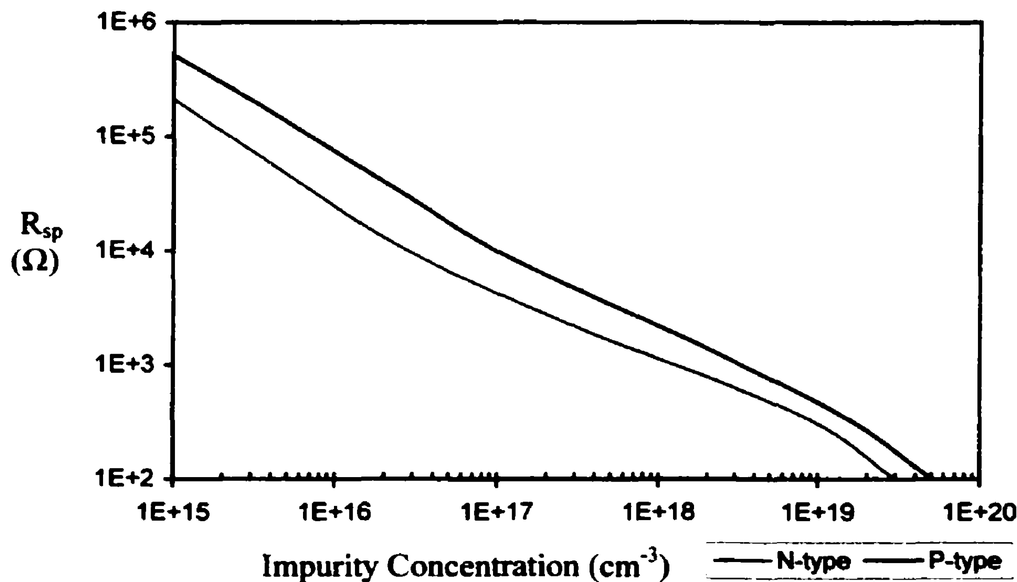


Figure 3.9 Spreading resistance as a function of dopant concentration for n-type and p-type silicon for a contact radius of 30 nm.

n-type silicon for a given dopant concentration. When the dopant concentration is increased from 1×10^{15} - 1×10^{20} cm^{-3}, the spreading resistance drops from 200 kΩ to 30Ω for n-type silicon and from 500 kΩ to 50Ω for p-type silicon.

3.6 Tip-Surface Contact Radius

Calculations in this chapter have been based on a contact radius of 30 nm (typical radius of curvature for a tip). However, the tip-to sample surface contact area does not only depend on the tip's radius, but also depends on the force exerted on the tip. For a hemispherical tip of radius R exerting a force F on an elastic surface, the contact radius "*a*" can be calculated from the expression given below **[62]**

$$a = \left(\frac{3RF}{4E^*}\right)^{1/3} \quad \textbf{(3.18)}$$

where $E^* = [(1-\nu_1^2)/E_1 + (1-\nu_2^2)/E_2]^{-1}$ and E_1, ν_1 and E_2, ν_2 are Young's modulus and Poisson's ratio of the tip and sample, respectively. As mentioned earlier the contact area should be maintained as small as possible in order to achieve high spatial resolution. From equation 3.18, it can be seen that a small contact area can be obtained by utilizing a sharp tip and minimizing the applied force. For the SSCM measurements, the force can be reduced by decreasing the set-point of the force control system.

CHAPTER 4

CAPACITANCE SENSOR DEVELOPMENT

Introduction

The capacitance sensor is the heart of both the conventional Scanning Capacitance Microscope and the Schottky Scanning Capacitance Microscope. Its circuit consists of an oscillator, a resonator, and a simple diode peak detector (or RF detector). The oscillator drives a resonator that is used to sense the capacitance to be measured. The resonator has three parallel-coupled transmission lines in which the center line is a resonator, to which a SSCM tip is attached. The outer lines serve as the input and output. Resonators have characteristics similar to very narrow notch filters. This means that the amplitude of the resonator's output strongly depends on the frequency of the drive signal. A typical resonant curve for the resonator appears is shown in Figure 4.1. As a sample is scanned beneath the SSCM tip, the variation of the tip-to-sample capacitance shifts the resonant frequency of the resonator. If the drive frequency is offset from the resonant frequency, the shift in resonant frequency of the resonator will result in the modulation of the amplitude of the resonator's output (see Figure 4.1). Therefore, the envelope of the amplitude modulation signal is proportional to the magnitude of the tip-to-sample **capacitance change**. The resulting AM envelope is then extracted by a diode peak-detector and is measured by a lock-in amplifier.

Traditionally, a capacitance bridge or simple L-C circuits have been employed to obtain C-V profiles for use in depletion capacitance measurements. However, in the case of SCM scanning probe instruments, the metal-semiconductor contact (junction) area is so small that several difficulties have to be overcome. When the contact size is reduced to less than 100 nm in diameter, the sensitivity of the capacitance measurements must be on the order of 10^{-18} F in a 1 kHz bandwidth. The contact capacitance is overwhelmed by the stray

capacitance, typically ~10^{-12} F, and conventional measurement methods are not capable of detecting such small capacitance or capacitance change.

In this chapter, a capacitance sensor is presented that has a sensitivity in the order of 10^{-21} F/$\sqrt{Hz}$. The basic idea of this sensor is based on the RCA capacitance sensor originally used for a VideoDisk decoding system [71]. Before describing the design of our capacitance sensor, a review of the RCA capacitance sensor and design theory is presented in the following section. Some of its theory of operation is directly applicable to the design of our capacitance sensor.

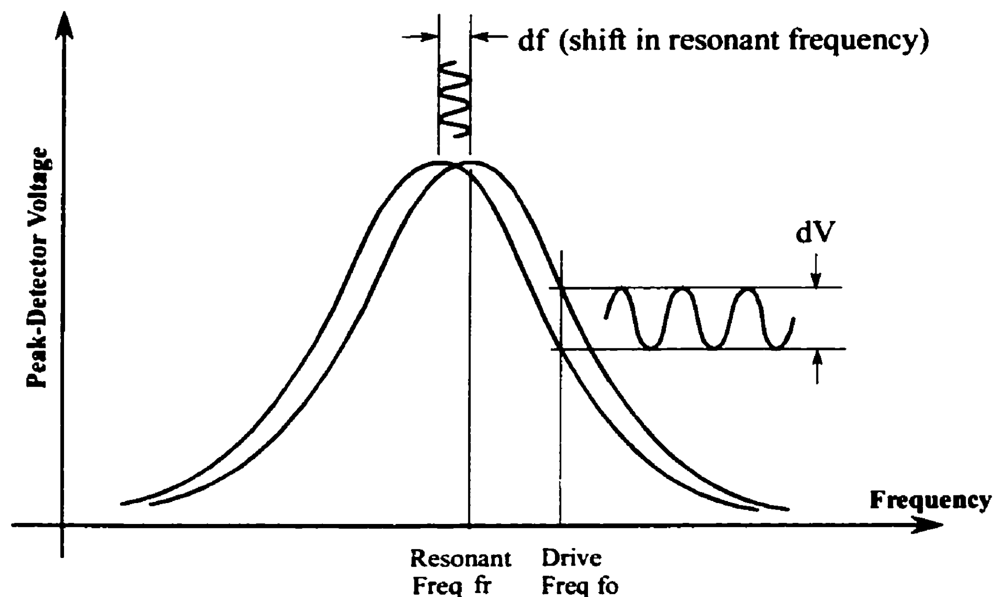


Figure 4.1 The response of the peak-detector output as a function of drive frequency showing how the shift in resonant frequency is converted into an output amplitude change.

4.1 RCA Capacitive-Pickup Circuitry For VideoDiscs

The RCA capacitive pickup was originally developed to read signals from a plastic disc that contained stored video and audio information. The disc has a fine spiral groove to guide a stylus that contains a thin electrode. The video and audio information is stored in the form of depressions in the bottom of this groove. The stored information is read by measuring capacitive variations between the electrode on the stylus and the surface of the disc. Detection of these small capacitive variations is performed by varying the tuning of a resonant circuit with the stylus-disc capacitance.

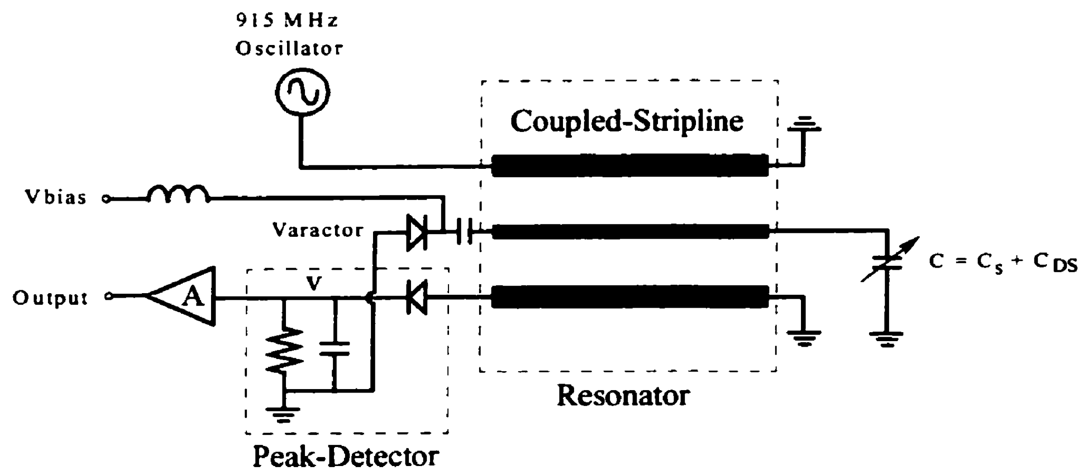


Figure 4.2 Schematic diagram for the RCA capacitance sensor

The resonant circuit (or resonator) is constructed using three coupled-striplines[12]. The resonator has characteristics similar to a very narrow band-pass filter with a bell-shaped transfer function. Figure 4.2 shows the basic schematic of the RCA capacitive-pickup circuitry. In this circuit, the resonant circuit is excited by an oscillator with a frequency of 915 MHz on the slope of the resonant curve (see Figure 4.1). In normal operation, variation

12.A stripline (sometime called triplate line) is a transmission line that is sandwiched between two parallel ground planes in which one is placed on top and the other at the bottom of the transmission line (see Figure 4.3). The separation gap between the transmission line and the top ground plane is equal to the gap between the transmission line and the bottom ground plane. In addition, the medium surrounding the transmission line and between the ground planes is usually filled with a homogeneous material of a dielectric constant ε_r

in the stylus-to-disc capacitance C_{DS} shifts the resonant frequency so that the drive signal in effect moves up and down the flank of the tuning curve thus resulting in an AM signal at the resonator output port. The envelope of this AM signal is then detected with a simple peak detector. Thus, the detected signal varies with the stylus-to-disc capacitance. The magnitude of the detected signal depends the slope of the resonant curve at the operating frequency.

In general, the center frequency of the resonator depends on the capacitance introduced to the ends of the resonator line (center line of three coupled-striplines). In order to tune it, a varactor diode is connected at the end of the resonator transmission line (see Figure 4.2). The varactor diode acts like a variable capacitor in which the capacitance can be controlled by a reverse bias voltage applied across the diode.

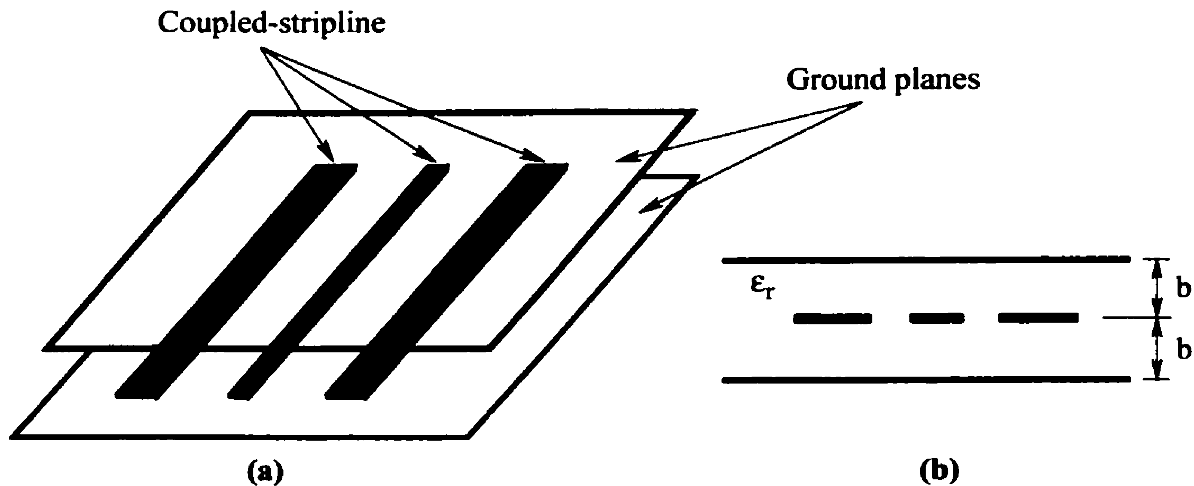


Figure 4.3 Configuration of coupled-stripline transmission lines
(a) Pictorial view, (b) Cross-sectional view

4.1.1 RCA Capacitance Sensor Sensitivity

In order to detect a small capacitance variation, the sensor should have high sensitivity. The pickup sensitivity is defined as the rate of change in diode voltage 'v' at the peak detector with respect to the change in the stylus-to-disc capacitance. Thus, the sensitivity can be expressed by

$$\frac{\Delta v}{\Delta C_{DS}} = \frac{dv}{df_r} \cdot \frac{df_r}{dC_{DS}} \quad \textbf{(4.1)}$$

where f_r is the center frequency of the resonant circuit, and C_{DS} is the stylus-to-disc capacitance. The first term in the right hand side of the equation (4.1) is called voltage sensitivity and the second term is called frequency sensitivity. Actually, voltage sensitivity dv/df_r is just the slope of the resonant curve at the operating frequency. The magnitude of dv/df_r depends on the magnitude of the drive signal and upon where the oscillator frequency falls on the resonant curve (this is assuming that there is no signal loss in the resonator). For a bell-shaped resonant curve, the diode voltage as a function of frequency is given by [71]

$$v(f) = \frac{V_p}{\sqrt{1 + \left[\frac{2(f-f_r)}{B}\right]^2}} \quad \textbf{(4.2)}$$

where f is the frequency, f_r is the resonant frequency, V_p is the detected diode voltage at the peak of the resonant curve, and B is the half power bandwidth (or -3dB bandwidth). A half power bandwidth is defined as $B = (f_2 - f_1)$, where f_2 and f_1 are the frequencies that fall on the right-hand side and left-hand side of the resonant frequency respectively such that the diode voltages at these frequencies are 3dB lower than the peak diode voltage V_p. Figure 4.4 shows an example of a typical resonant curve. The graph is plot of the normalized detected diode voltage (normalized to the peak detected diode voltage) as a function of frequency. The calculation is performed by assuming that the resonant frequency is 900 MHz and the half power bandwidth is 20 MHz.

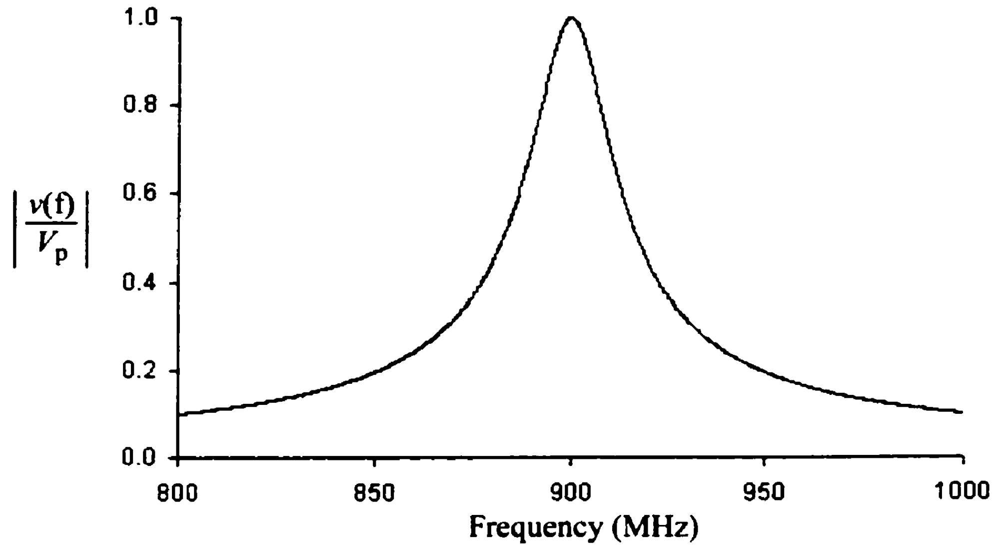


Figure 4.4 An example of the shape of a typical resonant curve. The graph is obtained by plotting the magnitude of v(f) over the peak detected diode voltage Vp.

4.1.1.1 Voltage Sensitivity

The slope of the resonant curve as a function of frequency can be obtained by differentiating equation 4.2 with respect to frequency. Thus, the slope of the resonant curve as a function of frequency is given by:

$$\frac{dv(f)}{df} = -\frac{4(f-f_r)B^2}{\sqrt{[B^2+4(f-f_r)^2]^3}}\left(\frac{V_p}{B}\right) = \alpha(f)\frac{V_p}{B} \qquad (4.3)$$

where $\alpha(f)$ is the coefficient of voltage sensitivity.

Figure 4.5 shows an example of voltage sensitivity that is normalized to the detected diode voltage at the peak of the resonant curve. Again, the calculations are performed by assuming f_r = 900 MHz and B = 20 MHz. It can be seen that the voltage

sensitivity is increased as the drive frequency approaches the resonant frequency. The frequencies at which the maximum voltage sensitivity occurs are determined by solving the equation $d^2v(f)/df^2 = 0$. Solving this equation, these frequencies are:

$$f = f_r \pm \frac{B}{2\sqrt{2}} \tag{4.4}$$

Substituting equation (4.4) into equation (4.3), the maximum voltage sensitivity is:

$$\left.\frac{dv(f)}{df}\right|_{max} = \pm\frac{4}{3\sqrt{3}}\frac{V_p}{B} \tag{4.5}$$

It should be noted that the vertical scale in Figure 4.5 does not necessarily represent the voltage sensitivity of the actual capacitance sensor. The purpose of this curve is to show the shape of voltage sensitivity as a function of frequency.

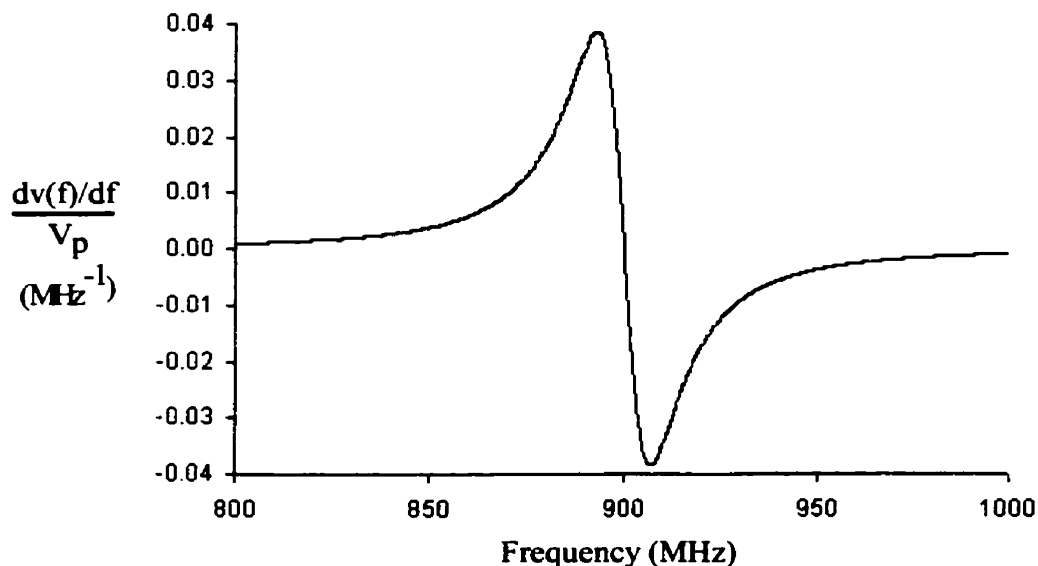


Figure 4.5 An example of the slope of the resonant curve. The graph is obtained by plotting dv(f)/df over the peak detected diode voltage Vp.

4.1.1.2 Frequency Sensitivity

Frequency sensitivity is defined as the rate of change in resonant frequency with respect to the change in capacitance at the pickup electrode. The frequency sensitivity is given as df_r/dC. Figure 4.6 shows the resonant circuit that is formed by a resonator line and the end capacitances.

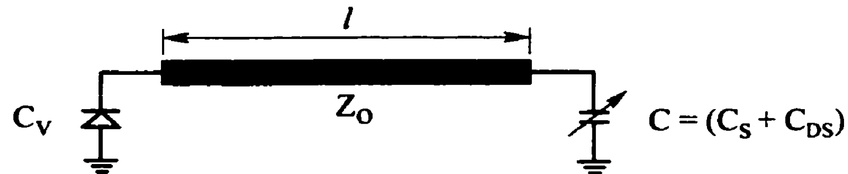


Figure 4.6 A schematic of a resonator transmission line with capacitances at its ends

The circuit is in resonance when equation (4.6) is satisfied (assuming that the line is lossless) [71]:

$$\frac{1}{j\omega C} + Z_o \frac{\frac{1}{j\omega C_v} + jZ_o \tan\beta l}{Z_o + \frac{1}{\omega C_v}\tan\beta l} = 0 \qquad \textbf{(4.6)}$$

where $C = C_S + C_{DS}$ in which C_S is the stray capacitance, C_{DS} is the stylus-to-disc capacitance, C_V is the varactor diode capacitance, Z_O is the characteristic impedance of the resonator line, $\beta = \omega/v_p$, ω is the angular frequency ($\omega = 2\pi f$) and v_p the velocity of propagation in the transmission line, l is the physical length of the resonator line, and βl is the electrical length of the resonator line. The first term in equation (4.6) represents an impedance seen from the stylus electrode toward the disc and the second term an impedance seen from the electrode toward the transmission line.

The electrical length is given by

$$\beta l = \frac{\omega}{v_p} l = \frac{2\pi f\sqrt{\varepsilon_r}}{c} l \tag{4.7}$$

where c is the speed of light in free space (c = 3x10^8 m/s), and ε_r is the dielectric constant of the medium surrounding the transmission line. Equation (4.6) can be re-arranged and it becomes:

$$\tan\beta l = \frac{\omega Z_o (C_v + C)}{CC_v\omega^2 Z_o^2 - 1} \tag{4.8}$$

Differentiating equation (4.8) with respect to ω and C, the frequency sensitivity df/dC can be obtained as:

$$\begin{aligned} \frac{df}{dC} &= -\left[\frac{1 - \frac{1}{\omega C_v Z_o \tan\beta l}}{2 + \left(\frac{1}{C_v} + \frac{1}{C}\right)\frac{1}{\omega Z_o \tan\beta l}[\beta l(\tan\beta l + \cot\beta l) - 1]}\right]\frac{f}{C} \\ &= -\gamma(f)\,\frac{f}{C} \end{aligned} \tag{4.9}$$

where $\gamma(f)$ is the coefficient of frequency sensitivity. It has been shown in [71] that the frequency sensitivity increases proportionally with the characteristic impedance of the resonator line. By using a stripline configuration with a large spacing between ground planes, the characteristic impedance of the resonator line can be as high as 300 Ω. Once the parameters C_v, C, Z_0 are known, the physical length of the resonator line at a desired frequency can be calculated from equation (4.7) and (4.8), and the frequency sensitivity calculated from equation (4.9). The frequency sensitivity of the RCA capacitance sensor has been determined to be 1.15 MHz/fF at 915 MHz when the resonator line has a characteristic impedance of 300 Ω [71].

4.1.1.2 Total Sensitivity

The total sensitivity was defined in equation (4.1). Combining equations (4.3), (4.9), and (4.1), the total sensitivity can be re-written as:

$$\frac{\Delta v}{\Delta C_{DS}} = \left[\alpha(f)\frac{V_P}{B}\right]\left[\gamma(f)\frac{f}{C}\right] \tag{4.10}$$
$$= \alpha(f)\gamma(f)\frac{V_P Q}{C}$$

where $Q = f/B$ is called quality factor of the resonator. For the RCA capacitance sensor, the design parameters were specified as V_p = 4 V, B = 20 MHz, f = 915 MHz, and ΔC_{DS} = 0.1 fF. By using equation (4.5) with a frequency sensitivity of 1.15 MHz/fF, the maximum total sensitivity is calculated to be 175 mV/fF.

4.2 Development of the Capacitance Sensor

In the following sections, the design theory of the a capacitance sensor that was used for SSCM measurements is presented. As with the RCA system, our sensor incorporates an oscillator, a coupled transmission line resonator, an amplifier and a peak detector. In our circuit, the oscillator is a programmable phase-lock-loop (PLL) and a voltage controlled oscillator (VCO). Permitting its frequency to be controlled by the user via a computer. The resonator is composed of three coupled microstrip transmission lines that are milled from copper-clad, low loss dielectric material. The peak detector is constructed from a zero-bias Schottky diode.

4.3 Design Theory for the Microstrip Transmission Line Resonator

The basic operation of the sensor is the same as that of the RCA sensor. In our design, however, the resonant circuit (resonator including the detected capacitance at the resonator's tip) is constructed using a microstrip transmission line and is driven by a frequency controllable oscillator. Because the oscillation frequency can be set at any point on the resonant curve, the varactor diode required for tuning purposes in the RCA sensor was not needed in this circuit. The varactor diode is therefore replaced by a short circuit. Figure 4.7 illustrates our capacitance sensor circuit.

It can be seen from equation 4.10 that the sensitivity of the capacitance sensor can be improved in several ways. For example one can increase both peak detected voltage and operating frequency, decrease the capacitance and the bandwidth of the resonant curve or a combination of these. For the SSCM measurements, the capacitance (predominantly stray) depends on the interaction between the sample and the SSCM probe. This capacitance varies from sample to sample, and is therefore uncontrollable. Increasing the sensitivity by increasing the peak detected voltage is also limited because the voltage between the tip and the sample must be low to prevent excessive current flow that in turn may affect the quality of the capacitance images. As a result, the sensitivity can basically only be improved by increasing the operating frequency or decreasing the bandwidth. For this reason, the resonator was designed such that the drive frequency was typically operated at relatively high frequency, of about 1.85 GHz.

It should be noted that the sensitivity is determined by the electrical properties of the resonator (i.e. operating frequency, bandwidth, characteristic impedance of the lines, etc.) regardless of which structure is used to form the resonator (stripline or microstrip). Keeping the electrical properties the same, the only differences between these two structures are physical parameters such as the size of the resonator, the width of the lines, and the spacing between the lines. A microstrip structure was used in this design because it is very difficult to construct a stripline in our laboratory. The microstrip has an advantage over the stripline in that it is easily fabricated using etching or milling techniques. However, the theoretical analysis of this structure is complicated due to the presence of two different dielectric media

(see Figure 4.8 for the microstrip configuration). The boundary conditions at the plane interface between the substrate and the upper dielectric (air) cannot be satisfied by a pure TEM (Transverse Electro Magnetic) mode of propagation, which means that the characteristic impedance of the line is not defined. For a wide range of practical interest and low frequency applications, however, the actual propagating "waveguide" mode is sufficiently close to a TEM mode in most of its characteristics for it to be treated as such for analytical purposes [72][73]. For this reason, the quasi-TEM approximation has been assumed in most published works to analyze the microstrip structure. For the case of multi-coupled microstrip transmission lines, the theoretical analysis becomes more difficult. Unfortunately, there is no closed form expression for the determination of the electrical characteristics of multi-coupled microstrip lines (three lines or more) in terms of their physical dimensions. For the case of a microstrip resonator, a numerical analysis should be carried out in order to study the characteristics of the resonator (or obtaining a resonant curve). A numerical analysis was performed and is presented in section 4.3.2. In addition, the resonant characteristics were derived in terms of the scattering parameters of a lossless two port network (S-parameters) so that they could be directly compared to experiment results obtained from a Network Analyzer in the laboratory.

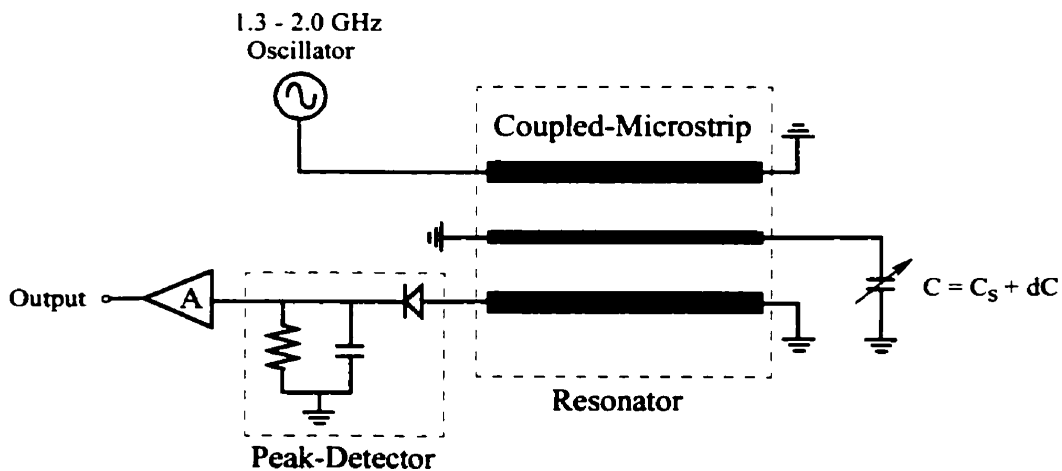


Figure 4.7 Schematic diagram of the new capacitance sensor

4.3.1 Microstrip Resonator

A microstrip is a two-conductor transmission line in which one conductor is fabricated on the surface of a dielectric substrate to form the circuit element and the other is placed at the bottom of the substrate to serve as a ground plane. Figure 4.8 shows the configuration of a microstrip resonator (note: the short circuit elements at the end of the lines are not shown in this figure). The resonator is made of a three parallel, rectangular cross-section microstrip transmission lines fabricated on a substrate of dielectric constant ε_r and height "h". The configuration of these transmission lines is such that the two outer transmission lines have the same width "W1" and are placed with an equal separation gap "S" from the center line (resonator line). Due to symmetry, either outer line can be used as an input/output port. The resonator line, however, has a width of "W2" that is different from "W1" (see Figure 5.6b). The characteristic impedance of the lines is determined by the width of these microstrip lines while the bandwidth of the resonant curve is determined by the spacing "S". To make the required short circuit for a transmission line, a hole is drilled vertically through the substrate so that a "via"[13] can be used connect the transmission line and the ground plane.

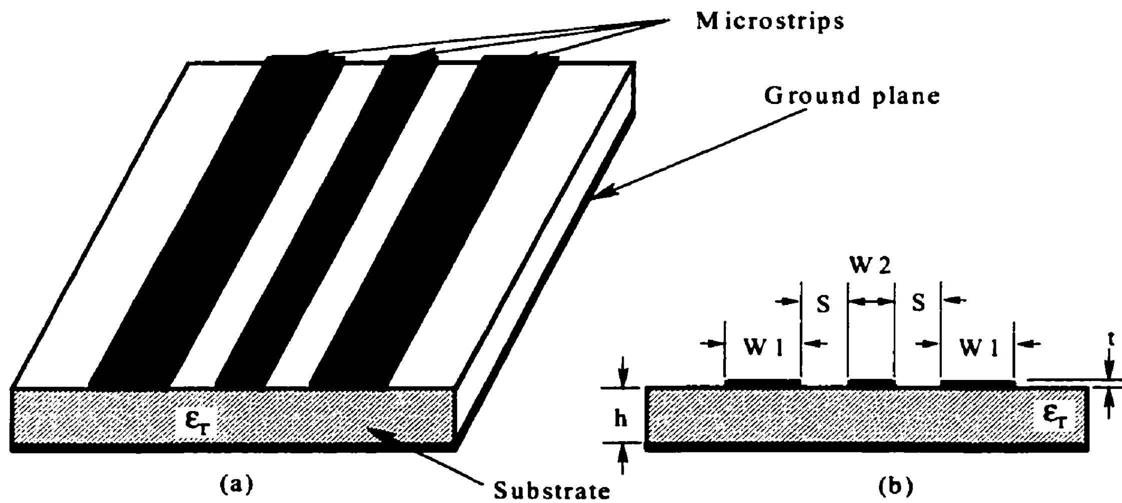


Figure 4.8 Configuration of coupled-microstrip transmission lines
(a) Pictorial view
(b) Cross sectional view

13. Via is a metallization process that is commonly used in multi-layers Printed Circuit Board (PCB) to connect circuit elements in different layers.

As was shown for the RCA sensor, the sensitivity of this sensor is defined as given in equation 4.1. In this case, however, the variation in capacitance is from the tip-to-sample contact capacitance instead of stylus-to-disc capacitance. Because the structure of the microstrip resonator is similar to the RCA resonator, the maximum voltage sensitivity can be derived from equations 4.2 to 4.5. The frequency sensitivity, however, is different to calculate due to the presence of the short circuit at the end of the resonator line. For an isolated resonator line shown in Figure 4.9 and assuming that the resonator line is lossless, the circuit is in resonance when:

$$\frac{1}{j\omega C} + jZ_o \tan\beta l_o = 0 \qquad \textbf{(4.11)}$$

where C is the total capacitance at the tip (stray plus the tip-to-sample contact capacitance), Z_O is the characteristic impedance of the resonator line, l_o and βl_o are the physical and electrical length of the line respectively. The first term in equation (4.11) represents the impedance seen from the tip toward the sample and the second term the impedance seen from the tip toward the transmission line. By solving equation (4.11), the electrical length of the resonator can be expressed in terms of other parameters and given by:

$$\tan\beta l_o = \frac{1}{\omega C Z_o} \qquad \textbf{(4.12)}$$

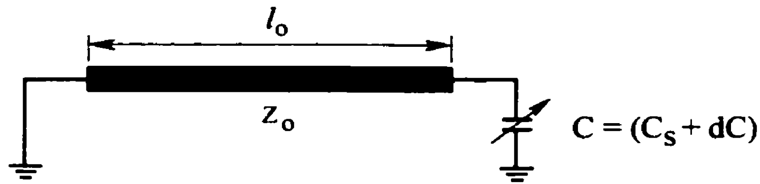


Figure 4.9 Equivalent circuit of a microstrip transmission line resonator.

It can be seen from equation (4.12) that if the capacitance C approaches zero, for example when the resonator is unloaded, the electrical length βl_o that is required to satisfy equation

(4.12) is an odd multiple of 90°. Therefore, the shortest physical length of the resonator for the unloaded condition is a quarter wave length ($\lambda/4$) at the desired resonant frequency ω.

Differentiating equation 4.12 with respect to C and ω, the frequency sensitivity can be obtained as:

$$\frac{df}{dC} = -\left[\frac{1}{1+\beta l_o(\tan\beta l_o + \cot\beta l_o)}\right]\frac{f}{C} \tag{4.13}$$

Suppose that a resonator line is built under unloaded conditions and it has a physical length of $\lambda/4$ at a design resonant frequency f_o. When the resonator is loaded with a capacitance C, the resonant frequency is shifted to $f_r < f_o$. Because the physical length of the resonator line does not change, however, the electrical length of the resonator line becomes:

$$\beta l_{new} = \frac{\pi}{2}\frac{f_r}{f_o} \tag{4.14a}$$

From equations (4.14a) and (4.12) the resonant frequency f_r can be expressed in terms of the loaded capacitance as:

$$C = \frac{1}{2\pi f_r Z_o \tan\left(\frac{\pi}{2}\frac{f_r}{f_o}\right)} \tag{4.14b}$$

Substituting equation (4.14a) and (4.14b) into equation (4.13), the frequency sensitivity can be expressed in terms of the resonant frequency f_r and characteristic impedance Z_O as:

$$\frac{df_r}{dC} = -\frac{2\pi Z_o \tan\left(\frac{\pi}{2}\frac{f_r}{f_o}\right)f_r^2}{1+\left(\frac{\pi}{2}\frac{f_r}{f_o}\right)\left[\tan\left(\frac{\pi}{2}\frac{f_r}{f_o}\right)+\cot\left(\frac{\pi}{2}\frac{f_r}{f_o}\right)\right]} \tag{4.15}$$

where Z_0 is the characteristic impedance of the resonator line, f_o the resonant frequency under unloaded conditions, and f_r the resonant frequency under loaded conditions. The resonant frequency f_r is an implicit function of the loaded capacitance C. Equation (4.15) shows that the frequency sensitivity is proportional to characteristic impedance of the resonator line and the resonant frequency. The magnitude of the overall sensitivity is then given by:

$$\frac{\Delta v}{\Delta C} = (\alpha V_p)\left\{\frac{2\pi Z_o \tan(\pi f_r/2f_o)}{1 + (\pi f_r/2f_o)\,[\tan(\pi f_r/2f_o) + \cot(\pi f_r/2f_o)]}\right\} f_r Q \quad \textbf{(4.16)}$$

In general, a transmission line which consists of $(n + 1)$ conductors in an inhomogeneous dielectric and in which one conductor is taken as ground supports n distinct "normal" quasi-TEM modes, each with a distinct phase velocity and with a distinct characteristic impedance for each line [75]. Degeneracies can occur due to symmetries in the structure. The case of a homogeneous dielectric (stripline structure) represents a sort of symmetry in which the quasi-TEM modes become true-TEM modes with different characteristic impedances but a single propagation velocity. Due to the existence of the multiple phase velocities among three coupled-microstrip lines, equation (4.15) for an isolated resonator line can be applied to a system of three coupled-microstrip lines when the spacing between these lines is large (loosely coupled-lines). It has been shown in [74] that the lines behave as three isolated microstrip lines as the distance between lines is increased. For our microstrip resonator, equation (4.15) can be used as a quick approximation for calculating the frequency sensitivity. The results obtained by using equation (4.15) will be compared to the numerical results in subsequent sections. In addition, it is expected that there are three distinct wavelengths associated with each of the three distinct phase velocities in the structure. Evaluation of the physical length ($\lambda/4$) of the three part coupled-microstrip resonator requires knowledge of these phase velocities. The physical length of the microstrip resonator can be numerically calculated.

4.3.2 Derivation of the Resonant Curve

In this sub-section, the resonant curve is derived in terms of the scattering parameters of a two port network. In this derivation, it is assumed that the microstrip lines are lossless transmission lines and that the short circuit elements at the end of the microstrip lines are perfect short circuits.Figure 4.10 shows the schematic of the microstrip resonator.

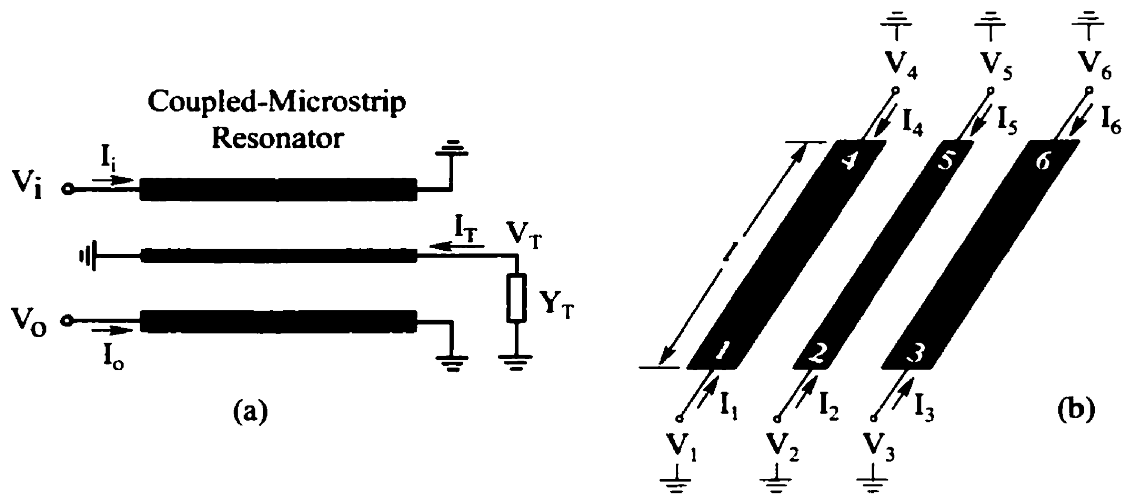


Figure 4.10 Three coupled-microstrip transmission lines as a resonator
(a) Schematic of three coupled-line resonator
(b) Schematic of three coupled-line six ports

In conventional circuit theory, the fundamental quantities of interest are voltages and currents, and the parameters used to express relationships between them are called impedances and admittances.Considering the resonator as a six-port network with the conventional port voltages and port currents are defined as shown in Figure 4.10b, the relationships between the port voltages and port currents can be expressed in terms of an admittance matrix as shown in equation (4.17):

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} & Y_{15} & Y_{16} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} & Y_{25} & Y_{26} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} & Y_{35} & Y_{36} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} & Y_{45} & Y_{46} \\ Y_{51} & Y_{52} & Y_{53} & Y_{54} & Y_{55} & Y_{56} \\ Y_{61} & Y_{62} & Y_{63} & Y_{64} & Y_{65} & Y_{66} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \\ V_5 \\ V_6 \end{bmatrix} \quad \textbf{(4.17)}$$

where I_n (n = 1,2,...,6) is the current into port "n", V_n (n = 1,2,...,6) is the voltage at port "n" and the Y-parameters are defined as follows:

Y_{nn} (n = 1,2,...,6) is the ratio of current into port "n" to voltage at port "n" with all other ports shorted.

Y_{mn} (m = 1,2,...,6; n = 1,2,...,6; $n \neq m$) is the ratio of current into port "m" to voltage at port "n" with all other ports shorted.

The terminal conditions for the loaded resonator section shown in Figure 4.10a are as follows:

$$V_2 = V_4 = V_6 = 0 \quad \textbf{(4.18a)}$$

$$V_1 = V_i \; ; I_1 = I_i \quad \textbf{(4.18b)}$$

$$V_3 = V_o \; ; I_3 = I_o \quad \textbf{(4.18c)}$$

$$V_5 = V_T \; ; I_5 = I_T \quad \textbf{(4.18d)}$$

Applying the terminal conditions to the admittance matrix in equation (4.17), the relationships between the currents and voltages at ports 1, 3, and 5 are governed by the following system of equations:

$$I_i = Y_{11}V_i + Y_{13}V_o + Y_{15}V_T \quad \textbf{(4.19a)}$$

$$I_o = Y_{31}V_i + Y_{33}V_o + Y_{35}V_T \quad \textbf{(4.19b)}$$

$$I_T = Y_{51}V_i + Y_{53}V_o + Y_{55}V_T \quad \textbf{(4.19c)}$$

Because the resonator structure is symmetrical, we have:

$$\begin{aligned} Y_{13} &= Y_{31} \\ Y_{11} &= Y_{33} \\ Y_{15} &= Y_{51} = Y_{35} = Y_{53} \end{aligned}$$

The system of equations (4.19) can be re-written as:

$$I_i = Y_{11}V_i + Y_{13}V_o + Y_{15}V_T \quad \textbf{(4.20a)}$$

$$I_o = Y_{13}V_i + Y_{11}V_o + Y_{15}V_T \quad \textbf{(4.20b)}$$

$$I_T = Y_{15}V_i + Y_{15}V_o + Y_{55}V_T \quad \textbf{(4.20c)}$$

However, from Figure 4.10a, the current and voltage at port 5 can be expressed as $I_T = -Y_T V_T$. Substituting $I_T = -Y_T V_T$ into equation (4.20) and performing a little algebraic manipulation, the relationship between the currents and voltages at the input and output ports can be expressed in a matrix form as follows:

$$\begin{bmatrix} I_i \\ I_o \end{bmatrix} = \begin{bmatrix} Y_{11} - \dfrac{(Y_{15})^2}{Y_T + Y_{55}} & Y_{13} - \dfrac{(Y_{15})^2}{Y_T + Y_{55}} \\ Y_{13} - \dfrac{(Y_{15})^2}{Y_T + Y_{55}} & Y_{11} - \dfrac{(Y_{15})^2}{Y_T + Y_{55}} \end{bmatrix} \begin{bmatrix} V_i \\ V_o \end{bmatrix} \quad \textbf{(4.21)}$$

Equation (4.21) tells us that the resonator is now reduced to a two-port network If the admittance parameters in equation (4.21) are normalized to the characteristic impedance Z_O of the measuring system (i.e. 50Ω), equation (4.21) can be re-written:

$$\begin{bmatrix} I_i \\ I_o \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_i \\ V_o \end{bmatrix} \quad \textbf{(4.22)}$$

where

$$y_{11} = y_{22} = \left[Y_{11} - \frac{(Y_{15})^2}{Y_T + Y_{55}} \right] Z_o \quad \textbf{(4.23a)}$$

$$y_{12} = y_{21} = \left[Y_{13} - \frac{(Y_{15})^2}{Y_T + Y_{55}} \right] Z_o \qquad \textbf{(4.23b)}$$

The scattering parameters (S-parameters) of the two-port network (resonator) can be calculated from the normalized admittance parameters using the expressions given below:

$$S_{11} = S_{22} = \frac{(1 - y_{11}^2) + y_{12}^2}{(1 + y_{11})^2 - y_{12}^2} \qquad \textbf{(4.24a)}$$

$$S_{12} = S_{21} = -\frac{2y_{12}}{1 + y_{11}^2 - y_{12}^2} \qquad \textbf{(4.24b)}$$

In order to calculate the S-parameters of the resonator, the admittance parameters in equation (4.21) must be evaluated. As mentioned in section 4.3.1, a transmission line which consists n conductors in an inhomogeneous dielectric supports n distinct "normal" quasi-TEM modes, each with a distinct phase velocity and a distinct characteristic impedance for each line. For the case of a microstrip resonator, it is expected that there are three possible quasi-TEM propagation modes referred to here as modes a, b, and c. For a lossless three coupled line structure, the admittance matrix parameters can be derived in terms of phase velocities and mode characteristic impedances as given in **[76][77]**:

$$Y_{11} = -j\frac{1}{2}\left[Y_{01a}\cot\beta_a l - \frac{R_{2c}Y_{01b}\cot\beta_b l - R_{2b}Y_{01c}\cot\beta_c l}{R_d} \right] \qquad \textbf{(4.25)}$$

$$Y_{13} = j\frac{1}{2}\left[Y_{01a}\cot\beta_a l + \frac{R_{2c}Y_{01b}\cot\beta_b l - R_{2b}Y_{01c}\cot\beta_c l}{R_d} \right] \qquad \textbf{(4.26)}$$

$$Y_{15} = j\frac{Y_{01b}\csc\beta_b l - Y_{01c}\csc\beta_c l}{R_d} \qquad \textbf{(4.27)}$$

$$Y_{55} = -j\frac{R_{2b}Y_{02b}\cot\beta_b l - R_{2c}Y_{02c}\cot\beta_c l}{R_d} \qquad \textbf{(4.28)}$$

$$\beta_{a,b,c}l = \frac{2\pi f}{v_{a,b,c}}l \tag{4.29}$$

with R_d is defined as:

$$R_d = R_{2b} - R_{2c} \tag{4.30}$$

and where $\beta_{a,b,c}l$ are the electrical lengths of the lines for the three modes a, b, and c respectively. "l" is the physical length of the structure, Y_{0ik} (i = 1, 2, 3 and k = a, b, c) is the characteristic admittance of line "i" for mode "k", $R_{ik} = V_{ik}/V_{1k}$ (i = 2, 3 and k = a, b, c) is defined as the ratio of voltage on the "ith" to the voltage on the first lines in mode "k". Furthermore, it has also been shown in [76] that all the parameters presented in equations (4.25) to (4.29) can be derived in terms of the coefficients of the static capacitance matrices per-unit-length Cd_{ij} and Ca_{ij} (i, j = 1, 2, 3) of the structure with the dielectric in place and removed, respectively. These capacitance matrices will be derived and evaluated in next section of this thesis. The parameters in equation (4.25) to (4.29) are calculated as follows:

$$Y_{01a} = v_a(Cd_{11} - Cd_{13}) \tag{4.31a}$$

$$Y_{01b} = v_b(Cd_{11} + R_{2b}Cd_{12} + Cd_{13}) \tag{4.31b}$$

$$Y_{01c} = v_c(Cd_{11} + R_{2c}Cd_{12} + Cd_{13}) \tag{4.31c}$$

$$Y_{02b} = \frac{v_b(R_{2b}Cd_{22} + 2Cd_{12})}{R_{2b}} \tag{4.31d}$$

$$Y_{02c} = \frac{v_c(R_{2c}Cd_{22} + 2Cd_{12})}{R_{2c}} \tag{4.31e}$$

where $v_{a,b,c}$ are the distinct phase velocities for mode a, b, and c respectively. The phase velocities and the ratios of voltages are given by

$$v_a = (B_1 - B_3)^{-1/2} \tag{4.32a}$$

$$v_{b,c} = \left[\frac{B_1 + B_3 + B_5}{2} \pm \frac{1}{2}\sqrt{(B_1 + B_3 - B_5)^2 + 8B_2B_4}\right]^{-1/2} \quad \textbf{(4.32b)}$$

$$R_{2b,2c} = \frac{1}{2B_2}\left[-(B_1 + B_3 - B_5) \pm \sqrt{(B_1 + B_3 - B_5)^2 + 8B_2B_4}\right] \quad \textbf{(4.33)}$$

where the constants $B_1 \ldots B_5$ are related to the elements of the capacitance matrices by:

$$B_1 = \frac{Cd_{11}(Ca_{11}Ca_{22} - Ca_{12}^2) + Cd_{12}Ca_{12}(Ca_{13} - Ca_{11}) + Cd_{13}(Ca_{12}^2 - Ca_{13}Ca_{22})}{v_o^2[Ca_{11} - Ca_{13}]\,[Ca_{22}(Ca_{11} + Ca_{13}) - 2Ca_{12}^2]}$$

$$B_2 = \frac{Cd_{12}(Ca_{11}Ca_{22} - Ca_{12}^2) + Cd_{22}Ca_{12}(Ca_{13} - Ca_{11}) + Cd_{12}(Ca_{12}^2 - Ca_{13}Ca_{22})}{v_o^2[Ca_{11} - Ca_{13}]\,[Ca_{22}(Ca_{11} + Ca_{13}) - 2Ca_{12}^2]}$$

$$B_3 = \frac{Cd_{13}(Ca_{11}Ca_{22} - Ca_{12}^2) + Cd_{12}Ca_{12}(Ca_{13} - Ca_{11}) + Cd_{11}(Ca_{12}^2 - Ca_{13}Ca_{22})}{v_o^2[Ca_{11} - Ca_{13}]\,[Ca_{22}(Ca_{11} + Ca_{13}) - 2Ca_{12}^2]}$$

$$B_4 = \frac{Cd_{11}Ca_{12}(Ca_{13} - Ca_{11}) + Cd_{12}(Ca_{11}^2 - Ca_{13}^2) + Cd_{13}Ca_{12}(Ca_{13} - Ca_{11})}{v_o^2[Ca_{11} - Ca_{13}]\,[Ca_{22}(Ca_{11} + Ca_{13}) - 2Ca_{12}^2]}$$

$$B_5 = \frac{Cd_{22}(Ca_{11}^2 - Ca_{13}^2) + 2Cd_{12}Ca_{12}(Ca_{13} - Ca_{11})}{v_o^2[Ca_{11} - Ca_{13}]\,[Ca_{22}(Ca_{11} + Ca_{13}) - 2Ca_{12}^2]}$$

where v_o is the speed of light in free space. It can be seen that the evaluation of the capacitance matrices [Cd] and [Ca] allows the calculation of the admittance parameters of the admittance matrix and, consequently, a knowledge of the S-parameters of the resonator (resonant curve).

4.3.2.1 Derivation of the Capacitance Element Matrices

Because the propagation modes in microstrip are assumed to be TEM, having components of neither the electric nor the magnetic fields in the direction of propagation, the determination of the characteristic impedance and propagation constant requires a study of fields only over the line cross section, within which they must obey Laplace's equation and the imposed boundary conditions [78]. Figure 4.11 shows a cross-sectional view of a three

coupled microstrip transmission line system. Let V1, V2, V3 and Q1, Q2, Q3 represent the voltage and total charge per unit length on conductors 1, 2, 3 respectively (see Figure 4.11). The charges and voltages are then related to the structure's per-unit-length static capacitances according to the charge equations:

$$Q_1 = c_{11}V_1 + c_{12}(V_1 - V_2) + c_{13}(V_1 - V_3) \tag{4.34a}$$

$$Q_2 = c_{21}(V_2 - V_1) + c_{22}V_2 + c_{23}(V_2 - V_3) \tag{4.34b}$$

$$Q_3 = c_{31}(V_3 - V_1) + c_{32}(V_3 - V_2) + c_{33}V_3 \tag{4.34c}$$

where c_{ii} (i = 1, 2, 3) are the self-capacitance of strip "i" per-unit-length and c_{ij} (i = 1, 2, 3 and j = 1, 2, 3 with $i \neq j$) the mutual capacitance between strip "i" and strip "j" per-unit-length. Due to symmetry, $c_{11} = c_{33}$, $c_{13} = c_{31}$, and $c_{12} = c_{21} = c_{23} = c_{32}$. Equation (4.34) can be re-written in a matrix form as shown in equation (4.35):

$$\begin{bmatrix} Q_1 \\ Q_2 \\ Q_3 \end{bmatrix} = \begin{bmatrix} (c_{11}+c_{12}+c_{13}) & -c_{12} & -c_{13} \\ -c_{12} & (2c_{12}+c_{22}) & -c_{12} \\ -c_{13} & -c_{12} & (c_{11}+c_{12}+c_{13}) \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} \tag{4.35}$$

The elements of the capacitance matrix in equation (4.35) are the elements of the capacitance matrices Cd_{ij} and Ca_{ij} (i, j = 1, 2, 3) of the structure in which [Cd] is evaluated with the dielectric in place and [Ca] evaluated with the dielectric replaced by air.

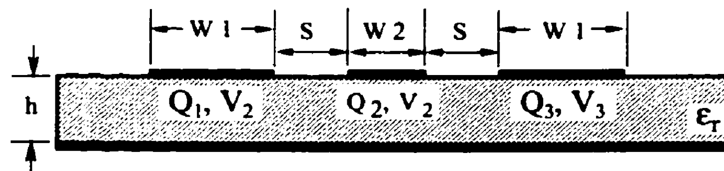


Figure 4.11 Cross-sectional view of a microstrip composed of a three coupled transmission line system

4.3.2.2 Numerical Solution of Laplace's Equation Using the Finite-Difference Method

As mentioned in previously, the fields over the line cross section of the structure must obey the two dimensional Laplace equation:

$$\frac{\partial^2\phi}{\partial x^2} + \frac{\partial^2\phi}{\partial y^2} = 0 \qquad (4.36)$$

In this section, the numerical solution of equation (4.36) is presented using the finite difference method. Once the equation is solved, the total charge per-unit-length on each conductor can be calculated and the capacitance matrix can be evaluated. In the finite difference method, Laplace's equation may be written by considering the configuration shown in Figure 4.12. Let the potential at "P" be ϕ_P and then expand the potential in Taylor's series about "P" to find the potentials at other points:

$$\phi_A = \phi_P - \Delta\frac{\partial\phi}{\partial x} + \frac{\Delta^2\partial^2\phi}{2!\,\partial x^2} - \frac{\Delta^3\partial^3\phi}{3!\,\partial x^3} + \dots\ \dots \qquad (4.37)$$

$$\phi_B = \phi_P + \Delta\frac{\partial\phi}{\partial x} + \frac{\Delta^2\partial^2\phi}{2!\,\partial x^2} + \frac{\Delta^3\partial^3\phi}{3!\,\partial x^3} + \dots\ \dots \qquad (4.38)$$

$$\phi_C = \phi_P - \Delta\frac{\partial\phi}{\partial y} + \frac{\Delta^2\partial^2\phi}{2!\,\partial y^2} - \frac{\Delta^3\partial^3\phi}{3!\,\partial y^3} + \dots\ \dots \qquad (4.39)$$

$$\phi_D = \phi_P + \Delta\frac{\partial\phi}{\partial y} + \frac{\Delta^2\partial^2\phi}{2!\,\partial y^2} + \frac{\Delta^3\partial^3\phi}{3!\,\partial y^3} + \dots\ \dots \qquad (4.40)$$

When the fourth order and higher terms are ignored, and equation (4.36) is used, the above relations yield:

$$\phi_A + \phi_B + \phi_C + \phi_D = 4\phi_P \qquad (4.41)$$

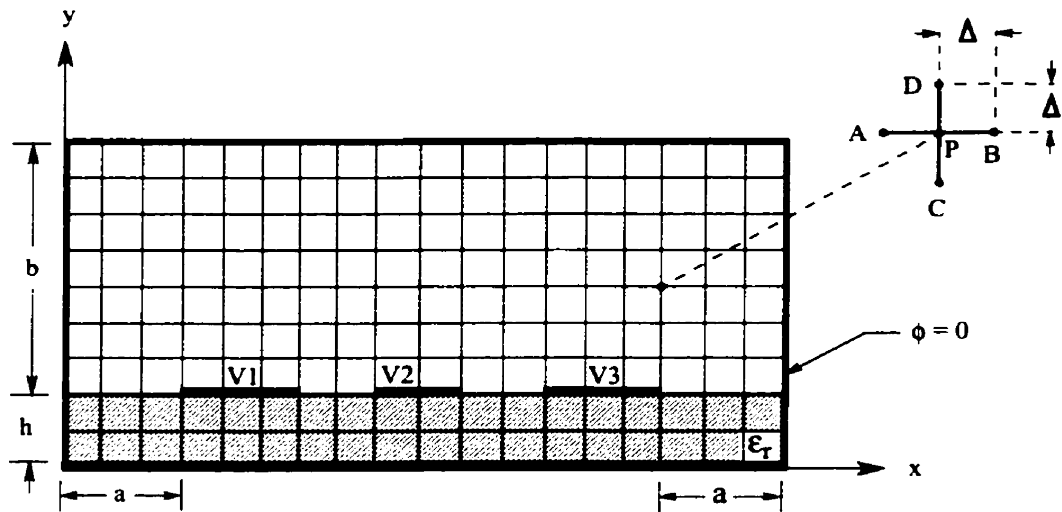


Figure 4.12 Enclosed microstrip lines for analysis by the finite difference method

The most common method of solving the finite difference equation (4.41) is the successive over-relaxation (SOR) method. This numerical method requires a systematic approach of assuming (by guessing) the net point potentials at every unknown point and comparing the left-hand side and right-hand side of equation 4.41. In subsequent passes through the array of potential values, with ϕ_P being replaced by $(\phi_A + \phi_B + \phi_C + \phi_D)/4$, the calculations converge to produce an array of potentials ϕ_i that satisfy Laplace's equation and the imposed boundary conditions. Once the potential distribution in the microstrip cross-section is obtained, the field distribution and the charge on each strip can be calculated from the integral equation:

$$Q = \varepsilon_o \varepsilon_r \oint E_n \cdot ds \qquad \textbf{(4.42)}$$

where the line integral is taken over a surface enclosing the strip conductor. Capacitance is obtained as the ratio of charge to voltage. Details of this method and the form of the finite difference equations can be found from **[78][79][80]** and are not presented here.

In general, the Finite Difference method requires a boundary condition. In this numerical simulation, a fictitious boundary that encloses the three coupled lines as shown in

Figure 4.12 is used even though our resonator is operated in an open environment (without an enclosure). The presence of the boundary may alter the impedances of the structure, especially when the boundary is placed close to the transmission lines. In order to avoid the effects of the boundary on the calculated impedances, the top-wall distance of the boundary should be greater than ten times the thickness of the substrate [82] and the side-wall distance should be two times greater than the width of the line [83].

4.3.2.3 Calculation of the Capacitance Coefficient Matrix

For the case of three coupled lines as shown in Figure 4.12, the elements of capacitance matrices [Cd] and [Ca] can be calculated as follows: 1) Set the voltage on the conductors to be V1 = 1, V2 = V3 = 0. 2) After solving Laplace's equation and calculating charges Q1, Q2, Q3, the elements Cd_{ij} of the capacitance matrix are obtianed from $Cd_{11} = Q1$; $Cd_{21} = Q2$; and $Cd_{31} = Q3$. 3) Due to symmetry, $Cd_{33} = Cd_{11}$, $Cd_{13} = Cd_{31}$, and $Cd_{12} = Cd_{23} = Cd_{32} = Cd_{21}$. 4) Recalculate charges on conductors with the voltages set as V1 = V3 = 0 and V2 = 1 and the element Cd_{22} obtained from $Cd_{22} = Q2$. 5) Calculate the elements of the capacitance matrix [Ca] by replacing the dielectric region with air.

As mentioned in section 4.3.1, a three coupled microstrip line system behaves as three isolated single microstrip lines as the distance between lines is increased. Furthermore, there is no closed form expression for determination of the relationship between the physical geometry of three coupled lines and the mode impedances. For a starting point, it is assumed that three coupled lines can be built as three isolated lines in which the two outer conductors have characteristic impedance of 50Ω while the center line has a characteristic impedance of 100Ω. The reason for choosing 50Ω is to match the impedance of the resonator to the impedance of the source (usually 50Ω), so that maximum power can be transfered. The resonant curves, given various spaces between these lines, are then simulated. From the simulation results, the spacing between the lines is chosen such that one obtains as high a

sensitivity as possible. For a single microstrip transmission line, the width of the line can be determined from a given characteristic impedance using the following expression **[81]** (assuming that the conductor has zero thickness):

$$W = \begin{cases} h\left(\frac{8e^{A}}{e^{2A}-2}\right) & if \quad A > 1.52 \\ \frac{2h}{\pi}\left\{B - 1 - \ln(2B-1) + \frac{\varepsilon_r - 1}{2\varepsilon_r}\left[\ln(B-1) + 0.39 - \frac{0.61}{\varepsilon_r}\right]\right\} & if \quad A \le 1.52 \end{cases} \quad \textbf{(4.43)}$$

where

$$A = \frac{Z_o}{60}\sqrt{\frac{\varepsilon_r + 1}{2}} + \frac{\varepsilon_r - 1}{\varepsilon_r + 1}\left(0.23 + \frac{0.11}{\varepsilon_r}\right) \quad \text{and} \quad B = \frac{60\pi^2}{Z_o\sqrt{\varepsilon_r}}$$

Z_O is the characteristic impedance of the microstrip line, "h" the substrate thickness, and ε_r the relative dielectric constant of the substrate. By using a substrate with dielectric constant $\varepsilon_r = 2.5$ and thickness of 62 mils, the widths of the 50Ω and 100Ω transmission lines are 176 mils (~ 4.47 mm) and 50 mils (~ 1.27 mm) respectively.

Also, the characteristic impedance Z_O of a microstrip transmission line can be determined from the line width "W" and the substrate thickness "h" using the following expression **[81]**:

$$Z_o = \begin{cases} \frac{\eta}{2\pi\sqrt{\varepsilon_{re}}}\ln\left(\frac{8h}{W} + 0.25\frac{W}{h}\right) & if \ (W/h \le 1) \\ \frac{\eta}{\sqrt{\varepsilon_{re}}}\left[\frac{W}{h} + 1.393 + 0.667\ln\left(\frac{W}{h} + 1.444\right)\right]^{-1} & if \ (W/h \ge 1) \end{cases} \quad \textbf{(4.44)}$$

where $\eta = 120\pi$, and ε_{re} is the effective dielectric constant of the medium in which the signal is propagated. The effective dielectric constant is related to the dielectric constant ε_r of the microstrip substrate by:

$$\varepsilon_{re} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} F\left(\frac{W}{h}\right) \tag{4.45}$$

$$F(W/h) = \begin{cases} (1 + 12h/W)^{-1/2} + 0.04(1 - W/h)^{-1/2} & if\ (W/h \le 1) \\ (1 + 12h/W)^{-1/2} & if\ (W/h > 1) \end{cases}$$

The structure parameters used to calculate the capacitance matrices are given as follows:

Width of outer conductors	W1 = W2 = 176 mils (~ 4.47 mm)
Width of center conductors	W2 = 50 mils (~ 1.27 mm)
Spacing between lines	S = 158 mils (~ 4.0 mm)
Conductor thickness	t = 0 mils
Substrate thickness	h = 62 mils (~ 1.57 mm)
Dielectric constant	$\varepsilon_r = 2.5$
Top-wall distance	b = 788 mils (~ 20 mm) (see Figure 4.12)
Side-wall distance	a = 590 mils (~ 15 mm) (see Figure 4.12)

A numerical routine was written to calculate the potential distribution in the microstrip cross-section in Figure 4.12. The potential at each of the nodes is calculated using the five-point formula (equation 4.41) which is known to give an error of the order Δ^2 (where Δ is the distance between two successive nodes). The execution of the developed finite-difference program continues until the difference between a new and old value of voltage at each node is less than 10^{-4}. After calculating charges on the conductors, the elements of the capacitance matrices [Cd] and [Ca] were found to be:

$$Cd = \begin{bmatrix} 10.832 & -0.224 & -0.057 \\ -0.224 & 5.273 & -0.224 \\ -0.057 & -0.224 & 10.832 \end{bmatrix} \varepsilon_o \quad \text{(F/m)}$$

$$Ca = \begin{bmatrix} 5.239 & -0.231 & -0.068 \\ -0.231 & 2.740 & -0.231 \\ -0.068 & -0.231 & 5.239 \end{bmatrix} \varepsilon_o \quad \text{(F/m)}$$

where [Cd] is the capacitance coefficient matrix with the dielectric in place, [Ca] is the capacitance coefficient matrix with the dielectric region replaced with air, and ε_o is the permittivity of free space ($\varepsilon_o = 8.8542\times10^{-12}$ F/m). Substituting the elements of calculated capacitance matrices back into equation (4.23) through to equation (4.33), the physical length of the microstrip resonator (effective $\lambda/4$) can be numerically calculated at a given design frequency. At this point, it should be noted that all parameters in these equations are functions of frequency although they are not explicitly expressed in terms of frequency. Assuming that the design frequency for an unloaded resonator is $f_0 = 2$ GHz, the required physical length was calculated to be 27.026 mm. Figure 4.13 shows the frequency response (transmission coefficient S_{21}) of the resonator. In order to verify the numerical calculations presented, the simulation results obtained from the Libra microwave simulator (HP EEsof software package; http://www.hp.com/go/hpeesof) are also presented in Figure 4.13. The Libra simulations were performed with the physical dimensions of the resonator given previously. In the simulation, the ground plane is assumed to be infinitely large. No boundary is assured to be enclosing the structure. From Figure 4.13, the results obtained by numerical analysis are agree well with Libra simulations except at the frequencies that are far from the resonant frequency. The discrepancy between the numerical analysis and Libra simulation results may be due to the presence of the boundary in numerical analysis. If this boundary is moved to infinity, it is believed that these two results would coincide. However, increasing the size of the boundary significantly increases the simulation time and was not practical in this investigation.

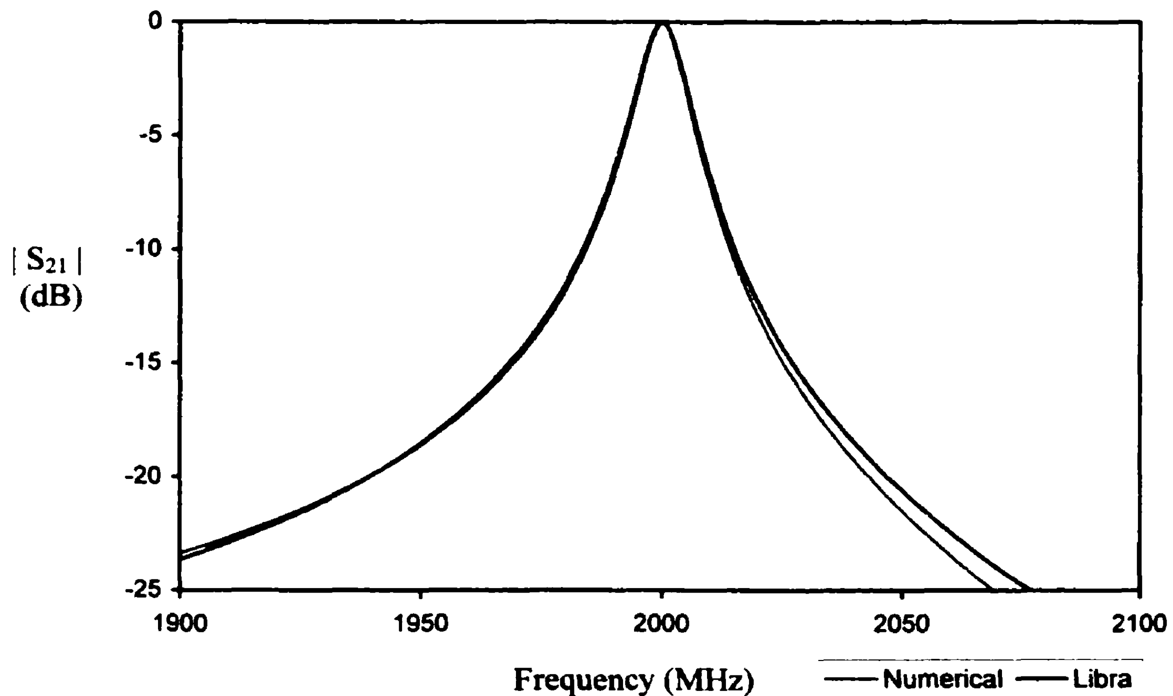


Figure 4.13 Numerical analysis and Libra simulation results that show the frequency response of the microstrip resonator (resonant curve)

The curves in Figure 4.14 are the plots of frequency response for a 2 GHz microstrip resonator for various spacings. The numerical calculations were performed with the widths of conductors and center conductor kept fixed. It can be seen that the -3dB bandwidth of the resonant curve increases when the spacing between transmission lines is decreased and vice versa. It should be noted that when the spacing is changed, that mutual capacitances also change. The physical length that is required for resonance at 2 GHz also changes. In summary, Table 4.1 contains the physical and electrical parameters of simulated resonators.

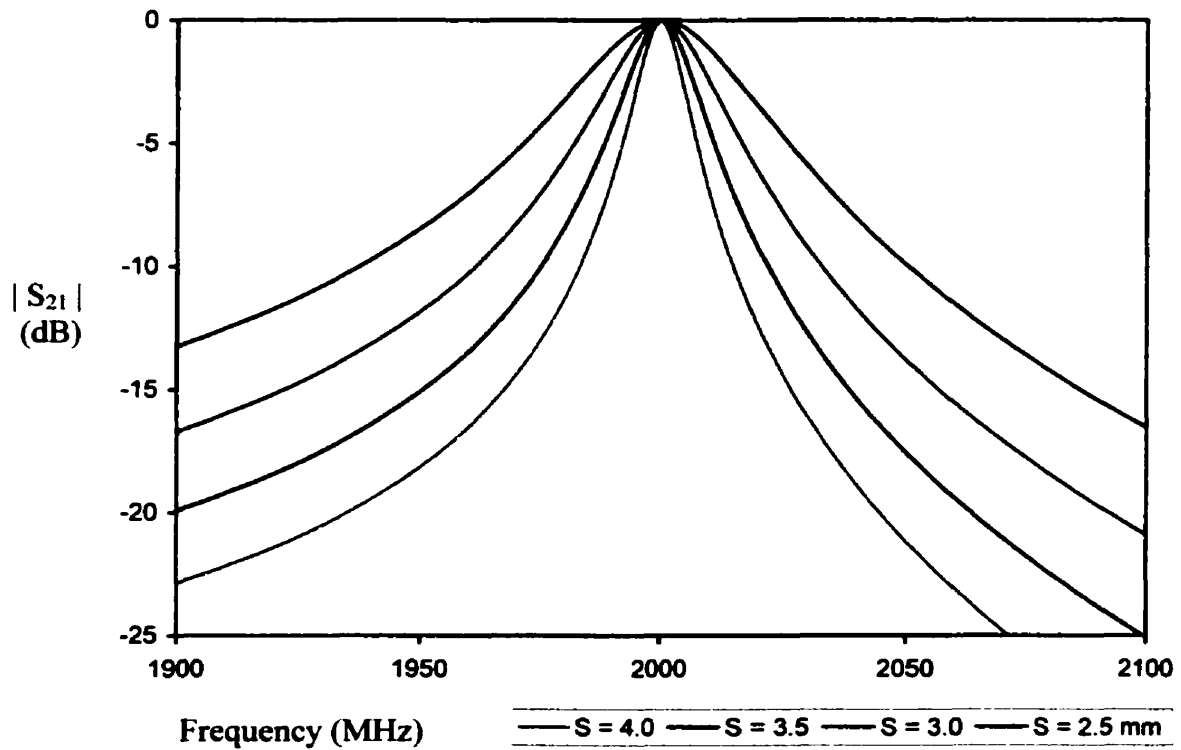


Figure 4.14 Resonant curves showing the dependence of the -3dB bandwidth on the spacing between three coupled microstrip transmission lines

Table 4.1: Physical and electrical parameters of simulated resonators

Width "W1" (mm)	Width "W2" (mm)	Spacing "S" (mm)	Length (mm)	Resonant f_r (MHz)	Bandwidth (MHz)	Quality Factor
4.47	1.27	4.0	27.03	2000	12	165
4.47	1.27	3.5	27.07	2000	16	125
4.47	1.27	3.0	27.13	2000	24	83
4.47	1.27	2.5	27.22	2000	37	54
4.47	1.27	2.0	27.34	2000	61	33

4.3.3 Frequency Sensitivity Of The Microstrip Resonator

Frequency sensitivity for a microstrip resonator is defined as the rate of change in resonant frequency with respect to the rate of change in capacitance at the tip. It is assumed that there is only capacitance C = Cs + dC at the tip (where Cs is stray capacitance, and dC is a change in capacitance). The resonant frequency changes due to a small change in capacitance dC can be numerically simulated. Figure 4.15 is plot of the frequency sensitivity versus resonant frequencies of a 2 GHz resonator (2 GHz for unloaded condition). Simulations were performed by calculating df_r/dC for different values of stray capacitance Cs. Simulations were performed for the spacing S = 4 mm, and the characteristic impedance of the resonator line Z_0 = 100 Ω. For comparison, the frequency sensitivity calculated using equation (4.15) is also included. In equation (4.15), the characteristic impedance of the resonator line (the center line of three coupled lines) was calculated using equation (4.44). In practice, for the case of three coupled microstrip lines, the characteristic impedance of the center line can not be explicitly calculated without the need of a numerical routine. However, we can see from Figure 4.15 that, for a spacing between the transmission lines of 4 mm, the resonator line (center line) behaves as an isolated transmission line and the frequency sensitivity can be approximately calculated using equation (4.15).

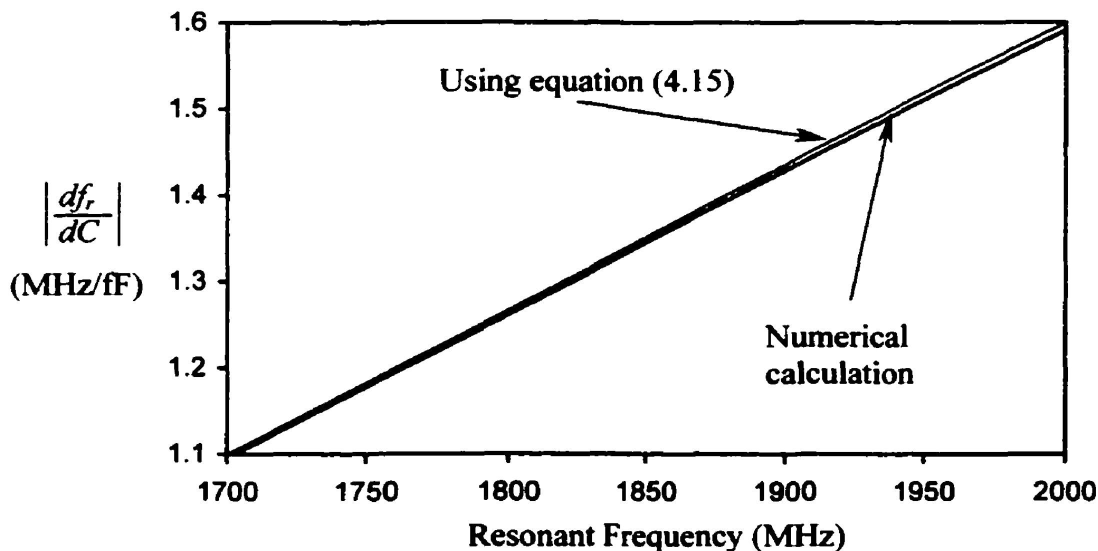


Figure 4.15 Frequency sensitivity of a microstrip resonator versus resonant frequency

Figure 4.16 shows the dependence of frequency sensitivity on the characteristic impedance of the resonator line. It can be seen from these curves that the frequency sensitivity increases proportional to the characteristic impedance at any given resonant frequency.

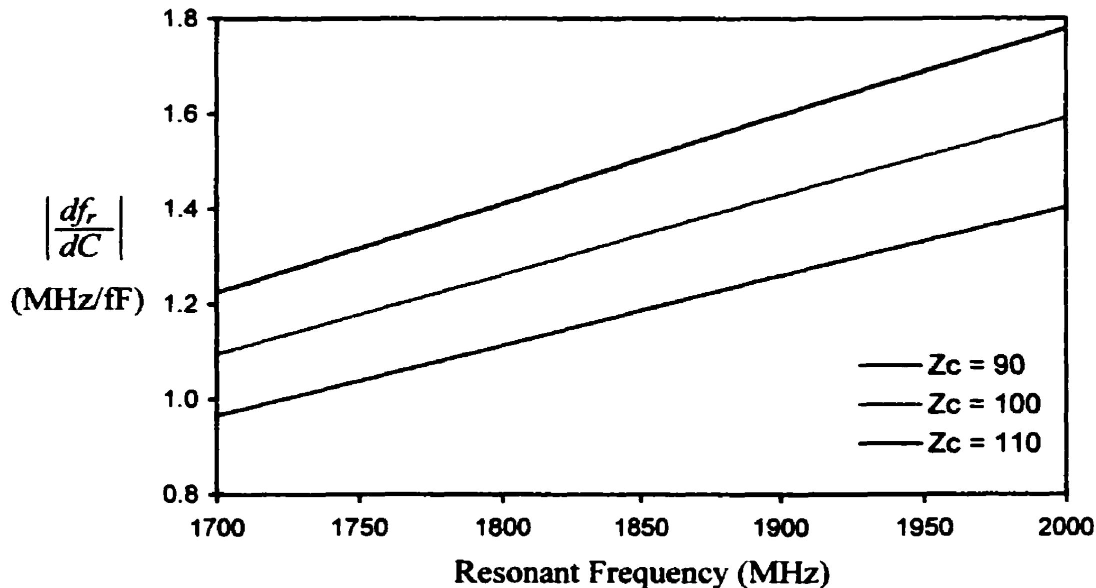


Figure 4.16 Frequency sensitivity versus resonant frequency for three resonators with different characteristic impedance.

As mentioned in section 4.3, the sensor sensitivity can be increased in two ways: by increasing the resonant frequency or by reducing the resonator bandwidth. Analysis shows that the bandwidth can be reduced if the spacing "S" between transmission lines is increased. In practice, the microstrip resonator is not a lossless device. Increasing the spacing "S" also increases the loss and therefore degrades the performance of the resonator. For this reason, the final version of the resonator was chosen such that the resonant frequency was 2 GHz (unloaded condition); it had a characteristic impedance of about 110 Ω (W2 ~ 1 mm), and a spacing between lines of 4.0 mm.

4.3.4 Calculations of RF-Voltage at the Tip

For the SSCM measurements, it has been observed that the magnitude of the RF-voltage at the resonator tip (junction) is a very important parameter. As this voltage is increased, the nature of the depletion layer at the junction is affected and results in aliasing effects at boundary between doped regions [64]. For this reason, the influence of the RF-voltage at the tip is investigated in this section.

Figure 4.17 is a schematic diagram of the microstrip resonator with a load admittance Y_T connected at the tip. The resonator is driven with a source of constant amplitude E(t) through a source admittance Y_S. The output of the resonator is terminated with load admittance Y_L. Considering the resonator in this case as a three port lossless network, the relationship between the terminal currents and terminal voltages are governed by a system of equations (4.20). These equations are re-written here:

$$I_i = Y_{11}V_i + Y_{13}V_o + Y_{15}V_T \quad \textbf{(4.46a)}$$

$$I_o = Y_{13}V_i + Y_{11}V_o + Y_{15}V_T \quad \textbf{(4.46b)}$$

$$I_T = Y_{15}V_i + Y_{15}V_o + Y_{55}V_T \quad \textbf{(4.46c)}$$

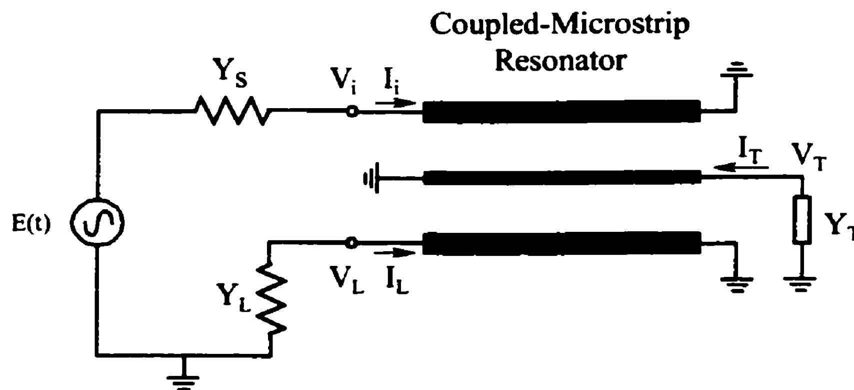


Figure 4.17 Schematic diagram of the resonator used for calculation of tip voltage.

The terminal conditions for the resonator shown in Figure 4.17 are as follows:

$$I_o = -Y_L V_o \quad \text{(4.47a)}$$
$$I_T = -Y_T V_T \quad \text{(4.47b)}$$
$$I_i = Y_s (E - V_i) \quad \text{(4.47c)}$$

Substituting equation (4.47a, b, c) into equations (4.46a, b, c) and simplifying yields the tip voltage as a function of source voltage and impedance for the three ports:

$$V_T = \frac{Y_{12eq} Y_s E}{Y_{12eq}^2 - (Y_{11eq} + Y_s)(Y_{22eq} + Y_T)} \quad \text{(4.48)}$$

where

$$Y_{11eq} = Y_{11} - \frac{Y_{13}^2}{Y_{11} + Y_L}$$

$$Y_{12eq} = Y_{15} - \frac{Y_{13} Y_{15}}{Y_{11} + Y_L}$$

$$Y_{22eq} = Y_{55} - \frac{Y_{15}^2}{Y_{11} + Y_L}$$

Assuming that the source voltage is a sinusoidal signal with a unit amplitude $E(t) = \sin(2\pi f t)$, the tip voltage in the time domain becomes:

$$V_T(t) = \left| \frac{Y_{12eq} Y_s}{Y_{12eq}^2 - (Y_{11eq} + Y_s)(Y_{22eq} + Y_T)} \right| E(2\pi f t + \theta) \quad \text{(4.49)}$$

where θ is the phase difference between the source and tip voltage signal given by:

$$\theta = \arg\left(\frac{Y_{12eq} Y_s}{Y_{12eq}^2 - (Y_{11eq} + Y_s)(Y_{22eq} + Y_T)} \right) \quad \text{(4.50)}$$

Figure 4.18 shows plots of the numerical analysis and Libra simulation results that show the open circuit voltage at the tip in the time domain. This is done by setting the admittance $Y_T = 0$ in equation (4.48). These results exactly match each other. The calculations were performed for a 2 GHz resonator at the resonant frequency. In addition, the load and source admittances (Y_L and Y_S) are assumed to be 0.02 Ω^{-1} (admittance of the measuring system). The curves in Figure 4.18 show that the maximum tip voltage can be 16 times higher than the source voltage. In practice, there is stray capacitance existing between the tip and sample. The magnitude of this capacitance is about 50 - 100 fF. The theoretical calculation, given this stray capacitance, would lower the tip voltage by about 7% at the resonant frequency. Furthermore, there is loss from the resonator when the tip is loaded on the sample. Therefore, it is expected that the tip voltage will be further decreased in normal operation as compared to Figure 4.18.

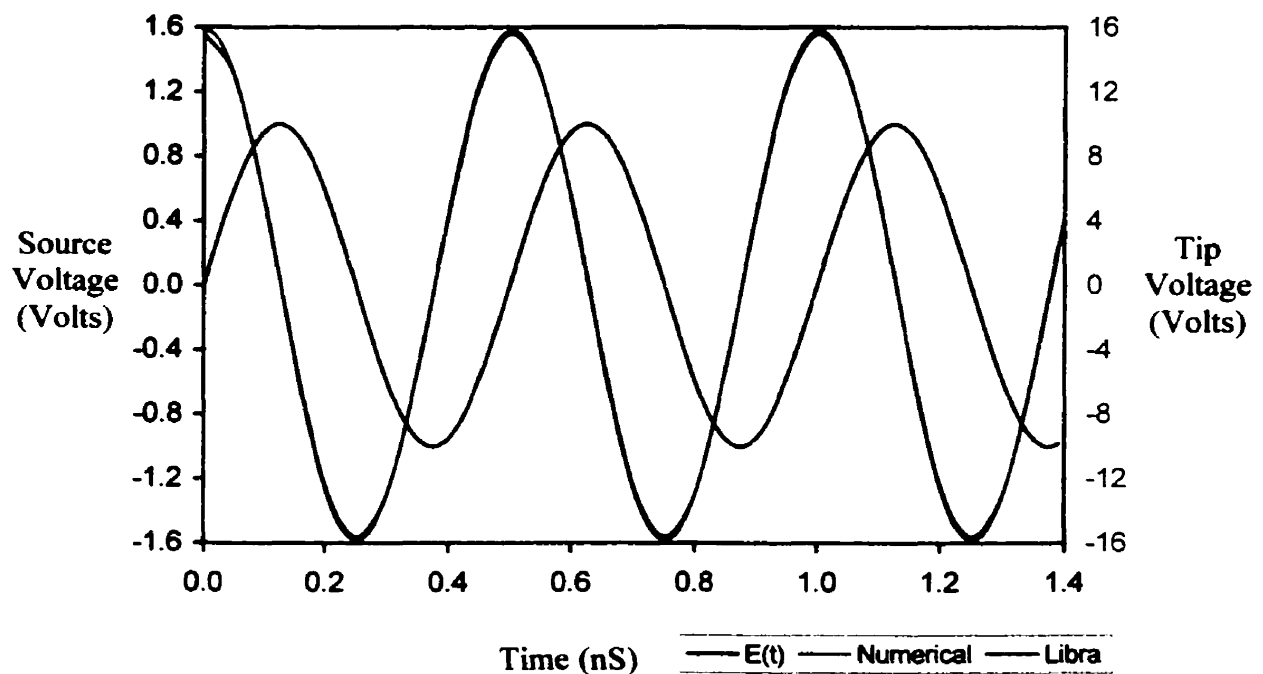


Figure 4.18 Numerical analysis and Libra simulation results showing the open circuit voltage at the tip of a 2 GHz microstrip resonator in the time domain. Calculations were performed at the resonant frequency.

The curve in Figure 4.19 represents the ratio of the tip voltage to source voltage as a function of frequency. As expected, the ratio is maximized at the resonant frequency. The decrease in the tip voltage away from resonance is due to the decreasing power that is coupled to the resonator line due to mismatch.

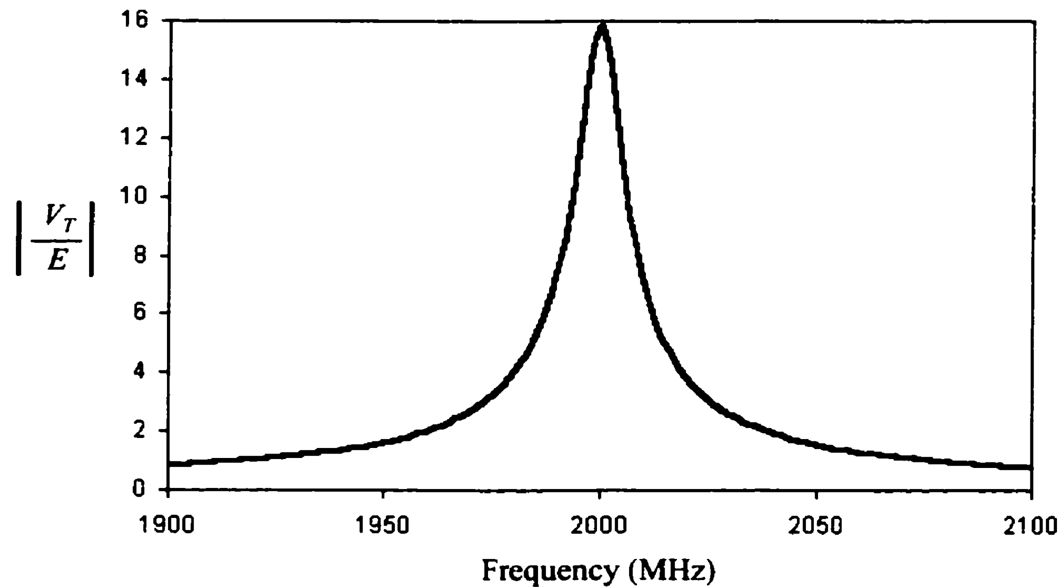


Figure 4.19 The ratio of tip voltage to source voltage as a function of drive frequency.

4.3.5 Simulations of the Effect of Tip-Sample Parameters on the Sensitivity

The calculations of sensitivity presented in previous sections were performed by assuming that there was only capacitance at the tip. Normally, the presence of other parameters such as resistance of the cantilever chip, spreading resistance, and contact resistance may affect the sensor sensitivity. The following discussion will investigate the effects of these parameters on the sensitivity.

4.3.5.1 The Effect of Cantilever Chip Resistance on Sensitivity

When a silicon cantilever chip is attached to the resonator and brought close to a sample surface, loss in the resonator significantly increases. The increase in loss at the resonant frequency is frequently observed to be about 7 - 12 dB when the tip is loaded on the sample. A part of the loss is due to the drop in RF field lines that are coupled to the sample. another contribution may be due to the presence of the cantilever chip resistance and any resistance that exists between the cantilever chip and ground plane (i.e. sample resistance, sample holder resistance, etc.). A schematic in Figure 4.20 is a model that is used for simulating the effect of tip resistance on sensitivity. In this model, R_T is the total of all resistances mentioned above, Cs is stray capacitance, and dC is the capacitance variation.

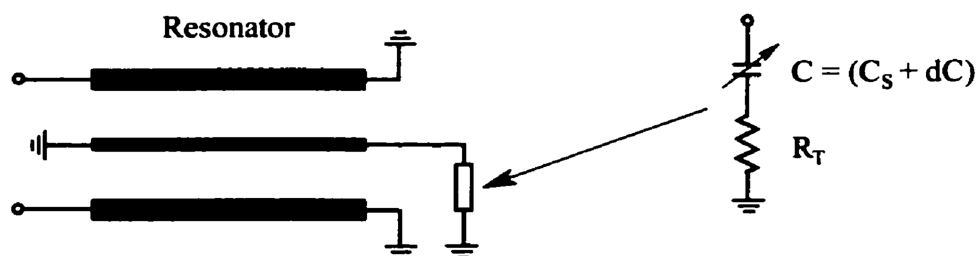


Figure 4.20 A circuit model used for simulating the effect of tip resistance on sensor sensitivity

The curves in Figure 4.21 are plots of frequency sensitivity and loss from the resonator at resonance as a function of resistance R_T. Numerical calculations were performed by using a stray capacitance of 75 fF. For simplifcity, it is also assumed that all the losses from the resonator are due to the resistance R_T. In Figure 4.21 frequency sensitivity stays constant when R_T is small and drops to a low value when the resistance R_T is comparable to the RF impedance of a stray capacitor at the operating frequency. The RF impedance of 75 fF stray capacitance was calculated to be about 1.15 kΩ at 1.85 GHz (1.85 GHz is a typical operating frequency of our sensor). The change in frequency sensitivity can be understood because when R_T is much less than the RF impedance of the stray capacitor, the resonator line directly

sees the stray capacitor, whereas, when the impedance R_T is much larger than that of the stray capacitor, the resonator line does not see the capacitor. Also shown in this Figure, the loss from the resonator at resonance begins as soon as resistance R_T starts to increase. Besides loss, theoretical calculations show that the quality factor (Q) drops from 165 to 20 as the resistance R_T is increased from 1 - 1000 Ω.

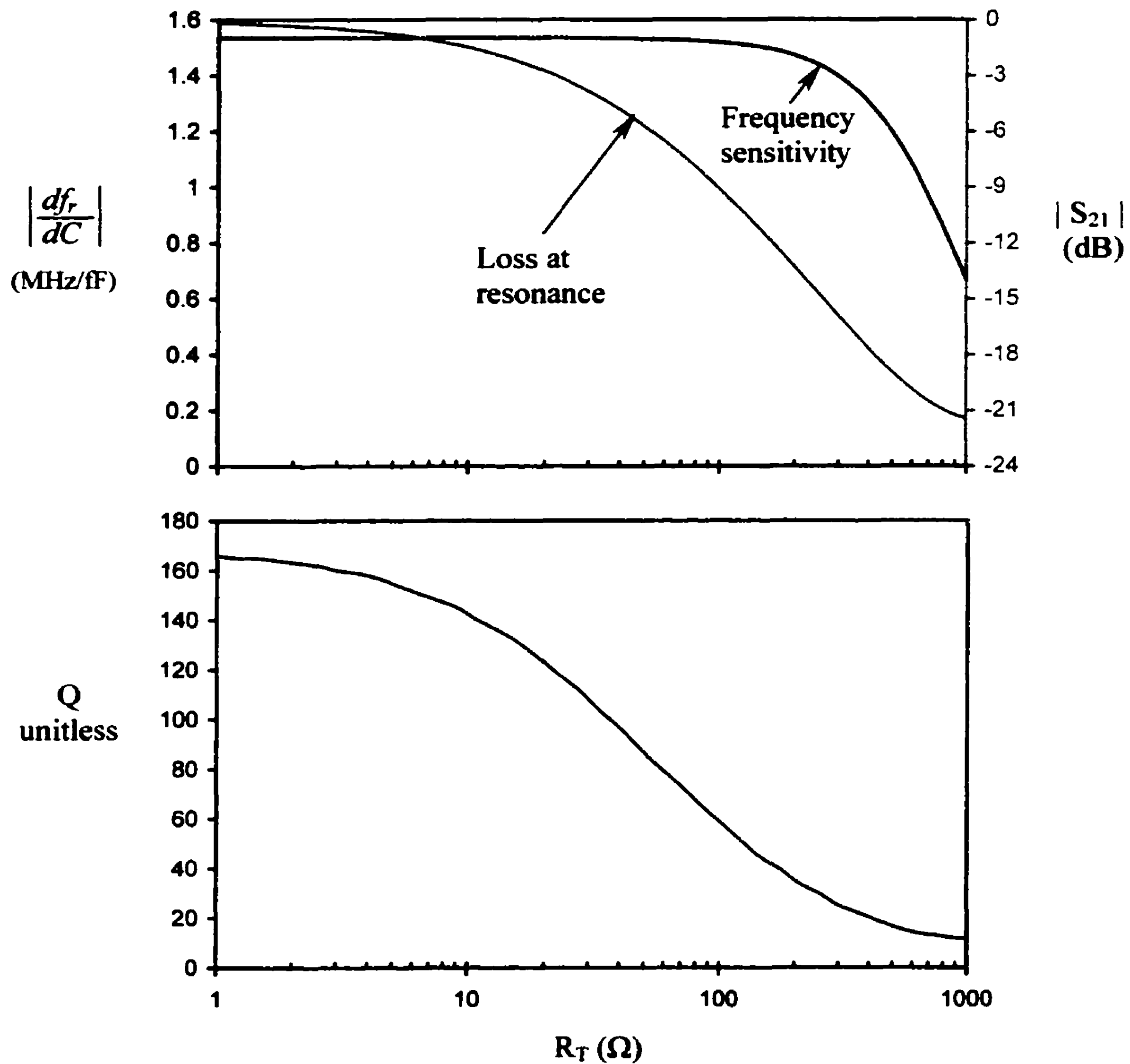


Figure 4.21 Numerical simulation results showing the frequency sensitivity, loss at resonance, and quality factor of the resonator as a function of the tip resistance.

In practice, the magnitude of the resistance R_T is unknown. When the resonator is loaded, however, the loss and quality factor of the resonator is routinely observed to be (10 - 15 dB) and (75 - 50) respectively. If the model in Figure 4.20 is correct, we expect that the resistance R_T should be small compared to the RF impedance of the stray capacitor. Therefore, the presence of a small tip resistance may not significantly effect the frequency sensitivity. However, it does effect the voltage sensitivity (dv/df) or total sensitivity (dv/dC) due to the increased loss and decreased Q for the resonant circuit.

4.3.5.2 The Effect of Spreading and Contact Resistance on Sensitivity

In this section, the effect of spreading resistance and contact resistance on the sensitivity is simulated. Figure 4.22 represents the circuit model that is used for simulation purposes. In this model, R_{sp} is the spreading resistance, R_C the contact resistance, C_C the contact capacitance of the tip-sample contact area, and C_S is the stray capacitance. Again stray capacitance is assumed to be 75 fF and a typical operating frequency of 1.85 GHz is used. In the computation, the spreading resistance and contact resistance were used as input parameters while the change in contact capacitance was held constant. The change in contact capacitance "dC" was then used to determine the frequency sensitivity (df/dC) by calculating the shift in resonant frequency "df" as a function of function of R_{sp} and R_C.

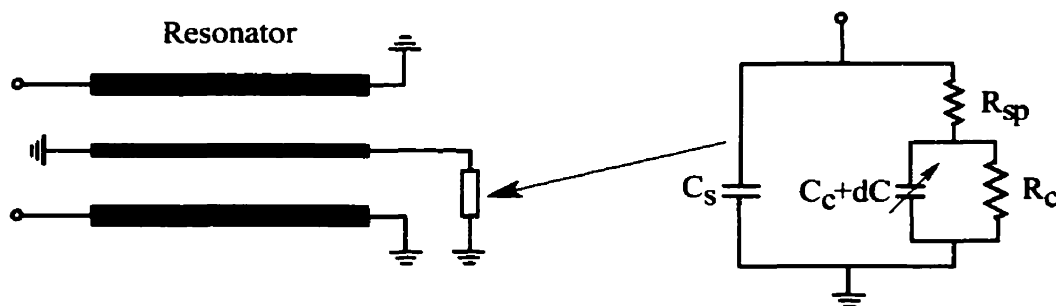


Figure 4.22 A circuit model used for simulating the effect of spreading resistance and contact resistance on sensor sensitivity

After simulation, the frequency sensitivity as a function of spreading resistance for various values of contact resistance is plotted as shown in Figure 4.23. The curves in this figure show that the frequency sensitivity starts dropping to a lower value when the ratio of the contact resistance to spreading resistance is smaller than about 100. For a small tip-to-sample contact area, however, the contact resistance is at least four orders of magnitude higher than the spreading resistance at any dopant concentration level except for the case where the junction is highly forward biased (this can be easily verified by theoretical calculations of spreading resistance and contact resistance presented in Chapter 3). Therefore, the presence of spreading resistance should not affect the frequency sensitivity. Also apparent from Figure 4.23, when the contact resistance is decreased to a value that is comparable to the RF impedance of the stray capacitor, the frequency sensitivity decreases significantly even when the spreading resistance is negligibly small compared with the impedance of other circuit parameters. For example, when the contact resistance is equal to 1 kΩ, the frequency sensitivity is about 1 MHz/fF even when the spreading resistance is replaced by a short circuit (1Ω in this case). Decreasing the contact resistance does not only reduce the frequency sensitivity (df/dC), but also increases the loss and decreases the Q of the resonator. The overall result is a decrease in voltage sensitivity (dv/df). Figure 4.24 shows plots of the Q and loss at resonant frequency as a function of the contact resistance. The calculations were performed by neglecting the spreading resistance in the circuit model. It can be seen that loss and Q start changing when the contact resistance is decreased below $10^6\,\Omega$. As defined in equation (4.1), the overall sensitivity is the product of (dv/df) and (df/dC). Decreasing both of these terms causes a dramatic degradation in the sensor sensitivity. These theoretical results may help to explain the drop in the measured voltage derivative *dC/dV* in the heavily doped regions of metal-semiconductor contacts observed using the SSCM technique (as discussed in Chapter 6).

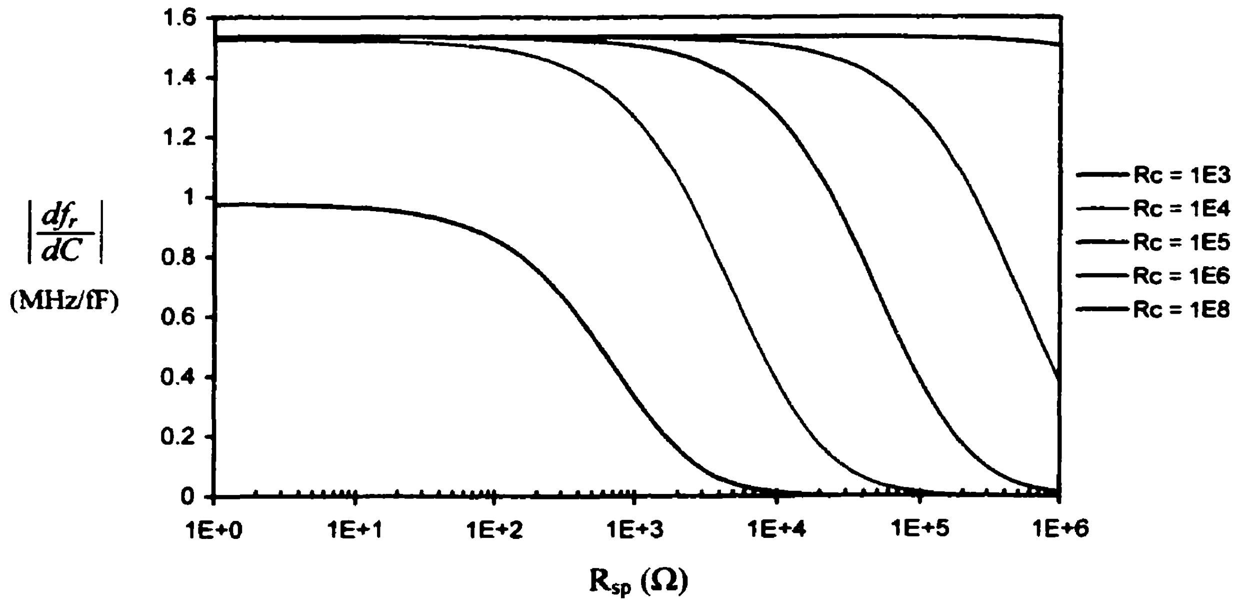


Figure 4.23 Numerical simulation results showing the dependence of frequency sensitivity on the spreading resistance and contact resistance.

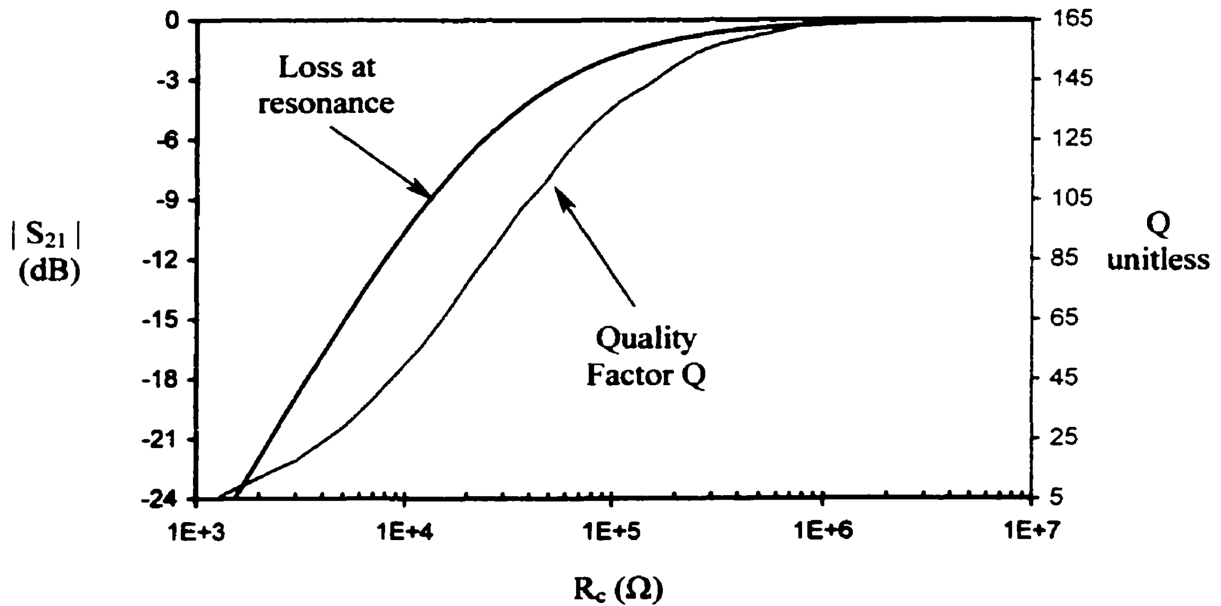


Figure 4.24 Numerical simulation results showing the Quality factor "Q" and losses of the resonator at resonance as a function of the contact resistance

4.3.6 Experimental Results

In order to verify the theoretical predictions, the frequency response and sensitivity of the actual resonator were determined experimentally. The frequency response (S-parameters) of the resonator is easily measured with a Network Analyzer. Frequency sensitivity was determined by attaching a metallic ball at the end of the resonator, and then measuring frequency shift as a function of the distance between the ball and a ground plane placed beneath the ball (this experiment is presented in sub-section 4.3.6.2). However, explicit measurements of the tip voltage on the resonator have proved challenging. Experiments using high-impedance active probes, such as the GGB Model 28 Picoprobe, fail due to the large capacitance (1×10^{-13} F) introduced between the buffered probe and the resonator. Another, more sensitive, approach based on a non-contact electrostatic force measurement technique [84] has also been used. However, this technique still results in signal coupling to the resonator which perturbs the results. Therefore, estimation of the voltage on the resonator tip is based only on theoretical predictions.

4.3.6.1 Measurements of Resonator S-Parameters

The frequency response of the resonator was measured using a calibrated Hewlett-Packard (Model HP 8753E) Network Analyzer. A 110 Ω test resonator (110 Ω characteristic impedance of the center line) was fabricated from copper-clad, low-loss dielectric material ($\varepsilon_r = 2.5$). Figure 4.25 shows a photograph of an unloaded 2 GHz resonator. It should be noted that this resonator included two 90° bends that were ignored in theoretical calculations. These two bends do not serve any special function in the resonator design. Their only purpose is to provide extra space for SMA connectors and interconnect cables to be attached to the resonator. Simulations have shown that the presence of these bends adds a little extra capacitance at the input and output port of the resonator, resulting in a shift in resonant frequency of 2 - 3 MHz.

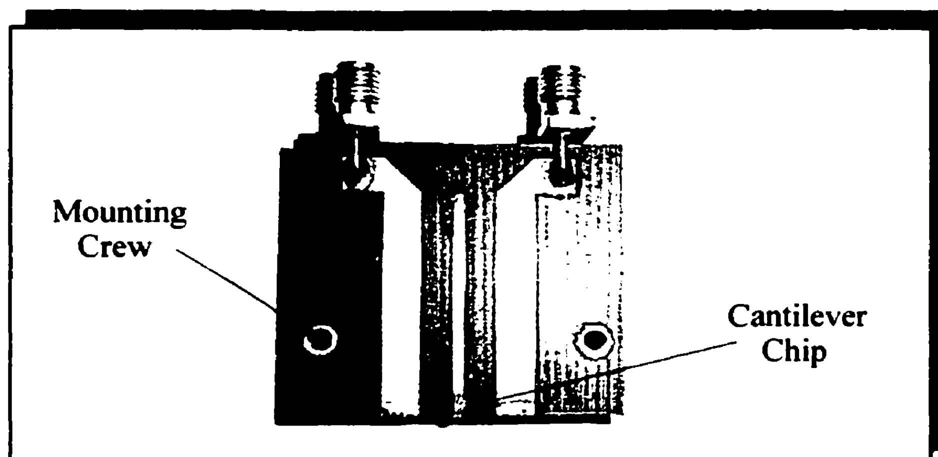


Figure 4.25 Photograph of a 2 GHz microstrip resonator

The curves in Figure 4.26 are plots of experimental results that show the frequency response of a 2 GHz unloaded microstrip resonator. For comparison, numerical calculations and simulation results are also included. It can be seen that the resonant frequency obtained by simulation and experiment agree within 3%. However, the loss and quality factor of the resonator were not well modeled. The discrepancy in these quantities can be understood because the resonator was assumed to be a lossless network for numerical calculation. Also, for the case of three coupled lines, the Libra simulator does not model the loss for the structure. In practice, there is some loss associated with the resonator such as radiation loss, loss due to mismatch, dielectric loss, conductor loss (ohmic loss), and loss through "vias" that are short-circuited to the transmission lines. In addition, a real resonator also has connectors that were not included in any simulation. In general, a "via" can be modeled as a lumped element consisting of a series inductance and resistance **[85]**. The inductance part can shift the resonant frequency while the resistance part introduces loss to the resonator.

The effect of "vias" can be investigated if the short-circuit elements at the end of transmission lines are replaced by equivalent circuits of "vias". Theoretical calculations show that, the resonant frequency is shifted down by 10 MHz and the loss at resonance is -3.87 dB if the inductance and resistance part of each via equivalent circuit are chosen to be 65 pH and 0.25 Ω respectively. In addition, the quality factor of the resonator drops from 165 to 125 under

these conditions. A resistance of 0.25 Ω may be too large to represent the resistance of a via. However, it is believed that these via holes actually contributed a part to the total loss that was observed from experimental results. To include the mentioned losses in simulation, the resonator had to be re-simulated using an Ensemble 5.1 software package (Ansoft Corporation; http://www.ansoft.com). The Ensemble simulation result is also plotted in Figure 4.26 for comparison. As expected, this simulation result is better fitted to experimental data than either the Libra simulation or the numerical calculation. Table 4.2 is a summary of experimental and simulation results for a 2 GHz microstrip resonator.

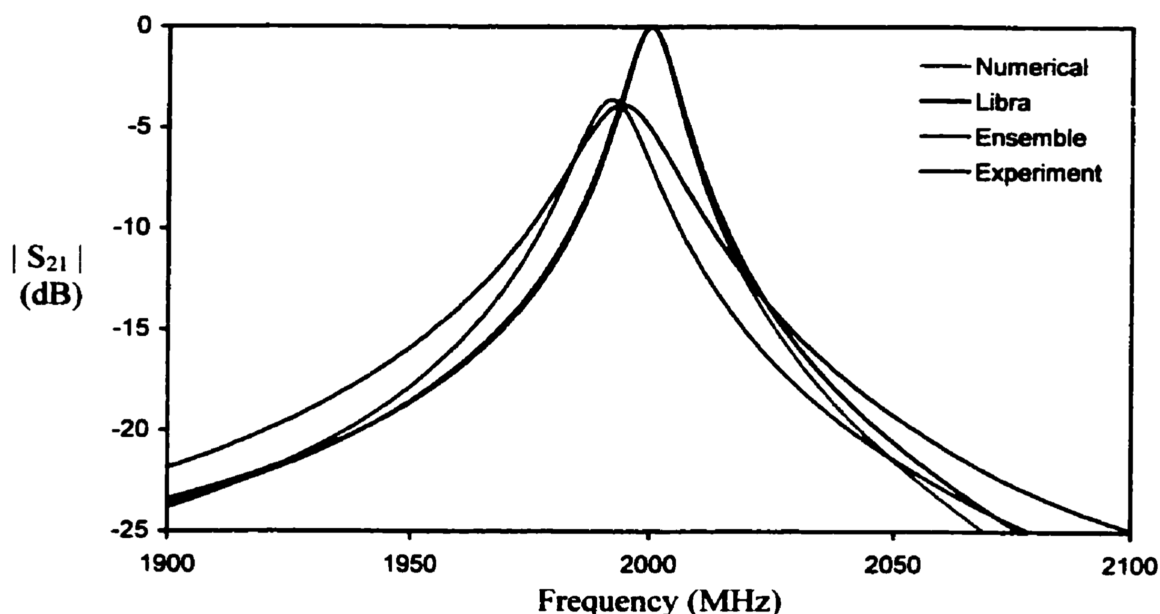


Figure 4.26 Simulation and experimental results showing the frequency response of a 2 GHz unloaded microstrip resonator

Table 4.2 Summary of simulation and experimental results obtained for the 2 GHz resonator

Electrical Properties	Experimental Results	Ensemble Simulation	Libra Simulation	Numerical Calculation
Resonant "f_r" (MHz)	1994	1992	2000	2000
Loss at resonance (dB)	3.9	3.6	0.0	0.0
-3dB Bandwidth (MHz)	21	16	12	12
Quality Factor "Q"	95	125	165	165

4.3.6.2 Measurements of the Frequency Sensitivity

In this section, the frequency shift as a function of capacitive loading is determined experimentally and compared with simulations. The experimental setup for determination of the frequency sensitivity is as follows: 1) A ball bearing of known diameter (2.37 mm) was attached to the end of the resonator in place of the cantilever/probe assembly and mounted on an XYZ translation stage as shown in Figure 4.27. Mounting the resonator in this configuration allowed the gap between the ball bearing and the grounded base-plate of the apparatus to be varied using a precision (80 turns/inch) Z microdrive of the translation stage. 2) A calibrated network analyzer (HP 8753E) was used to measure the resonator frequency response. 3) Measurements of resonant frequency as a function of separation gap "z" between the ball and ground plane were made with the network analyzer by touching the ball bearing to the ground plate, then backing the Z microdrive away from the ground plane. The resonant frequency was recorded as the Z microdrive was backing away from ground plane at every quarter turn.

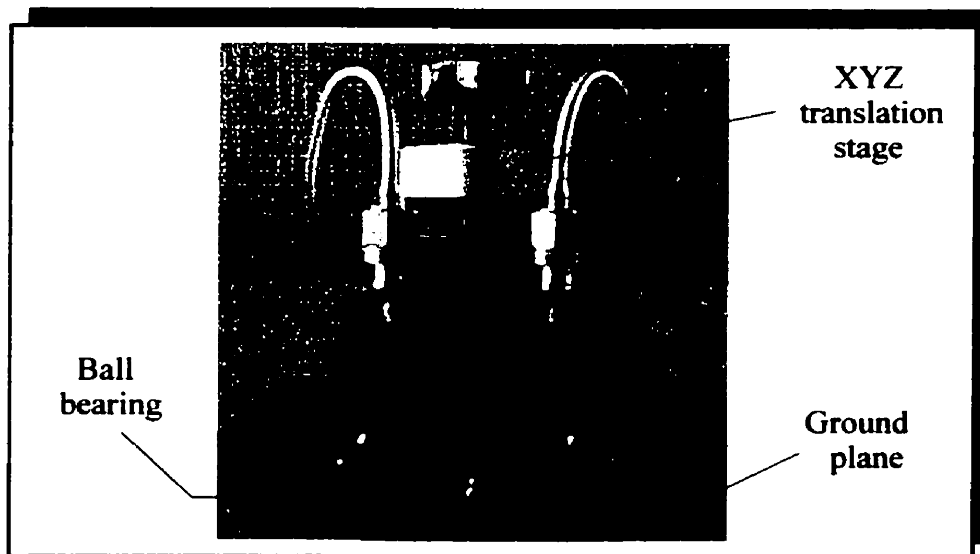


Figure 4.27 Experimental setup for testing the frequency sensitivity of the resonator

When not touching the base plate, the capacitance, C(z), between the ball bearing and the base plate can be described by the following equations **[86][87][88]**:

$$C(z) = 4\pi\varepsilon_o R \sinh\alpha \sum_{n=1}^{\infty} (\sinh n\alpha)^{-1} \qquad \textbf{(4.51)}$$

$$\alpha = \cosh^{-1}\left[\frac{z+R}{R}\right]$$

where "*z*" is the separation between the ball bearing and the ground plane and "*R*" is the radius of the ball bearing. It has been shown in **[86]** that the infinite sum in equation (4.51) can be approximated by:

$$C(z) = 2\pi\varepsilon_o R \ln\left(\frac{z+R}{R}\right) \qquad \textbf{(4.52)}$$

Using equation (4.52) it was possible to estimate the changes in capacitance between the ball bearing and the ground plane as "*z*" increases (this expression assumes that the resonator is perfectly grounded). Once the calculated capacitance C(z) was known along with the recorded resonant frequency, the measured shift in the resonant frequency as a function of capacitance C(z) could be calculated. Figure 4.28 shows plots of simulation and experimental results measured from a 100 Ω resonator line. Libra simulations were used to predict the frequency response of the resonator circuit. Changes in resonant frequency were simulated by adding a specified capacitance, corresponding to C(z), to the end of the modeled resonator circuit. The curves shown in Figure 4.28 show excellent agreement between simulation and experimental results. During the course of this experiment, the resonant frequency varied from 1650 MHz (close to the ground plane) to 1800 MHz (at the largest *z* value measured). In this range, the frequency sensitivity estimated from experimental results changed from 1.0 MHz/fF (at a resonant frequency of 1650 MHz) to 1.3 MHz/fF (at a resonant frequency of 1800 MHz). These values are what we expected from a resonator line with a 100 Ω characteristic impedance.

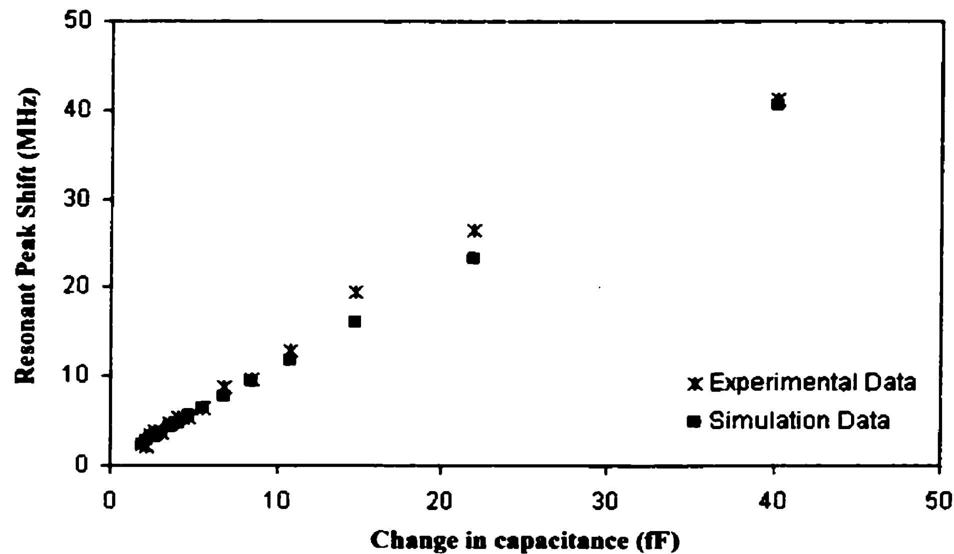


Figure 4.28 Simulation and experimental results showing shifts in resonant frequency due to changes in capacitance at the resonator tip

4.4 Development of the Peak Detector (RF Detector)

Detectors are essentially receivers which function on the basis of rectification of the RF signal through a non-linear resistive element (a diode). Generally detectors can be classified into two distinct types: the small-signal type (low level detectors), also known as a square-law detectors; and the large-signal type (high level detectors), also known as linear or peak detectors.

In these types of detectors, small-signal detector operation is dependent on the slope and curvature of the current-voltage (I-V) characteristic of the diode in the neighborhood of the bias point. The output of the detector is proportional to the power input to the diode. This means that the output voltage (or current) is proportional to the square of the input voltage (or current). On the other hand, the large-signal detector operation is dependent on the slope of the current-voltage (I-V) characteristic in the linear portion, consequently the diode functions essentially as a switch. In large-signal detection, the diode conducts over a portion of the input

cycle and the output current of the diode follows the peaks of the input signal waveform with a linear relationship between the output current and the input voltage.

In this section, an RF detector is built around a zero-bias Schottky diode (Hewlett-Packard HSMS-2850 series). Figure 4.29 shows a block diagram of a basic detector circuit. In this circuit, R_L represents the load resistance. C_b is the bypass capacitor that is used to separate the RF from the low frequency (LF) side of the circuit. This bypass capacitance should be chosen to be sufficiently large to provide a good RF short circuit to the diode such that all of the RF voltage appears across the diode terminals. However, its influence must be small at low frequencies, so that it does not load down the detector circuit. It can be seen later that the value of this capacitance determines the 3dB bandwidth of the detector circuit. When the detector is used as a peak detector circuit for SSCM measurements, the bypass capacitor should be chosen such that the bandwidth of the detector circuit is wide enough to recover the envelope of the amplitude modulation signal. The RF impedance matching network is vital for obtaining the best performance possible from a given circuit. It is used to transform the impedance of the diode to match the impedance of the source so that maximum power can be transfer to the load through the diode.

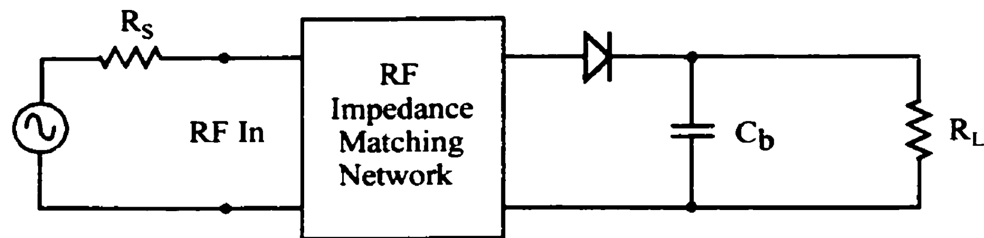


Figure 4.29 A basic block diagram of an RF detector circuit

In order to design a matching network, the equivalent circuit of the diode should be known. Since the diode used is a Schottky diode, it is expected that the equivalent circuit is similar to the one presented in Chapter 3. A Schottky diode can be represented by the linear equivalent circuit shown in Figure 4.30. In this figure, L_p is the package parasitic inductance, C_p

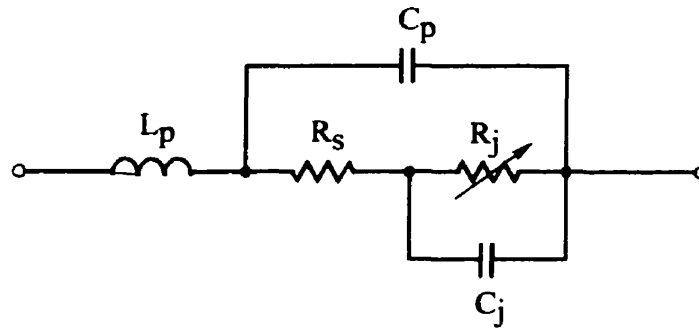


Figure 4.30 An equivalent circuit of a Schottky diode

is the package parasitic capacitance, R_S is the diode's parasitic series resistance, C_j is the junction parasitic capacitance, and R_j is the diode's junction resistance [89]. By combining Figure 4.29 and Figure 4.30, the basic detector circuit and its equivalent representations at both the RF and low frequency (LF) ports are shown in Figure 4.31. It should be noted that this equivalent circuit does not include the RF impedance matching network.

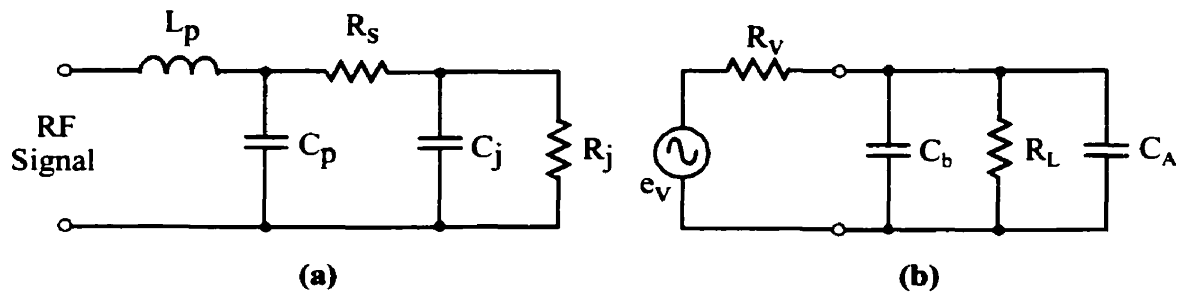


Figure 4.31 A complete RF detector circuit showing the equivalent circuit at the RF port (a) and the LF port (b)

4.4.1 Bandwidth of the Detector Circuit

In the equivalent detector circuit of Figure 4.31, R_V is the sum of R_j and R_S, R_L represents the load or the input resistance of an amplifier that follows the detector circuit. and

C_A represents the amplifier input capacitance as well as other capacitance components, such as stray capacitance, and particularly cable capacitances that may be connected to the detector circuit. These "R" and "C" elements will impose a limit on the upper 3 dB cut-off frequency of the detector circuit, which is given by:

$$f_c = \frac{1}{2\pi R_T\left(C_b + C_A\right)} \quad \textbf{(4.53)}$$

where R_T is the equivalent resistance in the circuit and can be computed from the expression:

$$R_T = \frac{R_v R_L}{R_v + R_L} \quad \textbf{(4.54)}$$

and $R_V = R_j + R_S$, in which R_j, the junction resistance, is given in **[89][90]**:

$$R_j = \frac{nkT}{q\,(I_s + I_b)} \quad \textbf{(4.55)}$$

where *n* is the ideality factor, k is the Boltzmann's constant, T is the absolute temperature, q is the electronic charge, I_S is the saturation current, and I_b is an external bias current. Using the diode (HSMS-2850) parameters given in the specification sheet, n = 1.06, I_S = 3 μA, and R_S = 25 Ω, the zero-bias resistance R_V was calculated at room temperature to be approximately 9 kΩ. This calculation assumes that the power level is low enough that the rectified current is small compared to the saturation current (large rectified current can lower the diode resistance). From equation 4.53, it can be seen that the effective bandwidth can be increased by reducing the elements of the time constant $R_T(C_b + C_A)$. However, these element values can only be reduced within certain limits. A severe reduction in the value of the RF bypass capacitance C_b will lead to poor RF/LF isolation and a decrease in signal level delivered to the diode. Alternately, either R_L or R_V can be reduced. The amount that R_L can be reduced is often limited if voltage amplification is desired since the output voltage of the detector is maximized by making R_L large. The load resistance R_L should be large compared to the resistance R_V to avoid the degradation in the detector circuit due to the diode-load

voltage divider action. R_V of the diode can be lowered by increasing the external bias current. However, increasing the bias current can reduce the detector voltage sensitivity [90]. For the SSCM measurements, the required bandwidth for the detector is just wide enough to recover the modulated signal at the modulation frequency (typically less than 100 kHz). This bandwidth can be obtained with a zero-bias diode if the capacitance C_b is properly selected. Furthermore, the detector's load resistance is normally much larger than resistance R_V. This load resistance is either the input impedance of the lock-in amplifier or may be the input impedance of the buffer amplifier that is placed between the detector and lock-in amplifier. Therefore, the total resistance R_T in this case is equal to the resistance R_V. The capacitance element C_A was estimated at approximately 25 pF. From equation 4.53, the bypass capacitance C_b was calculated for obtaining a bandwidth of 100 kHz is 152 pF. By choosing the bypass capacitance of 100 pF in the final design, the upper 3 dB cut-off frequency for our detector is 141 kHz. This bandwidth can be further increased if 50 pF is used for the bypass capacitance.

4.4.2 Detector Sensitivity or Voltage Sensitivity

Voltage sensitivity is the parameter that specifies the slope of the output detector voltage dropped across the load resistance versus the input RF signal power of the diode. It is bias, load resistance, signal level, and RF frequency dependent. In addition, the voltage sensitivity is also affected by losses due to the diode parasitics and the microwave impedance matching circuit. Given a knowledge of the parasitic parameters as shown in Figure 4.29 and the load resistance R_L, the voltage sensitivity of a Schottky diode can be calculated from the expression given in equation (4.56) [91][92] (this is assuming that there is a perfect, lossless impedance match at the diode's input):

$$\gamma = \frac{q}{2nkT} \frac{R_j}{\left(1+\frac{R_s}{R_j}\right)^2\left[1+\frac{\omega^2 C_j^2 R_s R_j^2}{R_s+R_j}\right]\left(1+\frac{R_j}{R_L}\right)} \tag{4.56}$$

where $\omega = 2\pi f$ and f is the RF frequency, γ is the voltage sensitivity and is normally expressed in millivolts/microwatt (mV/µW), all other parameters have been defined in previous sections. From equation 4.56, it can be seen that the load resistance R_L must be large compared with diode's junction resistance in order to prevent degradation in the voltage sensitivity. At room temperature, using the diode parameters given in the specification sheet: n = 1.06, R_S = 25 Ω, C_j = 0.18 pF, R_j = 9 kΩ, and taking load resistance R_L = 100 kΩ, the voltage sensitivity was calculated for the frequency of 1.85 GHz to be 75.5 mV/µW. In theory, this calculated value of voltage sensitivity can be achieved over a narrow band of frequencies through the use of a low loss impedance matching network at the input to the diode. However, this is unfortunately not the case at low frequency, where the reactance of the junction capacitance C_j is low, resulting in a very high value of impedance for the R_j - C_j parallel combination. The situation is even worse when the impedance matching network is realized in a low-Q medium such as a microstrip **[93]**.

A matching network using short-circuited stubs as shown in Figure 4.36 was built. It was fabricated from copper-clad, low loss dielectric material (ε_r = 2.5). The matching network was built such that the center frequency of the detector was 1.85 GHz (typical operating frequency of the sensor). Details of this matching network and design equations can be found in appendix C. Once the matching network's elements are known, the input match, expressed in terms of S-parameter S_{11}, as a function of frequency can be calculated using the expression:

$$S_{11}(f) = \frac{Z_g - Z_{in}(f)}{Z_g + Z\ \ (f)} \qquad \textbf{(4.57)}$$

where Z_g is the impedance of the source (assumed to be 50 Ω) and $Z_{in}(f)$ is the frequency-dependent input impedance of the detector including the matching network.

Figure 4.32 shows the magnitude of the input return loss (S_{11}) versus frequency using equation (4.57). The minimum input return loss occurred at the frequency of 1.85 GHz as expected. In these calculations, it is assumed that the input power level is low so that the

rectified current is negligibly small compared to saturation current. When the input power level is increased, the rectified current also increases, resulting in a change in the diode' parasitic parameters such as junction resistance and junction capacitance. In this case, the point at which the minimum return loss occurred is shifted.

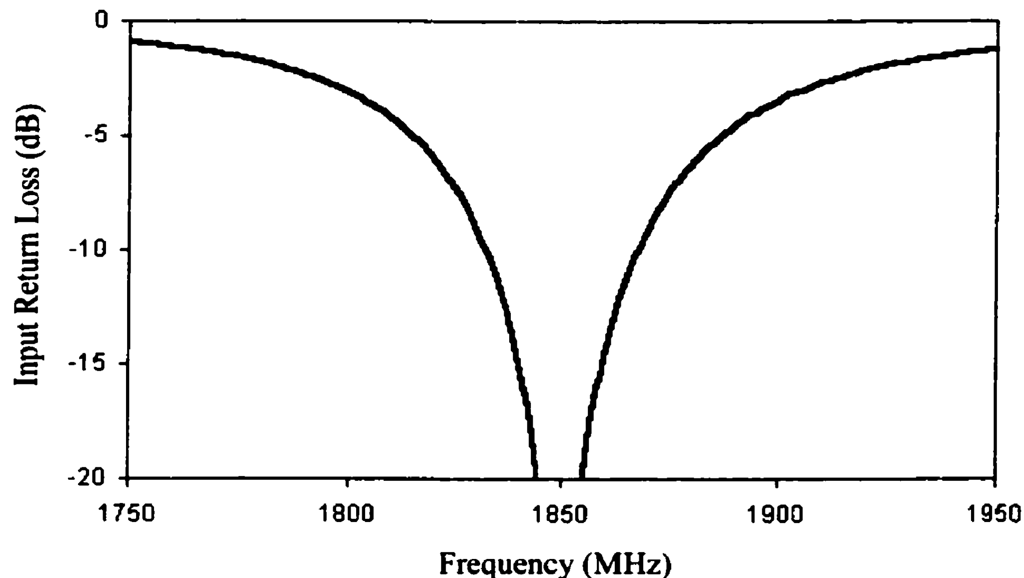


Figure 4.32 Theoretical simulation results show the magnitude of the input return loss of the RF detector as a function of frequency.

4.4.3 Detector Voltage Sensitivity Simulation

The analytical analysis of voltage sensitivity as a function of RF input power for a Schottky diode detector is complex. With the help of a simulation package, however, the DC output voltage of the detector versus RF input power can be easily determined by using the Harmonic Balance simulator (Libra non-linear simulator). In this simulation, the SPICE[14] model parameters of the Schottky diode obtained from the manufacturer were used to model

14. SPICE is an acronym that stands for Simulated Program with Integrated Circuit Emphasis. SPICE parameters are the electrical parameters of a device that is used by the simulated program.

the diode. The simulation circuit also includes the matching network presented in the previous section. The simulation was performed for a drive frequency of 1.85 GHz, at temperature T = 300 ^{o}K. The RF input power was used as a variable, and the desired DC output voltage appearing across a load was calculated while the input power was swept from - 45 dBm to - 20 dBm. Figure 4.33 plots the simulation results and characteristic transfer curves for various values of load resistance. The transfer curves follow the square law at low levels of input power (below -30 dBm, output voltage is proportional to the square of input voltage) and displays a quasi-linear behavior (output voltage proportional to input voltage) at higher levels. It is also observed that the detector sensitivity is proportional to the load resistance. The smaller the load resistance is, the smaller the voltage that can be output from the detector. The degradation factor in sensitivity is $R_L / (R_L + R_j)$, where R_L is the load resistance, and R_j is the junction resistance of the diode. However, for load resistance greater than 100 kΩ, the sensitivity is affected little by load resistance because the degradation factor approaches unity.

The RF detector voltage sensitivity, generally expressed in terms of (mV/μW), is the slope of the transfer curve. Figure 4.34 plots detector voltage sensitivity as a function of input power for various values of load resistance. It can be seen that voltage sensitivity is constant at low detection levels (below -35 dBm) and decreases if the input power is increased. The decreasing sensitivity can be explained by investigating the dependence of the junction resistance on input power. From equation 4.55, one can see that the junction resistance is inversely proportional to the saturation current for a zero bias detector. Within the circuit, there will also be another current component, the circulating current, $I_C = V_O / R_L$, produced by the rectification in the diode. Under small signal operation I_C is much less than the saturation current, and can therefore be ignored. However, as the input power levels are increased, I_C will increase and cause a corresponding decrease in junction resistance and hence decrease the sensitivity of the detector. Additionally, the change in the diode's impedance as the input power increases will also produce a mismatch with respect to the matching structure. This undesirable mismatch results in a reflection of some of the RF power, leaving only a portion of the available RF power for delivery to the load.

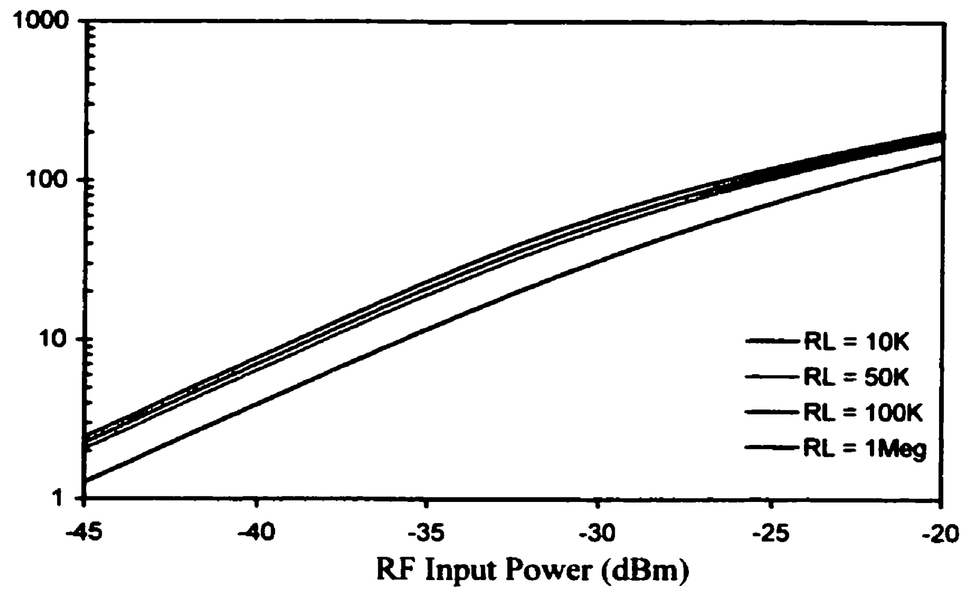


Figure 4.33 Characteristic transfer curves of detector output voltage versus input power for various values of load resistance.

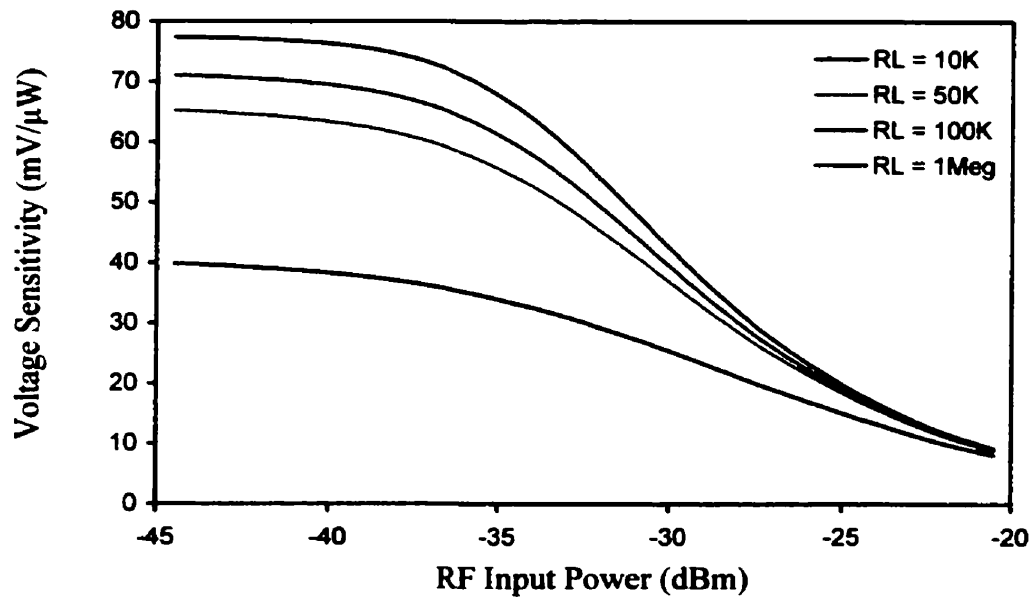


Figure 4.34 Voltage sensitivity of the RF detector versus input power for various values of load resistance.

4.4.4 Experimental Results

Figure 4.35 shows the measured input return loss of our detector (magnitude of S_{11}) as a function of frequency. The matching network was realized as a microstrip circuit as shown in Figure 4.36. The matching network's elements were chosen so that the load section of the transmission line had a length of 21.38 mm and width of 1.27 mm, and two short-circuited stubs of length 7.41 mm and width 4.47 mm (refer to appendix C for details). A network analyzer was used to measure the input return loss of the detector. The measurements were performed with an RF input power to the detector of -30 dBm. From figure 4.35, it can be seen that the frequency point at which minimum return loss occurred is 1.86 GHz. If the input power level is increased, this frequency point will be shifted further up. The reason is due to a change in detector input impedance as the input power level increases. Comparing with simulation results, the measured matching level of the detector agrees with simulation fairly well; however, the frequency where maximum match occurred is different by about 10 MHz.

To measure the response of our zero-bias detector, a high frequency signal generator (Rohde & Schwarz SMT 03) and a DC volt meter were used. The signal generator was used to generate the detector's input signal while the DC volt meter was used to measure the voltage generated by the detector. In this measurement, the frequency that drives the detector was selected (1.855 GHz) after adjusting for maximum output voltage at a low power level (-45 dBm). This frequency was fixed for the entire measurement. By changing the detector's input power from -45 dBm to -20 dBm and recording the detector's output voltage, a transfer characteristic curve of the detector could be constructed as shown in Figure 4.37.

The measured voltage sensitivity (slope of the characteristic transfer curve) was calculated and plotted in Figure 4.38. From these curves, it can be seen that the detector sensitivity decreases from its maximum value when the input power is higher than -30 dBm. The maximum measured voltage sensitivity that could be obtained from the detector is 42 mV/ µW at an input power below -35 dBm. Although the measured sensitivity is quite low compared with simulation results, it agrees well with the sensitivity quoted by Hewlett-Packard for the zero-bias Schottky diode HSMS-2850 series (30 mV/µW) measured at 2.45 GHz and input power = -40 dBm [89].

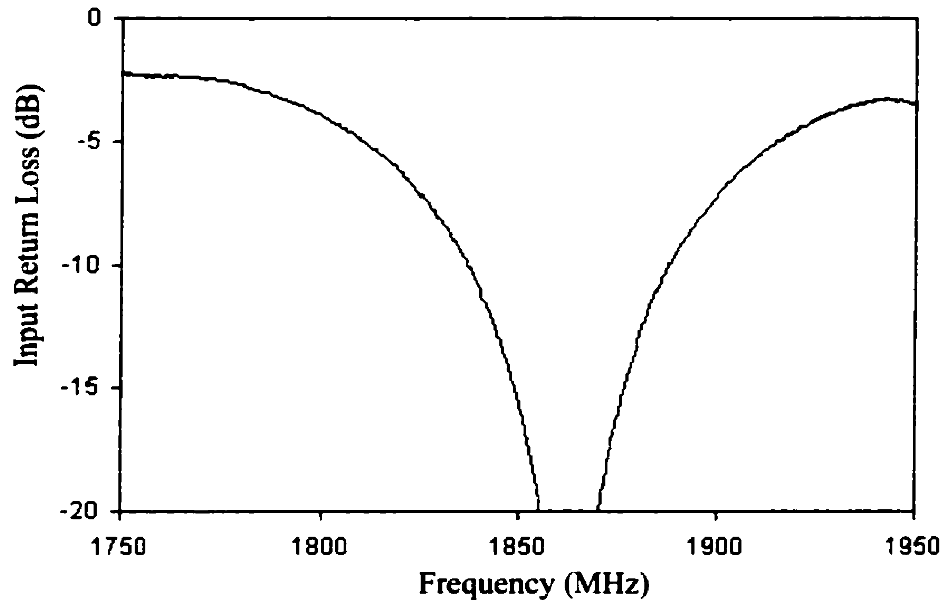


Figure 4.35 Experimental results showing the input return loss of the detector as a function of frequency. Measurements were performed at an input power level of -30 dBm.

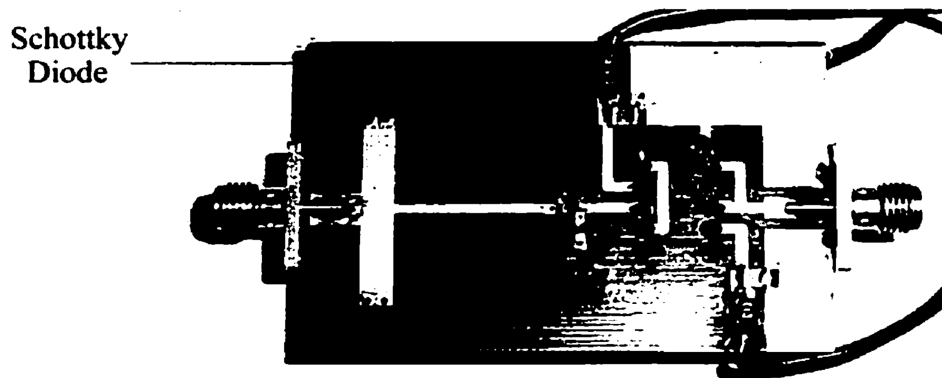


Figure 4.36 A photograph of 1.85 GHz RF detector using a zero-bias Schottky diode.

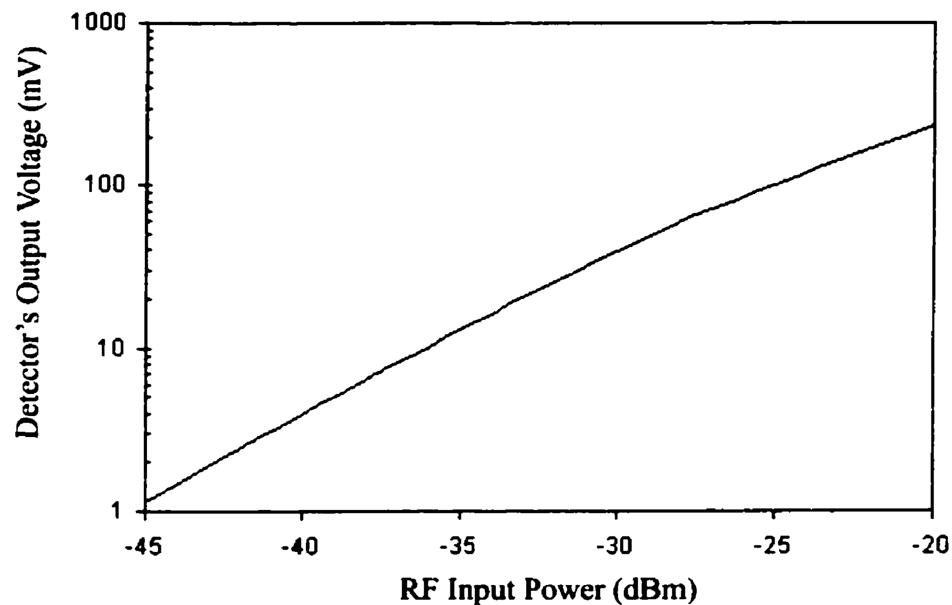


Figure 4.37 Experimental results showing the characteristic transfer curve (output voltage versus input power) of the zero-bias detector. Measurements were performed at a frequency of 1.855 GHz.

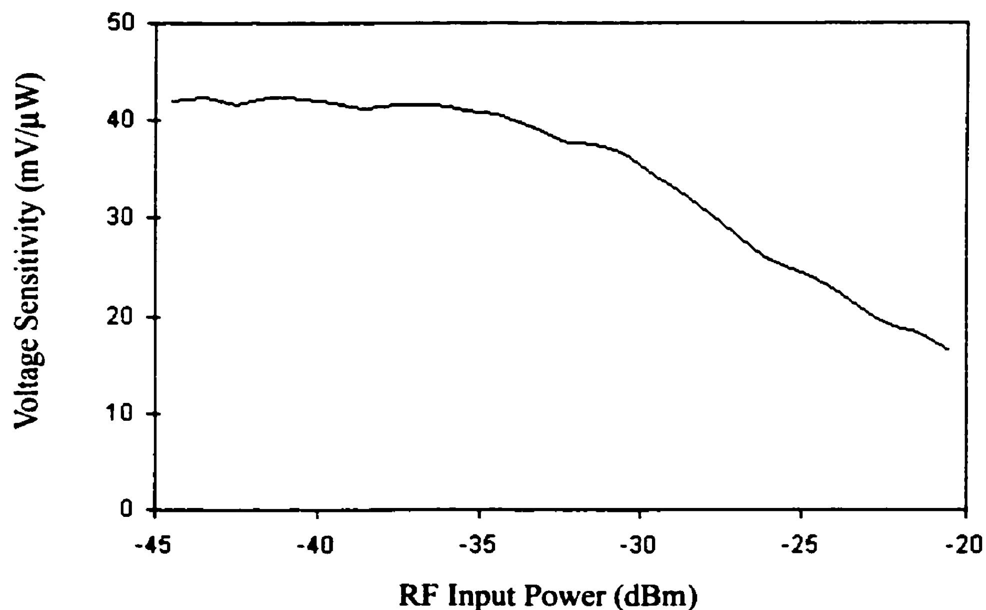


Figure 4.38 Measurement of voltage sensitivity of the zero-bias RF detector versus input power. Measurements were performed at a frequency of 1.855 GHz

Because this is a narrow band detector, it is expected that the voltage sensitivity should vary with operating frequency. If the drive frequency departs from the midband frequency (1.85 GHz), the voltage sensitivity is expected to decrease due to impedance mismatch. Figure 4.39 plots the detector's output voltage at an input power of -30 dBm (1 μW) as the drive frequency is swept from 1.75 GHz to 1.95 GHz. In this frequency range, we can see that the minimum voltage sensitivity is about 15 mV/ μW and the maximum sensitivity is about 40 mV/μW. For the SSCM measurements, a typical input power to the detector is less than - 25 dBm and the operating frequency is between 1.8 GHz and 1.9 GHz. Therefore, the detector sensitivity should lie in the range of 15 to 25 mV/μW. Because the detector sensitivity decreases with increasing input power and the HSMS-2850 has low breakdown voltage, it is recommended that the detector should not be used with input powers higher than -20 dBm [89].

The variation in the detector's sensitivity suggested that a wide bandwidth detector should be used. However, matching the impedance of a Schottky diode over a wide bandwidth is difficult. The simplest way to increase the detector's bandwidth, at the expense of detection sensitivity, is to add a shunt resistor of a 100 - 200 Ω across a diode. Adding this resistor will reduce sensitivity because the input RF current is split between the diode and the shunt. For very broadband detectors, a shunt resistor of few tens of ohms yields a good input impedance match. An commercial broadband detector (73N50) was used in this project.

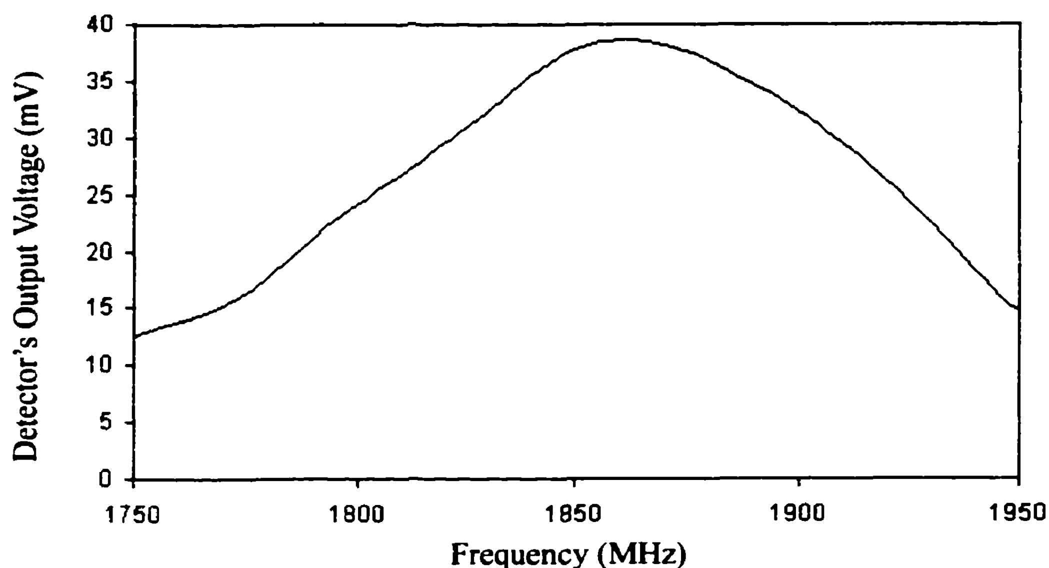


Figure 4.39 Measurement of detector output voltage versus drive frequency. Measurements were performed with an input power of -30 dBm.

4.5 Measurements of Sensor Sensitivity

The sensitivity of the capacitance sensor depends on the slope of the tuning curve (dv/df) and frequency sensitivity (df/dC). However, the minimum detectable capacitance is not only determined by sensor sensitivity, but also depends on the noise level at the sensor output. In this section, the sensor sensitivity was experimentally measured and the minimum detectable capacitance was calculated based on the experimental data. Both RF detectors, the commercial broadband 73N50 and our Schottky diode detector, were used in these experiments. The experimental set-up for sensitivity measurements is illustrated in Figure 4.40 and Figure 4.41 for the commercial broadband and Schottky detector respectively. An oscillator was used to generate the RF signal, and the signal was applied to the resonator via an attenuator. The purpose of the attenuator was to reduce the reflection signal from the resonator since it could cause the oscillator to become unstable. For SSCM measurements, the attenuator also served to limit the RF voltage between the tip and sample to prevent the aliasing effects. These effects will be discussed in next chapter.

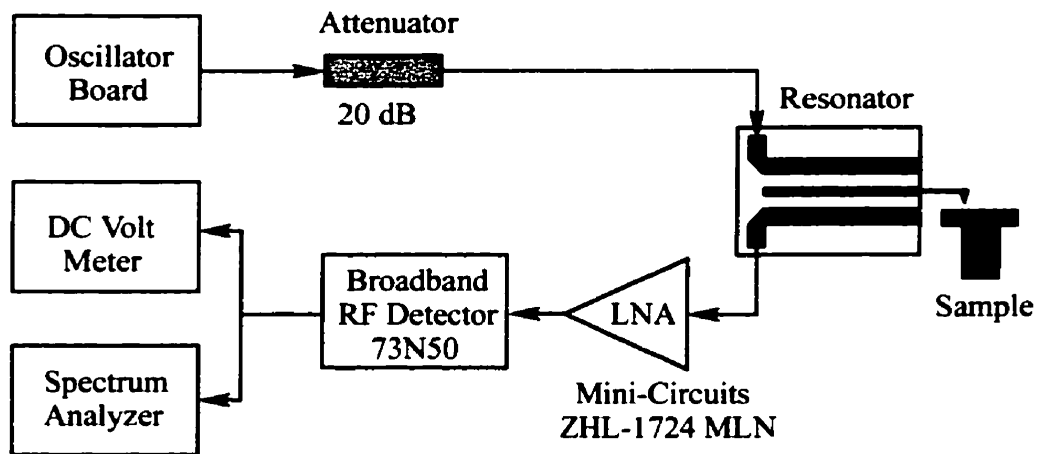


Figure 4.40 Experimental set-up for measurement of the sensor sensitivity. The RF detector used is a commercial broadband 73N50.

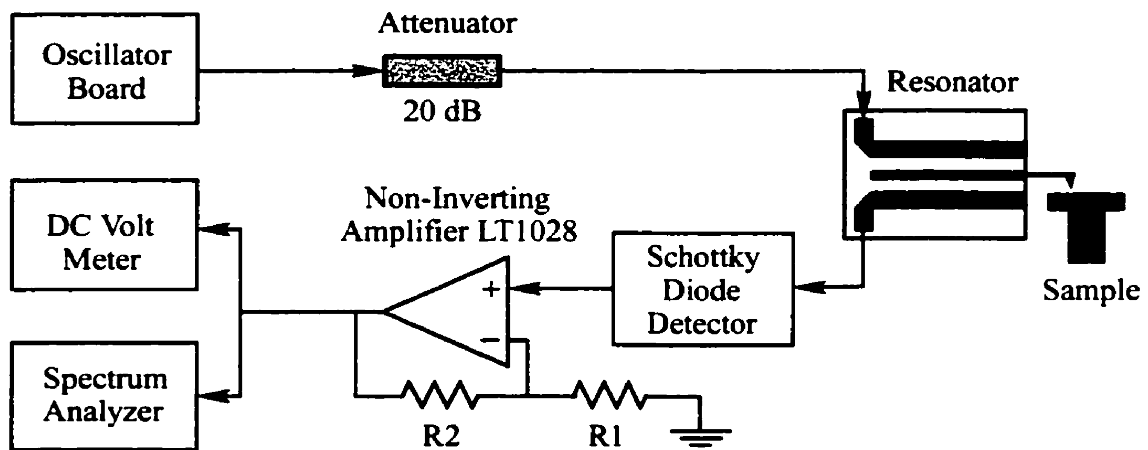


Figure 4.41 Experimental set-up for measurement of sensor sensitivity. The RF detector used is a zero bias Schottky diode detector.

In both measurements, a silicon cantilever (NT-MDT SCS12 series) was attached to the resonator and placed above a sample surface (a few μm) such that it could represent a scanning operating condition as much as possible. In Figure 4.40, a commercial Low-Noise-Amplifier (LNA) (ZHL-1724 MLN) with a gain of 28 dB was used to amplify the RF signal before it was applied to the detector. The purpose of this LNA was to improve the signal to noise ratio of the sensor. Similarly, a low noise non-inverting amplifier with a gain of 100 was used with the zero-bias Schottky detector as shown in Figure 4.41 (the gain was adjustable). A DC volt meter and a spectrum analyzer were connected at the detector output port so that the voltage and noise generated by the sensor could be measured simultaneously.

It should be noted that the sensor's voltage sensitivity (dv/df) depended upon where the oscillator frequency fell on the resonant curve (i.e. slope of the resonant curve). For both measurements, the operating point was chosen to be 3 dB down from the resonant peak. The reason for choosing this operating point was that it can be easily located with a network analyzer, even though operating the sensor at the 3 dB point did not give the maximum voltage sensitivity. The voltage sensitivity (dv/df) was measured by changing the oscillator frequency around the 3 dB point and then measuring the change in detector output voltage. Once the measured voltage sensitivity and noise is determined, the lower limit of capacitance in terms of $F/\sqrt{Hz}$ may be calculated from expression:

$$\delta C = \frac{V_{noise}}{(df/dC)(dv/df)} \quad \textbf{(4.58)}$$

where df/dC is the frequency sensitivity of the resonator from simulation results. Table 4.3 shows experimental results and calculated sensitivities for the two detectors described above. The sensitivity calculations were performed using df/dC = 1.5 MHz/fF. This was the simulated value of frequency sensitivity for a 110 Ω resonator at 1.85 GHz (see figure 4.16).

Table 4.3 Measurements of capacitance sensor sensitivity

Commercial Detector 73N50				**Schottky Diode Detector**		
Oscillator Frequency (GHz)	**Minimum Noise**[a] ($nV/\sqrt{Hz}$)	**Measured dv/df (mV/MHz)**	**Calculated Sensitivity** ($F/\sqrt{Hz}$)	**Minimum Noise** ($\mu V/\sqrt{Hz}$)	**Measured dv/df (mV/MHz)**	**Calculated Sensitivity** ($F/\sqrt{Hz}$)
1.872	29			2.15		
1.873	29	10.7	$1.81\text{x}10^{-21}$	2.10	520	$2.69\text{x}10^{-21}$
1.874[b]	28	10.5	$1.78\text{x}10^{-21}$	2.10	510	$2.74\text{x}10^{-21}$
1.875	28	10.0	$1.87\text{x}10^{-21}$	2.10	490	$2.86\text{x}10^{-21}$
1.876	28	9.7	$1.92\text{x}10^{-21}$	2.05	480	$2.85\text{x}10^{-21}$

a. Minimum level of noise in noise spectrum
b. Frequency at 3 dB down from the resonant peak

For the 73N50 detector, minimum noise at the detector output was 28 $nV/\sqrt{Hz}$ measured in 1 Hz bandwidth at 90 kHz (minimum level of noise in noise spectrum, see Figure 4.42). The voltage sensitivity dv/df was 10.5 mV/MHz. Therefore, the minimum detectable capacitance was determined to be $1.78\text{x}10^{-21}$ $F/\sqrt{Hz}$. Similar measurements were done for the zero bias Schottky detector. In this case, the minimum noise measured at the detector output was 2.1 $\mu V/\sqrt{Hz}$, and the voltage sensitivity was 520 mV/MHz. From these values, a minimum detectable capacitance was determined to be $2.74\text{x}10^{-21}$ $F/\sqrt{Hz}$. Typical noise spectra measured at the detector output for the wideband detector 73N50 and Schottky diode detector are shown in Figure 4.42 and Figure 4.43 respectively.

Experimental results have shown that the minimum detectable capacitance depends on the power level delivered to the detector for a particular experiment set-up shown in Figure 4.40. In one experiment, we replaced the attenuator shown in Figure 4.40 with a 10 dB attenuator and measured voltage sensitivity and noise at the detector output as previously described. It has been observed that the measured voltage sensitivity dv/df was increased to 30.2 mV/MHz and minimum noise level at the detector output was 58 $nV/\sqrt{Hz}$. As a result,

the minimum detectable capacitance decreased to 1.28x10^{-21} $F/\sqrt{Hz}$. From this experiment, the overall sensitivity is increased by a factor of 1.4. However, the RF voltage between the tip and the sample is expected to be increased by a factor of 3. Estimations of tip voltage for these operating conditions will be presented in next section.

As shown in section 4.1.1.1 the voltage sensitivity dv/df depends on the -3 dB bandwidth of the resonant curve (-3 dB bandwidth varies with the experimental setup). This depends on the degree of resonant curve degradation when a tip is brought close to the sample surface. In addition, the calculated sensitivity presented in this section does not include any tip resistance or tip-to-sample contact parameters that may affect the sensitivity in practice. Under normal operating conditions, a minimum detectable capacitance of 2x10^{-21} $F/\sqrt{Hz}$ may be representative of the sensitivity of our sensor.

In order to test the capability of detecting such a small capacitance, the sensor was used to measure the depletion capacitance of a test sample. The sample used for measurements was a 400 nm PMOS transistor. Details of this device can be found in the next chapter. Figure 4.44 shows the capacitance derivative $\partial C/\partial V$ images of the test device. Figure 4.44a is a capacitance image that was taken by using a combination of LNA and detector 73N50 as a peak-detector while Figure 4.44b is a capacitance image obtained by using a zero-bias Schottky diode as a peak-detector. In these images, the capacitance derivative dC/dV is represented by gray scale shading. Dark (black) signifies regions of negative dC/dV and represents a P-type region. White signifies regions of positive dC/dV and represents an N-type region. As indicated in Figure 4.44a, all regions such as gate, source/drain, oxide, and substrate are clearly identified.

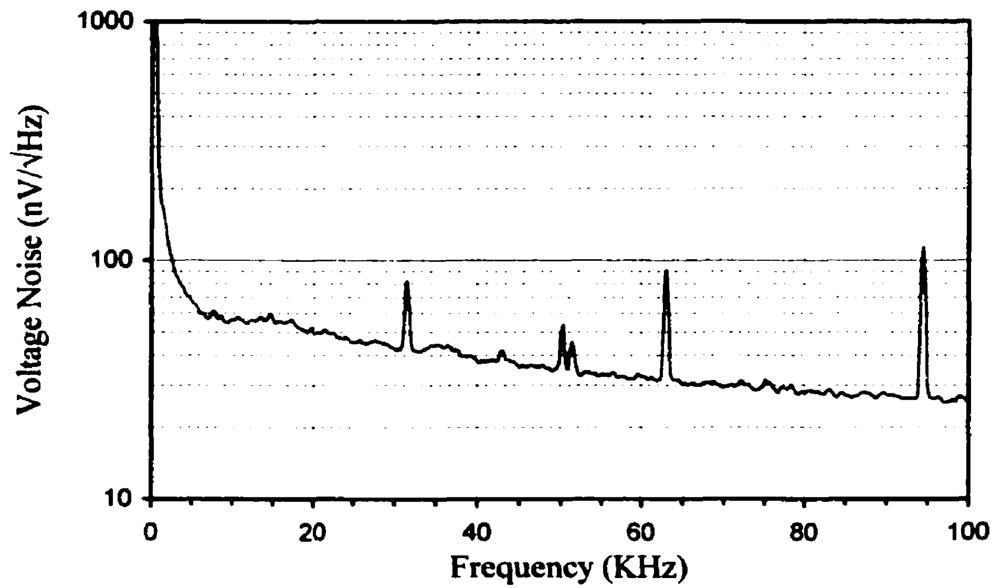


Figure 4.42 Noise spectrum at the sensor output using the wideband detector 73N50

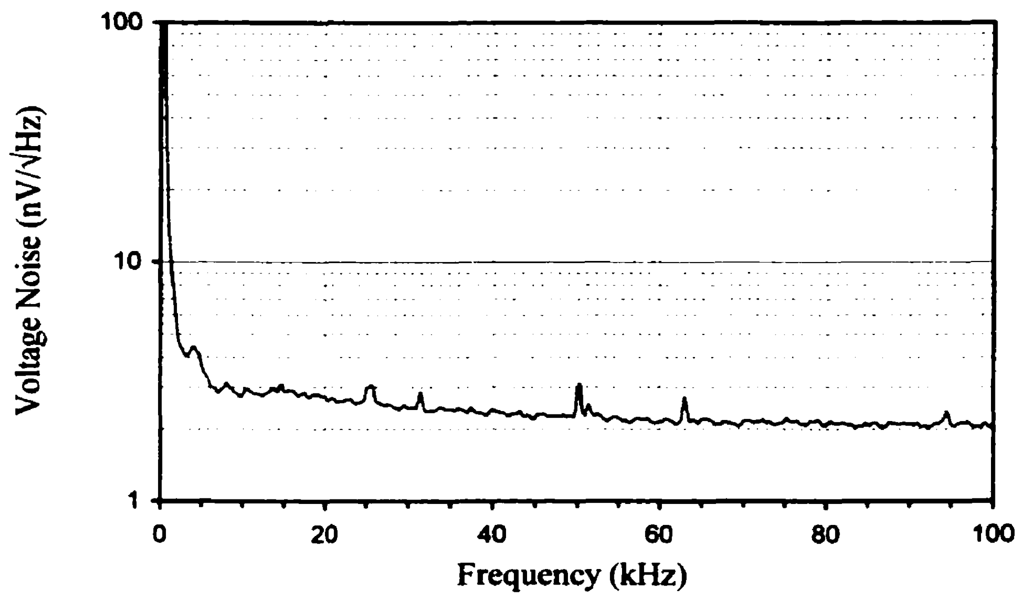


Figure 4.43 Noise spectrum at the sensor output using the zero bias Schottky detector

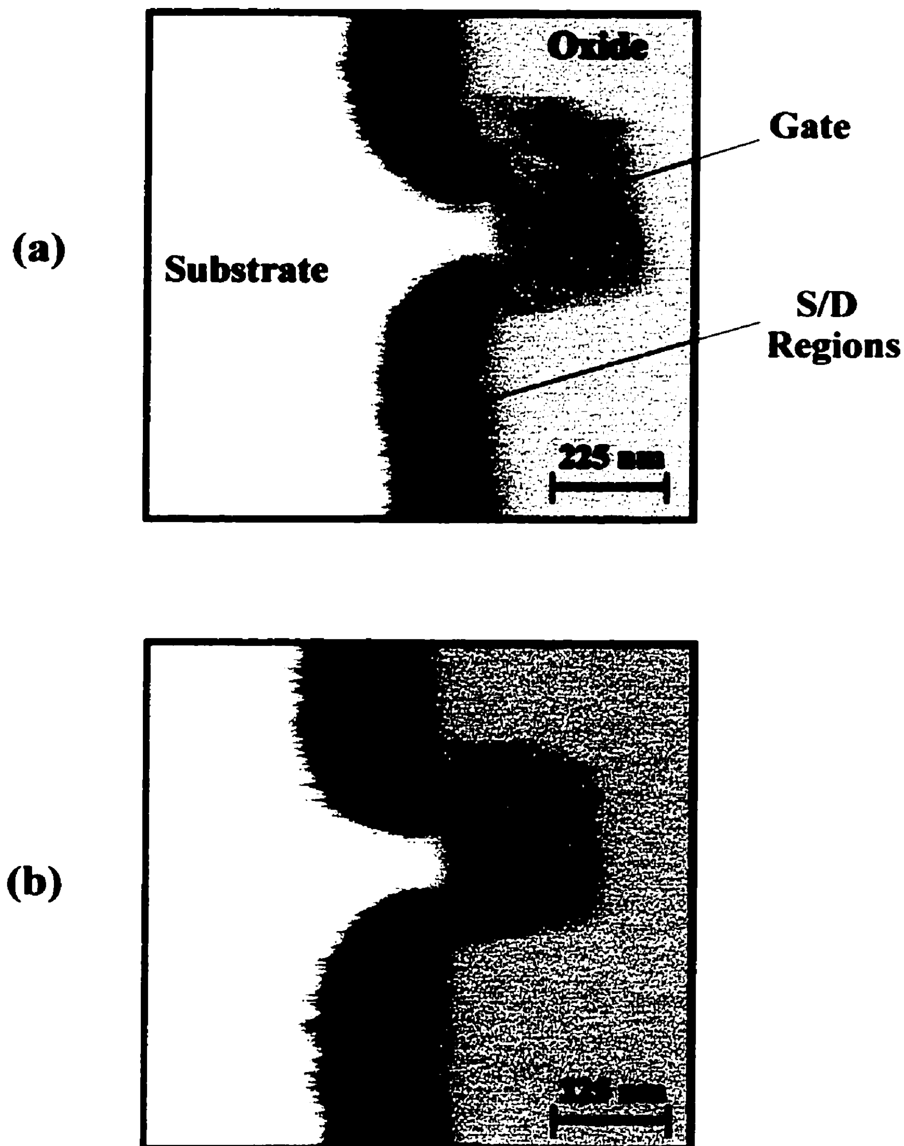


Figure 4.44 Capacitance derivative *dC/dV* images of a 400 nm PMOS transistor.
(a) Image was obtained by using a combination of commercial LNA and detector 73N50 as a peak-detector.
(b) Image was obtained by using a zero bias Schottky diode as a peak-detector.

4.6 Estimating the RF Voltage on the Tip for Operating Conditions

In the past, the RF voltage between the tip and the sample under operating conditions was determined experimentally. However, we did not successfully measure this voltage due to problems mentioned in section 4.3.6. Thus, the RF voltage on the tip can only be estimated based upon theoretical calculations. During the course of the experiment presented in the previous section, the oscillator voltage waveform was measured by using a digital oscilloscope (Tektronix). Without the attenuator and resonator, the oscillator voltage measured by the scope was 1.1 V peak-peak at 1.875 GHz. At the same time, the loss of the resonator at this frequency was measured using a network analyzer to be 18 dB. From Figure 4.40, the total attenuation due to the combination of attenuator and the resonator was 38 dB. Referring back to section 4.3.4, theoretical calculations show that the tip voltage is about 30V peak-peak if a 1V peak-peak voltage is applied to the resonator input under ideal conditions (ideal conditions assume no loss in the resonator and the operating frequency set at resonance). By including the attenuation factor in the analysis, the RF tip voltage in the previous experiment may be estimated as $V_{Tip} = 1.1\,(30)\,10^{-38/20} = 415$ mV peak-peak (this assumes that the source voltage does not change when the resonator is inserted in the circuit). It should be also noted that the analysis does not include the voltage drop across tip resistance if it is present in the circuit model.

CHAPTER 5

EXPERIMENTAL RESULTS

In this Chapter, SSCM results from imaging several semiconductor devices in cross-section are presented. These devices are include a 400 nm gate length MOSFET, a Bipolar-Junction-Transistor (BJT), a 180 nm gate length MOSFET, and MOSFETs from a 486 DX microprocessor chip. Aliasing effects resulting from a large amplitude of RF voltage on the tip will be demonstrated by imaging a sample with different RF voltage levels.

Figure 5.1 shows a complete experimental set-up that has been used for SSCM measurements in our laboratory. The sample to be imaged is mounted in a cross-sectional orientation on a piezo-tube scanner and scanned beneath a tip. A photo detector is used to monitor the deflection of the cantilever and provide a feedback signal to the digital controller for mapping the topographical information of the sample surface. This task is done within the controller by comparing the photo detector's output voltage to a set point. If a discrepancy is found between these voltages, the controller sends an appropriate voltage to the piezo tube to adjust the height of the sample in an attempt to compensate for the deflection of the SSCM cantilever. Typically, a set point of 25 nN - 50 nN was selected for most of images presented in this thesis. Topographic resolution of less than 1 nm can be achieved using the current cantilever and beam system. Besides the topographic image, a capacitance image can also be obtained from the capacitance sensor. In normal operation, a function generator is used to supply an AC modulation signal to the sample when the tip is grounded. It should be noted that the tip is grounded at the modulation frequency but it is open circuit at the RF frequency. The AC modulation signal is typically in the range of 100 - 500 mV peak-to-peak at 90 kHz. This frequency is chosen as it corresponds to a minimum value in the noise spectrum of the peak detector circuit (see figure 4.42). Application of AC modulation across the Schottky barrier

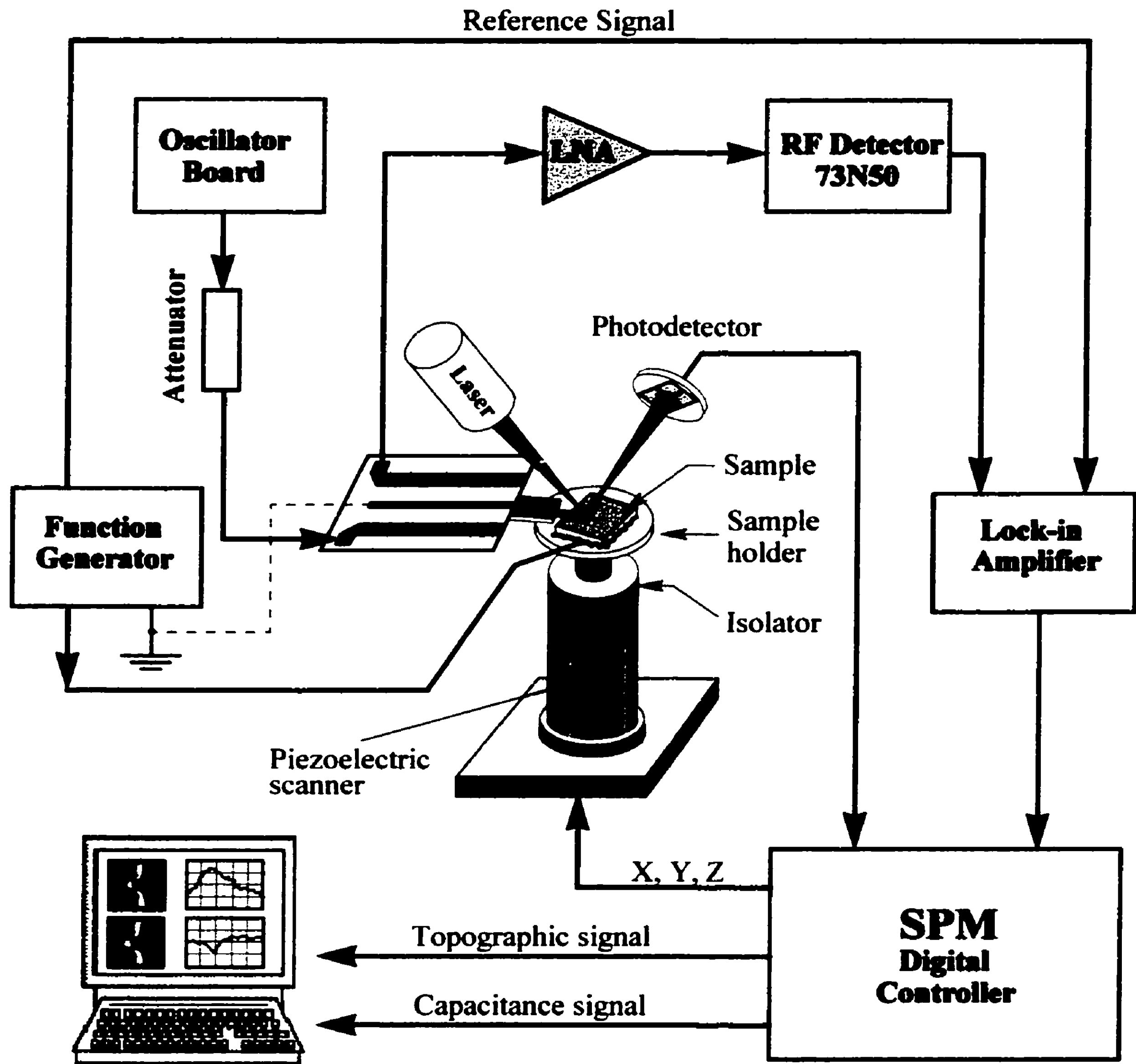


Figure 5.1 A complete experimental set-up for SSCM measurements

gives rise to a modulation of the tip-to-sample contact capacitance. Variation in contact capacitance will in turn shift the resonant frequency of the resonator, resulting in a modulation of the amplitude of the oscillator signal. The envelope of this amplitude modulated signal is then detected by the RF detector (73N50) and measured by a Lock-in amplifier (SR510). The Lock-in amplifier output signal is then input to the digital controller for processing and recorded in a PC computer. For our controller system, both topographic and capacitance signals can be simultaneously recorded and displayed on a computer screen. In the capacitance sensing circuit, an attenuator inserted between the oscillator and the resonator is used to limit the RF voltage on the tip. This attenuator is also serves to reduce the reflected signal from the resonator due to impedance mismatch between the oscillator and resonator. A combination of LNA and RF detector 73N50 is used as a peak detector because it has better performance and supports a wider frequency range than the designed Schottky detector.

Before the SSCM measurements are performed, the operating frequency of the sensor should be determined. Normally, this operating frequency is chosen at a point of 3 dB down from the peak of the resonant curve. The operating point is located by measuring the S-parameter S21 of the resonator with a network. The operating point should be determined while the tip is placed close to the sample surface.

5.1 Imaging Round-Robin MOSFETs (400 nm)

In this section, the SSCM results from imaging of P-channel MOSFET cross-sections are presented. These devices were fabricated at Texas Instruments and were provided by Semiconductor Manufacturing Technology (SEMATECH) as a part of a round-robin project aimed at evaluating profiling techniques. The results from different groups were compiled by SEMATECH, and a comparison of the data has been published. A sketch of these devices is shown in Figure 5.2. These devices have nominal gate length of 400 nm and were fabricated in cascade with a pitch of 1400 nm. From the SSCM results, the dimensions of the device such as gate length, channel length, source/drain junction depth the distance between gates were measured. Also dopant concentrations at several different locations around the

device were profiled.

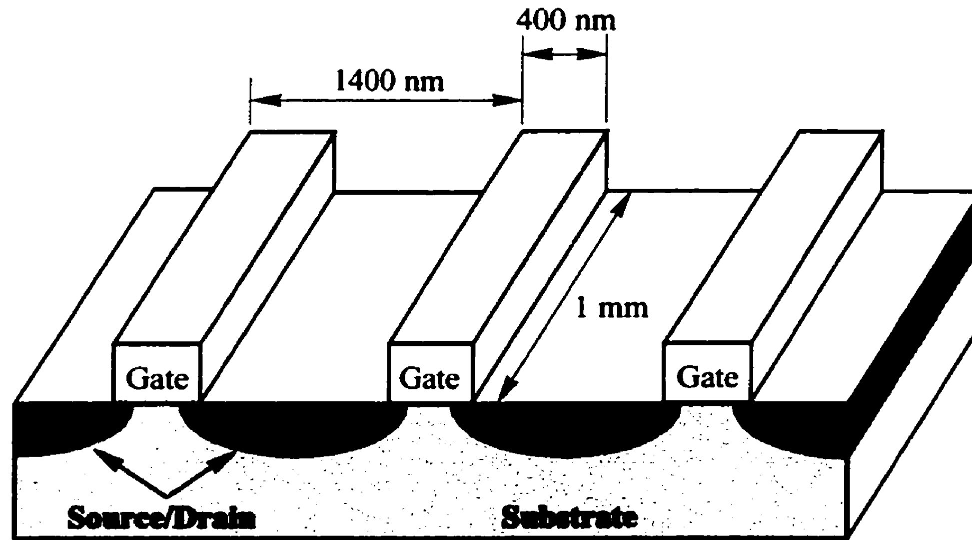
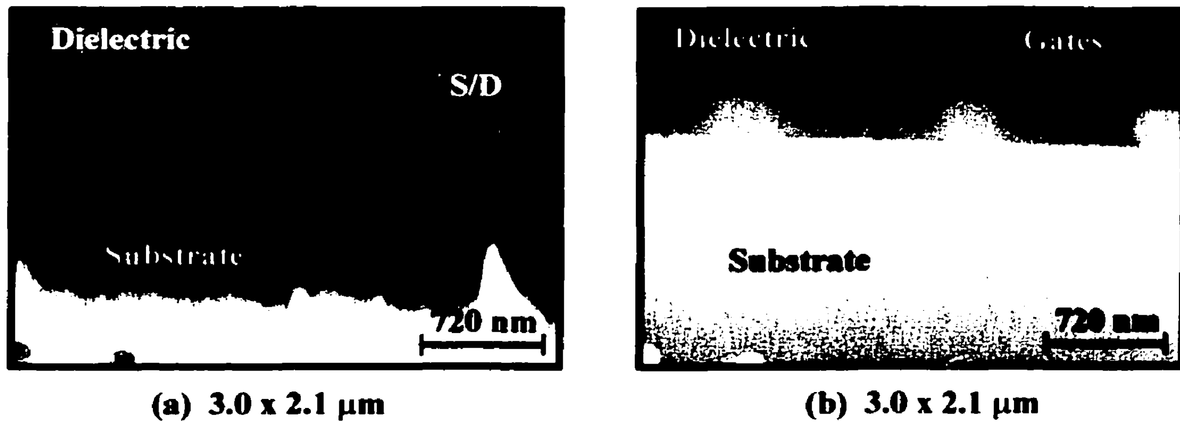


Figure 5.2 Sketch of the MOSFET sample. The nominal gate length is approximately 400 nm and the gate-to-gate pitch is 1400 nm.

From an instrumentation point of view, there is no fundamental difference between the top-surface and cross-sectional dopant profiles. The only difference comes in the sample preparation. For cross-section imaging, the sample was polished and mounted in cross-section. The sample preparation was described in section 2.6. After polishing, the surfaces of the sample were cleaned with hydrogen fluoride (HF) to remove any remaining contamination prior imaging. The polishing process takes several hours. Under normal conditions, however, the instrument can obtain a fresh image roughly every 5 minutes. Thus, a useful image can normally be obtained within an hour of the last HF cleaning step. The results obtained from imaging polished device cross-sections have been found to be repeatable and consistent within a day or two of the polishing step. However, this is not the case for a sample that is left in the air for a longer period of time (several days). Due to the buildup of oxide and deposition of contamination on the sample surface, a significant reduction in sensitivity and contrast has been observed in images obtained from such samples.



(a) 3.0 x 2.1 μm **(b) 3.0 x 2.1 μm**

Figure 5.3 Scanning Schottky capacitance profile of three p-channel MOSFETs
(a) Capacitance image
(b) Topographic image

Figure 5.3 shows both topographic and capacitance images of the MOSFETs in this round robin sample. The image size is 3000 x 2100 nm. The capacitance data were acquired at 0 V DC bias and using a sinusoidal modulation signal of 0.4 V_{p-p} at 90 kHz on the tip. The time constant of the lock-in amplifier was set at 10 mS and the set point of the controller used to maintain a constant contact force was 35 nN. Also, the image was obtained with a scan rate of 1 Hz (1 line-scan/s) with a fast scan axis along the direction that extended vertically across the source/drain regions. In addition, the capacitance image was obtained with the attenuator between the oscillator and the resonator set to -6 dB. With this attenuation and the loss from the resonator, the RF voltage between the tip and the sample was estimated to be more than 2.5 V_{p-p}. It can be seen from the images in Figure 5.3 that the gates are not equal in size. The center gate is a little smaller and rounded compared with the outer gates. This is attributable to polishing. The white and black circular dots presented in the topographic image and the capacitance image respectively are from surface contamination. From these images, we are able to measure the pitch of the devices in order to verify the calibration of the x/y dimensions of the SSCM piezo electric scanner. This can be done by taking a line profile (A - A') across the gate at half height from both topographic and capacitance images (see Figure 5.3a). These two profiles are plotted on the same axis, as shown in Figure 5.4. From these graphs, it can be seen that topographical line profile (red curve) gradually increases at displacements of 80 nm

and reaches the gate's top surface at 200 nm for the first gate. Similar results can be observed for the second gate. The observed slope at the gate edge may be attributed to 2 factors: first, this may be a result of the polishing that rounded the gate; second it could be because the side wall of the tip makes contact with the gate top edge before the vertex of the tip has actually reached the gate edge. It has been suggested that the location of the gate edge may be determined from topographical profiles by drawing 2 straight lines parallel to the topographical profile at the gate edge. The intersection of these lines is the location of the gate edge [94]. By doing this, the distance between two adjacent gates was measured to be 1300 nm (see Figure 5.4). This value is quite low compared to the specified value of 1400 nm. It should be noted that the pitch is measured based on the image size of 3000 x 2100 nm. From Figure 5.3, however, the full length of the images along the x-axis (horizontal axis) is estimated to be 3250 nm instead of 3000 nm, about an 8% discrepancy between the actual size and the size that was set for piezo scanner. The difference between these dimensions fairly well agrees with the measurement of the diffraction grating sample presented in Appendix A. If this discrepancy is taken into account, the measured pitch approximates the expected value.

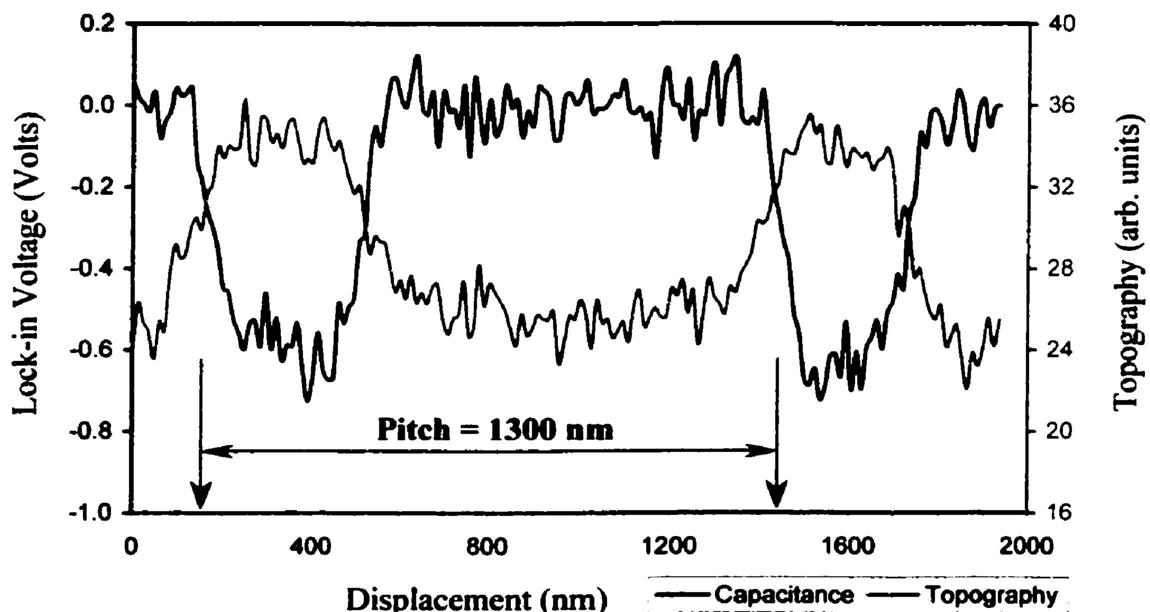


Figure 5.4 Capacitance derivative *dC/dV* and topographic line cross-section profiles taken across the gate at the half height from the images shown in Figure 5.3

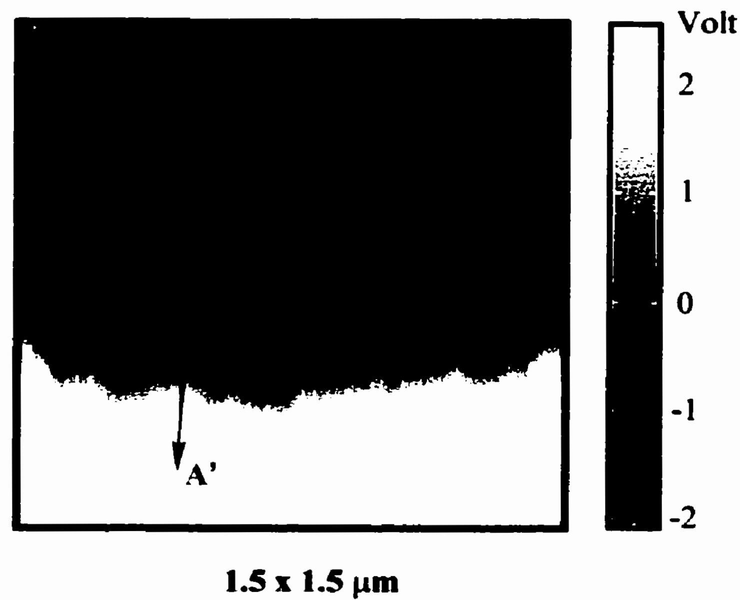


Figure 5.5 Scanning Schottky capacitance profile of a round robin 400 nm MOSFET

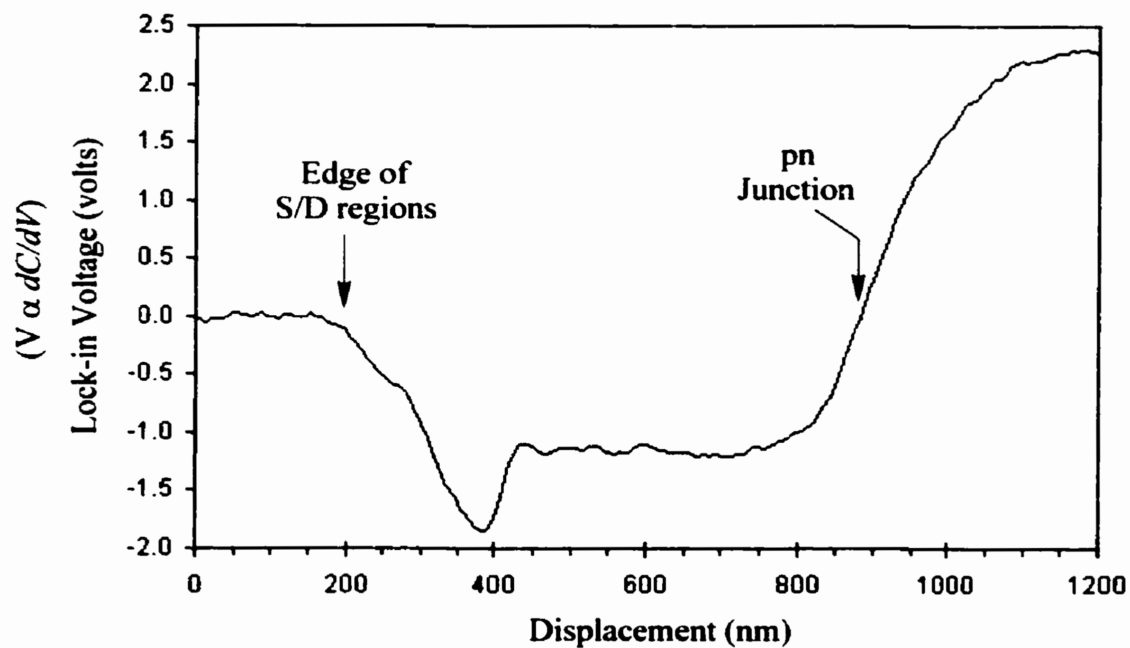


Figure 5.6 Line profiles taken across source/drain regions as shown in Figigure 5.5 above at the location that is marked (A-A').

Figures 5.5 and 5.6 show a capacitance derivative profile and line profile taken across a source/drain (S/D) region of another 400 nm MOSFET device respectively. From the line profile in Figure 5.6, 3 regions are observed:

1) A region of $dC/dV \sim 0$ V: this region ranges from 0 - 200 nm on the displacement axis. This region represents the insulating layer above the S/D regions. Since there are no carriers to deplete in the insulating layer, there is no capacitance change to be detected, resulting in $dC/dV = 0$.

2) A region of negative dC/dV: this region ranges from 200 nm - 880 nm on the displacement axis. It is divided into 3 sub-regions: the first ranges from 200 - 385 nm where the magnitude of dC/dV increases, the second ranges from 385 - 450 nm and where magnitude of dC/dV decreases, the last ranges from 450 - 880 nm. In the latter region, the magnitude of dC/dV is constant up to 810 nm and then decreases to zero at 880 nm on the displacement axis. The region that is covered by the first and second sub-region is an actual S/D region in which the first sub-region represents a highly doped region (near $dC/dV = 0$) while the second sub-region represents a lightly doped region. The reversal in the trend of dC/dV at a point of 385 nm appears to conflict with the simplistic interpretation of the junction behavior employed to this point (that the capacitance at the Schottky contact decreases with increasing carrier concentration). A possible reason, as explained in section 3.3.8, may due to a decrease in contact resistance at a highly doped level. Theoretical calculations of the capacitance sensor's sensitivity presented in Chapter 4 also show a significant degradation in sensitivity when the contact resistance falls below a certain level. The reversal in the trend of the magnitude of dC/dV causes some difficulties in discriminating a highly doped region from a region of light doping unless the location of one region is known in advance. This is a limitation of the SSCM technique. For this reason, the SSCM technique is suitable for measuring dopant densities ranging from 10^{14} to 10^{19} cm^{-3} due to the signal to noise ratio limited.

3) A region of positive dC/dV: this region ranges from 880 nm - 1200 nm on the displacement axis. As mentioned in Chapters 2 and 3, the sign of the measured dC/dV

identifies the type of carrier. The polarity of the voltage output of the lock-in amplifier is determined by the calibration of the measurement system. For this particular image, the positive *dC/dV* region represents the N-type substrate. In this region, the magnitude of *dC/dV* increases from 0 V at 880 nm and reaches a constant value above 1100 nm on the displacement axis. The curve in Figure 5.6 also suggests that the dopant density in the n-substrate is decreased from that in the substrate level toward the pn junction.

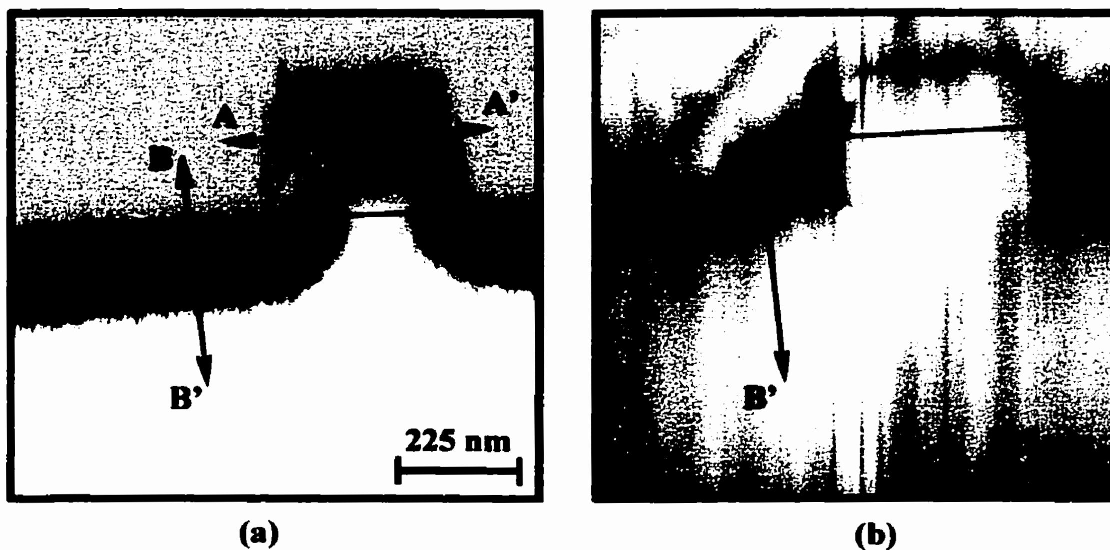
Another interesting region has been observed in Figure 5.6 where *dC/dV* is a constant. This region ranges from 450 - 810 nm. The presence of this region makes the measured image look unrealistic even though all parts making up the device are clearly shown (i.e. gate, source/drain, insulating layer, etc.). The cause of these artifacts is not well known and could not easily be explained. However, we expecte that such artifacts are related to the RF voltage level on the tip. During this research, these kinds of artifacts have frequently been observed when the RF voltage on the tip is sufficiently high. As mentioned earlier, the RF voltage on tip was larger than 2.5 $V_{p\text{-}p}$ when these images were taken. We will demonstrate later in the next section that this voltage level may be high enough to cause artifacts. High RF voltage on the tip may push the boundary of the pn junction deep into the substrate and can even change the sign of the measured *dC/dV*. Similar effects have been observed by several researchers who have been used the conventional SCM as the dopant profiler. O'Malley *et al.* **[95]** and Kleiman *et al.* **[96]** have been demonstrated the apparent movement of a pn junction location by varying the bias voltage applied to the tip. They observed that the images change in such a way that the apparent pn junction moves with bias voltage, and consequently the sign of *dC/dV* changes in the active regions of the device. These effects have been verified by process simulators and the results agree with observations made with SCM images **[95]**. For our case, it is suggested that large RF voltage on the tip may cause significant rectified current flow and therefore result in a "self-bias" of metal-semiconductor contacts even when the external DC bias is 0 V.

The dependence of the pn junction location on the RF voltage level is very complicated. The study of this relationship falls beyond the scope of this thesis will not be discussed in detail. Artifacts can be eliminated if the RF voltage on the tip is kept

low at the expense of losing capacitance sensor sensitivity. The location of the pn junction indicated in Figure 5.6 does not represent the actual pn junction. It is expected that the apparent pn junction should be somewhere around the point of 420 nm on the displacement axis.

In order to measure the gate length, channel length, and the S/D junction depth, the image shown in Figure 5.7 is used instead. These images were taken at the same time as the images shown in Figure 4.44. The measurements were performed with the RF voltage on the tip set to about 400 mV_{p-p}. The image shows excellent contrast between n-type and p-type regions and clearly delineates the boundary between them. The location of pn junction is therefore well defined as an interface between the black and white regions. In this gray scale image, the dark part of the S/D regions represents the regions of carrier concentration less than 10^{18} cm^{-3}. The part of S/D regions with near zero *dC/dV* is composed of heavily doped diffusion. We note that the magnitude of the signal in the heavily doped regions appears to be near zero because the carrier concentration in these regions is beyond the detectable range of this technique.

By taking line scans (A-A'), (B-B'), and (C-C') as shown in Figure 5.7, the gate length, S/D junction depth, and channel length of the device can be measured respectively. The curves in Figure 5.8 show line cross-section (A-A') profiles that were taken across the gate at half height from both capacitance and topographical images. The negative portion of *dC/dV* (blue curve) in the capacitance line profile represents the region of the gate. Non-zero *dC/dV* measured on the gate suggested that the gate is doped with the same carrier type as the S/D regions. Using a technique previously described, the edges of the gate could be located and the length of the gate could be measured to be 375 nm (see figure 5.8).



(a) (b)

Figure 5.7 Capacitance (a) and topographical (b) profile shows a close up view around the gate of a 400 nm MOFEST

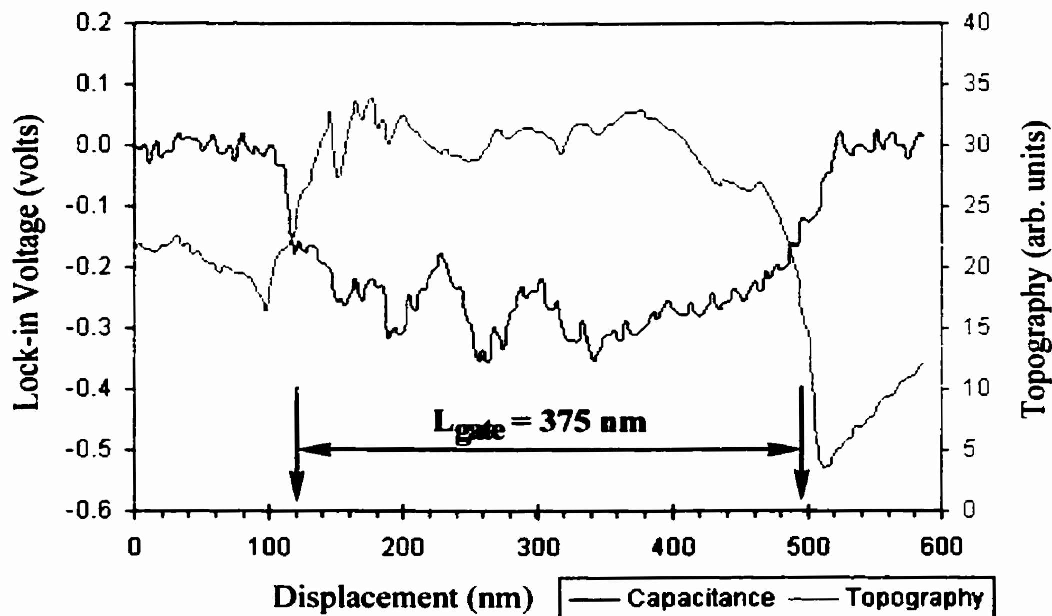


Figure 5.8 Capacitance derivative *dC/dV* and topographical line cross-section profile that is used to measure the length of the gate. (line A-A' shown in Figure 5.7)

Similarly, the curve in Figure 5.9 shows line cross-section (B-B') profiles that were taken vertically across the S/D region. From the capacitance line profile (blue curve), the positive portion of the *dC/dV* curve represents the n-type substrate while the negative portion represents the p-type S/D regions, and the zero *dC/dV* portion represents the insulating layer. The location of a built-in pn junction is naturally defined as a point where *dC/dV* crosses the zero voltage axis and changes in sign. The measured S/D junction depth depends on how accurately the edges of the junction on the heavily doped and lightly doped sides can be located. Because the capacitance derivative *dC/dV* is near zero when the measurement is made in the heavily doped region, we can not accurately locate the interface between the S/D and the insulating layer using the capacitance line profile. In this case, topographical line profiles are used instead. On the other hand, the capacitance line profile is used to locate the pn junction. From these two points, the S/D junction depth could be measured as shown in Figure 5.9 and it was found to be about 200 nm.

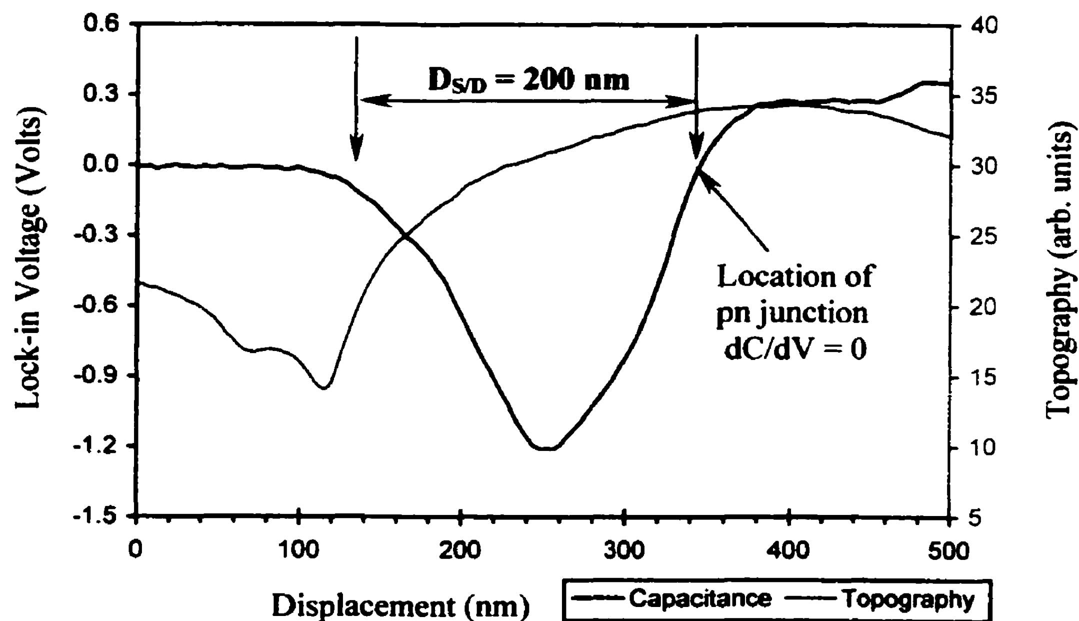


Figure 5.9 Capacitance derivative dC/dV and topographical line cross-section profile that is used to measure S/D junction depth. (line B-B' shown in Figure 5.7)

To measure the channel length, a line cross-section profile was taken along the channel (C-C') on the capacitance derivative image as shown in Figure 5.7. The results were plotted in Figure 5.10. In this graph, the positive portion of *dC/dV* represents the n-type region (substrate) while the negative portion represents p-type S/D regions. The channel length was determined by the locations of pn junctions (*dC/dV* ~ 0) that were formed by S/D regions and the substrate at the channel. The distance between these two points (channel length) was measured, as shown in Figure 5.10, to be 145 nm.

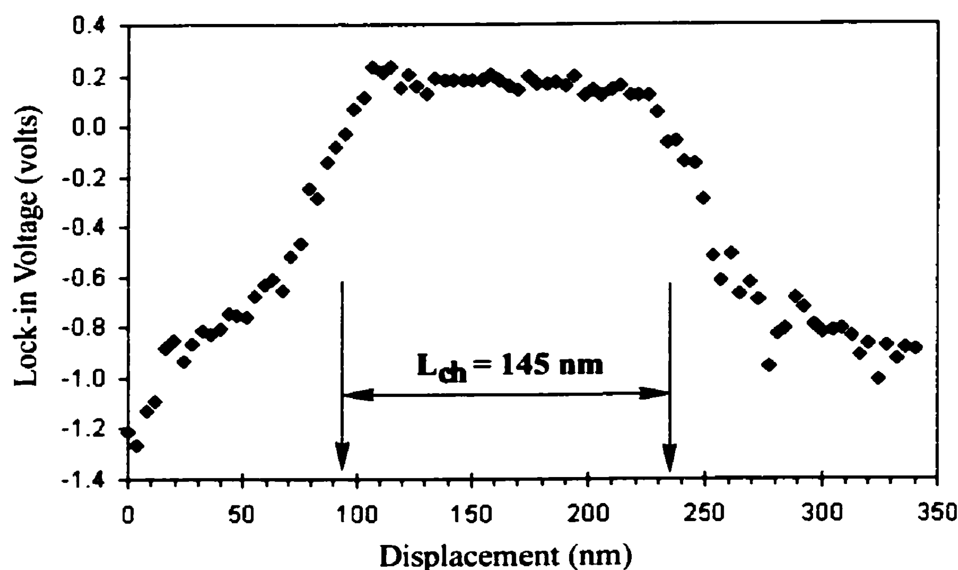


Figure 5.10 Capacitance derivative *dC/dV* line cross-section profile that is used to measure the channel length. (line C-C' shown in Figure 5.7)

The measurement of the distance between two adjacent gates (pitch) has shown that the actual dimension of the device should be about 8% larger than the dimension displayed in this section. Therefore, the dimensions of the gate length, junction depth, and channel length that were previously measured must be scaled to compensate for the discrepancy. Table 5.1 shows a summary of the results after the dimensions were scaled.

Table 5.1 SSCM measurements of parameters from a 400 nm MOSFET

Parameters	Dimension (nm)
S/D Junction Depth	216
Gate Length	405
Channel Length	157
S/D/G Overlap	124

5.2 Dependence of pn Junction Location on Tip Voltage

The movement of pn junction locations has been discussed in the previous section. This effect has been demonstrated by several research groups who used the SCM technique as a dopant profiler [95][96]. In this section, the artificial images that were produced by a high RF voltage applied to the probe/sample junction are demonstrated. Experiments were carried out by imaging the 400 nm p-channel MOSFETs at different levels of RF tip voltage. The amplitude of the RF voltage on the tip was controlled by adjusting the amount of attenuation between the resonator and oscillator (see Figure 5.1). Figure 5.11 shows experimental results. Data were obtained by scanning the same device with a sequence of attenuation levels of 10, 13, 16, 20, 23, and 26 dB respectively. In addition, the experiment was repeated several times, and all measurements were performed within a day. This ensured that data taken for each image was not influenced by the possible change in sensitivity (or resolution) that may result from surface contamination. The results were very consistent. Images shown in Figure 5.11 are 6 out of 18 images that were taken during the course of the experiment. From a knowledge of the resonator loss, the RF voltage on the tip corresponding to each attenuation level could be estimated and is indicated on the images. It can be seen from Figure 5.11(a), (b), (c) that the location of the pn junction is pushed toward the substrate if the RF voltage is higher than 500 mV_{p-p} (the pn junction is surrounded by a "shadow artifact"). The distance that the apparent pn junction can move depends on the amplitude of the RF voltage on the tip. The larger the RF voltage is, the deeper the pn junction is moved into the substrate.

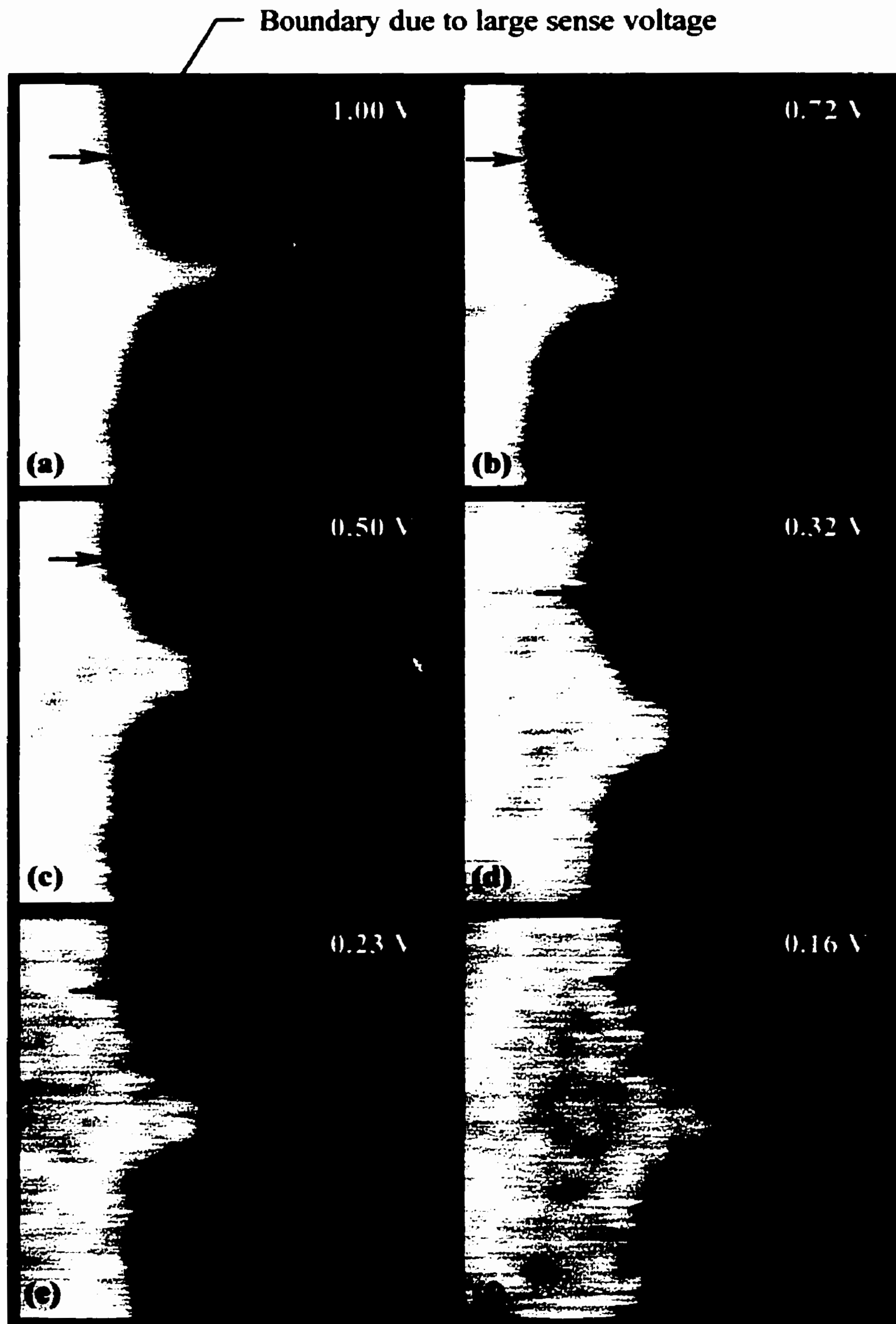


Figure 5.11 1μm x 1μm SSCM images of the 400 nm MOSFET obtained with various probe voltages. The image labels show the peak-to-peak voltage at the probe for that particular image. At higher voltages, the "shadowing" artifact at the boundary between the pn junction becomes more dominant.

The "shadow artifact" surrounding pn junction is not obvious with low voltages or does not exist at all. For SSCM measurements, the RF voltage on the tip should be maintained below 500 mV_{p-p} to avoid undesirable results. Even with this level of RF voltage, the sensitivity of the designed sensor was estimated to be well below 3×10^{-21} $F/\sqrt{Hz}$.

5.3 Imaging a Bipolar-Junction Transistor Device Cross Section

In this section, a discussion of a bipolar junction transistor cross-section is presented. The device is a PNP bipolar transistor that was specially fabricated as a test sample for characterizing SRM measurements [42]. The structure of this device is shown in Figure 5.12. Metal contacts to emitter, base and collector regions are identified by the letters "E", "B", and "C" respectively. Because the device was built for the purposes of SRM imaging, all the device regions were shorted out. This device was built in a p-type device well. The collector contact "C" makes contact to the lowly doped p-type collector region through a low resistance path provided by the "SINKER" and the p+ buried layer as shown in the schematic drawing of Figure 5.12. The device is also electrically isolated from adjacent devices using isolation structures "ISO" to reduce parasitic effects.

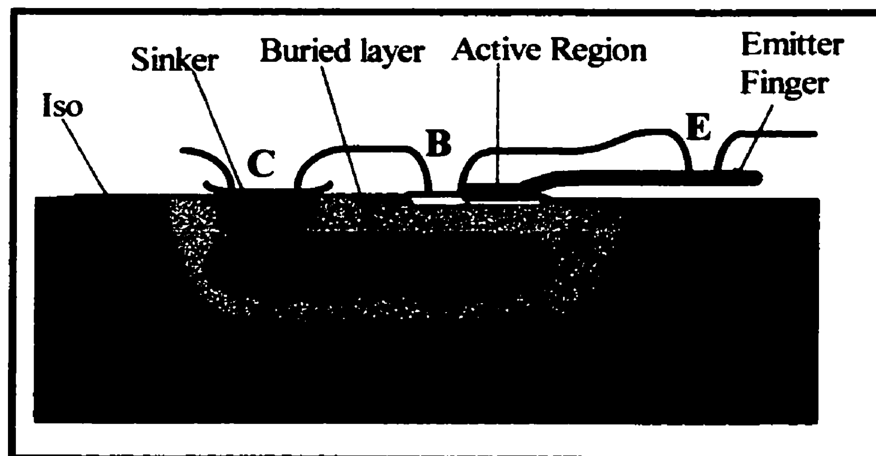


Figure 5.12 A schematic drawing of a PNP bipolar transistor. (not drawn to scale)

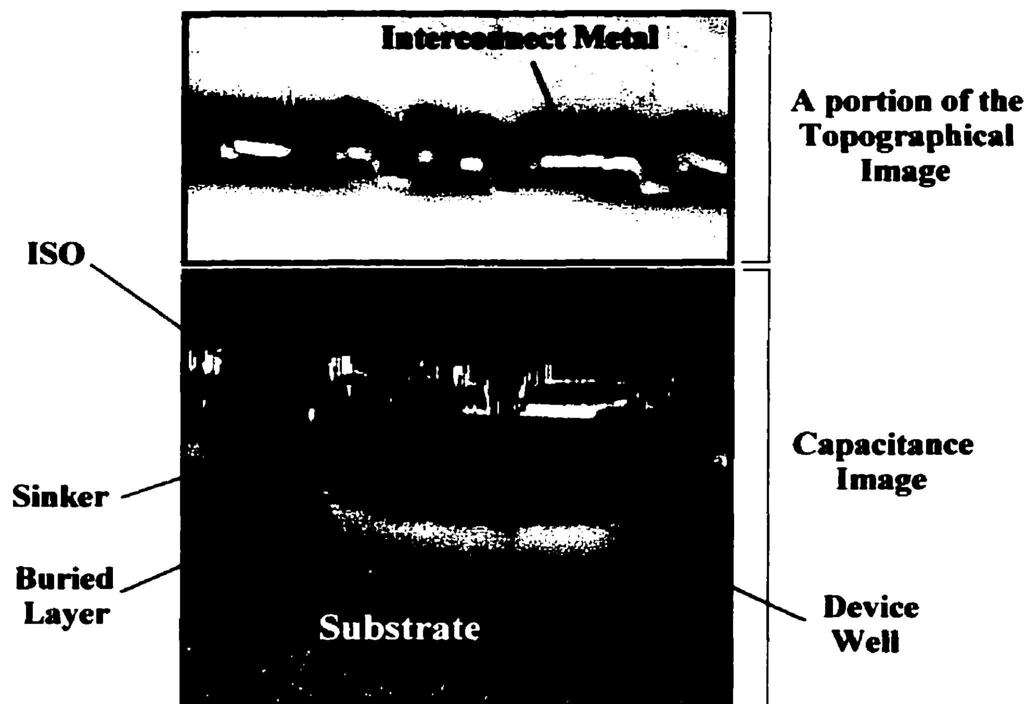


Figure 5.13 Capacitance derivative profiles of a PNP bipolar transistor: an overall image showing the device well, buried layer, sinker, and the other regions of the device. A portion of the topographical image is placed above the capacitance image to aid location of device regions.

An overall SSCM image of a test PNP bipolar transistor is shown in Figure 5.13 (image size is 18 x 18 μm). Data were acquired at 0 DC bias voltage and using a sinusoidal modulation signal of 0.5 $V_{p\text{-}p}$ at 90 kHz. The time constant of the lock-in amplifier was set at 10 ms with a scan rate of 1Hz. In the SSCM image, a very bright region on the gray scale signifies a region of positive *dC/dV* while a black region signifies a region of negative *dC/dV*. Although the resolution of the image is not ideal, all the parts of the device could be identified and were labeled as shown in Figure 5.13. For example, the gray region at the top in this image with *dC/dV* ~ 0 is the dielectric layer. The "Sinker" is shown as small, darker region with negative *dC/dV* and located below the collector contact. The sinker is attached to the buried layer that also has negative *dC/dV*. The device well appears as a darkest region with highest negative value of *dC/dV* (black region) surrounding the buried layer. Just right on top of the

buried layer, there is a very bright strip which is the base region (positive *dC/dV*). The active region, however, could not be identified in this image. Also in Figure 5.13, there are several bright spots on top of the image and a thin bright line that is running horizontally along the device. Those features are attributed to the interconnect metal layer that was used to join the device terminals (collector, base, and emitter) together. In theory, these features should not be present in the capacitance image because no capacitor forms between the metal tip and a metal layer.

The presence of these features can be understood because when a metal tip is touching a metal layer, the resonator is short-circuited and the resonant curve flattens out, resulting in a large change in the output of the capacitance sensor. This type of feature has been frequently observed (especially for a fresh polished sample) in form of a large voltage spike when we scan a tip over a region of metal on the sample surface. However, this feature is less likely to occur if the sample is left exposed for a longer period of time. The reason may due to the formation of native oxide that covers the sample surface and therefore prevents the tip from touching metal layers directly.

Figure 5.14(a) and 5.14(b) shows a close-up view of SSCM images of the test PNP bipolar junction device. The image in (a) shows the base contact "B" at the left hand side and the emitter contact "E" at the right hand side of the image respectively. The top part of this image is a topographical image that was taken along with the capacitance image (only a portion of the topographic image is shown here). In the capacitance image (figure 5.14a), a bright thin line running along and on top of the device is an interconnect metal layer that was connected to the base and the emitter via an emitter finger. The locations of the base and emitter contacts can be clearly seen in both topographic and capacitance images. The base region is shown as a bright (white) strip that is located beneath the base contact "B" and runs horizontally from the left edge of the image to the center. The image of the base contact also shows that the contact extended too far into the base region. Similarly, the emitter finger is shown as a bright strip located beneath the emitter contact "E" and running horizontally from the right edge of the image to the edge of the base contact "B". The emitter finger and the base region overlap each other at the center of the image. It was expected that the region sandwiched between the base and the emitter finger is the emitter region (or active region).

However, visual examination of the capacitance image did not show enough contrast to clearly locate the emitter region. The reason is that the size of the image is too large (10 x 10 μm) compared to the thickness of the emitter region. A line cross-section profile taken across the active region shows a depression of measured *dC/dV* when the tip crosses this region. The depression indicates the presence of the active region. Unfortunately, we do not have a higher resolution image to present here.

Figure 5.14 (b) is a close-up view of a SSCM image (4 x 4 μm) taken around the collector area. The image clearly shows the sinker, the buried layer, the device well, and the contrast between them. In gray scale representation, dark parts signify regions of negative *dC/dV* and represent a p-type device while gray parts that are labelled "insulating layer" signify regions of *dC/dV* ~ 0. The sinker and buried layer regions also have negative *dC/dV* and represent p+ regions, but the magnitude of measured *dC/dV* in these regions is smaller than *dC/dV* measured in the device well. Also from this image, the shape of the sinker resembles that shown in the schematic drawing of Figure 5.12.

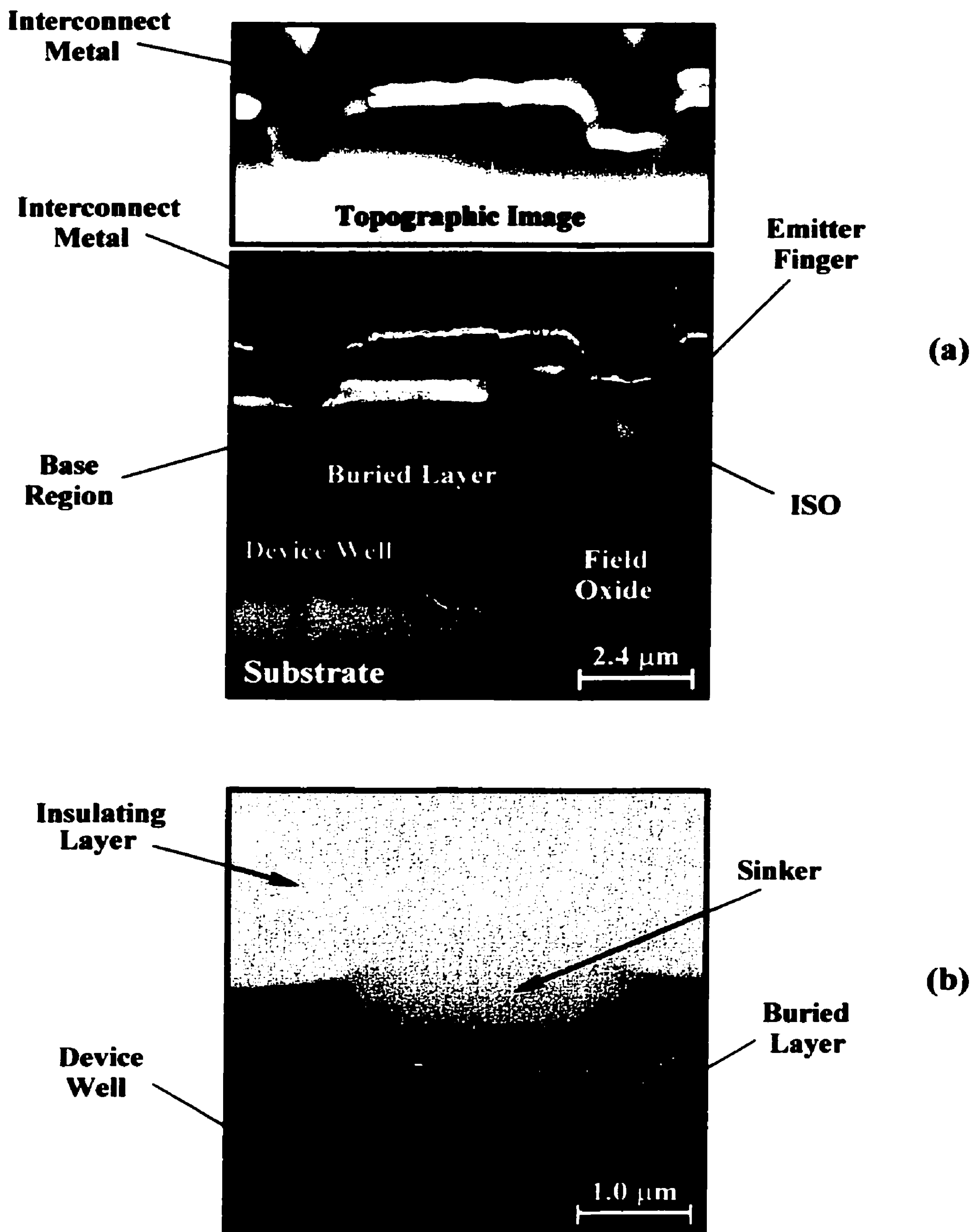


Figure 5.14 Capacitance derivative profiles of a PNP bipolar transistor.
(a) An image showing the base region, emitter finger, a part of buried layer and a part of the device well.
(b) A close-up view of the collector region

5.4 Imaging of Round-Robin MOSFETs (180 nm)

In this section, we present SSCM results from imaging of other Round-Robin MOSFET cross-sections with a nominal gate length of 180 nm. These devices were also provided by SEMATECH as a part of a round-robin project aimed at evaluating profiling techniques. The exact fabrication processes of these devices is unknown. Each sample under test has two devices, each fabricated side-by-side. One is a p-channel MOSFET transistor and the other is a n-channel MOSFET transistor. Although there are two devices on each sample, there is only one device type that meets the correct specifications. The results presented in this section were obtained from a p-channel MOSFET which met the specifications. From information given by SEMATECH, a suggested structure of these devices is shown in Figure 5.15. Both devices were fabricated on a p-type substrate. A p-channel MOSFET was fabricated by implanting a buried p+ layer in an N-well to form highly doped source/drain regions (HDD-S/D implant) of the device. Similarly an n-channel MOSFET was fabricated by implanting a buried n+ layer in a P-well to form highly doped source/drain regions (HDD-S/D implant) of the device. Generally, there should be an insulating structure located between these transistors. However, there was no information that confirmed the presence of ISO structures.

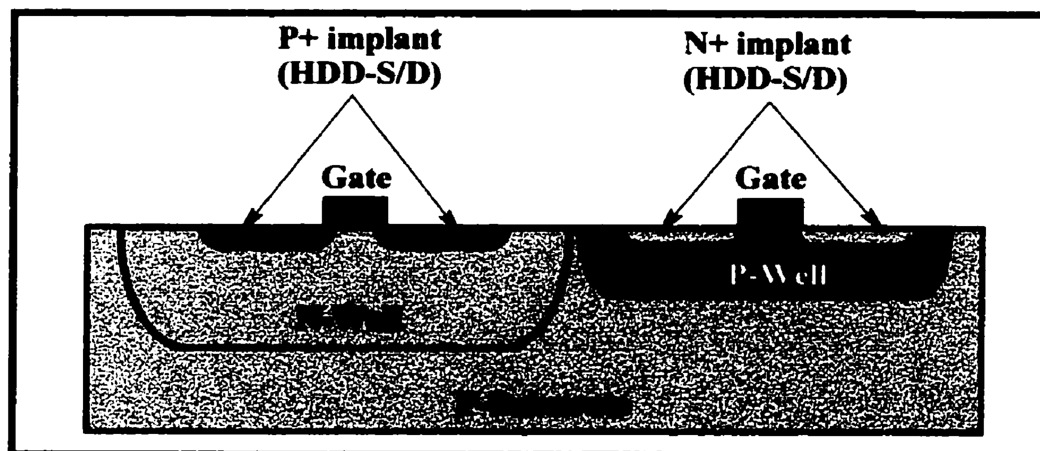


Figure 5.15 A schematic drawing of 180 nm Round-Robin MOSFETs. (not drawn to scale)

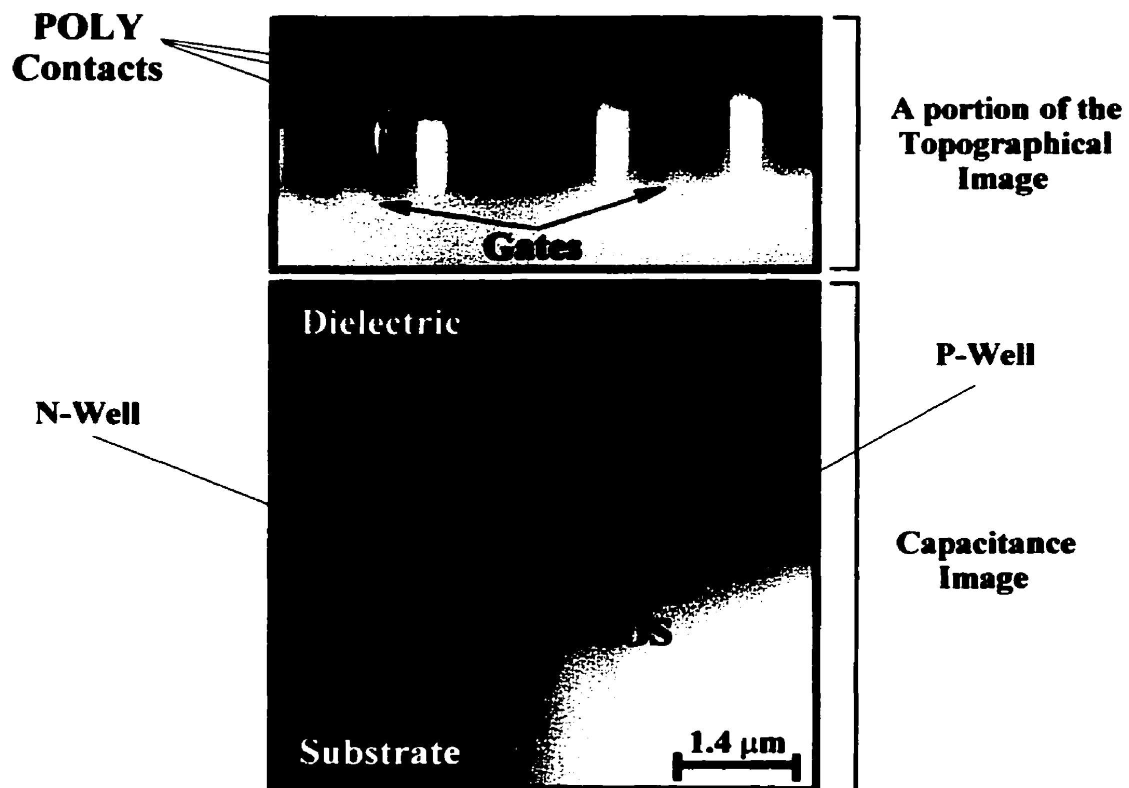


Figure 5.16 Capacitance derivative profiles of 180 nm MOSFETs. An overall image showing both pMOS, nMOS and the other regions of the devices. A portion of the topographic image taken along with the capacitance image shows the device's contacts.

Figure 5.16 shows an overall image (6μm x 6 μm in size) of the 180 nm MOSFET devices previously described. Again, the data were acquired at zero bias voltage and with an AC modulation signal of 0.5 $V_{p\text{-}p}$ at 90 kHz. The time constant of the lock-in amplifier was set at 10 ms and the scan rate was 1Hz. In addition, the phase of the lock-in amplifier was set-up such that black regions of the image represented negative *dC/dV* while white regions represented positive *dC/dV*. All regions that were schematically drawn in Figure 5.15 could be identified as shown in Figure 5.16. In this capacitance image, thin black strips located at the left hand side and at half the height of the image are the source/drain regions of a pMOS

device. An N-well is shown as a brighter region surrounding the pMOS. Similarly, thin white strips located at the right hand side and at half height of the image are the source/drain regions of an nMOS device. The P-well appears as a darker region surrounding the nMOS device. Also seen in this image are three black strips running vertically on top of the source/drain regions of both devices. These black strips are attributed to polysilicon layers that normally make contact to the devices at their S/D regions. These device contacts are clearly shown in the topographical image that was placed above the capacitance image. It should be noted that only a portion of the topographical image around the contacts was shown in Figure 5.16. The reason for seeing these contacts in the capacitance image has been described in previous sections.

Figure 5.17 shows a close-up view around the gate of the 180nm devices. Both of these images clearly show S/D regions, gate, and device well regions. This scan measures 1.0 μm x 1.0 μm in size. In these images, the capacitance derivatives of the tip-to-sample contact are represented by gray scale shading. For the image in (a), a pMOS transistor, black signifies regions of negative dC/dV and represents p+ implanted source/drain region while white signifies positive dC/dV and represents an N-well region. On the other hand, for an nMOS transistor (figure in (b)), white signifies regions of positive dC/dV and represents the n+ implanted source/drain region while black signifies negative dC/dV and represents a P-well region. In both of these images, gates have the same color as the source/drain region. This may suggest that these gates were heavily doped with the same type of dopant as the source/drain regions. This normally happenes in a self-aligned process in which a polysilicon gate is used as a resist mask for the source/drain implantation. The polysilicon gate and source/drain regions are then doped with a particular dopant type at the same time.

It was mentioned previously that the magnitude of dC/dV decreases when a tip is scanned over a heavily doped p-type region (see figure 5.9). The same results are observed here when we image an nMOS device. This is clearly shown in Figure 5.17b in which a very bright region represents the highest value of dC/dV measured in the source/drain region. When the tip entered the shallow end of the source/drain regions, the magnitude of measured dC/dV decreased. In addition, it was also observed that the measured dC/dV did not change in sign when a line profile was taken across the channel of the nMOS device. This unexpected

result could not be explained because this device did not meet the specifications as mentioned at the beginning of this section.

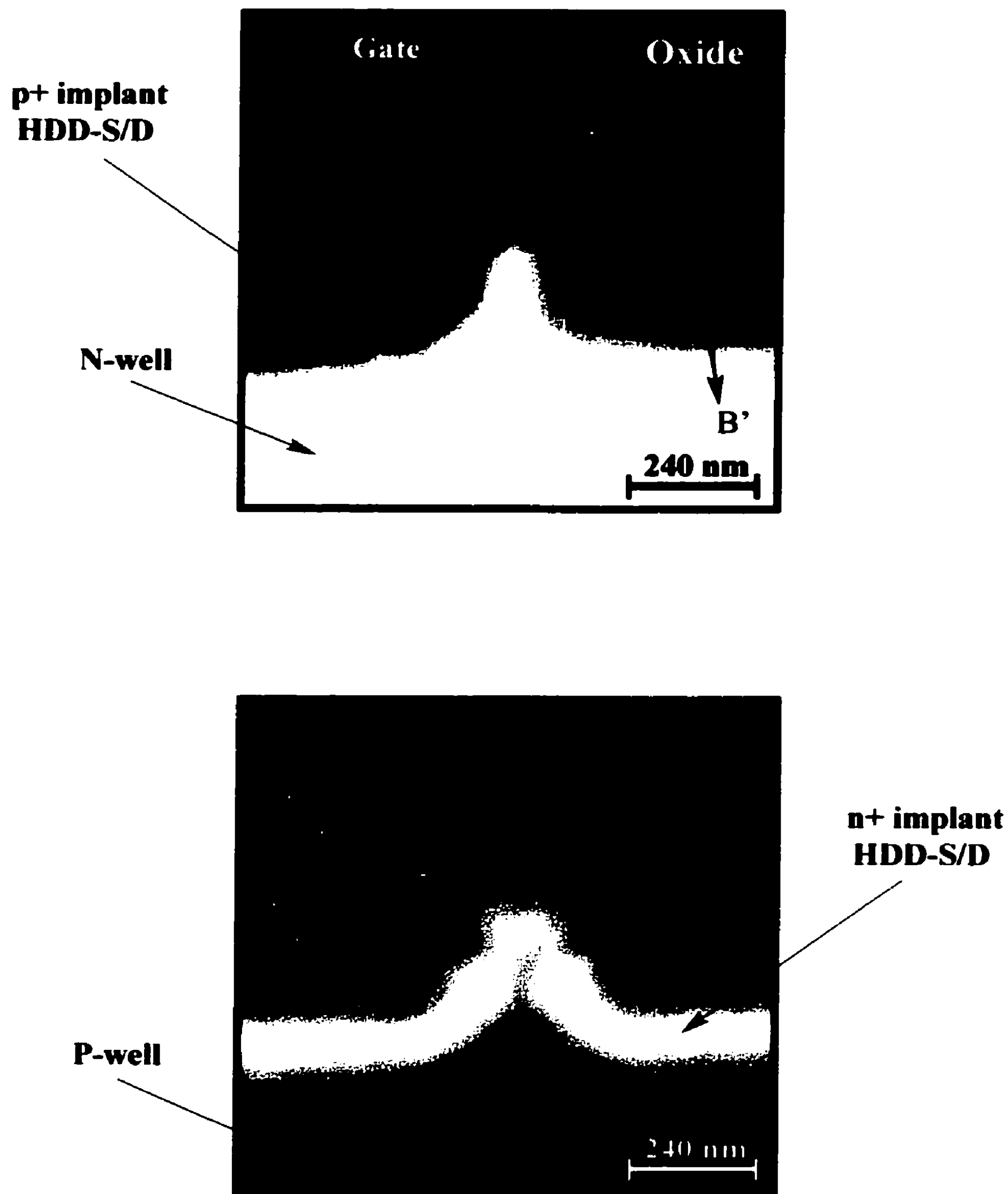


Figure 5.17 Capacitance profiles showing a close-up view around the gate of 180 nm MOSFET devices
(a) An image of a pMOS device showing the gate, channel, S/D regions
(b) An image of an nMOS device showing the gate, channel, S/D regions

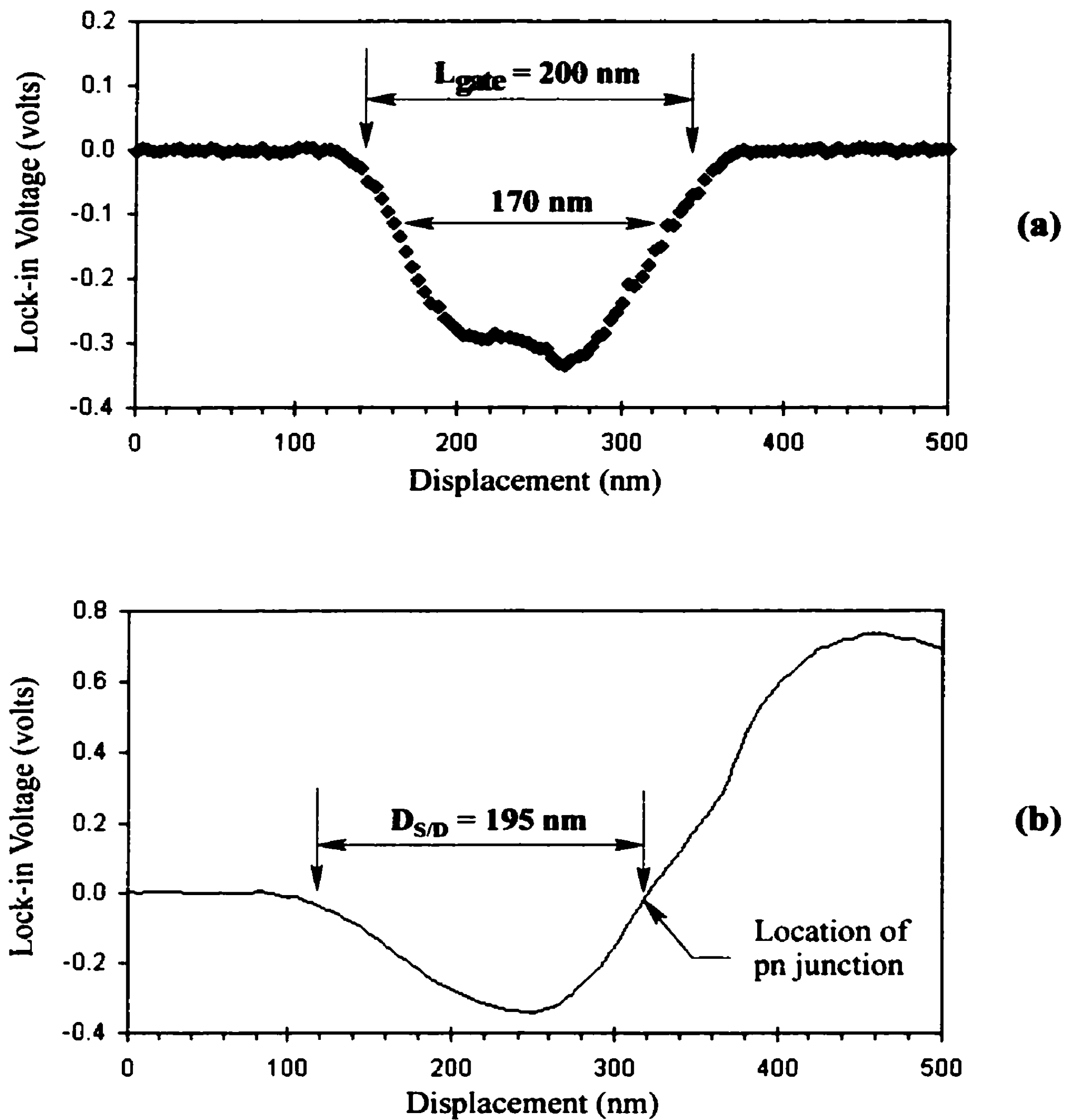


Figure 5.18 Capacitance derivative *dC/dV* line cross-section profiles that were taken:
(a) Across the gate at half height of the 180 nm pMOS device, and
(b) Across the source/drain regions of the 180 nm pMOS device

In order to measure the gate length and the junction depth of the pMOS device, line cross-section profiles were taken across the gate at half height and the source/drain regions respectively. The results of these profiles are plotted in Figure 5.18a and 5.18b respectively.

As mentioned earlier, the measurements of the gate length and junction depth depend on how accurately the edges of the gate and boundaries of the pn junction can be located. Normally, the topographic image taken along with capacitance image is used to locate these boundaries. However, the topographic image of the 180 nm pMOS was of poor quality and is not presented here. Thus, the capacitance image was used instead. As indicated in Figure 5.18a, the gate length was estimated to be between 170 nm to 200 nm. This estimated value agrees with the expected gate length of 180 nm. The junction depth was measured at about 195 nm as shown in Figure 5.18b. In Figure 5.17a, the shape of the channel did not resemble that shown in the schematic drawing well. As a result, the channel length could not be accurately measured.

5.5 Imaging MOSFETs from VLSI Integrated Circuits

In previous sections, the SSCM technique was successfully used to image several semiconductor devices. However, some of these devices were specially fabricated for characterizing profiling techniques. In this section, actual very large scale integrated circuits (VLSI) are imaged. The sample selected for imaging is an Intel 486 DX microprocessor. Sample preparation in this case is very simple. A chip of the Intel 486 DX microprocessor was cut in half to expose its cross-section. The polishing technique described in section 2.6 was then applied. After polishing, the sample surface was cleaned with HF to remove native oxide and any contamination that was remained from polishing. The sample was then mounted in cross-section orientation for imaging. All the pins of the chip package were tied together and attached to a sample holder using silver epoxy. The AC modulation signal that is normally required for dC/dV measurements was supplied to the sample via the pins of the package.

Figure 5.19 shows a SSCM image of the MOSFET devices that were scanned from the microprocessor chip. In this image black regions on the greyscale represent regions of negative dC/dV while bright regions represent regions of positive dC/dV. The regions shown in grey at the top of capacitance image have $dC/dV \sim 0$. In the capacitance image, two MOSFET transistors that were fabricated in cascade and that shared the same S/D regions can

be seen. The source/drain regions here are clearly observed as the darkest parts (black) in the image. The bright spots that separate the source and drain region are the channels of MOSFET devices. A large, white shaded area at the bottom of the image is the substrate. The device's gates could not be seen in this image; however, they can be easily seen from the topographic image that is placed above the capacitance image. Although the capacitance image clearly shows all regions of a MOSFET device, it does not tell us which device is nMOS or pMOS because the sign of measured *dC/dV* depends on the phase setting of the measuring system (lock-in amplifier).

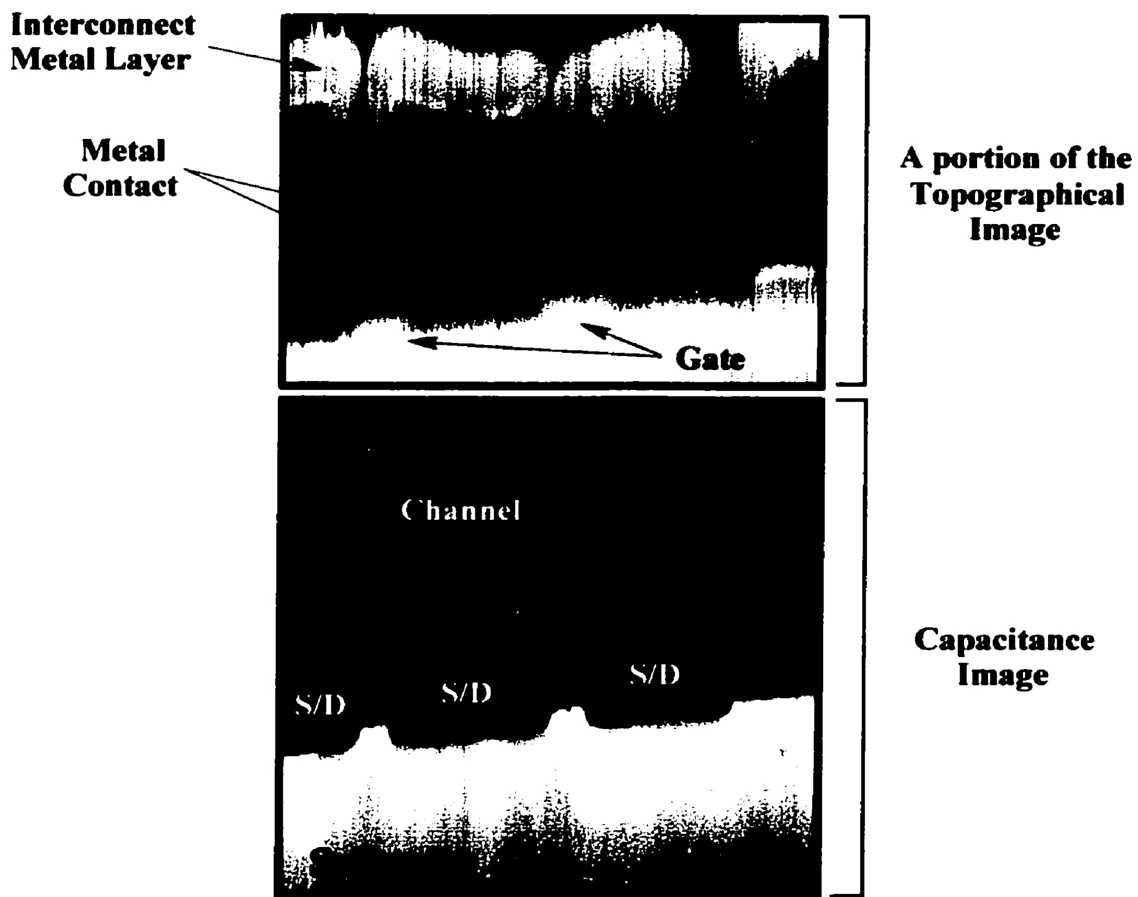


Figure 5.19 A SSCM image of MOSFET devices from an Intel 486 DX microprocessor chip.

In the topographic image, device gates appear as bright spots located on a large bright shaded area that represents the substrate. The complicated textures that run over these gates are metal contact and multi-layer interconnect metal layers. Also in this image, there are many vertical straight lines appearing over the entire image. These lines may be attributable to the vibration that was coupled to the SSCM cantilever from the surrounding environment.

Figure 5.20 shows a close-up view at the channel region of a MOSFET device in the Intel 486 DX microprocessor chip. The capacitance image clearly shows the source/drain region (black regions), and the channel as a white region. The gate can be identified from the topographical image as a white horizontal strip (labeled in the topographical image). From the capacitance image, the junction depths and the effective channel length were measured to be approximately 0.5 μm and 0.8 μm respectively.The gate length was measured from the topographical image to be approximately 1.0 μm and therefore the S/D overlap was 0.1 μm. It is believed that these dimensions reasonably represent the technology that was used to build the 486 microprocessor.

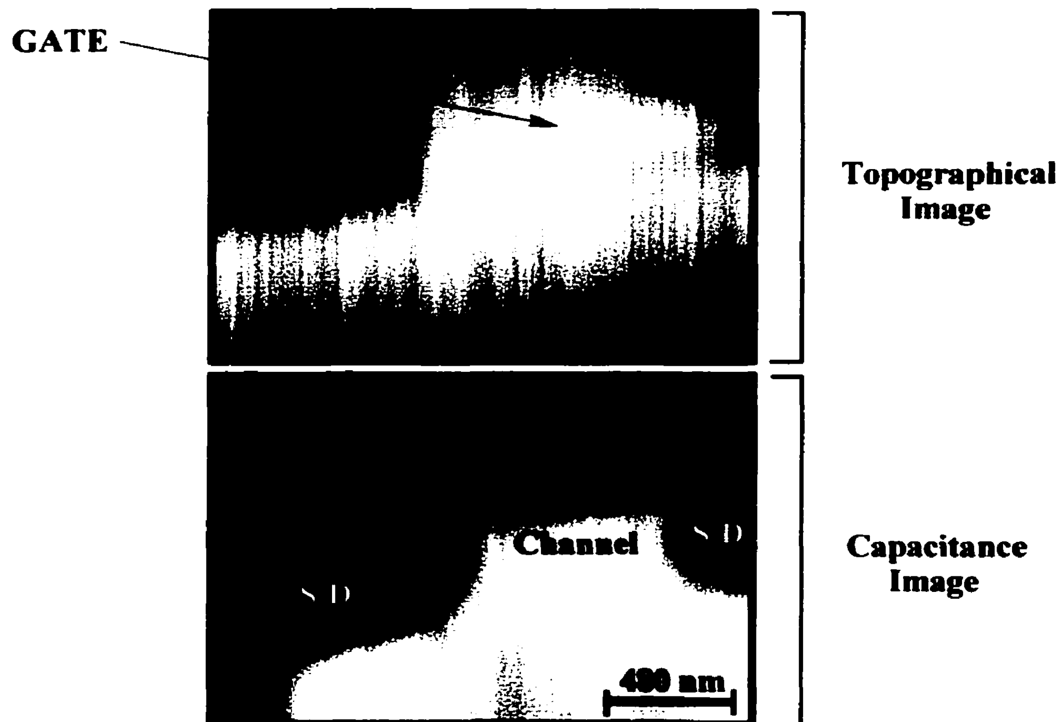


Figure 5.20 A close-up view showing a channel region of a MOSFET device that was taken from an Intel 486 DX microprocessor chip.

CHAPTER 6

CARRIER CONCENTRATION CONVERSION

The SSCM technique has proven itself as a method for 2D imaging of semiconductors using a wide variety of devices. The results presented here form a fraction of the number of semiconductor structures imaged with our instrument. So far, SSCM results have provided qualitative analysis of semiconductor devices in cross-section. Quantitative SSCM results may be achieved if the tip-to-sample junction can be theoretically and accurately modeled. Unfortunately, we observed that SSCM results did not agree with theoretical predictions for a well-behaved metal-semiconductor contact when carrier concentrations were relatively high (above 10^{18} cm^{-3}). Accurately modeling the tip-to-sample junction in this case becomes very complicated. Besides the need for an accurate model, the capacitance sensor output must be calibrated in terms of capacitance instead of voltage. This process requires an accurate determination of tip's radius and/or the radius of the tip-to-sample contact.

An alternative and simpler approach that can be used to extract the carrier density from the measured capacitance data is to use a calibration technique. In this approach, SSCM measurements are performed with the same tip on a uniformly doped wafer with known dopant density, and results are compared to those from SSCM measurements of an unknown wafer. The biggest limitation in calibration is the unavailability of self-contained calibration samples with regions doped from 10^{15} cm^{-3} to 10^{20} cm^{-3}. The advantage of using this type of sample over the separated standard samples is that it would help to eliminate systematic errors associated with changes in sample surface conditions. In this section, the conversion of measured *dC/dV* data to carrier concentrations using calibration data is presented. Due to the lack of a self-contained calibration sample in our laboratory, calibration curves were constructed using a set of separate standard samples instead.

6.1 Construction Of Calibration Curves

The standard dopant concentration samples used in this work were provided by Solid State Measurements, Inc. (Pittsburgh). These silicon samples were polished along the <100> plane and have dopant densities ranging from $10^{14}cm^{-3}$ to $10^{19}cm^{-3}$ for both n-type and p-type. Before *dC/dV* measurements were taken , surfaces were polished using collodial silica solution (similar to a standard polishing technique described in section 2.6). Samples were then dipped in a bath of 2% HF solution to remove native oxide and contamination. The sample was mounted on a sample holder in its lateral orientation and silver epoxy was used to make electrical contact .

The capacitance derivative *dC/dV* was measured for each standard sample using the technique presented earlier. Measurements were performed under force regulation and were repeated with the same tip. During these measurements a constant force was maintained on the probe from one measurement to another. This was done to ensure that the contact area and geometry of the junction was constant from one measurement to another. Factors that could cause a change in capacitance sensor output sensitivity, such as operating frequency and the slope of the resonant curve at operating point, was also recorded for later normalization. This ensured that the data taken on each sample were not influenced by changes in capacitance sensor sensitivity due to sample geometry. Also, the measurements were performed within a single day to ensure that the sample surfaces did not deteriorate while they were exposed to air. In addition, *dC/dV* measurements were performed by imaging a small area of the sample surface (a few hundred nm^2) and the average *dC/dV* was calculated from the measured data. This helps avoid cases in which the tip is loaded on a contaminated spot. For each sample, these measurements were performed several times, and the results were found to be repeatable.

Figure 6.1 shows a graphical representation of the variation of the capacitance derivative with substrate doping concentration. The capacitance data were acquired at 0V DC bias and using a sinusoidal modulation signal of 0.5 V_{p-p} at 90 kHz on the tip. The attenuation level between the resonator and oscillator was 20 dB. Since the tip-sample contact area is unknown, the scale of this curve is in arbitrary units. There are several observations that can be made on

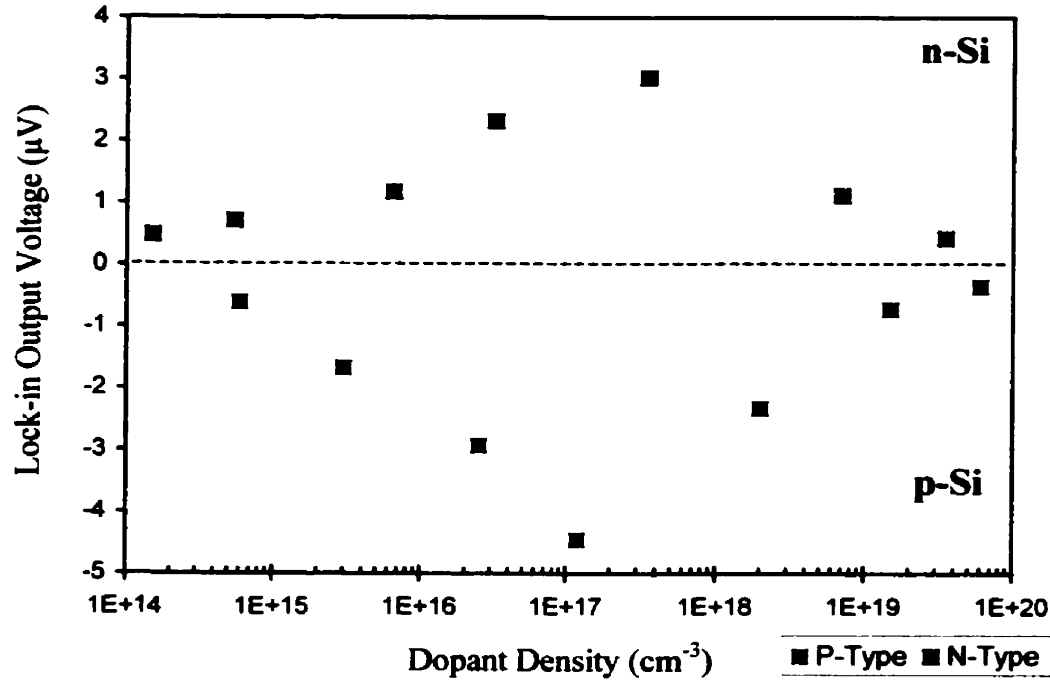


Figure 6.1 Capacitance derivative *dC/dV* versus doping concentration extracted from calibration samples. The measurements were performed for both p-type and n-type silicon substrates.

Figure 6.1. Firstly, measured *dC/dV* for P-type substrates is consistently negative while that for N-type substrates is positive for a given phase setting of the lock-in amplifier. These results agree with what we have observed in previous experiments where the sign of measured *dC/dV* changed as a tip was scanned across a pn junction. Secondly, the measured *dC/dV* monotonically increased over the doping concentration range of 10^{14} cm^{-3} to $10^{18} cm^{-3}$ and then decreased at high doping levels. This was true for both P-type and N-type substrates. For moderate doping concentration, *dC/dV* increased more rapidly as the doping concentration increased. Furthermore, a considerably steeper increase in the measured *dC/dV* values for P-type compared to N-type was observed.

For each doping level, *dC/dV* values for P-type material were consistently higher that those for N-type substrates. This agrees with the theoretical prediction shown in Figure 3.6. However, the prediction is only valid if the tip-sample contact area and the sensitivity of the measuring system (including capacitance sensor) do not change from one measurement to

another. In practice, these conditions may not have be satisfied.

6.2 Calculation of Carrier Density from Measured Data

In this section, the conversion of measured *dC/dV* data to carrier concentration for PMOS devices is presented (for NMOS devices, a similar procedure can be applied by using the n-type calibration curve). The conversion was done by comparing the measured *dC/dV* data to *dC/dV* data that were used to construct the calibration curve shown in Figure 6.1. In order to perform the conversion, the measured *dC/dV* was imported into Mathlab. Within Mathlab, the capacitance image was imported as a two dimensional matrix (256 x 256). Each entry of this matrix represented the value of measured *dC/dV* at each pixel in original image. In addition, the imported image was oriented such that each row vector of the matrix contained data that represented a line profile across the source/drain regions of the device. The data for each pixel were converted to carrier concentration. Some offsets were applied before the conversion. The magnitude of the offsets depended on how much the measured *dC/dV* in the insulating (oxide) layer was offset from zero *dC/dV* position. Offsets were determined by taking a small area on the insulating layer and then calculating the average *dC/dV* for this area. The whole image was then shifted up or down depending on whether this average *dC/dV* was negative or positive.

For each row vector, the data were divided into three different regions. The first region with near zero *dC/dV* represented the oxide region. The second region with negative *dC/dV* represented one type of carrier and the third region with positive *dC/dV* represented the other (see Figure 5.18b for a visualization of a typical line cross-section profile across the S/D regions). Due to the reversal of *dC/dV* data within the source/drain regions , as carrier concentration is increased above 10^{18} cm^{-3}, the *dC/dV* data in this region must be divided into two groups. The first group contained all the data that fell on the left hand side of the point of maximum *dC/dV* in magnitude in the S/D regions. The second group contained all the data that fell on the right hand side of the maximum *dC/dV* point in the S/D regions (see Figure 5.18b). The data in one of these two groups was then converted to highly doped carrier concentration and the other group converted to a lower doped carrier concentration. In this conversion, the

highly doped region of a MOSFET device were recognized as a region that was located next to the oxide layer and of course the pn junction was located on the opposite side.

Due to the non-linearity of the calibration data, a piece-wise-linear approximation was used. The p-type calibration curve used for the conversion process was divided into 8 bins in which each bin contained the range of *dC/dV* that was covered by two adjacent calibration data points. For each scanned line, a pn junction was selected by the program as a point located on the lowly doped side and from which *dC/dV* changed in sign. The oxide layer was selected as points located on the highly doped side and with $dC/dV \sim 0$.

Before conversion took place, the calibration curve was rescaled so that the maximum *dC/dV* value of the calibration curve matched the maximum value of *dC/dV* measured in the source/drain regions for each scanned line. When the program is started, the maximum *dC/dV* point is first located and then used as a reference point to separate a lowly doped from a highly doped side. For each data point within a row vector, the program determines which bin the data point belongs to. That data point is then converted to carrier density by using an appropriate equation of a straight line that joins two adjacent calibration data points. The process is repeated for all points. After conversion we can obtain the image of carrier density as a function of position.

Figures 6.2 and 6.3 show the results of carrier concentration produced by a point by point conversion of the measured *dC/dV* data in Figure 5.5 and Figure 5.17a respectively. The converted results are color coded and presented in form of the images. In both images, a dark red color on the top of the images represents the oxide layer (region of $dC/dV \sim 0$) while dark blue regions at the bottom of the images represent the n-Type substrate (region of positive *dC/dV*). The substrate was labeled here as an n-Type because both of these devices were PMOS devices. In practice, it should be noted that the *dC/dV* in the oxide layer is not exactly zero. It could be slightly positive, negative or zero due to the noise recorded by the instrument. For simplification purposes, however, thes data points were not converted to carrier concentration but were mapped to a single color instead. This explains why the oxide layer appears as a solid color in these images. Similarly, data in the substrate were also mapped to a single color although this does not correctly represent the carrier concentration.

All data with positive *dC/dV* on the lowly doped side were assigned to a single value (mapped to a solid color). In the conversion process, we only paid attention to mapping out the carrier concentration within source/drain regions. As expected, the carrier concentration in these regions decreased from 10^{19} cm^{-3} (heavily doped region) down to about 10^{16} cm^{-3} (lowly doped region) before entering the substrate.

It has been demonstrated that the carrier concentration can be extracted from the measured *dC/dV* data using calibration curves. However, the 2D conversion process presented in this section has several limitations that are worth mentioning:

- The conversion can only be applied to MOSFET devices. As mentioned earlier, the calibration curve needs to be scaled such that the point of maximum *dC/dV* of the calibration curve is matched to the point of maximum *dC/dV* measured in the source/drain regions of a device. For each scanned line, the conversion algorithm then uses this maximum *dC/dV* point in the source/drain regions as a reference point to separate highly doped from lowly doped regions. Data measured from a sample of homogeneous dopant concentration can not be correctly converted, since in this case, there is no reference point at all. The conversion algorithm can not recognize whether or not the measured data is due to a highly doped or lowly doped concentration level (the measured *dC/dV* at these two concentration levels may have the same magnitude and sign). However, the conversion may be used to convert the data that is measured from a sample which has a dopant gradient similar to the source/drain regions of a MOSFET device.

- In order to obtain a reasonably good 2D conversion image, *dC/dV* data measured in the source/drain regions of a device should be approximately constant. A large fluctuation of *dC/dV* data in the source/drain regions will cause difficulties when data is converted. In this case, each scanned line that makes up the image is scaled such that the point of maximum *dC/dV* of a calibration curve is matched to the point of maximum *dC/dV* measured in the source/drain regions (the point where the trend of measured *dC/dV* is reversed). The complexity of this process depends on how much the data in the source/ drain regions fluctuate. The exercise is therefore time consuming and needs great care to be exercised by the user. It is best to use high quality images for the conversion.

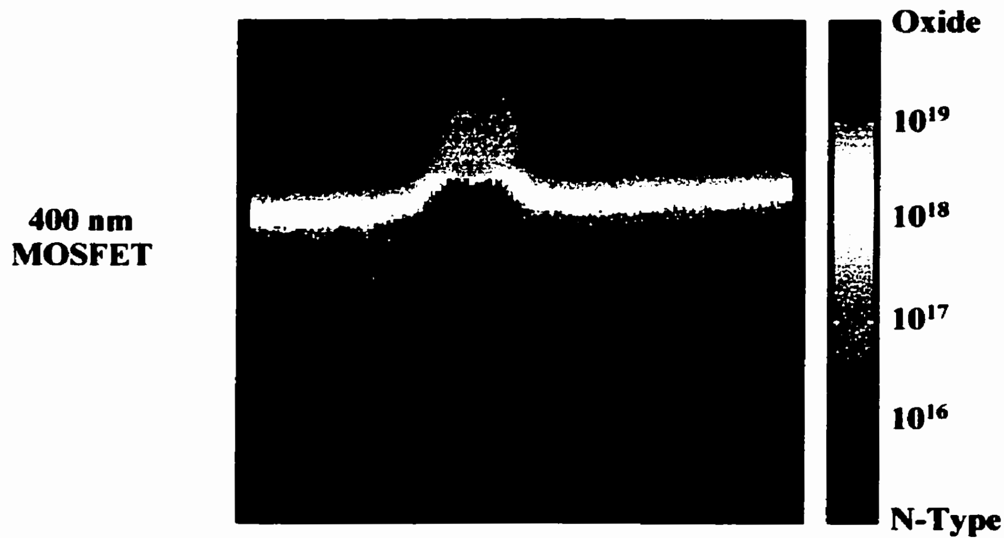


Figure 6.2 1.5 μm x 1.5 μm image of carrier concentration produced by a point by point conversion of the data in Figure 5.5 using the calibration data.

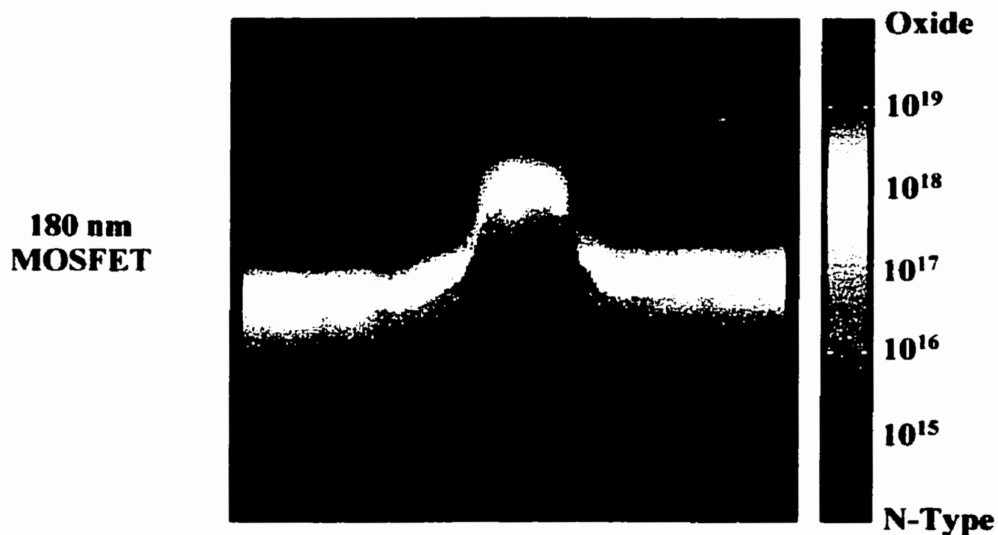


Figure 6.3 1.0 μm x 1.0 μm image of carrier concentration produced by a point by point conversion of the data in Figure 5.17a using the calibration data.

- Using calibration curves generated by measuring *dC/dV* from separate standard samples has two disadvantages: the first was discussed previously; the second is that the point of maximum *dC/dV* of a calibration curve is forced to occur at a concentration level of about 2×10^{17} cm^{-3} (see Figure 6.1). In practice, this may not be entirely true. Using such a calibration curve in the conversion may result in an inaccurate determination of the true position of carrier concentration within the source/drain regions. However, this problem can be limited by using a calibration curve that is constructed from a single self-contained calibration sample.

- As a tip is scanned across the gate of the device, the measured *dC/dV* was not zero as it is expected that to be. The magnitude of *dC/dV* in this region was normally found to be smaller than measured in the source drain regions. When conversion is applied to the gate region, an abrupt change in carrier concentration may appear in this region as shown in Figure 6.3. In Figure 6.2, *dC/dV* in the gate region is favorably small compared to *dC/dV* in the source/drain regions. The data for the gate of this device were forced in conversion to the highly doped concentration side. It should be noted that the converted data in the gate region Figure 6.2 and 6.3 do not accurately represent a true carrier concentration. This is an artifact of conversion. In practice, the exact dopant distribution in the gate region of a device is an unpredictable parameter and not well defined.

The conversion of *dC/dV* data to carrier concentration in two dimensions is complicated and time consuming. However, one dimensional conversion is simpler. Here, a cross-sectional line profile across the source/drain regions of a device is taken using an external image processing program (the NIH image program). Data are then saved and imported into Matlab as a vector. The imported data are normalized to the calibration curve. A point by point conversion is carried out and the carrier concentration versus position plotted. Figure 6.4 shows the result of converted data in form of 1D carrier concentration versus position. The 1D conversion was performed for a cross-sectional line profile across the source/drain regions of an sample used in Figure 5.7a. For comparison, SIMS measurements on the same device are also plotted. From the curves in Figure 6.4, we can see that the junction depths obtained from both experiments agree with each other (depth is between 220 - 250 nm). The dopant

concentration near the pn junction in the source/drain side is about 1 x 10^{16} cm^{-3}. However, the level of converted dopant concentration in the source/drain regions only qualitatively agrees with SIMS measurements.

It is well known that SIMS measures the chemical dopant profile while SSCM measures the electrically active dopant profile (or carrier profile). The carrier concentration should be equal to the dopant concentration if the dopant atoms are 100% ionized. In practice, the dopant atoms may not be 100% ionized. Incomplete ionization of the dopant may be possibly used to explain the discrepancy between the results of these two measurements. The discrepancy between the two results may also be attributed to the use of calibration curves in which the point of maximum *dC/dV* was forced to occur at 1.2 x 10^{17} cm^{-3}. As previously discussed, using this calibration curve may lead to an inaccurate determination of the true position of carrier concentration in the source/drain regions. If the P-type calibration curve shown in Figure 6.1 is slightly shifted to the right, the converted data shown in Figure 6.4 would shift up to match the data that were obtained by SIMS.

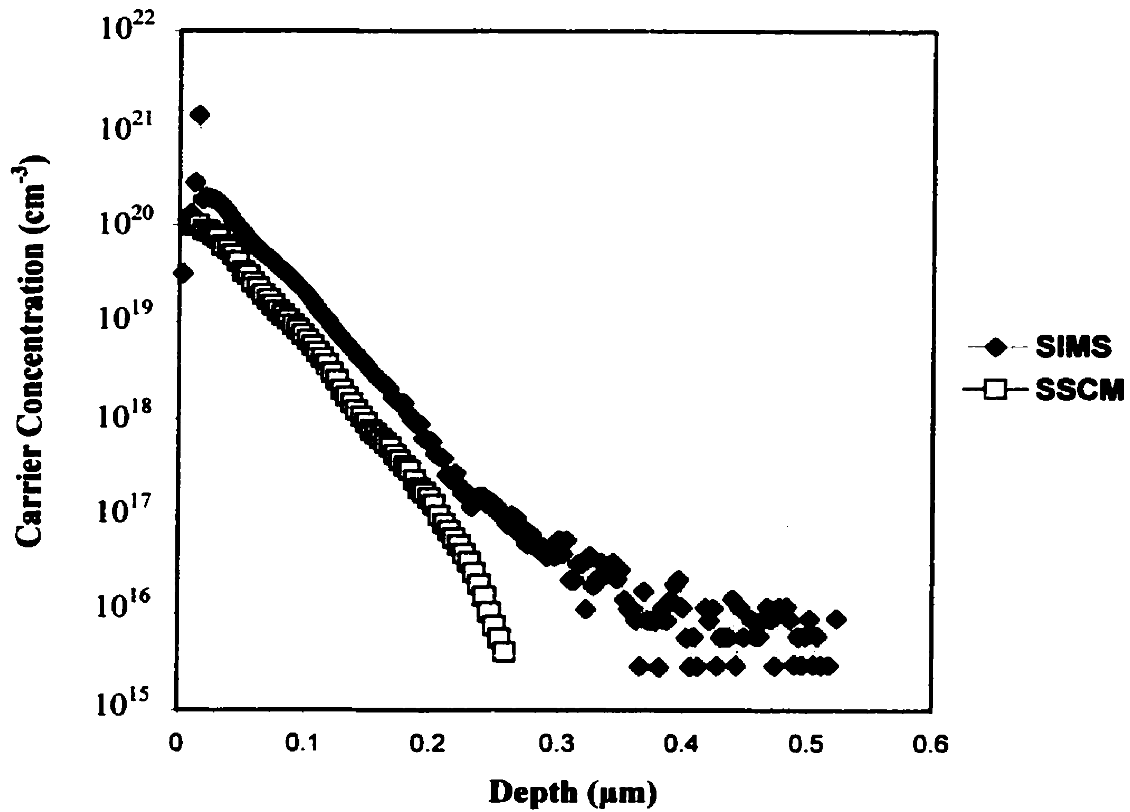


Figure 6.4 Comparison between 1D carrier concentration profiles obtained from SIMS and SSCM measurements on the 400 nm MOSFET. Data used for this conversion was taken across the source/drain regions of the device shown in Figure 5.7a

6.3 Conclusions And Recommendations

A discussion of the operating principle of the Schottky Scanning Capacitance Microscope was presented. The instrument combines the AFM based instrument with the measurement of the Schottky contact depletion capacitance. As a result, both topographical and carrier profiles can be obtained simultaneously. From the experimental results presented in this thesis, several conclusions and recommendations were drawn:

1) The SSCM was capable of distinguishing between regions of different dopant type on a sample surface. The type of dopant is determined by the sign of the capacitance derivative *dC/dV*. Therefore, this technique is ideally used for pn junction delineation with high spatial resolution.

2) Within a region of a given dopant type, the SSCM technique has monotonic response for concentrations of 10^{14} to 10^{18} cm^{-3}. The experimental results show that the capacitance derivative *dC/dV* monotonically increases as the dopant density is increased from 10^{14} to 10^{18} cm^{-3} and decreases after that. As a result, this technique is more suitable for semiconductor carrier profiling on a moderately doped surface. When a tip is scanned over a moderate dopant gradient, the amplitude of the capacitance derivative *dC/dV* represents the doping concentration.

3) The SSCM is capable of performing two-dimensional carrier profiling on cross-sections of devices. 2D carrier profiling performed on real devices of a very large scaled integrated circuit (VLSI) has also been demonstrated. The measurement technique can be applied directly on the sample surface or its cross-section without any need for beveling.

4) The conversion of measured *dC/dV* data to carrier concentration in one-dimension and two-dimensions was demonstrated. Although the conversion is not perfect, the use of calibration curves shows promise as a conversion technique. It is recommended that a self-contained calibration sample should be used instead of separated standard samples to eliminate systematic errors associated with changes in sample surface conditions.

The conversion technique should be refined or a more accurate model should be established to extract doping concentration from the capacitance measurements so that better results can be obtained.

5) Since the spatial resolution of this measurement is primarily limited by tip size, using a sharper conductive tip should improve the results of carrier profiling.

6) The sample preparation method used for the SSCM technique is simple and can be done in a short period of time. Since the measurements are performed in an air environment, they should be performed as soon possible after polishing to avoid a change in surface condition due to contamination by oxide and other materials. The experiments should be performed in a vacuum environment to minimize the surface contamination so that the sample surface can be repeatedly scanned over a longer period of time.

7) The capacitance sensor used for contact capacitance measurements was built and tested in our laboratory. During normal operating conditions, the overall sensitivity of the sensor was about 2×10^{-21} F/$\sqrt{Hz}$ with the RF voltage on the SSCM tip at less than 500 $mV_{p\text{-}p}$. The sensitivity can be influenced by the sample geometry. In one of the best cases, a sensitivity of 1×10^{-21} F/$\sqrt{Hz}$ was achieved [97]. Experimental results show that applying a large RF voltage on the tip may produce an artificial effect in a measured capacitance image. To avoid this effect, the RF voltage on the tip should be kept below 500 $mV_{p\text{-}p}$.

The sensitivities determined for the SSCM sensor may be compared to sensitivities reported for the RCA sensor [99]. The best reported data for the unloaded RCA sensor is 2.1×10^{-21} F/$\sqrt{Hz}$, while the corresponding loaded sensitivity is reported as 4.5×10^{-21} F/$\sqrt{Hz}$. While the SSCM instrument appears to provide at least a twofold improvement in sensitivity compared to the RCA sensor, it should be recognized that this comparison has not been undertaken with the same sense voltages, and same sample surface condition . As the SSCM sensor is different to the RCA sensor design, one of the initial goals was to match the

performance of the RCA sensor to the SSCM instrument using lower sense voltages. It was believed that operating at higher frequencies might enhance the SSCM instrument sensitivity. These aims have been achieved.

APPENDIX A

In this appendix, various components of the Schottky Scanning Capacitance Microscope are described. Those components include a deflection detection sensor, and a piezoelectric tube scanner. A method of calibration for the piezoelectric scanner is also presented.

A.1 Deflection Detection Schemes

May different methods have been developed for detecting the minute deflection of the cantilever [65]. Deflection detection schemes are characterized by their resolution, dynamic range, and ease of implementation. The desired characteristics in a deflection detection method should be high resolution, large dynamic range, good stability, and that it does not interfere with the operation of the cantilever.

In the past, the tunneling deflection detection technique had been implemented by placing a STM tip stationary above the back of a conducting cantilever [61]. The deflection of the cantilever was monitored by detecting the tunneling current between the STM tip and the cantilever. Since the tunneling current increases exponentially with decreasing separation, this method has the advantage of being very sensitive. This technique is excellent as far as resolution is concerned, however its performance depends on the quality of the tunneling current and suffers from the "1/f" noise inherent in the detected current. The capacitive deflection detection method [42] works similarly to the tunneling detection method. In this technique, the coupling capacitance between two tips is detected instead of a tunneling current. The method is very sensitive to movement of the scanning tip. In addition, it is also very sensitive to extraneous movement in the environment where the measurements take place.

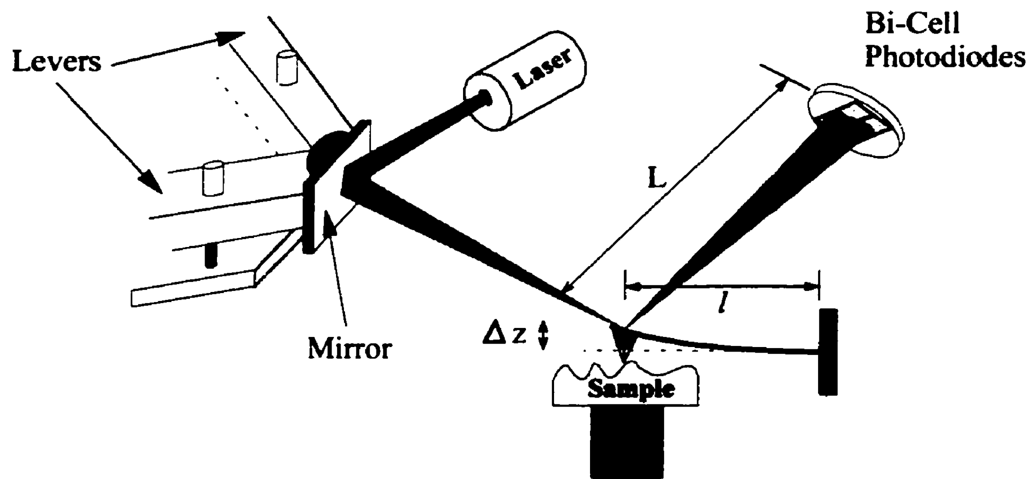


Figure A.1 A schematic drawing of a beam bounce detection system

For the SSCM measurements, both of these methods described above should not be used because the coupling capacitance between the two tips can interfere with the measurements of the depletion-layer capacitance. For this reason, the optical beam deflection scheme has been used for our SSCM microscope. Figure A.1 is shows the optical beam bounce deflection sensor that is currently used. The deflection sensor consists of a laser source, a mirror, and a photodetector. The mirror is mounted on the levers so that its orientation can be adjusted such that the reflection of the incident laser beam is positioned on the upper side of the cantilever. The reflection of the laser beam bouncing off the cantilever is then focused onto the face of a bi-cell photodetector. The photodetector is made up of two photo diodes placed side-by-side with a small separation gap. The output of the photodetector depends on the position of the laser spot falling on the photodiodes. The photodetector will output zero voltage if the laser spot is equally divided between these two cells. When the cantilever is deflected vertically, it changes the path of the laser beam reflecting from the cantilever. The deflection of the beam produces an inequality of the optical power in the bi-cells, resulting in a current generation at the output of the photodetector. The magnitude of generated current as a function of the cantilever deflection Δz and is given by [66]:

$$I = \frac{3\sqrt{2}\,NqL}{r_o\, l\sqrt{\pi}}\Delta z \quad \text{(Amps)} \qquad \textbf{(A.1)}$$

where q is the electronic charge, N represents the total number of photons in the beam falling on the detector per unit time, l and L are defined in Figure A.1, r_0 is the laser spot radius assuming that it is circularly-shaped (see Figure A.2), Δz is amount of vertical deflection of the cantilever, and I is the difference current between two cells ($I = I_A - I_B$ in which I_A and I_B are the currents generated by cellA and cellB respectively.). Equation A.1 tells us that the resulting signal can be increased by: using a shorter cantilever l, increasing the length of the laser beam reflected from the cantilever L and decreasing the radius of the laser spot. Decreasing the spot size of the laser is limited by diffraction. The sensitivity of the beam bounce detection technique has been reported to be $7.9\text{x}10^{-6}$ nm/$\sqrt{Hz}$ [67].

Normally, the generated current from each photo cell is converted to voltage by a current to voltage converter. The converted voltages are sent to a differential amplifier and a summing circuit simultaneously as shown in Figure A.2. The summing circuit in this case does not perform any special function. It only serves to tell an operator that the laser beam is properly positioned to the photodetector. The output of the differential amplifier is used as a feedback signal to maintain constant force between a tip and a sample during scanning process. This task is carried out within the SPM digital controller by comparing the feedback signal with a set point. If any error between these two signals is found, the SPM controller will adjust the height of the sample via a piezo tube to minimize the error. The amount of force initially loaded on the tip is determined by a selected set point. Before loading the tip on the sample surface, the photodetector should be positioned so that the output of the differential amplifier is zero and the output of the summing circuit is maximal.

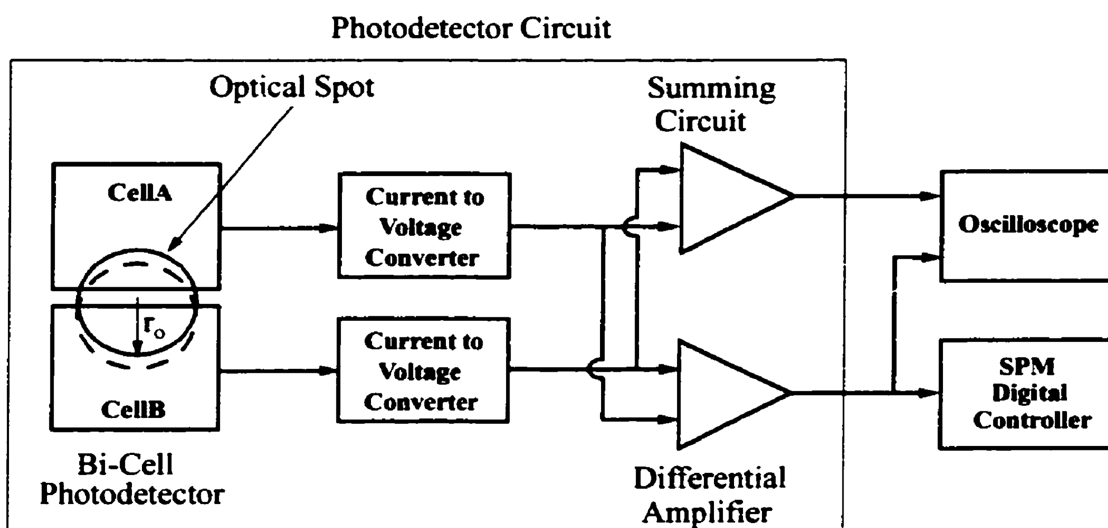


Figure A.2 A schematic circuit of a bi-cell photodetector

A.2 Piezoelectric Scanner

In all SPMs a probe is scanned relative to the sample under examination. In order to achieve the fine movements required by these microscopes, piezoelectric actuators are used. Piezoelectric materials deform or bend when a voltage is applied across them. These devices are widely used as electromechanical transducers to obtain minute movements and for micropositioning. There are two types of piezoelectric actuators that have been commonly used in SPMs applications. These are tripod actuators and piezoelectric tubes. Tripods are made up of three separate piezos glued together in an orthogonal fashion to provide motion in three dimensions X, Y, and Z. The motion inside the plane of the sample surface or perpendicular to the probe-to-sample separation axis is usually labelled X and Y, while Z refers to the motion along the probe-to-sample distance axis. A scanning tip is normally attached to the tripods at the point where three piezos are joined. The motion of the tip is controlled by applying voltages to the piezos which expand or contract along their own axis. This arrangement is mechanically complex, and suffers from various undesired

characteristics such as low mechanical resonances, large crosstalk between piezo rods, and small scan range.

Our SSCM utilizes a piezoelectric tube scanner. This device is a hollow cylinder of piezoelectric material with a single electrode on the inner wall and four symmetrical longitudinal electrodes on the outer wall as shown in Figure A.3. This tube is machined from a solid piece of piezoelectric material, metallized to form electrodes. The tube is sectored into five electrodes to give orthogonal X, Y and Z motion. The Z electrode is a solid electrode that is formed the inner wall of the tube. The outside of the tube is partitioned into four quadrants along the length of the tube. Two opposite quadrants are used as the positive and negative X electrodes, and the other two are used for the Y electrodes (see Figure A.3(b) for the arrangement of these electrodes). Movement is achieved by applying voltages to these electrodes.

Piezoelectric materials are characterized by their ability to expand or contract when under the influence of an electric field. Their movement can be approximated by a linear relation d = KV although in practice they are both nonlinear components and hysteresis. Here,

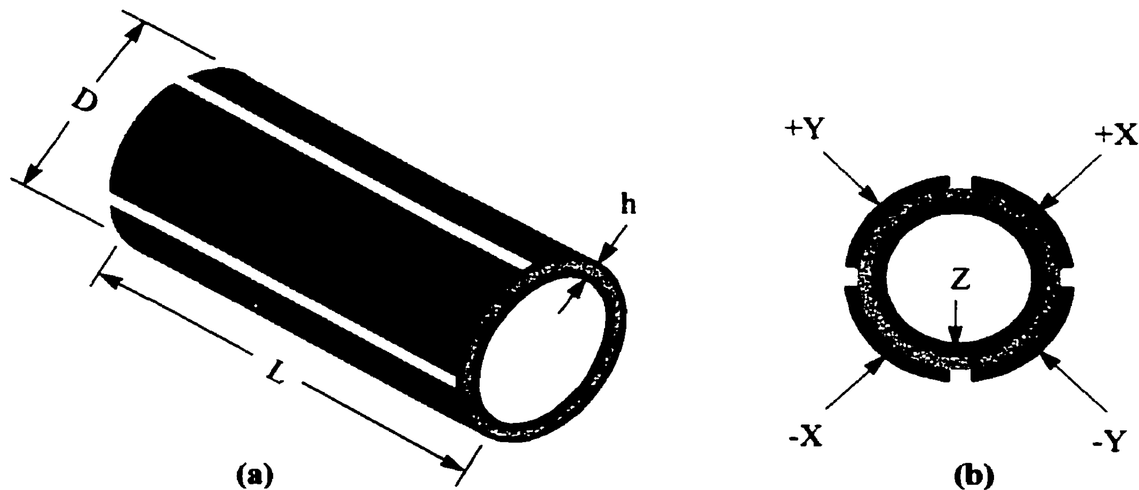


Figure A.3 A drawing of a piezoelectric tube scanner
(a) A pictorial view of the piezo tube and its physical parameters
(b) A cross-section view shows five electrodes

"d" is the distance moved by the piezoelectric material, V is the applied voltage, and K is the piezo constant. When a piezo tube is fixed at one end and two voltages, equal in magnitude and opposite in sign, are applied on the two opposite electrodes with the others grounded (i.e. $\pm V$ are applied on $\pm X$ electrodes respectively), the piezoelectric constant is given by [68]:

$$K_x = \frac{2\sqrt{2}\, d_{31} L^2}{\pi D h} \qquad \textbf{(A.2)}$$

where d_{31} is a relevant piezoelectric coefficient, L is the length of the tube, h is the tube's wall thickness, and D is the inner diameter of the tube assuming that the wall thickness is much smaller than the diameter. For a piezo with a thicker wall, the average of the inner diameter and outer diameter can be used for D. Due to symmetry, the piezo constant in the Y direction K_y is equal to K_x. Similarly, the piezo constant in Z direction K_z is given by:

$$K_z = \frac{L}{h} d_{31} \qquad \textbf{(A.3)}$$

The piezoelectric tube used for SSCM is the one purchased from Staveley NDT company, and its dimensions are: L = 25.40 mm, h = 0.51 mm, D = 5.84 mm, and d_{31} = 2.62 nm/V. Substituting these parameters into equations (A.2) and (A.3), the piezo constants can be calculated as:

$$K_x = K_y = 51.1 \text{ nm/V}$$

$$K_z = 13.0 \text{ nm/V}$$

With ± 200 V supplied by the SPM digital controller to the X,Y electrodes and 200V to the Z electrode, the motion ranges of the sample can be calculated to be 20.0 μm in the XY directions and 2.6 μm in the Z direction.

A.3 Calibration Of The Piezoelectric Scanner

The theoretical values of the piezo constants can be calculated using physical and mechanical properties of a particular piezo tube. Generally, when the SSCM is in operation a sample is mounted on the piezo. The X, Y, and Z displacements due to voltages applied to piezo tube may be different. Piezo tube calibration should be done in this case. There are two techniques that are commonly used to calibrate the piezo tube: 1) using an optical fiber interferometer [42], 2) imaging a diffraction grating of known structure. The latter technique was used and is presented in this section.

The grating that was used to calibrate the piezo X and Y axes was purchased from TED PELLA, Inc. This grating is made of silicon monoxide and has 2160 lines/mm crossed to form a square grid. Therefore, the side of each square can be calculated and is 463.2 nm. Figure A.4 shows a topographic image of the grating obtained using the SSCM in contact AFM mode.

Figure A.4 was taken with the piezo x and y-axis scan sizes set at 1500 x 1500 nm. Taking the separation distance between two adjacent lines to be 463 nm from center-to-center of these lines (shown as a double arrow line in Figure A.4), the true size of the image is estimated to be 1600 x 1600 nm. The true size and the size that was set for the piezo differed by about 7% in both x and y directions.

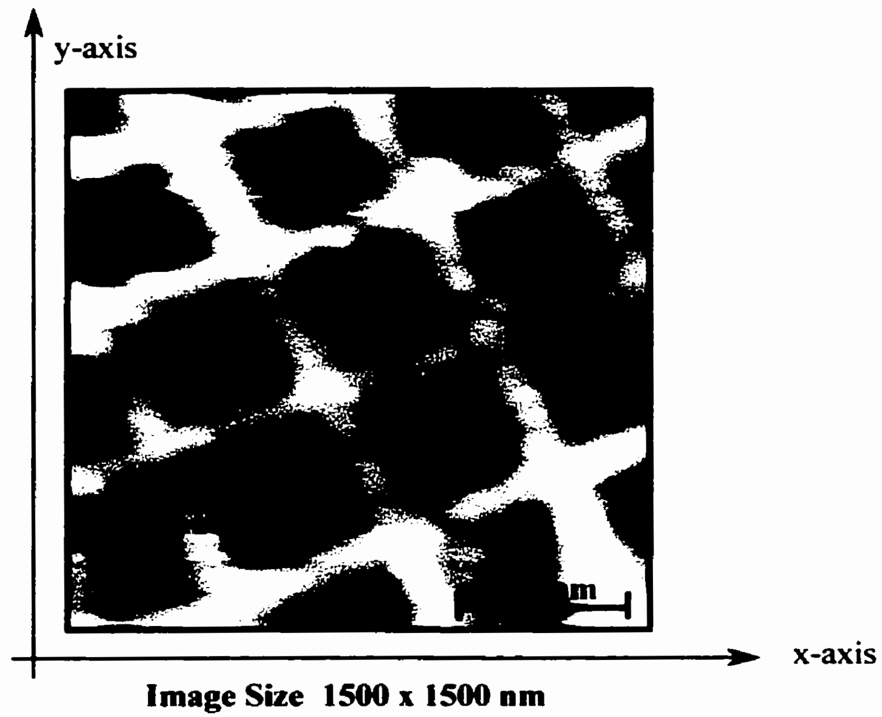


Figure A.4 A topographic image of a 463 nm diffraction grating

APPENDIX B

B.1 Current Transport Mechanisms

Current flows in a Schottky barrier because of charge transport from the semiconductor to the metal or in reverse direction. As shown in Figure B.1, there are four different mechanisms by which carrier transport can occur under forward bias (assuming a metal-n-type semiconductor junction) These mechanisms are known as: (a) thermionic emission over the barrier, (b) tunneling through the barrier (field emission), (c) carrier recombination (or generation) in the depletion region, (d) carrier recombination in the neutral region (equivalent to the minority carrier injection).

At zero bias, the depletion region of the Schottky barrier is in thermal equilibrium, and the rate of electron-hole pair generation in this region is balanced by the rate of recombination. In addition, the Schottky diode is a majority carrier device for not too high values of the forward bias [70]. The contribution to the total current flow of the processes (c) and (d) is expected to be small and can be neglected.

It is assumed that the current transport governed by mechanisms (a) and (b) act in parallel. The magnitude of current flow across the junction depends on several factors such as doping concentration, temperature, type of metal-semiconductor junction (barrier height). From equation 3.12, one can see that the depletion width becomes thinner if the doping concentration is increased. The thinner the depletion width, the greater the probability of charge carriers tunneling between the metal and semiconductor. For a fixed barrier height and at room temperature, the current flow between the tip and the sample should increase as the dopant concentration is increased. This is assumed that the barrier height of the metal-semiconductor contacts is constant and does not change with dopant concentration because of surface states.

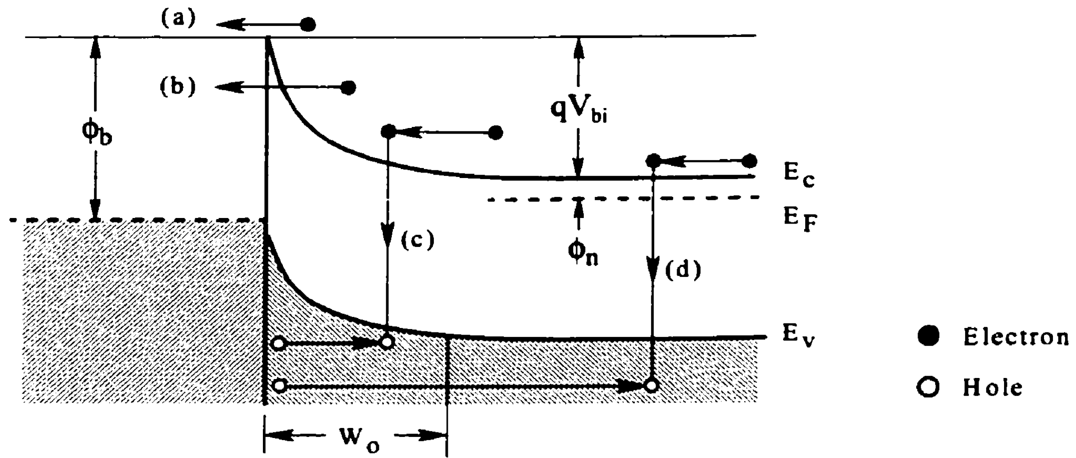


Figure B.1 Energy band diagram of a forward biased Schottky barrier on an n-type semiconductor showing different transport processes.

B.2 Thermionic Emission Over the Barrier

Thermionic emission is a process in which charge carriers are thermally excited over the metal-semiconductor energy barrier. The current density of charge carriers across a metal-semiconductor junction is governed by the conventional diode equation:

$$J_{TE} = J_s\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad \textbf{(B.1)}$$

$$J_s = A^* T^2 \exp\left(-\frac{q\phi_b}{kT}\right) \quad \textbf{(B.2)}$$

where J_S is the saturation current density at zero bias, V is the bias voltage applied across the junction (positive for forward bias), n is the ideality factor of the diode, k is the Boltzmann's constant, T is the temperature, ϕ_b is the barrier height of the metal-semiconductor contact, and A^* is the effective Richardson constant for thermionic emission. The value of A^* depends on the effective mass of the charge carrier (A^* = 112 for n-type Si, A^* = 32 for p-type Si) [70].

Equations (B.1) and (B.2) show that the thermionic emission current depends on the external bias voltage and the barrier height (or the type of metal-semiconductor). However, it does not depend on the dopant concentration of the semiconductor (this is assuming that the barrier height is a constant and does not change with doping).

B.3 Tunneling through the Barrier (Field Emission)

Besides thermionic emission mechanisms, charge carriers can also be transported across the barrier by quantum mechanical tunneling. Since the width of the Schottky barrier becomes narrower with increasing dopant concentration, the magnitude of current tunneling through the barrier depends on the dopant concentration of the semiconductor. The bias dependence of the field emission current density for a metal-semiconductor barrier at low temperature is given by:

$$J_{FE} = J_s\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad \textbf{(B.3)}$$

$$J_s = A^* T^2\left(\frac{qE_{00}}{kT}\right)^2\left(\frac{\phi_b - V}{\phi_b}\right)\exp\left(-\frac{2\phi_b^{3/2}}{3E_{00}\sqrt{\phi_b - V}}\right) \qquad \textbf{(B.4)}$$

where, again, J_S is the saturation current at zero bias, V is the external bias voltage (positive for forward bias), ϕ_b is the barrier height, and A^* is the effective Richarson constant. E_{00} is given by:

$$E_{00} = \frac{2}{\alpha}\sqrt{\frac{N_D}{2\varepsilon_s}} \qquad \textbf{(B.5)}$$

and

$$\alpha = \frac{4\pi\sqrt{2m^*}}{h} \qquad \textbf{(B.6)}$$

where "h" is Planck's constant, ε_s is the dielectric permittivity of the semiconductor ($\varepsilon_s = 11.9\varepsilon_o$), N_D is the semiconductor dopant concentration and m^* is the effective mass of the charge carrier. For silicon, the effective mass is direction dependent. For n-type silicon, It is approximately to be $2.05m_e$ for the <100> direction and $2.15m_e$ for <111> directions. For p-type silicon, $m^* = 0.66m_e$ and m_e is the mass of an electron [69]. Equations (B.4) and (B.5) tell us that the field emission current is sensitive to the semiconductor dopant concentration.

APPENDIX C

C.1 Development of an Impedance Matching Network

Matching the impedance of a Schottky diode over a wide bandwidth can present a challenge to the designer, especially for diodes with a high value of junction resistance. However, a general design approach for narrow bandwidths is straightforward. For a narrow frequency band, the impedance matching network for a zero-bias Schottky diode can be constructed using short-circuited stub transmission lines. In this section, a narrow band, microstrip matching network using short-circuited stubs is presented. These short-circuited stubs are also necessary to provide the return path for current generated in the diode.

The input impedance of the detector must be matched to the source impedance to maximize the power transfer. However, the impedance of the resonator in our case is not always constant, as it depends on the interaction between the tip and the sample. For testing purposes, the matching network will be designed to transform the diode's impedance to 50 Ω looking into its input port. The design approach, however, may be applied to match the diode's impedance to a different value with an appropriate modifications. Figure C.1 shows a microstrip matching network for our detector

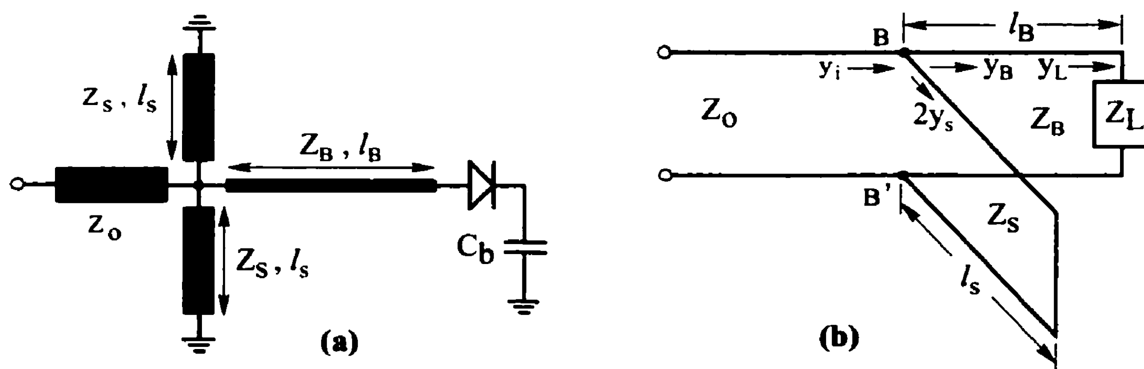


Figure C.1 An impedance matching network using transmission line stubs
(a) A microstrip configuration
(b) An equivalent circuit of (a)

using short-circuited stubs. The network consists of four transmission line sections: an input transmission line that has a characteristic impedance $Z_O = 50\ \Omega$, two short-circuited transmission line stubs each has a characteristic impedance Z_S and length l_s, and a last section that is a transmission line with characteristic impedance Z_B and length l_B connecting the matching network to the diode (see Figure 4.31a). Figure 4.31b is an equivalent circuit of the detector in which Z_L represents the diode's impedance (including a bypass capacitor) looking into the diode's input terminal. To complete a matching network, the length of the stubs "l_S" and the distance from the load "l_B" are required such that the impedance of the parallel combination to the right of points B-B' is equal to Z_O, the characteristic impedance of the input line. In the other words, the basic requirement is $Y_i = Y_B + 2Y_s = Y_o$, where $Y_o = 1/Z_o$ is the admittance of the input line. In terms of normalized admittances, the requirement becomes $1 = y_B + 2y_s$, where $y_B = Z_o Y_B$ is for the load section and $y_s = Z_o Y_s$ is for the short-circuited stub. Since the input admittance of a short-circuited stub is purely susceptive, y_s is purely imaginary, and the equation $1 = y_B + 2y_s$ can be satisfied only if:

$$y_B = 1 + jb_B \qquad \text{(C.1a)}$$

$$2y_s = -jb_B \qquad \text{(C.1b)}$$

From the equivalent circuit in Figure 4.31b, the normalized input admittance y_B for the load section to the right of points B-B' can be expressed in terms of the normalized impedance of the load $z_L = r_L + jx_L$, where $z_L = Z_L/Z_o$ are as follows:

$$\begin{aligned} y_B &= \frac{1}{k1}\left[\frac{(k1 - x_L t) + jr_L t}{r_L + j(x_L + k1 t)}\right] \\ &= g_B + jb_B \end{aligned} \qquad \text{(C.2)}$$

where $k1 = Z_B/Z_o$ is the normalized impedance of the load section transmission line, and:

$$t = \tan\beta l_B \qquad \text{(C.3)}$$

The real part g_B and imaginary part b_B of equation (C.2) are given by:

$$g_B = \frac{1}{k1}\left[\frac{r_L(k1 - x_L t) + r_L t(x_L + k1 t)}{r_L^2 + (x_L + k1 t)^2}\right] \quad \textbf{(C.4a)}$$

$$b_B = \frac{1}{k1}\left[\frac{r_L^2 t - (k1 - x_L t)(x_L + k1 t)}{r_L^2 + (x_L + k1 t)^2}\right] \quad \textbf{(C.4b)}$$

It should be noted that a perfect match requires the simultaneous satisfaction of equation (C.1a) and equation (C.1b). Equating g_B in equation (C.4a) to unity, "t" can be solved in terms of the other parameters:

$$t = \begin{cases} \frac{1}{r_L - k1^2}\left[k1 x_L \pm \sqrt{r_L(r_L - 1)(r_L - k1^2) + x_L^2}\right] & if\ r_L \neq k1^2 \\ \frac{k1^2(1 - k1^2) - x_L^2}{2x_L k1} & if\ r_L = k1^2 \end{cases} \quad \textbf{(C.5)}$$

The required length l_B can be found from equations (C.3) and (C.5) for each value of "t" as:

$$l_B = \begin{cases} \frac{\lambda}{2\pi}\tan^{-1}(t) & if\ t \geq 0 \\ \frac{\lambda}{2\pi}[\tan^{-1}(t) + \pi] & if\ t < 0 \end{cases} \quad \textbf{(C.6)}$$

For the short-circuited stub, the normalized input admittance y_s is given by:

$$y_s = -j\frac{1}{k2\tan\beta l_s} \quad \textbf{(C.7)}$$

$$k2 = Z_s/Z_o$$

Similarly, combining equations (C.1b), (C.4b), (C.5), and (C.7), the required length l_s can be calculated for each value of "t":

$$l_s = \begin{cases} \dfrac{\lambda}{2\pi}\tan^{-1}\left(\dfrac{2}{(k2)\,b_B}\right) & if\ b_B \geq 0 \\ \dfrac{\lambda}{2\pi}\left[\tan^{-1}\left(\dfrac{2}{(k2)\,b_B}\right) + \pi\right] & if\ b_B < 0 \end{cases} \tag{C.8}$$

where λ is the wavelength of the propagating signal at the operating frequency. For a microstrip structure, the wavelength λ of the propagating signal can be calculated by the expression

$$\lambda = \frac{c}{f_o\sqrt{\varepsilon_{re}}} \tag{C.9}$$

where c is the speed of light in free space, f_o is the operating frequency, and ε_{re} is the effective dielectric constant of the medium in which the signal is propagated. The effective dielectric constant can be calculated using equation (4.45).

In this design, the characteristic impedance of the load section microstrip transmission line was 100 Ω while the characteristic impedance of the short-circuited stubs was 50 Ω. The microstrip substrate used for the detector is the same as the one used for the resonator (h = 1.575 mm and $\varepsilon_r = 2.5$). The width of these microstrip transmission lines was calculated using equation (4.43). Also, the operating frequency that was chosen for calculation of transmission lines that made up the matching network is 1.85 GHz. This is a typical operating frequency of the sensor when the tip is loaded. Using equations (C.4) to (C.9) and parameters of the Schottky diode model HP HSMS-2850, the elements of the matching network for each value of "*t*" were computed and they are summarized as given below:

<u>For first value of "*t*"</u>

W_i = 4.47 mm   width of the input transmission line

W_S = 4.47 mm   width of the short-circuited stub

W_B = 1.27 mm   width of the load section transmission line

l_s = 7.41 mm	length of the short-circuited stub

l_B = 21.38 mm	length of the load section of the transmission line

For second value of "t"

W_i = 4.47 mm	width of the input transmission line

W_S = 4.47 mm	width of the short-circuited stub

W_B = 1.27 mm	width of the load section transmission line

l_s = 48.78 mm	length of the short-circuited stub

l_B = 25.25 mm	length of the load section of the transmission line

C.2 Frequency Synthesizer Circuit (Oscillator)

Figure C.2 shows a schematic of a standard frequency synthesizer (oscillator circuit board) that is given in [98]. It consists of a crystal oscillator, a phase-lock-loop (PLL), a lock detector circuit, a loop filter, an operational amplifier, and a voltage controlled oscillator (VCO) to form a closed loop system. Frequency synthesis is accomplished by using a National Semiconductor integrated circuit type LMX2325 that can be used for RF operation up to 2500 MHz. Any similar integrated synthesizer chip may also be used. The voltage controlled oscillator (VCO) is Mini-Circuit POS-2000 that operates from 1300 MHz to 2000 MHz. In this closed loop system, a sample of the VCO output is sent back to the PLL and drives a divide-by-64 prescaler which in turn drives a programmable counter. The output of this counter internally

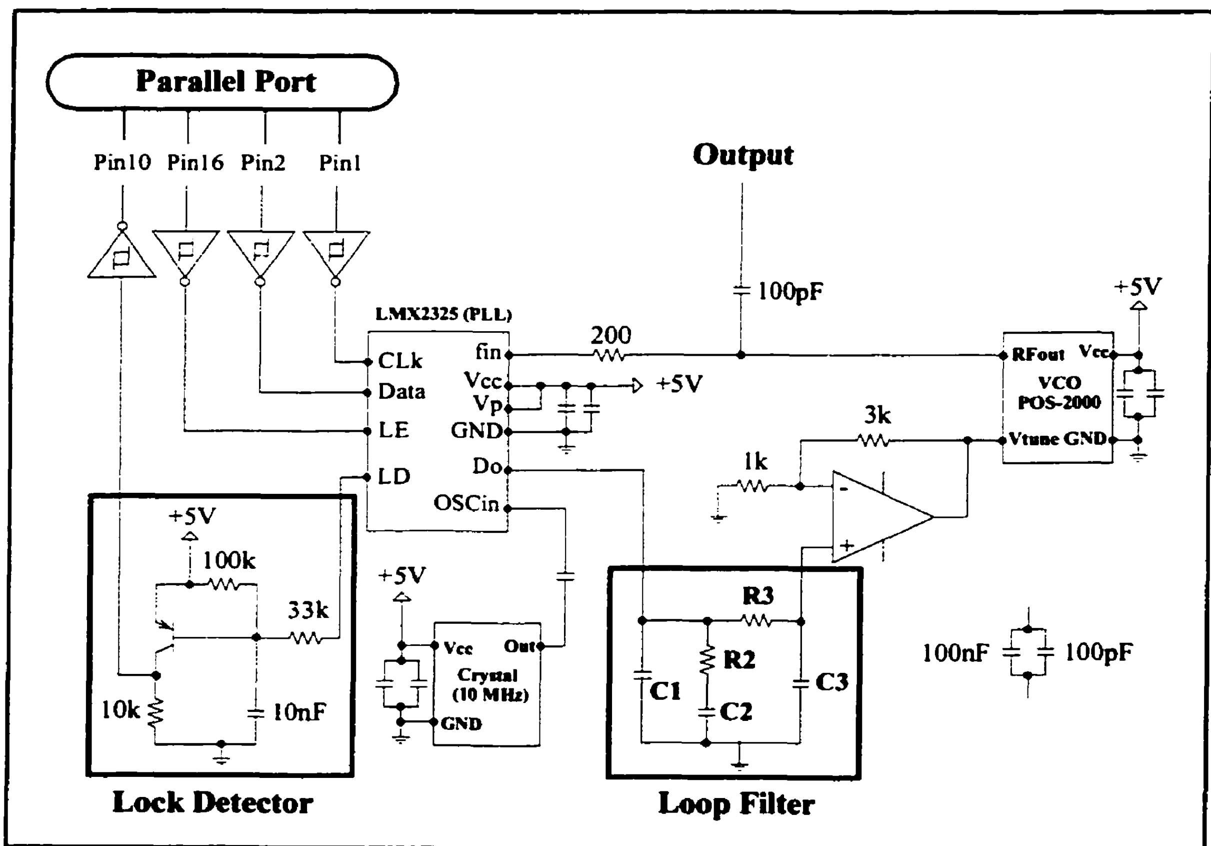


Figure C.2 The schematic diagram of an oscillator circuit

drives the phase detector. At the same time, the reference signal to the phase detector is obtained by dividing the reference signal by a constant via the reference counter. The reference signal is provided by an external 10 MHz crystal oscillator. It should be noted that all of these counters were located within the phase-lock-loop (PLL). The oscillator presented in this section was built such that the frequency of the output signal could be set by a user through a computer interface. During normal operation, a desired frequency is entered by an user from the keyboard. This data is sent to the oscillator circuit board via a parallel port and used to set divide ratios for both the reference counter and the programmable counter. These counters are programmed such that the crystal and VCO signals have same frequency (200 kHz for our oscillator). The output signals of these counters are sent to a phase detector for a phase comparison. When there is a phase error between the reference and the VCO signals, the phase detector outputs a series of current pulses corresponding to the frequency difference between the reference and VCO. The current pulses are filtered by a loop filter, amplified, and applied to the tuning port of the VCO to reduce the phase error, and therefore achieve phase lock. This process is continued until the phase error reduces to zero and at this stage the desired frequency is reached.

The voltage controlled oscillator used in this circuit is a wide band VCO. The tuning voltage needed for the VCO to operate at 2000 MHz ranges up to 20 V. However, the maximum DC voltage that can be output from the loop filter is 5 V for the use of LMX2325 (with 5V supply). Therefore, an operational amplifier with a gain of 4 is needed as shown in Figure C.2. The operational amplifier may be omitted if a narrow band VCO is used. Table C.2 gives the brief description of the circuit components that were used to construct an oscillator circuit. Most of the circuit elements are typical values used for most frequency synthesis applications except for the loop filter. These elements are determined by the characteristic of the VCO and the electrical properties of the PLL. They also depend on the divider ratios and the reference frequency that is set for the PLL **[98]**.

The parameters (C1, C2, C3, R2, and R3) of the third order loop filter (see Figure C.2) can be calculated as follows (full detail of the calculations can be found in the application note of **[98]** and are presented here as a reference). For a given loop filter shown in Figure C.2, the time constants which determine the pole and zero frequencies of the transfer function are

given by

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad \text{(C.11a)}$$

$$T2 = \frac{1}{\omega_c^2 (T1 + T3)} \quad \text{(C.11b)}$$

$$T3 = \sqrt{\frac{10^{ATTEN/20} - 1}{(2\pi f_{ref})^2}} \quad \text{(C.11c)}$$

From these time constants, C1 can be calculated and is given by

$$C1 = \frac{K_\phi K_{VCO} T1}{(N \omega_c^2)\, T2} \sqrt{\frac{1 + (\omega_c T2)^2}{[1 + (\omega_c T1)^2]\,[1 + (\omega_c T3)^2]}} \quad \text{(C.12)}$$

$$\omega_c = \frac{\tan\phi_p (T1 + T3)}{(T1 + T3)^2 + T1 T3} \left[\sqrt{1 + \frac{(T1 + T3)^2 + T1 T3}{[(T1 + T3)\tan\phi_p]^2}} - 1 \right]$$

where K_{VCO} is the VCO tuning voltage constant (the frequency versus voltage tuning ratio) that is expressed in (MHz/V), K_ϕ is the phase detector charge pump gain constant (expressed in mA), N is the main divider ratio that is defined as a ratio of the designed RF frequency to the reference frequency, f_{ref} is the reference frequency (expressed in kHz), ϕ_p is the phase margin that is defined as the difference between the phase of the filter transfer function at the unity gain point and -180°, ω_p is the loop bandwidth and is the frequency point at which the magnitude of the filter transfer function has unity gain, and lastly ATTEN is the side band attenuation factor. Once C1 is calculated, the C2 and R2 can be calculated using the expressions:

$$C2 = C1\left(\frac{T2}{T1} - 1\right) \quad \text{(C.13)}$$

$$R2 = \frac{T2}{C2} \tag{C.14}$$

Since the time constant T3 is defined as a product of C3 and R3, with the knowledge of T3 these parameters can be calculated if one is selected. For our oscillator, C1, C2, C3, R2, and R3 were calculated as:

K_{VCO} = 4x(45 MHz/V)

K_{ϕ} = 5 mA

RF_{opt} = 1850 MHz

F_{ref} = 200 kHz

N = RF_{opt} / F_{ref}

ω_p = 2π(20 kHz) Suggested value [98]

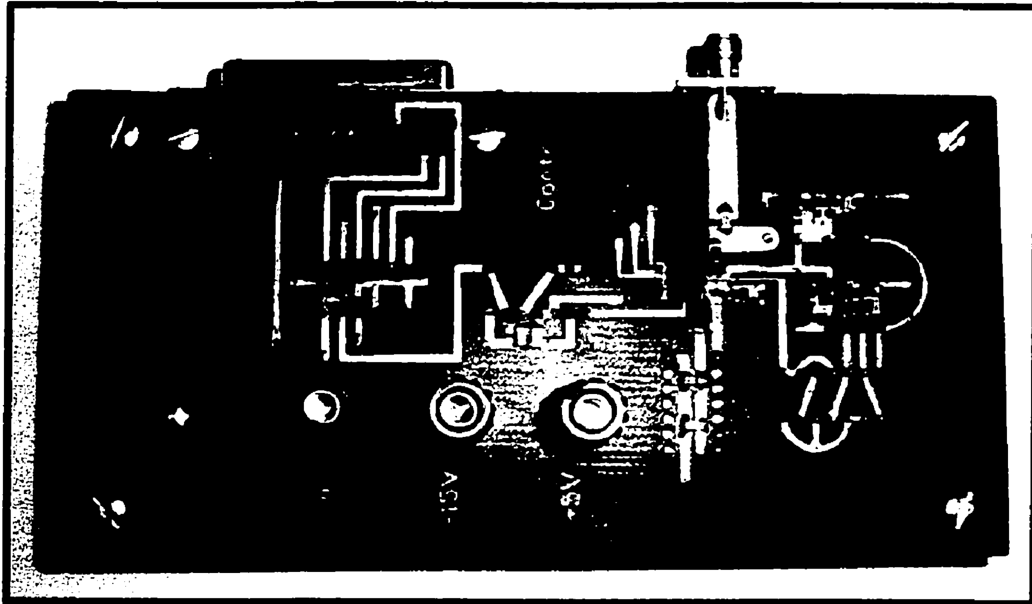
ϕ_p = 45° Suggested value [98]

ATTEN = 20 dB Suggested value [98]

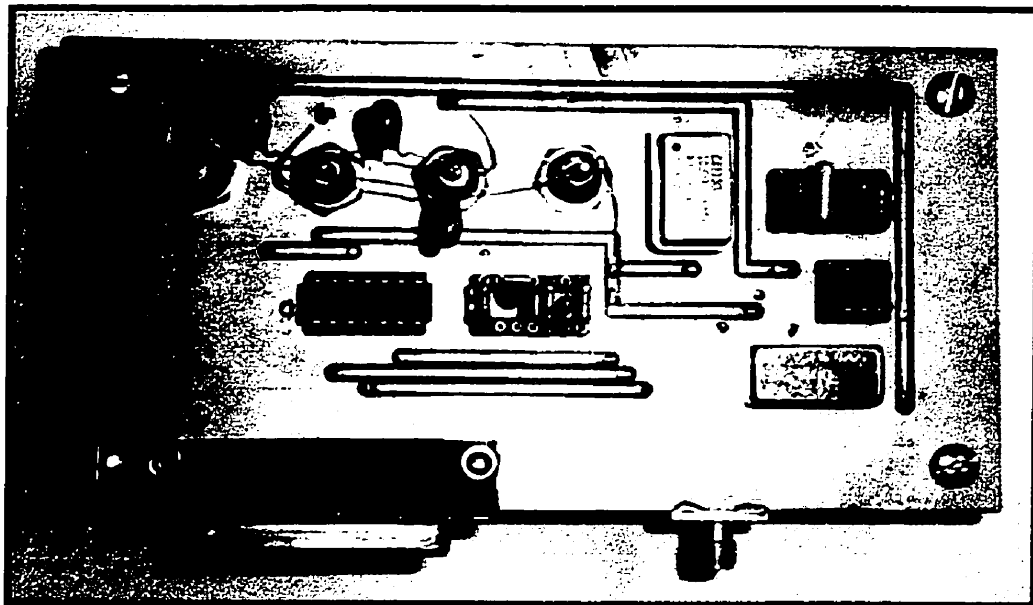
The calculated values of the loop filter are:

C1 = 4.7 nF
C2 = 47 nF
R2 = 770 Ω
By selecting C3 = 100 pF, R3 was calculated to be 23.7 kΩ

The oscillator circuit board was fabricated from copper-clad, low-loss dielectric substrate (ε_r = 2.5) and tested within our laboratory. It was capable of generating a sinusoidal signal with an output power of 6 - 7 dBm over a frequency band of 1300 MHz to 2000 MHz. The noise level at the oscillator output was about 1.0 - 1.5 $nV/\sqrt{Hz}$ measured in 1 Hz bandwidth at 90 kHz. Figure C.3 shows a photograph of the oscillator circuit.



(a)



(b)

Figure C.3 A photograph of 1300 MHz to 2000 MHz oscillator circuit
(a) Top view
(b) Bottom view

Table C.1: Function(s) Of Oscillator Circuit Components

Component	Function(s)
Computer	* Provides high level control of the oscillator board * Downloads low level serial data to the PLL (to set the divide ratio) * Informs user whether the frequency and phase are locked or unlocked
Crystal Oscillator	* Provides a stable reference frequency of known value (10 MHz)
Phase Locked Loop (PLL)	* Divides the reference and VCO frequencies by programmable amounts * Compares the phase of the two frequency-divided signals * Sources or sinks current if the reference leads or lags the VCO in phase
Lock Detect Circuitry	* Examines PLL signals to establish when the frequency and phase are locked
Loop filter	* Filters current pulses from the PLL to provide a voltage signal for the VCO * The voltage level is held steady, increased, or decreased according to the PLL output * Reduces the frequency noise of the VCO by attenuating high frequency fluctuations in the voltage level * Provides adequate phase margin to ensure stability of the closed loop system * Determines the lock time of the system
Voltage Controlled Oscillator (VCO)	* Converts a voltage level to a high frequency signal (GHz range) according to a monotonic, approximately linear relationship * The gain and input voltage range of the VCO can be adjusted by using an external amplifier
Parallel Port	* Means of communication between the computer and the oscillator board
Schmitt Triggered Inverter	* Eliminates noise and logic level problems in the communication pathway

APPENDIX D

In this appendix, an algorithm for 2D conversion that was used to convert measured *dC/dV* data to carrier concentration is presented. The algorithm was written for the Matlab software package. It should be noted that *dC/dV* data files are imported such that each row vector of the matrix contains the data that represents a line profile across the source/drain regions of the device. In addition, the imported image was oriented such that a MOSFET device's gate is located on the left hand side of the image. A new data file should be rotated or flipped, if necessary, such that its orientation is the same as described.

```
fid = fopen('P018_09C.inf','rt');          %%% Scan Information File
        n = 0;
        while 1
            if feof(fid) = = 1, break; end
          n = n + 1;
          [value,count] = fscanf(fid,'%f', 1);
          if (count = = 1), A(n,1) = value; end
          fscanf(fid,'%c',1);
        end
        fclose(fid);

Dim = round(A(11));
V_Max = A(15);
V_Min = A(16);
V_Abs = A(17);

fid = fopen('P018_09c.exp','r','ieee-le');  %%% Load dC/dV data file
Lock_in_Sen = 50;                           %%% Sensitivity set on Lock-In amplifier
Lock_in_Scale = Lock_in_Sen/10;
Scaler_C = Lock_in_Scale*V_Abs/(abs(V_Min)+abs(V_Max));
[Cap] = fread(fid,[256,256],'int16')*Scaler_C;
Cap = rot90(Cap);
Av = mean(mean(Cap(25:65,25:65)));   %%% Calculate average voltage on oxide layer
Cap = Cap - Av;

XY_Dim = Dim/1000;                          %%% X Or Y Dimension of an image in µm
Inc = XY_Dim/255;
X = 0:Inc:XY_Dim;
Y = 0:Inc:XY_Dim;

count = 0;
for i=1:256
       Min_Value = min(Cap(i,:));
       Min_point = find(Cap(i,:) = = Min_Value);
       if length(Min_point) > 1
          count = count + 1;
          Min_Value = Min_Value + 1E-6;
          Row(count,1) = i;
          Col(count,1:length(Min_point)) = Min_point;
          Cap(i,Min_point(2)) = Cap(i,Min_point(2)) + 1E-6;
    end
end

Image_Slope = 4.24E-3;  %%%  slope of resonant curve uses to obtain the current image
Max_Slope = 10.9E-3;   %%% Max slope of resonant curves uses to obtain calibration curves
Nom_Constant = Image_Slope/Max_Slope;  %%%--- Constant used for slope correction
```

```
P1 = -0.1000*Nom_Constant;  ND1 = 1.00E14;  n1 = log10(ND1);
P2 = -0.6129*Nom_Constant;  ND2 = 6.00E14;  n2 = log10(ND2);
P3 = -1.6717*Nom_Constant;  ND3 = 3.00E15;  n3 = log10(ND3);
P4 = -2.9287*Nom_Constant;  ND4 = 2.50E16;  n4 = log10(ND4);
P5 = -4.4501*Nom_Constant;  ND5 = 1.20E17;  n5 = log10(ND5);
P6 = -2.3234*Nom_Constant;  ND6 = 2.00E18;  n6 = log10(ND6);
P7 = -0.7250*Nom_Constant;  ND7 = 1.50E19;  n7 = log10(ND7);
P8 = -0.3500*Nom_Constant;  ND8 = 6.00E19;  n8 = log10(ND8);
P9 = -0.1500*Nom_Constant;  ND9 = 9.00E19;  n9 = log10(ND9);

Carrier = [ND1;ND2;ND3;ND4;ND5;ND6;ND7;ND8;ND9];
Lockin  = [P1;P2;P3;P4;P5;P6;P7;P8;P9];

Cal_Curve_Max = [Carrier,Lockin];
Min_Cal = min(Cal_Curve_Max(:,2));
Max_Cap_Signal = max(max(Cap))
Min_Cap_Signal = min(min(Cap))
Con_Factor = abs(min(Cal_Curve_Max(:,2))/Min_Cap_Signal);
Cap_Scale_Down = Cap*Con_Factor;
Min_Cal_Point = zeros(1,256);
Cal_Curve = Cal_Curve_Max;

for i=1:256

        Min_Value = min(Cap_Scale_Down(i,:));
        Min_Point = find(Cap_Scale_Down(i,:) = = Min_Value);
        Convert_Point = (1.875 - 1.525)*X(i) - 1.875;
        Cal_Curve(:,2) = Cal_Curve_Max(:,2)*(Convert_Point/Min_Cal);
        Min_Cal_Point(i) = min(Cal_Curve(:,2));

   for j=1:256
      Test_Min_Point = Cap_Scale_Down(i,j);

      if j >= Min_Point

         if Test_Min_Point <= Cal_Curve(1,2) & Test_Min_Point >= Cal_Curve(2,2)
            Slope = (n1 - n2)/(Cal_Curve(1,2)-Cal_Curve(2,2));
            Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(1,2)) + n1;
         elseif Test_Min_Point < Cal_Curve(2,2) & Test_Min_Point >= Cal_Curve(3,2)
            Slope = (n2 - n3)/(Cal_Curve(2,2)-Cal_Curve(3,2));
            Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(2,2)) + n2;
         elseif Test_Min_Point < Cal_Curve(3,2) & Test_Min_Point >= Cal_Curve(4,2)
            Slope = (n3 - n4)/(Cal_Curve(3,2)-Cal_Curve(4,2));
            Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(3,2)) + n3;
         elseif Test_Min_Point < Cal_Curve(4,2) & Test_Min_Point >= Cal_Curve(5,2)
            Slope = (n4 - n5)/(Cal_Curve(4,2)-Cal_Curve(5,2));
```

```
                Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(4,2)) + n4;
            else
                Map_Signal(i,j) = 13;
            end
        else
            if Test_Min_Point > Cal_Curve(5,2) & Test_Min_Point <= Cal_Curve(6,2)
                Slope = (n5 - n6)/(Cal_Curve(5,2)-Cal_Curve(6,2));
                Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(5,2)) + n5;
            elseif Test_Min_Point > Cal_Curve(6,2) & Test_Min_Point <= Cal_Curve(7,2)
                Slope = (n6 - n7)/(Cal_Curve(6,2)-Cal_Curve(7,2));
                Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(6,2)) + n6;
            elseif Test_Min_Point > Cal_Curve(7,2) & Test_Min_Point <= Cal_Curve(8,2)
                Slope = (n7 - n8)/(Cal_Curve(7,2)-Cal_Curve(8,2));
                Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(7,2)) + n7;
            elseif Test_Min_Point > Cal_Curve(8,2) & Test_Min_Point <= Cal_Curve(9,2)
                Slope = (n8 - n9)/(Cal_Curve(8,2)-Cal_Curve(9,2));
                Map_Signal(i,j) = Slope*(Test_Min_Point - Cal_Curve(8,2)) + n8;
            else
                Map_Signal(i,j) = 20;
            end
        end
    end
end

figure
set(gcf,'Position',[0 0 400 400])
set(gca,'Position',[0.18 0.18 0.72 0.64])
mesh(X,Y,Cap)
xlabel('X-Scan In (um)')
ylabel('Y-Scan In (um)')
title('Capacitance Image (Raw Data)')
axis([0 XY_Dim 0 XY_Dim min(min(Cap_Scale_Down)) max(max(Cap_Scale_Down))])
view(0,90)
colormap(jet)
colorbar
figure
set(gcf,'Position',[0 400 400 400])
set(gca,'Position',[0.18 0.18 0.72 0.64])
mesh(X,Y,Map_Signal)
xlabel('X-Scan In (um)')
ylabel('Y-Scan In (um)')
title('Capacitance Image (Carrier Density)')
axis([0 XY_Dim 0 XY_Dim min(min(Cap_Scale_Down)) max(max(Cap_Scale_Down))])
view(0,90)
colormap(jet)
colorbar
```

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