Modelling of Custom Power Devices on an Electromagnetic Transients Program

By

Leena Palav

A Thesis

Submitted to the Faculty of Graduate Studies
in partial fulfillment of the requirements for the degree of

Master of Science

The Department of Electrical and Computer Engineering

The University of Manitoba
Winnipeg, Manitoba, Canada

THE UNIVERSITY OF MANITOBA

FACULTY OF GRADUATE STUDIES

*****

COPYRIGHT PERMISSION PAGE

MODELLING OF CUSTOM POWER DEVICES ON AN ELECTROMAGNETIC TRANSIENTS PROGRAM

BY

LEENA PALAV

A Thesis/Practicum submitted to the Faculty of Graduate Studies of The University of Manitoba in partial fulfillment of the requirements of the degree of

MASTER OF SCIENCE

Acknowledgements

To Dr. Gole, my supervisor. It has been a rare pleasure to interact with your energetic and dynamic personality. Your vast range of knowledge, your amazing insights helped me resolve many a glitch in this thesis.

And to Anurag Thakur, my fiance and my closest friend .

Thanks are due to the HVDC Centre for funding this thesis and very much due to Rohitha and Ioni of the Centre for bearing my numerous queries with calm fortitude.

I would also like to express my gratitude to Dr. Menzies. Sir, you have been a very inspiring presence in my life here.

Abstract

Custom Power Devices comprise a group of power electronic controllers that seek to improve the level of quality of power available to the customer. Novel configurations using semiconductor switching devices can be designed to mitigate power quality problems such as voltage sags, harmonics and voltage flicker in distribution systems.

This thesis deals with the modelling of Custom Power topologies in the electromagnetic transient simulation programme PSCAD/EMTDC™. Several configurations of Solid State Breakers and Dynamic Voltage Restorers have been studied and their control logic designed, using this simulation tool. The results of various tests have been enumerated in this thesis and it is shown that dynamic power electronic controllers can be designed to provide high quality of power to sensitive loads. These Custom Power models can now be used for detailed system studies at the distribution level.

Table of Contents

Chapter 3. The Series Power Flow Controller

Chapter 4. The Dynamic Voltage Restorer Configurations

List of Symbols

GTO : Gate Turn Off Thyristor
IGBT : Integrated Gate Bipolar Transistor
HP : Horse Power
kHz : kilohertz (frequency)
SSB : Solid State Breaker
STATCOM : Static Compensator
SPFC : Series Power Flow Controller
DVR : Dynamic Voltage Restorer
FCL : Fault Current Limiter
SSTS : Solid State Transfer Switch
μs : microseconds (time)
kA : kiloamperes (current)
kV : kilovolts (voltage)
MVA : megavoltampere (apparent power)
MW : megawatts (real power)
MVAR : megavars (reactive power)
FFT : Fast Fourier Transform
RL Load : Load consiting of resistors and inductors only
p.f : power factor
S-L-G : Single Line to Ground (fault)
di/dt : rate of change of current
δ : Load Angle
Xl : Inductive Reactance
Xc : Capacitive Reactance
PWM : Pulse Width Modulation (Firing)
Vd : Capacitor DC Voltage
n : Transformer Turns ratio
pu : per unit
ma : Modulation Index
cosϕ : power factor
PCC : Point of Common Coupling
L-L : Line to Line (values)

List of Figures

Chapter 1

POWER QUALITY AND CUSTOM POWER

1.1 INTRODUCTION

There has been an increasing amount of focus on power quality in distribution systems. Due to factors like competitive generation patterns in a deregulated electric grid and an increasing level of sensitive end user devices, it has become necessary to ensure both reliable and quality power to the discerning customer.

Until recently, utility efforts in this direction were typically limited to installing passive filters or improving distribution capacity. If the customers require a high quality of power, low voltage power controllers, such as Uninterruptible Power Supplies, had to be installed at their end. But now, with the advent of cheap, high-power rated semiconductor devices like Gate Turn Off Thyristors (GTOs) and Integrated Gate Bipolar Transistors (IGBTs), it has become possible to design novel electronic controllers for high speed and precise control of power by the utility itself.

Such controllers are already in use in large transmission systems like Flexible AC Transmission Systems (FACTS) and High Voltage Direct Current Systems (HVDC) for providing functions like reactive power compensation, direct current transmission, damping of power oscillations etc. Custom Power now seeks to implement such designs for improving

dynamic power flow control in the distribution system and thus provide value added power to the customer [1].

1.2 SCOPE OF THIS THESIS

This thesis deals with the modelling of Custom Power topologies in the electromagnetic transient simulation programme PSCAD/EMTDC™. A brief description of the programme is given in Section 1.5.

With this objective, the scope of the thesis is

- to understand the issues involved in the operation of Custom Power topologies.
- to design control strategies that address most of these issues.
- to make simulation models in PSCAD/EMTDC for further studies in Power Quality.

The various Custom Power devices are enumerated in Section 1.4. The power quality problems and their traditional solutions are discussed in the following section.

1.3 RELIABILTY AND QUALITY OF POWER

1.3.1 Common Power Quality Issues

Reliability of power forms the first component of power quality requirements. IEC (1000-

-2-2/4) and CENELEC (EN50160) standards define power quality as the physical characteristics of the electrical supply provided under normal operating conditions that do not disrupt or disturb the customers' process. Therefore, reliability of power is the first prerequisite to power quality issues.

A power supply may be said to supply reliable power if there are no outages or if there is a fast recovery from outages by fast fault clearance or backup generation. A considerable amount of reliability has been ensured by the various utilities over the years by increasing grid networking and improving breaker devices. But due to the complexity of the distribution network, outages and interruptions are far more common on the distribution system than on the transmission grid [6].

Quality of power combines all the elements of reliability with additional considerations to the voltage waveforms at the customer bus. Ideally this voltage should be a perfect SunView without any distortions, at it's nominal magnitude and nominal frequency. Further, for a three phase system, the voltages should form a perfectly balanced set, with each phase displaced by 120 degrees with respect to the others [2].

Distortions in the voltage waveform may be due to harmonics, transients, voltage over shoots or undervoltages. Such distortions, which were hitherto tolerated, manifest as severe problems when it comes to highly sensitive consumer devices such as the computers, lamps, communication systems, industrial sensors and controls.

Table 1 gives a concise summary of the various power quality problems, their causes and effects, based on a literature review with references like [4]....[8].

Table 1: A Summary of Various Power Quality Problems

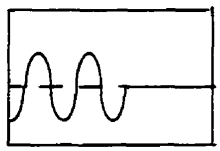
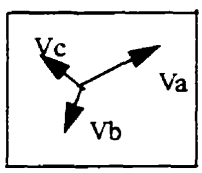
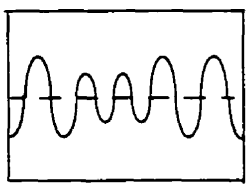
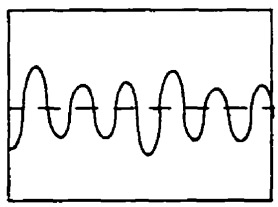
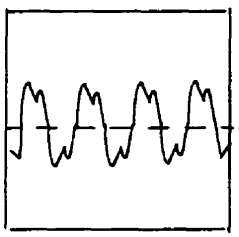
TERM	EFFECTS	CAUSES	TRADITIONAL SOLUTIONS
Voltage regulation	A decrease in the voltage at the utilisation terminal.	Impedance drops in the feeders, house wiring etc.	Reducing impedance by paralleling transformers. Increasing primary feeder voltages, feeder size.
Voltage outages/ interruptions 	A complete loss of voltage; called an interruption if it is for < 5 mins. An expensive loss to the industry due to long downtime.	Open circuit faults in the cables. Operation of protective equipment during fault clearance.	Faster fault clearance. Increasing parallel feeders and grid networking.
Voltage unbalance 	Produces negative sequence components. May cause sags. Three phase motors, if run on single phase generate excessive heat.	Mostly caused due to Single Line to Ground faults. May be caused by unbalanced loading such as railway load or even by untransposed lines.	Improved balancing of loads. Faster fault clearance
Voltage dips/sags 	A reduction in the rms value of voltage for 0.5-30 cycles. Cause malfunctioning in loads such as computers and VCRs; tripping of relays, motor contactors in drives, mercury lights.	Remote faults /parallel faults, lasting until fault clearance. Reclosing operations may give multiple sags. Starting of induction motors may initiate/aggravate a sag.	Mechanical transfer of sensitive loads in a selective type of system. Localised application of a saturated ferrotransformer.
Voltage flicker 	A momentary fluctuation in voltage, causing irritation to the human eye if resulting in visible light fluctuations. May interfere with functioning of sensitive equipment.	Motor start-up, switching on of large capacitor banks, operation of arc furnaces and rolling mills. May also be caused by fractional HP motors as in refrigerators.	Use of saturable reactors / ferrotransformers. Isolation of heavy duty loads from sensitive loads.

Table 1: A Summary of Various Power Quality Problems

TERM	EFFECTS	CAUSES	TRADITIONAL SOLUTIONS
Harmonics 	A superimposition of voltages of different frequencies on the fundamental, leading to additional losses and overheating. Possible resonances with local inductances. Telephone interference.	Mainly electronic switching load such as thyristor drives, rectifiers, UPS etc. Non linear loads such as lights.	Y-Δ transformers to restrict third harmonics. Underground cabling to use shunt capacitance filtering. Passive low-pass/ tuned filters near the customer end.

1.3.2 Power Quality Standards

There are attempts by the concerned agencies such as the IEEE [4] [5] [7], to fix a set of standards to accurately define and quantify the quality of power supplied to the customer. But standards for the amount of allowable power line disturbance vary with the type of load and the magnitude of the disturbance. Indeed, power quality is firstly defined to be that level of power which satisfies the customer. The CEA 9109 U 856 Series classifies the power quality into five classes ranging from "pure" Class A, as in the Uninterrupted Power Supply (UPS), to "almost ideal" Class B, as for the Computer Business Equipment Manufacturers Association (CBEMA) Voltage Tolerance Curve, and so on till Class E where frequent outages for long seconds could be allowed.

A general idea of the power quality requirements could be had from Table 2 below, which are taken from IEEE Standards 446-1987 for the Computer Manufacturing Industry.

Table 2: Typical Range of Input Power Quality and Load Parameters of Major Computer Manufacturers

	Parameters	Range or Maximum
1	Voltage regulation	+5,-10% to +10,-15%
2	Undervoltage	-25% to -30% for less than 0.5 s; -100% acceptable for 4 to 20 ms; (see Figure 1.1)
3	Transient overvoltage	+150 to 200% for less than 0.2 ms
4	Voltage harmonic distortion	3 to 5% with a linear load
5	Frequency variation	60 Hz +/- 0.5 Hz to +/- 1 Hz
6	Noise	No standard
7	3 ϕ voltage unbalance $= \left(\frac{3 \cdot (Vmax - Vmin)}{Va + Vb + Vc} \cdot 100 \right)$	2.5 to 5%
8	Power factor	0.8 to 0.9

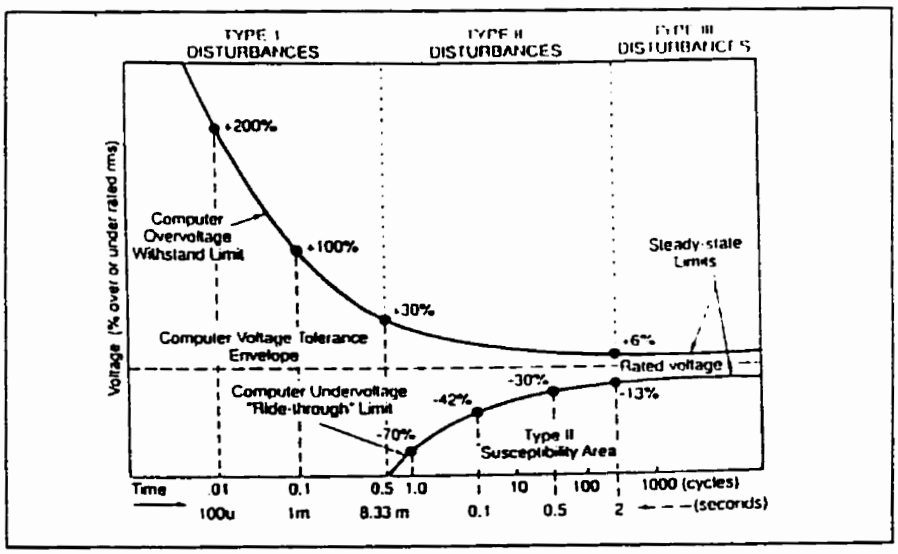


Figure 1.1: The CEBA graph for Voltage Tolerance (IEEE Std. 446-1987)

Figure 1.1 shows the CBEMA curve for voltage quality for computers, which is mostly used as a guide for voltage quality studies. It can be seen that while a 13% sag can be borne for 2 seconds, a 70% sag cannot be tolerated for even 16 ms.

It is more difficult to set a standard for voltage flicker as it is primarily defined to be that level of fluctuations in brightness that would cause irritation to the human eye.

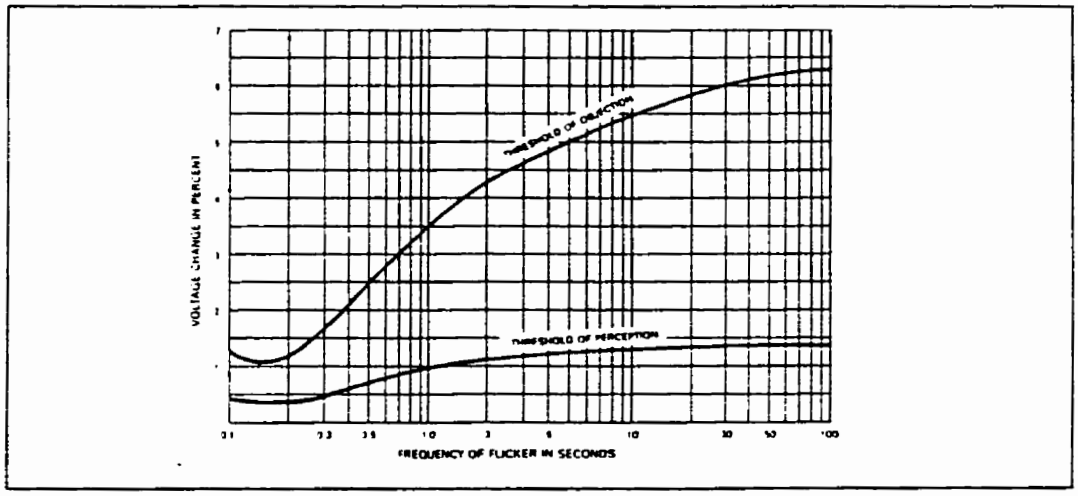


Figure 1.2: Range of Objectionable Flicker versus Time (IEEE Std. 141 -1986)

Figure 1.2 may be used to determine whether voltage fluctuations will cause objectionable fluctuations in the light output of incandescent lamps. The range between permissible flicker and objectionable flicker is to accommodate the differences in human perception and the environmental conditions. It can be seen that even a 2% change for 1/2 second is intolerable. It also shows that the flicker is mostly in the range of a few hertz, say 7-9 Hz.

1.4 CUSTOM POWER

1.4.1 The Static Controllers

As was stated in the introductory paragraph, it is now possible to use fast acting switching

semiconductor devices to improve power quality, which is the objective of this thesis.The semiconductor devices can not only be used as simple switches, they can also be used to generate complex waveforms with controllable magnitude, phase or frequency and to inject them into the line and thus compensate for quality problems from the source.These devices have only been possible due to the rapid strides in the semiconductor industry which offers high power rating devices such as GTOs with ratings such as 3 kA and 4.5 kV peak values (for a symmetrical GTO pair) or IGBTs, which can bear higher switching frequencies like 2 kHz[12]. The rapid response of such devices enable them to operate in real-time and online and provide continuous and dynamic control of the supply [1].

These devices are incorporated into the following topologies to improve various power quality problems.

1. The Distribution Static Compensator (D-STATCOM) for reactive compensation and flicker control by being placed in shunt with the load for dynamic compensation.

2. Active Filters for harmonic elimination by injection of a controlled harmonic current to oppose the instantaneous harmonics produced by the load.

3. The Solid State Fault Current Limiter (SSB-FCL) for reducing fault current levels to that of the downstream protection devices.

4. The Solid State Transfer Switch (SSTS) for fast transfer of sensitive loads to protect against system side faults such as voltage sags.

5. The Series Power Flow Controller (SPFC) for series reactive power flow.

6. The Dynamic Voltage Restorer (DVR) for compensation of voltage sags by series injec-

-tion of a controlled voltage.

7. A Unified Power Controller or Conditioner, seeking to incorporate all the features of the above mentioned devices into one.

8. A rechargeable source of energy such as the Superconducting Magnetic Energy Storage (SMES).

1.4.2 Contributions of the Thesis

This thesis has covered

i) development of the power circuits of

(a) The Transfer Switch

(b) The Fault Current Limiter

(c) The Series Power Flow Controller

(d) The Series Voltage Regulator

(e) The Dynamic Voltage Restorer

ii) analysis of the various issues involved in the performance of these devices.

iii) designing of control strategies that would result in successful, working models.

iv) testing for various conditions and evaluation of results.

These configurations are modelled, analysed and discussed in individual chapters later in this thesis. While the Transfer Switch and the Fault Current Limiter use the thyristor

switching device as a plain Solid State Breaker, the rest of the topologies involve the GTO switching device in a STATCOM configuration with a Pulse Width Modulated (PWM) type of switching control.

The results are computed with the help of a simulation tool PSCAD/EMTDC^{TM}: a word on it follows.

1.6 PSCAD/EMTDC

PSCAD is a collection of programs, providing a very flexible interface to electromagnetic transient simulation software. EMTDC is the library of power system component models and procedures which constitutes the simulation software[3]. Together, they offer a very powerful tool for transient analysis.

Circuits are drawn using the graphical DRAFT module, which are then compiled and run using the RUNTIME module. Parameters can be accessed and changed during a run and the results can be plotted using the MULTIPLOT module.The basic code is in FORTRAN.

Chapter 2

SOLID STATE BREAKER CONFIGURATIONS

2.1 INTRODUCTION

The time required for mechanical interruption of faults on a transmission line is known to be typically in the order of 1.1-10 secs.[9]. Similarly, mechanical transfer of loads from a faulty feeder to a healthy one can cause a power interruption of at least 2 secs [10].

On a distribution line, sensitive equipment like computers, programmable drives, consumer electronic equipment like televisions and VCRs cannot tolerate a disturbance of such a length of time and show perceptible effects in their operation. As was shown in Chapter 1, even a small sag of 30% lasting for half a second can cause malfunction in a computer. Further, many industries using thyristor based drives have reported hours of equipment downtime and considerable losses due to voltage sags [11].

A Solid State Breaker (SSB), on the other hand, typically acts within 1/4 of a cycle and offers fast isolation / transfer of feeders or loads [1]. This swift action can be used advantageously, even in conjugation with the slower mechanical breakers, for protection schemes. The objective of this chapter is to study the possible applications of the SSB that can be used with the existent distribution network.

Figure 2.1 shows three configurations that are possible with the SSB viz. a Transfer Switch, a Bus Tie Breaker and a Fault Current Limiter.

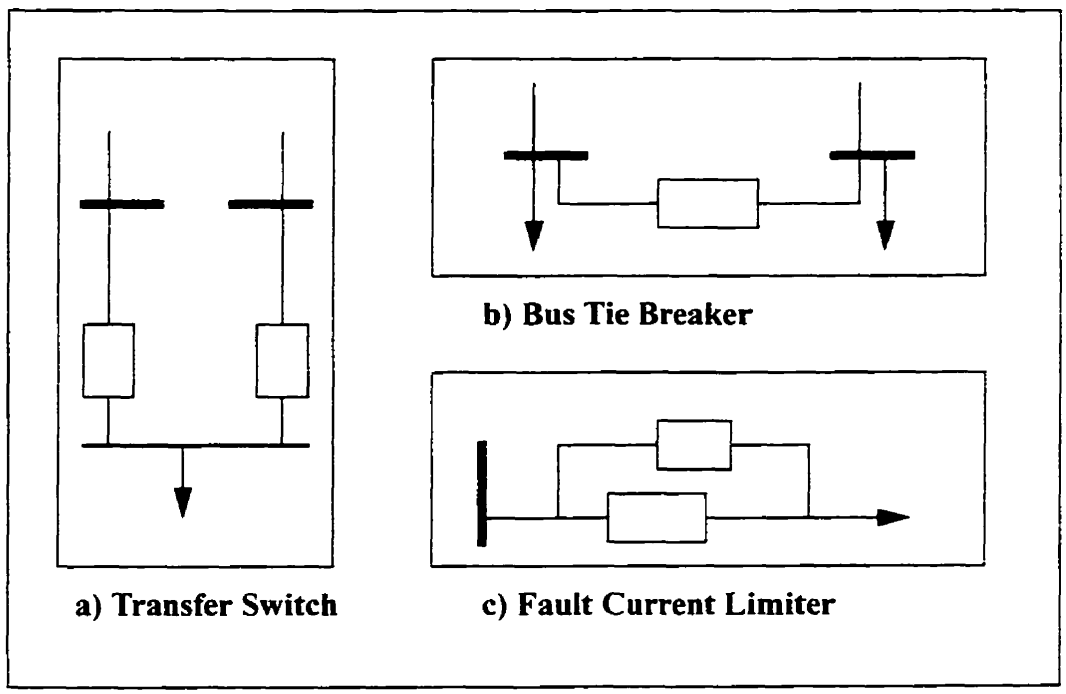


Figure 2.1 : Various applications of the Solid State Breaker

A Solid State Transfer Switch (SSTS) is used to protect sensitive loads by switching it onto a healthy backup feeder if there are any problems on the main feeder. This can be incorporated using thyristors. A Solid State Breaker-Fault Current Limiter (SSB-FCL) is used to limit fault current levels to downstream protection device levels and can be designed using both GTOs and thyristors.

A Bus Tie Breaker is used to isolate buses during faults and can easily be incorporated by using just a self commutated GTO based SSB. Present designs rely on expulsion fuses, which have to be reset manually. A Bus Tie Breaker can be considered to be a special case of the Fault Current Limiter and hence only the other two configurations are further studied in this chapter.

2.2 THE SOLID STATE BREAKER AS A TRANSFER SWITCH

2.2.1 Introduction

The transfer switch is used to protect sensitive loads from system side faults.These could include outages, voltage swells, sudden phase changes, but they are most predominant as voltage sags. Detailed descriptions of sags, their causes and their effects have already been discussed in Chapter 1. The transfer switch here is used to mitigate the effects of such sags on sensitive loads. Generally, it could be used in two configurations as shown in Figure 2.2.

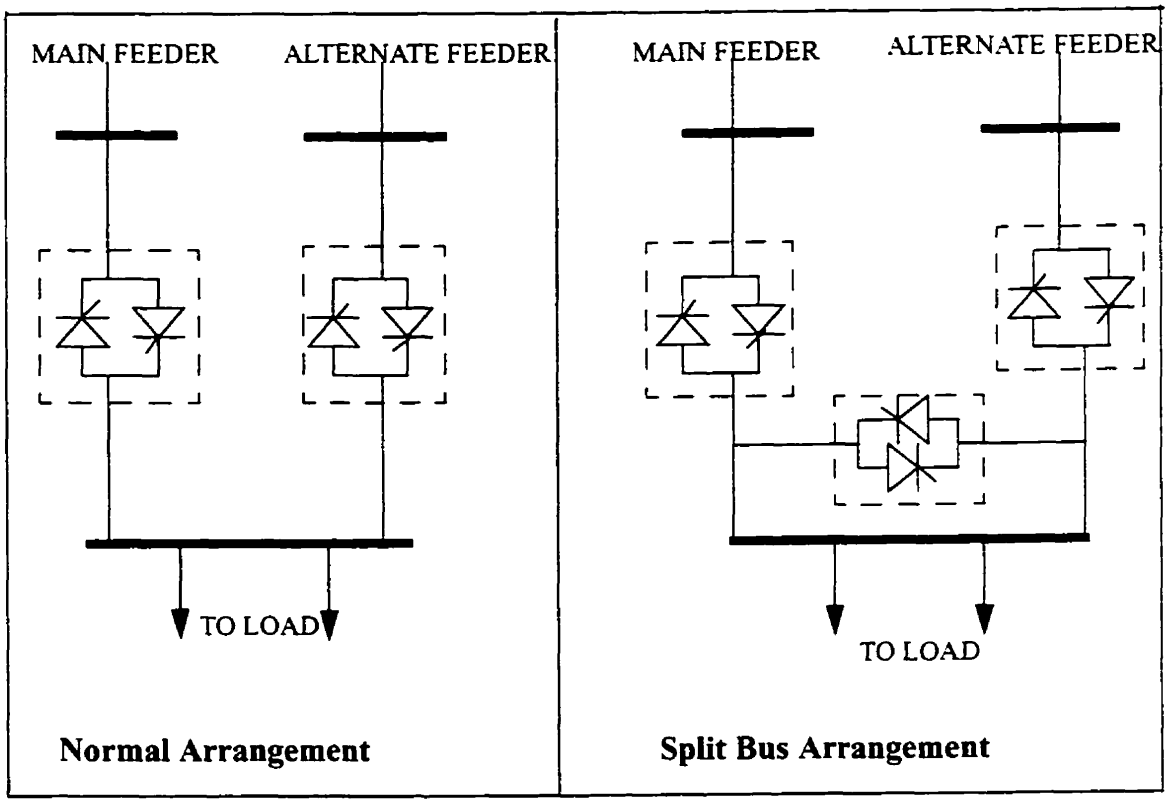


Figure 2.2 : Two Configurations of the Transfer Switch

Normally, this SSTS is designed to detect a voltage disturbance within 4 ms and immediately transfer power for sensitive loads from one source to another healthy source [1]. The two feeders could be at different points on the same network or they could be from entirely different systems, as in a stand-by emergency supply. The split bus arrangement is used to reduce transients during handover.

The semiconductor device used in the SSTS are thyristors. This is so because the switch is in continuous conduction mode and requires in addition to a continuous current rating, a short time overcurrent rating equal to the load side faults. Thyristors have a high short time overcurrent rating of 16 kA and also have low conduction losses [12].

The thyristors in the main branch are normally continuously energised by continuous, synchronised firing. On detection of a sag, these firing pulses are stopped. The thyristors which would have then stopped conducting at the first natural current zero in that phase, are now subjected to a high reverse voltage from the other feeder and are immediately turned off. Current interruption is thus achieved in sub cycle.

Some considerations that are to be addressed while incorporating this device [10], [11], [12], and used in this thesis for the design of the control system include :

1. The detection method for a sag should be fast (preferably within 1/4 th of a cycle) and should be so even in the presence of a reasonable amount of harmonics or transient phase changes or unbalance.

2. There should be no transfer in case of sags due to faults on load side.

3. There should also be no transfer if the phase difference between the two feeders is considerable (taken here to be >10 degrees) as this would cause high inrush currents for loads such as induction motors and transformers.

2.2.2 Controls for the Transfer Switch

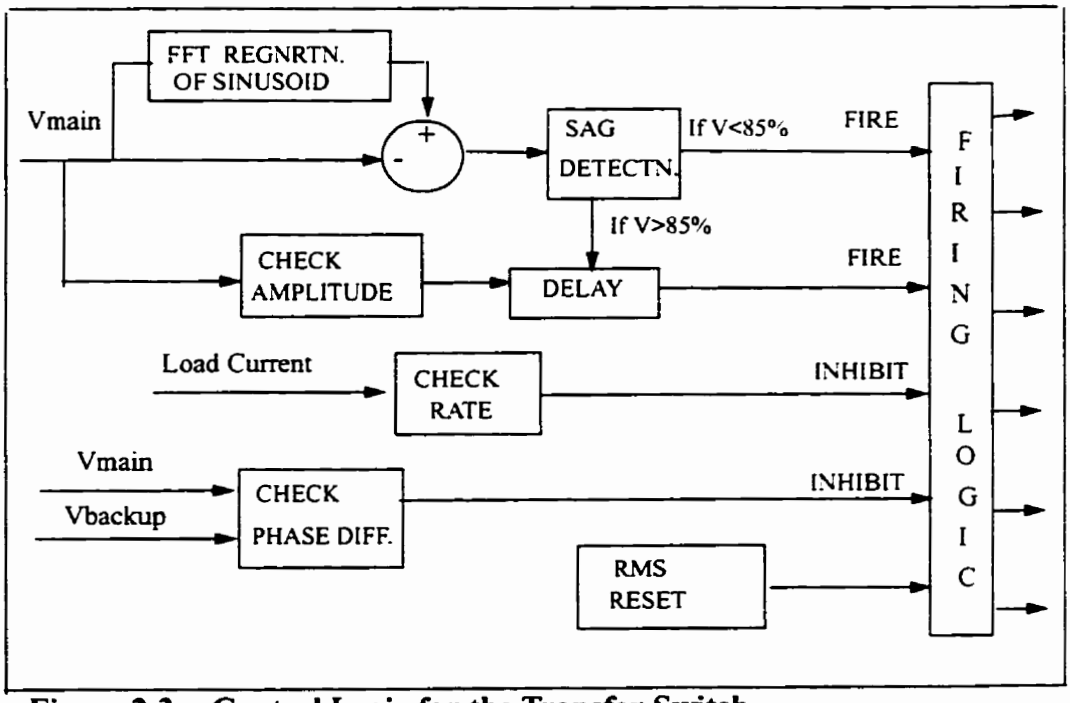


Figure 2.3 : Control Logic for the Transfer Switch

Instantaneous detection of a sag is obtained by constant comparison of the voltage waveform with a ideal sinusoid in phase with it and having a magnitude equal to the pre -sag value. This sinusoid is reconstructed using the fundamental frequency component of the Fast Fourier Transform of the voltage waveform from a previous cycle. If the actual waveform has a lower instantaneous value over the predicted waveform, an error signal is generated for a sag, as shown in Figure 2.4.

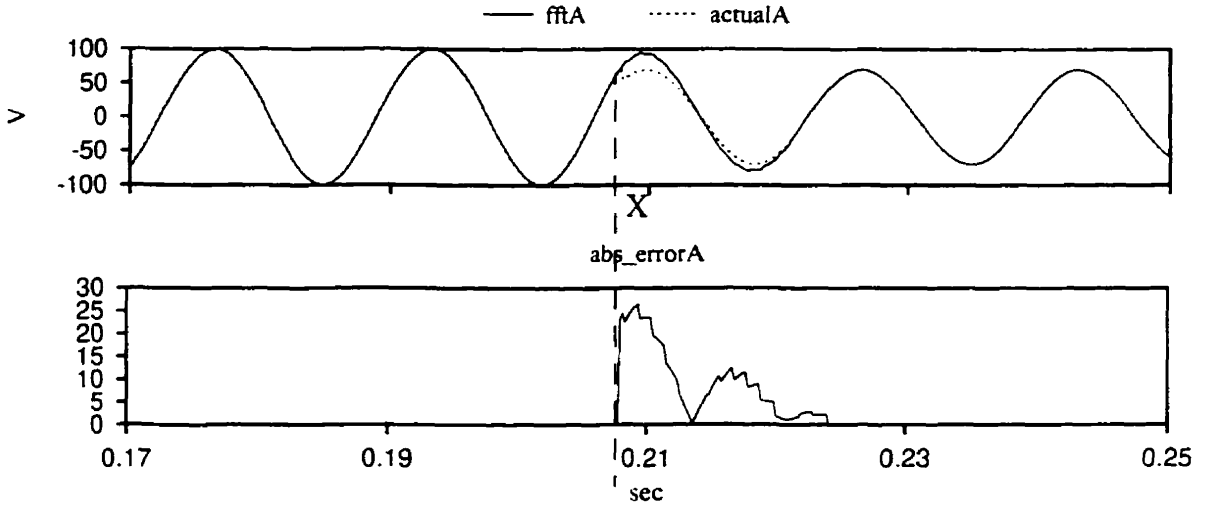


Figure 2.4 : Generation of an error signal using FFT

The sag is applied at point 'X'. It is seen that the FFT generated waveform 'fftA', which is delayed by 1 cycle, remains at the previous steady state value for at least 1 cycle, giving rise to an instantaneous detection of an error, lasting for 1 cycle. This can be further processed for developing the firing pulses for the thyristors.

It is obvious that such an error signal will be generated for any other form of distortions such as a phase change, harmonics or voltage swells. This would give rise to "nuisance tripping" and in order to avoid that, a more robust method of detection for small sags is used, whereby some more time (1/2 cycle) is used to check the peak of the waveform and detect a sag.

Inhibition blocks are used to detect faults on load side and / or excessive phase differences between the two feeders and prevent the transfer.

2.3 RESULTS OF SIMULATIONS

2.3.1 The Simulation System

Simulations were performed on a three phase 100 MVA system as shown below. This system is identified as a suitable candidate for Transfer Switch studies [11].

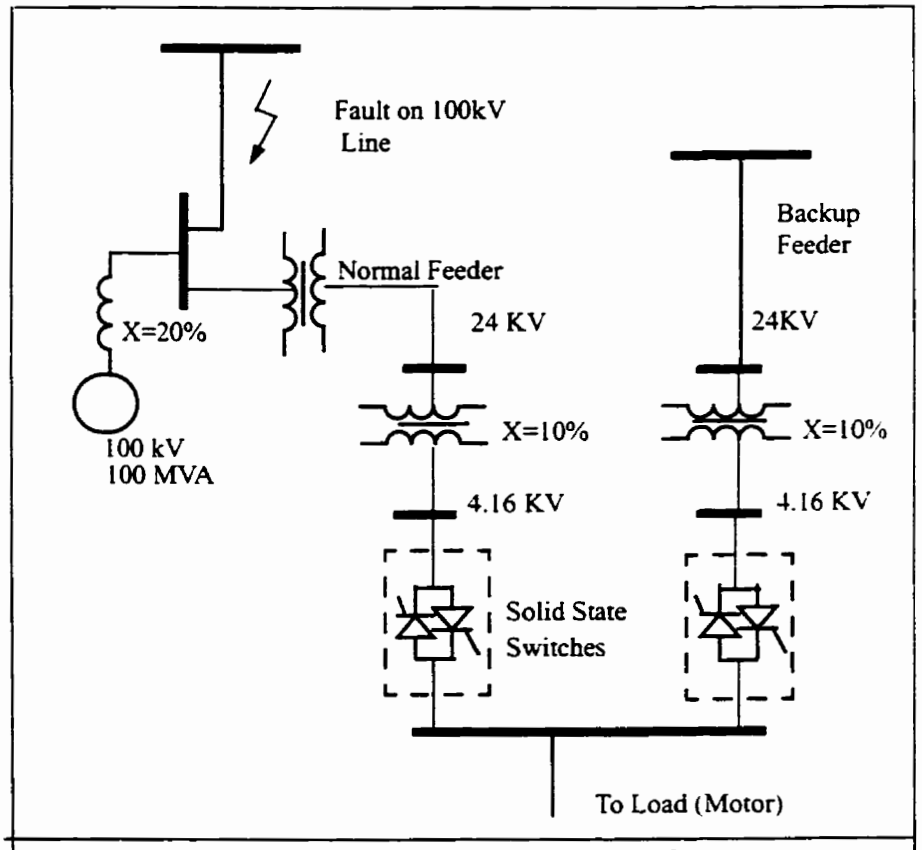
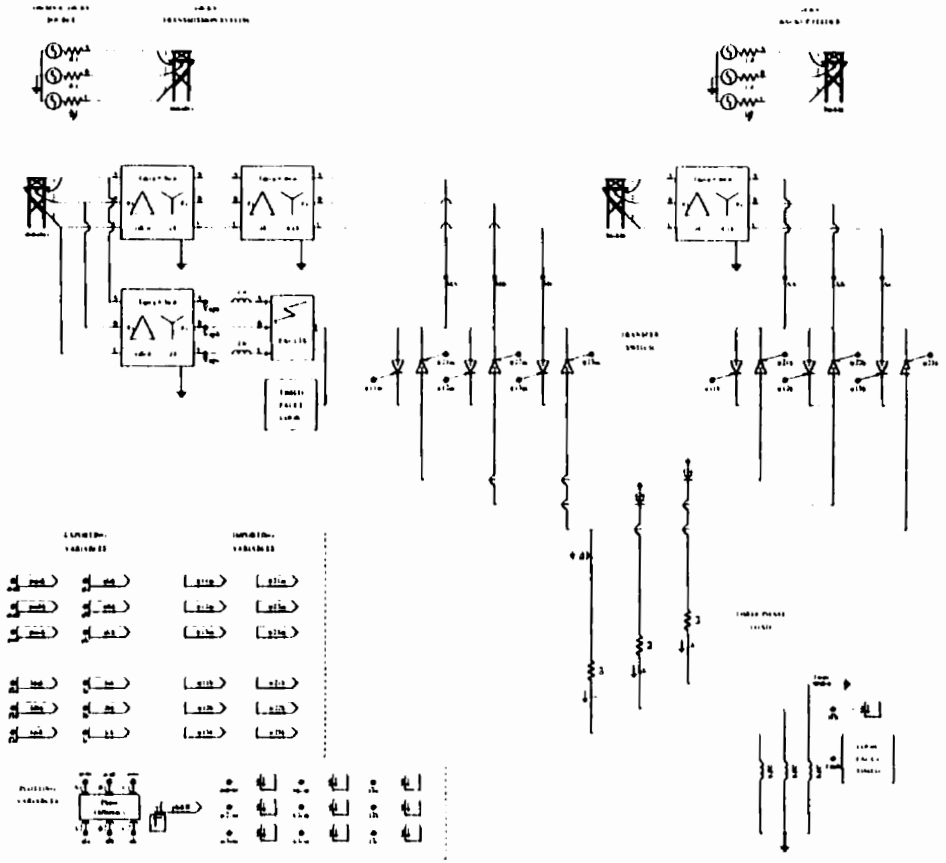


Figure 2.5 : Test system for the Transfer Switch

Faults are applied on a parallel line to induce the necessary levels of sags on the main feeder. The circuit is tested for two types of loads: a 0.7 p.f. RL load and a Induction Motor load.The detailed PSCAD/EMTDC Draft circuit is shown next in Figure 2.6.



University of Manitoba, EE Dept.

Solid State breaker as a Transfer Switch

Created:	June 01, 1997 (leena)
Last Modified:	September 21, 1998 (leena)
Printed On:	September 21, 1998 (leena)

SS 1

Subsystem #1 of 2

2.3.2 Response to Different Levels of Sags

Figure 2.7 illustrates the rapid action of the transfer switch for a remote fault on the main bus, causing a sag of around 40%. The alternate bus was at zero phase difference with respect to the customer bus and the load was a 12 MVA load at 0.8 p.f.

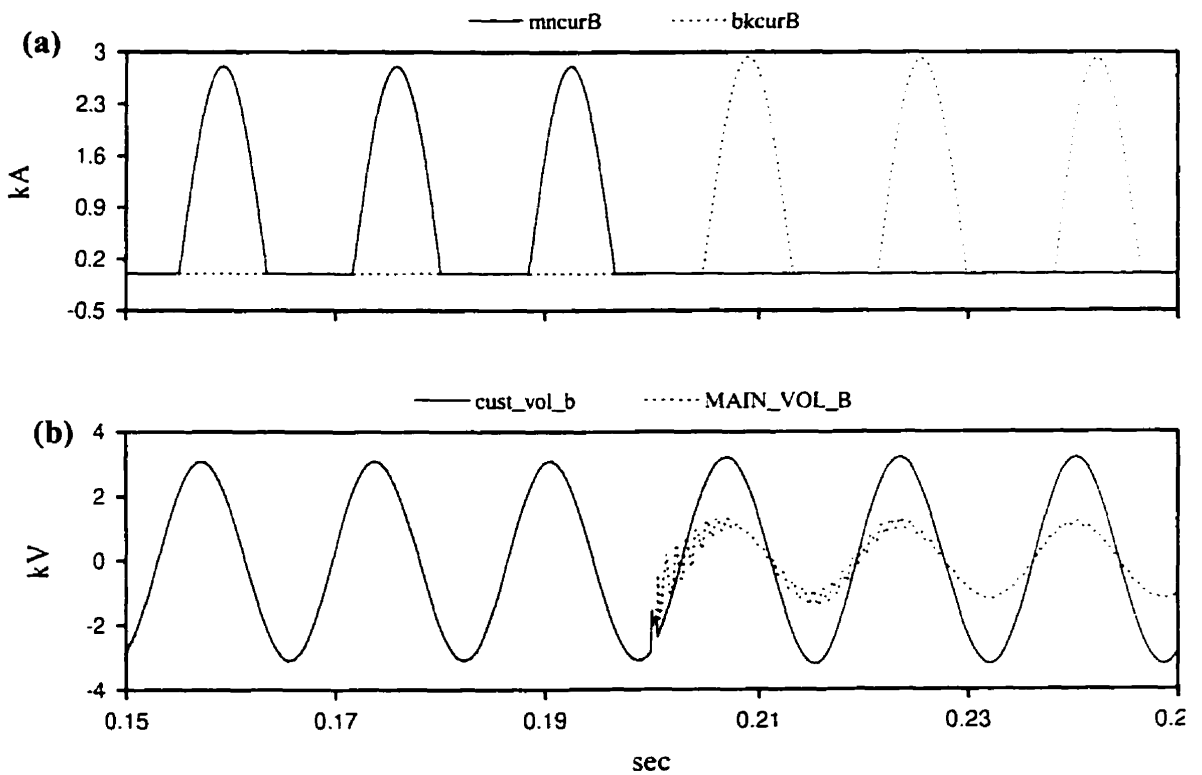


Figure 2.7 : Transfer of a RL load for a 40% sag

Figure 2.7(b) shows the voltage at the customer bus. Since the sag was well above 20%, it got detected within 1/4th of a cycle and an immediate transfer was initiated. The customer voltage remained almost undistorted.

For sags smaller than 15%, as was mentioned earlier, a higher margin of time is allowed for detection by measurement of the amplitude of the source voltage.

2.3.2 Response to Unbalanced Sag

Figure 2.8 shows the result of applying an unbalanced 90% sag, by putting a S_L_G fault on a parallel feeder. It can be seen that while the affected phase transfers almost instantaneously, the unaffected phases (phase C) are made to transfer only at a current zero, to reduce thyristor stresses.

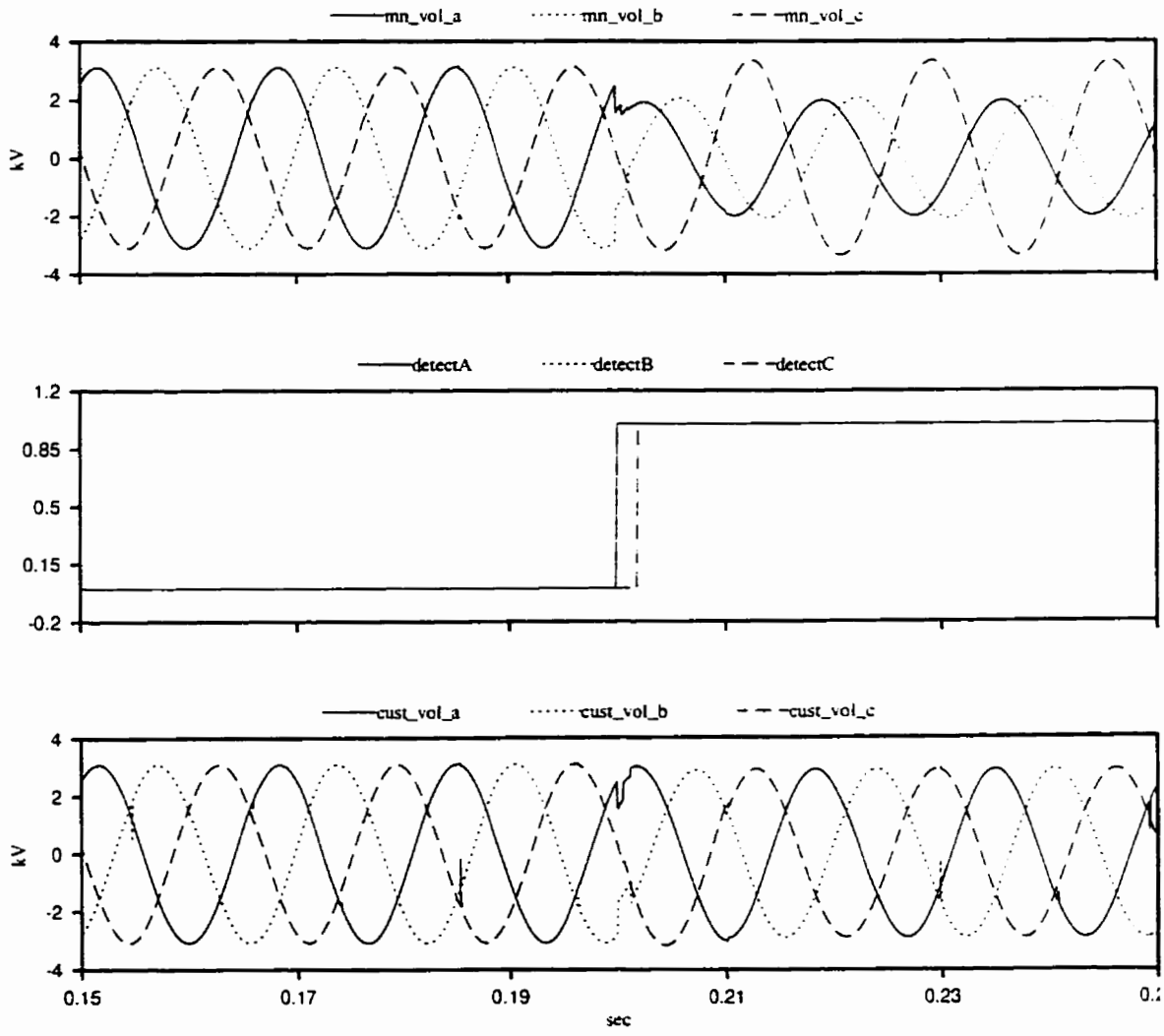


Figure 2.8 : Transfer for an unbalanced sag

2.4 MAKE BEFORE BREAK OR BREAK BEFORE MAKE

2.4.1 Problem with Mechanical Breakers

The type of transfer logic used for the Transfer Switch is a make-before-break transfer in which the main feeder is disconnected only after the alternate feeder is switched. This type of transfer is known to cause the least amount of transient in the customer voltage [11]. If mechanical transfer switches were used with a make-before-break type of transfer. there could be a high momentary short circuit through the breakers.This short circuit current increased with increase in the phase difference between the two feeders and could be quite severe.

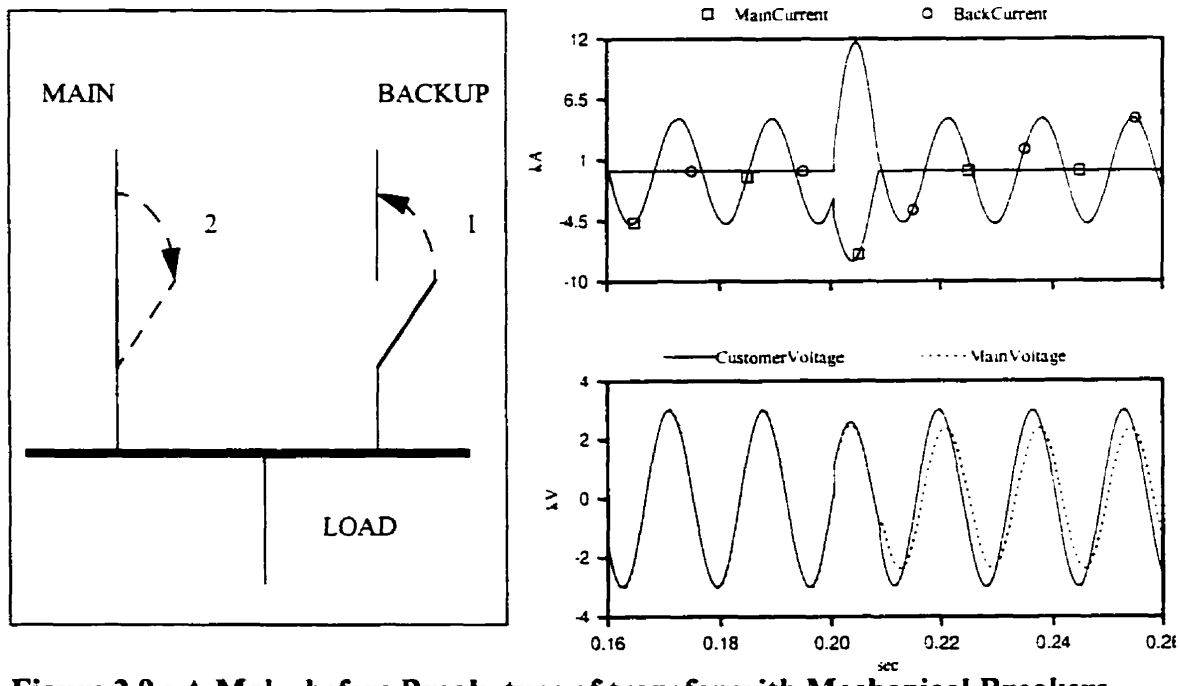


Figure 2.9 : A Make before Break type of transfer with Mechanical Breakers and a 30 degree phase difference

This problem could be avoided if the type of transfer is changed to a break before make type of transfer wherein the load is disconnected from both systems momentarily before switching it onto the backup feeder, after phase monitoring, if necessary. But this, of course, distorted the voltage at the customer bus for a long period.which is not the aim of Custom Power.

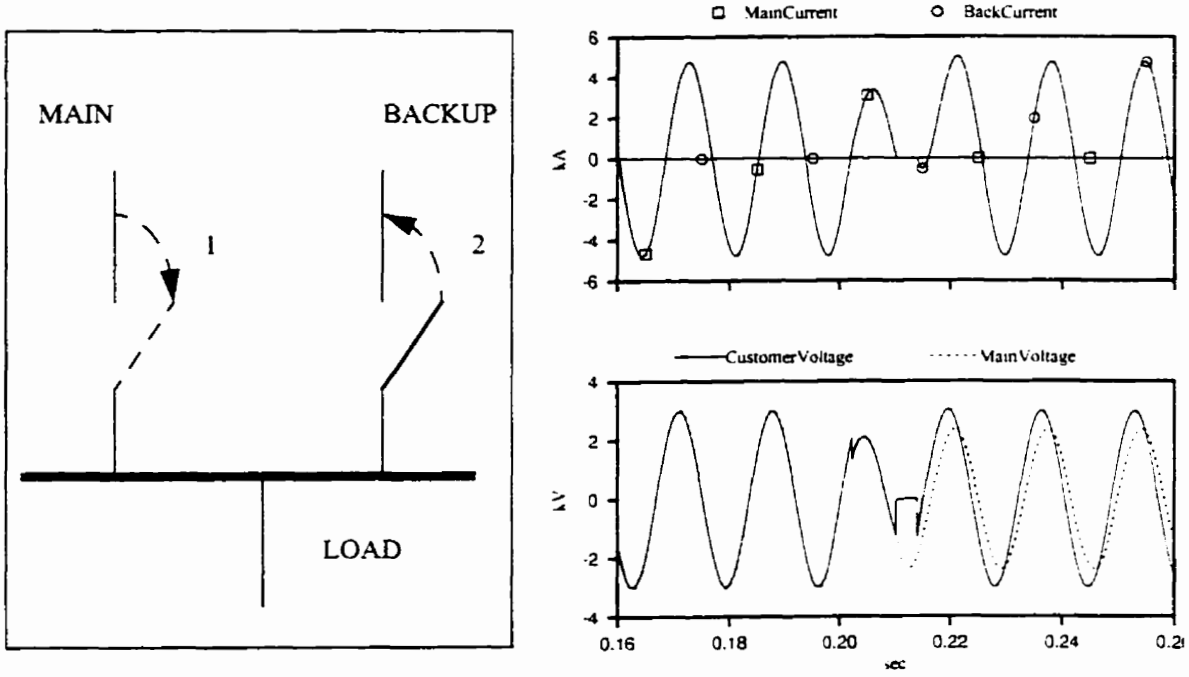


Figure 2.10 : A Break before Make type of transfer with Mechanical Breakers and a 30 degree phase difference

2.4.2 Advantage of Intelligent Polarity Selection with SSTS

The advantage offered by thyristor based breakers is that there is no single bi-directional breaker per line but there are *two* opposite polarity thyristors which form one breaker. Each thyristor conducts only for half a cycle at the maximum while the voltage across it is

a forward bias and stops conducting in the other half when the current through it reaches zero. This makes it possible to achieve a degree of freedom per half cycle, which can be used advantageously to eliminate short circuit currents through the thyristor breakers.

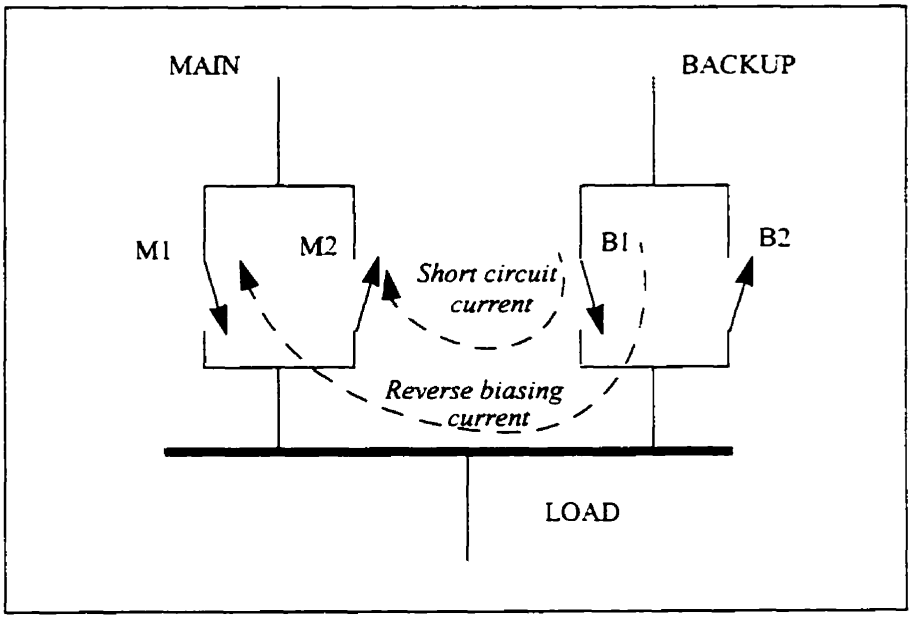


Figure 2.11 : Make before Break type of Transfer with SSTS

If there is a make before break type of transfer performed with a thyristor based transfer switch, (Figure 2.11) and if we use a transfer logic whereby M1, M2 and B1, B2 are both either on or off, as in the mechanical breakers, we can see that there are two types of currents that can flow per half cycle. A momentary reverse bias current flowing due to the sag on the main feeder which is necessary to turn off the thyristor (say M1) on the main branch. And a momentary short circuit current which would flow through B1 and M2 at high phase differences between the main feeder and the backup. (This current would not flow if there is no phase difference as M2 would not be conducting in the half cycle that M1 would be conducting in).

Thus this short circuit current can be easily avoided if we completely ensure that M2 is never on when M1 is on - even at high phase differences- which can be easily had by not issuing a pulse to M2 when there is a pulse for M1. Thus even if M2 may become forward biased at large phase differences, it will not conduct since there is no firing pulse for it. This method of polarity selection ensures that there is absolutely no short circuit current through the breakers at any phase difference between the feeders.

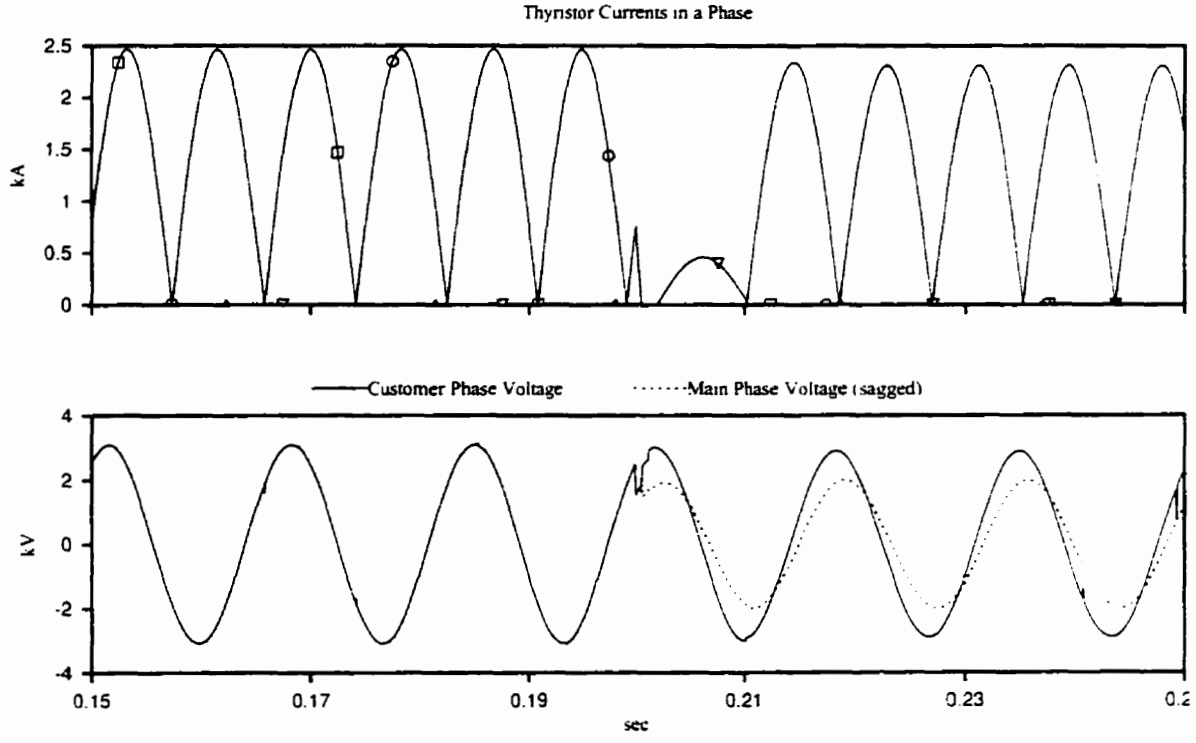


Figure 2.12 : A Make before Break type of transfer with an SSTS and a phase difference of 30 degrees between the main and the backup source

2.4.3 Response to Induction Motor Load

For loads such as induction motors, the dynamics during transfer also depend on factors

such as motor residual voltage and phase angle between this voltage and the power supply voltage and a mismatch between them may induce abnormally high inrush currents and shaft torques[11]. These high currents may again aggravate a sag during transfer. Thus even if a Make before Break type of transfer is possible with a SSTS, it may not be the best logic for an Induction Motor load.

Figure 2.13 shows some results that are obtained with an induction motor load of 3000HP transferred to an alternate feeder at 30 degrees phase difference with the main feeder.

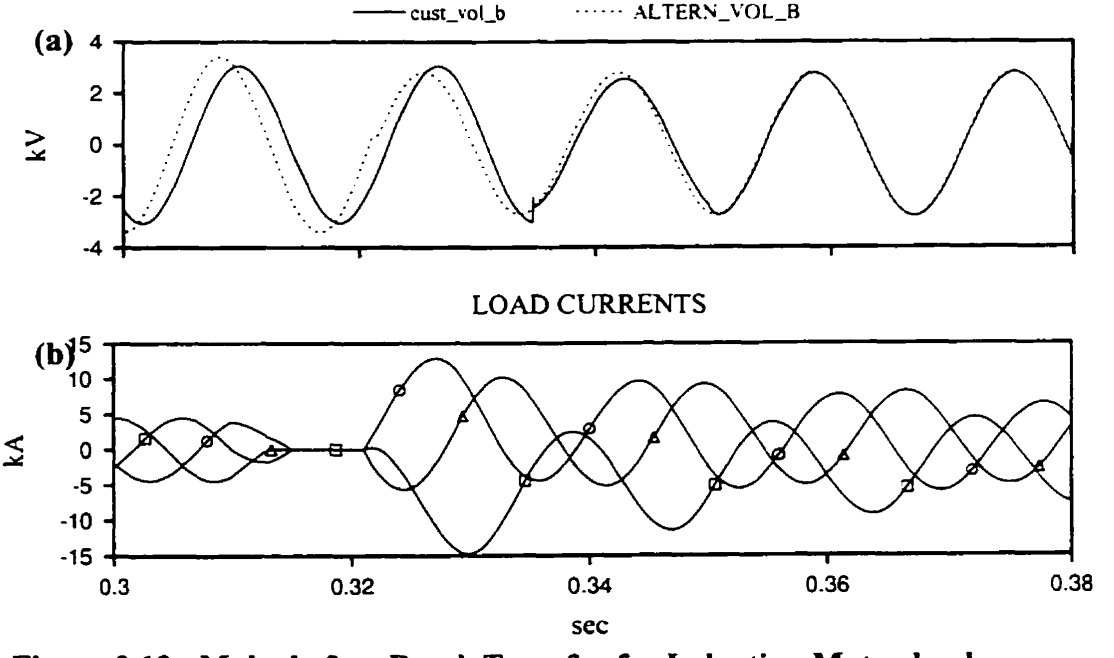


Figure 2.13 : Make before Break Transfer for Induction Motor load

It is seen that the customer voltage gets minimum distortion due to the main source voltage, but it draws very high inrush currents(Figure 2.13(b)) on being re-energised by a voltage at a high phase difference (around 70 degrees). These currents may be so high that they can cause an additional sag.

Figure 2.14 shows the possible advantages of allowing the induction motor bus to develop certain voltage and phase characteristics of it's own and closing the alternate feeder switch only if the phase difference is within 10 degrees. The load currents drawn are reduced significantly as shown in Figure 2.14 (b).

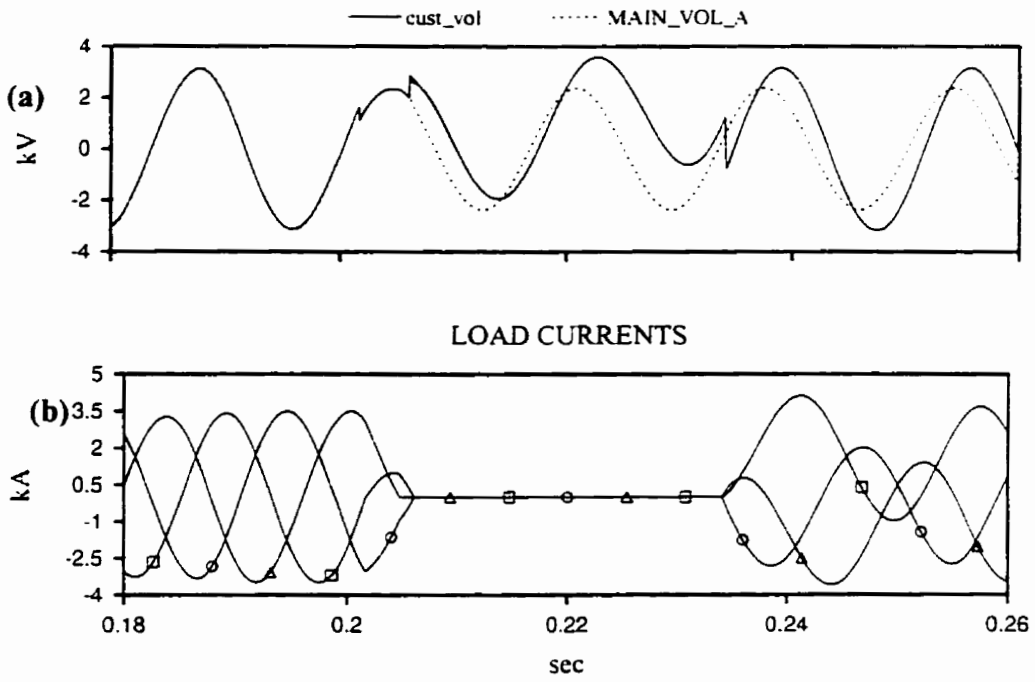


Figure 2.14: Break before Make transfer for an Induction Motor load

Issues regarding the Induction Motor load have different schools of thought [11], [21]. The decision for a Make before Break type of transfer or the reverse, for such a load, shall have to be made only after a complete analysis of the particular load behaviour.

2.5 THE SOLID STATE BREAKER AS A FAULT CURRENT LIMITER

2.5.1 Introduction

The present-day ac networks have an increasing level of short circuit faults. This is due to addition of system interconnections, paralleling of generation or increased loading[13]. Therefore, it sometimes happens that the level exceeds the ratings of the switchgear installed on the line and jeopardises protection operations during faults. Fault current limiters are, therefore, used upstream, to interrupt the fault and limit it to the protection level of the downstream protection devices.They only allow sufficient current to initiate downstream breaker operations. They can also be used in cases where an essential load has to be supplied. A Bus -tie Switch can be taken to be a special case of a Fault Current Limiter without the Current Limiting option.

The typical fault current limiter consists of an overcurrent fuse in parallel with a current diverting reactor. The fuse blows within 1/4 th of a cycle of the fault and diverts the current to the reactor. Fuses are limited in rating to 27 kV and have to be manually replaced.

2.5.2 Topology of a SSB-FCL

The SSB is connected directly in series with the line and is capable of providing sub-cycle interruptions(<1ms) on faulty feeders [1].

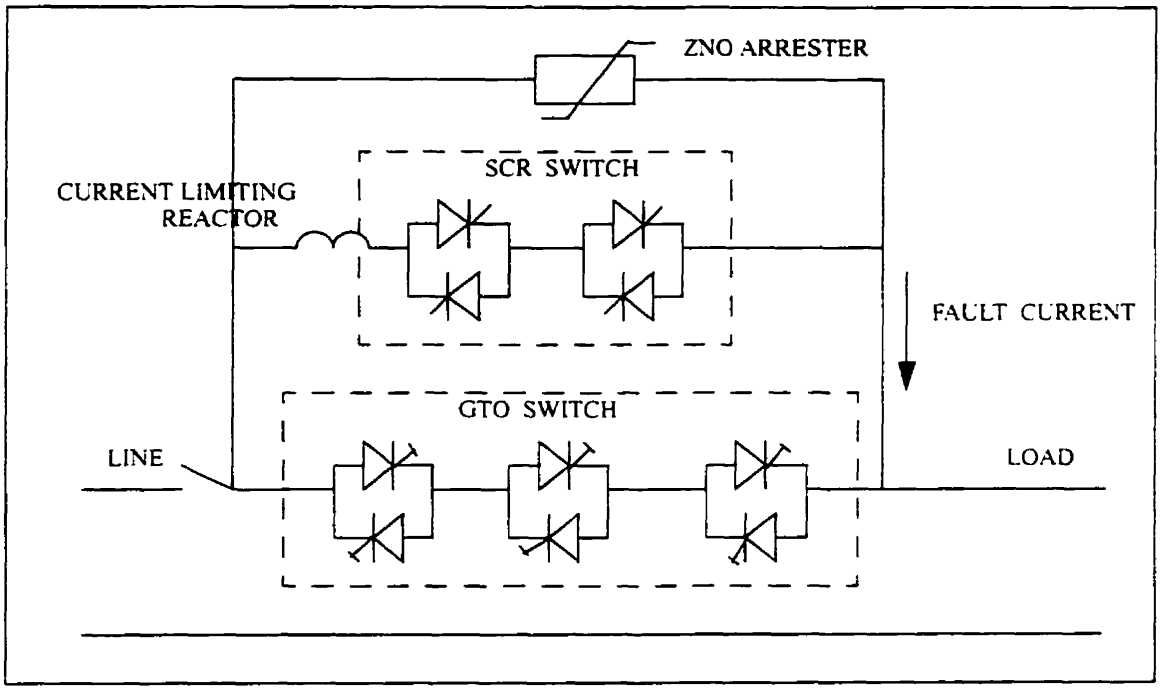


Figure 2.15 : A Solid State Breaker with a Fault Current Limiting unit

The GTO provides rapid interruption capability. During normal value of load currents the GTO branch works like a short circuit, but if the value increases beyond a certain preset level, the control circuitry switches off the GTO modules. Current immediately gets transferred to a parallel thyristor switch module with a current limiting reactor. A resistor could also be used at the risk of higher thermal losses.

The benefits of GTOs is that they are capable of instantaneous turn off with negligible delay on application of a appropriate gate signal. Since the general view of protection equipment for the distribution class is of 15kV, 600 A (with fault currents of value greater than 6kA) [12], a 3 kA rated GTO has sufficient margin to detect and turn off at the fault current. It thus provides an interruption at the first fault loop itself and eliminates the complexities of trying to introduce a high impedance at the very first loop [14], as

would be the case if current limitation is attempted using the typical Moulded Circuit Breakers with the resultant arc complexity [14]. Here, there is no attempt to insert the reactance until the current has been brought to zero.

But the GTO cannot carry the fault current for greater than 1 cycle due to its limitation of rating (a di/dt of 500 A/us). It is, therefore, difficult to use the SSB by itself in a practical electrical system, where the device has to coordinate with slower downstream protection systems. Except for a bus -tie location where protection coordination is not required, a SSB has to carry the fault current for a limited period of time till the slower breakers downstream are actuated and the fault is cleared [12]. A survey conducted by EPRI[12] indicated that the current interrupting device has to be able to conduct fault currents for about 10-15 cycles repeatedly for 3-4 times, consistent with the fault clearing sequences of existing distribution reclosers.

Therefore the current is transferred to a high inductance shunt branch for the remainder of the fault. The shunt branch can also have back to back thyristors, whose firing can be controlled to further limit the fault currents and thus reduce the size of the reactor used. The ZNO Arrester provides a clamping level of voltage and protects from lightning surges. Further, this design also responds to source side faults on a bus -tie situation, where there is source capacity on both sides [12].

Some considerations that are to be addressed while incorporating this device are:

1.The detection method should be almost instantaneous and should recognise both symmetrical and asymmetrical faults.

2. The breaker should not contribute to "nuisance tripping", hence, it should be closely tuned for all possible maximum transients by loads such as switching of capacitors and starting of induction motors.

3. It should be able to coordinate with the slower downstream protection devices.

4. The reactor should not cause any resonances with any capacitor banks.

5. There should be a reclosing option.

2.5.3 Controls for the Fault Current Limiter

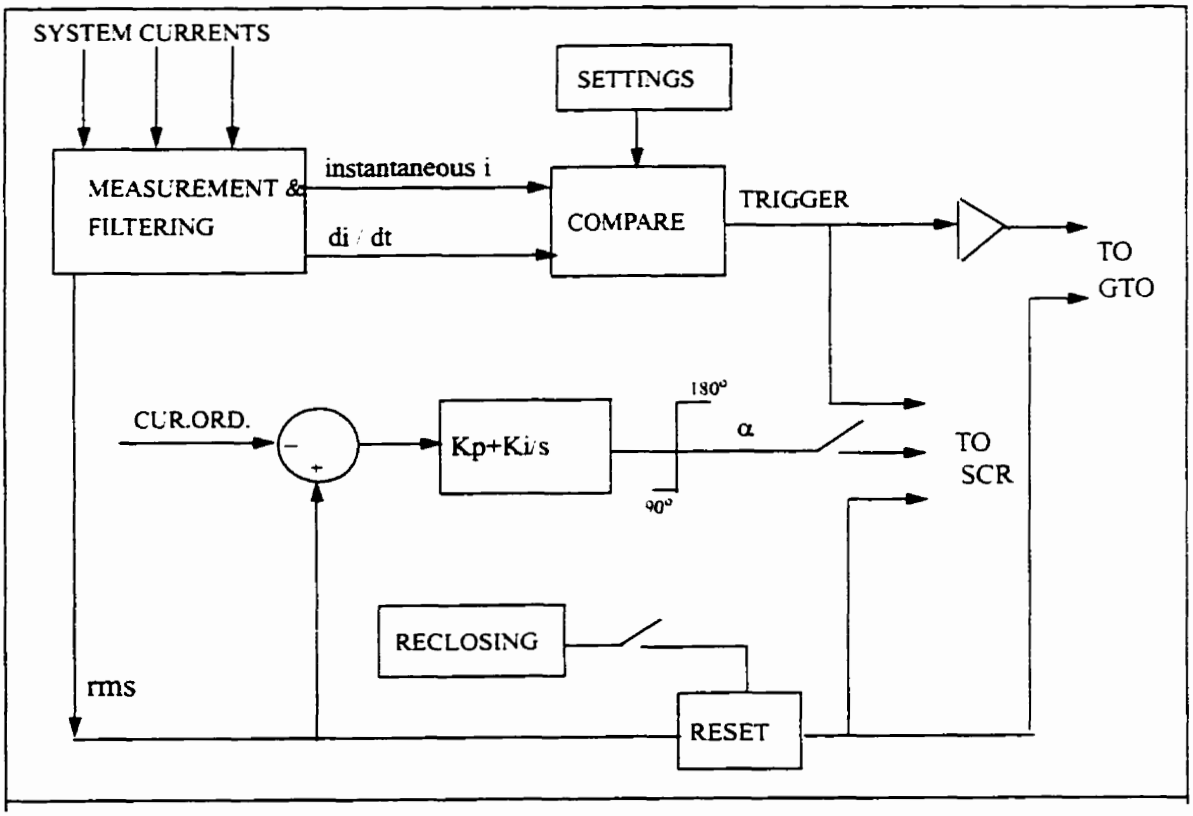


Figure 2.16 : Basic Control Blocks for the SSB-FCL

Detection of a fault is based on both overcurrent measurements and measurement of di/dt. Continuous instantaneous values are recorded and the SSB can be set to operate at any

point on the waveform. Operation is instantaneous and can be achieved in approximately 1/4th of a cycle.

Comparison of the rms value of the load current with the current order is used to generate a value of the phase control angle α for the thyristors; α is kept between 90° and 180°, to achieve symmetrical firing in the inductive thyristor branch. Though it is the reactor which primarily limits the fault current, the alpha modulation by thyristors also helps in reducing the rms values of the current and thus the cost of the reactor.

Resetting could be done by considering the rms value of the current, where, once the fault is cleared the total current is less than the current order for at least one cycle. Automatic reclosing for transient faults is offered as a separate option and is controlled by detection of the first zero crossing of the current as shown in Figure 2.17.

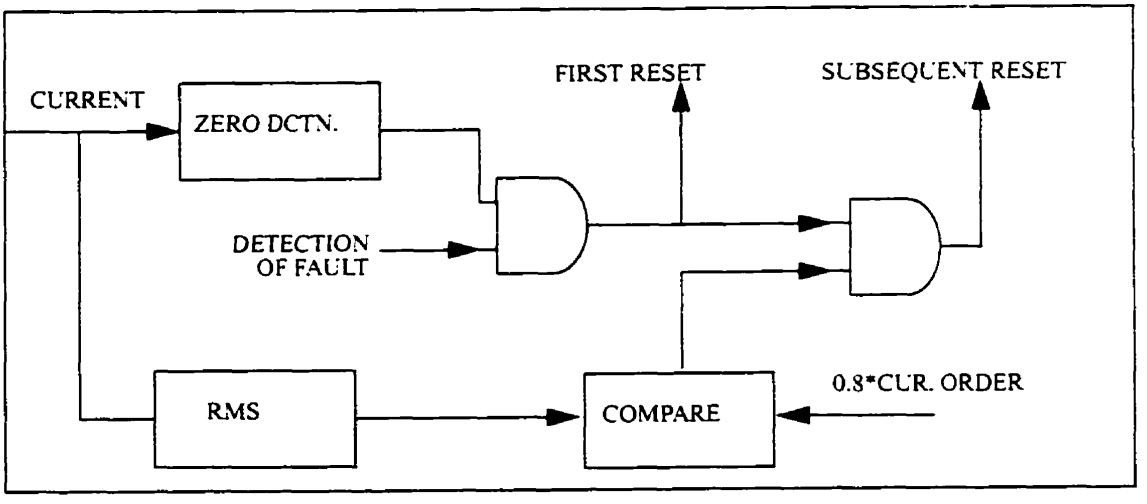


Figure 2.17 : Control Algorithm for Automatic reclosing mode

2.6 RESULTS OF SIMULATIONS

2.6.1 The Simulation System

Simulations were performed on a 11kV/50 MVA system as shown below in Figure 2.19.

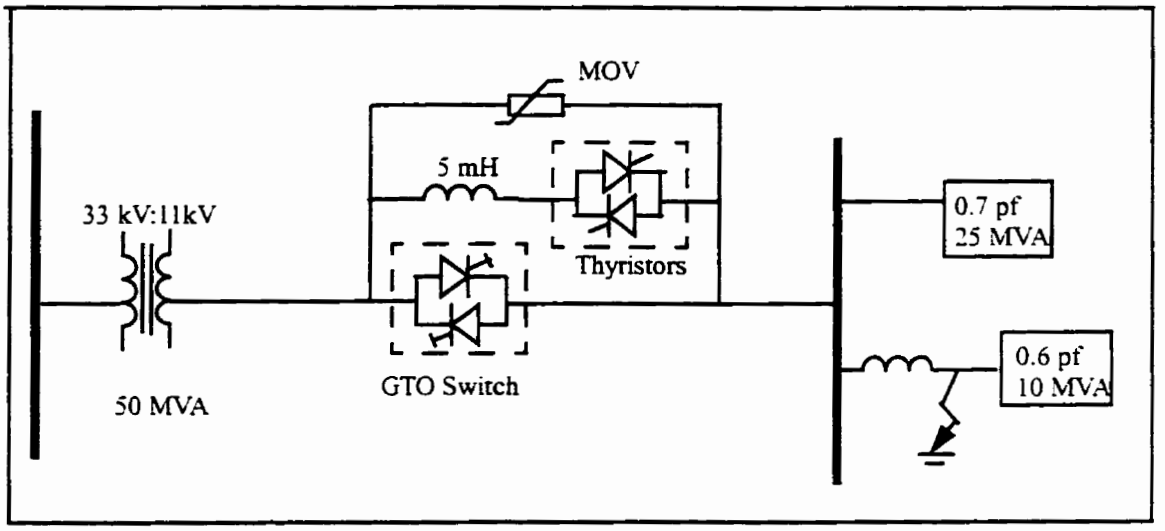
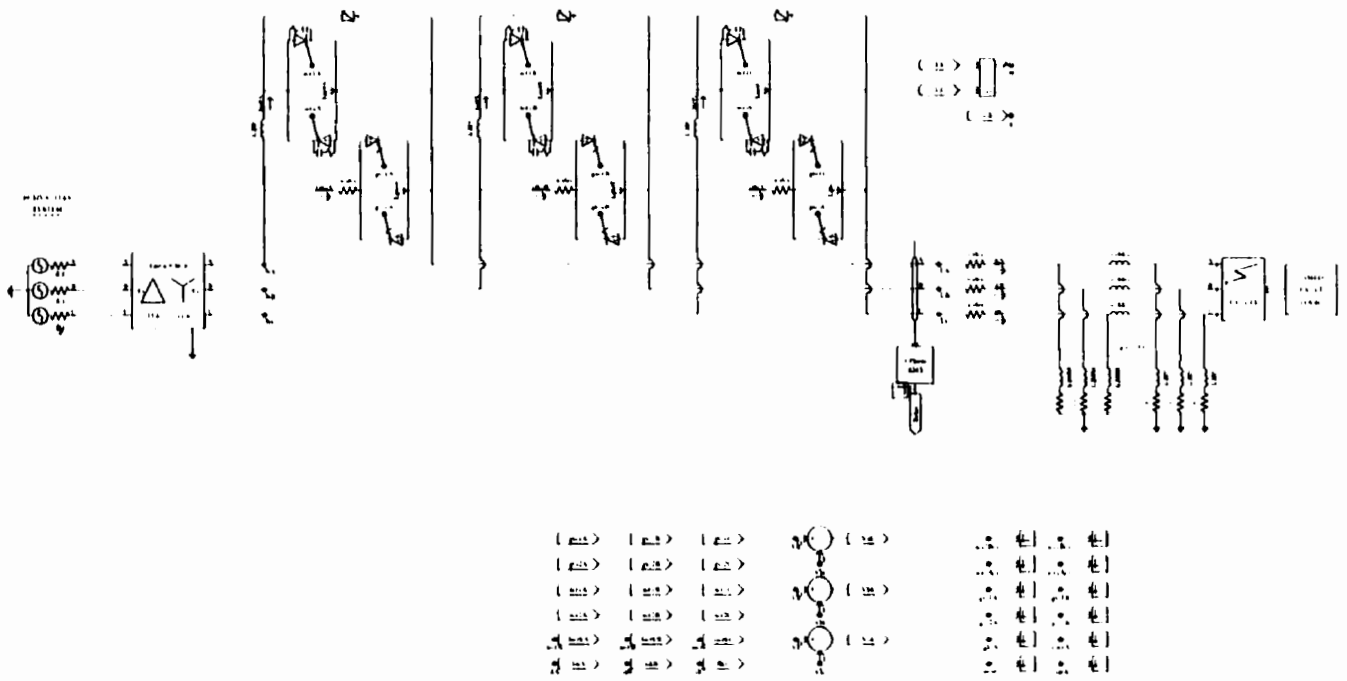


Figure 2.18 : Simulation System for the SSB -FCL

Faults were applied on the load side and a fault level of 6 kA was obtained. The detailed PSCAD circuit is shown in Figure 2.19.

2.6.2 Response of the Breaker

Though the SSB is never used by itself, except in a Bus Tie position [1], this result is used to illustrate the swift action that can be brought about by the GTO branch. A fault current level of 6.0 p.u. is chopped down to zero within 1/4th of a cycle as seen in Figure 2.20.



University of Manitoba, EE Dept.

Solid State Breaker with fault current limiter

Created:	February 23, 1997 (leena)
Last Modified:	August 31, 1998 (leena)
Printed On:	August 31, 1998 (leena)

SS 1

Subsystem #1 of 3

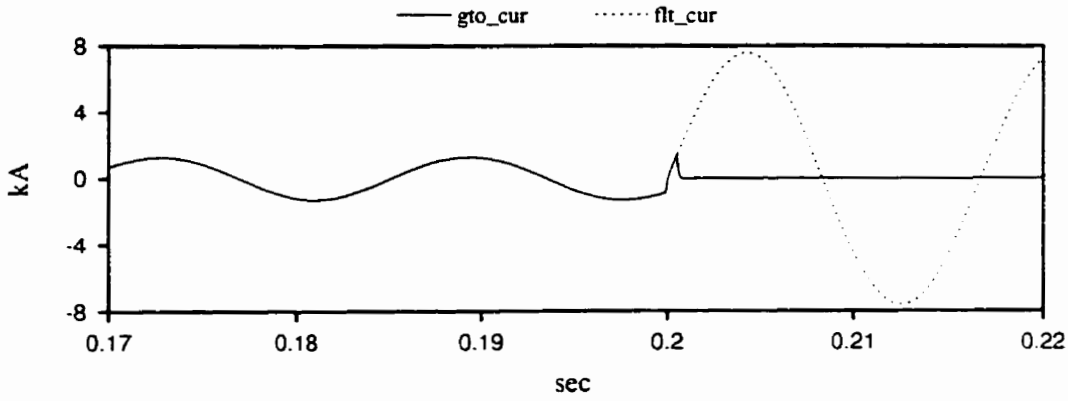


Figure 2.20: GTO Switch Operation during Faults

2.6.3 Response with Current Limiting Reactor

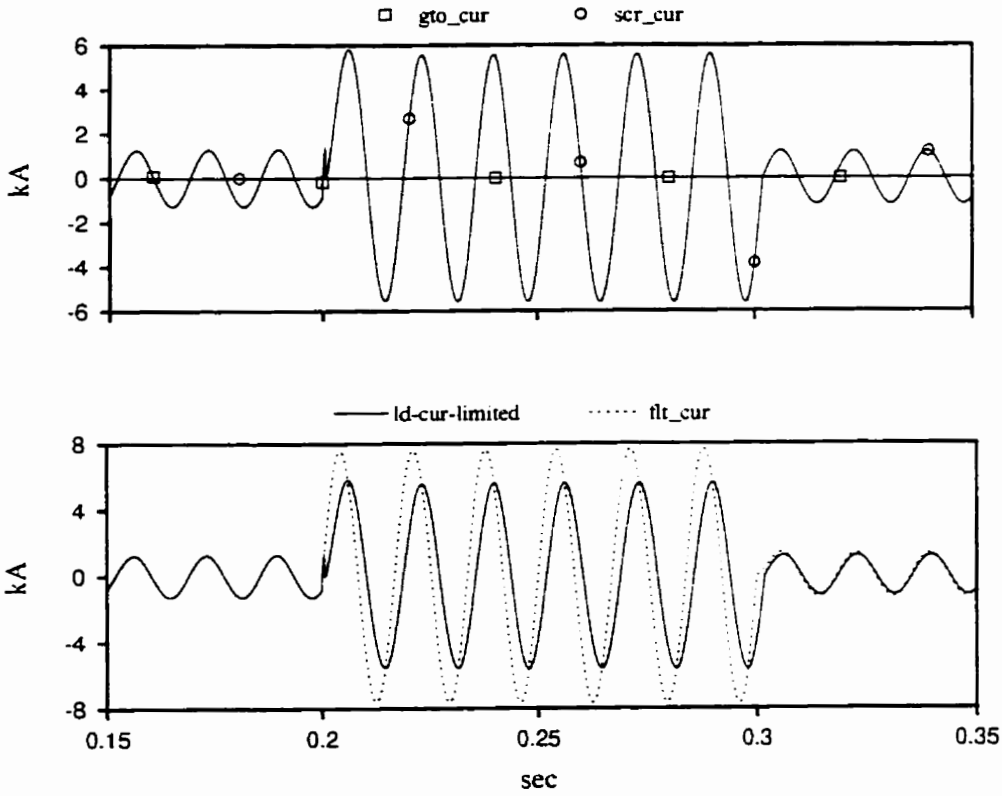


Figure 2.21 : Response with Current Limiting Reactor only

After the GTO switch brings down the current to zero, the resultant surge of high voltage developed across it forces the current through the parallel current limiting reactor (scr_cur

in Figure 2.21) and thus reduces it to around 4 kA from the 6 kA fault level. The high voltage is clamped to a protection level by the MOV.

2.6.4 Response with Current Control by Thyristors

Figure 2.22 shows current controlled to 1 kA. Without α control, the fault current was just limited by the impedance imposed by the reactor alone, and it is seen to be around 4 kA.

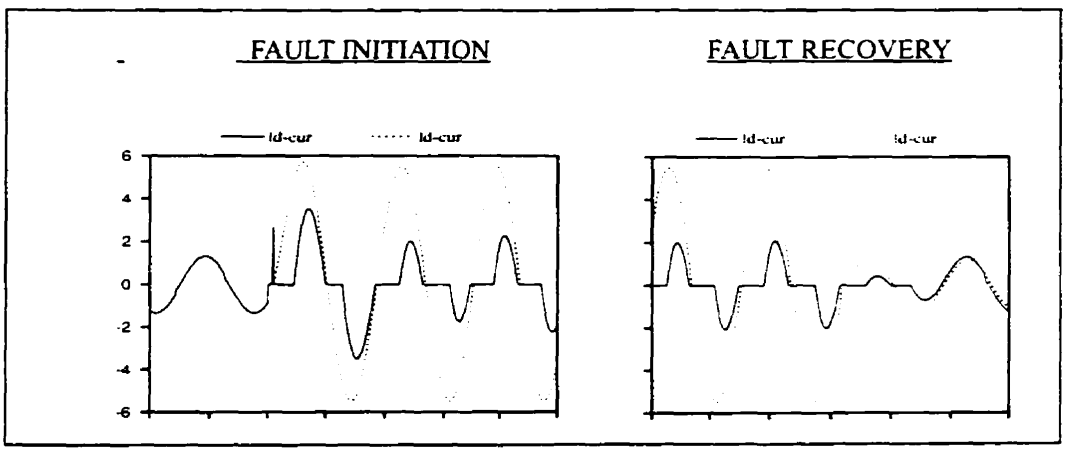


Figure 2.22 : Load current waveforms with current modulation loop

It can be seen that with r.m.s. control for the thyristors, there is a delay of one cycle before the current settled to its new current order. It can also be seen in the first cycle of the fault that the fault current was momentarily zero - specifically for the time the gto controls were solely in operation and had brought down the current to zero - before the thyristor control loop took over. The initial upswings in the currents shown in Figure 2.22 above is because the thyristor loop began in a fully conducting state ($\alpha = 90^{o}$).

2.6.5 Response to Transient Faults

The fact that the thyristor can only be switched off at a natural zero, brings in a delay of one cycle for reclosing. Reclosing can, at best, be had at the first current zero. This is offered as a separate option. Figure 2.23 (a) shows the working of the SSB-FCL in the automatic reclosing mode for a normal fault, where after a single recloser, the Breaker detects the fault again and operates. Figure 2.23(b) shows it working for a transient fault wherein it gets resetted after a cycle.

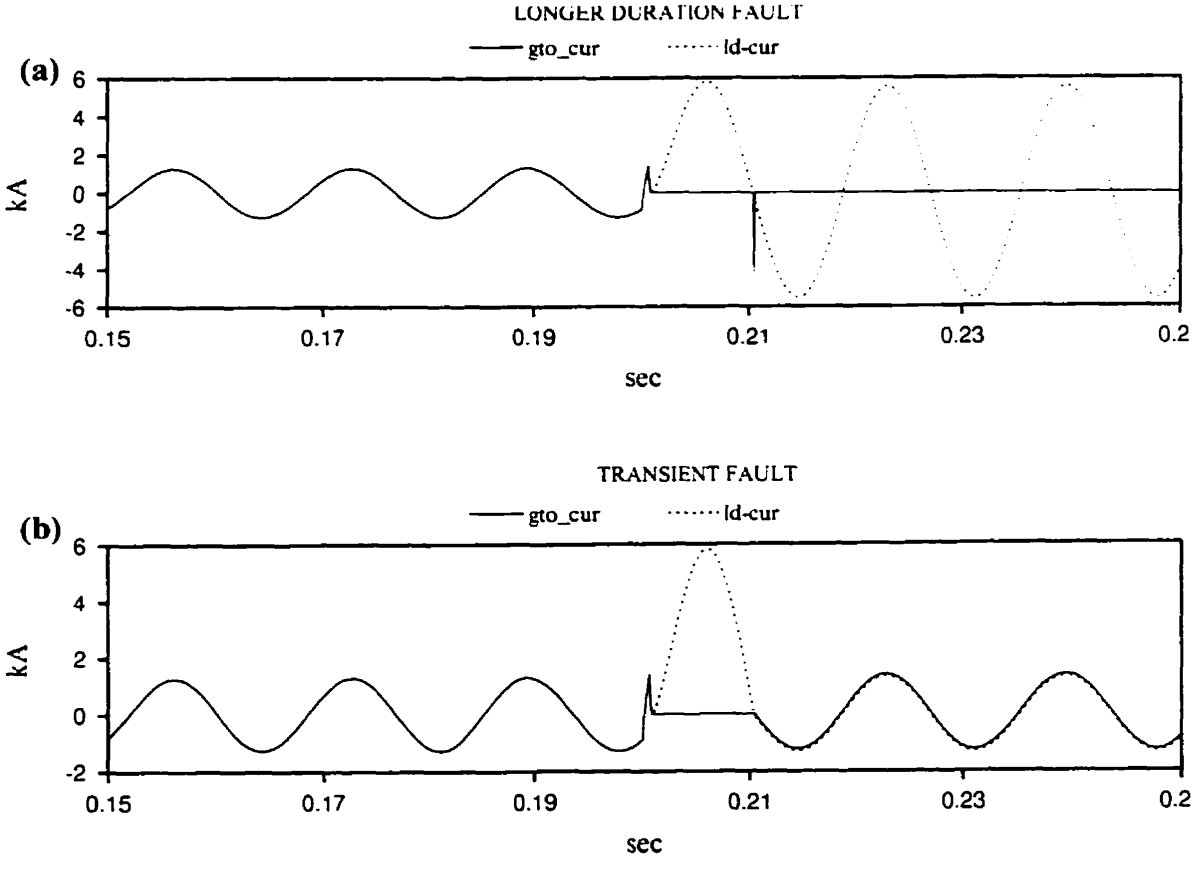


Figure 2.23 : Response of the SSB -FCL in the Automatic Reclosing Mode

2.7 CONCLUSIONS AND FUTURE WORK

Some applications of the Solid State Breaker have been presented in this chapter. Control algorithms to address the various issues in using the Solid State Breaker as a Transfer Switch and as a Fault Current Limiter have been developed. The advantages offered by thyristors over mechanical breakers in a Make before Break type of transfer have been presented. A control scheme for instantaneous detection of voltage sags has been developed. The importance of current zeroes while working with thyristors has been highlighted.

It has been shown that a GTO based Solid State Breaker, when used online in a system within its ratings, can achieve instantaneous current interruption. This can then be used in a Fault Current Limiter to immediately insert a high inductance in series with the line and limit the fault current. With an additional thyristor based current limitation, it can be shown to reduce the rating of the reactor used in a typical Fault Current Limiter.

Future work would involve analysing the effects of particular loads such as capacitors and induction motors on the operation of these devices.

Chapter 3

THE SERIES POWER FLOW CONTROLLER

3.1 INTRODUCTION

This chapter analyses the use of the STATCOM as a Series Power Flow Controller (SPFC). The ability of the STATCOM to generate fast, precise and complex voltage shapes is exploited for various functions such as controlling dynamic power flow, injecting compensating harmonics or even injecting a voltage boost. This chapter studies the use of the SPFC for series reactive compensation.

Reactive compensation by a SPFC in distribution systems can be considered for improving voltage regulation in long distribution lines, as in the rural distribution systems. But since the basic SPFC is used to control the power flow in a line [15], [16], [18], it is first studied here for dynamic power flow control at subtransmission levels, by reactive compensation. The model is then used for voltage regulation, as discussed later in the chapter.

3.2 SERIES REACTIVE POWER COMPENSATION

3.2.1 Basic Theory of Series Reactive Compensation

The SPFC, in its most basic form can supply continuously variable series reactive power

to the distribution line. The theory for series reactive power compensation can be illustrated by the following simple analysis.

The power transmitted through a transmission line can be approximately written as

$$P = \frac{(VsVr\sin\delta)}{Xl}$$

where Vs = the sending end voltage

Vr = the receiving end voltage

Xl = the series inductive reactance of the line

δ = the load angle

If part of this series inductance *Xl*, could be cancelled out by a series capacitance, the power flow in the line can be increased by a factor

$$Xl / (Xl-Xc)$$

where the current is

$$I = \frac{Vs - Vr}{jXl - jXc}$$

and the power transferred can be increased for the same load angle.

This method of increasing power transfer through a line is well known and is typically achieved with the use of series capacitors. The series capacitors are also controlled by thyristor switches (TSC) to vary the capacitance inserted in the line. But the problems with these devices viz. potential resonances with shunt reactors or alternators, switching transients/ overvoltages, reactive power flow control by step changes of capacitance only, make the series capacitors option more difficult for fast dynamic power flow control.

3.2.2 Advanced Static Series Compensation

The Advanced Static Series Compensator, instead, makes use of an injected *voltage* of arbitrary magnitude, frequency and phase, which can affect the power flow along the line.

The voltage could be obtained from a Voltage Source Inverter and the series connection could be obtained by a series transformer. Details of the topology are discussed further in this chapter in Section 3.3, but the basic concept can be seen in Figure 3.1.

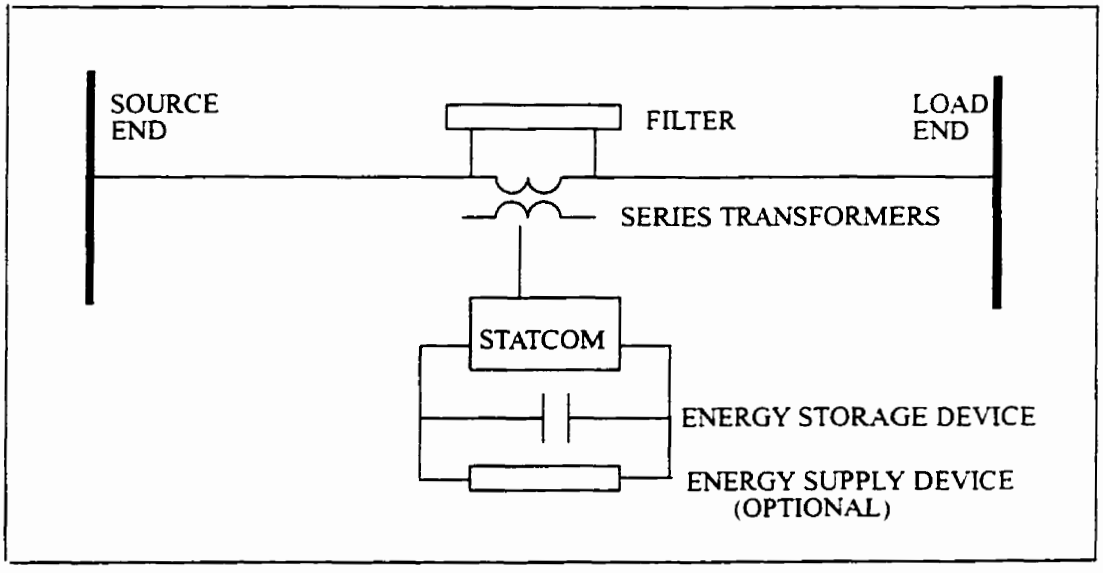


Figure 3.1: The Basic SPFC

Though the phase of this inserted voltage can be controlled to any arbitrary angle, for purely reactive power compensation, this voltage has to be at 90 degrees to the line current in the steady state.

As compared to a capacitor for series compensation, the SPFC is an attractive alternative as it is unlikely to cause resonances with passive components of the system. The size of

the capacitor required here for transitory energy storage is much smaller than that required for series capacitors.The dynamic performance is also tremendously improved.

3.2.3 Phasor Diagrams

If we have a transmission line connecting two strong sources with equal voltages and a constant phase angle δ between them, and if we connect a series power flow controller which injects an arbitrary voltage in quadrature with the line current such that

$$V_{spfc} = \pm j \cdot X_{spfc} \cdot I$$

in Figure 3.2 below,

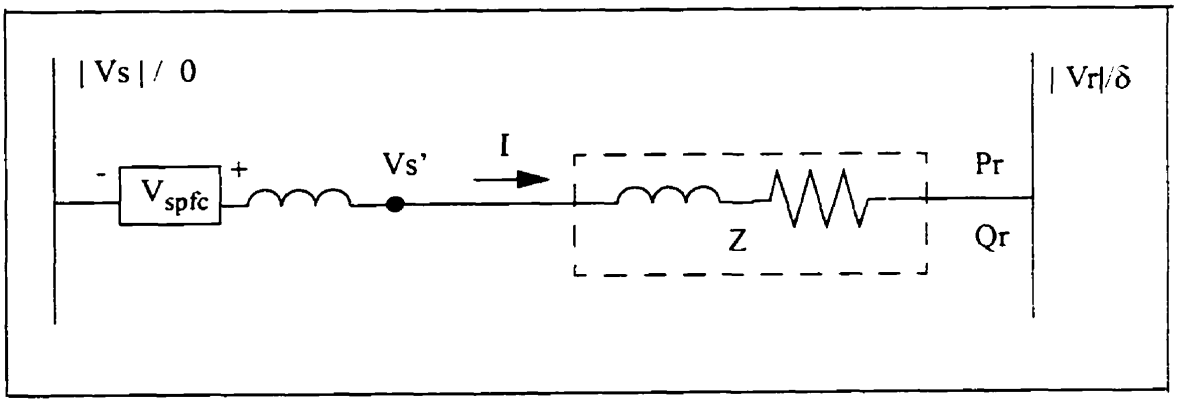


Figure 3.2: Series Power Flow Control by Voltage Insertion

We can write the current to be $I = \dfrac{Vs - Vr}{jXl \pm jX_{spfc}}$

Thus it is seen that the magnitude of the current (and hence the real power flow) can be controlled by the magnitude of the constant "X_{spfc}", which could be achieved by a Voltage Source Inverter. It has to be noted here, though, that the Voltage Source Inverter offers

only the voltage V_{spfc} for controllability and that there cannot be a direct control of X_{spfc}, as in the capacitor, unless the line currents are continuously measured. The power flow equations then differ, as shall be discussed in section 3.2.4.

The magnitude of the inserted voltage is limited by the rating of the device, or the dc link voltage of the inverter and the turns ratio of the series transformer. Since the inserted voltage is in quadrature to the current, it does not draw any real power. It affects the real power flow along the line by changing the magnitude and phase of the line current.

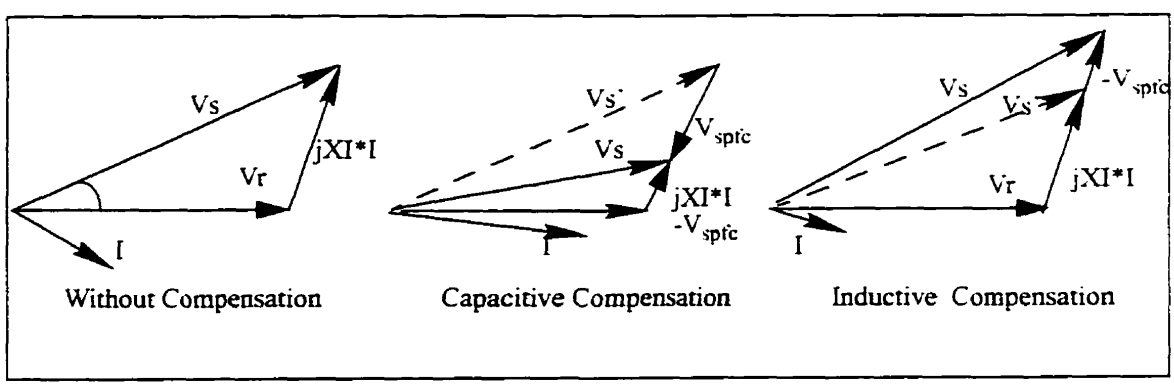


Figure 3.3: Phasor Diagrams for Series Power Flow Control

It can be seen from Figure 3.3 that the inserted voltage V_{spfc} is always in quadrature to the line current, either decreasing the line inductance (capacitive compensation) or increasing it, as in inductive compensation. Inductive compensation is not generally needed, but could be used in fault current limiting situations [1]. It could also be effectively combined with a fixed capacitor to provide a wide range of compensation at reduced sizes [15]. It can also be inferred from the phasor diagrams that there could be no power flow control by purely series reactive compensation if Vs and Vr are in phase, as can be done with a Phase Angle Regulator [15].

3.2.4 Comparison of Various Series Controllers

As an exercise, the operating characteristics of various series power flow controllers were compared for the same value of voltage insertion.

The devices selected are a Fixed Series Capacitor, a Thyristor Switched Variable Series Capacitor (TSC), a Phase Angle Regulator (PAR) and the Series Power Flow Controller (SPFC).

An example system of a 100 MVA transmission system with 100 kV sending and receiving voltages and a inductive reactance of Zl = j0.05 pu is used. Details of the calculations are to be found in Appendix A, but the final power control characteristics for each device, with respect to the load angle (δ) can be seen in Figures 3.4 (a), (b) and (c) below.

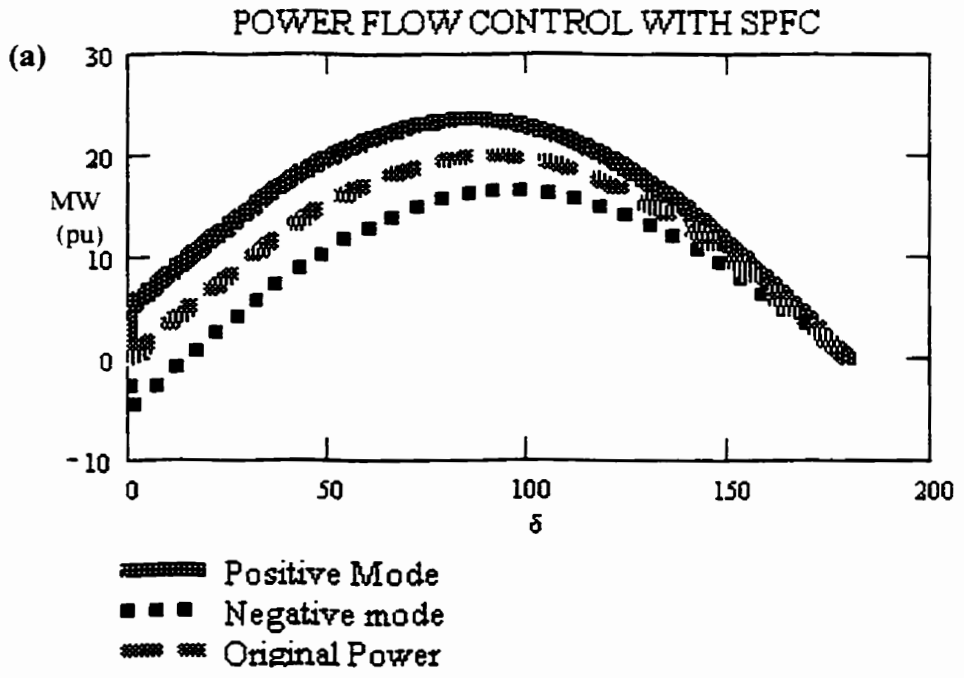


Figure 3.4: Comparison of Series Power Controllers for Various Load Angles (δ)

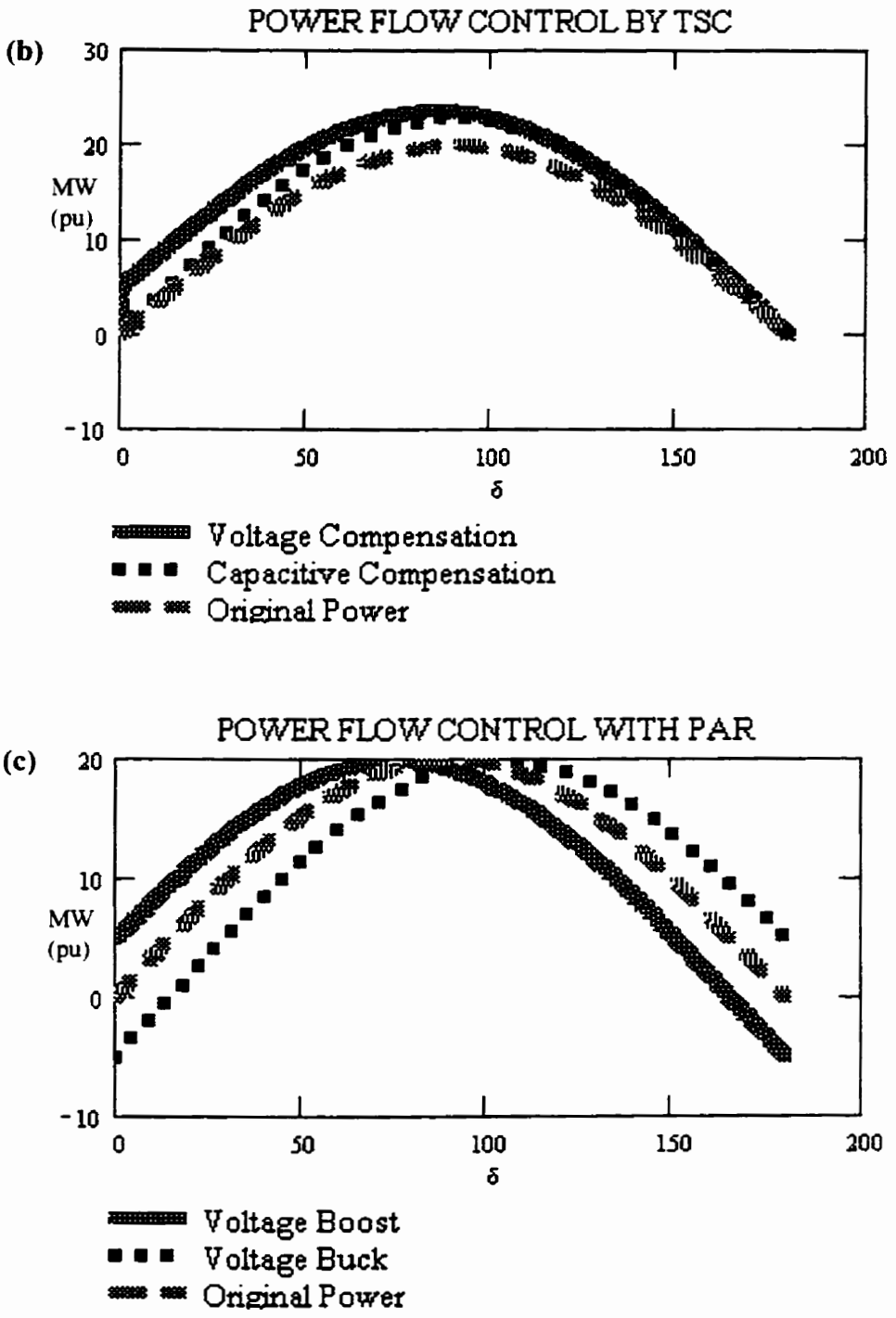


Figure 3.4: Comparison of Series Power Controllers for Various Load Angles (δ)

The three devices were compared on the basis of equal voltage insertion in the line. It can be seen from Figures 3.4(a) and (c) that both the SPFC and the PAR can offer either an

increase or a decrease in power, at any load angle. The TSC will not be able to perform this unless it is biased by inductors. Furthermore, the capacitors are also additionally limited by their ratings, based on the worst line current that may be expected to flow through them. If this is taken into consideration, the nature of power flow characteristic will change, as shown as "Capacitive Compensation" in (c).

The three devices can also be compared [Appendix A] for a fixed load angle (say, 30°) and the result can be seen in Figure 3.5.

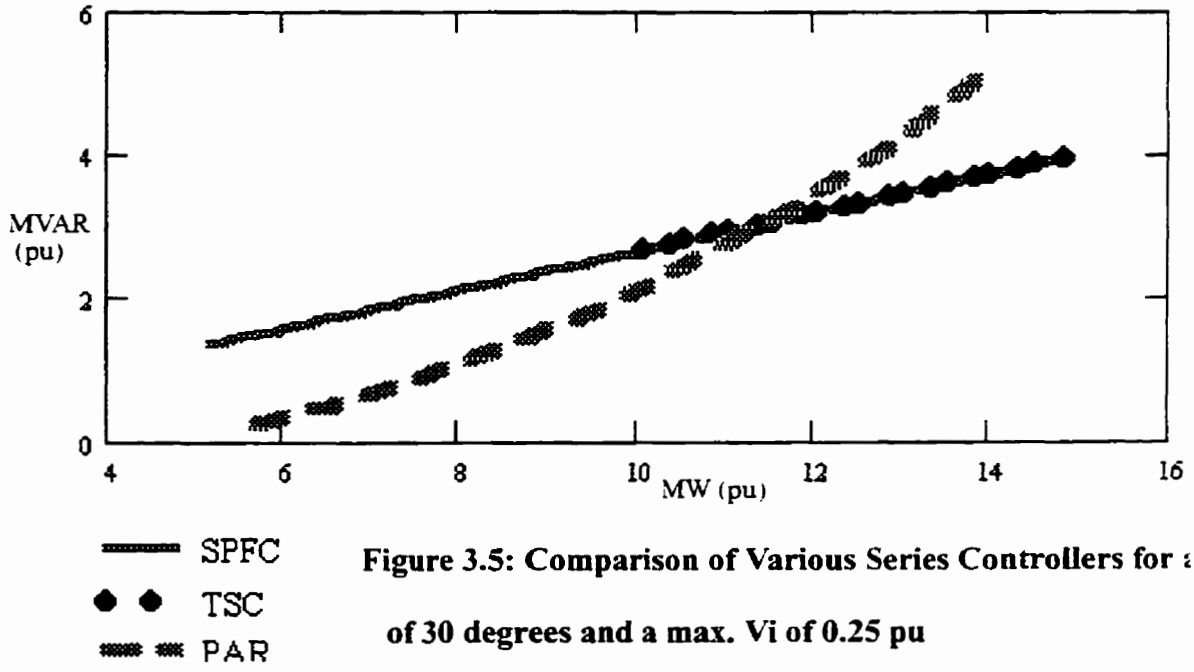


Figure 3.5: Comparison of Various Series Controllers for a of 30 degrees and a max. Vi of 0.25 pu

The series capacitor here, is again assumed to have sufficient MVA to allow constant Vi at any load angle.

There are two caveats to be noted in series reactive compensation. For a line with a lower X/R ratio, increase in current by reactive compensation may lead to an increased drop across the resistance, which is not compensated [17] and further, there may be dangers of overvoltages at higher levels of compensation.

3.3 THE TOPOLOGY OF THE SERIES POWER FLOW CONTROLLER

3.3.1 The STATCOM Configuration

The Voltage Source Inverter used here is a Basic 6 pulse STATCOM. Multipulse configurations can be considered for better harmonic performance.

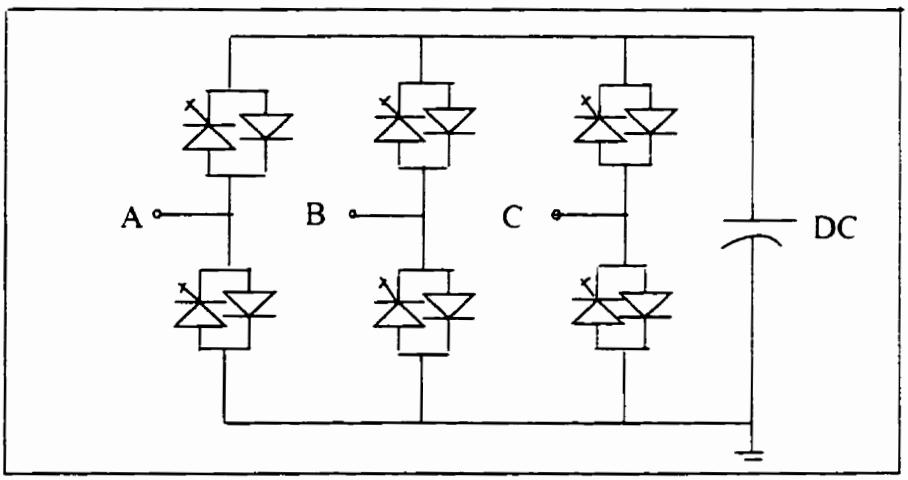


Figure 3.6: A Basic 6 Pulse STATCOM

A 6 pulse STATCOM consists of 6 solid-state switches - here, self-commutated GTO switches- with anti-parallel diodes (Figure 3.6). The firing of each can be controlled to generate a set of three alternating voltages at terminals A, B and C, with controllable amplitudes, phases and frequencies. The capacitor is kept charged to provide the dc stored energy, when necessary.

A sinusoidal pulse width modulation technique [2] is used to control the upper and lower arms of each branch; the PWM switching pattern is determined through the comparison of

a sine wave with a synchronised, high frequency triangular wave. A carrier frequency of 900 Hz. is employed. Neglecting the harmonics, the value of the fundamental voltage (peak) obtained is

$$V_{AN}\angle 0 = \frac{1}{2} \times ma\angle 0 \times Vd = \frac{1}{2} \times \frac{V_{SIN}\angle 0}{V_T} \times Vd$$

and so for phases BN and CN.

where ma = modulation index

= ratio of peak of modulating signal (V_{SIN}) to peak of carrier signal (V_T).

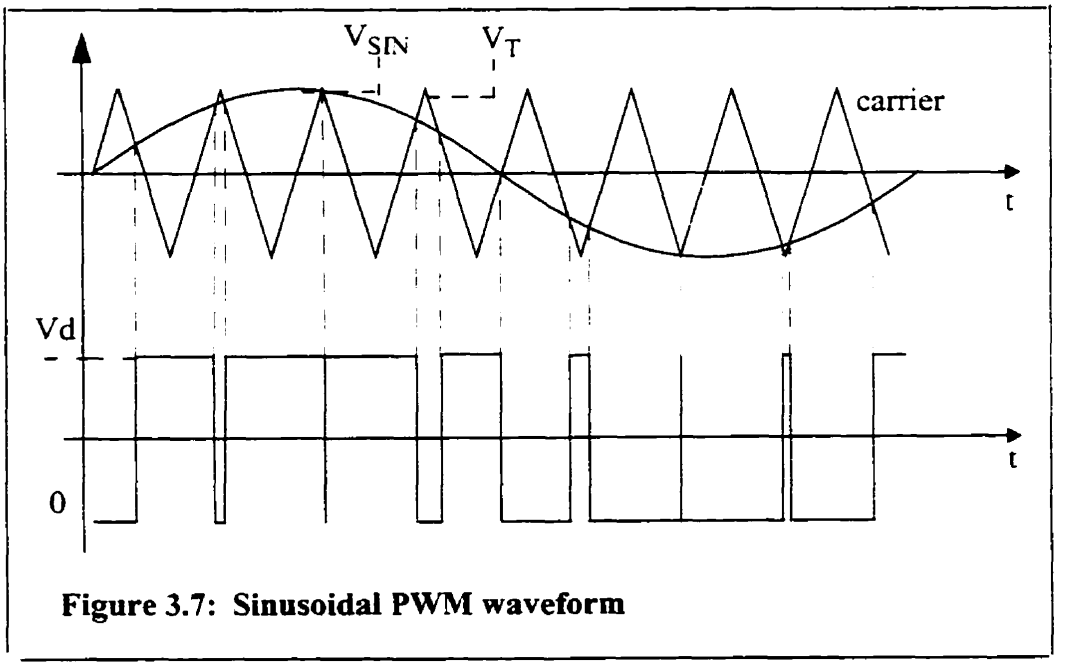


Figure 3.7: Sinusoidal PWM waveform

The instantaneous value of the output voltage is determined by the magnitude of the modulating signal with respect to that of the carrier, which can be controlled and the dc capacitor voltage Vd, which is kept constant. The instantaneous phase is determined by the phase of the modulating signal, which can be also controlled.

3.3.2 The Transformer and Filters

When this voltage is applied in series in the line via an injection transformer, its magnitude is scaled according to the turns ratio (n) of the transformer. Further, the intratransformer connections on the STATCOM side and their polarity also has a bearing on the performance [16].

A floating Y connection [Figure 3.8] with a dc voltage of Vd, gives a primary side peak phase voltage of $(n \cdot ma \cdot Vd/2)/\sqrt{3}$, while a delta connection with the same dc voltage gives a primary voltage of $n \cdot ma \cdot Vd/2$ but has increased line currents on the secondary side. A delta connection prevents zero sequence currents from entering the STATCOM and thus protects it from system faults. Further, three single phase STATCOMs give the best performance in terms of harmonics produced [16], but they involve at least 12 switches, as compared to 6 switches for a three phase type. Therefore, the type of transformer connection shall be decided by an optimization of needs and limitations.

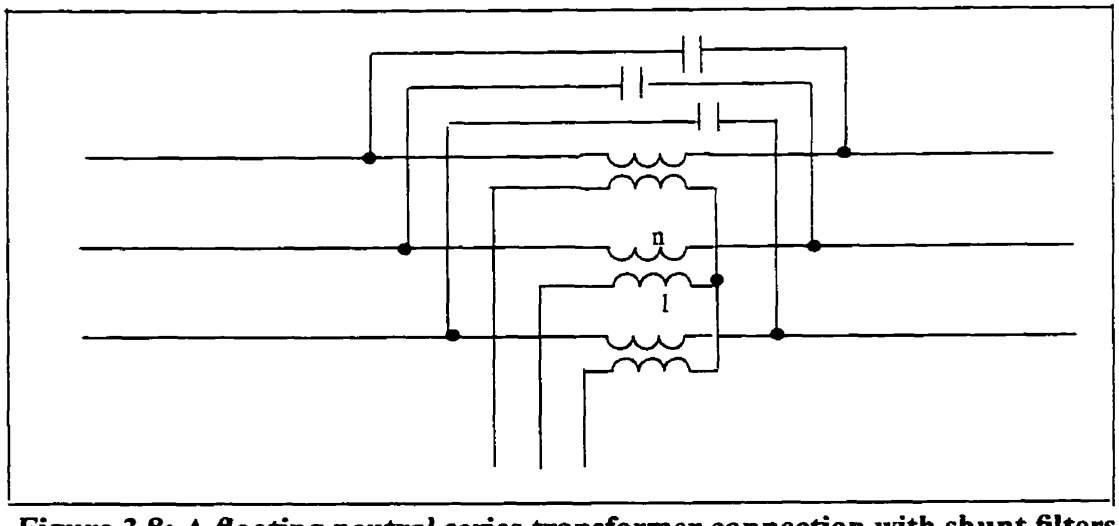


Figure 3.8: A floating neutral series transformer connection with shunt filters

Harmonics could be filtered using passive LC circuits where the L is supplied by the transformer inductance [19]. Significant harmonics are not expected as a suitable PWM firing scheme can be designed (Section 3.3.1). With a switching frequency of 15 *f_o, f_0 being the fundamental frequency of 60 Hz, the major harmonics expected were at 14, 16, 29, 31.... or "$f_o \pm 1$, $2f_o \pm 1$ ..." [2].

For a low modulation index like 0.2, the value of these harmonics could be as high as 1.24 times the fundamental, but they decrease with higher values of modulation index to around 0.6 Vo [2]. Also, the amount of distortion in the load voltage is almost negligible, as can be seen from Figure 3.9. which is at a low modulation index of 0.3.

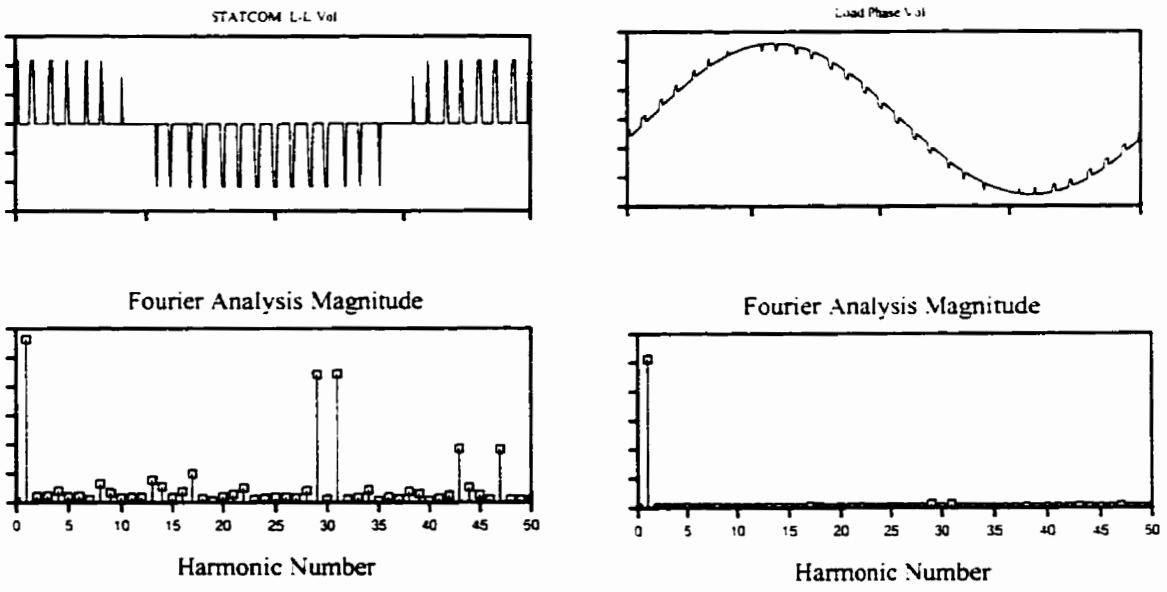


Figure 3.9: Fourier Analysis of Voltage Waveforms obtained in a SPFC operatio

With such considerations, no filters were used in the simulation system and some complexity was reduced.

3.3.3 STATCOM Controls for the SPFC

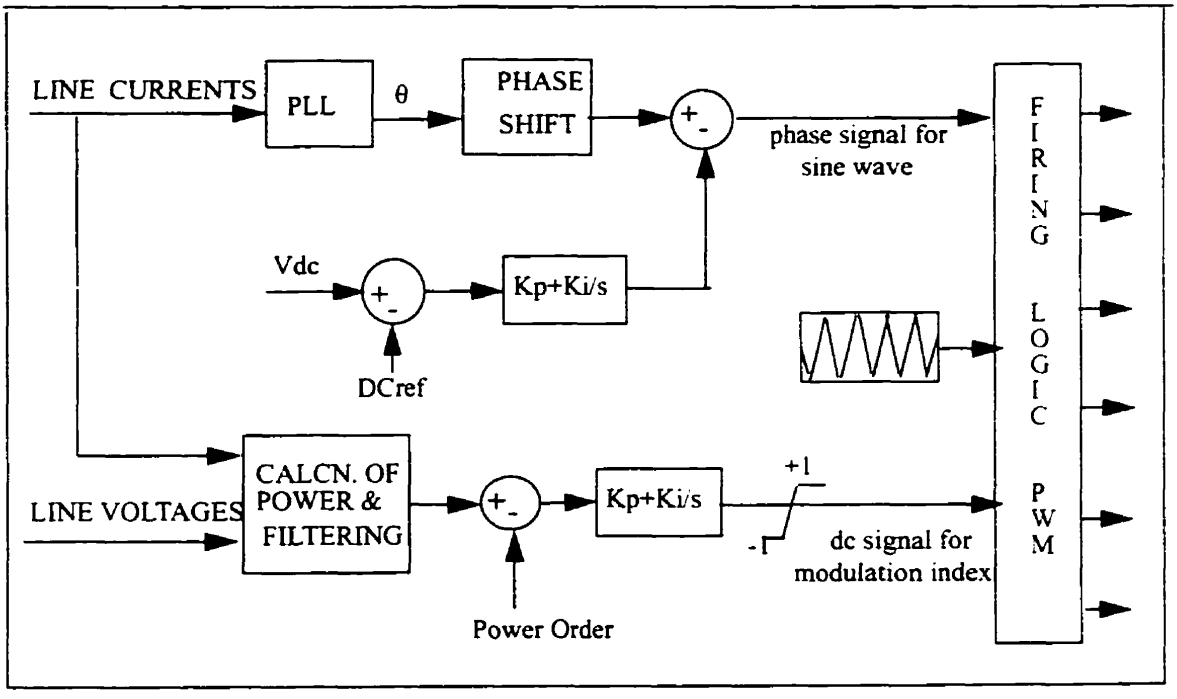


Figure 3.10: Block Diagrams of the SPFC-STATCOM Controls

The line currents are used for synchronisation, as they are ones with the least distortion during SPFC operation and the reference for firing can be easily generated with respect to the line currents. For low PWM switching frequencies, even the triangular signal is kept synchronised to reduce harmonics [2].

The phase of the output voltage of the STATCOM is controlled by adding a phase shift to the phase of the line currents. The charging and discharging of the capacitor is taken to be an indication of real power exchange and therefore the change in dc voltage is fed as an error signal to the phase control. A PI controller drives this error to zero such that the dc voltage is restored to the reference value and the STATCOM voltage is held at almost 90° to the current, except for small differences to compensate for losses [18].

The main power loop is driven by a Real Power signal, computed from instantaneous values of the line currents and voltages and filtered. This is compared to a Power Order and the error is fed through a PI controller as the modulation index (ma), defined in Section 3.3.1. Inductive or capacitive compensation is generated automatically as the polarity of the index changes with the change in the type of compensation required. A hard limit is placed at ma =1, though overmodulation could also be considered [19].

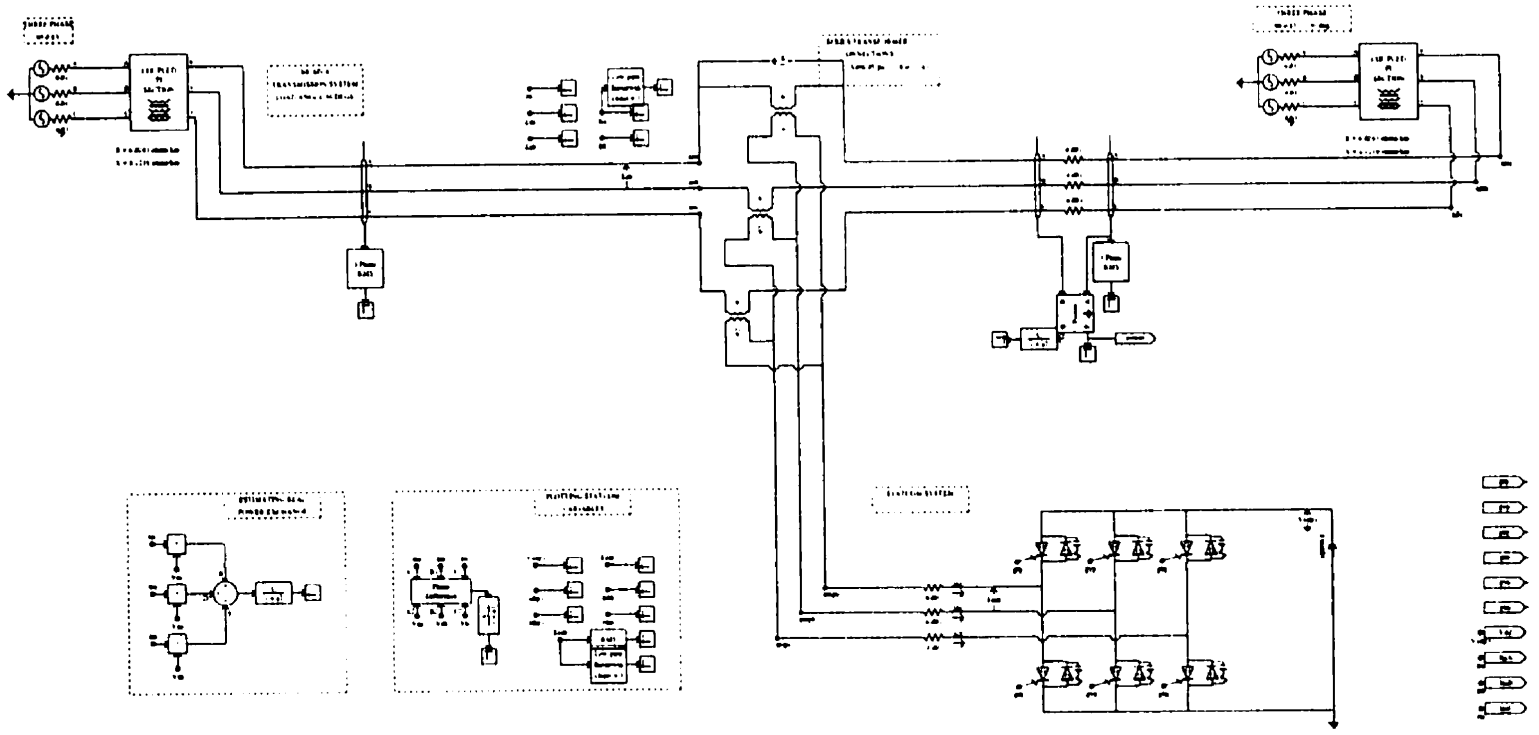
The two PI control loops are decoupled by different time constants, with the DC control loop being much slower. Further, the change in polarity of the index is fed to the gains of the DC Control loop to change the direction of control with a change in polarity of required compensation.The voltages injected are always maintained balanced and synchronised to the positive sequence of the currents.

3.3.4 The Transmission Line System for Simulations

The SPFC is placed at the midpoint of a 200 km line with equal sending and receiving end voltages of 66 kV, with a base short circuit MVA of 300 and a load angle of 30 degrees. The sequence parameters of the line are as below.

PARAMETERS	R(Ω/km)	L(Ω//km)	C(MΩ km)
Pos. sequence	0.02430	0.1219	400.0
Zero sequence	0.12	0.18	410.0

The size of the capacitor was kept 10000 μF to reduce the ripple content. The dc link voltage was maintained to 8 kV by rectification from the line.



University of Manitoba, EE Dept. *THE SERIES POWER FLOW CONTROLLER*	Created: October 14, 1993 (kurs3) Last Modified: September 21, 1998 (leena) Printed On: September 21, 1998 (leena)	*Main System* Subsystem #1 of 2

Using methods outlined in Appendix A, the nominal power flow and the expected range of increase in power is shown in Figure 3.12. The nominal line power at $\delta=30^{o}$ is 87 MW. The maximum voltage that can be injected with a transformer turns ratio of 6.0 / 5.0 kV and a dc voltage of 8 kV is $\left[\sqrt{3}\cdot\frac{(1\cdot 8/2)}{\sqrt{2}}\right]\cdot\frac{6}{5}$ = 5.88 kV r.m.s. and the rating of the SPFC is 18 MVA.

Hence maximum increase in power at any given load angle is shown in Figure 3.12.

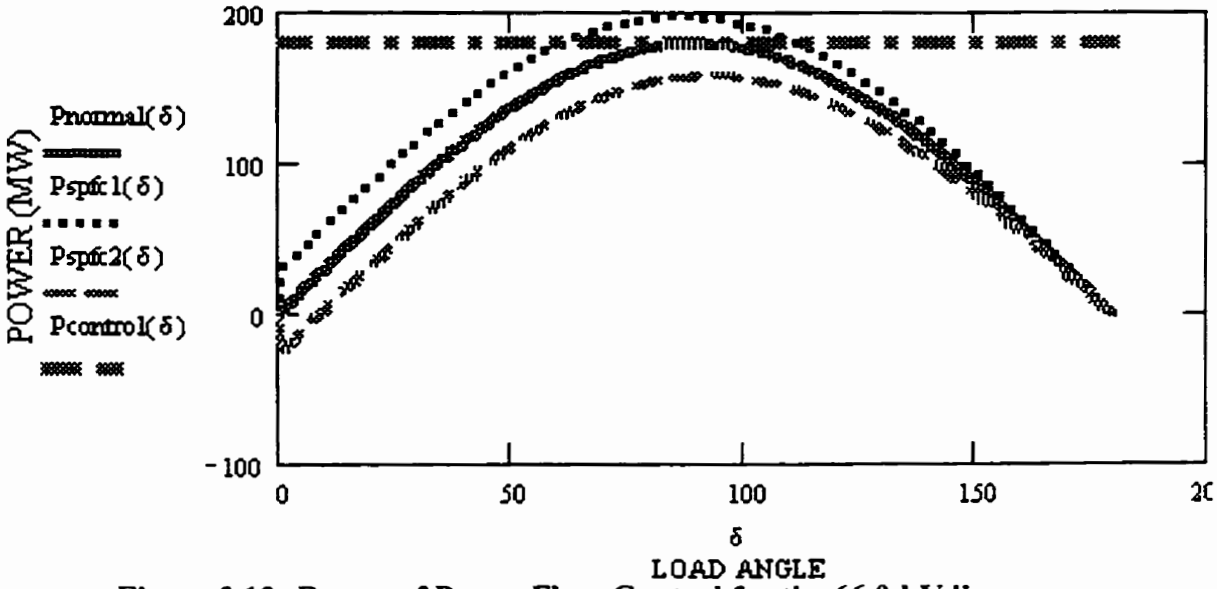


Figure 3.12: Range of Power Flow Control for the 66.0 kV line

Here Pnormal(δ) is the nominal line power at that load angle. Pspfc1(δ) and Pspfc2(δ) show the maximum increase or decrease in power that can be brought about by the 18 MVA SPFC at that load angle. Pcontrol(δ) shows the actual performance of the SPFC controls as the actual value of the power is controlled to that of the Power Order fed to the controls. There could be a greater increase in line power by the same SPFC, if the transformer turns ratio is increased further. But this would also lead to increased currents on the STATCOM side, which is not advisable.

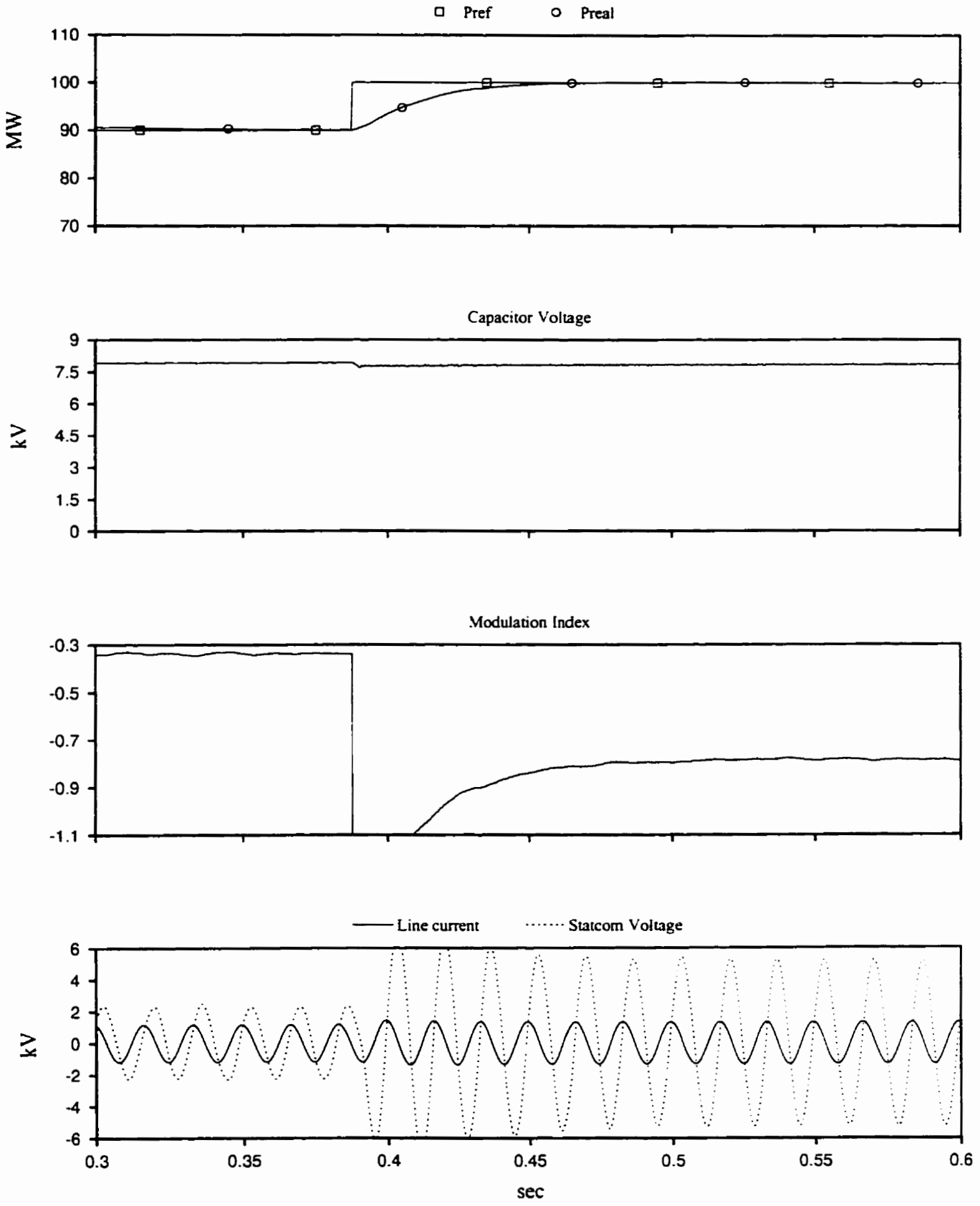


Figure 3.13 : Response of the SPFC to a step increase in Power Order

3.4 RESULTS OF SIMULATIONS

3.4.1 Response to Step Changes in Power Order

It is seen from Figure 3.13 that a substantial increase in transmission power can be brought about by almost no exchange of real power between the SPFC and the line. The capacitor voltage is steady at 8 kV. There seems to be a slight delay in the catching up of 'Real Power' measured in the line as compared to the Pref, the Power Order in Fig. 3.10. But, as can be seen in the plot of instantaneous line current, the change in line current is much faster. The delay in response of Preal can be attributed to the time constant of the power measurement device. Power control by this 18 MVA SPFC for this line can be had from 105 MW (maximum) to 70 MW (minimum), where 87 MW is the nominal value.

3.4.2 Inductive Compensation

As was discussed earlier, the SPFC can also operate in the inductive region as long as it is purely a reactive device. Since the normal operating point is Po = 87 MW, any decrease in power would have to be attained by increasing the impedance in the line by inductive compensation. As is seen in Fig. 3.14, the change from capacitive to inductive is smooth, even if it is from 100% capacitive to 100% inductive. The line current moves from leading the STATCOM output voltage to lagging the STATCOM output voltage, and the power decreases to the minimum of 70 MW.

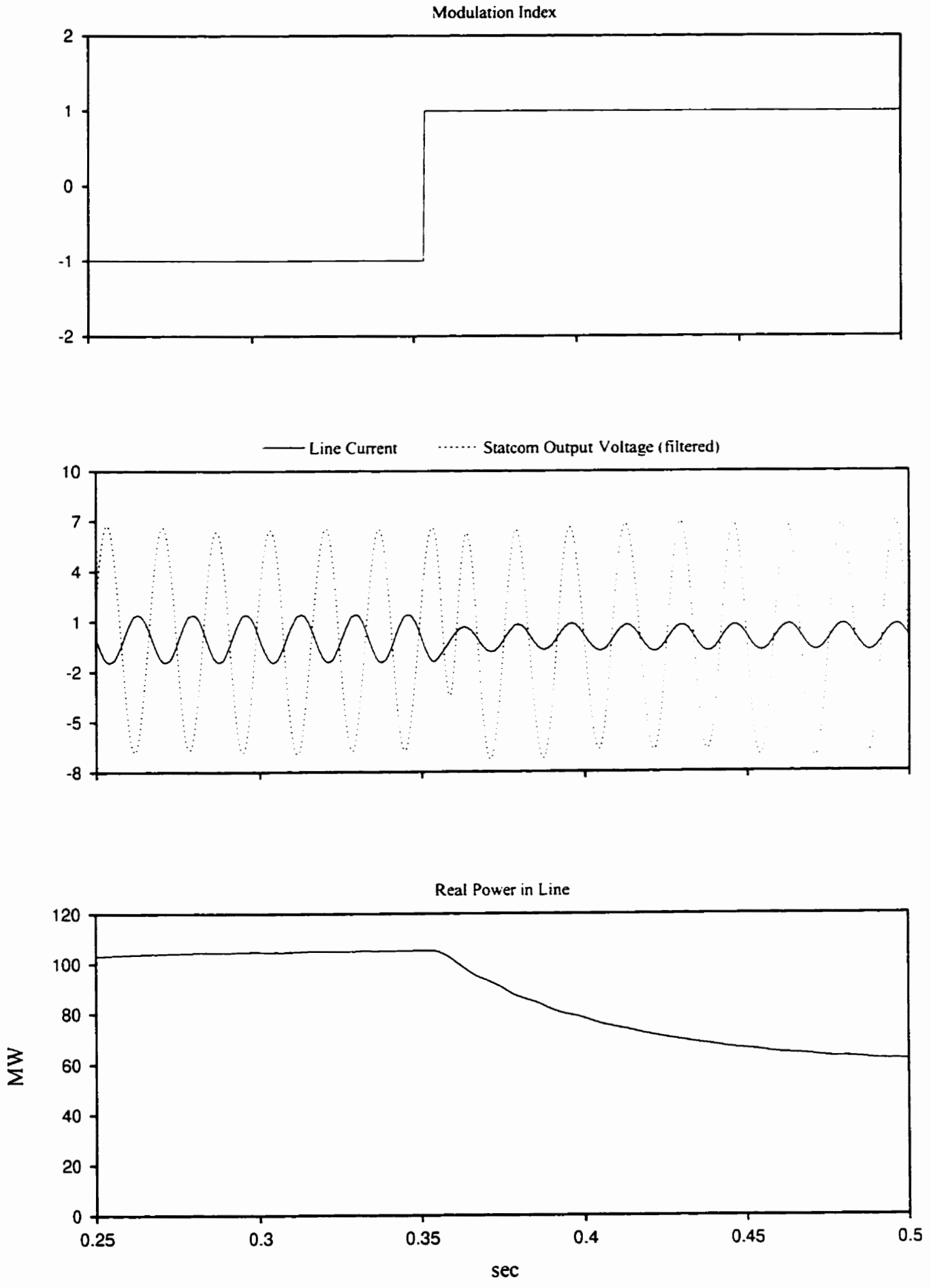


Figure 3.14 : A STEP CHANGE FROM CAPACITIVE TO INDUCTIVE

3.4.3 Response to a Swing in Load Angle

As a test of the robustness of the controls to system parameters, the load angle was given a step change from 30 degrees to 40 degrees. It can be seen that the controllers are stable and power is brought down to the control order.,albeit with a delay in the power measurement transducer.

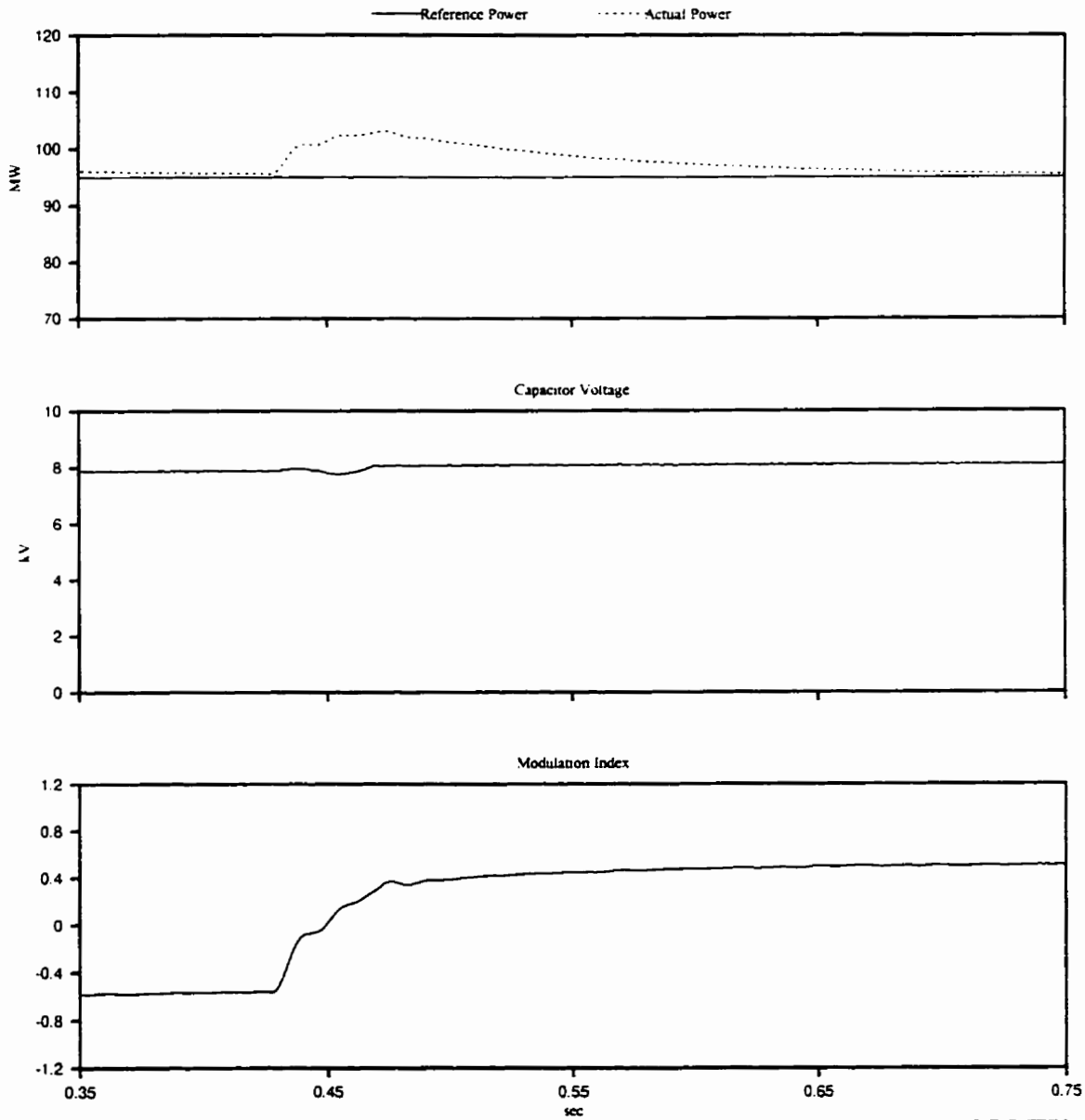


Figure 3.15: Response to a 10 degree jump in load angle at power = 95 MW

3.4.4 Reactive Compensation for Voltage Regulation

As was mentioned earlier, reactive compensation in distribution systems would be of significance only for improving voltage regulation. The voltage at the end of a distributing line is not usually equal to that of the sending end, but is reduced by the amount of voltage dropped across the line impedance. A SPFC can also behave like a series capacitor and reduce the apparent inductive reactance drop in the line and bring back the load voltage to 1 pu or equal to the sending end voltage.

The distribution system used here is a 13.8 kV system with a 20 MVA load of 0.7 pf. The inductive reactance in the line is taken to be an exaggerated 0.38 pu. It can be seen from Figure 3.16 that the load voltage is maintained equal to that of the source.

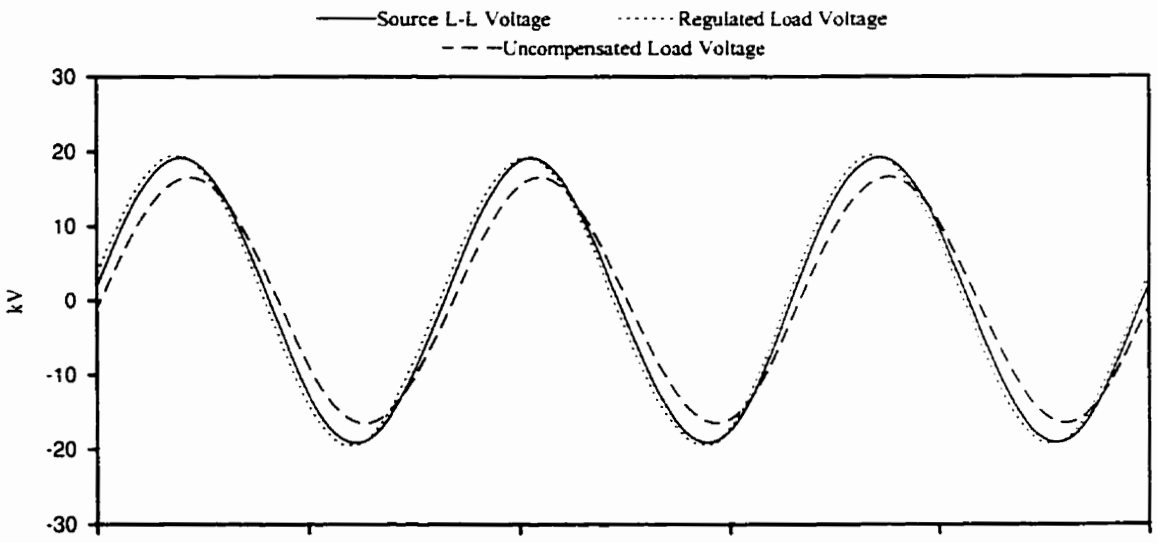


Figure 3.16: Voltage regulation in a distribution system with a SPFC

The load currents in a distribution system can vary widely from time to time, and the SPFC has to work for voltage regulation at any value of load current. Unlike a capacitor, where the required change in series compensation with load current is naturally brought about [22] - I_L*Xc changes with a change in I_L*Xl - the series compensation by a SPFC would have to be *controlled* likewise.

This is done by measuring the load voltages and comparing it to a reference voltage, not dependent on load current, and feeding the error through a PI controller to the modulating signal of the PWM firing scheme. As can be seen in Figure 3.17, this control strategy works even for a change in load current.

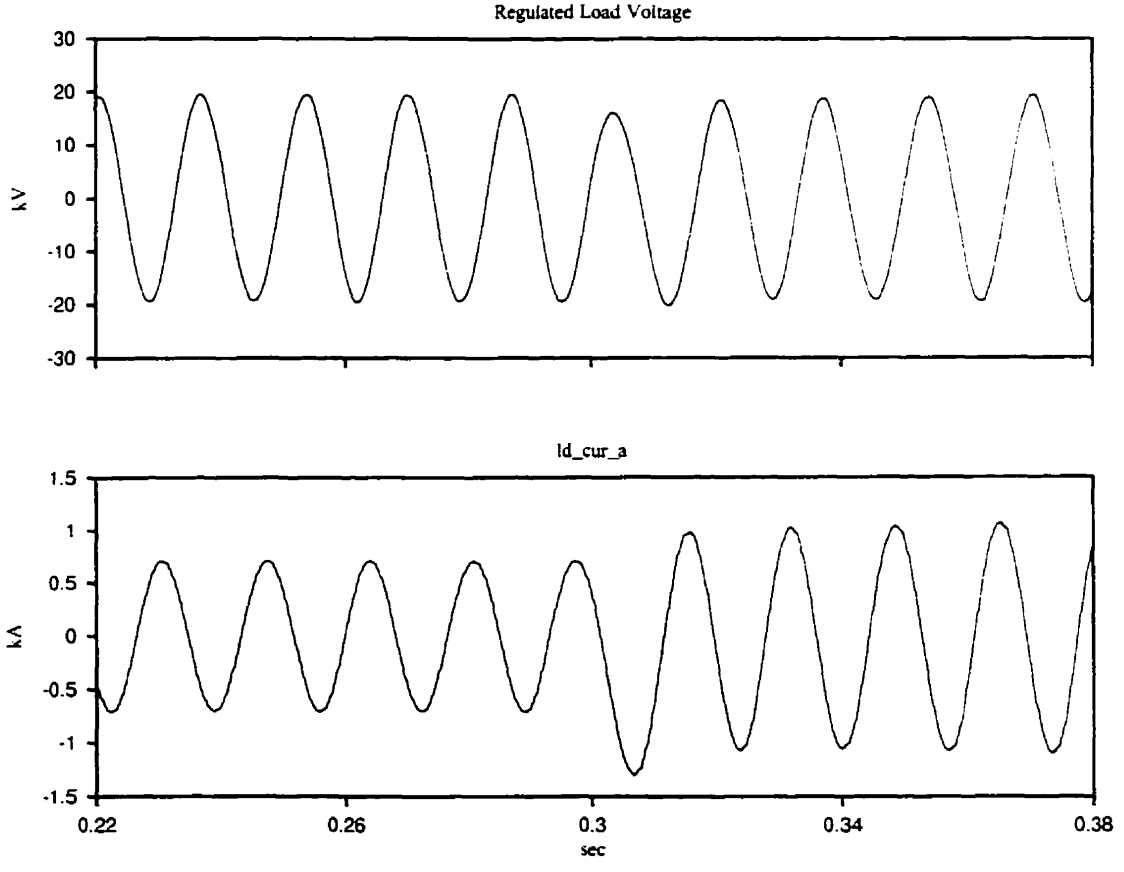


Figure 3.17: Voltage regulation by a SPFC with changes in the load current

3.5 CONCLUSIONS AND FUTURE WORK

A Series Reactive Power Compensator was presented in this chapter and the controls were designed to achieve successful performance. This device can be effectively used for reactive compensation in longer distribution lines.

This chapter has shown the use of reactive compensation for transmitting increased power in a transmission network and also the use of reactive compensation for improving voltage regulation in a distribution network. Furthermore, this topology can also used to compensate for source side voltage sags. This aspect will be discussed in the following chapter. More work would have to be done for SPFC studies to check for adaptivity of the controller to system side faults. A DQ method of control could be studied for improved speed of response of the system.

Chapter 4

THE DYNAMIC VOLTAGE RESTORER

4.1 REQUIREMENTS FOR A DYNAMIC VOLTAGE RESTORER

As discussed earlier in Chapter 1, a Dynamic Voltage Restorer is required to inject a controllable voltage of such a magnitude and phase that the voltage at the customer bus suffers minimum distortion if the voltage on the source side suffers a sag.

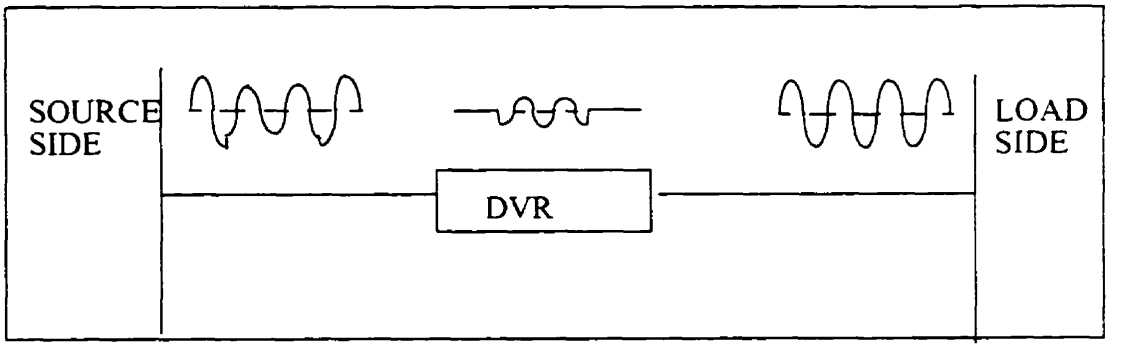


Figure 4.1: Operation of the DVR during system voltage sags

Voltage sags can occur at any instant of time, with amplitudes ranging from 10 - 90% and a duration lasting for half a cycle to one minute [7]. Further, they could be either balanced or unbalanced, depending on the type of fault and they could have unpredictable magnitudes, depending on factors such as distance from the fault and the transformer connections. The DVR is required to detect a such a voltage sag instantaneously and inject a controlled voltage with a certain phase value such that the voltage at the customer bus remains at its original magnitude and phase.

The Series Power Flow Controller (or SPFC) discussed in Chapter 3, could also be used as a DVR to compensate for voltage sags by an addition of it's voltage in quadrature to the line current. But there are limitations to sag compensation by reactive compensation alone, as discussed later in Section 4.2. Ideal sag compensation would additionally require real energy from the DVR. This requirement, though, is for a short duration - the duration of the sag - and therefore, this real energy could easily be obtained from a stored energy source such as a Superconducting Magnetic Energy Source (SMES) [1] or even a very large capacitor. It could also be taken from another point on the system itself, as in the Unified Power Flow Controller (UPFC), which is discussed in Section 4.4.

It is seen that the rating and hence the cost of the device then very much depends on the maximum magnitude and duration of the probable voltage sag expected at that point [1].

Another special requirement for the DVR is that the device has to be of such a design that its impedance during normal conditions is very low. Since the DVR is expected to stay online without functioning for most of the time, it must have low steady state losses. Unlike a strong transmission system, a distribution system has no definite receiving end voltage and exhibits poorer voltage regulation in comparison. Therefore, it is imperative that the DVR has a low impedance online. This is achieved by either keeping the DVR fired continuously or by shorting the transformer connections on the DVR side if it is not working. The secondaries are also immediately shorted on detection of a load side fault to protect the DVR from high current surges.The shorting switch could be another solid state

switch as discussed in Chapter 2.

This chapter discusses some models for dynamic voltage restoration by series injection of voltages, whether reactive or real, and keeping into consideration the requirements outlined in this section.

4.2 THE SERIES POWER FLOW CONTROLLER AS A DVR

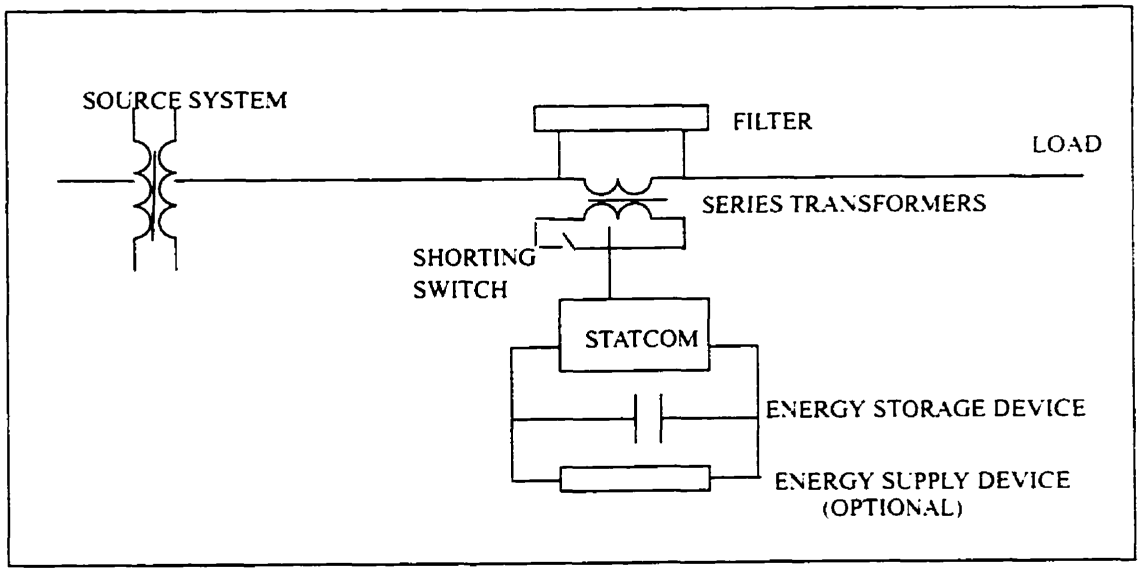


Figure 4.2: The SPFC - DVR

4.2.1 Discussion on Feasibility and Limitations

As a purely reactive compensator, the SPFC is limited in it's role as a DVR; it can only *mitigate* the effect of a source side voltage sag by compensating for the reactive voltage

drop in the line. Further, if the X/R ratio of the line is low, it can be even less effective due to the increased voltage drop across the resistance, which would then draw even more reactive power [17].

The SPFC also does not ensure that the phase of the load voltage is maintained in phase with the voltage on the source side. In Figure 4.3 (a) below, if the injected voltage Vin is held at 90 degrees to the current, as in the SPFC, the load voltage is no longer in phase with the source side voltage though it may get restored to it's original value [Fig 4.3 (c)].

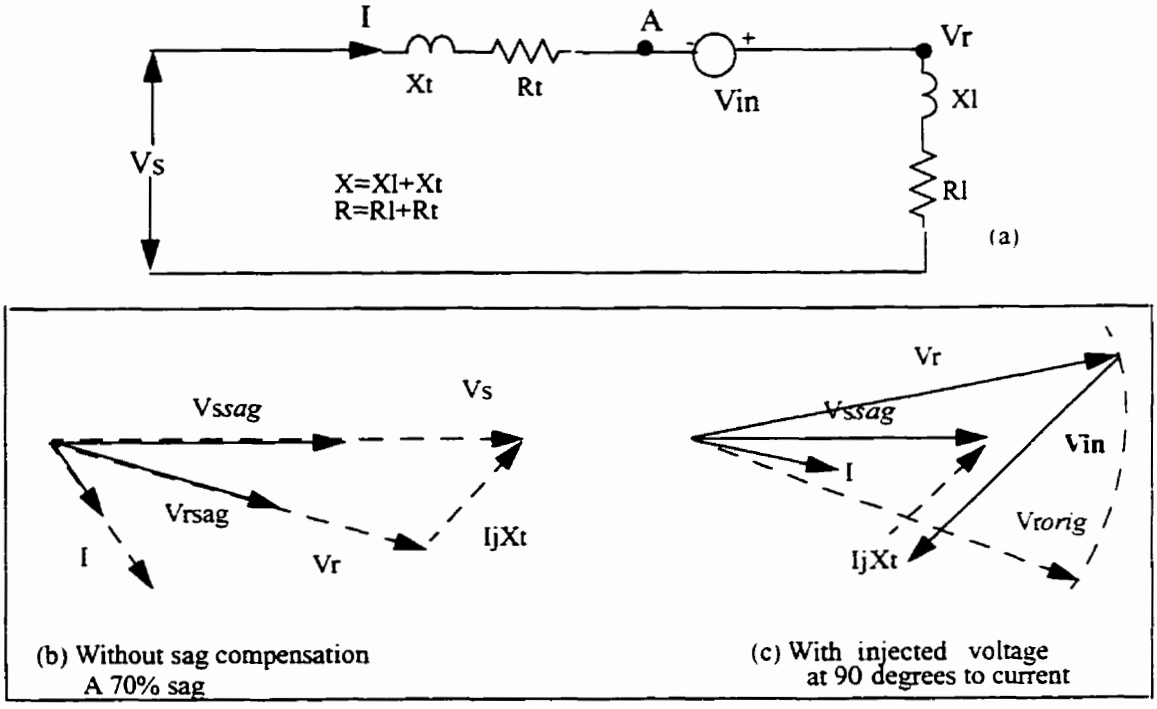
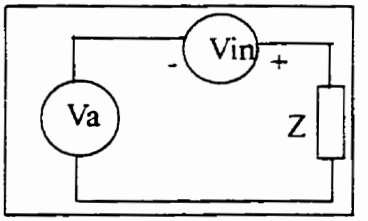


Figure 4.3: Phasor Diagrams for Compensation of a Sag

But if the magnitude of the load voltage is the only consideration, the reactive device SPFC -DVR can also completely compensate for certain value of sags within limitations. The formulae governing the effectivity of the SPFC as a DVR are deduced next.

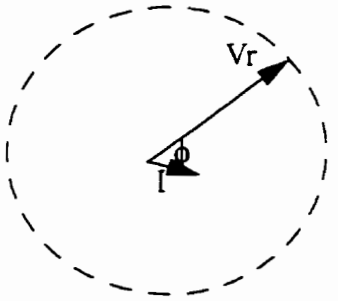
4.2.2 Formulae for Sag Compensation by SPFC-DVR

Consider a simplified version of the circuit shown earlier where Va is the source side voltage as seen by the load and therefore, Va is the voltage undergoing a sag.



(a) The Worst Sag that can be Compensated by a SPFC-DVR:

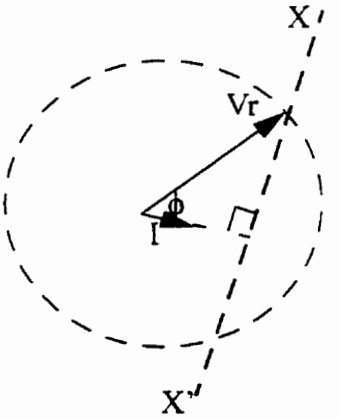
If the SPFC -DVR is required to restore the load voltage to 1 p.u. without considering the phase and if the source side parameters are neglected (measuring the voltage only at point "A" in Figure 4.3 as Va), we can draw the phasor diagrams after compensation as,



1 p.u.

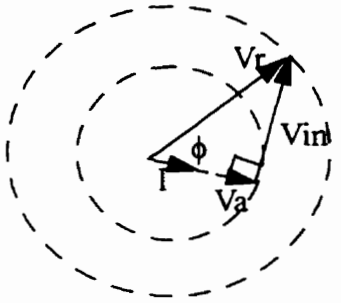
where Vr is the restored voltage at any arbitrary phase. But I is the restored current at a constant phase diff. with respect to Vr, since the load is constant and $Vr = I^*(Rl + jXl)$

If Vin is the injected voltage constrained to be at 90° to the line current, then the locus of Vin is line XX' and the sagged voltage Va would be any point on any circle intersecting the locus, such that $Vr = Va + V_{spfc}$



1 p.u.

Then the worst sag that can be compensated by V_{spfc}, is the smallest circle of Va touching the locus XX'.



1 p.u.

from which it can be deduced that that the worst voltage that can be compensated against is

$$|Va| = |Vr| \cdot \cos\phi$$

where the Vin required is

$$|Vin| = |Vr| \cdot \sin\phi$$

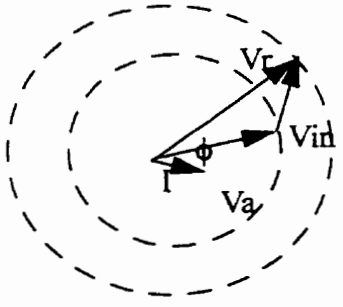
Or the worst sag that can be compensated is

(1- cos ϕ) p.u.

The foremost point that can be inferred from this is that the SPFC is more effective at poorer power factors. In fact, if the power factor is 0, theoretically, almost any magnitude of sag can be compensated for!

(b) Limitation of Rating:

The above analysis assumes that we have an unlimited magnitude of injected voltage with the only constraint being that this voltage is held in quadrature to the line current. But, in fact, we also have a limitation on the maximum magnitude of the injected voltage that can be delivered by the SPFC-DVR.



1 p.u.

Then, if we have a constant power factor load and a maximum Vin, |Vin| < |Vr |sin ϕ, the worst sag that can be compensated for is

$$|Va| = \sqrt{|Vr|^2 - (2 \cdot |Vr| \cdot |Vin| \cdot \sin\phi)}$$

These, and other issues are demonstrated in the simulation studies for the SPFC -DVR.

4.3 SIMULATION STUDIES FOR THE SPFC DVR

4.3.1 The Simulation System

Simulations were performed on typical distribution system rated at 13.8 kV with a load of 12 MVA, 0.8 p.f. (Figure 4.4). Each single phase transformer for the DVR was rated for 3 MVA, 6.0 /4.0 kV with a low impedance of 0.05 p.u on it's base.The secondary windings of the transformers were made into a delta connection, to prevent zero sequence components from entering the STATCOM. Faults were applied on a parallel 30 MVA system to induce the necessary levels of sags on the main line.

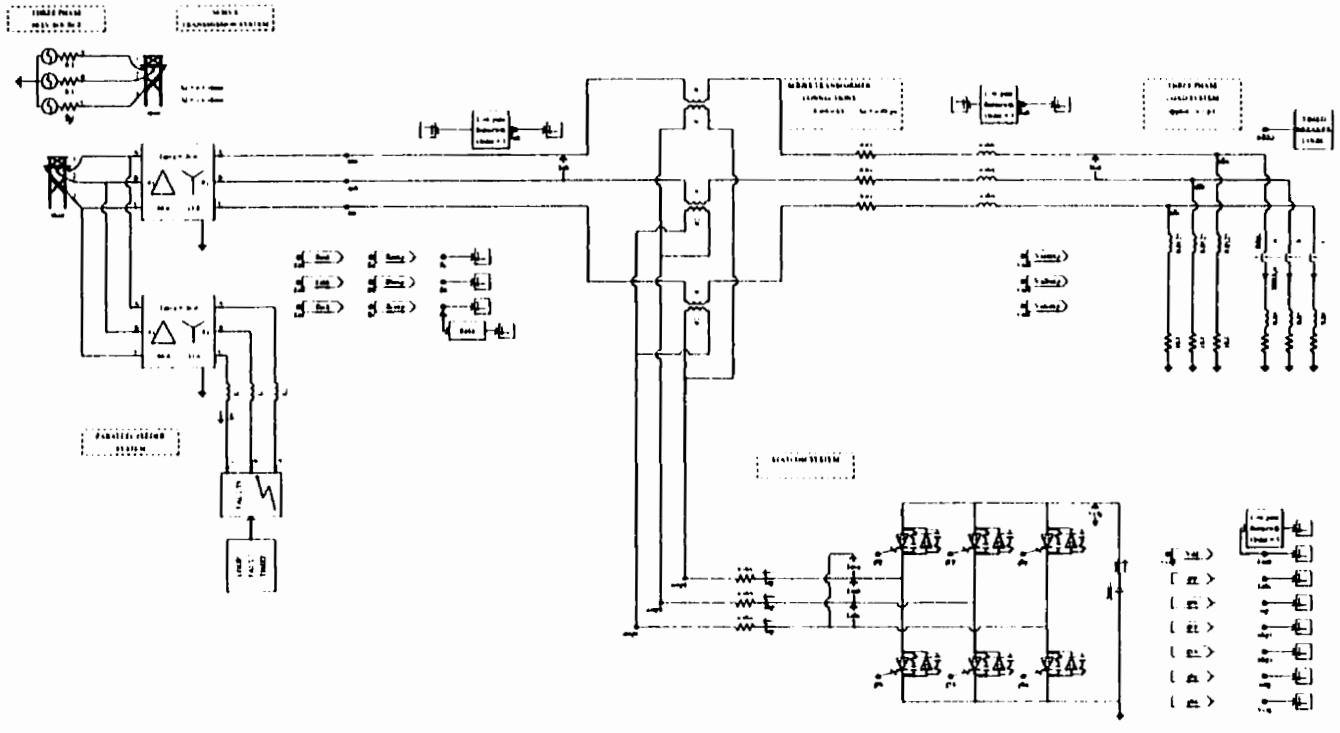
The capacitor on the dc link was precharged to a voltage of 5 KV and then maintained to that level. With a capacitor size of 2000 μF, the energy stored is 25 KJoules or approximately 1.5 MVA, if the period of discharge is taken to be one cycle or 16 msecs. As a pure SPFC-DVR, this level of energy is expected to remain unchanged except for dynamic operations.

The maximum rms line- line voltage that can be inserted by the SPFC-DVR, is at ma =1

$$Vin = \frac{\sqrt{3} \cdot ma \cdot Vdc}{2 \cdot \sqrt{2}} \cdot n$$

Here, with a Vdc of 5 kV and a transformer turns ratio of n = 6 / 4 kV, the maximum inserted voltage is 4.6 kV and the rating of the device is approximately

3*Vin*|I| = 8.26 MVA.



University of Manitoba, EE Dept.

THE SPEC DVR

Created:	October 14, 1993 (kurs3)
Last Modified:	September 21, 1998 (leena)
Printed On:	September 21, 1998 (leena)

Main System

Subsystem #1 of 2

4.3.2 Controls for the SPFC -DVR

The controls for the SPFC -DVR are almost similar to that of the SPFC itself. The only difference is that the modulation index is controlled by a voltage error measurement, rather than a power error, as in the SPFC.

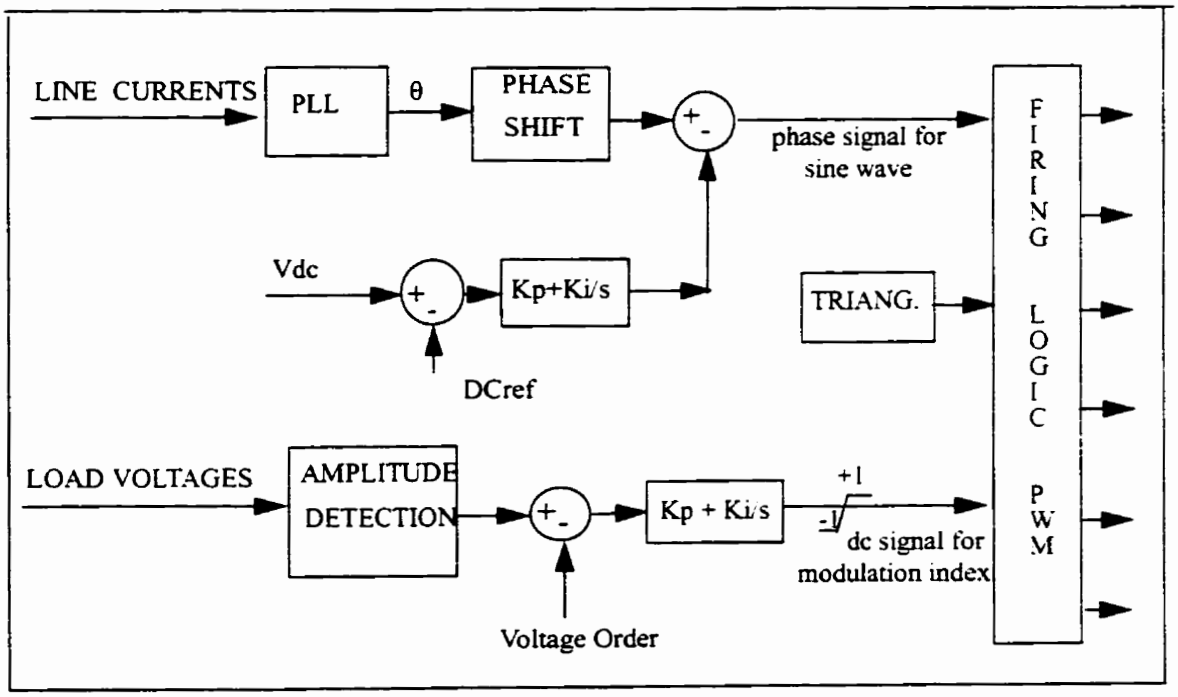


Figure 4.5: Block Diagrams of the SPFC-DVR Controls

4.3.3 Results of Simulations:

The following pages illustrate the effectivity of the SPFC -DVR for various sags under various load power factors. It can be seen from Figures 4.6 (a) and (b) that a higher magnitude of sag can be compensated for only if the load power factor is poorer.

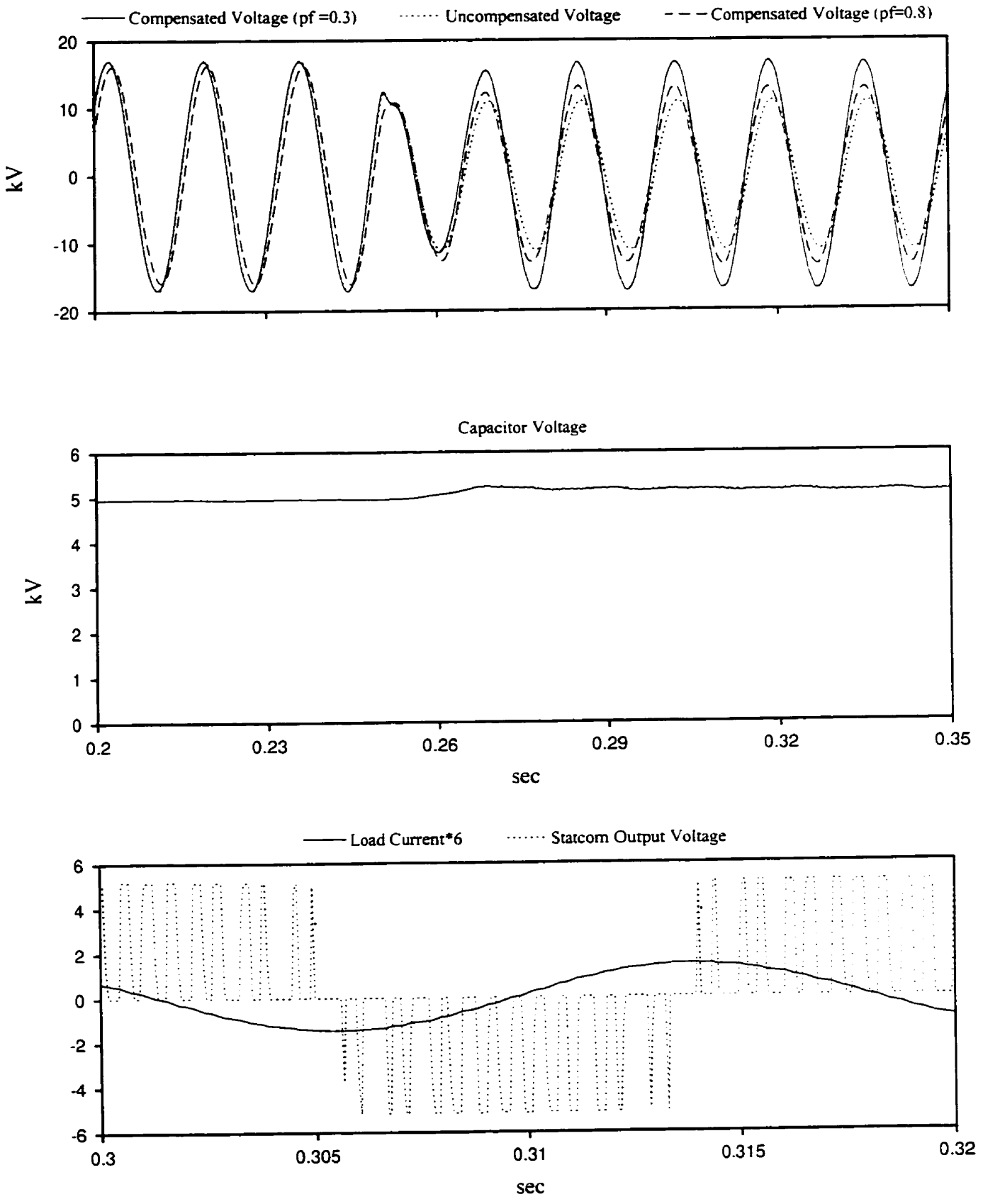


Figure 4.6 (a) : COMPENSATION BY SPFC-DVR FOR A 50% SAG

FOR DIFFERENT POWER FACTORS OF LOAD

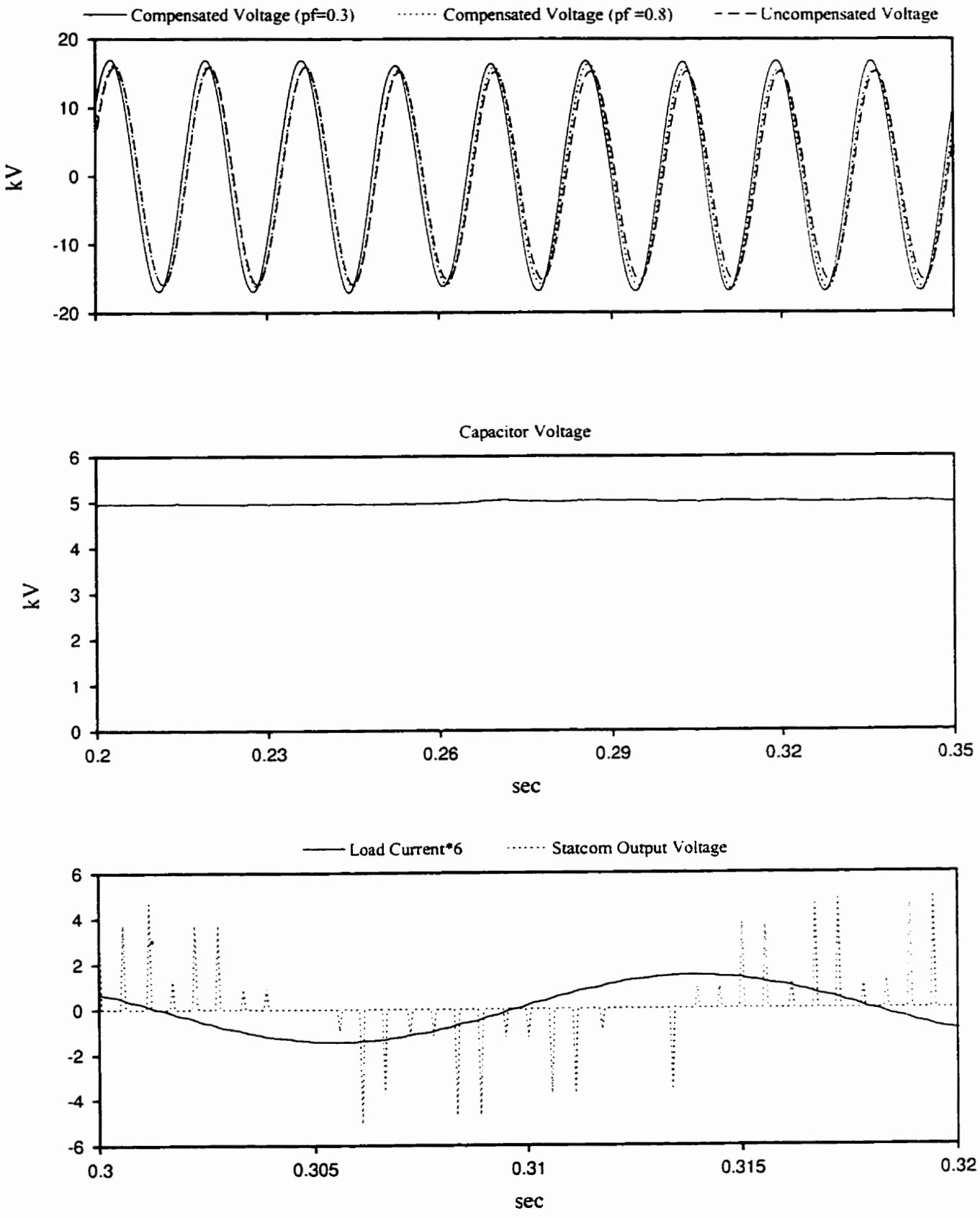


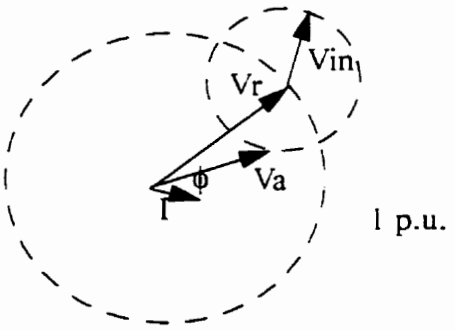
Figure 4.6 (b) : COMPENSATION BY SPFC-DVR FOR A 10% SAG

FOR DIFFERENT POWER FACTORS OF LOAD

4.4 IDEAL SAG COMPENSATION

4.4.1 Introduction:

If the vector for injected voltage Vin [Ref. Section 4.2] is not constrained to be in quadrature to the current but is allowed to be generated with any phase value, we see that we can, then, compensate for a greater sag in source voltage. Furthermore, the sag compen--sation does not depend on the power factor and the *worst* sag that can be compensated with a maximum Vin is now



$$|Va| = |Vr| - |Vin|$$

Ideal sag compensation can be achieved by assuming the reference voltage as the positive sequence component of the steady state voltage Vr ($Vr = Va_{presag}$)and synthesising Vin as the difference required to restore Vr to it's original phase and magnitude if Va undergoes a sag.

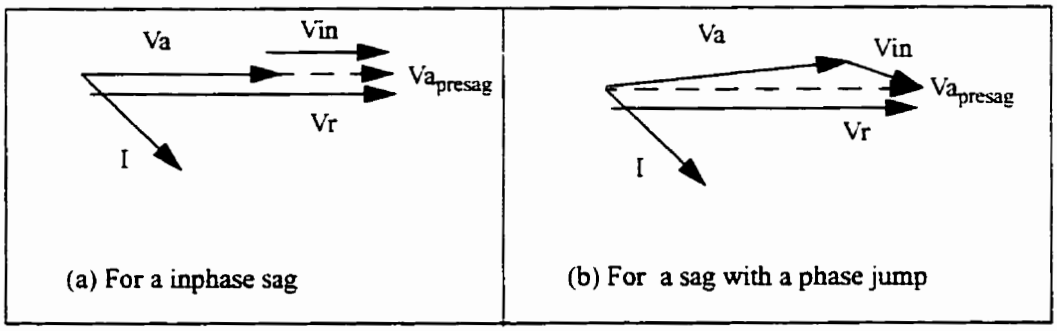


Figure 4.8: Phasor Diagrams for Ideal Sag Compensation

As can be seen in Figure 4.8, this method of sag compensation ensures that the load voltage is restored without any phase shift, for both inphase and out of phase sags.

4.4.2 Modification to the SPFC -DVR for Ideal Sag Compensation

Sag compensation, thus, requires some sort of energy exchange between the DVR and the line, depending on the amount of sag to be compensated and the amount of phase jump that can be tolerated. If the SPFC has to be used as a DVR for ideal sag compensation, it must not have the constraint of 90 degrees phase shift with the line current and it must also have a capacitor of a size large enough to store sufficient energy.

The energy stored by the capacitor could be calculated from $E = \frac{C \cdot V^2}{2}$ J, where C is the value of the capacitance and V is the voltage developed across it. The power delivered by it could be approximately calculated as the maximum energy stored divided by the total time required for complete discharge while compensating a sag. The energy level is thus determined by both the magnitude and the duration of the sag that it compensates. A higher level of sag would be compensated for a lesser duration as compared to a more shallow sag. The size of the capacitor is determined accordingly.

The dc voltage is restored by another dc source replenishing the energy lost by the capacitor. There could be a 'trickle charger' which would keep the capacitor 'topped up' to it's nominal value. Or there could be a constant source of energy drawn from the system itself, as discussed in Section 4.5 on the Shunt Fed DVR. But there is no DC voltage control loop here which will restrain the phase of the injected voltage to that which will keep the capac-

-itor charged, rather than the phase required for ideal sag compensation.

The size of the capacitor is also influenced by the amount of ripple that is to be allowed on the dc link. Any ripple here quickly appears as a harmonic on the ac side as the impedance of the transformer is too low to absorb it.

4.4.3 Controls

The modified SPFC- DVR was kept shorted out of the main circuit until it was needed. Otherwise the charged capacitor, not being used, would open circuit the secondary terminals of the series transformer and hence produce great distortions on the system side.

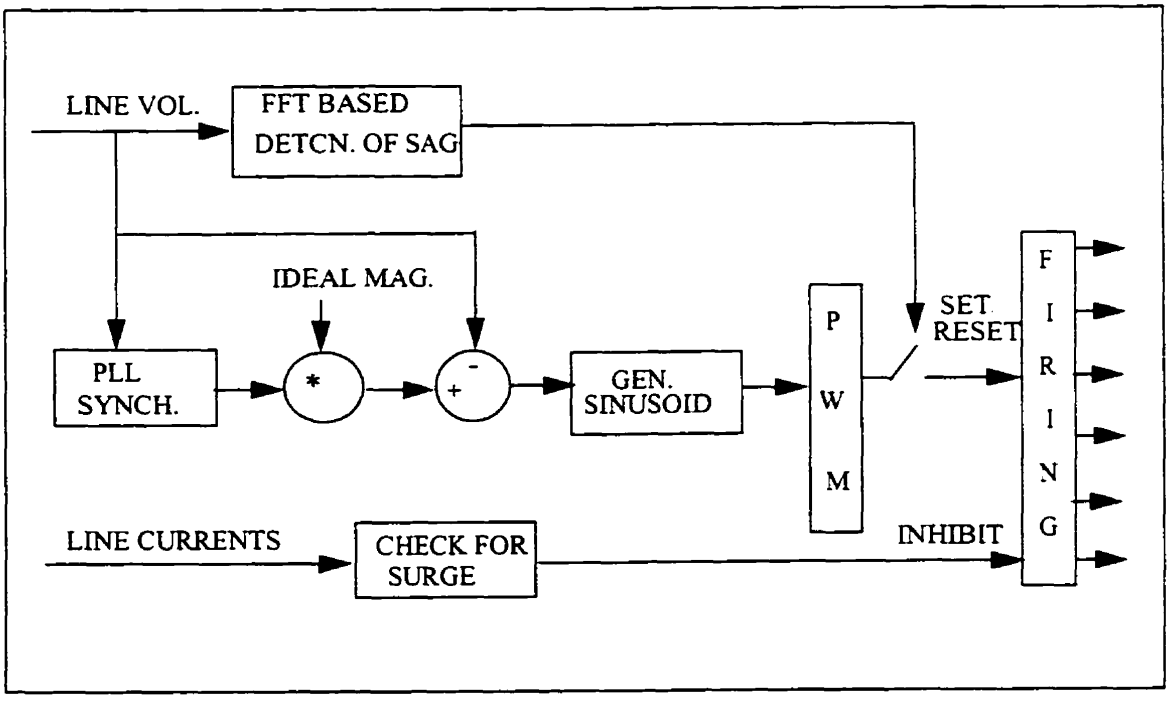


Figure 4.9: Controls for the modified SPFC DVR

Controls for the modified SPFC-DVR are different in three respects:

i.) There is no DC voltage control loop.

ii.) The DVR is switched ON only on the detection of a sag.

iii.) Firing of the STATCOM is done with respect to line voltages.

The detection method for a sag in a modified SPFC-DVR, is the same as the one employed for the Transfer Switch, where the instantaneous value of the voltage is compared with the fundamental value of a sinusoid generated using a Fast Fourier Transformation. The error signal is generated twice: for the first time a voltage dip occurs and then again when the voltage increases back to the pre-sag value.

These signals are used for Set and Reset for the modified SPFC-DVR. There is a slight delay allowed, though, to first detect if the sag is due to a surge in load current and an inhibit signal is generated.

Instantaneous compensation is achieved as the reference sinusoid for the PWM firing is continuously generated directly by the instantaneous line voltages as an error signal as shown in Figure 4.10(b).

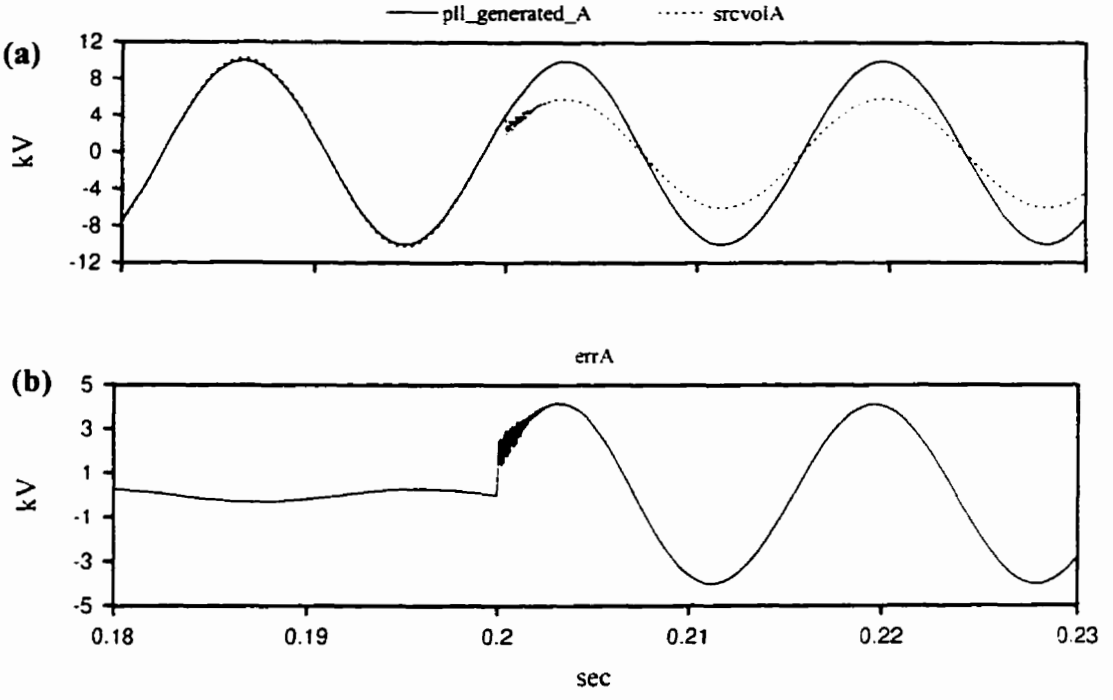


Figure 4.10: Generation of error signal for ideal sag compensation

This error signal would be the exact voltage that must be injected into the line for ideal sag compensation. Since this would be have to be generated as the line-to-line voltage by the STATCOM, while the modulating signals of the PWM generate the STATCOM *phase* voltages, a matrix transformation is used to compute the instantaneous modulating sinusoids required as

$$\begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} = \begin{bmatrix} 1 & 0 & -1 \\ -1 & 1 & 0 \\ 0 & -1 & 1 \end{bmatrix} \cdot \begin{bmatrix} Vab \\ Vbc \\ Vca \end{bmatrix}$$

which unique transformation is true if the zero sequence components is not considered. This is achieved by the delta connection of the transformer secondary windings.

Another control feature included for the modified SPFC -DVR is compensation for the drop in the capacitor voltage - since there is no DC control loop - by multiplying the index

by a factor $\frac{Vref}{Vactual}$, which is calculated from $ma_{ref} \cdot Vref = ma_{actual} \cdot Vactual$.

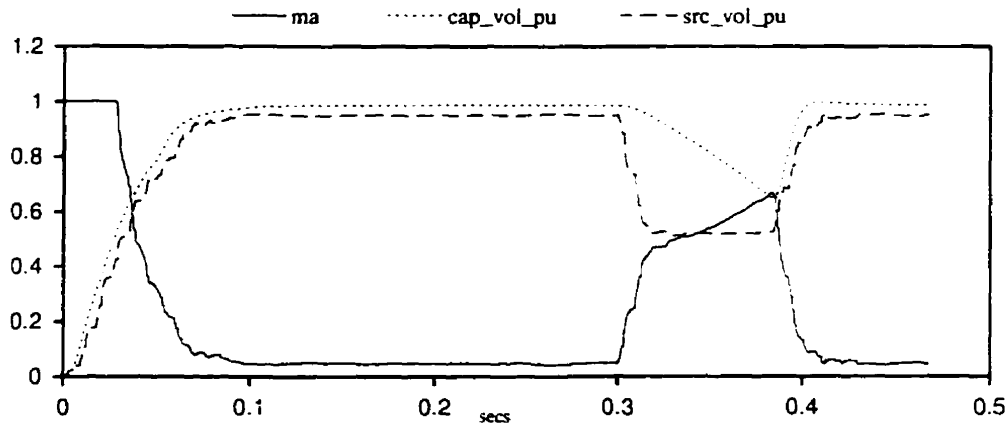


Figure 4.11: Changes in Modulation Index with changes in Capacitor Voltage.

Figure 4.11 shows how, during the sag period of 0.3 to 0.4 secs., if the capacitor voltage also drops down, the modulation index increases in comparison. This is to reduce the effect of the DC voltage droop on the output voltage of the DVR.

4.4.4 Simulations for the modified SPFC-DVR

Figure 4.12 shows the working of a modified SPFC-DVR, which is ON only on the occurrence of a sag - as was discussed in Section 4.4.3 on Controls - and which does not have a DC control loop. It can be seen that sufficient performance can be had only if the size of the capacitor is increased to 100 mF. At 1 mF, the capacitor quickly discharges and the load voltage reaches the uncompensated value. A better way to achieve ideal sag compensation without resorting to high values of capacitors is to have constant charging of the capacitor by energy drawn from the system itself, as discussed later in Section 4.5.

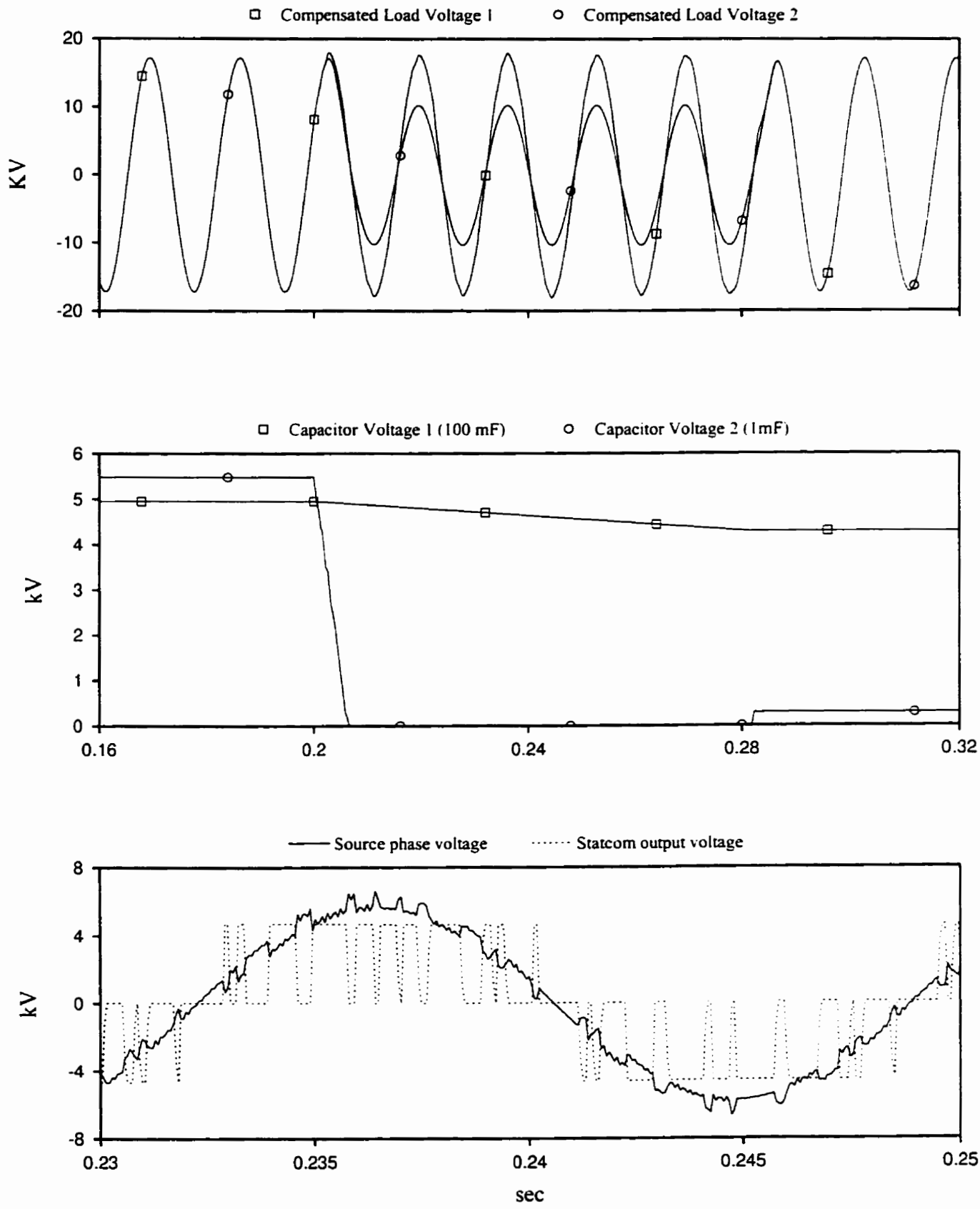


Figure 4.12 : COMPENSATION WITH A MODIFIED SPFC-DVR

FOR A 30% SAG ON A 0.788 p.f LOAD

4.5 THE SHUNT FED DYNAMIC VOLTAGE RESTORER

4.5.1 Introduction

The best way of supplying real energy to the DVR, from the point of view of performance, is by placing either a controlled or an uncontrolled shunt rectifier on the source side of the DVR. The configuration is shown in Figure 4.13. This option may be more expensive than the ones mentioned earlier, but it offers the possibility of ideal sag compensation without increasing the size of the capacitor to very large values.

An uncontrolled diode-bridge rectifier is used to draw energy from the system to keep the capacitor charged upto it's nominal value. But if the capacitor is overcharged, there cannot be any reversal of power through the diode bridge. Control of reverse power could have been achieved by a controlled bridge rectifier, as in the UPFC configurations used for higher system levels, but is not used here as it is a comparatively complex circuit.

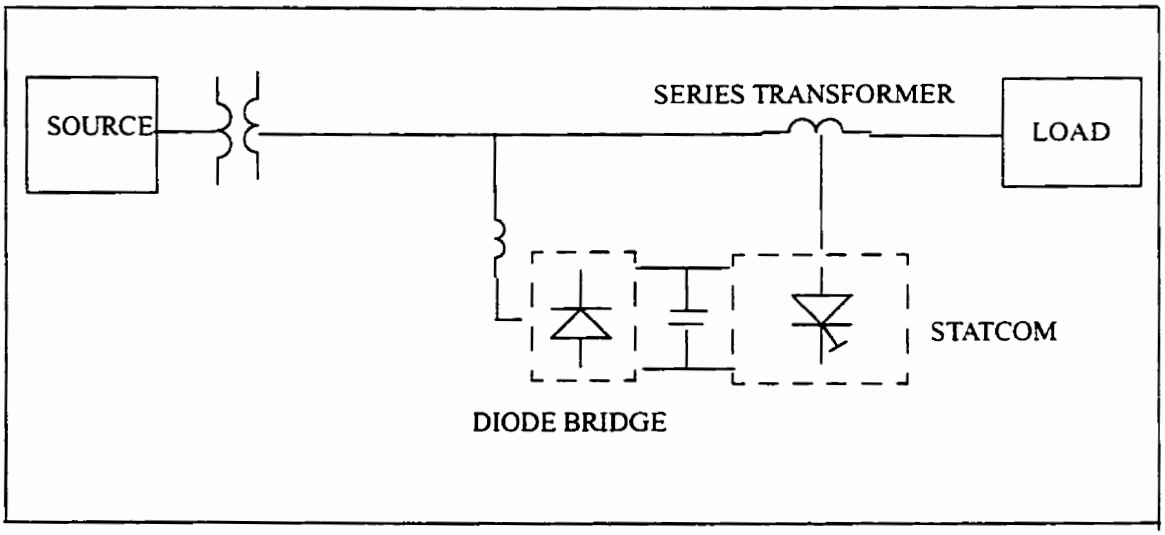


Figure 4.13: The Shunt Fed DVR

The capacitor link acts as a transient source of stored energy, while being constantly recharged by the diode bridge. The inductance associated with the diode bridge could be the leakage inductance of a transformer that is used for power balance or it could be a simple inductor.

4.5.2 The Simulated System

Simulations were performed on a 13.8 kV line with a load of approximately 12 MVA, 0.8 p.f., similar to the earlier cases. The series transformers were rated for 3 MVA each with a slight step up ratio to the line side. This ratio would depend on the maximum allowable current in the switching devices, the maximum amount of power that is required to be injected by the converter and the level of impedance of the converter as seen by the system that could be inserted without distorting the existent power flow. The leakage reactance of the transformer was kept low (0.05 p.u.) to prevent any voltage sag due to it; that of the transformer feeding the diode bridge was kept higher (0.1 p.u.) to prevent the switching harmonics from entering back into the line and to maintain a steady voltage on the capacitor.

The capacitor was of size 1 mF to increase the energy storage and to reduce the ripple on the dc link voltage. In normal circumstances, with a delta-delta shunt transformer connection the capacitor charges upto at least the peak value of the line-line voltage at the point of coupling of the diode bridge with the line, which is several times higher than the voltage

across the series transformer and can hence be used effectively to compensate for a substantial voltage sag. Of course, the level of voltage available at this point of coupling also reduced with the occurrence of a sag, but it was sufficient to compensate for most of the types of sags. In case the capacitor voltage did fall, it was not allowed to affect the magnitude of the injected voltage as, the modulation index was increased in compensation.

The DVR was kept in continuous operation, with minimum interference during normal conditions and a controlled injection of voltage during sags. It could have also continuously monitored other aspects of power quality such as harmonics[1] but this is not addressed here.

An approximate power balance analysis for the line under consideration can be made as follows

Line MVA = $\sqrt{3} * V_{l\text{-}l} * I_{max} = \sqrt{3} \times 13.8 \times 0.7 = 17.0$

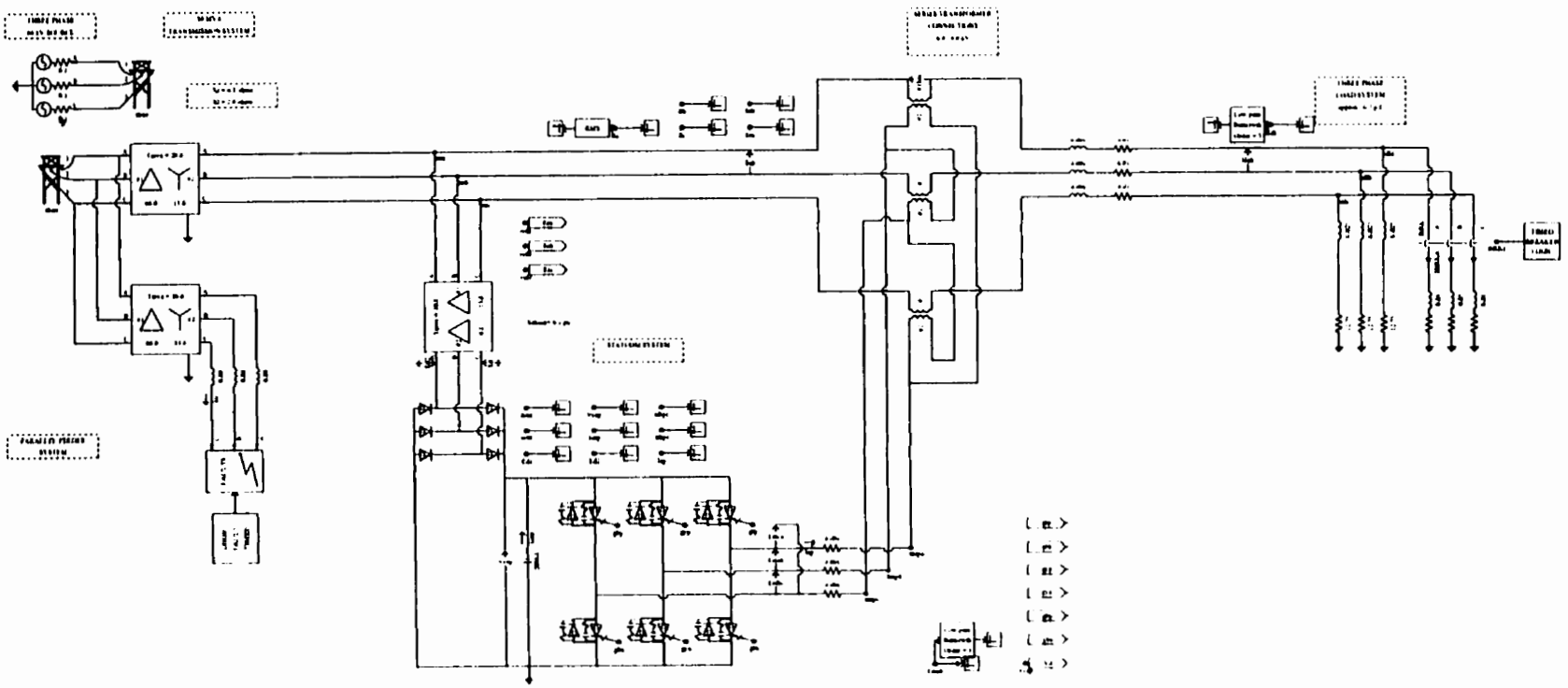
Series Injected Voltage MVA = $3 * V_{in} * n * I_{max}$

$$= 3 \times \langle \sqrt{3} \times \frac{5}{2\sqrt{2}} \rangle \times \frac{6}{4} \times 0.7 = 9.8$$

Shunt Transformer MVA = $\sqrt{3} * Vshunt * Ishunt$

$$= \sqrt{3} \times 13.8 \times 0.4 = 9.5$$

Faults were applied on a parallel 30 MVA system to produce the necessary levels of voltage sags on the primary line (Figure 4.14).



University of Manitoba, EE Dept.

THE DYNAMIC VOLTAGE RESTORER

Created:	October 14, 1993 (kurs3)
Last Modified:	September 21, 1998 (leena)
Printed On:	September 21, 1998 (leena)

Main System

Subsystem #1 of 2

4.5.3 Controls for the Shunt Fed DVR

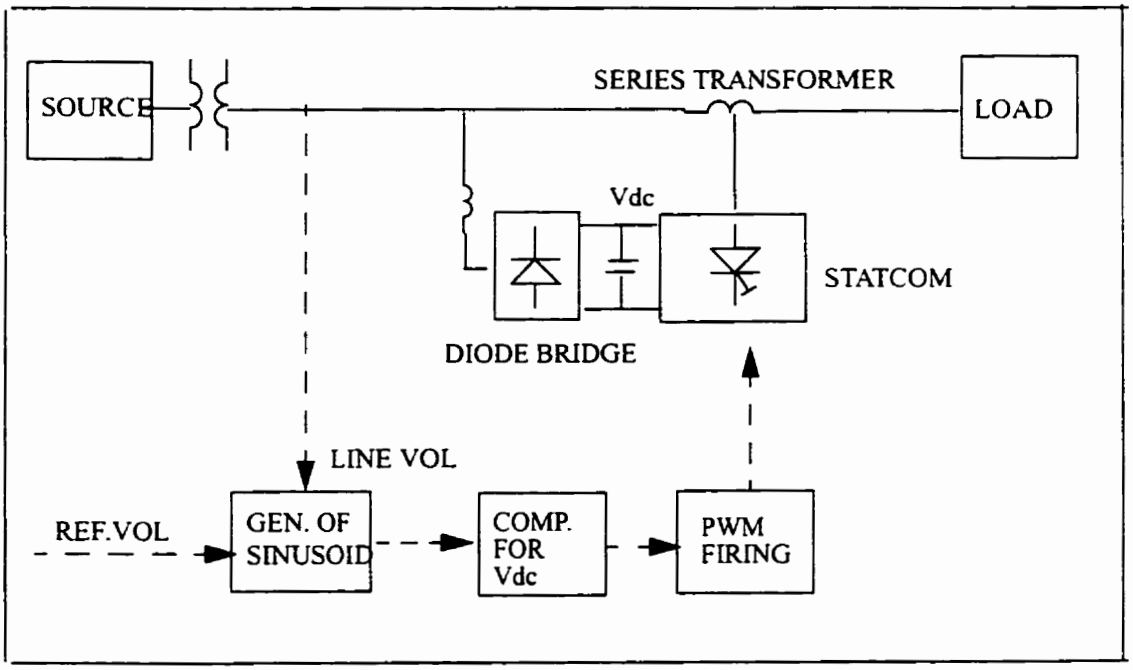


Figure 4.15: Controls for the Shunt Fed DVR

The control loops are based on the same logic as for the modified SPFC- DVR (Figure 4.9), except that the DVR is kept ON continuously to improve its speed of response.The capacitor is kept continuously charged without using a DC voltage control loop. Synchronisation is done with the line voltages for ideal sag compensation.Thus this configuration of the DVR seeks to implement the ideal features of both types of the SPFC -DVRs.

There is an expected decrease in capacitor voltage due to the sag occurring at the Point of Coupling of the diode bridge itself. This is compensated for by an increase in the modulation index.

4.6 RESULTS OF SIMULATIONS FOR THE SHUNT FED DVR

4.6.1 Compensation for Balanced Sags

The following pages (Figures 4.16 (a) and 4.16 (b)) show some results using the Shunt Fed DVR for sag compensation for balanced sags.

It can be seen that the Shunt Fed DVR injects equal voltages in phase with the phase voltages of the system. The capacitor voltage does drop down during the sag, but it is steady enough to compensate for a 30% sag for 0.8 seconds. It can be seen that the Shunt Fed type of DVR is better equipped to handle a greater range of sags for any type of a load.

There is a slight overvoltage seen on the capacitor when the system reenergises at the end of the sag. This is due to the fact that energy cannot be reversed through the diode bridge. The effect on the load voltage is reduced by compensation in the modulation index within limitations.

It can be seen that for the same rating of the series transformers and the same size of the capacitor, the shunt fed DVR offers greater flexibility and a greater level of sag compensation as compared to a SPFC -DVR, with no additional switching complexities or increase in capacitor voltage. Furthermore, the operation of the Shunt Fed DVR is not influenced by the power factor of the load.

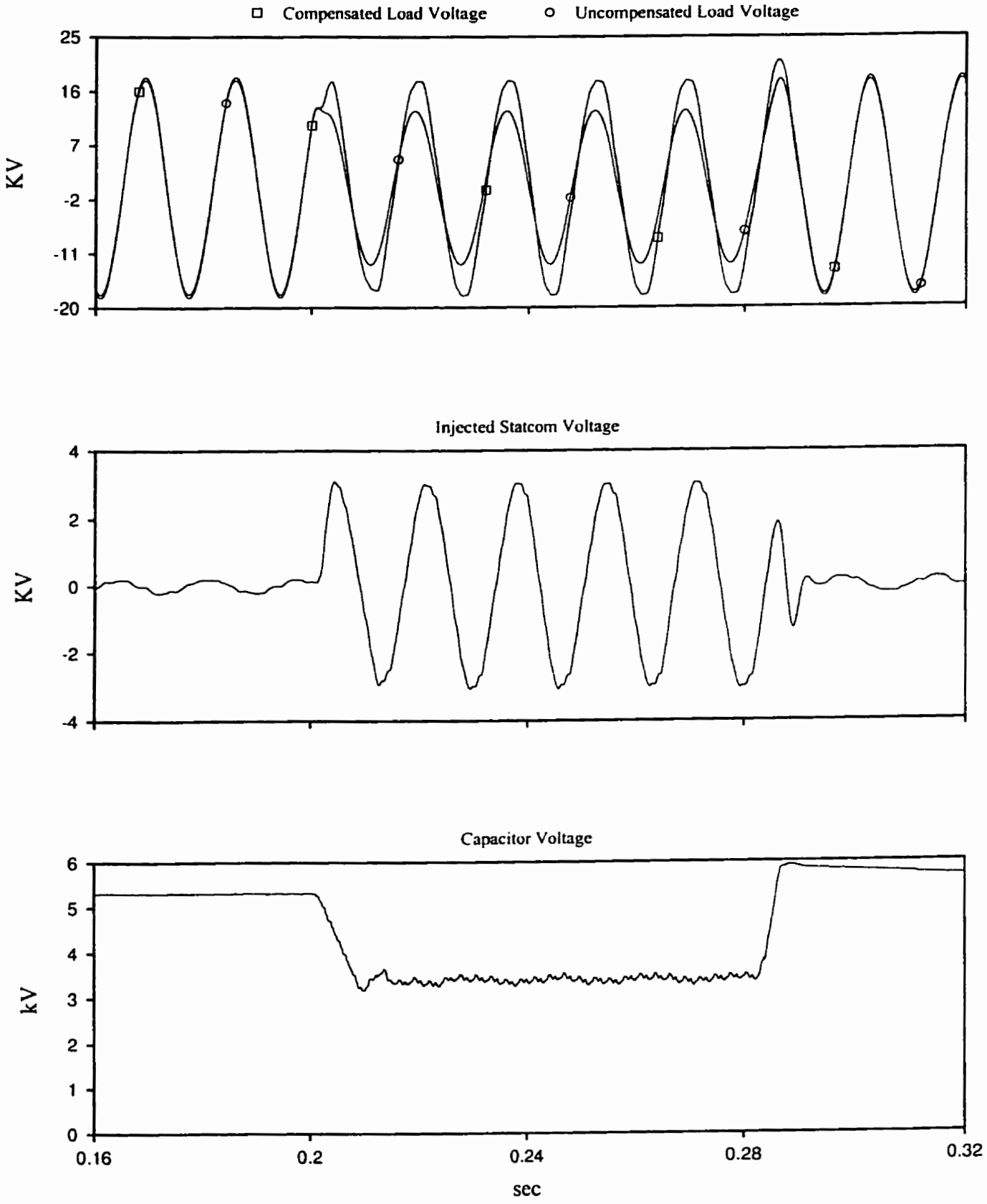


Figure 4.16 (a) : SAG COMPENSATION BY A SHUNT FED DVR

FOR A 30% SAG ON A 0.35 p.f. LOAD

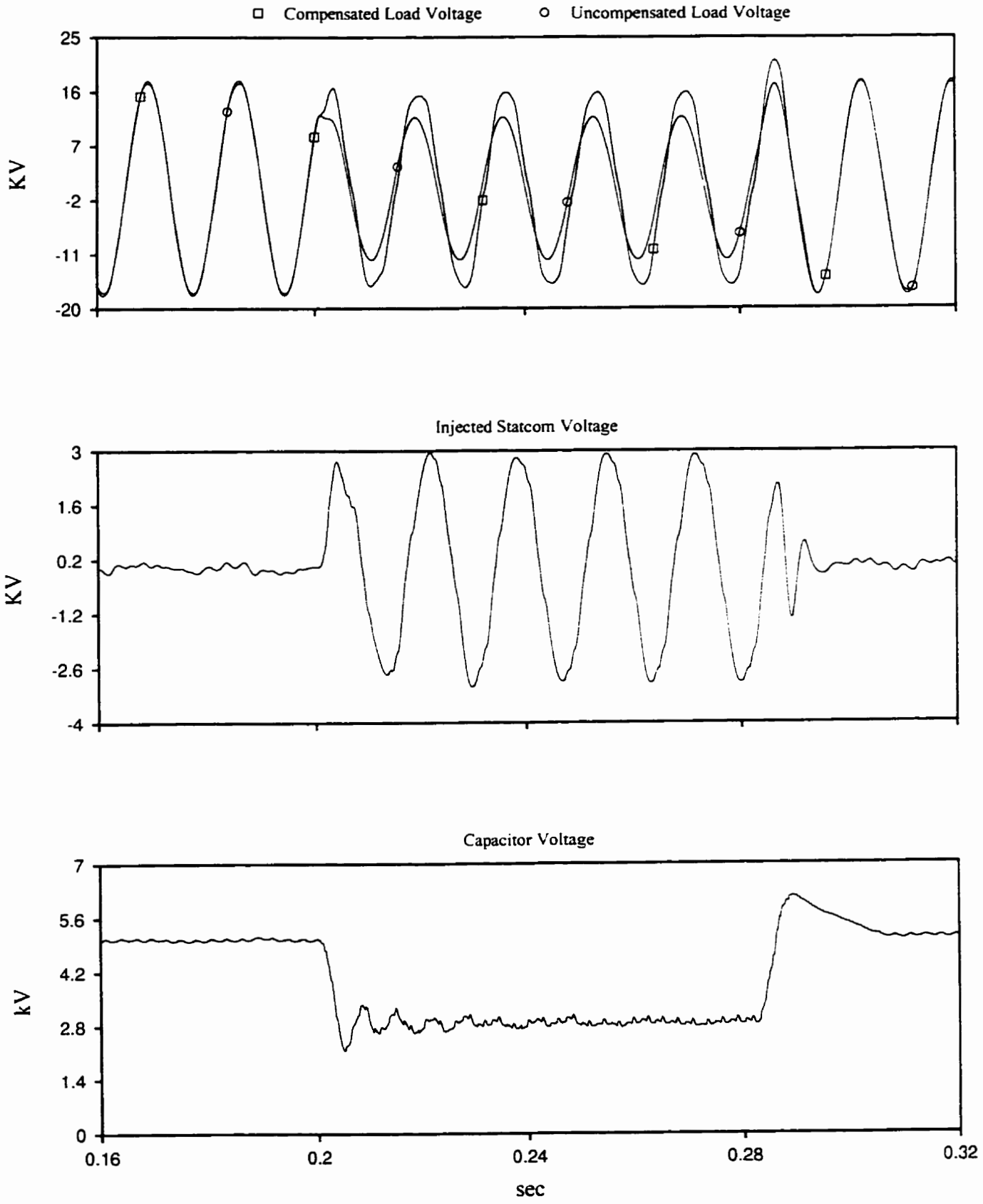


Figure 4.16 (b) : SAG COMPENSATION BY A SHUNT FED DVR

FOR A 40% SAG ON A 0.788 p.f. LOAD

4.6.2 Compensation for Unbalanced Sag

The only type of sag that had been considered till now was a balanced sag. But the fact that a Shunt Fed type of a DVR can easily supply real power to compensate for sags with no complex controls, could be exploited to generate all possible vectors of injected voltages to compensate for all types of sags, balanced or unbalanced.

Compensation of unbalanced sags is achieved by generating the fundamental positive sequence ideal voltage sinusoids in phase with the actual voltage sinusoids (as shown in Figure 4.8 (b)) and subtracting the actual voltage sinusoid to get an error signal for the PWM, which exactly compensates for the difference.

An unbalanced sag was created by applying a S-L-G fault on phase A, for which the source side voltages, the error signals generated and the load voltages are shown in Figure 4.17. As can be seen although considerable sag exists on the source side, the load voltages are reasonably constant in magnitude. A higher switching frequency for the PWM could generate more accurate compensation waveforms for better compensation.

It was found that the DVR could inject the exact voltage waveforms required for ideal sag compensation in each phase. But due to unbalanced firing the capacitor voltage showed a greater amount of ripple. This can be reduced by increasing the size of the capacitor.

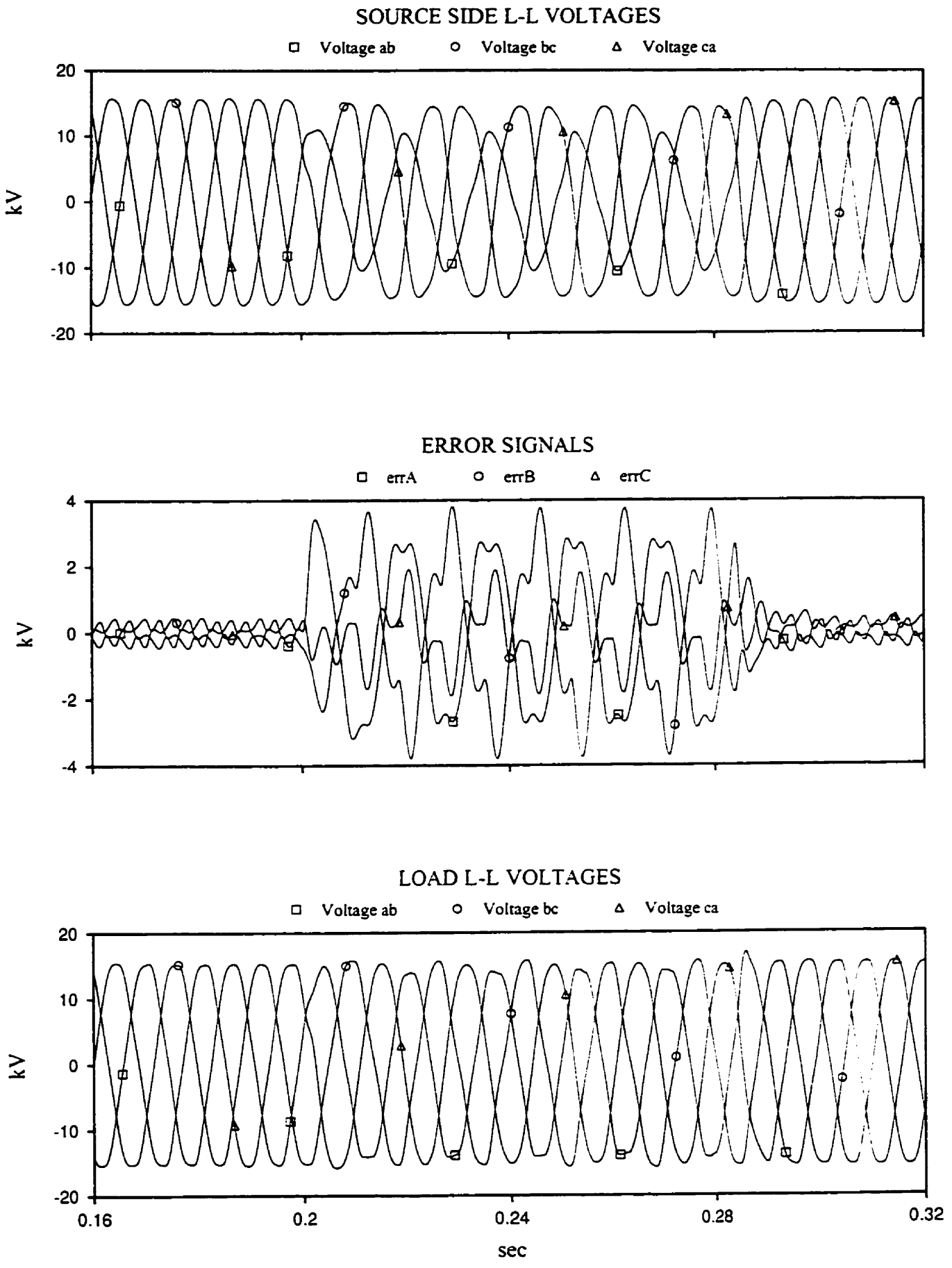


Figure 4.17 : COMPENSATION FOR AN UNBALANCED SAG

4.7 CONCLUSIONS AND FUTURE WORK

Some models incorporating series injection of voltage by a PWM-Voltage Source Inverter, for source voltage sag compensation, have been presented in this chapter.

The different topologies for the DVR were discussed; with and without energy supply to the capacitor. It is seen that a method of supplying real energy is imperative to complete compensation of voltage sags and that the Shunt Fed DVR is able to handle arbitrary sags more efficiently. Limits on the amount of sags that can be handled by a purely reactive type of DVR were also presented. Control strategies, with and without a dc control loop, were examined and found to work adequately for sag compensation.

Further work would involve a detailed study for load side variations. Also, designs could be studied for low level voltages using small inductors instead of transformers or even eliminating them entirely.

CONCLUSIONS FOR THE THESIS

The aim of this thesis was to explore the issues applicable to the operation of various Custom Power topologies and to subsequently develop adequate control strategies. The models for these topologies were prepared on an electromagnetic transients program and the developed control concepts were thoroughly verified.

The models included

a) The Static Transfer Switch

b) The Fault Current Limiter

c) The Series Power Flow Controller

d) The Series Voltage Regulator

e) The Dynamic Voltage Restorer

The important requirements for the Transfer Switch were rapid detection of a voltage sag for transferring between feeders with minimum overcurrents, without introducing excessive voltage distortion at the customer's bus. The FFT based undervoltage detection scheme was developed and proved to be effective. Demonstrations were also made, using the EMTDC model, for the advantages of a Make before Break type of transfer with thyristors and the effects on non -linear loads such as induction motors.

A GTO based Fault Current Limiter was also developed and it was shown that it allows rapid current interruption, analogous to a fuse. It was also shown that through the use of phase-control on a pair of back to back thyristors, the rating of the shunt reactor could be reduced and a good current regulation was possible. Control strategies for near- instantaneous detection of a fault current and for automatic reclosing options for a transient fault current were also developed.

Next, the Series Voltage Source Inverter based devices were studied. The power circuit and the control strategy for a Series Power Flow Controller, conventionally used for power modulation, were developed. It was further shown that this device can effectively perform reactive compensation for voltage regulation in distribution systems and further for voltage sag compensation. Limits on its operating range as a voltage sag compensator were established using theoretical analysis. Based on this the required control algorithm was developed and tested.

The most effective option, although it may be potentially expensive for dynamic voltage restoration, was found to be the Shunt Fed DVR. It proved to be more effective in handling arbitrary balanced or unbalanced sags, for a range of loads. A control algorithm for ideal sag compensation, using real and reactive power compensation, was developed for this device and was demonstrated to perform complete sag compensation successfully.

Future work in each type of device would include additional rigorous studies for application and economic justification in any particular system, testing of controls for greater variations in loads and system side parameters and comparison with different designs, if necessary.

Models for Active Filters have already been developed by the University of Manitoba Power Engineering group earlier and hence not included in this thesis.

Current work is being done to model the remaining topology, the D-STATCON for flicker control, which is also not included in this thesis.

These topologies now constitute a library of Custom Power models in the PSCAD / EMTDC™ simulation programme and can be used for any distribution system studies.

REFERENCES

1. G. A.Taylor, W. J. Laycock, N. H.Woodley, "A Total Solution Package : Custom Power" ERA Technology Conference, U. K. , January 1995.

2. Ned Mohan etal ; POWER ELECTRONICS : Converters, Applications and Design.

3. PSCAD / EMTDC^{TM} Users manual ; Manitoba HVDC Centre.

4. IEEE Std. 1250 -1995 Guide for Service to Equipment Sensitive to Momentary Voltage Disturbances.

5. IEEE Std. 141 -1986 Recommended Practice for Electric Distribution for Industrial Plants.

6. R. C. Settembrini etal, "Reliabilty and Quality Comparisons of Electric Power Distribution Systems." 1991

7. IEEE Std. 1159 -1995 Recommended Practice for Monitoring Electric Power Quality.

8. "Proposed Chapter 9 for Prediciting Voltage sags in Revision to IEEE Std. 493, the Gold Book" IEEE T&D Conference 1994.

9. IEEE Std. 242 - 1975 Estimated Clearing Time of Protective Devices.

10. Schwartzenberg, J.W.; De Donecker, R.W. "A 15kV Medium Voltage Transfer Switch." Proceedings of the IEEE IAS Annual Meetting, 1995.

11. Harshad Mehta, Le Tang et al, " Distribution System Voltage Sags : Interaction with Motor and Drive Loads." IEEE T & D Conference 1994.

12. N.Woodley,M. Sarkozi et al, " Solid Sate 13 -kV Distribution Class Circuit Breaker:Planning, Development and Demonstration" Trends in Distribution Switchgear Conference Proceedings, November 1994.

13. Alex Wu,Yuexin Yin, " Fault Current Limiters in Medium and High Voltage Power Systems." IEEE Transactions on Industrial Applications , Jan/Feb 1998.

14. P.Barkan, "The Current Diverting FCL-A Practical Solution to Fault Current Limiting"IEEE Transactions on Power Apparatus and Systems,Vol. PAS-99,March/April 1980.

15. S. L.Williams, R. J. Nelson, "Transmission Series Power Flow Control" IEEE Transactions on Power Delivery, January1995.

16. Pedro Barbosa, Edson Watanabe, "Series Connection of PWM-VSI for Reactive Power Compensation of Transmission Lines" 1996

17. L. Gyugyi, C. Schauder, K. Sen, "Static Synchronous Series Compensator : A Solid State Approach to the Series Compensation of Transmission Lines." IEEE / PES Winter Meeting, 1996.

18. X.Wang, S. Dai, B. Ooi, "A Series Capacitive Reactance Compensator Based on VSI-PWM Inverter." IEEE Transactions on Power Delivery, April1992.

19. Kevin Chan, Alexandra Kara, "Technical and Performance Aspects of a DVR." ABB.

20. N. H. Woodley, " Topologies of Custom Power Technologies for Voltage Support." Westinghouse Power Generation.

21. D. L. Hornak, D.W. Zipse, "Automated Bus Transfer Control for Critical Industrial Processes." Industrial and Commercial Power Systems Annual Technical Conference, 1990.

22. R. A. Barr, D. Platt, "Use of Saturating Choke in a Series Capacitor Compensation of Distribution Systems." Proceedings of the Generation, Transmission and Distribution Conference, January 1997.

Appendix A
COMPARISON OF SERIES POWER FLOW CONTROLLERS

Consider a 100 km lossless line with stiff voltage sources of 100 kV at sending and receiving ends, at a steady load angle of δ degrees. The impendance of the line is Z = j0.05 p.u. on a Pbase of 100 MVA.

Comparing the series power flow controllers for the same maximum series voltage insertion (say, 0.25 pu)

1. The normal power flow is given by

$\delta \quad 0, 1 .. 180$

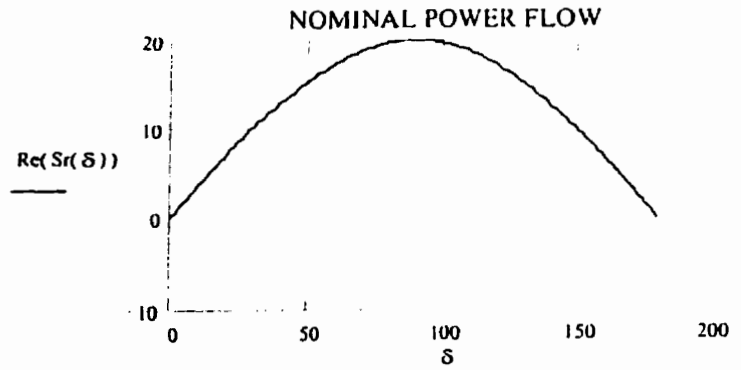
$Vs \quad 1 \cdot e^{i \cdot 0 \cdot deg} \quad pu$

$Vr(\delta) \quad 1 \cdot e^{i \cdot (-\delta) \cdot deg} \quad pu$

$Z \quad i \cdot 0.05 \quad pu$

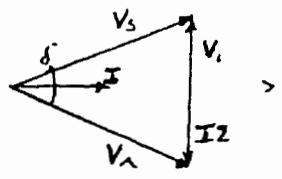
$Ir(\delta) \quad \frac{Vs - Vr(\delta)}{Z}$

$Sr(\delta) \quad Vr(\delta) \cdot \overline{Ir(\delta)}$



2. If a series voltage Vi is now injected in quadrature with the line current, we know that it would then be injected in a line parallel to Vs-Vr, since the line is completely inductive.

Vi could be inserted in either direction.
Let the maximum magnitude of Vi be 0.25 pu



$K \quad 0.25$

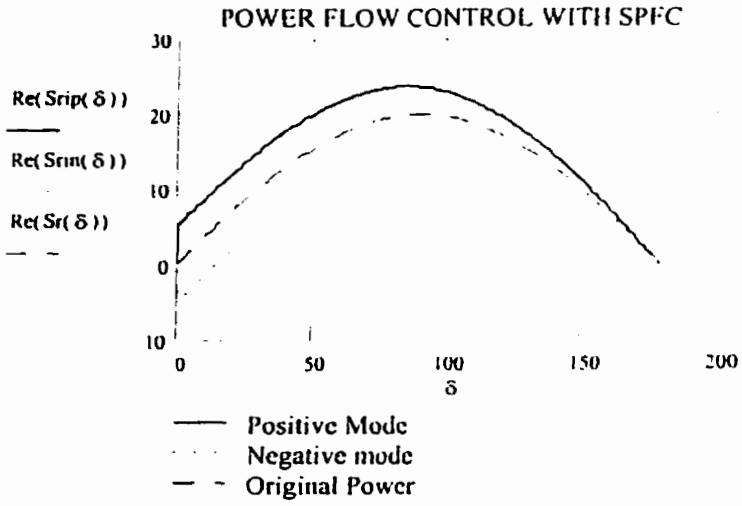
$$Vip(\delta) := \frac{K \cdot (Vs - Vr(\delta))}{|Vs - Vr(\delta)|} \qquad Vin(\delta) := K \cdot \frac{(Vs - Vr(\delta))}{|Vs - Vr(\delta)|}$$

$$Irip(\delta) := \frac{Vs + Vip(\delta) - Vr(\delta)}{Z} \qquad Irin(\delta) := \frac{Vs + Vin(\delta) - Vr(\delta)}{Z}$$

and power

$$Srip(\delta) := Vr(\delta) \cdot Irip(\delta)^{*} \qquad Srin(\delta) := Vr(\delta) \cdot Irin(\delta)^{*}$$

This is the increase in real power that can be obtained by a SPFC series injected voltage at it's rated value. At any operating point the increase could be either positive or negative, by capacitive or inductive compensation.

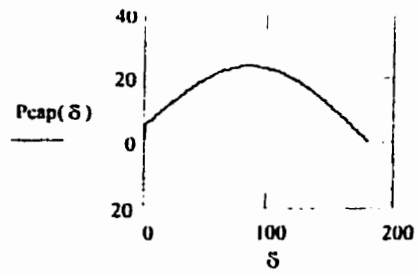


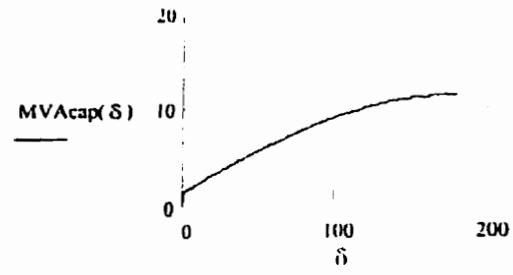
3. The power flow improvement with a thyristor controlled series capacitor can also be calculated for a maximum series injected voltage of 0.25 pu, assuming we have no limitation on the MVA rating of the capacitor, although in reality we would be limited by the MVA rating.

For a maximum voltage injection of 0.25 pu, it being in quadrature to the line current

for which the variations required in MVA

$$Pcap(\delta) := Re(Srip(\delta)) \qquad MVAcap(\delta) := |Vip(\delta) \cdot Irip(\delta)|$$



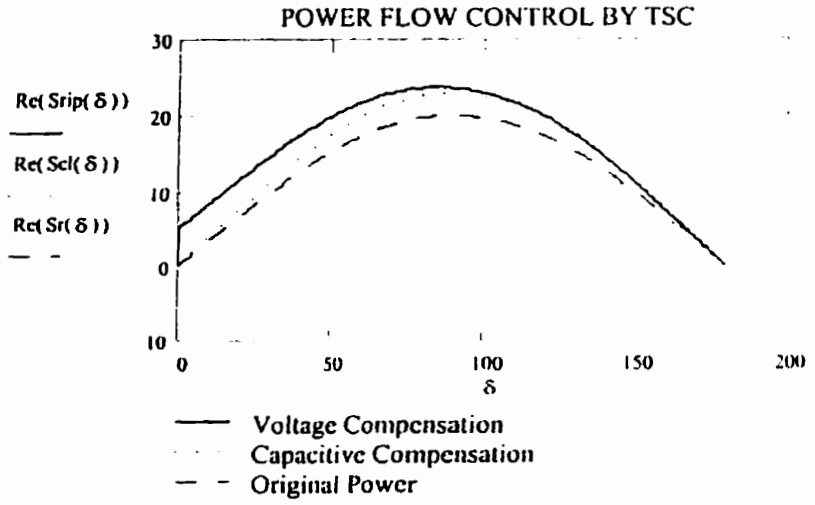


If this MVA is fixed, the range of direct capacitive compensation is further limited.
Let the maximum MVA of the capacitor be 10 pu or 1000 MVA.
Then we have

$$Xcc = \frac{0.25^2}{10}$$

$$Icl(\delta) = \frac{Vs - Vr(\delta)}{Z_i \cdot Xcc}$$

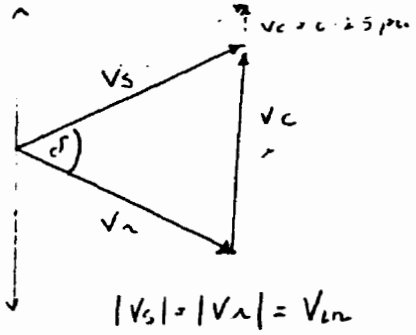
$$Scl(\delta) = Vr(\delta) \cdot Icl(\delta)$$



Thus there is a difference in the compensation characteristic, if it is in capacitive reactance mode (limitation on Xc) or in voltage insertion mode (limitation on Vi). With a voltage insertion mode, which is not dependent on the load current, we can see that there is a possibilty of increasing power flow even at zero load angle.

4. To calculate improvement in power flow using a phase angle regulator (PAR),

We know that the voltage required for full shift at is
Vc = 2 Vln sin δ/2
=0.518 pu
Since Vc here can be 0.25 pu at the maximum
the corresponding apparent movement in δ is
from δ+14.36 to δ-14.36
and the rise in line voltage is approximately 0.03 pu
or



$$Ir1PAR(\delta) := \frac{(1.03 \cdot Vs - Vr(\delta + 14.36))}{Z + i \cdot 0.002}$$

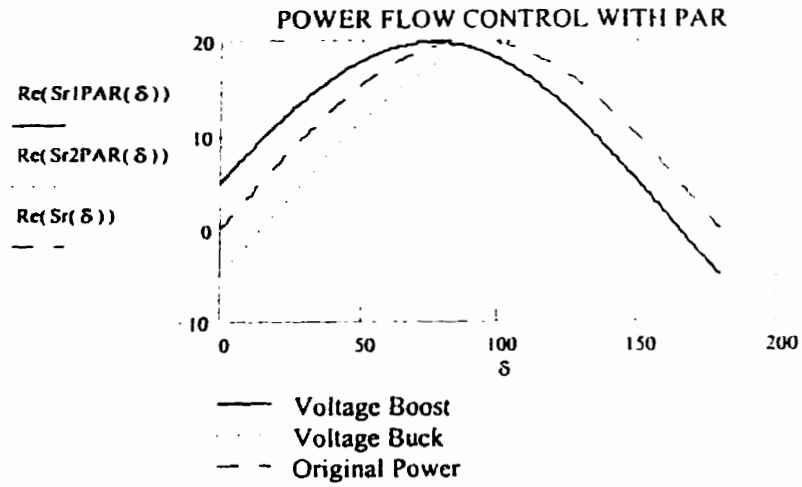
$$Ir2PAR(\delta) := \frac{(1.03 \cdot Vs - Vr(\delta - 14.36))}{Z + 0.002 \cdot i}$$

.....where 0.002 pu is the additional reactance due to the transformers

and hence the power

$$Sr1PAR(\delta) := Vr(\delta + 14.36) \cdot Ir1PAR(\delta)$$

$$Sr2PAR(\delta) := Vr(\delta - 14.36) \cdot Ir2PAR(\delta)$$



5. Finally, to compare the various Series Power Flow Controllers,at a specific load angle of 30 degrees

Calculations for the SPFC and TSC

$$Vin := 0.25, 0.24 .. 0.25$$

$$Vspfc(Vin) := \frac{Vin \cdot (Vs - Vr(30))}{|Vs - Vr(30)|}$$

$$Ispfc(Vin) := \frac{Vs + Vspfc(Vin) - Vr(30)}{Z}$$

$$Spfc(Vin) := Vr(30) \cdot Ispfc(Vin)$$

$$Cap(Vin) := Vr(30) \cdot Ispfc(|Vin|)$$

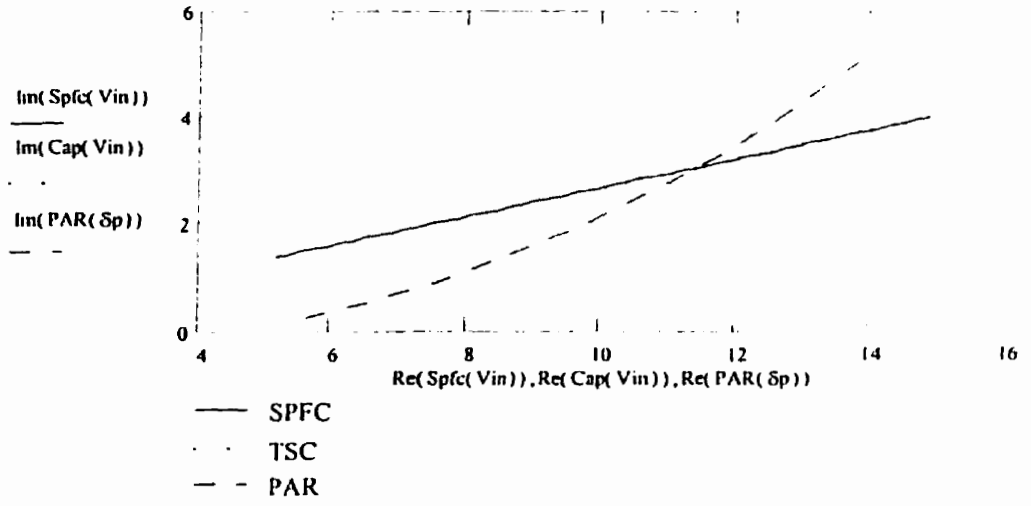
Calculations for the PAR

$$\delta p := 30 + 14.36, 30 + 13.36 .. 30 - 14.36$$

$$Ipar(\delta p) := \frac{1.03 \cdot Vs - Vr(\delta p)}{Z + 0.002 \cdot i}$$

$$PAR(\delta p) := Vr(\delta p) \cdot Ipar(\delta p)$$

Hence the various series power flow controllers can be compared as

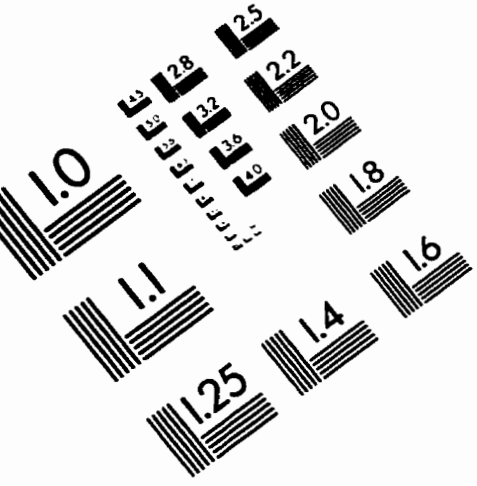


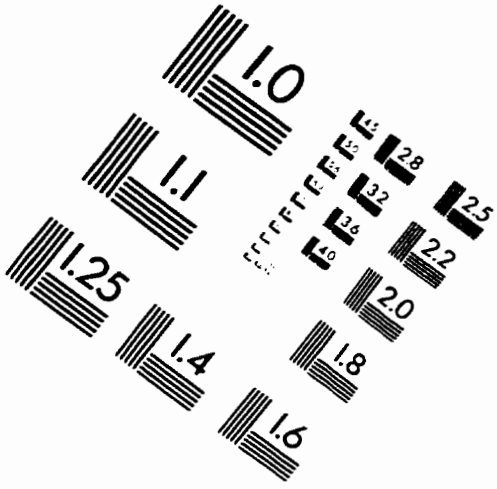
The SPFC is seen to be capable of power flow control on either side of nominal power flow point, like that of a PAR.

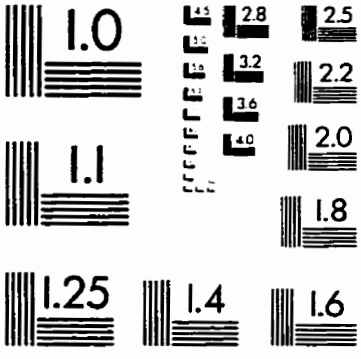
The TSC or Variable Capacitor is governed by constant voltage characteristics and hence it shows exactly the behaviour of SPFC, except that it is in the capacitive region only. If the characteristics were governed by constant Xc, they would be further limited.

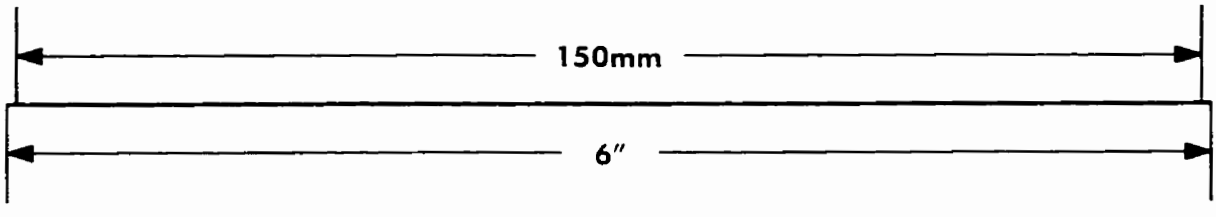
Note : For a smaller load angle and assuming the line to be totally inductive, the characteristics would further converge.

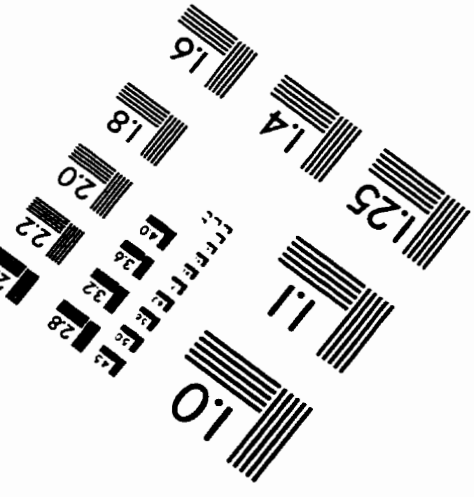
IMAGE EVALUATION
TEST TARGET (QA-3)

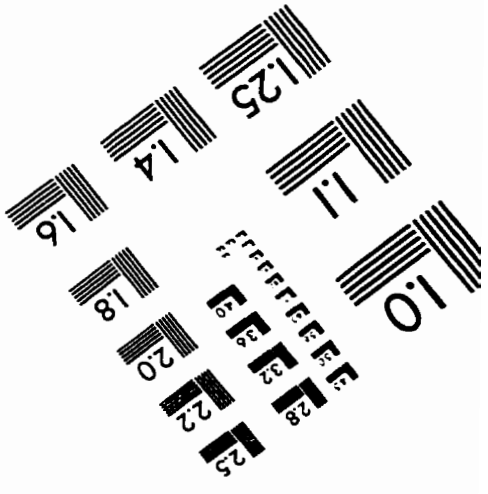












APPLIED IMAGE, Inc
1653 East Main Street
Rochester, NY 14609 USA
Phone: 716/482-0300
Fax: 716/288-5989